A 0.4-V Supply Curvature Corrected Reference Generator with 84.5-ppm/°C Average Temperature Coefficient within -40 to 130°C

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***Abstract*—This paper describes a low power current-mode voltage reference based on subthreshold transistors. A novel circuit configuration together with a high order temperature compensation scheme allow this voltage reference to operate with a supply voltage down to 0.4 V over a large temperature range (from -40 to 130°C). The circuit, fabricated with a standard 0.18-μm CMOS technology, provides an output voltage of 212 mV while consuming 192 nW. The measured average temperature coefficient (TC) is 84.5 ppm/°C.**

***Keywords*—Voltage reference, curvature correction, ultra-low voltage.**

I. Introduction

THE Internet of Things (IoT) is the network of physical objects that can be monitored and controlled through the internet. IoT is already a reality and it is growing rapidly. Portable and nomadic devices are pushing forward urgently the need of low voltage and nanoWatt-power integrated circuits. In such a scenario, sub-threshold circuits are becoming increasingly popular thanks to the offered power saving. In addition, sub-threshold operation allows the supply voltage scaling. However, devices biased in sub-threshold region are more sensitive to process variability and temperature variations. The challenge for the designers is, hence, to develop and apply suitable compensation techniques.

Voltage reference generators are key circuits in the above mentioned applications, as the generation of a DC voltage insensitive to temperature, supply voltage and process variations is an unavoidable need. Traditional bandgap voltage references (BGRs), which can be implemented using standard CMOS technologies exploiting parasitic vertical BJT devices, generate an output voltage, in first approximation almost independent from the temperature, of about 1.2 V. These circuits need a higher supply voltage, which makes them not suitable for meeting the low voltage constraint in low power applications. However, by means of resistive subdivision methods, this limit can be overcome for reference circuits utilizing the BGR principle and achieving sub-1V operation, [1], [2]. In order to achieve low power consumption while exploiting the BGR principle, often forward-biased pn-junctions are substituted with MOS transistors biased in sub-threshold region, [3], [4]. Other types of voltage references, implemented in standard CMOS technologies, are based on a weighted difference of the gate-source voltages of two MOS transistors working in saturation region, [5], or on temperature compensation techniques that exploit the different characteristics of MOS transistors in saturation and in sub-threshold, [6]–[8]. In order to scale down the supply voltage, sampled data systems and switched-capacitors implementations have been reported as well, [9]–[11].

Demanding requirements for analog blocks working with sub 1-V supply voltage and very low power should be satisfied by new circuit solutions using standard technologies. This work focuses on the design of a voltage reference generator based on the current-mode temperature compensation technique, [1], with PMOS transistors in deep sub-threshold region. The circuit has been fabricated in a conventional 0.18-μm CMOS technology without resorting to any special or additional process step. This design operates with a supply voltage down to 0.4 V and consumes 192 nW. The circuit uses a second order non-linearity compensation and generates a regulated voltage with an average TC of 84.5 ppm/°C in a very wide temperature interval ranging from -40 to 130°C. In this range, the maximum threshold voltage values of the available MOS transistors are about 0.4 V and -0.45 V for NMOS and PMOS devices, respectively.

This paper is organized as follows: the following Section describes in details the operating principle of the proposed voltage reference, its architecture and circuit implementation. Section III shows the measurements results and compare them with low power and low voltage competitors within the open literature. Finally, Section IV draws the conclusion.

II. Circuit Description

A. Topological modifications

The used schematic is a suitable transformation of the well-known band-gap concept, reminded in Fig. 1(a). The equal currents in the two branches generate a proportional to absolute temperature (PTAT) and a complementary to absolute temperature (CTAT) voltage. A proper weighted addition of these two terms equalizes positive and negative temperature dependencies and gives rise to the reference voltage, V_{REF}.

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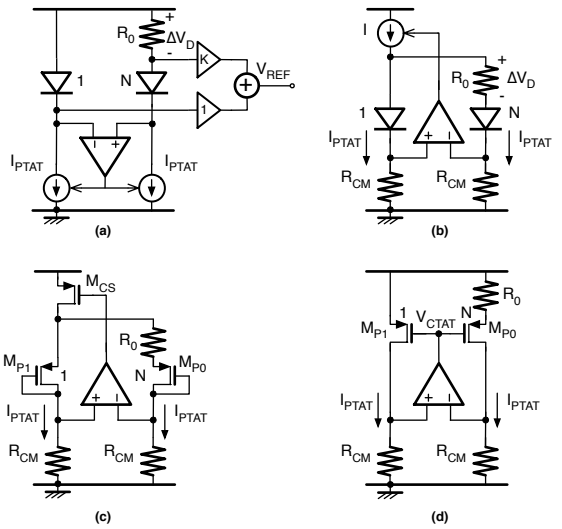

Fig. 1. Conceptual schemes and topological modifications leading to the proposed reference generator.

Fig. 1(b) depicts a topological variation of the basic scheme using current-mode operation to generate the PTAT current. Its simplified transistor level implementation is shown in Fig. 1(c). The feedback loop equates the two branch currents by equating the drop voltages on the nominally identical resistors R_{CM}. The two branch currents are PTAT and $I_{PTAT} = \Delta V_D/R_0$ holds. The implementation shown in Fig. 1(d) utilizes the same technique while eliminating the extra V_{DS} requirement of the current source in Fig. 1(c). Moreover, the circuit can operate at very low supply voltage since the voltage headroom required for the PMOS transistors is reduced from a V_{GS} to a V_{DS}. The drop voltage on R_{CM} can be at the lower limit established by the gain of the op-amp and the required differential sensitivity. With transistors in sub-threshold, V_{DS} can be few tens of mV and V_{GS} can be in the order of one to two hundreds of mV range. Another limit to the supply voltage comes from the amplifier. The scheme of Fig. 1(d) facilitates its design because the input common mode is very low and the required output is about half of the supply voltage. In addition, the circuit of Fig. 1(d) generates a CTAT voltage between source and gate of M_{P1} while the PTAT current flows in the two branches. Notice that in the scheme of Fig. 1(d), in order to generate a temperature compensated current, it is necessary to transform V_{GSP1} into a current.

The design of the circuit of Fig. 1(d) starts choosing the drop voltage across R_0. A suitable value is few tens of mV. A second element is the drop voltage across resistors R_{CM} that, for limiting the feedback loop gain to feasible values, must be a non-negligible fraction of the supply voltage. In this design, it is chosen around 100 mV. For a low power operation, I_{PTAT} should be few tens of nA. As a consequence, the resistors values become in the order of MΩs. During the optimization of the circuit device sizes, the trade-off between power and area has been considered while trying to achieve competitive TC performance.

B. Circuit implementation

Fig. 2 shows the core schematic diagram of this solution. The amplifier obtains a large gain thanks to a folded cascode scheme with p-channel input transistors and a second stage with resistive load R_1. The folded cascode amplifier (generation of voltages V_{b0}, V_{b1}, and V_{b2} not shown for the sake of simplicity) has 46-dB DC simulated gain (A_1) while consuming 55 nA. A scaled replica of the PTAT current of the core biases the folded cascode amplifier. By inspection of the circuit, the gain of the second amplifier stage is

$$|A_2| = g_{m,N0}R_1 = \frac{I_{CTAT}}{\eta V_T}R_1 = \frac{|V_{GSP1}|}{\eta V_T} \quad (1)$$

where η is the sub-threshold slope parameter. A current unbalance, ΔI_{in}, between M_{P0} and M_{P1} gives rise to a voltage signal at the input of the folded cascode equal to $\Delta V_{in} = \Delta I_{in}R_{CM}$. Going around the loop, the feedback loop gain is

$$|A_I| = |A_1|\frac{|V_{GSP1}|}{\eta V_T}\frac{I_{PTAT}}{\eta V_T}R_{CM} = |A_1|\frac{|V_{GSP1}|V_{CM0,1}}{(\eta V_T)^2} \quad (2)$$

Notice that the positive feedback loop gain is ignored due to the large source degeneration resistor R_0. Since A_1 is about 200, $|V_{GSP1}|/\eta V_T$ about 4, and V_{CM} about 100 mV, the current loop gain is approximately equal to 1600, enough for a suitable loop control.

In this design, the transistors are sized to obtain 0.2-V sub-threshold V_{GS} and 0.1-V saturation voltage, V_{sat}, at the nominal operating point. Since the drop voltage across the resistors R_{CM} of Fig. 2 is 0.1 V, this allows $V_{sat,MPa3}+V_{GS,in} \approx 0.3$ V for 0.4-V supply voltage. The internally generated bias voltages of $M_{Na4} - M_{Na7}$ and $M_{Pa5} - M_{Pa7}$ ensure 0.1-V V_{DS} drop across each transistor. Therefore, the nominal supply voltage is as low as 0.4 V. The second stage generates about 0.2 V at its output and operates properly with the supply of 0.4 V.

Since the drop voltage across the resistor R_1 is V_{GSP1}, the current that flows into M_{N0} is the CTAT current required for the first order temperature compensation. This current, mirrored by $M_{N0} - M_{N1}$ and $M_{P3} - M_{P4}$, flows into R_{OUT}. The PTAT component flowing into R_{OUT} is a replica of the current in M_{P0} and M_{P1}. A proper choice of N (for this design 16) and of the current mirrors sizing provide the temperature compensation.

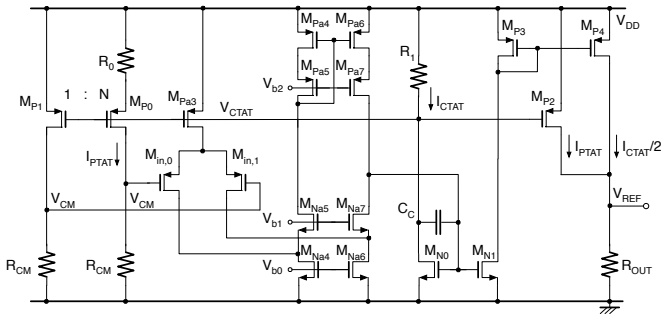

Fig. 2. Schematic diagram of the reference generator core.

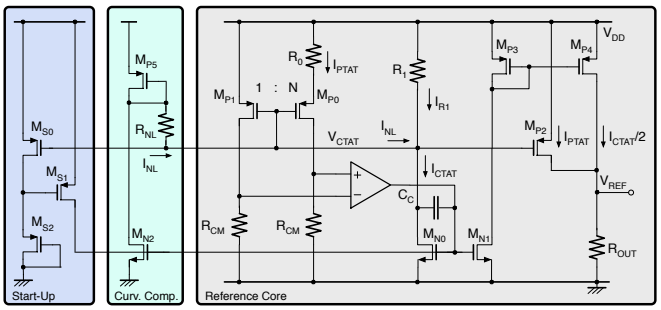

Fig. 3. Schematic diagram of the proposed voltage reference.

C. Temperature compensation

The circuit needs start-up and curvature correction for increasing the operating temperature range. The circuits in Fig. 3 achieve the two functions. The start-up circuit is a conventional static scheme. The curvature compensation is necessary because of the non-linear behavior of the gate-source voltage of MOS transistors in sub-threshold, namely the V_{GS} of M_{P0} and M_{P1}. The drain current of a MOS transistor operating in the sub-threshold region becomes almost independent of its drain-source voltage, V_{DS}, when V_{DS} is larger than $4V_T$, V_T being the thermal voltage. In this condition, the V_{GS} of PMOS transistors in sub-threshold is approximately expressed as [8]

$$|V_{GSp}| = |V_{th}| + \eta V_T \ln\left(\frac{I_D}{\mu_p C_{ox}\frac{W}{L}V_T^2}\right) \tag{3}$$

where μ_p is the hole mobility, V_{th} the PMOS threshold voltage. At a first approximation, V_T, V_{th}, and μ_p introduce dependence on temperature. Linear temperature dependence of V_{th} can be modelled as [8]

$$V_{th} = V_{th}(T_0) + k_{th}(T - T_0) \tag{4}$$

where $V_{th}(T_0)$ is the threshold voltage at reference temperature, and k_{th} is a negative coefficient. The second term in (3), generates non-linearity in $I_{R1} = |V_{GS1}|/R_1$ (Fig. 3). This term can be cancelled by injecting its equal and opposite replica current, i.e. I_{NL} into the node V_{CTAT}. The circuit in Fig. 3 shows the implemented solution. The current flowing in M_{P5} is CTAT, the difference between its gate-source voltage and the one of M_{P1} (driven with PTAT current) divided by R_{NL} determines I_{NL}

$$I_{NL} = \frac{|V_{GS1}| - |V_{GS5}|}{R_{NL}} = \frac{\eta V_T}{R_{NL}} \ln\left(\frac{(W/L)_5}{(W/L)_1}\frac{I_{D1}}{I_{D5}}\right) \tag{5}$$

Optimal transistor sizes and R_{NL} have to be chosen to cancel the non-linear term of I_{R1} so that $I_{NL} + I_{R1}$ leads to the I_{CTAT} that has only linear temperature dependency due to the threshold voltage. Hence, the condition that has to be satisfied for higher order compensation is obtained as

$$\frac{R_{NL}}{R_1} = \ln\left(\frac{(W/L)_5}{(W/L)_1}\frac{I_{D1}}{I_{D5}}\right) / \ln\left(\frac{\mu_p C_{ox}(W/L)_1 V_T^2}{I_{D1}}\right) \tag{6}$$

CTAT and PTAT currents are summed at the output branch generating an output reference on R_{OUT}

$$V_{REF} = R_{OUT}\left(\frac{V_{th}(T_0) + k_{th}(T - T_0)}{R_1} + \frac{\eta V_T \ln(N)}{R_0}\right) \tag{7}$$

In order to achieve a temperature independent output reference, the value of the resistor R_1 is obtained as follows by satisfying $\delta V_{REF}/\delta T = 0$:

$$R_1 = \frac{|k_{th}|}{\eta\frac{k}{q}\ln(N)} R_0 = K R_0 \tag{8}$$

where K is a temperature independent constant and is around 2.5 for this technology.

Finally, by substituiting (8) in (7), the resulting reference voltage is obtained as

$$V_{REF} = R_{OUT}\frac{V_{th}(T_0) - k_{th}T_0}{R_1}. \tag{9}$$

Fig. 4 plots the simulated currents flowing in the different branches of the circuit as a function of the temperature. Current I_{R1} does not replicate the expected CTAT behavior because of the non-linear temperature dependence of V_{GSP1}. Current I_{NL}, almost zero at low temperature, shows the expected opposite behavior.

III. Measurement Results

This voltage reference has been fabricated in a standard 0.18-µm CMOS technology (without any additional or special process step) and measured with the nominal supply voltage of 0.4 V. Fig. 5 shows the chip microphotograph with layout back-annotation. The active area (400×225 µm^2) is dominated by the resistors (74% of the total area), very large to reduce the power consumption. However, technologies having higher resistive layers would reduce the total area significantly.

A thermal chamber ESPEC BTZ-175E controls the chip temperature and gives rise to the waveforms of Fig. 6. It shows the measured output voltage of the available 5 samples as a function of the temperature. R_1 is trimmed to achieve the best temperature coefficient. The average of the generated reference voltage is 212.4 mV with a mean TC of 84.5 ppm/°C over the

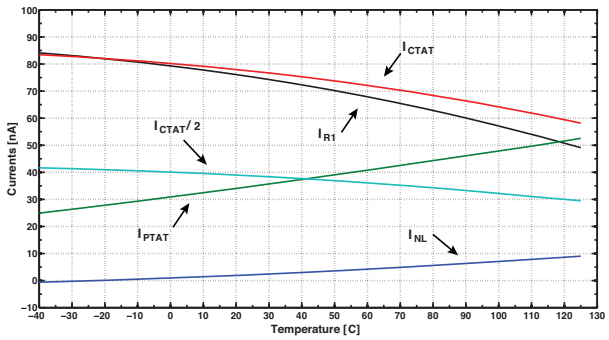

Fig. 4. Simulated currents of different circuit branches as a function of the temperature.

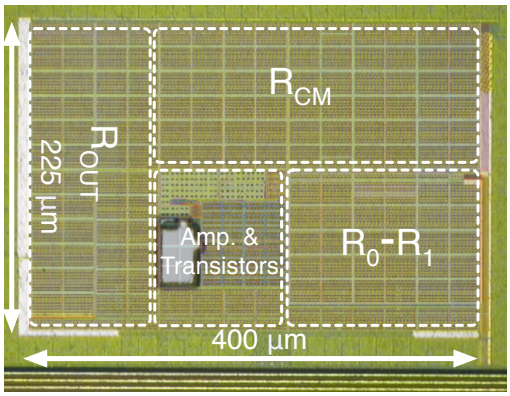

Fig. 5. Chip microphotograph with layout back-annotation.

temperature range from -40 to 130°C. The measured supply current at room temperature is 480 nA, which is bringing the power consumption to 192 nW with the nominal supply voltage. Experimental results match well with the simulations.

Since the 5 available samples are from the same wafer and also not enough to have a proper statistical information, the distribution of the reference voltage and of the untrimmed temperature coefficient obtained through 100-point process and mismatch Monte Carlo simulation runs are given in Fig. 7. The simulated mean value is 213.1 mV with a standard deviation of 1.75 mV, leading to an expected untrimmed 3σ accuracy of 2%. The output voltage has a mean TC of 93.7 ppm/°C with a standard deviation of 20.64 ppm/°C.

Fig. 8 shows the power supply rejection (PSR) at the nominal supply voltage and room temperature measured from 1 Hz to 100 kHz together with the simulated results (solid line). The matching between measurements and simulations is good and the measured PSR at 100 Hz is -40 dB. Fig. 8 gives the generated output voltage as a function of the supply voltage at room temperature as well. The circuit starts working properly when the supply voltage is equal to 0.4 V. In the supply voltage range from 0.4 V to 1.2 V, the line sensitivity is 0.957 %/V. There was no start-up issue at any measurement temperature.

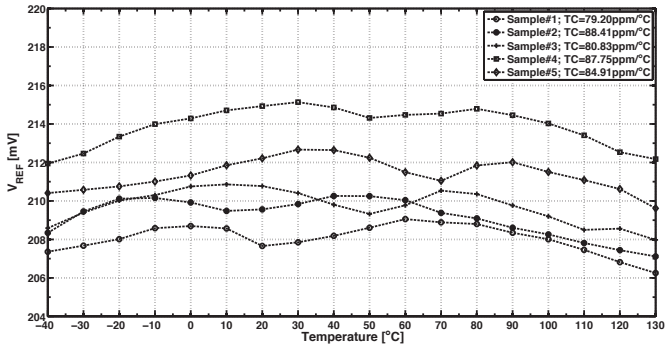

Fig. 6. Measured reference voltage as a function of the temperature on the available 5 samples.

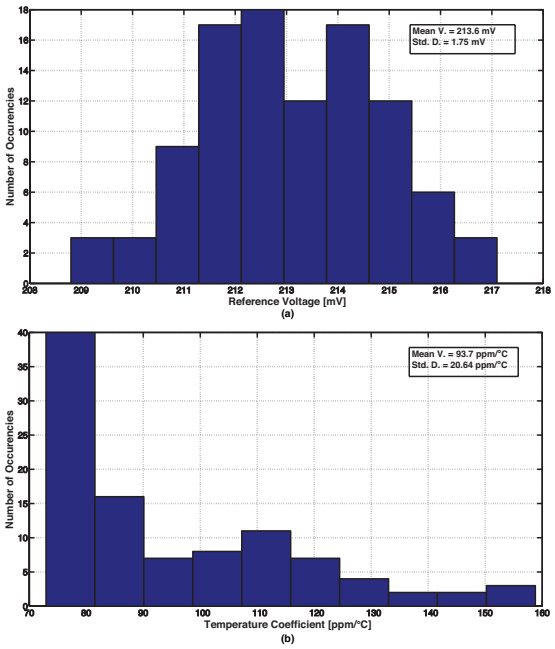

Fig. 7. Simulated distributions obtained through 100-point process and mismatch Monte Carlo runs: (a) untrimmed reference voltage, (b) untrimmed temperature coefficient.

Fig. 9 shows the power spectral density of the output voltage measured without filtering capacitors from 1 Hz to 100 kHz together with the simulation results. The spectrum analyzer available for the experiment limits the measured range. Simulations and measurements are in good agreement. Using the simulated data, the root mean square voltage noise integrated from 0.1 Hz to 10 Hz is 17.45 µV. The measured output noise amplitude in the flat band region is 1.1 µV/Hz. A pole in the used measurement setup dominated the high frequency behaviour. From the noise analysis of the circuit, flicker noise of transistors M_{N0} and M_{N1} are the dominant noise sources for the frequency range 0.1 Hz–100 Hz, while the channel thermal noise of transistors M_{P0} and M_{P1} are the

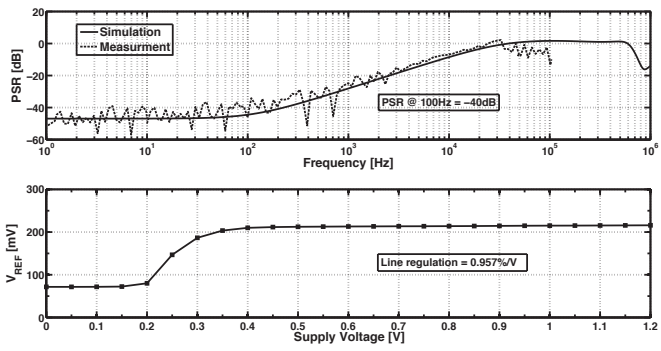

Fig. 8. Measured power supply rejection and line regulation.

TABLE I. PERFORMANCE SUMMARY AND COMPARISON WITH OTHER PUBLISHED STATE-OF-THE-ART REFERENCE CIRCUITS.

Parameter	This Work	[8]	[10]	[12]	[11]	[13]	[9]	[14]
CMOS Technology [μm]	0.18	0.18	0.13	0.09	0.18	0.18	0.13	0.18
Output Voltage [mV]	212.4	257.5	500	241	193	548	185	323
Minimum Supply Voltage [V]	0.4	0.45	0.5	0.55	0.65	0.7	0.75	0.75
Power Consumption [nW]	192	2.6	32	482000	318.5	52.5	170	4000
TC [ppm/°C]	84.5	165	75	150	43	114	40	15
Temperature Range [°C]	-40–130	0–125	0–80	10–100	0–120	-40–120	-20–85	-60–130
PSR @100Hz [dB]	-40	-45	-40	-35	-50	-56	N/A	-34*a*
Untrimmed Accuracy (3σ)[%]	2^b	12	2^b	5	0.8	4.8	3	N/A
Area [mm^2]	0.09	0.043	0.0265	0.07	0.195	0.025	0.07	0.039

a: Estimated from the line regulation value, b: Simulated values.

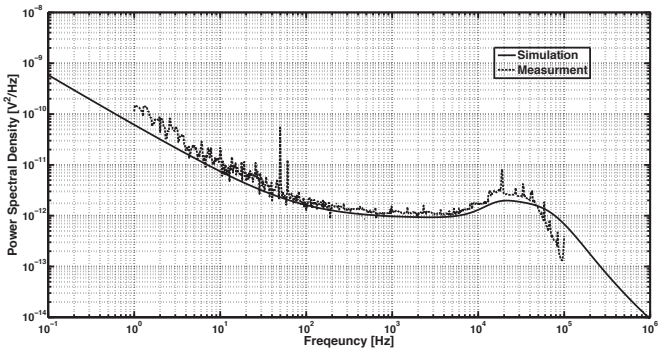

Fig. 9. Measured power spectral density of the output voltage.

dominant noise sources for the frequency range 100 Hz to 1 MHz.

Table I summarizes the measurement results of the typical performance chip and compares them with previous state-of-the-art voltage references implemented in standard CMOS process. From the comparison it results that the proposed circuit achieves the lowest supply voltage and is able to work over a very wide temperature range. This is obtained while preserving competitive temperature coefficient, PSR, line sensitivity, and area occupation.

IV. CONCLUSION

An ultra low voltage and very low power voltage reference circuit, fabricated in a standard 0.18-μm CMOS process, is presented. The use of a novel current-mode circuit topology together with MOS transistors in sub-threshold region allows a reduction of the current consumption and the use of a supply voltage as low as 0.4 V, the lowest reported in the open literature. A high order temperature compensation designed to extend the temperature operating range of the circuit has been described and its effectiveness has been experimentally validated.

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