A 1-V, 3-GHz Strong-Arm Latch Voltage Comparator for High Speed Applications

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***Abstract*—This paper proposes a parallel path based strong-arm latch voltage comparator. The proposed architecture improves the speed performance when compared to the conventional strong-arm latch. The improvement is achieved by the addition of parallel paths to the output node. This increases the effective transconductance at the output node, allowing the load capacitor to discharge faster during the regenerative phase. The architecture has been designed and extensively simulated at pre- and post-layout level in a 65-nm CMOS technology with a supply voltage of 1 V and it achieves a 3-GHz bandwidth. The speed increases by approximately 50% with respect to the conventional topology. The Monte-Carlo analysis is performed for 200 samples, which results in an offset standard deviation of 2.05 mV.**

***Index Terms*—Regenerative comparators, high speed designs, offset, positive feedback**

I. Introduction

TODAY, comparators have become an integral part of many analog and mixed-signal designs. In the era of high speed and low power devices, it is essential to design a comparator that satisfies the state-of-the-art requirements. Lowering the technology node has aided in achieving these requirements to a certain extent. Nevertheless, there still exists a need to enhance the performance of the comparator. Clocked comparators [1] are usually preferred over continuous-time comparator, as the static power dissipation is virtually zero. The positive feedback circuit in the clocked comparator enhances the speed of its operation. Various works have been explored in literature that have either increased the speed or have decreased the offset and power consumption. One of the techniques to enhance the speed consists in using cascaded pre-amplifiers before the regenerative latch. The pre-amplifiers amplify the input differential voltage, thereby reducing the decision-making time for the latch to resolve the difference at the inputs. Additionally, pre-amplifiers also contribute in the reduction of the offset voltage [2]. However, this comes at the cost of higher power dissipation and larger area. Alternatively, the speed performance of the comparator can be improved by reducing the threshold voltage of the regenerative latch. The body biasing technique [3] is used to reduce the threshold voltage of the transistor. However, it suffers from an increased offset due to non-linear effect on the comparator. A sub-threshold operating comparator was designed to reduce the power dissipation in [4]. However, operating in the sub-threshold region leads to higher leakage currents, resulting in a higher offset voltage [5]. Thus, the sizes of the transistors are maintained large enough to operate them in sub-threshold, which results in significant area overhead. In literature, the performance of these comparators has been analyzed in terms of noise [6], offset [7], kick-back noise [8].

This work focuses on increasing the performance of the comparator in terms of speed, without consuming significant power in comparison to the conventional strong-arm latch comparator. The performance improvement is achieved by adding N-parallel paths at the output node to have a faster-discharging rate. The circuit has been designed and simulated in a 65-nm CMOS technology at the transistor and at the post-layout level. The proposed technique achieves a reduction in the delay by approximately 50%, when compared to the conventional strong-arm latch comparator.

The paper is further organized as follows. The conventional strong-arm latch comparator is discussed in Section II. Section III explores the proposed comparator along with the mismatch analysis. Simulation results are addressed in Section IV. Design consideration has been discussed in Section V and conclusions are drawn in Section VI.

II. Conventional Strong Arm Latch Comparator

The schematic diagram of a conventional strong-arm latch comparator is shown in Fig. 1. When the clock signal, CLK, is low (CLK = 0), the comparator operates in the reset phase. When CLK is high, the circuit operates in the regenerative phase. In this phase, the tail transistor turns ON, while M3 and M4 turn OFF. The time required for the Outm node to reach $V_{\text{DD}} - |V_{\text{thp}}|$ or M8 transistor to turn ON is here referred to as t_0. Also, the time required to reach the differential output to $V_{\text{DD}}/2$ after M8 turns ON is defined as t_{latch}. The total delay [9] is given by

$$t_{delay,conv} = \frac{2C_L|V_{\text{thp}}|}{I_0} + \frac{C_L}{g_{m,eff}} \ln\left(\frac{V_{\text{DD}}}{4\,|V_{\text{thp}}|\,\Delta V_{\text{IN}}}\sqrt{\frac{I_0}{\beta_{1,2}}}\right) \quad (1)$$

where $\beta_{1,2}$=$\frac{1}{2}\mu_n C_{ox}(\frac{W}{L})_{1,2}$, C_L represents the load capacitance, I_0 is the tail current flowing through the tail transistor Mtail, and $g_{m,eff}$ indicates the total transconductance of the back-to-back connected inverters, i.e., $g_{m,eff} = g_{m6,8}+g_{m5,7}$. The delay is inversely proportional to the differential input voltage, i.e., it takes a larger time to resolve as ΔV_{IN} reduces.

The offset mainly occurs due to input transistors mismatch, threshold mismatch, and load capacitor mismatch. Here, the

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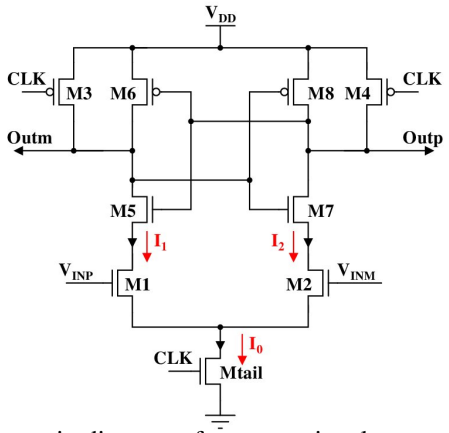


Fig. 1: Schematic diagram of a conventional strong-arm latch comparator.

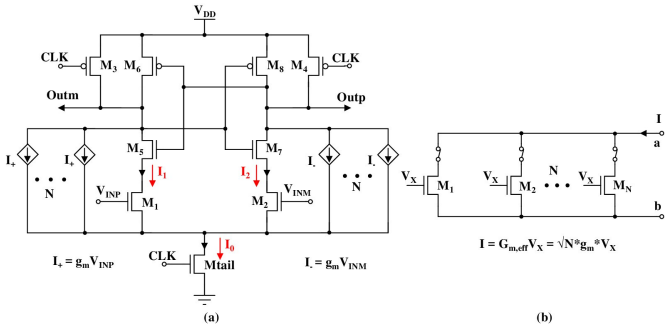


Fig. 2: (a) N-parallel path based proposed strong-arm latch comparator, (b) equivalent model of parallel branches.

change in width and threshold voltage variations are taken into consideration for mismatch calculations. The mismatch analysis was done in [7] and the change in current for the conventional comparator can be given by,

$$\Delta I_{conv} = \Delta I_1 + \Delta I_2 = -\frac{1}{2} g_m \Delta V_{t1,2} + \frac{1}{2}\left(\frac{\Delta\beta_{1,2}}{\beta_{1,2}}\right) I_0 \quad (2)$$

where $\beta_{1,2}$ represents the width of the input differential pair, $\Delta\beta$ is the mismatch in the input transistor width, ΔV_t is the mismatch in the threshold voltage of the input differential pair M1 and M2, which is given by

$$\Delta V_{t1,2} = V_{t1} - V_{t2} \quad (3)$$

The offset in the conventional comparator is then given by,

$$V_{os,conv} \mid M_{1,2} = \frac{\Delta I_{conv}}{g_{m1,2}} = \Delta V_{t1,2} + \frac{\Delta\beta_{1,2}}{\beta_{1,2}} . \frac{V_{DSAT1,2}}{2} \quad (4)$$

where $V_{DSAT1,2}$ indicates the overdrive voltage of the input differential pair. Thus, the offset voltage in the comparator can be reduced by increasing the effective transconductance of the input transistors, which is possible by increasing their widths. Also, the offset voltage can be nullified using offset reduction techniques [10]. However, increasing the input transistors width has no impact on the overall delay of the comparator [9]. This work presents a technique consisting of the addition of N-parallel branches at the output node, which not only decreases the offset but also reduces the overall delay of the comparator.

III. Proposed Strong-Arm Latch Comparator

The conventional architecture has a single path for the capacitor to discharge, which can considerably increase the delay of the comparator. The proposed work minimizes the delay by providing N-additional current paths for the load capacitor, which is conceptually shown in Fig. 2(a). The current through the additional paths depends on the magnitude of the input voltage of the differential pair, i.e. V_{INP} and V_{INM}. It can be observed from the equivalent model of the parallel branches in Fig. 2(b) that the total current in the parallel branches will be $\sqrt{N}$ times the current through the conventional architecture. The transistor level implementation of the proposed architecture is depicted in Fig. 3. During the reset phase, the proposed architecture operates in the same way as the conventional comparator. During regenerative phase, the capacitor starts discharging through the parallel paths. The input signal is fed to all the N-parallel branches, each allows a current of $g_m V_{IN}$ to flow through it. Thus, the total current from the load capacitor discharges through N+1 branches. However, the total current through the tail transistor remains constant. Also, for N-parallel branches, the effective transconductance at the output node will increase by $\sqrt{N}$ times, thereby resulting in reduction in delay. Once the output is generated, the conventional comparator has no current path from V_{DD} to ground and thus, has no static power consumption. However, in the proposed architecture, the additional branches continuously dissipate power even after the output is settled. This issue can be resolved by providing an additional auxiliary clock (CLK1), as shown in Fig. 3. This additional auxiliary clock can be generated as shown in Fig. 3. The ON-time duration of the pulse (CLK1) depends on the worst case delay of the comparator, which is adjusted by the delay element. The addition of the parallel paths reduces the overall delay of the proposed comparator, which turns out to be equal to

$$t_{delay,prop} = \frac{2C_L|V_{thp}|}{I_0} + \frac{C_L}{\boldsymbol{G}_{m,prop}} \ln\left(\frac{V_{DD}}{4\,|V_{thp}|\,\Delta V_{IN}}\sqrt{\frac{I_0}{\beta_{1,2}}}\right) \quad (5)$$

where $G_{m,prop} = g_{mp} + g_{mn} + \sqrt{N} * g_{m1,2}$, g_{mp} and g_{mn} indicates the transconductance of the latch transistors ($M_{3,4}$ and $M_{5,6}$), while $g_{m1,2}$ is the transconductance of the input transistor ($M_{1,2}$).

A. Mismatch Analysis

For the proposed comparator architecture, the tail transistor current is same as that of the current discharging through the load capacitor. Hence, the second term in equation (2) remains unchanged. However, as the transconductance from all the branches adds up to the output node, the effect of threshold mismatch on the current becomes $\sqrt{N}$ times. Thus, the change in current for the proposed comparator can be expressed as-

$$\Delta I_{prop} = \Delta I_1 + \Delta I_2 = -\frac{1}{2}\sqrt{N} g_{m1,2} \Delta V_{t1,2} + \frac{1}{2}\left(\frac{\Delta\beta_{1,2}}{\beta_{1,2}}\right) I_0 \quad (6)$$

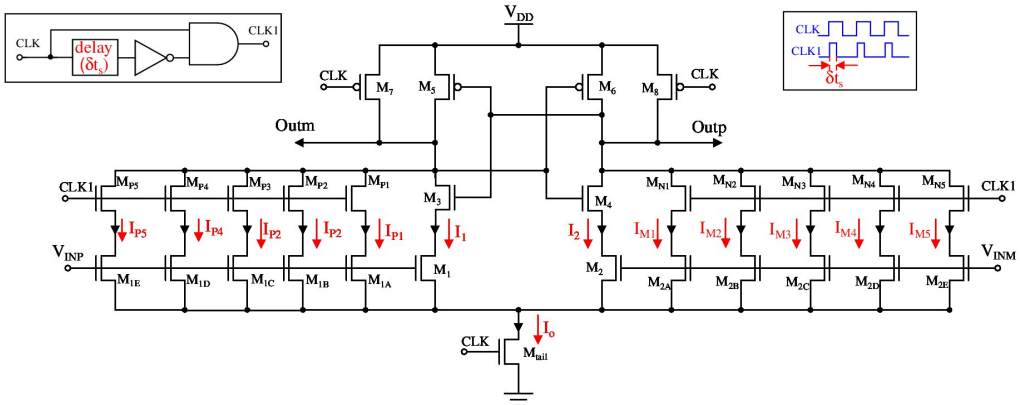


Fig. 3: Transistor level implementation of the proposed srtong-arm latch comparator.

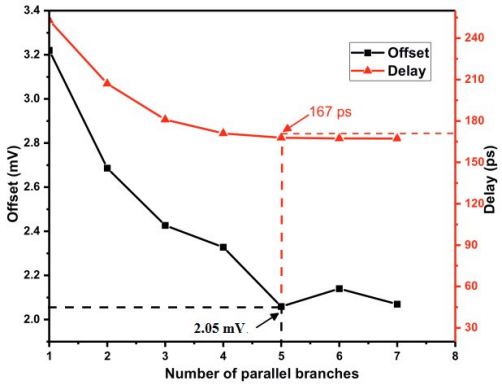


Fig. 4: Simulated delay and offset as a function of the number of parallel paths.

The offset of the proposed comparator can be derived as,

$$V_{os,prop} \mid M_{1,2} = \frac{\Delta I_{prop}}{\sqrt{N} * g_{m1,2}} = \Delta V_{t1,2} + \frac{1}{\sqrt{N}} \frac{\Delta\beta_{1,2}}{\beta_{1,2}} . \frac{V_{DSAT1,2}}{2} \tag{7}$$

It can be seen from equation (7) that the offset due to threshold mismatch does not depend on the number of parallel branches. This is due to the fact that the change in current due to threshold mismatch from the transistors of parallel branches is nullified by the increased transconductance due to the parallel branches. Thus, the first term in equation (7) is independent of N, whereas the second term is reduced by $\sqrt{N}$ times. As the second term depends on the ratio of $\Delta\beta/\beta$, the net effect of parallel branches cancels out in the equation of change in current as seen from equation (6). Thus, the second term in equation (7) reduces by $\sqrt{N}$ times as compared to the conventional comparator.

B. Choice of N

The delay and Monte-Carlo analysis for offset were carried out for different number of parallel branches. The output was driven by the output buffer, whose input capacitance was 14 fF. The results are plotted in Fig. 4. As derived from equation (5) and (7), the delay and offset decrease with an increase in the number of parallel paths. However, as the value of N becomes large, the second term in equation (7) becomes negligible and the impact of $\Delta V_{t1,2}$ dominates the offset voltage. This can be noted from Fig. 4. For more than 5 branches in parallel, the offset remains close to 2.1 mV. For 5-parallel branches, if the threshold has a mismatch of 5% and the transistor width has a mismatch of 1%, then the offset calculated from equation (7) for $V_{DSAT} = 0.4\ V$ turns out to be 2.4 mV. This value of offset is close to offset found from the simulation results in Fig. 4.

TABLE I: Transistors size used in the proposed comparator design (all sizes are in μm).

Transistor	Size
$M_{1,2}$, M_{1A-E}, M_{2A-E}	8/0.09
$M_{3,4}$	8/0.06
$M_{5,6}$	8/0.06
$M_{7,8}$	2/0.06
M_{P1-5}, M_{N1-5}	2/0.06
M_{tail}	16/0.09

IV. Results & Discussion

The proposed architecture was designed and simulated at the transistor level using a 65-nm CMOS technology with a nominal supply voltage of 1 V. The total number of parallel branches is chosen to be 5. The size of the transistors used in the proposed design are tabulated in Table I. The layout of the proposed architecture has an area of 32.6 μm x 18.5 μm as shown in Fig. 5. The following analyses were performed to verify the effectiveness of the proposed comparator.

A. Transient Analysis

A ramp input signal was given to the comparator. The delay of the comparator increases with decrease in the input common-mode voltage. For a worst case scenario, the reference voltage (V_{INM}) was fixed to 0.5 V. To achieve a rail-to-rail output voltage swing and to increase the driving capability of the comparator, a buffer is connected to each of the output node. The result of a transient analysis with $\Delta V_{\mathrm{IN}} = 2\ mV$ for the conventional and the proposed comparator is shown in Fig. 6. The delay for the proposed comparator before and after connecting the buffer at the output node was found to be 217 ps and 167 ps respectively, whereas the conventional comparator has 466 ps and 377 ps respectively. The speed performance of the proposed comparator has therefore increased by a factor of 2.

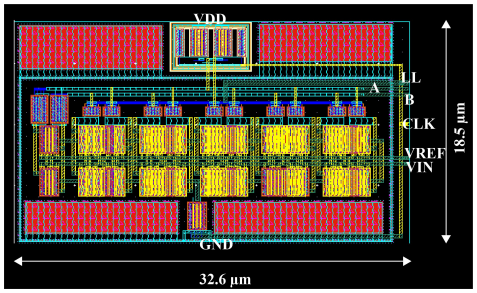


Fig. 5: Layout implementation of the proposed comparator architecture.

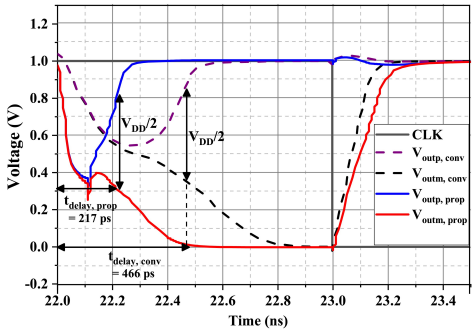
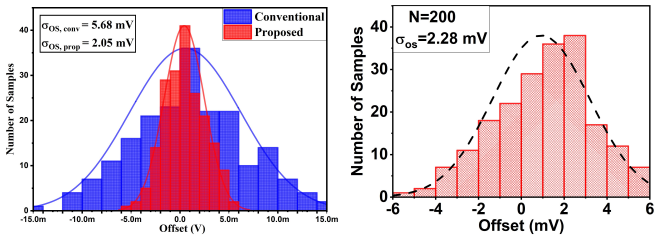
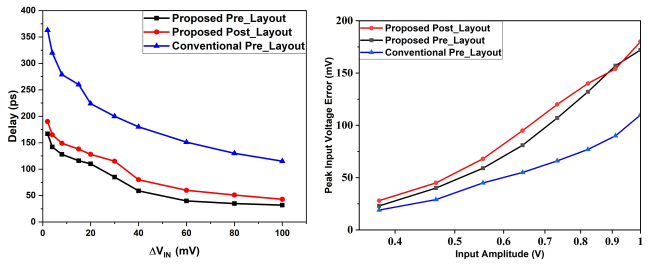


Fig. 6: Transient simulation at ΔV_{IN} = 2 mV and V_{DD} = 1 V for the conventional and proposed architecture.



(a) (b)

Fig. 7: Monte-Carlo simulation results for offset of (a) pre-layout conventional and proposed architecture, (b) post-layout proposed architecture.



(a) (b)

Fig. 8: (a) Simulated delay as a function of the input differential voltage, (b) variation of the peak input voltage error due to kickback noise with respect to amplitude of the input signal.

B. Monte-Carlo Analysis

Monte-Carlo simulation was performed to analyze the effect of process variation and mismatch in the transistors. The offset standard deviation for the conventional and the proposed comparator is shown in Fig. 7(a). It can be observed that the conventional comparator has a standard deviation of the offset equal to 5.68 mV, whereas the proposed comparator has 2.05 mV for 200 samples. The result can be confirmed also from equations (4) and (7). The offset resulted from the post-layout simulation for the proposed comparator for 200 samples is 2.28 mV as shown in Fig. 7(b).

C. Delay as a function of ΔV_{IN}

The differential input signal was swept from 2 mV to 100 mV and the delay analysis was carried out. The overall delay was plotted with respect to the differential input voltage (ΔV_{IN}) as shown in Fig. 8(a). It can be noticed that the proposed architecture has a delay of 167 ps at $\Delta V_{\text{IN}} = 2\ mV$, whereas the conventional architecture has a delay of 377 ps. Also, the delay decreases with increase in the differential input voltage for both the conventional and the proposed comparator, which is evident from equations (1) and (5). Furthermore, the increase in the delay due to the parasitics from the post-layout simulations are also indicated with circle symbol in Fig. 8(a).

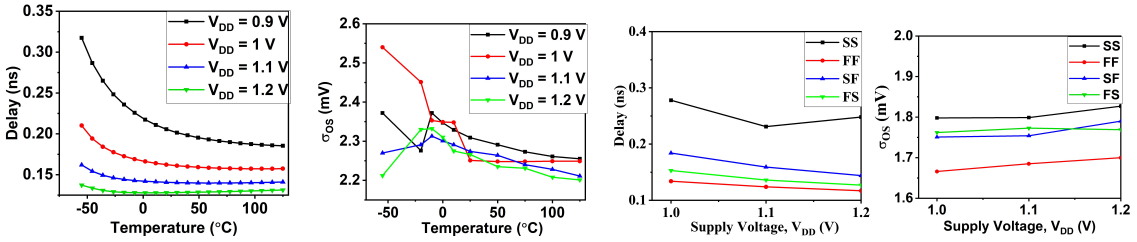
D. Kickback Noise Analysis

The latch output transition results in disturbance at the inputs of the comparator, known as kickback noise. Thus, it becomes mandatory to evaluate the kickback noise for the comparators working at high speed. The kickback noise was simulated and the peak error in the input voltage is plotted with respect to the input signal amplitude as shown in Fig. 8(b). It can be observed that the peak error increases with the increase in the input voltage. The proposed architecture has higher kickback noise compared to the conventional architecture. It was analysed in [8] that the high speed and power efficient comparators suffers from large kickback noise.

E. Delay and offset as a function of PVT variations

The variations in delay and offset of the proposed comparator as a function of PVT variations are shown in Fig. 9. It can be observed from Fig. 9(a) that the delay at a supply voltage of 1 V varies from -2% to 8% with respect to room temperature. Similarly, the variation in the offset standard deviation is $\pm 10\%$ with respect to room temperature at a supply voltage of 1 V. Also, the variation in delay and offset at different corners is shown in Fig. 9(c) and (d) respectively. It is important to note that the SS corner results in the maximum deviation in delay and offset.

The performance of the comparator is compared with the state-of-the-art comparator architectures as tabulated in Table II. The energy consumed by the comparator in one conversion is referred to as energy per conversion. The design in [12] has the lowest energy per conversion. However, it has the disadvantage of large offset. The reduction in delay of the proposed comparator increases the maximum operating frequency of the comparator, which turns out to be 3 GHz. The proposed design shows the best performance with respect to speed, offset and delay for a reduced ΔV_{IN} of 2 mV.



(a) (b) (c) (d)

Fig. 9: Performance variations as a function of (a), (b) PVT variations, (c), (d) corner variations.

TABLE II: Comparison with the state-of-the-art architectures.

Parameters	This Work	Conventional	[11]	[12]	[13]
Technology	**65 nm**	65 nm	65 nm	65 nm	130 nm
Supply voltage	**1 V**	1 V	1.2 V	1.2 V	1.2 V
f_{max}	**3 GHz**	2 GHz	7 GHz	NA	1.25 GHz
Energy per conv.	**108 fJ**	55 fJ	186 fJ	30 fJ	480 fJ
Delay or Delay / log(ΔV_{IN})	**62 ps/dec**	140 ps/dec	64ps @ΔV_{IN}=18.6 mV	85 ps/dec	NA
σ_{os}	**2.05 mV**	5.68 mV	NA	5.4 mV	7.78 mV
Area	**603** μm^2	134 μm^2	320 μm^2	125 μm^2	NA

V. Design Procedure

While designing the comparator, it must be ensured that the capacitance seen at the output node must be minimum to reduce the delay arising due to parasitic capacitance under no load condition. The parasitic capacitance seen at the drain terminal of $M_{P,N}$ can be given by $C_D = C_{DB} + (1 - \frac{1}{A_V})C_{GD} \approx C_{DB} + C_{GD}$, where A_V indicates the gain of the $M_{P,N}$ transistors. Thus, the equivalent capacitance at the output terminal (Outp, Outm) with N parallel branches can be written as, $C_D = N(C_{DB} + C_{GD}) + C_{latch}$, where C_{latch} indicates the total latch capacitance seen at the drain of $M_{3,4}$ and $M_{5,6}$. To have faster regeneration, the width of the latch transistors are kept higher than M_{P1-5} and M_{N1-5}. Thus, the effective capacitance seen at the output node is dominated by the latch. However, the additional parasitics at the output node due to N-parallel branches increases the power consumption as given by,

$$\Delta P = 2{*}\Delta C_L{*}V_{DD}^2{*}f = 2{*}N(C_{DB}{+}C_{GD}){*}V_{DD}^2{*}f \quad (8)$$

For N=5, ΔC_L=5 fF, V_{DD}=1 V, and f=1 GHz, the increase in the dynamic power consumption turns out to be 50 μW. The power analysis was done for conventional comparator with nominal widths and with five times increase in the width of the input transistors. It was found that the power increases from 100 μW to 120 μW at f=1 GHz. The power consumed by the proposed comparator for N=5 at f=1 GHz is 157 μW, which is 37 μW higher than the conventional comparator due to the additional parasitics at the output node. The width of the transistors M_{1A-E} and M_{2A-E} are kept the same as that of the input transistors $M_{1,2}$. The ON-duration width of the clock pulse (CLK1) is decided by the worst case delay of the comparator.

VI. Conclusions

In this paper, a strong-arm latch comparator consisting of N-parallel path was presented. The design was implemented in a 65-nm CMOS technology with a supply voltage of 1 V. From the theoretical analyses and simulation results, it was verified that N=5 is the best choice for the number of parallel paths in the proposed comparator. The delay of the proposed comparator is decreased by approximately 50% compared to conventional topology.

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