DCR performance in neutron-irradiated CMOS SPADs from 150 and 180 nm technologies

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***Abstract*—Single photon avalanche diodes (SPADs) fabricated in two different CMOS technologies were exposed to a neutron source up to a maximum fluence of 3×10^{11} 1 MeV neutron equivalent cm^{-2}. Significant changes in the dark count rate, with a strong dependence on the fluence and on the device active area, were detected after irradiation. A model for the probability of dark count rate degradation, accounting for the source spectrum and the geometry of the device under test (DUT), was proposed and proved to be in good agreement with experimental data. The model may be helpful in performing worst-case analysis of SPAD based detection systems under neutron irradiation.**

***Index Terms*—Bulk damage, CMOS SPAD, dark count rate.**

I. Introduction

THE use of single photon avalanche diodes (SPADs) is rapidly spreading to a large set of applications. SPADs are regarded as the ultimate solution for the development of optical sensing systems based on time correlated single photon counting techniques. They can guarantee state-of-the-art space and time resolution in capturing weak optical signals while covering quite a large set of applications, including optical ranging, fluorescence lifetime imaging, positron emission tomography, Raman spectroscopy and single molecule fluorescence spectroscopy [1], [2]. SPADs also represent the fundamental building blocks for silicon photomultipliers (SiPMs), which provide a compact, magnetic-field insensitive and versatile alternative to vacuum tube PMs in implementing medical diagnostic techniques, such as combined positron emission tomography/magnetic resonance imaging (PET/MRI), and in many low light level applications [3], [4], including Cherenkov light and γ-ray detection, calorimetry and charged particle tracking in astro- and particle physics experiments [5], [6].

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SPADs have been and are fabricated in a range of different custom processes tuned for best device performance. However, in recent times, CMOS SPAD technologies are emerging as an extremely flexible solution for the design of sensor arrays with monolithically integrated processing electronics [7].

In some of the above mentioned applications, SPADs are exposed to ionizing and non-ionizing radiation, which may affect the device performance. Among the different SPAD parameters, the dark count rate (DCR), i.e., the average value of spurious pulses triggered by random carrier generation in the device sensitive volume, may be found to increase significantly after irradiation, so that the device might eventually stop working properly [8]. Modeling radiation damage is therefore of paramount importance to anticipate the time to failure of a SPAD-based detector and may be used as a tool to maximize the system radiation tolerance.

This paper discusses the effects of neutron irradiation on SPAD devices fabricated in two different CMOS technologies, provided by two different foundries. The prototypes, conceived for integration in a dual layer structure [6], were developed to target charged particle tracking in low rate, relatively clean environments, such as the experiments at the future linear colliders [9]. In these applications, the DCR becomes the main parameter affecting the false hit rate properties of the detector, while photon detection efficiency (PDE) seems less of a concern. On the other hand, operation at low signal hit rates relaxes the constraints on the dead-time properties of the device. Effects of neutrons and of ionizing radiation on SPADs fabricated in one of the two technologies have been discussed in a paper [10] previously published by some of the authors of this work. The present paper, which is solely concerned with neutron-induced damage, significantly extends the older one by including new experimental results on the same SPADs and on SPADs fabricated in a different technology, therefore enabling a direct comparison between two different process nodes. In addition, this work also presents and validate a

TABLE I
ACTIVE AREA OF THE SPAD STRUCTURES AVAILABLE IN THE CHIPS UNDER TEST (SIZE IS IN $\mu m \times \mu m$)

180 nm SPADs	150 nm SPADs
20×20	43×45
30×30	40×40
36×40	35×35
	30×30

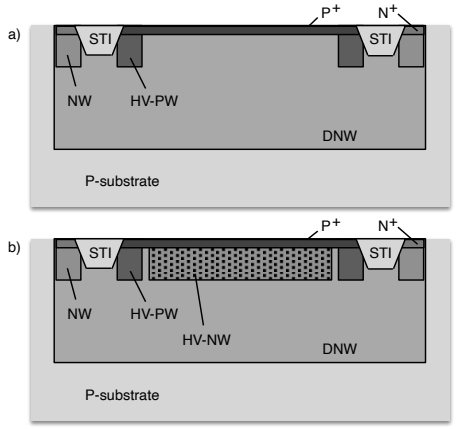

Fig. 1. Simplified cross-section of the two types of SPAD devices in 180 nm CMOS technology tested in this work: a) DPD and b) DPH structures.

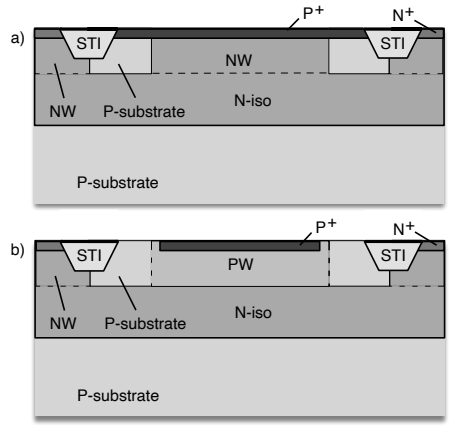

Fig. 2. Simplified cross-section of the two types of SPADs in 150 nm CMOS technology tested in this work: a) type 1 and b) type 2 structures.

simple model for the probability of damage, measured in terms of DCR increase, in SPADs irradiated with a non-monochromatic neutron source. Such a model can be used to perform a worst-case analysis on SPAD based detection systems exposed to neutrons.

II. DUT DESCRIPTION

The experimental results presented in this work were obtained from the characterization of two SPAD arrays designed and fabricated using two different CMOS technologies. The first test vehicle was manufactured in a 180 nm CMOS technology with high voltage option. Among other structures, the chip includes a SPAD array of 17 columns×18 rows with integrated front-end electronics. In the array, SPADs of three different kinds and sizes are available. The active area of the structures integrated in the chip is displayed in Tab. I. Each cell in the array is 100 μm long and 50 μm wide. Of the overall area, a 50 μm×50 μm region is reserved for the sensor, the remaining part (again 50 μm×50 μm) for the processing channel. Fig. 1 shows a simplified cross-section for two sensor structures integrated in the SPAD array (the ones which were

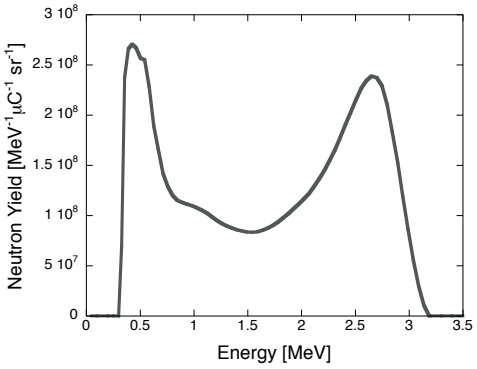

Fig. 3. Distribution of the neutron yield of the INFN Laboratori Nazionali di Legnaro source at a 0° emission angle (from [13]).

characterized for this work). The one in Fig. 1 a) is based on a shallow P^+/DNW (deep N-well) junction. In the structure in Fig. 1 b), the junction is formed between a P^+ diffusion and an additional HV-NW (high-voltage N-well) layer.

An array of 48×16 SPADs was also fabricated in a 150 nm CMOS process. The chip includes two different kinds of devices, whose cross-sections are shown in Fig. 2. The SPAD in Fig. 2 a) uses a shallow P^+ diffusion and an N-well (NW) to form the junction, while in the second structure, the sensitive region of the device is located deeper under the surface, at the boundary between a P-well diffusion and a buried N-type layer (N-iso). The cell area is 50 μm×75 μm, with one third of the cell reserved for the front-end electronics. Half of the cells in the chip has an active area of 43 μm×45 μm, the other half being subdivided in smaller regions containing SPADs with smaller active area (see Tab. I). Data relevant to the characterization of the 150 nm devices presented in this work, including photon detection probability and cross-talk measurements, can be found in the literature [11], [12].

While different readout options were implemented in the chips under test, data presented in this work refer to the case of front-end circuits based on a passive quenching architecture.

III. SOURCE AND IRRADIATION PROCEDURE

A set of 180 nm CMOS chips and one of 150 nm chips were exposed to neutrons at the INFN Laboratori Nazionali di Legnaro. In the source, neutrons emerge from a thick beryllium target bombarded with 5 MeV protons. The neutron yield $Y_n(E,\Omega)$ of the source consists of the number N of neutrons given off by the source per unit energy E, per unit charge Q hitting the Be target and per unit solid angle Ω,

$$Y_n(E,\Omega) = \frac{1}{Q}\frac{d^2N(E,Q,\Omega)}{dE\ d\Omega}. \quad (1)$$

Fig. 3 shows the neutron yield, at a 0° emission angle, for the source used in the tests carried out in this work [13]. The samples were located at a distance $r = 50$ mm from the source, apart from one single case where the chip was located at 98 mm from the Be target. Since the area A of the chips, in the order of 10 mm^2, is much smaller than r^2, the SPAD arrays cover just a small solid angle $\Delta\Omega$ around the

TABLE II
MEAN PRE-IRRADIATION BREAKDOWN VOLTAGE FOR THE DUTS.

180 nm SPADs		150 nm SPADs	
DPD	**DPH**	**type 1**	**type 2**
22.3 V	13.3 V	18.2 V	22 V

zero degree emission angle (with respect to the proton beam axis), such that the neutron yield can be considered constant over the entire DUT area. The total number of neutrons N_T emerging from the source and hitting the chip under test is given by

$$N_T \simeq Q_T \Delta\Omega \int_{E_i}^{E_f} Y_n'(E) dE, \tag{2}$$

where $\Delta\Omega \simeq \frac{A}{r^2}$, Q_T is the total amount of charge hitting the beryllium target. $Y_n'(E)$ is the neutron yield around the zero degree emission angle, where the dependence on the solid angle can be neglected. It is assumed to have support in $[E_i, E_f]$. In the same solid angle, the relationship between $Y_n'(E)$ and the spectral fluence $\phi(E, r)$ at a distance r from the source is given by

$$\phi(E, r) = \frac{Q_T \Delta\Omega}{A} Y_n'(E) \simeq \frac{Q_T}{r^2} Y_n'(E). \tag{3}$$

The maximum fluence reached during the campaign was 10^{11} 1 MeV neutron equivalent cm^{-2} for 180 nm devices and three times as large for 150 nm SPADs. The DUTs were not biased during irradiation and, after irradiation, were always kept at 0°C while not being characterized. Both irradiation and measurements were performed at a temperature of 25°±0.5° C.

IV. NEUTRON EFFECTS ON DCR: EXPERIMENTAL RESULTS

The DUTs were characterized in terms of breakdown voltage and DCR before irradiation and after exposure to neutrons from the above described source. For irradiated samples, measurements started immediately after the end of the irradiation step and were concluded in about 30 minutes. The average value of the breakdown voltage, as resulting from pre-irradiation measurements performed on the four kinds of SPADs under test, is shown in Tab. II. Changes not exceeding a few percent and without any preferential trend, largely within measurement and interpolation errors, were detected after irradiation at any of the considered fluences. The lack of any significant variation in the breakdown voltage is consistent with the fact that, at the low fluences considered in this work, and with the doping concentrations typical of CMOS processes, no change is expected for the effective doping on the two sides of the junction in any of the DUTs. As far as 180 nm SPADs are concerned, more details about breakdown voltage, also including ionizing radiation effects, have been published in a previous paper [10].

DCR was instead found to be significantly affected by exposure to the neutron source. Fig. 4 and Fig. 5 show the percent increase in DCR, $\Delta DCR_{\%}$, for 180 nm CMOS SPADs of the DPD and of the DPH kind respectively, after irradiation with two different neutron fluences, 10^{10} and 10^{11} cm^{-2}. For each single SPAD, the percent DCR increase is defined as

$$\Delta DCR_{\%} = \left(\frac{DCR\ after\ irradiation}{DCR\ before\ irradiation} - 1 \right) \times 100. \tag{4}$$

The five plots refer to devices belonging to two different chips, one exposed to 10^{10}, the other to 10^{11} neutrons cm^{-2}. On the X axis, the number of the cell along a column of the array (the column where, respectively, DPD and DPH SPADs with passive quenching readout were accommodated) is indicated. Fig. 5 b) and c) refer to SPADs in two different columns of the same irradiated chip, containing the same kind of devices with identical size and front-end electronics. DCR was measured at an excess voltage V_{ex} of 1.3 V. Mean and median DCR values for both DPD (12 samples for each size) and DPH SPADs (18 samples for each size) are displayed in Tab. III for the fresh devices and after exposure to a neutron fluence of 10^{10} and 10^{11} cm^{-2}. Note that, in the case of the DPH devices with active area of 20×20 μm^2, mean and median values at 10^{10} cm^{-2} are smaller than in the pre-irradiation case. There is actually no contradiction in these results, nor any indication of a DCR reduction after irradiation. Pre-irradiation data were obtained from a set of 18 SPAD cells. Of them, 6 were exposed to a fluence of 10^{10} cm^{-2}, 12 to a fluence of 10^{11} cm^{-2} (see Tab. V). Therefore, mean and median DCR values after irradiation with a 10^{10} cm^{-2} neutron fluence were calculated just on a subset of 6 devices. In DPD devices, at the smaller fluence, on average a smaller increase (if any) is observed in the case of the devices with smaller active area (20×20 and 30×30 μm^2) as compared to the largest ones. In DPH SPADs, instead, even some of the largest devices showed no significant change in DCR after being subjected to the 10^{10} neutrons cm^{-2} irradiation step. At the higher fluence, both for DPD and DPH SPADs, a huge increase in DCR was detected, always in excess of 100%, with the exception of one single device, cell 13 in Fig. 5 c), where a less than 3% increase was observed. Such a small change is fully compatible with little temperature fluctuations during the experiments and with the

TABLE III
MEAN AND MEDIAN DCR (IN KHZ) FOR 180 nm CMOS SPADS AT DIFFERENT FLUENCE AND DIFFERENT ACTIVE AREA.

		DPD		DPH	
active area	**fluence**	**mean**	**median**	**mean**	**median**
20×20 μm^2	**pre-irradiation**	0.281	0.257	3.38	2.42
	10^{10} cm^{-2}	0.41	0.27	1.89	1.45
	10^{11} cm^{-2}	229	160	1170	1290
30×30 μm^2	**pre-irradiation**	0.68	0.58	42.1	8.14
	10^{10} cm^{-2}	20.9	0.95	465	40.4
	10^{10} cm^{-2}	354	399	1170	1010
36×40 μm^2	**pre-irradiation**	1.64	1.07	41.4	18.8
	10^{10} cm^{-2}	29.3	19.8	181	138
	10^{11} cm^{-2}	543	485	1960	2230

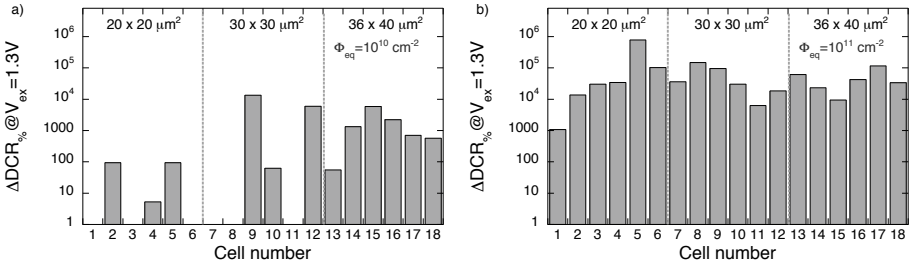

Fig. 4. Percent increase of DCR in 180 nm CMOS SPADs of the DPD kind after irradiation with different neutron fluences: a) 10^{10} 1 MeV neutron equivalent cm^{-2} and b) 10^{11} 1 MeV neutron equivalent cm^{-2}.

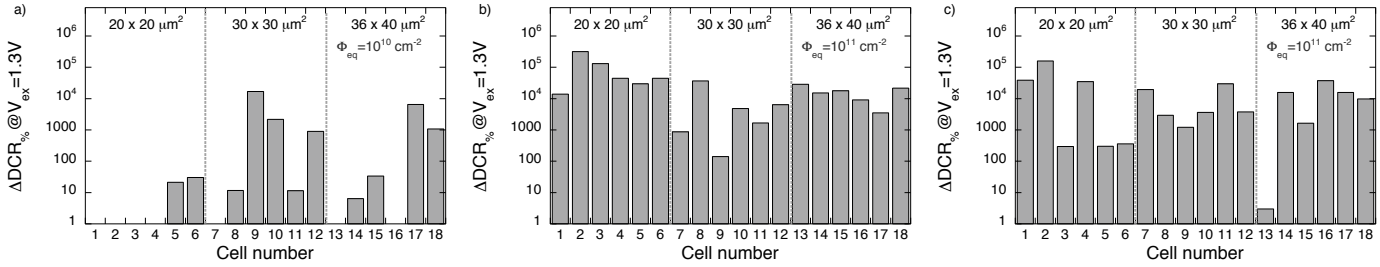

Fig. 5. Percent increase of DCR in 180 nm CMOS SPADs of the DPH kind after irradiation with different neutron fluences: a) 10^{10} 1 MeV neutron equivalent cm^{-2} and b), c) 10^{11} 1 MeV neutron equivalent cm^{-2}.

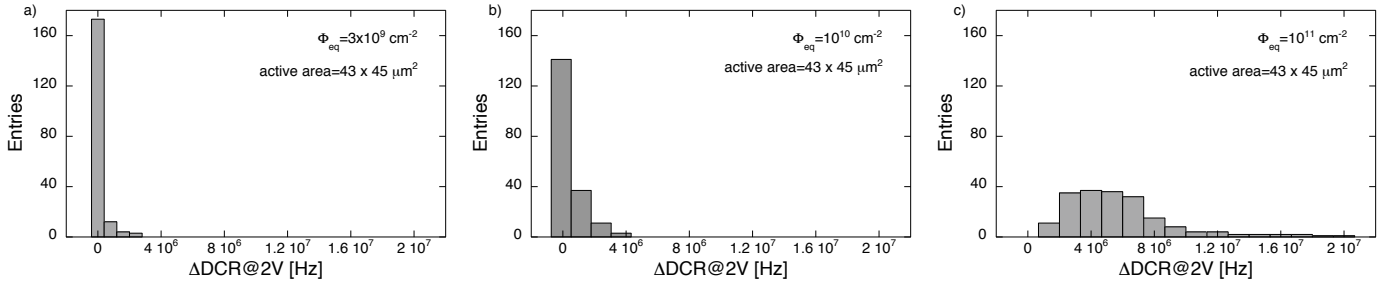

Fig. 6. Distribution of the DCR increase in type 1, 150 nm CMOS SPADs after irradiation with different neutron fluences: a) 3×10^9 1 MeV neutron equivalent cm^{-2}, b) 10^{10} 1 MeV neutron equivalent cm^{-2} and c) 10^{11} 1 MeV neutron equivalent cm^{-2}.

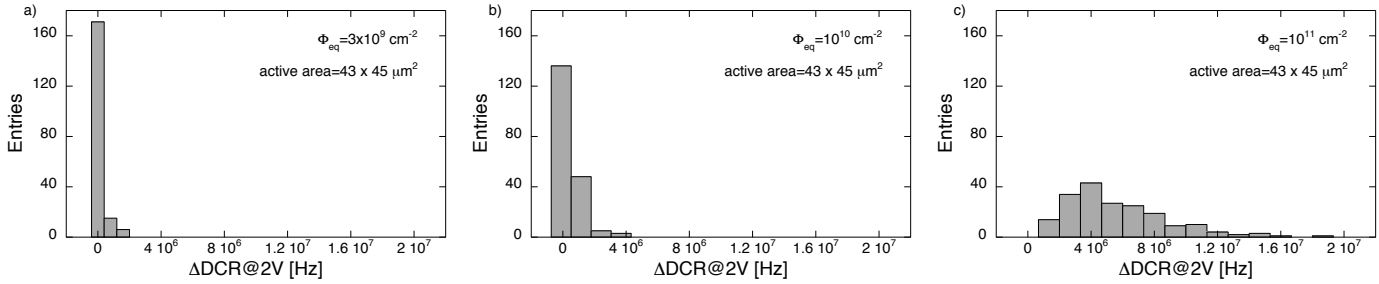

Fig. 7. Distribution of the DCR increase in type 2, 150 nm CMOS SPADs after irradiation with different neutron fluences: a) 3×10^9 1 MeV neutron equivalent cm^{-2}, b) 10^{10} 1 MeV neutron equivalent cm^{-2} and c) 10^{11} 1 MeV neutron equivalent cm^{-2}.

counting noise typical of Poisson processes, and it is very likely not related to an actual damaging event from neutron irradiation.

Figures 6 and 7 show the distribution of DCR increase, ΔDCR, over a population of 192 SPADs with a 43×45 μm^2 active area fabricated in the 150 nm CMOS technology. ΔDCR is defined as the difference between post-irradiation and pre-irradiation DCR. In the two figures, one referring to type 1, the other to type 2 devices, each histogram is relevant to a different fluence: 3×10^9, 10^{10} and 10^{11} neutrons cm^{-2}. Mean and median DCR values for SPADs with the same active area as those in Figures 6 and 7 are shown in Tab. IV in the case of non irradiated devices and for fluences of 10^{10} and 10^{11} cm^{-2}. For both SPAD types, the mean value of the distribution gets higher with the fluence. At the largest fluence considered in the figures, the most probable value is

TABLE IV
MEAN AND MEDIAN DCR (IN KHZ) FOR 150 nm CMOS SPADS WITH 43×45 μm^2 ACTIVE AREA.

	type 1		type 2	
fluence	**mean**	**median**	**mean**	**median**
pre-irradiation	17.8	11.9	14.4	7.8
$\mathbf{10^{10}}$ **cm**$^{-2}$	507	191	467	197
$\mathbf{10^{11}}$ **cm**$^{-2}$	5780	5040	5670	4820

around 4 MHz, but a few samples can be observed to feature a DCR increase in excess of 15 MHz.

The experimental results shown in the above figures are consistent with the statistical nature of neutron damage in silicon devices, which is more apparent when relatively low fluences and devices with small sensitive volumes are involved. The macroscopic effects of small fluxes of neutrons on micro-volumes of silicon are actually exploited to investigate formation and annealing of defects produced by single particle interactions [14]. Irradiation with neutrons is responsible for the creation of deep level defects in the bulk of SPAD devices. For each single interaction, the amount of damage (number of displaced atoms and volume of the resulting disordered region) depends on the incident neutron energy [15]. When these defects are created in the depleted volume of a pn junction, they behave like Shockley-Read-Hall generation centers [16]. In the case of SPADs, such radiation-induced centers are responsible for the observed DCR degradation.

It seems reasonable to assume that the probability of detecting some dark count rate increase in SPADs exposed to neutrons becomes larger as the active volume and/or the fluence increase. Experimental data in Fig. 4 a) and b), relevant to DPD SPADs, seem in line with this assumption: the devices with the largest active volume show a significant DCR increase also at the lower fluence, while at the larger fluence, all of the SPADs show a huge DCR degradation. In the case of DPH devices, in Fig. 5, the stochastic quality of neutron damage phenomena emerges instead more clearly. At the lower fluence, two among the six SPADs with the largest area show no change in DCR, whereas only one among those with 30×30 μm^2 active area exhibits no effect. Moreover, in Fig. 7 b) and c), one cell out of 24 exposed to the larger fluence features no significant degradation.

The stochastic character of neutron damage is also emphasized by the results in Figures 6 and 7, obtained for the 150 nm CMOS SPADs. The increase in DCR detected in irradiated devices can be actually treated as a random variable. Its distribution depends on the distribution of the number of neutron-silicon interactions (intrinsically a binomial distribution) and on the distribution of the non-ionizing energy released in each interaction [17], [18], [19], [20].

V. MODEL FOR SPAD DAMAGE PROBABILITY

In the following, a simple model for predicting the probability of DCR degradation in SPADs exposed to a non-monochromatic neutron source is discussed and compared with the experimental data. The model is not meant to anticipate the amount of radiation-induced damage (in terms of DCR increase). Equations modeling the statistical distribution of DCR in neutron-irradiated SPADs were presented and discussed in a paper from some of the authors of the present work [21]. The simpler model proposed here may be valuable in quickly carrying out worst-case analysis in SPAD based systems operated in radioactive environments and/or in performing consistency checks on data from neutron irradiation tests of large SPAD arrays.

A. Damage probability for a single incident neutron

At the energies of the neutron source used in this work, ranging from around 300 keV to about 3.2 MeV (see Fig.3), elastic and, to a lesser extent, inelastic scattering of neutrons with silicon lattice nuclei is the fundamental mechanism responsible for the creation of radiation-induced defects in the bulk of SPADs. The probability of interaction depends on the energy E of the impinging particle and on the density of atoms N_{at} in the target material ($N_{at} \simeq 5\times10^{22}$ cm^{-3} in silicon). The scattering probability per unit distance travelled by a neutron through the target volume is generally expressed through the macroscopic cross-section Σ_s

$$\Sigma_s(E) = N_{at}\sigma_s(E) = N_{at}\left[\sigma_{es}(E) + \sigma_{is}(E)\right]. \qquad (5)$$

In the previous equation, σ_s is the microscopic cross-section, or simply cross-section, of the target nuclei for scattering interactions, while σ_{es} and σ_{is} are the elastic and the inelastic scattering cross-sections respectively. It is worth mentioning here that the effects of neutrons are not limited to bulk damage. The energy imparted by the impinging neutron to the primary knock on atom during a collision is actually partitioned between atomic processes, which include lattice displacement, and electronic processes, which include ionization phenomena. Partitioning as a function of the recoil energy is described by the Lindhard's partition function [18]. In silicon, ionization is a transient effect, not yielding any permanent damage. It may instead lead to positive charge build up in silicon dioxide, resulting in local field modifications and affecting the main electrical parameters of CMOS transistors, such as threshold voltage, transconductance and noise, as well as SPAD operation. However, calculations show that for the neutron source used in this work, at the highest fluence, the total ionizing dose (TID) in SiO_2 is in the order of 10 rad. This result is consistent with data available in the literature for the spectrum of a reactor neutron source, covering an energy span, in the few MeV range, not dissimilar from the one of the source used in this work [22]. Such a small TID can be regarded as completely harmless for CMOS devices belonging to the 180 nm and 150 nm technology nodes, which can actually tolerate multi-megarad doses [23], and for SPADs, whose DCR was found to be only slightly affected after exposure to a 1 Mrad(SiO_2) dose [10].

As already mentioned, the increase of DCR in SPADs can be ascribed to neutron-induced defects in the device depleted

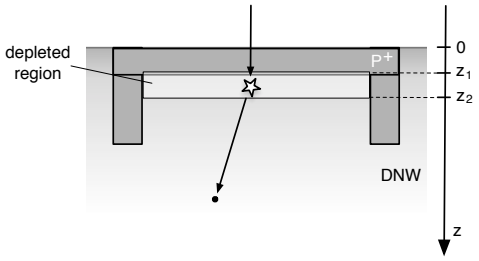

Fig. 8. Neutron interaction in the depleted region of a SPAD.

region. Fast neutrons, i.e., neutrons with energies from tens of keV to about 10 MeV (like neutrons from the source used in this work), do not lose their entire energy in a single collision, but may undergo multiple collisions before coming to a stop [24]. Actually, the large majority of the impinging neutrons will pass through the device bulk without interaction. An extremely small fraction of those interacting at least once will interact a second time. A much smaller portion of them will create a defect exactly in the depleted region, with a safely negligible probability of creating more defects in the same region after one or multiple collisions.

In the following, consistently with the setup geometry, neutrons will be assumed to hit the target perpendicularly to its surface. The probability $P_z(z)$ that a scattering event takes place between the device surface and a point at a depth z in the substrate is

$$P_z(z) = 1 - e^{-\Sigma_s z}. \tag{6}$$

Therefore, with reference to Fig. 8, the probability P_d of a neutron undergoing a scattering event, for the first time after emission, in the depleted region of the SPAD is given by

$$P_d(E, \Delta z) \simeq \Sigma_s(E)\Delta z, \tag{7}$$

where Δz=z_2-z_1. This result is obtained under the assumption that $\Sigma_s(E)z_1 \ll 1$ and $\Sigma_s(E)z_2 \ll 1$, as is the case with SPADs, featuring a shallow junction and a thin depleted region.

B. Damage probability for a given source spectrum

The probability of a single neutron at a given energy E_k not creating any defect in the SPAD depleted region is $1 - P_d(E_k, \Delta z)$. Since the scattering events are statistically independent, the probability $P_{nd}(E_k, \Delta z)$ of $N_n(E_k)$ neutrons at energy E_k not damaging the SPAD junction is given by

$$P_{nd}(E_k, \Delta z) = \left[1 - P_d(E_k, \Delta z)\right]^{N_n(E_k)}, \tag{8}$$

where $E_k = E_i + k\Delta E$ and

$$N_n(E_k) = Q_T Y_n'(E_k)\Delta\Omega\Delta E \simeq \frac{A_s}{r^2} Q_T Y_n'(E_k)\Delta E \tag{9}$$

is the number of neutrons with energy in $[E_k, E_k{+}\Delta E]$ hitting the SPAD active area A_s. According to Bernoulli statistics, the overall probability $P_{nd,T}$ of having no damage in the device active volume, accounting for the whole energy spectrum of the source, can be approximately calculated by subdividing the spectrum support $[E_i, E_f]$ into $M{=}\frac{E_f - E_i}{\Delta E}$ equal subintervals and computing the limit

$$P_{nd,T} = \lim_{\Delta E \to 0} \prod_{k=0}^{M} \left[1 - P_d(E_k, \Delta z)\right]^{N_n(E_k)}. \tag{10}$$

By taking the natural logarithm of both sides, the previous equation can be rewritten as

$$\ln(P_{nd,T}) = \lim_{\Delta E \to 0} \ln\left(\prod_{k=0}^{M} P_{nd}(E_k)\right), \tag{11}$$

where the interchange between the logarithm and the limit operator is made possible by the continuity of $\ln(x)$, under the hypothesis that the limit exists. Now

$$\ln\left(\prod_{k=0}^{M} P_{nd}(E_k)\right) = \sum_{k=0}^{M} N_n(E_k) \ln\left(1 - P_d(E_k, \Delta z)\right). \tag{12}$$

Therefore

$$\ln(P_{nd,T}) \simeq -\frac{Q_T A_s \Delta z}{r^2} \int_{E_i}^{E_f} Y_n'(E)\Sigma_s(E)dE. \tag{13}$$

Eventually, the probability $P_{d,T}$ of at least one neutron undergoing a scattering event in the active volume of the SPAD is given by

$$P_{d,T} \simeq 1 - e^{-A_s \Delta z \int_{E_i}^{E_f} \phi(E,r)\Sigma_s(E)dE}. \tag{14}$$

The probability $P_{d,T}$ can be expressed as a function of the 1 MeV neutron equivalent fluence $\Phi_{eq}(r)$,

$$\Phi_{eq}(r) = k_\phi \int_{E_i}^{E_f} \phi(E, r)dE. \tag{15}$$

In (15), $k_\phi \simeq 1.041$ is a hardness factor characteristic of the source, which can be calculated based on the displacement damage cross-section for neutrons in silicon [25]. $P_{d,T}$ can therefore be rewritten as

$$P_{d,T} \simeq 1 - e^{-\Phi_{eq}(r)\frac{A_s \Delta z}{k_\phi \int_{E_i}^{E_f} \phi(E,r)dE} \int_{E_i}^{E_f} \phi(E,r)\Sigma_s(E)dE}. \tag{16}$$

Equation (16) (as well as (14)) points to the fact that the only SPAD characteristic affecting the probability of DCR degradation is the device active volume, $A_s\Delta z$. In particular, the larger the volume, the more probable is that the DCR increases significantly after irradiation. The choice of the device active area, A_s, is generally made at the circuit design level, also in compliance with the application requirements in terms of space resolution. For a given overall detector area, a reduction in A_s, which is beneficial for the SPAD radiation tolerance, would positively impact also on the detector resolution, while adversely affecting the complexity of the readout electronics due to the increased number of elementary cells. On the other hand, the thickness Δz of the depleted region relies on the process options made available by the selected technology

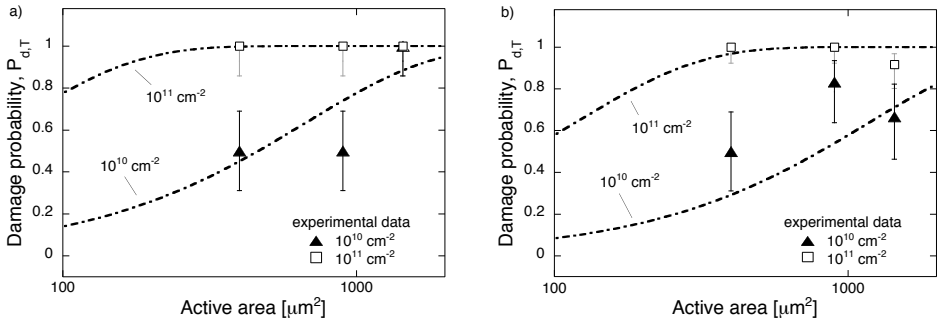

Fig. 9. Damage probability in 180 nm CMOS SPADs irradiated with different 1 MeV neutron equivalent fluences as a function of the device active area: a) DPD and b) DPH devices. Theoretical curves (lines) are compared with experimental data (symbols).

and on the relevant doping profiles. However, a thin depleted region, while reducing the probability of a neutron hit, may unacceptably degrade the detection efficiency. In addition, a thin active region may also be associated to a high electric field, and thus to a high DCR due to field-enhanced generation. Therefore, while evaluating the radiation tolerance properties of a particular SPAD structure, one should make sure that its pre-irradiation characteristics are compatible with the target application.

TABLE V
NUMBER OF IRRADIATED SPAD CELLS.

180 nm SPADs				**150 nm SPADs**		
area [μm^2]	**DPD**	**DPH** $\left(@\frac{10^{10}}{cm^2}\right)$	**DPH** $\left(@\frac{10^{11}}{cm^2}\right)$	**area [μm^2]**	**type 1**	**type 2**
20×20	6	6	12	**30×30**	32	32
30×30	6	6	12	**35×35**	32	32
36×40	6	6	12	**40×40**	32	32
-	-	-	-	**43×45**	192	192

C. Model validation

The model for the probability of DCR degradation developed in the previous sections was validated against the results from the characterization of irradiated SPADs. The number of irradiated cells for each technology and for each different device active area is summarized in Tab. V. Where not otherwise stated, for a given area, the same number of samples was tested for all the irradiation steps.

Figures 9 a) and b) show the theoretical damage probability $P_{d,T}$, computed based on (16), as a function of the device active area for DPD and DPH devices respectively (dash-dotted curves). In both figures, $P_{d,T}$ is plotted for two different values of the fluence, 10^{10} and 10^{11} 1 MeV neutron equivalent cm^{-2}. The depleted junction thickness Δz has been estimated by taking into account the measured breakdown voltage [26] (see Tab. II). A value of 0.8 μm was calculated in the case of DPD SPADs assuming a linearly graded junction model, a value of 0.5 μm was found instead in the case of DPH devices under the hypothesis of one-sided step junction. The neutron yield of the source at a 0° angle shown in Fig.3, was used for the calculation of $P_{d,T}$. Tabulated data for elastic and inelastic scattering cross-section of neutrons in silicon as a function of energy, also needed for computing $P_{d,T}$, can be found online [27].

Both in Fig. 9 a) and in Fig. 9 b), the theoretical probability curves are compared with the experimental data, represented by empty square and full triangle markers. Each point represents the fraction of SPADs featuring a post-irradiation DCR increase of at least 5% as compared to the pre-irradiation value. The 5% threshold was chosen to account for possible uncertainties in dark count rate measurements due to temperature fluctuations and Poisson counting noise. DCR was measured at an excess voltage of 1.3 V both for DPD and for DPH SPADs. The error bars (in these plots and in those of the following figures) represent the 68% confidence interval computed according to the Wilson score method [28]. This was done under the assumption that the data can be treated as a series of success-failure experiments (Bernoulli trials), where a successful experiment corresponds to a SPAD featuring a DCR increase beyond the 5% threshold. The theoretical model turns out to be in good agreement with the experimental results at the fluence of 10^{11} cm^{-2}. The less good agreement which can be detected at the smaller fluence may be ascribed to statistical fluctuations in the experimental data, due to the limited number of samples under test (see Tab. V).

Figures 10 a) and b) show the theoretical damage probability $P_{d,T}$ calculated as a function of the 1 MeV neutron equivalent fluence for type 1 SPADs with different active area (dot and dashed-dotted curves). The thickness of the depleted volume Δz used in the calculation, 0.76 μm, was computed under the hypothesis of one-sided abrupt junction. This result is consistent with the outcome of TCAD simulations performed on very similar structures fabricated in the same technology [11]. In the figures, the theoretical probability curves are compared to experimental data (full triangles), each representing, as in the case of DPD and DPH devices, the fraction of SPADs with a post-irradiation DCR increase exceeding 5% of the pre-irradiation value at the different fluences. DCR was measured at an excess voltage of 2 V. In all the plots, a fairly good agreement between theoretical curves and experimental data can be detected.

In Figures 11 a) and b), the theoretical damage probability $P_{d,T}$ is plotted as a function of the 1 MeV neutron equivalent fluence for type 2 SPADs (dashed-dotted curves). As

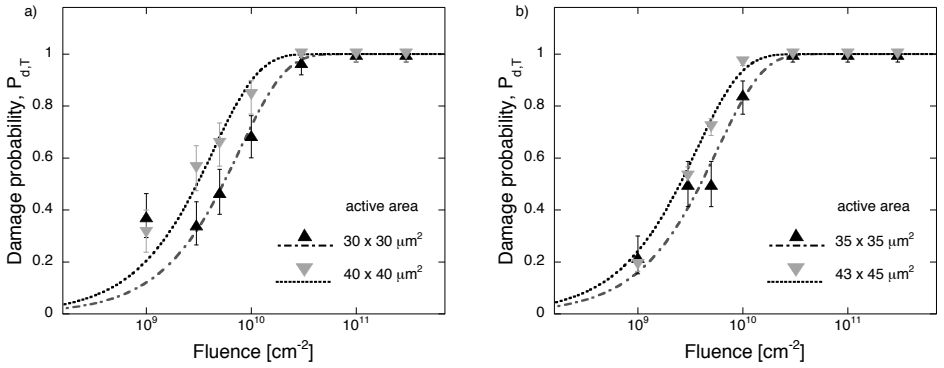

Fig. 10. Damage probability in type 1 150 nm CMOS SPADs as a function of the fluence. Theoretical curves (dot and dash-dot lines) are compared with experimental data (symbols). The two figures refer to SPADs with different active area: a) 30×30 μm^2 and 40×40 μm^2, b) 35×35 μm^2 and 43×45 μm^2.

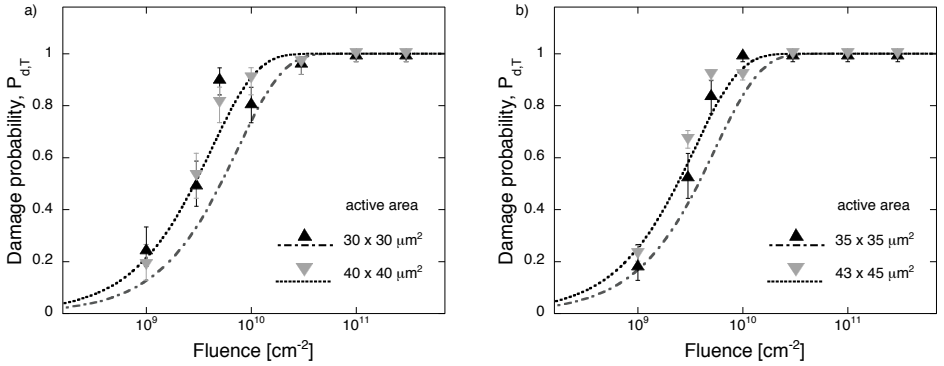

Fig. 11. Damage probability in type 2 150 nm CMOS SPADs as a function of the fluence. Theoretical curves (dot and dash-dot lines) are compared with experimental data (symbols). The two figures refer to SPADs with different active area: a) 30×30 μm^2 and 40×40 μm^2, b) 35×35 μm^2 and 43×45 μm^2.

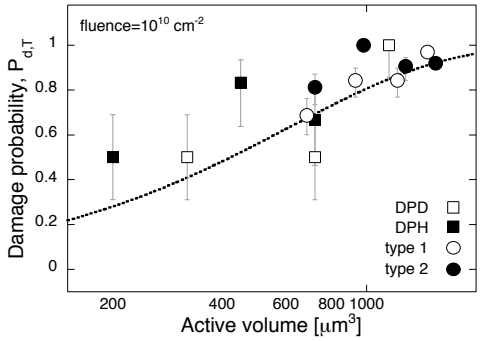

Fig. 12. Damage probability as a function of the active volume at a fluence of 10^{10} cm^{-2}. The theoretical curve is compared with the experimental data relevant to the four kinds of SPADs investigated in this work.

in Fig. 10, the plots refer to devices with different active area, from 30×30 μm^2 to 43×45 μm^2. The thickness of the depleted volume Δz used for the calculation of the theoretical probability, 0.8 μm, was computed under the assumption of linearly graded junction. As for type 1 devices, a similar result was obtained from TCAD simulations of P-well/N-iso SPADs [11]. In the figures, the calculated probability curves are compared to experimental data, represented by full triangle markers. DCR was measured at an excess voltage of 2 V. Again, experimental data are found to be in quite a good agreement with the values predicted by (16).

Fig. 12 shows the damage probability as a function of the active volume at a fluence of 10^{10} cm^{-2}. The theoretical curve (dotted line), based on (16), is compared to the experimental data (markers) relevant to the four kinds of SPADs tested in this work. While the overall behavior of the irradiated devices is in good agreement with the trend of the damage probability with the sensitive volume, the model seems to slightly underestimate the characterization results. One should refrain from using Fig. 12 to compare the different SPADs to each other in terms of radiation tolerance, since data may be strongly affected by statistical fluctuations, as already pointed out in particular for 180 nm devices. Indeed, the developed model indicates that two SPADs with the same active volume, exposed to the same neutron fluence, are supposed to feature the same damage probability, regardless of the fabrication technology.

It is worth emphasizing once again here that (16) represents the probability of having at least one neutron scattering event in the active volume of the SPAD for a given device geometry and for a given spectrum of the source. The good agreement of the model with the experimental data, representing the fraction of SPADs showing some amount of DCR degradation points to the fact that, with a very good approximation, any neutron interaction in the sensitive volume of a SPAD leads to an at least 5% increase in DCR. The breakdown voltage, used to extract the thickness of the depleted region, is indeed the only SPAD electrical parameter employed by the model. A more

accurate knowledge of the device electrical characteristics affecting DCR, such as the shape and the strength of the fields in the depleted region and possibly related field enhancement and tunneling effects [29], might be needed in case one wanted to estimate the amount (and not just the probability) of DCR degradation induced by neutrons, which is actually beyond the scope of this paper.

VI. Conclusion

The effects of neutrons from a non-monochromatic source on CMOS SPADs fabricated in two different technologies have been investigated paying particular attention to dark count rate degradation. The stochastic nature of neutron interaction with silicon is emphasized by the relatively low fluences and by the small size of the active volumes involved in the irradiation experiments. At a given fluence, in large populations of SPADs, like in detection systems based on sensor arrays, quite a large spread in DCR increase can be observed after irradiation. A statistical model for computing the damage probability in SPADs exposed to a neutron source with a given energy spectrum has also been presented and discussed. The theoretical prediction, based on the geometrical features of the devices under test and on the spectrum of the emitting source, was demonstrated to be in good agreement with measurement results. The developed model provides the designers with useful indications on how to minimize the susceptibility of SPADs to neutrons from the standpoint of DCR. Study of the effects of other particles, like protons and electrons, on SPAD devices, may shed some light on the DCR degradation mechanisms at play. Possible relationships of the studied effects with those detected in different typologies of devices, such as CMOS imagers, might also be worth investigating.

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