A Hybrid Single-Inductor Bipolar-Output DC–DC Converter With Floating Negative Output for AMOLED Displays

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***Abstract*— This article presents a hybrid single-inductor bipolar-output (SIBO) dc–dc converter for active-matrix organic light-emitting diode (AMOLED) displays, which are relatively more sensitive to the supply noise on the positive supply. First, to improve the display quality we adopt a floating negative output configuration to migrate all the switching ripples into the negative output, achieving a near-zero voltage ripple on the positive output. Second, we design low-power shunt regulators, which only deal with a small portion of the output ripple, to regulate the positive output voltage further, improving the load transient response. Besides, the hybrid topology and the proposed cross-coupled bootstrap-based level-shifter, with a dual-PMOS inverter buffer, only uses standard CMOS devices without deep-n-well, reducing the chip area and cost. The proposed converter, implemented in 0.35-μm CMOS with 5-V devices, operates at 1 MHz, leading to a measured positive output voltage ripple lower than 1 mV (all conditions). It achieves a measured 3-mV undershoot voltage and, an unnoticeable overshoot voltage on the positive output, when the output current varies between 30 and 350 mA. The measured peak power efficiency is 89.3% at 1.1-W output power. The maximum output power is 3.5 W.**

***Index Terms*— AMOLED display, bipolar output, dual-PMOS inverter, floating negative output, hybrid converter, shunt regulator, single-inductor multiple-output (SIMO).**

I. Introduction

IN RECENT years, active-matrix organic light-emitting diode (AMOLED) displays have been extensively used in various applications for their high energy efficiency and superior display quality features [1]–[10]. To drive the strings of the AMOLEDs requires a tunable high voltage close to 10 V. To be compatible with the analog control voltage domain, bipolar supply rails are usually necessary, with a fixed positive voltage supplying the current sources for pixel-level color control. A programmable negative supply voltage controls the display output power for brightness. Therefore, having a dc–dc converter with bipolar output voltages becomes important.

The typical two thin-film transistors (TFT) one storage capacitor (2T1C) pixel-level driving circuit of AMOLED displays is shown in Fig. 1. The switching TFT, STFT, allows the storage capacitor, C_{ST}, to store the data voltage, V_{DATA}. The driving TFT, DTFT, operates as a current source and converts the data voltage to the right amount of current to drive the OLED. As shown in Fig. 1, the voltage variation on the positive supply rail, V_P, changes the gate–source voltage of the TFT current source, notably affecting the display quality. On the other hand, the negative supply rail, V_N, changes the drain–source voltage of the TFT current source. Therefore, a high-quality AMOLED display requires a clean V_P from the SIBO converter with fast line/load transient response, good line/load regulation, and a small switching ripple. Indeed, power efficiency is also an essential factor for thermal management and for extending the battery life.

In conventional solutions, [1] and [2] integrated two separate dc–dc converters, one boost converter and one inverting flyback converter, on a single chip to provide the bipolar supply rails. This solution benefits from the short time-to-market but suffers from a bulky size and high cost due to the two power inductors. Several SIBO converters emerged in recent years [3]–[10] to shrink the device size and lower the cost. In [3]–[7], the SIBO converters operate with three phases, as in Fig. 1. V_P is charged with boost mode, and V_N is charged with inverting flyback mode, respectively. Compared to the SIBO converter operated with two phases and charging V_P and V_N simultaneously with inverting flyback mode [8], the inductor current ripple can be reduced and the efficiency can be improved. Similar to the ordered power distributive control (OPDC) in single-inductor multiple-output (SIMO) converters [11], [12], the SIBO converter shown in Fig. 1 uses a comparator to regulate V_P with a higher priority, while uses a PI controller to regulate V_N. The advantages of the

Manuscript received October 19, 2020; revised January 28, 2021; accepted February 20, 2021. Date of publication March 9, 2021; date of current version August 26, 2021. This article was approved by Associate Editor Piero Malcovati. This work was funded in part by The Science and Technology Development Fund (FDCT), Macao SAR (File no. 0093/2019/A2 and SKL Operating Fund), and the Research Committee of University of Macau under grant MYRG2018-00102-AMSV. *(Corresponding author: Yan Lu.)*

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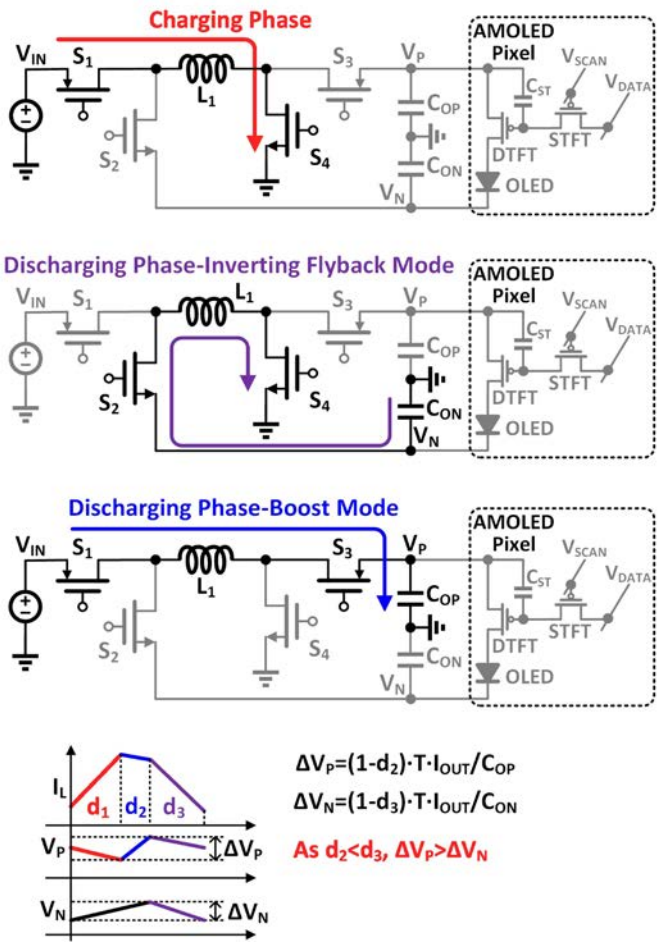

Fig. 1. Typical 2T1C pixel-level driving circuit of AMOLED displays, the conventional SIBO converter with a three-phase operation scheme and its relevant waveforms.

OPDC include fast transient response and no cross-regulation for V_P, which are quite favorable for the AMOLED displays. However, this control scheme results in a positive voltage ripple larger than the negative. Mao *et al.* [9] present a two-phase SIBO converter that simultaneously transfers energy to the positive and negative outputs, extending the positive output's charging duration, and thus reducing the output ripple to a certain extent. In [9], a current-mode pulsewidth modulation (PWM) controller regulates the positive output. Thus, improving the line and load regulations of this SIBO converter. However, the transient response severely degrades, and the measured undershoot/overshoot can be as large as 292 mV/430 mV when a load transient happens. Finally, the regulation of the negative output in [9] requires a temporary phase that decreases or increases the energy delivered to the positive output, causing a cross-regulation issue.

To overcome the drawbacks from prior arts, we propose a hybrid SIBO converter with floating negative output and shunt regulators [10]. In the design, the shunt regulators only deal with a tiny portion of the total ripples and consume low power, reducing the output ripple and improving the transient response. When the input voltage of the proposed SIBO converter is higher than 3 V, the maximum output current is larger than 200 mA. Thus, it can be used to supply AMOLED displays up to 7 in, such as smartphone or small tablet screens.

The organization of the remaining of the article is as follows. Section II introduces the architecture and operation principle of the proposed SIBO converter. Section III shows the circuit implementation of the critical blocks and simulation results. Section IV presents and discusses the measurement results. Finally, Section V draws the conclusions.

II. Proposed Hybrid SIBO Converter With Floating Negative Output

A. System Architecture and Operation Scheme

Fig. 2 shows the proposed hybrid SIBO converter's system architecture with floating negative output and shunt regulators. It includes four power transistors, S_1–S_4, one Schottky diode, D_1, one power inductor, L_1, one flying capacitor C_{FLY}, one output capacitor, C_O, and one filtering capacitor, C_{OP}, for the positive output, V_P. As shown in Fig. 2, all the power transistors, buffers, and control circuits are integrated on the chip. In the proposed topology, most of the output variations affect the negative output, V_N. Ideally, the positive output can be very clean without using a fast control loop like the OPDC. Unlike previous works [1]–[8], only the positive output V_P has an output capacitor C_{OP} serving as an anchor while V_N, V_{X1}, and V_{X2} are floating. To accommodate the nonideal effects, the shunt regulators fine-tune V_{P}. The main output capacitor C_O stabilizes $V_P - V_N$.

As V_N is floating, the three-phase operation scheme, which charges V_P and V_N separately, is not applicable here. Therefore, we adopt a two-phase operation scheme. S_1 through S_4 are on-chip power switches, and V_{DR1} through V_{DR4} are the corresponding gate driving signals. D_1 is an off-chip Schottky diode. To overcome the large inductor current ripple in the two-phase operation, an added flying capacitor, C_{FLY} [5], forms a hybrid SIBO converter. The C_{FLY} used in this work decreases the inductor current ripple, and reduces the voltage stress across the power switches, allowing us to use a standard 5-V CMOS process, and increasing the power efficiency. Besides, we use a cross-coupled bootstrap-based level-shifter (CCBB-LS) and a dual-PMOS inverter buffer, to avoid the need for the deep N-well.

Fig. 3(a) and (b) displays the charging and discharging phases of the proposed SIBO converter, respectively. Here, R_L represents the AMOLED pixel array. V_{X1}, V_{X2}, and V_{X3} are the switching nodes. The charging phase refills C_{FLY}, thus energizing the inductor. In the discharging phase, all the circuit nodes, except V_P, are floating. If we ignore the parasitic capacitors, all the inductor current I_{L} will flow into C_O and establish V_P–V_N directly, with no current flows into or out of C_{OP}. Therefore, C_{OP} operates as an anchor capacitor defining the voltage of V_P. Ideally, there should be no voltage variation on V_P. Fig. 3(c) plots the relevant waveforms and equations for ΔV_P and ΔV_N. In practice, a parasitic capacitor C_{PN} exists on the node V_N, as highlighted in Fig. 4. Consider C_{PN} is in series with C_{OP}, and then in parallel with C_O, providing another current path. Therefore, the voltage variation on C_O

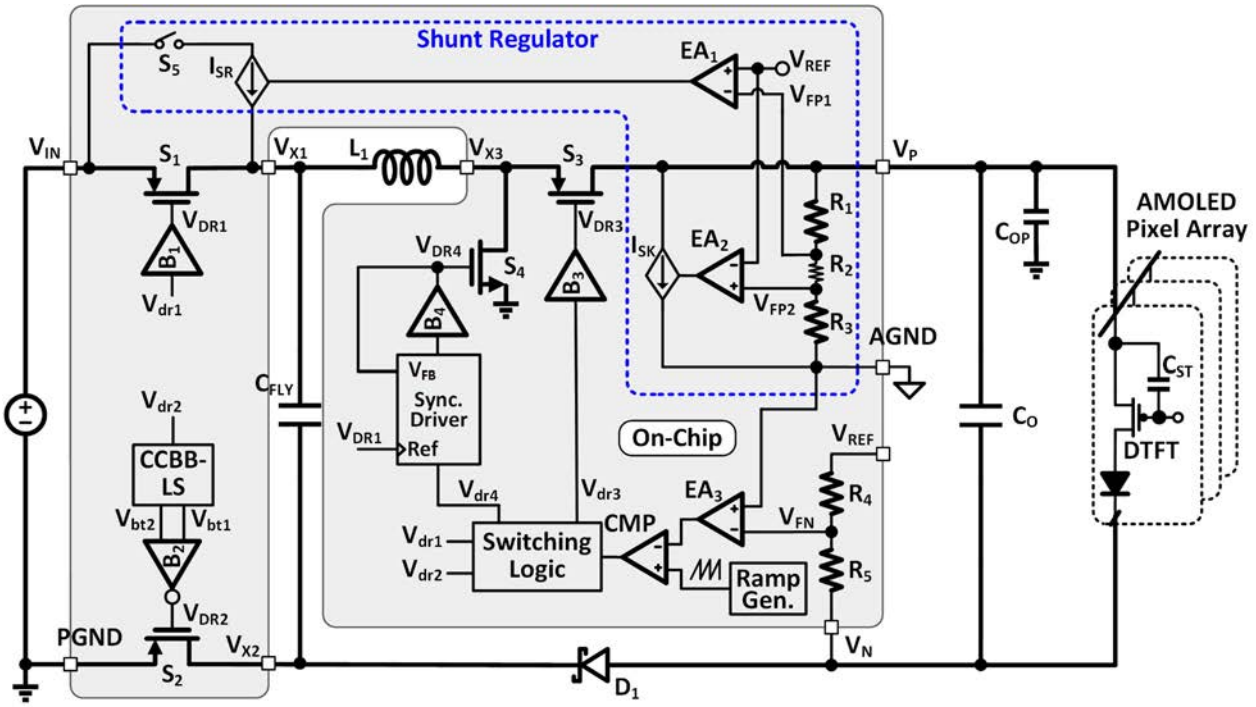

Fig. 2. System architecture of the proposed hybrid SIBO converter with floating negative output.

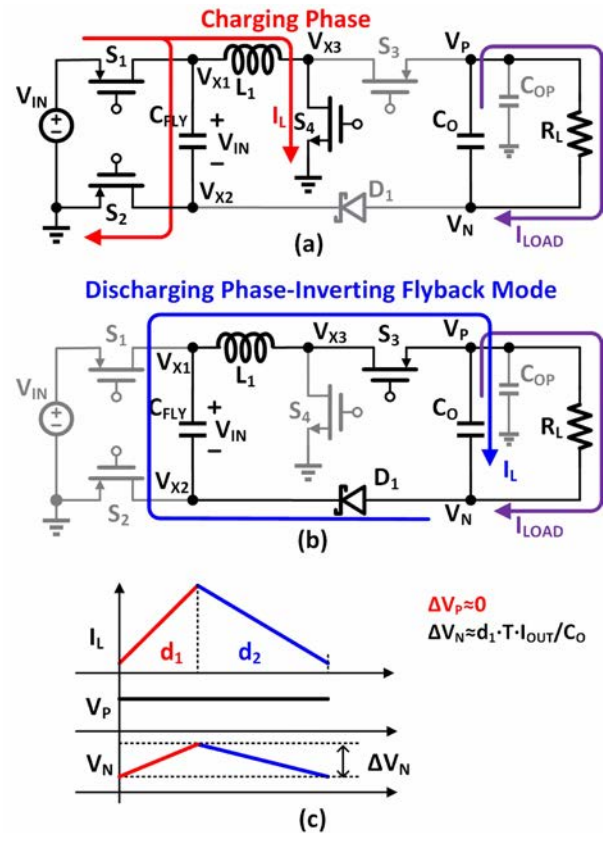

Fig. 3. (a) Charging phase and (b) discharging phase of the proposed SIBO converter. (c) SIBO converter with C_{PN} and (c) its waveforms.

is distributed to V_P and V_N, according to the C_{PN}/C_{OP} ratio. We can set C_{OP} to be thousands of times larger than C_{PN}, making, therefore, ΔV_P almost zero.

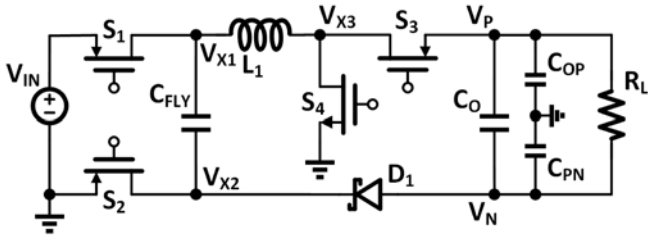

Fig. 4. SIBO converter with C_{PN}.

B. Unbalanced Charge Injection of C_{OP}

Besides the C_{PN}-caused V_P ripple mentioned above, three other mechanisms may cause charge to unbalance on C_{OP}, resulting in V_P variations, and thus require extra care.

1) *C_{OP} Charge Injection from Switch Timing Mismatch:* During the transition between the two phases, it is impossible to turn ON/OFF S_1, S_2, and S_4 simultaneously, due to the control circuit and buffers' delay mismatches. S_2 turns-on slightly later, and turns-off slightly earlier, remaining off during the phase transitions. Thus, we only need to consider the synchronization issue between S_1 and S_4.

Fig. 5 exhibits the unwanted charge or discharge currents to C_{OP}, when there are S_1 and S_4 timing mismatches. During Δt_1, S_1 is ON, and S_4 is OFF. The unwanted charge current I_{UCC} flows from V_{IN} into C_{OP} through the body diode of S_3, causing unexpected voltage variation on V_P. Similarly, the unwanted discharge current I_{UDC} exists during Δt_2, with S_1 being OFF and S_4 being ON.

When V_{DR1} is leading V_{DR4}, I_{UCC} appears during the transition from the discharging phase to the charging phase, and I_{UDC} occurs during the charging to discharging phase transition. When V_{DR1} lags behind V_{DR4}, it is the other way

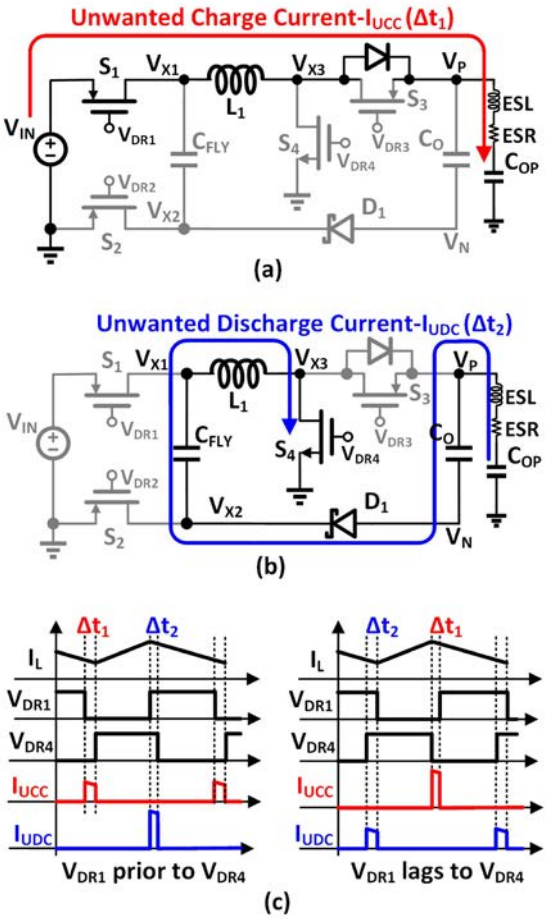

Fig. 5. Circuit configurations when (a) unwanted charging current and (b) unwanted discharging current happens, and (c) relevant waveforms when V_{DR1} is prior to or lags to V_{DR4}.

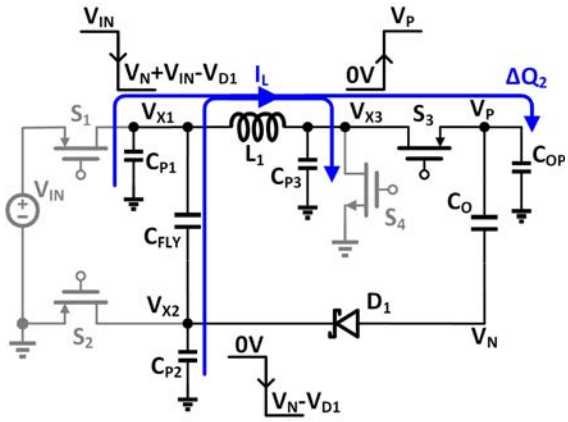

Fig. 6. Charge injection of C_{OP} caused by the parasitic capacitors of the switching nodes.

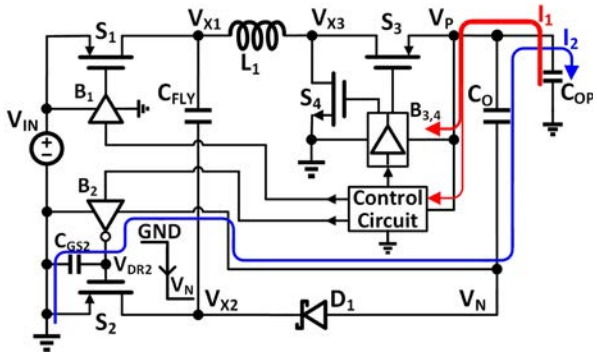

Fig. 7. Charge injection of C_{OP} caused by the supply current of the control circuit and buffers.

around. As Δt_1 and Δt_2 are much smaller than the operation period, then $I_{UCC} \approx I_{VALLEY}$ and $I_{UDC} \approx I_{PEAK}$, where I_{VALLEY} and I_{PEAK} are the valley and peak values of I_L, respectively. The C_{OP} charge injection caused by I_{UCC} and I_{UDC} in each cycle, ΔQ_1, becomes

$$\Delta Q_1 \approx \Delta t_1 I_{VALLEY} - \Delta t_2 I_{PEAK}. \quad (1)$$

ΔQ_1 can be positive or negative, and accumulates over cycles, causing V_P voltage ripple and dc voltage shift. To minimize $|\Delta Q_1|$, we use an additional synchronous control loop, which considers the S_1 gate-drive signal V_{DR1} as a reference, to generate the gate-drive signal for S_4. Then, in the steady state, V_{DR4} synchronizes with V_{DR1}. Section III-B discusses the detailed schematic and operation of the synchronous operation.

2) C_{OP} Charge Injection From the Parasitic Capacitors: Besides the timing mismatches between S_1 and S_4, the parasitic capacitors at the switching nodes will also cause charge injection to C_{OP}. In Fig. 6, during the phase transition from charging phase to discharging phase, V_{X1} switches from V_{IN} to $(V_{IN} + V_N - V_{D1})$, V_{X2} switches from the ground to $(V_N - V_{D1})$, and V_{X3} switches from the ground to V_P, respectively, where V_{D1} is the D_1 diode voltage drop. C_{P1}, C_{P2}, and C_{P3} are the parasitic capacitors on V_{X1}, V_{X2}, and V_{X3}, respectively. There will be a charge transfer between the parasitic capacitors and C_{OP} during the phase transitions. The amount of injected charge ΔQ_2 on C_{OP} in each cycle is $(C_{P1}+C_{P2}) \times |V_N - V_{D1}| - C_{P3}V_P$. In this design, the estimations of $C_{P1}+C_{P2}$ and C_{P3} are 275 and 168 pF, respectively. With these values, ΔQ_2 is positive. Furthermore, the resulting ripple on V_P is $\Delta Q_2/C_{OP}$, which is <0.5 mV with a C_{OP} of 1 μF. The same as ΔQ_1, ΔQ_2 also accumulates over cycles.

3) C_{OP} Charge Injection From the Gate-Drivers and Control: From Fig. 7, the third source of V_P variation derives from sourcing and sinking the gate-drive currents. Here, we use V_P to supply the control block and the gate-drive buffers of S_3 and S_4, by sourcing current I_1. Furthermore, V_P also sinks current I_2 from the gate-drive buffer of S_2. The total C_{OP} charge injection, ΔQ_3, caused by I_1 and I_2 in each cycle is

$$\Delta Q_3 = \int_0^T (I_2 - I_1) dt. \quad (2)$$

ΔQ_3 is favorably negative as the total size of S_3 and S_4 is several times larger than S_2, and as the current consumption of the control block is much smaller than the gate-drive currents.

Above all, the total C_{OP} charge injection in one cycle, ΔQ_T, is

$$\Delta Q_T = \Delta Q_1 + \Delta Q_2 + \Delta Q_3. \quad (3)$$

Here, as the synchronous driver minimizes ΔQ_1, ΔQ_T is mainly determined by ΔQ_2 and ΔQ_3, both tightly related to

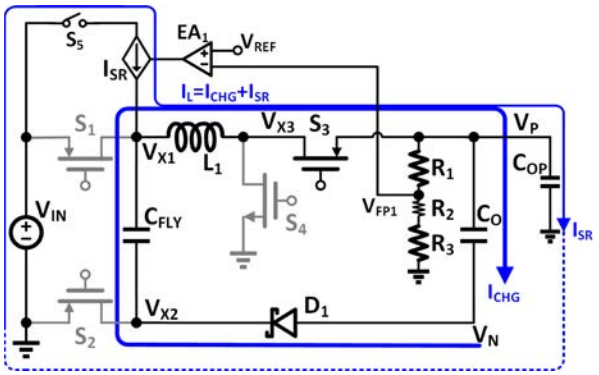

Fig. 8. Proposed solution for the C_{OP} charge compensation and V_P voltage regulation.

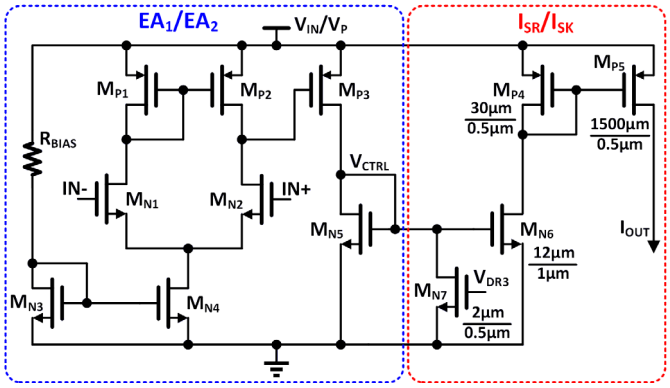

Fig. 9. Schematic of EA_1 or EA_2 and a current mirror output stage driving I_{SR} or I_{SK}, respectively.

the power transistor sizes. In this design, $|\Delta Q_3| > |\Delta Q_2|$, and thus ΔQ_T is negative, indicating that the supply V_P should come from a small auxiliary shunt regulator, discussed next.

C. Charge Compensation and Output Voltage Regulation

Fig. 8 presents our solution to compensate for the C_{OP} charge injection, with a fast response shunt regulator. As V_{IN} is provided by a Li-ion battery, it ranges from 2.7 to 4.5 V, and is lower than V_P. So, the shunt regulator cannot directly supply current to V_P from V_{IN}. Therefore, we move the voltage-controlled current source I_{SR} to the left side of L_1, crossing the voltage gap with L_1. In the SIBO converter discharging phase, the switch S_5 turns on, I_{SR} flows through L_1, S_3, C_{OP}, ground, and V_{IN}, forming a closed loop. In the other current loop, I_{CHG} charges C_O and provides power to the load. The sum of I_{SR} and I_{CHG} equals the inductor current I_L. Here, it is worth to note that I_{SR} is only a small portion of I_L and will not affect the power delivered to the load. During the charging phase, S_5 is OFF, and I_{SR} is zero.

As Fig. 2 shows, besides the current source I_{SR}, there is a current sink I_{SK} connected to V_P preventing V_P of being overcharged during the startup process. Unlike a conventional converter, the load current in the proposed SIBO converter it does not discharge V_P even in overcharge. Here, the error amplifier EA_1 controls I_{SR}, targeting a V_P of 5.3 V. With V_P overcharged, the current sink I_{SK} controlled by EA_2 will pull V_P back to 5.33 V quickly. Since V_P also provides currents to the controller and gate drivers, it will be pulled down below 5.3 V slowly by those currents. A small resistor R_2 inserted between R_1 and R_3 that generates a 30-mV offset for EA_1 and EA_2 avoids I_{SR} and I_{SK} to conduct simultaneously.

As the shunt regulator controls V_P, then the voltage across C_O determines V_N. Therefore, regulating V_N means regulating the total output voltage, $V_P - V_N$. To this end, this work uses a typical voltage-mode type-II PWM controller.

III. Circuit Implementation and Simulation Results

A. Shunt Regulators

Fig. 9 illustrates the schematic of the error amplifiers, EA_1 and EA_2, and the current mirror output stage driving the

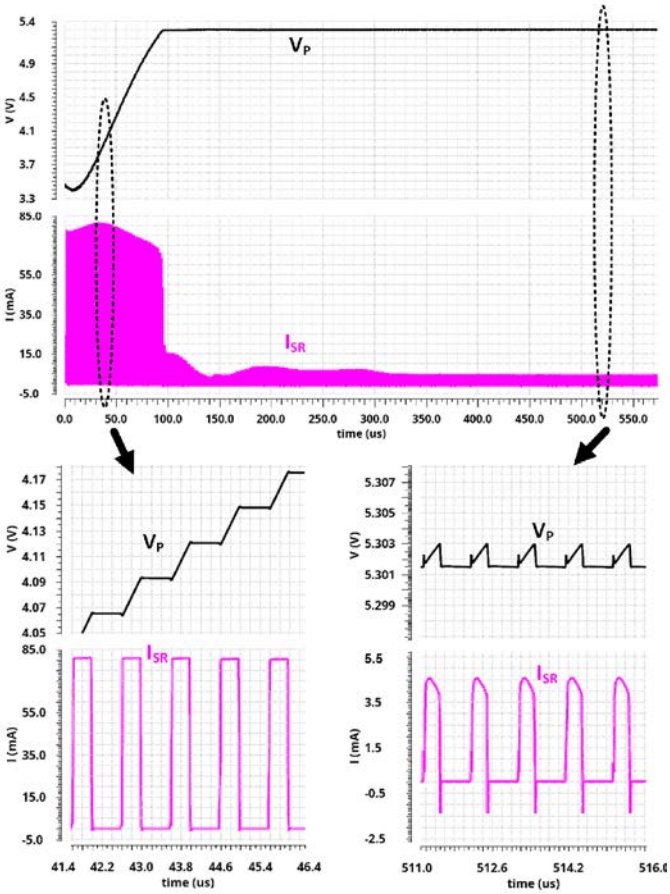

Fig. 10. Simulated regulation process of V_P when $V_{IN} = 3.7$ V and $I_{LOAD} = 100$ mA.

current source/sink, I_{SR}, and I_{SK}, respectively. V_{IN} supplies EA_1 and I_{SR}, while V_P supplies EA_2 and I_{SK}. Here, instead of using S_5 in series with I_{SR}, there is M_{N7} that performs the function of S_5 to disable I_{SR} in the SIBO converter charging phase. In such a way, we can cut off the current mirror output stage and the I_{SR} together with a small-sized transistor. M_{P5} in Fig. 9 is the output transistor, and a current ratio of 50 with M_{P4} is selected to provide a high enough compensation current in each cycle with an acceptable silicon area.

Fig. 10 plots the simulated regulation process of V_P when $V_{IN} = 3.7$ V and $I_{LOAD} = 100$ mA. In the beginning, V_P is

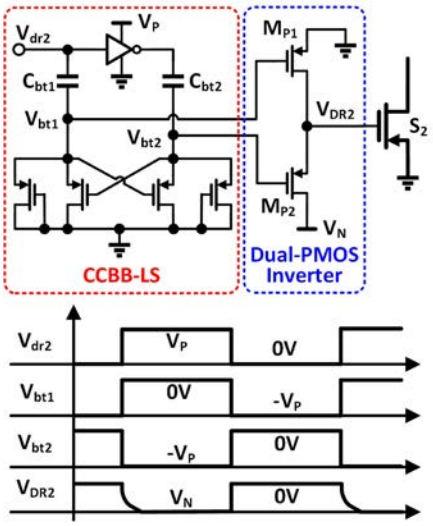

Fig. 11. Schematic of the CCBB-LS and the dual-PMOS inverter buffer, and the voltage waveforms.

much smaller than the targeted 5.3 V. So, I_{SR} is quite large, and V_P increases rapidly. When V_P is close to 5.3 V, I_{SR} drops quickly. When the shunt regulator becomes stable, 5.3 V regulates V_P and I_{SR} will be small.

B. CCBB-LS and Dual-PMOS Inverter Buffer

The control of the power PMOS S_2 is a negative voltage for the turn on and a zero voltage for the turn off. Fig. 11 presents the designed cross-coupled bootstrap-based level shifter (CCBB-LS) and a dual-PMOS inverter buffer B_2 to alleviate the device voltage stress and eliminate the need for DNWs. The CCBB-LS supplied by V_P generates differential driving signals, V_{bt1} and V_{bt2}, swinging from $-V_P$ to 0 V, without using high-voltage (HV) devices nor DNWs. Besides, the gate-drive buffer with two P-type transistors, M_{P1} and M_{P2}, can drive the large power transistor S_2 without using DNWs, reducing the required bootstrap capacitance ($C_{bt1} = C_{bt2} = 20$ pF and are integrated on chip in this work). When V_{DR2} swings from 0 V to V_N, the V_{GS} of M_{P2} keeps decreasing, and the falling edge is relatively slow. Because we only use S_2 to charge C_{FLY}, which is a hard-charging process, the slow turn on of S_2 does not affect power efficiency.

C. Synchronous Driver for S_4

In Fig. 12, we have the block diagram of the synchronous driver for S_4. It consists of two delay-locked loops (DLLs), of which the upper is for the turn on timing tuning and the lower is for the turn off timing tuning. During the operation, we detect the turn on and turn off timing of S_1 and S_4 by the ON/OFF-detection blocks first, compared afterward by the phase detectors (PDs). After that, the charge pumps (CPs) integrate and convert the phase difference to the analog control voltages, V_{ON} and V_{OFF}, and feed them to the voltage-controlled delay lines (VCDLs). Finally, the rising edge and falling edge of V_{dr4} delay accordingly, achieving a synchronized V_{DR4}. V_{IN} supplies the synchronous driver and buffer B_1, while V_P supplies the buffer B_4.

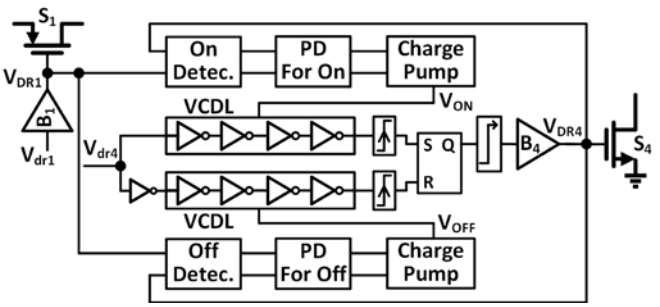

Fig. 12. Block diagram of the synchronous driver for S_4.

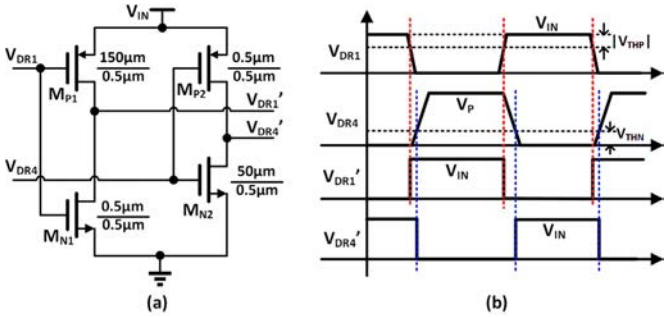

Fig. 13. (a) Schematic of the ON/OFF detection circuit and (b) corresponding waveforms.

As $V_{IN} < V_P$, we use a level shifter to connect the synchronous driver and B_4.

Fig. 13 draws the on-detection and off-detection circuits with the same schematic, plus the corresponding waveforms. In general, S_1 turns ON/OFF when its gate–source voltage V_{GS} is smaller/larger than V_{THP}, and S_4 turns ON/OFF when its V_{GS} is larger/smaller than V_{THN}, where V_{THP} and V_{THN} are the threshold voltages of PMOS and NMOS, respectively. In Fig. 13(a), the width of M_{P1} is much larger than that of M_{N1}. Thus, both the falling and rising edges of V_{DR1}' are very close to the points where $V_{DR1} - V_{IN} = V_{THP}$. Therefore, we can regard them as the ON and OFF timing of S_1, respectively. Similarly, the falling and rising edges of V_{DR4}' can be the ON and OFF timing of S_4, respectively.

The CP and VCDL circuits used in this work are the same as those in [13]. We carefully design them to work correctly within the supply voltage range.

Fig. 14(a) plots the simulated waveforms before the proposed gate drivers get synchronized, where I_{S1} and I_{S4} are the currents flowing through S_1 and S_4, respectively, and I_{COP} is the current flowing into C_{OP}. Here, by observing the rising/falling edges of I_{S1} and I_{S4}, the exact turn on/turn off timing of S_1 and S_4 can be determined, respectively. In Fig. 14(a), the rising edge of I_{S4} appears prior to that of I_{S1} by 4 ns, and the falling edge of I_{S4} appears prior to that of I_{S1} by 8 ns. As a result, I_{UDC} happens when S_4 is turned on, and S_1 is off; I_{UCC} happens when S_4 turns off, and S_1 is on. The control voltages for VCDL, V_{ON}, and V_{OFF} are then charged up by a small step to delay the rising and falling edges of V_{DR4}, respectively. When the synchronous gate driver of S_4 gets stable, V_{DR1} and V_{DR4} get synchronized. As shown in Fig. 14(b), the rising/falling edge of I_{S4} is almost coincident

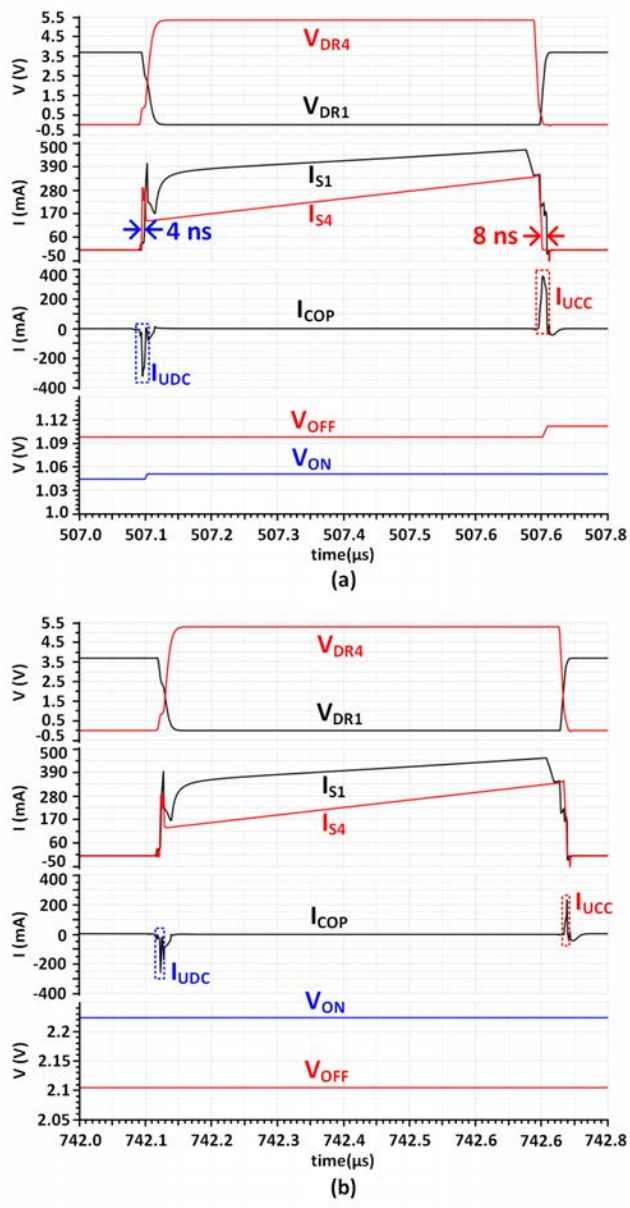

Fig. 14. Simulated waveforms of the synchronous driver (a) before the steady state and (b) in the steady state when $V_{\rm IN} = 3.7$ V and $I_{\rm LOAD} = 100$ mA.

with the one of I_{S1}. The narrow pulse of $I_{\rm UDC}$ and $I_{\rm UCC}$ shows that $V_{\rm DR1}$ and $V_{\rm DR4}$ are not perfectly synchronized due to the mismatch of the trip point of the ON-/OFF-detection circuit. Nonetheless, it is much narrower than what Fig. 14(a) presents, indicating the minimization of ΔQ_1 in (3).

IV. Measurement Results

The proposed hybrid SIBO converter, fabricated in a 0.35-μm CMOS process with 5-V devices, occupies a chip area of 3.68 mm^2, and the proposed shunt regulator only occupies 0.035 mm^2. Fig. 15 shows the chip micrograph of the SIBO converter. It operates at 1 MHz with a power inductor of 10 μH, a flying capacitor of 4.7 μF, a C_O of 10 μF, and a $C_{\rm OP}$ of 1 μF. The SIBO converter works with an input voltage ranging from 2.7 to 4.5 V. The targeted V_P and V_N are 5.3 and -4.7 V, respectively.

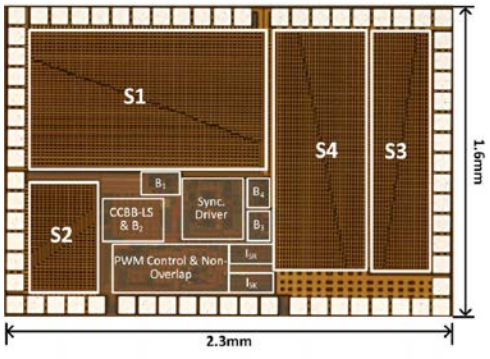

Fig. 15. Chip micrograph of the proposed SIBO converter.

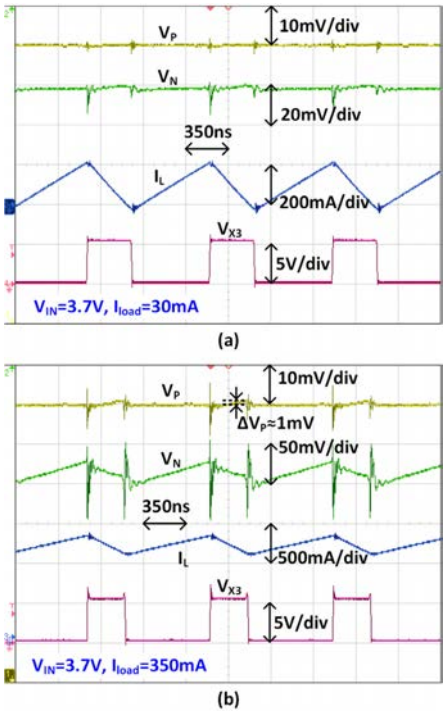

Fig. 16. Measured waveforms of V_P, V_N, I_L, and V_{X1} when $V_{\rm IN} = 3.7$ V, and (a) $I_{\rm LOAD} = 30$ mA and (b) $I_{\rm LOAD} = 350$ mA, respectively.

Fig. 16 plots the measured waveforms with 3.7-V input and load currents of 30 and 350 mA, respectively. The bandwidth of the voltage probe is 20 MHz. Besides the small ringing glitches observed during the phase transition, probably caused by the probe loop inductance, the voltage ripples on V_P are always lower than 1 mV for a load current $I_{\rm LOAD}$ ranging from 30 to 350 mA. On the other hand, the ripples on V_N are the expected overall output voltage ripple of the bipolar outputs related to the load current. We observe a maximum V_N ripple of 30 mV in the heavy load condition. Fig. 17 displays the measured waveforms with a 4.2-V input voltage.

Fig. 18 shows the measured load transient response when $I_{\rm LOAD}$ varies between 30 and 350 mA, with a slope of 250 mA/μs. Due to the floating negative output topology and the fast response shunt regulator, the undershoot voltage on V_P is only 3 mV, and the overshoot voltage is unnoticeable, as most of the output variations migrate to V_N.

TABLE I

COMPARISON WITH THE PRIOR WORKS

	[3]		[4]		[5]		[6]		[7]		This Work	
Process	0.5µm Power BiCMOS		0.5µm BCD		0.5µm BCD		90nm 8V devices		0.18µm BCD		0.35µm 5V devices	
Chip Area (mm^2)	4.1		5.75		7		N/A		1.16		3.68	
Frequency (MHz)	1		1.25		1.25		0.5		1.5		1	
Inductor (µH)	4.7		4.7		4.7		10		4.7		10	
Flying Cap (µF)	4.7		4.7		4.7x2		N/A		N/A		4.7	
Max Eff.	82.3% @ 0.33W		87.1% @ 0.6W		89% @ 0.6W		90.1% @ 0.11W		88% @ 0.6W		89.3 % @1.1W	
Input Range	2.7~4.5V		2.7~4.5V & 5V		2.7~3.7V		3.0~4.2V		2.5~4.5V		2.7~4.5V	
Max Power (W) @ V_{IN} = 3.7V & Eff.> 80%	0.5		2.4		2.6		0.22		1.4		3.5	
Output Voltage (V)	V_P	V_N	V_P	V_N	V_P	V_N	V_P	V_N	V_P	V_N	V_P	V_N
	4.58	-6.24	4.6	-5.4	4.6	-5.4	4.8	-2.5	5	-5	5.3	-4.7
Output Cap (µF)	4.7+4.7		10+10		10+10		10+10		4.7x3+4.7x3		10+1	
Line Regulation (mV/V)	6	18	13.8	7.6	15.6	9.7	1.25	2.5	N/A	N/A	18	2
Load Regulation (mV/mA)	0.25	1	0.12	0.2	0.27	0.35	0.03	0.06	N/A	N/A	0.1	0.06
Output Ripple(mV)	@ 100mA		@ 300mA		@ 200mA		@ 20mA		@ 60mA		@ 30~350mA	
	80**	30**	50	60	80	65	17	50	20	20	≤ 1	≤ 30

*: Capacitors in compensation network are not included.

**: Ripples at heavy load condition estimated from measurement waveforms.

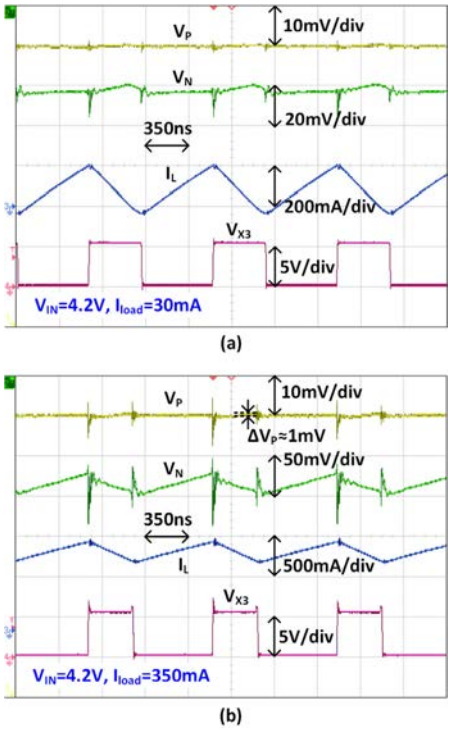

Fig. 17. Measured waveforms of V_P, V_N, I_L, and V_{X1} when $V_{IN} = 4.2$ V, and (a) $I_{LOAD} = 30$ mA and (b) $I_{LOAD} = 350$ mA, respectively.

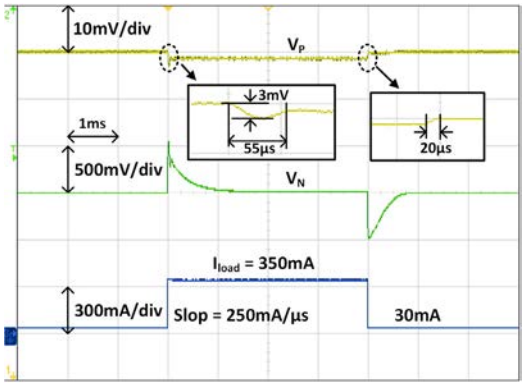

Fig. 18. Measured load transient waveforms with $V_{IN} = 4.2$ V.

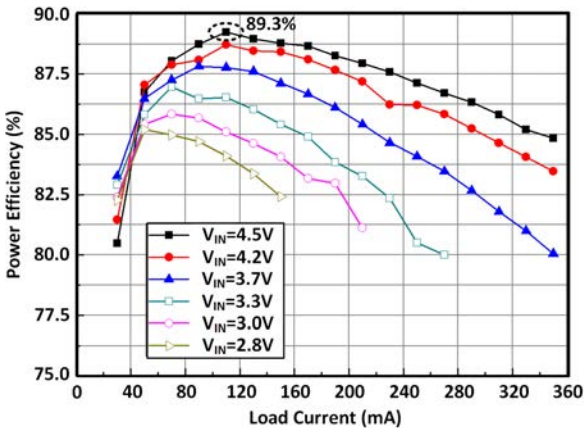

Fig. 19. Measured power conversion efficiencies as a function of the load current for different input voltages.

Fig. 19 exhibits the measured power conversion efficiencies with different input voltages and load currents. There is a peak efficiency of 89.3% when the input voltage is 4.5 V, and the output power is 1.1 W. The measured efficiency remains above 80% even at the 30-mA light load condition, proving that the shunt regulators do not introduce significant conduction losses.

Table I compares the proposed SIBO converters with the prior works. By only using 5-V devices, this work achieves the highest output power with a small chip area. We obtain a negligible ripple on V_P and the smallest total ripple on the bipolar outputs, with smaller filtering capacitors.

V. Conclusion

AMOLED displays have more stringent requirements on its positive supply than the negative supply. That is because the positive supply affects the V_{GS} of the pixel current source, while the negative only determines the V_{DS} of the current source. This article presented a hybrid SIBO converter with a floating negative output voltage for high-quality AMOLED displays. With careful considerations on the charge injection to the positive output, a shunt regulator regulated the positive output voltage, while we applied a voltage mode PWM controller to regulate the negative output. The hybrid converter topology and the proposed CCBB-LS do not require HV devices nor DNW, thus reducing the chip area and cost. Measurement results verified the near-zero voltage ripple on the positive output and a fast load transient response. The peak power conversion efficiency is 89.3% with an output power of 1.1 W. The maximum output power is 3.5 W.

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