Analog Front End of 50-Gb/s SiGe BiCMOS Opto-Electrical Receiver in 3-D-Integrated Silicon Photonics Technology

Farhad Bozorgi, Melchiorre Bruccoleri, Elham Rahimi, Matteo Repossi, Francesco Svelto, *Fellow, IEEE*, and Andrea Mazzanti, *Senior Member, IEEE*

***Abstract*— This work presents a 3-D-integrated opto-electrical receiver (RX) analog front end (AFE) operating up to 50 Gb/s. The electronic integrated circuit (EIC) is fabricated in ST SiGe BiCMOS-55-nm technology and flipped and mounted on top of the ST photonic integrated circuits (PICs) die through copper pillars (Cu-Pi). In the RX chain, a low-power fully differential shunt-feedback trans-impedance amplifier (FD SF-TIA) is exploited to reduce the input-referred noise. Following the TIA, a postamplifier (PA) based on a novel active feedback circuit topology extends the bandwidth (BW) and a buffer delivers the output electrical signal to the 100-Ω differential off-chip load. An automatic offset cancellation loop is included to protect the RX from any offset source at the input. The RX AFE consumes 56 mW from 1.8-V supply voltage and provides a trans-impedance (TI) gain of 78.7 Ω with 27-GHz BW. By exploiting the FD SF-TIA with low parasitic capacitance of the germanium photodiodes (Ge-PD) in the photonic die as well as BW recovery by the PA, the RX achieves the sensitivity of −7.5-dBm OMA at Ge-PD and −2.3-dBm OMA at the single-mode fiber (SMF) optical output with bit error rate (BER) of $<10^{-12}$ and PRBS-7. To the author's best knowledge, among published state-of-the-art 50-Gb/s TIAs and RX exploiting SiGe BiCMOS technologies, this work proves the best energy efficiency ((pJ/bit)) and figure of merit (FoM) ((Gbps/μA.mW)) in terms of sensitivity and power consumption.**

***Index Terms*— 3-D-integrated, active feedback, limiting amplifier (LA), opto-electrical receiver (RX), trans-impedance amplifier (TIA).**

I. Introduction

HUGE amount of data generated by various breakthrough applications, such as cloud computing, mobile communications, and the Internet of Things, has pushed the ICT domain into the zettabyte era. The majority (around 77%) of the data traffic is exchanged within data centers [1] where optical transceivers are the most suitable technology for interconnection between different clusters in the 10 m–10 km range [2]. Most of the current optical transceivers are based on discrete optical components. However, as data rate increases and data centers expand, size, power, and cost reductions of such components are critical. This is particularly true for communication systems exploiting wavelength-division multiplexing (WDM), requiring bulky and expensive optical multiplexing/de-multiplexing devices [3]. Silicon photonic technology allows monolithic integration of optical and electrical components on a single chip, though at the cost of some limitations in the design of the electronic circuits on photonic substrates or vice versa. This poses limitations in either electronic or photonic IC design. To circumvent the issue, 3-D integration is a promising approach [4]. As shown in Fig. 1(a), the 3-D assembly can be exploited to maximize the flexibility in technology selection for the design of the electronic integrated circuit (EIC), which is then connected through copper pillars (Cu-Pi) on top of a photonic integrated circuit (PIC), where miniaturized optical components can be manufactured at low cost. It should be noted that in current commercial silicon photonics technologies, optical components, such as grating couplers, entail larger insertion loss than discrete technologies (VCSEL, DML, and so on). However, research results on silicon photonics to address the loss issue are ongoing and results are promising [5]. This work presents a 3-D-integrated two-channel WDM opto-electrical receiver (RX) operating up to 50 Gb/s/channel with the focus on the analog front end (AFE), in particular TIA and postamplifier (PA). The AFE has to provide low power and high sensitivity with enough gain and bandwidth (BW) to deliver an error-free (BER $<10^{-12}$) large-signal electrical output. To characterize the RX AFE (or TIA), the following figure of merit (FoM) has been introduced [6]:

$$\text{FoM} = \frac{\text{DR(Gbps)}}{I_{\text{in,min}}(mAp - p)\,.\,\text{Power(mW)}} \tag{1}$$

where DR is the maximum data rate, $I_{\text{in,min}}$ is the minimum detectable current at the TIA input to reach the error-free detection, and power is the power consumption. The higher the data rate, the more BW is required, which intrinsically leads to higher integrated noise and power dissipation. The TIA plays a key role to maintain high sensitivity. The two most

Manuscript received January 18, 2021; revised May 12, 2021 and June 29, 2021; accepted June 30, 2021. Date of publication July 19, 2021; date of current version December 29, 2021. This article was approved by Associate Editor Hui Pan. This work was supported by the European Union Horizon H2020 Program (H2020-ICT27-2015) under Grant COSMICC 688516. *(Corresponding author: Farhad Bozorgi.)*

Farhad Bozorgi was with the Department of Industrial and Information Engineering, The University of Pavia, 27100 Pavia, Italy. He is now with the Barkhausen Institut, 01187 Dresden, Germany (e-mail: farhad.bozorgi@barkhauseninstitut.org).

Melchiorre Bruccoleri is with STMicroelectronics, 20010 Milan, Italy.

Elham Rahimi is with Silicon Austria Labs, 4040 Linz, Austria.

Matteo Repossi is with STMicroelectronics, 27100 Pavia, Italy.

Francesco Svelto and Andrea Mazzanti are with the Department of Industrial and Information Engineering, The University of Pavia, 27100 Pavia, Italy.

Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSSC.2021.3094995.

Digital Object Identifier 10.1109/JSSC.2021.3094995

commonly employed TIA topologies are the common base (gate) [7], [8] and the shunt-feedback TIA (SF-TIA) [9]. The common-base TIA offers very wide BW and robust operation, and however, noise of the load and the biasing elements is directly referred to the input, which makes it challenging to reach high sensitivity. Better performance is possible with the SF-TIA, provided that the gain-BW product of the open-loop amplifier is sufficiently high. By leveraging the high cutoff frequency of CMOS nodes, such as FinFet 14/16 nm [10]–[12], the SF-TIA realized with a simple inverter amplifier is enough to target high RX sensitivity up to 65 Gb/s. In less advanced (and cheaper) technologies, shunt and/or series inductive peaking [13], [14] may be exploited to extend BW. However, besides the large area and the extra parasitic capacitance introduced by on-chip inductors, inductive peaking alone hardly satisfies the required BW extension if very low noise is targeted at 50 Gb/s. The two-stage TIA presented in [15] and [16] is an interesting approach in which the BW of the SF-TIA is deliberately limited to reduce the input-referred noise and a PA with high-frequency peaking is introduced to recover the BW. As proved in [15], scaling down the TIA BW by n allows R_F to be scaled up by n^2. This may decrease the white noise of R_F and subsequent stages by n^2 and n^4, respectively.

The RX in this work combines the two-stage front-end approach with an FD SF-TIA. Leveraging the low parasitic capacitance of the SiGe photodiode in the photonic IC, the implemented differential SF-TIA yields a remarkable noise reduction compared to a single-ended (SE) SF-TIA. The TIA architecture, originally introduced in [9] without a formal performance analysis, was explored at 25 Gb/s in [17]. This article presents a thorough analysis and comparison of feedback TIA implementations and extends the FD SF-TIA concept to higher data rate. In the complete front end, after the TIA, a PA with active feedback extends the BW and rises the overall gain. Realized in a SiGe BiCMOS-55-nm technology without resorting to peaking inductors, the complete RX meets the BW for 50 Gb/s with a record energy efficiency and FoM [see (1)] against previously reported RX in BiCMOS technologies. This article is organized as follows. In Section II, the opto-electrical RX system architecture and 3-D assembly are discussed. Section III introduces and analyzes the proposed SF-TIA, while Section IV describes the design of the RX circuits. Experimental results are reported in Section V and the conclusion is drawn in Section VI.

II. Photonic IC and RX Architecture

Fig. 1(a) and (b) shows the cross section and top view of the 3-D-integrated opto-electrical RX presented in this work. Two individual optical data streams with the wavelengths of 1310 and 1330 nm can be multiplexed and carried on a single-mode fiber (SMF). The SMF is surface coupled into the PIC through a 2-D polarization splitting grating coupler (PSGC). The PSGC is followed by an integrated wavelength-division de-multiplexer. The two outputs of the demux are coupled to germanium photodiodes (Ge-PD) through integrated optical waveguides. The simulated and measured optical transfer functions of the optical demux are

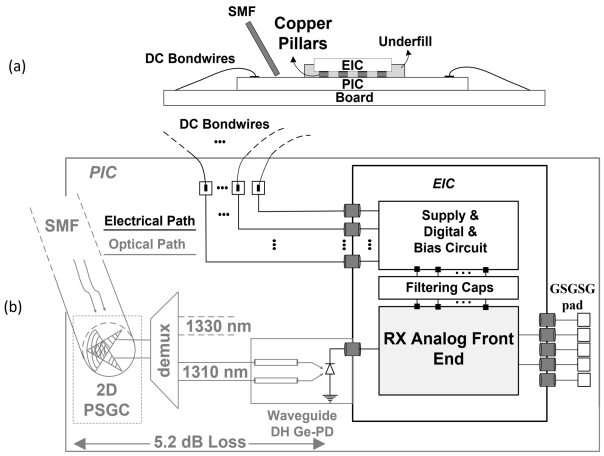

Fig. 1. (a) Cross section and (b) top view of the 3-D integrated of a 3-D assembly opto-electrical RX.

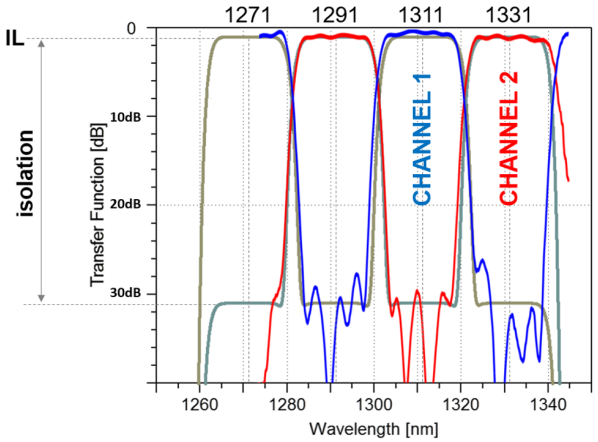

Fig. 2. Demux transfer function versus optical input wavelength in simulation (gray line) and measurement.

plotted in Fig. 2. The demux features bandpass filtering at two different wavelengths: 1310 and 1330 nm. The filters have wide and flat response ($\simeq$15 nm) with low intra-channel ripple ($<$1 dB) and low losses ($<$2 dB). The isolation between the two channels is around -30 dB, low enough to limit crosstalk between the two channels.

Under 1-V reverse bias, each Ge-PD converts the optical power into an electrical current with 1 A/W responsivity. Confirmed by measurements on separated optical components that were fabricated alone for testing, the total optical power loss from fiber output to the Ge-PD is 5.2 dB (1.5 dB from the optical demux and 3.7 dB from the PSGC and integrated optical waveguide). Two identical and independent AFE in the EIC receive the transduced signal from the Ge-PDs through Cu-Pi and deliver the conditioned electrical signal to the output pads, sensed by a GSGSG differential probe for testing purposes. The supply voltage and reference currents provided by the test board enter into the PIC die through bondwires and are then transferred with Cu-Pi to the EIC.

The block diagram of the RX AFE is shown in Fig. 3. The output of the Ge-PD is SE and connected to one input of the differential SF-TIA in the EIC. A Cherry–Hooper (CH)

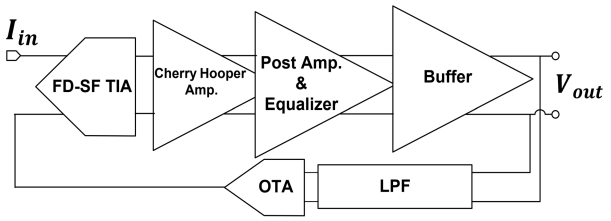

Fig. 3. RX AFE block diagram.

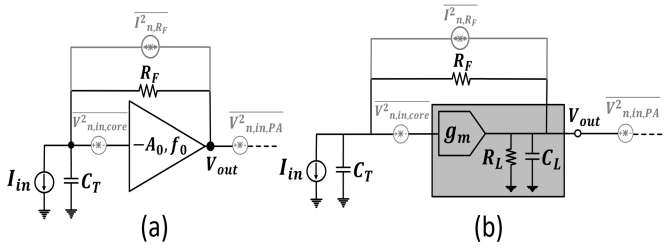

Fig. 4. SE SF TIA model with (a) ideal voltage amplifier and (b) g_m-cell.

amplifier follows the TIA and drives the PA. The latter provides further amplification with high-frequency peaking to compensate for the TIA BW and reach an overall BW wide enough to support 50 Gb/s. Finally, a differential buffer drives the output pads. DC offsets are nulled with a low-frequency feedback loop. As shown in Fig. 3, an OTA, after a first-order RC low-pass filter (LPF) senses the differential output offset voltage and feeds a correcting dc current to the ac grounded input of the differential SF-TIA.

III. SE and Differential SF-TIAs

This section reviews the performance of the SF-TIA and analyses the benefit of a fully differential implementation. First, the gain, BW, and noise tradeoffs are evaluated in the classical SE SF-TIA with an ideal voltage amplifier. Then, the impact of replacing the voltage amplifier with a transconductor is considered. Finally, the fully differential (FD) SF-TIA topology is introduced and its advantages are analytically quantified.

A. Single-Ended SF-TIA

The schematic of the SE SF-TIA modeled with a voltage amplifier is drawn in Fig. 4(a). A_0 and f_0 are the voltage gain and BW of the voltage amplifier (with gain–BW product GBP $= A_0 f_0$). The current source I_{in} represents the photodiode current, R_F is the feedback resistance, and C_T is the total capacitance at the input node, comprising the photodiode capacitance (C_{PD}) and the equivalent input capacitance of the amplifier (C_{in})

$$C_T = C_{\text{in}} + C_{\text{PD}}. \tag{2}$$

Assuming that $A_0 \gg 1$, a second-order trans-impedance (TI) transfer function can be easily derived as

$$Z_T = \frac{V_{\text{out}}}{I_{\text{in}}} \simeq \frac{\frac{A_0\omega_0}{C_T}}{S^2 + \left(\omega_0 + \frac{1}{R_F C_T}\right)S + \frac{A_0\omega_0}{R_F C_T}} \tag{3}$$

with dc gain $R_T \simeq R_F$. For a maximally flat response, the amplifier BW must satisfy

$$f_0 = \frac{1}{2\pi}\frac{2A_0}{R_F C_T} \tag{4}$$

leading to a closed-loop BW

$$BW \simeq \frac{1}{2\pi}\frac{\sqrt{2}A_0}{R_F C_T}. \tag{5}$$

From (3)–(5), an upper bound on the feedback resistance (known as TIA limit) [9], [18] is found

$$R_F \le \frac{A_0 f_0}{2\pi\, BW^2 C_T}. \tag{6}$$

Considering the thermal noise of R_F, $\overline{V^2_{n,RF}}$, the equivalent input noise of the core amplifier, $\overline{V^2_{n,\text{in,core}}}$, and the equivalent noise of the cascaded PA, $\overline{V^2_{n,\text{in,PA}}}$, the power spectral density of the equivalent input-referred noise current is

$$\overline{I^2_{n,\text{in}}} = \frac{4kT}{R_F} + \frac{\overline{V^2_{n,\text{in,core}}}}{R_F{}^2}\left(1 + \omega^2 R_F{}^2 C_T{}^2\right) + \frac{\overline{V^2_{n,\text{in,PA}}}}{R_F{}^2}. \tag{7}$$

The analysis so far assumed an ideal voltage amplifier. Realization of such an amplifier requires a low-impedance output buffer, which rises noise and power consumption and limits BW and voltage swing. As shown in Fig. 4(b), the implementation of the SF-TIA with a simple transconductor (g_m) and a load resistor (R_L) is typically preferred. In this case, the following TI transfer function can be derived:

$$Z'_T \simeq \frac{\frac{g_m}{C_L C_T}}{S^2 + \left(\frac{1}{R_L C_L} + \frac{1}{R_F C_L} + \frac{1}{R_F C_T}\right)S + \frac{g_m}{R_F C_L C_T}} \tag{8}$$

where C_L is the load capacitance. The gain and BW of the open-loop amplifier, drawn inside the gray box in Fig. 4(b), are $A_0 = g_m R_L$ and $\omega_0 = 2\pi f_0 = (1/R_L C_L)$. By defining $\alpha = 1 + (R_L/R_F)$, the required amplifier BW to have a maximally flat closed-loop frequency response is

$$f_0 = \frac{1}{2\pi}\frac{2A_0}{\alpha^2 R_F C_T} \tag{9}$$

leading to a closed-loop BW and a TIA limit expressed by

$$BW \simeq \frac{1}{2\pi}\frac{\sqrt{2}A_0}{\alpha R_F C_T} \tag{10}$$

$$R_F \le \frac{A_0 f_0}{2\pi\, BW^2 C_T}. \tag{11}$$

Notably, while f_0 and BW depend on the parameter α (i.e., on the R_L & R_F), the TIA limit remains the same as previously derived for the case of a voltage amplifier. Since $A_0 f_0 = (g_m/C_L)$, the TIA limit in (11) can be rewritten as

$$R_F \le \frac{g_m}{(2\pi)^2 BW^2 C_T C_L}. \tag{12}$$

Considering the primary noise sources in Fig. 4(b), the power spectral density of the equivalent input noise current for the g_m-based SF-TIA has roughly the same expression derived for the implementation with a voltage amplifier given by (7). If the transconductor is implemented with a simple

common-emitter BJT, the two most relevant noise sources are thermal noise of the extrinsic base resistance, r_b, and the collector current shot noise. Then, the equivalent input noise of the core amplifier is

$$\overline{V^2{}_{n,\text{in,core}}} = 4kTr_b + \frac{2kT}{g_m}. \tag{13}$$

Replacing (13) in (7), the dominant input-referred white noise current power spectral density of the g_m-based TIA can be expanded as

$$\overline{I^2{}_{n,\text{in}}} = \frac{4kT}{R_F} + \frac{4kTr_b}{{R_F}^2} + \frac{2kT}{g_m {R_F}^2} + \frac{\overline{V^2{}_{n,\text{in,PA}}}}{{R_F}^2}. \tag{14}$$

From (14), increasing R_F (i.e., the TIA gain) results into lower input-referred noise and higher sensitivity. However, the maximum R_F is bounded by the TIA limit given by (12). By replacing (12) into (14), the noise power can rewritten as

$$\overline{I^2{}_{n,\text{in}}} = \lambda \cdot 4kT\sigma + \lambda^2 \cdot \left(4kTr_b + \frac{2kT}{g_m}\right)\sigma^2 + \lambda^2 \cdot \overline{V^2{}_{n,\text{in,PA}}}\sigma^2 \tag{15}$$

where

$$\sigma = 2\pi \cdot BW \cdot C_L \tag{16}$$

$$\lambda = \frac{BW}{\left(\frac{g_m}{2\pi C_T}\right)} = \frac{BW}{f_T^*}. \tag{17}$$

In (17), $f_T^* \leq f_T$, where f_T is the cutoff frequency of the transistor in the transconductor. f_T^* is equal to f_T if the PD capacitance is negligible, compared to the TIA input capacitance. From (15) to (17), the equivalent input noise power spectral density is reduced by decreasing σ, i.e., targeting a lower BW (and then using a PA with peaking for BW extension), or by reducing λ, which means increasing f_T^* for given BW. It is worth noticing that increasing the current to rise g_m of the transistor does not necessarily improve the noise performance. In fact, the transistor size has to be increased, to maintain the optimal current density, leading to a proportional increase of the parasitic capacitance at the input (C_T) and output (C_L). According to (14)–(17), larger C_T and C_L impairs the effect of higher g_m on the SE TIA noise performance. As a result, self-loading sets a bound on the noise performance improvement that can be reached by simply increasing the power consumption. The implementation of a fully differential SF-TIA, presented in Section III-B, is a viable technique to reduce the equivalent input noise below the level achieved by the SE architecture.

B. Fully Differential SF-TIA

The fully differential shunt-feedback trans-impedance amplifier (FD SF-TIA) is drawn in Fig. 5. It is realized around an FD transconductor and the unused input is ac grounded by a large capacitor (CB). Compared with the SE SF-TIA in Fig. 4(b), assuming that the amplifier (enclosed in the gray area in Fig. 5) is a differential pair with resistor loads, the transconductance of the stage is $g_m/2$ and the differential load resistance and capacitance are $2R_L$ and $C_L/2$.

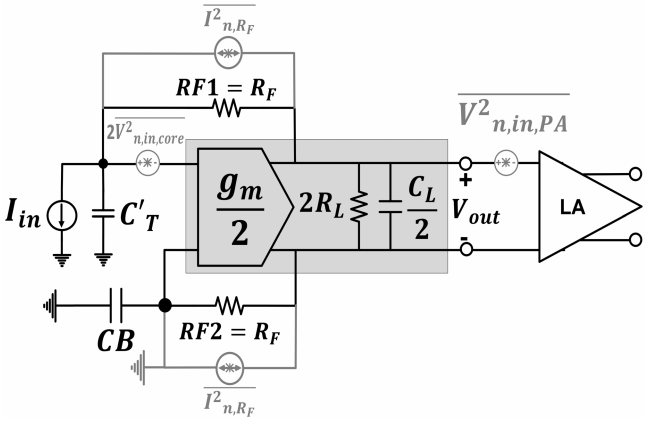

Fig. 5. FD SF-TIA small-signal model.

The open-loop gain, A_0, and BW, f_0, are the same as for the s.e. transconductor considered in the SE SF-TIA.

Due to the differential structure, the equivalent input capacitance of the amplifier is halved, and thus, the total capacitance shunting the current source I_{in} in Fig. 5 is now

$$C'_T = C_{\text{PD}} + \frac{C_{\text{in}}}{2}. \tag{18}$$

From circuit analysis, the TI of the FD SF-TIA is

$$Z'_T \simeq \frac{\frac{g_m}{C_L C'_T}}{S^2 + \left(\frac{1}{R_L C_L} + \frac{1}{R_F C_L} + \frac{1}{R_F C'_T}\right)S + \frac{g_m}{2R_F C_L C'_T}}. \tag{19}$$

Equation (19) differs from (8) by the factor $1/2$ in the last term at denominator because the in-band gain is twice the R_F, compared to the SE SF-TIA

$$R_T \simeq 2R_F. \tag{20}$$

Following the same approach as in the previous case, the limit for the feedback resistance, R_F, that gives maximum TI gain with maximally flat response is:

$$R_F \leq \frac{g_m}{2(2\pi)^2 BW^2 \mathbf{C'_T} C_L} = R_{F,\max}. \tag{21}$$

By combining (9), (10), and (21), the value of R_L to have maximally flat response is found

$$R_L = \frac{R_F}{2\pi\sqrt{2} \cdot BW \cdot R_F \cdot C_L - 1}. \tag{22}$$

If the PD capacitance is negligible compared to the amplifier input capacitance, C'_T in (18) is nearly one half of C_T given by (2). Hence, the denominator of (21) would be equal to (11), proving that the maximum feedback resistance in the FD SF-TIA is the same as in the SE implementation. This allows to effectively double the TI gain [see (20)] for the same BW reducing the equivalent input noise and sensitivity. In the FD SF-TIA, the noise sources of the core amplifier are doubled, and however, capacitor CB shunts the noise of RF2 to ground and, with the potential of doubling the gain, the total noise power when referred to the input is finally reduced. From circuit analysis, the equivalent input-referred

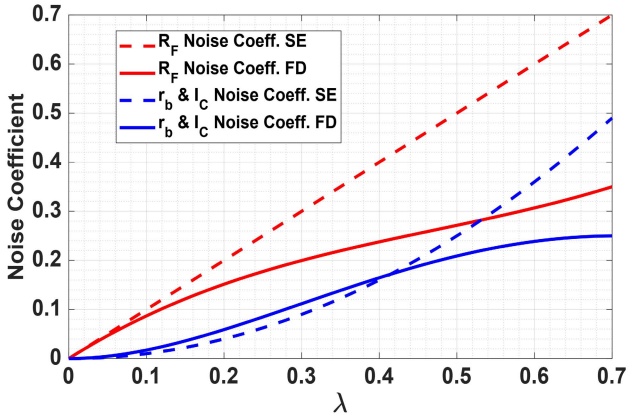

Fig. 6. Noise coefficient of R_F, r_b, and I_C in FD and SE SF-TIA versus λ.

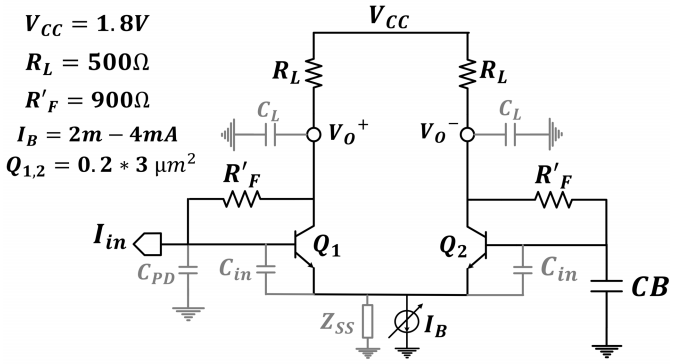

Fig. 7. Circuit schematic of the implemented FD SF-TIA.

noise power spectral density for the FD SF-TIA can be written as

$$\overline{I^2_{n,\text{in}}} = \lambda \frac{1+\left(\frac{R_F}{R_F+R_L}\right)^2}{2} \cdot 4kT\sigma + \lambda^2 \frac{\left(1+\frac{R_F}{R_F+R_L}\right)^2}{2} \cdot \left(4kTr_b + \frac{2kT}{g_m}\right)\sigma^2 + \frac{1}{4}\lambda^2 \cdot \overline{V^2_{n,\text{in,PA}}}\sigma^2. \quad (23)$$

Comparing (23) with (15), valid for the g_m-based SE SF-TIA, for the same BW, the FD SF-TIA yields $\sim 4X$ reduction of the post TIA amplifier's white noise (last term). By replacing R_F and R_L given by (21) and (22), (23) can be rewritten as

$$\overline{I^2_{n,\text{in}}} = \lambda\left(1-\sqrt{2}\lambda+\lambda^2\right) \cdot 4kT\sigma + \lambda^2\left(\sqrt{2}-\lambda\right)^2 \cdot \left(4kTr_b + \frac{2kT}{g_m}\right)\sigma^2 + \frac{1}{4}\lambda^2 \cdot \overline{V^2_{n,\text{in,PA}}}\sigma^2. \quad (24)$$

The first term in (15) and (24) represents the feedback resistor (R_F) noise power in SE and FD SF-TIA, respectively. Likewise, the second term is related to the core amplifier's input transistor noise, including base resistance (r_b) noise and collector current shot noise (the noise associated with the g_m of the TIA). Fig. 6 shows the coefficients of the two terms versus λ for both SE and FD SF-TIAs. It can be seen that in both cases, the lower λ (i.e., the higher f_T^* compared to the target BW), the lower equivalent input noise power. However, if f_T^* is comparable to BW, which could be the case when targeting high data rate and low power consumption, the dominant R_F noise contribution is remarkably reduced in the FD SF-TIA. The second term contributions (the transistor noise) in both structures are nearly the same up to $\lambda = 0.4$ and are suppressed in FD for higher λ.

IV. RX Design

The circuit implementation of the RX is described in this section. Fig. 7 shows the schematic of the FD SF-TIA. A low BW, compensated by peaking in the PA, improves sensitivity by reducing λ. Hence, BW= 16 GHz (nearly 1/3 of the 50-Gb/s maximum data-rate) is selected. The transistors are HBTs with emitter area of $0.2*3$ μm^2. The Ge-PD equivalent capacitance is 15 fF and the estimated parasitic capacitance of Cu-pi that connects the PD to the TIA is 5 fF. The equivalent input capacitance of the core amplifier is around 82 fF and dominates the input pole. The supply voltage is $V_{CC} = 1.8$ V and the programmable tail bias current, I_B, is nominally set to 3 mA. $R_F = 900\ \Omega$ and $R_L = 500\ \Omega$ are selected according to (21) and (22).

The analysis in Section III assumed an ideal tail current source, with infinite output impedance. Considering a finite equivalent impedance of the current source, Z_{SS} in Fig. 7, the TIA gain changes to

$$R'_T = \frac{1+2g_mZ_{SS}}{2+2g_mZ_{SS}} \cdot \frac{2R_L(g_mR_F-1)}{2+g_mR_L}. \quad (25)$$

With the selected component values $g_mR_L = 20$ ($\gg 2$), then the above equation is well approximated by

$$R'_T = \frac{\text{CMRR}}{1+\text{CMRR}} \cdot 2R_F \quad (26)$$

where CMRRR is the common-mode rejection ratio of the differential amplifier. Therefore, with respect to (20), the in-band gain is reduced by (CMRR/1 + CMRR). From simulations, the CMRR of the core amplifier in the TIA is 23 dB at 1 GHz, leading to a gain reduction of 0.6 dB compared to the case of an ideal current source. The finite impedance of the tail current source slightly changes also the relative contributions of the different noise sources in the TIA. Fig. 8 shows the results of noise simulations with an ideal and the real (MOS transistor) current source. With finite current source, the impedance part of its noise is transferred to the output, but the noise contributed by R_F, r_b, and the core amplifier transistors are slightly reduced. As a result, the overall TIA noise performance is only mildly impacted by the use of a real current source.

The simulated -3-dB cutoff frequency of the TIA is 15.5 GHz and the estimated f^*_T is 64 GHz, giving $\lambda = 0.24$. Based on the results of the analysis in the previous section, confirmed by simulations, compared to an SE SF-TIA, the proposed design allows 75% reduction of the PA noise

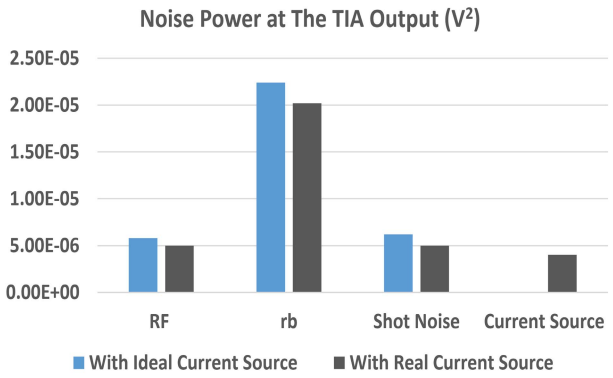

Fig. 8. TIA integrated noise power comparison with ideal and real current source (CS).

and, from Fig. 6, the R_F noise, which is the most important contribution, is reduced by 30%.

Looking at Fig. 7, the input signal experiences two different paths to the output nodes. One is from Q_1 to $V_o{}^+$. The second path is $Q_1 - Q_2 - V_o{}^-$. The difference in group delay between the two paths is 2.5 ps. From simulations, the pk-to-pk jitter at 50 Gbs on the differential eye diagram at the output of the TIA is 2.1 ps, and it rises to 4.5 ps at the output of the complete RX. The capacitance CB in Fig. 7 is 10 pF, of which 10 pF are MOM caps (0.18 f/μm^2) and 2 pF is the equivalent output capacitance of dc offset cancellation block that is connected to the unused input of the TIA. The overall TIA frequency response features a zero in the origin with a pole at 0.9 MHz, set by the offset cancellation loop, and an additional zero-pole pair that rises the gain by roughly 6 dB at 17 MHz due to CB. The high-pass profile is responsible of baseline wander. From a step response simulation, the level drop with the run length of PRBS-7 and PRBS-31 sequences is 0.18 and 0.63 dB, respectively.

After the TIA, a low headroom CH amplifier [19] shown in Fig. 9 is employed. Despite higher power consumption (since it is a two-stage amplifier) with respect to other topologies, two important features made it suitable for wideband operation. First, the miller input capacitance effect is greatly mitigated, and hence, the BW and stability of the TIA are not compromised. Second, the CH amplifier can be designed with relatively low output impedance, key to maintain wide BW and good driving capability. The CH stage is designed to provide a fairly high gain of 12 dB with 30-GHz BW and draws 3 mA. Following the CH stage, a PA with peaking in the frequency response is implemented to rise the gain and extend the limited TIA BW. To implement frequency peaking without resorting to inductors, the active feedback topology with block diagram shown in Fig. 10(a) is implemented. The active feedback leads to a second-order transfer function, which can provide peaking (p) at frequency ω_r given by

$$\omega_r = \omega_n\sqrt{1-\xi^2}$$
$$p = \frac{1}{2\xi\sqrt{1-\xi^2}} \tag{27}$$

where ω_n and ξ are the natural frequency and damping factor, respectively. Considering the block diagram in Fig. 10(a),

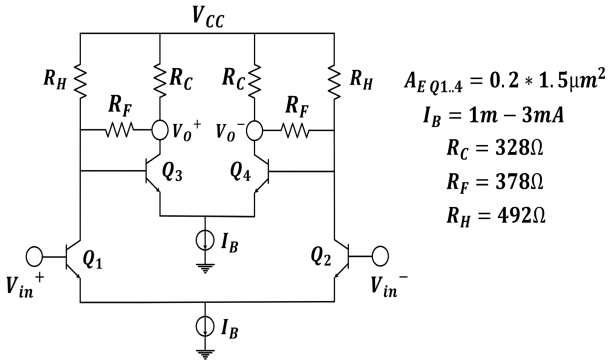

Fig. 9. CH limiting amplifier (LA) with low voltage headroom.

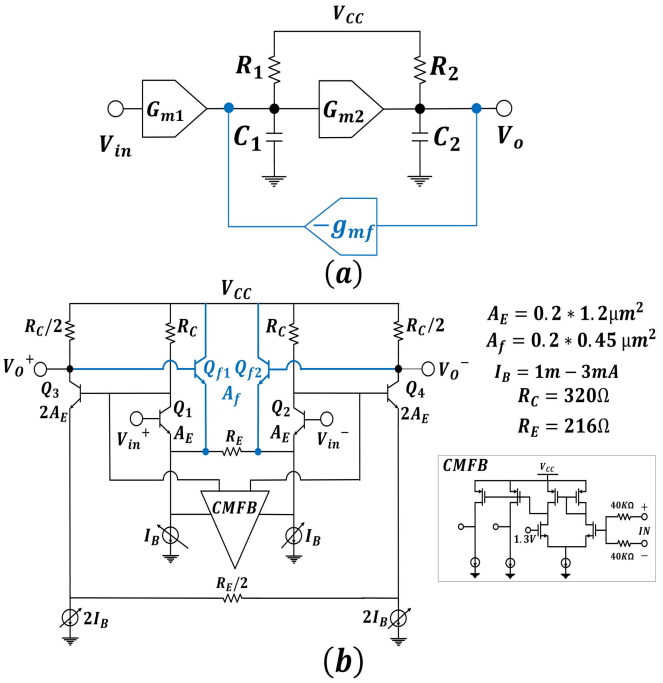

Fig. 10. (a) Active feedback topology and (b) proposed circuit implementation.

the dc gain (A_0), ω_n, and ξ are [18]

$$A_0 = \frac{G_{m1}G_{m2}R_1R_2}{1+G_{mf}G_{m2}R_1R_2}$$
$$\omega_n = \sqrt{\frac{1+G_{m2}G_{mf}R_1R_2}{1+C_1C_2R_1R_2}}$$
$$\xi = \frac{R_1C_1+R_2C_2}{2\sqrt{R_1R_2C_1C_2\left(1+G_{m2}G_{mf}R_1R_2\right)}}. \tag{28}$$

The block diagram in Fig. 10(a) is typically realized by implementing the three transconductors with differential pairs ($Q_{1,2}$, $Q_{f1,2}$, and $Q_{3,4}$). In this work, a novel circuit configuration is proposed and drawn in Fig. 10(b). The forward path [G_{m1} and G_{m2} in Fig. 10(a)] is implemented with two emitter degenerated differential pairs. Both stages have identical gain, but transistors size and bias currents are scaled up ($2\times$) to improve the load driving capability. The active feedback is implemented by $Q_{f1,2}$. They are in common collector and

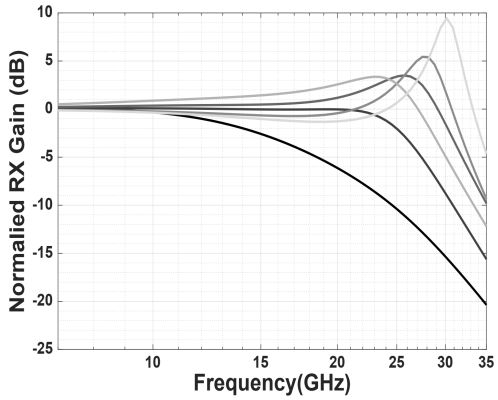

Fig. 11. Normalized RX transfer functions for different bias currents of the second stage of the active feedback PA.

share the bias current with the transistors of the first forward gain stage $Q_{1,2}$. G_{m1}, G_{m2}, and G_{mf} in (28) are linked to component parameters by the following equations:

$$G_{m1} = \frac{g_{mQ1,2}}{1 + g_{mQ1,2}\left(\frac{R_E}{2} || \frac{1}{g_{mQf1,2}}\right)}$$
$$G_{m2} = \frac{g_{mQ3,4}}{1 + g_{mQ3,4}\left(\frac{R_E}{2}\right)}$$
$$G_{mf} = \frac{g_{mf1,2}}{1 + g_{mf1,2}\left(\frac{R_E}{2}\right)}. \quad (29)$$

The peaking can be externally controlled by a 3-bit tunable bias current of the second stage ($2I_B$) to change g_{mQ1-4}. Fig. 11 shows the simulated normalized RX transfer function with different currents in the second stage of the active feedback PA, showing the different peaking profiles. The dc gain variation among the curves is within 6 dB.

Compared to previously reported realizations, where the feedback amplifier is implemented with a transconductor sharing the load with the first stage of the forward path [6], [18], the proposed solution provides two advantages.

1) The bias current of the feedback transistors $Q_{f1,2}$ does not flow through R_C (the load of $Q_{1,2}$). Hence, the circuit can operate under a lower supply voltage.
2) The equivalent input capacitance is decreased. To gain insight, Fig. 12 shows the half circuit of the input stage of the proposed amplifier. The equivalent input capacitance is given by

$$C_{\text{in}} = \frac{C_\pi}{1 + \left(g_m + g_{mf}\right)\left(\frac{R_E}{2}\right)}\left(1 - (A_0 - 1)g_{mf}\frac{R_E}{2}\right) \quad (30)$$

where C_π is the base–emitter junction capacitance of $Q_{1,2}$.

In order to avoid negative capacitance and instability, the condition $(A_0 - 1)g_{mf}(R_E/2) < 1$ must be satisfied. From (30), the input capacitance of the PA is reduced by $(1/(1 - (A_0 - 1)g_{mf}(R_E/2)))$ (1.4 times in this design) with respect to simple emitter degeneration. This helps to relax the design of the preceding stage (CH) for wideband. After the PA, a buffer shown in Fig. 13 and biased with 16-mA dc current is implemented to drive a 100-Ω differential external

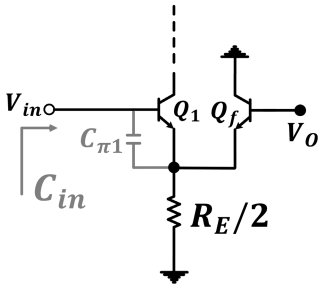

Fig. 12. Modeled half circuit input stage of the circuit shown in Fig. 10(b).

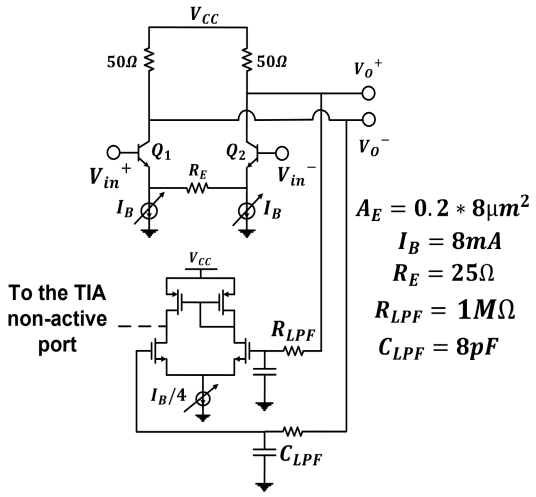

Fig. 13. Output driver and dc offset cancellation circuit.

load with good impedance matching to avoid reflections. Resistive degeneration is adopted to limit the distortion at high output amplitude. Fig. 13 also shows the dc offset cancellation loop implementation where an OTA senses the differential dc voltage at the buffer output and draws an SE correction current only from the non-active input of the TIA (base of Q_2 in Fig. 7). In this way, the input of the TIA is not loaded by extra parasitic capacitance that would limit the BW. The correction dc current at the quiescent point can be up to 750 μA. However, with the input signal from the PD, the maximum offset current that can be compensated is limited to 450 μA to avoid a penalty on the eye quality due to TIA saturation.

The plot from the post-layout simulations in Fig. 14 presents the TI gain and −3-dB BW at the output of the TIA, CH and PA+driver. The BW at the TIA and driver output is 15.5 and 27 GHz, respectively. The total RX TI gain is 78.7 dBΩ. In our previous design [17], where the PA was implemented with cascaded differential-pair stages with capacitive degeneration, the group delay variation within the −3-dB BW was 13 ps. By using the proposed active feedback PA, the group delay variation is reduced to 5 ps. Compared to our previous work in [17], the improvement in group delay variation enables 50-Gb/s operation, as proved by measurements presented in Section V.

The contribution to the total power consumption by each block is shown in Fig. 15. The contribution to the input-referred noise of components and stages in the RX chain

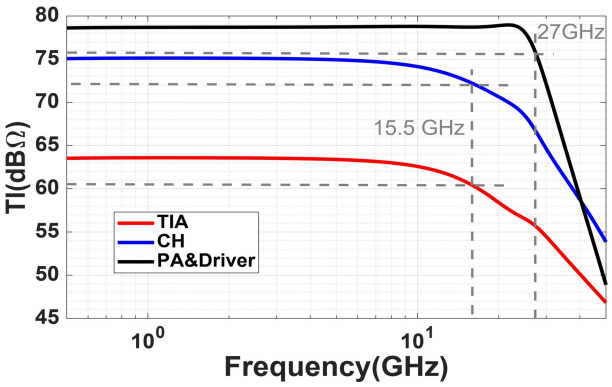

Fig. 14. TI gain at the output of different stages extracted from post-layout simulations.

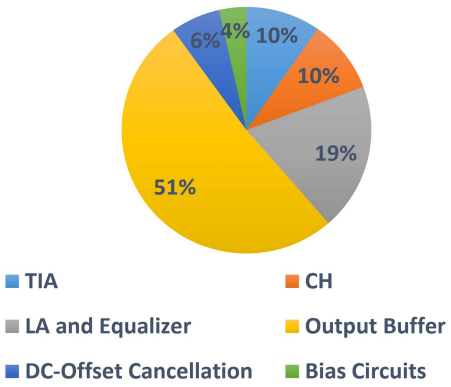

Fig. 15. Contribution to power consumption for each block.

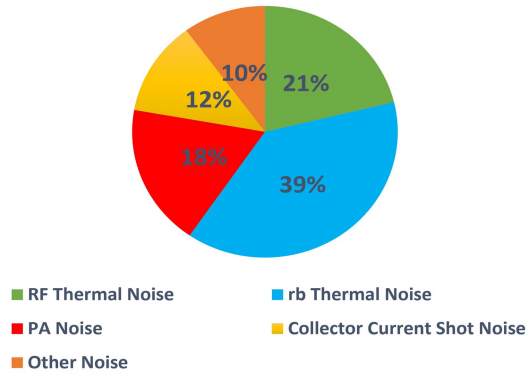

Fig. 16. Noise power shares profile at the RX input.

is shown in Fig. 16. Based on simulation results, 80% of the input-referred noise is generated by the TIA and only 20% is contributed by the CH+PA stages. The noise contributed by the TIA feedback resistor, R_F, which is typically the most important in the SF-TIA, is remarkably suppressed by the adoption of the proposed FD SF-TIA. Consequently, the thermal noise of r_b is now the principal contributing factor to the overall RX noise.

By integrating noise power in post-layout simulations up to 27 GHz (the BW of the RX), the RMS input noise current is 8.4 μA_{rms}, which corresponds to an average input-referred noise current density of 51 pA/$(Hz)^{1/2}$.

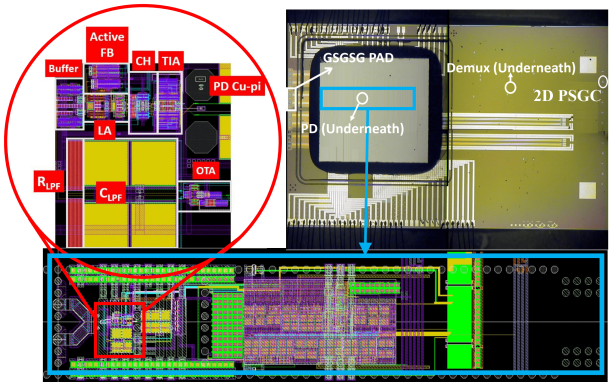

Fig. 17. Chip microphotograph and layout.

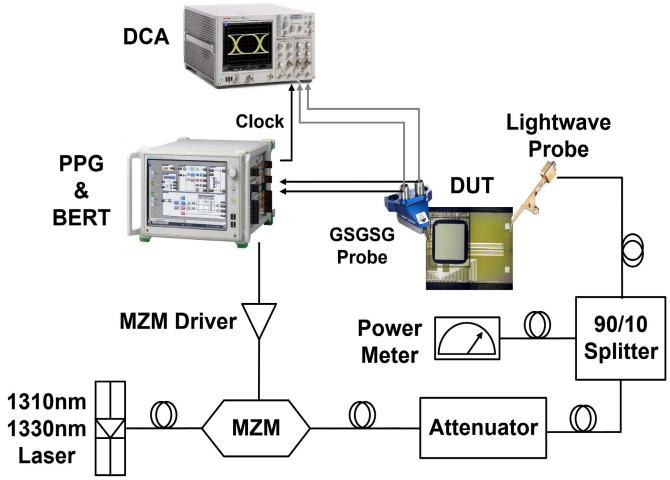

Fig. 18. Test setup for output eye diagram measurement.

V. Experimental Results

A micro-photograph of the implemented 3-D-integrated silicon photonic RX is reported in Fig. 17 with the EIC mounted face down. The same figure shows the layout of one channel of the EIC (in blue rectangular box), which includes the AFE, filtering cap, digital programming, and bias circuitry. Details of the AFE sub-block layouts are magnified in the red circle. Cu-Pi can be seen in small hexagonal shape in the layout. Multiple redundant Cu-Pi is employed, transferring supply and ground, to maintain the mechanical as well as thermal equilibrium of the chip. The active silicon area is 0.72 mm^2. The whole RX consumes 56 mW from 1.8-V supply, leading to an overall energy efficiency of 1.12 pJ/bit when operating at 50 Gb/s.

The −3-dB BW measured on the opto-electrical transfer function is 26.7 GHz.

Opto-electrical bit error rate (BER) measurements are performed with the experimental setup shown in Fig. 18. An Agilent 81672B continuous-wave tunable laser source with its wavelength set at 1310 nm feeds a Photline MXAN1300-LN-40 Mach–Zehnder modulator (MZM). An Anritsu MP1900A is used for pattern generator (up to 50 Gb/s), and with the help of Photline DR-DG-40-MO wideband driver amplifier, the PRBS electrical signal is applied to the MZM arm. The modulated optical eye at the

TABLE I

COMPARISON WITH ≥40-Gb/s BiCMOS IMPLEMENTATION STATE OF THE ARTS

	BiCMOS Technology	Supply Voltage (V)	Data Rate (Gbps) / PRBS	PD Responsivity (A/W)	Energy Efficiency (pJ/bit)	Sensitivity @TIA Input (μA p-p)	TIA FoM ($\frac{Gbps}{W.\mu Ap-p}$)	RX FoM ($\frac{Gbps}{W.\mu Ap-p}$)	Inductorless
RFIC '15 [20]	130nm	1.2	40 / 31	0.75	1.9	120	NA	4.3	No
ESSCIRC '16 [21]	250nm	2.1	40 / 31[1]	0.7	1.35	676	NA	1.1	No
JSSC '18 [6]	180nm	3.3	50 / 9	0.8	7.9	96	5.48	1.3	No
OFC '19 [22]	250nm	NA	40 / 31 50 / 31[2]	0.9	2.5 2	159 191	2.5 2.6	2.5 2.6	Yes
OFC '20 [23]	55nm	NA	50 / 15	10	2.8	363	0.9	0.9	NA
This Work	55nm	1.8	32 / 7 40 / 7 50 / 7	1	**1.75** **1.4** **1.12**	56 100 177	**33.4** **41.8** **52.3**	**10.2** **7.1** **5**	**Yes**

[1] BER = 4.5 x 10^{-11}

[2] BER = 7 x 10^{-6}

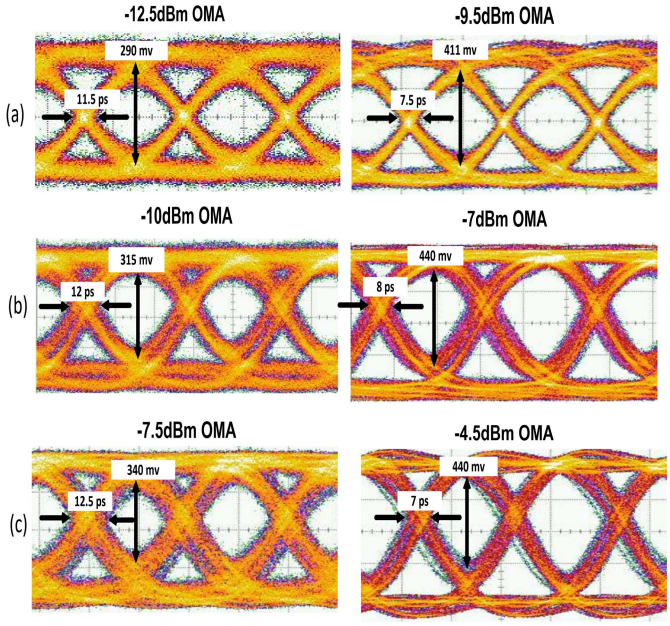

Fig. 19. Electrical output eye at sensitivity and 3 dB above at (a) 32 Gb/s, (b) 40 Gb/s, and (c) 50 Gb/s.

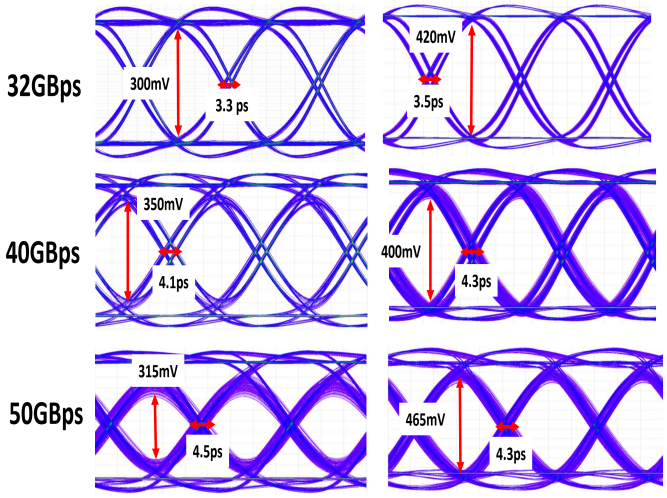

Fig. 20. Post-layout simulated eye diagram with worst case PRBS-31 input pattern at sensitivity (left column) and 3 dB above (right column) at 32, 40, and 50 Gb/s.

MZM output achieves an extinction ratio of 12.4 dB. Then, an SMF delivers the optical signal to the RX chip with a fiber probe, which is precisely aligned to the PSGC on the PIC. The differential electrical output eye diagram is measured on an Agilent DCA-X 86100D sampling oscilloscope. An Anritsu MP1900A also measures the BER.

The measured eye diagrams are shown in Fig. 19. They are measured for 32 Gb/s [see Fig. 19(a)], 40 Gb/s [see Fig. 19(b)], and 50 Gb/s [see Fig. 19(c)] at the input optical power equal to the sensitivity (left) and 3 dB above (right). The modulated optical input test pattern is PRBS-15 and above 400 hits are recorded per each measurement. Post-layout simulated eye diagrams are shown in Fig. 20. The simulation has been performed with the worst case sequence of a PRBS-31 pattern and with a simple PD diode model comprising a current source with a parallel capacitance. The higher pk-to-pk jitter in the measured eye diagrams of Fig. 19, particularly at the sensitivity level, is due to the jitter in the optical input signal and additive noise which are not considered in simulations.

Fig. 21(a) shows the BER curves versus the optical power estimated at the PD input for different data rates with a PRBS-7 pattern. The sensitivity at PD input for BER $<10^{-12}$ at 50 Gb/s is -7.5 dBm OMA with 12.5-ps peak-to-peak jitter. Considering the 3.7-dB loss of the 2-D PSGC plus optical waveguide on the PI, C, and the 1.5-dB loss of the optical demux, the sensitivity at the fiber output is -2.3-dBm OMA. Fig. 21(b) shows the bathtub curves at different data rates with

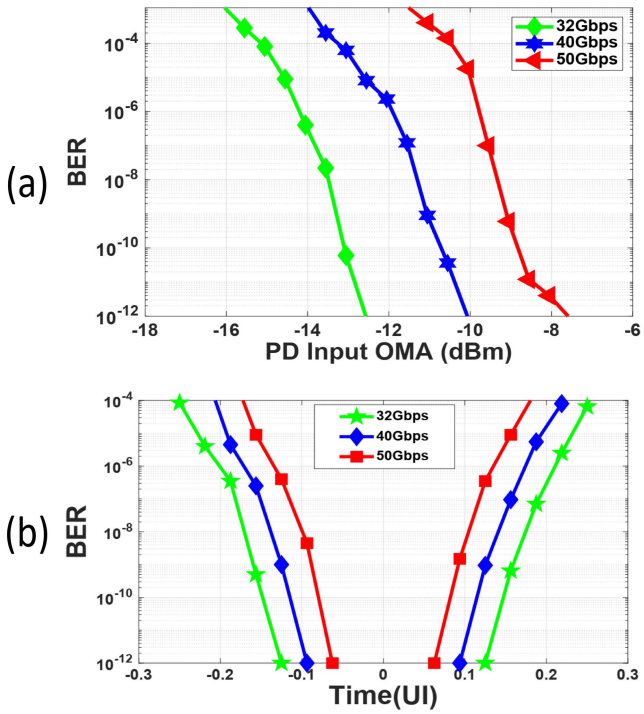

Fig. 21. (a) BER versus the input power and (b) bathtub curve at the sensitivity for different data rates.

input optical power at the sensitivity. The horizontal opening at 50 Gb/s is 0.16 UI. Test performed on the other optical channel in the module, with the laser tuned at 1330 nm, proved the same performance. At the chip size, no issues have been detected that may compromise the performance of the two channels working concurrently.

The measured performance of the RX module is summarized in Table I and compared against recently published RXs for >40 Gb/s in SiGe BiCMOS technology nodes. At 50 Gb/s, the presented RX displays a minimum power efficiency of 1.12 pJ/bit. With the sensitivity of 177 μA at the TIA input, both the TIA and complete RX prove the best energy efficiency and FoM [see (1)] among BiCMOS realizations.

VI. Conclusion

A 3-D-integrated silicon photonic RX operating error-free up to 50 Gb/s has been presented. The sensitivity has been improved by leveraging a low-noise FD SF-TIA followed by a novel active feedback PA for BW extension. The complete RX is designed without using inductors and operates with a low supply voltage of 1.8 V only, reducing significantly the power consumption. This work demonstrates very high FoM, i.e., data rate normalized to sensitivity and power consumption, among previously reported RX and TIAs in BiCMOS technologies.

References

[1] D. V. Plant, M. Morsy-Osman, and M. Chagnon, "Optical communication systems for datacenter networks," in *Proc. Opt. Fiber Commun. Conf.*, Los Angeles, CA, USA, 2017, pp. 1–47.

[2] C. F. Lam, "Optical network technologies for datacenter networks," in *Proc. Nat. Fiber Opt. Eng. Conf.*, 2010, pp. 1–3, Paper NWA3.

[3] D. Mahgerefteh *et al.*, "Techno-economic comparison of silicon photonics and multimode VCSELs," *J. Lightw. Technol.*, vol. 34, no. 2, pp. 233–242, Jan. 15, 2016.

[4] F. Boeuf *et al.*, "Silicon photonics R&D and manufacturing on 300-mm wafer platform," *J. Lightw. Technol.*, vol. 34, no. 2, pp. 286–295, Jan. 15, 2016.

[5] E. Temporiti *et al.*, "Insights into silicon photonics Mach–Zehnder-based optical transmitter architectures," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 3178–3191, Dec. 2016.

[6] T. Takemoto *et al.*, "A 50-Gb/s high-sensitivity (−9.2 dBm) low-power (7.9 pJ/bit) optical receiver based on 0.18-μm SiGe BiCMOS technology," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1518–1538, May 2018.

[7] C. Li and S. Palermo, "A low-power, 26-GHz transformer-based regulated cascode transimpedance amplifier in 0.25 μm SiGe BiCMOS," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, Atlanta, GA, USA, Oct. 2011, pp. 83–86.

[8] C. Kromer *et al.*, "A low-power 20-GHz 52-dBΩ transimpedance amplifier in 80-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 6, pp. 885–894, Jun. 2004.

[9] E. Säckinger, *Broadband Circuits for Optical-Fiber Communication*. Hoboken, NJ, USA: Wiley, 2005.

[10] I. Ozkaya *et al.*, "A 64-Gb/s 1.4-pJ/b NRZ optical receiver data-path in 14-nm CMOS FinFET," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3458–3473, Dec. 2017.

[11] J. E. Proesel *et al.*, "A 32 Gb/s, 4.7 pJ/bit optical link with −11.7 dBm sensitivity in 14-nm FinFET CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 4, pp. 1214–1226, Apr. 2018.

[12] M. Raj *et al.*, "Design of a 50-Gb/s hybrid integrated Si-photonic optical link in 16-nm FinFET," *IEEE J. Solid-State Circuits*, vol. 55, no. 4, pp. 1086–1095, Apr. 2020.

[13] S. S. Mohan, M. D. M. Hershenson, S. P. Boyd, and T. H. Lee, "Bandwidth extension in CMOS with optimized on-chip inductors," *IEEE J. Solid-State Circuits*, vol. 35, no. 3, pp. 346–355, Mar. 2000.

[14] J. Kim and J. F. Buckwalter, "Bandwidth enhancement with low group-delay variation for a 40-Gb/s transimpedance amplifier," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 8, pp. 1964–1972, Aug. 2010.

[15] D. Li *et al.*, "A low-noise design technique for high-speed CMOS optical receivers," *IEEE J. Solid-State Circuits*, vol. 49, no. 6, pp. 1437–1447, Jun. 2014.

[16] I. G. López, "100 Gb/s differential linear TIAs with less than 10 pA/$\sqrt{\text{Hz}}$ in 130-nm SiGe:C BiCMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 2, pp. 458–469, Feb. 2018.

[17] F. Bozorgi, M. Bruccoleri, M. Repossi, E. Temporiti, A. Mazzanti, and F. Svelto, "A 26-Gb/s 3-D-integrated silicon photonic receiver in BiCMOS-55 nm and PIC25G with −15.2-dBm OMA sensitivity," *IEEE Solid-State Circuits Lett.*, vol. 2, no. 9, pp. 187–190, Sep. 2019.

[18] B. Razavi, *Design of Integrated Circuits for Optical Communications*. Hoboken, NJ, USA: Wiley, 2012.

[19] E. M. Cherry and D. E. Hooper, "The design of wide-band transistor feedback amplifiers," *Proc. IEEE*, vol. 110, no. 2, pp. 375–389, Feb. 1963.

[20] Z. Xuan *et al.*, "A low-power 40 Gb/s optical receiver in silicon," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Phoenix, AZ, USA, May 2015, pp. 315–318, doi: 10.1109/RFIC.2015.7337768.

[21] M. H. Eissa *et al.*, "A wideband monolithically integrated photonic receiver in 0.25-μm SiGe:C BiCMOS technology," in *Proc. 42nd Eur. Solid-State Circuits Conf. (ESSCIRC Conference)*, Lausanne, Switzerland, 2016, pp. 487–490.

[22] H. Andrade, T. Hirokawa, A. Maharry, A. Rylyakov, C. L. Schow, and J. F. Buckwalter, "Monolithically-integrated 50 Gbps 2 pJ/bit photoreceiver with cherry-hooper TIA in 250 nm BiCMOS technology," in *Proc. Opt. Fiber Commun. Conf. (OFC)*, San Diego, CA, USA, 2019, pp. 1–3.

[23] S. A. Srinivasan *et al.*, "Highly sensitive 56 Gbps NRZ O-band BiCMOS-silicon photonics receiver using a Ge/Si avalanche photodiode," in *Proc. Opt. Fiber Commun. Conf. (OFC)*, San Diego, CA, USA, 2020, pp. 1–3.

Farhad Bozorgi received the B.Sc. degree in electrical engineering from the K. N. Toosi University of Technology, Tehran, Iran, in 2011, the M.Sc. degree in electronics engineering, circuits and systems from the University of Tehran, Tehran, in 2014, and the Ph.D. degree from the Analog Integrated Circuits Laboratory, The University of Pavia, Pavia, Italy, in 2020. During his Ph.D. degree, he has worked on the realization of 50-Gb/s serial data transceiver.

He was a Research Assistant with the University of Tehran, working on implantable neural stimulator/recording, until 2016. In 2016, he joined the Analog Integrated Circuits Laboratory, The University of Pavia, as a Research Assistant. In 2020, he joined Barkhausen Institut, Dresden, Germany, as a Research Associate, where he currently works on RF design enablement of joint communication and sensing architectures. His research interests include wideband, RF, and mm-wave analog integrated circuit designs for various applications, such as 5G, the IoT, and medical in CMOS/BiCMOS technologies.

Melchiorre Bruccoleri received the Laurea degree in electronics engineering from the University of Genova, Genoa, Italy, in 1993.

He has been working with STMicroelectronics, Milan, Italy, since 1994. He has been working in several areas concerning BiCMOS and CMOS analog and RF design, first in Hard disk drive read and write (HDD R/W) channel in the storage ICs design [advance peak detection and partial-response maximum-likelihood (PRML)] for HDD applications, wireless [ultra wideband (UWB) RF Transceiver ICs and digital base band (DBB) ICs for W-USB and Video link], and wireline communication (serializer/deserializer (SERDES), serial advanced technology attachment (SATA), and Miphy IPs). In 2008, he became the Advance Research and Development Senior Manager and Interface versus external University and Research centers in the High-Speed Interfaces Group-DCG Product Group. Since 2015, he has been working as the Research and Development Senior Manager of the Digital and Mixed Processes ASIC (DMA) Division, Digital Product Group. He has been involved in research and research and development programs for high-speed low-energy communications (Horizon 2020 European Funded Projects: COSMICC, TERABOARD, and STREAMS) and RF telecommunication systems (European Funded projects: DREAM-H2020, TARANTO-ECSEL, and DRAGON-H2020). He has authored or coauthored several U.S. patents (32) and IEEE journal articles/conference papers (19).

Elham Rahimi received the B.Sc. degree in electrical engineering (electronics) from the K. N. Toosi University of Technology, Tehran, Iran, in 2011, the M.Sc. degree in microelectronics from the Amirkabir University of Technology, Tehran, in 2014, and the Ph.D. degree in microelectronics from The University of Pavia, Pavia, Italy, in 2019. Her Ph.D. thesis was focused on high-efficiency millimeter-wave power amplifiers and direct-conversion transmitter for 5G networks.

In 2019, she joined Silicon Austria Labs (SAL), Linz, Austria, where she is currently Research Scientist, working on mm-wave analog front-end for 5G/6G hardware implementation. Her main research interests include analysis and design of RF/mm-wave BiCMOS/CMOS building blocks.

Matteo Repossi received the Laurea and Ph.D. degrees in electronics engineering from The University of Pavia, Pavia, Italy, in 2002 and 2006, respectively.

In 2005, he was a Guest Researcher with the Department of Electronic and Information Engineering (DIEI), University of Perugia, Perugia, Italy, in the framework of a national research project on wideband RF-micro electro-mechanical systems (MEMS) circuits. In 2006, he joined STMicroelectronics within the Studio di Microelettronica, Pavia, where his research is focused on the design and characterization of high-speed components and circuits for RF, silicon photonics, and serializer/deserializer (SerDes) communication applications, with a particular focus on high-frequency design methodologies and signal integrity aspects. Since 2020, he has been working as an Electromagnetic Modeling and Signal Integrity Staff Engineer with Digital and Mixed Processes ASIC (DMA) Division, Digital Product Group, supporting the design and integration of SerDes IPs for datacenter and space and defense applications.

Dr. Repossi was a recipient of the Second Best Student Paper Award at the 2004 Applied Computational Electromagnetics Software Conference, Syracuse, NY, USA.

Francesco Svelto (Fellow, IEEE) received the Laurea and Ph.D. degrees in electrical engineering from The University of Pavia, Pavia, Italy, in 1991 and 1995, respectively. During his Ph.D. studies, he focused on the design of low-noise electronic circuits for high-energy physics experiments.

He was an Associate Researcher for a few months in several international institutions: the Brookhaven National Laboratory, Upton, NY, USA, Lawrence Berkeley National Laboratories, Berkeley, CA, USA, C.E.R.N., Meyrin, Switzerland, and the Laboratoire de l' Accelerateur Lineaire, Orsay, France. From 1996 to 1997, he held a grant from STMicroelectronics, Milan, Italy, for research in the area of CMOS wireless circuits. In 1997, he was appointed as an Assistant Professor with the University of Bergamo, Bergamo, Italy. In 2000, he joined The University of Pavia, where he is currently a Professor and the Vice-Rector for knowledge transfer. He has been the Technical Advisor of RFDomus Inc., Irvine, CA, USA, a startup he co-founded in 2002 dedicated to highly integrated GPS receivers. After merging with Glonav Inc., Dublin, Ireland, RFDomus has been acquired by NXP Semiconductors in 2007. Since January 2006, he has been the Director of the Scientific Laboratory, joint between The University of Pavia and STMicrolectronics, dedicated to research in microelectronics. His research interests include RF and mm-wave systems for wireless communications, high-speed serial links, and ultrasound electronics for medical diagnostic. Silicon photonics, both in the area of optical components and electronics transceiver design, is drawing more and more research interest.

Dr. Svelto is the Solid-State Circuits Society Distinguished Lecturer. He has been a member of the Technical Program Committee of the International Solid-State Circuits Conference, the Custom Integrated Circuits Conference, and the Bipolar/BiCMOS Circuits Technology Meeting: all organized by the Institute of Electrical and Electronics Engineers (IEEE). He is a member of the Technical Program Committee of the European Solid-State Circuits Conference. He was a co-recipient of the IEEE JOURNAL OF SOLID-STATE CIRCUITS 2003 Best Paper Award. He has served as an Associate Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS from 2003 to 2007 and a Guest Editor for a Special Issue on the IEEE JOURNAL OF SOLID-STATE CIRCUITS in March 2003.

Andrea Mazzanti (Senior Member, IEEE) received the Laurea and Ph.D. degrees in electrical engineering from the University of Modena and Reggio Emilia, Modena, Italy, in 2001 and 2005, respectively.

During the summer of 2003, he was an Intern with Agere Systems, Allentown, PA, USA. From 2006 to 2009, he was an Assistant Professor with the University of Modena and Reggio Emilia. In January 2010, he joined The University of Pavia, Pavia, Italy, where he is currently a Full Professor. He has authored more than 100 technical articles. His main research interests include device modeling and IC design for high-speed communications, RF, and millimeter-wave systems.

Dr. Mazzanti has been a member of the Technical Program Committee of the IEEE Custom Integrated Circuit Conference (CICC) from 2008 to 2014, the IEEE European Solid-State Circuits Conference (ESSCIRC), and the IEEE International Solid-State Circuits Conference (ISSCC) from 2014 to 2018. He has been Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS from 2012 to 2015 and a Guest Editor of Special Issues of the IEEE JOURNAL OF SOLID-STATE CIRCUITS dedicated to CICC 2013–2014 and ESSCIRC-2015. Since 2017, he has been serving as an Associate Editor for the IEEE SOLID-STATE CIRCUITS LETTERS.