A Broadband 22–31-GHz Bidirectional Image-Reject Up/Down Converter Module in 28-nm CMOS for 5G Communications

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***Abstract*— This article presents a *Ka*-band bidirectional transceiver front end and its integration in an image-reject up/down converter module in 28-nm bulk CMOS. In the radio frequency (RF) front end, a transformer-based transmit/receive (T/R) switch is exploited for minimum area occupation without affecting the linearity and the isolation between the transmitter (TX) and receiver (RX) paths. The TX front end shows 19-dB power gain with an output-referred $OP_{1\,dB}$ of 14 dBm and 18.7% power-added efficiency (PAE). Tested with a 100-MHz 64-QAM orthogonal frequency-division multiplexing (OFDM) modulated input signal, the error vector magnitude (EVM) is below 5% up to an average output power of 6.6 dBm, with a corresponding 7% PAE. The RX in the front end features a minimum noise figure (NF) of 4.9 dB, with 17-dB power gain. The measured input IP3 is −9.2 dBm, while the power consumption is only 35 mW. The RF bandwidth is 22–31 GHz, wide enough to cover the fifth-generation (5G) new radio (NR) bands n257, n258, and n261. The RF front end is also monolithically integrated along with a broadband bidirectional frequency up/down converter, capable of translating the 5G modulated signal from/to a 3-GHz intermediate frequency (IF). The up/down converter is realized with a single bidirectional quadrature mixer shared between the TX and RX paths. At the IF, a single hybrid coupler is used for quadrature phase shifting in upconversion and recombination in downconversion while concurrently keeping the TX and RX IF paths isolated from each other. In the upconversion mode, the module features a 22-dB programmable conversion gain, with a 40-dB minimum in-band image rejection ratio (IRR). The downconversion path shows a 29-dB programmable conversion gain and a minimum measured NF and IRR of 8.5 and 30 dB, respectively, while consuming 110 mW.**

***Index Terms*— 28-nm CMOS, doubly tuned transformer, fifth generation (5G), hybrid coupler, image rejection, transceiver, transmit/receive (T/R) switch.**

I. Introduction

THE ever-increasing demand for higher data traffic volume has driven the recent development of silicon-based millimeter-wave (mm-Wave) phased-array transceivers for wireless communications [1]–[24]. The fifth-generation (5G) mobile network exploits carrier frequencies in the *Ka*-band to support high data rates and low-latency transmission links between the base station and mobile devices. Centered at around 28 GHz, multiple sub-bands have been allocated, namely, the 5G new radio (NR) bands n257, n258, and n261, spanning from 24.25 to 29.5 GHz [25]. While several recently published works address 5G building blocks and transceivers at 28 GHz [1]–[18], [21]–[24], [26]–[37], to the authors' knowledge, transceivers covering the whole 24.25–29.5-GHz frequency range have not been demonstrated in bulk CMOS technology yet, with the only notable exception of [7], which, however, does not include any frequency conversion circuit.

In [23], a broadband 22–31-GHz radio frequency (RF) transceiver front end, comprising a low-noise amplifier (LNA), a power amplifier (PA), and a transmit/receive (T/R) switch, was presented, covering all the *Ka*-band 5G sub-bands with margin. The work presented in this article moves a step forward, complementing the front end reported in [23] with a broadband bidirectional frequency up/down converter, capa-

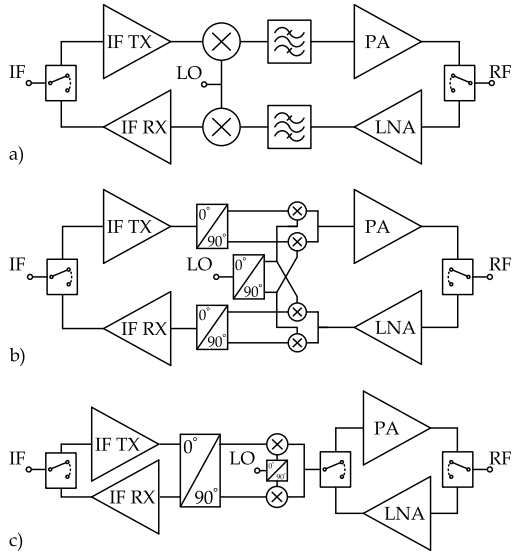

Fig. 1. Simplified block diagram of (a) typical high-IF frequency converter, (b) typical low-IF image-reject frequency converter, and (c) proposed low-IF bidirectional image-reject frequency converter.

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ble of translating the 5G modulated signal from a 3-GHz intermediate frequency (IF) to the 22–31-GHz frequency range (and vice versa).

A few different options are available to implement a up/down converter suitable for mm-Wave 5G transceivers, as shown in Fig. 1. They are all typically based on variations of the heterodyne architecture. Hence, as wideband and even multiband designs [21], [22], [24], [35], [38]–[41] are becoming more and more popular in the literature, the issue of image rejection comes to the forefront, both in terms of rejection of interferers in the image band for the receiver (RX) and reduction of spurious emissions, which could violate the emission mask, for the transmitter (TX). The choice of the IF drives the selection of the countermeasures used to tackle the image issue.

If a high intermediate frequency (high-IF) is selected (e.g., 7 GHz as in [3] and [12] or up to 16 GHz as in [42]), on-chip bandpass filters in the signal chain can be used to easily suppress any spurious signal at the image frequency, as shown in Fig. 1(a). In this way, a single-phase mixer, not requiring quadrature (I/Q) local oscillator (LO), or quadrature phase shifting and recombination of the desired signal, can be used in the TX and RX paths. Consequently, the transceiver architecture is simplified. However, the distribution of a high-IF signal to multiple up/down converters on printed circuit board (PCB), as proposed in [12], leads to large power consumption. Furthermore, if the IF is selected to be fairly high to simplify the filtering of the image, the LO feedthrough in the RX mode may compromise the system linearity by saturating the IF stages [42].

The alternative is to select a relatively low intermediate frequency (low-IF). In this case, the image signal is likely within the system passband, which calls for highly selective image-reject filters with steep roll-offs. The latter are hardly realizable in integrated fashion at mm-Wave frequencies and are thus typically implemented as external components, as reported, e.g., in [3]. If a selective bandpass filter is not a viable option, a quadrature up/down converter architecture is required [8], [38], [43]–[46]. In this case, as shown in Fig. 1(b), four mixers (i.e., two I/Q pairs) are required in the TX and RX paths, along with quadrature phase shifting and recombination circuits at the IF TX and RX interfaces, leading to higher power consumption and larger silicon area with respect to the simpler architecture in Fig. 1(a).

In this work, we investigate a different solution. A bidirectional architecture, based on building block reuse, is leveraged to reduce the hardware complexity of a low-IF up/down converter to a level comparable to the simple architecture of Fig. 1(a) while achieving a large image rejection without the need of any off-chip filters. The proposed architecture is shown in Fig. 1(c). A single bidirectional quadrature mixer is shared between the TX and RX paths. Moreover, a hybrid quadrature coupler is used to phase shift the IF signal in upconversion and also recombine the I/Q signals in downconversion while concurrently keeping the TX and RX IF paths isolated from each other.

A detailed block diagram of the proposed broadband 22–31-GHz bidirectional frequency converter is shown in Fig. 2. The RF antenna interface is shared between the TX and RX paths by means of a wideband T/R switch [23]. The switch is based on an asymmetric topology made of a shunt switch at the LNA input and an impedance inverter. The latter is implemented as a doubly tuned transformer network [47], [48] (as opposed to a conventional $\lambda/4$ transmission line) to save area while providing good isolation and low loss. The image-reject frequency converter employs highly linear quadrature CMOS passive mixers, which are intrinsically bidirectional, and a transformer-based 3-GHz quadrature hybrid coupler, similar to the one reported in [49]. The mixer linearity is enhanced by exploiting transmission gates made of the parallel combination of pMOS and nMOS devices [50], [51]. Wideband 19–28-GHz LO quadrature generation is achieved by means of a two-stage transformer-based hybrid coupler [38], [49], followed by a three-stage inverter-based LO buffer, which drives the mixers. On both the TX and RX IF paths, a variable gain feature is implemented.

Overall, the proposed frequency converter, implemented in a 28-nm bulk CMOS technology, shows a remarkable measured performance. The upconversion path features a 22-dB programmable conversion gain while displaying a minimum in-band image rejection ratio (IRR) of 40 dB. The downconversion path shows a 29-dB programmable conversion gain and a minimum measured noise figure (NF) and an IRR of 8.5 and 30 dB, respectively.

This article is organized as follows. Section II discusses the design of the bidirectional transceiver front end introduced in [23]. The design of bidirectional up/down converter and the quadrature LO generation chain is described in Section III, while Section IV presents the measurement results and a comparison with the state of the art of the two proposed integrated circuits. Eventually, Section V concludes this article.

II. RF Front End

A block diagram of the proposed RF front end is shown in Fig. 3 [23]. The TX and RX paths share a single antenna port (ANT). Matching networks MN1 and MN6, together with switch *S*, implement a compact T/R switch while also realizing single-ended-to-differential conversion. The two paths also share a common RF port through matching network MN3 such that the front end is bidirectional. Doubly tuned transformer-based matching networks [47] are used for interstage ac coupling and wideband operation both in the TX and RX paths. The front-end RX path is made of a two-stage wideband LNA, an inductively degenerated common-source stage (LNA in Fig. 3) is followed by a cascode amplifier (CC in Fig. 3). The TX path is realized as a three-stage wideband amplifier: a first common-gate (CG) stage (CG in Fig. 3), whose relatively low input impedance, $Z_{\mathrm{IN}}^{\mathrm{CG}}$, simplifies the matching to the RF input port, is followed by a two-stage PA (driver stage (DR) and PA in Fig. 3). The bias point of blocks CC (in RX) and CG (in TX) is reconfigured to select the active path (RX or TX) by changing the voltage of a node in the network MN3 common to both blocks.

A. T/R Switch Design

A good T/R switch is fundamental in time division duplexing (TDD) systems to preserve the efficiency of the TX while

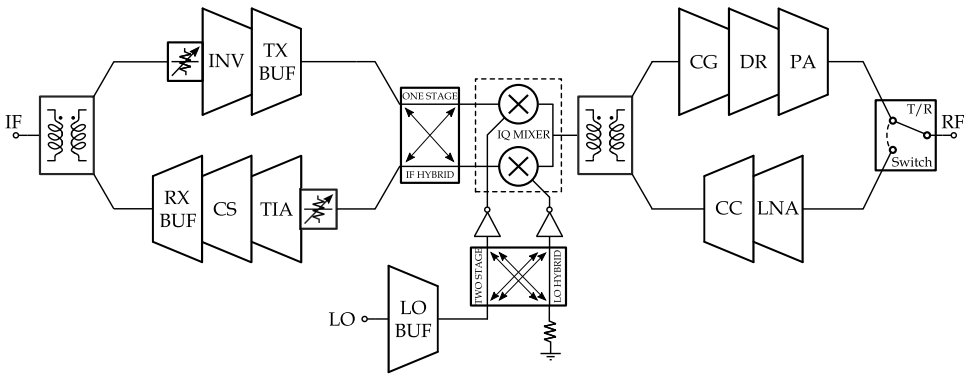

Fig. 2. Block diagram of the proposed low-IF bidirectional image-reject up/down converter.

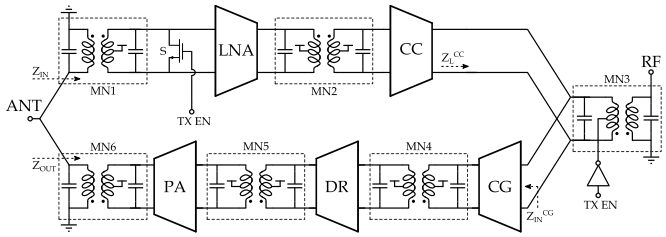

Fig. 3. Block diagram of the proposed transceiver front end.

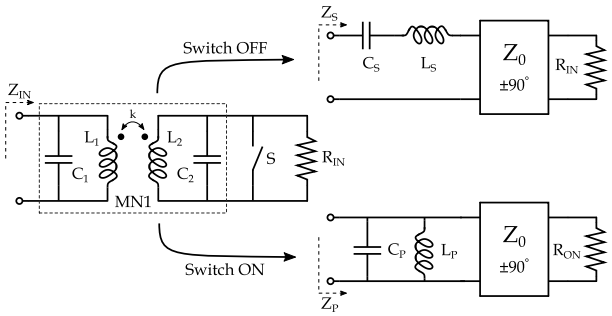

Fig. 4. Equivalent circuits for MN1 in RX (switch OFF) and TX (switch ON) modes.

keeping the NF of the RX low. Several solutions have been presented in the literature [10], [11], [15], [16]. In [10], a conventional and area-consuming $\lambda/4$ transmission line is used to realize an impedance inverter, while the solution proposed in [11] is only viable for single-ended RXs. In [15] and [16], a compact T/R switch interface is realized by means of a trifilar transformer: the resulting frequency response is, however, rather narrow. In Fig. 3, the solution proposed in this work is illustrated. The conventional $\lambda/4$ transmission line impedance inverter is replaced by a doubly tuned transformer-based matching network MN1, an approach that is compact and low loss at the same time. In the RX mode, the TX path is turned off and the input impedance of the LNA (Fig. 3) is matched to the ANT port through the combination of the matching network MN1 and the output impedance of the PA (Z_{OUT} in Fig. 3). In the TX mode, the matching network MN1 implements a large step-up transformation (namely, an impedance inversion) of the equivalent ON-resistance of the switch, R_{ON}, minimizing the loading on the PA.

The behavior of the matching network MN1 can be better grasped using the equivalent circuits shown in Fig. 4. The input impedance of the LNA is represented by a parallel RC circuit; in Fig. 4, the resistance is R_{IN}, while the capacitance is embedded in C_2. In the neighborhood of the resonance frequency

$$\omega_S = \frac{\omega_{1,2}}{\sqrt{1-k^2}} \tag{1}$$

where $L_2C_2 = L_1C_1 = 1/\omega_{1,2}^2$, and the doubly tuned transformer network approximates the behavior of an impedance inverter [47]. Depending on the load conditions, the network equivalent circuit is made of a combination of an ideal impedance inverter and a series, or a shunt resonator.

In reception, the switch S is open, and the equivalent circuit is made of the series combination of a series tank and an ideal impedance inverter. The LNA input resistance, R_{IN}, is scaled to 50 Ω by the impedance inverter as

$$\Re e(Z_S) = \frac{Z_0^2}{R_{\mathrm{IN}}} = 50\ \Omega \tag{2}$$

where

$$Z_0 = \omega_S\sqrt{L_1L_2}\frac{1-k^2}{k}. \tag{3}$$

In this operating mode, the PA is OFF and its output impedance, Z_{OUT}, can be modeled as a parallel resonator R_{EQ}, L_{EQ}, and C_{EQ}, as shown in Fig. 5. Z_{OUT}, combined with the equivalent series resonator of MN1, makes up a ladder filter, which can be designed for wideband operation. In this way, broadband input matching is achieved, as demonstrated by the simulated and measured input reflection coefficient, $\Gamma_{\mathrm{in,RX}}$, in Fig. 21.

In transmission, when the switch S is closed, the equivalent circuit of MN1 is made of an ideal impedance inverter and a shunt resonator (C_P–L_P in Fig. 4). Over the band of operation of the front end, the switch ON-resistance, R_{ON}, is scaled up by the impedance inverter to avoid loading the PA, while the combination of C_P–L_P in Fig. 4 and MN6 in Fig. 3 resonates.

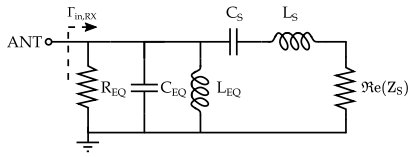

Fig. 5. Equivalent ladder network synthetized by MN1 and MN6 for RX broadband operation.

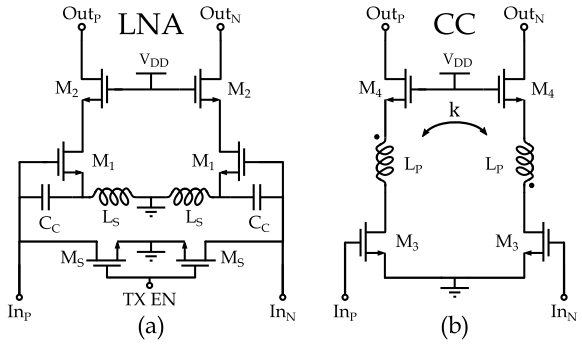

Fig. 6. RX active stages: (a) LNA and (b) cascode amplifier.

Hence,

$$\Re e(Z_P) = \frac{Z_0^2}{R_{\rm ON}} \gg 50\ \Omega. \tag{4}$$

The values of L_1 and L_2 and the coupling factor k are chosen to minimize the losses, following the guidelines discussed in [47] and [48]. Assuming a comparable quality factor for L_1 and L_2, the turn ratio $n = \sqrt{L_2/L_1}$ is to be maximized, while the coupling factor is selected to be $k_{\rm opt} = 0.5$. The values of the reactive components of MN1 are reported in Table I.

B. RF Receive Path Design

The front-end receive path is made of a cascade of two pseudo-differential stages (see Fig. 6). In the first stage (LNA), inductive degeneration is used to synthesize the resistive termination necessary to match the antenna port. The value of the degeneration inductors L_S is limited, as the input admittance of the LNA has to display a parallel RC behavior in the frequency range of operation, as discussed in Section II-A. Cascode transistors are used to ensure the stability of the LNA.

The switch S is realized by a pair of nMOS transistors [M_S in Fig. 6(a)]. In the TX mode, the switch turns off the LNA by grounding the gate of transistors M_1. At the same time, transistors M_S load the secondary side of MN1 (Fig. 3) with their ON-resistance, $R_{\rm ON}$. As discussed, to preserve the efficiency of the TX, $R_{\rm ON}$ should be as low as possible. A lower bound to the attainable value of $R_{\rm ON}$ is, however, set by the sum of the parasitic capacitance of the switch and the input capacitance of the LNA, which must not exceed the desired value of C_2 in Fig. 4. This limits the maximum width of M_S and, consequently, the minimum $R_{\rm ON}$.

To properly drive the RF port and avoid a reduction of the gain of the RX path, an additional stage is added after the LNA (CC in Fig. 3). The additional stage is a cascode amplifier

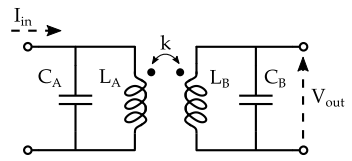

Fig. 7. Prototype of the doubly tuned transformer-based matching networks.

TABLE I
SUMMARY OF THE VALUES OF THE COMPONENTS OF THE DOUBLY TUNED TRANSFORMER-BASED MATCHING NETWORKS

	MN1	MN2	MN3	MN4	MN5	MN6
k	0.5	0.3	0.6	0.3	0.45	0.78
L_A [pH]	260	320	195	700	170	70
L_B [pH]	450	625	320	315	400	250
C_A [fF]	166	105	255	50	295	250
C_B [fF]	96	55	155	112	125	70

with peaking inductors L_P between the driver and cascode transistors, as shown in Fig. 6(b). The peaking inductors L_P enhance the gain and simplify the layout of the bidirectional front end. Magnetic coupling between the two branches is used to increase the quality factor of the differential-mode inductor. AC coupling between the LNA and CC stage (MN2 in Fig. 3) is achieved by means of a doubly tuned transformer matching network designed for broadband operation. A low magnetic coupling k and turn ratio $n > 1$ can be leveraged to obtain broadband operation and passive voltage gain, respectively. A concentric planar layout is used to implement the required transformer with low magnetic coupling and a turn ratio larger than one in a simple fashion. All interstage matching networks shown in Fig. 3 (MN2, MN4, and MN5), are realized similarly to make the frequency response of the circuit broadband [47], [48]. A prototype of the doubly tuned transformer network used to implement the interstage matching networks is reported in Fig. 7. The values of the reactive components of all the matching networks are reported in Table I.

C. RF TX Path Design

The architecture of the three-stage TX front end is shown in Fig. 3. In the TX mode, the RF port is matched to the input impedance of the CG stage, $Z_{\rm IN}^{\rm CG} = 30\ \Omega$, by the matching network MN3. To match the single-ended port impedance $Z_C = 50\ \Omega$ to the differential CG input impedance $Z_{\rm IN}^{\rm CG}$, the transformation ratio introduced by MN3 has to be $m = (Z_{\rm IN}^{\rm CG}/Z_C)^{1/2} = 0.77$. In the RX mode, this impedance transformation results in a load impedance for the RX cascode amplifier (CC in Fig. 3) equal to $Z_L^{\rm CC} = m^2 Z_C = 30\ \Omega$, as MN3 is shared between the TX and RX paths. To avoid loading effects between TX and RX paths, CC and CG stages are turned off in TX and RX operation, respectively.

Both the DR and the PA in Fig. 3 are realized as neutralized pseudo-differential pairs. The differential-mode stability of the TX path is ensured in both stages by neutralization capacitors. Neglecting the losses in the output network, the PA is

designed targeting an output-referred 1-dB compression point $OP_{1\,dB} = 15$ dBm. Reliability constraints limit the achievable voltage swing at the output of the active stages. Considering a maximum drain-gate voltage rating $V_{dg}^{max} = 1.5$ V and the supply voltage $V_{DD} = 0.9$ V, a pseudo-differential pair is capable of a maximum differential zero-peak voltage swing of about $V_{max} = 1$ V. This constraint directly translates into an optimal load resistance of $R_{opt} \approx 15\ \Omega$.

The required impedance transformation and the differential-to-single-ended conversion are provided by the matching network MN6 (Fig. 3). Since the losses of MN6 are critical to the efficiency of the TX path, this output matching network is designed with particular emphasis on efficiency. Doubly tuned transformer networks can be optimized differently, depending on the specific design goal that is prioritized. To achieve high efficiency, the magnetic coupling of the transformer is to be maximized, while the network has to be operated at its lower parallel resonance frequency [47], [48]. The transformer in MN6 is realized with a stacked layout using the top three metal layers of the back-end-of-the-line; the two-turn inductor connected to the ANT port is placed in the middle, while two shunted windings, realized with metals above and below, make up the coil connected to the PA transistors. This solution allows to achieve a relatively large magnetic coupling while maintaining the quality factor of the coils high.

III. Up/Down Quadrature Frequency Conversion

As shown in Fig. 2, a bidirectional up/down converter complements the bidirectional RF front end discussed in Section II, providing a frequency conversion feature to the module. The up/down converter is made of two passive mixers driven by quadrature LO signals, whose generation is described in Section III-D. At IF, quadrature phase shifting (for TX operation) and quadrature recombination (in RX mode) are performed by a single hybrid coupler, interfaced to the IF amplifiers (Fig. 2). In the following, insights on the operation and design of the bidirectional mixer and a detailed description of the IF amplifiers are provided.

A. Conversion Gain of the Up/Down Converter

The core of the bidirectional up/down frequency converter is shown in Fig. 8. At the IF side, the mixers are connected to ports 2 (THRU) and 3 (CPL) of a differential quadrature hybrid operating at 3 GHz. In the TX mode, the IF signal to be upconverted is fed to port 1 (IN) of the hybrid, while in the RX mode, the downconverted RF signal is made available at port 4 (ISO) of the hybrid. At the RF side, the signals of the mixers in the in-phase and quadrature paths are combined. The mixers are then connected to the RF front end shown in Fig. 3 and described in Section II. Notice that, in Fig. 8, the RF front end is simply modeled as a Norton equivalent circuit made of the load impedance Z_L in the TX mode and by the source impedance Z_S and the current source I_{RF} in the RX mode. The purpose of the inductors L_x (Fig. 8) will be discussed momentarily.

The transistor-level schematic of each mixer is reported in Fig. 9. The switches are implemented as transmission gates,

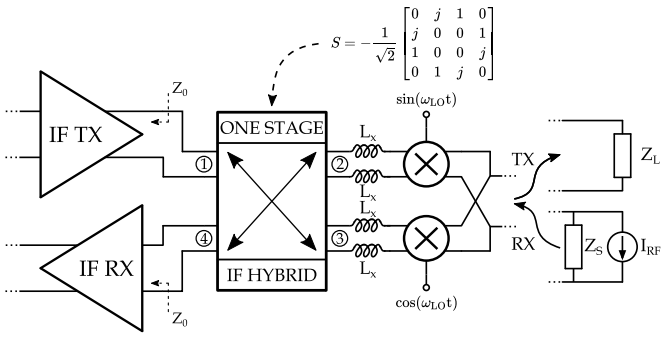

Fig. 8. Block diagram of the bidirectional up/down converter.

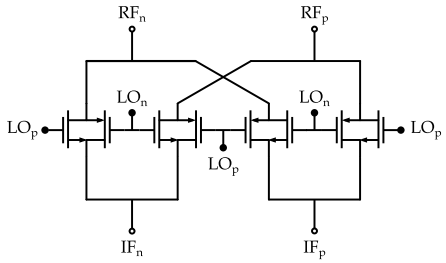

Fig. 9. Schematic of the proposed passive mixer based on transmission gates.

driven by anti-phase LO signals, yielding an improved linearity (important in TX mode), compared to n-type (or p-type) only pass transistors, due to a more constant ON-resistance, R_{SW}, across the signal excursion [50], [51]. In the proposed implementation, $R_{SW} = 10\ \Omega$. A 25% duty-cycle LO is commonly adopted to drive passive mixers in RF transceivers, resulting in a higher conversion gain and in the suppression of undesirable crosstalk between the in-phase and quadrature paths [52], [53]. However, the generation of such an LO at mm-Wave is challenging and power hungry. Thus, a 50% duty-cycle LO is used in this work, similar to the RXs in [54] and [55].

Because of the bidirectional arrangement of the proposed up/down converter, the selection of an appropriate characteristic impedance, Z_0, for the IF hybrid coupler is relevant to have a balanced conversion gain between the TX and RX modes of operation. In order to single out an optimal Z_0 value, expressions of the conversion gain in TX and RX modes are needed, which we will derive under strong simplifying assumptions. The results, although being but a coarse approximation of the actual behavior of the circuit, will convey significant design insight.

We carry out our analysis assuming an ideal behavior for the IF hybrid coupler, which can consequently be described by the scattering matrix reported in Fig. 8. We further assume that the IF amplifiers connected to ports 1 and 4 of the hybrid are matched to Z_0 and that the RF front-end equivalent impedances are purely resistive, i.e., $Z_L = R_L$ and $Z_S = R_S$. In other words, we assume that the up/down frequency converter is time-variant but memoryless. In this scenario, the up/down frequency converter can be described by the equivalent models shown in Fig. 10. In downconversion, the behavior of the circuit is described by the model in Fig. 10(a).

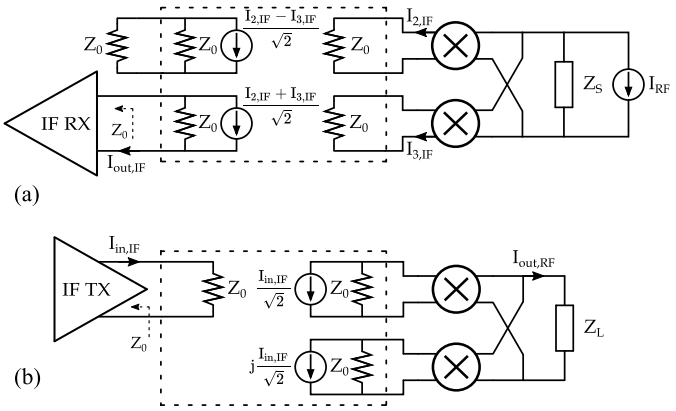

Fig. 10. Simplified equivalent model of the up/down converter in (a) RX mode and (b) TX mode.

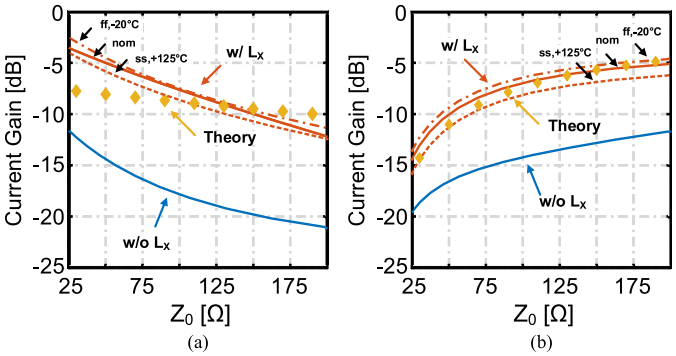

Fig. 11. Simulation of the current conversion gain versus Z_0 and comparison to (5) and (6) in (a) reception and (b) transmission.

The conversion gain, in this case, can be computed to be

$$\frac{I_{\text{out,IF}}}{I_{\text{in,RF}}} = \frac{2}{\pi\sqrt{2}} \frac{R_S}{R_S + Z_0/2 + R_{\text{SW}}} \tag{5}$$

where R_{SW} is the ON-resistance of the mixer switches. In upconversion, the behavior of the circuit is described by the model in Fig. 10(b). The conversion gain, in this case, can be computed to be

$$\frac{I_{\text{out,RF}}}{I_{\text{in,IF}}} = \frac{4}{\pi\sqrt{2}} \frac{Z_0}{Z_0 + 2R_L + 2R_{\text{SW}}}. \tag{6}$$

From (5) and (6), it is clear that the selection of Z_0 sets a tradeoff between the conversion gain in reception and transmission because a low Z_0 favors the gain in downconversion, while a high Z_0 improves the gain in upconversion. In both cases, as intuitively expected, a larger R_{SW} penalizes the gain. In the proposed design, $Z_0 = 100\ \Omega$ is selected as an optimal compromise to obtain a balanced conversion gain in the RX and TX modes.

In Fig. 11, the simulated upconversion and downconversion gain of the circuit in Fig. 8, while setting a nil L_x, is reported, and compared to (5) and (6). The discrepancy between simulations and analytical derivations is remarkable and urges to reconsider the assumptions of our analysis. Since the passive mixer is transparent and does not provide any isolation between the impedances connected to its ports, the memory elements present in the circuit interact with each other, influencing the behavior of the frequency converter in a complex and sometimes cumbersome way [56]–[58]. In particular, every time the mixer switches commutate, there might be a discontinuity in the state variables of the inductors and capacitors connected to them (i.e., the currents through the inductors and the voltages across the capacitors), leading to additional losses in the circuit, notches, and/or frequency shifts in the harmonic transfer functions of the system and other non-intuitive consequences [57]. In our case, the impedances at the hybrid ports are equal to Z_0 around the $f_{\text{IF}} = 3$ GHz IF, but they differ at all the other frequencies that are relevant for the mixer operation, namely, $kf_{\text{LO}} \pm f_{\text{IF}}$, where k is an integer and f_{LO} is the LO frequency. Likewise, the RF front end shows resistive impedances in the 22–31-GHz passband, while this is not the case around the higher LO harmonics. In summary, the interaction between the memory elements at the various ports of the passive quadrature mixer is identified as the main source of the decrease of conversion gain observed in Fig. 11.

To increase the conversion gain of the proposed circuit, the isolation between the RF and IF ports of the quadrature mixer is to be improved, especially at higher frequencies. To this aim, small inductors, $L_x \approx 150$ pH, are employed, following an approach similar to [58]. Fig. 11 shows that the introduction of L_x significantly increases the conversion gain to levels close to the predictions of (5) and (6), with robustness over the process variations corners. The performance of the frequency converter is thus improved. Moreover, this suggests that if the circuit memory elements connected at the mixer ports are kept sufficiently isolated from each other, the assumptions leading to (5) and (6) are reasonably satisfied.

B. IF Quadrature Hybrid Coupler

An equivalent schematic of the differential IF quadrature hybrid coupler is shown in Fig. 12. The conventional coupled transmission lines are replaced by equivalent LC coupled π-networks, which results in a more compact implementation at 3 GHz [38], [49], [54]. For a given (differential) characteristic impedance Z_0 and desired operation frequency $\omega_{\lambda/4}$, we have

$$L = \frac{Z_0}{2\omega_{\lambda/4}\sqrt{1-k^2}}, \qquad C = \frac{2}{Z_0\omega_{\lambda/4}\sqrt{1-k^2}} \tag{7}$$

where $C = C_G/(1-k) = C_M/k$ and k is the magnetic coupling. By selecting $k \approx 0.7$, the transformer-based hybrid coupler is designed with $L = 3.75$ nH and $C = 1.5$ pF. Similar to [49], the various coil windings are arranged in an interleaved layout. The magnetic coupling between positive and negative half-circuits is leveraged to reduce the size of the coils and save die area such that the implementation of the differential quadrature hybrid coupler occupies a single transformer footprint, measuring $360 \times 360\ \mu\text{m}^2$.

C. IF Amplifiers

The amplifying stages in the IF section are shown in the block diagram of Fig. 2. The RX and TX paths share the same pad for the off-chip interface through a

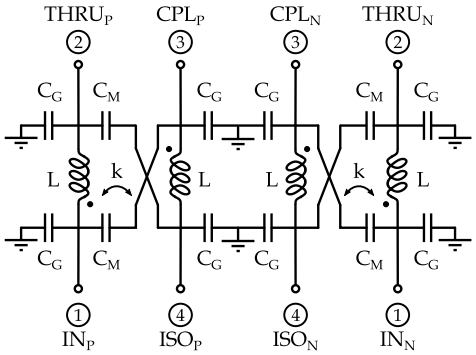

Fig. 12. Equivalent schematic of the differential IF hybrid coupler.

transformer-based matching network, which also provides single-ended-to-differential conversion.

The RX path, fed by the signal at port 4 of the hybrid coupler, is made of a variable attenuator followed by a transimpedance amplifier (TIA), a cascode stage (CS), and a buffer (RX BUF). The schematic of the TIA with input variable attenuator is shown in Fig. 13(a), while the schematic of CS is reported in Fig. 13(b).

The differential TIA is made of a common-gate stage [transistors M_2 in Fig. 13(a)] with shunt–shunt feedback, implemented by transistors M_1, which lowers the input impedance. This topology is a passband variation of the one presented in [46]. Shunt inductors L_B have a moderate quality factor. They feed the dc bias current and resonate out all the parasitic capacitances at the output nodes of the TIA. The variable attenuator placed at the TIA input has the purpose of terminating the hybrid coupler to its characteristic impedance while introducing a coarse RX gain control. It is implemented as a 4-bit R–$2R$ ladder network with switches that route the currents in the various branches of the ladder either to a differential ac ground or to the low-impedance input of the TIA stage. The differential input impedance of the ladder, $Z_{\rm IN}$ in Fig. 13(a), does not depend on the switch configuration, thus offering a constant termination to the hybrid coupler as the RX gain is changed. To obtain a constant-in-dB gain variation, only a subset of the possible ladder configurations is used. As a consequence, the variable attenuator covers a 24-dB gain variation range in 6-dB steps.

Following the TIA, the dc-coupled CS increases the total gain of the RX IF path. Fine gain control is achieved in this stage using current steering. The cascode quad [M_4 in Fig. 13(b)] is segmented in a bank of four binary-weighted blocks, implementing a 4-bit gain control. The last stage of the RX IF amplifying chain (RX BUF in Fig. 2) is a cascode stage, which drives the IF bidirectional interface, made of a doubly tuned transformer network.

Moving from the IF input toward the mixers, the TX path is made of a programmable resistive attenuator for gain control, followed by a two-stage amplifier. The attenuator provides up to 20-dB gain variation in ≈1-dB steps and can be disconnected from the IF transformer using transmission gates, to avoid loading the IF output buffer in the RX mode.

The schematic of the TX IF amplifier is shown in Fig. 14. The first stage is a transconductor based on complementary

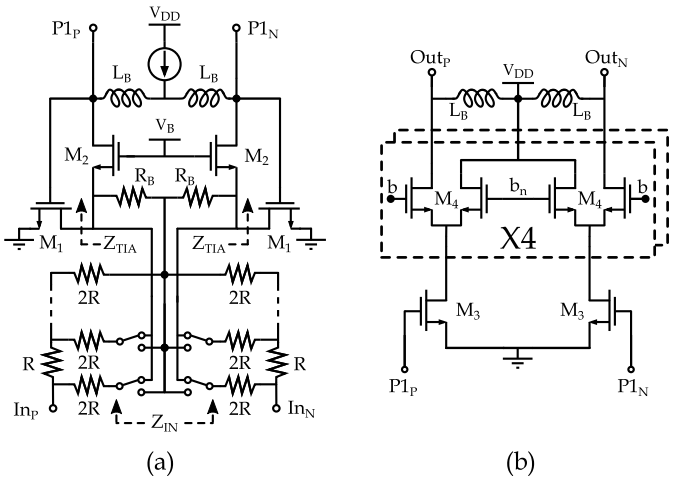

Fig. 13. Schematics of (a) IF RX TIA with R–2R ladder programmable attenuator and (b) IF RX cascode stage with current-steering gain control.

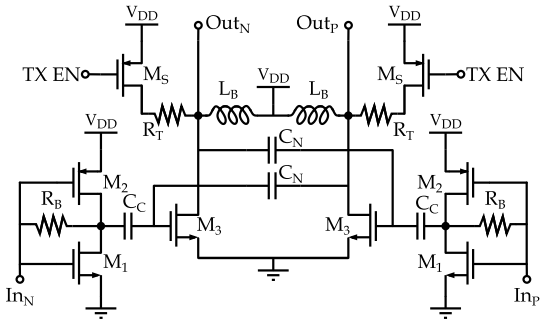

Fig. 14. Schematic of the two-stage IF TX amplifier.

transistors. To obtain a higher voltage swing, the second stage is a pseudo-differential pair with nMOS transistors only, supplied through the center tap of a low-Q inductor, which resonates with the parasitic capacitors at the output nodes. Capacitive neutralization is introduced to enhance the differential-mode stability. In the RX mode, the TX IF amplifier is turned off, while transistors M_S in Fig. 14 are turned on, such that resistors R_T provide the required termination at port 1 of the hybrid coupler.

D. LO Quadrature Generation Chain

With an IF signal at 3 GHz, the target of 22–31-GHz output RF frequency range requires LO signals covering the 19–28-GHz range. The block diagram of the quadrature LO generation chain is shown in Fig. 15. The matching network MN7, realized with a doubly tuned transformer, provides single-ended-to-differential conversion and a broadband input termination. Then, a buffer (LO BUF in Fig. 15), realized with a neutralized pseudo-differential nMOS pair, feeds the quadrature generation network through another doubly tuned transformer network (MN8 in Fig. 15). Wideband quadrature signals are generated with cascaded differential hybrid couplers, implemented with lumped elements [38], [49], [54], as opposed to high-order RC–CR polyphase filters (PPFs) [59] or single-stage calibrated PPF [46], which would require

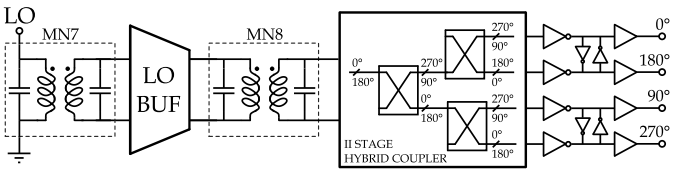

Fig. 15. Block diagram of the LO quadrature generation chain.

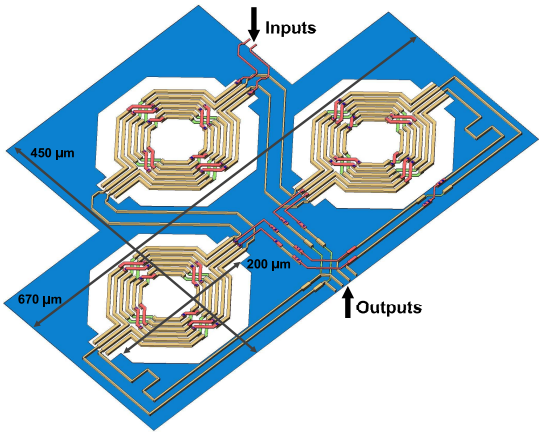

Fig. 16. 3-D view of the two-stage LO hybrid coupler.

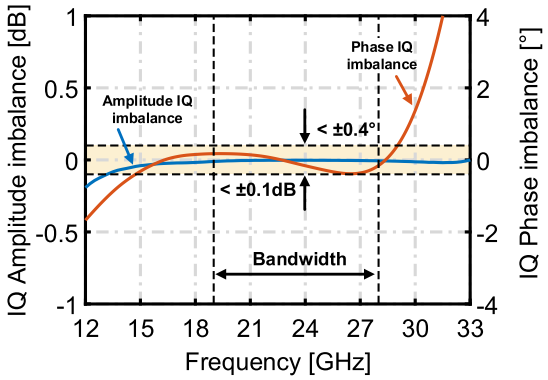

Fig. 17. Simulated amplitude and phase I/Q imbalances of the LO chain.

additional power consumption to compensate for the network losses at mm-Wave.

A two-stage cascade of differential hybrid couplers results in small I/Q phase and amplitude imbalances over the wide target 19–28-GHz band, as the I/Q magnitude and phase errors at the output of the first stage are compensated by the subsequent stage, substantially extending the useful operation bandwidth [49]. A 3-D layout view of the implemented quadrature generation network is shown in Fig. 16.

The quadrature generation network is followed by three-stage inverter-based buffers that drive the mixers. After the first buffer stage, back-to-back inverters are used to improve the common-mode rejection and the waveform 50% duty cycle. Overall, the designed LO quadrature generation chain attains very small I/Q amplitude and phase imbalances, as illustrated by the simulation results presented in Fig. 17. In the bandwidth of interest, the quadrature and amplitude errors are within ±0.4° and 0.1 dB, respectively.

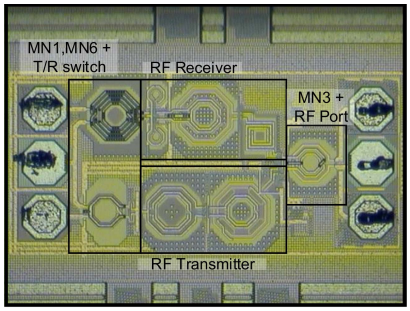

Fig. 18. Microphotograph of the RF front end [23].

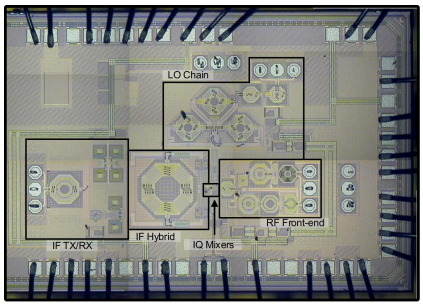

Fig. 19. Microphotograph of the up/down frequency converter chip.

IV. Measurement Results

Prototypes of the RF front end presented in Section II and the complete bidirectional up/down converter module discussed in Section III were realized in a 28-nm bulk CMOS technology. The chip microphotographs are shown in Figs. 18 and 19 for the RF front end and the up/down converter, respectively. The RF front end occupies a compact area of 0.25 mm^2, while the area of the up/down converter is 1.15 mm^2. In the following, detailed measurement results of both circuits are reported.

A. RF Front End

The measured and simulated S-parameters of the TX path of the RF front end are reported in Fig. 20. The TX path transducer gain, $G_{T,\mathrm{TX}}$, has a 3-dB bandwidth spanning from 22 to 31 GHz, with a peak value of 19 dB. The measured input reflection coefficient $\Gamma_{\mathrm{in,TX}}$, which is below −13 dB over the band of interest, demonstrates good matching between the RF port and the TX common-gate input stage. The agreement among measurements and simulations is excellent.

The measured and simulated S-parameters of the RX path of the RF front end are shown in Fig. 21. The measured RX transducer gain, $G_{T,\mathrm{RX}}$, has a peak of 17 dB with a 3-dB bandwidth spanning from 22 to 30.6 GHz. Good matching is observed at the ANT port, with the reflection coefficient, $\Gamma_{\mathrm{in,RX}}$, smaller than −10 dB from 24 to 31 GHz. Fig. 21 also reports the measured and simulated NF. The minimum measured NF is 4.9 dB, with small fluctuations across the RX passband. The RX path consumes 35 mW from 0.9-V voltage supply. As for the TX path case, very good agreement between measurements and simulations is observed.

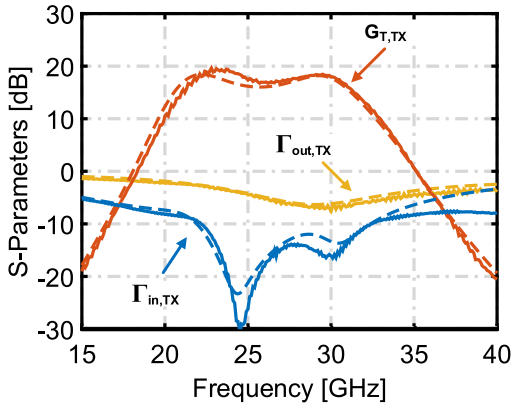

Fig. 20. Measured (solid line) and simulated (dashed line) *S*-parameters of the TX RF front-end path.

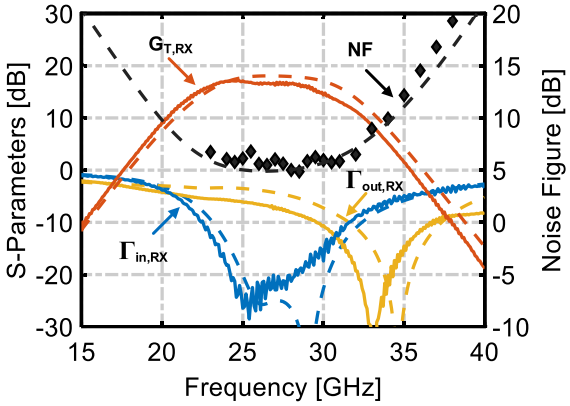

Fig. 21. Measured (solid line) and simulated (dashed line) *S*-parameters of the RX RF front-end path.

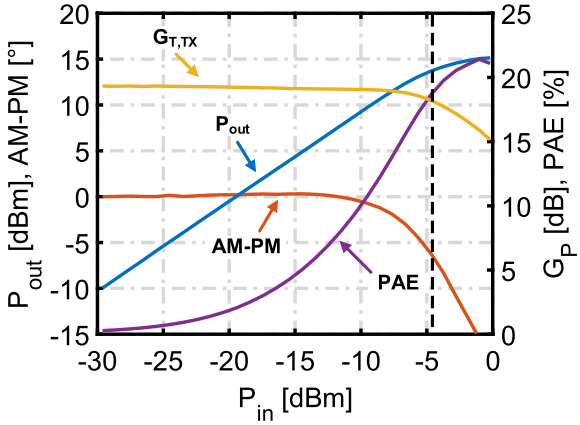

Fig. 22. Measured large-signal CW performance of the TX front end.

The linearity of the TX front end is evaluated by means of large-signal tests. Fig. 22 shows the measured performance with a 28-GHz test signal. The TX measured output-referred 1-dB compression point is 14 dBm, with a corresponding power-added efficiency (PAE) of 18.7%. Up to the compression point, the measured AM-PM distortion is lower than 6°. The RX linearity is instead evaluated by means of a two-tone test, which shows an input-referred IP3 of −9.2 dBm at 28 GHz.

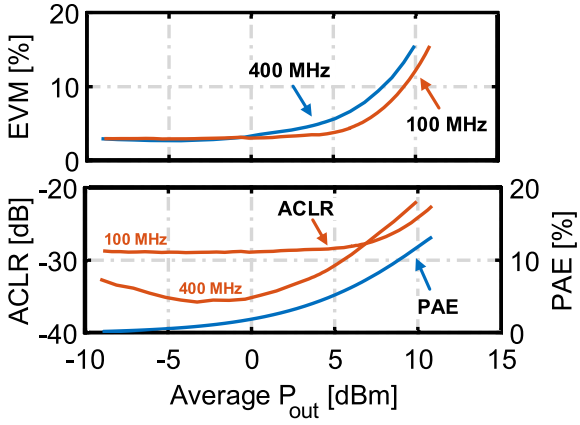

Fig. 23. Measured EVM, ACLR, and corresponding PAE, versus average output power of the TX front end.

The viability of the TX front end for 5G communication systems is verified using modulated input signals. The selected modulation for the test signals is 64-QAM orthogonal frequency-division multiplexing (OFDM). Two 100- and 400-MHz channel bandwidths are used to evaluate the impact of the TX frequency response on the error vector magnitude (EVM). The two test signals show a slightly different PAPR depending on the channel bandwidth, that is, 9.6 and 10.4 dB for the 100- and 400-MHz cases, respectively. The carrier frequency is set to 29 GHz in both cases. Fig. 23 reports the measured EVM versus the average output power for both modulated test signals. The TX front end displays an EVM equal to 5% at an average output power of 6.6 and 4.3 dBm, with a corresponding PAE of 7% and 4.5%, for the 100- and 400-MHz test signals, respectively. Over the operating 24–31-GHz band, the average output power at 5% EVM changes as little as 1.3 dB. The measured adjacent channel leakage ratio (ACLR) is always lower than −28 dBc.

A 5G NR standard-compliant signal is also employed to test the TX front end. The signal bandwidth is 400 MHz and the PAPR is 8.1 dB. The carrier frequency is 28 GHz. Results are reported in Fig. 24. The average output power at 5% EVM is 6.2 dBm, while the ACLR is below −28 dBc. Fig. 24 also shows the TX spectrum and the demodulated signal constellation.

The performance of the proposed transceiver front end is summarized in Table II and compared to state-of-the-art 5G transceiver designs in CMOS technology. With respect to the literature, the proposed front end shows very broadband operation with small area occupation and competitive power consumption.

B. Up/Down Converter Module

The IF and RF pads are shared between TX and RX paths, requiring two different setups for the characterization of the designed module. During reception, the 22–31-GHz RF or the 16–25-GHz image (IM) signal, generated by a continuous-wave (CW) signal source, are fed to the RF port, while the output IF signal is measured with a spectrum analyzer. During

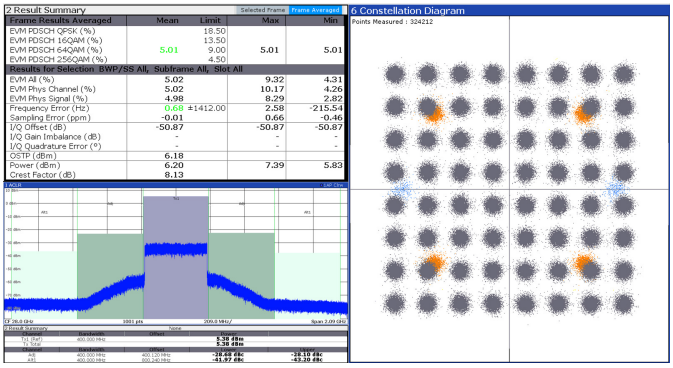

Fig. 24. Measured TX front-end constellation and spectrum with a 5G NR test signal.

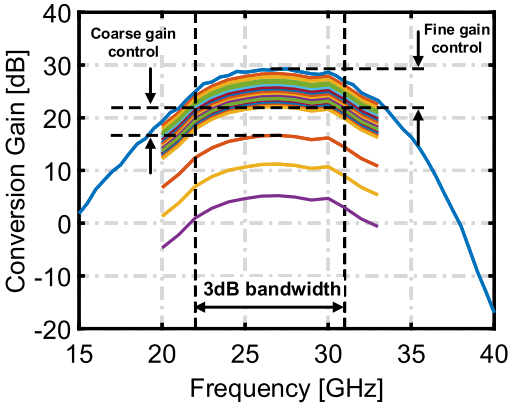

Fig. 25. Measured conversion gain of the up/down converter in the RX mode for different gain settings.

TABLE II

PERFORMANCE SUMMARY OF THE RF FRONT END AND COMPARISON WITH THE LITERATURE

	This Work	[15]	[14]	[11]	[16]
CMOS Tech.	28 nm	65 nm	65 nm	28 nm	65 nm
Freq. [GHz]	22-31	27	26.5-29.5	28.5	24-28
Supply [V]	0.9	1	-	1.05	-
TX gain [dB]	19	35	20	35	27*
TX P_{1dB} [dBm]	14	14.4	11.3	9.5	16.1
TX PAE_{1dB} [%]	18.7	14.5	-	8.5	16.6
RX NF [dB]	4.9	5.9	4.2-5	5.6	4.4
RX gain [dB]	17	25.5	17	24	23.2
$P_{DC,RX}$ [mW]	35	50	112	50	40
Area [mm^2]	0.25	0.26	0.58	0.52	0.94

* Graphically estimated.

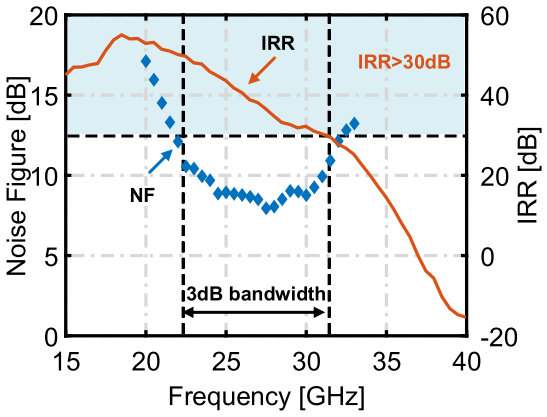

Fig. 26. Measured NF and IRR of the up/down converter in reception.

transmission, the 3-GHz IF signal, generated by a CW signal source, is fed to the IF port, while the output spectrum at RF is measured with a spectrum analyzer. The 19–28-GHz LO signal is generated by an additional CW signal source and injected into the LO port in both TX and RX setups.

The converter RX path has a peak conversion gain of 29 dB with a 3-dB bandwidth spanning from 22 to 31 GHz. Up to 30-dB gain variation is achieved using the 0.5-dB/step fine control, combined with the 6-dB/step coarse control mechanism, as shown in Fig. 25. The measured NF has a minimum value of 8.5 dB, at maximum RX gain setting, with small fluctuations in the wide RX passband (Fig. 26). Compared to the measured NF of the stand-alone RF front end, reported in Fig. 21, the loss introduced by the passive quadrature downconverter degrades the noise performance; the NF is, however, kept below 10 dB. To further desensitize the RX NF from the losses introduced by the passive mixer, in a redesign of the module, additional gain stages should be introduced before the mixing stage.

The RX IRR, measured at maximum RX gain, is reported in Fig. 26. It exceeds 30 dB even at the upper edge of the passband, where the image signal falls in-band, which is in line with the state of the art, as shown in Table III. The linearity of the RX path is evaluated by means of a two-tone test, which yields an input-referred IP3 of -19.3 dBm at the maximum gain setting. The measured input-referred IP3 increases to -13.9 dBm when the gain is decreased by 10 dB.

The peak conversion gain of the converter TX path is 22 dB, with a bandwidth extending from 22 to 31 GHz, similar to the RX case. The gain variation feature allows for up to 20-dB gain variation in constant 1-dB steps, as shown in Fig. 27. The purity of the TX output spectrum is evaluated by means of LO leakage and IRR, which are reported in Fig. 28. When the LO frequency falls in-band, the LO leakage measures -30 dBm, with small variations across the passband. The TX IRR is excellent: it is larger than 40 dB over the TX passband. This performance is also confirmed in Fig. 29, which shows the measured output spectrum for $f_{RF} = 31$ GHz.

Large-signal tests were performed to evaluate the linearity of the converter TX path. The measured performance with a test signal at 28 GHz is reported in Fig. 30. The TX shows an output-referred 1-dB compression point equal to $OP_{1\,dB} = 12$ dBm, which is slightly lower compared to the $OP_{1\,dB}$ of the stand-alone RF front end, reported in Fig. 22. This decrease of $OP_{1\,dB}$ was tracked down to be due to the limited linearity of the TX IF amplifier. The measured overall PAE at $OP_{1\,dB}$ is 7.25%, which accounts for the power consumption of the upconverter, the quadrature LO generation, and the RF front end.

TABLE III

PERFORMANCE SUMMARY OF THE UP/DOWN CONVERTER AND COMPARISON WITH THE STATE OF THE ART

	This Work	[1]	[2]	[4]	[10]	[11]	[12]	[19]	[24]	[38][e]
Technology	28 nm CMOS	120 nm SiGe	65 nm CMOS	130 nm BiCMOS	130 nm BiCMOS	28 nm CMOS	28 nm CMOS	28 nm CMOS	65 nm CMOS	45 nm CMOS SOI
RF Frequency [GHz]	22 – 31	22.6 – 31.6	26.5 – 29.5	22 – 44	27 – 29	25.8 – 28	25 – 32.5	37 – 40	28/37	24.5 – 43.5
IF Frequency [GHz]	3	BB	4	2 – 7	3	BB	6.5	10.8/11.2	BB	3.5
3-dB Bandwidth (TX/RX) [GHz]	9/9	3.9/8.4	3/3	22/22	2/2	2.2/2.2	7.5/5.5	1.5/1.5	2.5/2.5[d]	-/19
TX Gain [dB]	2 – 22	18.4 – 26.6	0 – 10	-2 – 18	28 – 36	-	34 – 44	30 – 60	43.5/40	-
TX OP_{1dB} [GHz]	11.5	11.9 – 13.7	14 – 15.7	8 – 9	13.5	10	12	8.8	14/14.2	-
TX IRR [dB]	40	25	40	30	-	60	-	-	30/26	-
TX P_{DC} [mW]	220[a]	465	299[b]	480	143.8	680 (8 ch.)	360 (4 ch.)	1840 (16 ch.)	169	-
RX Gain [dB]	5 – 29	12.7 – 13	0 – 10	-6 – 18	30 – 36	30 – 69	32 – 34	16 – 59	44/37	17 – 35
RX NF [dB]	8.5	8.6	4.1[c]	11	6	6.7	4.4	4.2	7.9/8.8	5.3[f]
RX IRR [dB]	30	-	40	-	-	-	-	-	35/35	32.5
RX P_{DC} [mW]	110	297	148	380	103.1	400 (8 ch.)	168 (4 ch.)	624 (16 ch.)	99	60

[a] at OP_{1dB} [b] at 5 dB back-off [c] without T/R switch [d] TX/RX at both 28 GHz and 37 GHz RF frequency [e] RX only [f] with T/R switch

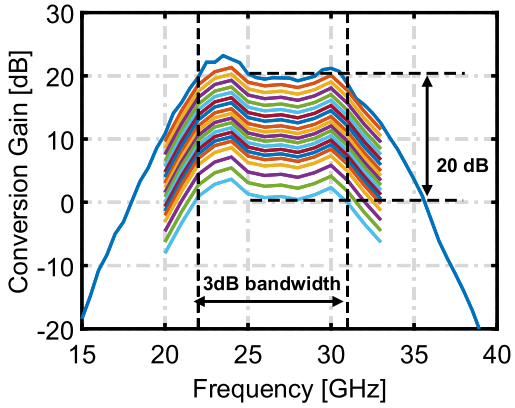

Fig. 27. Measured conversion gain of the up/down converter in the TX mode for different gain settings.

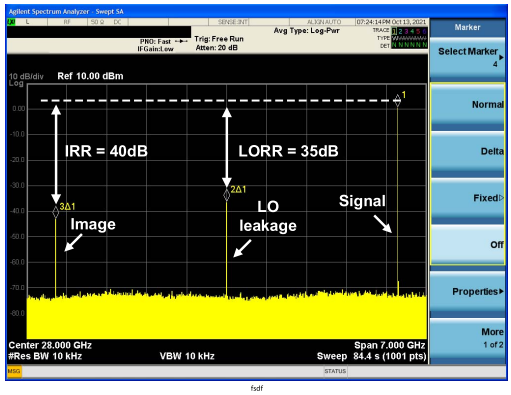

Fig. 29. Measured output spectrum of the up/down converter, showing IRR and LO leakage for a 31-GHz desired TX output signal.

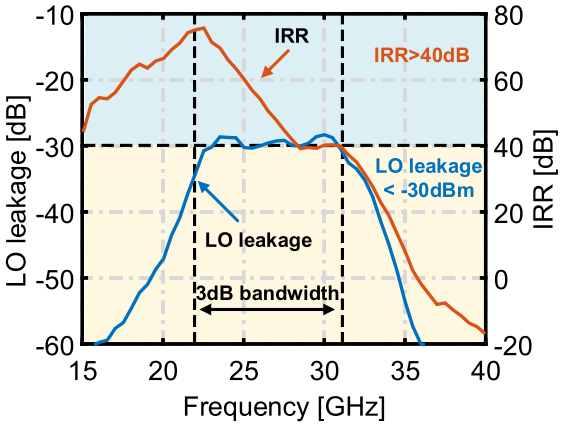

Fig. 28. Measured LO leakage and IRR of the up/down converter in transmission.

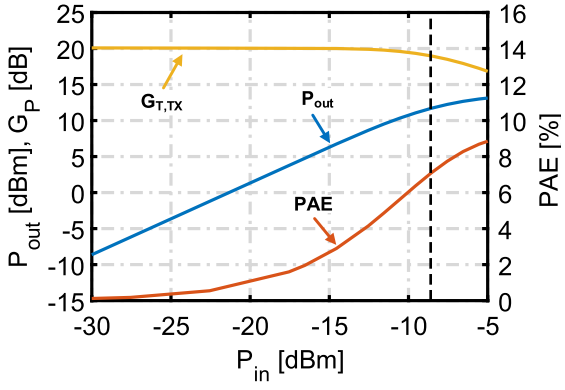

Fig. 30. Measured large-signal CW performance of the TX path of the up/down converter.

The TX path of the up/down converter is tested with a 5G NR standard-compliant signal. The signal bandwidth is 400 MHz, the PAPR is 9.3 dB, and the carrier frequency is 28 GHz. The results are reported in Fig. 31. The measured average output power at 5% EVM is 5.2 dBm. Compared to the performance of the stand-alone RF front end, reported in Fig. 24, the average output power at 5% EVM is slightly

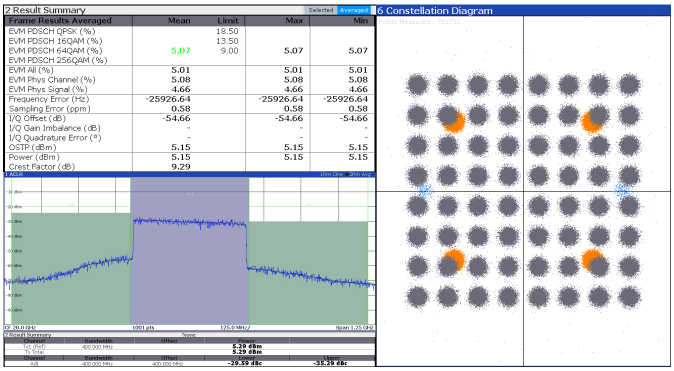

Fig. 31. Measured constellation and spectrum with a 5G NR test signal of the up/down converter in transmission.

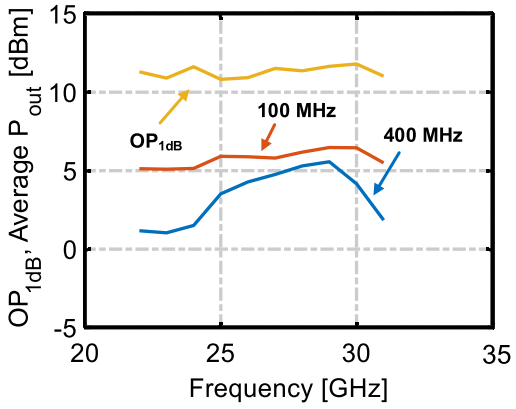

Fig. 32. Measured $OP_{1\,dB}$ and average output power of the up/down converter in transmission at 5% EVM.

decreased, as a result of a reduced $OP_{1\,dB}$. The measured ACLR is below −29 dBc. Fig. 31 also shows the TX spectrum and the demodulated signal constellation. Eventually, Fig. 32 shows the measured $OP_{1\,dB}$ and average output power at 5% EVM across the TX bandwidth. Results from tests with signals with a 100-MHz bandwidth are also reported. Overall, the linearity of the mixer and IF amplifier does not considerably affect the linearity of the whole up/down converter module.

The performance of the proposed bidirectional image-reject up/down converter module is summarized in Table III and compared to state-of-the-art 5G transceivers. With respect to the literature, the designed up/down converter module is the only CMOS implementation covering the whole 24.25–29.5-GHz frequency range with margin, while featuring state-of-the-art IRR in both transmission and reception, achieved by the proposed bidirectional image-reject architecture.

V. Conclusion

This article presented the design of a broadband bidirectional transceiver front end and its integration into a complete image-reject up/down converter module in a bulk 28-nm CMOS technology. Doubly tuned transformer-based matching networks are used to broaden the circuit bandwidth without forsaking compactness, achieving a 22–31-GHz RF passband in both transmission and reception. The proposed solution demonstrated the first bulk CMOS transceiver capable to cover all the 5G NR sub-bands that have been allocated around 28 GHz. Leveraging wideband matching network design, the proposed transformer-based T/R switch offers a compact and low-loss solution, which is suitable for bidirectional applications in TDD systems. Furthermore, the issue of the image rejection in broadband low-IF transceivers has been tackled by introducing a bidirectional image-reject up/down converter, which achieves an IRR in excess of 30 and 40 dB in the RX and TX modes, respectively.

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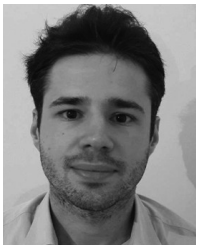

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