Ultra-Low-Power Low-Input-Voltage Charge Pump for Micro-Energy Harvesting Applications

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***Abstract*— A subthreshold input voltage charge pump based on the well-known cross-coupled voltage doubler and using boosted gate voltages for the transfer switches is presented. A level shifter and some inverters, including a novel inverter architecture proposed in this work and referred to as negative low-state voltage inverter, are used to generate the clock signals for the switching transistors with the purpose of significantly improving their drive capability. A complete analysis of the proposed charge pump is provided to highlight the advantages of the implemented structure, revealing the power efficiency improvement when the input voltage is below the threshold voltage of the transistors. An extensive experimental characterization of silicon prototypes in 180 nm CMOS technology was carried out, showing that the proposed scheme is able to pump charge from an input voltage as low as 110 mV. The experimental peak efficiency remains above 70% for input voltages between 180 mV and 400 mV and input power levels from 45 nW to 25 μW, which are appropriate for different miniaturized transducers implementable on chip.**

***Index Terms*— Charge pump, gate voltage boosting, low power, low voltage, subthreshold, switched capacitor DC-DC converter.**

I. Introduction

HARVESTING energy from the environment has become a very suitable option for supplying IoT nodes, especially in wearable and bio-implantable devices, where finite battery life is a major drawback. In miniaturized energy harvesting powered devices, the available sources and amount of energy are very limited, making it essential to use circuitry capable of operating with very low power consumption as well as with low supply voltages.

DC-DC converters, in particular voltage boosters, are an essential block in an energy harvesting powered device, where a low voltage often needs to be raised to a usable value to supply the subsequent blocks, for example sensors or communication modules, or to charge a battery or any energy reservoir. DC-DC converters can be mainly classified as switched inductor or switched capacitor systems. The former are suitable for high power level applications [1], [2], but are not recommended for integrated circuits because they usually require external inductors, which have low integration density [3], [4]. The latter are more suitable for low power applications and can be implemented fully on chip more successfully [5], [6], [7], [8], [9].

Among switched capacitor DC-DC converters [10], [11], the most widely used topologies to be integrated on chip are Dickson charge pump (CP) [12], [13], [14], [15] and the cross-coupled (CC) voltage doubler [16], [17], [18], [19], [20], [21]. Previous publications demonstrated that the CC voltage doubler structure offers better power efficiency than Dickson CP [22]. Furthermore, Dickson topology usually needs additional circuitry to properly drive the switches. On the other hand, in the CC voltage doubler CP, when the input voltage drops below the threshold voltage of the switching transistors (subthreshold input voltage), the on-resistance of the switches becomes very high, thus making the drive capability of these devices too small to be used in a practical application. One possible solution could be to use devices with low threshold voltage or apply forward body biasing [23], [24], [25], [26] to reduce the effective threshold voltage of the switches but, in this case, the leakage current increases exponentially, and so do the power losses due to this effect. An alternative option to avoid these problems is to use a boosted voltage at the gate of the switching transistors to increase their overdrive voltage. This boosted voltage can be generated by using either an auxiliary charge pump [27] or an additional structure that raises the driving voltage to an adequate value [28], [29], [30], [31], [32], [33].

This paper proposes a low-power low-input-voltage charge pump that consists of four cascaded CC voltage doublers and uses boosted gate voltages in order to significantly improve the drive capability of the switches. The boosted gate voltages are generated by using a level shifter, regular inverters, and

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specific inverters, referred to as negative low state voltage (NLSV) inverters, introduced in this paper that are all supplied by an additional two-stage classical CC charge pump connected to the output of the main charge pump. The overall structure as well as the individual blocks were optimized to reduce the power consumption, thus improving the power efficiency of the whole system. The novel NLSV inverters provide negative voltages to improve the drive capability of the PMOS switches without requiring a dedicated circuit to invert the voltage, which causes a negligible impact on the power consumption. The target of the design is to be part of a fully autonomous micro-energy harvesting system able to work using energy sources with voltage values below 400 mV and power levels from the nanowatt to the microwatt range. These values are in accordance with miniaturized transducers, for instance, solar cells integrated on chip [34], [35], [36]. The circuit was designed to provide at least 1 μW of maximum output power for an input voltage of 250 mV while maintaining good power efficiency, i.e., an efficiency of at least 60%, with input power levels as low as few nW: the constituent circuitry must therefore feature reduced power consumption. A proof of concept chip was fabricated in 180 nm CMOS technology using a total switching capacitance of 1.12 nF integrated on chip. The experimental characterization demonstrated that the proposed implementation is able to pump charge even with an input voltage as low as 110 mV and delivers up to 16.8 μW of output power when the input voltage is 400 mV. The peak power efficiency remains above 70% for input voltages from 180 mV to 400 mV.

The paper is outlined as follows. The boosted-gate CC voltage doubler is introduced in Section II, mathematically justifying its use over the conventional CC structure in the case of a subthreshold input voltage. Section III illustrates the proposed charge pump circuit as well as the novel NLSV inverter, also including a model for power efficiency estimation. Section IV reports experimental characterization results of the fabricated samples. Finally, conclusions are drawn in Section V.

II. Boosted-Gate Cross-Coupled Voltage Doubler

Fig. 1 shows the conventional CC voltage doubler [16] (Φ and $\overline{\Phi}$ are complementary clock phases). This circuit delivers an output voltage, V_{out}, that is equal to the sum of the voltage V_{in1}, plus the switching amplitude applied to the flying capacitors C_{fly1} and C_{fly2}, V_{in2}, in the absence of load current. When $V_{in1} = V_{in2} = V_{in}$, the output voltage will be the double of the input voltage, V_{in}, hence the name of this circuit. The conventional CC voltage doubler works well if the switching voltage amplitude is high enough to power on the switching transistors properly, but its pumping capability degrades significantly when the switching amplitude is reduced or when the load current increases and, hence, the output voltage decreases. To solve this issue, boosted voltages can be used to drive the gates of the switching transistors [17], [37], [38] so as to ensure an overdrive voltage high enough and hence substantially improve the drive capability of these devices.

The effect of the voltages at the gates of the switching transistors is briefly discussed next in order to compare the

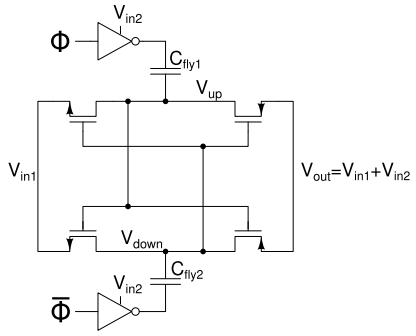


Fig. 1. Cross-coupled voltage doubler.

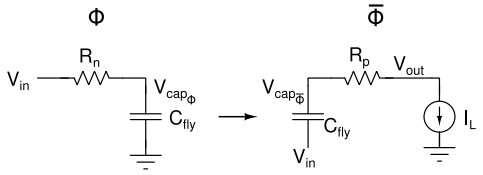


Fig. 2. Model of the CC voltage doubler.

circuit operation in the weak inversion (W.I.) and strong inversion (S.I.) regions of these devices. First of all, the voltage across a capacitor, C, being charged/discharged to a given voltage, V_{ch}, through a resistor, R, can be calculated as

$$V_{cap} = V_{ch} + (V_{initial} - V_{ch})e^{\frac{-t}{RC}} \tag{1}$$

where $V_{initial}$ is the voltage across the capacitor at time $t = 0$.

The output voltage of the CC voltage doubler at steady state, i.e., when the voltage waveform at any node will be identical in all clock cycles, in the presence of a non-zero load current I_L, neglecting the output voltage ripple, and setting $V_{in1} = V_{in2} = V_{in}$ and $C_{fly1} = C_{fly2} = C_{fly}$, can be estimated using the model in Fig. 2. In this figure, which is specifically referred to the upper branch in the CC voltage doubler of Fig. 1, R_n and R_p represent the equivalent on-resistance of the NMOS and the PMOS transfer switch, respectively. As can be seen, during clock phase Φ, the considered branch of the voltage doubler can be modeled as a simple RC circuit following equation (1), so that we can state that the on-resistance, R_n, of the NMOS transistor, has a direct impact on the allowed maximum operating frequency. If the criterion for assuming slow switching limit (SSL) operation is ensuring 95% of charge transferred during the considered half period (Φ high), then the maximum operating frequency in the slow switching regime, $f_{SSL} = 1/T_{SSL}$, can be calculated as follows:

$$e^{\frac{-T_{SSL}}{R_n C_{fly}}} = 0.05 \rightarrow T_{SSL} \approx 3R_nC_{fly} \rightarrow f_{SSL} \approx \frac{1}{6R_nC_{fly}} \tag{2}$$

At the end of phase $\overline{\Phi}$, i.e., from the right side of Fig. 2, we have a constant current across the resistor R_p:

$$V_{cap_{\overline{\Phi}}} = V_{out} + R_p \cdot I_L \tag{3}$$

From the left side of the same figure, we see that, during clock phase Φ, the behaviour of the circuit model follows

equation (1), where the initial voltage is the voltage across the capacitor at the end of previous clock phase $\overline{\Phi}$, $V_{cap_{\overline{\Phi}}} - V_{in}$, so that, at the end of phase Φ, we have

$$V_{cap\Phi} = V_{in} + (V_{cap_{\overline{\Phi}}} - 2 \cdot V_{in}) e^{\frac{-T}{2R_n C_{fly}}} \tag{4}$$

Applying charge conservation in an entire cycle, we obtain

$$C_{fly} V_{cap\Phi} = C_{fly}(V_{cap\overline{\Phi}} - V_{in}) + \frac{I_L T}{2} \tag{5}$$

Then, rearranging the terms and by substituting $T = 1/f$, the output voltage of the CC voltage doubler can be expressed as

$$V_{out} = 2V_{in} - I_L \underbrace{\left(R_p + \frac{1}{2fC_{fly}\left(1 - e^{\frac{-1}{2fR_nC_{fly}}}\right)} \right)}_{\text{Output resistance}} \tag{6}$$

The fraction in the term in parentheses can be split as

$$\underbrace{\frac{1}{2fC_{fly}}}_{\text{switched capacitor resistance}} + \underbrace{\frac{1}{2fC_{fly}\left(e^{\frac{1}{2fR_nC_{fly}}} - 1\right)}}_{\text{NMOS impact on output resistance}} \tag{7}$$

where the first element corresponds to the equivalent resistance of the switching capacitor, R_{SC}, and the second represents the impact of the on-resistance of the NMOS switch on the output impedance of the voltage doubler. Summing the impact of the on-resistance of the NMOS switch and the on-resistance of the PMOS switch, R_p, we have the effect of the on-resistance of the switches on the output impedance of the CP, R_{SW}.

Then, the power loss contribution of the on-resistance of the switches, $P_{R_{SW}}$, can be expressed as

$$P_{R_{SW}} = I_L^2 \left(\frac{1}{2fC_{fly}(e^{\frac{1}{2fC_{fly}R_n}} - 1)} + R_p \right) \tag{8}$$

The dynamic power losses associated to charging/discharging the switches gate capacitance, $P_{D_{SW}}$, can be calculated as

$$P_{D_{SW}} = 2fC_g V_g^2 \tag{9}$$

where C_g is the gate capacitance of the switch transistors in one branch and V_g is the switching voltage amplitude at the gate of these transistors. The total power losses in the switching transistors can therefore be expressed as

$$P_{switch} \approx 2\ fC_g V_g^2 + I_L^2 \left(\frac{1}{2fC_{fly}(e^{\frac{1}{2fC_{fly}R_n}} - 1)} + R_p \right) \tag{10}$$

When the gate-to-source (source-to-gate) voltage of the NMOS (PMOS) switch transistors is far below the module of the threshold voltage (weak inversion condition), the drain-to-source (source-to-drain) conductance can be calculated as [39]

$$G_{n(p)_{W.I.}} = \frac{\partial I_{d_{W.I.}}}{\partial V_{ds(sd)}} \approx I_{sn(p)} \frac{W}{L} \frac{e^{\frac{-V_{ds(sd)}}{V_T}}}{V_T} e^{\frac{V_{ovn(p),W.I.}}{n_{n(p)} V_T}} \tag{11}$$

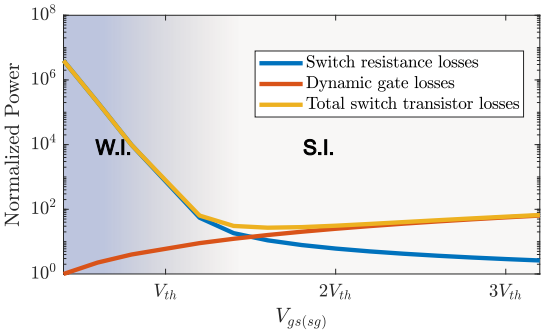


Fig. 3. Evaluation of switch transistor power losses when varying the gate voltage swing.

In the above equation, $I_{sn(p)} = 2n_{n(p)}\mu_{n(p)}C_{ox}V_T^2$ is the characteristic current of the transistors, $n_{n(p)}$ being the subthreshold slope factor, $\mu_{n(p)}$ the electron (hole) mobility, and C_{ox} the gate capacitance, $V_{ovn(p),W.I.} = (V_{gs(sg)} - |V_{thn(p)}|)_{W.I.}$ is the overdrive voltage in the weak inversion condition, V_T is the thermal potential, and $V_{thn(p)}$ is the threshold voltage of the NMOS (PMOS) devices. If the gate-to-source (source-to-gate) voltage of the switches is higher than the module of the threshold voltage (strong inversion condition), the drain-to-source (source-to-drain) conductance can be expressed as

$$G_{n(p)_{S.I.}} = \frac{\partial I_{d_{S.I.}}}{\partial V_{ds(sd)}} = \mu_{n(p)} C_{ox} \frac{W}{L} \left(V_{ovn(p),S.I.} - V_{ds(sd)} \right) \tag{12}$$

where $V_{ovn(p),S.I.} = (V_{gs(sg)} - |V_{thn(p)}|)_{S.I.}$ the overdrive voltage in the strong inversion condition.

The ratio of the resistances in S.I. and W.I. is equal to:

$$\frac{R_{n(p)_{W.I.}}}{R_{n(p)_{S.I.}}} = \frac{G_{n(p)}|_{S.I.}}{G_{n(p)}|_{W.I.}} = \frac{1}{2nV_T^2} \cdot \frac{V_{ovn(p),S.I.} - V_{ds(sd)}}{e^{\frac{V_{ovn(p),W.I.} - n_{n(p)}V_{ds(sd)}}{n_{n(p)}V_T}}} \tag{13}$$

Taking, as example values, $V_{th} = 0.5$ V, $V_{gs,S.I.} = 1$ V, $V_{ds} = 0.05$ V, $V_{gs,W.I.} = 0.25$ V, $n = 1.3$, and $V_T = 0.026$ V, the above ratio takes a value of about $2.8 \cdot 10^6$. The fact to be highlighted here is that if the voltage swing at the switch transistor gates is increased to bring the devices from weak to strong inversion, the power losses due to the switches on-resistance is reduced by several orders of magnitude. At the same time, the power loss due to charging/discharging the gate capacitances is worsened by only a power of two of the corresponding voltage ratios, i.e., by a factor $(V_{gs,S.I.}/V_{gs,W.I.})^2$. When using the example parameters above, the dynamic power loss of charging/discharging the gate capacitances is increased by a factor of only 16. To illustrate the impact of the gate voltage swing on the switches losses, Fig. 3 shows the calculated power, normalized to the minimum plotted value, associated to the channel resistance of the switching transistors and the dynamic losses due to charging/discharging the gate capacitances using expressions (8) and (9), respectively, and the sum of the two contributions following equation (10). As can be seen, the improvement in resistive losses when going out of the sub-threshold regime is much greater than the increase in dynamic losses: the aim of the design is thus to keep the switches in strong inversion when turned on.

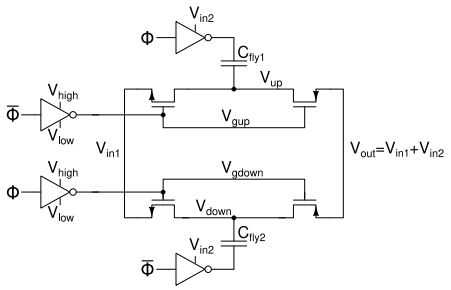


Fig. 4. Boosted-gate cross-coupled voltage doubler.

By inspecting the classical CC voltage doubler in Fig. 1, it is clear that the gate voltages of the switching transistors, V_{up} and V_{down}, will oscillate between V_{in} and $2V_{in}$ while, at steady state, the source voltage of the NMOS device will be equal to V_{in} and the source voltage of the PMOS will be at most equal to $2V_{in}$. Consequently, the gate-to-source (source-to-gate) voltage of the switching transistors will be at most equal to V_{in}, and therefore if V_{in} has a value below the threshold voltage, the switching transistors will operate in weak inversion, thus offering a huge on-resistance. For this reason, the boosted-gate structure shown in Fig. 4 is used in the proposed CP. In the boosted-gate CC voltage doubler, the signals at the gates of the switch transistors are replaced by a clock with high and low levels equal to V_{high} and V_{low}, respectively, with the aim of making the overdrive voltage well above zero and hence significantly improving the drive capability. Besides, using higher signal amplitudes at the gate terminals allows using smaller transistors, so that the gate capacitance is reduced and therefore the dynamic power losses are decreased.

In two previously proposed solutions [37], [38], additional circuitry is used to ensure an oscillation amplitude at the gate terminals of the switch transistors equal to the input voltage even when the load current is high. However, when the input voltage is low, so is the oscillation amplitude and therefore the drive capability. On the other hand, the implementation called low voltage scheme in the paper by Favrat et al. [17] makes use of a level shifter supplied by the output voltage of the charge pump to increase the clock voltage amplitude. The scheme ensures an oscillation amplitude at the gate terminals of the switch transistors equal to two times the input voltage, thus offering better performance for low input voltages than the two above mentioned solutions [37], [38]. However, the gate voltage oscillation amplitude equal to $2V_{in}$ could be a limitation in the case of very low input voltages. The circuit proposed in this paper is based on a level shifter and several inverters, two of which provide a negative low-state voltage (see Section III), supplied with a boosted voltage. The boosted voltage is generated with an additional charge pump connected to the output of the circuit, thus offering a significantly higher gate voltage amplitude than the previously described architectures and, hence, very substantially increasing the drive capability of the switching devices of the charge pump in the subthreshold input voltage condition. Besides, the generated high-amplitude gate voltages are shared between different charge pump stages, thus simplifying the circuit and therefore reducing the dynamic power losses.

III. Proposed Charge Pump Circuit

A. Charge Pump Description

Fig. 5 shows the proposed CP. The input/output pins of the circuit are the input voltage, V_{in}, an external clock signal, Φ, which has a swing amplitude equal to V_{in}, and the output terminal, V_{out}. The CP is composed of four main blocks. The first one (*4-stage boosted-gate CC main charge pump*) is made up of four CC voltage doublers with boosted gate voltages connected in cascade, which generates the output voltage, V_{out}. The second block (*Additional CC doubler CP*) is an additional charge pump, consisting of two cascaded conventional CC voltage doublers, used to increase V_{out} to a boosted value V_{bst}. The third block is the *Level Shifter* [40], [41], [42], [43] used to raise the amplitude, V_{in}, of the input clock to the V_{bst} level, thus generating boosted clock phase $\Phi_{shifted}$. Finally, the fourth block (*Gate voltages generator*) generates the clock signals to be fed to the main CP from signal $\Phi_{shifted}$ and voltages V_{bst} and V_{in}. The *Gate voltages generator* consists of two inverters that buffer the $\Phi_{shifted}$ clock signal, which oscillates between 0 and V_{bst}, and connect it properly to the second, the third, and the fourth stage in the charge pump (clock signals V_{gupi} and V_{gdowni}, $i = 2$ to 4), and two negative low-state voltage (NLSV) inverters that generate the gate signals for the first stage of the charge pump (clock signals V_{gup1} and V_{gdown1}). The reason for using a negative voltage for the low state of the clock signals of the first stage of the CP is to have a sufficiently high source-to-gate voltage for the PMOS transistors in their on state. If a low-state voltage equal to zero were used, when the PMOS switches are *ON*, their source-to-gate voltage would be equal to the output voltage of this stage, V_{o1}, which will be less than $2V_{in}$ when a non-zero load current is demanded at the output. Instead, by using a low state value of the clock signal close to $-V_{in}$, the overdrive voltage of these switches is increased and therefore the switch resistance is decreased, which results in a much higher allowed current flow. In summary, the gate signals of the main charge pump oscillate between $\approx -V_{in}$ and V_{bst} in the first stage and between 0 and V_{bst} in the second, the third, and the fourth gain stages.

All transistors in the circuit in Fig. 5 were implemented with standard devices, with nominal threshold voltages of 462 mV and -490 mV for NMOS and PMOS transistors, respectively, in order to reduce the leakage current and, therefore, the static power consumption. Besides, due to the specified low value of the minimum input voltage, transistors with a threshold voltage lower than that of the standard ones, featuring nominal threshold values of 291 mV and -154 mV for NMOS and PMOS devices, respectively, were used to implement all the inverters that are supplied with voltage V_{in} as well as the M_{1CP} device in the NLSV inverter (Fig. 6).

B. The Negative Low-State Voltage Inverter

To obtain the negative low-state voltage clock signal, the NLSV inverter shown in Fig. 6 is proposed. The NLSV inverter consists of a conventional inverter, composed of transistors M_{Ninv} and M_{Pinv}, and an ancillary charge pump that provides the negative supply voltage, V_{CP}, for this inverter

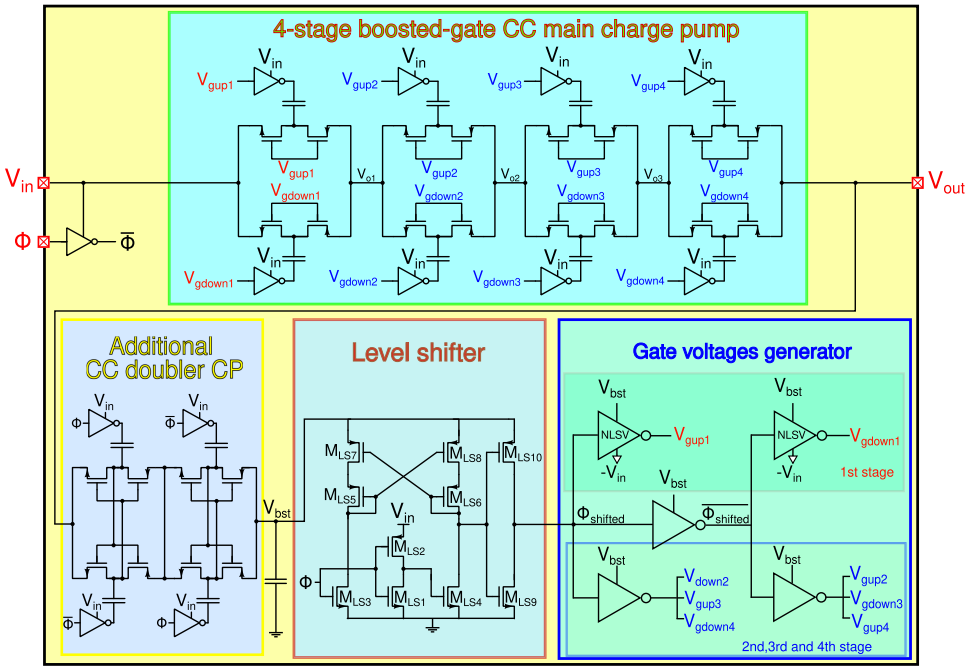


Fig. 5. Proposed Charge Pump.

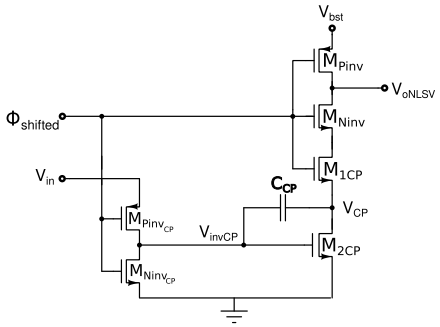


Fig. 6. Negative low-state voltage inverter.

(the positive supply voltage of the inverter is V_{bst}). The negative charge pump is formed by the devices at the bottom in the schematic, namely M_{1CP}, M_{2CP}, $M_{Ninv_{CP}}$, $M_{Pinv_{CP}}$, and C_{CP}. When $\Phi_{shifted}$ is low, M_{Pinv} and M_{2CP} are turned on or, more precisely, have an overdrive voltage that could be below zero but still offer a resistance low enough to make V_{oNLSV} equal to V_{bst} and V_{CP} equal to ground at the end of the phase $\overline{\Phi_{shifted}}$. At this point, the voltages at the right and the left terminal of capacitor C_{CP} are approximately equal to 0 and V_{in}, respectively. When $\Phi_{shifted}$ switches to the high level (V_{bst}), V_{invCP} is lowered to ground through device $M_{Ninv_{CP}}$ while M_{Ninv} and M_{1CP} are turned on: charge is pumped away from the node V_{CP} and consequently from the output of the inverter, V_{oNLSV}, which therefore reaches a value below ground, thus generating the desired negative low-state voltage of the inverter. The expected low-state voltage value of V_{oNLSV} can be estimated by using charge conservation law for the two clock states ($\Phi_{shifted}$ low and high). The expression for the low-state output voltage (right after the falling edge of the output signal), V_{oNEG}, where a load capacitance C_{load} is assumed, can easily obtained as

$$V_{oNEG} \simeq -\frac{V_{in} - \frac{C_{load}}{C_{CP}} V_{bst}}{1 + \frac{C_{load}}{C_{CP}}} \tag{14}$$

Using the values in our implementation, where the load capacitance has been estimated as 30 fF and C_{CP} has been set equal to 4 pF, the expected low-state output value, for $V_{in} = 250$ mV and $V_{bst} = 1$ V, is -241 mV.

One thing to consider is that the proposed NLSV inverter does not maintain the low-state voltage permanently. This happens because, in the high state of the input clock signal, transistor M_{2CP} drives some current. Assuming subthreshold operation of this device and neglecting the effect of the bulk-to-drain forward biased PN junction in the low-state, the current flowing through M_{2CP} can be approximated as

$$I_H \simeq I_{sn} (W/L)_{M_{2CP}} (1 - e^{\frac{-V_{CPH}}{V_T}}) \cdot e^{\frac{V_{in} - V_{thH}}{n_n V_T}} \tag{15a}$$

$$I_L \simeq I_{sn} (W/L)_{M_{2CP}} (1 - e^{\frac{V_{CPL}}{V_T}}) \cdot e^{\frac{0 - V_{CPL} - V_{thL}}{n_n V_T}} \tag{15b}$$

where V_{thH} and V_{thL} represent the threshold voltage of the transistor in the high and the low output state, respectively, and V_{CPL} and V_{CPH} are the voltages at node V_{CP} in the two states. The threshold voltage of M_{2CP} in the low output state becomes lower than the threshold voltage in the high output state due to the body effect and, therefore, at the beginning of the low output state, M_{2CP} will drive more current than in the high output state. However, this drive capability in the low output state degrades rapidly because the gate-to-source voltage of M_{2CP} decreases over time (and, even though less importantly, the threshold voltage of device M_{2CP} also progressively increases) due to the source voltage increase. Note that in this state, because of the symmetry of the MOS transistor, the "drain" terminal of M_{2CP} (i.e., its upper terminal

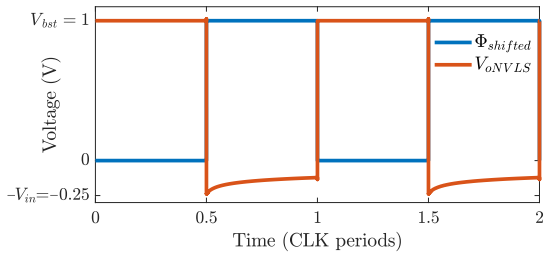


Fig. 7. Simulated waveforms of the NLSV inverter.

in Fig.6), works as a source and, vice versa, its "source" terminal works as a drain because V_{CP} is below ground. The ratio of the effective resistances of M_{2CP} in the low and the high output state can be written as

$$\frac{R_L}{R_H} = \frac{I_H}{I_L} \simeq \frac{e^{\frac{V_{in}-V_{thH}}{n_n V_T}}}{e^{\frac{|V_{CP}|-V_{thL}}{n_n V_T}}} = e^{\frac{V_{in}+\gamma(\sqrt{\Phi_0-|V_{CP}|}-\sqrt{\Phi_0})-|V_{CP}|}{n_n V_T}} \quad (16)$$

From this equation, the effective resistance of M_{2CP} becomes significantly larger in the low output state when the absolute value of V_{CP} is reduced and, hence, the time required to achieve a value close to zero in the low state would be several times larger than the time required for the same purpose in the high output state.

In conclusion, the NLSV inverter is able to provide a negative low-state voltage for a certain period of time with a negligible impact on the static power consumption and without requiring an additional dedicated voltage inverter.

The simulated response of the proposed NLSV inverter over time is shown in Fig. 7, when an input voltage $V_{in} = 250$ mV, a boosted voltage $V_{bst} = 1$ V, a load capacitor of 30 fF, and a frequency of operation equal to 100 kHz are used. As can be seen, the output voltage oscillates between 1 V and -238 mV. Even though the low level does not remain constant due to the fact that M_{2CP} is not fully turned off when its gate voltage is zero, the output of the NLSV inverter will remain sufficiently below ground time enough to adequately improve the drive capability of the PMOS switches in the first stage of the CP.

C. Power Efficiency

The power efficiency of a charge pump can be calculated with the general expression

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} = \frac{P_{out}}{P_{out} + P_{res} + P_{dyn} + P_{sta}} \quad (17)$$

where P_{out} is the power delivered to the output and P_{loss} represents the power losses, which have a resistive component, P_{res}, and a dynamic term, P_{dyn}, the latter contribution being associated to charging/discharging the intrinsic and parasitic capacitances of the system. Furthermore, as the CP is designed to work from ultra-low input power levels, a term for the static power dissipation, P_{sta}, is included, in order to allow a more accurate prediction at very low power levels.

As shown in Section II, the output resistance of a single voltage doubler can be calculated as the sum of two terms, namely R_{SC} and R_{SW}. The total output resistance of a charge pump with N stages can therefore be calculated as

$$R_{CP} = \sum_{i=1}^{N} \left(R_{SC_i} + R_{SW_i}\right) = N \cdot \left(\overline{R_{SC} + R_{SW}}\right) \quad (18)$$

where $\overline{R_{SC} + R_{SW}}$ is the average output resistance of each stage. From the above equation, resistive power losses are easily assessed as

$$P_{res} = N I_L^2 \left(\overline{R_{SC} + R_{SW}}\right) \quad (19)$$

Dynamic power losses can be estimated as:

$$P_{dyn} \simeq f \cdot C_{g0} \sum_j A_j \Delta V_j^2 \quad (20)$$

where A_j is the total gate area seen at each node j, C_{g0} is the gate capacitance per unit area (which also includes a rough estimation of the contribution of the parasitic capacitances associated to the node, so that $C_{g0} A_j$ is the total capacitance at the node), f is the frequency of operation, and ΔV_j is voltage swing at the node.

The estimation of the static power dissipation is performed by multiplying the leakage current, I_{lk_k}, of each branch, k, by its supply voltage, V_k. More in detail:

$$P_{sta} \approx \sum_k N_k I_{lk_k} V_k = N_{in} I_{lk_{in}} V_{in} + N_{bst} I_{lk_{bst}} V_{bst} \quad (21)$$

where $I_{lk_{in}}$ is the leakage current of the inverters supplied from V_{in}, $I_{lk_{bst}}$ is the leakage current of the inverters supplied from V_{bst}, and N_{in} and N_{bst} are the number of branches supplied from V_{in} and V_{bst}, respectively. By calculating the output voltage of the charge pump as

$$V_{out} = (N+1) \cdot V_{in} - N \cdot I_L \left(\overline{R_{SC} + R_{SW}}\right) \quad (22)$$

and replacing P_{out} with the product $V_{out} I_L$, the power efficiency of the charge pump can be rewritten as

$$\eta \simeq \frac{(N+1) V_{in} I_L - N \left(\overline{R_{SC} + R_{SW}}\right) I_L^2}{(N+1) V_{in} I_L + f C_{g0} \sum_j A_j \Delta V_j^2 + \sum_k N_k I_{lk_k} V_k} \quad (23)$$

where the resistive losses of the additional CP are neglected.

By inspecting equation (23), increasing f, dynamic losses increase and hence the power efficiency is degraded. If I_L is too small, dynamic and static losses are comparable to P_{out} and therefore the efficiency is reduced. On the other hand, if I_L is too large, V_{out} and, thus, P_{out} are reduced due to the output resistance of the CP, so the efficiency decreases and approaches zero. It should be noted that the above model assumes correct operation of the constituent blocks independently of V_{out} and f. In a real implementation, a minimum boosted voltage - maximum frequency pair of values ($V_{bst,min}$, f_{max}), is required for proper operation of the level shifter and the inverters. The condition ($V_{bst,min}$, f_{max}) is ascribed to the fact that the propagation delay of a CMOS digital inverter is inversely proportional to the supply voltage [44], so that the maximum allowed frequency of operation decreases as the supply voltage, V_{bst} for these blocks, decreases.

TABLE I

PARAMETER VALUES FOR POWER EFFICIENCY ESTIMATION

	tt	ss	ff
$\overline{R_n}$, $\overline{R_p}$	20 kΩ	30 kΩ	10 kΩ
$I_{lk_{in}}$	920 pA	185 pA	4 nA
$I_{lk_{bst}}$	8 pA	1 pA	50 pA
C_{g0}	10 fF/μm^2	10.4 fF/μm^2	9.4 fF/μm^2

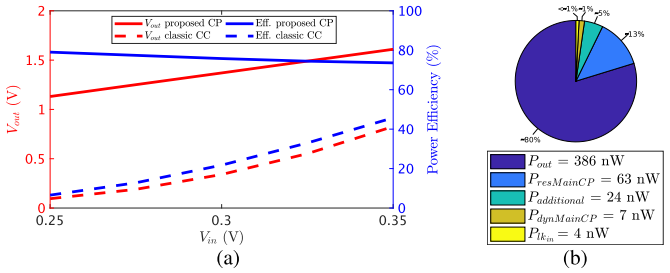


Fig. 8. Simulation results: (a) comparison between the proposed CP and an equivalent CP based on the conventional CC voltage doubler. (b) Power breakdown when $V_{in} = 250$ mV, $f = 50$ kHz and $R_L = 3.2$ MΩ.

Section IV will provide a comparison between experimental data and the developed simplified model for the typical-typical (tt), slow-slow (ss), and fast-fast (ff) corners, assuming $N = 4$, $N_{in} = 16$, $N_{bst} = 8$ and using the parameter values, estimated by simulation, shown in Table I.

D. Simulation Results

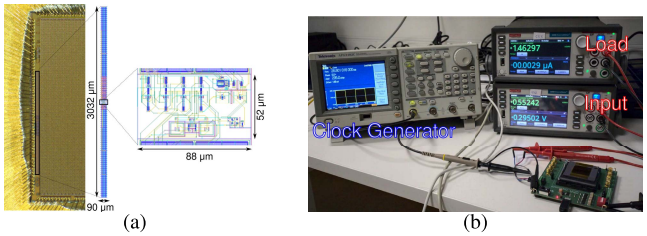
In order to illustrate the improvement provided by the proposed scheme, Fig. 8a shows a comparison obtained by computer simulation between the circuit in Fig. 5 and a CP consisting of four conventional cascaded CC voltage doublers. The same C_{fly} and the same sizes of switching transistors are assumed in the two cases. The comparison was performed by using a load resistance of 5 MΩ and a clock frequency of 35 kHz, and varying V_{in} between 250 mV and 350 mV. As can be seen, the proposed CP offers a significantly higher V_{out}, specifically for lower input voltages, which highlights the lower equivalent output resistance of the circuit and, therefore, also its better power efficiency. This improvement is much more significant for lower V_{in} because the gate boosting maintain the switches in the strong inversion region meanwhile in the classical structure the switches are in weak inversion. When V_{in} approaches the threshold voltage, the on-resistance of the switches of the conventional CC voltage doubler diminishes, making charge transfer more effective and therefore showing an output voltage and a power efficiency closer to (although still much lower than) the values of the proposed circuit. The power efficiency decrease for increasing values of V_{in} in the proposed structure is ascribed to the higher dynamic and static losses, as expected by equations (20) and (21), while the load resistance is maintained constant. If the load current is increased for higher input voltages, the power efficiency would achieve a higher value than the one shown in this simulation.

The simulated power consumption breakdown of the proposed CP is shown in Fig. 8. The estimation of the power values was done as follows. First, the dynamic power consumption at a gate node (specifically, V_{gup1}) was evaluated and averaged over time, and the obtained value was multiplied by 8 to achieve the dynamic losses of the main charge pump, $P_{dynMainCP}$. Then, the power consumption of the additional circuitry, $P_{additional}$, was estimated as the input power to the additional charge pump minus the dynamic power of the main charge pump. To continue, the leakage power, $P_{lk_{in}}$, was approximated as 16 times the static power loss in an inverter supplied by V_{in}. Finally, the remaining power losses are attributed to the resistive loss in the main charge pump, $P_{resMainCP}$. As an example, for $V_{in} = 250$ mV, a load resistance of 3.2 MΩ, and $f = 50$ kHz, a power efficiency of 80% was obtained. The simulation showed that 13% of the input power is lost due to the output resistance of the main CP, 5% is consumed by the additional CP feeding the level shifter and the main CP gate voltage drivers (this contribution substantially corresponds to the power loss for switching clock signal generation for the main charge pump), 1.4% is attributed to the dynamic losses of the main CP, while about of 0.8% is ascribed to the leakage current of the low threshold voltage inverters supplied at V_{in}.

IV. EXPERIMENTAL RESULTS

A prototype of the proposed architecture was fabricated in CMOS 180 nm technology using 1.8 V devices. Fig. 9a shows a photograph of a silicon die highlighting the area occupied by the circuit (3032 × 90 μm^2) together with the layout of both the entire CP and the control section (namely, the clock driving inverters, the level shifter, the gate voltages generator and all switching transistors) without capacitors. The elongated shape of the circuit layout is due to the fact that the die area is shared among several projects. Each fly capacitor in the charge pump was set to $\simeq$ 140 pF, which makes the total CP boosting capacitance equal to approximately 1.12 nF. These capacitors were implemented using PCAP devices, i.e., PMOS transistors with drain, source, and bulk terminals short-circuited to form one electrode, the counterelectrode being formed by the gate terminal. PCAP capacitors offer high capacitance density but are not rated for high gate-to-drain/source voltage operation. The capacitors in the NLSV inverters and in the additional CP were therefore implemented using metal-insulator-metal (MiM) devices, with a value of 4 pF in each NLVS inverter and 8 pF for each fly capacitor in the additional CP. Also, a storage MiM capacitor of 8 pF was internally connected to the output node of the main charge pump, thus making the total non-boosting capacitance equal to 48 pF. The total silicon area occupied by the circuit is 272880 μm^2, with 4575 μm^2 occupied by the active devices.

The experimental characterization was performed using a Tektronik AFG3102C function generator to provide the clock signal, which was always set to an amplitude equal to V_{in}, and two source meter units (SMU) Keithley 2450 to provide V_{in} and draw the load current, respectively, as can be seen in Fig. 9b. V_{out} was limited to 1.6 V by the SMU used as the load in order to avoid possible transistor damages because the internal voltage V_{bst} will be higher than V_{out} and could overcome the rated voltage of the transistors. In more detail,



(a) (b)

Fig. 9. (a) Chip microphotograph highlighting the implementation area (left) and layout captures of the whole CP (middle) and active devices only (right). (b) Measurement setup.

V_{bst} can be expressed as $V_{bst} = V_{out} + 2 \cdot V_{in} - I_{Lbst} R_{bstCP}$, I_{Lbst} and R_{bstCP} being the load current and the output resistance of the additional charge pump, respectively, and its value, obtained by simulation, is around $V_{out} + V_{in}$ in most of the observed cases. The measurement procedure is described next. First, the input voltage, V_{in}, is set. Then, the frequency of operation, f, is set too, starting from the lowest considered value (1 kHz). Once V_{in} and f are set, the load current is swept from low to high values, and this sweep is stopped when the output voltage drops below the input voltage. To continue, the frequency of operation is increased and a new I_L sweep is made. When f is too high and the charge pump is not able to operate, V_{in} is increased and the whole process is repeated. The experimental results showed that the proposed CP is able to work with V_{in} as low as 110 mV and an input power of 3.6 nW, delivering in this case an output power of 244 pW with an efficiency of 6% when $f = 2.24$ kHz is used. The peak power efficiency and the maximum output power of the CP varying both V_{in} and f are shown in Fig. 10a and Fig. 10b, respectively. From Fig. 10a, the highest measured peak efficiency was 83% with $V_{in} = 395$ mV and $f = 139$ kHz. Under these conditions, the circuit delivers an output power of 5.73 μW. From Fig. 10b, the maximum P_{out} that can be delivered by the circuit (limiting V_{out} to 1.6 V) is 16.8 μW when V_{in} is 400 mV and f is 518 kHz. At the highest value of the output power, the measured efficiency was 78%. As can be seen in Fig. 10c, the peak power efficiency remains above 70% for V_{in} between 180 mV and 400 mV.

The output voltage dependence on I_L for 4 cases of operating conditions (V_{in}, f) is shown in Fig. 11a. From this figure, an output impedance of 988 kΩ, 298 kΩ, 308 kΩ, and 157 kΩ was obtained for case 1, 2, 3, and 4, respectively. Subtracting the contribution of the equivalent resistance of the switching capacitors, calculated as $4 \times 1/2 f C_{fly}$, the effect of the switch resistance on the output impedance of the CP can be estimated. By following this approach, the impact of the switches resistance has been determined as 248 kΩ, 99 kΩ, 110 kΩ, and 54 kΩ, respectively. The dependence of the estimated switch resistance on the operating frequency can be easily explained because higher f means higher V_{out} for a given I_L (indeed, R_{SC} is reduced) and, thus, a higher high voltage level of the gate signals, V_{bst}, so the on-conductance of the transistors is greater, as expected from equation (12). The circuit behaviour when varying the clock frequency can be seen in Fig. 11b for 4 different operating conditions (V_{in}, I_L).

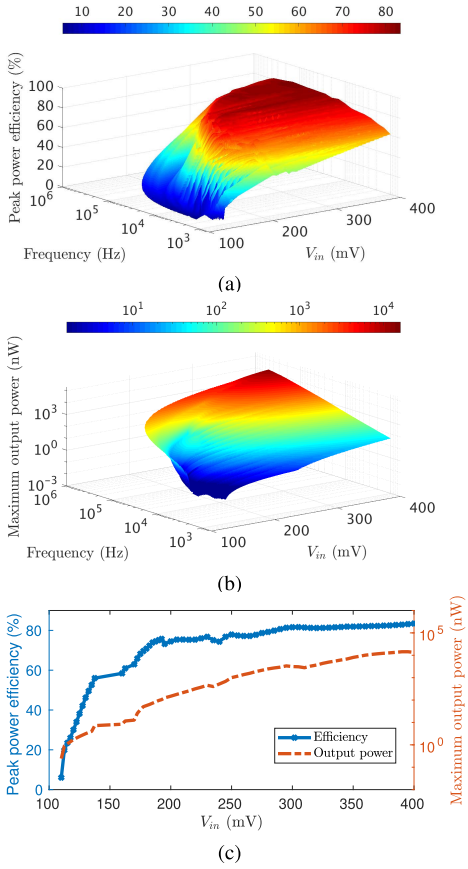


Fig. 10. Experimental characterization of the CP: (a) peak power efficiency and (b) maximum P_{out} varying V_{in} and f; (c) peak power efficiency and maximum output power vs. V_{in}.

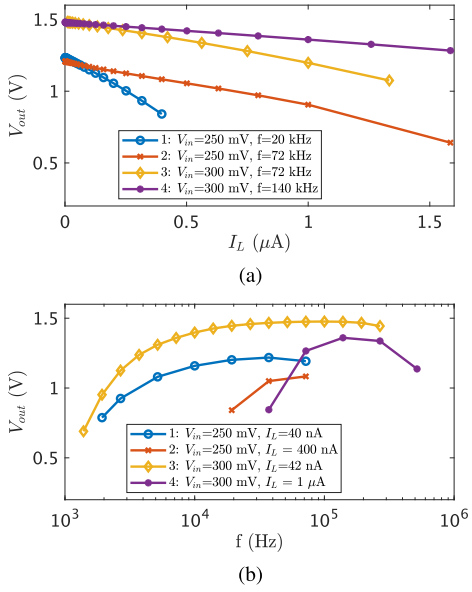


Fig. 11. Measured output voltage as a function of: (a) the load current and (b) the frequency of operation.

The observed response is in agreement with expression (6) from which a decreasing output impedance with increasing f is expected until the fast switching limit (FSL) is reached. Above this limit, the output resistance increases significantly.

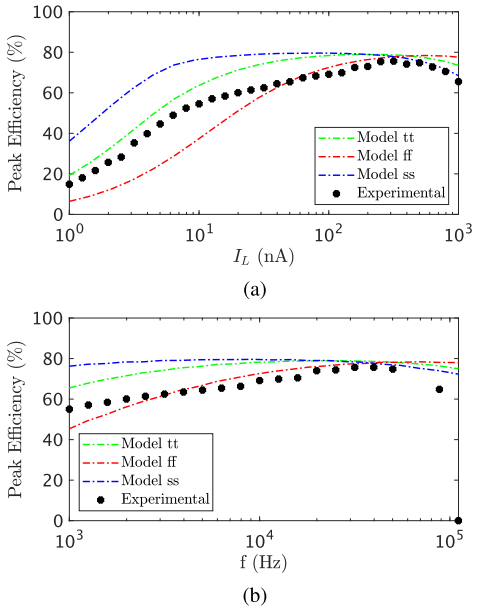


Fig. 12. Peak power efficiency of the proposed CP (V_{in} = 250 mV): experimental data (black circles) and results from the model in Section III-C using parameter values from Table I; (a) vs. load current and (b) vs. frequency of operation.

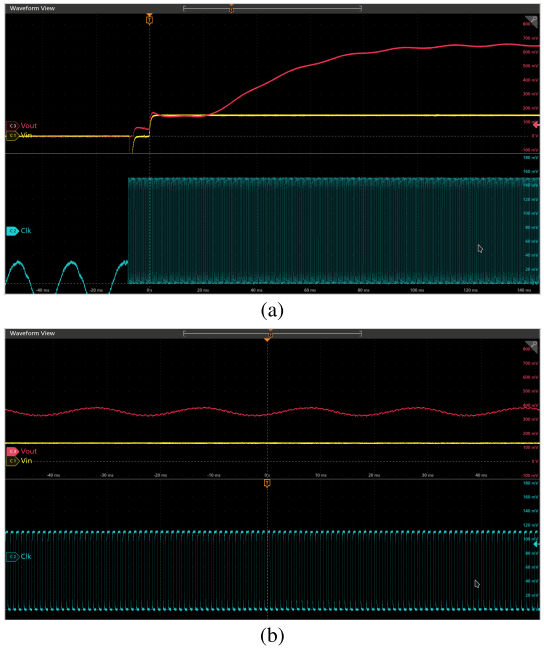


Fig. 13. (a) Startup of the proposed charge pump with V_{in} = 150 mV. (b) Charge pump operating at the lowest input voltage of 110 mV.

The circuits that generate the boosted clock signals of the CP stages as well as the clock inverters stop working correctly at a certain operating frequency, as expected for a CMOS digital circuit, and as a consequence, the CP stops working.

The power efficiency of the proposed CP was then evaluated varying both I_L and f for $V_{in} = 250$ mV. The obtained peak power efficiency for each I_L and for each f is shown in Fig. 12, where the experimental data (black circles) are plotted together with the curves obtained by the simplified model in equation (23). As can be seen, the experimental results show a behaviour in agreement with the prediction of the model: the proposed circuit features a power efficiency higher than 60% for I_L above 25 nA, with a maximum of 77%, and delivers a maximum I_L of 1.26 μA (P_{out} = 1.02 μW). These values meet the design specifications pointed out in Section I.

With respect to the circuit startup, Fig. 13a shows the transient response when the input voltage, with a value of 150 mV, and the clock signal are connected to the circuit. For input voltages below 150 mV, the circuit cannot start pumping if V_{out} is too low, because V_{bst} is not high enough to power on the level shifter and the gate voltages generator. When the circuit works, i.e., when the output voltage is around 500 mV, the input voltage can be decreased down to 110 mV and the charge pump still operates. Fig. 13b shows the CP still working with V_{in} = 110 mV after decreasing the input voltage from higher values. Note that the proposed charge pump requires a high load resistance when V_{in} is low to start working (letting V_{out} and V_{bst} raise to improve the drive capability of the switching transistors). This goal could be achieved by adding, between the output of the CP and the load, a switch driven by a control unit, if the load current is expected to be too high at the startup process. A possible simple control of the startup can be implemented by using a subthreshold level detector like the one proposed by Chen et al. [45], which can be designed to consume a power level in the order of pW [27].

Table II shows a comparison of the proposed architecture with state-of-the-art CPs with low V_{in}. Two implementations [24], [48] offer the highest output power among the compared solutions, which is mainly achieved thanks to the use of large off-chip capacitors. On the other hand, two approaches [49], [51] show a good P_{out} in relation with their on-chip pumping capacitance thanks to the use of a relatively high clock frequency (several MHz). This high clock frequency has the associated drawback of a relative large power consumption, thus reducing power efficiency and making the circuits not suitable for ultra-low power environments. Another proposal [46] makes use of the dynamic gate-boosting, achieving a power efficiency, not including the clock generator, equal to 43.5% when the input voltage is only 100 mV and using a switching capacitance as low as 82 pF. The main drawback of the implementation is the use of a more advanced technology node, which means a significantly higher fabrication cost. A different solution [47] uses a dynamic voltage frequency frequency scaling to adequate the clock frequency and oscillation amplitude to the load thus reducing the dynamic losses of the clock. It offers a relatively good performance and very reduced silicon area, but it is not suitable for ultra-low power environments because the design operates with frequencies of megahertzs. Another implementation [30] uses a dedicated circuit structure to select the gate voltage for the CP switches and offers a good behaviour in terms of efficiency at low output power, but requires a reference voltage and makes use of a low threshold voltage transistor in switches, thus reducing its applicability in ultra-low power applications. In the last solution considered in this comparison [50], boosted-voltage clock signals are provided

TABLE II

PERFORMANCE COMPARISON WITH STATE-OF-THE-ART LOW INPUT VOLTAGE CHARGE PUMPS

Parameters	This work	TCASII'22 [46]	AICSP'22 [47]	IJCTA'21 [48]	ISCAS'20 [30]	TCASII'18 [49]	CICC'17 [50]	JSSC'15 [24]	ASPDAC'12 [51]
CMOS Process (nm)	180	65	130	180	180	65	55	130	65
Minimum V_{in} (mV)	110	40	150	132.5	120	80	200	150	120
Integrated oscillator	no	no	yes	no	yes	yes	yes	no	yes
Peak efficiency@V_{in} (%@mV)	6@110 57@150 78@250 83@395	10.5@40 43.4@100	44.76@150 46.6@170 58@300	85@300	42.6@120	45@200	37.4@220	72.5@0.45	38.8@120
Max. P_{out}@V_{in} (μW@mV)	0.00024@110 0.158@200 1.005@250 3.97 @ 300 16.8 @ 400	0.48@100	-	11000@300	1@120 16.9@180	4.38@200	10.45@220	10.5@180 >608@500	2.5@120 10@160
Fly capacitance (pF)	1120 on-chip	82 on-chip	- on-chip	5000000 off-chip	1512 on-chip	∼tens of pF on-chip	720 on-chip	60000 off-chip	286 on-chip
Area (mm^2)	0.27	0.2278	0.093	0.395	1.84	0.032	0.74	0.066	0.78

as in our approach: more in detail, the voltage of preceding stages are used to supply the inverters that generate the clock signals for each stage of the CP. Besides, this solution uses forward body biasing to reduce the effective threshold voltage of the switches and a clock frequency of 2.15 MHz, showing relatively good values of peak efficiency and output power with an input voltage of 220 mV. Nevertheless, the circuit was designed for a microwatt application and is not appropriate for the ultra-low-power target of our design. Other approaches, such as [35] concern the design of a complete harvester and are therefore not listed in Table II. In [35] an auxiliary CP is used to generate boosted clock signals to be used by the main Dickson-type charge pump. The harvester shows a power efficiency of 67% when the input voltage is 0.31 V and when the input power is in the microwatt range, efficiency and output power values slightly below our proposal under the same conditions, while the circuit occupies a similar silicon area. On the other hand, our proposed charge pump offers a high degree of flexibility, able to operate with a wide range of V_{in} and P_{in}, allowing the operation with power sources from few nW when the input voltage is less than 250 mV to several μW when the input voltage exceeds 250 mV. It should be noted that the clock signal in our case is external since the circuit is intended to be part of a harvester system which will determine the appropriate operating frequency of the CP and, therefore, the impact of the clock generator on efficiency is not considered in Table II. Proposals for an oscillator with a power consumption as low as 120 pW/kHz can be found in the literature [52], so that the efficiency drop due to a specifically designed oscillator would be significant only for very low output powers, i.e., for V_{in} well below 200 mV. The preliminary design of a clock generator based on the above mentioned solution [52] has been simulated. The power consumption obtained for the oscillator leads to a peak power efficiency loss in the charge pump below 1% for input voltages above 200 mV when the oscillator is supplied with V_{in}.

V. CONCLUSION

In this paper, a charge pump circuit based on the CC voltage doubler that also includes boosted gate voltages for the switches, is proposed and experimentally characterized. The boosting is performed by using a level shifter and some inverters properly connected to the main charge pump stages, all supplied by an additional charge pump connected at the output of the circuit. Special inverters able to provide a negative low state voltage are proposed in this work to improve the behaviour of the first stage of the main CP. The prototype is suitable for use in ultra-low power energy harvesting applications, needing only a square clock signal, apart from the input voltage, to operate. The silicon prototype is able to pump charge even from an input voltage of only 110 mV and an input power of 3.6 nW. The experimental peak power efficiency remains above 70% when the input voltage is higher than 200 mV, achieving a maximum output power of 16.8 μW and offering an efficiency of 78% at an input voltage of 400 mV and a frequency of 518 kHz.

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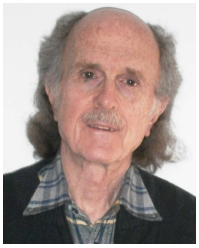

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