Analysis and Design of a 195.6dBc/Hz Peak FoM P-N Class-B Oscillator with Transformer-Based Tail Filtering

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***Abstract*—A complementary p-n class-B oscillator with two magnetically coupled second harmonic tail resonators is presented and compared to an N-only reference one. An in depth analysis of phase noise, based on direct derivation of the Impulse Sensitivity Function (ISF), provides design insights on the optimization of the tail resonators. In principle the complementary p-n oscillator has the same optimum Figure of Merit (FoM) of the N-only at half the voltage swing. At a supply voltage of 1.5V, the maximum allowed oscillation amplitude of the N-only is constrained, by reliability considerations, to be smaller than the value that corresponds to the optimum FoM even when 1.8V thick oxide transistors are used. For an oscillation amplitude that ensures reliable operation and the same tank, the p-n oscillator achieves a FoM 2 to 3dB better than the N-only depending on the safety margin taken in the design. After frequency division by 2, the p-n oscillator has a measured phase noise that ranges from -150.8 to -151.5dBc/Hz at 10MHz offset from the carrier when the frequency of oscillation is varied from 7.35 to 8.4GHz. With a power consumption of 6.3mW, a peak FoM of 195.6dBc/Hz is achieved.**

***Index Terms*—Oscillator, voltage-controlled oscillator (VCO), distributed oscillator, class-B, class-C, class-F, phase noise, Figure of Merit (FoM).**

I. Introduction

In LC oscillators reducing the power consumption while preserving low phase noise is a key goal especially for mobile applications. This can be achieved acting on the oscillator topology and/or on the tank quality factor (Q). Oscillator topology affects the power vs phase noise trade-off in two equally important ways. First, acting on the conversion of circuit noise into phase noise through the impulse sensitivity function (ISF) [1]; second, changing the maximum achievable power conversion efficiency (η_P), i.e. the conversion of DC power (P_{DC}) into resonator RF power (P_{RF}), which directly affects phase noise [2]. The use of voltage-biased topologies [3]–[5] eliminates a source of phase noise (i.e. the current generator) and improves power efficiency, but increases the sensitivity to supply voltage variations. Large voltage swings (relative to the supply voltage) are desirable to achieve high voltage efficiency, thus high power efficiency, and to reduce phase sensitivity to device noise, but they can drive the active devices into the triode region, thereby loading the tank, potentially degrading phase noise. Class-C oscillators [6], [7] use sharp current pulses to improve current efficiency, but voltage efficiency is limited to avoid loading the tank. Adopting a low supply voltage (e.g. 0.475V in [3]), the active devices do not enter into triode even as the signal swing approaches (or exceeds) the supply rails, but performances become very sensitive to supply voltage variations [8] and, to preserve power efficiency, a dedicated switch-mode voltage regulator may be needed, thus increasing cost. In class-F oscillators [9] a non-sinusoidal waveform is created using higher order resonators, increasing the signal slope and reducing the ISF. However, as shown in [2] this requires multiple high-Q inductors. Alternatively, the multiple resonances of a transformer can be exploited, reducing area occupation. If a step-up transformer is used to magnetically couple gate and drain, the gate voltage swing can be enhanced [9], further reducing the ISF. The clip-and-restore [5] oscillator deliberately pushes the active devices into deep triode in order to create a non-sinusoidal waveform at the drain that alters the ISF. When the active devices are ON their drain voltage is nearly flat, desensitizing the oscillation phase to circuit noise. Tank loading is countered using two step-up transformers in series to boost the gate voltage swing and reduce the ISF. Class-D oscillators operate the LC tank in a peculiar time-variant regime, resulting in high η_P and low phase noise. However, the peak voltage swings of about three times the supply voltage forces the choice of a low supply voltage (0.4V in [4], [10]) and results in frequency pushing. Among the proposed solutions [3], [4], [7], [9]–[27], the one that has achieved the best efficiency, as measured by the Excess Noise Factor (ENF) [2], is the Class-B oscillator with an additional LC tank (resonating at $2\omega_0$) inserted at the source of the active devices [26]. The switching transistors can enter the triode region without loading the tank since, intuitively they see a high impedance in series with them, effectively altering the active devices ISF in a way similar to the class-F_2 oscillator in [28], achieving high η_P and low phase noise. Ideally 100% η_P can be achieved, but with voltage swings approaching π times the supply voltage. Adopting a complementary (push-pull) topology, the peak efficiency is reached at lower (theoretically half) voltage swing compared with an N-type-only one, avoiding reliability concerns. For this reason we present a high efficiency complementary Class-B oscillator with dual LC tail filter, which can use efficiently the supply current and achieve a low phase noise. In Section II we briefly recall the definition of ENF and its expression for an important class of LC-oscillators. Section III analyzes the phase noise in class-B oscillators (both N-only and p-n) with tail filter and derives an accurate closed-form expression for phase noise and ENF, providing useful design insights. Section

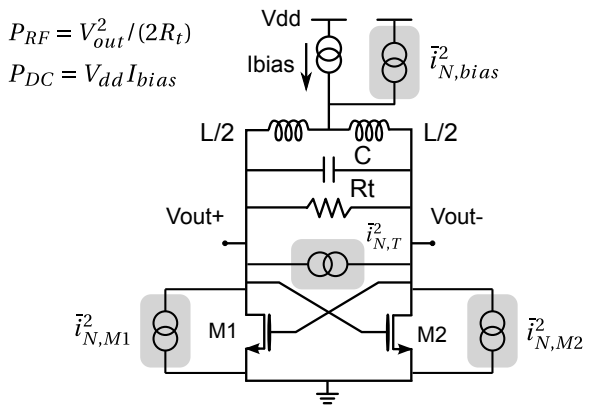

Fig. 1: Class-B oscillators with main noise sources: LC-tank losses, switching transistors and bias circuitry

IV gives more details on the practical design aspects of the proposed p-n oscillator with transformer-based tail filtering and reports on the experimental results. Section V draws the conclusions.

II. Excess Noise Factor in LC-Tank Oscillators

To benchmark the performance of an oscillator we rely on the widely used Figure of Merit [29] (FoM) that normalizes phase noise to frequency of oscillation (ω_0), offset frequency from the carrier ($\Delta\omega$) and power consumption (P_{DC}). The phase noise of a classic LC-tank oscillator (Fig. 1) can be estimated, using the theory of Hajimiri and Lee [1], computing the ISF for the main noise sources. Considering only the noise coming from the tank losses, assuming a sinusoidal waveform and that the energy restoring element does not load the tank (such that the ISF of the tank has a mean square value of $1/2$), when the power conversion efficiency η_P ($= P_{RF}/P_{DC}$) is 100% the oscillator FoM reaches a thermodynamic limit (FoM_{max}) that depends only on the Q of the tank:

$$FoM_{MAX} = -10\log\left(\frac{k_B T}{2\cdot 10^{-3} Q^2}\right) = 173.8 dBc/Hz + 10\log(2Q^2) \quad (1)$$

The ENF, defined [2] as the difference between FoM_{MAX} and the actual FoM, provides a figure of merit of the topology, independent from the tank Q. For a VCO where the negative resistance transistors have a gate-to-source voltage equal to the tank single-ended voltage, Mazzanti and Andreani [6], [30], [31] have shown that, if the active devices do not load the tank, the transistors contribution to phase noise is γ_{MOS} times the tank noise. Using this result ENF is given by:

$$ENF = 10\log\left(\frac{1+\gamma_{MOS}}{\eta_P}\right) \quad (2)$$

This shows that in a classic LC-tank oscillator which drives the tank with high impedance phase noise is minimized by maximizing power efficiency. The use of an additional LC tank at the source of the active devices of a class-B oscillator (Fig. 3a) was originally proposed to reduce the current source noise [26] thanks to the filtering action of the large capacitance (C_{top}) in parallel with it. This topology has, however, two other important advantages. First, the common source node can swing below ground, increasing the maximum achievable voltage swing. Since current efficiency remains nearly constant, η_P is also increased, ultimately reaching a value close to 90%. Second, the switching transistors can enter the triode region without loading the tank since they see a high impedance in series with them. Hence, as suggested by (2) the peak efficiency corresponds also to the peak FoM because, thanks to the tail resonator, noise remains constant even when the switching transistors are pushed deeply into linear region. Table I compares the measured performance of various VCOs with different topologies, including their ENF[1] (computed using the data available in the referenced papers). The comparison shows that the class-B oscillator with tail filter in [26] is superior by more than 1dB compared to any reported VCO (assuming accurate Q estimation). The main problem of this topology is the fact that for the optimum FoM the peak voltage across the transistors is more than twice the supply voltage. For the oscillator in [26], implemented in a $0.35\mu m$ CMOS technology and biased from 2.5V, the peak FoM of 195.4dBc/Hz is reached with a η_P of 81% for a peak swing of 6.4V (computed from the values of tank Q, inductor and current provided in the paper). Large voltages can seriously damage the transistors and reduce significantly their lifetime [32], [33]. This issue can be solved if a low supply voltage is chosen (e.g. 0.4V in [4]). However, when the oscillator is embedded in a complex system its supply voltage must be derived from an available switched-mode power supply (SMPS), possibly shared by other analog rather than digital blocks to avoid unacceptable spur levels and keep costs low. The difference between the SMPS level and the oscillator supply voltage will be absorbed by a low-voltage drop supply (LVDS) regulator. For a fixed SMPS voltage level, a low oscillator supply voltage leads inevitably to a low LVDS efficiency and therefore to a degradation of the overall power efficiency. In today's platforms these voltages are often larger than 1.2V, with typical values in the range of 1.5V to 1.8V (Fig. 2) [34]–[42]. This makes attractive the use of a complementary p-n topology, shown in Fig. 3b, which has twice the current efficiency of the N-only one and achieves the same peak power efficiency (or equivalently reaches the same peak FoM), but with half the voltage swing. In [17] a p-n version of the oscillator of reference [26] was presented which achieved a FoM of 183.8dBc/Hz and a ENF of 11dB. However, the focus of that work was to reduce the tail current $1/f$ noise, not to reduce ENF. This solution will be studied in depth and compared with the N-only topology in the next section.

III. Analysis of Class-B Oscillators with Tail Filter

The Class-B oscillator with tail filter can achieve low ENF thanks to the possibility to obtain very good efficiency without increasing the noise. In fact a big capacitor filters out the noise

[1]Even though for class-D and class-F the hypotheses used to derive (2) are often violated, (1) still provides a useful practical reference to compare different topologies.

TABLE I: Comparison table

Ref	Topology	Tech	Area $[mm^2]$	V_{dd} [V]	V_{out} [V]	f_{osc} [GHz]	Tuning Range %	Phase Noise [dBc/Hz]	FoM [dB]	FoM_T [dB]	Q	ENF [dB]
[7]	Class-C p-n	0.18um CMOS	0.075	1.8	0.9	6.1/7.5	18%	-120/-123 @$2MHz$	189-191	196	10	5.8
[6]	Class-C N-only	0.13um CMOS	-	1	1.24	4.5/5	10.5%	-132.8 @$3MHz$	193.5-196	196.4	17	5.4
[26]	Class-B N-only	0.35um CMOS	-	2.5	6.4 [1]	1.2	-	-153 @$3MHz$	195.4	-	14	4.3
[4]	Class-D	65nm CMOS	0.12	0.4	1.28	2.5/3.3	46%	-144 @$5MHz$	189-190	199	10	6.8
[3]	Colpitts	0.13um CMOS	0.28	0.48	1.5	4.9	2.4%	-136.3 @$3MHz$	196.2	184.2	18	5.8
[43]	Clip and restore	65nm CMOS	0.19	1.5	3.5	3.64/4	10.2%	-135 @$1MHz$	190.1	190.3	11	7.6
[9]	Class-F	65nm CMOS	0.12	1.2	2	5.9/7.6	25%	-142.2 @$3MHz$	192.2	200.2	16	8.7
[28]	Class-F_2	65nm CMOS	0.2	1.3	4.5	7.2/8.8	19%	-144.8[2] @$3MHz$	191.8	197.4	14	7.92
This Work	Class-B N-only	55nm CMOS	0.17	1.5	2.1 [1]	7.4/8.4	13%	-152.8[2] @$10MHz$	190.5-192.3	194.5	15	8
This Work	Class-B p-n	55nm CMOS	0.19	1.5	1.6 [1]	7.4/8.4	13%	-151.5[2] @$10MHz$	194.3-195.6	197.8	15	4.7

[1] Estimated from calculations
[2] After division by 2

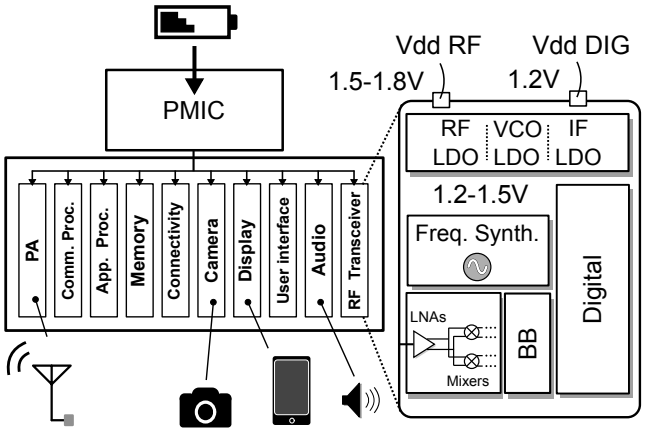

Fig. 2: Conceptual block diagram of a complete mobile system

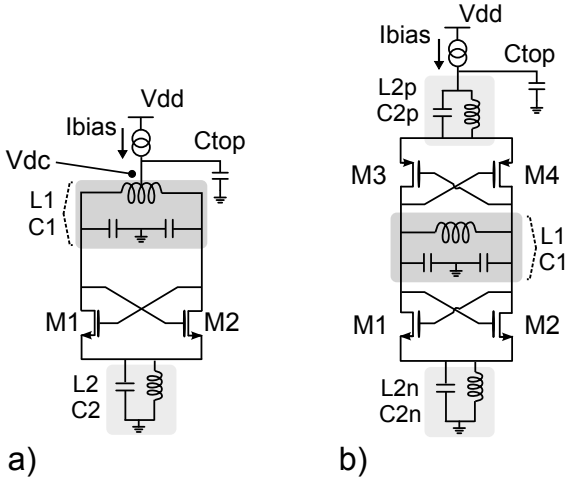

Fig. 3: Class B with tail filter: a) N-only b) p-n. Numerical examples assume $L_1 = 600pH$, $Q_1 = 20$ and $L_2 = 400pH$, $Q_2 = 20$ at 2GHz.

of the current generator (that allows to minimize the voltage headroom dedicated to it), while the tail LC filter provides a high source impedance, allowing to push the oscillator towards a high power efficiency without incurring into phase noise degradation. In the following analysis the goal is to demonstrate this intuitive argument and, obtaining a closed form expression for the phase noise, to give some insights on the design of this type of oscillators. The details of the derivation will be reported in Appendix A. At first the N-only topology will be studied and then the analysis will be extended to the p-n topology.

A. N-only class-B Oscillator with Tail Filter

The analysis will refer to the top-biased oscillator in Fig. 3a, but the same considerations can be done for a bottom biased oscillator. The main LC tank resonates at the fundamental

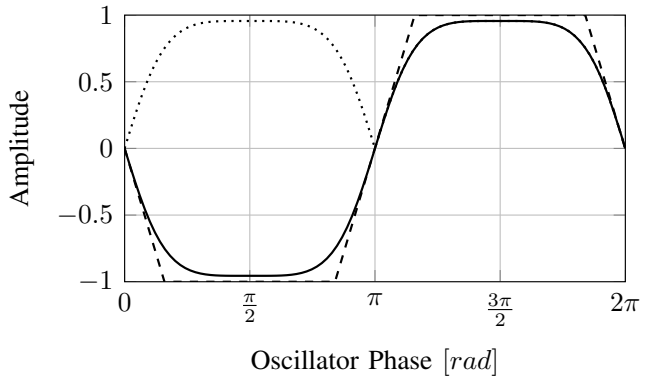

Fig. 4: Soft switching behavior (oscillator of Fig. 3a): idealized (dashed), smoothing function $f(\varphi)$ (continuous), and its modulus $g(\varphi)$ (dotted)

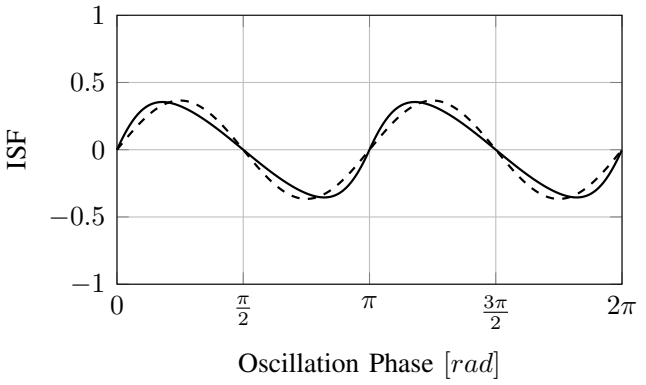

Fig. 5: Impulse Sensitivity Function of the second harmonic tank (oscillator of Fig. 3a): considering the more complete analysis (continuous) and approximated with just second harmonic (dashed)

frequency (f_0) and the tail tank resonates at $2f_0$. The ISFs are calculated starting from the state vector $\vec{X}$ [1], [44], [45]:

$$\vec{X} = [V_{C_1} \quad \sqrt{\frac{L_1}{C_1}} I_{L_1} \quad \sqrt{\frac{C_2}{C_1}} V_{C_2} \quad \sqrt{\frac{L_2}{C_1}} I_{L_2}] \tag{3}$$

where the four state variables correspond to voltages on the capacitors and the currents flowing through the inductors, scaled in such a way that the squared sum of the state variables is proportional to the stored energy, as done in [2], [46], where this approach was found to be accurate. In steady state $V_{C1} = A_1 \sin(\omega_0 t)$ and $V_{C2} = A_2 \cos(2\omega_0 t)$, where C_1 and C_2 are the total capacitance at the main LC tank and tail tank respectively.

1) Main Tank losses: If a noise charge is injected across the main tank it will appear across capacitor C_1, creating a perturbation in the first state variable $\Delta X_1 = \Delta q / C_1$. As a result the ISF associated with the main tank losses can be directly calculated as shown in Appendix A as:

$$\Gamma_1 = \frac{\cos(\omega_0 t)}{\left(1 + 4\frac{C_2}{C_1}\frac{A_2^2}{A_1^2}\right)} \tag{4}$$

where the constant q_{max} is set equal to $A_1 C_1$.

2) Tail Tank losses: If a noise charge Δq is injected across the tail tank, it will affect the oscillator nodes in a time-dependent manner, due to the transistors switching action. During the oscillation period it is possible to distinguish two cases: first, the plateau, when one transistor is ON and the other one is OFF; second, during transitions, when both transistors are ON. When one transistor is ON the charge injected at the source will be instantaneously divided between capacitors $2C_1$ and C_2[2], affecting both tank voltages ($\Delta V_1 = \pm \Delta V_2$, where V_1 and V_2 are the voltages across the main tank and tail tank respectively, depending on whether M_1 or M_2 is ON). During transitions instead the capacitance sees only C_2 and there is no effect on V_1. To account for this soft switching behavior, idealized by the dashed line in Fig. 4, a smoothing function $f(\omega_0 t)$ (thick line in Fig. 4) and its modulus $g(\omega_0 t) = |f(\omega_0 t)|$ (dotted line in Fig. 4) are introduced. $f(\varphi)$ is defined as the difference between the active devices V_{ds} normalized to their sum and it can be expressed as a function of the steady-state oscillation state as:

$$f(\varphi) = \frac{A_1 \sin(\varphi)}{2(A_2 \cos(2\varphi) - V_{dc})} \tag{5}$$

where V_{dc} is the effective supply voltage, as shown in Fig. 3a. Using the above definition, the effect of Δq on the tank voltages V_1 and V_2 can be approximated as follows:

$$\Delta V_1 = -\frac{f(\varphi)\Delta q}{2C_1 + C_2} \quad \Delta V_2 = -\frac{g(\varphi)\Delta q}{2C_1 + C_2} - \frac{\Delta q}{C_2}(1 - g(\varphi)) \tag{6}$$

Following the same steps as for the ISF of the main tank, reported in Appendix A, the ISF of the tail tank (Γ_2) can be calculated. The plot of the corresponding waveform is reported in Fig. 5 (thick line). Approximating Γ_2 with its dominant harmonic component at $2f_0$, a sufficiently accurate closed form expression is found ($\Gamma_{2,2f_0}$), shown as dashed line in Fig. 5.

$$\Gamma_{2,2f_0} \cong \frac{1}{\left(1 + 4\frac{C_2}{C_1}\frac{A_2^2}{A_1^2}\right)} \left(2\sqrt{2}\frac{A_2}{A_1}\sin(2\varphi)\right) \tag{7}$$

3) Active Devices: To derive the ISF of the active devices we study the effect of a noise charge Δq injected between the tail node and one output node. A charge injected at one output node is equivalent to the superposition of one differential plus one common mode charge injection both of $\Delta q/2$. Differential and tail charge injection have already been discussed. A common mode charge injected at the main tank, through the switching action of the transistors, appears periodically also across the tail capacitor and its effect can be approximated as:

$$\begin{aligned} \Delta V_1 &= -\frac{\Delta q}{2C_1} + f(\varphi)\left(\frac{\Delta q}{2(2C_1 + C_2)} + \frac{\Delta q}{4C_1}\right) \\ \Delta V_2 &= \frac{\Delta q \cdot g(\varphi)}{2(2C_1 + C_2)} + (1 - g(\varphi))\frac{\Delta q}{C_2} \end{aligned} \tag{8}$$

[2]Here we assume that during the plateau the ON transistor operates close to an ideal switch. This assumption proves more accurate at higher amplitudes of operation, which is the optimum operation region of the oscillator.

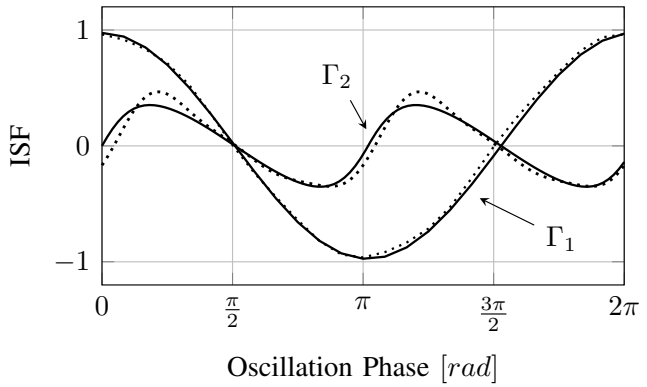

Fig. 6: Main tank and tail tank ISFs simulated (dotted) and evaluated (continuous) of Fig. 3a

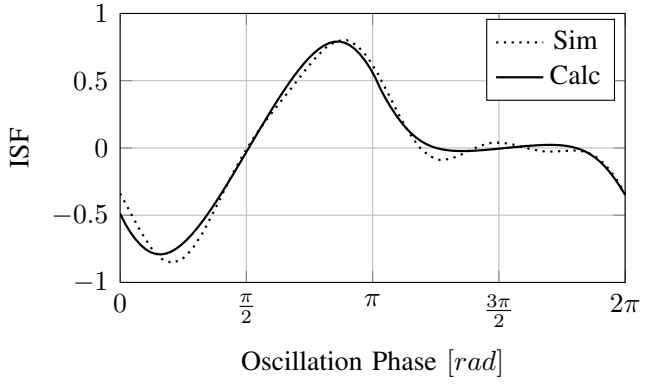

Fig. 7: Active devices ISF simulated (dotted) and evaluated (continuous) of Fig. 3a

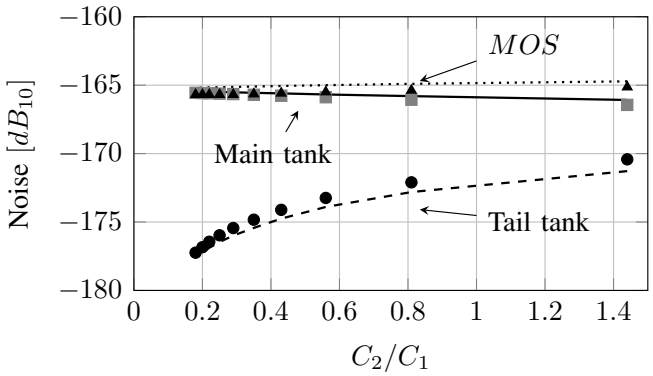

Fig. 8: Output noise not normalized to the carrier of the different sources: simulated (markers) and calculated (lines) of oscillator of Fig. 3a

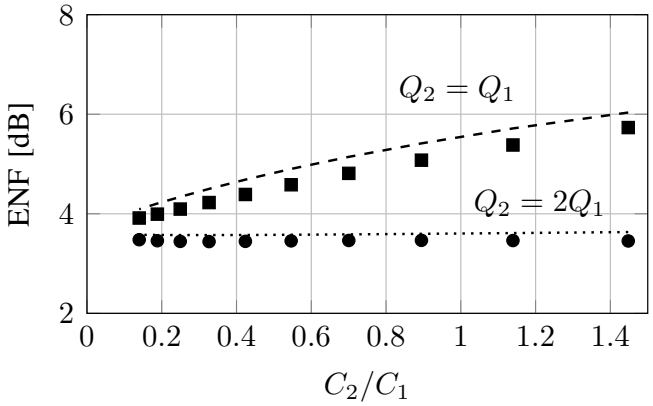

Fig. 9: ENF for different values of tank capacitors and quality factors simulated (markers) and calculated (lines)

Adding up all the contributions the transistors ISF Γ_M is found as:

$$\Gamma_M = \frac{1}{A_1\left(1+4\frac{C_2}{C_1}\frac{A_2^2}{A_1^2}\right)}\Big(-\frac{A_1}{2}\cos(\varphi) - 2A_2\sin(2\varphi) + \frac{(4C_1+C_2)\cos(\varphi)(A_1 f(\varphi) + 8A_2 g(\varphi)\sin(\varphi))}{4(2C_1+C_2)}\Big) \tag{9}$$

The above expressions were validated against numerical simulations for different values of device parameter using the method suggested by Pepe *et al.* [47], based on periodic transfer function simulations. The results for a representative case are plotted in Fig. 6-7.

4) Total Phase Noise: Starting from the ISFs expression in (4), (7) and (9) the corresponding phase noise contributions have been calculated, as shown in Appendix A. The results are compared with simulation results in Fig. 8. It can be seen that our analysis accurately models not only the overall phase noise, with less than $0.5dB$ error, but also its main individual contributions, with an error always less than 1dB. Using further simplified ISF expressions, i.e. considering only the harmonic components at f_0 and $2f_0$, the following closed form expression for the oscillator phase noise is found:

$$L_{tot}(\Delta\omega) = 10\log\Big(\frac{k_B T}{2P_{sig}}\left(\frac{\omega_0}{\Delta\omega Q_1}\right)^2 \cdot \frac{(1+\gamma)(1+16\frac{A_2^2}{A_1^2}\frac{C_2}{C_1}\frac{Q_1}{Q_2})}{\left(1+4\frac{C_2}{C_1}\frac{A_2^2}{A_1^2}\right)^2}\Big) \tag{10}$$

Based on (10) the ENF has been calculated for different values of the tank capacitors and quality factors and compared with simulations in Fig. 9. A few considerations can be made. As (10) suggests, as a general rule the quality factor of the second harmonic tank should be maximized. In this way three effects are achieved. First, the absolute noise is reduced. Second, the impedance seen by the main tank during the switching transitions is increased, reducing loading effects. This translates into a reduction of the factor that multiplies $1+\gamma$ in (10). Third, power efficiency is increased. Another design choice is the size of the tail capacitance C_2. Notice that C_2 appears squared at the denominator and instead it is linear at the numerator in (10). However, C_2 is always multiplied by the square of A_2 and, if C_2 is increased, A_2 decreases, leading to a higher phase noise. The ENF shows an optimum for a relatively small values of

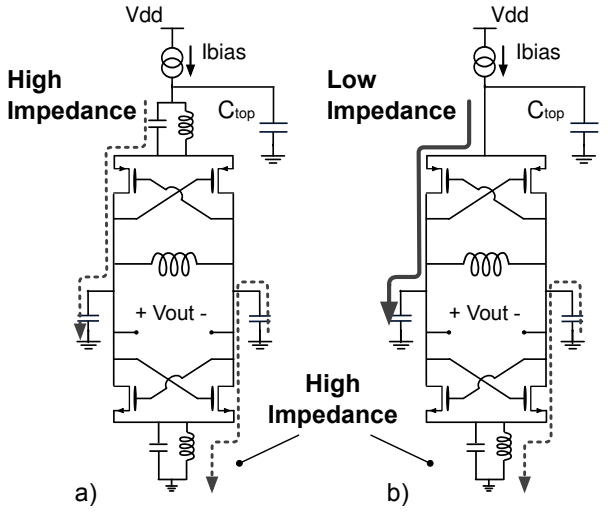

Fig. 10: Complementary p-n class-B oscillator with a) dual and b) single $2\omega_0$ LC tanks at the tails

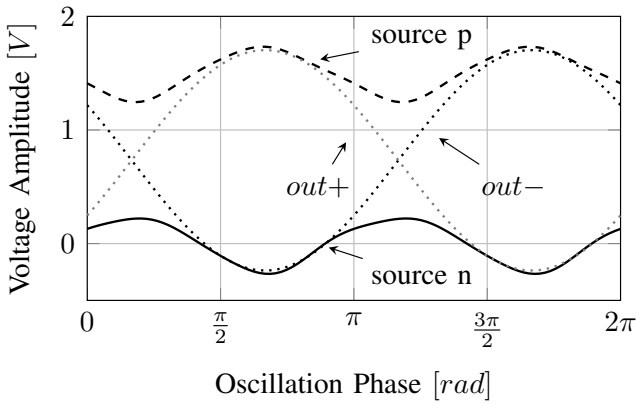

Fig. 11: Simulated voltage waveforms of the oscillator in Fig. 10a

C_2 which depends on the quality factors ratio Q_2/Q_1. If Q_2 is larger than Q_1 then the value of C_2 has a reduced effect. Assuming a very high Q_2, the numerator in (10) approaches $1+\gamma$ and eventually surpassing the behavior of a "close to ideal" oscillator as given by (2). It is worth mentioning that a good approximation of the switching behavior is mandatory to obtain an accurate result (a key difference compared to the class-F analysis in [2]).

B. P-N class-B Oscillator with Tail Filter

Let us now consider the p-n Class B oscillator shown in Fig. 3b, where two second harmonic tail resonators are used, one at the NMOS source and the other at the PMOS source. Notice that, a simpler solution would be the one shown in Fig. 10b, where the source of the PMOS transistors is connected directly to the current source and to the large capacitor C_{top}. It was shown by Andreani [48] that assuming a perfectly differential tank capacitance and a high impedance on one side, a complementary class-B oscillator has the same phase noise behavior of an N-only oscillator. However, since the tank cannot be made perfectly-differential, the PMOS transistors noise would see a low impedance path to ground, thereby loading the tank and increasing phase noise at large amplitudes [49]. The impulse sensitivity function theory can be applied to resonators which consist of more energy storing elements (e.g. a transformer). According to the ISF theory when a noise impulse charge is applied, only the voltage across the capacitor changes and no effect is present on the current flowing through the inductor [1]. This will be confirmed by simulation results at the end of this section. To compute the ISF for each noise source the starting point is the definition of the state vector, that in this case is of sixth order since three tanks are present:

$$\begin{aligned}\vec{X} = [V_{C_1} \quad & \sqrt{\frac{L_1}{C_1}} I_{L_1} \quad \sqrt{\frac{C_{2n}}{C_1}} V_{C_{2n}} \\ & \sqrt{\frac{L_{2n}}{C_1}} I_{L_{2n}} \quad \sqrt{\frac{C_{p2}}{C_1}} V_{C_{2p}} \quad \sqrt{\frac{L_{2p}}{C_1}} I_{L_{2p}}]\end{aligned} \tag{11}$$

Now referring to Fig. 11 the steady state is approximated $V_{C1} = A_1 \sin(\omega_0 t)$, $V_{C_{2n}} = A_{2n}\cos(2\omega_0 t)$ and $V_{C_{2p}} = -A_{2p}\cos(2\omega_0 t)$.

1) Noise Sources and ISF: Following the same steps outlined above for the N-only oscillator, the ISF for the main tank can be calculated as

$$\Gamma_1 = \frac{\cos(\omega_0 t)}{\left(1 + 4\frac{C_{2n}}{C_1}\frac{A_{2n}^2}{A_1^2} + 4\frac{C_{2p}}{C_1}\frac{A_{2p}^2}{A_1^2}\right)} \tag{12}$$

It is clear that (12) is equal to (4) if $A_{2n} = A_{2p} = A_2$ and $C_{2n} = C_{2p} = C_2/2$ and everything else is the same. To model the effect of cross-coupled pairs switching on the tail tanks, the functions $f_n(\varphi)$ and $f_p(\varphi)$ are defined, similarly to the $f(\varphi)$ function for the N-only oscillator:

$$f_{n,p}(\varphi) = \frac{A_1 \sin(\varphi)}{2(A_{2n,p}\cos(2\varphi) - V_{dc})} \tag{13}$$

where V_{dc} is the common mode output voltage. Using the above definitions, the effect of Δq on the tank voltages V_1 and V_{2n}/V_{2p} can be written similarly to (5) with $f(\varphi)$ replaced by $f_n(\varphi)$/$f_p(\varphi)$. The underlying assumption is that a charge injected at the NMOS tail has no effect on the PMOS tail capacitance and vice versa. Following the same steps as for the N-only oscillator, the ISF of the tail tanks Γ_{2n} and Γ_{2p} can be calculated. A simple analytical expression can be found extracting only the dominant harmonic component at $2f_0$:

$$\Gamma_{2,n/p} \approx \frac{\left(2\sqrt{2}\frac{A_{2,n/p}}{A_1}\sin(2\varphi)\right)}{\left(1 + 4\frac{C_{2n}}{C_1}\frac{A_{2n}^2}{A_1^2} + 4\frac{C_{2p}}{C_1}\frac{A_{2p}^2}{A_1^2}\right)} \tag{14}$$

As for the main tank ISF, (14) is equal to (7) if $A_{2n} = A_{2p} = A_2$ and $C_{2n} = C_{2p} = C_2/2$ and everything else is the same. To evaluate the ISF of the transistors, we start considering the effect of a charge injected between the drain and source of the NMOS transistor M2 in Fig. 3b. The injected charge Δq can be decomposed into a charge injected at the source plus an opposite charge injected at the drain that can be split into equal common-mode and differential components. The effect of the differential charge injected at the drain is only on the main tank capacitors: $\Delta V_1 = \Delta q/2C_1$. The combined effect

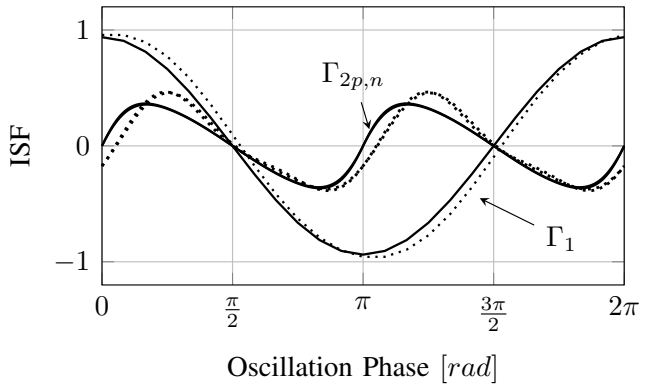

Fig. 12: Main tank (Γ_1) and tail tanks (Γ_2) ISFs simulated (dotted) and evaluated (continuous) of oscillator of Fig. 3b

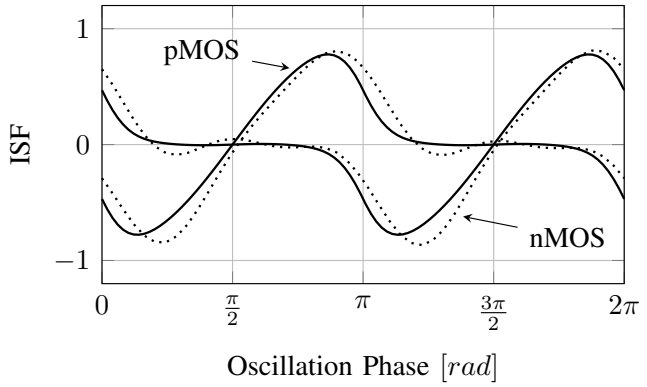

Fig. 13: Active devices (nMOS, pMOS) ISF simulated (dotted) and evaluated (continuous) of oscillator of Fig. 3b

of injecting Δq at the source and $\Delta q/2$ at the two drains is highly time-varying. When M2 and M3 are ON, we have:

$$\begin{aligned}\Delta V_1 &= -\frac{\Delta q}{2C_1+C_{2p}} - \frac{\Delta q}{2C_1+C_{2n}}\\ \Delta V_{2,n} &= \frac{\Delta q}{2C_1+C_{2n}}\\ \Delta V_{2,p} &= -\frac{\Delta q}{2C_1+C_{2p}}\end{aligned} \tag{15}$$

When M2 and M3 are OFF, the sign of ΔV_1 is reversed, while ΔV_{2n} and ΔV_{2p} stay the same. During switching transitions $\Delta V_1 = \Delta V_{2p} = 0$ and $\Delta V_{2n} = \Delta q/C_{2n}$. As a result the ISF is well approximated as:

$$\Gamma_{M,n} = \frac{\left(\frac{A_1}{2}\cos(\varphi) + 2A_{2,n}\sin(2\varphi)\right)}{A_1\left(1 + 4\frac{C_{2n}}{C_1}\frac{A_{2n}^2}{A_1^2} + 4\frac{C_{2p}}{C_1}\frac{A_{2p}^2}{A_1^2}\right)} \tag{16}$$

Similarly, the ISF of the PMOS transistors can be derived as:

$$\Gamma_{M,p} = \frac{\left(-\frac{A_1}{2}\cos(\varphi) - 2A_{2,p}\sin(2\varphi)\right)}{A_1\left(1 + 4\frac{C_{2n}}{C_1}\frac{A_{2n}^2}{A_1^2} + 4\frac{C_{2p}}{C_1}\frac{A_{2p}^2}{A_1^2}\right)} \tag{17}$$

Fig. 12-13 report the simulated and calculated waveforms for the main tank, the tail tanks and the NMOS and PMOS transistors ISFs, showing in all cases quite good accuracy.

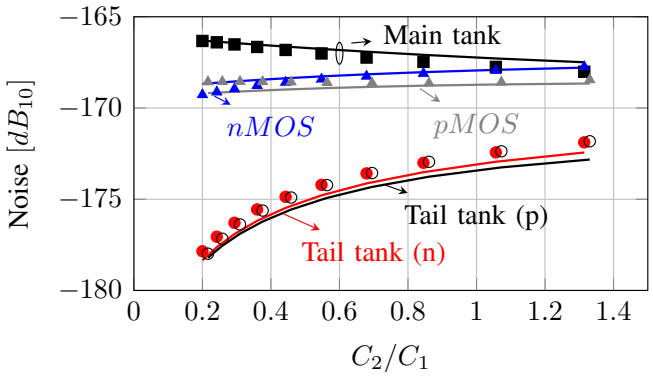

Fig. 14: Output noise not normalized to the carrier of the different sources: simulated (markers) and calculated (lines) of oscillator of Fig. 3b

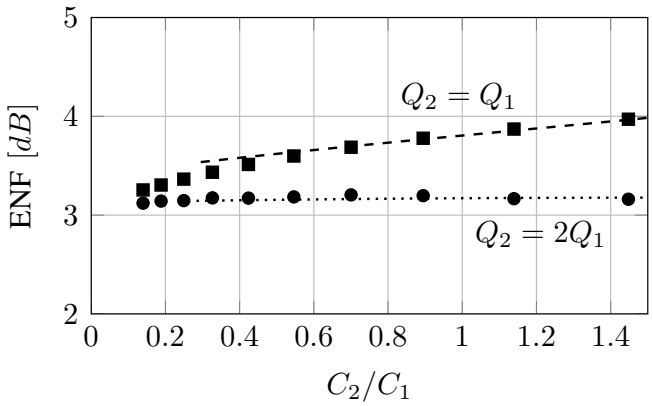

Fig. 15: Simulated Excess Noise Factor of N only (markers) and p-n (lines) (oscillators of Fig. 3)

2) Overall Phase Noise and ENF: Starting from the ISFs expressions in (12), (14) and (16)-(17) the corresponding phase noise contributions have been calculated, as shown in Appendix A. The results are compared with simulation results in Fig. 14 showing very good accuracy as for the N-only oscillator. To compare p-n and N-only oscillators the ENF has been calculated and simulated for both and the results are plotted in Fig. 15 for different values of tail tanks capacitance and quality factors. In the designs the p-n oscillator is operated at twice the supply voltage of the N-only and the tail capacitors C_{2n}, C_{2p} are both set to $1/2$ the value of C_2 in the N-only. As expected the ENF of the two oscillators is essentially the same, showing once again that in principle, when no design constraints are imposed, N-only and p-n structures achieve the same efficiency. One main drawback in using the p-n oscillator with tail filter is related to the need of two tail filters, which means more than doubling the filter's area occupation [50]. The use of a transformer at the tail represents a suitable solution to this problem without changing the ISF and thus the characteristic of this topology (Fig. 16 shows the simulated transistor's ISF with and without the magnetic coupling). The use of a transformer, however, leads to practical limitations, since for example in general is easier to achieve a better quality

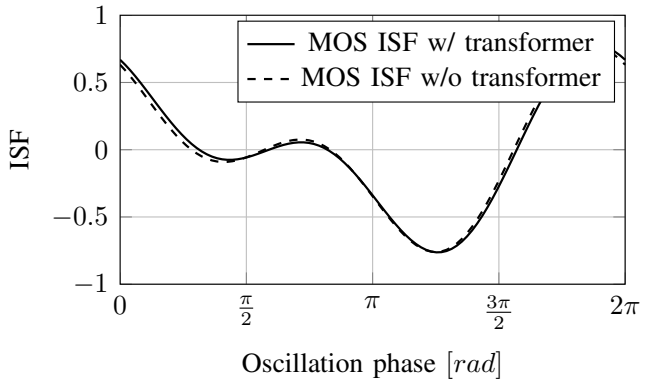

Fig. 16: Simulated ISFs with and without transformer coupling of Fig. 18

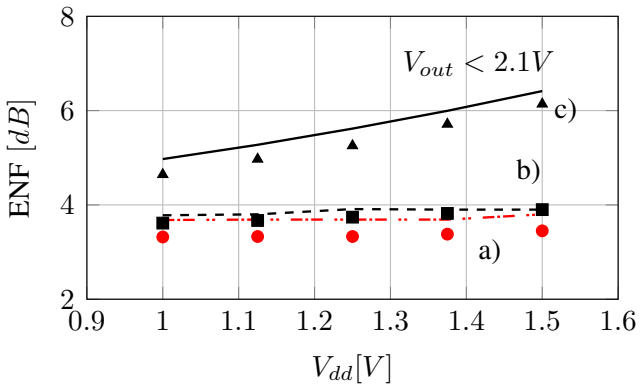

Fig. 17: Excess noise factor of a) p-n (red) and b,c) N only (black) oscillators (Fig. 3) as a function of supply voltage: simulated (markers) and calculated (lines)

factor by using two separate inductors instead of a transformer, but the analysis presented is a suitable tool to determine the impact on the overall performance.

C. Effect of supply voltage limitations on P-N and N-only oscillators

The above analysis has disregarded any consideration related to technology reliability limitations. When these limitations are considered, depending on the type of transistors, the topology and on the available voltage supply the minimum achievable ENF can be affected. The large electric field experienced by the gate oxide in high swing oscillators can potentially reduce their long term reliability mainly due to time-dependent dielectric breakdown (TDDB) [51]. In our design a 55nm CMOS technology was adopted, which provides standard transistors with a nominal supply of 1.2V and high voltage thick (3.4nm) oxide transistors having a nominal supply voltage of 1.8V. The data extrapolated from the manufacturer TDDB reliability guidelines suggest a maximum DC oxide voltage of 2.4V for thick oxide devices for 10-years 0.1% chip failure rate at 125^oC. Recent publications [28], [51] analyze more in detail reliability issues in oscillators suggesting that such limits may be overly pessimistic. Publicly available data [51] on 3.5nm thick oxide devices indicate a characteristic time to breakdown (η) of $8 \cdot 10^5 s$ (for 63.3% probability) at 4V oxide voltage and 140^oC for an area of $10^3 \mu m^2$. Applying the Weibull distribution [51] with a slope factor $\beta = 2$, a voltage acceleration factor $n = 40$ and a device size of $50\mu m^2$ the estimated maximum voltage is about 3.2V [3] for a time to breakdown (T_{BD}) of 10 years with a circuit failure rate of 0.002% (roughly corresponding to a $10mm^2$ chip failure rate of 0.1% for a $0.2mm^2$ circuit area). An accurate technology reliability characterization is necessary to correctly estimate the maximum voltage for the desired T_{BD}. In our design a conservative 2.1V maximum VCO swing (peak differential) was taken as a design target that corresponds to about 2.15V maximum gate-source voltage swing. This was obtained from the maximum oxide voltage specified by the manufacturer reduced by about 10% to take into account the uncertainty in the control of the maximum VCO swing in the presence of technology temperature and supply variations. Keeping the (fairly aggressive) safety margin of 10% but starting from the less conservative maximum oxide voltage of 3.2V the maximum VCO swing becomes about 2.8V. An N-only topology achieves the same minimum ENF of a corresponding complementary pn-structure at twice the voltage swing and is therefore more affected by reliability constraints. In Fig. 17 we report the minimum achievable ENF for a p-n (curve a) and an N-only (curve b) class-B oscillators with resonant tail filters as a function of the supply voltage. The simulations were carried out using high voltage transistors. In curve b the N-only oscillator is pushed to its maximum voltage swings and it achieves approximately the same ENF of the p-n oscillator. However, for a supply voltage of 1.5V the maximum swing is close to 3.8V, which exceeds even more the relaxed oxide reliability limits. If the maximum voltage swing is limited to 2.1V, curve c is obtained. At 1.5V the minimum achievable ENF increases by as much as 3dB. The penalty gradually reduces as the supply voltage is reduced and is below 1dB for 1V supply voltage.

[3]Notice that, given the exponential dependence between T_{BD} and oxide voltage, the fact that the oxide reaches the peak voltage only for a small fraction of the oscillation period does significantly change the maximum allowed voltage in AC regime with respect to DC [28].

IV. Oscillator Design and Experimental Results

The difficulty to extract the tank Q, together with the high sensitivity of phase noise to Q, limits the ability to accurately assess the potential of a new topology. Because of this we have built a test chip that allows to compare the proposed topology with a reference oscillator, both working in the same operating conditions. The implemented chip prototype includes the class-B complementary p-n oscillator (with magnetically coupled tail filters), together with a class-B N-only oscillator with a single tail filter (used as reference) and was fabricated in a 55nm standard CMOS technology with only one thick metal layer. Circuit schematics are reported in Fig. 18. The oscillators use thick oxide devices and are biased from a 1.5V internal supply derived from the external 1.8V supply through an on-chip band-gap referenced programmable low-voltage-drop regulator. Both use identical tanks and can be tuned from

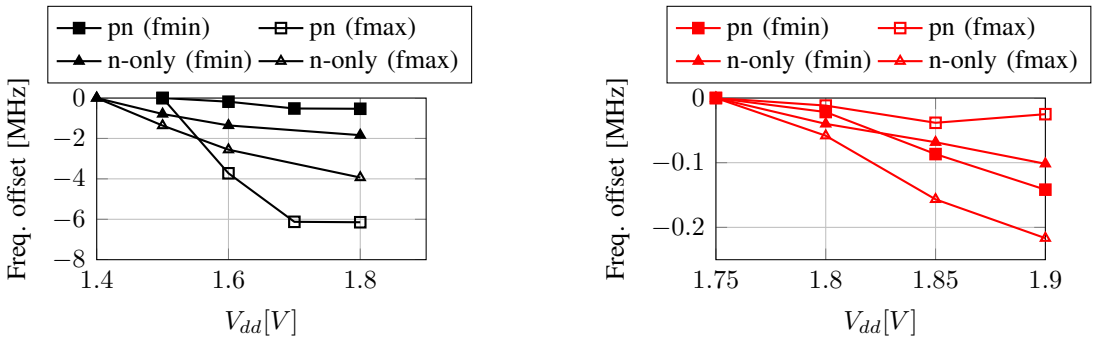

Fig. 23: Frequency pushing measurements (after frequency divider): measured frequency offset from nominal as function of the supply voltage (a) and as a function of the regulator supply voltage (b).

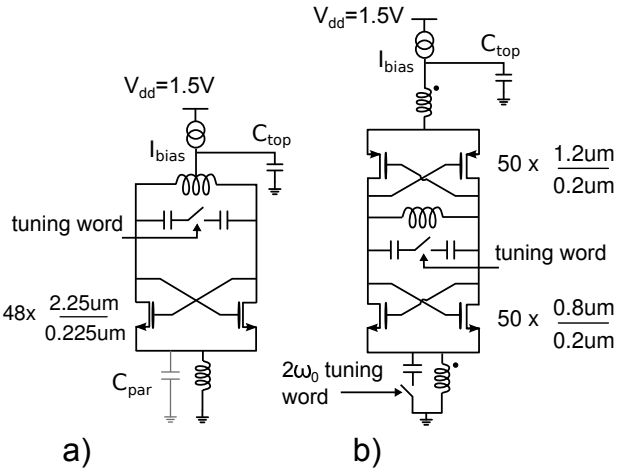

Fig. 18: Class-B oscillators with $2\omega_0$ LC tail filters: a) N-only and b) p-n

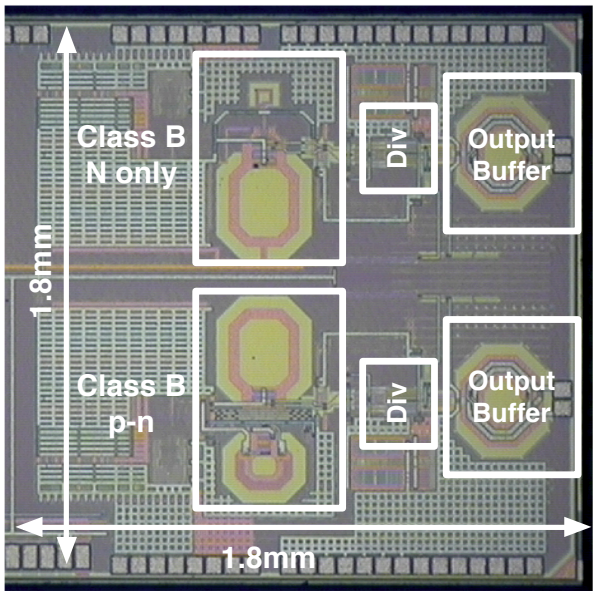

Fig. 19: Chip photo

about 7.4GHz to 8.4GHz (before frequency division by 2, using a classical CML divider) with a 5 bits MOM capacitor bank. Small sized varactors (used for fine tuning) were not included. For the tail tank the main design goal is to maximize its impedance at $2\omega_0$. This can be achieved using a high Q tank and/or a large inductor. A small inductor with high Q is preferable because it allows to use very large switching devices (with very low r_{ON} but large parasitic capacitance). This allows to improve power efficiency and gives about 1dB phase noise improvement (from simulations), although at the cost of an extra capacitor array for the tuning of the $2\omega_0$ tank. Using coupled inductors allows to save area and to use single tunable capacitor array. The coupled tanks (with inductor values of 180pH and 130pH and a coupling factor of 0.7) have a quality factor of about 10. A single 3-bit capacitor bank at the NMOS switching transistors source (controlled independently from the main tank) is used for tuning them. For the N-only oscillator the single tail tank has a quality factor of about 6 and uses an inductor of 300pH. A die photograph of the oscillators is shown in Fig. 19: the N-only and p-n oscillators have an active area of $0.17mm^2$ and $0.19mm^2$ respectively. Figure 20 shows the measured phase noise at the minimum and maximum frequencies for both oscillators. The $1/f^3$ noise corner is between 200kHz and 400kHz for the p-n oscillator and between 400kHz and 600kHz for the N only while the $1/f^2$ noise exceeds the 2G TX specification at 20MHz frequency offset by more than 7dB for the p-n oscillator and by 8 dB for the N-only, giving sufficient margin for other non-idealities. N-only oscillator (Fig. 20) has higher flicker noise sensitivity compared to the p-n, probably due to a slightly mistuning of the tail filter [52]. Fig. 21 shows the phase noise of both oscillators at the maximum frequency as a function of power consumption. The p-n oscillator reaches a minimum phase noise of $-151.5dBc/Hz$ for an estimated oscillation amplitude of $1.6V$. The p-n oscillator has 0-1dB lower phase noise of the N-only one with half the power consumption (i.e. the same output voltage for the same tank) thanks to the higher Q of the tail resonator. The N-only oscillator reaches its minimum phase noise of $-156dBc/Hz$

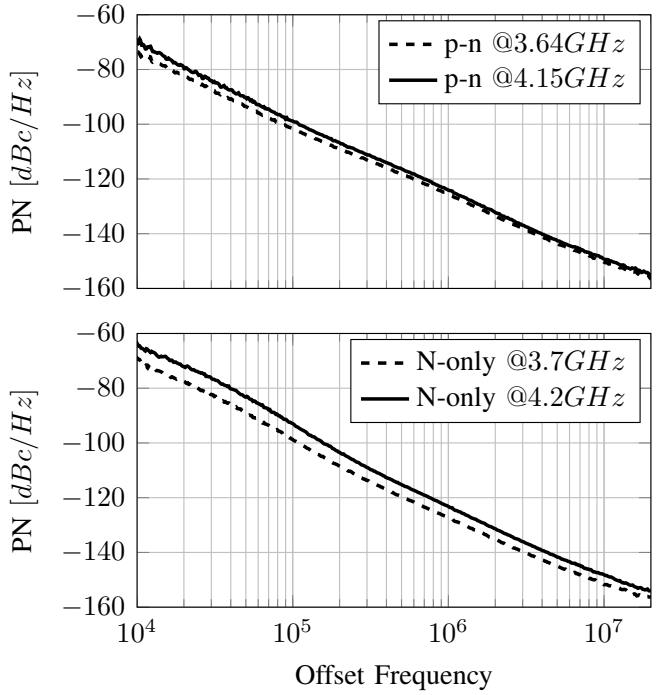

Fig. 20: Phase noise measurements (after freq divider by 2) at the minimum and maximum frequency of oscillation

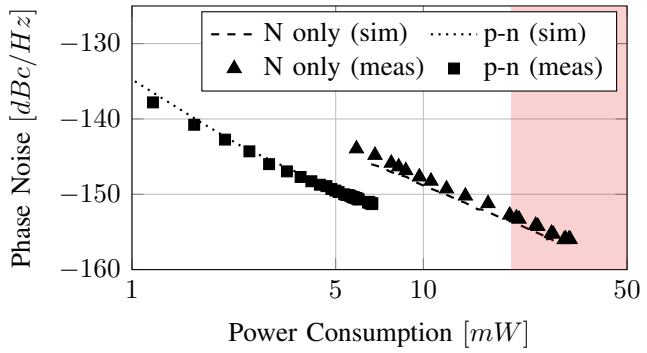

Fig. 21: Measured (dots) phase noise at 10MHz offset after freq. divider by 2 and simulated (lines) phase noise with 6dB reduction as a function of power dissipation of p-n and N only oscillators. Shaded area corresponds to voltage swings in excess of 2.1V

at ~ 4 times the power consumption of its p-n counterpart (i.e. for an amplitude of $\sim 3.2V$). The tail tank of the N-only is not tunable, which leads to some residual loading effects, responsible for an estimated 0.5-1dB phase noise degradation. The best achievable FoM is 195.6dBc/Hz for the p-n oscillator and 192.3dBc/Hz for the N-only, if conservatively limited to AC output voltage of 2.1V, and it varies about 1.3dB and 1.8dB respectively across the tuning range (Fig. 22). Pushing the N-only to its limit oscillation amplitude further improves its FoM to 193.5dBc/Hz, but poses reliability concerns. Table I compares the two prototype oscillators with the state of the art. With the exception of [3], the average FoM over the tuning range of the p-n oscillator is the highest reported. However

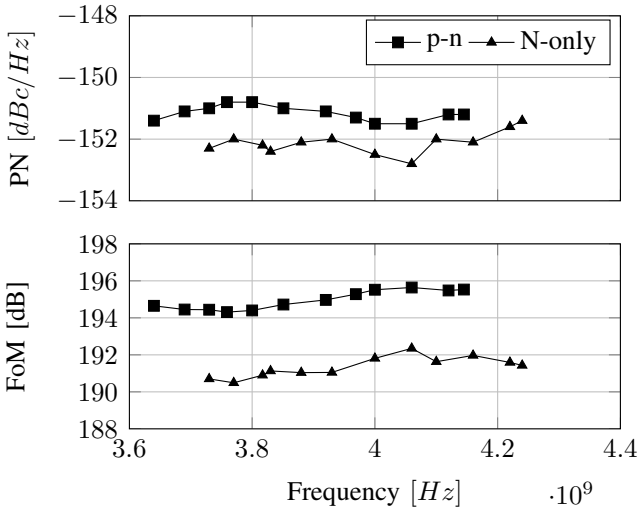

Fig. 22: Measured phase noise and FoM at 10MHz offset over tuning range

the oscillator in [3] has an unpractical low supply and its FoM drops by 1dB for a 25mV supply voltage variation. For a further comparison the ENF was computed. The Q of the two prototype oscillators was estimated measuring both the minimum supply current needed to start-up oscillations and the maximum absorbed current for a given supply voltage. Fitting the measured number with simulation gives in both cases an estimated Q between 14 and 15. Together with the same oscillator topology of the N-only oscillator in [26] (that does not take into account any possible stress effect), the presented pn-oscillator has the lowest reported ENF. The p-n oscillator also has a high FoM_T of 197.1dBc/Hz , which is among the best of the high FoM and low ENF oscillators reported in the literature. Frequency pushing was measured at maximum and minimum frequencies by changing the regulator output voltage and varying the regulator supply voltage and the results are reported in Fig. 23.

V. Conclusion

The phase noise of N-only and p-n class-B oscillators with second harmonic tail resonant tanks has been analyzed. An accurate analytical formula is found that provides useful design insights. The analysis shows that the p-n oscillator outperforms the N-only for supply voltages of 1V or higher. We have proposed a complementary class-B oscillator with transformer based tail filtering that exhibits a high efficiency and has 3-4dB better FoM than a reference N-only oscillator, when the maximum AC output voltage is conservatively limited to less than 2.1V, at a supply voltage of 1.5V. The transformer based tail filter permits to save area compared to classical implementations and allows to achieve a more constant FoM across the tuning range thanks to the tuning. The fabricated 55nm CMOS oscillator displays one of the best reported ENF avoiding reliability concerns.

$$L_M(\Delta\omega) = 10\log\Big(\frac{2}{T}\int_0^T \frac{4k_BT\gamma\sum_{k=0}^{\infty} kI_{k,out}\cos(k\omega_0 t+\phi_k)}{2q_{max}^2\Delta\omega^2}(\frac{A_1}{2}\cos(\omega_0 t)+2A_2\sin(2\omega_0 t))\,dt\Big) \tag{A.5}$$

APPENDIX A

The system can be represented as the steady-state vector $\vec{X}_0$ [1], [44], [45] in (A.1) to which a random perturbation vector ΔX will be added:

$$\vec{X}_0 = [A_1\sin(\omega_0 t) \quad A_1\cos(\omega_0 t) \quad A_2\sqrt{\frac{C_2}{C_1}}\cos(2\omega_0 t) \quad A_2\sqrt{\frac{C_2}{C_1}}\sin(2\omega_0 t)] \tag{A.1}$$

When a charge pulse Δq is applied across one of the capacitors a steady state phase error is produced in the oscillator. The phase error $\Delta\phi_i = \Gamma(\omega_0 t)\Delta q/q_{max}$ is a function of the time instant (within the oscillation period) when the charge pulse is injected and is proportional to the Impulse Sensitivity Function Γ. Neglecting the component of ΔX orthogonal to the trajectory, the phase perturbation $\Delta\phi$ can be derived from the state variables derivatives dX/dt [1], [45] where the ISF in terms of state-space vectors is given in (A.2) [1], [45].

$$\Gamma_i = \omega_0\frac{q_{max}}{\Delta q}\frac{\Delta\vec{X}_i\cdot\dot{\vec{X}}}{|\dot{\vec{X}}|^2} \tag{A.2}$$

In (A.2) q_{max} is just a normalizing factor, being the maximum charge across the capacitor placed between the nodes of interest.

Once the phase responses of the noise sources have been evaluated, the phase noise $L(\Delta\omega)$ caused by a white current noise source $\overline{i_{n,i}^2}$ can be obtained using (A.3).

$$L(\Delta\omega) = 10\log\left[\frac{\Gamma_{i_n,rms}^2\overline{i_{n,i}^2}/\Delta f}{2q_{max}^2\Delta\omega^2}\right] \tag{A.3}$$

This assumes that the noise perpendicular to the steady state-space trajectory of the oscillation does not generate any contribution to phase noise. Andreani and Wang [45], based on the more accurate phase noise evaluation proposed by Demir *et al.* [53] and Kaertner [44], have demonstrated that the error made without considering this component, using appropriate normalization factor of the state variables, is in fact negligible.

The active devices are clearly non-stationary sources: $\overline{i_{n,MOS}^2} = 4k_BT(\gamma g_m(\omega_0 t)+g_{ds}(\omega_0 t))$. Their phase noise contribution can be calculated using the general expression:

$$L_M(\Delta\omega) = 10\log\left(\frac{1}{T}\int_0^T\frac{i_{n,MOS}^2(\omega_0 t)\Gamma_M^2(\omega_0 t)}{2q_{max}^2\Delta\omega^2}\right) \tag{A.4}$$

It is easy to show that since g_{ds} is large only when Γ_M is close to zero, its contribution can be neglected, hence $g_m(\omega_0 t)$ can be expressed as $(\partial I_D/\partial t)/(\partial V_{gs}/\partial t)$. Furthermore, since $\partial V_s/\partial t$ is close to zero during the switching transients, as shown in Fig. 11, i.e. when both $g_m(\omega_0 t)$ and $\Gamma_M(\omega_0 t)$ are non-zero, $\partial V_{gs}/\partial t$ in (A.4) can be approximated as $-\partial V_{ds}/\partial t$ yielding the simplified expression in (A.5).

Where $\Gamma_M(\omega_0 t)$ was approximated considering only the first and second harmonic. In A.5 only the first and second harmonic of the drain current, equal respectively to the main and tail tank currents, give a non-zero integral. The resulting overall phase noise expression is reported in (10), confirming the general result that the active devices contribute γ times the phase noise contribution due to the tanks losses. Notice that the general result found in [6], [30] in principle cannot be applied since the active devices work in deep triode and they do not act as a memory-less transconductor due to the tail tank.

ACKNOWLEDGMENT

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