A 40-67 GHz Power Amplifier with 13dBm P_{SAT} and 16% PAE in 28nm CMOS LP

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ABSTRACT

Pushed by the availability of large fractional bandwidths, many well-established applications are focusing mm-wave spectrum for product deployment. Generation of broadband power at mm-waves is challenging because a key target such as the efficiency trades with the gain-bandwidth (GBW) product. The major limit is the capacitive parasitics at the interstage between driver and power devices. The latter are designed with a large form factor so as to deliver the desired output power and are commonly biased in class-AB to achieve high drain efficiency, penalizing GBW. In this paper, a design methodology for interstage and output matching networks targeting large fractional bandwidth and high efficiency is proposed. Leveraging inductively coupled resonators, we apply Norton transformations for impedance scaling. In both networks, topological transformations are employed to include a transformer, achieve the desired load impedance and minimize the number of components. A two-stage differential PA with neutralized common source stages has been realized in 28 nm CMOS using low-power devices. The PA delivers 13dBm saturated output power over the 40-67GHz bandwidth

with a peak power-added efficiency of 16% without power combining. To the best of author's knowledge, the presented PA shows state-of-the-art performances with the largest fractional bandwidth among bulk CMOS mm-wave PAs reported so far.

LIST OF KEYWORDS

Millimeter wave integrated circuits, Power amplifiers, Broadband amplifiers, Resonator filters, CMOS integrated circuits, Gain-bandwidth product, Coupled resonators

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I – INTRODUCTION

The design of wideband systems at mm-waves is drawing more and more attention, enabling high data rate short-range wireless systems using simple modulation schemes, key for low-cost consumer applications [1, 2]. In addition, other industrial areas, such as remote sensing and imaging systems, are focusing new portions of the spectrum, towards mm-waves. Well-established applications, such as body scanners for homeland security and medical screening imagers for diagnosis and treatment, push for very wide fractional bandwidths to achieve high spatial resolution and minimize acquisition time [3, 4].

Circuit techniques for wide instantaneous bandwidths are presently being investigated, both at receiver and transmitter sides [5-8]. CMOS, the technology of choice for cost reasons, lends itself to narrow-band operation leveraging LC resonances of capacitive parasitics to restore gain at high frequency. But the gain-bandwidth (GBW) product of a LC loaded common source stage is g_m/C, with g_m the device transconductance and C the load capacitance, thus setting a trade-off between gain and bandwidth. Circuits aimed at processing small signals such as front-end low noise amplifiers tackle the problem using multi-stages thus extending GBW at the price of increased power consumption. On the other hand, generation of broadband power at mm-waves is challenging, because a key target such as efficiency trades with GBW. Typical design techniques are selected for best power efficiency [9-16]. To increase output power without compromising efficiency, power combining techniques has been exploited in [14-16].

Recently, designs tailored to wide bandwidth have been proposed: staggering is an established technique due to its simplicity, but it limits the gain and efficiency, which are precious at mm-wave frequency [12]. Distributed amplifiers can also be exploited to achieve wideband performance by absorbing transistor parasitic capacitors into transmission lines. However, conventional distributed amplifiers suffer from low power efficiency due to varying output voltage levels at different distribution stages and power consumed on resistive terminations.

Tapered distributed amplifiers can obtain the same output voltage for all stages and thus improve power efficiency [13]. However, they typically require a large die area and provide limited gain. Considering that GBW is primarily limited by interstage parasitics between driver and power stage, i.e. by the input capacitance of the last amplifier stage, this work follows a different approach, exploiting networks of order higher than two so as to achieve flat bands, as wide as possible, not compromising efficiency at given target output power. The realized PA uses two stages [8]. Design techniques for interstage and output networks are proposed to achieve flat response over a very wide frequency range. In both networks, topological transformations are employed to include a transformer for differential to single-ended conversion, to set the desired load impedance and to minimize the number of components. Implemented in a 28nm bulk CMOS LP process, the class-AB PA leverages the proposed techniques and shows broadband operation from 40GHz to 67GHz with 13dBm saturated output power, 13dB gain and 16% PAE.

II – GBW Trade-Offs in Power Amplifiers

To gain insight in the trade-offs between different PA parameters, we focus on a two-stage amplifier whose block diagram is shown in Fig. 1. The matching network is used to scale the antenna impedance to the load resistance R_L. The network has to introduce minimum insertion loss to preserve the efficiency. In addition, it should accommodate the large pad capacitance C_{pad} and the drain parasitic capacitance $C_{o,PA}$ of the output transistor M_{PA}. The latter is designed with a large form factor to deliver the desired power to R_T and it is commonly biased in class-AB to achieve high drain efficiency. GBW of the output stage is limited by the large drain capacitance $C_{o,PA}$ and low transconductance of M_{PA} due to class-AB biasing. With a target output power of few tens of mW, R_T must range in the tens of Ωs. Impedance transformation limits the operation bandwidth and further decreases GBW of the output stage.

The low value of R_T limits the gain of the output stage and transistor M_{DR} is required to drive M_{PA} increasing the overall gain of the PA. Inductor L_1 provides the supply current to M_{DR} and it

is sized to resonate out the interstage parasitic, mostly determined by the input capacitance $C_{i,PA}$ of the output stage. To maintain high power efficiency, a large scaling factor between power and driver stage transistors is desirable, but M_{DR} needs to drive a large input capacitance $C_{i,PA}$ of M_{PA} with a small transconductance, significantly limiting GBW of the driver, $\sim g_{m,DR}/C_{i,PA}$. Therefore, given a target gain, the design of the driver stage sets a severe trade-off between bandwidth and PA efficiency.

In the following paragraph, insights on the trade-off are given through a quantitative example when no matching network is employed. Then, we discuss how the employment of a network aimed at GBW enhancement can relax the aforementioned trade-off, allowing enhanced efficiency at the same fractional bandwidth and gain level.

Simulations of the differential version of the 60GHz PA of Fig. 1 have been performed in a 28nm CMOS technology with a 1V supply. The width of the last stage transistors is set to 200μm. In order to investigate the impact of the driver stage design on the PA bandwidth and efficiency, the output matching network has not been included. L_2 resonates out $C_{o,PA}$ at 60GHz and a 50Ω load resistance is assumed, leading to a maximum saturated output power of P_{SAT}=14dBm. The driver is loaded by resistor R_D that determines gain and bandwidth. Simulations have been performed for different driver sizes: for each of them inductor L_1 and resistor R_D were adjusted to resonate at the center of the passband and maintain constant gain. A smaller resistance increases the bandwidth, but a larger driver size, and hence power dissipation, is required to restore the gain. Fig. 2 shows a plot of the overall PA peak efficiency when it delivers P_{SAT}, as a function of the driver bandwidth. Class-A and class-AB biasing of the output stages are compared. In both cases, a severe trade-off between bandwidth and efficiency is evident. For example, in class-AB biasing, extending the bandwidth from 20% to 55% needs a 5x increase of the driver transistor size, reducing the efficiency from 26% to 10%. Interestingly, when looking for very high fractional bandwidths, class-A is preferable in terms of efficiency. If,

for example, a 60% fractional bandwidth is targeted, biasing the output stage in class-AB yields an efficiency of 8% while biasing it in class-A yields a 50% higher efficiency. This is because, for the same bandwidth, the higher gain of the class-A output stage allows to reduce the driver size, thus saving power.

In both cases, to keep high efficiency when targeting wide bandwidth, a network aimed at extending GBW is key, compared to the use of a single interstage inductor. The GBW enhancement (GBWEN) can be exploited to scale down the driver size reducing its power dissipation. If, for example, a fractional bandwidth of 55% were targeted, assuming class-AB output stage operation, an interstage network with GBWEN=3 would allow the designer to select a 5x smaller driver size and improve efficiency from ~10% to ~26%.

Output and interstage matching networks play a critical role in PA design and motivate investigations. Coupled resonators are introduced in the next section as a mean to implement both interstage and output matching networks with GBWEN, thus optimizing bandwidth and efficiency.

III – Inductively Coupled Resonators

Techniques to enhance the GBW of amplifiers have been of great interest since the early beginning of the 19th century. Chief among many results, Bode proved that the maximum achievable GBWEN for a two-port passive network is $\pi^2/2 \cong 4.93$, when the input capacitance is equal to the output capacitance [17]. Still, many inductors or transmission lines are necessary to support a wide bandwidth, resulting in high power losses and the need of restoring gain, thus dramatically reducing efficiency, key figure of merit of power amplifiers. Furthermore, the topology of the network and the component values should enable a compact layout to minimize parasitics, particularly critical at mm-waves.

Coupled resonators technique has been recently exploited for wireless communication components and systems, such as LNAs [18,19] and wideband receiver front-ends [5,18]. Fig. 3

shows the general schematic, where the current injected into the first resonator (C_1 - L_1) is coupled to the second resonator (C_3 - L_3) through inductor L_2 for wideband operation. Circuit design is usually assumed under symmetric resistive load condition (i.e. doubly terminated filters), which however does not apply to the case of power amplifiers. In fact, as detailed in the following sections, resistors R_3 or R_1 can be neglected when coupled resonators are employed as interstage or PA output matching networks, respectively. That is, compared to previous works, coupled resonators are here revisited focusing on asymmetric load termination (i.e. singly terminated filters). Insights are given on the gain-bandwidth product enhancement properties and efficiency, particularly critical in power amplifier design.

In the case R_1 is neglected, the frequency transfer function $T(j\omega) = V_{out}(j\omega)/I_{in}(j\omega) = N(j\omega)/D(j\omega)$ can be approximated as

$$N(j\omega) = j\frac{\omega R_3}{\omega_0 Q}\frac{m}{1+d},$$

$$D(j\omega) \cong \left(1 + \frac{j\omega}{\omega_L Q_1} - \frac{\omega^2}{\omega_L^2}\right)\left(1 + \frac{j\omega}{\omega_H Q_2} - \frac{\omega^2}{\omega_H^2}\right), \quad (1)$$

where $\omega_0 = 1/\sqrt{L_1 C_1} = 1/\sqrt{L_3 C_3}$, $m = L_1/L_2$, $l = L_3/L_2$, $d = m + l$ and $Q = \omega_0 R_3 C_3$. $\omega_L = \omega_0$, $\omega_H = \omega_0\sqrt{1+d}$ are the resonant frequencies of the two biquadratic terms and

$$Q_1 = \frac{d}{m}Q, \qquad Q_2 = \frac{d\sqrt{1+d}}{d-m}Q. \quad (2)$$

Detailed calculations and assumptions leading to (1) are reported in the Appendix. Assuming a moderately large network $Q = \omega_0 R_3 C_3$, and $m = l$, $T(s)$ is equal at the two resonant frequencies and a symmetric response can be achieved. The value of $d = m + l = (L_1 + L_3)/L_2$ determines the bandwidth of the system. Once the lower edge of the bandwidth ω_L is set, increasing the value of d splits more and more the poles pair apart, thus widening the bandwidth. Coupling inductance L_2 is decreased and the two resonators are separated in frequency. As a consequence,

a wider bandwidth can be achieved at the expense of an increased in-band ripple. This behavior is clearly captured in Fig. 4 for the case $m = l$, where the response of the proposed network is plotted as a function of the parameter d $(0.95, 1.45, 1.95)$ for a fixed network Q $= 2$ and $\omega_0 = 2\pi$ 40GHz (assuming it is employed as output network, $R_3 = 50\Omega$ and $C_3 = 160fF$ to take into accont for pad and interconnects parasitic capacitance). An expression for the ripple R as a function of m and Q is reported in the Appendix.

As discussed in Section II, a network with high GBW is key in developing highly efficient power amplifiers. By exploiting the separation of the two capacitors by means of inductor L_2, coupled resonators realize a bandpass filter of higher order enhancing GBW. Indeed, compared to simply resonating (C_1+C_3) by means of an inductor, coupled resonators offer an improvement in gain-bandwidth product of

$$GBWEN = \alpha(R)(1 + C_1/C_3), \quad (3)$$

where $\alpha(R)$ depends on the in-band ripple. In the case of symmetric response (i.e. $m = l$), $C_1/C_3 = 1$ and $\alpha(R) = 1$, yielding a GBWEN of 2. If an in-band ripple up to 3dB is tolerable, $GBWEN$ is further increased to ~3. This behavior is captured by Fig. 4, where the designed networks with 0dB and 3dB ripple show a GBW of 23.7GHz and 38GHz, respectively, yielding an improvement ratio of $\alpha(R) \approx 1.55$ as predicted. It is worth noticing that a remarkable GBWEN of 2 is achievable with a symmetric response and 0dB in-band ripple with the use of 3 inductors only.

The analysis carried out so far assumed ideal lossless passive components. However, the finite quality factor of passive components significantly affects the efficiency and the frequency response of the network. As derived in Appendix, in the case of coupled resonators with symmetric response (i.e. $m = l$) the efficiency $\eta = P_{OUT}/P_{IN}$ at the edges of the band is given by:

$$\eta(\omega_L) \approx \eta(\omega_H) \approx \frac{1}{1+\frac{1}{Q_{Ind}Q}\left(Q+\frac{1}{m}+\frac{1}{m^2}\right)}\frac{Q_{Ind}}{Q_{Ind}+Q}\,, \tag{4}$$

where Q_{Ind} is the quality factor of the inductor components and P_{OUT} and P_{IN} are the power developed on resistor R_3 and the input power, respectively. Calculated and simulated efficiency are compared in Fig. 5 as a function of inductors' quality factor Q_{Ind} with $Q = 2$ for designs with 0dB and 3dB ripple, showing good agreement. Efficiency improves, though slightly, at higher ripple and hence bandwidth: bandwidth is widened by increasing m and decreasing inductor L_2, which consequently reduces its amount of losses.

Besides impairing network efficiency, lossy passive components affect the frequency response as well, compromising the gain flatness and hence the bandwidth. A very important feature of the proposed network of Fig. 3 is that it can be designed with a pre-emphasis in order to achieve flat response once implemented with lossy components. This behavior is illustrated by means of a design example. Fig. 6 shows the network response for a fixed $d = 1.5$ and three decreasing values of m: 0.75, 0.83 and 0.93 ($l = d - m$ is 0.75, 0.67 and 0.57, respectively). As it can be seen, relative values of m set the in-band gain and the symmetry of the response. In particular, the response peaks at the upper edge of the bandwidth as the relative value of m increases, realizing a peak of

$$\left|\frac{T(j\omega_H)}{T(j\omega_L)}\right| \cong \frac{m}{d-m}. \tag{5}$$

This is a very important degree of freedom to equalize the network frequency response. This feature is highlighted in Fig. 6b, where the network response is plotted as a function of finite inductors' quality factor Q_{Ind} ranging from 40 to 15 with step of 5. It is clear that by properly choosing m, the detrimental effect of lossy inductors can be minimized, equalizing the frequency response while widening the bandwidth.

IV – Power Amplifier Design

A 60-GHz PA in 28nm CMOS LP technology leveraging the design criteria emerging from sections II and III is presented in this section. Design targets are to deliver a P_{SAT}≈13dBm with PAE>10% over a fractional bandwidth greater than 40% and a supply of 1V. Fig. 7 shows the complete schematic of the PA prototype. The active stages rely on capacitively neutralized common-source pairs to improve gain, stability and reverse isolation [20,21]. The superior power gain of the neutralized amplifier stage allows a lower current density for the same gain, thus increasing efficiency. Design procedures are detailed in Subsec. IV-A and IV-B, respectively.

a) Output Stage

The coupled resonators network of Fig. 3 is exploited to implement the output matching network. The parasitic capacitance of the output pad and the large drain capacitance of the PA active stage are conveniently absorbed in C_3 and C_1, respectively. R_3 is the 50Ω antenna resistance while R_1 can be neglected because R_3, together with the pad capacitance, determines a low network $Q \cong 1.2$ at 40GHz, while quality factor at the drain of the output stage devices is ~4 at 40GHz. In principle, delivering a saturated output power of 13dBm with V_{DD}=1V would be feasible even without transforming the load impedance R_L. However, the simulated quality factor of a 100pH inductor realized with the topmost BEOL layer and $10\mu m$ width determines Q_{Ind} of 13 at 60GHz. With a network $Q \cong 1.2$ and a passive quality factor Q_{Ind} of 13, Eq. (4) predicts that using coupled resonators to widen system bandwidth yields a maximum achievable efficiency of ~75%, thus reducing the power effectively delivered to the load R_L. To restore the output power to the desired level, a wideband impedance transformation is then needed. Moreover, a transformer is desirable for differential to single-ended conversion to the output. Finally, to have a symmetric network response (i.e. $m = l$), $C_1 = C_3$ is required, a condition which is not verified in practice, because the pad capacitance is usually smaller than the power device parasitic capacitance.

To address these issues and meet the above targets, a design procedure, starting from the network of Fig. 8a and leading to the equivalent network of Fig. 8d, is proposed. The technique makes use of Norton impedance transformations, which allows input impedance scaling and rearranges circuit topology without changing the order and response of the network itself [6,22]. No approximations are employed through the transformations depicted in Fig. 8. As such, the shape of the transfer function is preserved while absolute value is scaled corresponding to the input impedance level.

The design procedure starts from the coupled resonator network shown in Fig. 8a. If the lower resonance frequency of the network f_L is set to 40GHz, a value of $d = 2.5$ determines f_H of ~74GHz, yielding a fractional bandwidth of ~60%. As discussed in Sec. II, once the value of $d = m + l$ is set, m and l can be chosen to properly pre-emphasize the network response in order to obtain a flat response once implemented with lossy components. From Eq. (5), $m \cong 1.4$ and $l \cong 1.1$ realize a peaking of ~2dB.

As a first step of the transformation, inductor L_2 is split into L_{2a} and L_{2b}, as shown in Fig. 8b. A Norton transformation is performed on inductors L_{2b} and L_3 that become topologically swapped in the network, as in Fig. 8c. An impedance downconversion ratio $n = (L_{2b} + L_3)^2/L_3^2$ is thus achieved [22]. To restore the output power to the desired level, $n \cong 1.7$ and R_L is downconverted to $\sim 40\Omega$, such that each single-ended output of the last stage has $\sim 20\Omega$ load. In this design, a moderate transformation ratio is implemented and the need for a broadband matching network is motivated by the large output transistor parasitic capacitance and the large pad and interconnect parasitics. As a last step, through a Π-network to T-network transformation and transformer model, inductors in the dotted box of Fig. 8c are equivalent to a transformer and series inductor L_{2s} with component values related to L_1, L_{2a}, L_{2b}, L_3 and n [23,24]:

$$L_p = L_s = \frac{L_1(L_{2a} + L_3\sqrt{n})}{(L_1 + L_{2a} + L_3\sqrt{n})n}$$
$$k = \frac{L_3}{L_3 + L_{2a}/\sqrt{n}} \quad (6)$$
$$L_{2s} = \frac{L_{2a}(L_3\sqrt{n} - L_1)}{(L_1 + L_{2a} + L_3\sqrt{n})n} + \frac{L_{2b}}{\sqrt{n}}$$

Fig. 9 shows the real and imaginary part of the synthesized impedance at the input of the network in presence of a limited quality factor of passive components $Q_{Ind} \cong 13$. The network shows a broadband response with an average value of ~40Ω input impedance and variations within 15%. The final matching network consists of a transformer with $L_p = L_s \cong 70pH$, $k \cong 0.7$ in series with inductor $L_{2s} \cong 38pH$. Note that the proposed network lends itself to a compact layout. Also, scaling impedances through Norton transformations raises the input capacitance to nC_1, thus allowing the designer to easily embed the drain parasitic capacitance of the power device.

The layout view of the output matching network is shown in Fig. 10. Being the secondary of the transformer floating, inductor L_{2s} is conveniently implemented with the two traces connecting the output of the transformer to the ground pads. The effectiveness of the proposed design is shown in Fig. 11, where a peak efficiency of 76% is achieved at the center of the band. Transistors of the output stage are 200μm/28nm and biased in class-AB with $V_{bPA} = 400$mV ($g_m/g_{ds} \cong 8.5$ and $f_T \cong 160$GHz). Output stage shows some gain expansion, which is leveraged to partially counteract gain compression of the driver stage, allowing an overall 1dB compression point closer to P_{SAT}.

b) Driver Stage

The GBW enhancement offered by coupled resonators is exploited in the interstage network to scale down the size of the driver transistors, for the target gain and bandwidth, thus reducing power dissipation and improving the overall PA efficiency.

Design of the interstage network starts from the schematic shown in Fig. 12a, derived from the coupled resonator circuit in Fig. 3. The large input capacitance of the PA output stage and the drain capacitance of the driver transistors are absorbed in C_3 and C_1, respectively. Resistor R_1 determines the network quality factor while resistor R_3 can be neglected because the gate capacitance of the output stage displays much higher quality factor ($Q \approx 12$) than the drain capacitance of the driver ($Q \approx 2$). To maintain the same bandwidth of the PA output matching network, the network Q has to be reduced further to 1.25, and an additional resistor R_a is assumed, in parallel with the output resistance of the driver stage r_0, so that $R_1 = r_0 // R_a$. Furthermore, to design the network with $m = l$, the two resonator capacitors must be equal and an additional capacitor C_a is assumed in parallel with the driver output capacitance C_0 so that $C_1 = C_0 + C_a = C_3$.

Norton transformation can be applied to scale up the impedance of the network in Fig. 12a and remove the need for R_a and/or C_0. For a target gain, the width of the driver transistor can be consequently scaled. Similarly to the output stage, inductor L_2 is split into L_{2a} and L_{2b}, as shown in Fig. 12b. The Norton transformation is then performed on inductors L_{2a} and L_1 that get topologically swapped in the network (see Fig. 12c). The transformation scales up the impedances at the driver side by $t = (L_{2a} + L_1)^2 / L_1^2$, which is equal to 1.5^2 in our design. Since the voltage gain V_3/V_1 is $1/\sqrt{t}$, the transistor size scales down by $\sqrt{t}$ to maintain the same gain. In this case, C_1 is completely realized by the parasitic capacitance of the driver transistor, while R_1 accounts for the output conductance of the driver and the loss of the inductors of the network.

The schematic of the final matching network is depicted in Fig. 12d, where the T of inductors is implemented by means of a transformer with $L_p = L_s \cong 200pH$ and $k \cong 0.8$ [23,24]:

$$L_p = L_s = (L_1 + L_{2a})\sqrt{t}$$
$$k = \frac{L_1}{L_1 + L_{2a}} \quad (7)$$
$$L_{2s} = (L_{2b} - L_{2a})\sqrt{t}$$

The layout view of the interstage matching network is shown in Fig. 13. The transformer simplifies the layout and biases the stages. Inductor L_{2s} isolates the two windings of the transformer from inductor L_3, which can be conveniently laid out close to the input of the PA stage. Fig. 14 shows a post-layout simulation of the gain V_3/V_{in} of the cascaded structure of the driver and interstage matching network. Transistors are 40μm/28nm and biased in class-A with $V_{bDR} = 600$mV, yielding a $g_m/g_{ds} \cong 6.5$ and $f_T \cong 210$GHz. A gain of ≈ 8.5 dB is achieved with less than 1dB ripple over a bandwidth from 36 to 78GHz, proving the capabilities of the proposed technique.

Compared to the solution based on L-C resonant tank explored in Sec. II, the proposed interstage matching network allows saving a factor 3 on the driver power consumption, while maintaining the same gain G_d and bandwidth BW_d. A factor of 2x is provided by the GBWEN offered by coupled resonators and a factor of 1.5x is gained through a Norton transformation.

At the input, a 2-section ladder network similar to [25] is adopted to achieve wideband matching. Additionally, a combination of series inductor and inductive degeneration is proposed. Coupling the inductors reduces the size of the degeneration inductor that can be conveniently laid out inside the series inductor to minimize the layout parasitics and losses.

V – Measured Results

A prototype of the PA has been fabricated by STMicroelectronics. Fig. 15 shows the die microphotograph of the chip. It occupies a total area of 620x540 μm^2 including pads with a core

area of 470x120 μm^2. The measurements are performed on a high-frequency probe station where the single-ended RF input and output pads are directly accessed by GSG probes. The DC signal pads are wire-bonded to a PCB. The supply voltage is 1V.

The small-signal measurements and simulations are shown in Fig. 16. The PA achieves a peak gain of 13dB with a 3dB bandwidth of 27GHz extending from 40GHz to 67GHz. Fig. 17 shows the measured group delay, which has less than ±4ps variations for frequencies higher than 46GHz. Along with the S21 measurement, it confirms the validity of the proposed interstage and output matching network design techniques for wideband operation. Fig. 18 shows the measured K stability factor of the PA. It is much greater than unity for all frequencies, thereby providing the necessary condition for the unconditional stability of the amplifier.

Fig. 19 shows the measured gain, output power and power added efficiency (PAE) of the PA at 50GHz. The PA achieves a saturated output power (P_{SAT}) of 13dBm with a peak PAE of 16%. The measured P_{-1dB} at 50GHz is 12dBm. Fig. 20 shows the measured gain, output power and PAE as a function of frequency to assess the wideband behavior of the realized prototype. Uniform P_{SAT} and P_{-1dB} are achieved over all the operation bandwidth. The linearity of the PA is also characterized by the S-parameter measurement with a power sweep. AM-PM distortion test measurement results are reported in Fig. 21. At 1dB compression point (i.e. P_{IN}=-1dBm), the maximum AM-PM distortion is 2.6 degrees.

Gain flatness and -1dB bandwidth are critical parameters in high-speed communication systems. The presented PA shows a measured P_{SAT} and P_{-1dB} -1dB bandwidth ranging from 46GHz to 62GHz: in this frequency range S21 variation is within +/-0.6dB. In the 57-66GHz unlicensed band, S21 and P_{SAT} show +/-0.75dB and +/-0.5dB variations, respectively, demonstrating the ability of the presented PA toward high-speed communication systems.

For long-term reliability, the effects of RF stress on the PA, particularly critical in ultra-scaled CMOS technologies, were measured for a period of 10 hours. The saturated output power (P_{SAT}) degrades by 0.3dB and the power added efficiency (PAE) drops from 16% to 14%.

Table I shows a comparison of state-of-the-art mm-wave CMOS PAs published so far in the literature. The proposed PA shows the highest fractional bandwidth and PAE among bulk CMOS PAs, still achieving P_{SAT} comparable to other PAs. The effectiveness of the proposed technique is proven by the large achieved GBW, comparable to [26], [12] and [27], where however a higher power supply is employed. In [12], a higher fractional bandwidth is achieved thanks to the SOI technology, but the PA shows a lower PAE despite the use of a 2.2V supply. In [20, 16], a higher output power is achieved with the aim of power combining technique. Nevertheless, both works show a smaller fractional bandwidth and lower GBW. [20] shows an outstanding PAE, most likely due to high quality factor of passive components.

VI – Conclusions

In this paper, a design methodology for ultra wideband interstage and output matching networks has been proposed. Inductively coupled resonators are investigated as a mean to achieve large gain-bandwidth product enhancements while keeping high efficiency. Norton transformations are then applied for impedance scaling, while topological transformations are employed to include a transformer, to achieve the desired load impedance and to minimize the number of components. Applied to the design of a two-stage power amplifier, the proposed network design technique leads to a two-stage differential PA with neutralized common source stages. The PA delivers 13dBm saturated output power over the 40-67GHz bandwidth with a peak power-added efficiency of 16% without power combining. The fabricated chip demonstrates state-of-the-art performances and the widest reported fractional bandwidth among bulk CMOS PAs.

Appendix

Referring to Fig. 3, this Appendix derives equations for gain, poles' position, ripple, efficiency and GBWEN as a function of component values for the inductively coupled resonators in the case of asymmetric filter termination. That is, in the following analysis resistor R_1 is neglected, but, due to network reciprocity, the same result holds in case R_3 is neglected.

A two-port passive network, can be characterized by the admittance matrix:

$$[Y] = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}. \tag{A1}$$

The transimpedance gain $T(s = j\omega)$ of the circuit of Fig. 3 can be calculated as [23]

$$T(j\omega) = \frac{V_{OUT}}{I_{IN}} = \frac{y_{21}}{y_{11}y_{22} - y_{12}y_{21}}. \tag{A2}$$

By inspection, the following expressions for the admittances are derived:

$$y_{11} = j\frac{\sqrt{1+m}}{\omega_0 m L_1}\left(\frac{\omega}{\omega_0\sqrt{1+m}} - \frac{\omega_0\sqrt{1+m}}{\omega}\right),$$

$$y_{22} = \frac{1}{R_3}\left(1 + jQ\sqrt{1+l}\left(\frac{\omega}{\omega_0\sqrt{1+l}} - \frac{\omega_0\sqrt{1+l}}{\omega}\right)\right),$$

$$y_{21} = y_{12} = \frac{j}{\omega L_2}, \tag{A3}$$

where $\omega_0 = 1/\sqrt{L_1C_1} = 1/\sqrt{L_3C_3}$, $m = L_1/L_2$, $l = L_3/L_2$ and $Q = \omega_0 R_3 C_3$. For values of Q high enough, numerator and denominator of $T(j\omega) = N(j\omega)/D(j\omega)$ can be approximated as

$$N(j\omega) = j\frac{\omega R_3}{\omega_0 Q}\frac{m}{1+d},$$

$$D(j\omega) \cong \left(1 + \frac{j\omega}{\omega_L Q_1} - \frac{\omega^2}{\omega_L^2}\right)\left(1 + \frac{j\omega}{\omega_H Q_2} - \frac{\omega^2}{\omega_H^2}\right), \tag{A4}$$

where $d = m + l$, $\omega_L = \omega_0$, $\omega_H = \omega_0\sqrt{1+d}$ are the resonant frequencies of the two biquadratic terms and

$$Q_1 = \frac{d}{m}Q, \qquad Q_2 = \frac{d\sqrt{1+d}}{d-m}Q. \tag{A5}$$

By evaluating T($j\omega$) at the two resonant frequencies, an approximate expression for the peaking can be derived as

$$\left|\frac{T(j\omega_H)}{T(j\omega_L)}\right| \cong \frac{m}{d-m}. \quad (A6)$$

The input impedance $Z_{in}(j\omega)$ of the circuit of Fig. 3 can be calculated as [23]

$$Z_{in}(j\omega) = T(j\omega)\frac{1+d-m}{d-m}\left(1+\frac{j\omega}{\omega_M Q_3}-\frac{\omega^2}{\omega_M^2}\right), \quad (A7)$$

where $\omega_M = \omega_0\sqrt{1+d-m}$ and $Q_3 = Q\sqrt{1+d-m}$.

Efficiency of the network is derived referring to Fig. A1(a), where resistances R_{1p}, R_{2p} and R_{3p} represent the losses introduced by the limited quality factor of inductors L_1, L_2 and L_3, respectively. At $\omega = \omega_0$, the circuit in Fig. A1(a) can be conveniently reduced to the one in Fig. A1(b). Therefore, the efficiency can be calculated as

$$\eta \approx \frac{P_{R_L}}{P_{R_L}+P_{R_{1p}}+P_{R_{2p}}+P_{R_{3p}}} \approx \frac{1}{1+\frac{1}{Q_{Ind}Q}\left(\frac{1}{l}+\frac{l}{m}Q+\frac{1}{lm}\right)}\frac{Q_{Ind}}{Q_{Ind}+Q}, \quad (A8)$$

where $Q_{Ind} = L_1\omega_0/R_{1p} = L_2\omega_0/R_{2p} = L_3\omega_0/R_{3p}$.

In the case $m = l$ and frequencies of operation close to the center frequency $\omega_0\sqrt{1+m}$, $T(j\omega)$ can be approximated to $T'(j\omega) = y_{21}/(y'_{11}y'_{22}-y_{12}y_{21})$, where:

$$y'_{11} \cong j\frac{\sqrt{1+m}}{\omega_0 m L_2}2\left(\frac{\omega-\omega_0\sqrt{1+m}}{\omega_0}\right),$$

$$y'_{22} \cong \frac{1}{R_3}\left(1+j2Q\sqrt{1+m}\left(\frac{\omega-\omega_0\sqrt{1+m}}{\omega_0\sqrt{1+m}}\right)\right). \quad (A9)$$

The gain magnitude $|T'(j\omega)|$ shows a minimum $|T'_{MIN}(j\omega)|$ at $\omega_{MIN} = \omega_0\sqrt{1+m}$ and two maxima $|T'_{MAX}(j\omega)|$ at frequencies symmetric with respect to ω_{MIN}. The in-band ripple R can be calculated as the ratio of $|T'_{MAX}(j\omega)|$ and $|T'_{MIN}(j\omega)|$:

$$R = \frac{2(mQ)^2}{\sqrt{(1+m)(4m^2Q^2-m-1)}}. \quad (A10)$$

As expected, the in-band ripple depends on $m = l$ (and hence L_2) and Q and increases with increasing values of m (i.e. ripple increases with bandwidth). The value of m that sets the in-band ripple to 0dB is $m_{0dB} = \left(1+\sqrt{1+8Q^2}\right)/(2Q)^2$.

In the case of 0dB ripple, substitution of m_{0dB} in $|T'(j\omega)|$ and $|T'_{MAX}(j\omega)|$ yields the maximum gain $|T'_{MAX,m0dB}(j\omega)|$ and 3dB fractional bandwidth BW_{m0dB}

$$|T'_{MAX,m0dB}(j\omega)| = \sqrt{2}R_3, \qquad BW_{m0dB} = \left(\sqrt{2}Q\sqrt{1+m_{0dB}}\right)^{-1}. \quad (A11)$$

By simply resonating capacitances $(C_1 + C_3)$ with a single inductor at frequency $\omega_0\sqrt{1+m_{0dB}}$, the achieved gain $|G_{LC}(j\omega)|$ and 3dB fractional bandwidth BW_{LC} are

$$|G_{LC}(j\omega)| = R_3, \qquad BW_{LC} = \left((1+C_1/C_3)Q\sqrt{1+m_{0dB}}\right)^{-1}. \quad (A12)$$

By comparing (A11) to (A12), coupled resonators offer an improvement of the gain-bandwidth product of $(1 + C_1/C_3)$, which is equal to 2 due to the $m = l$ assumption. Following the same procedure for a 3dB in-band ripple case, GBWEN further increase by a factor $\alpha(R) \approx 1.55$, yielding a maximum GBWEN for coupled resonators of ~3.

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LIST OF FIGURES

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