A 106-dB A-Weighted *DR* Low-Power Continuous-Time ΣΔ Modulator for MEMS Microphones

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Abstract

This paper presents a low-power, high-performance continuous-time ΣΔ modulator for MEMS microphones front-end. The ΣΔ modulator 3rd-order loop filter has been implemented with a low-noise, power-optimized active-RC architecture that uses only two operational amplifiers. This solution, along with the use of a 15-level quantizer and of a feedback DAC with three-level current-steering elements, which minimizes the noise contribution for small input signals, allows achieving a *DR* larger than 100 dB, while consuming less than 0.5 mW, as required in always-running audio modules for portable devices. The proposed ΣΔ modulator, realized in 0.16-μm CMOS technology with an area of 0.21 mm^2, achieves 106-dB A-weighted *DR* and 91.3-dB peak *SNDR*, consuming 390 μW from a 1.6-V power supply.

Index Terms

ΣΔ Modulator, MEMS Microphone, A/D Converter, Audio Converter, Continuous-Time.

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I. Introduction

Nowadays, voice recognition technologies are becoming integral part of products and services in several application fields. Sophisticated voice interfaces are already commonplace in call centers and the rapid rise of powerful mobile devices is making voice interfaces even more useful and pervasive. A growing number of people now talk to their mobile devices, asking them to send e-mails and text messages, to search for directions, or to find information on the internet. Furthermore, as a next step in the direction of offering a completely hand-free experience, such devices would require continuous listening. Therefore, the input audio modules (i. e. the microphones) must be always active. For this reason, the interface circuits, required for digitizing the microphone capacitance variation, have to feature extremely low power consumption ($<$ 1 mW for the full channel), while maintaining the HiFi audio performance ($DR > 100$ dB A-weighted, $THD < 0.01\%$), required for advanced audio signal processing.

The last stage of digital microphone interface circuits is typically a $\Sigma\Delta$ Modulator ($\Sigma\Delta$M) that exploits oversampling to achieve the required Dynamic Range (*DR*). These $\Sigma\Delta$Ms are often realized with Switched-Capacitor (SC) techniques [1], at the cost of larger power consumption with respect to Continuous-Time (CT) $\Sigma\Delta$Ms, which require operational amplifiers (opamps) with lower bandwidth. The CT-$\Sigma\Delta$M advantage over SC-$\Sigma\Delta$Ms in terms of power consumption is, however, achieved at the expense of performance robustness, due to the higher sensitivity of CT-$\Sigma\Delta$M to some implementation aspects (such as opamp slew-rate, jitter, spikes, etc.) [2], thus preventing their use in portable devices. Therefore, aggressive design solutions have to be developed to achieve the target performance with low-power CT-$\Sigma\Delta$Ms.

In this scenario, this paper focuses on the implementation of a CT-$\Sigma\Delta$M able to achieve a *DR* larger than 100 dB A-weighted with a power consumption lower than 500 μW, by exploiting several low-power techniques, such as feedforward CT-$\Sigma\Delta$M architecture, multi-bit quantizer, DAC with three-level current-steering elements, and a 3rd-order loop filter that requires only two opamps, instead of three or four as in conventional solutions.

The paper is organized as follows. Section II describes the 3rd-order CT-ΣΔM architecture, focusing on the loop-filter structure, the excess loop delay compensation, and the multi-bit topology. The actual implementation of the different building blocks of the CT-ΣΔM is described in detail in Section III. Finally, Section IV reports the achieved measurement results, while Section V draws same conclusions.

II. Architecture

A. Loop Filter Architecture

The two main architectures for implementing a 3rd-order ΣΔM are the Cascade-of-Integrators in Feed-Back (CIFB) topology and the Cascade-of-Integrators in FeedForward (CIFF) topology. The CIFF architecture is popular in the literature [3], since it features a reduced integrator output swing and, hence, typically requires lower power consumption and area with respect to the CIFB topology.

In addition, high-*DR* ΣΔMs are usually designed with optimized placement of the noise transfer function (NTF) zeros. Complex conjugate poles in the loop filter (corresponding to the NTF zeros) are placed close to the upper edge of the band, in order to lower the quantization noise in this region. These loop-filter complex poles are implemented with a resonator obtained by adding a local feedback around the last two integrators of the ΣΔM, as shown in Fig. 1a, leading to the transfer function

$$H_{loop}(s) = \frac{a_1 s^2 T_s^2 + a_2 s T_s + a_1 g_1 + a_3}{s T_s (s^2 T_s^2 + g_1)}. \quad (1)$$

The same NTF can be obtained with the loop-filter structure depicted in Fig. 1b, where resonator and integrator are swapped. In this case, the resonator features a single output, which is crucial to implement it with a single-opamp structure, thus reducing area and power consumption [4], [5]. The resonator transfer function, given by

$$H_{res}(s) = \frac{a_1 s T_s + a_2}{s^2 T_s^2 + g_1}, \quad (2)$$

has two complex conjugate poles at ω_0, a zero at ω_z, and a DC gain G_{DC}, given by

$$\omega_0 = \frac{\sqrt{g_1}}{T_s} \quad \omega_z = \frac{a_2}{a_1 T_s} \quad G_{DC} = \frac{a_2}{g_1}. \tag{3}$$

The transfer function from the output of the resonator to the output of the loop filter is then

$$H_b(s) = \frac{sT_s + a_3/a_2}{sT_s}. \tag{4}$$

This allows the loop filter transfer function given by (1) to be exactly synthesized.

Finally, the structure of Fig. 1b can be further modified to achieve the structure of Fig. 1c, without affecting the overall transfer function. The final adder is moved in front of the integrator, thus preventing the use of an active (power hungry) or passive (inaccurate) adder at the output of the loop filter. The feedforward path is differentiated before adding it at the input of the integrator. This power-efficient solution can be implemented only if the resonator is moved at the input of the loop filter.

B. Excess-Loop-Delay Compensation

In a CT-ΣΔM, the time required for the multi-bit quantizer and the feedback DAC operation strongly affects the overall performance. This time, called Excess-Loop-Delay (ELD) and indicated with τ_d, depends on several design and implementation parameters, and can spread significantly in the presence of process, voltage, and temperature (PVT) variations. A small ELD variation, if not properly handled, could dramatically worsen the CT-ΣΔM performance. Specific solutions are required to minimize these ELD variation effects.

In the solution shown in Fig. 2a, a fixed and well-known amount of time, typically $T_s/2$ or T_s, is allocated for the quantizer and DAC operations, by placing a D-flip-flop in front of the feedback DAC. This arrangement makes the ELD value constant and independent of PVT variations. This fixed ELD value is compensated [6] by adding a feedforward path a_{0c}, which processes the difference between the input and the feedback DAC signals. This difference, however, is not easily accessible. Therefore, this

structure has to be modified, leading to the scheme shown in Fig. 2b, where the feedforward path a_{0c} is split in path a_{0c1}, which processes the input signal, and path a_{0c2}, which processes the feedback DAC signal, both easily accessible.

In the CT-ΣΔM coefficient sizing, the allocated and well-known ELD value has then to be taken into account to achieve the desired NTF. For the adopted 3rd-order ΣΔM topology, the coefficients a_{1c}, a_{2c}, and a_{3c}, as well as the additional coefficients a_{0c1} and a_{0c2}, introduced for ELD compensation, become

$$\begin{cases} a_{0c1} = a_{0c2} = a_1\tau_d + a_2\dfrac{\tau_d^2}{2} + a_2\dfrac{\tau_d^6}{6} \\ a_{1c} = a_1 + a_2\tau_d + a_2\dfrac{\tau_d^2}{2} \\ a_{2c} = a_2 + a_3\tau_d \\ a_{3c} = a_3 - a_1 g_1 \end{cases} . \tag{5}$$

As a further optimization, the same technique used in Fig. 1c for handling the original ΣΔM feedforward paths is adopted for the ELD compensation feedforward (a_{0c1}) and feedback (a_{0c2}) paths, which are not connected in front of the quantizer, but in front of the preceding integrator, thus avoiding an additional adder. In this case, paths a_{0c1} and a_{0c2} have to be differentiated to compensate for the integrator transfer function. The resulting CT-ΣΔM architecture, to be realized with active-RC structures, is shown in Fig. 3.

C. Multi-Bit CT-ΣΔM Architecture

The use of a multi-bit quantizer in a CT-ΣΔM is highly beneficial both for improving the performance and reducing the power consumption. This is because the quantization noise is lower than in a single-bit ΣΔM and, therefore, a lower slew-rate is required in the opamps of the loop filter, which directly translates into a power consumption reduction. Moreover, the same *DR* is achieved with a lower oversampling ratio (and hence opamp smaller bandwidth and lower power). Finally, multi-bit CT-ΣΔM are less sensitive to the clock jitter in the feedback DAC.

In the proposed CT-ΣΔM, a good trade-off between the benefits offered by a multi-bit quantizer and the exponential increase of the implementation complexity is offered by a 15-level quantizer. The main

$\Sigma\Delta$M feedback loop is then closed with a 15-level DAC, realized with three-level current-steering unitary elements, while a 15-level SC feedback DAC is used for implementing the local feedback path for ELD compensation. The use of a current-steering DAC in the main $\Sigma\Delta$M feedback path eliminates the need for accurate reference voltages, thus saving a significant amount of power and avoiding additional external components (e. g. filtering capacitors [3]), that would increase the board bill-of-material. Moreover, current-steering DACs are much less sensitive than resistor-based topologies to fluctuations of the opamp virtual ground [7], which would lead to distortion.

The proposed CT-$\Sigma\Delta$M has been designed for the audio (20 kHz) signal bandwidth with an oversampling ratio of 75. The target *DR* in nominal conditions is 106 dB A-weighted, which is in excess of the 100-dB audio applications specification. The safe margin is to accomodate DR performance loss due to implementation issues. In fact, the adopted active-RC CT implementation suffers from parameter deviations due to PVT variations (resistor and capacitor deviations result in time constant variations up to 30% of the nominal value), which could reduce the actual *DR*. In this design, the loop-filter transfer function has been optimized to guarantee stability even in the presence of PVT variations and without the implementation of a power-and-area hungry tuning circuit to control the time constants. In a Montecarlo analysis with 500 simulations, the A-weighted *DR* evaluated for a -60-dB$_{FS}$, 1-kHz input signal, considering a time constant variation of $\pm 30\%$, is shown in Fig. 4. For any sample, the achieved A-weighted *DR* is larger than 103 dB, satisfying the application request.

III. Circuit Design

A. Loop Filter

The loop filter used in the proposed CT-$\Sigma\Delta$M is implemented with active-RC structures (to achieve the target linearity) and with only two opamps. The first one is used to realize the resonator, while the second one is used to implement the integrator and the adder in front of the quantizer.

The single-opamp resonator, originally introduced in [5], is proven on silicon for the first time for audio application in the proposed CT-$\Sigma\Delta$M. In order to achieve the desired transfer function $H_{res}(s)$, the opamp

feedback, originally realized with a complex cross-coupled network, has been simplified to just an RC cross-coupled path (C_1-C_2 and R_1-R_3), as shown in Fig. 7. According to [5], if the component values are designed such that

$$\frac{C_1}{R_3} + \frac{C_2}{R_3} + \frac{C_3}{R_1} = 0, \tag{6}$$

then $H_{res}(s)$ features $\omega_0 = 1/\sqrt{R_1 R_3 C_1 C_2}$, $\omega_z = 1/(R_3 C_2)$, and $G_{DC} = R_1/R_i$.

Assuming that the value of R_i is bounded by thermal noise constraints, the resulting component values are

$$\begin{cases} R_1 = G_{DC} R_i = \dfrac{a_{2c}}{g_1} R_i \\ R_3 = \dfrac{R_1}{(\omega_z/\omega_0)^2 + 1} = \dfrac{R_1}{a_{2c}^2/\left(a_{1c}^2 g_1\right) + 1} \\ C_2 = \dfrac{1}{\omega_z R_3} = \dfrac{T_s a_{1c}}{a_{2c} R_3} \\ C_1 = C_2 \dfrac{R_1 - R_3}{R_1} \end{cases}. \tag{7}$$

On the other hand, the integrator implements the transfer function $H_b(s)$ that achieves 0-dB gain at frequency $\omega_i = a_{3c}/(a_{2c} T_s) = 1/(R_4 C_4)$. The need for an additional summing amplifier is avoided by using capacitive feedforward branches (C_f) directly connected to the summing node of the final integrator [8], thus implementing a straight gain coefficient. The feedforward gain is the ratio C_f/C_4. The transfer function of the integrator/adder is then

$$H_b(s) = \frac{1 + sR_4 C_f}{sR_4 C_4}. \tag{8}$$

The complete schematic of the proposed loop filter is obtained by cascading the single-opamp resonator and the final integrator/adder, as shown in Fig. 7.

B. Passive Components

The proposed CT-ΣΔM is implemented in a 0.16-μm CMOS process with 5 metal layers, MIM capacitors (2 pF/μm^2), and polysilicon resistors (0.33 kΩ/μm^2). The MIM capacitors are realized with the top

metal layers (metal 4 and metal 5), while the resistors require only metal 1 for contacting the polysilicon. In the layout it is, therefore, possible to place the capacitors on top of the resistors to save area. With this approach, the overall area is optimized if resistors and capacitors have approximately the same size. To achieve this goal and considering that input resistors R_i are designed as low as 47 kΩ to fulfill the thermal noise requirements (Section III-F), the ΣΔM coefficients must be scaled with respect to the values given by (7), in order to reduce the total resistance and increase the total capacitance.

The coefficient scaling can be achieved dividing by a factor K the transfer function of the resonator and multiplying by the same factor the transfer function of the integrator/adder, according to

$$H_{loop}(s) = \left[\frac{1}{K} \cdot H_{res}(s)\right] [KH_b(s)]\,. \tag{9}$$

For increasing the total capacitance and decreasing the total resistance, K must be larger than 1.

Choosing $K > 1$ leads also to further benefits. Indeed, in the resonator, the peak gain value at ω_0 is determined by the open-loop gain of the opamp at this frequency $A(\omega_0)$, since the feedback loop at ω_0 is basically open. As a result, the resonator Q factor is limited by $A(\omega_0)$ and by the resonator gain G_{DC}, as illustrated in Fig. 5a. The resonator Q factor can be increased by either increasing the open-loop gain of the opamp at ω_0 (i. e. increasing the opamp bandwidth), at the expense of a larger power consumption, or decreasing the resonator gain G_{DC}, or, rather, increasing K, as shown in Fig. 5a. The main advantage of achieving a higher resonator Q factor is the improvement of the ΣΔM NTF at the edge of the audio band, as shown in Fig. 5b.

Another benefit of selecting $K > 1$ is the reduction of the resonator output swing, as shown in Fig. 6. The 1-kHz, full-scale (1 V_{rms}) differential input signal is shown in Fig. 6a, while the corresponding loop-filter output signal (i. e. the quantizer input signal) is shown in Fig. 6b. The differential resonator output signals obtained with the original and the scaled coefficient values are shown in Fig. 6c and Fig. 6d, respectively. As expected, with the scaled coefficients, the voltage swing at the output of the resonator is attenuated by K. A good trade-off among area, resonator Q factor, and resonator output swing is obtained

for $K = 2$. The scaled passive component values are summarized in Tab. I.

C. Operational Amplifiers

The opamp used in the resonator (OA_1) is realized using a two-stage Miller topology, which features relatively low output impedance, as required for achieving the desired resonator transfer function [9]. In fact, the RC cross-coupled feedback network of the resonator works properly only assuming an opamp output impedance sufficiently low, thus preventing the use of other opamp topologies (e. g. folded cascode) with higher output impedance. The resonator Q-factor depends on the opamp open-loop gain at the resonance frequency (ω_0). Although this gain needs to be larger compared to a conventional implementation (i. e. simple integrator as first stage of the $\Sigma\Delta$M), in order to guarantee a Q-factor large enough, the extra amount of gain is provided at no cost by the increased value of the input pair transconductance, required to fulfill thermal noise constraints (Section III-F). These concepts, in conjunction with the low output voltage swing guaranteed by the feedforward architecture, further halved by choosing $K = 2$, allows the opamp to be designed focusing on the optimization of the frequency response and not of the output swing or the current driving capability, thus saving power.

The circuit schematic of OA_1 is shown in Fig. 8. The input differential pair (M_1-M_1') is realized with p-channel transistors with long channel to lower the $1/f$ noise. Transistor M_3 sets the bias current of the input differential pair to 20 μA, thus achieving a transconductance value which fulfills the thermal noise constraints. The class-A second stage (M_4-M_4') ensures a constant and relatively low output impedance. The opamp is compensated with R_z and C_m.

The common-mode feedback (CMFB) circuit of OA_1, is shown in Fig. 9. The quiescent output voltage at nodes V_{1p} and V_{1m} in Fig. 8 (which is also the gate-source voltage of M_4-M_4') sets the bias current of the second stage. To set this current accurately, the CMFB circuit regulates voltage V_{cmfb}. The reference voltage V_{cm} is the desired output common-mode voltage of the opamp, equal to $V_{DD}/2$. Due to the low voltage swing at nodes V_{om} and V_{op}, the linearity of the common-mode voltage detector is not critical. The

quiescent current through each output branch of the opamp (M_4 and M_4') is 14 μA. The total bias current of OA_1, including the CMFB circuit, is 50 μA, with a DC gain of 78 dB and a *UGB* of 18 MHz.

The integrator/adder opamp (OA_2) is also based on a two-stage topology, since it has to sustain the full-scale voltage swing (1.4 V) present at the input of the multi-bit quantizer. The circuit schematic of the opamp is shown in Fig. 10. The input differential pair, in this case, is much smaller than in OA_1, since the noise contributions of OA_2 are negligible when referred to the loop-filter input. For the same reason, the bias current of the input differential pair can be as low as 4 μA, since it is necessary to fulfill only the bandwidth requirement.

Since the output voltage swing of OA_2 is large, linear operation of the CMFB circuit is ensured by using resistive averaging to detect the output common-mode voltage, as shown in Fig. 11a. Capacitors C_p = 250 fF provide a high-frequency path, bypassing the resistive common-mode detector and the error amplifier [3], thus improving stability. In OA_2 the bias currents of transistors M_4 and M_4' are 1.5 times larger than the bias currents of transistors M_5 and M_5'. The bias current difference is provided by the CMFB circuit, which regulates the gate voltage of M_6 and M_6' (V_{cmfb1}). This solution, reducing the loop gain, ensures stability and reliable operation of the CMFB loop. The bias current in each output branch of OA_2 (M_4 and M_4') is 12 μA. A second CMFB circuit is necessary to adjust the common-mode voltage at nodes V_{1p} and V_{1m} and, hence, the bias current in M_4 and M_4', as shown in Fig. 11b. Resistive averaging is used again to detect the common-mode voltage and, through an error amplifier, adjust voltage V_{cmfb2}, to ensure that $\left(V_{1p} + V_{1m}\right)/2 = V_{ref}$. To control the bias current of M_2 and M_2' accurately, the reference voltage V_{ref} is derived from a diode-connected transistor biased with a fixed current. The total bias current of OA_2, including both CMFB circuits, is 30 μA, with a DC gain of 60 dB and a *UGB* of 9 MHz.

D. Quantizer

The 15-level quantizer used in the proposed CT-ΣΔM is illustrated in Fig. 12. It is a flash ADC realized with 14 identical differential comparators and a resistive divider from the analog power supply for generating the threshold voltages.

The circuit schematic of the comparator and the corresponding clock waveforms are shown in Fig. 13. The input voltage of the quantizer ranges between 0.1 V and 1.5 V. Therefore, the nominal quantization step is 93.3 mV, relaxing the offset requirements of the comparators. During clock phase ph_1 the threshold voltages are connected to one plate of capacitors C_{inp} and C_{inm}, while voltage $V_{DD}/2$ is applied to the other plate, which is also connected to V_{c_p} and V_{c_m}. During clock phase ph_2 the quantizer input signals (i. e. the output signals of the loop filter) are connected to C_{inp} and C_{inm}, thus actually obtaining at nodes V_{c_p} and V_{c_n} the difference between the threshold voltages and the input signals. The actual comparator core consists of a differential pair (M_1 and M_2) with a latch (M_3, M_4, M_5 and M_6) as active load. The differential pair is biased with a constant current (provided by M_7), avoiding large dynamic current consumption during the comparison time. The comparator decision takes place during clock phase ph_2, while during $\overline{ph_2}$ the comparator is reset. A SR flip-flop holds the comparator output during the reset phase and guarantees the required output driving capability.

A problem that can occur in a latched comparator is metastability. Indeed, the latch has to produce a valid logic level within half of the clock period ($T_s/2$) after reset. When the input voltages are very close to each other, the time required for achieving a valid logic level increases, potentially exceeding $T_s/2$ and, hence, resulting in a metastable condition. The metastability error can adversely affect the accuracy of the comparator and, therefore, of the quantizer. The probability of metastability is inversely proportional to the equivalent comparator gain at $T_s/2$. The latch regeneration time as a function of the comparator bias current is shown in Fig. 14. In order to achieve a sufficiently low probability of metastability, even in the presence of PVT, the hold time before reset should be kept larger than 80 ns. For this reason, for each comparator a bias current of 2.8 μA has been chosen, thus reducing the latch regeneration time and, hence, increasing the equivalent gain. The static bias current of the whole 15-level quantizer is, hence, 40 μA.

E. Feedback DACs

A simplified schematic of the 15-level current-steering DAC, used for closing the main ΣΔM feedback loop, is shown in Fig. 7. Each three-level current-steering element injects into the virtual ground of the resonator a current either equal to $+I/7$, 0 or $-I/7$, depending on the control bits $p[i]$, $n[i]$, and $z[i]$. Although 7 identical three-level elements are sufficient to achieve 15 levels, 8 elements are actually used because of the requirements of the Dynamic Element Matching (DEM) circuit. With this solution, for low input signals (< -17 dB_{FS}), only one DAC element is used and the DAC injects minimum noise current, maximizing the *SNR* and, hence, the *DR*. By contrast, for large input signals (> -17 dB_{FS}), several DAC elements are used, increasing the DAC noise contribution, which becomes dominant, limiting the peak *SNR*.

In order to improve the ΣΔM linearity in the presence of mismatches in the DAC current-steering elements, a 1st-order DEM technique specific for three-level DAC elements has been used. In the DEM circuit, a data shuffler cell shapes the mismatch error in each pair of three-level elements [10]. The input and output signals of each shuffler cell consist of a pair of signed-thermometer-coded bits (i. e. "10" for +1, "00" for 0, and "01" for -1). All these cells are then connected in a butterfly network to form a 16-bit signed-thermometer-coded data shuffler, as shown in Fig. 16. The input signal of the data shuffler is derived from the 14-bit unsigned-thermometer-coded output word of the quantizer. The outputs of the data shufflers are the control bits *dem_p*[*i*] and *dem_n*[*i*] for the DAC elements, while the remaining control bit *dem_z*[*i*] is generated from *dem_p*[*i*] and *dem_n*[*i*] with a NOR logic gate.

The amount of mismatch among the DAC elements is a critical aspect to be considered in order to achieve a $DR > 100dB$ dB A-weighted. From the statistical analysis shown in Fig. 17, it turns out that for achieving the target *DR*, the mismatch value has to be lower than 0.3%. This can be achieved by increasing the area of the current sources, with the additional benefit of lowering their flicker noise as well.

In the design of the current-steering DAC, the input-referred offset of OA_1 is particularly critical [10].

Indeed, this offset voltage changes the drain voltage of the current sources in the DAC depending on the input signal, thus leading to a nonlinear DAC transfer characteristic (i. e. it results in a dynamic mismatch). In order to alleviate this problem, cascode current sources have to be used for implementing the DAC elements [10].

The circuit diagram of a single three-level DAC element is shown Fig. 18. Both the *p*-channel (M_3) and *n*-channel (M_1) current sources have the same channel length (20 μm), and channel width equal to 9.4 μm and 5.4 μm, respectively. The large channel length used reduces the flicker noise and decreases the transconductance (g_m) of the transistors, thus lowering the thermal noise too. The current generated by M_1 and M_3 is I_{unit} = 2.1 μA. Transistors M_2 and M_4 implement a high-compliance cascode structure. The switches SW_1-SW_6 are realized with minimum size transistors to reduce the capacitive load for the control bits, thus allowing a fast transition from one state to another. The amount of mismatch among the DAC elements turns out to be 0.22% (lower than the required 0.3%), thus ensuring that the in-band shaped mismatch error is not be the limiting factor of the *DR*.

The DAC current sources are biased with a reference current *I*, obtained as the ratio between the main ΣΔM reference voltage and a resistor matched with R_i, in order to guarantee a unity ΣΔM gain even in the presence of PVT variations. The static current consumption of the complete DAC is 70 μA.

The technique proposed in [10] to remove the Inter-Symbol Interference (ISI) in the DAC cannot be implemented in this case because the conversion of the current-steering DAC output into a voltage actually takes place in the resonator. Therefore, to alleviate the problems related to ISI, a latch is placed in each control bit path, as shown in Fig. 19. The path becomes transparent during the time interval *T* following the falling edge of the sampling clock (f_s). In this way a fixed amount of delay is allocated in the feedback loop, as required for ELD compensation [9]. When the latches are transparent, they are driven by identical inverters, to make the rise and the fall times of the control bits equal. In the layout, the latches have been placed close to the corresponding DAC elements, minimizing the mismatches among the metal lines carrying the control bits to the switches of the DAC elements, thus limiting the ISI impact.

Moreover, the timing requirements of the combinational logic in front of the latches are relaxed, since almost half period of the sampling clock is available to set the output values, thus saving power.

The local feedback path for ELD compensation is implemented with the 15-level SC-DAC shown in Fig. 20, which is directly coupled to the virtual ground of opamp OA_2. The DAC switches are controlled with the thermometer code generated by the quantizer, suitably delayed as required for ELD compensation. The total charge injected into the virtual ground is, hence, proportional to the thermometer code and the resulting feedback gain ratio is C_{tot}/C_4, where $C_{tot} = 14C_{dac}$. Each DAC element switches only when the corresponding thermometer-code bit changes and, therefore, only few elements are switching in each clock cycle. Moreover, since all the possible DAC non-idealities are attenuated by the loop-filter gain, the supply voltages can be used as references for the DAC. For the same reason, a DEM circuit is not required. Therefore, the local feedback DAC requires a negligible amount of power and area compared to the main feedback DAC.

F. Noise Analysis

Since the resonator is used as input stage of the loop filter, its input-referred noise determines the performance of the entire CT-$\Sigma\Delta$M. Therefore, it is very important to evaluate its noise contributions in the audio band. One of the main noise contributions is introduced by the input resistors R_i, whose noise is entirely added to the input signal. Considering the fully-differential implementation, the input-referred RMS noise of R_i in the audio band B is given by

$$v_{ni,R_i} = \sqrt{8kTR_iB}. \tag{10}$$

Another relevant noise contribution is introduced by the resonator opamp. This contribution is referred to the the loop-filter input with a transfer function which, in the audio band, is approximately given by

$$H_{ni,OA_1}(s) \approx \frac{1 + R_1/R_i}{R_1/R_1} = 1 + \frac{R_i}{R_1}. \tag{11}$$

Since, according to (7), $G_{DC} \gg 1$, $R_1 \gg R_i$ and, hence, $H_{ni,OA_1}(s) \approx 1$, leading to $v_{ni,OA_1} \approx v_{n,OA_1}$, where v_{n,OA_1} denotes the RMS opamp noise over the audio band referred to its input.

The input-referred RMS noise contribution of resistors R_1 over the audio band is given by

$$v_{ni,R_1} = \sqrt{8kTR_1 \left(\frac{R_i}{R_1}\right)^2 B} = \frac{v_{ni,R_i}}{G_{DC}}. \tag{12}$$

Since $G_{DC} \gg 1$, v_{ni,R_1} is more than two orders of magnitude lower than v_{ni,R_i} and, hence, it is negligible.

The noise contribution of R_3 is referred to the loop-filter input with a transfer function approximately given by

$$H_{ni,R_3}(s) = \frac{sR_iC_2}{1 + sR_3C_2}, \tag{13}$$

and, hence,

$$v_{ni,R_3} = \sqrt{8kTR_3 \left(\frac{R_i}{R_3}\right)^2 \frac{B - \frac{\arctan(2\pi BC_2R_3)}{2\pi R_3C_2}}{R_3^2}}. \tag{14}$$

Therefore, the noise of R_3 is high-pass filtered. Moreover, if $1/(2\pi R_3C_2) \gg B$, as required, the noise of R_3 is attenuated over the whole band of interest and, hence, it is negligible ($v_{ni,R_3} \approx 0$).

Finally, the input referred noise contribution introduced by R_4 is also negligible, since it is strongly attenuated in the audio band by $H_{res}(s)$. Therefore, it is possible to freely choose the value of R_4 for area optimization.

In conclusion, the input-referred RMS noise of the loop filter is approximately given by

$$v_{ni,LF} \approx \sqrt{v_{ni,R_i}^2 + v_{ni,OA_1}^2}. \tag{15}$$

The analytical expression of the input referred noise of the loop filter, given by (15), has been verified with simulations. Tab. II summarizes the different noise contributions integrated over the audio band (20 Hz-to-20 kHz). The noise contributions of the loop-filter resistors are taking into account the fully-differential implementation (e. g. $R_i = R_{i+} + R_{i-}$). The main noise contribution is produced by the input resistors R_i, while, as expected form (12) and (14), the noise contributions of the other resistors are not

dominant.

The total input-referred noise contribution of OA_1 is 8 dB lower than the noise contribution of the input resistors R_i. Simulations confirm that the noise of OA_1 is mainly due to the thermal noise of the input differential pair, since the flicker noise has been reduced by using long-channel transistors.

The total input-referred noise of the loop filter turns out to be -104.4 dB_V, validating (15). This is a constant noise contribution (independent of the input signal) in the CT-$\Sigma\Delta$M.

As mentioned in Section III-E, the main feedback DAC is directly connected to the input nodes of OA_1. Therefore its RMS current noise contribution ($i_{n,DAC}$) is referred to the $\Sigma\Delta$M multiplied by R_i.

The input-referred noise contribution of a single DAC element, determined in static conditions (i. e assuming that the noise is constantly injected in the loop filter), is reported in Tab. II. The noise contributions of the different DAC elements are uncorrelated. Therefore, when the input voltage is at full scale and 7 DAC elements are used, the total input-referred noise contribution becomes $\sqrt{7}$ times the value reported in Tab. II. By contrast, the noise contribution of the DAC bias generator is common to all the DAC elements. Therefore, when the input voltage is at full scale and 7 DAC elements are used, this noise contribution becomes 7 times the value reported in Tab. II.

The total input-referred noise of the $\Sigma\Delta$M when a single DAC element is connected is, therefore, -102.1 dB_V. However, for low input signal level (< -17 dB_{FS}), the single DAC element used is constantly switching from the +1 or -1 state to the 0 state (in which no noise is injected), depending on the instantaneous value of input signal and quantization noise. For this reason, the total $\Sigma\Delta$M input referred-noise for input signals lower than -17 dB_{FS} is between -104.4-dB_V and -102.1 dB_V. This means that the expected DR, without A-weighting, is approximately 103 dB. Considering A-weighting, this value is increased approximately by 3 dB, leaving enough margin to target a $DR > 100$ dB A-weighted even in presence of PVT variations.

IV. Experimental Results

The proposed CT-ΣΔM has been fabricated using a 0.16-μm CMOS technology. The micrograph of the 0.21-mm^2 chip is illustrated in Fig. 21.

In the measurements, the differential input audio signal has been provided by an Audio Precision SYS-2722 source, while the system clock has been generated with a Hewlett-Packard 33120A waveform generator. The ΣΔM output bits are captured using a Tektronix TLA 704 Logic Analyzer and then processed with Matlab®. For the spectral analysis, a 2^{16}-points FFT with Hanning window has been used.

Fig. 22 shows the measured *SNDR* as a function of the input sinusoidal signal amplitude at 1 kHz. The full-scale input signal (0 dB_{FS}) corresponds to 1 V_{rms} differential. The achieved *DR* is 106 dB (A-weighted), corresponding to an $ENOB > 17$ bits, whereas the peak *SNDR* is 91.3 dB. The change of slope in the SNDR curve for input signal amplitudes larger than -17 dB_{FS} is due to the increased current-steering DAC noise when more than one three-level DAC element is used (acceptable for the microphone application, where the performance for large input signals is limited by the microphone itself).

The CT-ΣΔM output spectra obtained with -60-dB_{FS} and -1-dB_{FS}, 1-kHz input signals are shown in Fig. 23. As expected, at -1 dB_{FS} the noise floor increases of about 10 dB with respect to -60 dB_{FS}, due to the increased DAC noise. Fig. 24 shows the measured inherent antialiasing properties of the CT-ΣΔM. The spectral components around f_s are aliased back to the audio band attenuated by more than 70 dB, in excess of the application requirements. This value is in line with what expected for a CT-ΣΔM based on the CIFF topology [8].

The analog section of the 3rd-order ΣΔM consumes 350 μW, while the digital blocks (i. e. DEM and thermometer-to-binary converter) consume 40 μW, both from a 1.6-V power supply and during conversion. The achieved Schreier Figure-of-Merit, defined as $FoM_S = DR + 10\log(B/P)$ (B being the bandwidth and P the power consumption), is 180 dB, which is among the highest reported for audio ΣΔM. Tab. III shows the achieved performance summary, as well as a comparison among audio ΣΔMs with $DR > 100$ dB. Fig. 25 shows a comparison with the state-of-the-art from [11].

V. Conclusions

This paper presents an audio CT-ΣΔM for MEMS microphones. The CT-ΣΔM 3rd-order loop filter is realized with only two opamps, whereas conventional solutions require up to four opamps. In the proposed loop filter part of the power consumption saved by reducing the number of opamps has been reallocated to the first opamp, thus lowering its thermal noise and increasing the overall *DR*. Moreover, the feedback DAC, realized with three-level current-steering elements, introduces only a small amount of noise for low input signal levels, thus allowing the *DR* to be further increased without power consumption penalty. The proposed CT-ΣΔM achieves a *DR* of 106 dB A-weighted with a power consumption as low as 390 μW, leading to the very high FoM_S = 183 dB A-weighted. The inherent antialiasing properties and the relatively high input impedance of the CT-ΣΔM (47 kΩ) allow the simplification of the microphone front-end circuit, saving power and area also in the overall system.

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BIOGRAPHIES

Claudio De Berti received the B. S. and M. S degrees in electronic engineering from the University of Pavia, Italy, in 2009 and 2012, respectively. In 2016, he received the Ph. D. degree in microelectronics from the University of Pavia. In summer 2012 and 2014, he was with Conexant Systems, Irvine, CA as intern in the Analog and Mixed-Signal Group, were he was involved in the design of audio delta-sigma ADCs. In 2015, he joined Conexant Systems, where he is presently a Mixed Signal Designer. His current interest is the design of high-resolution delta-sigma A/D and D/A converters for audio applications and low-noise acoustic interfaces.

Piero Malcovati (S'92-M'95-SM'05) graduated in electronic engineering from the University of Pavia, Italy, in 1991. In 1992, he joined the Physical Electronics Laboratory (PEL) at the Federal Institute of Technology in Zurich (ETH Zurich), Switzerland, as a Ph. D. candidate. He received the Ph. D. degree in electrical engineering from ETH Zurich in 1996. From 1996 to 2001, he was an Assistant Professor at the University of Pavia. Since 2002, he is an Associate Professor in the same University. His research activities are focused on microsensor interface circuits and high performance data converters. He is member of the technical program committee of several conferences, including ISSCC and ESSCIRC. He is IEEE Senior Member.

Lorenzo Crespi received the Laurea degree in Electrical Engineering from University of Pavia, Italy, in 1997. He joined Rockwell Semiconductors in Newport Beach, California in 1997 working as analog designer on the development of ICs for telecommunications. Since 2000 he has been with Conexant Systems in Irvine, California where he has worked on data converters and analog front-ends with applications in ADSL, WLAN, and Imaging. He is currently Director of Analog Mixed-Signal design at Conexant, working on development of audio and power-management products.

Andrea Baschirotto (M'95-SM'01-F'14) graduated in electronic engineering from the University of Pavia, Italy, in 1989. In 1994, he received the Ph. D. degree in electronic engineering from the same University. In 1994, he joined the University of Pavia as Assistant Professor. In 1998, he joined the University of Lecce, Italy, as Associate Professor. From 2007, he is Associate Professor at the University of Milano-Bicocca, Italy. His research activity is focused on the design of CMOS mixed analog/digital integrated circuits, in particular for low-power and/or high-speed signal processing. He is member of the technical program committee of several conferences. He is IEEE Fellow.

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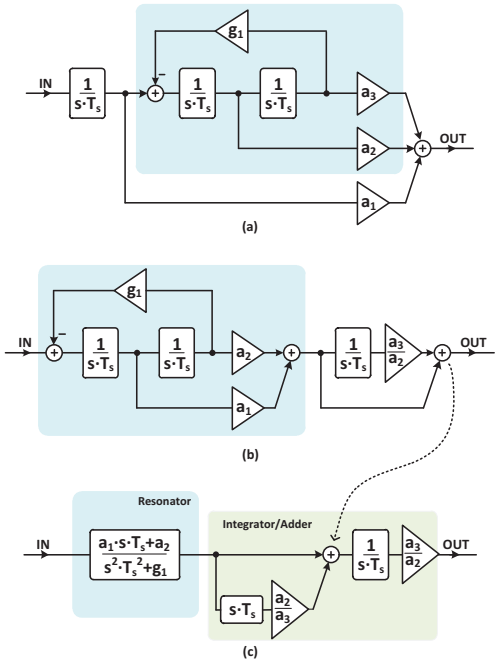
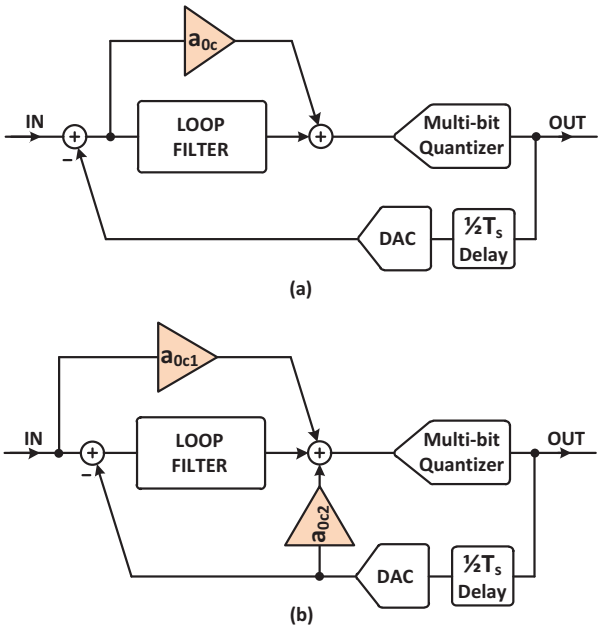


Fig. 1. 3rd-order loop filter



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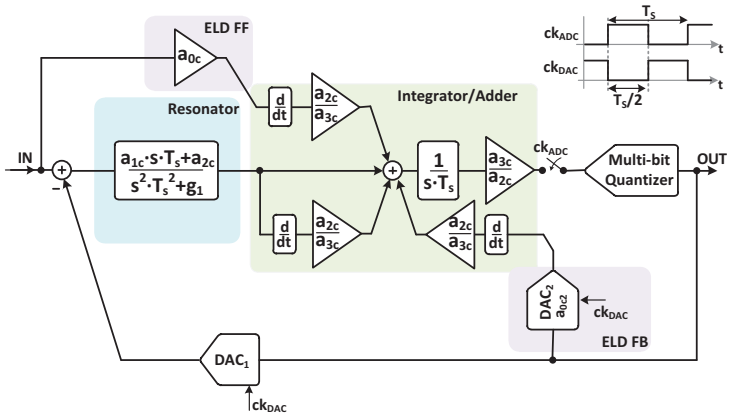

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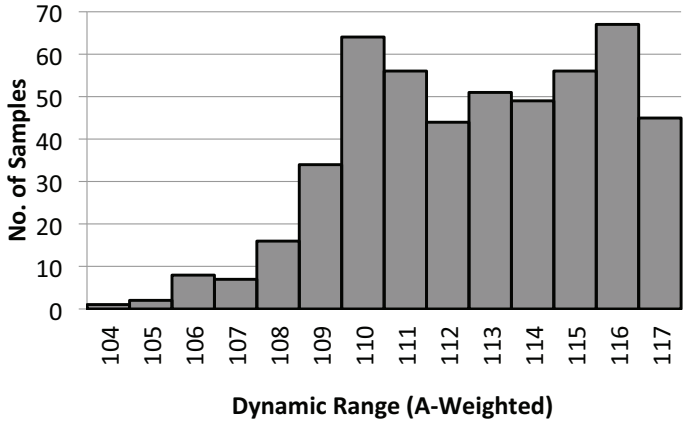

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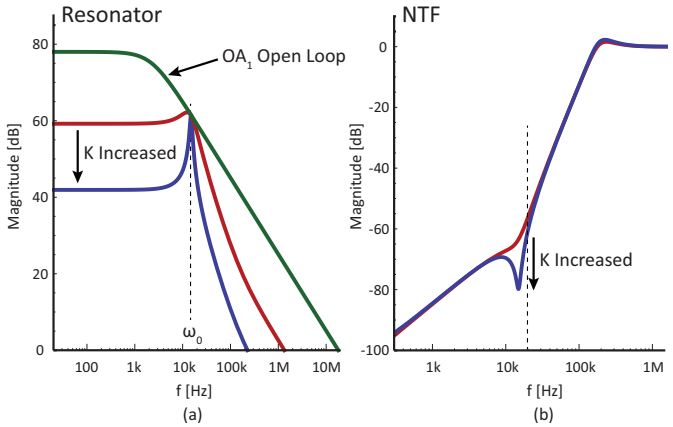

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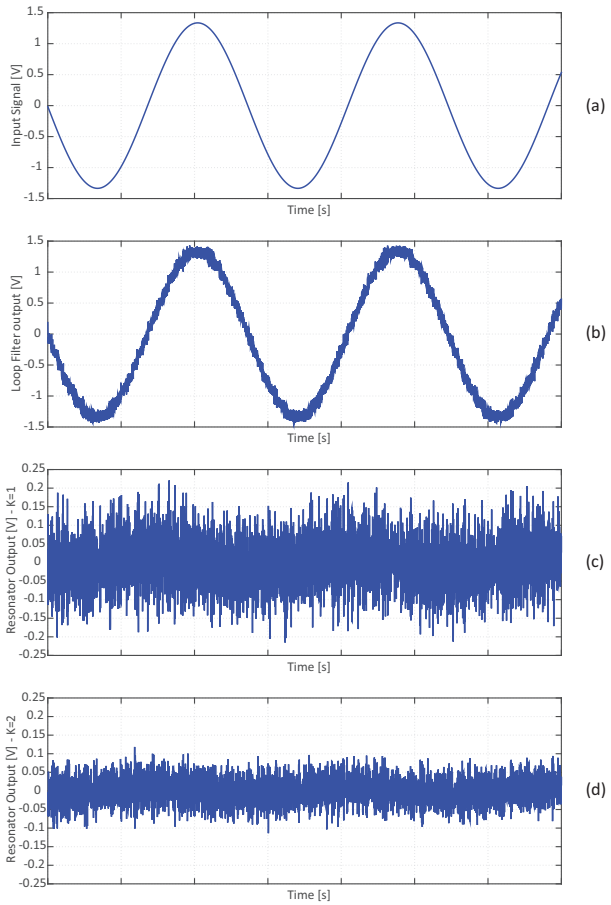

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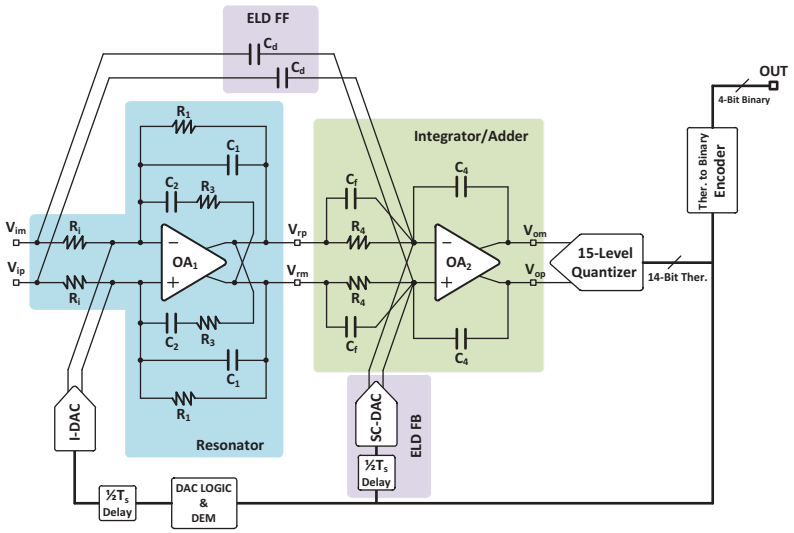


Fig. 7. Schematic of the proposed CT-ΣΔM

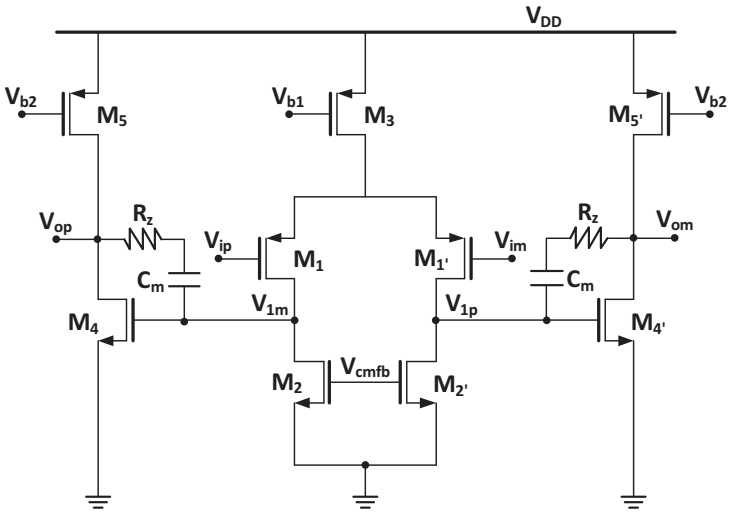
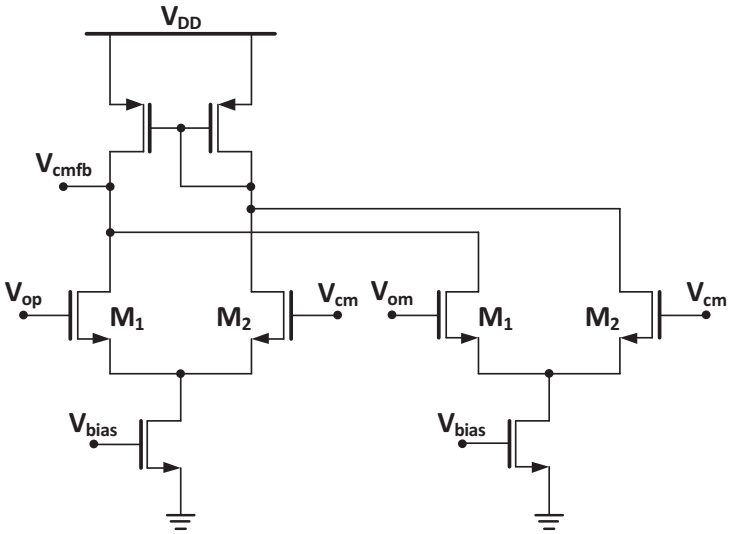


Fig. 8. Circuit schematic of the opamp (OA_1) used in the resonator



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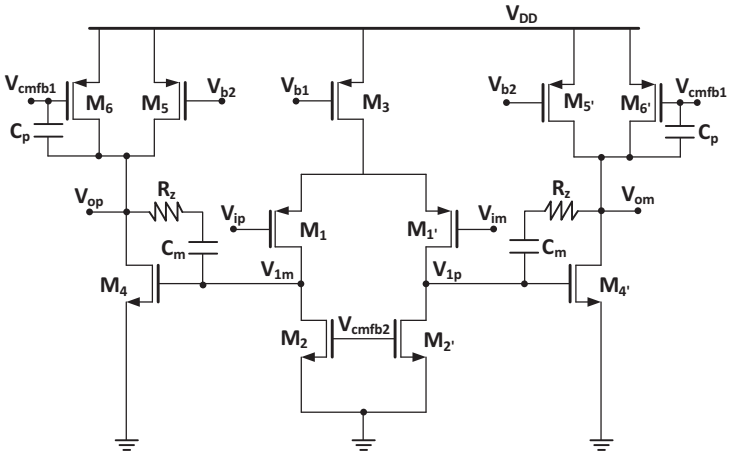

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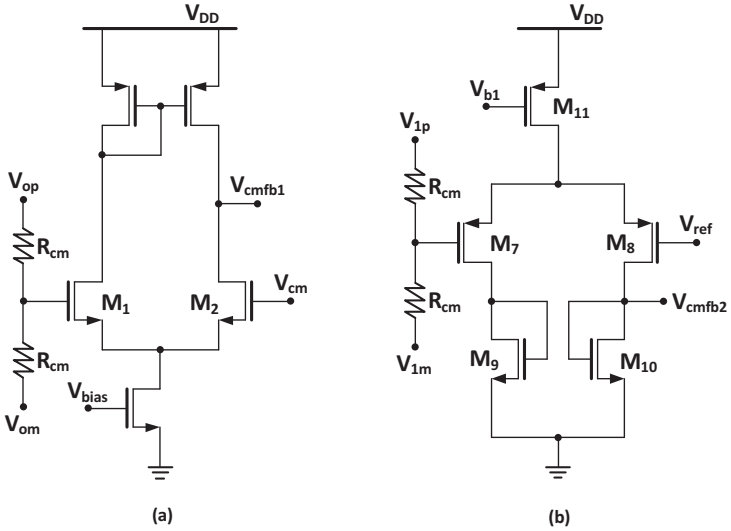
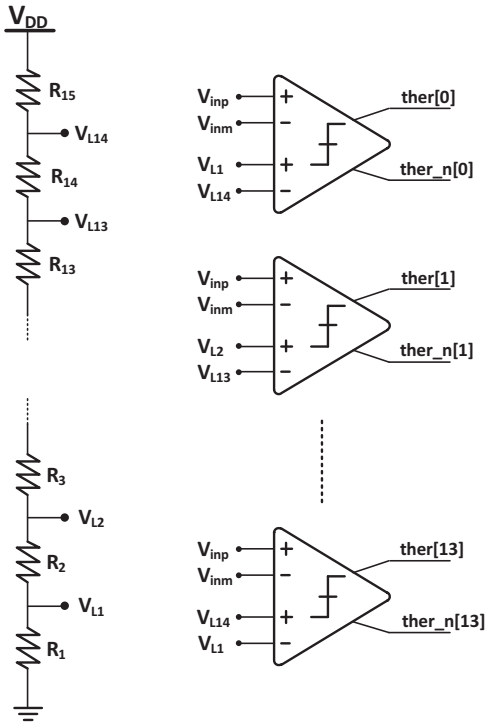


Fig. 11. Circuit schematic of the CMFB circuits used for OA_2



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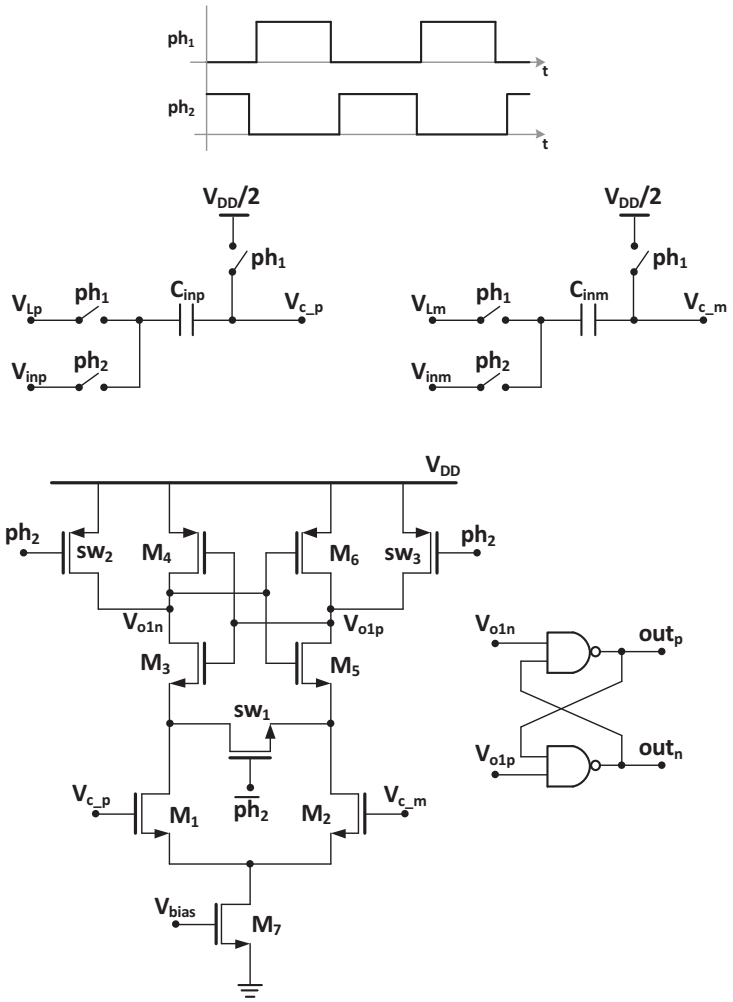

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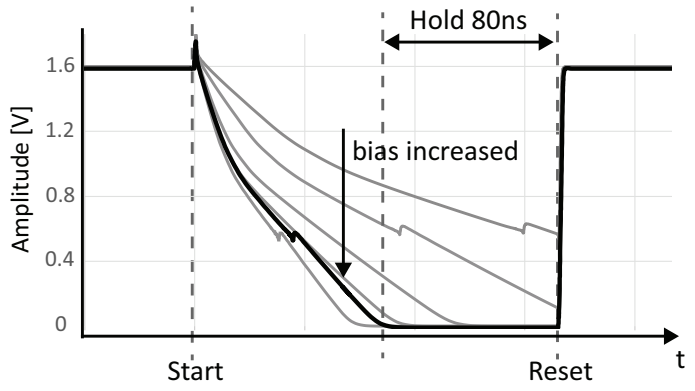

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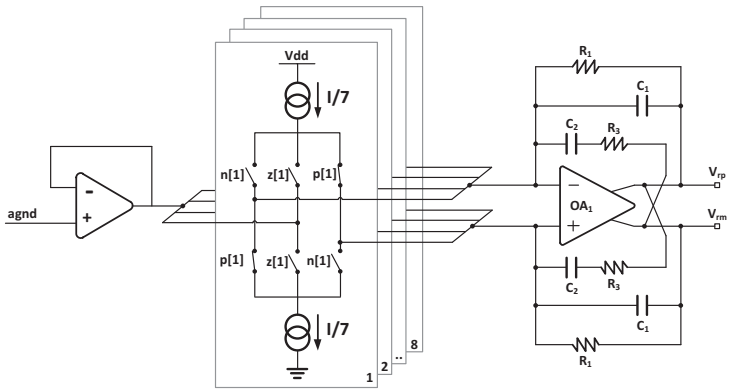

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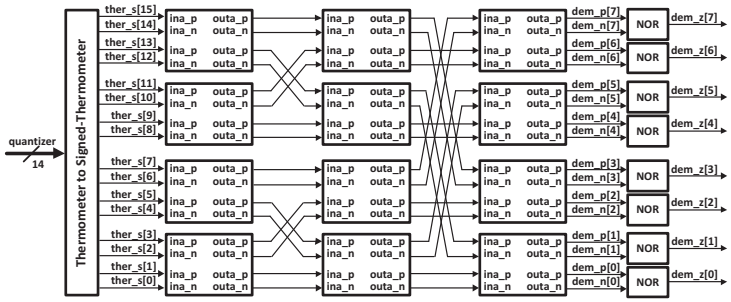

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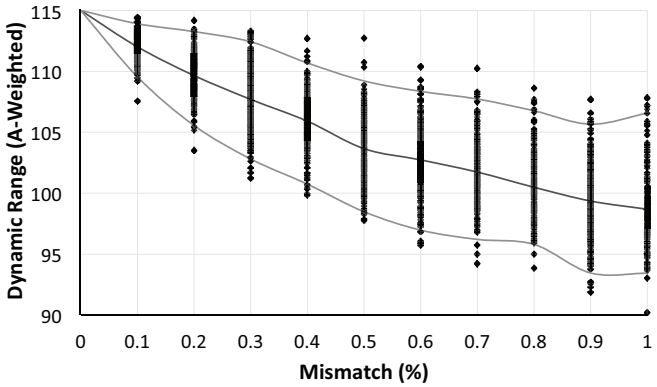
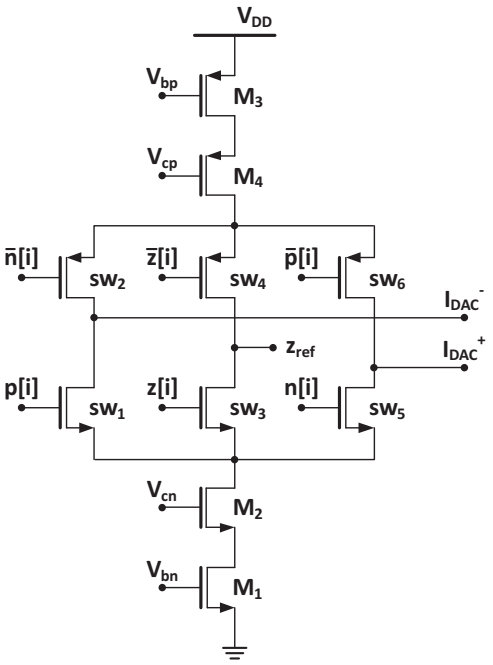


Fig. 17. In-band *DR* (A-weighted) as a function of the random mismatch among the DAC current sources obtained by running 200 simulations for each value of mismatch (the lines identify the the best 5%, average, and worst 5% cases, respectively)



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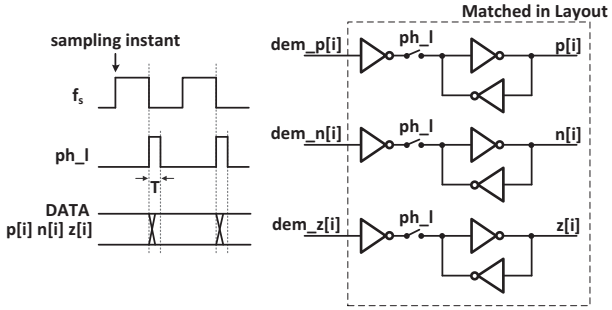

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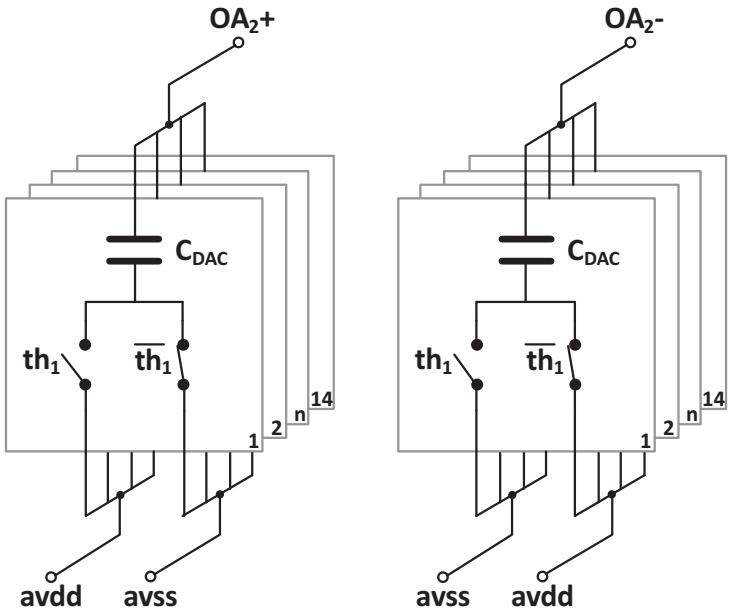

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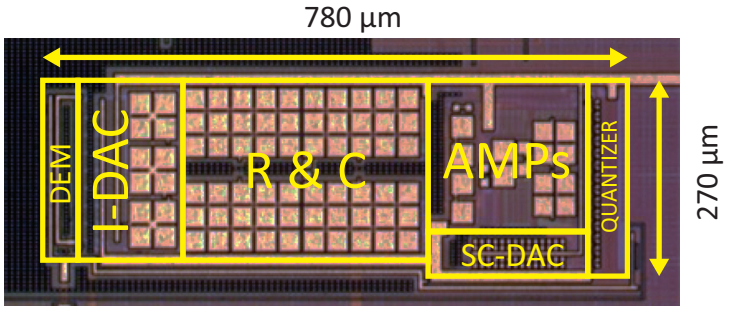


Fig. 21. Chip micrograph of the proposed CT-ΣΔM

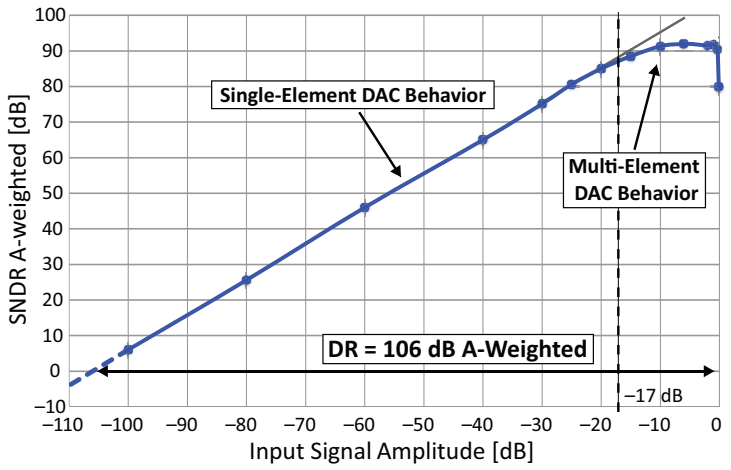
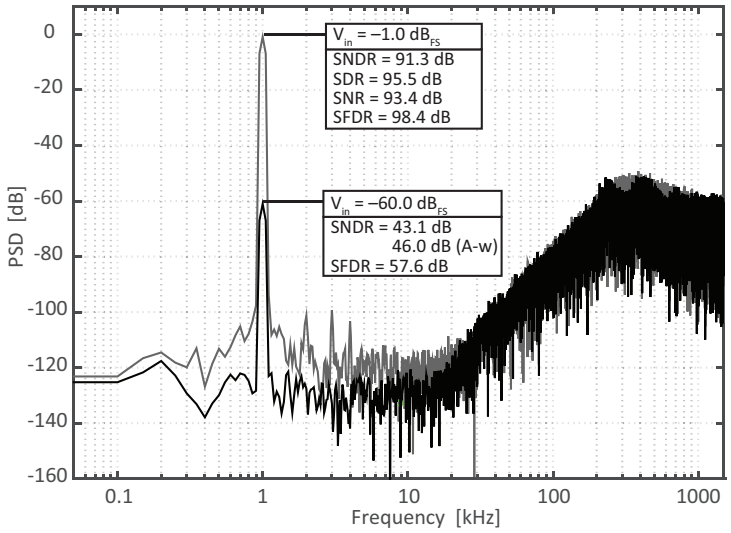


Fig. 22. Measured *SNDR* of the proposed CT-ΣΔM as a function of the input signal amplitude



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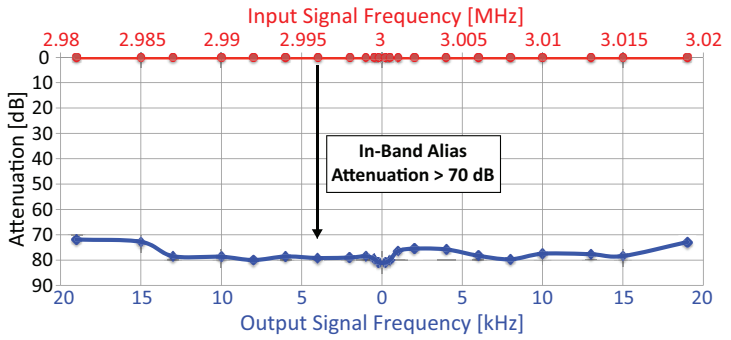

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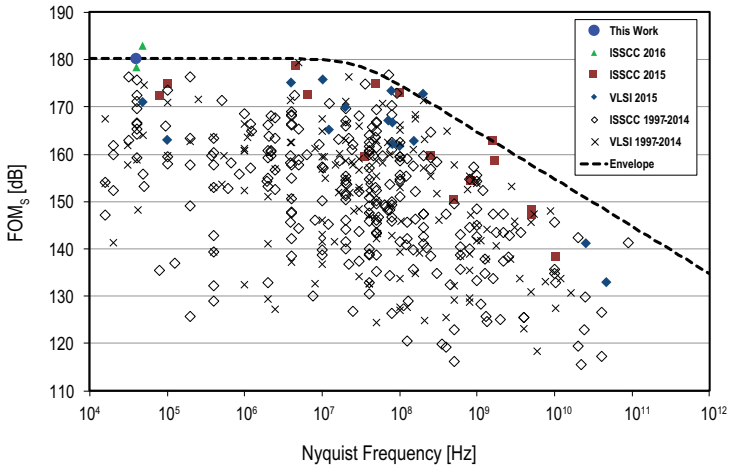

Fig. 25. Comparison with the state-of-the-art based on *FoM*$_S$ from [11]

TABLE I
PASSIVE COMPONENT VALUES WITH SCALED COEFFICIENTS (K = 2)

Resistor	Value
R_i	47 kΩ
R_1	5.7 MΩ
R_3	57 kΩ
R_4	1 MΩ
Area	$\approx$ 0.041 mm^2

Capacitor	Value
C_1	18.5 pF
C_2	18.7 pF
C_f	2.1 pF
C_4	1 pF
Area	$\approx$ 0.041 mm^2

TABLE II
SIMULATED INPUT-REFERRED NOISE CONTRIBUTIONS IN THE CT-ΣΔM

Component	RMS Noise [dB$_V$]
R_i	−105.1
OA_1	−113.2
R_1	−126.1
R_3	−128.4
R_4	−136.2
Total Loop-Filter Noise	**−104.4**
DAC Element	−107.5
DAC Bias Circuit	−110.9

TABLE III
PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE-OF-THE-ART OF HIGH-*DR* AUDIO ΣΔMS

Parameter	This Work	[12]	[13]	[14]	[15]	[1]	[16]	[2]	[17]	[18]	[19]	[20]
Technology [nm]	160	180	40	180	180	350	130	350	65	180	180	160
Architecture	CT	CT	CT/SC	SC	SC	SC	SC	CT/SC	CT/SC	CT/SC	CT	SC
Supply Voltage [V]	1.6	1.8	2.5/1.2	0.7	5.0/1.8	5.0/1.8	3.3	3.3	3.3	3.3	1.8	1.8
***P* [mW]**	0.39	0.28	0.50	0.87	1.10	68.00	9.90	18.00	15.00	37.00	0.28	1.65
***B* [kHz]**	20	24	24	25	20	20	20	20	20	20	24	20
OSR	75	128	135	100	64	153.6	128	128	256	128	128	282
Area [mm^2]	0.21	0.24	0.05	2.16	0.38	5.62	0.49	0.82	0.28	0.65	1.33	0.16
Peak *SNDR* [dB]	91.3	98.2	90	95	99.3	105	97.5	99	85	95	98.5	98.3
***DR* [dB]**	103.1	103	102	100	101.3	—	—	—	—	—	103.6	107.5
$DR_{\text{A-Weighted}}$ [dB]	106	—	—	—	—	114	105	106	101	102	—	—
FoM_S [dB]	180	182	179	175	174	166	165	163	159	156	183	178