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65 nm CMOS analog front-end for pixel detectors at the HL-LHC

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ABSTRACT: This work is concerned with the design and the experimental characterization of analog front-end electronics conceived for experiments with unprecedented particle rates and radiation levels at future high-energy physics colliders. A prototype chip integrating different test structures has been submitted in the framework of the CHIPIX65 project. These structures are standalone channels for the readout of hybrid pixels, featuring a charge sensitive preamplifier as the first stage of the readout chain, a high-speed comparator and a circuit for fine threshold tuning. The paper thoroughly discusses the results, mainly focused on the charge sensitive amplifier, coming from the characterization of the submitted test structures.

KEYWORDS: Pixel detectors, Analog Front-end, CMOS, High-Luminosity LHC.

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Contents

1. Introduction

Next generation pixel chips at the High-Luminosity (HL) LHC will be exposed to extremely high levels of radiation and particle rates. In the so-called Phase II upgrade, ATLAS and CMS will need a completely new tracker detector, complying with the very demanding operating conditions and the delivered luminosity (up to 5 $\times 10^{34}$ cm^{-2}s^{-1} in the next decade). Target pixel size for such experiments will be 50 μm $\times$ 50 μm for the innermost layers of the tracker, with a power budget close to 0.5 W/cm^2 and a hit rate in the order of 2 GHz/cm^2. With respect to current hybrid pixel detectors, featuring a typical sensor substrate thickness of 300 μm, thinner sensing devices are being proposed for the Phase II upgrades. This will lead to smaller signals, exacerbating the requirements on the noise performance of the analog front-end electronics. In particular, a limit for the equivalent noise charge can be set around 150 electrons, taking into account that the analog readout has to be operated at relatively low threshold (close to 1000 electrons) in order to retain good performance from the detection efficiency standpoint.

The 65 nm CMOS technology exhibits a high degree of radiation tolerance [1] and allows the designer to integrate very dense in-pixel analog and digital functions. Such a technology node is the target technology of the RD53 Collaboration for the development of readout chips for the innermost pixel layers of ATLAS and CMS at the HL-LHC [2].

The CHIPIX65 project [3], funded by the Italian Institute for Nuclear Physics (INFN), shares the design efforts of the RD53 consortium by exploring the 65 nm CMOS technology in the development of pixel front-end electronics for future colliders. It is focused on the design of core elements in analog and digital electronics and on the chip integration issues, particularly important when complex digital circuits, with a huge amount of transistors, have to be integrated with the analog front-end electronics. In the framework of CHIPIX65, a prototype chip called CHIPIX-VFE-1, including different test structures, has been submitted and a comprehensive characterization activity

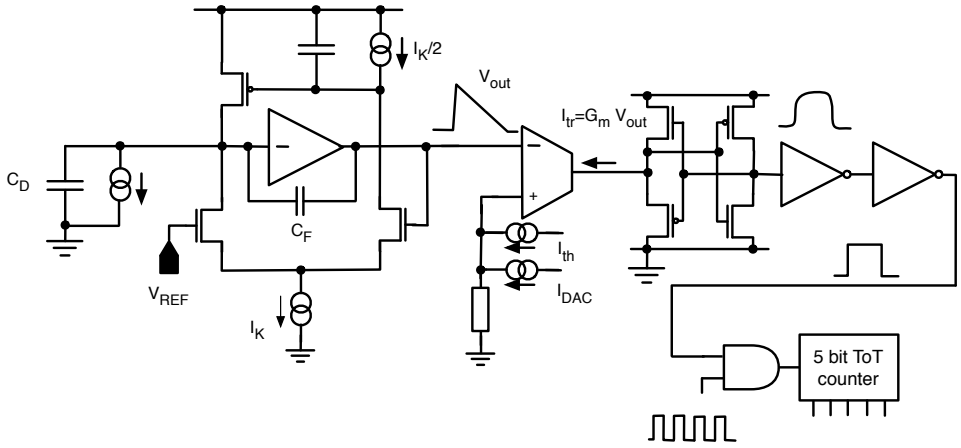

Figure 1. The analog front-end integrated in the CHIPIX-VFE-1 chip.

is ongoing. CHIPIX-VFE-1 includes two small matrices with different front-end designs (the one discussed in this work, based on an asynchronous architecture, and one based on a synchronous front-end [4], not described in this work) both using a common digital configuration and readout architecture, and standalone analog channels. This work describes the design and the experimental characterization of the CHIPIX-VFE-1 standalone channels, which represent the fundamental building blocks for the development of an innovative pixel front-end chip for the HL-LHC.

2. Analog Front-end

The asynchronous analog front-end integrated in the CHIPIX-VFE-1 chip is shown in figure 1. The readout chain includes a charge sensitive amplifier (CSA) featuring a Krummenacher [5] feedback complying with the expected large radiation induced increase in the detector leakage current. The choice of a single amplification stage in the front-end channel has been simply dictated by power consumption constraints. The signal from the CSA is fed to a high-speed, low power current comparator [6] that, combined with a 5-bit, dual edge time-over-threshold (ToT) counter, is exploited for time-to-digital conversion. The ToT counter is operated by means of a relatively slow, 40 MHz clock which allows for a 400 ns maximum time over threshold. Channel to channel dispersion of the threshold voltage is addressed by means of a local circuit for threshold adjustment, based on a 4-bit binary weigthed DAC generating the current I_{DAC}. The front-end chain is designed for a maximum input charge equal to 30000 electrons and features an overall current consumption close to 4 μA.

The characterized test structures include two standalone charge sensitive amplifiers, featuring a PMOS transistor or a metal-insulator-metal (MIM) structure as the feedback capacitor, and two channels including the CSA, the threshold discriminator and the trimming DAC. Each test structure includes a 30 fF injection capacitance and a few programing bits which can be properly set in order to obtain different channel configurations. In particular, the CSA can be operated in high gain and low gain mode by acting on the feedback capacitance, whereas the recovery current, I_K,

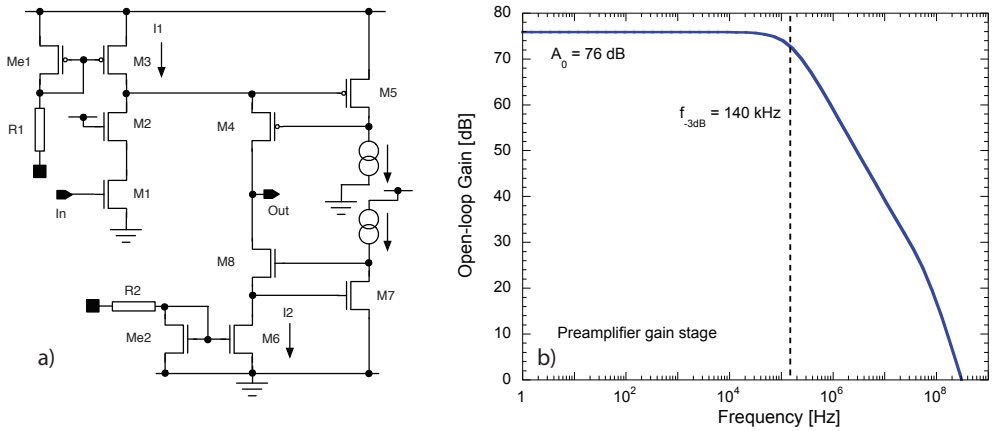

Figure 2. a) Charge sensitive amplifier forward gain stage. b) Simulated open loop gain of the preamplifier.

in the Krummenacher feedback network, can be set to 12.5 nA or 25 nA. Two programming bits are used to set the detector emulating capacitance, C_D, at the preamplifier input.

3. Charge sensitive amplifier

The core element of the charge sensitive amplifier is the gain stage shown in figure 2a). This is a folded cascode architecture including two local feedback networks, composed by the M4-M5 and M7-M8 pairs, boosting the signal resistance seen at the output node. With a current flowing in the input branch equal to 3 μA and a current in the cascode branch close to 200 nA, the CSA is responsible for most of the power consumption in the analog front-end. The schematic diagram also shows the bias networks of the preamplifier, which include two external transistors, Me1 and Me2, mirroring the reference currents in the pixel cell. Figure 2b) shows the simulated open loop

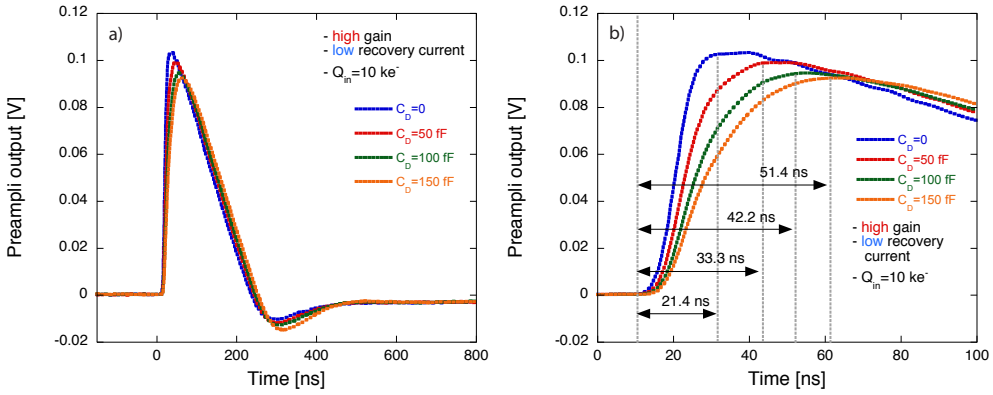

Figure 3. a) Preamplifier output response to an input charge Q_{IN}=10000 electrons. The preamplifier, featuring a MOS feedback capacitor, is configured in high gain mode, low recovery current (I_K=12.5 nA). b) Rising edge of the preamplifier output signal.

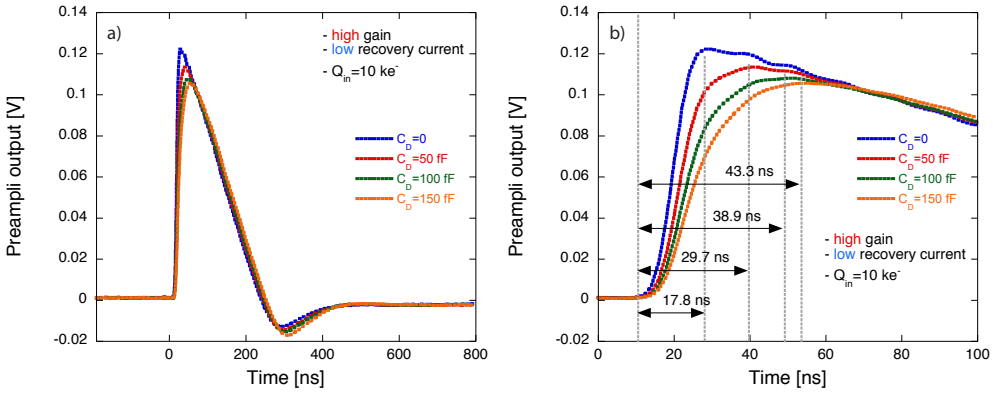

Figure 4. a) Preamplifier output response to an input charge Q_{IN}=10000 electrons. The preamplifier, featuring a MIM feedback capacitor, is configured in high gain mode, low recovery current (I_K=12.5 nA). b) Rising edge of the preamplifier output signal.

gain of the preamplifier, whose DC gain is equal to 76 dB with a cutoff frequency close to 140 kHz.

3.1 CSA response and charge sensitivity

The response of the preamplifier featuring a MOS feedback capacitance, for an input charge equal to 10000 electrons, is shown in figure 3a). In particular, the plot shows the preamplifier output for different values of the detector emulating capacitor, C_D, ranging from 0 to 150 fF, with the CSA configured in high gain mode and low recovery current (I_K=12.5 nA). It is worth noticing that the total capacitance shunting the preamplifier input also includes the 30 fF injection capacitance, which adds to the C_D capacitance. A zoom of the rising edge of the output signal is shown in figure 3b), which points out a maximum peaking time equal to 51.4 ns for a detector capacitance C_D=150 fF. Similarly, figure 4a) shows the response of the preamplifier, configured in the same

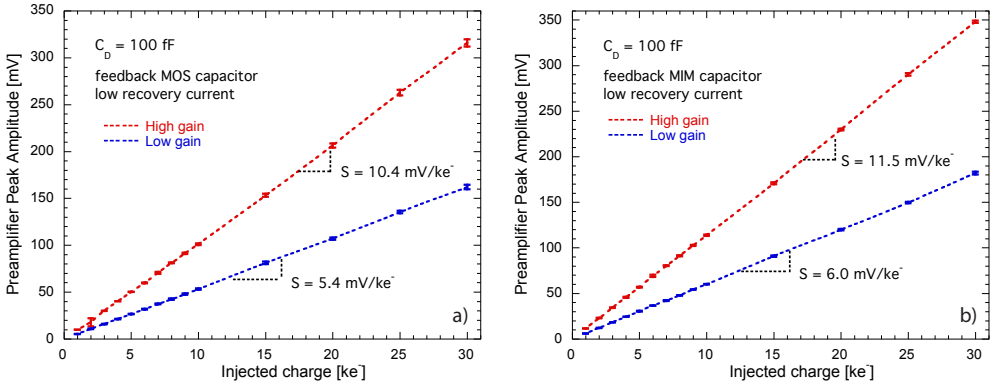

Figure 5. Preamplifier peak amplitude as a function of the input charge for the CSA with a PMOS a) and a MIM feedback capacitor b). Red curves are relevant to the preamplifier configured in high gain mode, blue ones refer to the low gain configuration.

way, with a MIM feedback capacitor. This version of the CSA is slightly faster compared to the version including a PMOS transistor as the feedback element. In particular, a maximum peaking time equal to 43.3 ns has been measured for the MIM feedback capacitor version of the preamplifier, as shown in figure 4b).

The charge sensitivity of the preamplifier, designed to be about 13.5 mV/ke$^-$ for the high gain configuration, is defined as the slope of the fitting straight line of figure 5, showing the preamplifier peak amplitude as a function of the injected charge. The plots actually show the average peak values measured on a set of four different samples, with error bars indicating the standard deviations (smaller than 3% of the mean values for all the possible configurations). Red curves refer to the preamplifier configured in high gain mode, whereas blue ones are relevant to the low gain configuration of the channel. As expected, the ratio between the charge sensitivity in high gain mode and the one evaluated for the low gain mode is close to 2, since two equal value capacitors are connected in parallel in the low gain configuration while just one of the two is used in high gain mode. The integral non linearity is smaller than 1.5% for all the configurations. As shown in figure 5b), a slightly higher charge sensitivity for the preamplifier featuring a MIM feedback capacitor has been detected.

3.2 Equivalent noise charge measurements

The equivalent noise charge (ENC) has been measured for the preamplifier in different configurations. As an example, figure 6 shows the ENC as a function of the total preamplifier input capacitance (which includes both the detector emulating capacitance, set by means of the programming bits, and the 30 fF injection capacitor) for the preamplifier configured in high gain (red squares) and low gain (blue circles) with a recovery current I_K equal to 12.5 nA. In particular, figure 6a) refers to the CSA featuring a MOS feedback capacitance whereas figure 6b) refers to the MIM capacitor version of the feedback. ENC increases by increasing the preamplifier input capacitance, and turns out to be higher for the channel configured in low gain mode. Measured ENC is in fairly good agreement with simulation data, as shown in figure 6a), where the gray diamonds refers to the

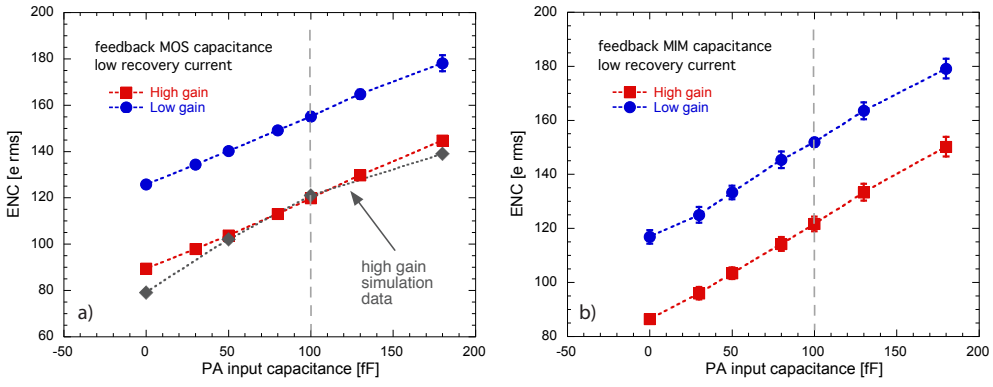

Figure 6. Equivalent noise charge as a function of the total preamplifier input capacitance for the CSA with a PMOS a) and a MIM feedback capacitor b). Plot a) also shows the simulated ENC (gray diamonds), for the channel configured in high gain mode.

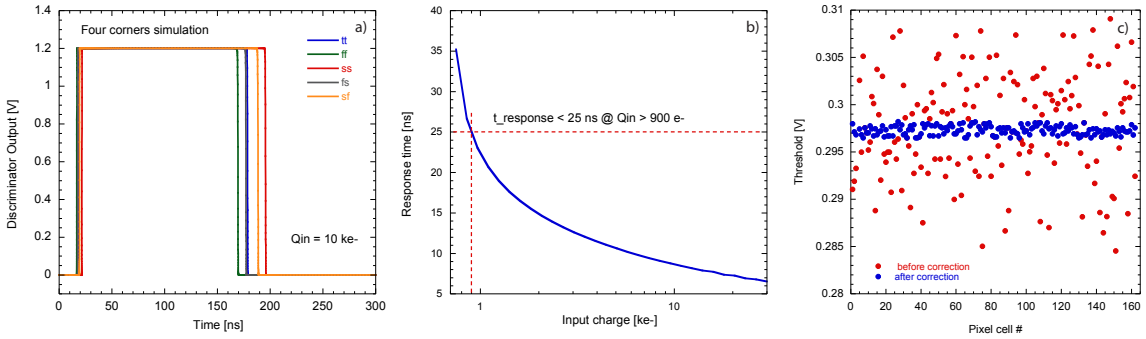

Figure 7. a) Four corners simulation of the comparator output response to a 10000 electrons input charge. b) Simulated front-end response time as a function of the injected charge. A threshold equal to 750 electrons has been set in the simulation. c) Simulated threshold, in Volts, for a number of pixels before and after threshold correction.

simulated ENC for the preamplifier configured in high gain mode. For a target input capacitance of 100 fF and the CSA in high gain configuration, an ENC equal to 120 electrons has been measured, below the 150 electron ENC limit mentioned in the introduction.

4. Threshold discriminator with trimming DAC

As previously mentioned, the front-end channel includes a high-speed, low power threshold discriminator, based on current comparison, connected at the preamplifier output. Shown in figure 1, it includes a transconductance stage whose output current is fed to the input of a transimpedance amplifier [7] providing a low impedance path for fast switching. A couple of inverters is used after the transimpedance amplifier in order to consolidate the logic levels. Unfortunately, some problems have emerged with the test of the channels equipped with the comparator. Such problems are likely due to the use of a quite large custom designed digital buffer used to read out the discriminator output signal. The buffer, which consists of a tapered chain of 8 inverters (the size of the bigger one being two thousands times the size of the unit inverter of the 65 nm technology used in the design), features very high switching current, responsible for noticeable bouncing on power lines. This results in undesirable bounces in most of the nodes of the analog front-end whenever the comparator flips, including the preamplifier output and the comparator input threshold nodes. Such bounces in turn are responsible for generating spurious hits at the comparator output, making this effect somehow self-sustained and, ultimately, measurements on the comparator impossible. This behavior has been investigated and reproduced in circuit simulations by adding parasitic inductances on power lines. A new version of the chip, including smaller (a factor of 6) readout buffers, has been submitted in order to fix the issue. Due to the lack of measurements on the threshold discriminator, just some simulation data are reported in this section. In particular, figure 7a) shows the results of a four corners simulation of the comparator response to an injected charge, at the preamplifier input, equal to 10000 electrons. Very small variations in the time at which the comparator flips can be observed for the rising edge of the output signal. On the other hand, non negligible changes in

the pulse width have been detected in the four corners simulation. Figure 7b) shows the simulated response time of the whole channel as a function of the input charge. From this plot it is possible to notice that the channel response time is smaller than 25 ns for an input charge greater than 900 electrons. A threshold equal to 750 electrons was set in the simulation. The current consumption of the comparator is close to 1 μA, which, added to the one relevant to the preamplifier, results in a total power consumption close to 5 μW. The performance of the analog front-end in terms of threshold dispersion are greatly improved by the use of a 4 bit, in-pixel binary weighted DAC providing local threshold trimming. As a qualitative insight into the behavior of the tuning system, figure 7c) shows the threshold, in Volts, for a number of pixels before (red circles) and after (blue circles) correction. From circuit simulations, threshold dispersion before correction is equal to 380 electrons, reduced down to 35 electrons after tuning.

5. Conclusion

A prototype chip called CHIPIX-VFE-1 has been submitted in a 65 nm CMOS technology in the framework of the CHIPIX65 project. A comprehensive characterization of the standalone channels, mainly focused on the charge preamplifier in its different configurations, has been carried out showing encouraging results for both the version of the preamplifier. Slightly better performance have been detected for the CSA version with a MIM feedback capacitance, featuring a faster response and a charge sensitivity closer to the design value. Some problems have emerged with the experimental characterization of the threshold discriminator. Such problems are likely due to the use of a quite large custom designed digital buffer used to read out the discriminator output signal. A new version of the chip has been submitted in order to fix such problems.

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