

A SAW-Less 2.4GHz Receiver Front-End with 2.4mA Battery Current for SoC Coexistence

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ABSTRACT

A 2.4 GHz receiver for short-range communications with +6dBm out-of-band IIP3 and only 2.4 mA battery current is presented. The single-ended input is coupled through an integrated transformer to a push-pull differential LNTA followed by a current mode passive mixer that drives a single-opamp biquad TIA. This approach ensures sufficient linearity to enable coexistence with large out-of-band interference arising from other on-chip/on-board transceivers. An efficient block stacking technique is proposed to minimize the current drawn from a standard 1.8V supply. The first stages of the two opamps used in the I and Q base-band Rauch filters are placed above and below the LNTA core, thereby sharing its DC current. Two active inductors isolate the RF and BB signal paths. Several techniques are used to limit the impact of the 1/f noise of the RF blocks on the receiver and to minimize nonlinearities due to interactions between blocks sharing the same current. The entire receive signal path draws 2.4mA from a 1.8V supply and has a noise-figure of 7.8 dB at 2.4GHz and an OOB 1dB compression point of -5 dBm. The chip, implemented in 28nm LP CMOS, occupies an active area of 0.4 mm².

INDEX TERMS

Coexistence; Low Power; Current Reuse; Active Inductor; Bluetooth.

I. INTRODUCTION

Smart terminals provide connectivity for different applications such as cellular, Wi-Fi and Bluetooth (BT) [1]-[4]. An enabling factor for the widespread adoption of these devices has been the availability of low-cost, small form factor single chip radios [5]-[7]. The proliferation of frequency bands for cellular communications [8]-[11] and the emergence of the Internet of Things (IoT) [12][13] has increased the pressure to further reduce cost and form factor by increasing integration and reducing the off-chip components such as SAW filters and duplexers [10] [14]-[19]. As a result, concurrent operation (coexistence) of different radios operating on contiguous frequency bands becomes more and more difficult [20][21]. In a typical coexistence scenario, the signal from one radio (aggressor) acts as interferer for another radio (victim), located on the same platform or even on the same SoC, leading to very challenging blocking requirements. To meet these goals, the receiver front-end must have both low phase noise and enhanced linearity, i.e. IIP2, IIP3 and 1-dB compression point. Satisfying these requirements is more difficult for short-range links, where the power budget is very tight. As an example, Fig. 1 reports a typical coexistence scenario [22] where a BT radio is the victim while cellular and Wi-Fi are the aggressors, with peak transmitted power levels of 30 dBm and 20 dBm respectively. Moreover, continuous-wave (CW) blockers must also be tolerated, with levels that can be as high as -10dBm [23]. Coexistence can be addressed through a sophisticated frequency planning that supersedes the operation of the terminal. Nonetheless, with the increased spectrum density of newer standards (e.g. LTE and soon 5G), avoiding proximity of RX and TX channels becomes problematic. Therefore, it is important to improve receiver interference immunity while keeping power consumption low. Various strategies have been introduced to address this challenge e.g. current re-use, voltage supply reduction,

interference filtering/cancellation, etc. However, all of them have limitations that may affect their viability. Self-interference (SI) filtering/cancellation techniques try to mitigate the SI at known frequencies (e.g. the TX), thereby relaxing RX linearity requirements. Albeit attractive in principle, practical implementations have highlighted limitations in terms of amount of SI that can be handled, cancellation bandwidth, increased noise and power dissipation [24]-[27]. In [24] a translational loop based notch filter consumes 4 mA of current to handle up to -38 dBm of TX leakage. The active canceler in [25] can handle up to 2 dBm SI power with only 0.8 dB NF degradation but burning up to 72 mW. Passive cancelers perform low-power SI cancellation but typically require a large TX-RX isolation for proper operation. As an example, in [26] the maximum SI power is limited to -23 dBm and 50 dB TX-RX isolation is required. Therefore, SI cancellation solutions suitable for short-range low-power receivers remain a challenging research target. On the other extreme of the spectrum, current reuse techniques minimize power dissipation but either sacrifice noise or increase area while supply reduction compromises linearity and may not save power if an efficient low supply is not available on the platform. In this paper we target current reduction through extensive re-use of the RF and Base-Band (BB) sections of the receiver assuming only a standard 1.8 V supply is available. At the same time, achieving high linearity is our main goal for the reasons outlined above. System considerations are discussed in Section II. Section III describes in detail the circuit design, focusing on noise, linearity and the low power frequency compensation strategy for the BB opamp. Sections IV and V report measurements and draw the conclusions respectively.

II. SYSTEM DESIGN CONSIDERATIONS

Short range wireless links such as BT, BT Low Energy (BLE) or Zig-Bee, require very low power transceivers [28]-[37]. The main strategies adopted to achieve this goal are:

low-voltage design, current-reuse and building block/device reuse. In the first one the supply voltage is scaled down to 1V or below [16][35], leading to sub-mW power consumption for the entire RF front-end. Aggressively scaling down the supply, however, leads to poor linearity and reduced immunity to interferers. In wireless sensors, where the node is often powered by an energy-harvester, a low supply voltage may in fact be desirable. On the other hand, in SoC based platforms, only a few supply voltages are available because generating an efficient very low dedicated supply is most often not justified by the extra cost. A typical analog supply ranges between 1.5 to 1.8 V [38]-[41]. In these cases, a more appropriate figure of merit of the efficiency is the current drawn from the battery as opposed to the power associated with the super low supply [42]. An alternative technique is to reuse a device or even a building block to perform multiple functions. In [36] a “recursive receiver” is introduced, where the same block amplifies both RF and down-converted signals. This solution is attractive but simultaneously processing RF and IF signals with the same device is a potential source of extra distortion. Moreover, noise could also increase if the recursive receiver is not carefully designed. In current-reuse, different blocks are stacked to reuse the same DC current. Albeit attractive, this approach introduces new issues such as DC level compatibility and signal isolation that need to be addressed to reap its potential benefits. Furthermore, stacking generally reduces voltage headroom and increases distortion. In [29] LNA, active mixers and VCO share the DC current, forming an LMV cell. Active mixers suffer from poor $1/f$ noise and signal injection in the VCO may cause locking from large blockers. The current-reuse receiver in [43] has improved IIP3, bandwidth, power and area. The LNA, active mixers and BB filters are directly coupled and share the bias current. Active mixers allow to reuse the LNA current in the BB current-mode filters but degrade $1/f$ noise, while a directly-coupled single-ended input LNA degrades

IIP2. Industrial BLE transceivers [30]-[34] typically achieve sensitivities well in excess of standard requirements while dissipating low power at the price of limited linearity. To handle large blockers, they feature low-gain modes, with reduced sensitivity. In this paper, to have low power consumption from a standard 1.8V supply and high linearity we re-use the current of a common-gate low-noise transconductance amplifier (LNTA) in the opamps of the BB filters for both the I and Q paths [44]. As shown conceptually in Fig.2, the BB I and Q filters are stacked above and below the LNTA core, thereby sharing the same DC current (I_{LNTA}). A 25% duty-cycle passive mixer ensures high linearity and low flicker noise. Large capacitors at its output enhance OOB linearity but increase noise from the BB. Reusing the large LNTA current in the opamp lowers its noise, enabling the use of large capacitors for better OOB IIP3 and 1dB compression point (CP). The necessary signal isolation is achieved by interposing an active inductor between each BB filter and the LNTA. At its input port, connected to the LNTA output, the active inductor provides high impedance at high frequency and low impedance near DC, while at its output port, connected to the BB filter, it acts as a current source.

III. RECEIVER CHAIN

The current in a common-gate LNTA defines the front-end noise, linearity and input impedance. To get sufficient noise and linearity for coexistence a current level in the order of one mA is required. A similar current is also required in each BB TIA opamp to make its contribution to the receiver noise figure (NF) small. Hence, stacking the LNTA with both the I and Q TIA opamps gives an almost optimal bias level for the three blocks while reducing the current budget by a factor close to three. A current reuse factor (χ) can be used to quantitatively assess the amount of current savings in a current-reuse architecture (see Fig. 3). χ is defined as the ratio between the current consumption in the conventional, i.e. non-stacked, structure and in the stacked structure: $\chi =$

$I_{CONV}/I_{STACKED} = (I_{LNTA} + I_{BBI} + I_{BBQ}) / (I_{BBI} + I_{BBQ} - I_{LNTA})$, where $I_{BBI} = I_{BBQ}$ is the total current used in each BB stage, including the current re-used from the LNTA (I_{LNTA}). In the limit case $I_{BBI} = I_{BBQ} = I_{LNTA}$, the proposed solution leads to a χ equal to 3, but in practice a slightly smaller value is achieved.

A. Transformer-based LNTA

A simplified schematic of the LNTA is shown in Fig. 4.a. It is a push-pull differential common gate amplifier driven by a 1:1 on-chip transformer which acts as a balun. The NMOS and PMOS transistors work in parallel, halving the current required to give the same transconductance, i.e. the same noise, with respect to an NMOS-only stage. Furthermore, the NMOS/PMOS configuration operates in push-pull, substantially improving the 1-dB CP. Two cross-coupled feed-forward capacitors effectively double the device transconductance, halving the impedance seen by the antenna and the input devices noise contribution. In this way, an equivalent LNTA transconductance of 20 mS and 50 Ω matching are achieved with a total current of only 1.4 mA. As an added benefit, capacitive cross-coupling improves immunity to common-mode signals and eliminates third-order intermodulation products caused by the so called “second-order interaction” [45], increasing IIP3. The transformer has two turns in both primary and secondary and uses a stacked topology to maximize the coupling factor (k). To reduce losses, both ultra-thick copper (UTM) and aluminum redistribution (AP) layers are used. Each winding is split into two parallel traces to overcome design rules limitations on the maximum metal width. Losses in primary and secondary windings contribute in a similar manner to the overall NF. Since AP series losses are much greater than UTM, both primary and secondary windings consist of a series connection of AP and UTM half-windings, as shown in Fig. 4.b, thus achieving nearly equal losses in primary and secondary.

B. Active Inductor

The LNTA current is reused twice, in the input stage of both BB opamps, i.e. the most critical TIA blocks from the noise point of view. Fig. 5 reports the schematic of the NMOS portion of the stack, i.e. the one implementing the I path. A similar structure, with n-type and p-type devices interchanged, is used at the bottom of the stack, i.e. in the Q path, but is not shown in the figure for clarity. An active inductor (AI) is used to isolate the RF and BB sections. On the LNTA side the AI presents an impedance which at RF is much higher than the mixer input impedance, while at DC it is much lower. In this way the RF signal is routed toward the mixer while the DC current is sent to the BB opamps. At the same time, on the BB side the AI acts like a cascoded load for the opamp input stage. With reference to Fig. 5, the RF impedance-is given by:

$$Z_{RF}(s) = \frac{(1+sR_{AI}C_{AI})}{g_{m_{AI}}\left(1+\frac{sC_{AI}}{g_{m_{AI}}}\right)} \parallel \frac{1}{sC_{RF}} \quad (1)$$

where C_{RF} is the parasitic capacitance at the source of M_{AI} . The front-end noise includes the contributions of the AIs at RF, injected at the LNTA output, as well as at low frequencies, injected into the BB. The noise factor, not including the BB, is given by:

$$F = 1 + \frac{\gamma}{2} + \frac{R_{bal}}{R_S} + 4R_S \left(\gamma g_{m,AI} + \frac{1}{R_{AI}} \right) \left(1 + \frac{R_{bal}}{2R_S} \right)^2 + K_1 \frac{V_{fk,LNA}^2}{4kTR_S} + K_2 \frac{V_{fk,AI}^2}{4kTR_S} \quad (2)$$

The term $1+\gamma/2$ represents the noise of the capacitive cross-coupled common-gate stage [45], the balun losses are represented by an equivalent series resistor R_{bal} and all the other terms come from the AIs. The AIs RF noise injection come from the white noise of MOS transistors M_{AI} and resistors R_{AI} , while the BB noise injection come mainly from the flicker-noise of the LNTA ($M_{1,2,3,4}$) and of the AI's MOS (M_{AI}). These contributors are due to a low frequency direct path from LNTA to BB through the AIs. This path does not exist in a conventional architecture since the mixer up converts low frequency noise in addition to being AC coupled. To reduce LNTA low frequency noise

coupling, the AI MOSs are split into two halves and recombined at the output with opposite signs, as shown in Fig. 6.a. In this way flicker noise is injected as common mode at the BB opamp first stage output and rejected by the differential second stage ($K_1 \sim 0$). Since cancellation does not apply to AI noise, this is minimized by resistively degenerating M_{AI} , as shown in Fig. 6.b, taking advantage of the low flicker noise of the resistors. In (2) g_{mAI} is replaced with $g_{mAI}/(1+g_{mAI}R_{deg})$ and $K_2 \ll 1$, making the last term negligible. The value of R_{deg} creates a trade-off between voltage headroom and noise reduction. For a given total voltage drop minimum noise is obtained using wide transistors working in sub-threshold. The body of AI MOS transistors is connected to the source terminals to lower the MOS threshold, decreasing their V_{GS} . As a compromise, $R_{deg} = 570 \Omega$ was chosen, with a degenerated transconductance of 2.85 mS for each AI. Simulations of the RF front-end with an ideal 1:1 transformer give a NF of 3.2 dB before down-conversion, in good agreement with (2).

C. Front-end Linearization

The combination of a push-pull input stage together with cross-coupling feed-forward capacitors enables the LNTA to achieve both high linearity and high 1dB CP with a small current. However, the AIs that isolate LNTA from BB introduce additional nonlinear effects that can potentially limit the IIP3. More specifically, the common-mode impedance presented by the AIs to the LNTA, introduces a nonlinear modulation that could degrade the linearity of the RF section. A brief introduction to the problem and the adopted solution are given below. Let us firstly model the RF input transistors in Fig. 7 (left) as non-linear transconductors with zero output conductance. With two tones at the receiver input (V_{IN}) of amplitudes V_{B1}, V_{B2} and frequencies ω_1 and ω_2 ,

$$V_{IN} = V_{B1}\cos(\omega_1 t) + V_{B2}\cos(\omega_2 t) \quad (3)$$

the second-order non-linearity in the transconductance of the LNA input transistors (g_2)

creates an intermodulation component in their drain current at frequency $(\omega_1 - \omega_2)$

$$I_{D0} = V_{IN}g_{m1} + V_{IN}^2g_2 + \dots = V_{IN}g_{m1} + \frac{1}{2}V_{B1}V_{B2}g_2\cos(\omega_1 - \omega_2)t + \dots \quad (4)$$

and in the drain voltage (V_{D2}) of the same transistors at frequency $(\omega_1 - \omega_2)$ according to:

$$V_{D2} = \frac{1}{2}V_{B1}V_{B2}g_2\cos(\omega_1 - \omega_2)t Z_{AI}(\omega_1 - \omega_2) \quad (5)$$

where $Z_{AI}(\omega_1 - \omega_2)$ is the active inductor input impedance evaluated at the frequency of the intermodulation term. Here $Z_{AI} = Z_{RF}$, as given by (1), where g_{mAI} is replaced with $g_{mAI}/(1 + g_{mAI}R_{deg})$. Notice that the 2nd-order intermodulation voltage is a common-mode signal. Now, taking into account channel-length modulation, the drain signal current of the input transistor (M1) is given by $I_D = I_{D0}V_{IN}(1 + \lambda V_D)$. It follows that, the 2nd nonlinear voltage component V_{D2} at $(\omega_1 - \omega_2)$ modulates the drain currents linear terms $g_{m1}V_{B1}$ and $g_{m1}V_{B2}$ at frequency ω_1 and ω_2 , leading to the two third order intermodulation tones (I_{D3}) in the drain current at $(2\omega_1 - \omega_2)$ and $(2\omega_2 - \omega_1)$ given below.

$$I_{D3} = \frac{1}{4}g_{m1}g_2\lambda Z_{AI}(\omega_1 - \omega_2)[V_{B1}^2V_{B2}\cos(2\omega_1 - \omega_2)t + V_{B1}V_{B2}^2\cos(2\omega_2 - \omega_1)t] \quad (6)$$

The input impedance of the AI (Z_{AI}) increases with frequency, going from $1/g_{m,AI}$ near DC, to a much higher value (R_{AI}) at higher frequencies (inductive behavior with equivalent inductance $L_{EQ} = C_{AI}R_{AI}/g_{m,AI}$) before decreasing due to the parasitic capacitance C_{RF} . Hence, as the two-tones frequency spacing $(\omega_1 - \omega_2)$ increases, so does the nonlinear drain voltage (V_{D2}), correspondingly degrading the LNTA IIP3. To reduce this undesired effect, the active inductor common-mode input impedance is lowered by exploiting the symmetry of the circuit. We observe that, since the 2nd-order nonlinear current generated by M1 (M2) is a common-mode signal, it cannot flow through the LNA differential driving impedance. As a result, neglecting the common-mode parasitic at the input nodes, the magnitude of the common-mode 2nd-order

distortion current at the drain of the four input transistors (M1-M4) is the same. On the other hand, the resulting non-linear voltage at the drains of M1 (NMOS) and M3 (PMOS) have opposite phase. Furthermore, making the input impedance of the PMOS and NMOS AIs to be the same, these terms will be equal in magnitude and opposite in phase, i.e. $V_{dM1}=V_{dM2}=-V_{dM3}=V_{dM4}$. Hence, it is possible to lower the common-mode impedance at the drain of the input transistors by capacitive cross coupling the NMOS and PMOS AIs, as shown in Fig. 7 (right). With the cross-coupling, the common-mode impedance Z_{AI} decreases with frequency, instead of increasing as with the conventional AI design, going from $1/g_{m,AI}$ near DC to $1/(2g_{m,AI})$ at higher frequencies. The common-mode impedance seen looking into the active inductor is now given by:

$$Z_{RF,XCPL}(s) = \frac{(1+sR_{AI}C_{AI})}{gm_{AI}(1+2sR_{AI}C_{AI})} \parallel \frac{1}{sC_{RF}} \quad (7)$$

As a result, the nonlinear mechanism described above is substantially reduced and is no more the limiting factor. Notice that, for the differential signals the AI impedance is still given by (1) because an input differential signal generates in-phase signals at the drains of M1 and M3 (M2 and M4). To verify the effectiveness of the proposed solution IIP3 simulations using two tones with variable frequency spacing have been carried out for both configurations. Fig. 8 reports both the impedance Z_{AI} and the IIP3 for the two cases versus frequency spacing. With the standard configuration Z_{AI} is about 800Ω near DC, reaches a peak value of $3k\Omega$ near $50MHz$ and then decreases due to the load capacitors. The corresponding IIP3 degrades when the frequency spacing (f_2-f_1) is increased, reaching a minimum of $3.5dBm$ near the Z_{AI} peak. As opposite, for the cross-coupled configuration the impedance Z_{AI} decreases with frequency, going from 800Ω near DC to below 400Ω above $50MHz$. Correspondingly, the IIP3 remains around $10dBm$ for frequency offsets up to $200MHz$.

D. 25% Current-mode passive resonant mixer

The two LNTA outputs, from NMOS and PMOS, are summed through a capacitive combiner, made of 8 MOM capacitors, connected to the two I and Q 25% current-mode passive mixers, which are followed by two stacked second order Rauch filters, as shown in Fig. 2. Two different DC voltages must be used at the input of the I and Q BB filters due to the stacked architecture. Therefore, the quadrature passive mixer is divided into two halves, working at two different DC voltage levels, i.e. 1.3 V for I and 500 mV for Q, as shown in Fig. 9. A parallel LC tank resonating at the fourth harmonic of the LO is placed in series with the mixer on the base-band side [15]. This creates a high impedance at the 3rd and 5th harmonic of the LO on the RF side, thanks to the bilateral nature of passive mixers, reducing noise folding and improving harmonic rejection. Simulation shows that about 0.8 dB NF reduction and over 1.5 dB gain increase is obtained using this technique. Finally, care is taken to minimize parasitic capacitance at the LNA output, to maximize the BB driving resistance due to switched capacitor effect [46]. This resistance, together with the BB capacitance C_1 in Fig. 10, used to reject LO harmonic injection, determines the BB opamp noise transfer function.

E. Baseband filter

The BB Rauch filter can significantly attenuate the blockers with low power since it provides 2nd order low-pass filtering while using a single opamp. Fig. 10.a shows the schematic of the filter and how it is interfaced with the mixer. The filter uses a three stage opamp that burns 1.74 mA. The 1.4mA current in the first stage is provided by the LNTA through the two AIs that act like cascoded current sources. The second and third stages, jointly requiring 340uA, are not stacked and can use the whole supply voltage in order to maximize the available voltage swing. The resulting overall current reuse factor between the LNTA and the two BB opamps is 2.45. Fig. 11 gives more details about the internal structure of the opamp used in the I path. The one in the Q

path has a similar structure with n-MOS transistors in place of the p-MOS. The amplifier input stage is a P-type pseudo differential pair loaded by the two AIs that draws 1.4 mA. To intuitively understand why a large current is desirable in the OTA first stage, in Fig. 10.b we compare the gain seen by a noise source at the input of the LNTA and of the Rauch OTA, indicated respectively as V_{LNA} in Fig. 9 and V_{OTA} in Fig. 10.a. The voltage gain from V_{LNA} to the output is equal to 28 dB and can be easily derived from the down-conversion gain considering that input power matching, capacitive cross-coupling and the complementary LNTA structure contribute 6 dB gain reduction each. The gain from V_{OTA} to the output is given by two factors: first, the output impedance of the passive mixers, that is sensitive to the LNTA output impedance [46]; second, the large Rauch capacitor C_1 . By only referring to the second mechanism, which is the easiest to compute, a conservative noise gain value is obtained (dotted line in Fig. 10.b). A large valued C_1 is necessary to improve OOB linearity. For $C_1=220\text{pF}$, the gain of V_{OTA} is 28.9 dB at 2 MHz, a value close to that of V_{LNTA} . Hence, the proposed topology allows to reuse the LNTA current where it is most needed for noise, while implementing a current-mode receiver for enhanced OOB linearity.

The second OTA stage is an n-type differential pair whose load displays a high differential mode impedance equal to $2r_o$, a low common mode-impedance equal to $1/g_m$, and consumes 100uA. This structure, needs no common-mode feedback and precisely defines the bias current of the following stage by the size ratio of the equivalent current mirror made up of M9 and M11 (M10-M12). The output is a class-A pseudo differential stage that consumes 200uA. The quiescent current of the 2nd and 3rd stage is chosen to meet the linearity requirement with the lowest power consumption. The schematic level simulated NF of the receive chain at 2.4 GHz LO and 1 MHz output frequency is 5.7 dB and the noise contributed by the various sub-

blocks is reported in Fig. 10.c. More accurate NF simulations, including post-layout parasitic, are reported in Section IV.

Due to the stacked topology 2 CMFBs are needed, one at the output of the first and one at the output of the third stage, as shown in Fig. 12. The first one (CMFB1) simultaneously performs two functions. First, it sets the second stage input common-mode voltage by sensing its value with a resistor adder, comparing it with its target of 1.5V and feeding the error to the differential transconductor GM_{CM_IN} that closes the loop. Second, it sets the quiescent V_{GS} of the input devices in such a way that they absorb the current supplied by the AIs while remaining in saturation. This is done by adjusting the difference between the output and input CM voltages injecting a current, nominally 40uA, into the two 10 k Ω feedback resistors (R_2 in Fig. 10). Notice that the input CM voltage is near V_{DD} for the top amplifier and near GND for the bottom one, so opposite current must be injected in the feedback loop for the two cases. The second CMFB circuit (CMFB2) sets the output CM voltage around $V_{DD}/2$, to have the largest possible swing. This is done again sensing the actual CM voltage with a resistor adder, comparing it with its target and feeding the error to the transconductor GM_{CM_OUT} .

F. Baseband filter stability analysis

To study stability it is convenient to re-draw the Rauch filter loop as shown in Fig. 13.a. At high frequencies the passive feedback network loads the OTA with the series of a capacitance of 2.23pF and a 90 Ω resistance. As shown below, compensating this opamp to ensure stability even for unity gain would have required a large current in the second and third stages, greatly reducing the current reuse factor. We choose as target at least 30dB of loop gain at 2MHz to have a precise filter response and suppress nonlinearities. Since the feedback loop attenuates the signal by 28dB at 2MHz, an OTA gain of nearly 60dB at 2MHz is required, or equivalently a gain-bandwidth product of over 2GHz.

Using a Miller or nested Miller compensation, with a load capacitance of 2.23pF, to push the output pole to at least twice the unity-gain bandwidth (GBW), requires a g_m of the output stage of over 40mS and a current of several milliamps. On the other hand, taking into account the effect of the feedback on the stability, we achieve our design target with a three-stage OTA that has 100MHz loop GBW while requiring a small g_m in the last two stages. The first stage reuses the current of the LNTA and has a gain A_1 of 27dB over a wide bandwidth, thanks to the small input capacitance of the second stage, which is much smaller than the first one. No compensation capacitor is used across the last two stages, as it is done in a nested Miller configuration. The second and third stages draw very little current and they have a g_m of 800uS and 1mS respectively. Only one small Miller compensation capacitor C_M (1pF) is placed across the third stage. This capacitance would be insufficient for a classic Miller compensation since it sets the unity-gain frequency ω_U of the last two stages at 120MHz while the output non-dominant pole ω_{P2} is set by g_{m3} and C_2 at 71MHz. However, as we shall see, including the effect of the Rauch feedback network, the chosen C_M ensures stable operation. The Miller dominant pole ω_{P1} is around 1MHz, hence between ω_{P1} and ω_{P2} the OTA gain is approximately $-jA_1\omega_U/\omega$. The feedback network frequency response has two poles, ω_{P0} and ω_{P3} at 80kHz and at 800MHz respectively, and two zeros both around 8MHz (ω_Z). Hence, the gain of the feedback network, between ω_Z and ω_{P3} is approximately $j\omega/\omega_{P3}$. As a result, the loop gain stays constant at $-A_1\omega_U/\omega_{P3}$ (~ 9 dB) from ω_Z up to ω_{P2} . The pole introduced by the first stage, around 150MHz, is near the unity gain frequency of the loop. To compensate for its effect on stability, improving stability, a resistor R_M is added in series with C_M , introducing a zero around 300MHz. At frequencies below 8MHz, the loop-gain rises sharply, with a 40dB/decade slope due to the double zero in the feedback network, reaching more than 32 dB at 2MHz, i.e. the

OTA gain at 2MHz is 60dB. The adopted solution, in typical condition has about 100 MHz GBW and more than 80° a phase margin (PM). This is a very conservative design and an even smaller output stage current could have been used while still ensuring stability. Actually, while the zeroes and poles associated with the feedback are well controlled, the ones in the OTA, especially the first stage, can vary significantly over temperature and process. Because of this, the large nominal PM is leveraged upon to ensure good stability even in the worst-case corner. Simulation results for worst case conditions are reported in Fig. 13.b-d, showing a PM of 58.2°.

G.Receiver Image Rejection

Since the I and Q paths operate at different voltages and are implemented with different devices, systematic quadrature mismatches are expected. Thanks to the closed loop topology, BB filters gain is rather insensitive to opamp device mismatch. Simulations of systematic I/Q gain and phase mismatch at nominal and +/-10% supply voltage as well as Monte-Carlo simulations of DC offsets and gain/phase mismatches are reported in Fig. 14 for a 1MHz output frequency. Systematic gain and phase errors of 0.4 dB and 0.03° with standard deviations of 0.02 dB and 0.02° are observed. +/- 0.2 dB and +/- 0.4° gain and phase variations result changing the supply by +/- 10%. Considering both systematic and random errors, an image rejection better than 32 dB is expected.

IV. EXPERIMENTAL RESULTS

The complete receiver schematic is reported in Fig. 15. It includes LNA, quadrature passive down-conversion mixers and two 2nd order Rauch low-pass filters. The mixers down-convert the signal to a low-IF between 1 and 2 MHz. This allows to minimize the impact of 1/f noise. The quadrature mixers are driven by a 25% duty-cycle LO signal generated by an on-chip low-noise frequency divider by two [15]. No special care was taken to reduce the power dissipation of the frequency divider and LO buffers which,

reusing the design in [47], draw 6.5 mA from a 1 V supply. The LO power dissipation could be considerably reduced e.g. using the main 1.8V supply and adopting charge-reusing techniques [33], where stacked LO buffers are used. The receiver was implemented in TSMC 28nm LP CMOS process and occupies an active area of 0.4mm², as shown by the chip photo (Fig. 16). If an LC oscillator was included in the chip, careful layout and sufficient separation between the oscillator and the receive chain inductors would be required to minimize undesired magnetic couplings. For characterization the chip was directly bonded on a PCB. A carefully optimized set-up and an extensive measurement campaign were implemented. Because of this some of the data shown below are different compared with those reported in [44] where only preliminary measurements were performed. Measured and simulated receiver gain and NF are plotted in Fig. 17 as a function of the RF frequency. The simulated gain has a maximum of 43.8 dB and varies by less than 0.5 dB from 2 to 2.8 GHz. The measured gain has a maximum of 43.7 dB, with less than 1.3 dB variation across the whole band. NF goes from 7.5 to 8.7 dB in the frequency range from 2 to 2.8 GHz, i.e. from 0.1 to 0.5 dB higher than simulations. Agreement between simulation and measurements is even better including the almost perfect correlation between the loss of gain and the increase in NF (less than 0.1 dB discrepancy across the entire frequency range). To verify the effectiveness of the harmonic rejection filter placed at the mixer output, the down-conversion gain at the third harmonic of the signal has been measured for various settings of the tuning circuit. As shown in Fig. 18, 3rd harmonic rejection goes from 22 dB at $f_{LO}=2\text{GHz}$ to 35 dB at $f_{LO}=2.6\text{GHz}$, mostly due to the low-pass filtering action of the matching components on the PCB, and is almost independent of the harmonic-rejection filter tuning. This is attributed to a design error that was identified in the tuning circuit of the harmonic filter after the tape-out and that negatively affects harmonic

rejection and consequently NF and Gain. RX IIP3 vs. two-tones frequency spacing is plotted in Fig. 19 for an LO of 2.4 GHz. It starts at -20 dBm for in-band signals, where linearity is limited by the BB, and reaches 6 dBm when the frequency spacing is 200 MHz, where IIP3 is limited by the LNA. IIP3 approaches 9 dBm for a spacing of 600 MHz. Thanks to the push-pull LNA the small-signal gain 1dB CP due to an out-of-band CW blocker is also very high, over -5 dBm for frequency offsets above 200MHz, as reported in Fig. 20. In-band compression is reached when the BB output swing approaches rail-to-rail at 1.8V supply, which corresponds to -30 dBm input power. Improved in-band compression could be achieved lowering the BB trans-resistance gain (R_2 in Fig. 10.a), with a small impact on noise. Careful design would be needed, however, to ensure stability in all the gain settings. As a further test of the robustness to OOB blockers, the receiver NF was measured in the presence of an OOB CW blocker. Fig. 21 reports the measured NF as a function of the blocker power for an LO of 2GHz and blocker frequencies of 2.1 GHz and 2.18GHz. In both cases, the measured NF increases by less than 3dB up to the maximum OOB blocker power, which for BT is -10dBm. Thanks to the fully-differential topology the receiver IIP2 is also very high. With two closely spaced tones at 200MHz offset from the carrier IIP2 is 60 dBm. With two widely-spaced tones (1.2 and 3.601 GHz), the IIP2 is limited by the LNA to 48.2 dBm. The image rejection ratio (IRR) as a function of the output frequency (Fig. 22) was measured by feeding the receiver I and Q outputs to the BB modulation inputs of an RF vector signal generator and displaying the modulated carrier on a spectrum analyzer. An IRR better than 31 dB is maintained between 1 and 2 MHz even as the supply is varied by +/- 10%. Overall, a good agreement between measurements and simulations is observed, demonstrating that the proposed solution is suitable for low-power wireless applications where coexistence is critical. The current consumption of

the down-conversion chain, excluding LO driving circuitry, is only 2.4 mA. Table I summarizes performance and compares it to recently published low-power receivers. Similar or lower noise, comparable current consumption and higher OOB IIP3, IIP2 and 1dB CP with respect to prior implementations are achieved. The mixer-first solution in [37] reaches similar OOB IIP3 (measured at low blocker levels) but suffers from low 1dB CP and, furthermore, it has significant LO leakage. This may cause system issues making this solution unsuitable for some applications. For the circuits in [16] and [35] power dissipation is quite low but performance is inferior both in terms of noise and linearity. A low current consumption is achieved by the current-reuse receiver in [29] at the price of high NF and low OOB linearity. On the other hand, current consumption is similar to that of industrial BLE transceivers [30][33] but OOB linearity is significantly improved without reducing the gain.

V. CONCLUSION

Co-existence between different transceivers on the same chip/board operating concurrently becomes increasingly difficult at low power consumption when external SAW filters are eliminated for cost reasons. A low-power highly linear receiver based on a current reuse topology was proposed for wireless SoC co-existence. Power dissipation is minimized using a high linearity push-pull LNA topology and reusing its current twice, for the I and Q path, in the BB filtering TIA. The LNA and part of the two TIAs are stacked and isolated using two AI. The front-end operates from a 1.8V supply that can be derived from an efficient power supply voltage converter. The receiver front-end meets the Bluetooth OOB blocking requirements without the need for an external SAW. Adjacent-channel interference rejection would need to be improved in order to be fully compliant with standard requirements, as reported in [30], e.g. by introducing a low-gain mode or a complex-filter with enhanced selectivity

instead of the real low-pass filter adopted in this design.

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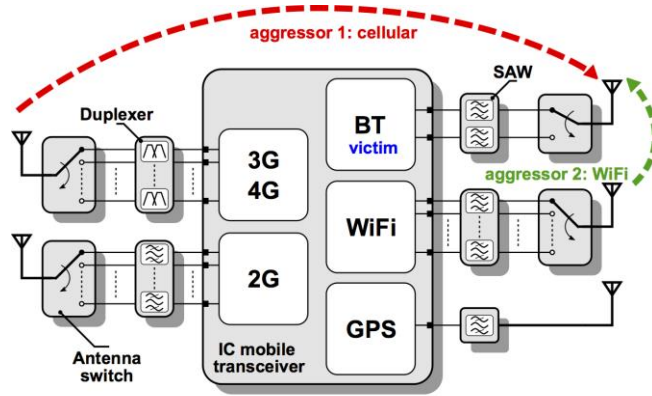


Fig. 1: Coexistence issue in a smart terminal.

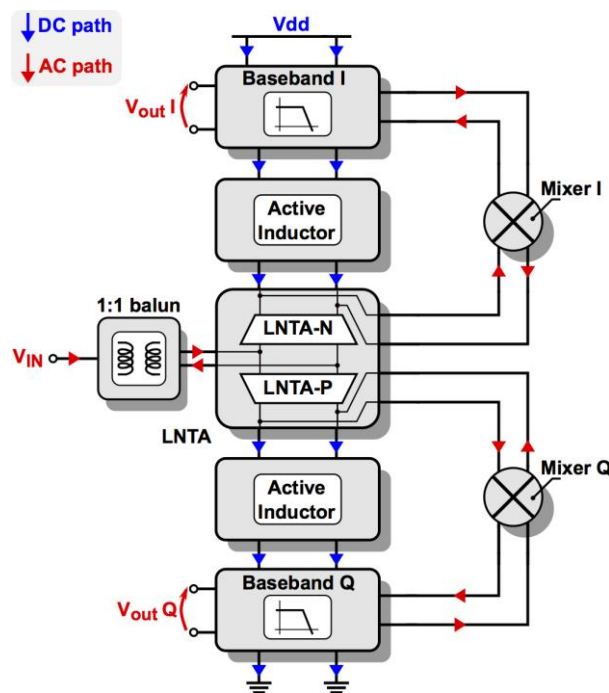


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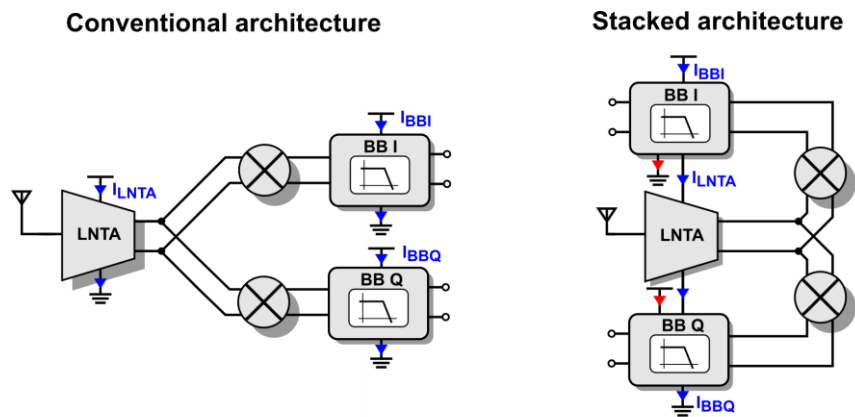


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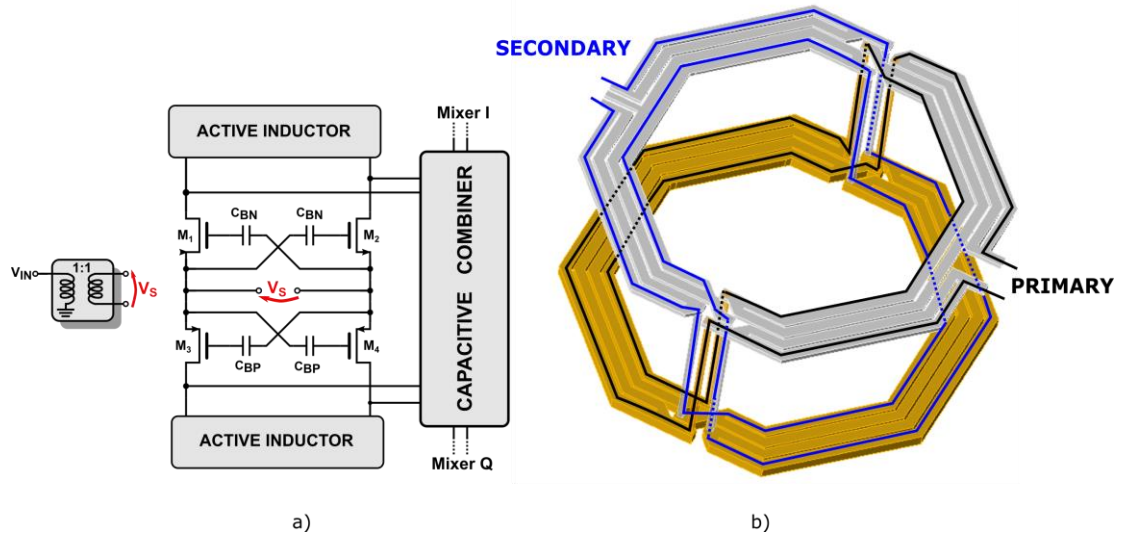


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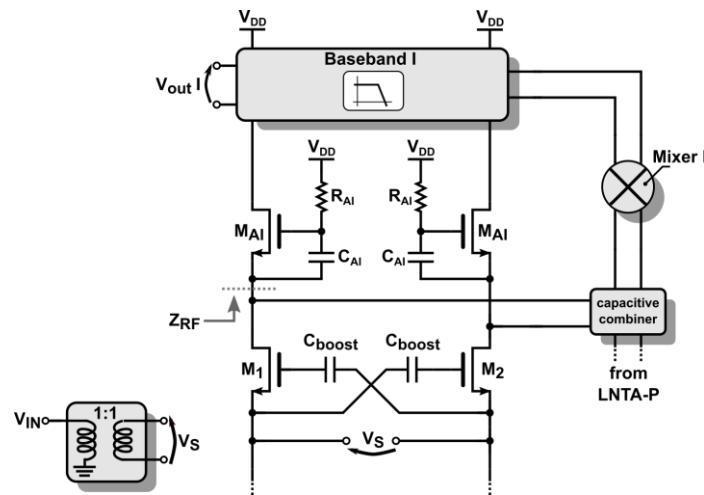


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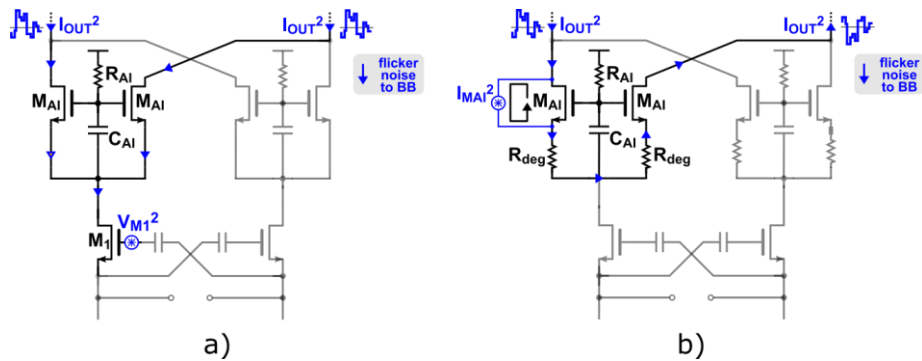


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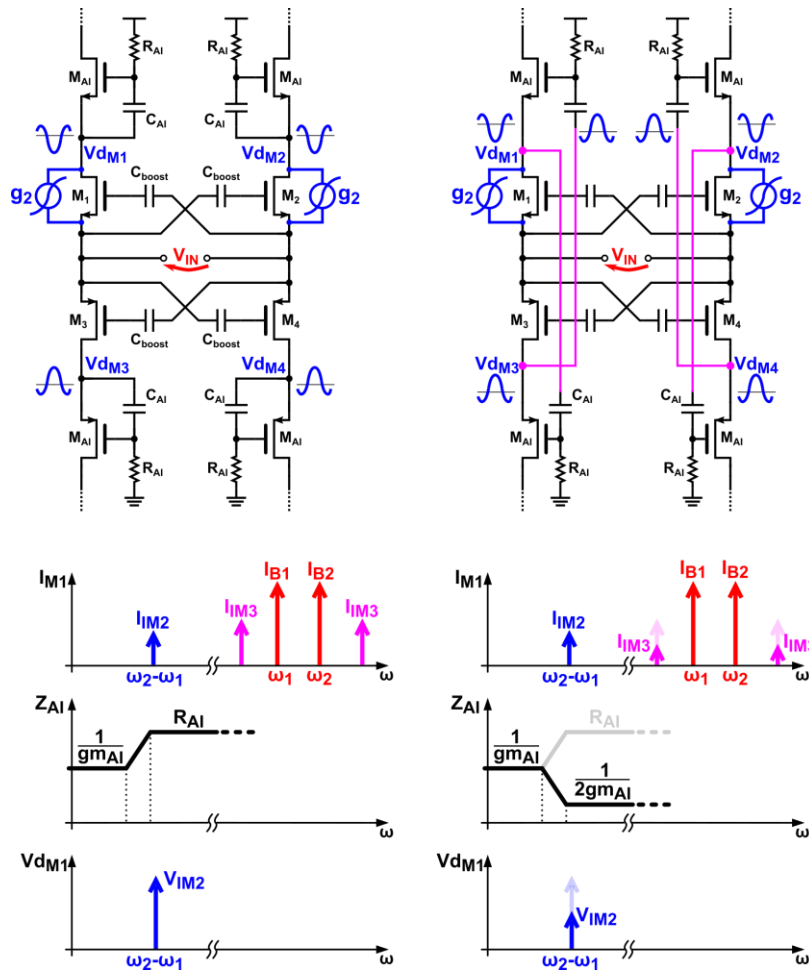


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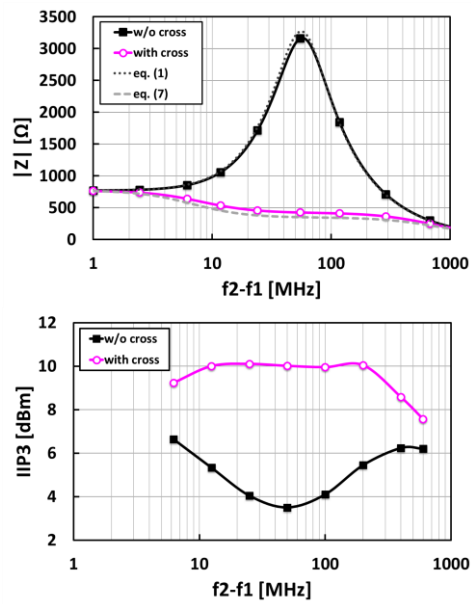


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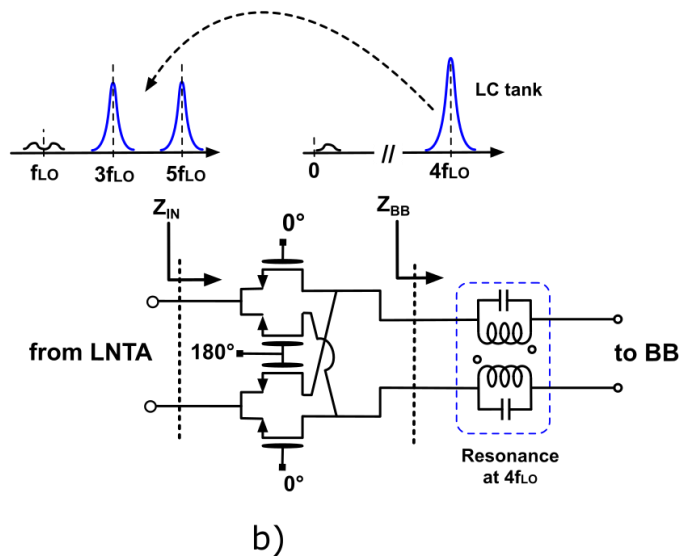
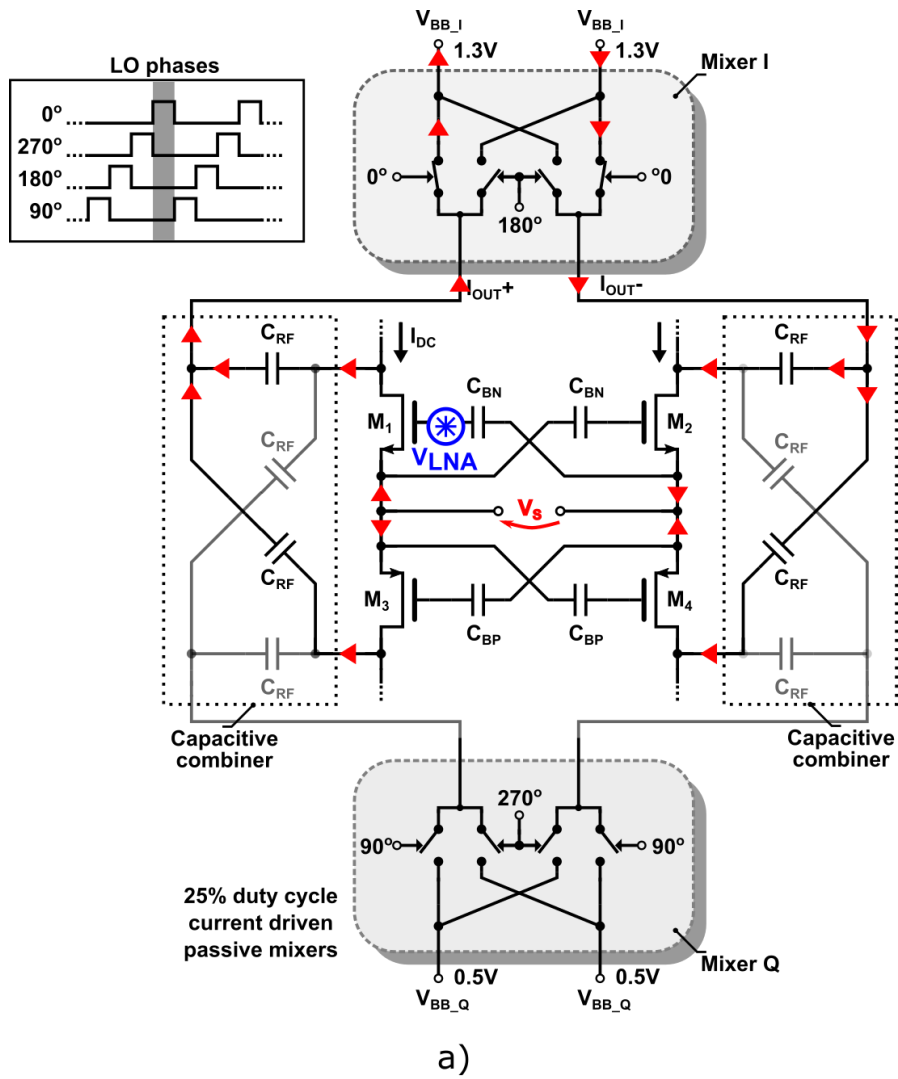


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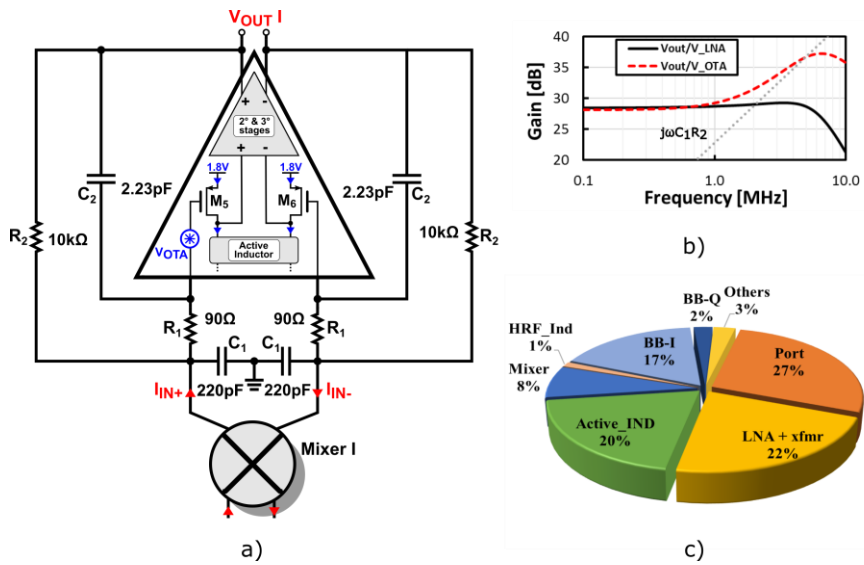


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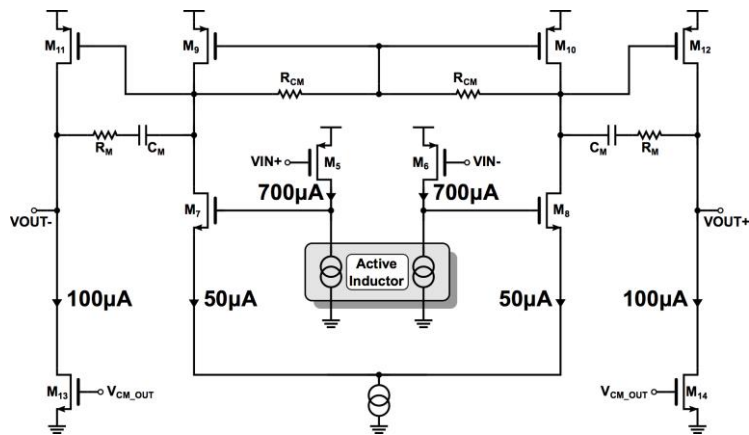


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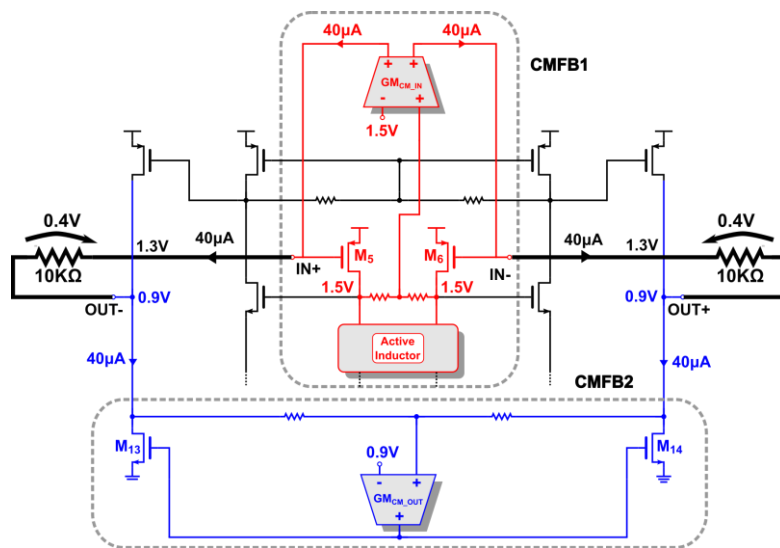


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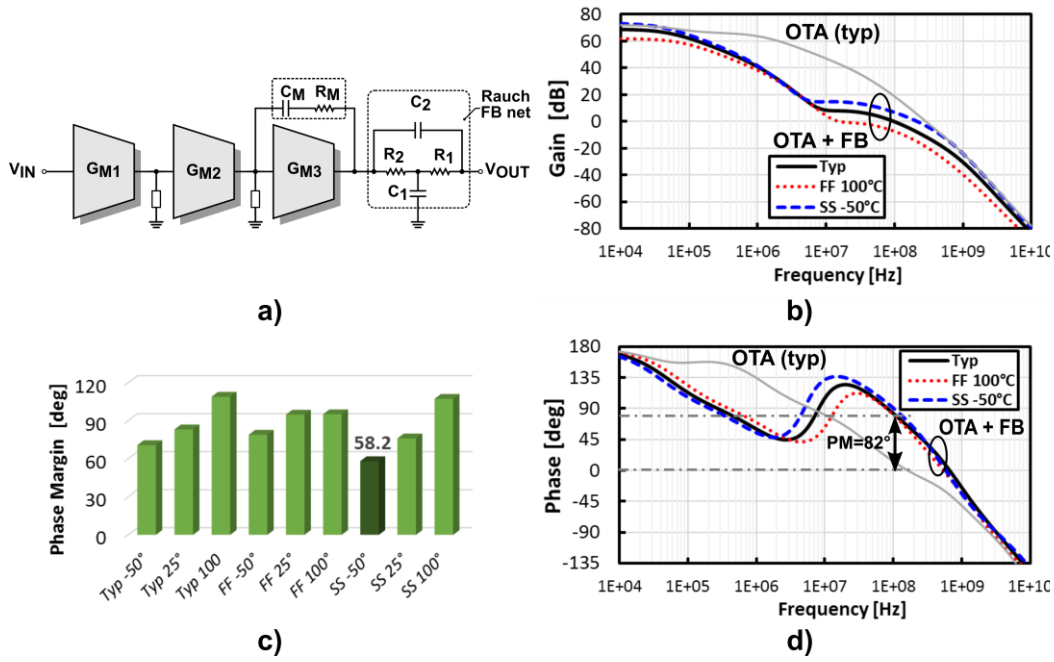


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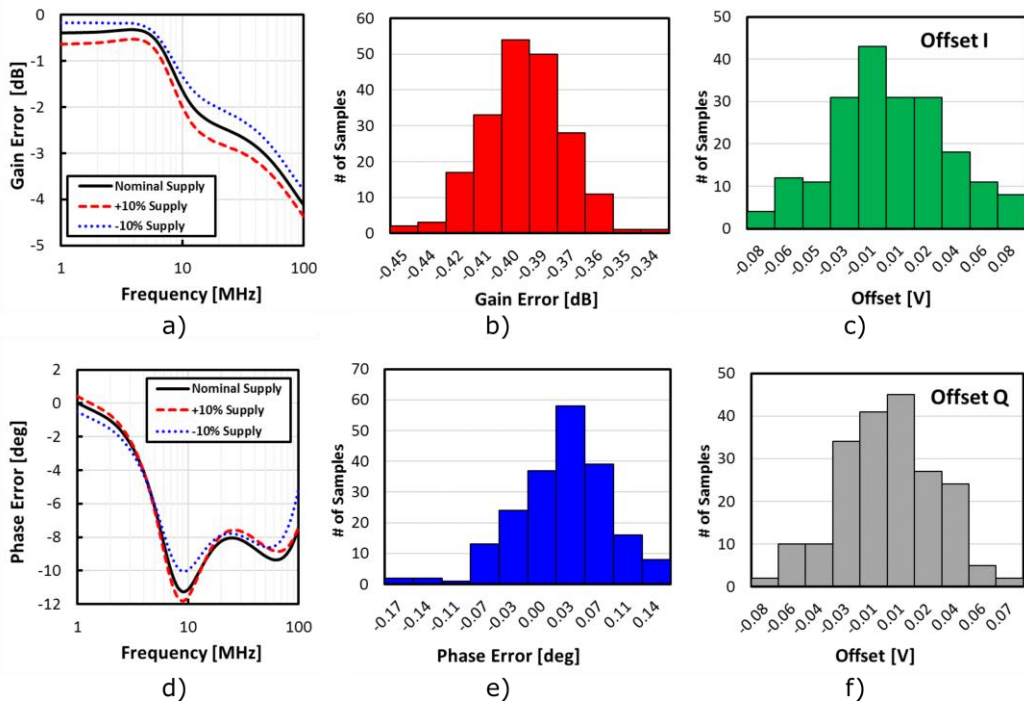


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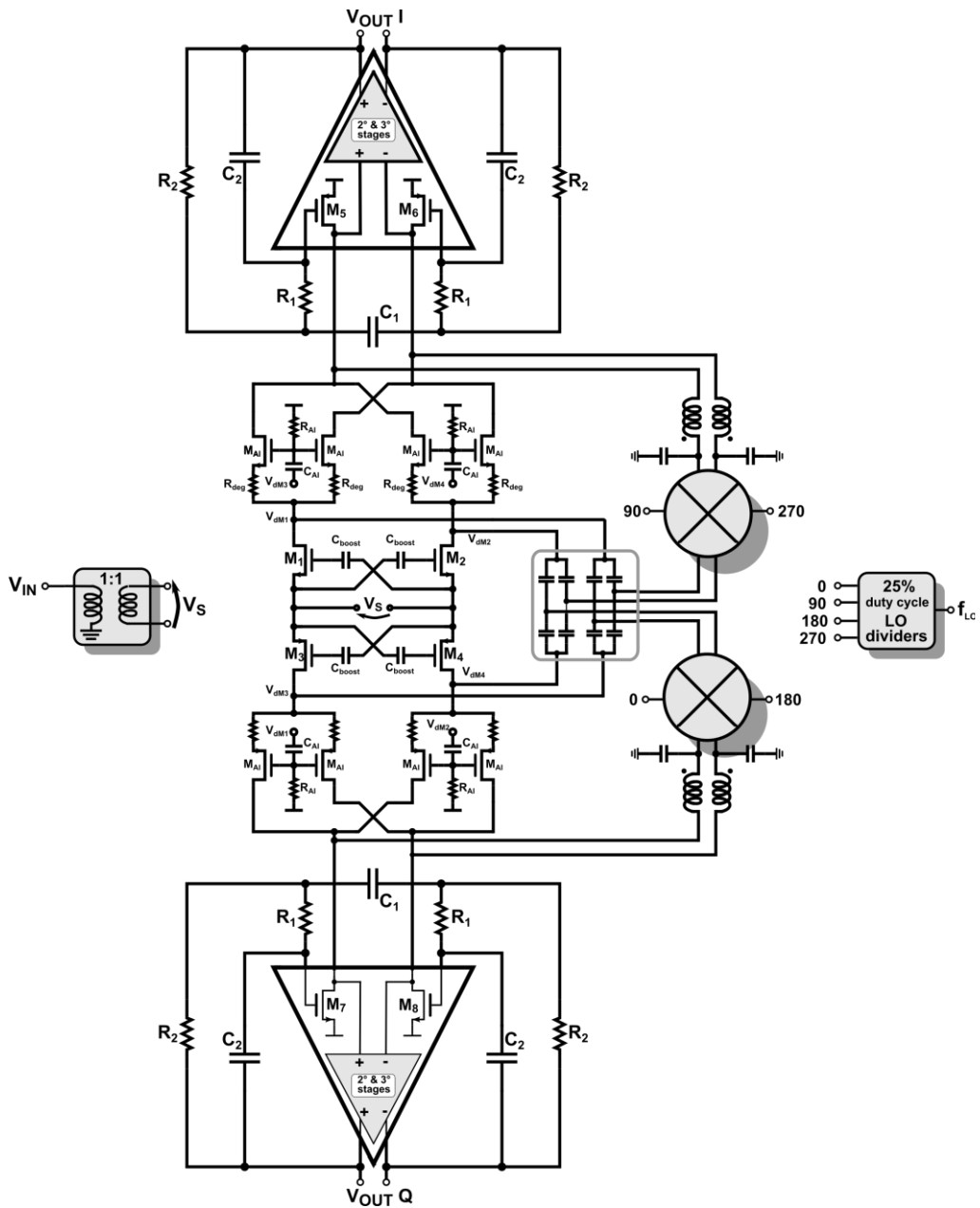


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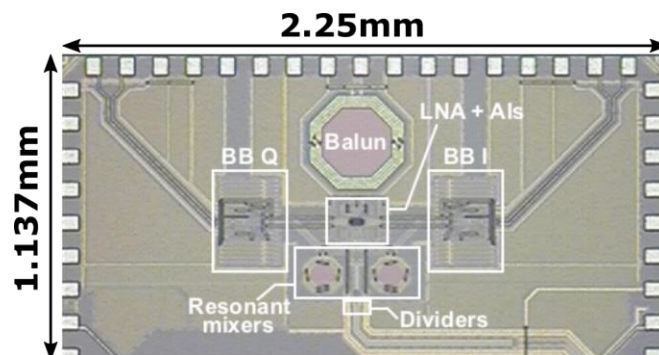
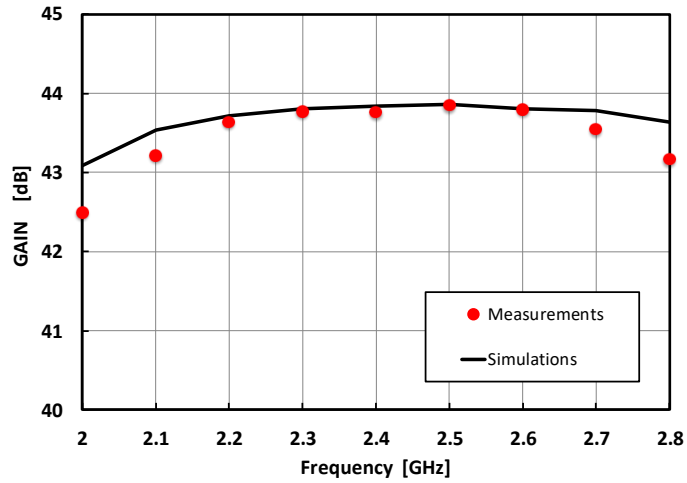
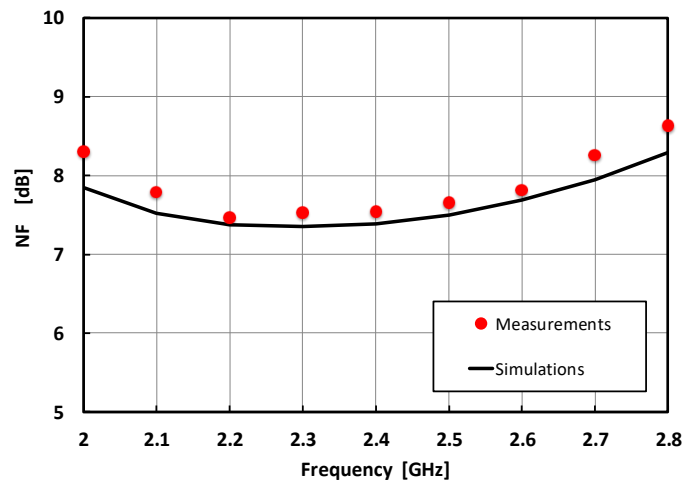


Fig. 16: Chip microphotograph.



(a)



(b)

Fig. 17: Measured and simulated receiver Gain (a) and NF (b).

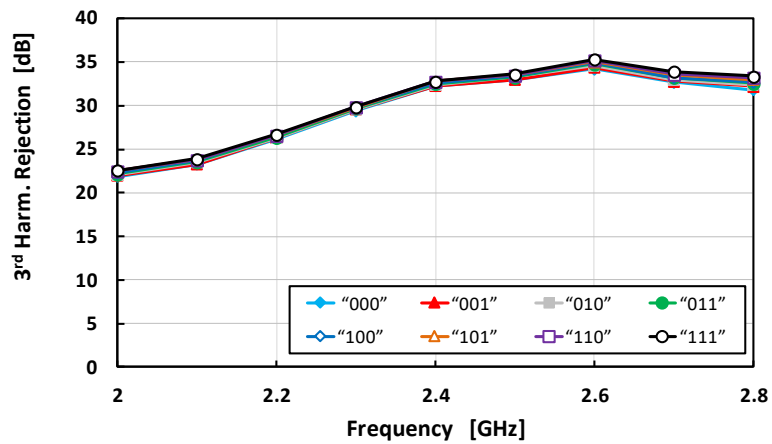


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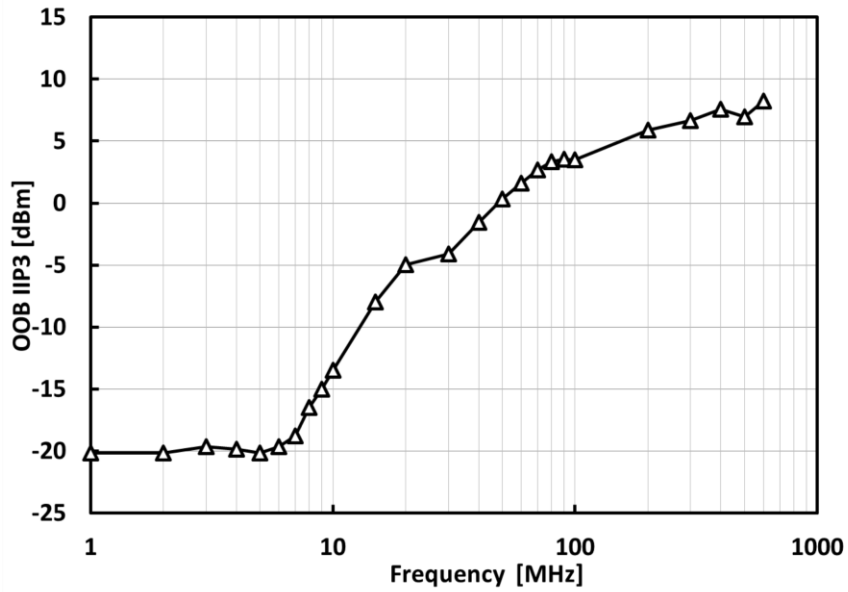


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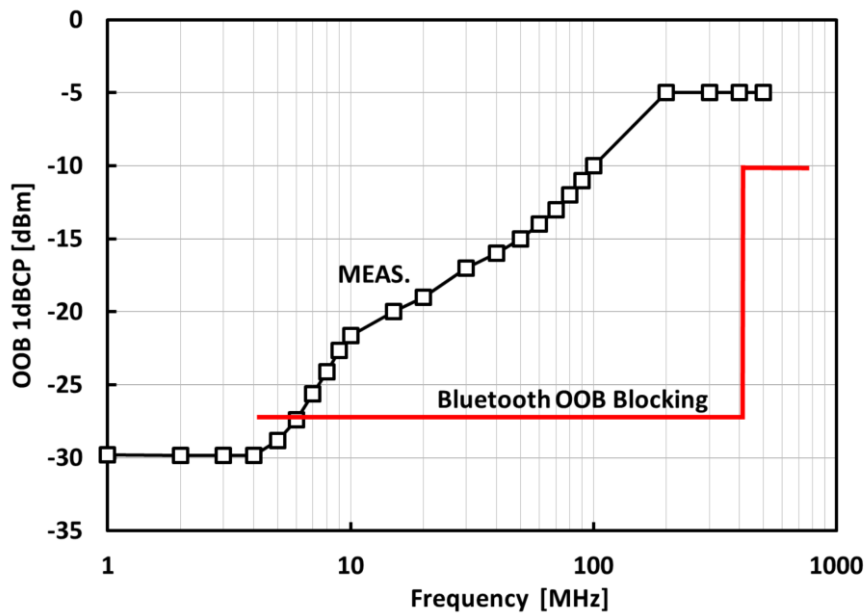


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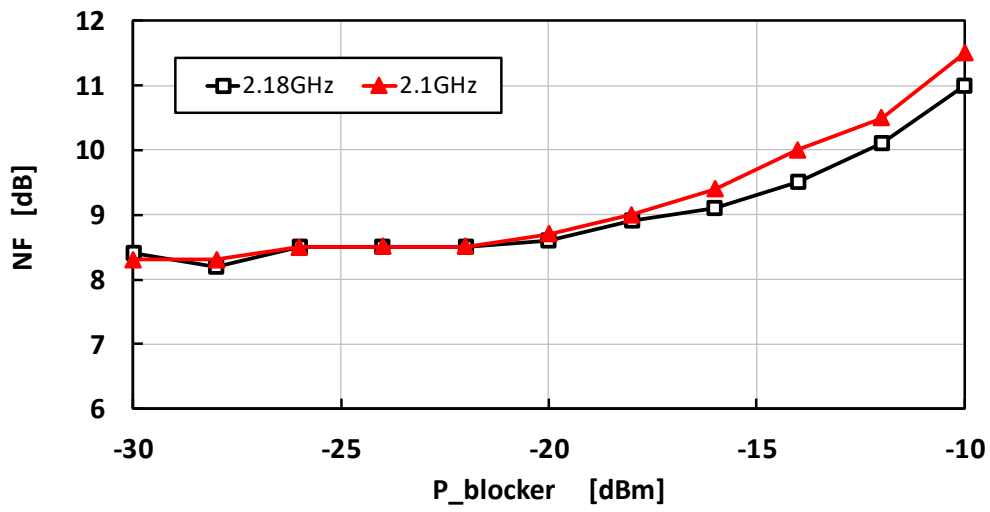


Fig. 21 Receiver NF in presence of an out-of-band blocker as a function of blocker power. LO frequency is 2 GHz, blocker frequency is 2.1 or 2.18 GHz.

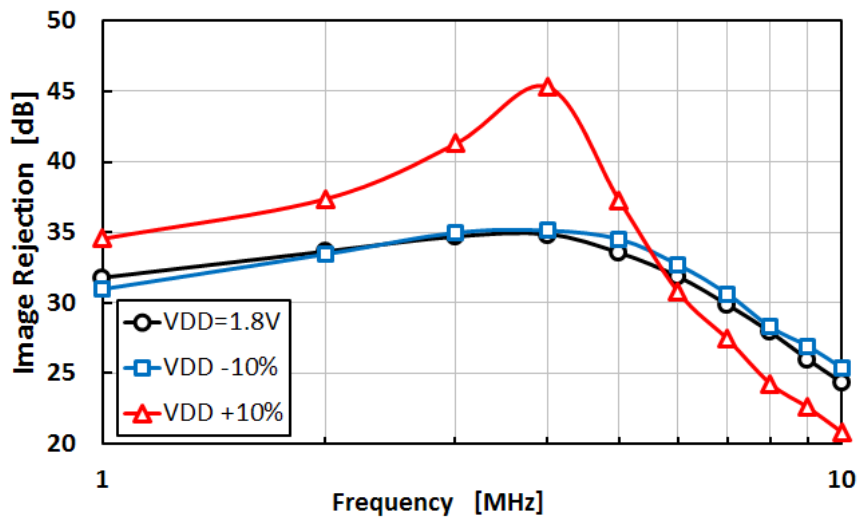


Fig. 22 Measured image rejection ratio vs output frequency.

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TABLE I
PERFORMANCE COMPARISON TABLE

	This work	JSSC 2014 [43]	JETCAS 2014 [16]	RFIC 2014 [36]	RFIC 2012 [37]	JSSC 2015 [29]	ISSCC 2017 [35]	JSSC 2015 [33]	JSSC 2016 [30]
Tech.	28nm	65nm	65nm	130nm	65nm	130nm	28 nm	55nm	65nm
f (GHz)	2.4	2.4	2.6	0.96	0.7-3.2	2.4-2.5	2.4	2.4-2.5	2.4-2.5
Supply (V)	1.8	1.2-0.6	0.85	1.2	1.2	0.8	0.18	1.2 (internal)	0.6/1.1
Current (mA)	2.4	1@0.6V 0.33@1.2V	0.12	2.6	1.5	0.8 ^{c)}	2.1 ^{c)}	1 ^{f)} /8 ^{e)}	1.6@0.6V 1.1@1.1V
TOT Power (mW)	4.3	1.7	0.55	3.1	1.8 / 12 ^{e)}	0.6	0.382	11.2 ^{e)}	2.2 / 5.5 ^{e)}
Gain (dB)	43.4	57	41	59.6	36	55.5	34.5	27 ^{f)}	72
NF (dB)	7.5	8.5	9.6	8.2	7.8 ^{b)}	15.1	11.3	5.5 ^{f)}	6.4
IF (MHz)	1.5	2	0	0.5	0	2	1	1	0.25
BB Filtering	2nd ord. low-pass	1 biquad + 4 complex poles	1 real pole	1 real pole	N/A	2 complex poles	3 real poles	2 complex poles	3rd ord. low-pass
IRR (dB)	31	36	36	30.4	N/A	30.5	26.2	N/A	N/A
LO-RF leak. (dBm)	-70	-61	-69	N/A	N/A	N/A	N/A	N/A	N/A
OOB ^{a)} P -1dB (dBm)	-5	N/A	-15	N/A	-20	N/A	-29	-10 ^{f)} (low-gain)	N/A
OOB ^{a)} IIP3 (dBm)	6	-6	-3	-19	4	-17 ^{d)}	-12.5	N/A	N/A
OOB ^{a)} IIP2 (dBm)	60	N/A	29.5	N/A	24	N/A	N/A	N/A	N/A
Active area (mm ²)	0.4	0.24	0.15	0.12	2.9	0.25	1.65	2.9 ^{g)}	9 ^{h)}

^{a)} with 200MHz frequency offset; ^{b)} at 2.4 GHz. ^{c)} includes VCO current; ^{d)} two-tones at 5 and 8 MHz offsets; ^{e)} complete receiver including PLL; ^{f)} LNA only; ^{g)} transceiver including pads; ^{h)} including pads and digital baseband