A+25 dBm IIP3 1.7-2.1 GHz FDD Receiver Front-End with Integrated Hybrid-Transformer in 28nm CMOS

Ivan Fabiano, Member, IEEE, Matteo Ramella, Member, IEEE, Danilo Manstretta, Member, IEEE, and Rinaldo Castello, Fellow, IEEE

Abstract—A highly-linear receiver front-end with integrated hybrid-transformer (HT) for frequency-division duplexing mobile communications is reported. The HT, implemented with a three-winding coplanar transformer, is used to interface the receiver front-end with the antenna and the power amplifier. The primary is driven at its center tap with the transmitted signal and at one input with the antenna signal, while the other input is connected to an on-chip programmable balancing impedance. The two secondary drive a differential push-pull common-gate LNA. Assuming a perfectly linear hybrid only 45 dB of TX-RX isolation and 35 dB of common-mode rejection are required to meet the intermodulation specs thanks to the +25 dBm receiver IIP3. This would drastically simplify hybrid balancing and adaptation loop. Cascaded noise figure of duplexer, LNA and base-band is below 6.7 dB and TX insertion loss below 4.3 dB from 1.7 to 2.1 GHz. The implemented prototype in 28 nm CMOS has an active area of 0.7 mm² and requires only 26 mW.

Index Terms—Cellular communications, duplexers, FDD, isolation, tunable circuits, SAW-less, blocker tolerant, 3G, LTE, 5G, current-mode, low power, direct conversion.

I. INTRODUCTION

To meet the stringent specifications of frequency-division duplexing (FDD) cellular standards, for each operating band, a highly selective duplexer, based on surface acoustic wave (SAW) filters, connects receiver and transmitter to the shared antenna. A typical duplexer provides more than 50 dB TX-RX isolation (ISO_{TX-RX}) in the transmitter (TX) band and around 45 dB in the receiver (RX) band [1]. To keep up with the demand for mobile data traffic, the number of supported bands has grown tremendously, exceeding 30 for FDD in Rel. 12 [2]. This has a considerable impact of the RF front-end bill of materials (BoM). As features like multiple-input multipleoutput (MIMO) and Carrier Aggregation (CA) are extended to further increase the throughput, the number of passives is bound to increase even further. Recently, we have witnessed attempts at replacing external passives with tunable on-chip ones to reduce board complexity [1][3]-[16]. In [9] two transformers in series combine transmitter and receiver and an RF digital-to-analog converter, in shunt with the receiver, cancels the transmit signal, creating a virtual ground across the receiver. This preserves the transmitter efficiency and provides 50 dB ISO_{TX-RX}. The transmit power is, however, limited to less than 13 dBm and the canceler consumes 60 mW. In [10] an artificial transmission-line realizes selectivity through constructive and destructive interference but ISO_{TX-RX} is only 23 dB. An N-path filter further reduces TX noise injection into the receiver but its effectiveness reduces at high TX power levels due to nonlinear effects, degrading the receiver noise figure (NF). Same-channel full-duplex transceivers face a similar TX-RX isolation problem. In [11][12] an integrated circulator based on N-path filters is proposed as an integrated antenna interface for full-duplex communications achieving 40 dB ISOTX-RX. However, N-path consume considerable power and introduce filters nonlinearities, limiting the maximum TX power to less than 8 dBm. Other works rely on separate antennas for TX and RX to provide some isolation to be complemented with selfinterference cancellation techniques [13]. So far, the solutions that have demonstrated the highest ISO_{TX-RX} combined with high linearity, are based on the hybrid transformer (HT) [1][3]-[8], as shown in Fig. 1. In HT-based transceivers ISO_{TX-} _{RX} is based on impedance-balancing. Multi-band operation is achieved programming an on-chip balancing impedance. This solution has several potential problems. 1) Both TX and RX suffer a theoretical minimum 3 dB loss that reduces TX efficiency and increases RX NF. TX losses can be reduced but with a corresponding increase in RX NF. This is probably the main intrinsic limitation of this approach. However, it can be observed that, even though other approaches do not suffer from this theoretical 6 dB total loss, they face severe practical challenges that limit their performance: e.g. the circulatorbased receiver in [12] has 2-4 dB TX-antenna loss and 6.3 dB NF. 2) While SAW duplexers strongly attenuate out-of-band (OOB) RX blockers, HT front-ends let them pass unattenuated, requiring a very challenging receiver linearity. 3) Un-cancelled TX noise leaks in the RX band, causing desensitization. This has been addressed with dual-frequency HT [6][8] that can provide 50 dB of isolation across both TX and RX bands. 4) The TX leaks through the hybrid as a common mode (CM) signal. No low-noise amplifier (LNA)

Ivan Fabiano was with University of Pavia, Pavia, 27100 Italy. He is now with Silicon Mitus, Pavia, 27100 Italy.

Matteo Ramella was with University of Pavia, Pavia, 27100 Italy. He is now with Advanced Circuit Pursuit, Zurich, Swizterland.

Danilo Manstretta and Rinaldo Castello are with University of Pavia, Pavia, 27100 Italy.



Fig. 1: HT-based front-end with floating RX port.

able to withstand this effect without excessive distortion has been demonstrated. One solution [1] addresses this important issue using differential ports for antenna, transmitter and receiver at the cost of two integrated transformers and an external balun. Alternatively, a different HT configuration, with single-ended LNA, has been proposed in [14] but RX IIP2 is a problem in this case. 5) The linearity of the HT and especially of its balancing impedance is critical. A very linear balancing impedance has been demonstrated in SOI CMOS [7], with an IIP3 of 70 dBm and an isolation level exceeding 50 dB. In general, maintaining high isolation across tens of MHz for the antenna impedance variation that occurs during operation is extremely challenging and typically requires an antenna tuning unit and balancing adaptation rates in the order of 10 ms [21]. Even assuming to achieve 50 dB ISO_{TX-RX}, the linearity required to the LNA to satisfy the specs remains much higher than what has been reported so far. In this work we propose a high linearity receiver that could meet cellular blocking requirements with less than 45 dB ISOTX-RX assuming a very linear hybrid [7] was available. Excessive distortion in either the measurement set up or the balancing impedance allows proving the above statement only for two out of three intermodulation reference scenarios. Nonetheless, based on the results of [7],[1] we are confident that our solution has the potential to fulfill all the specs for FDD SAWless transceivers. This is achieved revisiting the common-gate (CG) LNA in [19] and exploiting the HT to get an improved topology that partially breaks the trade-off between noise and IIP3 [16]. Furthermore, the proposed LNA is able to withstand a much higher TX common mode leakage (CML) through the hybrid compared to previous implementations. The paper is organized as follows: section II discusses system design considerations for cellular receivers using integrated duplexers taking 3G standard as a reference. Section III presents the proposed LNA together with the integrated duplexer (based on a hybrid transformer) and reports a detailed analysis of noise and IIP3. Section IV describes the design of the overall frontend in 28 nm CMOS and reports the experimental results. Section V draws the conclusions.

II. HYBRID TRANSFORMER AND LNA DESIGN

An HT-based duplexer, first proposed in [3], replaces the external duplexer with an on-chip hybrid transformer that decouples TX from RX through impedance balancing instead of filtering. In the first implementation a narrow isolation

bandwidth was achieved. To overcome this problem a better solution was proposed in [4] (Fig. 1). The PA drives the center tap of the primary winding of a transformer, antenna and tunable impedance (Z_{BAL}) are connected to the primary terminals, while the differential LNA is connected to the secondary. When the antenna impedance equals Z_{BAL} , the TX and the differential input of the LNA are perfectly decoupled. Although the circuit is inherently wideband, the sharp variation of the antenna impedance with frequency limits the ISO_{TX-RX} bandwidth [6]. Moreover, due to capacitive coupling between transformer windings, a large TX CML reaches the LNA input. In the LNA, the combination of a CML at frequency f1 and a differential-mode (DM) signal like an OOB RX blocker at frequency f2 generates differential 3rd order intermodulation products (IM3) at 2f₁-f₂ and CM IM3 at 2f₂-f₁. For a pseudo-differential LNA the amount of IM3 generated by either two DM signals or by a CM and a DM signal is the same. For a balanced LNA, this is not the case and a CM IIP3 (IIP3_{CM}) and a DM IIP3 (IIP3_{DM}) should be defined. When the CML is higher than the DM leakage, the latter due to residual hybrid unbalance, the IIP3_{CM} may become the limiting factor. This issue was addressed in [1] using differential ports for antenna, transmitter and receiver. The LNA IIP3 is relaxed because the CML is partially cancelled by the fully differential topology. This comes at the cost of two integrated transformers (larger area) and an external balun, increasing cost, NF and/or losses. Because of this, in our receiver the configuration in Fig. 1 is adopted and its main drawbacks are tackled as follows. First, a fully-differential LNA with large CM immunity is adopted to drastically reduce the intermodulation between CML and DM blockers. Second, the transformer is carefully optimized to reduce its capacitive coupling between primary and secondary. Third, exploiting the fact that in an HT the LNA does not need to be powermatched, a push-pull common gate LNA whose input impedance is much lower than its driving impedance is used. For the same NF and current this gives both 20 dB more IIP3 than a common-source LNA and a lower trans-conductance thereby relaxing the required baseband linearity at the cost of some extra noise.

A. Linearity Requirements for FDD

In FDD systems, due to finite TX-RX isolation, the TX signal leakage intermodulates with blockers, leading to challenging receiver IIP3 (IIP3_{RX}) requirements [20][22]. The three reference scenarios that cause intermodulation, i.e Half-Duplex-Spaced (HDS), Full-Duplex-Spaced (FDS) and Adjacent Channel (AC) are sketched in Fig. 2. The three scenarios are defined by the relative position in frequency between the TX leakage and the RX blocker. In the HDS case the blocker is located half-way between the RX band and the TX band, so the IM3 that falls in-band is the one at frequency 2 $f_{BLK} - f_{TX}$. In the FDS case the blocker is located on the other side of the TX band with respect to the RX band. In this case the IM3 that falls in-band is the one at frequency 2 $f_{TX} - f_{BLK}$. In the AC case the RX blocker is located in the channel adjacent to the RX band on the side of the TX leakage. Here



Fig. 2: Blocker and TX-leakage intermodulation scenarios: half-duplex spaced, full-duplex-spaced and adjacent-channel.

the in-band distortion term is due to cross modulation between the modulated TX leakage and CW RX blocker. For the three cases, to keep IM3 below the RX noise floor for blocking tests, e.g. in 3G -96 dBm, the required antenna-referred IIP3 are IIP3_{HDS} > $(P_{TX} + 2 P_B + 96 \text{ dBm}) / 2$, IIP3_{FDS} > $(2 P_{TX} + P_B)$ $+96 \text{ dBm}) / 2 \text{ and IIP3}_{AC} > (2 (P_{TX} - 3) + P_{JAM} + 96 \text{ dBm}) / 2$ respectively. In the above equations P_{TX}, P_B and P_{JAM} are TX, blocker and jammer power in dBm referred at the antenna. As an example, with 23 dBm P_{TX}, -15 dBm P_{BLK}, and -43 dBm P_{JAM} , IIP3_{HDS} > 44.5 dBm, IIP3_{FDS} > 63.5 dBm and IIP3_{AC} > 46.5 dBm. A typical SAW-based duplexer reduces P_{TX} and P_B by nearly 50 dB [1], drastically relaxing receiver IIP3_{RX}, but leaves PJAM almost the same. This makes AC the most critical scenario, which sets the required IIP3_{RX} to -3.5 dBm. In HTs the blocker sees hardly any filtering, hence the required IIP3_{RX} in the three scenarios becomes: IIP3_{HDS} – ISO_{TX-RX} /2, IIP3_{FDS} - ISO_{TX-RX} and IIP3_{AC} - ISO_{TX-RX}. Even though up to 70 dB ISO_{TX-RX} 70 dB were reported over a very narrow band, for a realistic antenna model, the achievable isolation across just a few MHz is below 50 dB [6]. With the blocker passing unfiltered and 50 dB isolation, the most stringent IIP3_{RX} requirement is set by the HDS scenario at 19.5 dBm. On the other hand, in the FDS and AC scenarios, the TX CML could become the limiting factor. Considering a TX CML of -40 dB [1], the FDS scenario sets the most stringent IIP3_{RX-CM} requirement at IIP3_{FDS} – $ISO_{CM} = 23.5$ dBm. The TX leakage sets the requirements for the receiver second-order intercept point: IIP2 > $2(P_{TX} - ISO_{TX-RX}) + 96$ dBm. With 50 dB differential-mode isolation and 23 dBm PTX (-27 dBm TX leakage), the minimum receiver IIP2 is 42 dBm. This is less challenging to achieve with respect to the IIP3 requirements. A differential LNA helps attenuating TX CML, which is not the main limiting factor for IIP2.

B. Hybrid-LNA Co-Design

An ideal four-port HT can be designed to achieve simultaneously power match at each port and bi-conjugacy: i.e. the power entering from any of the four ports splits between two ports and no power is delivered to the fourth (conjugated) one [5]. In the context of an FDD front-end, the conjugated ports are transmitter / receiver and balancing / antenna. The power from the transmitter is split between



Fig. 3: Hybrid auto-transformer ideal operation: a) TX mode; RX mode superposition analysis: b) differential and c) common-mode excitation.

antenna and balancing ports and the power from the antenna is split between TX and RX ports. The conditions necessary to achieve these properties can be easily derived for the symmetrical hybrid auto-transformer of Fig. 3 with 1:1 turns ratio and antenna impedance equal to R_s (nominally 50 Ω). In transmit mode (Fig. 3.a), the current entering the TX port is split between the antenna impedance R_S and the balancing impedance R_{BAL} . In the balanced condition, $R_{BAL} = R_S$, the input impedance at the TX port is Rs/2, the voltages at ANT and BAL ports are equal and the RX port is isolated from TX. In receive mode, the antenna signal can be represented as the superposition of equal DM and CM signals applied at the antenna and balancing ports (Fig. 3.b-c). For the DM signal the RX input current is $I_{RX} = 2 V_S / (2 R_S + R_{RX})$ and $V_{ANT,DF} =$ $V_S R_{RX} / (2 R_S + R_{RX})$. For the CM signal, the current at the RX port is zero and $V_{ANT,CM} = V_{TX} = V_S R_{TX} / (R_S + 2 R_{TX})$. Hence the Norton equivalent at the RX port is a current generator $I_S=V_S/2R_S$ with shunt impedance $2R_S$ and is independent of R_{TX}. The antenna input impedance (computed from $V_{ANT} = V_{ANT,DF} + V_{ANT,CM}$ is :

$$Z_{ANT} = \frac{R_{S} \left(R_{RX} + 4R_{TX} \right) + 4R_{TX} R_{RX}}{4R_{S} + R_{RX} + 4R_{TX}}$$
(1)

and, from superposition, the voltage gain at BAL is:

$$\frac{V_{BAL}}{V_S} = \frac{R_{TX}}{R_S + 2R_{TX}} - \frac{R_{RX}}{4R_S + 2R_{RX}}$$
(2)

From (1) it can be seen that the impedance seen at the antenna port is dependent on both R_{RX} and R_{TX} , while (2) gives the condition for ANT-BAL isolation. In summary, to achieve bi-conjugacy and power matching at all ports the conditions are: 1) same balancing and antenna impedance to isolate RX from TX; 2) TX driving impedance equal to R_{RX}/4 to isolate BAL from ANT port; 3) R_{RX} equal to 2R_s to ensure power matching. In actual HT designs the major concern from the receiver point of view is the TX-RX isolation, hence the first condition is always fulfilled. The second condition may be violated without major consequences since the largest signal at the BAL port, which sets the linearity of the balancing impedance, is the TX signal, not the received signal. The third condition is also generally violated in favor of LNA noise optimization. Previous HT used a CS LNA, whose capacitive input impedance can be resonated out by the HT



Fig. 4 Circuit schematic of the proposed XCG LNA integrated with the hybrid transformer.

winding inductance, resulting in $R_{RX} >> R_S$. This boosts the LNA input voltage ($V_{RX} \approx 2 V_S$) and reduces noise. ANT port matching depends on R_{TX} : $Z_{ANT} \approx R_S + 4 R_{TX}$ or 6 dB return loss (RL) for TX port matched to $R_S / 2$. This is acceptable since no SAW filters that require 50 Ω termination are used [1][4]. In this work, a low-input impedance common-gate (CG) LNA is proposed to simultaneously improve noise and linearity. With low $R_{RX} I_{RX} \approx V_S / R_S$. With $R_{RX} \approx R_S/4$ and the TX port matched to $R_S/2 Z_{ANT} \approx R_S ||R_{TX}$ with an RL of 8.2 dB.

III. LOW-NOISE FRONT-END DESIGN

CG LNAs are good candidates to achieve simultaneously low noise, high linearity and low current consumption. Moreover, push-pull topologies allow to nearly halve the required current for a given transconductance while also largely improving compression. In [19] a push-pull CG LNA with transformer gate-boosting was presented. A four-winding transformer (one primary and three secondaries) was used to perform single-ended to differential conversion, drive the two (NMOS and PMOS) CG inputs and, via the third secondary, the gate of the input transistors with an amplified signal, lowering noise. In principle the LNA input transformer could be merged with the HT. However, the design of such transformer is quite challenging, potentially leading to higher than expected noise, as shown in [19]. The LNA proposed in this work consists of a push-pull CG amplifier driven by an on-chip three-winding HT. The NMOS and PMOS LNA input transistors are driven at both gate and source by the two secondaries of the hybrid using feed-forward capacitors [23][24], as shown in Fig. 4. Capacitive cross-coupling not only improves noise but, even more importantly, it strongly reduces the IM3 terms due to the CM TX leakage that was the main limitation in earlier single-ended HTs. Furthermore, contrary to what was done in [19], here the LNA is not power matched. Removing this design constraint enables further performance improvements. When the CG input impedance is much smaller than its driving impedance, transistors noise and distortion are recirculated, as in a cascode, improving both NF and IIP3. In balancing condition (Z_{BAL}≈Z_{ANT}=R_S) the LNA driving impedance is 2Rs times n², where n is the transformer turns ratio. A much smaller LNA input impedance can be obtained with a moderate bias current thanks to the feedforward capacitors and the complementary topology. In this way, as shown below, excellent noise and IIP3 are achieved.

A. Noise Analysis

For simplicity in the noise analysis, we consider an LNA consisting of a single cross-coupled pair and an ideal 1:n transformer with one secondary. The CG cross-coupled (XCG) LNA driving impedance is equal to $n^2 (R_{ANT} + R_{BAL})$, while its input impedance is $1/g_m$ (both taken differentially). As discussed in Section II.B, adequate matching at the hybrid antenna port does not require LNA power matching. For a balanced hybrid ($R_{BAL} = R_{ANT} = R_s$) and XCG LNA the transconductance gain from the antenna port to the LNA output and the noise factor are given by:

$$G_{m,XCG} = \frac{2ng_m}{1+2n^2g_mR_s}$$
(3.a)

$$F_{XCG} = 2 + \frac{\gamma}{2n^2 g_m R_s}$$
(3.b)

where the factor 2 in (3.b) is due to the balancing impedance and the second term is due to the transistors thermal noise ¹. When $2n^2R_S >> 1/g_m$ the transconductance gain is $\approx 1/(nR_s)$ and transistors noise is highly suppressed, as in a cascode. Increasing n and/or g_m increases the LNA impedance mismatch, which reduces the transistor noise thanks to more recirculation. It is instructive to compare these results with the ones for a HT followed by a differential CS amplifier. In the latter, the LNA input impedance is much higher than R_s and its input voltage is given by the antenna signal boosted by n, resulting in the following expressions:

$$G_{m,CS} \cong ng_m$$
 (4.a)

$$F_{cs} = 2 + \frac{2\gamma}{n^2 g_m R_s} \tag{4.b}$$

In both cases, to achieve a low NF a large gm and/or a large n must be used. However, for the same current consumption (i.e. same g_m) the transistor noise contribution in the CS LNA is four times higher than in the XCG LNA. This fact, together with the improved linearity is a strong motivation for the use of a XCG configuration. Fig. 5 reports the simulated and calculated NF of an ideal HT followed by either a CS or a XCG LNA as a function of both the transformer turns ratio n (Fig. 5.b) and of the device transconductance (Fig. 5.a). To achieve a NF of 4 dB using n=1, a gm of 80 mS is required for the CS compared with 20 mS for the XCG. Similarly, for a gm of 36 mS, a NF of 4 dB requires n=1.4 for the CS and n=0.7 for the XCG. A large n helps to achieve low noise with moderate power consumption in both cases. However, as it will be explained below, n has completely different effects on the linearity of CS and XCG LNAs. The NF given above,

¹ Notice that in power matching condition $g_m=1/(n^2 2R_{ANT})$ gives $F=2+\gamma$ that is exactly twice the noise factor of a simple cross-coupled CG LNA. Similarly, the 3 dB power loss of the hybrid degrades F_{CS} by a factor of 2.



Fig. 5. Simulated (symbols) and calculated (dashed lines) NF of HT front-end with XCG and CS LNAs: a) NF versus input device gm (an ideal transformer with turns ratio of 1 is used); b) NF versus transformer turns ratio (n) for an input device with gm = 36 mS.

 TABLE I

 CONTRIBUTIONS TO THE LNA NOISE FACTOR

BAL + ANT	Hybrid Transformer Losses	Transistors	TOT F=2.92
68%	22%	10%	100%

however, neglects transformer losses. Lumping all the transformer losses into a single resistor R_P in parallel with its primary, the driving impedance becomes $n^2 (2R_{ANT} \parallel R_P)$ and the noise factor (F):

$$F = 2 + \frac{4R_s}{R_p} + \frac{\gamma}{2n^2 g_m R_s} \left(\frac{2R_s + R_p}{R_p}\right)^2 \tag{5}$$

where the factor 2 is due to the balancing impedance, the second term represents transformer losses and the last transistors noise. When the complementary (p-n) structure is used, (5) remains valid with $g_m=g_{m,NMOS}+g_{m,PMOS}$. This gives a factor of 2 noise reduction for the same power consumption. With the 1:1:1 transformer used in this design and gm = 70 mS (6 mA total current), the simulated NF is 4.7 dB, with the main contributions listed in Table I. NF with noise-less transformer would be 1.1 dB lower. Further improvements may be possible by optimizing the transformer.

B. High Linearity Front-End Design

OOB IIP3 is very critical in a SAW-less receiver due to the strong OOB blockers that reach its input unfiltered. After the

mixer, large capacitors provide a low-impedance path to OOB blockers, reducing the intermodulation generated by nonlinearities within the mixer itself and in the TIA. As a result, the main OOB IIP3 limitation comes from the LNA. To complete the comparison between the HT followed by either a pseudo-differential CS amplifier or a XCG amplifier, we analyze the IIP3. Detailed calculations are reported in the Appendix. In the first case the IIP3 is that of the CS amplifier divided by the voltage amplification in front of it (n).

$$IIP3_{CS} = \sqrt{\frac{4g_m}{3n^2g_{m3}}} \tag{6}$$

where g_{m3} is the transconductance 3rd order nonlinear coefficient. For a given V_{GS}, IIP3_{CS} is independent from the bias current and it degrades if a step-up transformer (n>1) is used to improve noise. Using techniques such as derivative superposition the IIP3 of a CS amplifier can be significantly improved (e.g. 16 dBm in [26]). However, sensitivity to process and bias variations drastically reduces the IIP3 that can be achieved in practice (between 0 dBm and 6 dBm depending on two-tone frequency spacing in [26]). The IIP3 of a XCG amplifier is now considered. First, the IIP3 of a simple CG amplifier is degraded by the fact that IM3 is contributed by both transconductance 3rd order non-linearity as well as 2nd order non-linearity, through a mechanism referred to as "second-order interaction" in [24]. Cross-coupling the gates eliminates second-order interaction [24]. However, the gatesource voltage swing of the input devices is doubled and, in matched condition, the IIP3 is only slightly higher than that of a CS amplifier. On the other hand, when the LNA input impedance is made much smaller that its driving impedance, IIP3 is greatly enhanced. This is because the voltage swing across the active devices is reduced and the nonlinearity is mostly recirculated inside the transistor, as shown by the analysis in the Appendix. The IIP3 of a hybrid transformer followed by a XCG amplifier is:

$$IIP3_{XCG} = \sqrt{\frac{4g_m}{3n^2g_{m3}}} \left(1 + 2n^2g_mR_s\right)^{3/2}$$
(7)

Fig. 6 reports simulated IIP3 for a loss-less symmetric HT followed by either a CS or a XCG LNA versus the input device gm for n=1 (Fig. 6.a) and versus n for an input device gm = 36 mS (Fig. 6.b). For a CS amplifier, IIP3 is essentially independent of gm and it degrades linearly as n is increased due to input voltage boosting. For a XCG amplifier instead, IIP3 improves increasing either g_m or n. When the complementary (p-n) structure is considered the expression in (7) remains valid provided that $g_m = g_{m,NMOS}+g_{m,PMOS}$ and $g_{m3} = g_{m3,NMOS}+g_{m3,PMOS}$ are used, giving nearly the same IIP3 at half power consumption.

C. Linearity and Common-Mode Rejection

As explained before, in the FDS scenario the intermodulation between CML and an OOB RX blocker creates in-band differential intermodulation products. In an HT with CS LNA, (where $IIP3_{CM} = IIP3_{DM} = IIP3_{RX}$) the



Fig. 6. Linearity of IDT front-end with CG and common-source LNAs: a) IIP3 versus input device transconductance (an ideal transformer with turn ratio of 1 is used); b) IIP3 versus transformer turn ratio for an input device with gm = 36 mS. Dots are simulated values, lines represented calculations based on (4) and (5).

antenna-referred IIP3 due to this mechanism is given by IIP3_{RX} plus by the hybrid common-mode rejection ratio (CMRR) in dB where CMRR is the ratio between the DM and CM voltage gain. CM gain is determined by the primary-tosecondary capacitive coupling and by the secondary CM inductance (L_{par} in Fig. 7). The latter, is lower than the DM inductance since the mutual coupling between secondary windings subtracts from the auto-inductance instead of adding as for differential signals. Nonetheless, CML is typically the limiting factor in receiver intermodulation as opposed to HT unbalance [1]. Moreover, if the secondary inductance and the turns ratio n are increased together, the TX CML increases, e.g. 1:3 turns ratio was used in [1], giving a CMRR of -37 dB. In an HT with a XCG LNA, the feed-forward capacitors make the input devices gate-source voltage nearly zero for CM input This strongly signals (Fig. 7.b). suppresses this intermodulation mechanism. IIP3_{CM} can be computed from IIP3_{DM} in (7) considering that the differential signal at the LNA input is V_S $n/(1 + 2n^2g_mR_s)$ and the CM signal at the secondary V_{CM} is further suppressed by a factor A_{C-FFW} thanks to the LNA feedforward capacitors. As shown in the Appendix, the antenna-referred IIP3 is given by:

$$IIP3_{ANT,CM} = CMRR \cdot A_{C-FFW} \sqrt{\frac{4g_m}{3g_{m3}}} \left(1 + 2n^2 g_m R_S\right)^{1/2}$$
(8)

The simulated and calculated IIPANT,CM for a perfectly



Fig. 7. Intermodulation between CM TX leakage and RX blocker in IDT front-end with CG and common-source LNAs: a) CM leakage with common-source LNA; b) CM leakage with cross-coupled CG LNA; c) IIP3_{ANT,CM} versus transformer turns ratio for an input device with gm = 70 mS and a TX leakage of -43 dB. Dots are simulated values, lines represent calculations based on (4)-(6) with A_{C-FFW} =18

balanced hybrid is reported in Fig. 7.c versus n and for a fixed TX CML of -37 dB. For a CS LNA the IIP3 is constant at 42 dBm, independent of n, while for the XCG IIP3 is 68 dBm for n=1, used in this design, exceeding the 63 dBm required in FD, which is the worst case scenario from this point of view.

IV. IC DESIGN

The schematic of the complete chip prototype [16] is shown in Fig. 8. The LNA drives two (I/Q) 25% duty cycle passive mixers followed by second order Rauch filters. The mixer is AC coupled to the LNA with 2 pF series capacitors. A parallel LC resonating at the 4th harmonic of the LO is placed in series with the mixer on its base band side. This creates a high impedance at the 3rd and 5th harmonic of the LO on the RF side of the mixer, avoiding noise folding [19]. Care was taken to minimize parasitic capacitance at the LNA output to maximize the baseband equivalent driving resistance, that has a dominant effect on baseband noise. The Rauch filter strongly attenuates the out of band blockers with low power consumption thanks to the use of a single Op-Amp. The filter bandwidth was set to 3 MHz in accordance with the 3.84 MHz channel bandwidth in 3G, that was taken as a reference for this work. To minimize noise and maximize linearity for a given bias current, the Op-Amp uses a complementary p-n input differential pair and a push-pull output stage. More details on the OPAMP topology can be found in [19], where a similar implementation in 40 nm CMOS is reported. The achieved input referred IIP3 of the baseband increases with the distance between the interferers and the filter band edge. The base band distortion becomes negligible compared with the front-end



distortion for a frequency offset of the lower interferer higher than 50 MHz. Within the front-end, third order distortion is dominated by the LNA independent of the frequency offset. Simulation shows that he third order distortion of the passive mixer, thanks to the low impedance at its output provided by the Rauch filter, is always negligible. The base-band contributes less than 0.3 dB to the overall receiver NF. RX to TX isolation relies on balancing the hybrid by making the programmable balance impedance (Z_{BAL}) exactly equal to the antenna impedance (ZANT). As a consequence, both the real and imaginary part of Z_{BAL} have to be programmable with sufficient resolution over a wide range of values. A parallel array of switched resistors at the BAL port and two switchable capacitors at the ANT and BAL ports are used to achieve balancing [5]. The two capacitor arrays allow to compensate both for capacitive as well as inductive antenna impedances. To reduce voltage swing across the switches and to improve linearity a stack of 8 series transistors is used. Drain/source-tobulk parasitic capacitors generate uneven voltage distribution across the stack, making the technique only partially effective. To cope with this effect, minimum channel length 28 nm thin oxide NMOS transistors with floating bulk and deep N-wells are used. Moreover, fixed resistors/capacitors in parallel with the switches ensure that each switch has a gate-source/drain AC voltage swing of just 1/16 of the stack input voltage. A fixed resistance/capacitance in series with the stack provides another 2x attenuation at the price of a reduced tuning. The BAL resistance can be varied between 35 and 70 Ω and the ANT/BAL capacitances between 200 and 400 fF. This accomodates variations in the 50 Ω antenna resistance by +/-35%, while it compensates for a parallel reactive impedance of +/- 400 Ω at 2 GHz. The covered impedance range is similar to earlier implementations [5] but, especially the reactive part, may be considered too narrow for reliable practical applications. With the chosen switch configuration, where 8 unit capacitors are used in series, increasing the capacitor array is costly in terms of area. A possible way to reduce the array size by using fewer elements in series is to toggle the bulk terminal of the NMOS switch in the opposite direction of the gate [7] instead of keeping it at a constant value. This increases the voltage swing required to turn ON a device biased in the OFF state and may allow to use fewer series elements in the stack (four were used in [7] that however was



Fig. 9. Hybrid transformer design: a) Layout; b) metal cross-section; c) simplified equivalent circuit

implemented in an FDSOI technology). The HT design optimization is important part of this work [30]. The hybrid should have the maximum k and Q while minimizing capacitive coupling between windings. Stacked transformers have high k but low Q if only one thick metal is available. Coplanar topologies reduce capacitive coupling and maximize the Q of both primary and secondary but have a poor k. Using several metal layers in parallel increases Q but also capacitive coupling. Considering the above trade-offs, the coplanar three coils transformer with n = 1 was implemented as in Fig. 9. The technology features a 3.4 µm thick copper top metal (M6) and an aluminum 1.4 µm thick redistribution layer (AP). The secondary windings (outer and inner rings) use parallel AP/M6 layers, while the primary uses only the M6 layer. An equivalent circuit of the hybrid is shown in Fig. 9.c. The simulated differential inductance and quality factor of the three HT windings and the effective coupling factors amongst them are reported in Fig. 10.a-d. At 2 GHz, the effective series loss resistance for the primary (middle coil), secondary 1 (inner coil) and secondary 2 (outer coil) are 3.2 Ω , 2.2 Ω and 3.1 Ω respectively. At 2 GHz, the coupling factor between primary and secondary 1 and 2 is 0.64 and 0.66 respectively, while the coupling between secondary 1 and 2 is ≈ 0.45 . Fig. 11 reports the simulated transmission and isolation between the TX port and the antenna and RX ports. When the antenna and balance ports are loaded by ideal 50 Ω loads, the RX ports (secondaries) are well isolated from the TX port (center-tap), while the TX power is split between antenna and balancing impedance (inherent 3 dB loss) with less than 1 dB extra-loss due to HT losses. At 2 GHz the isolation between the TX port



Fig.10. Hybrid transformer simulated inductances and quality factors of primary (a), inner (b) and outer (c) secondary; coupling factors between primary and each secondary and between secondaries (d).



Fig. 11: Hybrid transformer transmission between TX and antenna ports and isolation between TX and LNA ports (common-mode and differential modes) when antenna and balancing ports are loaded with 50 Ω .

and the differential and common-mode RX ports is more than 72 and 48 dB respectively.

V. EXPERIMENTAL RESULTS

The HT-based front-end was implemented in TSMC 28nm LP CMOS with an active area of 0.72 mm², as shown in Fig. 12. The chip was wire-bonded to a four-layers FR4 PCB for test purposes and the TX port was matched to 50 Ω using an on-board L-matching network. Measured and simulated gain and NF of the receiver are plotted in Fig. 13.a-b. NF varies from 6.5 dB to 6.8 dB going from 1.7 to 2.3 GHz, i.e. ≈ 0.8 dB above simulation. The extra noise can be explained assuming to use a mixer with no harmonic rejection. This occurs because of an error in the tuning circuit of the LC tank at the mixer output that makes the circuit almost ineffective. Such conclusion is also confirmed by harmonic rejection measurements, that are significantly lower than expected and



Fig. 12: Chip microphotograph

show essentially no variation while tuning the mixer LC tank. This was not the case for the previous correct implementation of the same circuit [16]. The gain is about 36 dB and varies by less than 1 dB across the frequency range of operation. TX-to-Antenna insertion loss is between 4 and 4.3 dB between 1.5 and 2 GHz, i.e. 1 to 1.3 dB above the theoretical minimum of 3 dB due to the power split between antenna and balancing impedance. Measured return loss at antenna and TX port is reported in Fig. 13.c. The IIP3_{RX} is limited by the baseband filter for in band interferers and by the LNA for OOB interferers and is plotted in Fig. 14 versus two-tones frequency offset for an intermodulation frequency (f_{IM}) of 100 kHz. It starts at -10 dBm with tones in band and increases as they move out of band. At 10 MHz IIP3_{RX} is 13.5 dBm, it exceeds 20 dBm beyond 30 MHz and has a peak of 25 dBm around 50 MHz. From the measured IIP3_{RX}, HDS, FDS and AC blocking requirements would be fulfilled with only 45 dB ISO_{TX-RX} and 35 dB CMRR assuming a sufficiently linear balancing impedance. In Fig. 14 the measured IIP2 is reported. It ranges from 56 to 64 dBm for offset frequencies above 8 MHz. The balancing network can be programmed to balance the hybrid across the whole band of operation. The optimal balancing configuration can be found manually or with an automated control loop. Details on the optimization algorithm, convergence time and tracking can be found in [27]. The effective ANT port impedance is transformed by the PCB traces and bonding wires. To test the circuit with close to 50 Ω antenna port impedance the HT is first coarsely balanced for a balancing impedance of 50 Ω using an on-board L-match. Measured ISO_{TX-RX} vs. TX frequency is shown in Fig. 15.a for different balancing impedance control bit configurations, optimized for different center frequencies. A maximum of 70 dB is achieved and 40 dB are maintained across ≈ 100 MHz bandwidth, limited by the on-board L-match network. In practice the antenna frequency selectivity determines the isolation bandwidth. Measured ISO_{TX-RX} with a 2.4 GHz Planar Inverted-F Antenna (PIFA) [25] connected to the



Fig. 13: Measured (dots) and simulated (lines) IDT receiver performance: a) RX gain and TX insertion loss (ILTX-ANT); b) RX noise figure; c) measured return loss at TX and antenna ports.

antenna port is shown in Fig. 15.b. Isolation is above 45 dB across 14 MHz. These values are consistent with ones used in Section II.A, and confirm that the HDS scenario is the most critical one for RX linearity. IIP3_{HDS} was measured for 100 MHz TX-RX separation (Fig. 16). IIP3 was tested with two tones, one representing the CW blocker and the other representing the TX leakage, placed at 50.5 MHz and 100 MHz offset from the RX carrier respectively. The receiver IM3 varies with the square of the blocker and linearly with the transmitter leakage, hence IM3 should have a 2 dB/dB slope and a 1 dB/dB slope versus blocker power (P_{BLK}) and the TX power (P_{TX}) respectively. This was experimentally verified, as reported in Fig. 16.a-b. For an IIP3_{RX} of 23 dBm the



Fig. 14: Measured receiver IIP2 and IIP3 vs. two-tones frequency offset with $f_{IM} = 100$ kHz.



Fig. 15: Measured TX-to-RX isolation (ISO_{TX-RX}) vs. TX frequency: a) with 50 Ω termination resistor at the antenna port on the PCB for different balancing configurations; b) with a 2.4 GHz PIFA at the antenna port.

relationship IIP3_{HDS} = IIP3_{RX}+ ISO_{TX-RX}/2 is verified to within 1 dB up to ISO_{TX-RX} = 40 dB and IIP3_{HD} = 43 dBm. Beyond this point IIP3_{HDS} increases with a smaller slope and eventually saturates at \approx 50 dBm. IIP3 in FDS scenario follows the theoretical law i.e. IIP3_{FDS} = IIP3_{RX} + ISO_{TX-RX} only up to about 45 dBm which corresponds to an ISO_{TX-RX} of only 22 dB. Beyond this point IIP3_{FDS} increases with a smaller slope and eventually saturates at \approx 50 dBm similarly to the HDS case. This behavior is remarkably similar in the two cases even though they depend in a different way from ISO_{TX-RX}. We conclude that this is due to distortion mechanisms, not considered in our analysis, which do not improve with ISO_{TX-RX}. RX. Furthermore, we exclude that the limiting factor is TX CML since it affects IIP3_{FDS} and not IIP3_{HDS}. Either Z_{BAL}



Fig. 16: HDS intermodulation between TX and RX blocker. (a-b) measured IM3 referred at the antenna input; (c) antenna-referred IIP3_{HDS} vs frequency (f_{TX} -f_{BLK}=50MHz).

TABLE II IIP2 Measurements Results

	IIP2 _{RX}	IIP2TX (20dB ISO _{TX-RX})	IIP2TX (40dB ISO _{TX-RX})
Adj. Channel IIP2 [dBm]	30.6	73	106
OOB IIP2 [dBm]	58.4	99	105.5

nonlinearity or the experimental setup intrinsic limitations [29] can give rise to such a behavior. To confirm that the measured IIP3_{FD} is not limited by the HT CM isolation, additional IIP3 and IIP2 measurements were performed. IIP3 measurements with two closely-spaced tones applied to the TX port have been carried out with ISO_{TX-RX} of 45 dB. This measurement is not affected by CM isolation at RF since RX IIP3 is limited by the BB TIA. In this case, IIP3 should improve by $1.5xISO_{TX-RX}$ or >67 dB with respect to the IIP3_{RX}. Instead measured IIP3 was \approx 50 dBm, confirming that HT CM isolation is not the limiting factor in our design. IIP2 two-tones tests have been carried out injecting 1 MHz spaced signals at the TX port at 2.6 and 50 MHz offset frequencies from the RX LO and the results are reported in Table II as adjacent channel and OOB

IIP2 respectively. The tests have been repeated at different frequencies corresponding to different levels of ISO_{TX-RX}. With low isolation levels the effective IIP2 improves with respect to the RX IIP2 as expected, i.e. $IIP2_{TX} = IIP2_{RX} + 2$ ISOTX-RX. As isolation increases the measured IIP2 eventually saturates at around 105 dBm irrespective of the frequency spacing from the RX LO. This may be due to the limited dynamic range of our measurement setup [29]. Measured LO leakage at the antenna is less than -70 dBm. Finally, power consumption excluding LO division and distribution is only 18 mW, while the total power is 26 mW. Table III summarizes the results, showing significant performance improvement over prior HT-based receivers. Similar NF compared with prior implementations is achieved over a broad frequency range with equal or better power consumption (notice that [14] includes only the LNA). TX-to-antenna loss is also comparable with [6] when balun loss is considered and is ≈ 1 dB higher than in [14], where duplexer loss is tilted in favor of the TX-antenna path. Further improvements in NF are expected (≈ 1 dB) by optimizing the transformer+LNA for lower transformer loss and improving the harmonic-rejection filter. Receiver IIP3 is 19 dB higher than in [14] and 30 dB higher than in [6]. IIP3_{HDS} compared with the ones in [14] and [6] as estimated from $IIP3_{RX}$ and the effective isolation derived from the triple-beat test is improved by > 20 dB.

VI. CONCLUSION

Fully integrated duplexers need improvements primarily on their linearity to compete with passives ones. 25 dBm RX IIP3 brings the required HT balancing accuracy to around 45 dB. This drastically simplifies hybrid balancing and adaptation loop accuracy. Combined with very linear and dual-band balancing impedance designs as in [7][8], this potentially paves the way to duplexer integration in mobile applications. This architecture can be extended to full-duplex applications but significant improvements are needed such as a higher inband linearity and improved TX leakage suppression, e.g. using additional cancellation paths in the digital domain.

$APPENDIX-IIP3 \ DERIVATION$

To derive the IIP3 expressions for the HT with CS and XCG LNAs we start from the results of the small-signal analysis in Section III. In the CS front-end (Fig. 8.a) we apply a signal V_{ANT} to the antenna port. Assuming $Z_{RX} >> R_S$, the differential voltage at the CS LNA input is $V_{IN} = 2n V_{ANT}$, i.e. each transistor has a $V_{gs} = n V_{ANT}$. It follows that, the IIP3 voltage referred to the antenna is 1/n that of a simple MOS transistor, i.e. from [28] $V_{IIP3} = \sqrt{(4/3) g_m/g_{m3}}$, where g_{m3} is the third-order nonlinear coefficient of the MOS I-V characteristic Taylor series expansion and the nonlinearities associated with the output conductance have been neglected. From the above considerations, (6) follows immediately. In a cross-couple CG LNA, the differential RX input impedance $(1/g_m)$ is relatively small compared with R_s but not negligible. The RX input voltage, that is also the gate-source of each input device, is equal to $V_{GS} = 2nV_{ANT}/(1+2n^2 g_m R_S)$ and the

	[7]	[6] [14]		This work
Design	Hybrid	Hybrid + RX	Hybrid + LNA	Hybrid + RX
Technology	0.18µm SOI	65nm CMOS	0.18µm CMOS	28nm CMOS
Area [mm ²]	1.75	2.2	0.35	0.72
Power [mW]	N/A	51.1	10.5	26
Freq [GHz]	1.9-2.2	1.7-2.2	1.6-2.2	1.7-2.1
RX Gain [dB]	N/A	45	N/A	35
RX NF [dB]	3.9	6.7 ¹	6.5	6.7
IIP3 _{RX} [dBm]	72	-4.6	6.2	25
IL _{TX-ANT} [dB]	3.7	4.5 ¹	3.2	4
ISO TX-RX [dB]	>50	>50	>60	>40
IIP3 _{FDS} [dBm]	70	48.6 ²	45.7	>50
IIP3 _{HDS} [dBm]	N/A	22 ²	25 ³	>46.5

TABLE III Comparison with State-of-the-art

¹ Includes 0.8 dB ext. balun loss; ² extrapolated from triple-beat test and RX IIP3; ³ extrapolated from IIP3_{FDS} and RX IIP3.

current at its drain is $2ng_m V_{ANT}/(1+2n^2g_m R_S)$. The non-linearity in the device transconductance generates a third-order nonlinear current given by (A.1), where the denominator represents the suppression factor due to recirculation.

$$i_{IM3} = \frac{g_{m3}V_{gs}^3}{1 + 2n^2 g_m R_s}$$
(A 1)

When $2n^2R_S \gg 1/g_m$ the intermodulation distortion is highly suppressed, as is the noise. If we apply two tones at the antenna port of amplitude V_A and frequencies ω_1 and $\omega_2 V_{ANT}$ = $V_A \cos(\omega_l t) + V_A \cos(\omega_2 t)$ and i_{IM3} is:

$$i_{IM3} = \frac{3g_{m3} (2nV_A)^3}{4(1+2n^2 g_m R_S)^4} \cdot (A.2)$$
$$\cdot (\cos(2\omega_1 - \omega_2)t + \cos(2\omega_2 - \omega_1)t)$$

Equating i_{IM3} to the linear drain current $G_{m,XCG}V_{ANT}$, with $G_{m,XCG}$ given by (3.a), we find the antenna-referred IIP3 as given by (7).

When a CM signal is applied at the LNA input, due to the capacitive cross-coupling and the parasitic capacitance seen at the gate, a small fraction of it, $1/A_{C-FFW}$, appears as a gate-source voltage V_{GS}. If a DM signal $V_A cos(\omega_2 t)$ is applied at the antenna port and a signal $V_A cos(\omega_1 t)$ is applied at the TX port with the HT perfectly balanced but with finite CMRR, the two signals generate a DM i_{IM3} that is still given by (A.1), but where V_{gs} is given by $V_A/(CMRR \cdot A_{C-FFW})cos(\omega_1 t) + 2nV_A/(1+2n^2 g_m R_S)cos(\omega_2 t)$. Hence, the differential i_{IM3} is:

$$i_{IM3} = \frac{3g_{m3}(2n)V_A^3}{\left[2(1+2n^2g_mR_s)A_{C-FFW}CMRR\right]^2}\cos(2\omega_1 - \omega_2)t \text{ (A.3)}$$

Equating i_{IM3} in (A.3) to the linear current $G_{m,XCG}$ $V_A cos(\omega_2 t)$, with $G_{m,XCG}$ given by (3.a), we find the antenna-referred IIP3 as given by (8).

REFERENCES

- S. H. Abdelhalem, P. S. Gudem, L. E. Larson, "Hybrid Transformer-Based Tunable Differential Duplexer in a 90-nm CMOS Process," in *IEEE Trans. on Microwave Theory and Techniques*, vol. 61, no. 3, pp. 1316–1326, Mar 2013
- [2] ETSI, "LTE (E-UTRA) User Equipment (UE) radio transmission and reception", 3GPP TS 36.101 ver. 12.5.0, Release 12, Nov 2014
- [3] M. Mikhemar, H. Darabi, A. Abidi, "A tunable integrated duplexer with 50dB isolation in 40nm CMOS," 2009 IEEE ISSCC Dig. Tech. Papers, pp. 386-387, Feb. 2009.
- [4] M. Mikhemar, H. Darabi, A. Abidi, "An on-chip wideband and low-loss duplexer for 3G/4G CMOS radios," in 2010 IEEE Symposium on VLSI Circuits, pp.129-130, 16-18 June 2010.
- [5] M. Mikhemar, H. Darabi and A. A. Abidi, "A Multiband RF Antenna Duplexer on CMOS: Design and Performance," in *IEEE Journal of Solid-State Circuits*, vol. 48, no. 9, pp. 2067-2077, Sept. 2013.
- [6] S. H. Abdelhalem, P. S. Gudem, and L. E. Larson, "Tunable CMOS Integrated Duplexer with Antenna Impedance Tracking and High Isolation in the Transmit and Receive Bands", in *IEEE Trans. on Microwave Theory and Techniques*, vol. 62, no. 9, pp. 2092-2104, Sept. 2014.
- [7] B. van Liempd, et al., "A 70dBm IIP3 Single-Ended Electrical-Balance Duplexer in 0.18µm SOI CMOS", 2015 IEEE ISSCC Dig. Tech. Papers, San Francisco, CA, pp 32-33, Feb 2015.
- [8] B. Hershberg, B. van Liempd, X. Zhang, P. Wambacq, J. Craninckx, "A Dual-Frequency 0.7-to-1GHz Balance Network for Electrical Balance Duplexers", 2016 IEEE ISSCC Dig. Tech. Papers, pp 356-357, Feb 2016.
- [9] S. Ramakrishnan, L. Calderin, A. Puglielli, E. Alon, A. Niknejad and B. Nikolić, "A 65nm CMOS transceiver with integrated active cancellation supporting FDD from 1GHz to 1.8GHz at +12.6dBm TX power leakage," 2016 IEEE Symposium on VLSI Circuits (VLSI-Circuits), Honolulu, HI, 2016, pp. 1-2.
- [10] H. Yüksel, et al., "A Wideband Fully Integrated Software-Defined Transceiver for FDD and TDD Operation," in *IEEE Journal of Solid-State Circuits*, vol. 52, no.5, May 2017.
- [11] J. Zhou, N. Reiskarimian and H. Krishnaswamy, "Receiver with integrated magnetic-free N-path-filter-based non-reciprocal circulator and baseband self-interference cancellation for full-duplex wireless," 2016 IEEE ISSCC Dig. Tech. Papers, San Francisco, CA, pp. 178-180, Feb 2016.
- [12] N. Reiskarimian, M. B. Dastjerdi, J. Zhou and H. Krishnaswamy, "Highly-linear integrated magnetic-free circulator-receiver for fullduplex wireless," 2017 IEEE Int. Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2017, pp. 316-317.
 [13] T. Zhang, A. Najafi, C. Su, J.C. Rudell, "A 1.7-to-2.2GHz Full-Duplex
- [13] T. Zhang, A. Najafi, C. Su, J.C. Rudell, "A 1.7-to-2.2GHz Full-Duplex Transceiver System with >50dB Self-Interference Cancellation over 42MHz Bandwidth", 2017 IEEE Int. Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2017, pp. 314-315.
- [14] M. Elkholy, M. Mikhemar, H. Darabi, K. Entesari, "Low-Loss Integrated Passive CMOS Electrical Balance Duplexers With Single-Ended LNA", in *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 5, pp. 1544-1559, May 2016
- [15] C. k. Luo, P. S. Gudem and J. F. Buckwalter, "A 0.2–3.6-GHz 10-dBm B1dB 29-dBm IIP3 Tunable Filter for Transmit Leakage Suppression in SAW-Less 3G/4G FDD Receivers," in *IEEE Trans. on Microwave Theory and Techniques*, vol. 63, no. 10, pp. 3514-3524, Oct. 2015
- [16] M. Ramella, I. Fabiano, D. Manstretta, and R. Castello, "A 1.7-2.1GHz +23dBm TX Power Compatible Blocker Tolerant FDD Receiver with Integrated Duplexer in 28nm CMOS", 2015 IEEE Asian Solid-State Circuits Conference (A-SSCC), Xiamen, 2015, pp. 1-4.
- [17] C.-Y. Yu, I. Lu, Y.-H. Chen, L.-C. Cho, C. Sun, C.-C. Tang, H.-H. Chang, W.-C. Lee, S.-J. Huang, T.-H. Wu, C.-S. Chiu, and G. Chien, "A

SAW-Less GSM/GPRS/EDGE Receiver Embedded in 65-nm SoC," in *IEEE J. of Solid-State Circ.*, vol. 46, no. 12, pp. 3047–3060, Dec 2011.

- [18] D. Murphy, H. Darabi, A. Abidi, A. Hafez, A. Mirzaei, M. Mikhemar, and M.-C. Chang, "A blocker-tolerant, noise- cancelling receiver suitable for wideband wireless applications," in *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 2943–2963, Dec 2012.
- [19] Fabiano, I.; Sosio, M.; Liscidini, A.; Castello, R., "SAW-Less Analog Front-End Receivers for TDD and FDD," in *IEEE Journal of Solid-State Circuits*, vol.48, no.12, pp.3067'3079, Dec 2013.
- [20] H. Darabi, A. Mirzaei, and M. Mikhemar, "Highly Integrated and Tunable RF Front Ends for Reconfigurable Multiband Transceivers: A Tutorial," in *IEEE Trans. Circuits Syst. I - Reg. Papers*, vol.58, no.9, pp.2038,2050, Sept. 2011.
- [21] L. Laughlin, M. A. Beach, K. A. Morris and J. Haine, "Electrical balance duplexer adaptation in indoor mobile scenarios," 2015 9th European Conference on Antennas and Propagation (EuCAP), Lisbon, 2015, pp. 1-5.
- [22] ETSI, "Digital Cellular Telecommunications System (Phase 2+); Radio Transmission and Reception, 3GPP TS 36.101 Version 11.2.0 Release 11, 2013.
- [23] X. Fan, H. Zhang, E. Sanchez-Sinencio, "A Noise Reduction and Linearity Improvement Technique for a Differential Cascode LNA," in *IEEE J. of Solid-State Circuits*, vol.43, no.3, pp.588-599, March 2008
- [24] Wei Zhuo, S. Embabi, J. P. de Gyvez and E. Sanchez-Sinencio, "Using capacitive cross-coupling technique in RF low noise amplifiers and down-conversion mixer design,", *Proc. of the 26rd European Solid-State Circuits Conference (ESSCIRC)*, Stockholm, Sweden, 2000, pp. 77-80.
- [25] D. Montanari, L. Silvestri, M Bozzi, and D. Manstretta, "Antenna Coupling and Self-Interference Cancellation Bandwidth in SAW-less Diversity Receivers", 46th European Microwave Conference 2016, London, 4-6 Oct 2016
- [26] W. H. Chen, G. Liu, B. Zdravko and A. M. Niknejad, "A Highly Linear Broadband CMOS LNA Employing Noise and Distortion Cancellation," in *IEEE Journal of Solid-State Circuits*, vol. 43, no. 5, pp. 1164-1176, May 2008
- [27] G. Castellano, D. De Caro, A. G. M. Strollo and D. Manstretta, "A low power control system for real-time tuning of a hybrid transformer-based receiver," 2016 IEEE Int. Conference on Electronics, Circuits and Systems (ICECS), Monte Carlo, Monaco, 2016, pp. 328-331.
- [28] B. Razavi, "RF Miroelectronics", 2nd ed., Prentice Hall, New York, 2012
- [29] B. van Liempd et al., "A +70-dBm IIP3 Electrical-Balance Duplexer for Highly Integrated Tunable Front-Ends," in *IEEE Trans. on Microwave Theory and Techniques*, vol. 64, no. 12, pp. 4274-4286, Dec. 2016.
- [30] Hung-Ju Wei, Chinchun Meng, Ta-Wei Wang, Tai-Lin Lo, and Chia-Ling Wang, "60-GHz Dual-Conversion Down-/Up- Converters Using Schottky Diode in 0.18 μm Foundry CMOS Technology," in *IEEE Trans. Microw. Theory Tech.*, Vol. 60, No. 6, pp. 1684-1698, June 2012.



Ivan Fabiano (S'13) was born in Milano, Italy, in 1986. He received the B.S. and M.S. degrees in electrical engineering from the University of Pavia, Pavia, Italy in 2009 and 2011 respectively. In 2014 he then received the Ph.D. from University of Pavia working on integrated analog system for mobile applications. From 2014 to 2017 he was with Marvell Semiconductor Inc., Pavia, Italy, where he was involved in the high data speed interfaces development. In 2017 he joined Silicon Mitus, Pavia, Italy.

His research interests include high-speed mixed-signal, radio-frequency circuits and systems and high speed serial link.



Matteo Ramella (S'15) was born in Vigevano, Italy, in 1984. He received the B.S. and M.S. degrees in electrical engineering and the Ph.D. degree in Microelectronics from the University of Pavia, Italy, in 2009, 2011 and 2015, respectively. From 2013 to 2015 he was with Marvell Semiconductor Inc. (Pavia, Italy) as intern RF-Analog Design Engineer. Currently, he is a Senior Design Engineer with Advanced Circuit Pursuit (ACP) AG in Zurich, Switzerland. His research interests are in CMOS RF circuits and systems for

wireless communications.



Danilo Manstretta (M'03) received the Laurea degree (*summa cum laude*) and the Ph.D. degree in electrical engineering and computer science from the University of Pavia in 1998 and 2002, respectively. During his studies, he worked on CMOS RF front-end circuits for direct-conversion wireless applications.

From 2001 to 2003 he was with Agere Systems as a Member of Technical Staff, working on WLAN transceivers and linear power amplifiers for base stations. From 2003 to 2005 he was with Broadcom Corporation, Irvine, CA, working on

RF tuners for TV applications. In 2005 he joined the University of Pavia as an Assistant Professor and was granted tenure in 2008. His research interests are in the field of analog, RF and millimeter-wave integrated circuit design.

Dr. Manstretta is a member of the Technical Program Committee of the IEEE Radio Frequency Integrated Circuits (RFIC) Symposium since 2006 and of the Steering Committee for the same conference since 2017. He was Guest Editor of the IEEE Journal of Solid-State Circuits May 2017 Special Section dedicated to the 2016 RFIC Symposium. He was co-recipient of the 2003 IEEE Journal of Solid-State Circuits *Best Paper Award*.



Rinaldo Castello (S'78–M'78–SM'92–F'99) graduated from the University of Genova (*summa cum laude*) in 1977 and received the M.S. and the Ph. D. from the University of California, Berkeley, in '81 and '84. From '83 to '85 he was Visiting Assistant Professor at the University of California, Berkeley. In 1987 he joined the University of Pavia where he is now a Full Professor. He consulted for ST-Microelectronics, Milan, Italy up to 2005 in '98 he started a joint research centre

between the University of Pavia and ST and was its Scientific Director up to '05. He promoted the establishing of several design centre from multinational IC companies around Pavia, among them Marvell for which he was a consultant from 2005 to 2016. He is now consulting for InvenSense. Rinaldo Castello has been a member of the TPC of the European Solid State Circuit Conference (ESSCIRC) from 1987 to 2016 and of the International Solid State Circuit Conference (ISSCC) from '92 to '04. He was Technical Chairman of ESSCIRC '91 and General Chairman of ESSCIRC '02, Associate Editor for Europe of the IEEE Journal of Solid-State Circuits from '94 to '96 and Guest Editor of its July '92 special issue. From 2000 to 2007 he has been Distinguished Lecturer of the IEEE Solid State Circuit Society. Prof Castello was named one of the outstanding contributors for the first 50 and 60 years of ISSCC and a co-recipient of the Best Paper Award at the 2005 Symposium on VLSI of the Best Invited Paper Award at the 2011 CICC and of the Best Evening Panel Award at ISSCC 2012 and 2015. He was one of the two European representatives at the Plenary Distinguished Panel of ISSCC 2013 and the Summer 2014 Issue of the IEEE Solid State Circuit Magazine was devoted to him. Rinaldo Castello is a Fellow of the IEEE.