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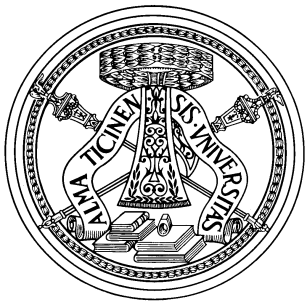

Ph.D. Thesis in Microelectronics
XXIX Cycle

Design of mm-Wave Local Oscillator Building Blocks for Next-Generation Mobile Backhaul

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Though much is taken, much abides.
Alfred Tennyson, Ulysses (1833)

Abstract

Point-to-point wireless links in the E-Band (71-76GHz and 81-86GHz bands) can provide high-data-rate, easily-deployable, cheap and flexible backhaul solutions, important enablers for the mobile network evolution towards 5G. The development of CMOS/BiCMOS integrated transceivers for E-Band backhaul applications can help reducing the cost and footprint of the equipment, but presents design challenges, mostly related to the use of spectrally-efficient high-order modulations, which mandate high linearity and low phase noise.

In this dissertation, local-oscillator generation requirements for E-Band backhaul applications are addressed. Phase-noise specifications for the frequency synthesizer are identified, and custom analog building blocks, namely a VCO and a frequency quadrupler, are proposed. The blocks have been designed in 55nm BiCMOS technology, and measurement results on test chips are presented.

A noise-scalable multi-core oscillator is proposed as a key block of the frequency synthesizer. It achieves ultra-low phase noise performance, and allows to trade noise and power consumption according to system requirements, a useful feature in E-Band communications. An analytical model describing the effect of mismatches on the multi-core oscillator is also presented. It provides understanding of the robustness of the proposed solution, and useful insights on in-phase coupled oscillator design.

Measurement results demonstrate advances over state of the art, primarily in terms of low phase-noise performance, and show how the proposed circuits are suitable as local oscillator building blocks in direct-conversion E-Band backhaul transceivers.

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List of Acronyms

5G	Fifth Generation
BER	Bit Error Rate
BiCMOS	Bipolar and Complementary Metal-Oxide-Semiconductor
BTS	Base Transceiver Station
BEOL	Back End Of the Line
CMOS	Complementary Metal-Oxide-Semiconductor
EIRP	Equivalent Isotropic Radiated Power
FEOL	Front End Of the Line
FET	Field Effect Transistor
FoM	Oscillator Figure of Merit
FSPL	Free-Space Path Loss
GBW	Gain-Bandwidth product
GP	General Purpose
HBT	Heterojunction Bipolar Transistor
IC	Integrated Circuit
ISF	Impulse Sensitivity Function
KCL	Kirchhoff Current Law
LoS	Line of Sight
LP	Low Power
LTE	Long Term Evolution
LTI	Linear Time Invariant
LTV	Linear Time Variant

MIMO	Multiple Input Multiple Output
nLoS	non Line of Sight
PA	Power Amplifier
PtP	Point to Point
PLL	Phase-Locked Loop
Q	Quality factor
QVCO	Quadrature Voltage Controlled Oscillator
RMS	Root Mean Square
RX	Receiver
SiGe	Silicon Germanium
SNR	Signal-to-Noise Ratio
SINR	Signal-to-Interference-and-Noise Ratio
TR	Tuning Range
TX	Transmitter
UDN	Ultra-Dense Network
UTM	Ultra-Thick Metal
VCO	Voltage-Controlled Oscillator
XFMR	Transformer

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Berkeley, Nov 14th 2016

Introduction

The ever increasing mobile data traffic, expected to grow by >8x from 2015 to 2020 [1], is driving continuous innovation in wireless communications, and next-generation mobile networks (i.e. 5G and beyond) are expected to provide several Gbps user data rate. Although the picture is not clear yet on how to overcome the performance limitations of the current 4G-LTE standard, all the proposed hardware solutions involve a further increase in the base-transceiver-station (BTS) density, following the trend which has kept going in the last twenty years [2].

The BTS density increase rises the complexity of the network, and the backhaul infrastructure, i.e. the set of links connecting the BTS to the network core, is emerging as a critical bottleneck in future-generation mobile networks [2, 3]. To push forward with the network evolution, two directions are emerging in the backhaul industry. First, new hardware solutions are being investigated to provide high-capacity, easily-deployable, medium-range backhaul links, suitable for dense BTS environments. Among the proposed competitors, mm-Wave wideband wireless links, in the E-Band in particular, are emerging as a promising technique [2, 4]. Second, as BTS reach high-volume productions, fully-integrated BTS transceivers in CMOS or BiCMOS technology can reduce the cost of backhaul equipment [4]. These emerging paths create new opportunities in mm-Wave integrated circuit design.

Unlike other mm-Wave applications such as 60GHz WLAN or automotive radars, E-Band links employ high-order modulations to maximize the channel capacity. This mandates challenging specifications for integrated transceivers, especially concerning power-amplifier (PA) linearity and local-oscillator (LO) phase noise.

In this work, E-Band LO phase noise requirements are addressed, proposing novel frequency-generation building blocks, namely a voltage-controlled oscillator (VCO) and a frequency multiplier. In particular, a multi-core VCO is introduced as the key block of the frequency synthesizer. The oscillator achieves ultra-low phase noise with CMOS-compatible power supply, and allows power-efficient noise scaling according to the system requirements, a useful feature in E-Band transceivers. Prototypes were realized in BiCMOS 55nm technology, BiCMOS being the preferred technology platform for mm-Wave backhaul transceivers [4]. The research activity has been carried on in collaboration with STMicroelectronics, in the framework of the MiWaveS project, funded by the European Union 7th Framework Programme.
The dissertation is structured as follows.

In **Chapter 1**, an overview of E-Band wireless backhaul links is provided. The motivation for mm-Wave backhaul deployment in future-generation mobile scenarios is examined, propagation characteristics and spectrum regulations in the E-Band are outlined, and the state of the art of integrated transceivers is briefly reviewed.

In **Chapter 2**, phase noise specifications for E-Band LO generators are derived. A simplified model to quantitatively estimate the effect of phase noise on signal integrity degradation is described. Next, after introducing some system-level considerations, target noise specifications for the oscillator are deduced and compared with performance of the state of the art. Finally, the proposed frequency synthesizer architecture is disclosed.

In **Chapter 3**, a phase-noise-scaling technique leveraging multi-core oscillators is presented. After outlining the operating principle of the circuit, an analytical model describing system behavior and phase noise performance of resistively-coupled oscillators in presence of component mismatches is provided, to assess the robustness of the proposed circuit. In conclusion, a 20GHz quad-core VCO is presented.

Chapter 4 deals with design techniques for wideband frequency quadruplers. A transformer-coupled solution is proposed, and an isolation technique to reduce common-mode coupling in inter-stage transformers is presented.

In **Chapter 5**, practical circuit design details related to the implementation of the aforementioned building blocks in BiCMOS 55nm technology are discussed. An overview of the realized test chips is also provided.

In **Chapter 6**, measurement results are presented, and the performance of the proposed circuits is compared with the state of the art.

Chapter 1

E-Band Links for Wireless Backhaul

In this chapter, an overview of E-Band mm-Wave links for backhaul applications is provided. First, backhaul requirements in future-generation mobile networks (i.e. 5G and beyond) are outlined. Then, wireless links in the E-Band are briefly described, both concerning propagation characteristics and emerging standards and regulations, in particular the European ETSI standard. Finally, state of the art of E-Band integrated transceivers is reviewed.

1.1 The Road to 5G

The evolution of mobile networks towards 5th generation (5G) is driven by three main requirements. First, higher data rates (i.e. several Gbps), are required to enable pervasive cloud computing and high-definition video streaming [2]. Second, low latency (i.e. < 1 ms) and high-reliability links will enable real-time wireless control and new mission-specific applications [5]. Finally, ultra-low-power links and protocols dealing with a high number of connected devices per unit area are key to enable the Internet of Things [6]. A detailed list of envisioned 5G network use cases, most of which fall in either of these cathegories, are summarized in Fig. 1.1. The aforementioned requirements partly clash with each other, and will require an holistic, heterogeneous environment having to deal with multiple network layers and several co-existing access and backhaul technologies [2, 6, 7].
Focusing on data-rate increase, there are several techniques that are being investi-

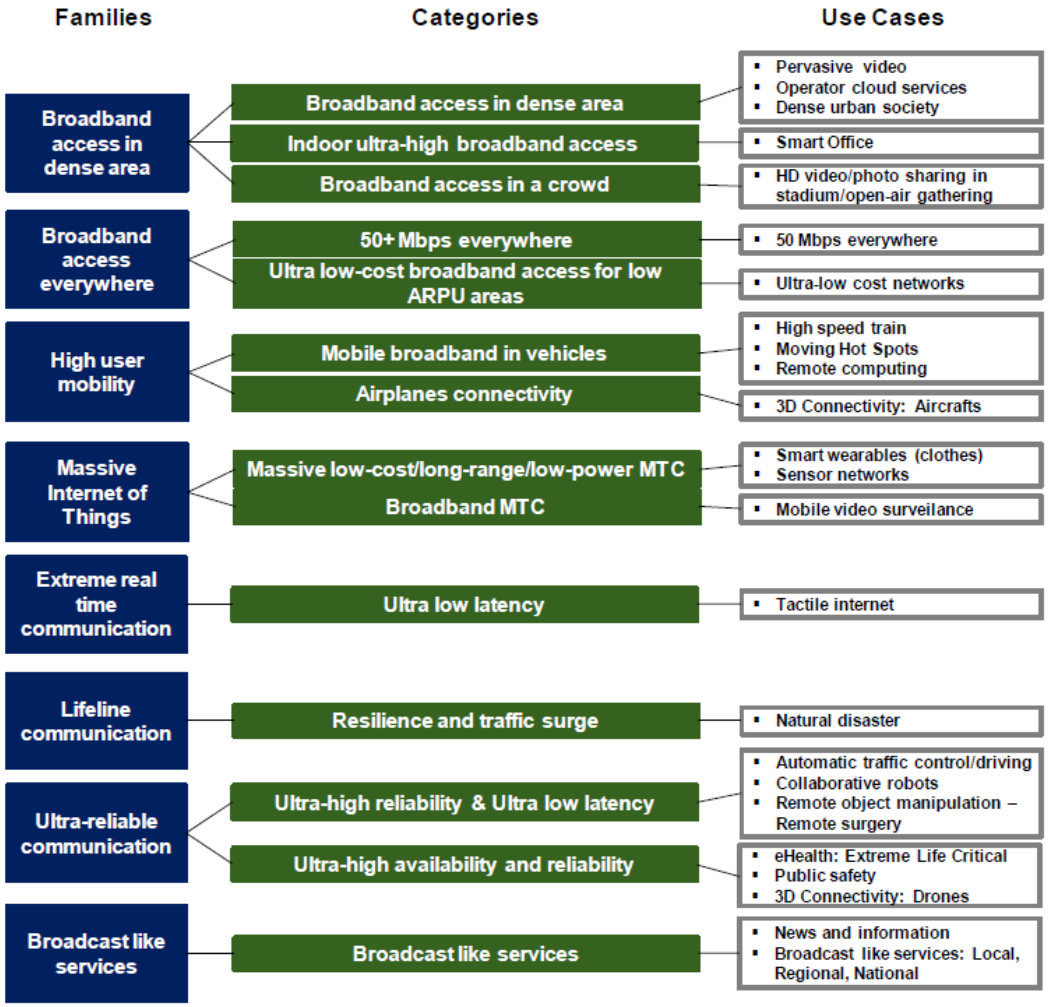

Figure 1.1: Envisioned 5G use cases [7].

gated to overcome the performance limits of LTE. Chief among them, three solutions are emerging as the more competitive ones [2].

Cell coverage area shrinking and BTS densification enable efficient spectral reuse leveraging spatial diversity, and an increase in the Signal-to-Noise Ratio (SNR) at given bandwidth, thus allowing more spectrally-efficient modulations [8]. This solution follows the path which has already been traced in previous network generations, as shown in Fig. 1.2. However, as BTS densify the Signal-to-Interference-and-Noise Ratio (SINR) becomes limited by interference, which does not scale with cell area reduction [2]. This requires new

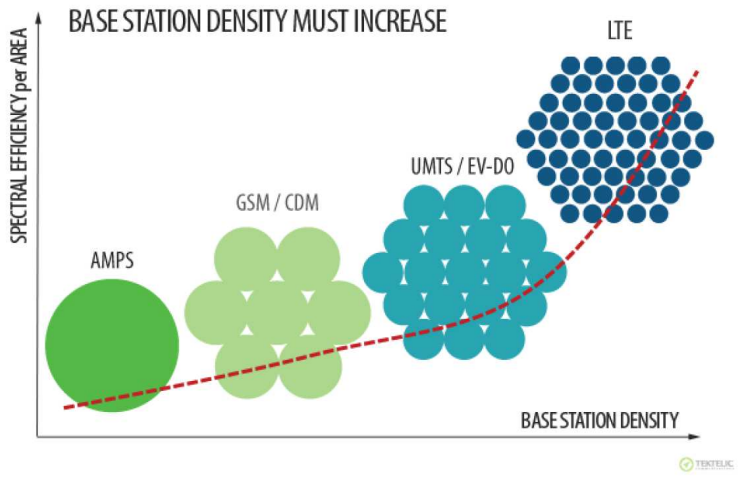

Figure 1.2: Cell coverage area shrinking and BTS densification in previous-generation mobile networks (source: Tektelic).

architectures and techniques for interference mitigation, both in BTS and user terminals [8]. When considering moving users, a critical issue in dense BTS networks is the increasing frequency of handover between neighboring cells. To face this problem, hierarchical BTS infrastructure decoupling data and control planes are proposed: wide-area macro BTS manage control signals, allocate spectrum resources and cater for handover procedures, whereas micro cells provide data offload [2, 3, 9].

mm-Wave links, exploiting the mostly unused spectrum above 30 GHz, can widely increase the communication bandwidth [4, 10]. Several spectrum portions are considered by mobile operators. In the lower mm-Wave domain, 28GHz (∼1 GHz spectrum available) and 38GHz (up to ∼4 GHz spectrum available, depending on the countries) licensed bandwidths are available, and propagation in urban and suburban environments has been studied with promising results for mobile access [10, 11]. The 60GHz band, featuring up to 9GHz unlicensed spectrum, is also be an option for mm-Wave access, although high propagation losses would require a very dense BTS environment [4]. Finally, 71-76GHz and 81-86GHz bands, featuring lower atmospheric attenuation and currently allocated for licensed fixed backhaul radio links, could

be used for mobile service as well[1] [13].

To compensate high free-space path loss (FSPL) at mm-Waves, high-directivity links should be employed, at least on the BTS side. Beamformers based on multi-user MIMO (Multiple-Input-Multiple-Output) techniques, capable of steering different data streams to different users at the same time, are being investigated for this purpose [11]. Millimiter-wave access links widely benefit from dense BTS environments. Indeed, as cells are shrinked path losses become less detrimental, Line-of-Sight (LoS) links become more likely, and the set of users to be covered scales down, thus reducing the complexity of the beamformer. Finally, as mm-Wave links are mostly noise-limited, rather than interference-limited, the SINR efficiently scale with cell area shrinking [2].

Massive MIMO systems have also been recently proposed as a way of increasing the channel capacity manyfold using spatial diversity, even at RF frequencies [14, 15]. These multi-user MIMO systems are based on large arrays of M antennas, serving K$\ll$M users. The remarkable redundancy in the number of antennas at the BTS yields high beamforming gains, thus improving SNR and interference rejection, and enables distributed, low-complexity algorithms for channel estimation. Moreover, since performance of each individual transceiver front-end (e.g. noise, output power) benefit from array gains, each element can be built using inexpensive, low-power components.

Many implementation challenges arise when developing a hardware massive MIMO system, such as dealing with coordination, calibration and data distribution in such a complex transceiver, while keeping array size, power and cost under acceptable values [15, 16]. As a result, massive MIMO testbeds realized so far are usually based on $\sim$100 antennas serving $\sim$10 users [16]. In this framework, massive MIMO systems benefit as well from cell area shrinking, which implies having to manage a reasonable amount of users.

Each of the aforementioned techniques mandate a further increase in the BTS density. In the development towards 5G, the mobile infrastructure is expected to evolve towards small-cell (or pico-cell) ultra-dense networks (UDN), where thousands of

[1]Since mm-Wave wireless communications are highly directive, the same frequency range can be used for both access and backhaul, tackling interference through spatial diversity. This concept, usually referred to as "in-band backhauling", is emerging in 5G network architectures [3, 12].

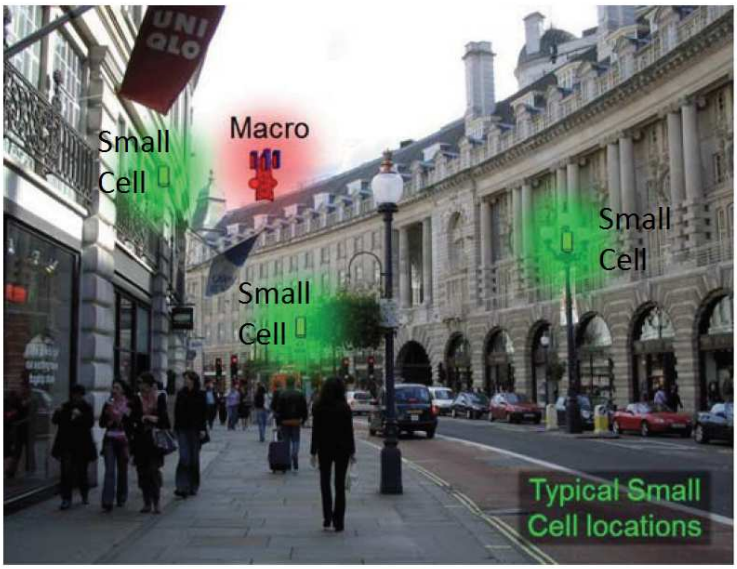

Figure 1.3: Envisioned small-cell ultra-dense network scenario [17].

compact BTS located at the street level will provide mobile service to users, as shown in Fig. 1.3 [9, 12]. However, as cell density rises, the backhaul infrastructure complexity increases.

1.2 5G Backhaul Challenges

Providing a backhaul infrastructure to 5G and small-cell networks is challenging, and backhaul capacity and power consumption are expected to become a major bottleneck in the network evolution [2, 4, 9]. 5G scenarios need high-capacity (>10 Gbps), low-latency (< 1 ms), reliable backhaul connections [3]. On the other hand, small-cell backhaul links have to be cheap, easy to deploy and reconfigure. Energy efficiency is also an important feature, as the backhaul consumption is expected to grow up to ∼50% of the BTS power budget [3].

The mobile backhaul network currently employs two main solutions: sub-40GHz Point-to-Point (PtP) microwave links, which currently constitute ∼60% of the global network [18], and wired optical links. Optical connections can reach extremely high data rates, but they are expensive and difficult to implement in ultra-dense scenarios [2, 3, 8]. On the other hand, PtP microwave links are not expected to provide enough channel capacity for next-generation networks, including LTE-Advanced [18].

As a solution, 10 GHz of spectrum in the mm-Wave domain, in the E-Band in particular, have been allocated by both FCC (Federal Communication Commission) in the USA and ECC (Electronic Communications Committee) in Europe for next-generation PtP wireless backhaul links [19, 20]. E-Band PtP links are expected to provide wideband, medium-range LoS links, suitable for backhauling small-cell UDN [3, 17, 21]. Millimeter-wave backhaul is expected to co-exist with legacy wired and wireless links, to create a toolbox of diverse solutions enabling the evolution towards small-cell networks [17].

1.3 E-Band Wireless Point-to-Point Links

Point-to-Point wireless links in the E-Band are currently allowed over two 5GHz bandwidth: 71-76 GHz and 81-86 GHz. An additional 92-95GHz band is allocated in the USA only. Most regulators around the world manage the E-Band PtP spectrum using a light-licensing scheme, such that channels are allocated to providers using a more flexible procedure and cheaper fees compared to RF communications [4].

As shown in Fig. 1.4, atmospheric attenuation in the E-Band is around 0.5 dB/km, much lower than in the 60GHz band. Significant FSPL (i.e. $\sim$130 dB over 1 km distance) can be easily compensated in LoS PtP links by using high-gain antennas, which can be very compact at mm-Waves. Using high-directivity beams also helps minimizing interference and enables efficient spectral reuse.

Another important source of losses in the E-Band is absorbtion by water particles in the atmosphere. While fog attenuation is negligible, rain losses can get up to tens of dB/km, as shown in Fig. 1.5. Rain attenuation limits the range of E-Band PtP links in most of the world to 1-2 km, which is still suitable for small-cell backhauling [22].

Significant rain attenuation in the E-Band produces wide variations in received signal conditions over time. In order to always achieve the maximum available channel capacity, proposed PtP mm-Wave standards employ adaptive-modulation techniques, so as to change the modulation order according to channel conditions [23, 24], as shown in Fig. 1.6. When high SNR is received, spectrally-efficient modulations like 64QAM and beyond are employed. Instead, if the received SNR is poor (e.g. during heavy rain outage), simpler modulations such as QPSK are used.

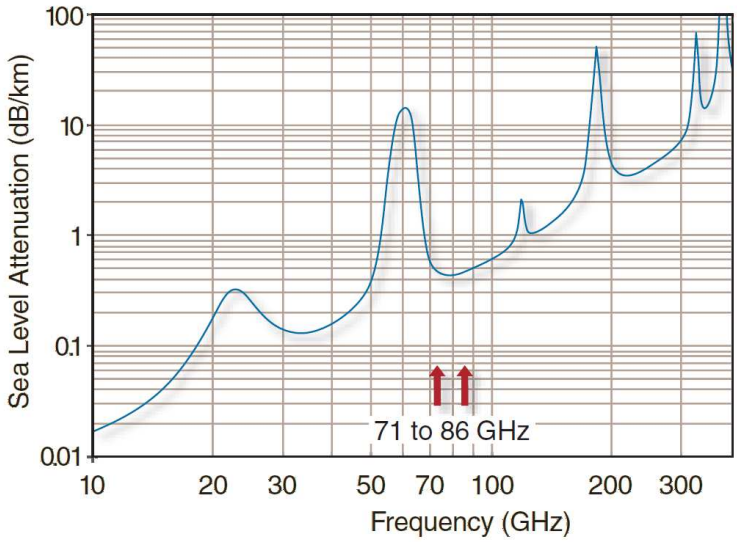

Figure 1.4: Atmospheric attenuation in the mm-Wave spectrum [22].

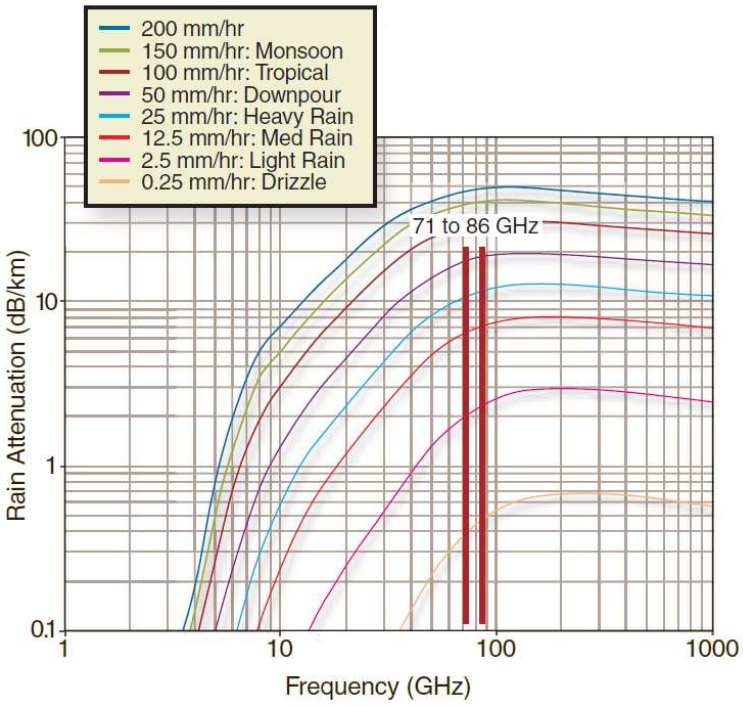

Figure 1.5: Rain attenuation in the mm-Wave spectrum [22].

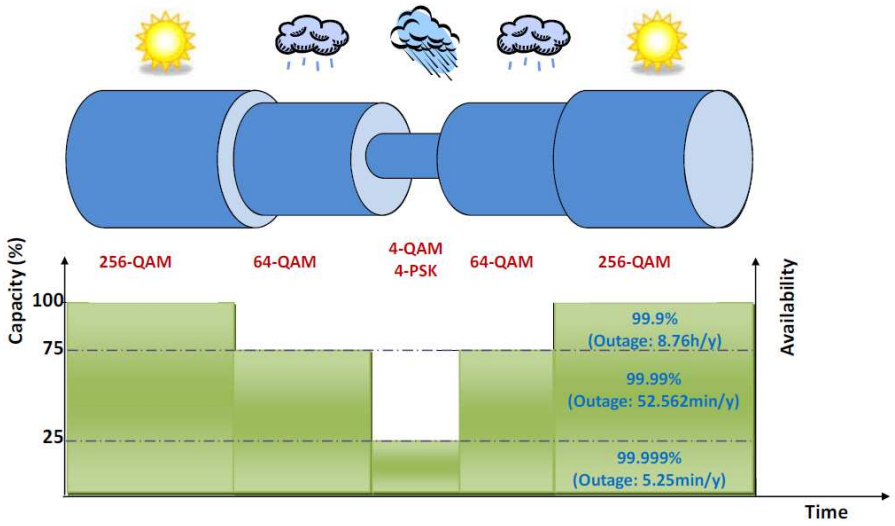

Figure 1.6: Adaptive modulation according to weather conditions in PtP radio service [23].

1.3.1 European E-Band PtP Links Standard

To gain more insight in E-Band PtP communications, we provide a brief overview of the ETSI (European Telecommunications Standards Institute) standard for E-Band PtP links. These recommendations are part of the ETSI standard 302-217 (Fixed Radio Systems), which provides rules for all the PtP radio equipment in the European Union [25].

Recommended channel spacings and modulation orders are summarized in table 1.1, together with the minimum required data rate. Standard channels are 250MHz wide, but they can be split in two or four smaller sub-channels, or aggregated into wider channels up to 2 GHz, if required. Modulations up to 256QAM are expected for standard channels, while lower-order solutions (e.g. 16QAM) may be used in channel-aggregation scenarios. The data rate should reach ∼3 Gbps using spectrally-efficient modulations. The standard explicitly allows to change both the channel bandwidth and the modulation order on the fly according to channel conditions, i.e. using bandwidth-adaptive and adaptive-modulation techniques. Other significant requirements for E-Band transceivers are outlined in table 1.2.

	Channel spacing [MHz]									
Number of symbols	62.5	125	250	500	750	1000	1260	1500	1750	2000
2	35	71	142	285	427	570	712	855	997	1140
4	71	142	285	570	855	1140	1425	1710	1995	2280
8	106	212	425	850	1275	1700	2125	2550	2975	3400
16	142	285	570	1140	1710	2280	2850	//	//	//
32	219	438	875	1750	2625	//	//	//	//	//
64	262	525	1050	2100	3150	//	//	//	//	//
128	306	612	1225	1450	//	//	//	//	//	//
256	350	700	1400	2800	//	//	//	//	//	//

Table 1.1: Minimum required data rate (in Mbps) for E-Band PtP transceivers complying to the ETSI standard 302-217, as a function of channel spacing and number of modulation symbols.

Min Bit Error Rate (BER)	10^{-6} or 10^{-10}
Carrier frequency tolerance	$\pm$50 ppm
Max EIRP	85 dBm
Max TX power	30 dBm
Min antenna gain	38 dBi

Table 1.2: Significant requirements for E-Band wireless systems, according to the ETSI standard 302-217 and in compliance with European regulations.

1.4 Integrated E-Band Transceivers

Compared to the traditional BTS counterpart, small-cell transceivers have to be more compact, cheap and energy-efficient [2, 4]. These requirements, together with the expected growth in the BTS equipment sales, motivate a shift towards high-volume CMOS and BiCMOS technologies, and the use of low-power design techniques. SiGe BiCMOS processes are usually considered as the preferred choice, mainly because of the higher peak power levels achievable in linear regime using SiGe power amplifiers [4].

Developement of integrated transceivers for E-Band backhaul is still in an early stage. However, Infineon has presented a SiGe E-Band transceiver, shown in Fig. 1.7, supporting modulations up to 64QAM [26]. As shown in the block diagram,

the transceiver features a complete analog TX and RX front-end. LO generation is performed using a push-push VCO, embedded in an external PLL, followed by a frequency doubler and a polyphase filter to generate I and Q phases. Two chipsets are commercially available, each covering one 5GHz band [27].

IBM is also working on BiCMOS E-Band transceiver developement, and recently presented a complete system transmitting modulated data up to 128QAM [28]. The prototype includes a TX and RX analog chain, and a complete frequency synthesizer. However, high-order-modulation transmission (i.e. 64QAM and 128QAM) was only achieved using an external LO. A BiCMOS E-Band integrated phased array based on injection locked oscillators was also lately proposed by UC San Diego [29].

Research on analog building blocks for E-Band integrated transceivers is mainly focused on two different tracks, namely the most challenging blocks for this application: transmitters and frequency synthesizers. On the TX side, efforts have been focused on developing modulators enabling high-order constellations [30] and PAs with high saturated output power [31–33]. In the frequency synthesis domain, solutions have been proposed to achieve wide tuning range [34], provide accurate quadrature generation [35, 36] and minimize phase noise to enable high-order modulations [37, 38].

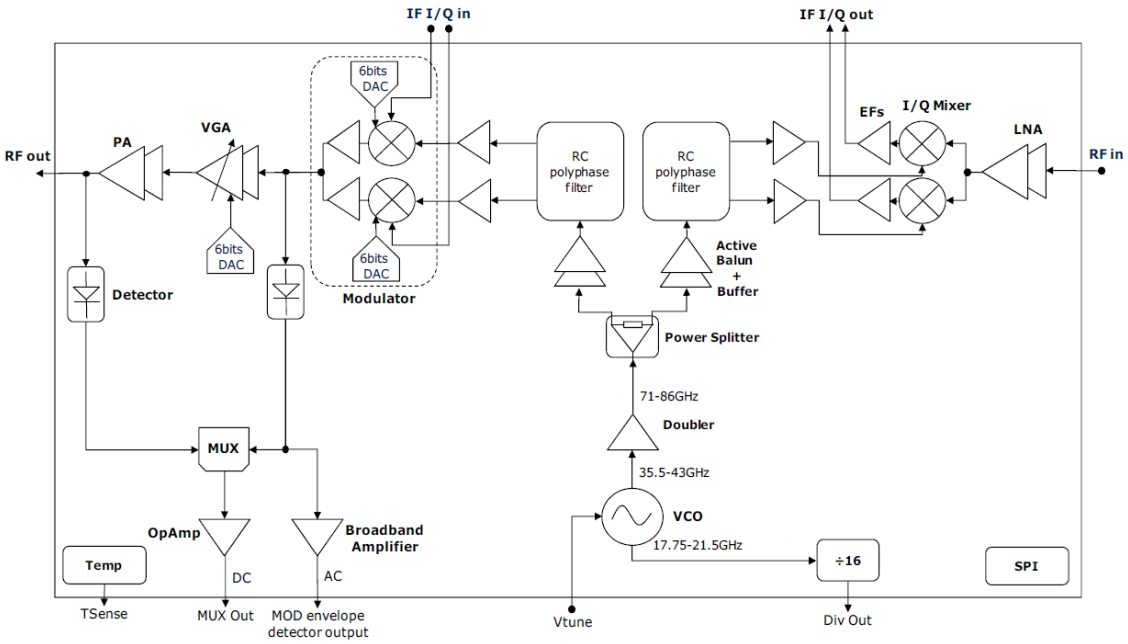

Figure 1.7: Block diagram of the Infineon E-Band backhaul transceiver [26].

1.5 Conclusions

Point-to-Point links in the E-Band can provide Gbps, km-range wireless communication, suitable for small-cell backhaul infrastructure. Such easily-deployable, high-capacity backhaul links are expected to be a fundamental enabler for the evolution of mobile networks towards 5G and beyond. To achieve the required capacity, high-order modulations are employed when needed to maximize spectral efficiency. On the other hand, substantial rain attenuation produces wide variations in the channel conditions. To guarantee good quality of service in varying environmental conditions, adaptive-modulation techniques are used.

Development of E-Band transceivers in integrated technology can help reducing cost, weight and volume of small cells. To cope with the demanding requirements of backhaul links, more efforts have to be done to improve the performance of analog building blocks, especially PAs and frequency generators. In the following, the design of frequency-synthesis building blocks is addressed.

Chapter 2

Frequency Synthesizer Requirements and Architecture

In this chapter, system-level considerations on the design of frequency synthesizers for E-Band backhaul applications are presented. First, the effect of the local oscillator phase noise on Signal-to-Noise Ratio (SNR) degradation is outlined. Next, phase-noise filtering operations by both the Phase-Locked Loop (PLL) and the baseband carrier-phase estimator are described. Combining these aspects allows to set VCO noise specifications for M-QAM communications in the E-Band. Finally, the proposed frequency synthesizer architecture is disclosed.

2.1 Phase Noise in Oscillators: Basics and Metrics

It is well known that every physical oscillator system is affected by phase noise, i.e. random fluctuations in the phase of the generated waveform. As shown in Fig. 2.1, phase noise produces noise "skirts" around the carrier frequency in the waveform spectrum. Phase noise is quantified as $L(f) = v_n^2(f)/P_{sig}$, where $v_n^2(f)$ is the noise power spectral density (PSD) at an offset f from the carrier, and P_{sig} is the carrier signal power. The root-mean-square (RMS) phase fluctuation is given by $\sigma_{n,rms} = \sqrt{2\int L(f)df}$. A complete review of phase noise theory is beyond the scope of this dissertation, and extended literature has been made available in recent years. However, we introduce here some basic concepts that will be widely used in the following.

It has been first shown by Leeson in 1966 through experiments [39] that phase noise

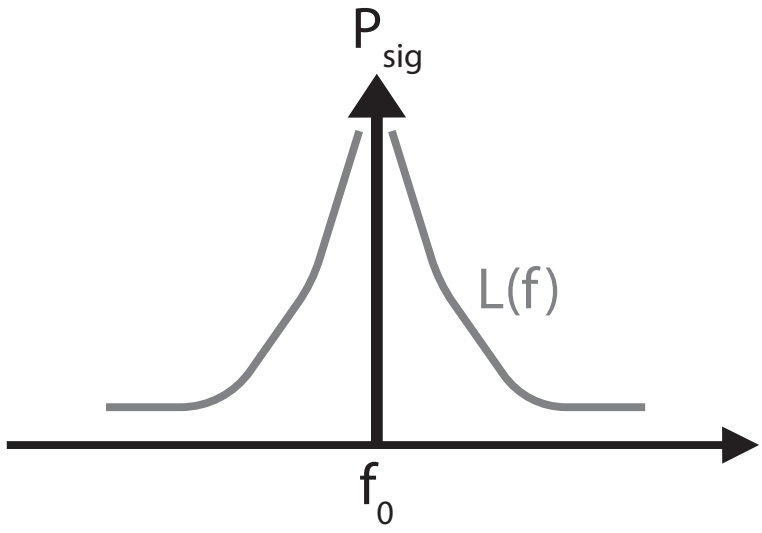

Figure 2.1: Spectrum of an oscillator waveform in presence of phase noise.

close to the carrier in LC-tank harmonic oscillators may be expressed as

$$L(f) = 10\log_{10}\left[F\frac{kTR_T}{A_0^2}\left(\frac{f_0}{2Qf}\right)^2\left(1+\frac{K}{f}\right)\right] \tag{2.1}$$

where f is the frequency offset from the carrier, f_0 is the oscillation frequency, k is Boltzmann's constant, T is the absolute temperature, Q is the tank's quality factor, A_0 is the differential oscillation swing, R_T is the tank's parallel resistance, F and K are parameters taking into account additional thermal and flicker noise, respectively, produced by noise sources other than the tank resistor (e.g. active transconductor). Although Leeson's analysis was a simple euristic derivation, eq. (2.1) has later been verified in formal terms. Amongst the many formal theories describing phase noise phenomena, Hajimiri's linear-time-variant (LTV) model [40], based on the Impulse Sensitivity Function (ISF), is the more widely used nowadays in the IC designer community.

It has been demonstrated that, neglecting bias-circuits noise and under reasonable assumptions, F only depends on the noise coefficient γ of active devices, regardless the oscillator topology [41]. Conversely, flicker-noise conversion into phase noise, quantified by the K parameter, is related to second-order effects, that depend on topology and implementation choices [42–47].

The performance of an oscillator is usually assessed through a figure of merit (FoM)

that normalizes phase noise to frequency and power consumption P_{DC} [48]:

$$FoM = L(f) + 20\log_{10}\left[\frac{f}{f_0}\right] + 10\log_{10}\left[\frac{P_{DC}}{1\text{mW}}\right] \tag{2.2}$$

Over the last years, many works have been published deriving analytical expressions and theoretical limitations of commonly-used integrated oscillator topologies [49–51] and novel oscillator arrangements [41, 52, 53]. Moreover, topology comparisons by virtue of FoM or FoM-related metrics were carried on [54, 55].
Finally, it was noticed that the FoM in eq. (2.2) does not take into account a metric which is fundamental when designing voltage-controlled oscillators (VCO): the frequency tuning range (TR). Therefore, another figure was introduced to take into account noise, power and tuning range [56]:

$$FoM_T = FoM - 20\log_{10}\left[\frac{TR}{10}\right] \tag{2.3}$$

As tuning range and tank quality factor are usually correlated, FoM_T is sometimes a fairer metric to compare VCO performance.

2.2 Impact of Phase Noise on SNR Degradation

In mm-Wave transceivers, where linearity constraints are more relaxed than in RF counterparts, phase noise requirements for the Local Oscillator are usually set by SNR degradation concerns [57]. Indeed, as shown in Fig. 2.2, phase noise in the LO produces a random rotation of the received constellation, degrading SNR.
In even-order M-QAM modulations, the Bit-Error Rate (BER) is linked to the SNR at the detector (SNR_{DET}) by the formula [58]

$$BER \approx \frac{1}{\log_2 M} 4\left(1 - \frac{1}{\sqrt{M}}\right) Q\left(\sqrt{\frac{3}{M-1} SNR_{DET}}\right) \tag{2.4}$$

where Q is the well-known Q-function. BER curves for QPSK, 16QAM, and 64QAM are plotted in Fig. 2.3. It can be noticed that if M is multiplied by four the SNR has to increase by ∼6 dB to achieve the same error probability. For example, assuming $BER = 10^{-6}$, the minimum SNR_{DET} requirement is approximately 13.6 dB for QPSK, 20.4 dB for 16QAM and 26.6 for 64QAM.
The impact of phase noise on the performance of a communication system employing

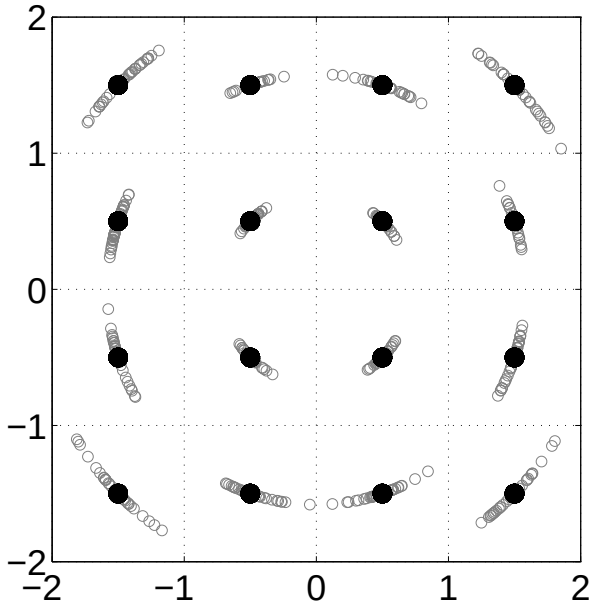

Figure 2.2: 16QAM constellation in presence of phase noise in the Local Oscillator.

M-QAM modulation has been studied in depth, leading to rather complex analytical models [59, 60]. Here, we provide a simplified and intuitive analysis to gain some useful insight for the circuit designer. Considering the block diagram shown in Fig. 2.4, assuming an ideal mixer and a noisy Local Oscillator, the LO integrated phase noise can be approximated as an uncorrelated noise process which degrades the SNR of the received signal (SNR_{RF}) according to [61, 62]

$$SNR_{DET} \approx \left[\frac{1}{SNR_{RF}} + \frac{1}{SNR_{LO}}\right]^{-1} \tag{2.5}$$

where $SNR_{LO} = [2\int L(f)df]^{-1}$ is the SNR of the local oscillator, namely the integrated phase noise. The SNR degradation resulting from the mixing process can be calculated from eq. (2.5) as a function of SNR_{LO}/SNR_{DET}:

$$\left[\frac{SNR_{DET}}{SNR_{RF}}\right]_{dB} = 10\log_{10}\left[1 - \frac{SNR_{DET}}{SNR_{LO}}\right] \tag{2.6}$$

As plotted in Fig. 2.5, to guarantee negligible noise degradation (i.e. < 0.5 dB) SNR_{LO} has to be at least 10dB higher than SNR_{DET}. As a result, at given BER,

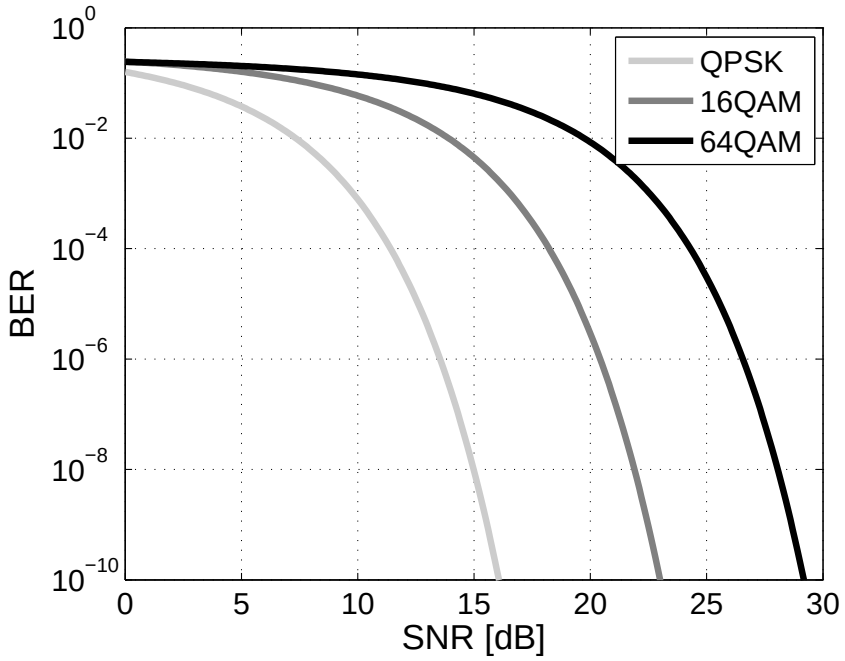

Figure 2.3: BER curves for QPSK, 16QAM and 64QAM according to eq. (2.4).

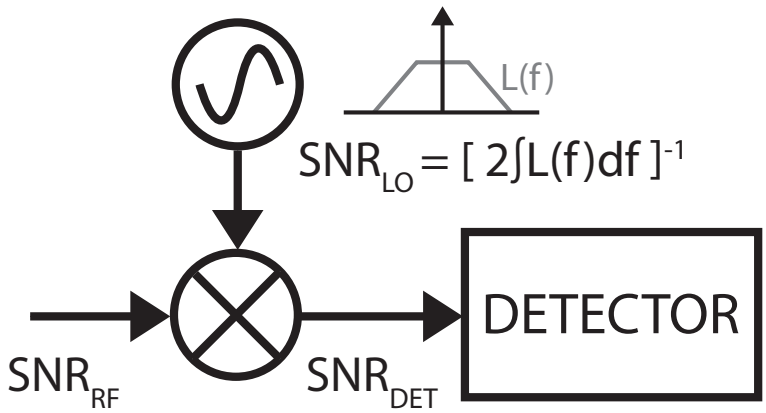

Figure 2.4: Simplified block diagram of the RX, stressing the LO noise contribution to the received SNR.

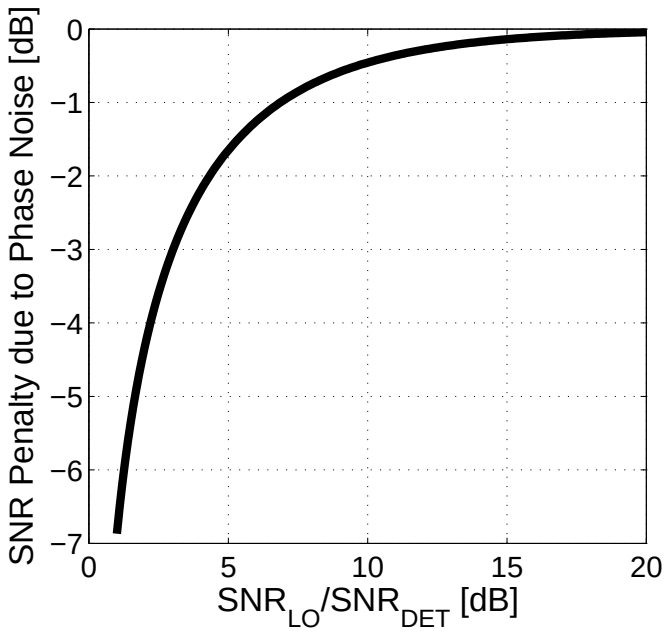

Figure 2.5: SNR degradation due to phase noise, as a function of SNR_{LO}/SNR_{DET}.

high-order modulations set a more challenging requirement for SNR_{LO}.
To derive VCO phase noise requirements from SNR_{LO}, we now need to consider how the oscillator noise is filtered in both the synthesizer and the receiver.

2.3 Phase Noise Filtering

Two main blocks perform filtering operations on the oscillator phase-noise spectrum in a transceiver. The first is the synthesizer PLL, which is assumed to be realized through a type-II analog III-order loop, whose bandwidth can be arbitrarily set. When performing system-level simulations, the in-band noise contribution of loop components was estimated through circuit simulations, while a phase noise spectrum from off-the-shelf low-noise crystal oscillators[1] was employed to model the reference noise.
The second key block is the carrier phase estimator, included in the baseband digital front-end. In PtP transceivers, this function is usually performed by a data-aided

[1]Three low-jitter crystal oscillators, with similar performance, were considered: the AE-X0A5XXXX-X family by NEL, Accusilicon X8/V8 and Rakon RXG1490L.

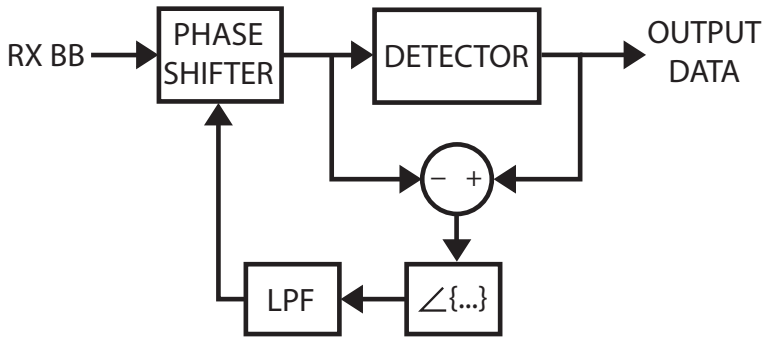

Figure 2.6: Data-aided phase tracking loop block diagram.

II-order tracking loop. As shown in Fig. 2.6, the loop evaluates the phase error of the received constellation and counter-rotates the baseband data stream through a digital phase shifter. Therefore, it acts as an additional PLL which high-pass filters the LO phase noise using the received data as a phase reference [63]. A wideband tracking loop is desirable to filter out most of the synthesizer phase noise. However, the loop bandwidth BW_{CT} is limited by two main issues. First, BW_{CT} has to be $\ll 1/T_S$, where $1/T_S$ is the symbol rate, for proper loop operation. Also, if the bandwidth is too high, a considerable amount of the AWGN channel noise is converted into phase noise, leading to an overall noise penalty [63].
In our case, $BW_{CT} \approx 750$ kHz was chosen as a suitable value according to system-level simulations. Since most of the phase noise filtering is performed by the tracking loop, simulations show that using a narrowband PLL (i.e. $BW_{PLL} < 100$ kHz) is beneficial. Indeed, this reduces the in-band noise contribution of loop components and crystal reference, that become significant at mm-Waves [64].

2.4 VCO Phase Noise Specifications

Simulated SNR_{LO}/SNR_{DET} is plotted in Fig. 2.7 versus VCO phase noise at 1MHz offset from an 80GHz carrier, assuming 250MHz channel bandwidth [25] for phase noise integration and SNR_{DET} equal to the minimum SNR requirement for $BER = 10^{-6}$ with the corresponding modulation. To keep SNR_{LO}/SNR_{DET} above 10 dB so as to make the oscillator noise contribution negligible, the VCO phase noise at 1MHz offset should be around -102dBc/Hz for 64QAM, -96dBc/Hz for 64QAM and -89dBc/Hz for QPSK. Therefore, also the oscillator noise specification depends

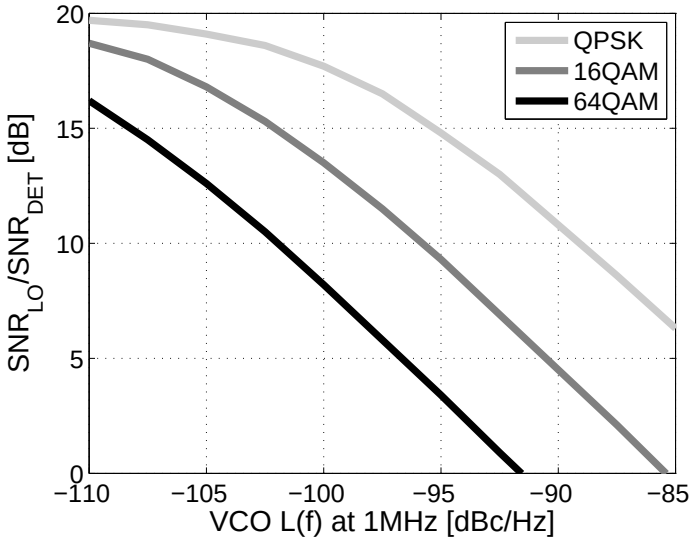

Figure 2.7: Simulated SNR_{LO}/SNR_{DET} versus VCO phase noise at 1MHz offset for different M-QAM modulations.

on the modulation order. The phase-noise specification for 64QAM is challenging for mm-Wave CMOS synthesizers, and requires to burn a significant fraction of the transceiver power in LO generation. Conversely, a synthesizer meeting 64QAM specifications would be widely over-designed when lower-order modulations are employed.

To conclude, since the VCO noise spectrum below BW_{CT} is high-pass filtered by the tracking loop, the design of the oscillator has to focus on minimizing phase noise above ∼1MHz offset. Furthermore, it is important to keep the flicker corner below BW_{CT}, where the tracking loop is effective.

2.5 mm-Wave VCO State of the Art

Much work has been done in the last decade to improve the performance of mm-Wave VCOs in CMOS and BiCMOS technologies. According to the conclusions drawn so far, two main aspects have to be taken into account when analyzing the state of the art. First, absolute phase noise performance in the E-Band, which is key to perform high-order modulations with negligible SNR degradation. Since only a few E-Band oscillators have been reported in literature compared to other mm-

Wave bands (e.g. 60 GHz), we considered here a broad spectrum of VCOs oscillating at different frequencies in the mm-Wave domain. For fair phase-noise comparison, for each considered oscillator we derived the equivalent phase noise performance at 1MHz offset from a 80GHz carrier, namely the target specification for E-Band synthesizer, through the formula

$$L_{eq,80G} = L_{meas} + 20\log_{10}\left[\frac{f_{0,meas}}{80\text{GHz}}\right] - 20\log_{10}\left[\frac{f_{meas}}{1\text{MHz}}\right] \tag{2.7}$$

where L_{meas} is the phase noise reported in literature, measured at an offset f_{meas} from a carrier frequency $f_{0,meas}$.

The second aspect is the oscillator power efficiency, evaluated through FoM and

Num	Reference
1	Nicolson, "Design and scaling of SiGe BiCMOS VCOs above 100GHz," BCTM 2006 [65]
2	Chu, "An 80GHz Wide Tuning Range Push-Push VCO with gm boosted full wave rectification," MWCL 2012
3	Vigilante, "An E-band Low-Noise Transformer-Coupled Quadrature VCO in 40 nm CMOS," ESSCIRC 2014 [35]
4	Padovan, "A SiGe Bipolar VCO for Backhaul E-band Communication Systems," ESSCIRC 2012 [37]
5	Liu, "A Low-Power K-Band CMOS VCO with Four-Coil Transformer Feedback," MWCL 2010
6	Wang, "A K-Band Low-Power Colpitts VCO With Voltage-to-Current Positive-Feedback Network in 0.18um CMOS," MWCL 2010
7	Nakamura, "A Push-Push VCO With 13.9-GHz Wide Tuning Range Using Loop-Ground Transmission Line for Full-Band 60-GHz Transceiver," JSSC 2012 [66]
8	Nakamura, "A 20-GHz 1-V VCO with Dual-transformer configuration and a pseudo-static divider," ESSCIRC 2009
9	Li, "A Colpitts LC VCO with Miller-Capacitance Gm Enhancing and phase noise reduction techniques," ESSCIRC 2011
10	Catli, "A 60 GHz CMOS combined mm-wave VCO/Divider with 10 GHz tuning range," CICC 2009
11	Chao, "Transformer-based dual-band VCO and ILFD for wide-band mm-wave LO generation," CICC 2013
12	Sun, "A Low-Phase-Noise 61 GHz Push-Push VCO with Divider Chain and Buffer in SiGe BiCMOS for 122 GHz ISM Applications," RFIC 2012 [67]
13	Yin, "A 57.5-90.1 GHz magnetically tuned multimode VCO," JSSC 2013
14	Kang, "A 100GHz Phase-Locked Loop in 0.13um SiGe BiCMOS process," RFIC 2011 [68]
15	Deng, "A Sub-Harmonic Injection-Locked Quadrature Frequency Synthesizer With Frequency Calibration Scheme for Millimeter-Wave TDD Transceivers," JSSC 2013
16	Lee, "A 75 GHz Phase Locked Loop in 90 nm CMOS Technology," JSSC 2008
17	Pohl, "A Low-Power Wideband Transmitter Front-End Chip for 80 GHz FMCW Radar Systems With Integrated 23 GHz Downconverter VCO," JSSC 2012
18	Wachi, "A 28GHz low-phase-noise CMOS VCO using an amplitude-redistribution technique," ISSCC2008 [69]
19	Chen, "W-band frequency synthesis using a Ka-band PLL and two different frequency triplers" RFIC 2011
20	Szortyka, "A 42mW 230fs-jitter sub-sampling 60GHz PLL in 40nm CMOS," ISSCC 2014
21	Zong, "A 60 GHz 25% tuning range frequency generator with implicit divider based on third harmonic extraction with 182 dBc/Hz FoM," RFIC2015 [70]

Table 2.1: State-of-the-art low-phase-noise mm-Wave VCO references for plots in Fig. 2.8 and 2.9.

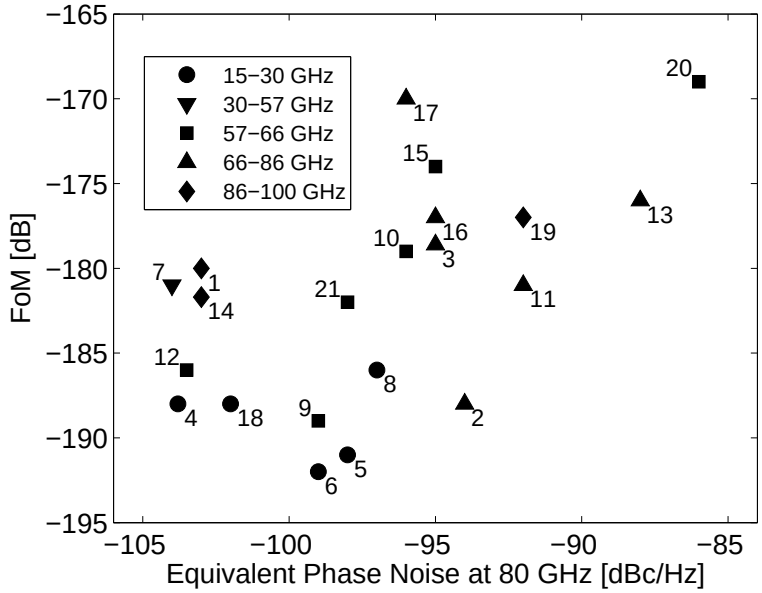

Figure 2.8: State-of-the-art oscillator FoM versus equivalent phase noise at 1MHz offset from 80 GHz. Different markers are used for different output frequency ranges.

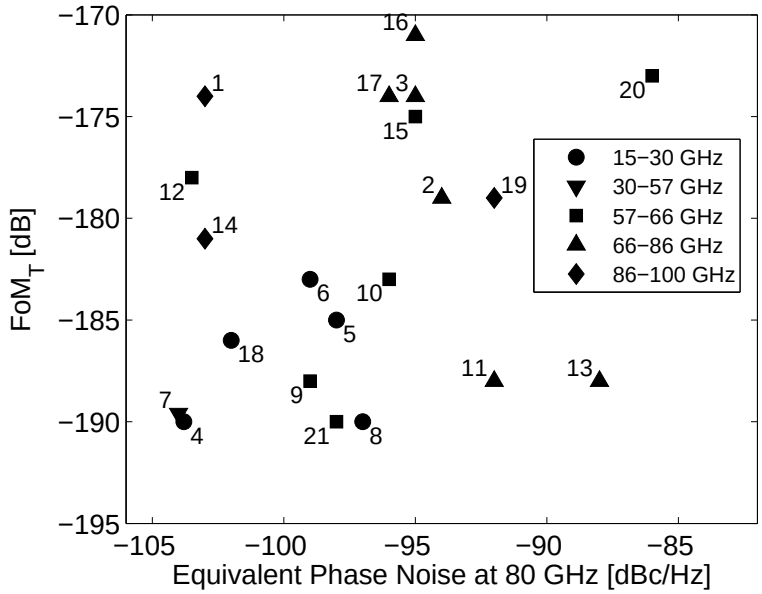

Figure 2.9: State-of-the-art oscillator FoM_T versus equivalent phase noise at 1MHz offset from 80 GHz. Different markers are used for different output frequency ranges.

FoM_T. In Fig. 2.8 and 2.9, FoM and FoM_T are reported, respectively, versus $L_{eq,80G}$ for high-performance mm-Wave VCOs reported in literature. In case of wide variations of the measured phase noise over the tuning range, an intermediate value between L_{min} and L_{max} was used as L_{meas}. Both fundamental-frequency VCOs and subharmonic oscillators followed by frequency multipliers were considered. In the latter case, the multiplier power consumption was included in the FoM calculation. Bibliography references are provided in table 2.1.

First, it can be observed that only a few VCOs achieve $L_{eq,80G}$ <-100 dBc/Hz. Most of them (i.e. ref. 1, 7, 12 and 14) are Colpitts oscillators in BiCMOS technology with high power supply (2.5-3 V) [65–68]. High V_{DD} can be exploited to maximize the oscillation swing, hence minimizing phase noise. Apart from ref. 7, the other VCOs feature a modest FoM_T, as a consequence of $TR < 10\%$, which is inadequate for E-Band applications. Reference 4, which is also a BiCMOS VCO with 3.3V supply, but based on a class-C topology, achieves very competitive FoM and tuning range, although at ∼20GHz only [37].

Reference 18 is the only CMOS VCO achieving $L_{eq,80G}$ <-100 dBc/Hz. It is a 28GHz oscillator exploiting a IV-order tank to maximize the swing with low supply (1.2 V) [69]. Although noise and power efficiency are good, it only achieves $< 7\%$ tuning range, too small for E-Band synthesizers. Also, noise performance varies by several dB over the tuning range.

To sum up, achieving <-100 dBc/Hz phase noise at 80GHz with good power efficiency and wide tuning range (i.e. $> 15\%$), as required by high-order-modulation E-Band transceivers, is very challenging for integrated VCOs. In the following, we will investigate design techniques to overcome performance limitations of state-of-the-art circuits, and achieve good performance with CMOS-compatible supply voltage.

2.6 Proposed Synthesizer Architecture

VCOs operating above ∼20 GHz suffer from severe phase noise degradations due to the poor quality factor of integrated capacitors at mm-Wave [71, 72]. Indeed, inductive quality factor rises with frequency, but it saturates to ∼30 above 20-30 GHz because of skin effect losses [73]. Conversely, capacitive Q decreases while frequency increases, and becomes the main source of losses at mm-Waves. As a result, as shown in Fig. 2.10, the overall quality factor of the LC tank starts to

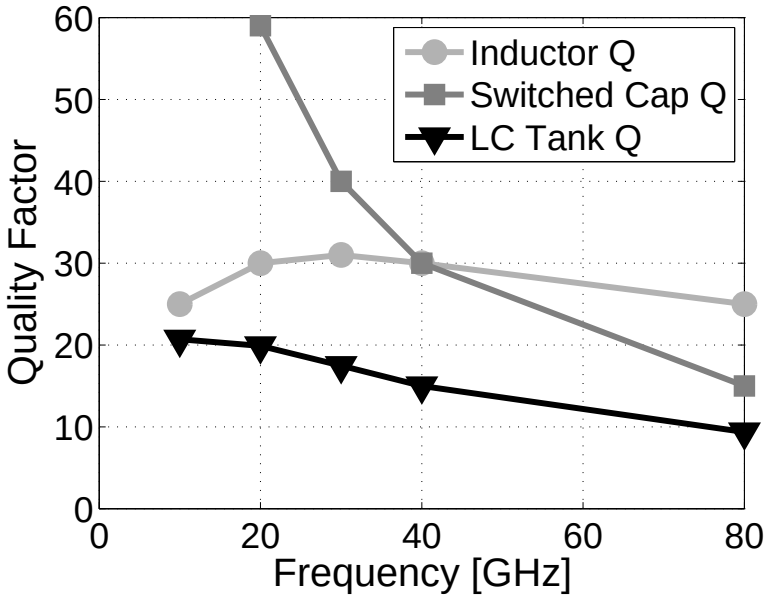

Figure 2.10: Simulated quality factor for integrated inductor, switched capacitor element and equivalent tank in BiCMOS 55nm technology.

significantly drop above 20 GHz, resulting in a phase noise penalty.

To maximize the LC-tank Q, the frequency synthesizer architecture in Fig. 2.11 is proposed. A ∼20GHz VCO, embedded in a PLL, is followed by a frequency multiplier by 4. This solution offers other additional advantages. First, a 20GHz layout considerably lowers the sensitivity to parasitics, resulting in a wider VCO tuning range. Also, one or more power-hungry pre-scaler stages can be avoided in the PLL chain, compensating the additional power required by the frequency multiplier. Finally, employing a subharmonic VCO allows to reduce the multiplication factor of the PLL, resulting in less in-band noise amplification.

The VCO has been designed with two targets. First, ultra-low phase noise with CMOS-compatible supply voltage, to achieve negligible SNR degradation in 64QAM communication. Second, power-efficient noise scaling, so as to reduce the power consumption when low-order modulations are adopted. A technique to achieve both targets using multi-core oscillators is presented in chapter 3.

The quadrupler has to provide a wideband transfer function (i.e. with >25% fractional bandwidth), in order to cover both 71-76GHz and 81-86GHz bands with some margin for process spreads. Design techniques to achieve broadband frequency mul-

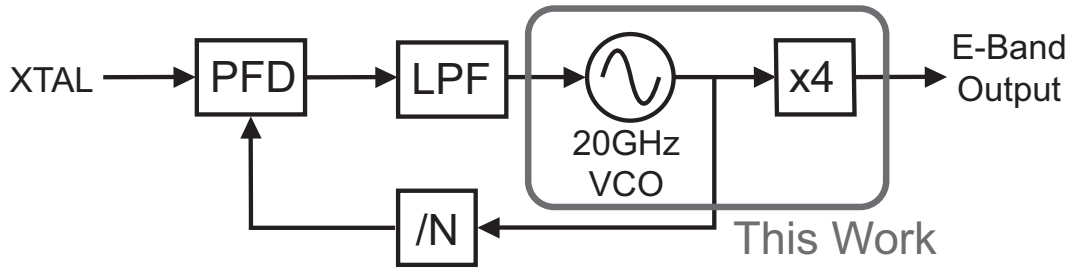

Figure 2.11: Proposed frequency synthesizer.

tiplication with low power consumption are discussed in chapter 4.

2.7 Conclusions

In this chapter, target phase noise specifications for frequency synthesizers in M-QAM E-Band communications were derived. Noise requirements depend on the modulation order, and they are very challenging for spectrally-efficient modulations (e.g. 64QAM) but fairly relaxed for simple modulations like QPSK. Therefore, in adaptive-modulation applications like E-Band PtP links, efficiently scaling noise and power in the LO according to the modulation order is a key feature.
Finally, the proposed synthesizer architecture was presented. It features a subharmonic PLL followed by a wideband frequency quadrupler. The oscillator is based on a multi-core topology, to achieve power-efficient phase noise scaling according to the system requirements.

Chapter 3

Noise-Scalable Multi-Core VCOs

In this chapter, the use of multi-core oscillator systems to perform power-efficient noise scaling and tunability, suitable for adaptive-modulation transceivers, is investigated. First, basic concepts of noise scaling are introduced, and the operating principle of the proposed multi-core oscillator is briefly described in an intuitive way. Later, an accurate analytical model is developed. The model provides useful insight on the effect of component mismatches on resistively-coupled multi-core oscillators. In conclusion, a 20GHz quad-core oscillator, to be employed in a frequency synthesizer for E-Band adaptive-modulation transceivers, is presented.

3.1 Noise Scaling in Oscillators

To better understand noise scaling in oscillators, eq. (2.1) may be rewritten replacing $A_0 = R_T I_{\omega 0}$, where $I_{\omega 0}$ is the fundamental-harmonic component of the tank current, and expressing $I_{\omega 0} = \eta_I I_{DC}$, where I_{DC} is the DC current drawn by the oscillator and η_I is a current-efficiency coefficient which depends on the oscillator topology [52]. This last relation holds assuming the transconductor is working in highly-nonlinear regime, a common case in electrical oscillators. Neglecting the flicker-noise contribution, phase noise may therefore be expressed as

$$L(f) = 10 \log_{10} \left[\frac{4kT}{R_T \eta_I^2 I_{DC}^2} \left(\frac{f_0}{2Qf} \right)^2 \right] \tag{3.1}$$

Scaling phase noise and power in an efficient way is not straightforward. Indeed, in eq. (3.1) phase noise and DC current do not trade linearly, and a current reduction

by a factor of N will lead to N^2 worse phase noise. Therefore, if current consumption is halved, the FoM is degraded by 3 dB.
The best FoM is obtained when I_{DC} is chosen such that the oscillation swing is maximized [74]. The maximum swing is set by the supply voltage V_{DD} and reliability issues, and can be written as $A_{0,max} = \eta_V V_{DD}$, where η_V is a voltage-efficiency parameter that depends on topology and technology [55, 74]. In the optimal operating condition $A_0 = A_{0,max}$, we may replace $R_T \eta_I^2 I_{DC}^2 = A_{0,max} \eta_I I_{DC} = \eta_V V_{DD} \eta_I I_{DC} = \eta_V \eta_I P_{DC}$. Eq. (3.1) and (2.2) can therefore be rewritten as

$$L_{MIN}(f) = 10 \log_{10} \left[\frac{4kT}{\eta_I \eta_V P_{DC}} \left(\frac{f_0}{2Qf} \right)^2 \right] \tag{3.2}$$

$$FoM_{MIN} = 10 \log_{10} \left[\frac{4kT}{\eta_I \eta_V} \frac{1}{Q^2} \right] \tag{3.3}$$

In [75], a technique for scaling noise and power by 6 dB at constant FoM, by changing the oscillator topology from N-only to complementary PN, is proposed. Indeed, complementary LC oscillators achieve the same FoM_{MIN} of an N-only VCO, but for different values of η_I and η_V, leading to 6dB lower power and 6dB higher noise in optimal operating condition [50]. The main drawback of the solution proposed in [75], if employed in the synthesizer architecture proposed in section 2.6, is that also A_0 is halved in the low-power mode. To guarantee the same output swing, the power consumption of the frequency multiplier should be increased, thus degrading the overall synthesizer efficiency. Also, noise and power cannot be scaled by $N \neq 4$.
Another way to scale noise in eq. (2.1) is by reducing the tank impedance R_T, while keeping the oscillation swing A_0 constant. $L(f)$ is linearly proportional to R_T, thus if the impedance is reduced by a factor of N, phase noise is scaled down by N. On the other hand, since $A_0 \sim R_T I_{DC}$, the DC current has to be increased by N in order to keep the oscillation swing constant. As a result, tank-impedance scaling allows to trade noise and power arbitrarily at constant FoM [76].

3.2 Multi-Core VCOs

To lower R_T without compromising the quality factor, the whole tank impedance, including reactive components, has to be scaled down. A way to do this is shown in Fig. 3.1.a, where an additional LC tank is connected through switches to the

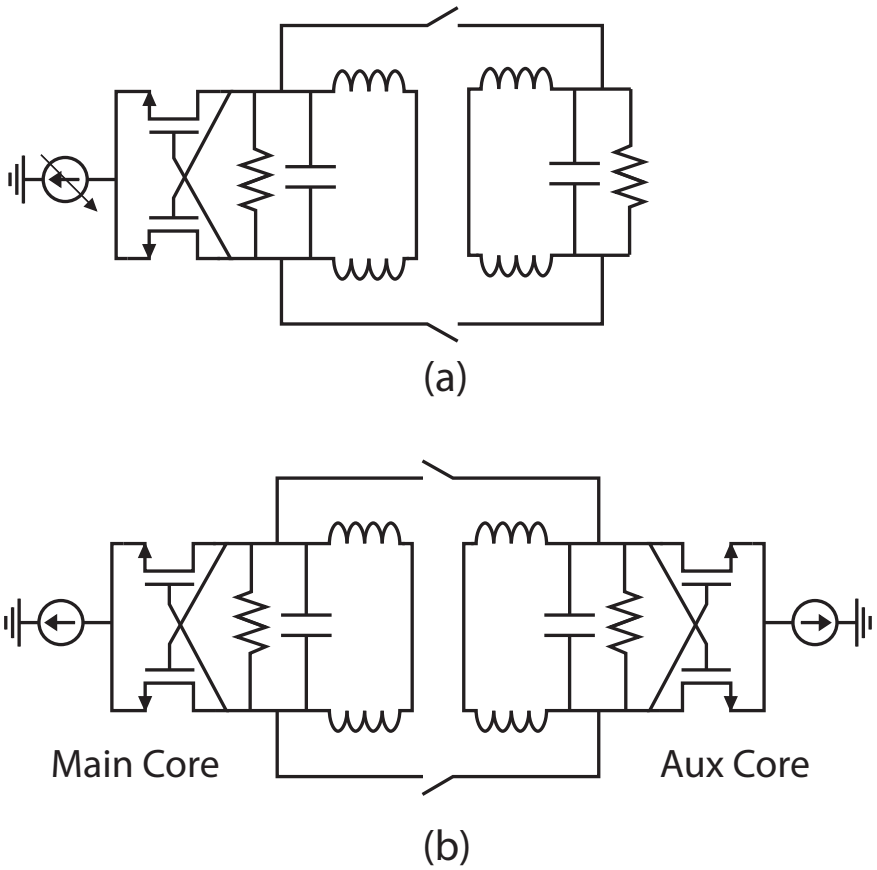

Figure 3.1: Multi-tank (a) and multi-core (b) noise-scalable oscillators.

main one. When the switches are turned on, the tank impedance is halved and, provided I_{DC} is doubled to keep A_0 constant, phase noise is reduced by 3 dB. The main drawback of this solution is that the oscillators loop gain drops when the tank impedance is reduced. Indeed, assuming square-law MOS transistors in the cross-coupled pair, the small-signal loop gain is given by

$$G_{LOOP} = g_m R_T = R_T 2\sqrt{k_{MOS}\frac{W}{L}\frac{I_{DC}}{2}} \tag{3.4}$$

where g_m is the cross-coupled pair's small-signal transconductance, k_{MOS} is the transistor's transconductance coefficient, and W and L are channel width and length respectively. If R_T is halved and I_{DC} is doubled, G_{LOOP} decreases by 3dB, resulting in potential start-up issues unless the loop gain is widely oversized.

A solution to the G_{LOOP} reduction problem, depicted in Fig. 3.1.b, is to replicate the

cross-coupled pair together with the LC tank. The idea can be extended to multiple oscillators. As a result, an in-phase-coupled multi-core oscillator is obtained, where auxiliary VCOs are selectively turned on and off and connected through switches in parallel with the main core, reducing the overall tank resistance. Since each core has auxiliary active devices that compensate the tank resistance scaling, A_0 and G_{LOOP} are independent of the number of cores.

The multi-core oscillator technique also allows to reach ultra-low phase noise by overcoming the limits of a single-core VCO [76]. Indeed, in eq. (2.1) Q depends on technology parameters, A_0 is limited to $\eta_V V_{DD}$, and at given quality factor R_T can only be reduced by shrinking the tank inductance L_T. When the tank inductor is reduced below a certain size (i.e. leading to ∼250pH at 20 GHz) the inductive Q starts to drop because of negative magnetic coupling between the two halves of the coil [76]. Conversely, by coupling more tanks in parallel the tank impedance can be arbitrarily reduced while keeping individual-core tanks optimized for maximum Q.

Multi-core LC VCOs employing in-phase coupling for noise reduction were presented before, although without noise-scaling capability. Both dual- and quad-core configurations, employing resistive [77], capacitive [78], magnetic [79], and active [80] coupling, were demonstrated at RF frequencies. In the mm-Wave domain, a magnetically-coupled 50GHz oscillator array was presented [81]. Regardless the coupling mechanism, a theoretical phase-noise reduction equal to $10\log_{10} N$, where N is the number of cores, is always achieved as long as the oscillators are coupled in phase. However, the type of coupling has influence on other factors such as stability of the in-phase mode, excess noise from the coupling devices and area. Magnetic coupling is attractive, since it allows to save area by overlapping the tank inductors. On the other hand, in a tunable VCO like the one we are proposing, it would be hard to achieve good isolation when auxiliary cores have to be turned off.

When introducing noise scaling by coupling the cores through switches, the *on* resistance of the switches has to be carefully selected in order to allow phase-noise reduction without penalizing the tuning range, especially at mm-Waves. Indeed, mismatches between the oscillator tanks lead to a phase-noise penalty that can be minimized by selecting a low coupling resistance, as will be shown in the following. On the other hand, this requires large switches, resulting in capacitive parasitics and tuning-range reduction. Furthermore, the switch capacitance changes between *on* and *off* states, resulting in a shift of the central frequency from single to quad-

core configuration. As a result, the effective tuning range where all the configurations overlap in frequency is reduced further.

3.3 Effect of Component Mismatches

In this section, we will present a model to describe the behavior of the multi-core oscillator in presence of component mismatch and finite coupling resistance. This allows to gain insights on the robustness of the adopted technique and to derive optimal and reliable design choices.

In the last decades, several studies have contributed to developing a complete and reliable theory to describe behavior and noise performance of injection locked oscillators [82] and actively-coupled quadrature VCOs (QVCOs) [83, 84]. On the other hand, literature on in-phase passively-coupled oscillator systems is scarce and fragmentary. In the 90s, York et al. [85–87] studied the behavior of arrays of coupled discrete microwave oscillators in presence of resonance frequency mismatch, and derived some useful results on locking range and noise performance. However, their analysis is based on the assumption of weak coupling between oscillators. Weak coupling allows to neglect amplitude dynamics and use Adler's equation [88] to describe the phase dynamics of the oscillator system. But, this is in general not the case for a resistively coupled oscillator, where coupling can be strong and, as will be shown in the following, amplitude dynamics plays a key role in noise degradation.

A more recent analysis, specifically related to in-phase resistively coupled oscillators, is provided in [76]. Here, by using a simple Linear Time-Invariant (LTI) model, authors show how a non-zero coupling resistance sets a finite bandwidth BW_C to the coupling transfer function between oscillators. As a consequence, phase noise is only scaled down up to an offset BW_C from the carrier. Although this effect has to be taken into account, it is a second-order limitation when compared to another effect, not modeled in [76], namely noise degradation in presence of oscillation frequency mismatch. Indeed, simulations show that, at least in the specific case of E-Band synthesizers, if switches are sized for robust operation with respect to component mismatch, in-band phase noise is always efficiently scaled.

To model the effect of mismatches, we developed a Linear Time-Variant (LTV) of a dual-core oscillator, leading to analytical expressions matching simulations and measurements with very good accuracy. The dual-core model is then extended to

the case of an N-core oscillator in an intuitive manner.

3.3.1 Dual-Core Oscillator

In analyzing component-mismatch effects in a dual-core oscillator, an analytical model is first developed, and expressions describing the system dynamics are derived. Secondly, phase noise contributions are calculated.

3.3.1.1 Oscillator Model

A single-ended resistively-coupled dual-core oscillator system, as shown in Fig. 3.2, is first considered. When the resonance frequencies f_{01} and f_{02} of the two LC tanks are the same, the oscillators are in phase at steady state, and no signal current flows in the coupling path. The oscillation amplitude is $A_0 = \eta_I I_{DC} R_T$, and the circuit behavior is independent of the coupling resistance RC.
If a mismatch $\Delta f_0 = f_{02} - f_{01}$ is present, the two oscillators may still be frequency-locked, and oscillate at a frequency f_{osc} between f_{01} and f_{02}. Both oscillators work off-resonance, meaning that $\angle Y_T \neq 0$, where Y_T is the tank admittance given by

$$Y_T = \frac{1}{R_T} + j\frac{Q}{R_T}\left(\frac{f_{osc}}{f_0} - \frac{f_0}{f_{osc}}\right) \approx \frac{1}{R_T} + j\frac{2Q}{R_T}\frac{f_{osc} - f_0}{f_0} \tag{3.5}$$

where j is the imaginary unit, and the approximation holds if $\delta f = f_{osc} - f_0 \ll f_0$. As a result, the tank voltage V_T and the tank current I_T are phase shifted, as shown in Fig. 3.3. The tank current in turn is the sum of two components. The first is the

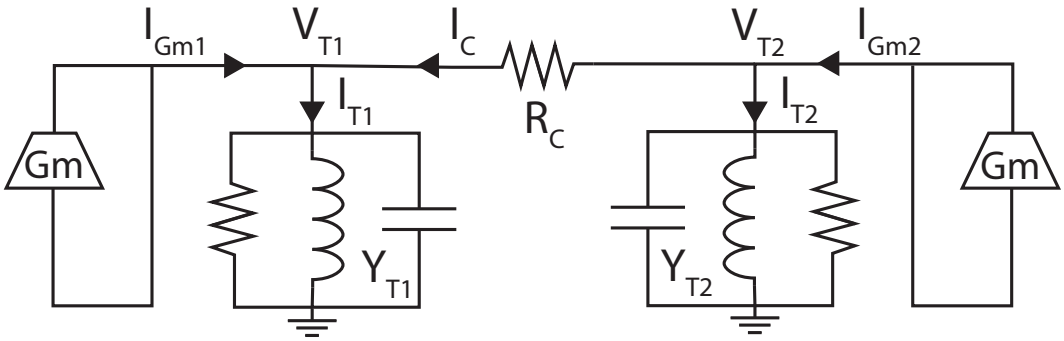

Figure 3.2: Schematic of a dual-core resistively-coupled oscillator system.

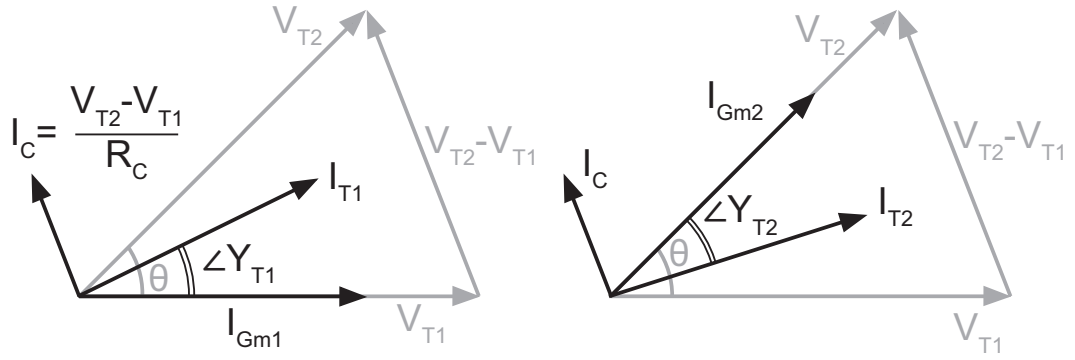

Figure 3.3: Voltage (grey) and current (black) phasors in the dual-core system.

current provided by the cross-coupled pair $I_{Gm} = \eta_I I_{DC}$, which neglecting second-order effects is in phase with V_T. The second is the coupling current I_C, given by $(V_{T2} - V_{T1})/R_C$. As shown in Fig. 3.3, $I_C \neq 0$ requires a non-null phase shift θ between the tank voltages V_{T1} and V_{T2}.

We now assume that the tanks have comparable quality factors $Q_1 \approx Q_2 = Q$, and that oscillators are biased with the same current $I_{DC1} = I_{DC2} = I_{DC}$, hence $|I_{Gm1}| = |I_{Gm2}|$. Referring to Fig. 3.2, the following equations link the LC-tank voltages and currents:

$$I_{T1} = I_{Gm1} + I_C \tag{3.6}$$

$$I_{T1} = V_{T1} Y_{T1} \tag{3.7}$$

$$I_{T2} = I_{Gm2} - I_C \tag{3.8}$$

$$I_{T2} = V_{T2} Y_{T2} \tag{3.9}$$

It can be verified that $|I_{Gm1}| = |I_{Gm2}|$ yields

$$\angle Y_{T1} = -\angle Y_{T2} \tag{3.10}$$

$$|V_{T1} Y_{T1}| = |V_{T2} Y_{T2}| \tag{3.11}$$

Now, provided $\Delta f_0 \ll f_0$ so that Y_T can be written with the approximated form in the right-hand term of eq. (3.5), $\angle Y_T$ is an odd function with respect to δf, while $|Y_T|$ is an even function of δf. As a result, eq. (3.10) yields $\delta f_1 = -\delta f_2$. Therefore, the oscillation frequency is given by

$$f_{osc} = \frac{f_{01} + f_{02}}{2} \tag{3.12}$$

Also, combining eq. (3.5), (3.11) and (3.12) we obtain $|V_{T1}| = |V_{T2}| = A$. Although rather intuitive, these simple results are important as they state that the oscillation frequency, and therefore also the phase shift $\angle Y_T$ between tank voltages and currents, does not depend on the coupling impedance.

Arbitrarily choosing tank voltage phases such that $V_{T1} = A$ and $V_{T2} = Ae^{j\theta}$, the coupling current is given by

$$I_C = \frac{2A}{R_C} \sin\frac{\theta}{2}\, e^{j\,\frac{\theta+\pi}{2}} \tag{3.13}$$

Replacing the previous calculations in eq. (3.6) yields

$$I_{T1} = \left[\eta_I I_{DC} - \frac{A}{R_C} + \frac{A}{R_C}\cos\theta\right] + j\frac{A}{R_C}\sin\theta \tag{3.14}$$

Combining eq. (3.5) and eq. (3.7), bearing in mind that $\angle V_{T1} = 0$, leads to the following expressions for magnitude and phase of I_{T1}

$$\angle I_{T1} = \angle V_{T1} + \angle Y_{T1} = \tan^{-1}\left[2Q\frac{f_{osc} - f_{01}}{f_{01}}\right] \approx \tan^{-1}\left[Q\frac{\Delta f_0}{f_0}\right] = \tan^{-1} K \tag{3.15}$$

$$|I_{T1}| = A|Y_{T1}| = \frac{A}{R_T}\sqrt{1 + K^2} \tag{3.16}$$

Where the variable $K = Q(\Delta f_0/f_0)$, was introduced for simplicity. We can now equate eq. (3.14) and (3.15-3.16) for phase and magnitude, leading respectively to

$$\frac{\sin\theta}{r\frac{\eta_I I_{DC}}{A}R_T - 1 + \cos\theta} = K \tag{3.17}$$

$$\left[\frac{\eta_I I_{DC}}{A}R_T + \frac{\cos\theta - 1}{r}\right]^2 + \left[\frac{\sin\theta}{r}\right]^2 = 1 + K^2 \tag{3.18}$$

where the variable $r = R_C/R_T$ was introduced. It is now useful to write $A = aA_0$, where A_0 is the oscillation swing in absence of frequency mismatch (i.e. when $I_C = 0$). It can then be noticed that $\eta_I I_{DC} R_T/A_0 = 1$, so eq. (3.17, 3.18) can be simplified as

$$\frac{\sin\theta}{\frac{r}{a} - 1 + \cos\theta} = K \tag{3.19}$$

$$\left[\frac{1}{a} + \frac{\cos\theta - 1}{r}\right]^2 + \left[\frac{\sin\theta}{r}\right]^2 = 1 + K^2 \tag{3.20}$$

This system can be solved analytically, leading to the following exact solutions for θ and a:

$$\theta = \sin^{-1}(Kr) \tag{3.21}$$

$$a = \left[1 + \frac{1}{r} - \sqrt{\frac{1-(Kr)^2}{r}}\right]^{-1} \tag{3.22}$$

Solutions exist provided two conditions, imposed by eq. (3.20) and (3.19) respectively, are satisfied:

$$r - \sqrt{1-(Kr)^2} < \frac{\sqrt{1+K^2}}{|K|} \tag{3.23}$$

$$r < \frac{1}{|K|} \tag{3.24}$$

It can be verified that eq. (3.24) is always a more stringent requirement than eq. (3.23). Therefore, the existence of solutions is guaranteed by eq. (3.24), which leads to the following expression for the locking range[1]:

$$\Delta f_{0,MAX} = \frac{f_0}{Qr} \tag{3.25}$$

[1]It is interesting to notice that, for every value of r, when $\Delta f_0 = \Delta f_{0,MAX}$ the tank voltages V_{T1} and V_{T2} are in quadrature. This may remind the behavior of an injection-locked oscillator, where the locking range is set by the condition of 90-degrees phase shift between the injected locking signal and the voltage waveform of the locked oscillator [82]. However, the condition imposed by eq. (3.25) is actually different since, when V_{T1} and V_{T2} are in quadrature, the injected signal I_C experience 45-degrees shift with respect to both tank voltages.

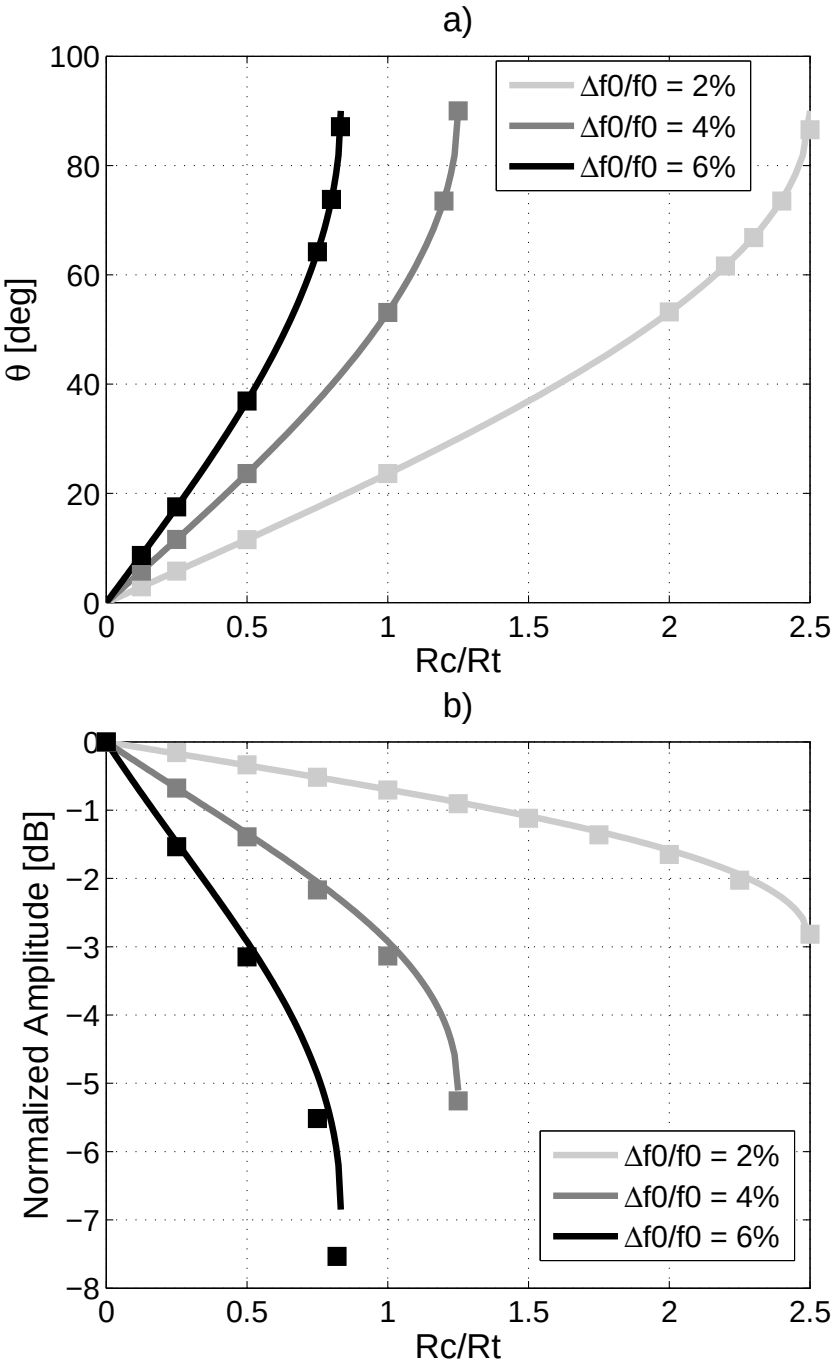

Figure 3.4: Phase shift between tank voltages (a) and amplitude reduction (b) in a dual-core resistively-coupled oscillator system with $Q = 20$: comparison between eq. (3.21-3.22) (solid lines) and circuit simulations (squares). Curves stop where the system loses locking.

To sum up, a resonance frequency mismatch between the cores causes a reduction of the oscillation swing and a phase difference between the oscillator voltage waveforms. Tank voltages are given by the following expressions

$$V_{T,1} = aA_0 \sin(2\pi f_{osc} t) \tag{3.26}$$

$$V_{T,2} = aA_0 \sin(2\pi f_{osc} t + \theta) \tag{3.27}$$

where a, θ and f_{osc} are expressed by eq. (3.22), (3.21) and (3.12) respectively. Both swing reduction and phase shift depend on R_C/R_T, and become negligible for $R_C \ll R_T$. The locking range is inversely proportional to $Q \cdot R_C/R_T$. The analysis can be easily extended to differential oscillators, where r is still the ratio between the coupling resistance and the single-ended tank resistance. Amplitude reduction and phase shifts calculated through eq. (3.22, 3.21) are plotted in Fig. 3.4 for an oscillator with $Q = 20$. The model matches very well circuit simulations.

To conclude, it is interesting to notice that one may be tempted by neglecting

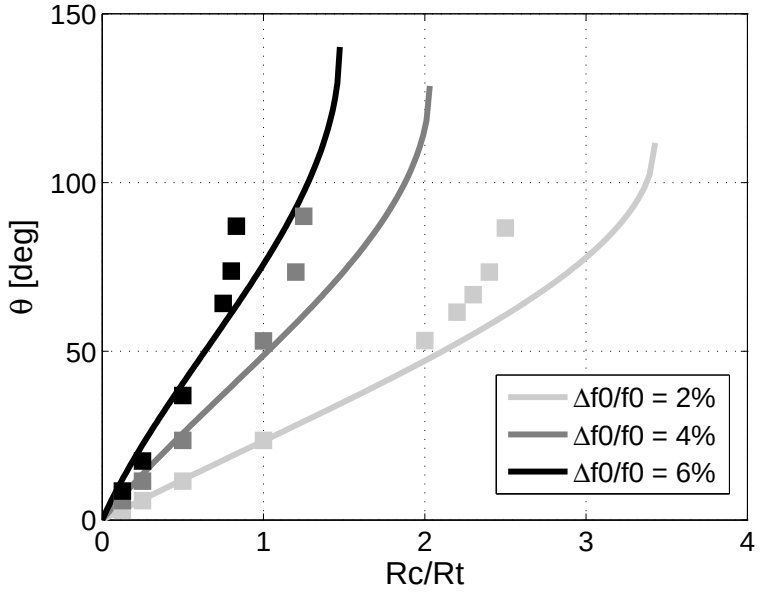

Figure 3.5: Phase shift between tank voltages in a dual-core resistively-coupled oscillator system with $Q = 20$: comparison between circuit simulations (squares) and simplified solution of eq. (3.19) assuming $a = 1$ (solid lines).

amplitude reduction effects, approximating $a \approx 1$ and solving eq. (3.19) without considering amplitude dynamics. This is a common practice in analysis on coupled oscillators (see for example [87]) as it allows to simplify calculations. However, it is found that in case of resistively coupled oscillators this procedure leads to incorrect expressions for θ and locking range, as shown in Fig. 3.5. Results only match eq. (3.21) for $r \to 0$ and $\Delta f_0/f_0 \ll 1$.

3.3.1.2 Phase Noise Analysis

The effect of both amplitude reduction and phase shift between tank waveforms on the oscillator phase noise is discussed in this section.

The effect of the amplitude reduction is evident from eq. (2.1), where replacing A_0 with $A = aA_0$ leads to a phase noise penalty proportional to $1/a^2$. This penalty can be compensated by increasing the tail current and restoring the oscillation swing. However, this will obviously worsen the oscillator FoM.

We may also expect phase shifts to have an impact on phase noise, as it happens for QVCOs [83, 84]. Indeed, circuit simulations show a noise penalty excess with respect to $1/a^2$. To analyze this effect, the Impulse Sensitivity Function (ISF) [40], which models how thermal noise is translated into phase noise, and the phase noise contributions from both the tank resistance and the active transconductor were calculated for the dual-core oscillator in Fig. 3.2. In all the following calculations, we will assume, as in most of the analysis concerning harmonic oscillators (see for example [40, 41, 83]) that the tank's quality factor is sufficiently high such that all higher harmonics of the current are filtered out and the oscillator voltage waveform is sinusoidal.

According to the theory from Hajimiri and Lee [40], phase noise in harmonic oscillators can be expressed as

$$L(f) = 10 \log_{10} \left[\frac{\sum_i N_{L,i}}{2(2f)^2 A^2 C_T^2} \right] \tag{3.28}$$

where, in a system including multiple resonators like the one we are considering, A and C_T are the oscillation amplitude across an arbitrary resonator and the corresponding tank capacitance. $N_{L,i}$, sometimes referred to as effective noise, is calculated as

$$N_{L,i} = \frac{1}{2\pi}\int_0^{2\pi} \Gamma_i^2(\varphi) i_{n,i}^2(\varphi) d\varphi \tag{3.29}$$

where $\varphi = 2\pi f_{osc} t$, t is time, $i_{n,i}^2$ is the noise PSD of the i-th noise source and Γ_i is the ISF calculated on the node where noise is injected. To calculate the integral in eq. (3.29), we first need to derive the tank ISF for a dual-core oscillator.

Tank ISF In [83], the tank ISF for a QVCO is analytically derived from the differential equations that describe the system behavior, by using the phase noise theory developed by Kärtner in [89]. The procedure can be extended to arbitrary-phase dual-core VCO systems.
A generic oscillator can be described by a nonlinear dynamic system in the form

$$\dot{\overline{x}} = F(\overline{x}, t, \overline{\xi}) \tag{3.30}$$

where $\overline{x}$ is the vector of state variables and $\overline{\xi}$ is the vector of noise sources. From Kärtner's theory, the ISF Γ_i at the i-th node a generic oscillator system can be derived as

$$\Gamma_i = 2\pi f_0 A y_i \tag{3.31}$$

where y_i is the i-th term of the solution of the system

$$\dot{\overline{y}}^T = -\overline{y}^T DF \tag{3.32}$$

and DF is derived from F as

$$DF_{ij} = -\left.\frac{\partial F_i}{\partial x_j}\right|_{\overline{x}=\overline{x}_0} \tag{3.33}$$

where $\overline{x}_0$ is the vector of state variables at steady state. Let us now consider the dual-core oscillator in Fig. 3.2, assuming a resonance frequency mismatch such that $f_{01} < f_{02}$. The state-variable vector is given by $x = [V_{C1}, I_{L1}, V_{C2}, I_{L2}]$, where $V_{C1,2}$ and $I_{L1,2}$ are voltages across capacitors and currents through inductors in the two cores. Eq. (3.30) may be written as

$$\dot{V}_{C1} = \frac{1}{C_1}\left[-\frac{V_{C1}}{R_1} + I_{Gm1}(V_{C1})\right] - \frac{I_{L1}}{C_1} + \frac{1}{C_1}\left[\frac{V_{C2} - V_{C1}}{R_C}\right] \tag{3.34}$$

$$\dot{I}_{L1} = \frac{V_{C1}}{L_1} \tag{3.35}$$

$$\dot{V}_{C2} = \frac{1}{C_2}\left[-\frac{V_{C2}}{R_2} + I_{Gm2}(V_{C2})\right] - \frac{I_{L2}}{C_2} - \frac{1}{C_2}\left[\frac{V_{C2} - V_{C1}}{R_C}\right] \tag{3.36}$$

$$\dot{I}_{L2} = \frac{V_{C2}}{L_2} \tag{3.37}$$

At steady state, $V_{C1,0} = V_{T1}$ and $V_{C2,0} = V_{T2}$ are given by eq. (3.26, 3.27), whereas $I_{L1,0}$ and $I_{L2,0}$ can be calculated by integrating eq. (3.35) and (3.37). As a result, $\overline{x}_0$ may be written as

$$V_{C1,0} = aA_0 \sin(\varphi) \tag{3.38}$$

$$I_{L1,0} = -\frac{aA_0}{\omega_{osc} L_1} \cos(\varphi) \tag{3.39}$$

$$V_{C2,0} = aA_0 \sin(\varphi + \theta) \tag{3.40}$$

$$I_{L2,0} = -\frac{aA_0}{\omega_{osc} L_2} \cos(\varphi + \theta) \tag{3.41}$$

where $\omega_{osc} = 2\pi f_{osc}$. Now, the DF matrix can be derived as in eq. (3.33). To simplify calculations, we assume that $I_{Gm}(V_C)$ is a square wave in phase with V_C, which according to simulations is still reasonable at 20GHz f_{osc}. Therefore, $\partial I_{Gm}/\partial V_C$ can be calculated as [83]

$$\frac{\partial I_{Gm,1}}{\partial V_{C,1}} = \frac{\pi}{2}\frac{1}{\omega_{osc} a R_1}\left[\delta(\varphi) + \delta\left(\varphi - \frac{\pi}{2}\right)\right] \tag{3.42}$$

$$\frac{\partial I_{Gm,2}}{\partial V_{C,2}} = \frac{\pi}{2}\frac{1}{\omega_{osc} a R_2}\left[\delta(\varphi + \theta) + \delta\left(\varphi + \theta - \frac{\pi}{2}\right)\right] \tag{3.43}$$

where δ is Dirac's delta function. The system (3.32) can then be written as

$$\dot{y}_{C1} = y_{C1}\frac{1}{C_1}\left[\frac{1}{R_1} + \frac{1}{R_C} - \frac{\partial I_{Gm,1}}{\partial V_{C,1}}\right] - y_{L1}\frac{1}{L_1} - y_{C2}\frac{1}{R_C C_2} \tag{3.44}$$

$$\dot{y}_{L1} = y_{C1}\frac{1}{C_1} \tag{3.45}$$

$$\dot{y}_{C2} = -y_{C1}\frac{1}{R_C C_1} + y_{C2}\frac{1}{C_2}\left[\frac{1}{R_2} + \frac{1}{R_C} - \frac{\partial I_{Gm,2}}{\partial V_{C,2}}\right] - y_{L2}\frac{1}{L_2} \tag{3.46}$$

$$\dot{y}_{L2} = y_{C2}\frac{1}{C_2} \tag{3.47}$$

We now need some guess on the mathematical form of the y_i functions. Functions y_{C1} and y_{C2} are proportional to the ISF for tank voltage noise (see eq. (3.31)). In an ideal single-core harmonic VCO, the tank ISF is a sinusoidal waveform in quadrature with the tank voltage [40]. On the other hand, it has been verified that in specific multi-core oscillators, i.e. QVCOs, it experiences phase shifts with respect to quadrature [83]. In the case we are considering, a guess on the form of the ISF was derived through circuit simulations using the technique described in [90]. Neglecting high-order harmonics, it is found that y_C functions have the form

$$y_{C1} = B\cos(\varphi + \psi) \tag{3.48}$$

$$y_{C2} = B\cos(\varphi + \theta - \psi) \tag{3.49}$$

where B and ψ are unknown parameters which vary with mismatch and coupling resistance. It is interesting to notice from eq. (3.48, 3.49) that, unlike in QVCOs, the ISFs of the two tanks in a resistively-coupled dual-core oscillator experience opposite-polarity phase shifts with respect to the tank voltage waveform. It is also verified that y_C functions with equal phase shift for both tanks, like the ones derived for QVCOs in [83], do not solve eq. (3.32) for the system we are considering.
The y_L functions can be calculated by replacing eq. (3.48, 3.49) in eq. (3.45, 3.47), yielding

$$y_{L1} = \frac{B}{\omega_{osc} C_1}\sin(\varphi + \psi) \tag{3.50}$$

$$y_{L2} = \frac{B}{\omega_{osc} C_2}\sin(\varphi + \theta - \psi) \tag{3.51}$$

We may now replace eq. (3.48-3.51) in eq. (3.44-3.47), integrate both terms as in

[83] and solve the equation to find ψ. As a result, the following equation is derived

$$K\cos(\varphi+\psi)=\left(1+\frac{1}{r}\right)\sin(\varphi+\psi)-\frac{1}{a}\cos\psi\sum_{n\ odd}\frac{\sin(n\varphi+\psi)}{n}+ \\ -\frac{1}{rc}\sin(\varphi+\theta-\psi) \tag{3.52}$$

where $c = C_2/C_1$. The square wave in eq. (3.52) can be approximated with its fundamental harmonic, leading to

$$K\cos(\varphi+\psi)=\left(1+\frac{1}{r}\right)\sin(\varphi+\psi)-\frac{1}{a}\cos\psi\sin\varphi-\frac{1}{rc}\sin(\varphi+\theta-\psi) \tag{3.53}$$

Approximating $c \approx 1$, solving eq. (3.53) yields

$$\psi=\tan^{-1}\left[\frac{2K}{1+\frac{1}{r}+\frac{\sqrt{1-(Kr)^2}}{r}}\right] \tag{3.54}$$

The B parameter can then be calculated by using the normalization condition $\overline{x}^T\cdot\overline{y} = 1$ from Kärtner's theory [83]. Replacing eq. (3.38-3.41) and (3.48-3.51) for $\overline{x}$ and $\overline{y}$ and approximating $f_{01}^2/f_{osc} \approx f_{02}^2/f_{osc} \approx f_{osc}$ yields

$$B=\frac{1}{NaA_0\omega_{osc}\cos\psi} \tag{3.55}$$

where N is the number of single-ended tanks in the oscillator system [83], i.e. $N = 2$ in the case we are considering, and $N = 4$ for a differential dual-core oscillator. Therefore, from eq. (3.31), (3.48-3.49) and (3.54-3.55) the tank ISFs for the dual-core oscillator system may be written as

$$\Gamma_1=\frac{1}{N\cos\psi}\cos(\varphi+\psi) \tag{3.56}$$

$$\Gamma_2=\frac{1}{N\cos\psi}\cos(\varphi+\theta-\psi) \tag{3.57}$$

As verified in Fig. 3.6, these equations agree very well with circuit simulations. To sum up, it can be observed that **in a resistively-coupled dual-core oscillator the ISF is no more in quadrature with the tank voltage in presence of**

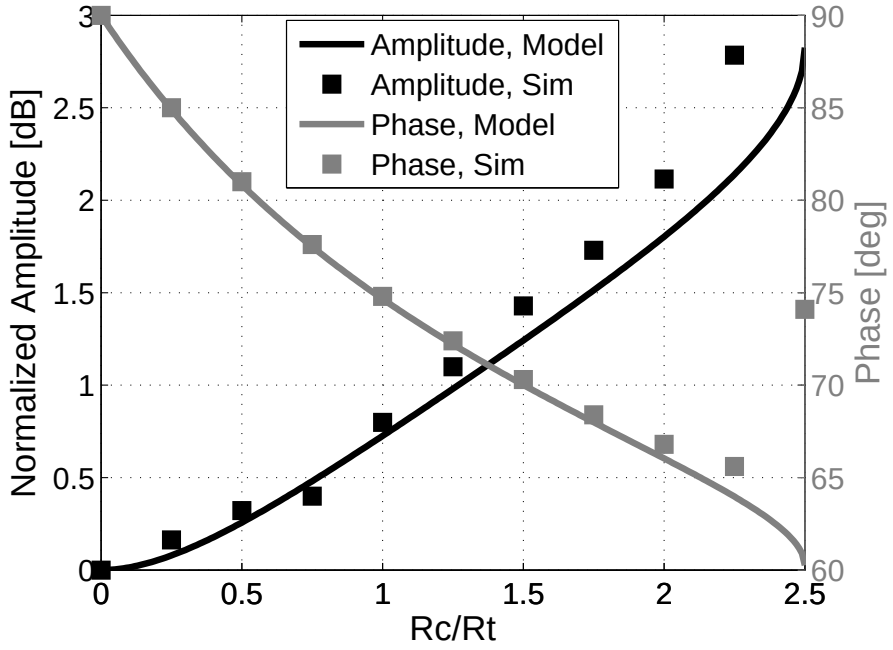

Figure 3.6: Tank ISF fundamental-harmonic phase and magnitude in a resistively-coupled dual-core oscillator with $\Delta f_0/f_0 = 2\%$ and $Q = 20$: comparison between eq. (3.56) and circuit simulations.

mismatch and non-zero coupling resistance. Although the expression for ψ in eq. (3.54) is cumbersome, it can be verified that the phase deviation ψ from quadrature converges to 0 for both $\Delta f_0 \to 0$ and $r \to 0$.

Tank Resistor Phase Noise Contribution We may now calculate the phase noise contribution of the tank resistors $N_{L,R}$, by replacing eq. (3.56) and (3.57) in eq. (3.29) and expressing $i_{n,R}^2 = 4kT/R$. Approximating $R_1 \approx R_2 = R_T$, the following result is obtained:

$$N_{L,R1} = N_{L,R2} = \frac{4kT}{R_T}\frac{1}{2\pi}\int_0^{2\pi}\left[\frac{1}{N\cos\psi}\cos(\varphi+\psi)\right]^2 d\varphi = \frac{2kT}{R_T}\frac{1}{N^2\cos^2\psi} \quad (3.58)$$

Coupling Resistor Phase Noise Contribution The tank resistor injects a noise current $i_{n,C}$ in both tanks. Since the resistor is floating, the noise current is injected in the tanks with opposite polarity. It it therefore rather intuitive to

understand that, provided $Y_{T1} \approx Y_{T2}$, $i_{n,C}$ will induce opposite, fully-correlated phase fluctuations in the two tanks. Considering the whole dual-core system, the two effects cancel each other, and the coupling resistor does not contribute to phase noise. This behavior is verified by circuit simulations.

Transconductor Phase Noise Contribution Calculation of the phase-noise contribution of the transconductor is more involved, since the time-variant transconductance $G_m(t)$ yields a cyclo-stationary noise PSD $i^2_{n,Gm}$. To proceed with calculations, we generalize the procedure in [41] removing two assumptions, namely the oscillator working at resonance and the ISF being in quadrature with the tank voltage. Instead, we assume that tank voltage waveforms are described by eq. (3.26, 3.27), and the ISFs are still sinusoidal, but shifted by an arbitrary angle with respect to the tank voltage, as in eq. (3.56, 3.57). As in [41], we start assuming that the current flowing in the cross-coupled pair is a generic periodic function whose Fourier series representation is

$$I_{Gm} = \sum_n I_n \sin(n\varphi + \phi_n) \tag{3.59}$$

where I_n and ϕ_n are arbitrary parameters. The noise PSD of the transconductor can be written as

$$i^2_{n,Gm} = 4kT\gamma G_m(t) = 4kT\gamma \frac{\partial I_{Gm}}{\partial V_T} = 4kT\gamma \frac{\sum_n nI_n \cos(n\varphi + \phi_n)}{aA_0 \cos\varphi} \tag{3.60}$$

Replacing (3.56) and (3.60) in (3.29) yields

$$N_{L,Gm} = \frac{4kT\gamma}{N^2 \cos^2\psi} \frac{1}{aA_0} \frac{1}{2\pi} \int_0^{2\pi} \frac{\sum_n nI_n \cos(n\varphi + \phi_n)}{\cos\varphi} \cos^2(\varphi + \psi) d\varphi \tag{3.61}$$

Expanding the trigonometric functions and integrating over $[0, 2\pi]$, eq. (3.61) can be rewritten as

$$\begin{aligned} N_{L,Gm} = & \frac{4kT\gamma}{N^2 \cos^2\psi} \left\{ \frac{I_{\omega 0}}{2aA_0} \left[\left(\cos^2\psi - \sin^2\psi\right) \cos\phi_1 + \sin 2\psi \cdot \sin\phi_1 \right] + \right. \\ & \left. + \sin^2\psi \frac{1}{2\pi} \int_0^{2\pi} G_m(\varphi) d\varphi \right\} \end{aligned} \tag{3.62}$$

We may now introduce again the reasonable assumption that the fundamental harmonic of the transconductor current is in phase with the tank voltage, namely $\phi_1 = 0$. As a result, eq. (3.62) is simplified as

$$N_{L,Gm} = \frac{4kT\gamma}{N^2 \cos^2\psi}\left[\frac{I_{\omega 0}}{2aA_0}\left(\cos^2\psi - \sin^2\psi\right) + \sin^2\psi \frac{1}{2\pi}\int_0^{2\pi} G_m(\varphi)d\varphi\right] \tag{3.63}$$

It can be easily verified that replacing (3.57) and (3.60) in (3.29) leads to the same result for tank 2. If $\psi = 0$, eq. (3.63) reduces to eq. (A8) in [41], which implies $N_{L,Gm} = \gamma N_{L,R}$ regardless any other property of the transistor. Conversely, it is interesting to observe that if the ISF is not in quadrature with the tank voltage, that is $\psi \neq 0$, no result on $N_{L,Gm}/N_{L,R}$ being independent of the $G_m(\varphi)$ function can be derived. This is consistent with results presented in [83, 84] for the specific case of QVCOs.

To proceed with calculations, we consider then (as we already did to derive eq. (3.44, 3.46)) the specific case of hard-switching transconductor, where I_{Gm} is a square wave toggling between 0 and $2I_{DC}$. This means the transconductor is only on during zero crossings, and $G_m(\varphi)$ can be written as

$$G_{m,HS} = \frac{I_{DC}}{aA_0}\left[\delta(\varphi) + \delta\left(\varphi + \frac{\pi}{2}\right)\right] = \frac{\pi}{2}\frac{I_{\omega 0}}{aA_0}\left[\delta(\varphi) + \delta\left(\varphi + \frac{\pi}{2}\right)\right] \tag{3.64}$$

Under the hard-switching assumption, the integral in eq. (3.63) can be easily solved and the expression can be simplified as

$$N_{L,Gm,HS} = \frac{4kT\gamma}{N^2\cos^2\psi}\frac{I_{\omega 0}}{2aA_0}\cos^2\psi = \frac{2kT\gamma}{N^2}\frac{I_{\omega 0}}{aA_0} = \frac{2kT}{R_T}\frac{\gamma}{(aN)^2} \tag{3.65}$$

where $A_0 = I_{\omega 0}R_T$ was used to derive the last term. Combining eq. (3.65) and (3.58), we can now express the ratio between noise contribution of active transconductor and tank losses for a hard-switching dual-core oscillator as

$$\frac{N_{L,Gm}}{N_{L,R}} = \gamma\frac{\cos^2\psi}{a} \tag{3.66}$$

as verified by simulations in Fig. 3.7. It can also be observed that, if $\Delta f_0/f_{osc}$ in the

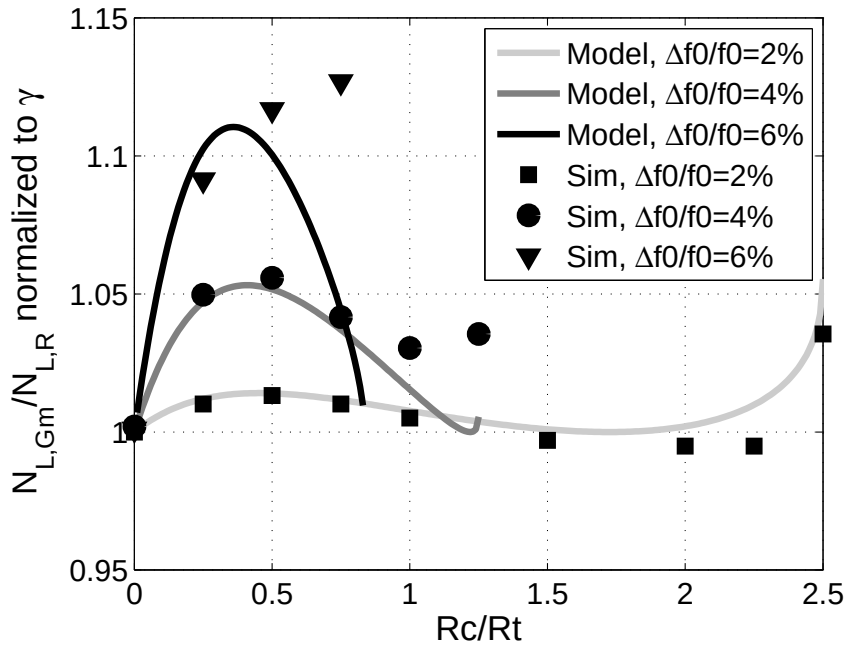

Figure 3.7: Phase noise contributions from transconductor and tank resistor, normalized to γ, vs R_C/R_T for different values of frequency mismatch, with $Q = 20$. Comparison between eq. (3.66) and circuit simulations.

order of some percents, $\cos^2 \psi/a \approx 1$. Therefore, for small mismatches the result in [41] still holds in first approximation.

Bias Circuits Phase Noise Contribution Although they are not included in the simplified model in Fig. 3.2, bias circuits (e.g. the tail current source) can contribute to phase noise [91]. However, by properly choosing the topology (e.g. class-C and class-B with tail filter) the bias contribution to phase noise can be efficiently rejected [41, 92].

To model this effect in a multi-core oscillator, the ISF should be calculated where the bias noise is injected, i.e. for example, for a current-biased differential cross-coupled oscillator, on the tail node T, as shown in Fig. 3.8. Although we did not perform calculations, we verified through circuit simulations that the magnitude of the tail-node ISF in a dual-core VCO does not significantly depend on either frequency mismatch and coupling resistance, as shown in Fig. 3.9. Therefore, the current-source phase noise contribution is not expected to increase with mismatches.

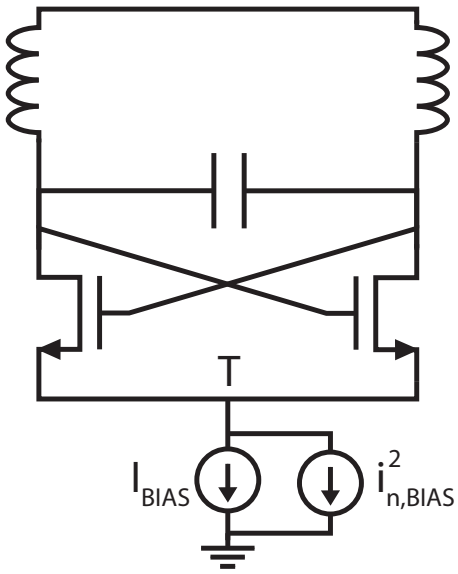

Figure 3.8: Current-source noise injection in a current-biased differential cross-coupled oscillator.

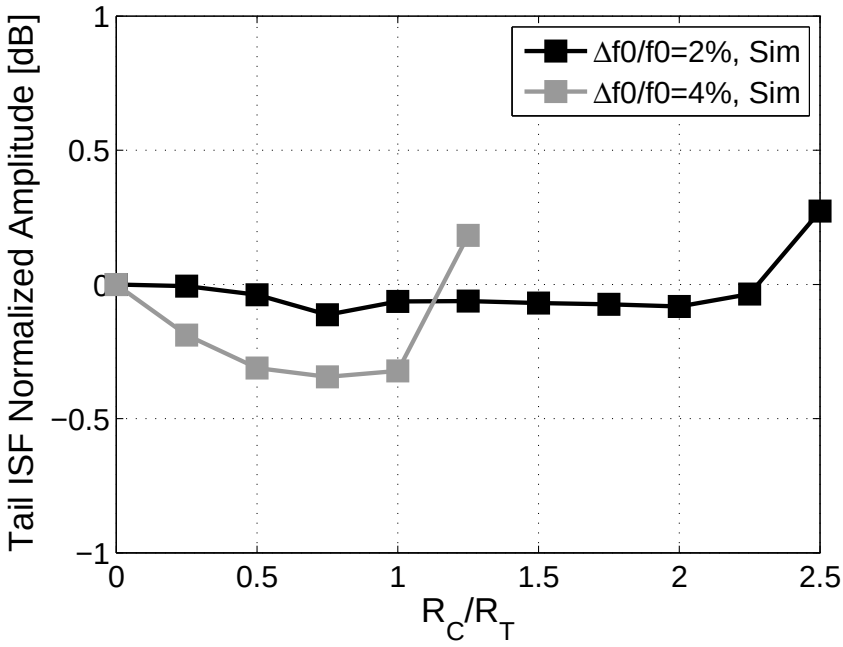

Figure 3.9: Simulated magnitude of the 2nd-harmonic component of the tail-node ISF for a dual-core current-biased differential cross-coupled oscillator in presence of mismatch and finite coupling resistance. Curves stop where the oscillator system loses locking.

Overall Phase Noise Neglecting bias circuits, we may now replace eq. (3.58) and (3.65) in eq. (3.28) to compute the overall phase noise of the dual-core oscillator. Approximating $\cos^2\psi \approx a$, the following expression is derived:

$$L_{2Core}(f) = 10\log_{10}\left[\frac{1}{2}\frac{4kTR_T}{A_0^2}\left(\frac{f_{osc}}{2Qf}\right)^2\frac{1}{a^3}(1+\gamma)\right] \tag{3.67}$$

Finally, the dual-core phase noise in eq. (3.67) can be compared to the one of a single-core oscillator, namely eq. (2.1). Replacing $F = 1+\gamma$ in eq. (2.1) according to [41], the following result is deduced:

$$L_{2Core}(f) \approx L_{1Core}(f) - 3\text{ dB} - 30\log_{10} a = L_{2Core,Ideal}(f) - 30\log_{10} a \tag{3.68}$$

To sum up, it is found out that **phase effects contribute to an additional phase noise penalty approximately proportional to $1/a$**. This penalty is only related

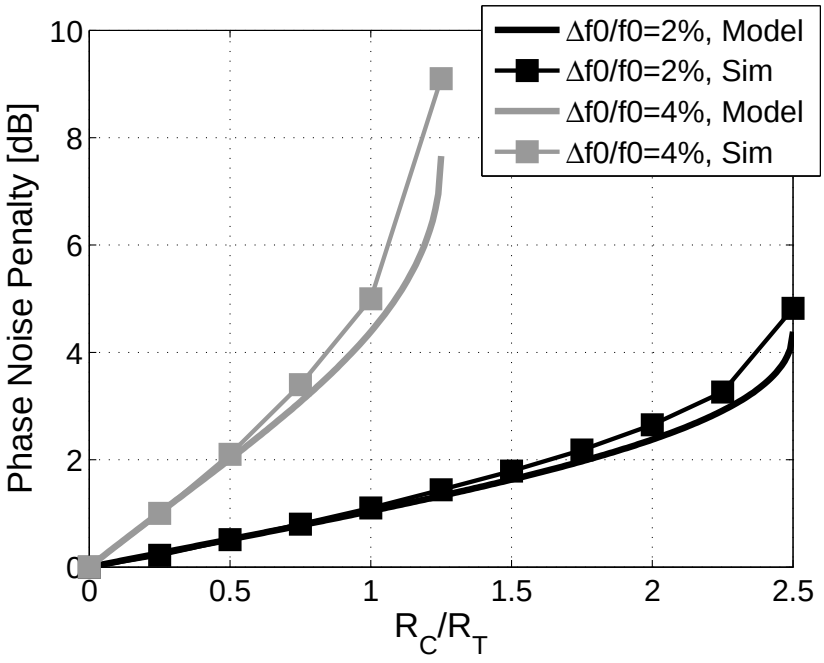

Figure 3.10: $1/f^2$ phase noise penalty for a dual-core oscillator system with $Q = 20$ in presence of mismatch and finite coupling resistance. Comparison between results from eq. (3.68) (solid lines) and circuit simulations (squares).

to changes in the ISF, therefore it cannot be compensated in any way by increasing the amplitude. Eq. (3.68) is compared with simulations in Fig. 3.10, where the phase noise penalty vs R_C/R_T with 2% and 4% mismatch is plotted, with very good agreement. Note how **the noise penalty can amount to several dB for high R_C/R_T values, thus causing oscillator coupling to be useless or even detrimental**. Therefore, mismatch effects have to be carefully taken into account, and correctly sizing the coupling switches is key. Simulations also show a $1/f^3$ noise penalty, as in the case of QVCOs [44]. This penalty rises with tank mismatch but becomes negligible as well for low R_C/R_T values.

3.3.2 N-Core Oscillator

The dual-core model allows to gain useful insight to analyze N-core systems, where each core is connected to more than one oscillator. As shown in Fig. 3.11, the current $I_{C,n}$ required to shift the oscillation frequency of the n-th tank from resonance is provided by the adjacent cores and satisfies

$$I_{C,n} = I_{T,n} - I_{Gm,n} = Y_{T,n}V_{T,n} - I_{Gm,n} \approx \left[\frac{1}{R_T} + j\frac{2Q}{R_T}\frac{\delta f_n}{f_{0,n}}\right] A - I_{Gm,n} \tag{3.69}$$

where $\delta f_n = f_{osc} - f_{0,n}$ and $f_{0,n}$ is the resonance frequency of the n-th tank. For simplicity, it was arbitrarily assumed that the tank voltage waveform $V_{T,n} = A$ is purely real. Expressing $A = aA_0 = aI_{Gm,n}R_T$, eq. (3.69) can be simplified as

$$I_{C,n} = \frac{A_0}{R_T}\left[(a-1) + ja2Q\frac{\delta f_n}{f_{0,n}}\right] \tag{3.70}$$

Now, we consider for simplicity the case of the oscillator being far from the locking-range limit, namely $a \approx 1$. Thus, the coupling current required by the n-th tank can be approximated as

$$I_{C,n} \approx j\frac{A_0}{R_T}2Q\frac{\delta f_n}{f_{0,n}} \tag{3.71}$$

An interesting implication of eq. (3.71) is that each oscillator behaves as a current source which sinks or injects a current proportional to the mismatch between its resonance frequency and the overall oscillation frequency of the system. KCL implies $\sum_n I_{C,n} = 0$, from which

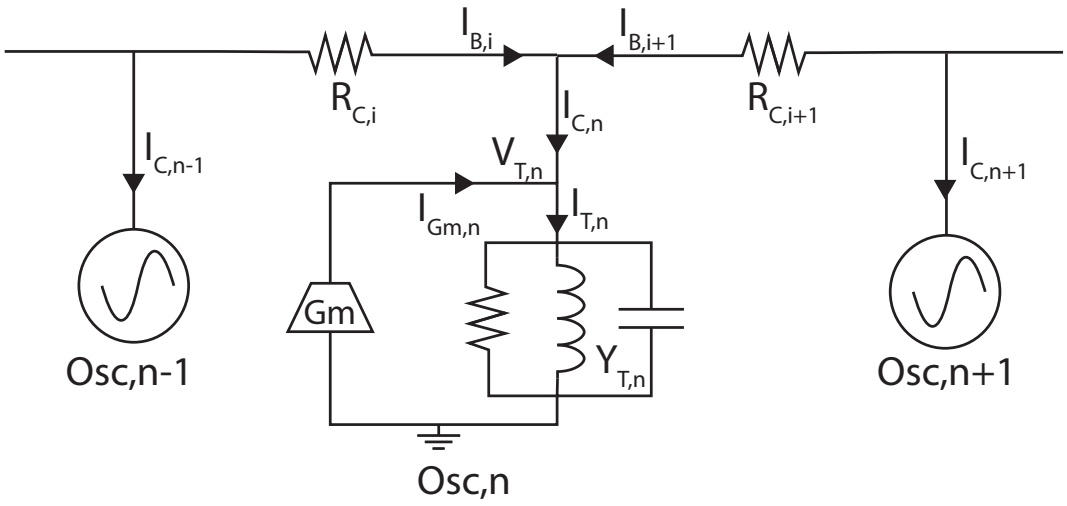

Figure 3.11: Schematic of a portion of a resistively-coupled N-core oscillator system.

$$f_{osc} = \frac{\sum_n f_{0,n}}{N} \tag{3.72}$$

easily follows. Therefore, even in the N-core case the oscillation frequency does not depend on the interconnection topology.

The coupling currents $I_{C,n}$ are distributed in the branches of the interconnection network. The current $I_{B,i}$ flows in the i-th branch if the two cores connected by the branch experience a phase shift θ_i with respect to each other. This can be calculated inverting eq. (3.13), yielding

$$\theta_i = \sin^{-1}\left[\frac{R_{C,i}|I_{B,i}|}{A}\right] \tag{3.73}$$

In case of small phase shifts, $\sin\theta_i \approx \theta_i$, and phase shifts are directly proportional to the voltage drop $R_{C,i}|I_{B,i}|$ across coupling resistances:

$$\theta_i \approx \frac{R_{C,i}|I_{B,i}|}{A} \tag{3.74}$$

Eq. (3.71) and (3.74) provide useful insights to compare different interconnection strategies in N-core oscillators, to minimize phase shifts and therefore maximize locking range and, more importantly, reduce the phase noise penalty.

In Fig. 3.12, three different interconnection networks for the quad-core oscillator

(i.e. nearest-neighbor chain coupling, nearest-neighbor ring coupling, and global coupling) are compared[2]. Each core is modeled as a current source, whose current $I_{C,n}$ is calculated through eq. (3.71). The currents $I_{B,n}$ flowing in the branches of the interconnection network are derived using simple circuit analysis. Finally, according to eq. (3.74), the phase shift between two adjacent cores is proportional to the

[2]For fair comparison, since in the network in Fig. 3.12c each core has three connections instead of two, coupling resistances have been risen by 50% with respect to Fig. 3.12a and 3.12b, assuming interconnection switch width is reduced so as to keep the same capacitive parasitics.

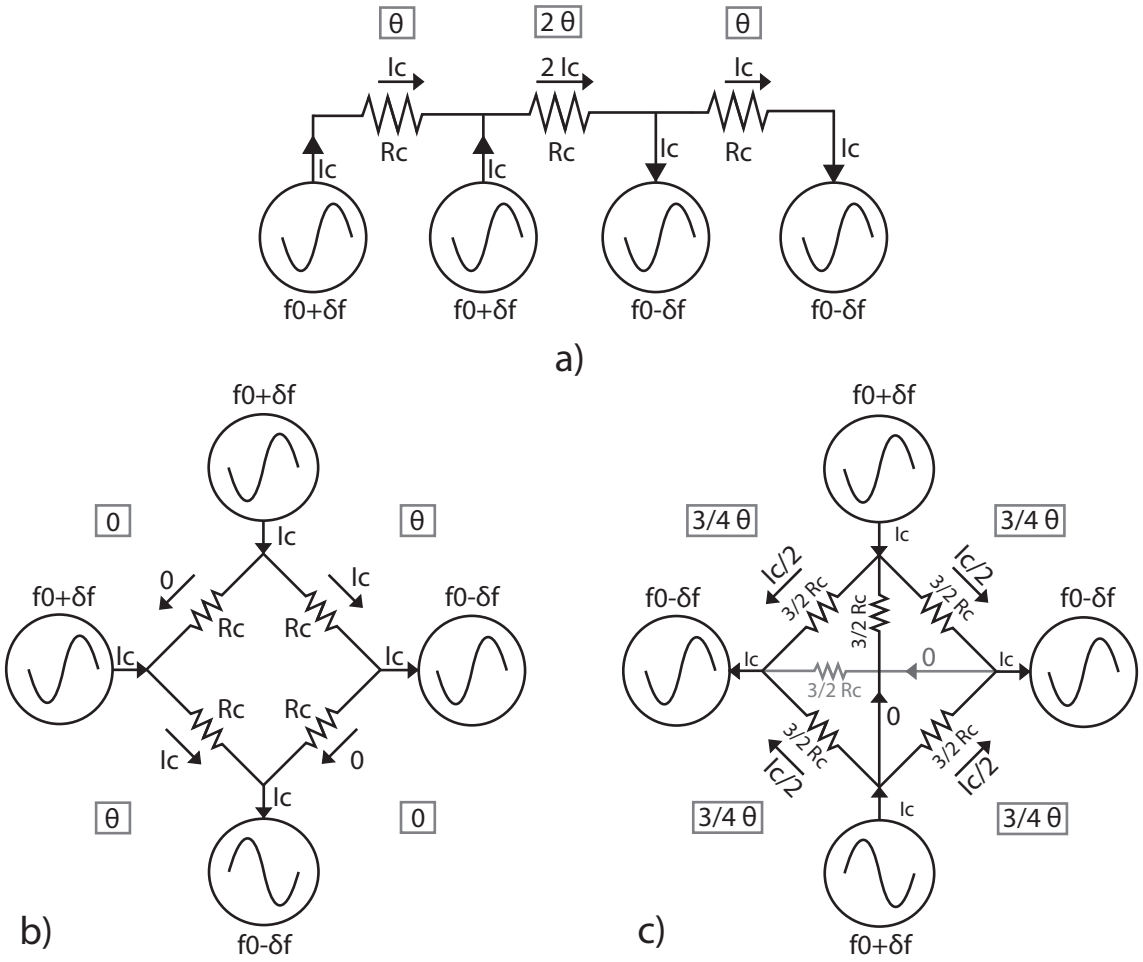

Figure 3.12: Comparison between three different single-ended quad-core oscillator systems: nearest-neighbor chain coupling (a), nearest-neighbor ring coupling (b) and global coupling (c). In each case, coupling currents are shown for the worst-case resonance frequency mismatch distribution, i.e. the one leading to the highest phase shifts.

voltage drop across the resistor connecting them.

Resonance frequency mismatch distributions leading to worst-case phase shifts are shown in Fig. 3.12. The chain topology leads to 2x phase shift in the central connection with respect to the ring, and it is therefore less robust. The global connection network leads to a slight improvement in phase shifts compared to the ring topology, at expense of increased complexity. The results have been verified by circuit simulations. Time-domain simulations of N-core oscillator arrays require long convergence time, especially close to the locking range. Conversely, the proposed model only requires a DC simulation, and it provides therefore a useful help in comparing interconnection strategies.

Finally, it is interesting to notice that the worst-case configuration for the nearest-neighbor quad-core ring topology, as shown in Fig. 3.13, actually corresponds to two identical mismatched dual-core systems. Since the two systems are identical, they experience 3dB noise reduction, with no penalties, when coupled together. Therefore, amplitude reduction, locking range and noise penalty can still be described by eq. (3.22, 3.25, 3.68). This result is not expected to hold for bigger arrays, as it was theoretically demonstrated in [93] that the locking probability of an array of N oscillators with random frequency mismatch tends to 0 when $N \to \infty$.

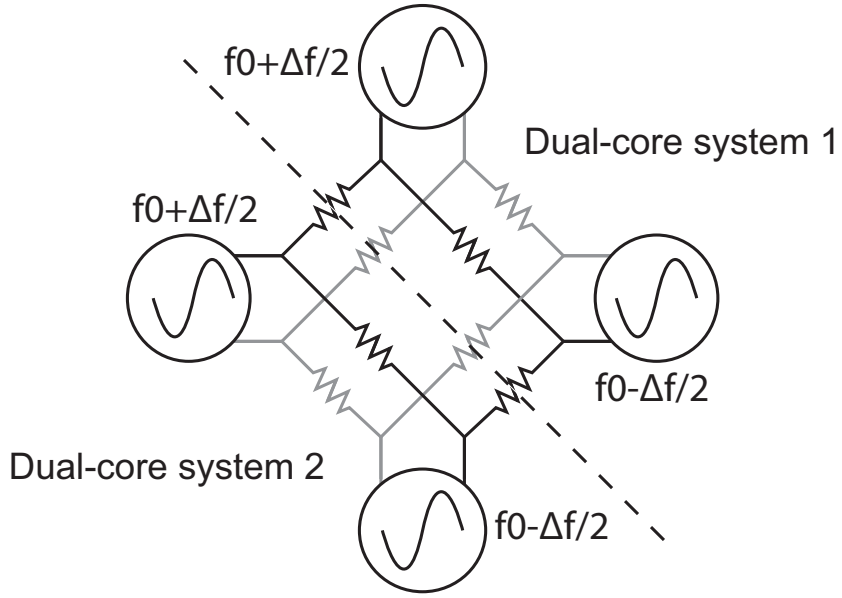

Figure 3.13: Worst-case frequency mismatch configuration in a quad-core oscillator with nearest-neighbor ring coupling.

3.4 20GHz Quad-Core Oscillator

A noise-scalable 20GHz quad-core VCO, shown in Fig. 3.14, was designed as a frequency reference for the E-Band synthesizer. The ring-like quad-core topology was employed as a compromise between reduced phase shifts and low complexity. Single, double and quad-core configurations are possible, leading to 3dB and 6dB noise improvement respectively. The layout is sketched in Fig. 3.15. The centrosymmetric arrangement of the four cores allows to minimize interconnection length, reduce footprint, and achieve maximum symmetry.

Connecting and disconnecting the cores through switches is not straightforward, since the voltage at the oscillator output usually swings above V_{DD}. As a result, a PMOS switch with the gate biased at V_{DD} would still be turned on for part of the

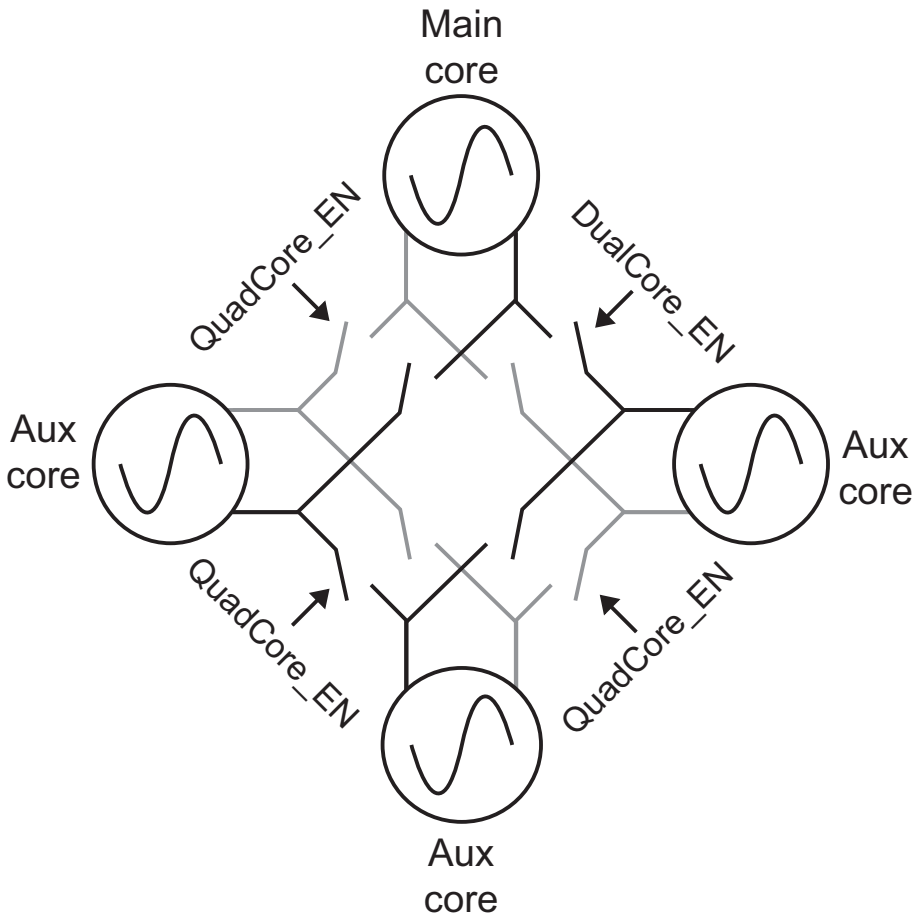

Figure 3.14: Schematic of the 20GHz quad-core VCO.

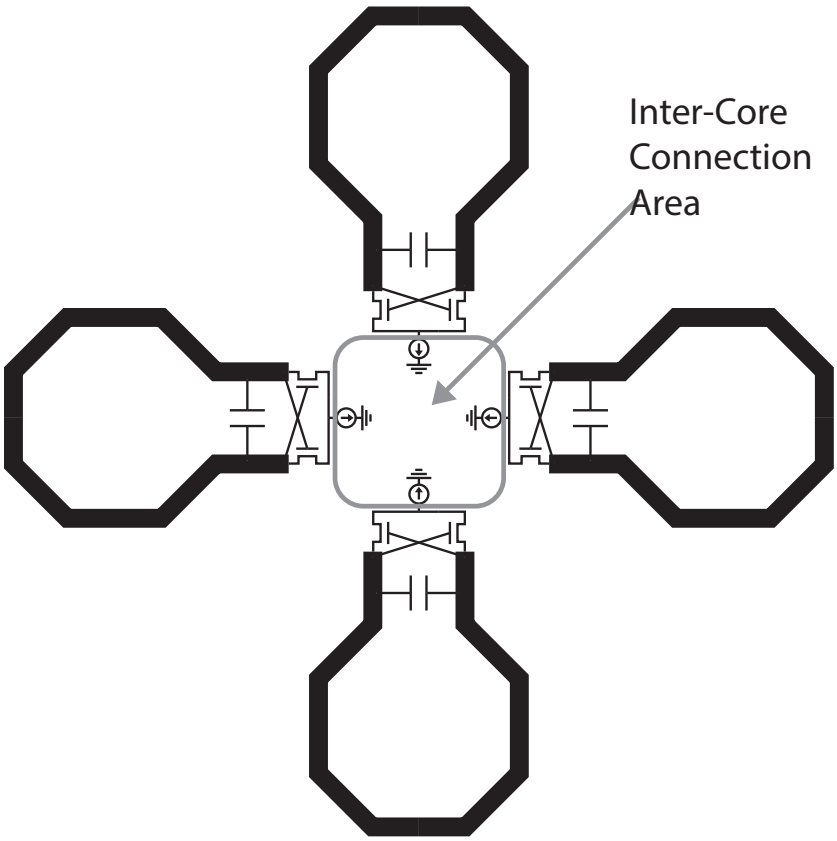

Figure 3.15: Centrosymmetric layout sketch of the quad-core oscillator. Interconnections between cores were omitted for simplicity, and are located inside the grey square.

oscillation period. A possible solution would be to AC-couple the PMOS switches and bias source and drain terminals to ground when the connections must be turned off. However, placing capacitors in the coupling paths can force the cores to oscillate in quadrature [94]. The stability of the quadrature mode depends on the value of coupling capacitances C_C and, according to simulations, guaranteeing in-phase oscillation would require to use $C_C \gg C_T$. This is impractical at mm-Waves as bottom-plate parasitics would degrade the tuning range. Therefore, in the proposed oscillator thick-oxide PMOS switches, whose bulk is biased at $2V_{DD}$, are employed in order to completely turn on and off inter-core connections when required.

The switch size was chosen as a compromise between robust noise reduction in presence of mismatches, and capacitive-parasitics minimization. A 5% worst-case tank components mismatch, leading to ∼2.5% relative frequency mismatch, was

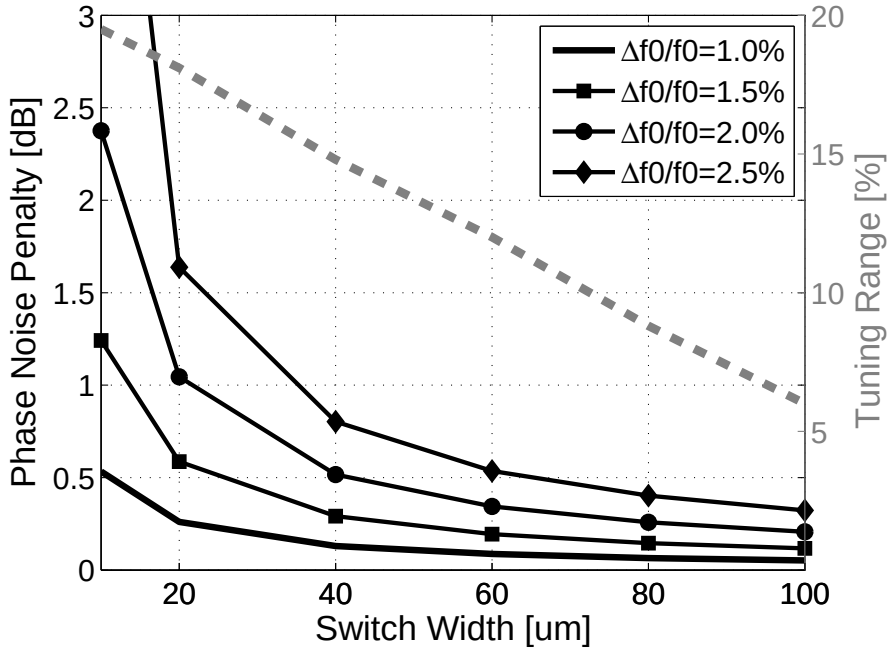

Figure 3.16: Simulated phase noise penalty (black solid curves) and tuning range (grey dashed curve) of the quad-core 20GHz oscillator when varying the coupling switch width.

considered. This captures both process-dependent mismatches and, more importantly, systematic differences due to layout asymmetries and unwanted couplings. Simulated phase noise penalty is plotted versus size of the coupling switches in Fig. 3.16, together with the tuning-range degradation due to switch capacitive parasitics. A 40μm wide switch can keep the worst-case noise penalty below ∼0.8dB. Wider switches show only a slight reduction of noise penalty, but they significantly impact on tuning range.

3.5 Conclusions

Switch-coupled multi-core oscillators were proposed to achieve both ultra-low phase noise performance and noise-scaling capability at constant FoM. By in-phase coupling N identical oscillators, phase noise is reduced by $10\log_{10} N$ and power consumption is increased by N.

Resonance-frequency mismatches between the cores result in a phase-noise penalty.

This penalty is a function of the ratio between the switch *on* resistance and the tank resistance. Correctly sizing the coupling switches can assure robust operation with negligible mismatch-related noise penalties. An analytical LTV model taking into account this effect was developed, providing understanding of the noise-penalty process and insights in how to compare interconnection strategies in N-core VCOs. Finally, a 20GHz quad-core oscillator, to be employed in the E-Band frequency synthesizer described in section 2.6, was presented. Leveraging the aforementioned multi-core concept, it achieves 3dB and 6dB noise and power scaling, to vary the synthesizer performance and consumption according to the modulation order.
Further design details on the individual VCO core are discussed in section 5.2, whereas experimental measurements are presented in section 6.1.1 and 6.2.

Chapter 4

E-Band Frequency Quadrupler

In this chapter, insights on the design of wideband, low-power frequency quadruplers for E-Band frequency synthesis are disclosed. When designing a frequency multiplier for the synthesizer architecture discussed in section 2.6, there are four main requirements. First, the circuit has to provide an output E-Band reference, possibly differential, to enable direct-conversion transceivers. Second, it has to achieve wide tuning range - at least 20% - to generate frequency reference in both 71-76GHz and 81-86GHz bands. Third, it has to provide negligible phase-noise degradation. Finally, low power consumption while keeping a reasonable output swing is desirable. Indeed, the multiplier power is a fixed overhead which, unlike the VCO consumption as discussed in chapter 3, does not scale with phase noise performance. To keep the VCO power-scaling feature effective on the whole synthesizer consumption, the multiplier power budget has to be lower than the VCO one.
In the following, frequency multiplication techniques commonly employed in mm-Wave ICs are first reviewed. Next, a frequency quadrupler leveraging transformer-coupled resonators for wideband operation with high power efficiency is described. Finally, performance limitations due to common-mode coupling in the transformers are discussed, and isolation techniques are proposed.

4.1 Frequency Multiplication Techniques

Frequency multiplier circuits at mm-Waves mainly belong to three groups. The first is based on mixer principle, the second on injection locking and the third on device nonlinearities. Mixer-based multipliers leverage the RF and LO ports of a

Gilbert cell to generate an output component at twice the input frequency [95]. Despite featuring very wide bandwidth, state-of-the-art realizations show >30mW power consumption, not acceptable within an E-Band transceiver link budget [95, 96]. Further, in order to suppress the fundamental component at the output, fully balanced topologies are employed, with the drawback of large capacitance at the input port, thus penalizing VCO tuning range [95].

The injection-locked frequency multiplier, beneficial for its low power, is one of the most popular topologies, usually for even-order frequency multiplication [71, 97, 98]. However, it usually suffers from small frequency locking range. As an example, state-of-the-art prototypes reported in [98] and [99] show a fractional bandwidth of 14.8% and 13.1%, respectively, too low if $> 20\%$ is needed for the application.

Another widely adopted solution is the selection of harmonic components generated by a nonlinear active device [100, 101]. The most popular configuration is shown in Fig. 4.1. Commonly known as push-push pair, it consists of two transistors operating in nonlinear conditions, i.e. class-B or class-C. The transistor current, rich of harmonic components, is filtered by a resonant load which selects the desired one. By using two transistors driven differentially, the fundamental and even-harmonic currents are canceled at the common drain node, improving harmonic rejection. Push-push doublers are commonly employed by virtue of their design simplicity, good power efficiency, and negligible phase-noise degradation. However, two issues

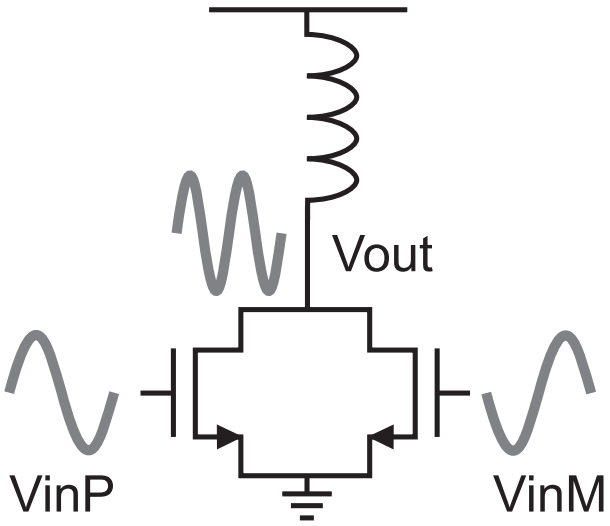

Figure 4.1: Operating principle of a push-push frequency doubler.

limit the usage of this topology. The first is the gain-bandwidth trade-off at the output LC resonator. For wideband operation, a low-quality-factor tank should be employed, but this reduces the tank impedance magnitude, thus degrading the multiplier voltage gain. Second, the absence of a differential output, needed to properly drive the following mixer and desirable to avoid the need of accurate modeling of dangerous current return paths typical of single-ended implementations.
Recently, a modified version of the classic push-push pair providing differential output, by transformer-coupling the signals at the transistor source and drain, was proposed. However, it only operates below 20 GHz [102]. To perform direct frequency multiplication by four, stacked push-push pairs have been proposed [103, 104], but they need an additional phase shifter at the input, and still provide a single-ended output.

4.2 Push-Push Transformer-Coupled Frequency Quadrupler

The proposed multiplier, depicted in Fig. 4.2, leverages the cascade of two push-push doublers to implement the x4 operation. In order to enhance the gain-bandwidth product (GBW), high-order networks can be employed as loads [105, 106]. However, in integrated technologies, the number of reactive components must be minimized to limit power losses. Furthermore, the topology of the network and the component values should enable a compact layout to minimize parasitics, particularly critical at mm-Wave frequencies.
In the proposed multiplier chain, both interstage and output matching networks are

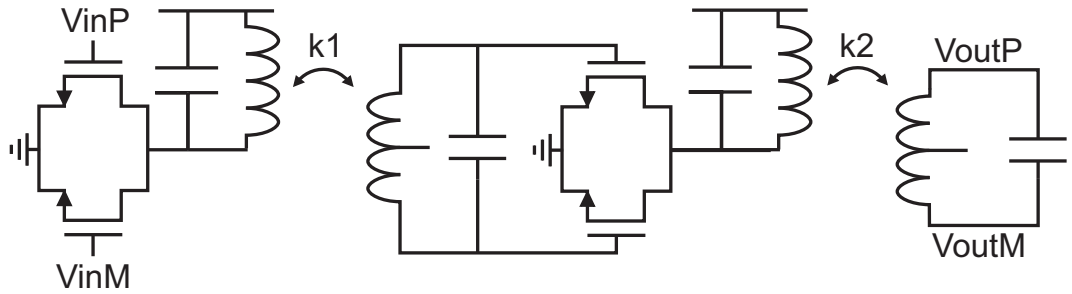

Figure 4.2: Proposed frequency quadrupler.

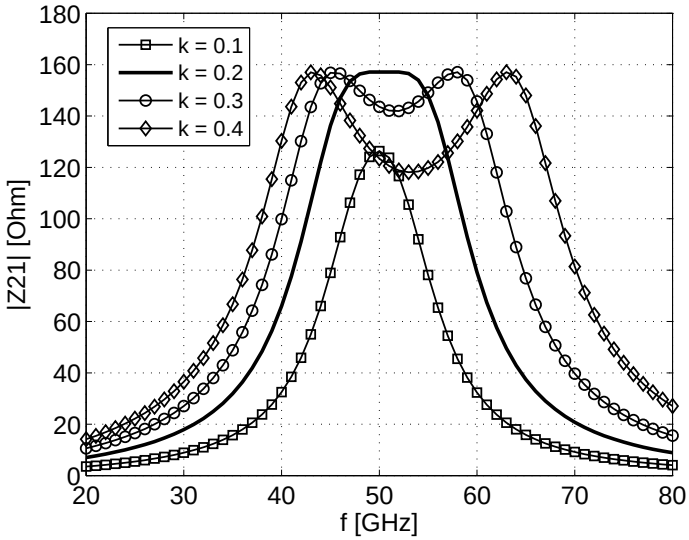

Figure 4.3: Simulated $|Z21|$ of a transformer-coupled-resonator system varying the transformer's coupling coefficient.

based on fourth-order magnetically coupled resonators, realized with low-k transformers. Compared to a second-order shunt LC load, they can provide up to 2x improvement in the gain-bandwidth product at given quality factor [107, 108]. The primary coil of the transformer resonates the push-push total drain capacitance, while the secondary coil resonates the differential input capacitance of the following stage.

The transformer's coupling coefficient k determines the transfer function of the coupled resonators, as shown in Fig. 4.3. Assuming $Q_P \approx Q_S = Q$, which are the quality factors of primary and secondary resonators respectively, the transimpedance Z_{21} of the so-defined network exhibits a flat response for the critical coupling condition $k = 1/Q$. If a higher k is chosen, $|Z_{21}|$ tends to broaden at the expense of some ripple.

Also, because of the fourth-order response, the out-of-band slope of $|Z_{21}|$ is steeper than a simple LC-shunt resonator. As a result, the frequency doubler transfer function resembles more a box-like function, and the bandwidth reduction resulting from cascading two multipliers is lower than if second-order loads were used [109].

The transformer also provides two other interesting features. First, it can be used to convert the common-mode second harmonic current of the push-push into a dif-

ferential output voltage, thus allowing the first doubler to drive the second, and the second stage to provide a differential output to the subsequent balanced mixer. Then, it allows to easily bias the gate of the following stage through the secondary coil's center tap, thus avoiding AC coupling capacitors which would lead to additional parasitics and losses at mm-Waves.

4.3 Common-Mode Isolation

At mm-Waves, capacitive coupling between balun coils can introduce non-negligible amplitude and phase mismatch in the differential outputs. As shown in Fig. 4.4, if the primary coil is driven single-ended, the voltage signal along the inductor goes from maximum swing at the push-push end to zero at the supply end. If an ideal transformer is considered (i.e. without capacitive coupling), magnetic coupling induces a voltage swing on the secondary coil which is perfectly antisymmetric with respect to the center tap. If capacitive coupling is introduced where the two coils cross each other, the voltage difference ΔV between the coils is different in the two crossing points. As a result, the two coupling currents do not cancel each other, resulting in a net common-mode current which is transferred from the primary coil to the secondary, as shown in Fig. 4.5.

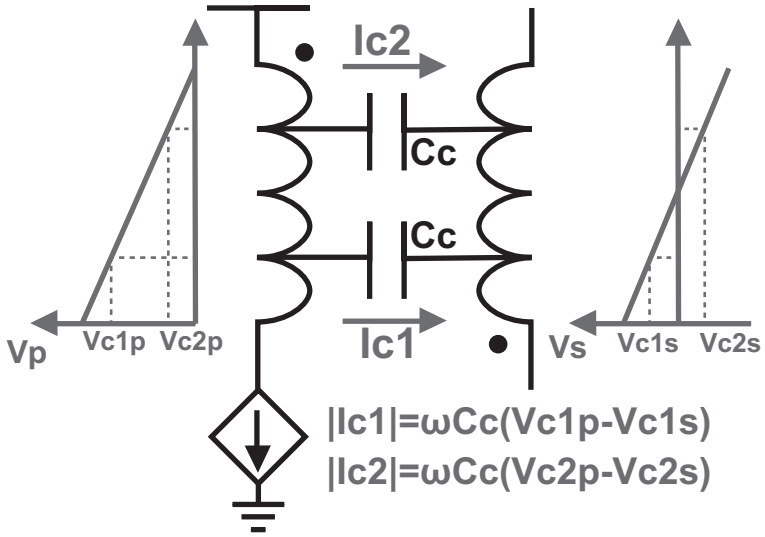

Figure 4.4: Voltage swing across the two coils of the balun, and inter-coil currents due to capacitive coupling.

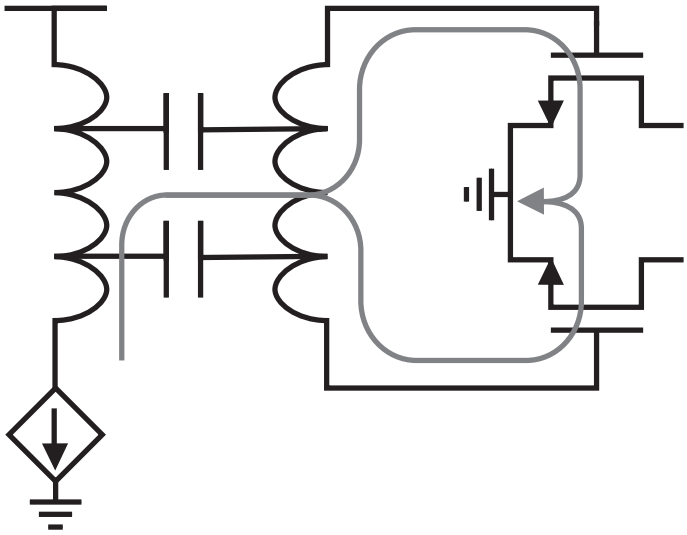

Figure 4.5: Inter-coil capacitively-coupled current path in a conventional balun.

From a circuit-level point of view, the coupling of a common-mode current to the output of the transformers generates two negative effects in the frequency quadrupler operation. First, to maximize the doubler gain one would like to convert 100% of the 2nd-harmonic current generated by the push-push couple into a differential output voltage. If, instead, part of the push-push current is wasted on a common-mode component, the voltage gain of each multiplying stage drops, thus lowering efficiency. Another undesired effect is a reduction of the quadrupler 2nd-harmonic rejection. To understand this effect, let us imagine that part of the 2nd-harmonic current generated by the first push-push doubler is converted into a common-mode output voltage. This voltage is fed to the second push-push doubler, which by construction rejects differential signals, but amplifies common-mode components. Therefore, the 2nd-harmonic common-mode component will not be frequency-doubled, and it will make its way to the output.

In order to avoid unwanted common-mode capacitive coupling, the grounds of the two coils are isolated by breaking the ground plane and connecting them to different pads, thus preventing inter-coil current due to the bondwire high impedance at mm-Waves. Further, a dummy coil is located under the primary winding, as shown in Fig. 4.6, in order to provide a low-impedance return path for the capacitive-coupling current. As a result, the net current flowing in the secondary winding is recollected in the dummy coil, without making its way to the transformers outputs, as depicted

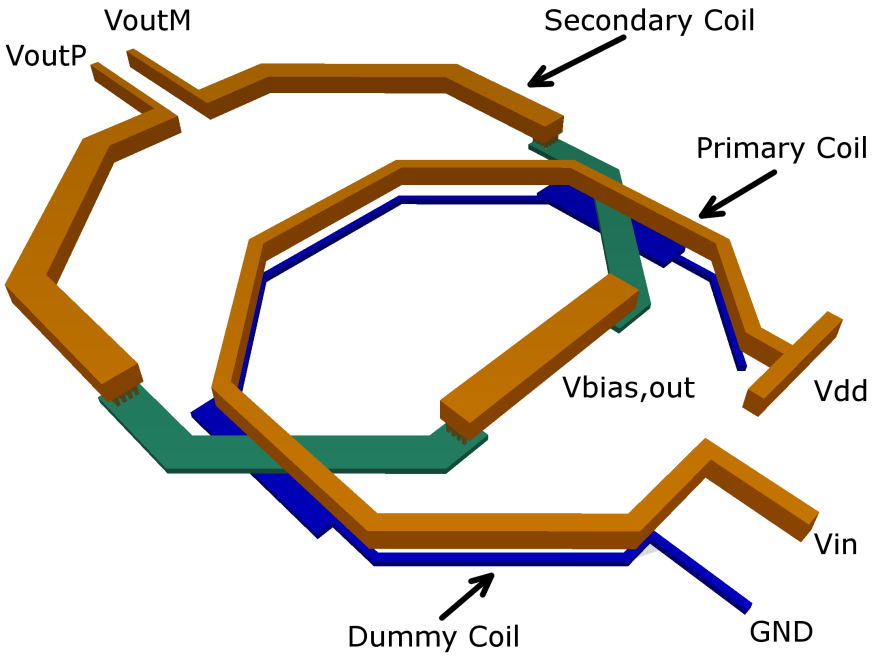

Figure 4.6: Layout of the transformer.

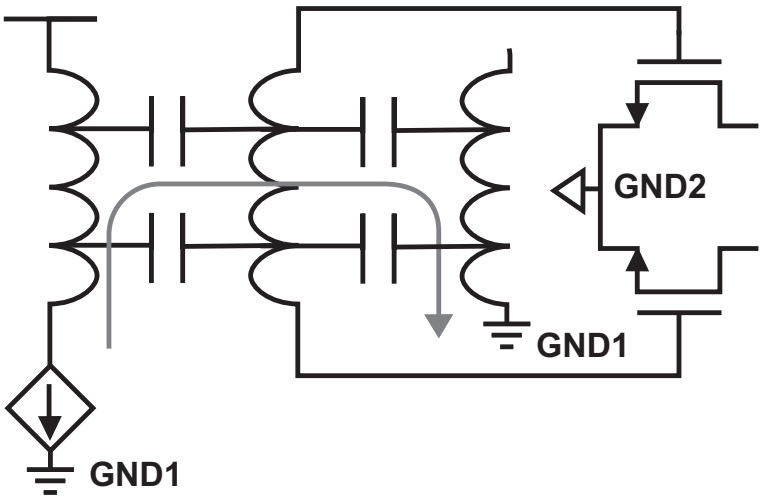

Figure 4.7: Inter-coil capacitively-coupled current path in the common-mode-isolated balun.

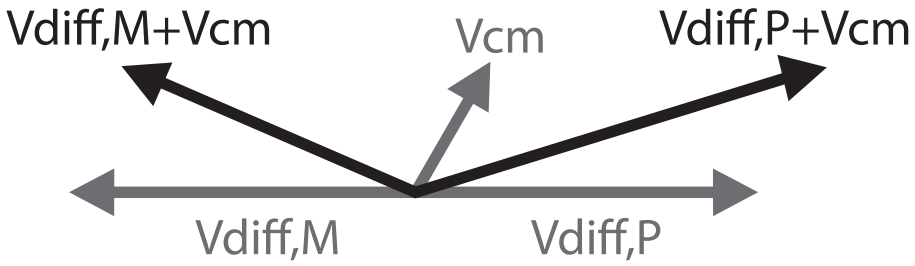

Figure 4.8: Effect of adding a common-mode component to a purely differential signal. The two resulting single-ended outputs, $V_{DIFF,P} + V_{CM}$ and $V_{DIFF,M} + V_{CM}$, are no more 180°-phase-shifted, and experience an amplitude imbalance.

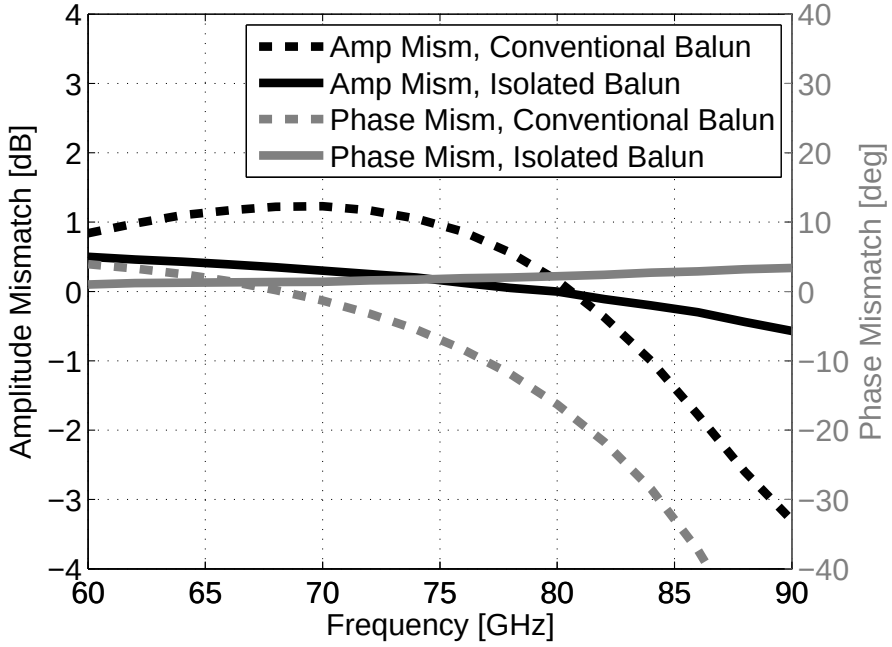

Figure 4.9: Simulated amplitude (black) and phase (grey) mismatch between positive and negative balun outputs of the second frequency doubler. Comparison between a conventional balun (dashed) and the proposed balun (solid).

in Fig. 4.7.
The effectiveness of the isolation techniques can be assessed by looking at the amplitude and phase imbalance between the two single-ended outputs. As graphically shown in Fig. 4.8, adding a random common-mode component to a purely differential waveform generates amplitude and phase asymmetries between the positive and negative outputs. This is a useful evaluation technique allowing to detect non-negligible common-mode components by only looking at the single-ended outputs. This leads to simulation results that can easily be compared with measurements, since high-frequency measurements are usually performed on the single-ended outputs.
As shown in Fig. 4.9, simulations confirm that the adopted isolation techniques significantly improve output imbalance. The ground-isolated balun leads to an amplitude mismatch below 0.5 dB over the whole bandwidth, and a phase mismatch below 5°. On the other hand, the conventional balun shows non-negligible output mismatch at high frequencies, especially concerning the phase. According to simulations, the entire frequency quadrupler with isolated baluns achieves 3-4dB gain improvement and 10-20dB higher 2nd-harmonic rejection, over the frequency range, compared to using a conventional balun.

4.4 Conclusions

In this chapter, design techniques to realize a wideband frequency quadrupler, suitable for the E-Band synthesizer in Fig. 2.11, were discussed. In the proposed circuit, cascaded push-push doublers were employed, leveraging their simplicity and power efficiency. Interstage networks based on low-k transformer-coupled resonators were exploited to increase the GBW and achieve broadband operation.
Common-mode capacitive coupling in the transformers limit the circuit performance at mm-Waves, introducing gain and harmonic-rejection penalties. A combination of ground isolation and introduction of a dummy coil in the transformer is proposed to tackle this problem.
More practical design details are disclosed in section 5.3, whereas measurements are presented in section 6.1.2.

Chapter 5

Circuit Design in 55nm BiCMOS

This chapter deals with the design of the frequency-synthesis building blocks in BiCMOS 55nm technology. After a brief overview of the technology features, design choices for the VCO, the frequency quadrupler and the output buffer chain are discussed. Finally, an overview of the realized test chips is provided.

5.1 Technology Overview

All the test chips were designed and fabricated in a 55nm BiCMOS technology provided by STMicroelectronics [110]. The technology cross section is shown in Fig. 5.1.

The Front End of the Line (FEOL) features both carrier-class 55nm CMOS FETs and epitaxially-grown high-speed SiGe *npn* heterojunction bipolar transistors (HBT). CMOS transistors come in three flavours: general purpose (GP), with 1V supply, low power (LP), with 1.2V V_{DD}, and thick-oxide (GO2), featuring 280nm minimum channel length and supply up to 2.5 V. High-speed SiGe bipolars achieve 320GHz GBW, with 1.5V collector-emitter open-base breakdown voltage (BV_{CEO}). Medium-voltage and high-voltage HBTs featuring higher BV_{CEO}, at expense of lower-speed operation, are also available.

The Back End of the Line (BEOL) features 8 copper metal layers: 5 thin layers M1-M5, 2 thick layers M6 and M7, and an ultra-thick metal (UTM) layer M8. The 3µm thick UTM represents the main difference with respect to the 65nm CMOS BEOL stackup. An aluminium capping layer is also available on top.

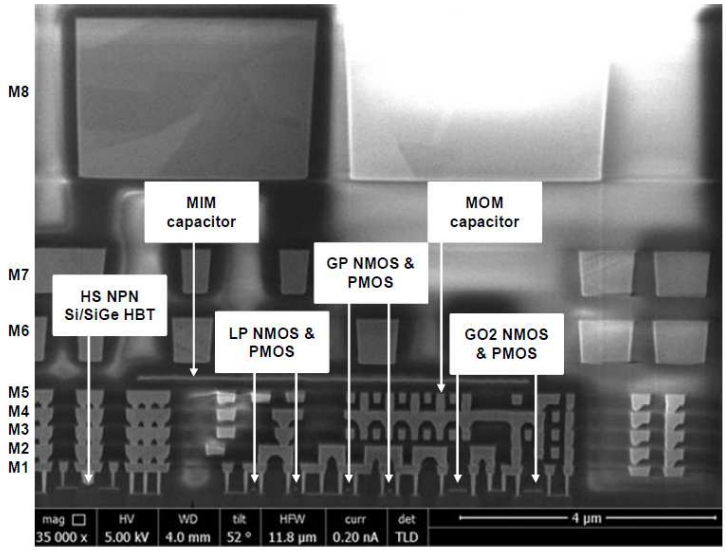

Figure 5.1: BiCMOS 55nm technology cross-section [110].

5.2 VCO Core Design

The individual oscillator core was designed to minimize phase noise. Among the many topologies presented, class-C oscillators [41] and class-B oscillators with tail filter [92] were found to be the most performant in terms of phase noise and power efficiency [55]. Class-F oscillators [53] are attractive as well, but they require a transformer-based tank, which would introduce unwanted capacitive parasitics at 20 GHz. Class-C VCOs provide very good FoM, but their oscillation swing has to be limited in order not to push transistors in triode region, thus setting a limit to the achievable absolute phase noise performance [41]. Conversely, the class-B VCO with tail filter allows maximum swing and phase noise levels close to the theoretical limit [111]. Moreover, it provides current-source noise filtering and reduced flicker-noise upconversion. Since the absolute noise performance, rather than the FoM, is the key requirement in E-Band synthesizers, the tail-filter topology was adopted, as shown in Fig. 5.2. To our knowledge, this is the first mm-Wave VCO employing this topology reported in literature.

Introducing mm-Wave tail filters in the quad-core oscillator presents some implementation issues. Indeed, in the centrosymmetric layout shown in Fig. 3.15, tail filter inductors would have to be squeezed in the middle of the array. This area is

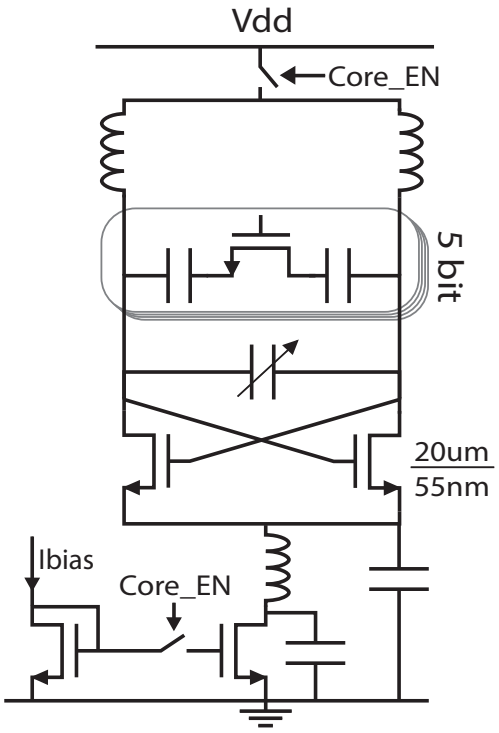

Figure 5.2: Individual VCO core, based on a class-B topology with tail filter.

too small to fit them and also already occupied by inter-core connections. Increasing the distance between the cores to create space for the tail filters would result in higher interconnection impedance and bigger footprint.

A first solution, which was adopted in the first two testchips, is to flip the tail inductor on top of the capacitor bank, as shown in Fig. 5.3. A ∼100pH inductor resonates with the cross-coupled pair source capacitance and a ∼80fF tunable capacitor bank. This implementation presents two main drawbacks. First of all, nodes A and B in Fig. 5.3 have to be short-circuited by a metal bar. Otherwise, the fundamental-harmonic current which is coupled from the tank inductance would create some non-negligible differential voltage swing at these nodes. This modulates the noise of the tail current source and raises the overall VCO phase noise. On the other hand, if nodes A and B are shorted, fundamental-harmonic magnetic coupling between tank and tail inductor results in a penalty in the tank's quality factor (∼10% in the considered case). The second issue, which becomes problematic at high frequencies, deals with the tail resonator's Q. It is shown in [112] that a tail resonator quality factor Q_{TAIL} higher than the tank's Q is desirable for optimal noise performance. This is hard to achieve

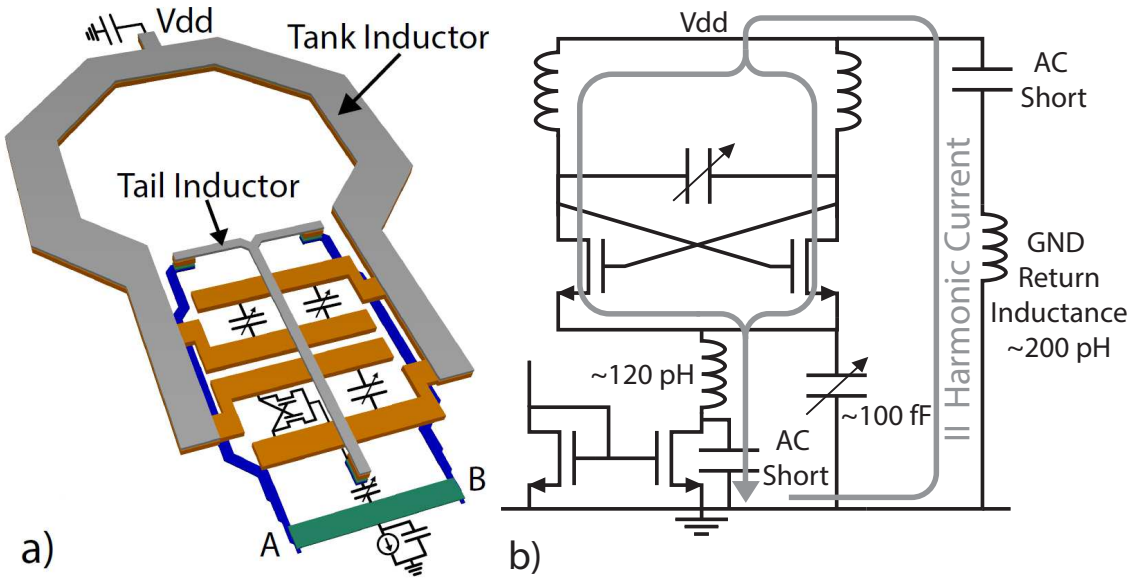

Figure 5.3: Layout of the resonant tail filter as implemented in the first test chips (a) and related oscillator schematic (b).

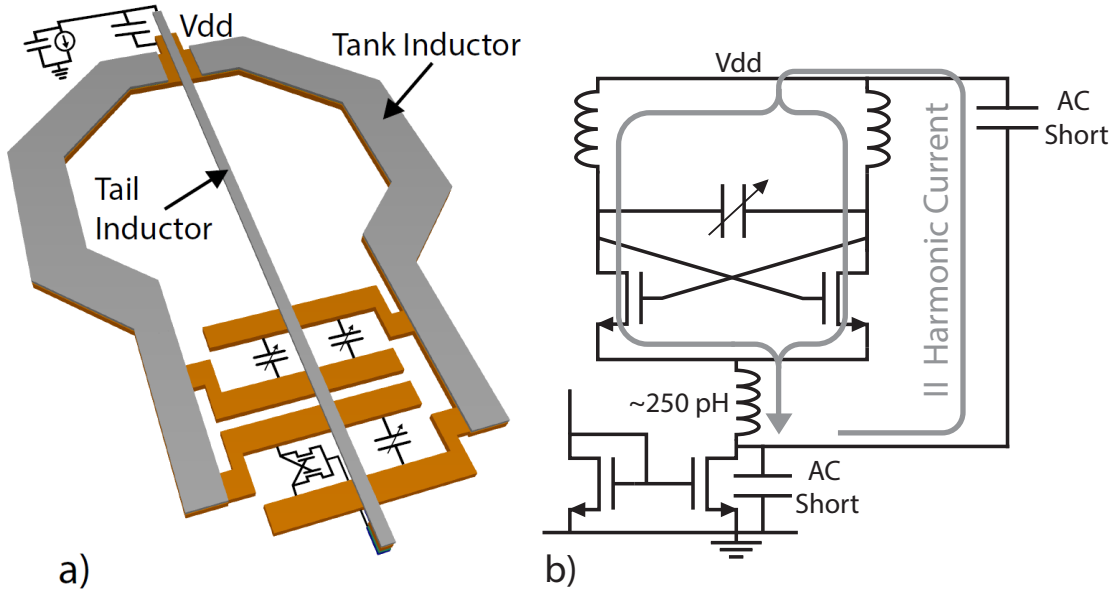

Figure 5.4: Layout of the inductive tail filter implemented in the last test chip (a) and related oscillator schematic (b).

in a 20GHz oscillator, as the tail filter works at the II harmonic, where capacitive losses significantly degrade the Q of LC tanks. If $Q_{TAIL} < Q_T$, $C_{TAIL} \ll C_T$ should be employed [112], but this would require a large tail inductance value which is hard to obtain in the layout in Fig. 5.3.

A better solution, which was implemented in the last test chip, is shown in Fig. 5.4. Instead of using an LC-shunt resonator, a ∼250pH inductance is introduced between the VCO tail node and the current source. At 40 GHz, its impedance is high enough to significantly filter the II-harmonic current. Also, its quality factor is higher than the one of a LC resonator due to low magnetic losses at mm-Waves. Simulations show a ∼2dB phase noise improvement with respect to the solution in Fig. 5.3. Finally, since the tail impedance is not based on a resonant filter, it performs wideband noise reduction. The tail inductor also acts as an escape path from the center of the quad-core structure, where the cross-coupled pair is, to the outer region. The current source is hence located close to the tank inductor's center tap, minimizing the ground return inductance which can lead to unwanted resonances in the tail filter. The tail inductance lies in the middle of the tank inductor, thus contributing to negligible Q degradation, as verified through EM simulations.

Frequency control is performed through a 5bit switched-capacitor bank and a small varactor for fine tuning. This solution reduces the amount of nonlinear capacity in the tank, which would result in phase-noise penalties and flicker-noise upconversion due to AM-PM conversion [42]. The tank inductance is ∼300pH. Inductive and capacitive quality factors are ∼30 and ∼60 respectively, resulting in an overall tank's quality factor $Q \approx 20$.

CMOS transistors were used for both crossed-coupled pairs and tail current sources. LP devices were chosen by virtue of the higher V_{DD}, to maximize the oscillation swing and minimize phase noise. A switch on the center tap and a pass-gate on the current mirror are employed to turn on and off the oscillator core.

5.3 Frequency Quadrupler Design

An E-Band frequency quadrupler, shown in Fig. 5.5, was designed using a cascade of two tranformer-coupled push-push doublers, as described in chapter 4. nMOS transistors were used for the first push-push pair, so that the multiplier can be directly connected to the VCO. Indeed, loading the VCO with bipolar devices would

require to limit the oscillation amplitude in order to avoid strong direct biasing on base-collector and base-emitter junctions, otherwise reducing the tank's Q. On the other hand, the second push-push pair is implemented using high-speed *npn* HBTs, featuring a lower output capacitance at given gain. Small switched-capacitor banks were included on both sides of the coupled resonators in order to compensate possible process mismatches between bipolar and MOS transistors. 1.2V supply was employed for both stages.

The transformer layout is shown in Fig. 4.6. Since the output/input capacitance ratio of the designed push-push couples is ∼1.5, the transformer ratio is ∼1.5. To guarantee more than 25% -3dB fractional bandwidth for the whole quadrupler, with <3dB ripple, $k_1 = 0.35$ and $k_2 = 0.25$ were chosen as coupling coefficients for the transformers. The low coupling coefficient is obtained by introducing an offset between the coil centers in the transformers. The specific values used in the design were obtained through accurate EM simulations. Both transformers were implemented with single-turn inductors, using M8 UTM layer for most of the coils, and M7 thick metal layer for the crossing sections. Simulated inductance and quality factor values are reported in Table 5.1.

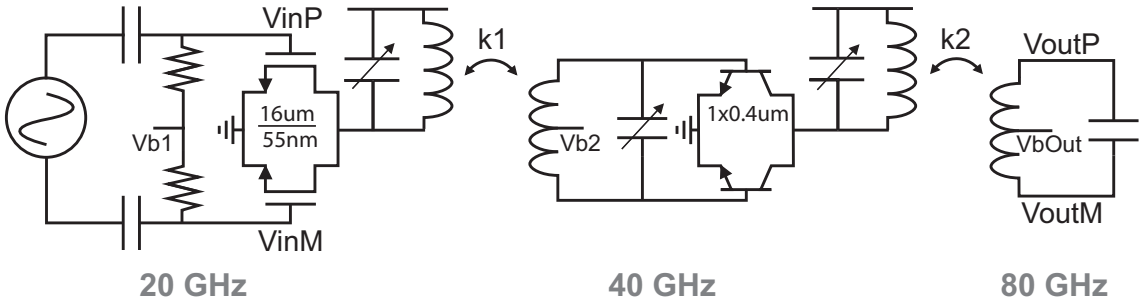

Figure 5.5: Schematic of the E-Band BiCMOS frequency quadrupler.

	Inductance	Quality factor
40GHz XFMR, primary coil	270 pH	23 at 40 GHz
40GHz XFMR, secondary coil	370 pH	22 at 40 GHz
80GHz XFMR, primary coil	105 pH	20 at 80 GHz
80GHz XFMR, secondary coil	150 pH	19 at 80 GHz

Table 5.1: Simulated inductance and quality factors of the transformer coils.

5.4 Output Chain Design

In order to measure the phase-noise performance of the E-Band frequency reference, the output signal is downconverted to ∼15 GHz, where the noise floor of the available spectrum analyzer is low enough to guarantee reliable measurements. To perform downconversion, the multiplier is followed by a double-balanced active mixer. The schematic is shown in Fig. 5.6. A 47-70GHz tone from an external signal generator is converted into differential by an on-chip balun and fed to the mixer LO port. When the MixerEN control is set to 1, switches SW1 and SW2 provide the bias voltage to the mixer transistors. When MixerEN control signal is set to 0, LO,p node is

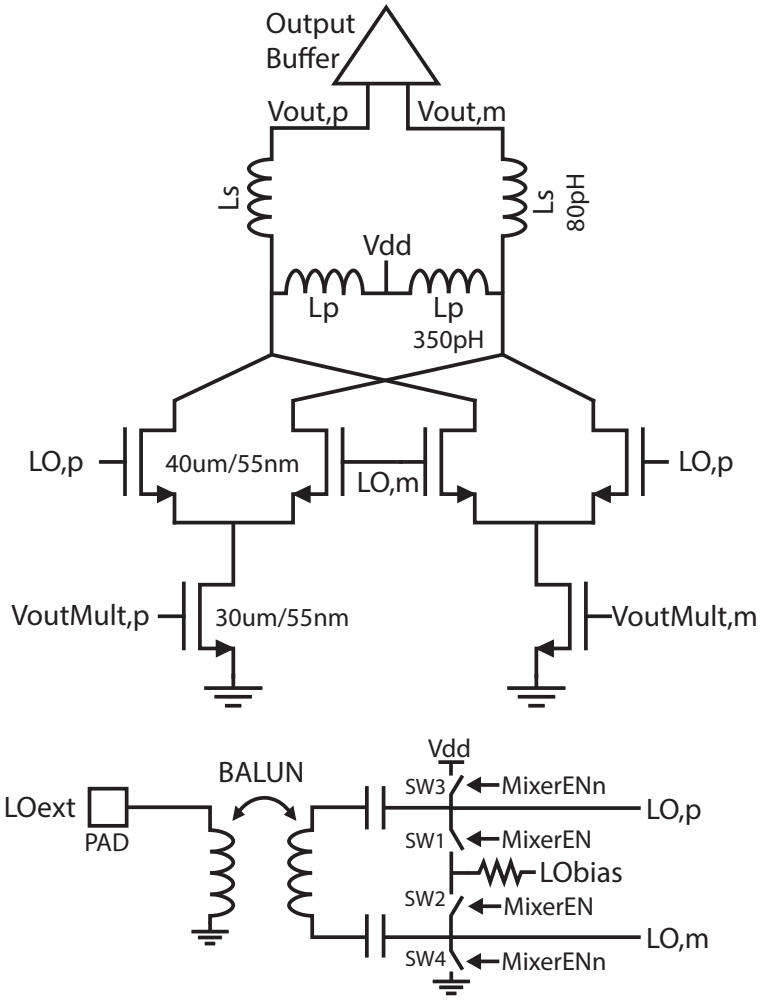

Figure 5.6: Schematic of the downconversion mixer/buffer, and the input network of the external LO.

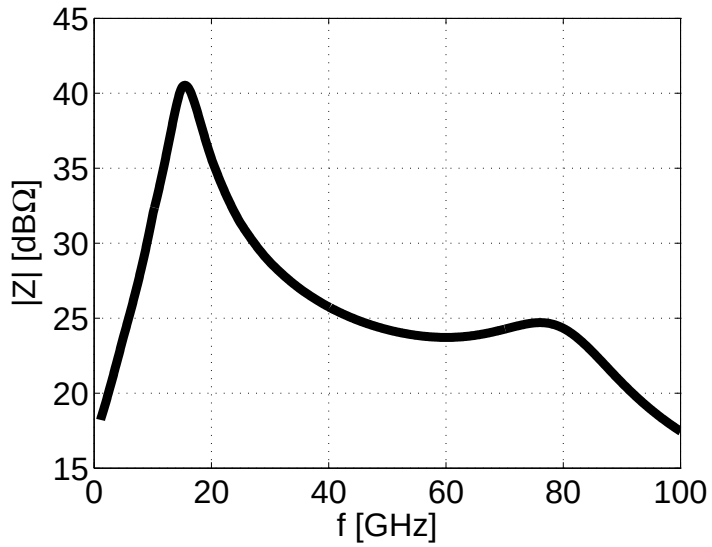

Figure 5.7: Simulated transimpedance magnitude of the mixer output matching network.

shorted to V_{DD} and the LO,m node to ground through switches M3 and M4. The crossing branches of the mixer are therefore turned off, and the circuits behaves as a pseudo-differential cascode transconductor. In this configuration, the external LO signal is turned off, and the mixer core acts as a buffer and amplifies the E-Band output, to perform high-frequency measurements without downconversion.

The mixer output matching network was designed to provide significant voltage gain in both configurations. Inductor Lp resonates the mixer output capacitance, providing a high-impedance peak around 15GHz. Inductor Ls, instead, provides series peaking to rise the impedance around 80 GHz. The overall simulated impedance of the network is plotted in Fig. 5.7.

The mixer is followed by a dual-stage output buffer, shown in Fig. 5.8, whose purpose is providing additional gain to compensate cable and probes losses. Both stages employ series peaking for wideband operation. The final stage is an open-drain buffer driving the 50Ω load of the spectrum analyzer. Transconductors were implemented as pseudo-differential couples, in order not to reject the common-mode component of the multiplier output and verify the proposed coil isolation technique. The buffer voltage gain is plotted in Fig. 5.9. The overall voltage gain of the output chain (i.e. mixer + buffer), from the differential multiplier output to the differential chip

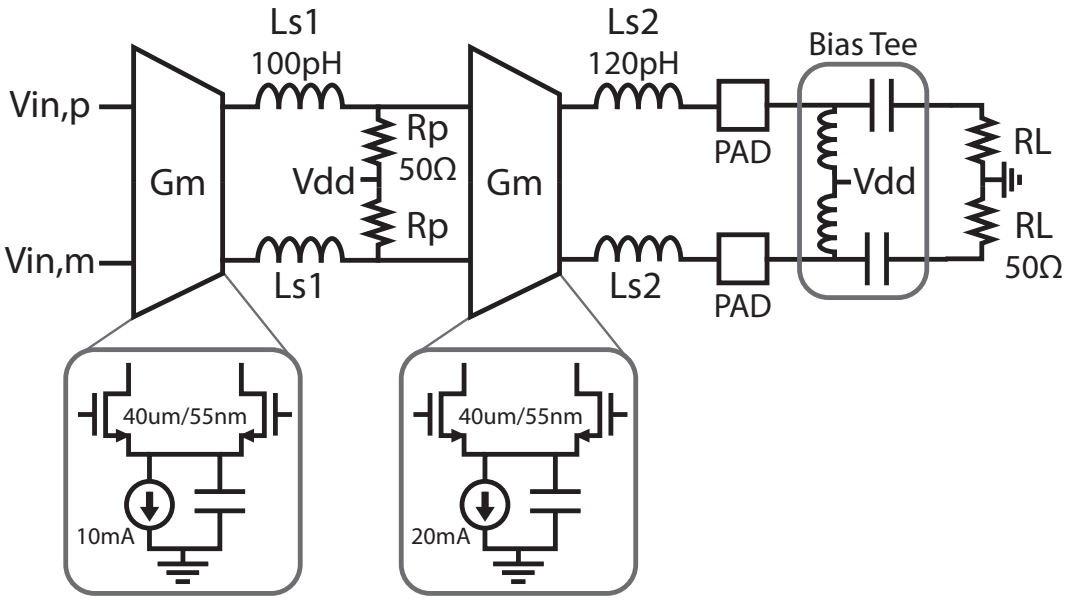

Figure 5.8: Schematic of the output buffer.

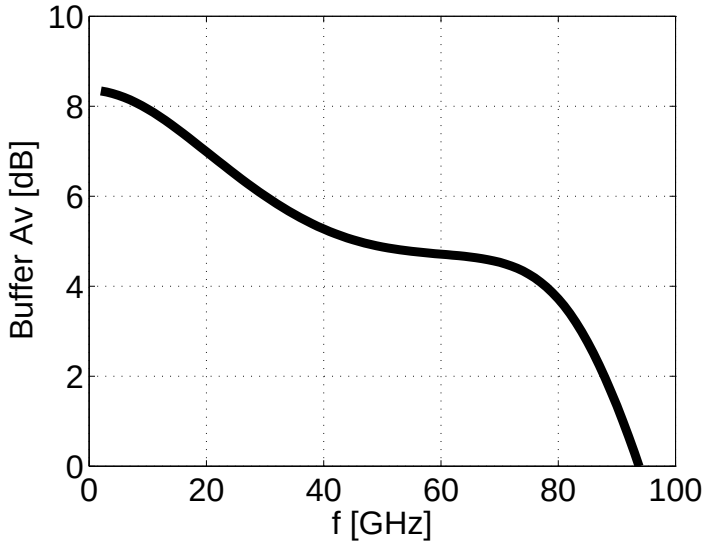

Figure 5.9: Simulated voltage gain of the output buffer.

output pad, is around 8 dB at 15 GHz in downconversion mode and 5 dB at 80 GHz in buffer mode.

5.5 Test Chip Overview

Three test chips have been realized.
The first which has been taped out, named EBANDVCO, includes the 20GHz quad-core VCO only. The VCO differential output is buffered by an open-drain pseudo-differential stage and fed to a GSGSG padframe for on-chip probing. Supply, analog tuning and digital frequency control are provided through bonding wires. The chip micrograph is shown in Fig. 5.10. The chip size is 0.9x0.9 mm^2, while the core area is approximately 0.7x0.7 mm^2.
The second chip, SAMARIS[1], features the cascade of the 20GHz VCO, the frequency quadrupler, and the high-frequency output chain described in section 5.4. An independent test structure for the multiplier, driven by an external input, is also included. The chip micrograph is shown in Fig. 5.11. The chip size is 1.8x1 mm^2, and the core circuits (i.e. VCO + multiplier) occupy approximately 0.85x0.7 mm^2. The stand-alone multiplier core area is around 250x400 μm^2.

[1] A tribute to the Franco-Belgian graphic novel "The walls of Samaris" by F. Schuiten and B. Peeters (Casterman, 1983).

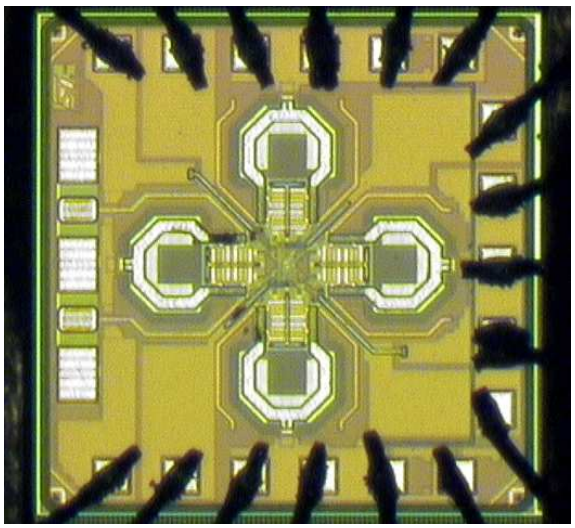

Figure 5.10: EBANDVCO chip micrograph.

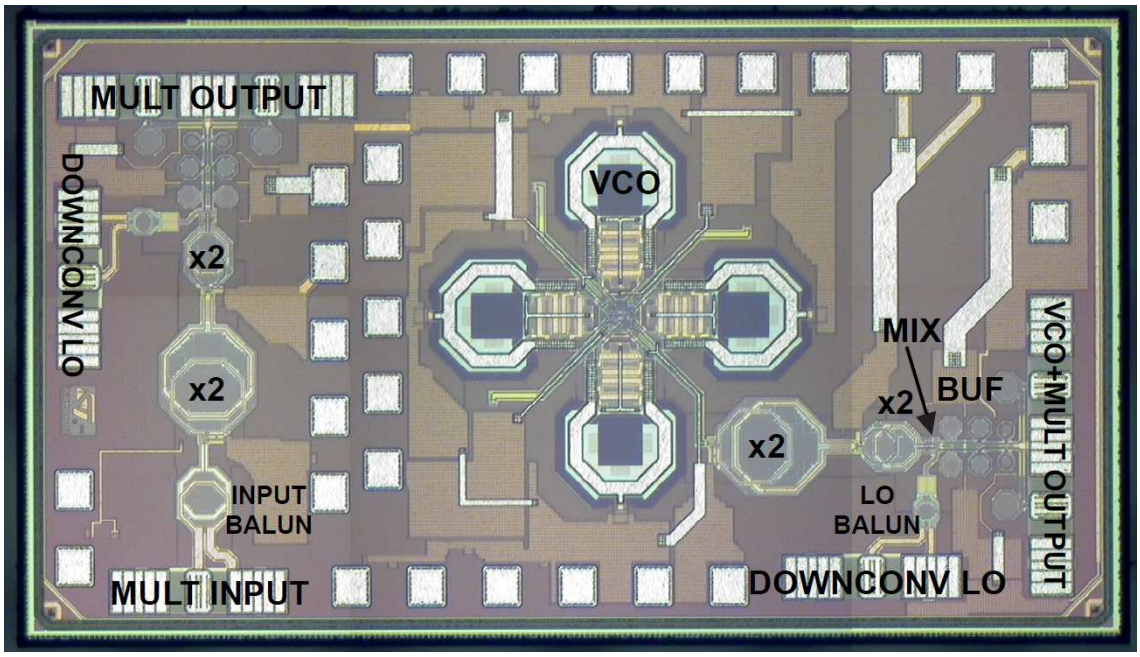

Figure 5.11: SAMARIS chip micrograph.

Finally, an improved version of the SAMARIS chip, named SAMARIS2, was realized. It mostly features two significant differences in the VCO with respect to SAMARIS. First, the oscillator-core tail filter was redesigned as in Fig. 5.4. The two VCO layouts for SAMARIS and SAMARIS2 are compared in Fig. 5.12. Additionally, independent frequency control of each oscillator core was included in SAMARIS2. This allows to force an artificial mismatch between the coupled oscillators, thus allowing to provide experimental verification of the model described in section 3.3. The 1.35x1 mm^2 SAMARIS2 test chip is shown in Fig. 5.13.

5.6 Conclusions

In this chapter, design strategies and implementation details for the realized frequency-synthesis building blocks, namely a 20GHz VCO and an E-Band frequency quadrupler, were presented. Three chips were realized in BiCMOS 55nm technology. In total, they include two testbench structures for independent characterization of VCO and multiplier, respectively, and two versions of the VCO+multiplier cascade. Measurements results are shown in the next chapter.

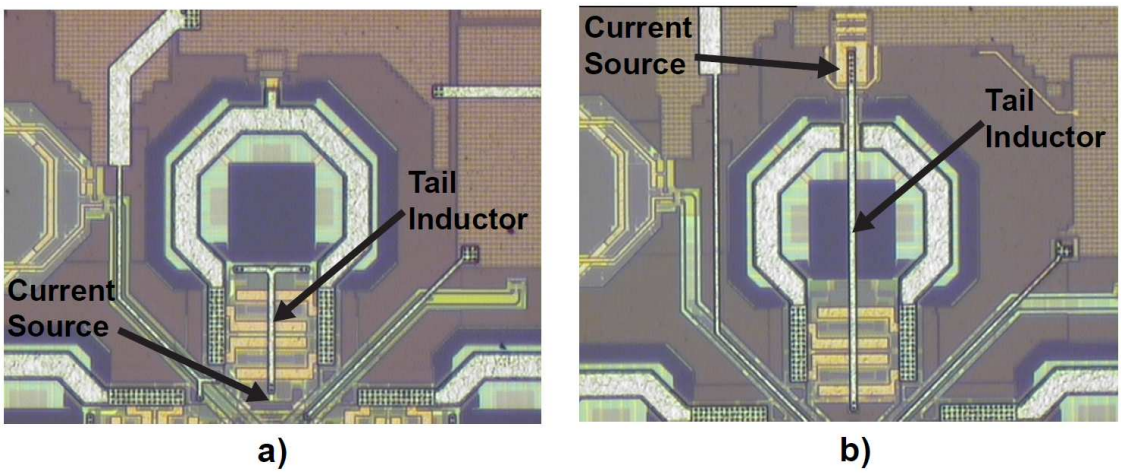

Figure 5.12: Comparison between the VCO cores in the (a) SAMARIS (see also schematic in Fig. 5.3) and (b) SAMARIS2 (see also schematic in Fig. 5.4) test chips.

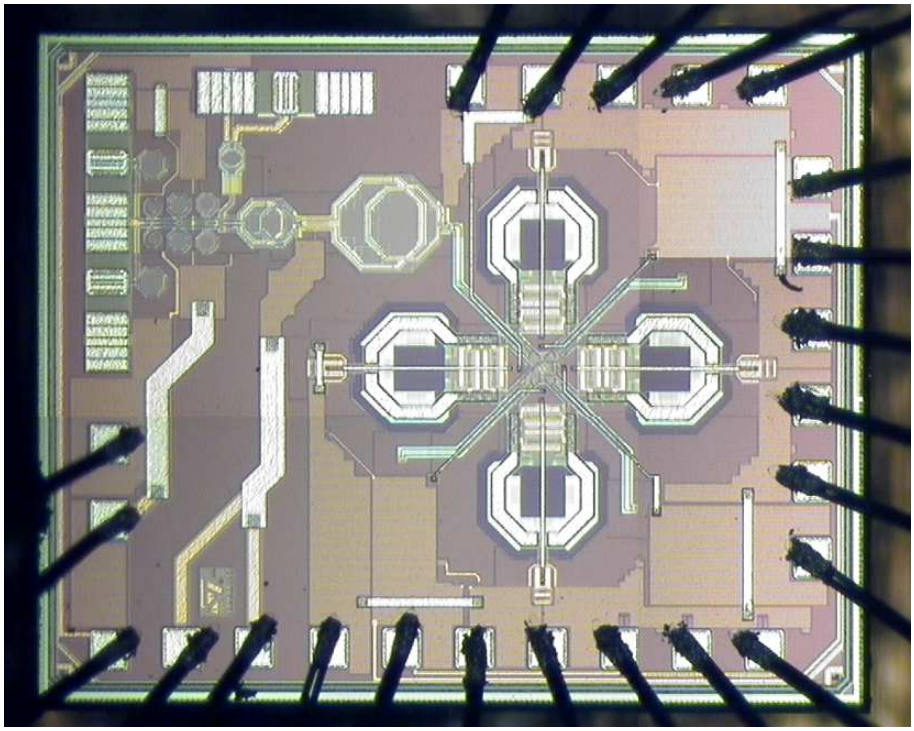

Figure 5.13: SAMARIS2 chip micrograph.

Chapter 6

Measurement Results

In this chapter, measurements on the test chips described in section 5.5 are presented. First, characterization results of the individual building blocks, i.e. the multi-core oscillator and the frequency quadrupler, are shown. Then, a complete overview of the performance of the E-Band frequency generator obtained by cascading VCO and multiplier is presented, and its performance is compared with other state-of-the-art implementations and with E-Band backhaul synthesizer requirements. Mismatch tests on the multi-core VCO, providing experimental verification to the model disclosed in section 3.3, are also displayed.

6.1 Stand-Alone Blocks Measurements

6.1.1 Quad-Core VCO

In this section, measurement results of the stand-alone quad-core oscillator implemented in the EBANDVCO test chip are presented. More extensive and accurate measurements on the E-Band frequency reference are shown in section 6.2.
The 20GHz VCO output signal is measured through a GSGSG probe, connected to a spectrum analyzer. Power supply, analog bias signals and digital controls are provided through bonding wires. The measurement setup is shown in Fig. 6.1. The oscillator consumes approximately 10 mW, 20 mW and 38 mW power from 1.2V supply in single, dual and quad core configurations, respectively.
Phase noise spectra at 20GHz oscillation frequency in single and quad-core configuration are shown in Fig. 6.2. It can be noticed how, when auxiliary oscillators

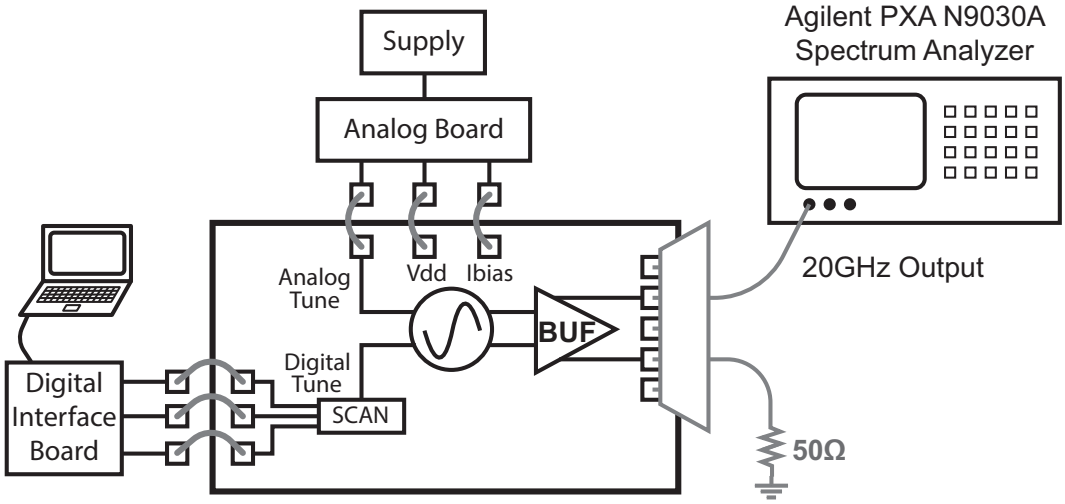

Figure 6.1: Measurement setup for the stand-alone VCO.

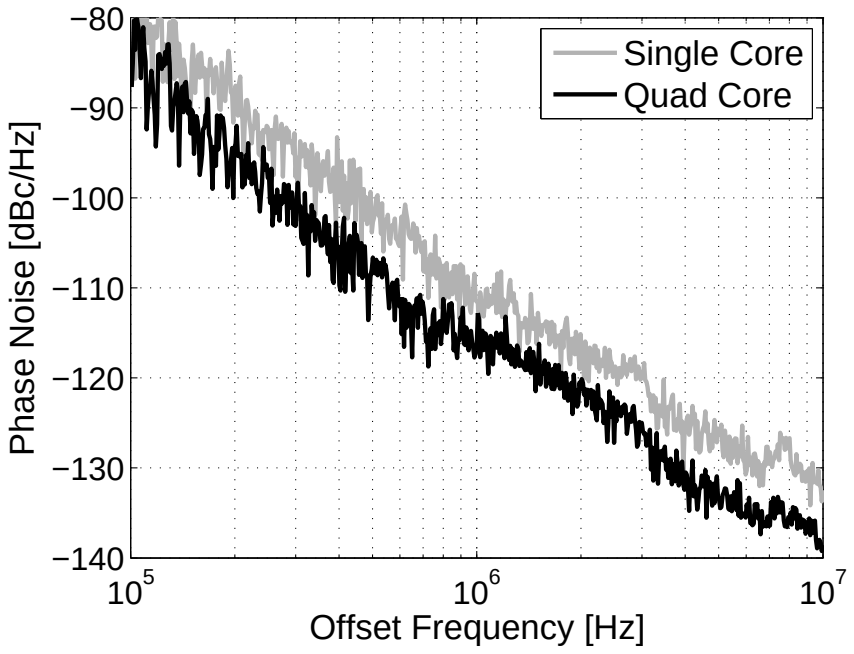

Figure 6.2: Measured VCO phase noise spectra at 20GHz frequency in single-core (grey) and quad-core (black) configurations.

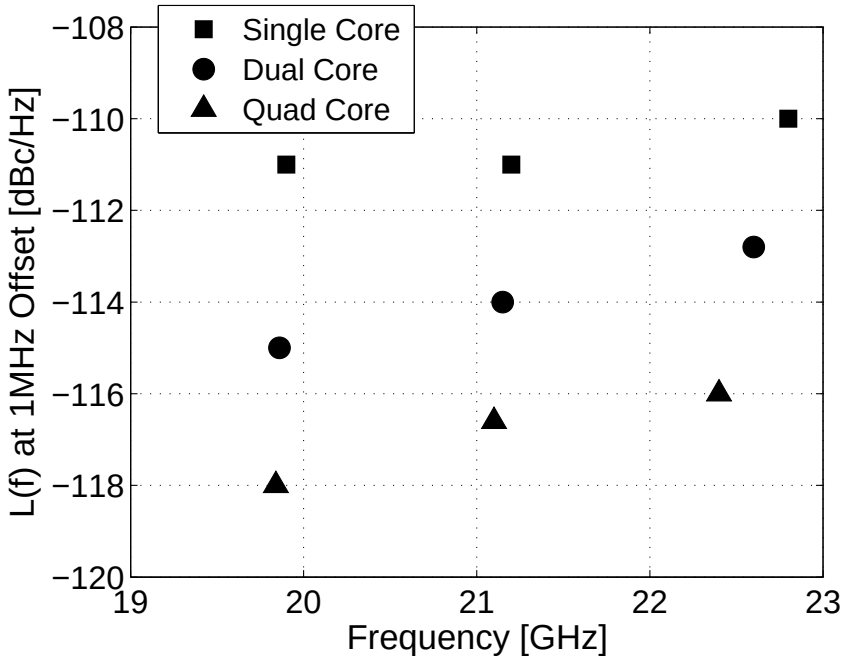

Figure 6.3: Measured VCO phase noise at 1MHz offset over the tuning range.

are turned on, the overall phase noise is significantly reduced, as expected from the multi-core oscillator analysis. The $1/f^3$ corner is around 800 kHz. Phase noise at 1MHz offset from the carrier, over the tuning range, is plotted in Fig. 6.3. The average phase noise is around -111 dBc/Hz for the individual core, -114 dBc/Hz in dual-core mode and -117 dBc/Hz in quad-core mode. Therefore, 3dB and 6dB noise reduction in dual- and quad-core configuration respectively is experimentally verified. The average FoM is around -188 dBc/Hz, and the tuning range is ∼14%.

6.1.2 Frequency Quadrupler

The frequency quadrupler was first measured as a stand-alone block to verify its performance. The measurements setup is shown in Fig. 6.4. An external signal generator drives an on-chip passive balun, providing 660mV,diff,0pk differential input to the first frequency doubler. A 47-70GHz tone from an external signal generator is used as a LO in the mixer, to downconvert the E-Band output to ∼15 GHz. Each stage draws 3 mA from 1.2V supply, resulting in ∼7 mW power consumption.
Fig. 6.5 shows the differential output swing of the multiplier, after mixer, buffer and

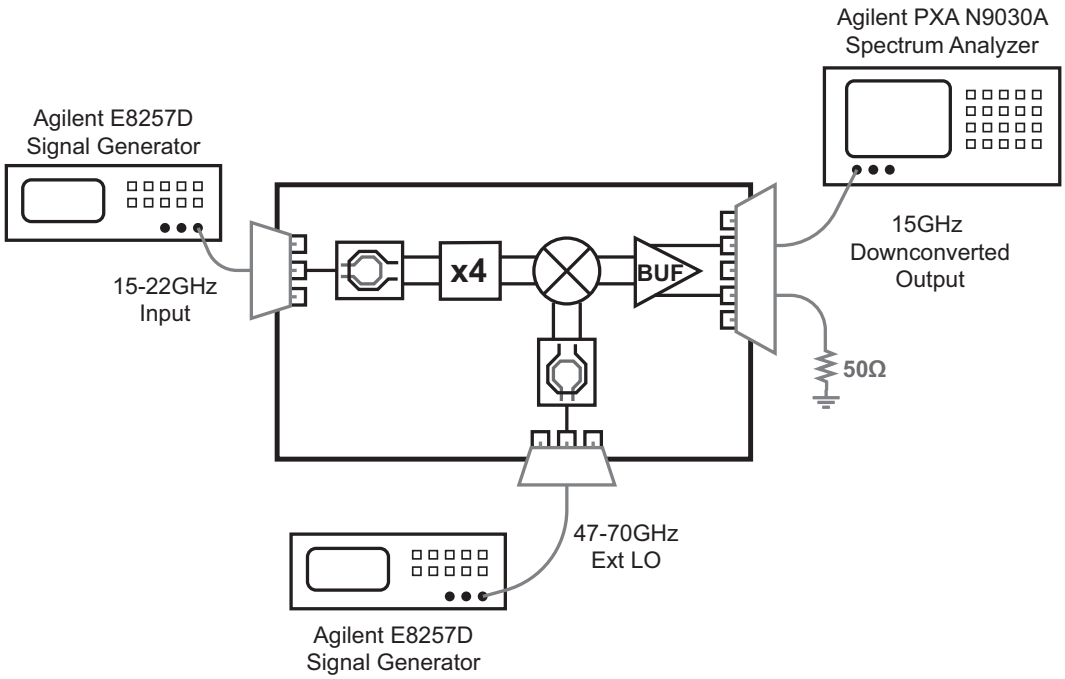

Figure 6.4: Measurement setup for the stand-alone frequency multiplier.

cable de-embedding. Black and grey plots correspond to different configurations of the tunable capacitive banks in the coupled resonators. The black curve constitutes the optimal configuration in terms of measured bandwidth. The maximum output voltage is approximately -12dBV with 27% fractional bandwidth around 74 GHz. Measurements show some gain penalty with respect to simulations, likely due to inaccurate EM simulation of the transformers and further non-idealities due to dummy filling. Measured amplitude difference between the positive and negative outputs is shown in Fig. 6.6. The imbalance is less than 0.5 dB over the whole frequency range, thus confirming that the capacitive-coupling-related mismatch in the transformers is successfully tackled.

Phase noise measurements are shown in Fig. 6.7. The circuit was fed by an external 17GHz tone featuring -110dBc/Hz phase noise at 100 kHz and -135dBc/Hz noise at 1 MHz. Note that this noise level is more than 10 dB better than state-of-the-art CMOS VCOs. The measured phase noise spectrum at the multiplier output (dark grey curve) is compared to the one of a noiseless multiplier (black curve). Phase noise at the output of an ideal noiseless frequency quadrupler is given by $L_{Out,IdMult} = L_{In}$+12dB, where L_{In} is the input phase noise. The 12dB noise penalty

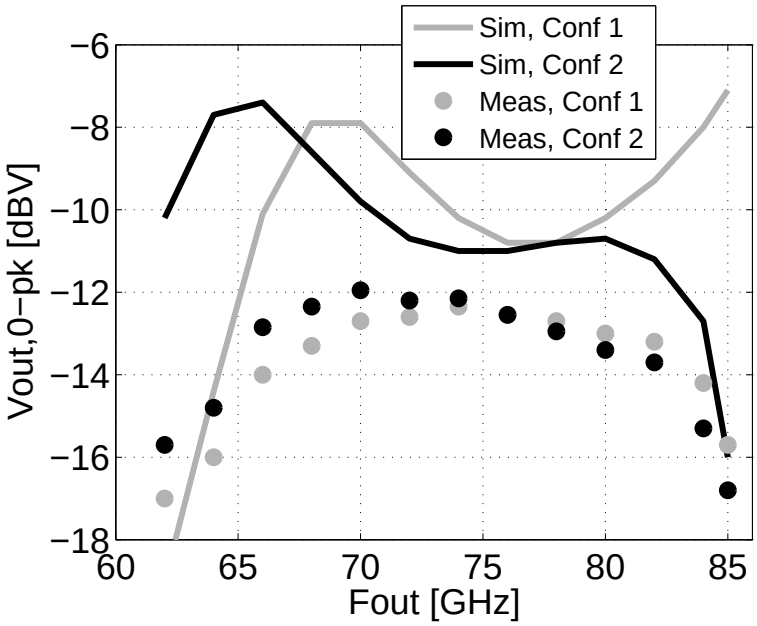

Figure 6.5: Measured and simulated multiplier differential output voltage over frequency, after mixer, buffer and cables de-embedding. Black and grey curves correspond to two different configurations of the tunable capacitive banks in the coupled resonators.

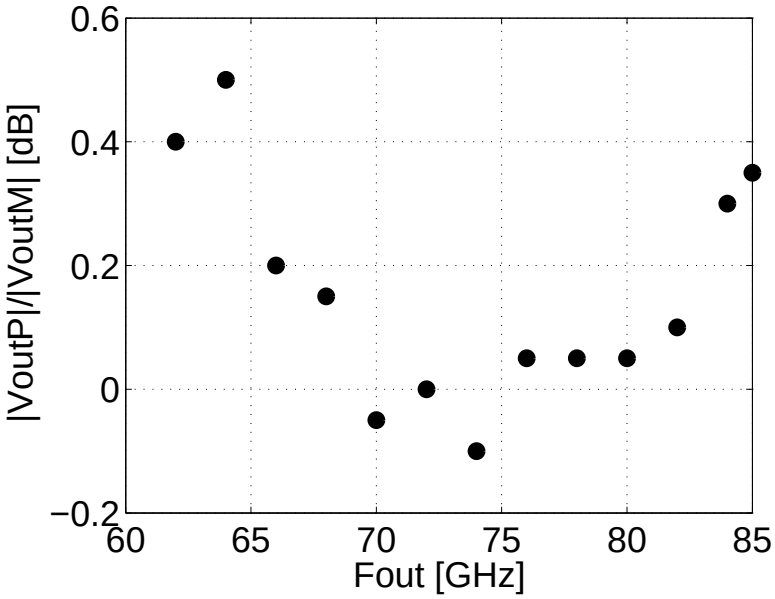

Figure 6.6: Measured amplitude imbalance between positive and negative multiplier outputs.

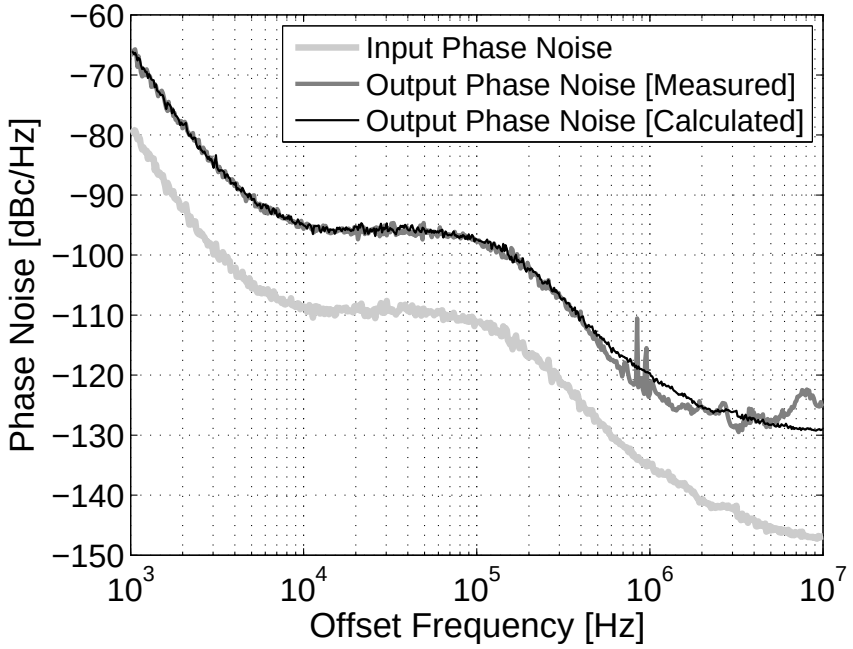

Figure 6.7: Measured phase noise spectrum at the multiplier's output (dark grey), compared with noise spectrum of the 17GHz input signal (light grey), and phase noise calculated from input spectrum assuming noiseless multiplier (black).

is inherent in the process of x4 frequency multiplication. To consider all the noise sources in the measurement setup, the phase noise of the external signal source used for downconversion has to be taken into account as well. Since the downconversion tone is uncorrelated with the input signal, its phase noise $L_{DownConv}$ is summed in power to the one of the multiplier output signal. Therefore, the black curve in Fig. 6.7 was calculated as:

$$L_{OutCalc} = 10\log_{10}\left[10^{\frac{L_{In}+12dB}{10}} + 10^{\frac{L_{DownConv}}{10}}\right] \tag{6.1}$$

The contribution of $L_{DownConv}$ is negligible below 1 MHz offset frequency, whereas its noise floor contribution on $L_{OutCalc}$ can be noticed in Fig. 6.7 above 1 MHz, where the black curve is more than 12dB higher than the input noise spectrum. The measured output noise spectrum plotted in Fig. 6.7 matches fairly well $L_{OutCalc}$, proving that the proposed multiplier does not introduce significant noise penalties, and it is therefore suitable as a building block of a low-phase-noise frequency synthesizer. The tones around 1MHz are due to unwanted couplings from external signals in the

	This work	[101]	[99]	[103]	[104]
Technology	**BiCMOS 55nm**	SOI 45nm	CMOS 65nm	SiGe 130nm	SiGe 100nm
Mult factor	**4**	2	2	4	4
Outputs	**Diff**	SE	Diff	SE	SE
f_{out} [GHz]	**74**	100	115	130	50
Frac BW	**27%**	16%	13%	5%	24%
V_{DD} [V]	**1.2**	3.6	1	1.6	3.3
P_{DC} [mW]	**7**	240	6	6.5	150
Gain [dB]	**-8**	-5	0	0.6∗	17
$A_{Out,0pk}$ [mV]	**250**	950	630	240∗	800
Fund Harmonic Rejection [dB]	**45**	N/A	N/A	N/A	>22
II Harmonic Rejection [dB]	**35**	N/A	N/A	N/A	>22
Area [mm^2]	**0.08**	N/A	0.015	0.03°	0.22

* Including 35mW input buffer
° Estimated from chip photograph

Table 6.1: Frequency quadrupler performance overview and comparison.

measurement setup and, as verified in the next section, do not show up when the VCO is used as an input.

Table 6.1 summarizes the quadrupler performance and compares to other state-of-art mm-Wave frequency multipliers. The proposed frequency quadrupler achieves the highest tuning range, together with very low power consumption. It also achieves high rejection of first and second harmonic components, and delivers an output voltage swing suitable for driving an on-chip mixer without requiring much amplification.

6.2 E-Band Frequency Generator Measurements

Finally, the E-Band frequency generator including the chain of multi-core VCO and frequency quadrupler was measured. We present here detailed characterization results of the SAMARIS2 chip, that achieves better noise performance leveraging

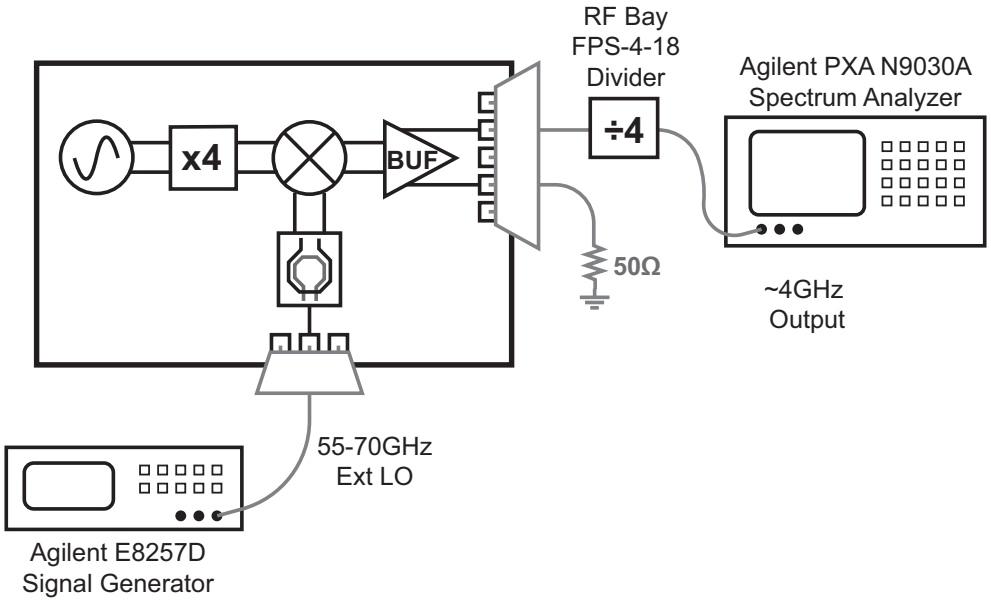

Figure 6.8: Measurement setup for the complete E-Band frequency generator.

the inductive tail filter depicted in Fig. 5.4. The performance is later compared with the SAMARIS chip, featuring an LC resonant tail filter as in Fig. 5.3.

The setup is shown in Fig. 6.8. It is very similar to the multiplier testbench in Fig. 6.4, although in this case the 20GHz input is generated on-chip by the VCO. To increase the precision of the noise measurement and reduce the oscillation-frequency drift, an off-the-shelf frequency divider-by-four was connected to the chip output.

The oscillator draws 9 mA, 18 mA and 36 mA current from 1.2V supply in single, dual and quad core configurations, respectively. The frequency quadrupler consumes 7 mW.

Phase noise spectra at the output of the frequency divider are plotted in Fig. 6.9 for the VCO working at minimum and maximum oscillation frequency. In both cases, significant noise reduction over the 100kHz-10MHz offset range, when the auxiliary cores are turned on, is verified.

Phase noise at 1MHz offset from the carrier over the tuning range, after divider de-embedding, is plotted in Fig. 6.10. The divider adds negligible excess phase-noise penalty, therefore it was de-embedded by adding 12 dB, resulting from the phase-division-by-four operation, to the measured noise data. The on-chip mixer does not significantly impacts on phase noise, as the external downconversion signal

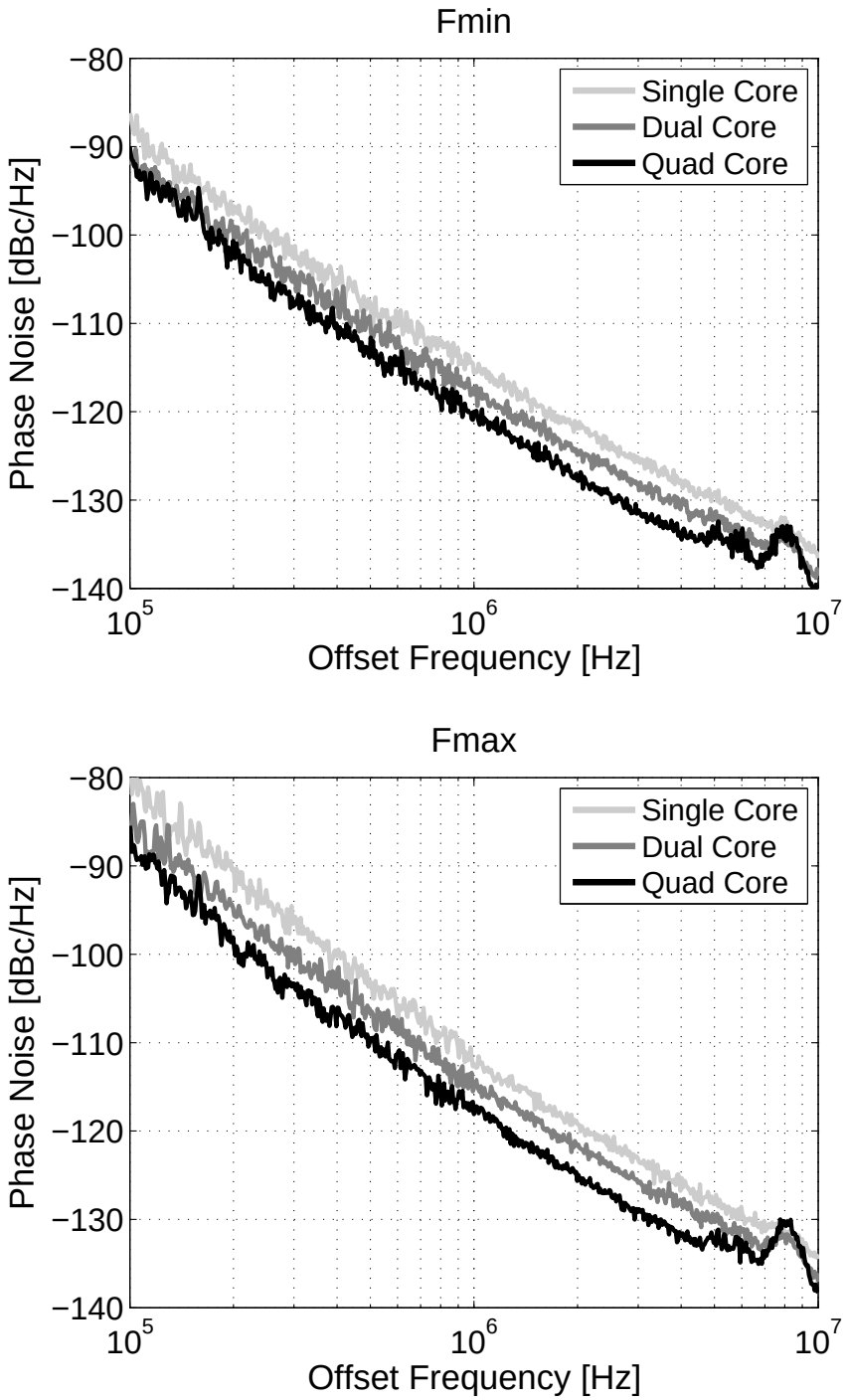

Figure 6.9: Measured phase noise spectra of the E-Band frequency generator operating at minimum (70 GHz) and maximum (82 GHz) oscillation frequency, after downconversion and frequency division by four, in single, dual and quad-mode configuration. Data are averaged over 10 measurements.

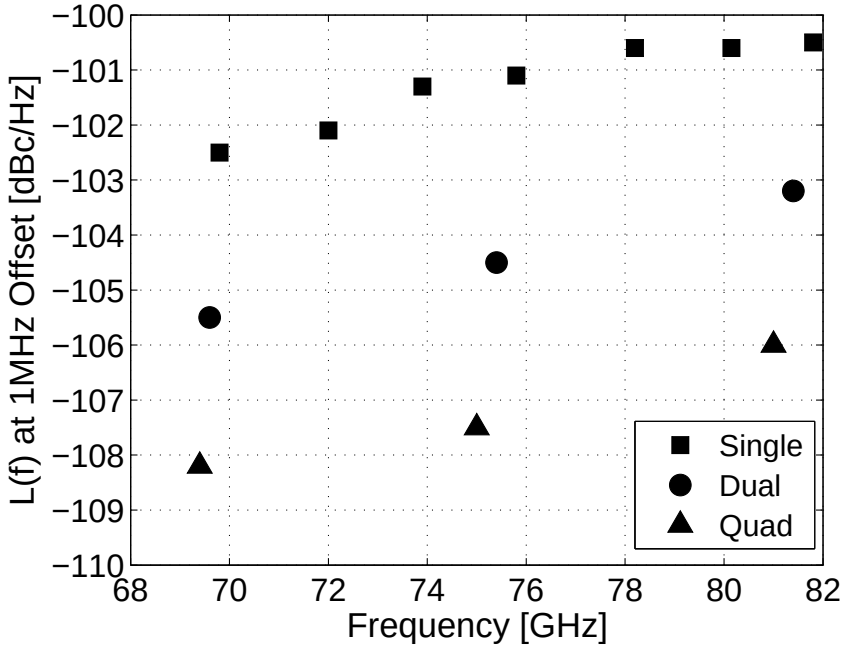

Figure 6.10: Measured E-Band phase noise at 1MHz offset over the tuning range in single, dual and quad-core configuration.

has a phase noise spectrum which is > 20dB lower than the one of the generated frequency reference.

As shown in Fig. 6.10, the measured VCO tuning range is 15%, and noise performance changes by ∼2 dB between $f_{MIN} \approx 70$ GHz and $f_{MAX} \approx 82$ GHz. 3dB and 6dB phase-noise reduction in dual and quad-core mode respectively is verified over the whole tuning range. On average, the circuit achieves -101dBc/Hz phase noise at 1MHz offset in single-core configuration and -107 dBc/Hz in quad-core mode. The latter value is compatible, with 5dB margin, with requirements for 64QAM E-Band transceivers derived in section 2.4.

The Figure of Merit at 1MHz offset is plotted in Fig. 6.11 over the tuning range. The FoM was calculated taking into account the power consumption of the whole frequency generator, including the multiplier. Since the multiplier power is a fixed overhead which does not impact on the noise performance, the FoM gets slightly better in quad-core configuration, where the quadrupler consumption is a smaller fraction of the total. The FoM ranges from -186 dBc/Hz to -188 dBc/Hz, while FoM_T ranges from -189.5 dBc/Hz to -191.5 dBc/Hz.

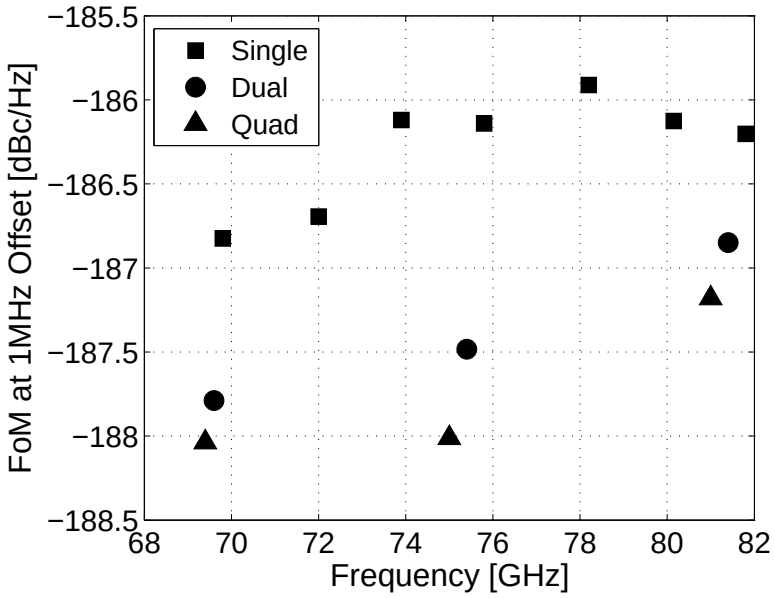

Figure 6.11: Measured E-Band FoM over the tuning range in single, dual and quad-core configurations.

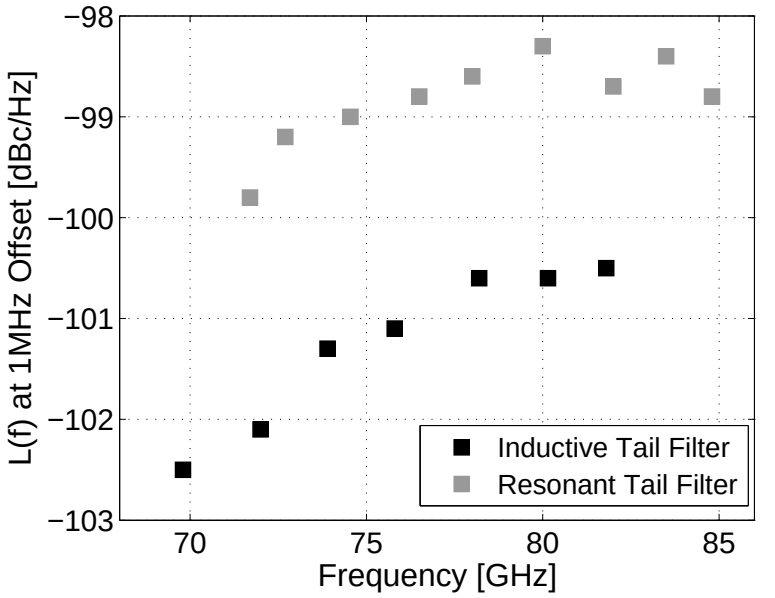

Figure 6.12: Measured E-Band phase noise at 1MHz offset over the tuning range in single-core configuration: comparison between the first design with resonant tail filter as in Fig. 5.3 (grey) and the improved design with inductive tail filter as in Fig. 5.4 (black).

	This work (single)	**This work (quad)**	[66]	[67]	[68]
Technology	**BiCMOS 55nm**	**BiCMOS 55nm**	BiCMOS 180nm	BiCMOS 130nm	BiCMOS 130nm
f_{out} [GHz]	**80**	**80**	52.5	62	93
Tuning range	**15**%	**15**%	26.5%	4.7%	8.3%
Phase Noise at 1MHz [dBc/Hz]	**-100.5**	**-106.5**	-108	-106	-102
$L_{eq,80G}$ [dBc/Hz]	**-100.5**	**-106.5**	-104.3	-103.8	-103.3
V_{DD} [V]	**1.2**	**1.2**	3	3	3.3
P_{DC} [mW]	**18**	**50**	132	39	90
FoM [dBc/Hz]	**-186**	**-187.5**	-181.2	-185.6	-181.8
FoM_T [dBc/Hz]	**-189.5**	**-191**	-189.6	-179	-180.2
Output	**Diff**	**Diff**	SE	SE	Diff
Area [mm^2]	**0.6**	**0.6**	0.17	0.1∗	0.05∗

∗ Estimated from chip photograph

Table 6.2: E-Band frequency generator (VCO + multiplier) performance overview and comparison.

In Fig. 6.12, phase noise at 1MHz offset in single-core configuration is compared with the one of the SAMARIS first implementation, featuring a resonant tail filter as in Fig. 5.3. The improved core design employing the inductive tail filter achieves approximately 2dB better phase noise.

Table 6.2 reports the performance overview and comparison with state of the art. As already discussed in section 2.5, for fair comparison phase-noise performance reported in literature has been normalized to 1MHz offset from 80GHz carrier ($L_{eq,80G}$), through eq. (2.7). Mm-Wave synthesizers featuring $L_{eq,80G} < -100$dBc/Hz are reported in the table. The proposed circuit achieves the lowest $L_{eq,80G}$, with FoM and FoM_T slightly better than other VCOs, and competitive tuning range. To authors' knowledge, this is the only synthesizer achieving these levels of phase noise at mm-Wave with <3V supply voltage. Moreover, the circuit features power-efficient noise scaling up to 6 dB.

A more extensive comparison with the state of the art is shown in Fig. 6.13 where, as already done in section 2.5, FoM and FoM_T are plotted versus $L_{eq,80G}$ for many mm-

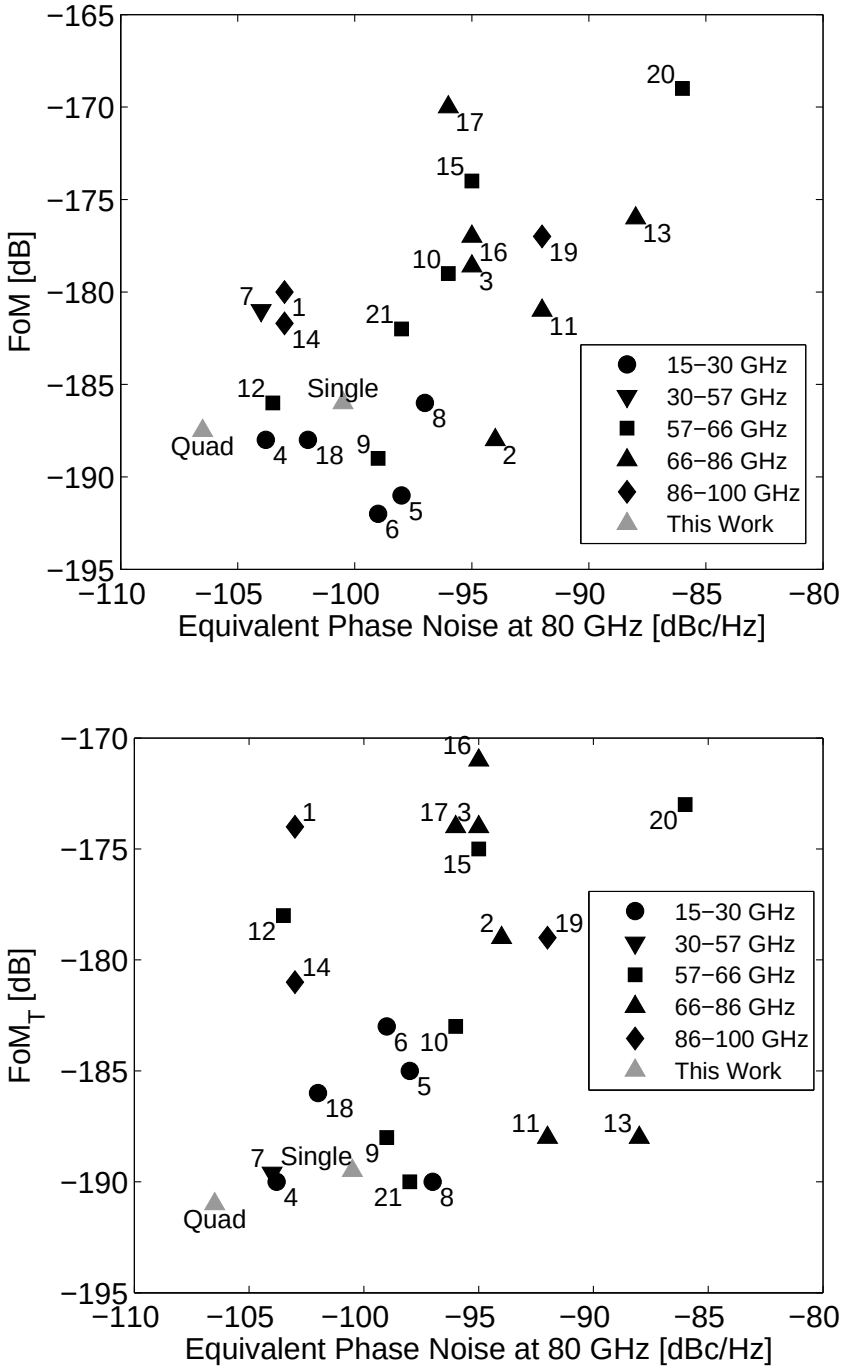

Figure 6.13: FoM and FoM_T versus equivalent phase noise at 1MHz offset from 80 GHz: comparison between measured results (grey markers) and state-of-the-art mm-Wave VCOs performance (black markers). Different markers are used for different output frequency ranges. References are provided in Table 2.1.

Wave VCO and VCO+multiplier implementations reported in literature. Measured data from the SAMARIS2 chip are now added to the plots.

6.2.1 Mismatch Tests

Two features were introduced in the SAMARIS2 chip to perform mismatch tests on the multi-core VCO, as depicted in Fig. 6.14. First, each core has an independent digital control of the tank capacitance. This allows to force a mismatch between cores, and experimentally measure locking range and phase-noise penalty resulting from component mismatch. Also, the coupling switches are segmented in two 20µm-wide transistors, individually controlled. As a result, the coupling switch width can be either set to 20 µm or 40 µm.

The measured phase-noise penalty in the dual-core VCO, when varying frequency mismatch, is plotted in Fig. 6.15 for the two switch size values. Consistently with eq. (3.25), when the switch width W_{SW} is doubled so that its series resistance is cut by half, the locking range is increased by ∼2. For both 20µm and 40µm wide switch, measured data match the model very well. Some excess noise with respect to the model is only seen close to the locking range, consistently with simulations (see Fig. 3.6 and 3.10).

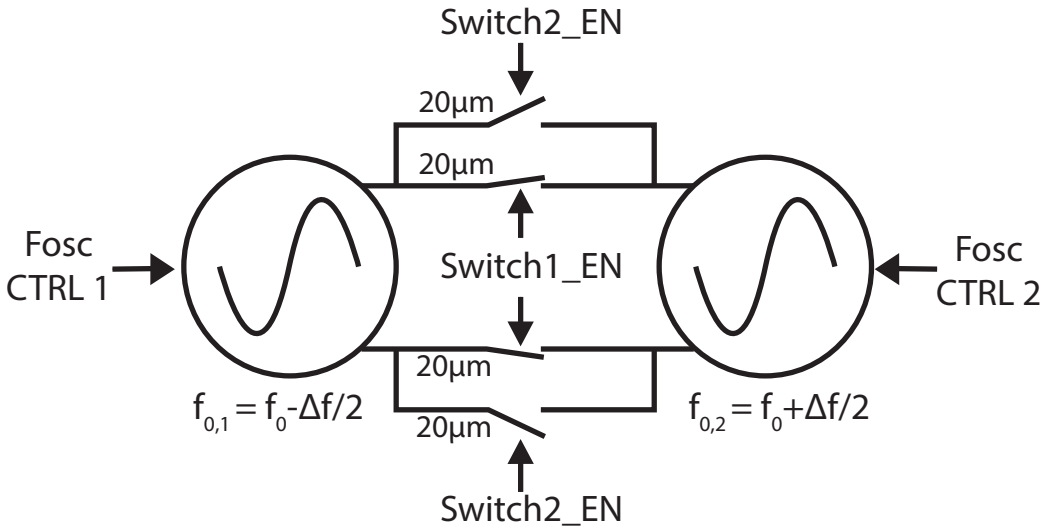

Figure 6.14: Independent resonance-frequency control and coupling-switch width selection employed in the mismatch tests.

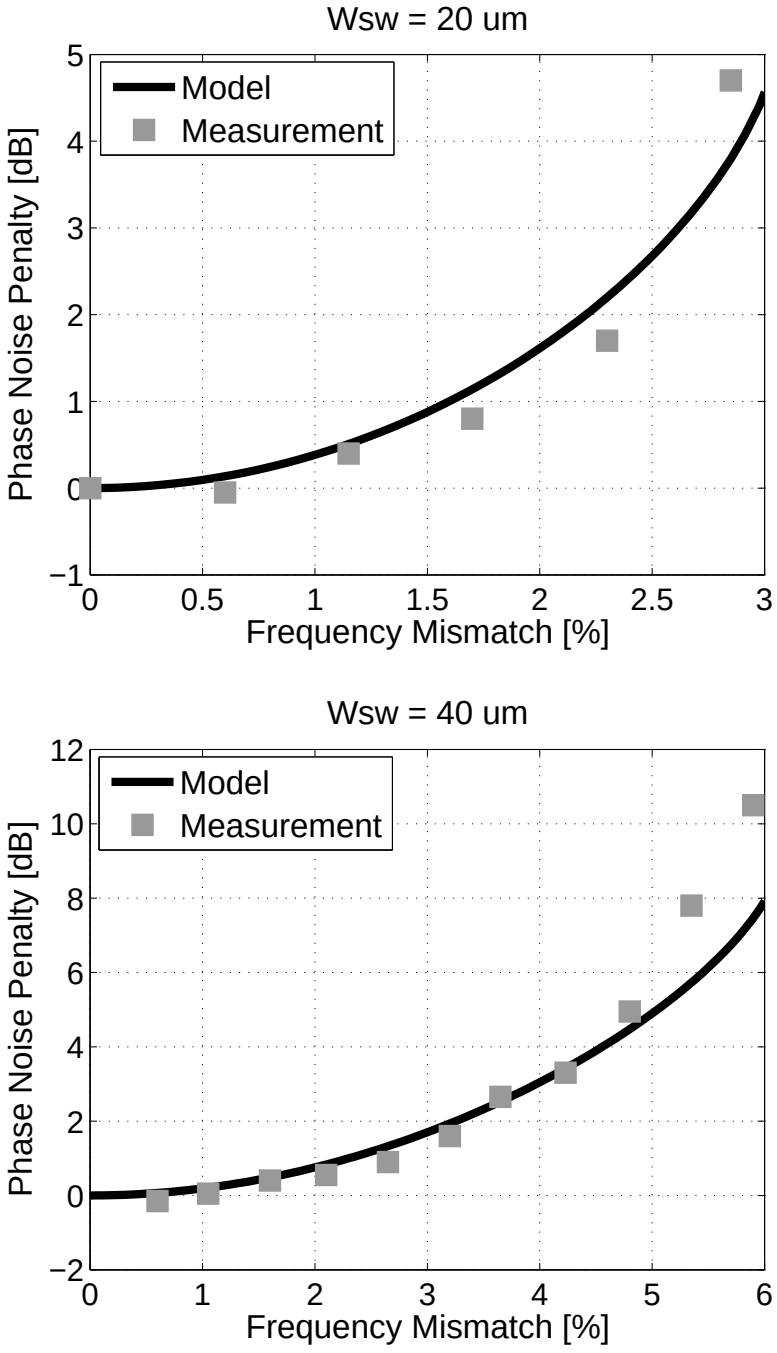

Figure 6.15: Phase-noise penalty at 5MHz offset versus resonance frequency mismatch in the dual-core oscillator: comparison between measured data (grey squares) and calculated values through eq. (3.68) (black line). The two plots correspond to 20μm and 40μm coupling-switch width respectively. Data stop where the system loses locking.

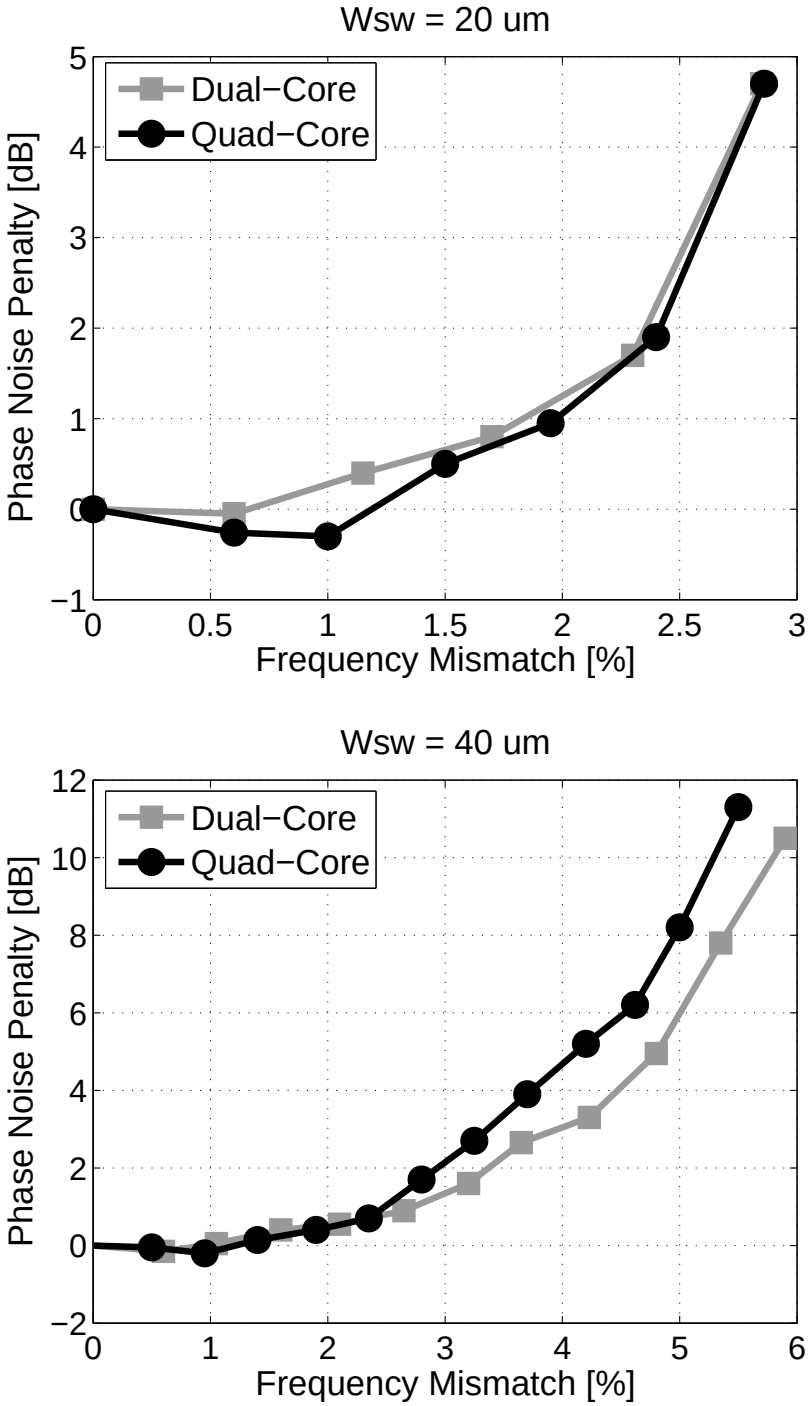

Figure 6.16: Measured phase-noise penalty at 2MHz offset versus resonance frequency mismatch: comparison between dual-core mode and quad-core mode. The worst-case mismatch distribution shown in Fig. 3.13 was used for the quad-core oscillator.

Mismatch tests have also been performed on the quad-core oscillator. First, it was verified that the worst-case mismatch distribution is the one depicted in Fig. 3.13, in agreement with simulation and model results. The measured phase-noise penalty when varying the resonance-frequency mismatch is plotted in Fig. 6.16, and compared with dual-core results. It can be noticed how dual- and quad-core oscillators have approximately the same locking range, and comparable noise penalties versus frequency mismatch. This is a specific property of quad-core oscillators connected in a ring-like fashion, as already pointed out in section 3.3.2. That observation is therefore experimentally verified.

6.3 Conclusions

In this chapter, measurement results on the proposed frequency-synthesis building blocks were presented. On the multi-core VCO, 3dB and 6dB noise reduction in dual-core and quad-core configurations were experimentally verified. The standalone frequency quadrupler achieves wideband operation, competitive with state-of-the-art broadband mm-Wave multipliers, with 27% fractional bandwidth. The effectiveness of the proposed common-mode isolation was also confirmed, and the multiplier showed negligible phase-noise degradation.

Cascading the two blocks, a low-noise E-Band frequency reference was obtained. Measured phase noise at 1MHz offset in quad-core mode ranges from -108 dBc/Hz and -106 dBc/Hz over a 70-82GHz tuning range, best among integrated E-Band synthesizers to our knowledge, despite using only 1.2V supply. The noise performance also meets requirements for 64QAM transceivers derived in chapter 2, with several dB of margin. Furthermore, the frequency generator shows very competitive FoM and FoM_T values. Thanks to multi-core operation, power consumption can be significantly reduced when the phase-noise performance is relaxed by 6 dB, with only $\sim$1.5dB FoM penalty. Finally, mismatch tests on the multi-core oscillator showed very good agreement with the model developed in chapter 3.

The oscillator's tuning range can be extended in future versions to cover both the 71-76GHz and 81-86GHz bands. An increase from the current 15% value to 20-25% is expected to be feasible by reducing the switch width in the capacitor bank. Although this would lower the tank's quality factor, simulations predict a phase-noise and FoM increase below 2dB.

Conclusions

Point-to-point wireless links in the E-Band (71-76GHz and 81-86GHz bands) can provide high-data-rate, easily-deployable, cheap and flexible backhaul solutions, important enablers for the mobile network evolution towards 5G. The development of CMOS/BiCMOS integrated transceivers for E-Band backhaul applications can help reducing the cost and footprint of the equipment, but presents design challenges, mostly related to the use of spectrally-efficient high-order modulations.

In this dissertation, we addressed LO generation requirements for E-Band backhaul applications. First, we identified phase-noise specifications for the frequency synthesizer, and their dependence on the modulation order. Second, we designed custom analog building blocks in BiCMOS 55nm technology, namely a VCO and a frequency quadrupler, to achieve the required performance with high power efficiency.

The VCO leverages multi-core operation to achieve ultra-low noise performance, and allows noise tunability according to system requirements. The topology was studied in depth, and an analytical model describing the system performance in presence of mismatches was developed. The model allows better understanding of the robustness of the proposed solution, and useful insights on how to compare interconnection strategies in in-phase coupled oscillators.

The frequency multiplier converts the $\sim$20 GHz oscillator tone in an E-Band frequency reference. It is based on the chain of two push-push frequency doublers, and exploits transformer-coupled resonators for bandwidth enhancement. The circuit achieves broadband operation with low power consumption and negligible noise degradation. Common-mode isolation techniques, resulting in higher power efficiency

and harmonic rejection, were investigated.
The cascade of the two building blocks provides an ultra-low noise E-Band frequency reference, suitable for LO generation in direct-conversion backhaul transceivers. The measured prototypes achieves around -107 dBc/Hz phase noise, the lowest reported in literature at these frequencies to our knowledge, over a 70-82GHz tuning range, with 50mW power consumption. Thanks to efficient noise scaling in the VCO, power consumption can be reduced by a factor of $\sim$3 when the phase-noise performance is relaxed by 6 dB, a useful feature in adaptive-modulation E-Band transceivers.
Further developments will include VCO tuning-range extension to cover both 71-76GHz and 81-86GHz bands and design of a block for generating quadrature phases starting from the realized frequency reference (e.g. a polyphase filter or an injection-locked oscillator), as well as the integration of the blocks in a complete E-Band frequency synthesizer.

List of Publications

1. L. Iotti, A. Mazzanti and F. Svelto, "A low-power 64-84GHz frequency quadrupler based on transformer-coupled resonators for E-Band backhaul applications", *2016 IEEE Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, June 2016, pp. 1-4.

2. L. Iotti, A. Mazzanti and F. Svelto, "A multi-core VCO and a frequency quadrupler for E-Band adaptive-modulation links in 55nm BiCMOS", *2016 IEEE European Solid-State Circuits Conference (ESSCIRC)*, Sept 2016, pp. 373-376.

   Submitted, under revision

3. L. Iotti, M. Bassi, A. Mazzanti and F. Svelto, "Design of low-power wideband frequency quadruplers based on transformer-coupled resonators for E-Band backhaul applications", *Integration, the VLSI Journal of* (invited paper)

4. L. Iotti, A. Mazzanti and F. Svelto, "Insights into switch-coupled multi-core VCOs for phase-noise scaling at mm-Waves", *IEEE Journal of Solid-State Circuits* (invited paper)

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