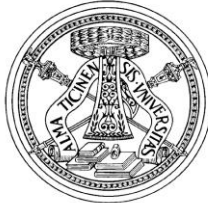# Universita degli Studi di Pavia

Facolta di Ingegneria
Dipartimento di Ingegneria Industriale e dell'Informazione

Doctoral Thesis in Microelectronics
XXX Ciclo

High Performance Building Blocks for SAW-Less Transceivers & Design of Ultra-Low Power Receiver for Wireless Sensor Networks

Supervisor:
Chiar.mo Prof. Danilo Manstretta

Coordinator:
Chiar.mo Prof. Guido Torelli

Author:
Ehsan Kargaran

A thesis submitted in fulfilment of the requirements
for the degree of Doctor of Philosophy.

October 2017

Declaration of Authorship

I, EHSAN KARGARN, declare that this thesis titled, "*High Performance Building Blocks for SAW-Less Transceivers & Design of Ultra-Low Power Receiver for Wireless Sensor Networks*" and the work presented in it are my own. I confirm that:

- ➢ This work was done wholly or mainly while in candidature for a research degree at this University.

- ➢ Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated.

- ➢ Where I have consulted the published work of others, this is always clearly attributed.

- ➢ Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work.

- ➢ I have acknowledged all main sources of help.

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Signed:

Date:

Abstract:

To keep up with the increasing demand for higher data rates, 5G will introduce new multiple-input multiple-output (MIMO) techniques and enhance existing ones such as beamforming and diversity. This, combined with larger bandwidths, more complex modulations and increased number of bands and modes will greatly increase terminal complexity. Presently, to meet the stringent specifications of frequency division duplexing (FDD) cellular standards, for each operating band, a highly selective duplexer (based on surface acoustic wave (SAW) filters) is used to connect receiver and transmitter to the shared antenna. In recent years, various interference mitigation techniques have been introduced with the goal of replacing the off-chip filters with tunable on-chip counterparts, thus significantly reducing system cost and complexity. Nonetheless, given the extremely challenging interference scenario, this is still an open issue. In the first part of this thesis, a highly linear low noise transconductance (LNTA) is proposed to be easily integrated in an advanced wireless receiver with a self-interference cancellation performance that significantly improves state-of-the-art while removing bulky component like SAW filter. The proposed LNTA demonstrated an antenna input referred IIP3 of 27 dBm while consuming only 14 mW and facilitating removing bulky and off-chip components like SAW filter leading to considerably cost benefit.

The increasing demand for wearable wireless devices has motivated the research on ultra-low power (ULP) transceivers. Some ULP applications, such as wireless medical telemetry and Wearable-Wireless Sensor Networks (W-WSN) require the portable devices to operate from a single Lithium Ion battery or to use energy harvested from the environment. This makes low supply voltage operation an additional stringent requirement. For WSN, it is especially critical to have a ULP receiver since the sensor is mostly operating in the receive mode rather than in transmit mode. As a consequence, its overall power consumption is determined by the receiver chain. Low Noise Amplifier (LNA) is the first block of the receiver chain and generally considered as one of the most power hungry blocks due to performing simultaneous tasks. In Bluetooth Low Energy (BLE) application, the RF spec is very relax in the favor of reducing dissipation power. Thanks to introducing a novel and efficient current reuse technique and also passive gm boosting, the LNA input impedance is reduced by factor of 24 compared to a single transistor using the same current. Hence, the proposed LNA with RF spec which far exceeded the requirements of intended application while consuming only 30 µW is presented in the second part of this thesis. In fact, the, overall performance of the proposed LNA is almost three times better than the stat of the art.

Furthermore, thanks to extensively utilizing current reuse scheme and employing forward back gate biasing in advanced technology of 22 nm FD-SOI, it enables to design an ULP receiver for BTLE application. The proposed receiver consumes much less power compared to state-of-the-art receivers and far exceed the requirements of wireless sensor network standards such as BT-LE. It can operate with supply voltage as low as 0.4V while consumes only 100 µW with much smaller chip area, better NF and better linearity compares to the-state-of-the-art.

Acknowledgments

And yet another chapter in my life has faded away, and it has taught me a precious little lesson:

"Patience is bitter, but its fruit is sweet."

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1 Chapter 1

Basic RF Concepts and LTE Standards

1.1 Motivation

The profusion of wireless and cellular communication standards facilitates the integration of multi-band, multi-mode radios into mobile devices a universal trend. A recent mobile platform usually requires to cope with other connectivity standards including Wi-Fi or Bluetooth along with 2G/3G/4G radio access technologies. Furthermore, the number of bands to has be supported by the developing radio standards, including LTE or WiMAX, has enlarged tremendously.

Fig.1.1 shows the crowded spectrum of today's wireless communication. The technology trend during the last few years is towards system on chip which is able to process multiple standards re-using most of the digital and digitization resources.
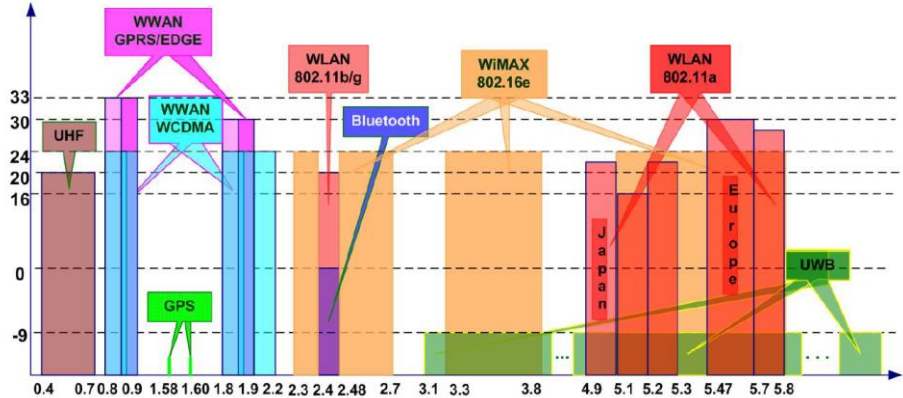
Figure 1-1: Crowded radio spectrum showing co-existence with multiple standards

A wireless transceiver requires the flexibility of operating within a wide range of frequencies, while simultaneously being able to deal with co-existence problems where, for instance, a receiver tries to detect a weak signal in the vicinity of at least one active transmitter. Strictly speaking, the problems associated with multi-mode operation are also present in narrowband dedicated transceivers. However, it is the wideband nature of a multi-mode transceiver that causes several of these problems to be much more pronounced.

For instance, Figure 1.2 represents the embedded RF blocks in the popular iPhone 5 smartphone, incorporating 2G/3G/4G, Bluetooth, WLAN, GPS and FM. It can be observing an external Power Amplifier (PA) and duplexer/SAW (surface acoustic wave) filter is utilized for each WCDMA/GSM/EDGE band. Additionally, for GPS, BT/WLAN 2.4 GHz, and WLAN 5 GHz transceivers, separate SAW filters are employed and leading to requiring in total 9 external SAW filters for all the transceivers.
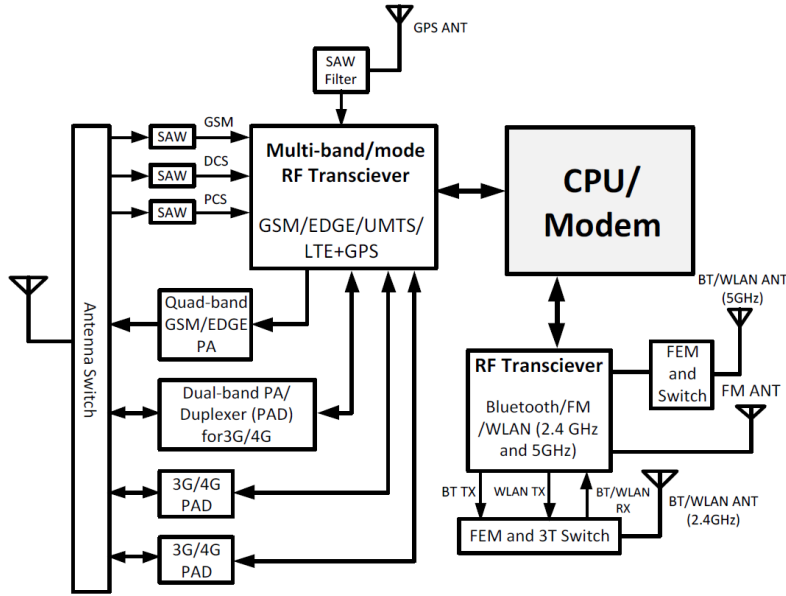
Figure 1-2: A simplified schematic of the newest multi-mode, multi-band iPhone 5 smartphone announced in 2012 [source: http://www.ifixit.com/Teardown/iPhone+5+Teardown/10525].

To address the requirements for highly mobile devices, manufacturers are interested in reducing size and cost by using minimal external components and allowing a flexible functionality such that minimum power to be consumed in mobile devices. High performance receiver use external SAW filter to encounter the stringent blocking conditions in cellular radios. SAW filters, however, are bulky and expensive; additionally, receiver flexibility can be reduced and it degrades the receiver sensitivity by 2 to 3 dB.

Fig. 1.3 is the SAW-less direct conversion receivers. It can be noticed that the dedicated expensive, off chip SAW filter is removed. The co-existence issue becomes more severe in broadband multi-standard receivers and is a bottle neck. Since the amount of out-of-band (OOB) power is excessive compared with the desired channel as can be seen in Fig. 1.1, the linearity of both front-end and digitizer becomes the main limitation for achieving the required performance. This issue is even more relevant for cost effective SAW-less architectures, where no or very weak RF filtering is present at the low noise amplifier (LNA) input. Non-linearities generate cross products and some of them are folded-back into the main channel increasing dramatically the in band noise level.
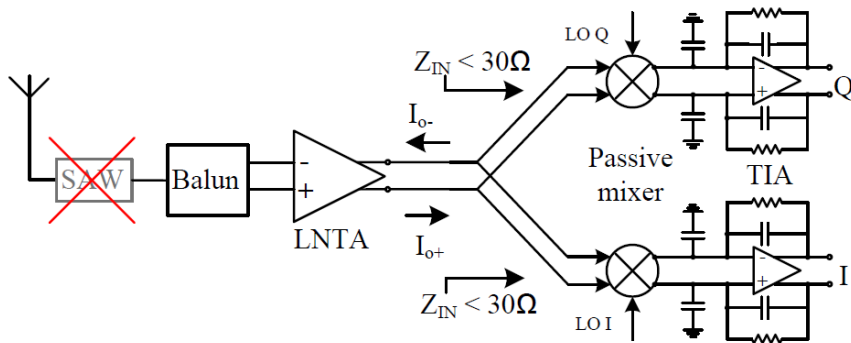
Figure 1-3: SAW less direct conversion receiver

Software defined radios (SDRs) achieve the required performance to replace the dedicated radios but also reconfigure to other standards and hence pose a benefit. Fixed, High-Q SAW filters are usually employed before the dedicated radio front ends to remove the large out of band interference. These SAW filters are expensive, not on CMOS process and not suited for reconfigurable radio concept. Removing this dedicated filter decreases the cost of the radio and makes the SDR possible but requires the radio receiver to accommodate much higher linearity than a standard dedicated radio. So this research focuses on the advancement of SDRs and implementing the radios on the inexpensive CMOS process by developing high linearity radio front ends. However, the RF front-end must co-exist with high power blockers due to the lack of RF filtering, hence demanding more linear LNAs and Mixers. In this way, this research advances the science and/or technology.

From a radio receiver's perspective, three main problems are exacerbated in wideband operation, namely: distortion, harmonic mixing, and phase noise. As will be seen from the subsequent discussion, these problems all dictate a higher linearity requirement for the receiver. Theoretically, a brick-wall noiseless channel select filter that would extract the desired signal right at the antenna would provide an ultimate solution to these problems.

1.2   Basic RF concepts:

1.2.1   Dynamic Range:

One of the most important figure of merit of receivers is the dynamic range since its definition includes both noise and non-linear behavior. This parameter can be defined in two possible ways. The first is simply called Dynamic Range (DR) and it refers to the maximum tolerable desired signal power divided by the minimum appreciable desired signal power (the sensitivity). This definition is limited by noise at the lower end and by the compression at the upper end as shown in Fig. 1.4a. The second type, called the Spurious Free Dynamic Range (SFDR), involves both noise and interferers. The lower end is still the sensitivity but in this definition the upper end is limited by the Intermodulation (IM) products, more specifically, the maximum input level in a

two-tones test for which the third-order IM products do not exceed the integrated noise of the receiver (Fig. 1.4b).
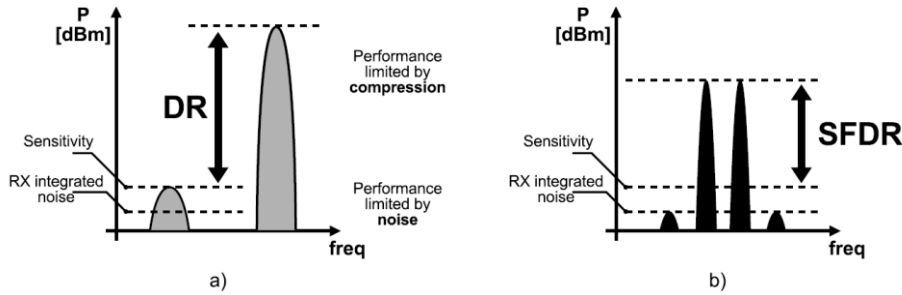
Figure 1-4: Dynamic range definitions: a) DR; b) SFDR

1.2.2   Gain Compression

Without any RF filtering in front of the RX chain a gain compression can happen due to the large out-of-band interferers as shown in Fig. 1.5. Desensitization can occur due to limited current range (slewing) or from limited voltage swing (clipping) and its main effect on a RX is the lower Signal-to-Noise- Ratio (SNR). In order to quantify desensitization is useful to express the gain with a power series in which there are the first non-linear terms.

$$y(t) = x(t).a_1 + x^2(t).a_2 + x^3(t).a_3 + ... \qquad (1.1)$$

where y(t) is the output signal x(t) is the input signal and α_1, α_2, α_3 are the linear amplification term, the second order and the third order nonlinear terms. When a desired signal is applied to a non-linear system described by Eq. (1.1) is possible to show that, with an input signal define as x(t)=A_{in}cos(ω_{in}t) + A_{blk}cos(ω_{blk}t) the non-linear terms affect the gain as shown in Eq. 1.2.

$$y(t) = (a_1 A_{in} + \frac{3}{4} a_3 A_{in}^3 + \frac{3}{2} a_3 A_{blk}^2 A_{in}) \cos(\omega_{in} t) + ... \qquad (1.2)$$

If the gain is perfectly linear only the first term α_1 is present, otherwise if it presents a non- linear behavior the third-order coefficient α_3 appears. This leads to a gain that is dependent from the amplitude of the input signal Ain and, if it is present, from the amplitude of the blocker signal A_{blk}. This means that the gain should be desensitized by the input signal itself or by an OOB blocker due to the fact that no RF filtering is provide in front of the RX chain.

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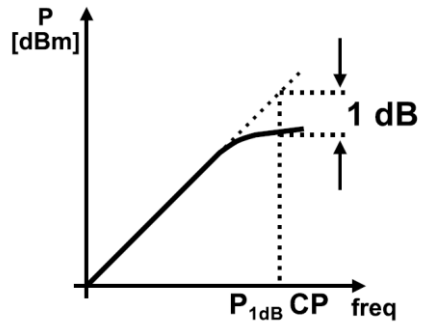
Figure 1-5: Gain 1dB compression point

1.2.3 Reciprocal Mixing

Since RF passive filtering has been ruled out, the convolution between a blocker spectrum and LO phase noise performed by the mixers can be a serious matter in a wideband RX. This phenomenon adds a further term in the total output noise increasing the NF of the RX (Fig. 1.6). Without any RF filtering, in order to obtain the same level of noise at the output of the chain, the LO phase noise must be reduced by a quantity equal to the increment in dB of the blocker power [7] [13].
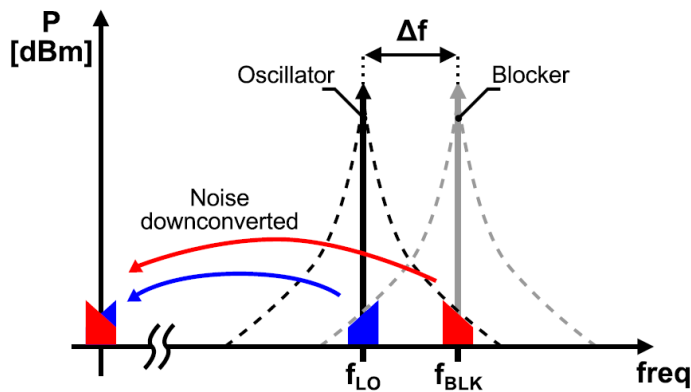
Figure 1-6: Reciprocal mixing

1.2.4   Harmonic Mixing

Due to the lack any filtering, the blockers located at multiple of the LO frequency can be also down converted to the Intermediate Frequency (IF) on top of the desired signal (shown in Fig. 1.7). The conversion gain of blockers at different frequencies is different and is related to the duty-cycle of the square wave used to drive the LO port of the mixer [7].
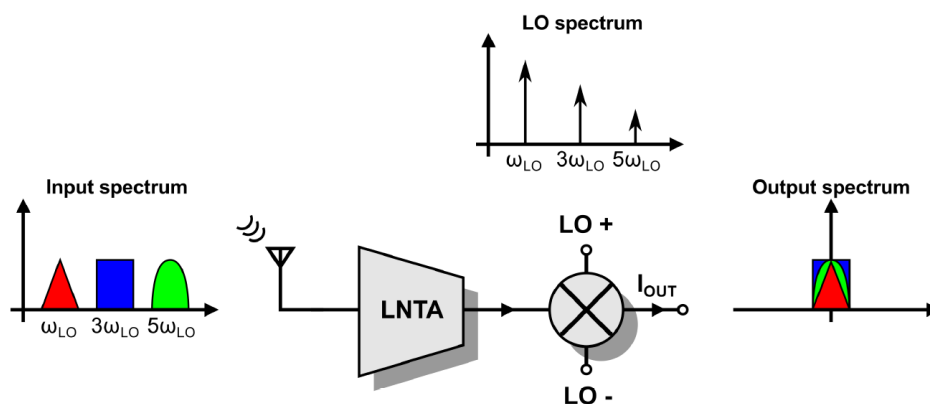
Figure 1-7: Harmonic mixing

1.2.5   Noise Folding

Folding of the LNTA output noise is another important issue which needs to be considered. The NF after mixer can be increased by the convolution between the LNTA output noise and the LO frequency components. The increasing noise at the mixer output depends on the frequency shaping of the LNTA output noise and from the number of phases that creates the LO signal. This can be shown in Fig.1.8. On the other hand, noise folding occurs even when no blocker is present and can only be reduced by minimizing the noise energy at the LNTA output at the LO harmonics or using more phases [7] [13].
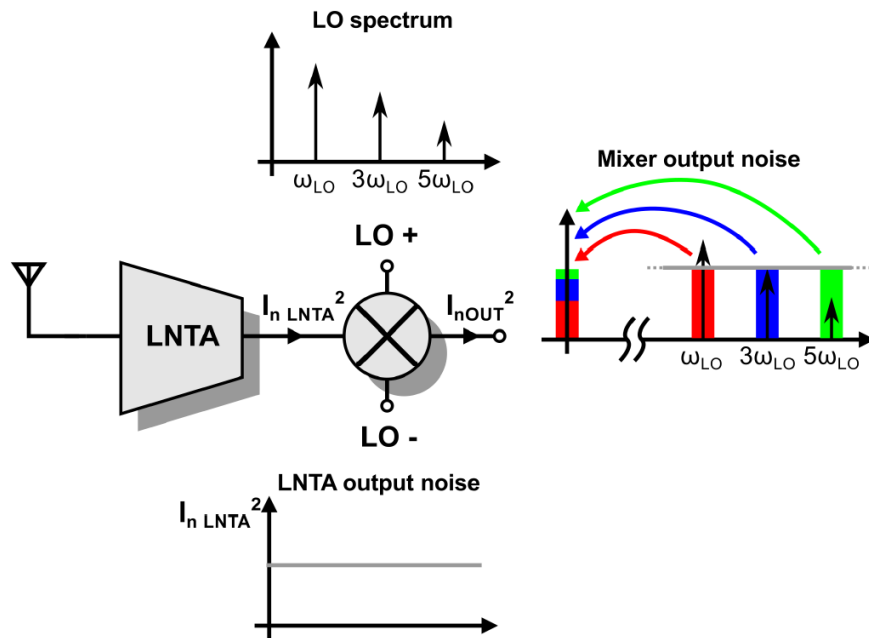
Figure 1-8: Noise folding

1.3 LTE Standard and Challenges

1.3.1 Introduction

Long Term Evolution (LTE) represents the most recent standard for wireless communication. Proposed for the first time in 2004, when its targets were defined, the standard was finalized in 2008 by 3GPP (Third Generation Partnership Project) [1]. 3GPP is a union of different telecommunications standard development organizations, called "Organizational Partners", working in cooperation to define the specifications of mobile systems [2]. All the new features that are introduced by the group over a certain period of time are "frozen" and collected in new versions of the standard called "Release".

LTE was formally included for the first time in Release 8. The introduction of several enhancements has lead the evolution of this standard through some new Releases until the number 12. LTE represents an evolution from previous wireless standards, like GSM and UMTS, which are classified as 2G and 3G systems respectively (2nd and 3rd Generation systems), and is usually referred to as a 4G system, even if formally such a network generation starts with Release 10 and the introduction of LTE-Advanced.

When it was introduced, LTE proposal was mainly to guarantee the competitiveness of the already existing 3G mobile networks for the future, by increasing the achievable data rates and the spectral efficiency, while reducing latency with respect to the previous Releases. The main features of the LTE standard are presented in this chapter, with particular focus on the requirements defined by 3GPP to achieve the desired performance and on their impact on the design of the receiver. In a second part of the chapter particular emphasis will be put on how such specifications become more

stringent when they are applied to the design of a so-called SAW-less receiver. 3GPP sets the specifications for both the Base Station (BS) and the User Equipment (UE), but from now on we will be considering only the latter.

1.3.2   Operation Band and Channels

LTE standard employs a number of frequency bands, covering a wide frequency range, in order to be exploitable all around the world. The list of available frequency bands is provided by 3GPP and its most updated version (included in Release 12) is reported in the Table A.1 of Appendix I [3]. As can be seen from the table both duplexing modes are supported: some frequency bands employ Frequency Division Duplexing (FDD), while others are based on Time Division Duplexing (TDD). We will be majorly interested in FDD.

The bandwidth of the channel is flexible and can assume values of 1.4, 3, 5, 10, 15 and 20 MHz. Not all the possible channel bandwidths are supported by every LTE band, for example wider channel bandwidths are typically compatible with bands endowed with a larger available spectrum and conversely smaller bands support narrower channels.

LTE in Downlink employs the Orthogonal Frequency Division Multiplexing (OFDM). It is a technique consisting of subdivision of the bit stream that has to be transmitted into a certain number N of sub-streams, each characterized by a reduced bit-rate, and impressing each of them on a different carrier frequency, called sub-carrier. This choice is motivated by the need to overcome the problem of multi-path fading, resulting from the reflections the electromagnetic signal experiences during its transmission from the Base Station to the mobile device. Such reflections cause the signal to be transmitted from TX to RX through different paths, with the appearance at the receiver antenna of different time-shifted versions of the same signal, seriously degrading its quality because of Inter Symbol Interference (ISI). Since this effect becomes important as the data rate of the transmitted signal increases, OFDM represents a possible solution, since the total occupied spectrum and data rate are unchanged with respect to the single-carrier solution, but each sub stream, being characterized by a lower bit-rate is less sensitive to multi-path effects [4].

In the specific case of LTE, the signal, instead of being spread over the entire channel bandwidth, is transmitted over a number of 15-kHz-wide sub-carriers, which are allocated to users in units of 12 each, called Resource Blocks (RB), characterized by 180 kHz bandwidth. Each LTE channel has a maximum number of RB that can be allocated inside it, defining the so called transmission bandwidth configuration (Figure 1.9). Such limit is reported for each channel in Table 1.1. From the Table it can be observed that the transmission bandwidth configuration measures only 90% of the channel bandwidth for all channel bandwidths, with exception of 1.4 MHz, where it is smaller. For example, in 5 MHz LTE a transmission bandwidth of 4.5 MHz is effectively occupied by the channel. This is motivated by the necessity of guaranteeing a certain margin at the edge of the channel in order to account for the finite transition band of the filters that are implemented to perform channel selection.
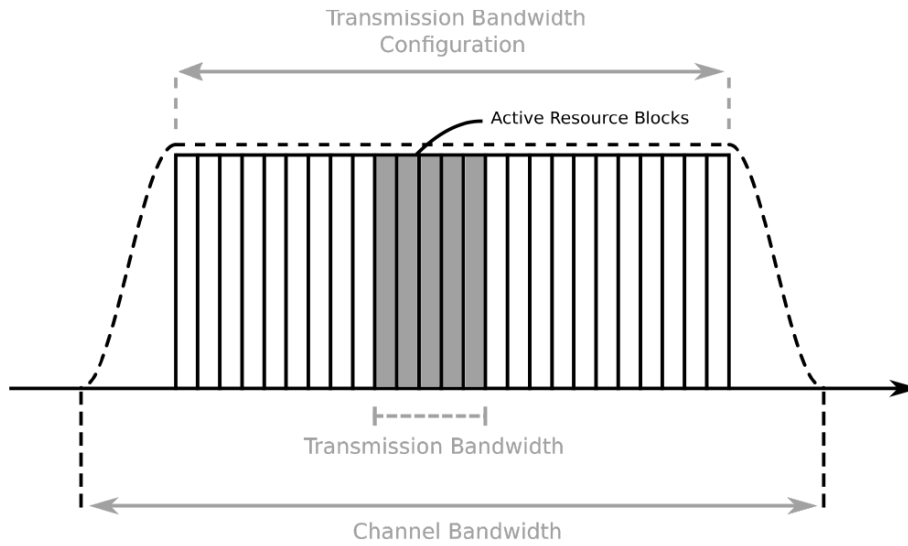
Figure 1-9: LTE channel bandwidth sub-division

Table 1-1: Maximum number of RB per channel

Channel Bandwidth (MHz)	1.4	3	5	10	15	20
Number of Resource Blocks	6	15	25	50	75	100

1.3.3 Sensitivity

One of the most important parameters to evaluate the performance of a receiver is its sensitivity. Sensitivity measures the capability of the receiver of detecting a small signal, with sufficient quality, in the presence of noise. It is formally defined as the minimum power of the input signal that can be detected by the receiver while achieving a given SNR at its output. Its value can be expressed (in dBm) by the following equation [4]:

$$P_{SENS} = 10Log(K_B T_0 B) + NF + SNR_{OUT} \quad (1.3)$$

In the equation KB represents the Boltzmann constant, having value $1.38 \times 10^{-23} JK^{-1}$, T_0 is the absolute temperature expressed in Kelvin, B stands for the channel bandwidth, NF is the Noise Figure in dB of the receiver and SNR_{OUT} is the minimum output signal-to-noise-ratio (again in dB) that has to be achieved at the output node of the receiver. The sum of the first two terms in the right side of the equation is usually referred to as "noise floor", and it represents the total integrated input referred noise of the receiver.

SNR_{OUT} is usually dependent on the kind of modulation employed for transmitting data, and by the minimum BER Bit-Error-Rate that must be guaranteed at the output of the receiving chain. For

example, 3GPP specifies for the sensitivity tests the employment of Quadrature-Phase-Shift-Keying (QPSK) Modulation, which, to guarantee a BER smaller than 10^{-4} needs a SNR of at least 8 dB [5], which goes down quickly if some redundancy is introduced coding the transmitted bits (a typical value assumed for LTE is SNR = -1 dB [6]).

A Reference Sensitivity level is specified by the standard for each channel width in each LTE band. Some examples are reported in Table A.2 of Appendix I. Once the Reference Sensitivity level of the desired channel is known, it is possible to compute the maximum tolerable noise that can be introduced by the receiver to comply with the requirements of the standard. For example, considering a channel bandwidth of 20 MHz for the LTE band 10, a -94 dBm Reference Sensitivity level is specified: starting from this requirement and from equation (1.3) it is possible to find out that the maximum tolerable NF for the receiver to achieve -1 dB of SNR at the output of the RX chain is around 8 dB (Figure 1.10).
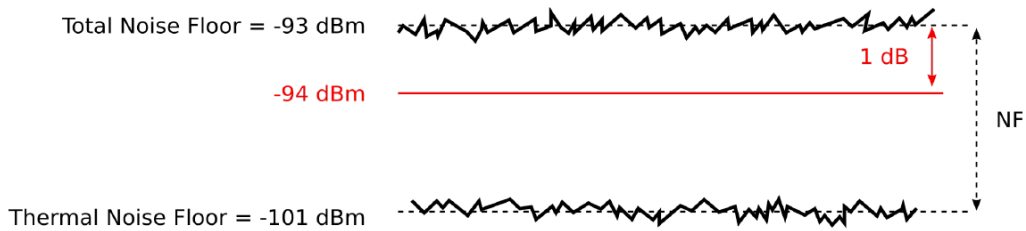
Figure 1-10: Graphical computation of the allowed Noise Figure

1.3.4   Adjacent Channel Selection and Blocking Specifications

An LTE-based wireless system must be able to operate in the correct manner even in the presence of an interferer placed at a specific frequency offset with respect to the desired channel. 3GPP provides a profile of interference the receiver must be able to deal with during its operation. Different tests are defined; the main ones are reported here.

1.3.4.1   Adjacent Channel Selectivity

Adjacent Channel Selectivity (ACS) measures the capability of the wireless system of receiving a desired signal in presence of an interferer located in the adjacent channel. It is verified by means of two tests. In the first one the mean power of the desired signal is set to 14 dB above the reference sensitivity level. The interferer, a LTE modulated signal, must be put in the adjacent channel, and must have a specified power and bandwidth, depending on the width of the wanted channel under test. For example, in the case of a 20 MHz channel the interferer power is set to 39.5 dB above the Reference Sensitivity level and its bandwidth is specified to be 5 MHz (Figure 1.11). The second test which has to be performed sets the interferer signal power to a higher level, -25 dBm, and the mean power of the desired signal to a channel-dependent value that in the example of a 20 MHz channel is -50.5 dBm.
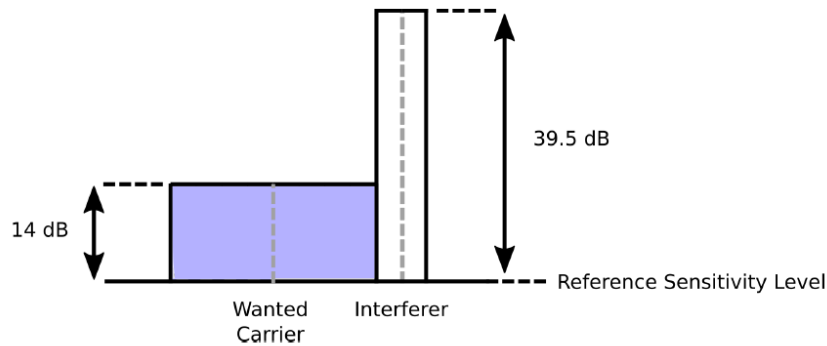
Figure 1-11: ACS test

1.3.4.2 Narrow Band Blocking

Narrow Band (NB) blocking is a different test that is required in regions where other telecommunication standards, like GSM, are in service [1]. In order to minimize the guard bands, i.e. unused portions of the spectrum introduced to prevent interference, which are responsible for system capacity reduction, it is necessary that the system is able to tolerate blockers at a small frequency offset from the desired channel. Unlike ACS, involving a LTE signal as interferer, NB blocking employs a Continuous Wave (CW) signal -55 dBm strong, shifted from the desired channel by an offset depending on the channel width. The signal power changes according to the channel under test. For example, in the 20 MHz case the interferer offset is set to 10.2075 MHz and the signal is 16 dB above the reference sensitivity level.

1.3.4.3 In-Band Blocking

A test very similar to the one performed for ACS is applied when measuring in band blocking tolerance of the system, evaluating the capability of the system to properly operate even in presence of an interferer falling in the same band as the desired signal. At a certain frequency offset from the desired channel it is applied a LTE interferer, having bandwidth and power level specified by the Release. As an example in Figure 1.12 it is reported the in-band blocking profile specified in [3] for a 20 MHz channel.

1.3.4.4 Out-of-Band Blocking

A different blocking profile is specified by 3GPP for out-of-band interference. The Release states that the test must be performed with an out of band CW interferer, whose amplitude is defined according to the frequency offset, like in the example reported in Figure 1.12, still referred to a 20 MHz channel width.

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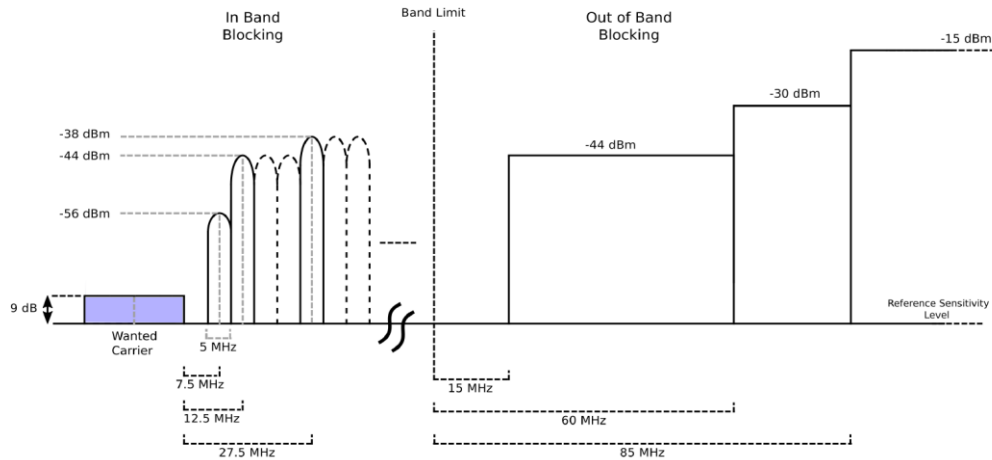
Figure 1-12: In-band and out-of-band blocking-profile

1.3.5   Intermodulation:

As will be clear in the following, when two signals at different frequency are sent at the input of a non-linear system, then additional tones are produced at the output, called intermodulation products. Since these products are likely to fall inside the signal band, this phenomenon can affect the proper functionality of mobile systems. The operation of a wireless receiver suitable for LTE standard must then be checked even in presence of two intermodulation signals, together with the desired one. According to the standard requirements [3] interference test must be performed with two interferers having amplitude corresponding to -46 dBm, with the one closer to the desired channel being a CW signal, while the other one a modulated signal, with a certain bandwidth defined according to the width of the wanted channel. The modulated interferer is put at a frequency offset from the desired channel which is two times the frequency offset of the CW interferer, in such a way that intermodulation product falls on the desired channel itself.

As an example, it is interesting to extract the requirement that is needed for a wireless receiver to comply with the intermodulation test. Assuming the channel width to be 20 MHz as in previous examples, the standard specifies that the signal power must be set to a level 9 dB above the reference sensitivity level [3]. This value sets an upper limit for the tolerable power of the intermodulation product (IM): intermodulation falling in the signal band can be considered as noise, and it is not allowed to raise the noise floor more than 9 dB. It means that IM power (referred to the input) can be at most around 8 dB above the noise floor computed for the sensitivity test.

Considering the example of band 10, the maximum allowed IM power results to be -85 dBm. Applying the formulas for Input Referred Intermodulation Product (IIP3) [4], the required IIP3 (in dBm) for the receiver turns out to be:

$$IIP3 = P_{INT} + \frac{P_{INT} - (N_{floor} + 8dB)}{2} = -46dBm + \frac{-46dBm - (-85dBm)}{2} = -26.5dBm \quad (1.4)$$

where P_{INT} represents the power associated with the interfering signal, while N_{Floor} is the noise floor computed for the sensitivity test. All quantities are expressed here in dBm. The obtained limit for IIP3 is not a dramatically critical parameter for typical receivers. In the following other problems will be highlighted requiring more stringent linearity performance for the receiver.

1.3.5.1   Poor TX-RX Isolation:

For the aim of this report particular interest must be put upon the problems arising from the poor isolation that is present between the Transmitter (TX) and the Receiver (RX) end of the same transceiver. The problem of poor isolation proves particularly challenging in modern FDD systems and in diversity receivers. As previously stated, in FDD systems the transmitted and received signals occupy separated bands. One external filter, referred to as duplexer, connects the antenna to the TX or to the RX end in a frequency-selective manner and performs isolation between TX and RX end of the transceiver. The continuous ask for reduced form-factor and re-configurability, characterizing recent wireless systems, results into a lowered quality of duplexers and then a reduced isolation between the TX and the RX end, producing critical undesired effect which compromise the system performance. These issues are much more stressed if the array of narrowband duplexers is replaced by a single broadband on-chip structure [7].
In addition, modern transceiver modules include multiple antennas, as previously put on evidence when discussing MIMO technology and diversity. Because of the reduced available area for transceivers the several antennas that are present in the system are spatially close to each other, being subject to poor isolation and reciprocal coupling. This point becomes particularly critical in the systems endowed with diversity path, since it produces the coupling of part of the TX signal (TX leakage) to the diversity RX antenna.
In traditional transceivers the leaked signal was filtered out by the High-Q external filter, then relaxing the receiver performance. In SAW-less implementations such filtering action is removed and the presence of a strong TX signal at the diversity or main RX input due to reduced TX/RX isolation imposes severe requirements on the receiver, especially in terms of third-order intermodulation and TX noise leakage falling in the RX band.

1.3.5.2   Third-order intermodulation

3GPP specifies that the maximum output power level that an LTE User Equipment (UE) is allowed to transmit is 23 dBm [3]. Supposing such a power level is transmitted by the main TX, then a strong OOB signal is likely to appear at the main or diversity RX and must be handled by the receiving chain. From now on we will focus on the problems associated with diversity, but analogous arguments apply to the case of poorly isolated TX/RX. Because of proximity an isolation value as low as -15 dB can be assumed [8] between the main and the diversity antenna, bringing a TX signal power of around 8 dBm at the diversity antenna. The SAW-filter included in typical implementations of diversity receiver is able to further attenuate such a signal by values in the order of 45 dB [8], lowering the power level at the input of the LNA to a level close to -37 dBm.
When the SAW-filter is removed because of reasons explained in previous sections, the receiver is asked to handle the strong 8-dBm OOB modulated TX signal.

According to 3GPP specifications, as also schematically represented in the left part of Figure 1.13, together with the modulated TX leakage signal also an OOB CW interferer as strong as -15 dBm can arrive at the receiver, and must be tolerated while guaranteeing signal integrity. The receiver in particular must be designed in such a way as to achieve good linearity performance, so as not to be desensitized by third-order interaction between the CW blocker and TX leakage.
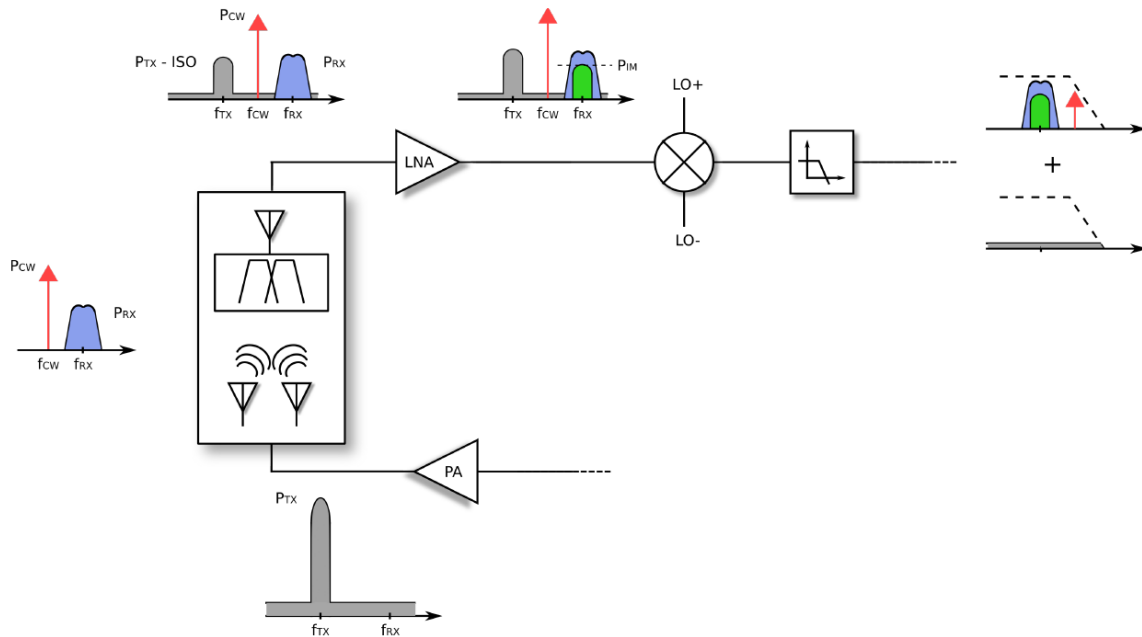
Figure 1-13: Schematic representation of the effects of 3rd order IM and TX-noise leakage in poorly isolated TX/RX systems

Such third order interaction can be analyzed by considering the same expression previously employed to describe the non-linear response of the receiver as a power series expansion (1.1). Considering again the input signal as superposition of two tones, the first one representing in a simple way the TX signal centered at ω_1, while the second the CW blocker at angular frequency ω_2, some output spurious terms appear at frequency $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$, because of third-order interaction between the two tones. These additional terms have amplitudes as reported in (1.5):

$$y(t) = a_1 A_1 \cos(\omega_1 t) + a_2 A_2 \cos(\omega_2 t) + ... + ...$$
$$+ ... + (\frac{3}{4} a_3 A_1^2 A_2) \cos(2\omega_1 - \omega_2)t + (\frac{3}{4} a_3 A_2^2 A_1) \cos(2\omega_2 - \omega_1)t + ...$$

$$(1.5)$$

If ω_1 and ω_2 are sufficiently close to each other, the third-order Intermodulation (IM) products fall very close to the linear terms at ω_1 and ω_2. In particular, the term at $2\omega_2 - \omega_1$ is very likely (in Band I for example) to locate inside the RX band, as schematically represented in Figure 1.14, possibly degrading the SNR at the receiver.
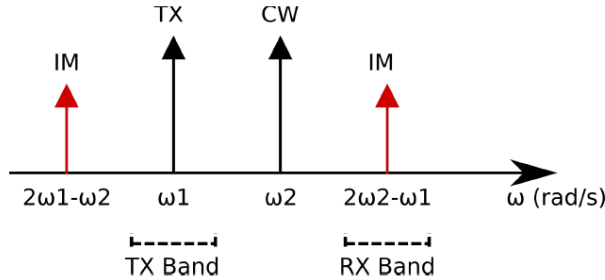
Figure 1-14: IM product falling in the RX Band

In particular, the IM product power is related to the TX power received at the diversity antenna, the CW interferer power and the receiver IIP3 by the relation [9]:

$$P_{IM} = 2P_{CW} + (P_{TX} - ISO) - 2IIP3 \quad (1.6)$$

where all power quantities are expressed in dBm and ISO stands for the total isolation between the TX and the input of the LNA expressed in dB. Starting from the reported equation, it is then possible to compute the maximum IM product that can be tolerated while satisfying the requirements imposed by 3GPP. When testing the receiver in presence of an OOB CW blocker, LTE standard specifies that the signal level must be set to 9 dB above the Reference Sensitivity level for the band of interest, corresponding to an equal maximum acceptable degradation of the SNR. Since IM power directly adds (in linear) to the noise introduced by the receiver, the maximum tolerable IM level turns out to be around 8.4 dB above the noise floor previously computed for the standard sensitivity test. Starting from this reference level it is possible to extract the formula for minimum necessary IIP3 which has to be guaranteed for the receiver to comply with the required sensitivity, by substituting in (1.6) the maximum tolerable IM power:

$$IIP3_{MIN,HD} = \frac{2P_{CW} + (P_{TX} - ISO) - (P_{SENS} + 8.4dB - SNR_{OUT})}{2} \quad (1.7)$$

In the following graph the achievable sensitivity as a function of the receiver IIP3 is reported for different levels of isolation between the TX and the RX. The transmitted power has been supposed to be 23 dBm, the CW interferer has been chosen -15 dBm strong as required by the standard, the receiver NF has been supposed to be 5 dB, while the required SNROUT has been fixed to -1 dB as usual. In the computation of the noise floor a 20 MHz channel bandwidth has been supposed.

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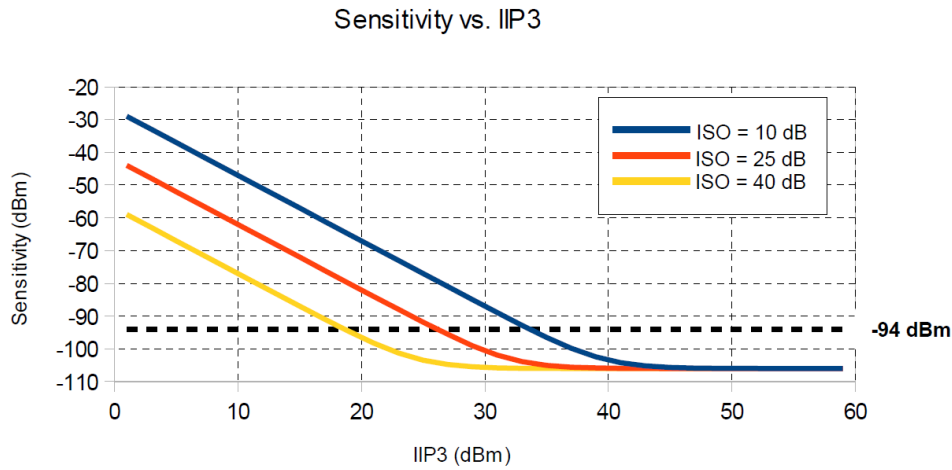
Figure 1-15: Achievable sensitivity as a function of the receiver IIP3 in HD case

From the reported plot it can be observed that in order to achieve a sensitivity level of -94 dBm (extracted from Band I requirements), a 19 dBm, 26 dBm and 34 dBm IIP3 is required for 40 dB, 25 dB and 10 dB of isolation between TX and RX, respectively. In the just presented situation the TX and RX bands were supposed to be widely separated in frequency, and the CW blocker was placed between such bands, as illustrated in Figure 1.16. This scenario is usually referred to as Half Duplex (HD).
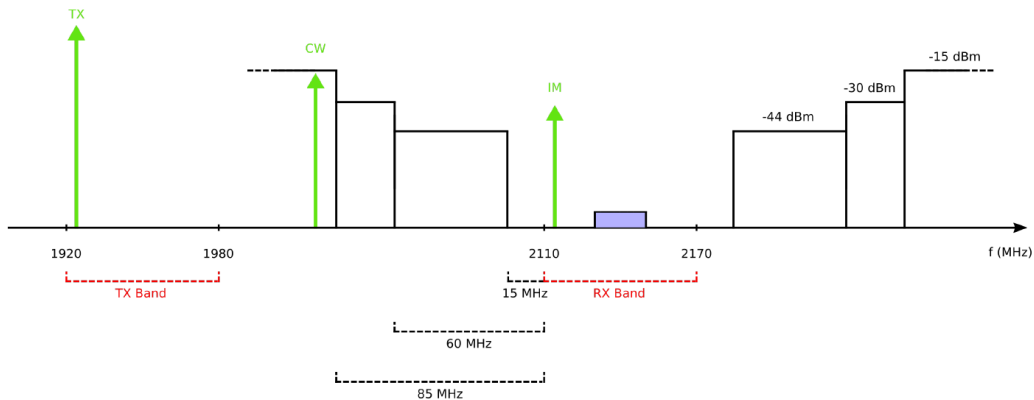
Figure 1-16: TX, CW and IM signals relative position in HD scenario

When the TX and RX bands are closer to each other in frequency, the blocking test must be performed by inverting the relative position of the CW signal and of the TX, with respect to HD (Figure 1.17).
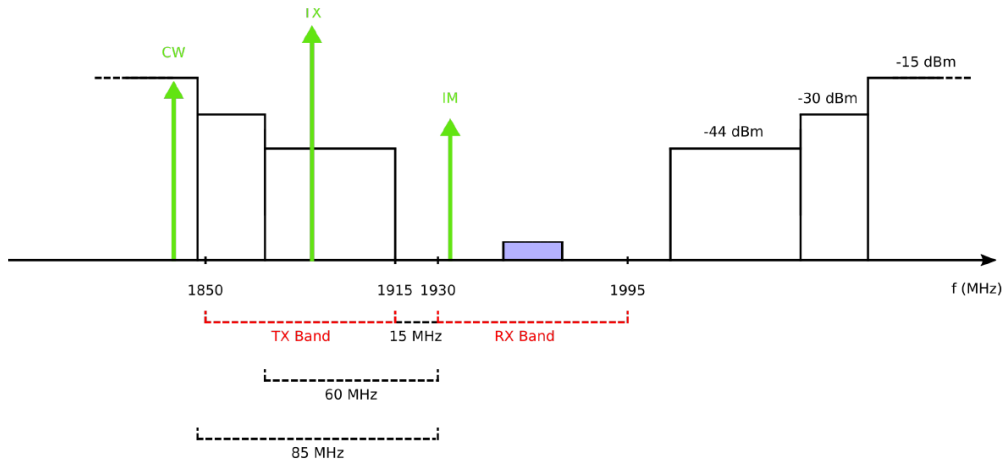
Figure 1-17: TX, CW and IM signals relative position in FD scenario

In this case it is usual to talk about Full Duplex (FD). In FD the formula for the computation of IIP3 becomes:

$$IIP3_{MIN,FD} = \frac{P_{CW} + 2(P_{TX} - ISO) - (P_{SENS} + 8.4dB - SNR_{OUT})}{2} \quad (1.8)$$

From the expression it can be immediately understood how the FD situation proves more challenging in terms of linearity requirements. Unlike in (9), in equation (10) it is the TX power to be multiplied by a factor two and not CW. The specified TX power is much higher than the CW blocker (23 dBm vs. -15 dBm), meaning that to achieve the same sensitivity as in the HD scenario a higher IIP3 is required. The variation of achieved sensitivity as a function of IIP3 for FD case is reported in Figure 1.18.
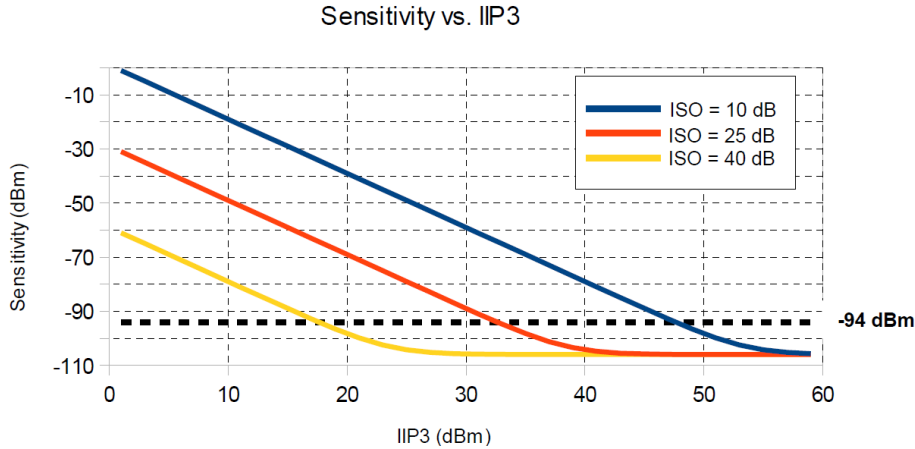
Figure 1-18: Achievable sensitivity as a function of the receiver IIP3 in FD case

In order to satisfy the reference sensitivity level requirement of -94 dBm it is necessary in this case to achieve 48 dBm, 33 dBm and 18 dBm of receiver IIP3 with a total TX-RX isolation of 10 dB, 25 dB and 40 dB, respectively.

From the reported values it can be inferred how stringent the required linearity performance for a SAW-less diversity receiver is. In particular, it is interesting to observe how the most challenging linearity requirement is set here by compliance with strong out-of-band blockers, rather than the intermodulation test specified by 3GPP.

Since the isolation offered by the antennas is typically poor (-15 dB of antenna isolation was previously assumed), together with the employment of a highly blocker-tolerant receiver, some additional measure to isolate TX and RX must be taken. Such solution is usually represented by the so called canceler, consisting of a circuit which basically draws the transmitted signal from the TX Power Amplifier (PA), adjusts it in magnitude and phase by means of some algorithm and subtracts it from the received signal, so as to cancel, at least in principle, the TX leakage.

Both passive [10,11] and active [9,12] solutions were developed in literature for the canceler, but they won't be further developed in this report, since major attention will be devoted to the improvement of linearity performance of the receiver.

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2 Chapter 2

State-of-the-art on Highly Linear LNTA

Numerous techniques have been proposed in the literature to facilitate the receivers to deal with interference and large blockers. This chapter reviews some of the prior art techniques to improve the linearity of the frond-end. Generally speaking, these techniques can be classified into four categories:

A: Cancelling third order nonlinearity of transistor

B: Noise and distortion cancelation

C: Feedback

D: Interference cancellation

2.1 Optimum Biasing

Distortion of MOS transistor is mostly generated by non-linear trans-conductance (g_m) and also output conductance (g_{ds}). In the literature, concentration is mostly allocated on the non-linear trans-conductance and introducing possible methods to improve the linearity behavior of frond-end by means of cancelling third order nonlinearity of transistor. A FET can be linearized by biasing at a gate-source voltage (V_{GS}) at which the 3rd order derivative of its DC transfer characteristic is zero [14]. High 3rd order input inter modulation distortion products (IIP3) can be achieved only in the neighborhood of the bias point usually called 'soft spot'; e.g. linearity improves for signal power under -25dBm. In addition, this linearization method is very sensitive to process, voltage and temperature (P.V.T.) variations. The sweet spot of $g_3 = 0$ can be seen in the Fig. 2.1 [14] at V_{GS} = 0.66V.
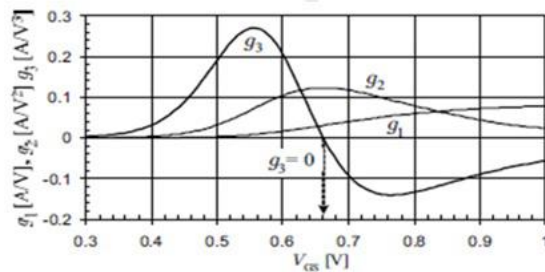
Figure 2-1: Optimum gate biasing sensitive to P.V.T. variations [14]

2.2 Derivative superposition method:

Research has been done to cancel 2nd order derivative of g_m for high linearity. One way of canceling is using two transistors working different region. Fig. 2.2 shows DC current, trans-conductance and its 1st order and 2nd order derivative of single transistor over V_{GS} with V_{DS} fixed.
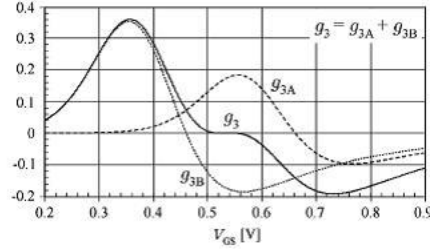
Figure 2-2: DS method of overlapping the 2nd order derivatives of gm in strong and weak
inversion transistors [15]

As we can see from the Fig. 2.2, 2nd order derivative of g_m in weak inversion region and that in strong inversion region have different polarity. Exploiting this characteristic, low distortion region could be achieved. Transistor level implementation is shown in Fig.2.3.
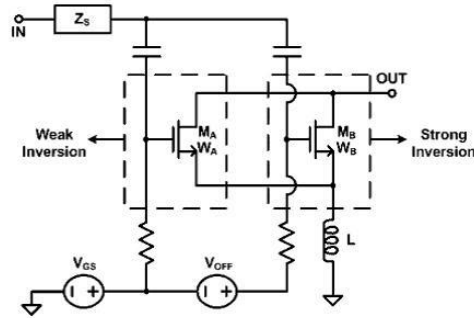
Figure 2-3: DS method implementation [15]

Supposing main transistor, M_B, is working in the strong inversion. Its 2nd order derivative of g_m is negative. The additional transistor, M_A, working in the weak inversion could minimize the 2nd order derivative of g_m. Since usually the positive peak magnitude of 2nd order derivative of g_m is larger than the negative peak magnitude, the size of the additional transistor is smaller than that of the main transistor. Thus, by combining g_3 of strong inversion and weak inversion transistors with opposite polarities, the effective $g_3 = g_{3A} + g_{3B}$ can be made zero. This conventional DS method has some drawbacks along with the benefits. If the transistor working region is not properly set, 1st order derivative of gm i.e, g_m' could be accumulated which consequently could increase the 2nd order distortion and affect the SNDR at the LNA output. Biasing could also be a potential problem. Constant voltage biasing for transistors is sensitive to process and temperature variation while constant current biasing is proved to be stronger against process and temperature variation.

2.3   Linearization by multi-gated transistors (MGTR):

To reduce the 3rd order Input referred Inter-modulation product (IIP3) sensitivity to the bias, an improved derivative superposition (DS) method was proposed in [16]. It employs multiple gated parallel (auxiliary) FETs of different widths and gate biases to achieve a composite DC transfer

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characteristic with an extended range in which the third-order derivative is close to zero. Schematic implementation of the MGTR is shown in Fig. 2.4. Simulated 3rd order distortion coefficient, g3 of the MGTR transistor is shown in Fig. 2.5. The effective g_3 is zero for wide range of input signal, making it robust to P.V.T. variations.
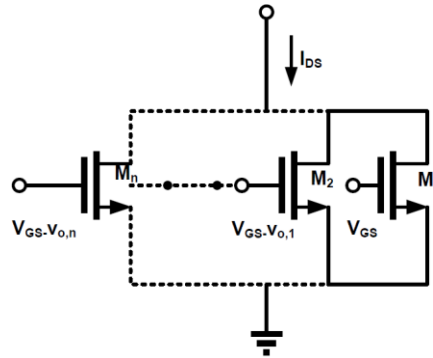
Figure 2-4: Schematic of MGTR with n transistors in parallel [17]
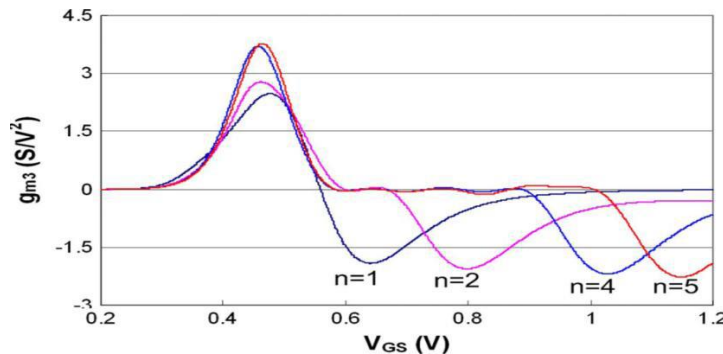
Figure 2-5: Simulated g3 of MGTR with different number of transistors [17]

These auxiliary transistors biased in sub-threshold region add higher order harmonic components because they turn on and off for large voltage swings. It is, however, difficult to achieve high linearity figures for all technology corners and temperature variations. With the increase in number of transistors the input range increases at the expensive of higher input capacitor. It should be remembering that this parasitic capacitor Cgs is nonlinear too. Beyond certain number of auxiliary transistors, the nonlinearity of Cgs can dominate the nonlinearity of g_m.

2.4   Noise and distortion cancelation:

Blaakmeer et al. proposed noise canceling common gate (CG) common source (CS) balun-LNA in [18] as shown in Fig. 2.6. Common-source (CS) stage acts as an error amplifier (EA) stage to cancel the noise/distortion (errors) of the input common-gate (CG) stage. This topology employed unequal trans-conductance gains (gm) in the CG and CS branches as well as unequal output

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impedances to minimize the noise contribution of the CS stage. The unbalanced devices are sensitive to process variations and therefore degrade the differential operation of the entire receiver. Also, the NF degrades if equal gm's are employed in both the branches of this topology under the same input matching constraints. Noise and distortion performance of this LNA is limited by the CS stage. Work reported in [19] improved the linearity of this amplifier topology by linearizing the CS stage with a linearization scheme proposed in [20]. It achieves good linearity but still suffers from high NF due to the use of equal load impedances for CG and CS stages.
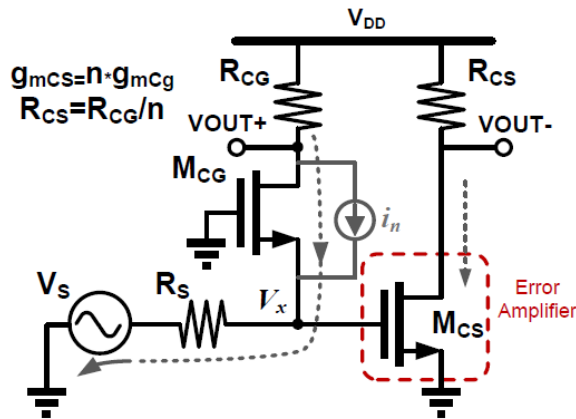
Figure 2-6: Noise and distortion canceling LNA [18]

Another implementation of noise and distortion cancelation is carried out in [19]. This implementation is fairly broadband linear fully balanced LNTA with P1dB>0dBm. The LNTA utilizes complimentary characteristic of NMOS and PMOS transistors to enhance the linearity. Like the original noise and distortion cancelation topology [5], noise and distortion of the CG amplifier is appeared as common mode signals at the output and cancelled in differential output. Additionally, input stage is implemented in current reuse Mn and Mp combination to reduce the power consumption, improving linearity, eliminating biasing inductors or any noise contribution from additional biasing circuity.

In the present of the large signal, P1dB is enhanced at the reduced bias current by operating the input push-pull CG stage like class AB amplifier. Besides, signal compression in the error amplifier stage is compensated by the signal expansion in the input CG stage results in improving the linearity. As can be clearly seen from the schematic, LNTA requires large supply voltage of 2.2V due to the stacking of NMPS, PMOS and also used series resistors at the output. To have IIP3 of greater than 10dBm, more than 35mW has to be consumed by the LNTA and NF can be increased to above 6dB at the 3GHz.
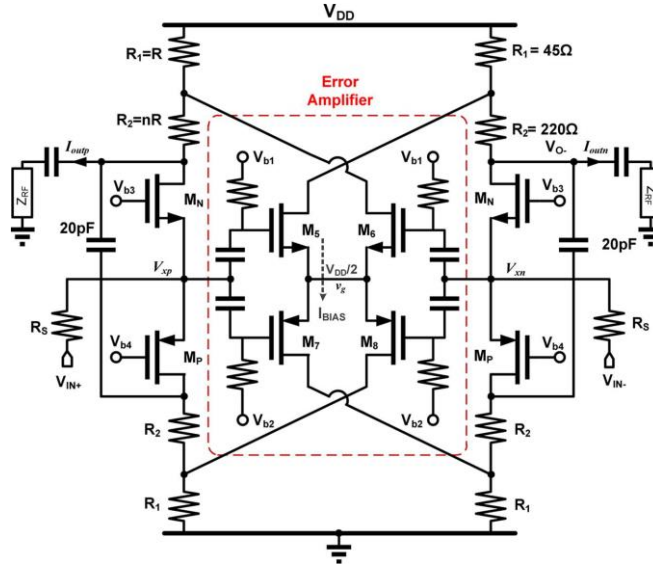
Figure 2-7: Complete schematic of differential LNTA [19].

One of the interesting ways of implementing programmable highly linear receiver for multi standard application is to take advantage of the noise and distortion cancellation concept. Apart from utilizing complimentary NMOS and PMOS characteristic of transistor, the common-source (CS) and common-gate (CG) LNTAs can be split into several cells whose bias point is individually programmed in class AB or C yielding a highly linear hybrid class-AB-C LNTA [21]. As shown in Fig. 2.8, once the input voltage of NMOS CS Gm cell goes more than $V_{gs}-V_{th}$ below its gate bias, NMOS turns off leading to the hard clipping and strong non-linear LNTA transfer curve. Using a greater $V_{gs}-V_{th}$ enhances the input swing range, however at the cost of reduced power efficacy. Overcoming the problem, PMOS Gm cell is biased in Class-C such that turning on and pushing out current when the NMOS is cut off. Therefore, combined transfer curve represents an almost twice as large linear amplification region and the input clipping nonlinearity is removed leading to a significantly higher tolerance to the input blocking signals. When it biased in Class-C mode, the CS Gm cell is not fully off and has small gm. Since the 3rd order distortion from the Class-C has opposite polarity than that of class-AB cell's, results in partially cancellation of the 3rd order nonlinearity like DS method. Depending on the requirement, CS Gm cell can be programed in different operating mode as shown in Fig.2.8. This approach requires two off chip chokes to provide biasing of the input stage which will be costly and also complicated biasing circuity. Although in high linearity mode, the maximum IIP3 of 21dBm is achieved, it requires to draw 33mA from supply voltage of 2.5V.
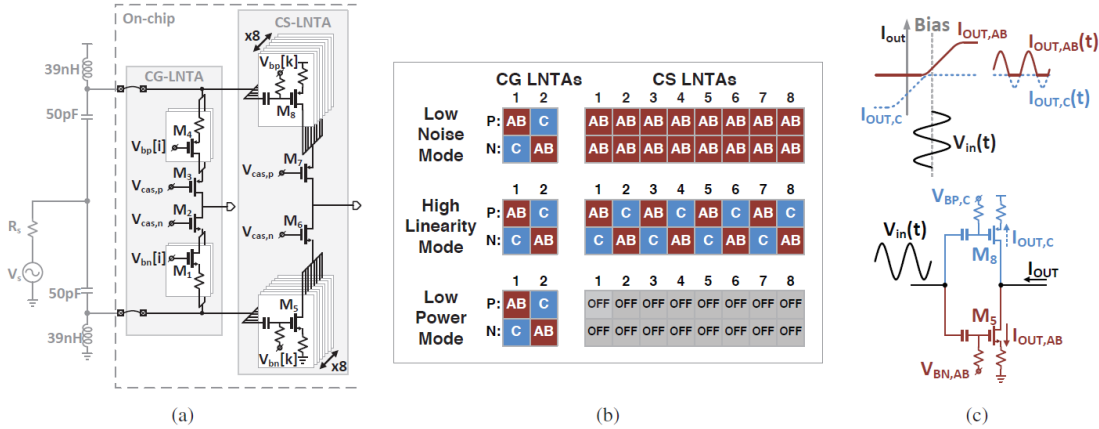
Figure 2-8: (a) Schematic of the CS-CG LNTAs (bias not shown); (b) LNTA bias configurations for the three operation modes tested; (c) the operation of the high linearity mode with an NMOS class-AB Gm cell and a PMOS class-C Gm cell [21].

2.5   Feedback:

Generally speaking, employing negative feedback in the amplifier improves the linearity by means of reducing distortion. One of the popular and efficient feedback loop in CG stage is to employ trans-conductance boosting which widely known as cross-coupled topology. It facilitates effectively gm enhancement by almost a factor of two and halves the thermal drain noise contribution at noise factor without consuming extra DC power. It is also well worth mentioning the other privilege of cross coupled configuration is to cancel the second order harmonic which drastically reject the common mode signal, thus it can reduce the effect of the second-order harmonic on the IIP3. Thanks to cancelling the second order harmonic, IIP3 can be improved by increasing loop gain, however, enhancing loop gain is limited by the imposed power matching constrain in this configuration. To solve the limitation of having low loop gain at higher frequency, the second feedback loop, voltage-current feedback, is employed by cross-coupling between drain node and the source node using a capacitor [22]. The proposed amplifier demonstrates very good performance, for instance, NF<2dB and power consumption of less than 2.9mW. Despite IIP3 or more than 9dBm is achieved, it is still not enough to remove SAW filter in the prior of the receiver. It should be pointed out this method is not fully integrated and requires 4 big inductors to provide biasing of the input and output voltage, beside two balun to perform single-ended to differential and vis versa.
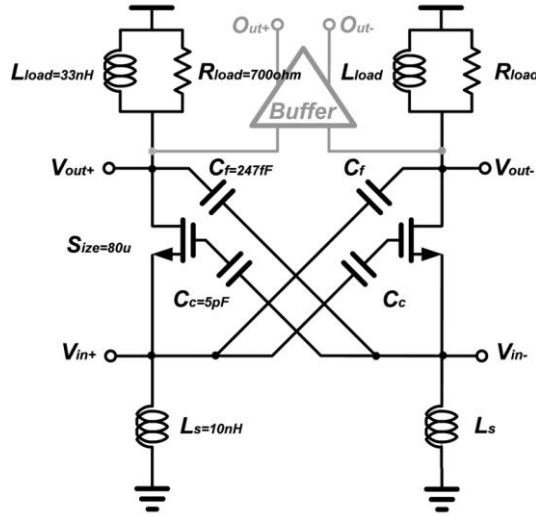
Figure 2-9: the proposed dual feedback cross-couple common gate (DCCG) amplifier [22]

2.6 Blocker Filtering Using Translational Impedance Mixing

Translational impedance mixing is an effective technique to improve the compression point of the receiver RF front-end, specifically LNA. it counts on the input impedance property of passive mixers [23]. Based on [24], it is shown in Figure 2.10 that a low-Q baseband impedance can be frequency-translated to RF utilizing a passive mixer and representing a high-Q bandpass filter response (HQBPF). This technique can improve the large-signal linearity performance (such as P1-dB or B1-dB) of the circuit, but it does not enrage the small-signal linearity performance (such as IIP3) significantly.
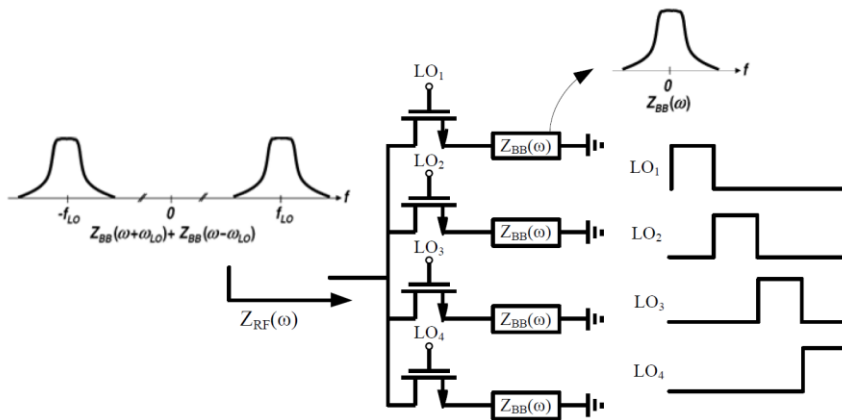
Figure 2-10: Translational impedance mixing property of a current-driven passive mixer [25].

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As shown in Figure 2.11, HQBPF is used at the input as well as the cascode node of a cascoded common-source (CS) amplifier. Due to large blockers, it can effectively prevent large voltage swings at these nodes. At the present of blocker, enabling HQBPFs results in a simulated 10 dB attenuation at the LNA input at 50 MHz frequency offset which is equivalent to the Q of approximately 150 for BPF [24]. At a presence of a 0-dBm blocker at ±80 MHz frequency offset, receiver gain is reduced by 0.8 dB and NF can be degraded to 10.8 dB [19]. 3.1 dB NF can be achieved by disabling the HQBPFs even though NF increases to roughly 8 dB when enabling the HQBPFs. [24] is the first reported "true SAW-less" quad-band 2.5G receivers in 65-nm CMOS technology due to the meeting the 3GPP requirements without a SAW filter.
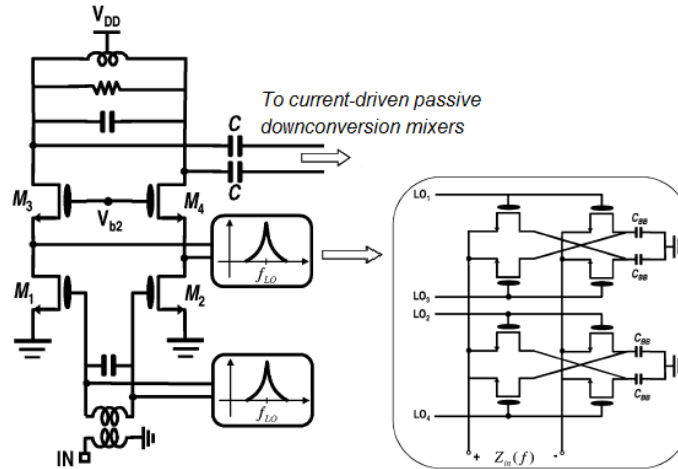
Figure 2-11: The LNA incorporating HQBPFs proposed and implemented by [24].

Highly selective LNTA capable of large signal handling for RF receiver is presented in [26]. A core block of the proposed LNTA is push-pull CG amplifier operating in Class-AB. The class-AB operation is beneficial since it relaxes the constraining universal trade-off between the power consumption and large dynamic range (or linearity) that exists for typical class-A amplifiers. The noise improvement of push-pull CG amplifier is performed using Z_L of the first stage to boost the effective trans-conductance. However, the successful large-signal operation of the push-pull CG depends on the Z_L which should be ideally zero to avoid any voltage swing at the drain node of the first stage. To circumvent this apparent trade-off between the noise and large-signal performance, ZL is proposed to be a high-Q band pass impedance to provide large in-band (IB) impedance (ZL,IB) for the desired signal and low out-of-band (OB) impedance (ZL,OB) for large input blockers. By using the impedance transformation property of a passive mixer, such an on-chip high-Q band pass filter (HQ-BPF) can be realized. The LNTA schematic is represented in Fig.2.12. The LNTA draws 7.5mA from 1.5V supply voltage. When HQ BPFs are enabled, the 3-dB RF bandwidth is equal to 40 MHz and the LNTA maintains 6 dB OB rejection for the frequencies between 1.5—2 GHz yielding to the out of band IIP3 of 20dBm. The measured NF is 6.5dB when the HQBPF is enabled. It is predicted according to the simulation NF is increased to above 8.5dB in the present of blocker. Additionally, one big off chip inductor is needed to provide the biasing of the input stage.
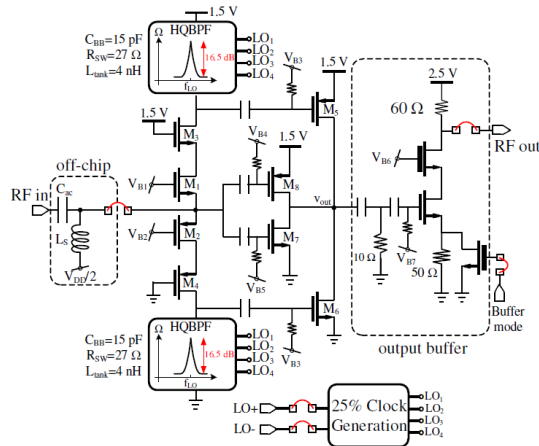
Figure 2-12: Simplified schematic of the implemented LNTA [26]

2.7 Active Feedforward Cancellation

An active feed-forward cancellation enabling out-of-band interference cancelation without using SAW filters was recently presented in [27]. Both the desired signal and the interference will be down converted using the down-conversion mixer in the auxiliary path (shown in Figure 2.13). To filter out the desired signal, a high pass filter is used and the unfiltered interference is up-converted and then subtracted from the output of the LNA. A narrowband bandpass (with large Q) response can be essentially created at the RF front-end. The LNA bandwidth is reduced from 220 MHz to 4.5 MHz with stop-band attenuation of 21 dB.

This technique can effectively improve the linearity requirement at the LNA output and subsequent stages, however the linearity requirement at the LNA input is not relaxed since the blocker can potentially cause the input devices to be driven into compression. Additionally, this topology increases the noise and power consumption and blocker filtering is heavily depended on the matching between the main and the auxiliary path.
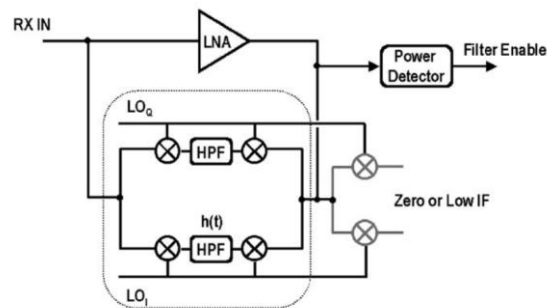
Figure 2-13: Active feed-forward cancellation topology proposed by [27].

Recent work on RF receiver has exploited N-path filters to address two critical issues, namely, blocker tolerance and high RF selectivity. To select the channel at RF, for instance GSM channel

with bandwidth of 200KHz, a very big capacitor at the input of LNA is required to perform this task. However, if an N-path notch filter is placed around the amplifier (three stages LNA), the resulting Miller multiplication of C_F manifests itself at the input outside the notch bandwidth, thereby providing selectivity [28]. The idea is very simple and elegant, but it opens up many issues including attenuating RF signal due to the parasitic capacitor placed on the feedback loop, saturating the latter stages of the LNA at higher power level which needs to be placed many loops around the LNA. Additionally, the various loops around the LNA raise stability concerns. The simplified schematic of the front-end is represented in Fig. 2.14. Having made a lot of effort to solve aforementioned issues, the performance is quite good from the noise and power consumption point of view. However, the linearity performance is still limited to 10dBm which is not sufficiently enough to remove the SAW filter. Furthermore, in the present of the 0dBm blocker with the offset frequency of 20MHz, NF raise to more than 5dB.
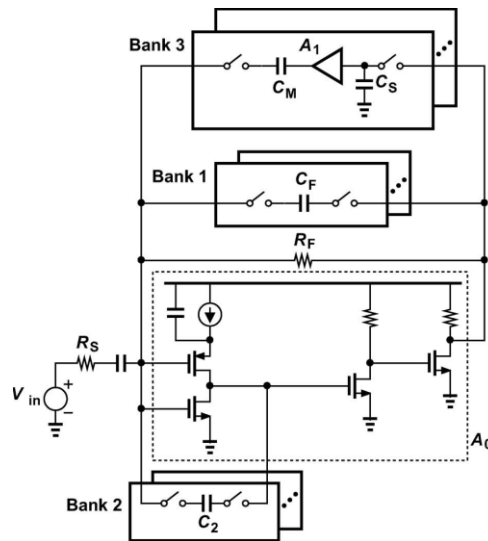
Figure 2-14: RX front-end with unilateral Miller path [28]

A channel-selecting, low-noise amplifier (CSLNA) is presented that meets the requirements for a SAWless diversity path receiver in frequency-division duplexing (FDD) cellular systems. A tunable CS-LNA with offset bandstop filtering was proposed in [29] and represented in Fig. 2.15. A g_{m2} and g_{m3} cancellation scheme improves the IB IIP3 while a 4-path filter feedback loop with shunt capacitors selects the LNA channel and provides TX leakage cancellation. The N-path filter is a series band-reject filter (BRF) that selects the pass band (channel) of the LNA and the location of the peak gain. A shunt capacitor in the N-path filter is added to form a π- network from the series and shunt capacitors. These shunt capacitors control the frequency at which OOB signal energy propagates through the filter. Thanks to utilizing programmable N-path filter to suppress TX blocker, a record of 36dBm IIP3 is achieved at lower frequency. On the other hand, IIP3 is not flat over RF frequency and degrades by 10dB at higher frequency passband. However, this approach is extremely power hungry and requires to consume almost 210mW. Moreover, NF can be raised to above 10dB at the present of 0dBm blocker with offset frequency of 200MHz.
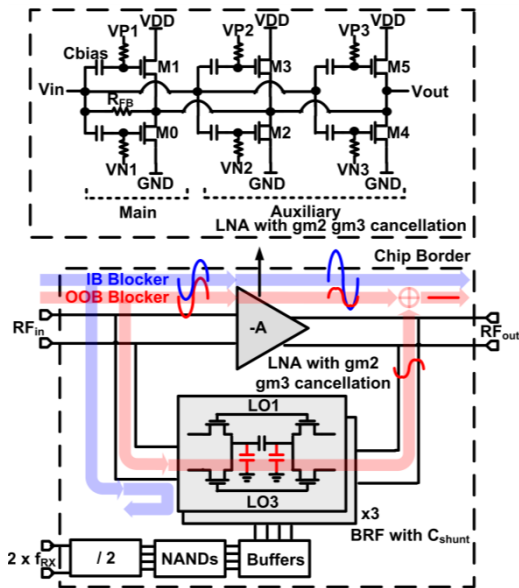
Figure 2-15: Schematic of the proposed CS-LNA [29].

3 Chapter 3

Design of Highly Linear LNTA for SAW-Less Diversity Receiver

In today's multi standard transceivers a dedicated radio for each band with external SAW filters is used. As MIMO and Carrier Aggregation (CA) are extended, both external passives and pin count increase. Using a SAW-based duplexer, transmitter leakage and blocker power are reduced by about 50 to 55 dB in FDD transceivers, drastically relaxing receiver IIP3. Diversity receivers (used in most high performance cellular systems) benefit from similar levels of SAW filtering. Hence, while removing external SAW filters and duplexers dramatically simplifies antenna interface and reduces cost, the integrated receiver (especially the LNTA) would face a daunting linearity challenge. Removing SAW filters, however, opens up an interesting possibility in that the power matching condition can, to a certain extent, be neglected. In this chapter, we propose a highly linear noise-matched current-mode common-gate LNTA for SAW-less FDD diversity receivers achieving similar antenna-referred IIP3 as SAW-based solutions and better noise at a much lower system cost. A series capacitor, together with the LNA input transformer, forms a broadband low-noise impedance boosting network that strongly suppresses the input transistors noise and distortion. The residual noise is limited by transformer losses while the IIP3 is ultimately limited by the cascode transistors nonlinearities. The impedance transformer is designed to minimize its noise for a 50Ω source, thereby minimizing also noise variations as a function of the antenna impedance variations.

3.1 Basic idea and comparing CG versus CS LNA:

Inductively degenerated Common source (CS) LNA is one of the popular and the efficient topologies to minimize the noise and maximize the gain, however it represents inherently narrowband response and suffers from fairly poor linearity. In fact, the dropped voltage across gate-source of transistor, V_{gs}, enhances by a factor of Q, (Q is the quality of the input passive network) leading to heavily soliciting the transistor, hence, degrading the IIP3 of the LNA.

A Common Gate (CG) amplifier, shown in Fig.3.1, is known for better operation in wide frequency band and high linearity, however it suffers from poor noise figure imposed by matching condition. In general, the noise factor of simple CG amplifier can be computed as follows

$$F = 1 + \frac{\gamma}{g_m R_S} \qquad (3\text{-}1)$$

Where ϒ is MOS excess noise factor, Rs and g_m are source resistance and MOS trans-conductance respectively.
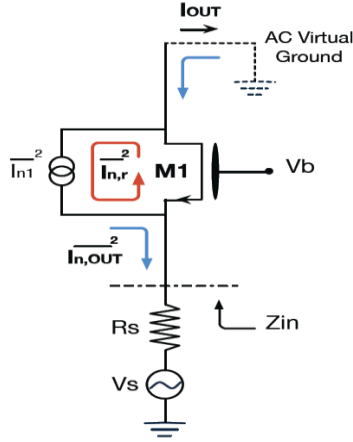
Figure 3-1: Common-gate topology with equivalent MOS noise current re-circulation

Linearity of CG is another metric which should be taken into the account especially when the bulky off-chip component like SAW filter is removed in prior of the receiver. In order to investigate this metric, Volterra series is applied to compute the nonlinearity coefficients of the CG amplifier and the results are as follows,

$$G_1 = \frac{g_{m1}}{1 + g_{m1}R_s}$$

(3-2)

$$G_3 = (-g_{m3} + \frac{2g_{m2}^2 R_s}{1 + g_{m1}R_s}).(\frac{1}{1 + g_{m1}R_s})^4$$

(3-3)

$$A_{IP3} = \sqrt{\frac{4}{3}(\frac{g_{m1}}{2g_{m2}^2 R_s}).(1 + g_{m1}R_s)^2}$$

(3-4)

Where g_{mi} shows i-th order nonlinearity of the transistor. Equations (3-2) and (3-3) represent the first and the third order nonlinearity coefficients of the CG. As can be seen from the equation (3-3), the first term is much smaller than the second term and therefore it can be easily ignored. Moreover, the third order nonlinearity coefficient of the topology is not depended on the 3rd order nonlinearity coefficient of the transistor and it is mostly determined by the second term which has high dependency on biasing point. Finally, the A_{IP3} can be computed according to equation (3-4) and by imposing power matching condition, it can be only improved by increasing second order nonlinearity coefficient of transistor which is bias depended.

One interesting possibility to improve the NF is to eliminate the power matching constrain, as can be clearly seen from the equation (3-1), by increasing the g_m or boosting the source impedance NF can be improved. A simple CG topology operating in current mode (ideally no voltage swing at the output) is depicted in Fig.3.1. Generally, the noise contribution of transistor at the output is proportional to the defined ratio between input and driving impedances represented in equ.(3-5).

$$\overline{i_{n,out}^2} = (\frac{1}{1+g_m R_s})^2 \overline{i_{n,tr}^2} \qquad (3\text{-}5)$$

As can be conceptually seen from Fig.3.1, if the driving impedance to be greater than the input impedance (which is equal to $1/g_m$ for an ideal MOS with low output impedance load), the transistor noise current is re-circulated, meaning that noise from active devices is suppressed.

Furthermore, Thanks to current mode operation (ideally no voltage swing at the output), the linearity of CG amplifier is proportional to gate-source voltage, Vgs, applied to the transistor induced by input source voltage; therefore

$$V_{GS} = -V_s \cdot (\frac{1}{1+g_m R_s})$$

$$(3\text{-}6)$$

As can be seen from (3-6), linearity performance can also be improved once the driving impedance to be greater than input impedance. In the similar behavior to the noise performance, non-linarites sources can be represented as current generators injecting their undesired products in parallel to the noise current source and since source impedance is greater than input impedance results in obligating to be circulated. Additionally, A_{IP3} with respect to the boosted source voltage can be simply computed by substituting R_B, boosted source impedance, instead of Rs in equations (3-3,3-5). The expression of A_{IP3} in unmatch condition can be expressed as follows;

$$A_{iip3@matching} = \sqrt{\frac{4 \cdot g_{m1}}{3 \cdot (2 g_{m2}^2 R_S)}} \cdot (1 + g_{m1} R_s)^2 \qquad (3\text{-}7)$$

$$A_{iip3@unmatched} = A_{iip3@matching} \cdot (\frac{g_{m1} R_s}{2})^2 \cdot (m)^3 \qquad (3\text{-}8)$$

Where $m = \sqrt{R_B / R_s}$, g_{m2} is the second order non-linearity of transistor and $g_{m1}.R_s=1$ at power matching condition. As can be obviously seen from the equation (3-8), A_{IP3} in unmatch condition is much greater than that of in match condition.

There is two approach to implement re-circulation technique. One is boosting source impedance and the other is to reduce input impedance. To reduce the input impedance, we simply enhance the g_m of the transistor and to boost the source impedance up, a simple LC resonance network is utilized as depicted in Fig.3.2. A combination of series capacitor and parallel inductance forms L-match resonance network and the R_B is boosted resistance when looking back from source of transistor toward the input port and L and C are chosen such that to resonate at the desired frequency as follows

$$C = \frac{1}{\omega_{ris} R_S} \frac{1}{\sqrt{R_B/R_S - 1}}$$ (3-9)

$$L = \frac{R_B}{\omega_{ris}} \frac{1}{\sqrt{R_B/R_S - 1}}$$ (3-10)
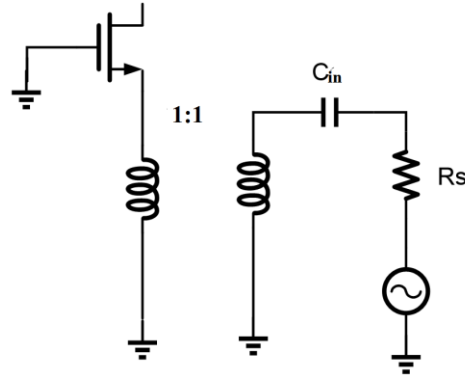
Figure 3-2: Resonance impedance boosting LC network

For instance, in simple CG amplifier with g_m of 20 ms, if we increase the source impedance to 200 Ω or input impedance to be 12.5 Ω, the IM3 product in un-match condition, decrease drastically by 22 dB and 15 dB respectively, compare to that of in match condition. On the other hand, while the fundamental is decreased by 2 dB in the first approach, it is enlarged by 4 dB in the second approach. In both cases, IIP3 improves significantly by almost 10 dB. It is well worth mentioning that in both approach not even noise figure is drastically reduced, but also it improves significantly linearity as well. Therefore, for given NF and IIP3, the second approach needs to be burned 4 times more power and it also provides 2 times higher total Gm compare to the first approach. Fig.3.3 shows the effectiveness of the re-circulation technique compare to the matched CG topology and it is improved by almost 2 dB. To prove the concept, output spectrum of the both approaches as well as the matched CG LNTA are depicted in Fig.3.4.

Furthermore, enhancing source impedance to very large value leads to the reduction of total trans-conductance. The equivalent total trans-conductance of LNTA is as follows;

$$G_m = \frac{i_{OUT}}{v_s} = \frac{1}{\sqrt{R_s R_B}}$$ (3-11)
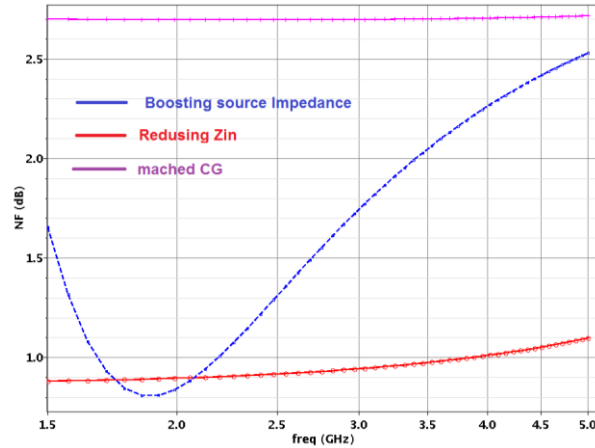
Figure 3-3: NF of the unmatch and match CG LNTA

-83.7dB

-168dB

1.9 2 2.1 2.2 freq(GHz)

match CG

-80dB

-183dB

1.9 2 2.1 2.2 freq(GHz)

Redusing Zin

-85.6dB

-190dB

1.9 2 2.1 2.2 freq(GHz)

Boosting source impedance
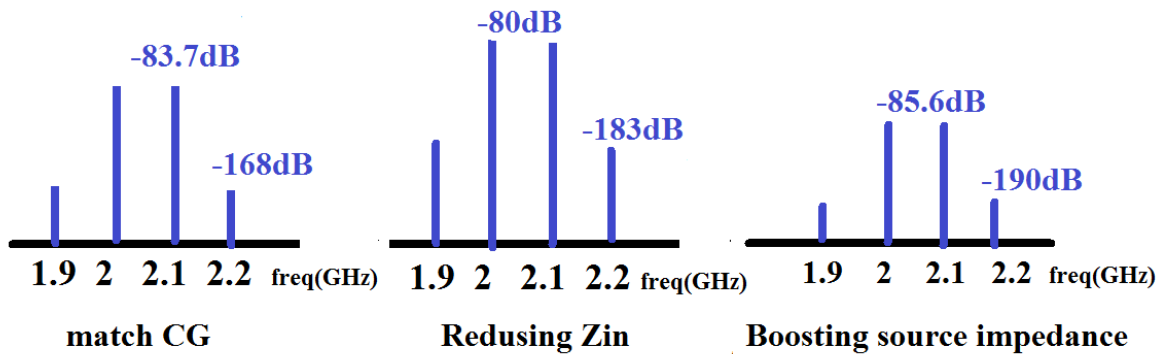
Figure 3-4: Output spectrum of the unmatch and match CG LNTA

So far the concept of re-circulation technique for simple CG topology is analytically and intuitively explained and it is also instructive to investigate the impact of boosting source impedance in simple CS topology. Since a simple undegenerated CS amplifier is potentially un-match, boosting the source impedance improves the noise figure like CG topology, but it considerably degrades the linearity due to the boosted input voltage. It means gate-source voltage of transistor is heavily solicited with higher voltage. Boosting source impedance with the same factor like CG, the fundamental and IM3 products enhance by 5 dB and 18 dB respectively. So, IIP3 degrades by 6 dB. On the other hand, increasing gm just improves noise figure and almost no impact on linearity performance. Therefore, CG topology represents better performance by means of boosting source impedance rather that CS topology. As can be seen from Fig.3.5, boosting the source impedance of the simple undegenerated CS or enhancing the gm improves the NF almost by 2 dB compare to that of simple undegenerated CS with gm of 20 mS.
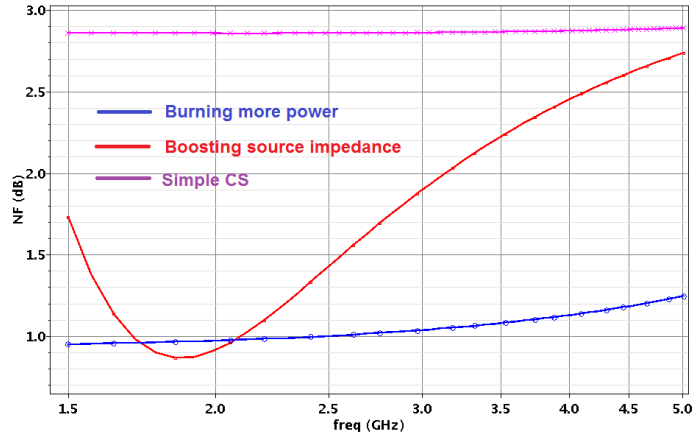
Figure 3-5: NF of undegenerated CS with boosting source impedance and burning power
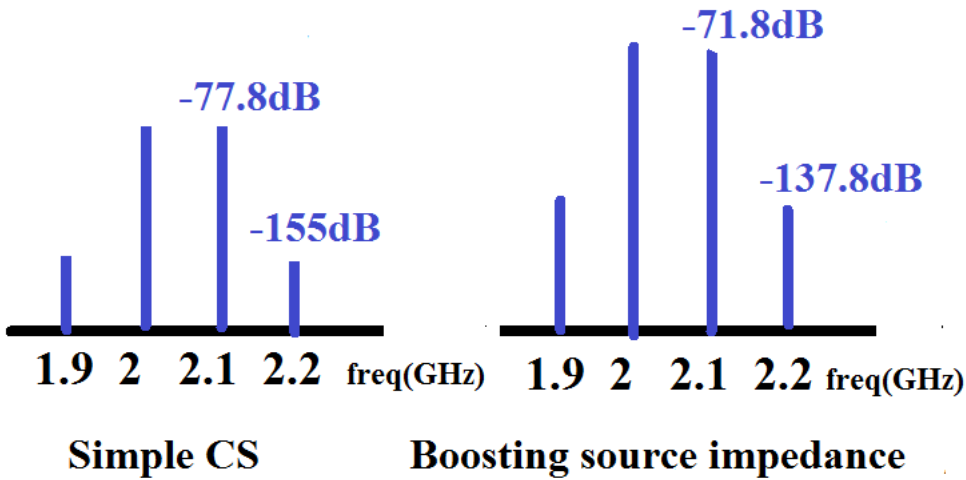
Figure 3-6: Output spectrum of the undegenerated CS with and without boosting source impedance

We can conclude that boosting source impedance is more efficient as long as the power consumption is concern, since the source impedance has to be boosted up by the L-matched network, there are some fundamental practical issues including loss of inductor, operating in narrow frequency band and also being highly sensitive to the source impedance variation which needs to be elaborated.

To boost source impedance, smaller capacitor should be chosen, so meaning imposed inductor to perform the resonance at the desired frequency. In general, we are interested in large inductor to represent large parallel loss, due to the limited Q of integrated inductor, boosted source impedance

should not be comparable with parallel loss of inductor; otherwise, NF will be heavily determined by the loss of inductor, even if considering re-circulated noise of active device.

To prove this practical issue, a typical Q of 10 is considered for integrated inductor while the driving impedance is boosted up to 200 Ω. Simulation result represents, shown in Fig.3.7, how the loss of inductor is degrading the noise performance.

(a)   (b)
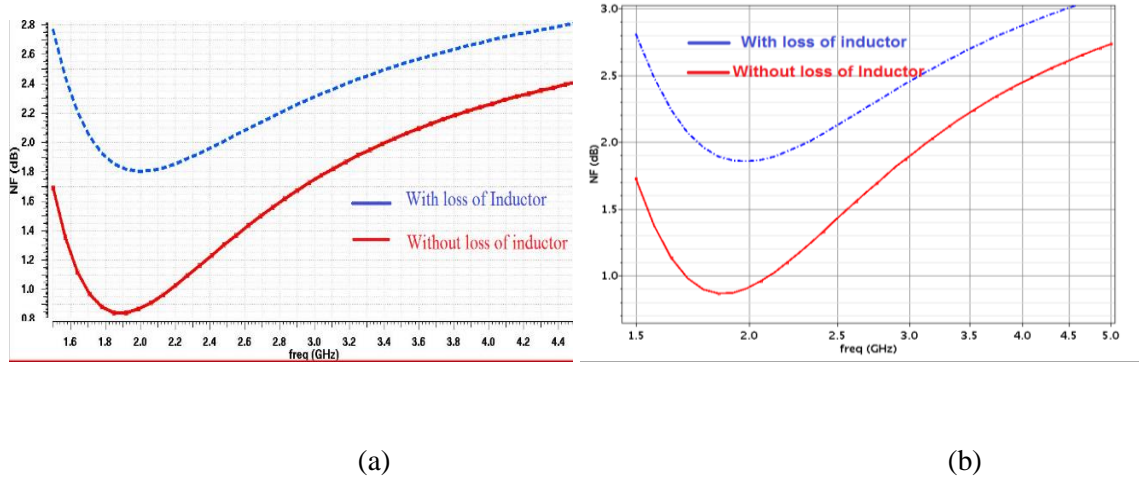
Figure 3-7: NF simulation of boosted source impedance with and without considering loss of inductor (a) CG topology, (b) CS topology

Due to the being unmatched, we are interested in minimizing the NF and its impact to the variation of the source impedance. Therefore, instead of boosting source impedance to the large value by designing L-match resonance network, it has to be designed to perform the recirculation of noise and distortion of active device and also providing optimum source impedance to be perfectly noise match.

Since the linearity of the single-ended CG Amplifier is mostly proportional to the second order non-linearity coefficient of the transistor, g_{m2}, as it is computed in (3-7), therefore one possibility to improve the linearity of the single ended CG LNA is to employ differential topology. In principle it can achieve high IP2 since the symmetric circuit produces no even-order distortion and ideally according to equation (3-4), IP3 has to improve. Of course, some random mismatch can occur and degrades the IP2 and also IP3 but IP2 will still be high. On the other hand, from the noise point of view, having imposed power matching condition, the noise of differential CG will be equal to that of single ended, but it requires to consume four times higher power.

The idea in [30] is to simply amplify the input by the factor of –A and apply the result to the gate of the CG. For an input voltage change of ΔV, the gate to source voltage changes by $– (1+A)\Delta V$ and the drain current by $– (1+A)g_m\Delta V$. Thus, the g_m is boosted by the factor of 1+A, lowering the input resistance to Rin=$[g_m(1+A)]^{-1}$ and raising the equivalent transconductance to the $(1+A)g_m$.

An auxiliary amplifier, A, can be simply formed by capacitive cross coupled configuration such that amplifying the signal by a factor of 2 without extra power dissipation. Noise factor for cross coupled configuration can be computed as follows,

$$F_{CC} = 1 + \frac{\gamma}{(1+A)^2 . g_m R_s} \qquad (3\text{-}12)$$

Where at power matching condition, $R_s = [g_m(1+A)]^{-1}$. A simple simulation is performed to show the effectiveness of cross couple configuration considering power matching constrain and compare the results with the same constrain in differential CG LNA. Illustrated in table 3.1, cross coupled configuration halves the thermal drain noise contribution of the active device while it needs to be consumed half the current compare to that of differential LNA at power matching condition. Thanks to the cross coupled configuration, common mode signal can be heavily suppressed. Moreover, it should be mentioned that there is IIP3 degradation in cross coupled configuration, since the provided gate to source voltage for transistor is doubled compare to that of in differential topology, therefore transistor will be solicited more.

Table 3-1: Comparing cross coupled and differential LNA at power matching condition

	NF(dB)	Idc(mA)	IIP3(dBm)
Diff. Topology	2.7	6	4.7
Cross coupled	1.6	3	1

It is well worth mentioning one of the main privileges of cross coupled configuration is to cancel the second order harmonic. As depicted in Fig. 3.8 [22], the output current of the second order signal is given by the following equation,

$$i_{2nd} = g_{m2}(v_{in} - A_1 v_{in})^2 \qquad (3\text{-}13)$$

Where A_1 is almost one. Thus, the transconductance for the second order frequency is zero.
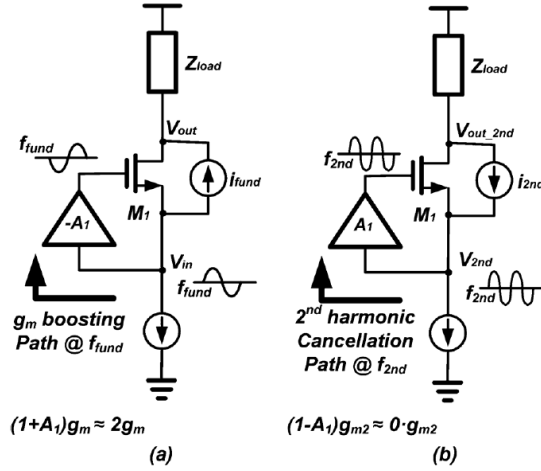
Figure 3-8: the feed forward mechanism of the cross coupled common gate circuit (a) fundamental frequency and (b) second harmonic frequency [22]

As a result, having canceled the second order harmonic, linearity of cross coupled CG LNA is depended on the first and the third order nonlinearity of transistor.

3.2   Design consideration of proposed LNTA:

The proposed class AB Common Gate LNTA is represented in Fig.3.9. The core of the LNTA consists of a pair of complementary cross-coupled CG amplifiers for higher 1dB compression point. Cascode transistors are used to enhance the output resistance of the LNTA for better operation in current mode and reducing the loading effect of using passive mixer loaded with low impedance, and also it improves reverse isolation. A feed-forward cross-coupled capacitors are employed to rejects the third-order distortion products due to MOS second-order nonlinear transconductance terms, improving IIP3. The cross-coupled configuration also improves noise by effectively doubling the device g_m, and lowering F to $1+\gamma/2$. However, in classical configuration scheme, when an external balun is used, costs increase and most of the noise improvement is lost. An on-chip balun-transformer was used in [31] to perform single-ended to differential conversion and gate boosting, introducing an additional degree of freedom (the transformer turn ratio) that allowed to trade-off noise, linearity and power. An IIP3 of 14 dBm was achieved but a complicated (lossy) four-winding transformer was required, leading to higher noise.

In [32] a similar core structure (complementary cross-coupled) was used, however the fundamental diffrenece is that LNTA was integrated within a hybrid-transformer (implementing the duplexer). In this case, the input power matching was performed by balancing impedance and leading to the source impedance boosting by a factor of 2 and reaching IIP3 of 23 dBm for the

entire receiver, but with an extra 3 dB NF penalty thanks to the lossy balancing impedance.

In the proposed unmatched LNTA, a transformer with one primary and two secondaries implements simultaneously the balun (to convert from single-ended to differential) and the impedance transformation function (in combination with the series capacitor C_{eff}). Considering the finite primary-secondary coupling factor (approximately 0.7), the transformer can be modeled as shown in Fig. 3.10. The series capacitor C_{eff} can be ideally represented as two capacitors in series: C and C_1. The series inductance $(1-k^2)L$ is resonated out by capacitor C at the center frequency. The parallel inductor k^2L forms, together with capacitor C_1, and impedance transformation network that boosts the source impedance R_S.
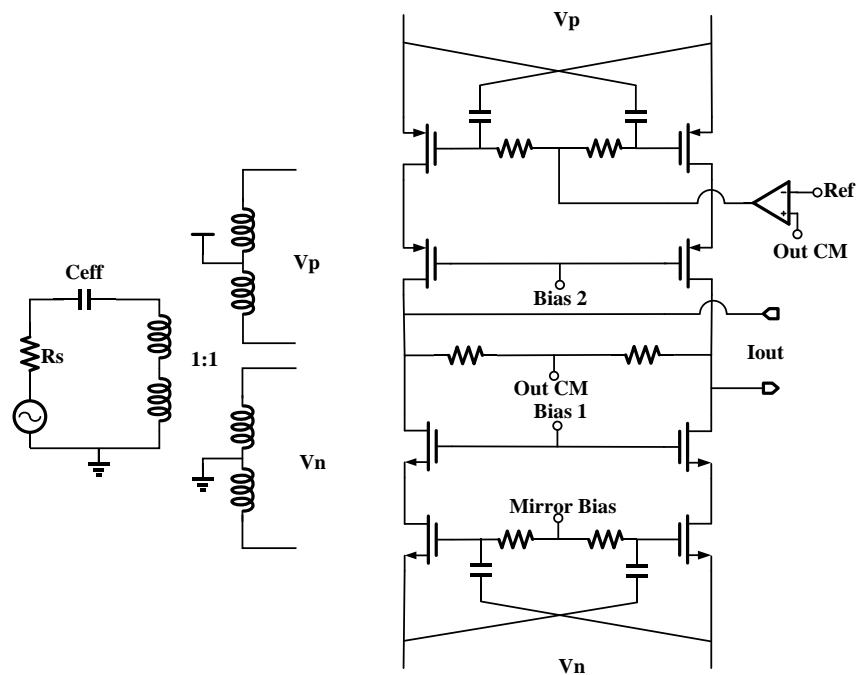
Figure 3-9: Schematic of the proposed LNTA
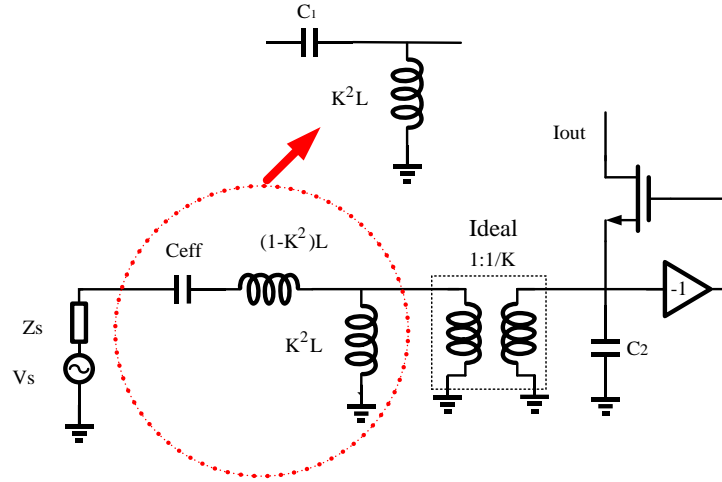
Figure 3-10: Simplified model for finite coupling factor transformer

3.2.1 Distortion and noise recirculation concept:

Linearity of LNTA is the most challenging parameters to be optimized. Thanks to current mode operation of the front-end (associated with the use of a passive mixer loaded by a low impedance) ideally no voltage swing occurs at the LNA output. In this case the distortion of the cross-coupled CG amplifier is defined by the gate-source voltage V_{GS} applied to its transistors and by the ratio between the input impedance (which is equal to $1/g_m$ for an ideal cross-coupled CG with a low impedance load) and its driving impedance. Disregarding power matching, i.e. making the amplifier input impedance much smaller than its driving impedance IIP3 can be drastically increased. Large impedance mismatch with small bias current is achieved thanks to: 1) gate-source cross-coupling; 2) complementary (p-n) topology; 3) LC network impedance boosting factor; and 4) transformer turn ratio. Source impedance boosted by the input LC network by a factor β affects IIP3 in two ways. First, it lowers the input signal current, lowering V_{GS}. Second, it makes the distortion term partially recirculate within the transistor that creates it. In fact, non-linearity products can be represented as current generators located between the source and drain of the transistors. When the source impedance is greater than input impedance the distortion terms are recirculated within the transistors. In this condition the IIP3 is:

$$A_{IP3@matching} = \sqrt{\frac{4}{3}\left|\frac{g_{m1}}{g_{m3}}\right|}(1+g_{m1}R_s)^{\frac{3}{2}}$$

(3-14)

$$A_{iip3@unmatched} = A_{iip3@matching} \cdot (\frac{g_{m1}R_s}{2})^{\frac{3}{2}} \cdot \beta$$

(3-15)

where $\beta = R_B/R_S$, g_{m3} is the third order non-linearity of transistor and $g_{m1}.R_s = 1$ at matching condition. Therefore, as it is intuitively and analytically shown in (3-14, 3-15), IIP3 can be improved disregarding power matching compare to that of in power matched.

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One way to improve IIP3 is to increase the bias current. As it is expected based on (3-15), it improves proportionally IIP3 value and verified by simulation, shown in Fig.3.11, and eventually limited in practice by the nonlinearity of the cascode transistors. It is also instructive to investigate the effect of series capacitor on IIP3 value. Choosing smaller series capacitor leads to boosting further source impedance and expecting IIP3 improvement. As can be clearly seen in Fig.3.11(a), IIP3 can be drastically improved to 35 dBm using small series capacitor of 0.4 pF, however with such a small series capacitor, the transformer loss heavily degrades the NF which will be discussed shortly. For a current consumption of 8 mA an IIP3 of around 27 dBm is achieved when the source impedance is boosted to almost 63 Ω.
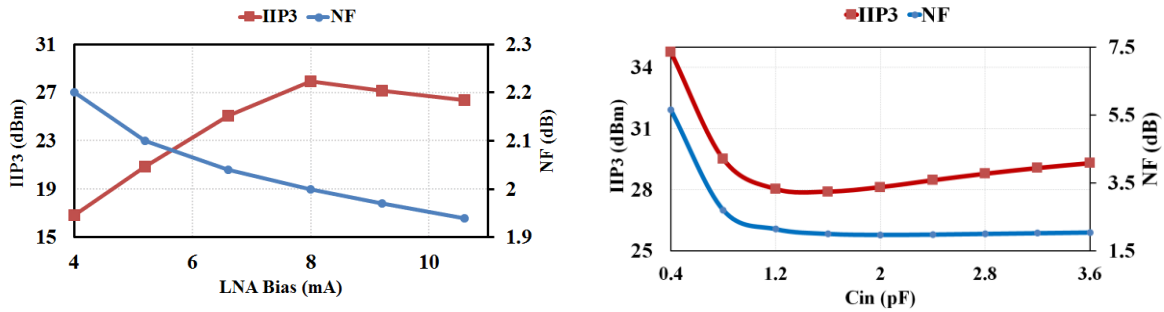
Figure 3-11: Simulation of IIP3 and NF at 2GHz (a) versus LNA bias with Cin=1.6pF, (b) versus Cin at nominal bias current.

Noise is the other key metric to be optimized. Disregarding the power matching improves the noise of amplifier as well. Once the driving impedance is greater than the input impedance of amplifier, the noise of the transistor is reduced. Initially having considered all losses associated with the transformer, the resulting noise factor of the proposed LNTA is,

$$F = 1 + \frac{\gamma}{4g_m R_B} + \frac{\omega_o L}{Q_{s1} R_s} + \frac{1 + (C_{eff} \omega R_s)^2}{R_s Q_{P1} \omega_o L (C_{eff} \omega)^2} + \frac{R_B}{Q_{P2} \omega_o L} + \frac{R_B \omega_o L}{Q_{s2}} (\omega_o C_2)^2 \qquad (3\text{-}16)$$

where, $Q_{S,K}$ and $Q_{P,K}$ are series and parallel Q in the k port respectively, C_2 is total parasitic capacitance in the secondary and R_B is equal to the source impedance R_S (nominally 50Ω), boosted by the input LC network by a factor β, n is the transformer turn ratio and g_m is the transconductance of the input transistors (assumed equal for PMOS and NMOS). According to (3-16), the second term represents the noise contribution of the active device, whilst the losses of primary and secondary winding contribute in different manner. The driving impedance is unequal in the primary and secondary (due to K<1), leading to the losses associated with the secondary winding to be more noticeable with respect to those of the primary winding. As can be intuitively seen in (3-16), boosting source impedance reduce significantly the noise contribution of active device, however, the total NF will be heavily degraded by the parallel loss of transformer. This effect can be easily confirmed by simulation, as shown in Fig.3.11. Boosting factor enlarges by reducing series capacitor value, and the NF degrades sharply (up to 6dB for small series capacitor of 0.4pF) due to being highly sensitive to the parallel loss of transformer. Therefore, it is required to optimize the overall noise contribution of the active and passive devices. Applying the classical noise

matched technique, the LNTA is designed such that the minimum noise figure (NF_{min}) is obtained for a source impedance (Z_{opt}) equal to 50Ω.

3.2.2 Transformer design considerations

Initially noise circle simulations were performed on a cross coupled configuration with g_m of 40 mS and Q = 10 and *k* = 0.7 for 3 different transformer inductance values. For each inductance value, optimum source impedance is capacitive when there is no capacitor in front, shown in Fig.3.12(a). Adding a series capacitor in front can be considered as a free noiseless component to move the imaginary part of the optimum source impedance. According to simulation result, the minimum noise is achieved when series capacitor (which is different for each inductance) shifts the optimum source impedance to real axis and providing purely real optimum source impedance. In all cases, for a 50 Ω source impedance, NF is improved with respect to the case where no series capacitor is added since the center of the noise circles moves closer to the real axis shown in Fig3.12(b). Moreover, it can be seen that, as the inductance value is increased, the 2 dB noise circle becomes larger and it shifts to the right, toward higher impedance values. This means that larger inductance values yield less sensitivity to the source impedance and, at the same time, the optimal source impedance (corresponding to F_{min}) shifts to higher (real) values. For the three inductances, the optimum source impedances are 40, 53 and 90 Ω respectively. If the source impedance stays reasonably close to 50Ω (e.g. with a VSWR of 2, corresponding to -10dB return loss) noise is minimized by choosing the middle value for the inductor and NF is less than 2dB.

Based on the designed L-match network (considering 1.6pF for series capacitor for noise matched purpose), the equivalent impedance seen the at source of the LNTA toward the antenna will be almost 63Ω at resonance frequency and the input impedance is almost 12Ω, hence creating mismatch between input impedance and driving impedance of LNTA to perform noise and distortion recirculation of active device. Even though similar concept was already used in [32], there is a fundamental difference at implementation of boosting source impedance leading to drastically improved NF of proposed LNTA. To clarify the effectiveness of proposed boosting source impedance with respect to the prior implementations in [31,32], all LNTAs are simulated with actual transformer on equal power consumption and as can be clearly seen in Fig.3.13, the proposed LNTA benefits simultaneously from privileges of both prior implementations (low NF of [31] and high IIP3 of [32]). The use of passive LC source impedance boosting allows us to achieve higher linearity and lower noise while keeping low power dissipation. Moreover, it is also interesting to point out that in the absence of the huge interference, it is plausible to halve the LNTA power consumption (4 mA in total) and still having a relatively good IIP3 value of 17 dBm with negligible NF penalty (0.2 dB degradation) as shown in Fig.3.11(a).
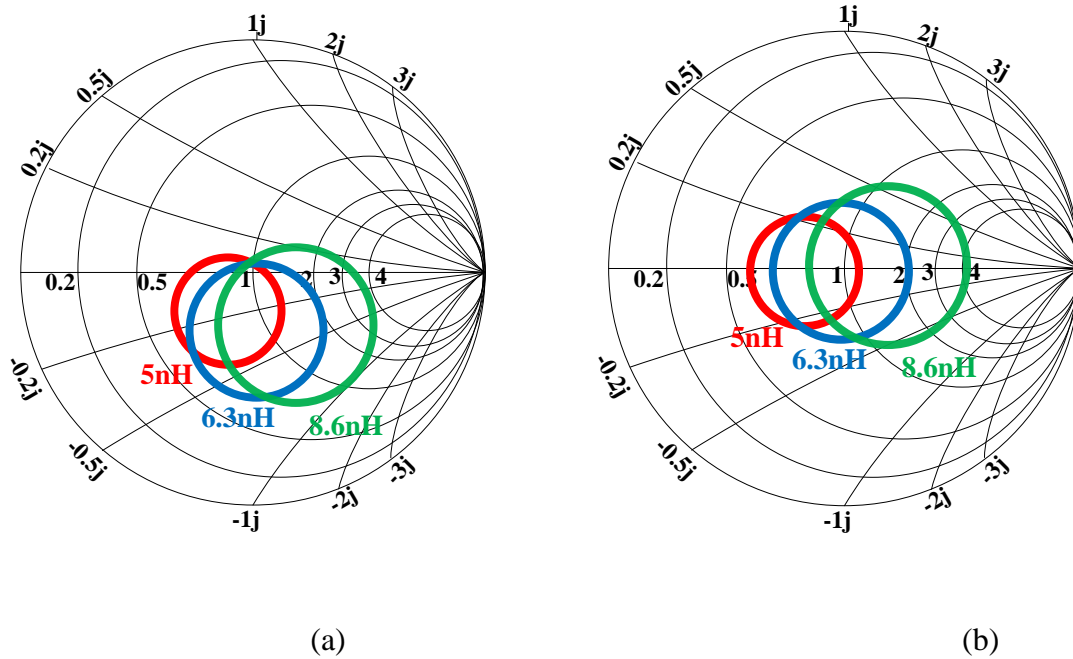
Figure 3-12: Noise circles (2dB NF contour plots) at 2GHz with different 1:1 transformer inductance (a) before adding capacitor, (b) with optimal series capacitance
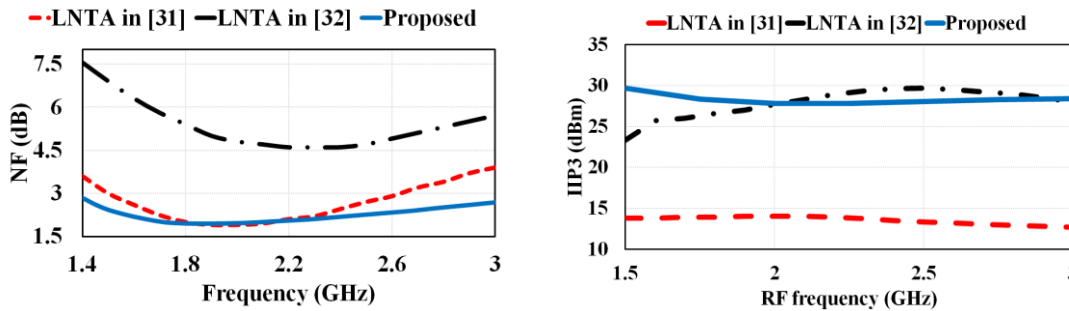
Figure 3-13: Simulation of IIP3 and NF versus frequency for the proposed LNTA and LNTA in [31] and [32] on equal power consumption.

The transformer plays an influential role for the proposed LNTA and its Q has to be maximized. Stack configuration represent highest coupling factor, however there was only one ultra-thick metal available in the 28nm technology, making this configuration unsuitable due to the unequal Q on both primary and secondary. In order to minimize losses and maximize both primary and secondary Q, the transformer is implemented in a coplanar configuration, with the primary as the center winding and the two secondaries as the inner and outer windings (connected respectively to the PMOS and NMOS transistors) to improve its coupling factor. The layout of the designed transformer is depicted in Fig.3.14. Winding width and spacing were set at 8μm and 2μm, respectively and it also represents Q of 11 and 13 for primary and secondary respectively.
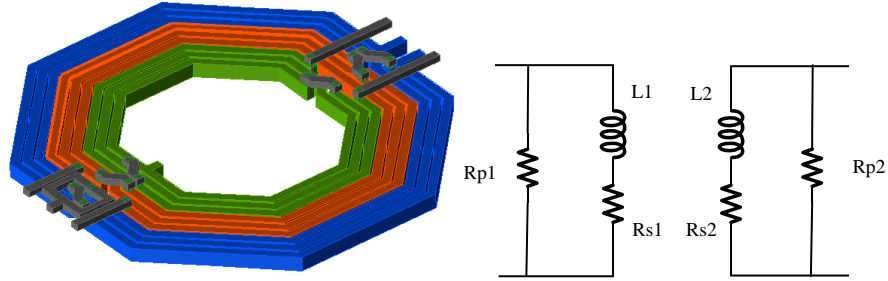
Figure 3-14: Layout of designed transformer and simplified loss models.

3.2.3 Effects of Antenna Impedance Variations

In reality source impedance may not be exactly 50 Ω, therefore it would be very interesting to show the effect of source impedance variation on IIP3. Assuming source impedance is complex impedance, Zs=Rs+jX, and for the given design (including optimum series capacitor in front) we can change Zs and simulate IIP3. In our simulation, it is assumed the real and imaginary parts of the source impedance can change from 12 Ω to 200 Ω (imaginary part could be both inductive or capacitive). As shown in Fig.3.15(a), node A has the highest IIP3 since the smaller series capacitor (yielding to higher capacitive part of source impedance) results in increasing Q of input network, i.e. the greater boosting source impedance and effectively making the driving impedance to be much larger than LNTA input impedance, hence more distortion recirculation of active device and drastically improved IIP3. As the real part decreases or increasing capacitive part of source impedance (lowering input Q), IIP3 reduces due to the lower boosting factor. By contrast in node B, the inductive part of source impedance resonates out with the series capacitor used in the design at the desired frequency and due to the lower real part of source impedance, the lowest IIP3 value is expected. Then, enlarging further the inductive part of source impedance tends to increase input network Q, i.e. boosted source impedance and improving IIP3 (node C). Simulation results (IIP3 contour plot) in Fig.3.15(a) represents if the source impedance stays reasonably close to 50Ω (e.g. with a VSWR of 2, corresponding to -10dB return loss) the minimum IIP3 value is 26 dBm.

It is also instructive to examine the effect of source impedance variation on the effective transconductance provided by the LNTA. It is expected as the source impedance increases, the dropped voltage across gate-source of transistor reduces and resulting in less effective transconductance. Intuitively the highest effective tranconductance can be achieved for small real part and also having inductive part in the source impedance to resonate out the effect of series capacitor used in the design owning to dropping more voltage across gate-source of transistor (e.g. node B in Fig.3.15(b)). As it is expected the optimum point to maximize Gm is opposed to the optimum IIP3 point. Gm contour plot simulation is shown in Fig.5 and if the source impedance stays reasonably close to 50Ω (e.g. with a VSWR of 2, corresponding to -10dB return loss), there is relatively acceptable Gm for LNTA. This provides the starting point for the optimization of the input passive network.

(a)   (b)
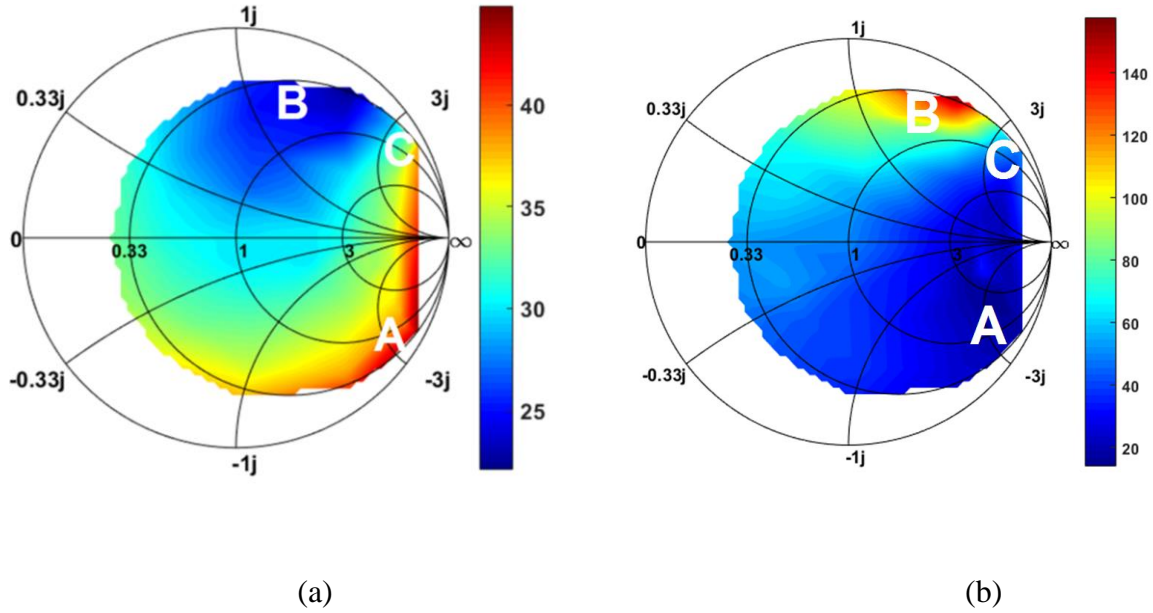
Figure 3-15: Simulation of (a) IIP3 (IIP3 contour plot), and (b) effective transconductance (Gm contour plot) for different source impedance.

3.3   Measurement and simulation results:

The LNTA is fabricated in TSMC 28nm LP CMOS process. It consumes 14.4mW from a 1.8V voltage supply. The chip, whose microphotograph is shown in Fig.3.16, has an active area of 0.29mm^2. An on-chip open drain buffer was integrated to facilitate measurements. The buffer has two modes of operation: a high-gain mode for noise measurements and a low-gain mode for linearity measurements. Unfortunately, due to unaccounted parasitics, the buffer did not provide sufficient gain in the high-gain mode to perform noise measurements. Therefore, we are reporting only post-layout simulation results for the noise in this paper. As a further validation, a modified version of the proposed LNTA (with different input series capacitor) was integrated in the receiver chain in [33], showing very good agreement between noise simulations and measurements as shown in Fig.3.17. The LNTA has a differential trans-conductance of 52 mS at 2 GHz. To measure linearity, two tones with 100 MHz offset frequency spacing were applied at 2 GHz and 2.1 GHz and as can be seen from Fig.3.18(a), an outstanding IIP3 of 27 dBm is measured which is well consistence with the simulation, thanks to both using cross-coupled complementary CG topology and the re-circulation technique. The measured IIP3 versus RF frequency is also represented in Fig.3.18(b) and its value stays above 25dBm over wide frequency range from 1.5 GHz to 2.8 GHz. The 1 dB compression point is almost 12.7 dBm. Fig.3.19(a), shows the simulated NF vs. frequency whose value is below 2.5dB over fairly wide frequency range from 1.5 GHz to 2.8 GHz. Noise circle (2.5 dB NF contour plot) simulation of the proposed LNTA is represented in Fig.3.19(b) and the optimum source impedance (corresponding to F_{min}) is almost 50 Ω.   The

blocker-NF is defined as in-band NF of the LNA when the blocker is entered into the LNA, the blocker is as close as 20 MHz to the desired frequency. At a blocker power of 0 dBm, the NF of the LNA is degraded by 0.3 dB as shown in Fig.19(c). Simulations reveal that the noise contribution of the active devices is only 15%, while the transformer contributes 21% of the total noise, confirming the effectiveness of the active device noise recirculation.

The overall performance of the LNTA and a comparison with recently published high linearity LNA are summarized in Table II. Our LNTA has the lowest power consumption with the exception of [26] which however has a much higher NF and a lower IIP3. Our IIP3 is much better than all other implementations with the exception of [29], which achieves a record 36 dBm IIP3 (when one of the blocker is at a pre-defined frequency) using programmable N-Path filters to suppress the TX blocker. This achievement however required an order of magnitude more power consumption and worse NF compared to our solution.
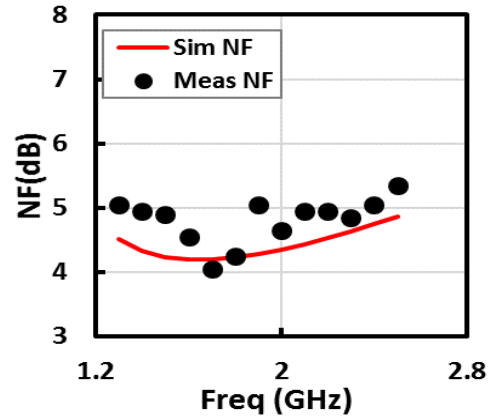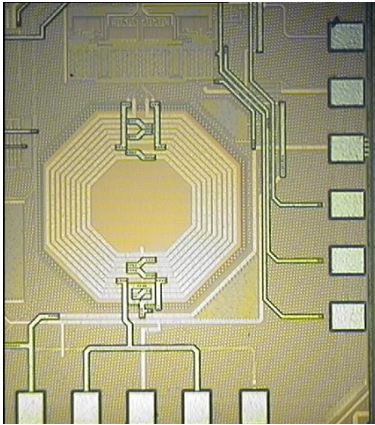
Figure 3-16: micrograph of proposed LNTA

Figure 3-17: Simulated and measurement of Receiver [33]
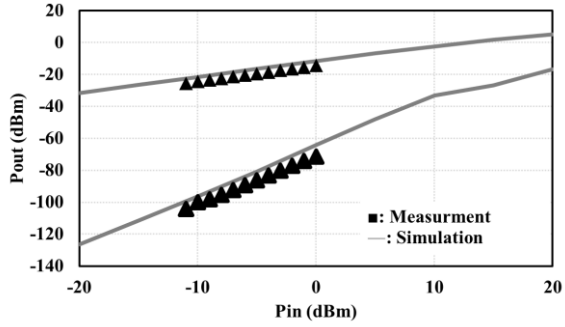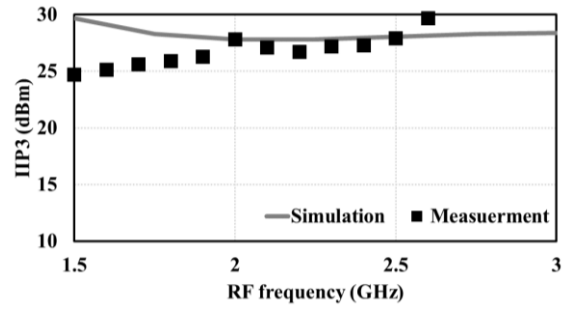
(a)   (b)

Figure 3-18: (a) Measured IIP3 with 100MHz offset frequency at 2GHz (b) Measured IIP3 versus RF frequency.
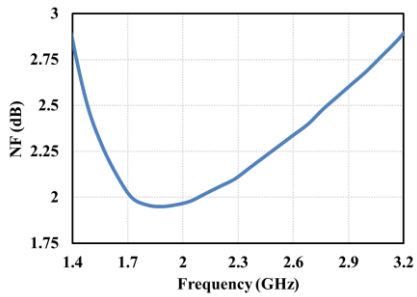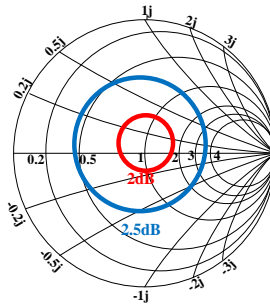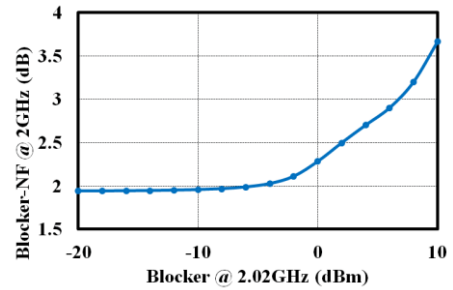
(a)   (b)   (c)

Figure 3-19: (a) Post layout simulation of (a) NF versus RF frequency (b) noise circle as a function of source impedance, (c) blocker NF

Table 3-2: performance comparison and comparison with the state of the art

Reference	This work	[29]	[28]	[26]	[34]	[35]	[36]	[37]
Technology (nm)	**28**	32	65	65	45	65	65	180
Freq. (GHz)	**1.5-2.8**	0.4-6	0.05-2.5	0.8-2.2	0.1-3	0.08-5.5	0.6-10.5	0.05-1.2
Pdc(mW)	**14.5**	81-209	20	11.5	16	16.8	72	18
NF(dB)	**1.9-2.5***	3.6-4.9	2.9	5.9	3.4-5	3*	4.5*	2.9
OOB IIP3(dBm)	**27**	36	10	20	12	15*	6.5^	7.5
Gm(mS)	**52***	NA	NA	100	34.5	100*	242*	10
Gain(dB)	**NA**	10	38	NA	NA	NA	NA	NA
External component	**NO**	NO	NO	YES	YES	YES	NO	YES
Area[mm^2]	**0.29**	0.28	0.82	N/A	0.06	1**	0.08	0.07

* Simulated, ^ Measured receiver IIP3, ** Receiver area

4 Chapter 4

Design and Analysis of 2.4 GHz 30 μW CMOS LNAs for Wearable Wireless Sensor Application

4.1   Introduction:

The increasing demand for Wireless Sensor Networks (WSN) has recently motivated extensive research efforts on ultra-low power (ULP) transceivers. For WSNs it is especially critical to reduce receiver power dissipation since the sensor is mostly operating in the receive mode rather than in transmit mode. Moreover, some ULP applications, such as wireless medical telemetry and Wearable-WSN (W-WSN), require the portable devices to operate from a single Lithium Ion battery or to use energy harvested from the environment, calling for ultra-low voltage (ULV) designs. The use of a drastically reduced supply voltage makes designing ULP receivers even more challenging. It prevents stacking of devices, limiting the achievable reverse isolation and the maximum available gain in amplifiers.

   Several low-power design techniques have been proposed to minimize the receiver power dissipation. The use of a low supply voltage (e.g. 300 mV in [38] and 180 mV in [39]) and the reuse of the same current in more than one block (e.g. [41,42,43]) are commonly adopted. The Bluetooth Low-Energy (BT-LE) receiver in [39] consumes as little as 382 μW. However, due to the extremely limited headroom, two stage inductive load LNA was used, leading to large chip area (1.65mm^2). To reduce power and area, a mixer-first approach can be utilized. However, by removing the LNA, the noise contribution of the transimpedance amplifier (TIA) that typically follows the mixer increases due to the significantly reduced TIA driving impedance. As a result, a much larger power has to be consumed in the TIA, leading to larger overall power dissipation [40]. Stacking several circuit blocks that perform different functions on top of each other [41-43] poses several isolation issues that adversely affect the overall performance and prevent true ULP operation. For this reason, an ULP LNA that adopts current-reuse within the same block is proposed.

   When the receiver noise requirements are relaxed, the main constraint on the LNA current consumption comes from the device g_m. This is due to the need to ensure impedance matching to the 50Ω source and sufficient gain to make the noise contribution of the following stages negligible. In [43] the LNA, which performs also quadrature signal splitting, has a NF of 15.8 dB but still draws 530 μA. In [44] an ULP common-gate (CG) LNA operating at 2.4 GHz with a power consumption of only 30 μW was presented. The LNA operates from a 0.8 V supply voltage and, by reusing the current several times and employing transformer-based g_m boosting, it reduces the LNA input impedance by a factor of 24 compared to a single CG transistor using the same current. In this chapter an extended analysis of the LNA in [44] is presented, including transformer optimization, stability and linearity analyses and process and supply-voltage sensitivity analyses. Moreover, the design is compared with an ULV LNA based on the same transformer-based g_m boosting technique, operating from a 0.18 V supply and consuming only 30 μW. The comparison highlights the differences between a current-reuse design with a higher supply voltage and a ULV design with the same power dissipation.

4.2   System Overview

   The main communication standards for short range and low power applications are IEEE 802.15.4, IEEE 802.15.6, and Bluetooth Low Energy (BLE). Among them, BLE is dedicated to ultra-low power consumption systems and targets applications for small and low-cost devices

powered by small batteries, such as wireless sensors [45-46]. BLE operates in the 2.4 GHz ISM band ranges between 2400 to 2483.5 MHz and 40 channels with 1MHz bandwidth are spaced within 2 MHz [45]. BLE uses frequency hopping and GFSK modulation operating at symbol rate of 1 Msps and its modulation index is 0.5. It has data rate of 1 Mbit/s with an average throughput of 270 kbit/s. The main requirements of the BLE receiver are summarized in Table 4.1 [47]. The required 20 dB NF was determined based on the following considerations. For the optimum modulation scheme, the minimum SNR is 12 dB [47]. A 10 dB margin above the basic sensitivity level of -70 dBm is typically targeted to account for implementation non-idealities and 2 dB insertion loss (IL) is associated to the SAW filter placed in front of the receiver. As a result, the noise floor equals -94 dBm [48-49]. For the IIP3 requirement the standard specifies that the input signal should be 6 dB above the sensitivity level, i.e. -74 dBm. The third order intermodulation power (IM3) together with the integrated receiver input noise floor of -94 dBm, can be at most 6 dB above the noise floor, i.e. -88 dBm. Hence the maximum IM3 is -89.2 dBm. The largest in-band interferers have a minimum offset frequency from the desired channel of 3 MHz and have a power level of -50 dBm. As a result, an antenna-referred IIP3 requirement of -30.4 dBm is derived, corresponding to -32.4 dBm IIP3 for the receiver, considering the 2 dB IL of the SAW. Out-of-band interferers are larger than in-band interferers, up to -30 dBm, but are strongly attenuated by the input SAW filter and therefore are less of a concern. In the same way, a very relaxed receiver IIP2 requirement of -12.7 dBm can be derived.

Table 4-1: Summary of BLE Receiver Requirement

RX Sensitivity	-80dBm
NF	20 dB
Maximum input power	-10dBm
Adjacent interference, $C/I_{@\ 1,\ 2,\ >3MHz}$	15, -17, -27dB
Image frequency interference, C/I_{Image}	-9dB
Phase Noise @2.5MHz	-102.5dBc/Hz
IIP3	-30.4dBm
IIP2	-12.7dBm
Minimum Image rejection	26dB

According to the aforementioned discussion, BLE standards have very relaxed requirements in terms of noise, linearity and image rejection. In WSN applications, it is extremely important to take advantage of the relaxed specifications to reduce the receiver power dissipation. The LNA is generally considered as one of the most power hungry and challenging blocks and typically dominates both the NF and the out-of-band (OOB) IIP3. The most popular LNA topologies (e.g.

inductive-degeneration, shunt-feedback, noise-canceling, etc.) were developed with the main goal of lowering the added noise. For WSN applications, instead, the main goal is to lower power dissipation. Hence, the noise-vs-power trade-off should be exploited to lower the power rather than to improve noise.

In the next section we will review the main LNA topologies that have been proposed to achieve this goal.

4.3 Review of Ultra-Low Power LNAs

Biasing transistors in the weak inversion region, where the maximum g_m/I_d can be achieved, is one of the most effective approaches to minimize the dissipated power in analog circuits [50]. However, weakly inverted transistors present very poor frequency response and, as a result, they cannot be widely used in RF circuit design. To optimize the ULP RF circuits, a figure of merit (FoM$_{RF}$), $g_m f_t/I_d$, was defined [50]. Maximizing FoM$_{RF}$ corresponds to the maximization of the gain-bandwidth-product (GBW) represented by the $g_m f_t$ product for a given bias current. Maximum FoM$_{RF}$ is achieved by biasing the transistors in moderate inversion region, which gives suitable compromise between current efficiency, i.e. g_m/I_d, and bandwidth (i.e. f_t). In this section, the fundamental limitations of popular Common Source (CS) and Common Gate (CG) LNA topologies for low power operation will be discussed. Then, the state-of-the-art LNA topologies for ULP will be investigated. In all topologies the noise contribution of the load will be neglected in order to emphasize the noise-power trade-off of the input devices.
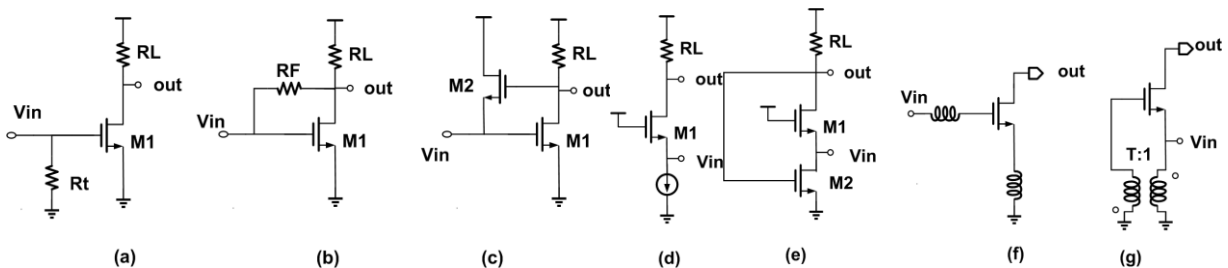
Figure 4-1: Basic LNA topologies: (a) resistively-terminated CS; (b) shunt feedback CS; (c) active shunt feedback CS; (d) common-gate; (e) active shunt feedback CG; (f) inductive degeneration LNA; (g) transformer-based CG LNA (gate boosting for T>1).

4.3.1 Resistively-terminated CS

The resistively-terminated CS amplifier shown in Fig. 4.1(a) is the simplest configuration that allows to fulfill the input matching condition independently from the device transconductance. This allows to achieve impedance matching while dissipating very low power. However, other key RF metrics are seriously degraded. The noise factor (F) of this LNA is given by:

$$F \geq 2 + \frac{4\gamma}{g_m R_s} \qquad (4\text{-}1)$$

where γ is the transistor thermal noise coefficient. To achieve a NF below 6 dB, the device g_m needs to be greater than 25 mS. The transconductance gain of the amplifier is simply given by the device g_m, hence if g_m is lower than 20 mS the LNA output current is lower than the input current and the LNA acts as a signal attenuator. Hence, lowering the bias current also leads to low gain and high noise from the following stages.

4.3.2 Shunt feedback CS

Shunt feedback CS amplifier is another popular topology and it can be relatively wideband (Fig. 4.1(b)). The noise factor (F), input impedance (Z_{in}) and the voltage gain (A_v) of the shunt feedback CS can be computed as follows:

$$F \geq 1 + \frac{\gamma}{g_m R_s} \qquad (4\text{-}2)$$

$$Z_{in} = \frac{R_F + R_L}{1 + g_{m1} R_L} \qquad (4\text{-}3)$$

$$A_V = \frac{g_{m1} + 1/R_F}{1/R_L + 1/R_F} \qquad (4\text{-}4)$$

According to (4-2), to attain a NF lower than 6 dB, the device g_m only requires to be greater than 5 mS, which corresponds to a current of approximately 300 μA in moderate inversion. To perform the input impedance matching, however, the device g_m cannot be less than 20 mS, as given by (4-3) for $R_L >> R_F$. Hence, with this topology, the consumed power is limited by input matching more than by the noise or gain constraints.

4.3.3 Active shunt feedback CS

In contrast to the resistive shunt feedback, active feedback can be utilized to perform input matching while minimizing power consumption (see Fig. 4.1(c)). A buffer is placed around a CS amplifier to provide shunt feedback without loading the CS amplifier output, as shown in Fig.4.1(c). The input impedance of the amplifier can be computed as follows:

$$Z_{in} = \frac{1}{g_{m2}(1 + g_{m1} R_L)} \qquad (4\text{-}5)$$

Both devices g_m can be easily less than 5 mS to provide input power matching (assuming resistive load of 1 kΩ), thus there is no significant power constrain from the input impedance matching condition. The NF of amplifier is given by:

$$F \geq 1 + \gamma \cdot g_{m2} R_s + \frac{\gamma (1 + g_{m2} R_s)^2}{g_{m1} R_s} \qquad (4\text{-}6)$$

It can be seen from (4.6) that, as the device g_m is reduced, the NF quickly degrades. To achieve a NF < 6 dB, $g_{m1} > 8$ mS and $g_{m2} > 1$mS are required. This is better than with the resistive shunt feedback but still not quite ULP. In fact, the current of the core amplifier (M1) is constrained by noise considerations.

4.3.4 Common-Gate

The common-gate (CG) topology is well-known for its inherent wide bandwidth. In its basic configuration, as reported in Fig. 4.1(d), the input device g_m is limited by input power matching constrain ($Z_{in}=1/g_m$) and needs to be 20 mS, similar to that of resistive shunt feedback CS amplifier.

4.3.5 Active shunt feedback CG

One of the effective methods to reduce the required device g_m for input matching constrain is to employ active shunt feedback in CG amplifier [52]. As shown in Fig. 4.1(e), the circuit utilize the CG transistor (M1) as the core amplifier, with shunt feedback provided by a CS transistor (M2). The input impedance of the amplifier is given by:

$$Z_{in} = \frac{1}{g_{m1}(1 + g_{m2} R_L)} \qquad (4\text{-}7)$$

According to (4-7), the feedback network boosts the effective g_m by loop gain, which facilitates good input matching with much less bias current. The required device g_m for CG is 20 mS divided by the loop gain ($g_{m2} R_L$). So it is reasonable to choose both device g_m to be less than 4mS (assuming resistive load of 1kΩ) to perform input matching, which allows to minimize power dissipation. The voltage gain and the noise factor are:

$$A_V = \frac{g_{m1} R_L}{R_S g_{m1}(1 + g_{m2} R_L) + 1} \qquad (4\text{-}8)$$

$$F \geq 1 + \frac{\gamma}{g_{m1} R_S} + \gamma g_{m2} R_S \qquad (4\text{-}9)$$

From (4.9), we can conclude that the main limitation of this configuration, with low device g_m, is higher NF. To attain NF<6dB, g_{m1} has to be greater than g_{m2} by a factor of approximately 4 (e.g. g_{m1}=7mS, g_{m2}=2mS and R_L=1kΩ).

4.3.6 Inductive degeneration LNA

So far the most popular inductor-less LNA topologies have been introduced. Now we can extend our exploration to magnetic devices based solutions. The inductive degeneration LNA is the most efficient method to perform low noise impedance matching (Fig. 4.1(f)). Assuming a loss-less inductor, input impedance matching can be achieved by resonating the reactive components (L_g+L_s with C_{gs}) and setting the real part g_mL_s/C_{gs} to R_s:

$$Z_{in} = \frac{g_m L_s}{C_{gs}} + s(Lg + Ls) + \frac{1}{sC_{gs}} \qquad (4\text{-}10)$$

where C_{gs} is gate-source capacitor and L_g and L_s are the gate and degeneration inductors respectively. In principle, it is possible to generate 50 Ω input impedance with a small g_m (e.g. 5 mS). However, to cancel the imaginary part of input impedance, it is required to employ very big series inductor at the gate to resonate it out. For large L_g and small L_s, the resonance condition can be written as $\omega_0 L_g = (\omega_t/\omega_0)(1/g_m)$, where $\omega_t = g_m/C_{gs}$ and ω_0 is the operating frequency. Assuming ω_t to be 4 times the operating frequency (e.g. 10 GHz for the 2.5 GHz band) a series inductor of more than 40nH would be required, which can hardly be integrated on chip. The noise figure of this topology, assuming ideal inductors, is given by:

$$F \geq 1 + \gamma g_m R_s \left(\frac{\omega_0}{\omega_t}\right)^2 \qquad (4\text{-}11)$$

According to (4.11), NF can be well below 6 dB for a g_m of 5mS. The input device transconductance is enhanced by a factor Q, equal to the quality factor of the input resonant network, improving noise and gain. However, as the input device g_m scales down (when power dissipation is reduced), performance quickly degrades. In fact, the input Q must be increased so as to keep the transconductance gain (G_m) at an acceptable level. This quickly degrades the amplifier linearity since the signal between the gate and source of the transistor increases proportionally to the Q. Moreover, the use of the larger inductors increases chip size and degrades the noise due to increased series resistance of the inductor. In summary, the main limitation of this topology for low-power designs comes from technology limitations such as inductor area and losses.

4.3.7 Transformer-based gate-boosting CG LNA

As stated earlier, the power dissipation of CG LNAs is mainly limited by the input impedance matching requirement. Applying voltage gain through an on-chip transformer across the gate and source terminals of the input transistor (gate boosting) can effectively reduce the required device g_m to perform input impedance matching. Assuming ideal and noiseless transformer, input impedance and NF of transformer-based LNA in Fig. 4.1(g) can be computed as follows:

$$Z_{in} = \frac{1}{g_m(1+T)} \qquad (4\text{-}12)$$

$$F \geq 1 + \frac{\gamma}{(1+T)^2 \, g_m R_S} \qquad (4\text{-}3)$$

where T is the transformer turns ratio. However, it is difficult to achieve voltage gain of more than 3 with an on-chip transformer. Moreover, even though the device noise can be significantly reduced, the loss of the transformer can drastically degrade the overall NF.

From the above discussion, it is quite difficult, with popular and conventional LNA topologies, to achieve reasonably good performance with very low power consumption (e.g. 100 µW). Therefore, we need to explore more innovative topologies to drastically reduce power dissipation.

4.3.8 ULP LNA Topologies

In [53] a 100µW LNA is presented. It is based on a complementary CS amplifier which is impedance matched to the source by the lossy LC resonant circuit at its input. This solution can be seen as an improved version of the resistively-terminated CS amplifier of Fig. 1(a). In fact, the inductor losses provide the resistive part of the input impedance, as required for power matching. Furthermore, the input resonator provides an effective passive voltage gain equal to its quality factor (~5), that boosts the LNA G_m. The main disadvantage is the degradation of the linearity but for ULP applications this may be acceptable. The complete receiver has a NF of 9dB, an IIP3 of -21dBm and consumes 400µW from a 0.8V supply. Another popular topology is shunt-feedback.

In [54] a complementary common-source amplifier with capacitive load and resistive shunt-feedback is presented. The resulting input impedance has a small resistive part and a large reactive part, which is resonated out using a large (10.2 nH) series inductor, leading to a large and resistive input impedance. Similar to [53], this passive impedance boosting scheme is used also to increase the gain. The resulting LNA has a NF of 5.3 dB at 2.4 GHz and draws only 150 µA from a 0.4 V supply. Even though the LNA performance and power are quite remarkable, the integration of the LNA in a complete receiver is not straightforward. In fact, the low supply voltage is hardly compatible with active mixers. On the other hand, the LNA would not work properly if a passive

mixer was directly connected at its output since a capacitive LNA load impedance is required to achieve input impedance matching.

   An improved active shunt feedback CG LNA is presented in [55]. Since reducing the bias current would severely degrade the NF, the power dissipation is reduced combining current reuse with a low voltage supply of 0.4V. Operating with ultra-low supply voltage degrades the intrinsic gain of transistors due to short channel effects. In [55], forward body biasing (FBB) technique is employed to alleviate output conductance degradation without consuming extra power. The CG LNA along with a complementary current reuse active shunt feedback and inductive g_m-boosting is utilized to improve the overall performance and decreasing power consumption. The resulting LNA has a NF of 4.5dB at 2.5 GHz and consumes 160 µW, however it requires 3 big inductors (30 nH total inductance), which significantly increase chip area.

   In [50] a single-ended LNA using g_m-boosting inductive feedback is presented. A differential inductor with grounded center-tap is connected between source and gate of input device (in AC). The stage resembles the LNA in Fig. 4.1(g) but where the input is taken at the gate terminal and the transformer acts as an auto-transformer, with unitary turns ratio, effectively halving the input impedance and doubling the input device trans-conductance. To boost the source impedance above 50Ω and lower the g_m of the input transistor required for impedance matching, the inductor, together with a series capacitor, form a high-pass L-match network. The LNA draws 100µA from a 1V supply and achieves a NF of less than 4dB at 1GHz. Compared with the other ULP solutions, the latter LNA achieves lower noise and requires less current but it is hard to further lower its power dissipation without severely degrading its noise. In fact, to push further the impedance boosting factor, an even larger input inductor would be required, increasing the impact of its losses until, as in [52], they determine the real part of the input impedance, with a considerable NF degradation.
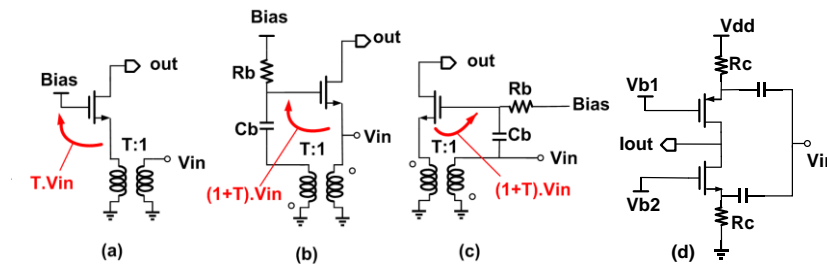
Figure 4-2: Passive g_m boosting CG amplifiers (a-c) and current-reuse CG amplifier (d) [44].

4.4   Circuit Description:

4.4.1   Gate-boosting and impedance boosting topology

   Transformer feedback has been used extensively in the literature to improve LNA performance. Various configurations have been proposed: drain-source feedback achieves very low NF [63], gate-source feedback achieves low NF and wideband operation [64-65], drain-gate transformer

feedback can be used to achieve gate-drain capacitance neutralization [66] improving the maximum gain at high frequencies. Transformer feedback can be used in combination with other techniques: in [67] gate-drain transformer feedback is used together with noise-cancellation to achieve lower noise [67] and dual-loop transformer feedback is used in [68] together with local positive feedback. Transformer feedback allows the LNA to operate at very low-voltage [38] and it has been employed also to achieve sub-1mW power dissipation [50]. The proposed CG LNAs can be described conceptually starting from the simplified schematic reported in Fig. 4.2(a). A transformer with a 1:T turns ratio can be used to lower the power consumption of a CG amplifier in two ways: first, using a step-up transformer (T>1) as a wideband impedance converter by a factor T^2. Compared with an LC impedance transformation network, transformers have wider bandwidth and are less sensitive to inductor losses. Second, a 1:T transformer can be used to boost the gate-source voltage by a factor 1+T, without requiring extra power (Fig. 4.2(b)). In this work the basic idea is to combine impedance transformation and passive signal-boosting. As shown in Fig. 4.2(c), the LNA input is connected to the primary of the transformer and to the gate of the input device, while the source of the same device is connected to the transformer secondary. Assuming (ideally) a transformer with k=1, the source voltage is boosted by a factor of T while the gate-source voltage is boosted by a factor 1+T with respect to the input. The G_m is therefore:

$$G_m = (1+T)g_m \qquad (4\text{-}14)$$

The input impedance is given by the impedance seen at the device source divided by T^2:

$$Z_{in} = \frac{1}{g_m T(1+T)} \qquad (4\text{-}15)$$

To evaluate the required device g_m and the achievable NF versus the transformer turns ratio, the schematic in Fig.4.2(c) with lossless transformer was simulated and the results are reported in Fig. 4.3. A step-down transformer (T<1) can provide higher signal current and also improve NF but it significantly raises the power consumption. For instance, for T=0.25, NF can be as low as 0.8 dB and the required device g_m to perform input power matching is 64 mS, which is extremely power hungry for this application. With a 1:1 transformer (T=1) the device g_m required for impedance matching is $1/(2R_s)$ and G_m is the same as with a CG amplifier that carries twice as much current (i.e. doubling the G_m/I_d ratio). To save power, a step-up transformer should be used instead. Neglecting transformer loss, for T>>1, the required device g_m (and therefore power consumption) scales down as T^2 while F converges to $1+\gamma$ (i.e. typically below 3dB). Hence, the noise-power trade-off is much better compared to other ULP topologies such as the resistive-termination amplifier. With T=2, the device g_m required for impedance matching is $1/(6R_s)$ and G_m is one half that of a CG amplifier that carries six times the current (i.e. three times as efficient). When T becomes large transformer losses are no longer negligible. Modelling transformer losses as a resistance R_{loss} at its secondary, the LNA noise factor is:

$$F = 1 + \frac{\gamma T}{1+T} + \frac{T^2 R_S}{R_{loss}} \qquad (4\text{-}16)$$

where γ is the MOSFET noise parameter, the second term on the right-hand side accounts for the transistor thermal noise. For T=2 and a loss-less transformer F=1+2/3γ, which corresponds to a NF of 2.2 dB at the desired frequency. For large T the third term dominates since R_{loss} does not scale up as T^2. At the same time the G_m scales down as 1/T, making the noise of the following stages more important. An additional power saving technique is highly desirable to achieve ULP operation. Two options will be investigated: current-reuse and ultra-low supply.

4.4.2   Current-reuse LNA Design

Stacking more devices to re-use bias current can improve voltage efficiency, further reducing power consumption. A current reuse scheme for CG amplifiers is shown in Fig. 4.2(d): a PMOS is stacked on top of an NMOS and the signal is fed at both sources through capacitors, resulting in an equivalent $G_m = g_{m,NMOS} + g_{m,NMOS}$. For the same input impedance and NF, this enables to halve the DC current. A similar solution was adopted in [51] but using large inductors instead of resistors. Merging passive gain boosting in Fig.4.2(c) and current reuse scheme in Fig.4.2(d), results in the device g_m required for impedance matching to be 1/(12R_s). One of the issues to deal with is the minimum supply voltage required by the voltage-stacking scheme. When a low supply voltage is used the value of the bias resistors must be reduced, increasing the NF. In this work, we assume that only a supply voltage of 0.8V is available and used for the entire design. Driving one of the two transistor sources with the secondary of the transformer eliminates one of the two bias resistors. This leaves plenty of voltage headroom that can be used to further reduce the DC current by stacking more devices. The schematic of the actual ULP LNA proposed in this work is depicted in Fig.4.4. Two NMOS and two PMOS share the same bias current and have the same gate-source voltage signal. To have equal g_m for all devices, PMOS size is 3 times that of NMOS and all devices are biased in moderate inversion for optimum FoM$_{RF}$. Assuming all devices to have the same g_m, the total equivalent G_m is equal to four times the device g_m. Combining this current-reuse scheme with a 1:2 transformer, the device g_m required for impedance matching is only 1/(24R_s). As a result, the LNA bias current can be as low as 38µA. The voltage drop across the 3 kΩ bias resistor is less than 120mV, leaving on average more than 170mV Vds across each MOS to ensure operation in saturation region. The gate-source voltage of each device is three times the LNA input voltage, resulting in a total G_m of 4x3/(24R_s)=10mS. This is one half that of a plain CG amplifier but with a current saving of 24x and a 12x G_m/I_d ratio. Including transformer losses, the noise factor of the proposed LNA is:

$$F = 1 + \frac{\gamma T}{1+T} + \frac{T^2 R_S}{R_{loss}} + + \frac{T^2 R_S}{R} \qquad (4\text{-}17)$$

where R_{loss} is the equivalent parallel loss resistance of the transformer at secondary, and R is the biasing resistor. The bias current is set through a 1:20 current mirror using two diode-connected

transistors in series, one NMOS and one PMOS, connecting to the gates of M2 and M3. The drain voltages of M4 and M1 are set to 0.65V and 0.25V respectively through two folded-cascode OPAMPs. Each OPAMP consumes 0.8 µA and its reference current (0.2 µA) is used also to generate Vref1 and Vref2. The total power dissipation of the references and bias circuits is 3.1 µW. In a complete receiver the proposed design can operate as low-noise transconductance amplifier (LNTA) in front of passive mixer since it has sufficiently large transcondutance of 10 mS and a sufficiently high output impedance is 1.25 kΩ. Notice that, if a cascode had been used instead of M2 and M3 in Fig.4.4, ideally the required device gm to perform input matching would be 1/(12Rs) and the required current would be doubled. To preserve the same drop voltage across drain-source of all transistors, the bottom resistor would have to be halved, degrading the NF.
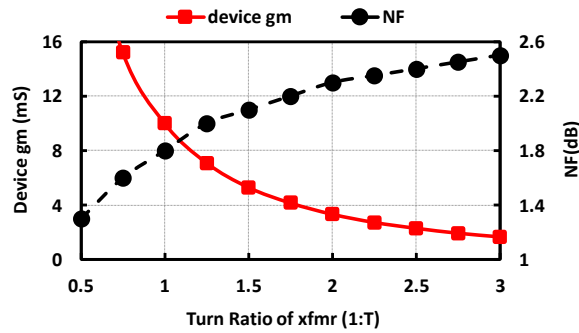
Figure 4-3: Simulation of required device gm and NF vs T
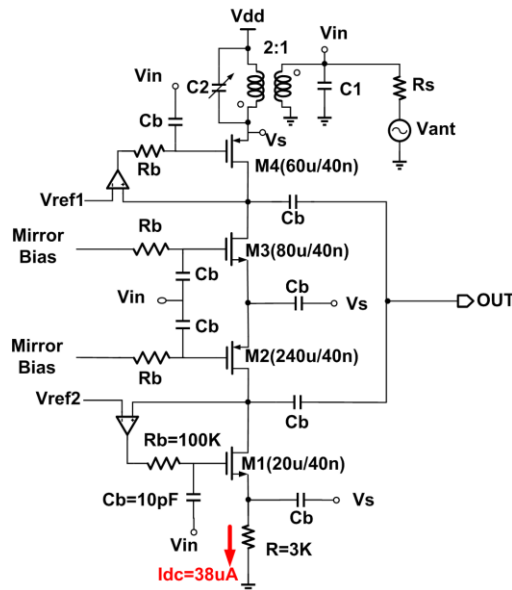
Figure 4-4: Schematic of Proposed ULP LNA [44]

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4.5   ULV LNA Design

In this section, we investigate feasibility of proposed impedance transformation and passive signal-boosting for ultra-low supply voltage LNA, as shown in Fig. 4.5. Instead of employing current reuse approach, we can drastically reduce supply voltage to minimize the power consumption. For fair comparison, the supply voltage is considered to be 0.18 V, similar to the average dropped voltage across drain-source of transistors in the current reuse LNA of Fig. 4. Additionally, for the same transformer turns ratio T=2, the required device g_m for impedance matching is $1/(6R_s)$. Using a four-times higher bias current compared to the current-reuse LNA of Fig. 4.4, the power consumption is nearly equal. Due to the extremely limited available voltage headroom, inductive load has to be used. Moreover, an ULP charge pump can be employed to boost the available supply voltage to the sufficient value to drive the gate of the transistor (e.g. in [39] the supply voltage of 0.18 V was boosted by factor of 3, reaching 0.54 V). Since a very small static current is required from the boosted voltage, the power dissipation and area occupation of the charge pump will be determined by other receiver building blocks and is not further investigated here. If we model the noise of the load inductor as a parallel resistor R_{load}, the equivalent noise factor can be computed as follows:

$$F = 1 + \frac{\gamma T}{1+T} + \frac{T^2 R_S}{R_{loss}} + \frac{4T^2 R_S}{R_{load}} \qquad (4\text{-}18)$$

where R_{load} is the equivalent loss of the load inductor. As can be clearly seen from (4-18), due to the limited Q of on-chip inductors, inductive load significantly contributes to the total noise factor. In fact, even assuming equal loss resistance for transformer and load inductor, the noise of the load directly goes to the output, while only half of the input transformer noise current goes to the output due to the input matching, as a result the input referred noise of the load counts 4 times more. As a consequence, the NF of the ULV is expected to be higher than for the current reuse LNA. For fair comparison, the load inductor is chosen such that the two LNAs have almost equal gain. The load inductor is chosen to be 3.5 nH and has a Q of 11.5. It is implemented in 4 turns, winding width of 6μm, spacing of 2μm and the occupied area is 0.048 mm². It is obvious that using inductive load leads to a narrow-band frequency response, as will be clearly shown in the simulation results (Fig.4.13).
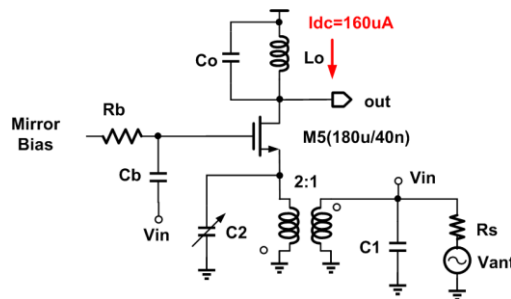
Figure 4-5: Schematic of ULV LNA

4.6   Stability

   In high frequency amplifier design, stability needs to be wisely taken into consideration. Even though standard CG LNAs are ideally very stable, it is interesting to investigate the stability of the proposed LNAs due to application of g_m boosting. The parasitic gate-drain capacitance introduces a high-frequency feedback path that reflects the load impedance at the input and can cause stability issues. This effect is more alarming for inductive loads. In fact, due to the Miller multiplication, inductive loads can create negative impedance at the input and potentially cause instability. The Rollett's stability factor (K factor), represents stability utilizing S-parameters and is expressed as follows [56]

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12}S_{21}|} \qquad (4\text{-}19)$$

   When K>1 circuit is unconditionally stable. It can be observed from the simulation results in Fig. 4.6 that the ULV LNA is unconditionally stable at all frequencies Initially the K factor of current reuse LNA was dangerously close to 1 at high frequencies. This is due to the fact that transistors M2 and M3 were oversized by factor of 4 with respect to M4 and M1 respectively in order to enable their biasing with gate voltages within the supply rails. Effectively M2 and M3 are biased in weak inversion, which strongly degrades their f_T. Using above-supply biasing as for the ULV LNA transistor would allow to reduce their size by 4x, significantly improving stability thanks to the lower S_{12}. As an alternative, in this work, a small 100 fF capacitor with 50Ω series resistor is added to the output. This increases losses at high frequencies, well above the 2.5 GHz signal band, reducing S_{22} and ensures unconditional stability also for the current reuse LNA as can be clearly seen in Fig.4.6.
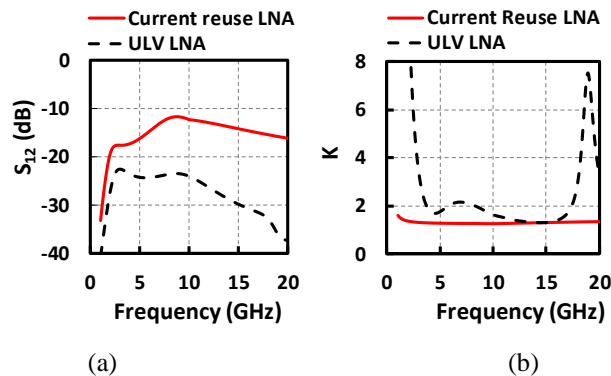
Figure 4-6: Stability simulations: (a) S_{12} and (b) K factor.

4.7   Linearity Analysis

The dominant sources of nonlinearity in a MOS transistor are the nonlinear transconductance g_m, which converts the linear input voltage to nonlinear output drain current, and the output conductance [57]. When the voltage gain is sufficiently low, as in the present case, the drain conductance nonlinearity can be neglected to simplify further the analysis. Hence, in this section IIP3 will be evaluated assuming a grounded output. The weakly nonlinear MOS model for analysis of IIP3 is expressed as follows:

$$i_d \approx g_{m1}V_{gs} + g_{m2}V_{gs}^2 + g_{m3}V_{gs}^3 \qquad (4\text{-}20)$$

To compute the IIP3 of the LNA, the simplified schematic of Fig. 4.7 can be used. The equivalent signal generator is represented at the source, scaled by the transformer by a factor T. The gate signal is therefore applied to an ideal amplifier that scales down the signal by 1/T. The complete derivation of the Volterra kernels is provided in Appendix II. The resulting IIP3 voltage A_{IP3} can be expressed as:

$$A_{IP3} \approx \sqrt{\frac{4}{3}\left|\frac{G_1}{G_3}\right|} \qquad (4\text{-}21)$$

The nth-order transconductance nonlinearity coefficients of the transistors (g_{mx}) are derived from simulations and used in (4-21) to estimate the expected LNA IIP3. For the current reuse LNA, g_{mx} is the summation of nth-order nonlinearity of all NMOS and PMOS transistors. In Fig. 8 the second-order (g_{m2}) and third-order (g_{m3}) nonlinearity transcondutance coefficients of transistors versus V_{gs} is reported and each of them is separately extracted at its nominal Vds in the entire LNA. In principle, complementary derivative superposition could have been used as an effective linearization method to improve the stacked LNA IIP3 [58,59]. For instance, one NMOS transistor can be biased in strong inversion and the other one in weak inversion such that the nonlinearity of the two have the same magnitude but opposite polarity and cancel out each other. In this design, however, the main constraint is given by the NF vs power trade-off. Biasing the transistors in strong inversion to improve linearity would lower the overall transconductance due to the lower g_m/I_d and degrade the NF or require a higher bias current. Moreover, in order to ensure operation of all the transistors in saturation a higher supply voltage or fewer stacked devices should be used.
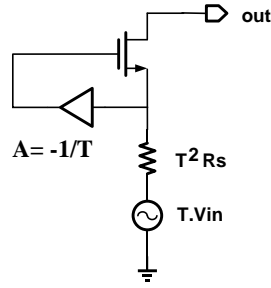
Figure 4-7: Simplified schematic for linearity analysis.

In this design the Vgs of all the devices are not equal: while M1 and M4 are biased in moderate inversion, the biasing of M2 and M3 was chosen to ensure that the gate of M2 stays above ground and the gate of M3 stays below the supply voltage. This avoids the use of a supplementary supply voltage but pushes M2 and M3 closer to weak inversion. The transistors small-signal nonlinear parameters at the nominal bias for the current reuse LNA (M1-4) and for the ULV LNA (M5) are reported in Table II. The IIP3 of the two LNAs is reported in Fig.4.9 as a function of the two-tones frequency spacing. An IIP3 of -11.3 to -10.3dBm for the current reuse LNA and -10.7dBm for the ULV LNA are achieved. Based on the extracted nonlinearity coefficients and equation (4.21), the estimated IIP3 are -9.2dBm and -11dBm for current reuse LNA and ULV LNA respectively. The excellent agreement between calculations and simulations confirms the validity of the nonlinearity analysis for the ULV LNA. For the current reuse LNA, the 1-2dB error is likely due to the approximation taken when computing the combined distortion of the four transistors. In fact, the nonlinear voltages at gate and source of the four transistors are not exactly equal since some of them, being AC coupled, differ in the second-order intermodulation terms at f_1-f_2, that are not propagated by the AC-coupling capacitors. Nonetheless, the IIP3 is mostly determined by the third order nonlinearity coefficients and it is dominated by M2 and M3, that are biased closer to weak inversion and share the same source node, leading to an acceptable error.
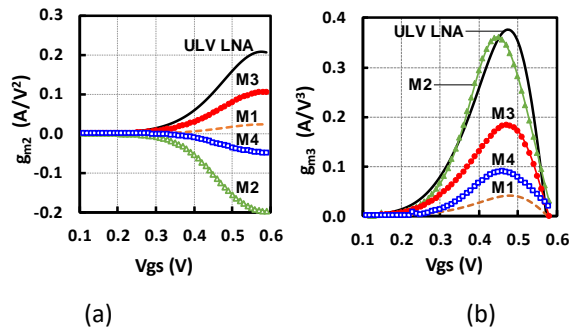
Figure 4-8: (a) Second-order (g_{m2}) and (b) third-order (g_{m3}) nonlinearity transcondutance coefficients of transistors versus Vgs.

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Table 4-2: extracted nonlinearity coefficients of transistors

	M1	M2	M3	M4	M5
g_{m1}(mA/V)	0.834	1.12	0.975	0.796	2.7
g_{m2}(mA/V^2)	7.35	-9.1	9.5	-7.2	18
g_{m3}(mA/V^3)	32.3	51.7	52	35.5	67.3
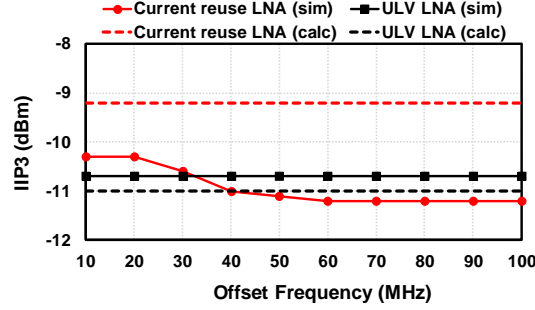
Figure 4-9: Simulated and calculated IIP3 vs offset frequency from 2.4 GHz for current-reuse LNA (V_{gs}: $M_{1,4}$=0.4 V; $M_{2,3}$=0.3 V) and ULV LNA (Vgs=0.35 V).

4.8   Transformer Design and Optimization

The transformer is attached to the LNA input, hence its noise (loss) is directly added to the antenna noise source and degrades the NF. Moreover, the transformer offers ESD protection and it boosts the input transistors source voltage by a factor of 2. To design a transformer, self-inductance (L), quality factor (Q), coupling coefficient (k), and self-resonance (f_{SR}) are the main parameters to be considered. Self-resonance should be chosen such that Q is maximized at the operating frequency (f_0). As a rule of thumb, f_{SR} can be chosen to be twice f_0. The overall performance is highly dependent on the adopted technology back end of line (BEOL) and on the adopted transformer configuration. In the 40nm CMOS technology used for this design only one ultra-thick metal with low sheet resistance (5 mΩ/sq) was available. A stacked transformer configuration has higher coupling factor but suffers from stronger capacitive coupling between primary and secondary. Moreover, the winding implemented in the high resistivity thin metal layer would lead to a lower Q. In contrast, coplanar configuration has less capacitive coupling resulting in high and more balanced Q on both primary and secondary but it has lower coupling factor. Since parasitic capacitive loading is present on both primary and secondary, both primary and secondary losses should be minimized. Hence, a coplanar configuration was selected.

The following aspects were considered to optimize the transformer. Transformer losses can be seen as a parallel loss resistance, which should be maximized. This calls for a high Q and high L. To maximize L, a large number of turns, large radius, and narrow spacing are required. Higher Q can be achieved by increasing the radius, winding width, and winding spacing. Finally, high k is achieved by increasing the number of turns and decreasing the inter-winding spacing. We are interested in designing a step up transformer (with turns ratio of 1 to 2), with highest Q and k. Two

and four turns were considered for primary and secondary windings respectively. Even though increasing winding width can improve the Q (up to the point where parallel losses linked with the substrate become dominant [38], [57]), in a coplanar transformer, this would degrade k and hence the effective turns ratio. In a step-up transformer, parallel loss is more important, especially in the secondary and therefore a relatively small (4 μm) winding width was chosen. Choosing a large radius (90 μm in this design) results in high inductance. For a given winding inductance, a large radius allows reducing the number of windings, thus reducing the parasitic capacitance and improving the Q. Additionally, to maximize k, minimum winding spacing of 2μm is chosen. The layout of the designed transformer, whose area occupancy is 0.065mm^2, is shown in Fig. 4.10. The two middle windings make up the primary, which is inserted between the inner and outer winding of the secondary to maximize the coupling factor. EMX software was used to optimize and perform Electromagnetic (EM) simulation to precisely model transformer properties especially self-inductance (L), quality factor (Q), coupling coefficient (k). According to the EM simulation, a lumped model was derived to characterize the transformer. As can be seen in Fig. 4.12, there is a very good agreement between EM simulations and the extracted lumped model, which allows to examine the transformer design. A good compromise between reducing the losses, maximizing coupling factor and minimizing the area were achieved. The designed transformer has Q of 9 and 14 for primary and secondary respectively and the coupling factor is close to 0.8 at 2.4 GHz. The step-up coplanar configuration exhibits higher Q on the secondary due to the higher self-inductance. The self-resonance occurs above 9 GHz and the peaks of the Q are between 4 and 6 GHz, which shows that substrate losses were properly minimized and ensures that high Q is achieved even in worst-case corner with lowest f_{SR}.
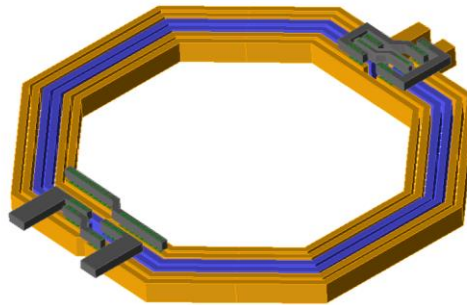
Figure 4-10: Layout of transformer
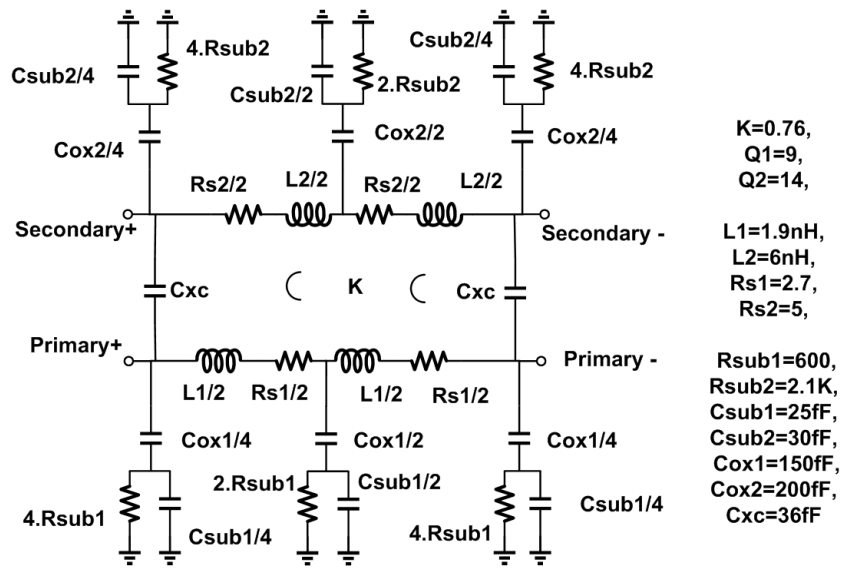
Figure 4-11: Lumped model of the transformer.

(a)

(b)

(c)

(d)
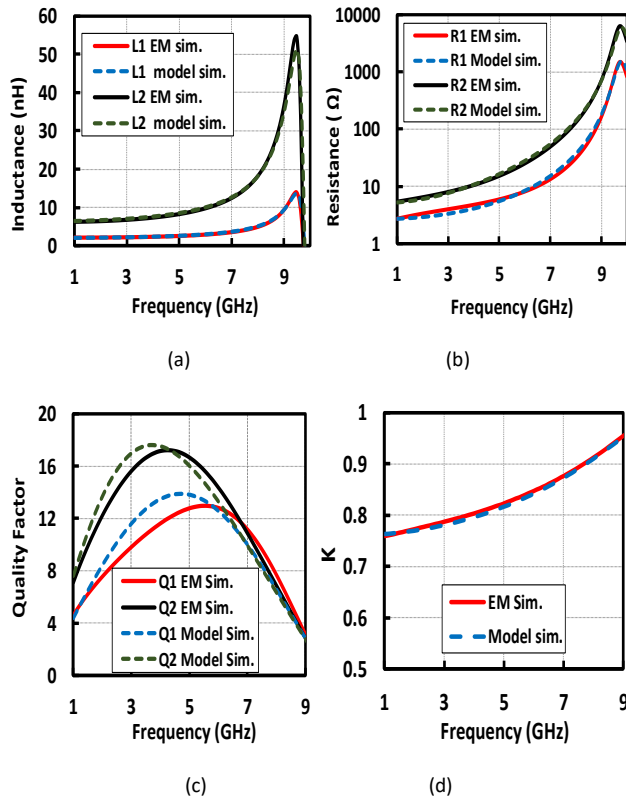
Figure 4-12: Simulation results of EM and lump model of transformer, (a) inductance, (b) loss, (c) Quality factor, (d) coupling factor

4.9   Simulation Results

The proposed LNA was designed in TSMC 40nm CMOS technology using low threshold devices. The current-reuse LNA has a supply voltage of 0.8 V. The ULV LNA has a supply voltage of 0.18 V, which can be generated directly from energy harvested from environment [2]. The dissipated power in both LNAs is only 30 μW excluding the biasing network. The LNAs were designed and optimized to operate at 2.4 GHz. However, thanks to the use of a wideband transformer, the operating frequency band can be easily tuned though a variable capacitor (C_2) placed on the secondary of transformer between 1 GHz and 4 GHz. However, for the ULV LNA, an additional variable capacitor for load tuning is also required. Fig. 4.13(a) shows the performance of the proposed ULP LNA when tuned to operate at 2.4 GHz for WSN applications. As can be seen, it has a well-matched input impedance (S_{11} = -22 dB) at the desired frequency and it achieves a voltage gain of 14.2 dB while its 3-dB bandwidth is 2 GHz.

The minimum NF is 3.3 dB, including the transformer losses. The effectiveness of the passive g_m-boosting in a CG LNA can be seen considering that, for a lossless transformer, the NF is only 2.3 dB at the desired frequency, a remarkable result with a DC current of just 38μA. The performance of the ULV LNA is plotted in Fig. 4.13(b). The input return loss is as low as -25dB. Voltage gain and NF are 14 dB and 5.2 dB respectively at the desired frequency. The noise contributors of both LNAs are represented in Fig. 4.14. Simulations do not include the noise contribution from the voltage regulator that would be required in real applications. As can be clearly seen, the noise contribution of transformer losses is less than 10% of the total noise in both cases, confirming the effectiveness of the transformer design optimization. Fig. 4.14(a) shows that for the current-reuse LNA the dominant noise contributor comes from the active devices, with a minimal contribution from the bias resistor. Fig. 4.14(b) shows that, for the ULV LNA, the losses of load inductor are dominant. This is due to the limited Q of the on-chip inductor but, more importantly, to the fact that the load inductor losses weigh 4 times more than for the input transformer, as indicated by (4.18). Unfortunately, it is unavoidable to use inductive loads at drastically reduced supply voltages. To simulate IIP3, two input tones are placed around 2.4 GHz with 20 MHz offset. Simulation results for current-reuse and ULV LNAs are -11.6 dBm and -8.6 dBm respectively, as reported in Fig. 4.15. A slight improvement/degradation is observed with respect to the IIP3 analysis carried out under low load impedance condition.
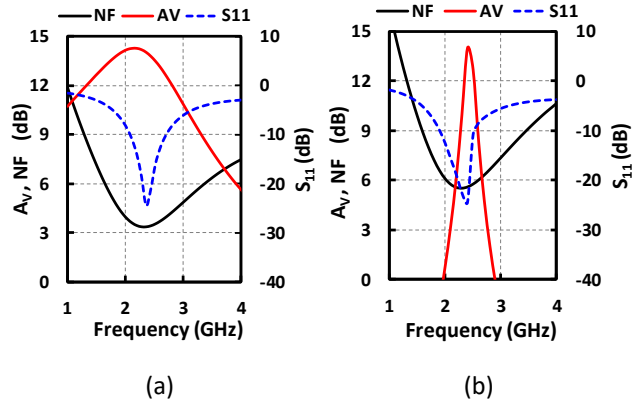
Figure 4-13: Voltage gain, NF and S_{11} of (a) current-reuse LNA and (b) ULV LNA.
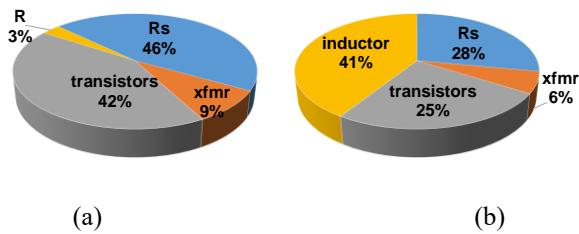
Figure 4-14: Noise contributors in % for (a) current-reuse LNA and (b) ULV LNA.
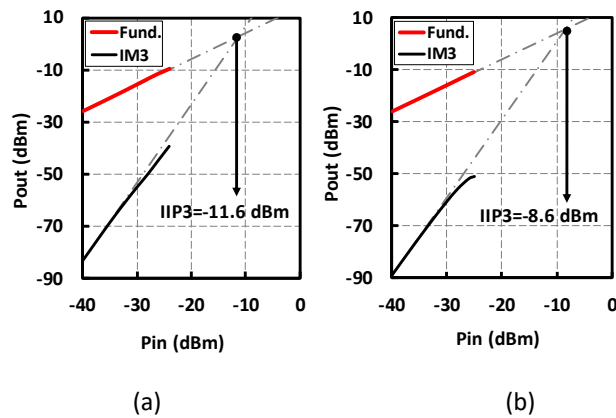
Figure 4-15: Simulated IIP3 of (a) current-reuse LNA and (b) ULV LNA.

4.9.1 Process and Supply Voltage Variations

It is very important to investigate the sensitivity of the LNAs performance to the variations in process corners and supply voltage. The effect of a supply voltage variation of +/-10% on voltage gain (A_V) and NF for both LNAs are reported in Fig. 4.16. The current-reuse LNA is almost insensitive to the 10% variation of supply voltage. However, if supply voltage reduces below 0.68V, the biasing mirror circuit does not work properly and the overall performance is degraded. The ULV LNA A_V is almost insensitive to variations in the low (0.18 V) supply since its gate bias voltage is generated from a separate (boosted) supply. The NF variation is less than 0.2dB. Gain, noise and input return loss simulations were performed in three different process corner cases (SS @+100ºC, TT @27 ºC, FF @-55ºC) and the results are reported in Fig. 4.16 (a) for the current-reuse LNA and in Fig. 4.16(b) for the ULV LNA. For the current-reuse LNA, A_V and NF variation in all corner cases are less than 1dB and 1.4dB respectively. ULV LNA performance is a bit more sensitive to the process corners and +/-1dB and +/-2dB peaking variation for NF and Av is shown respectively. In both LNAs, very good impedance matching is also preserved across process corners. The overall performance of both LNAs are acceptable with respect to the corner case variation.
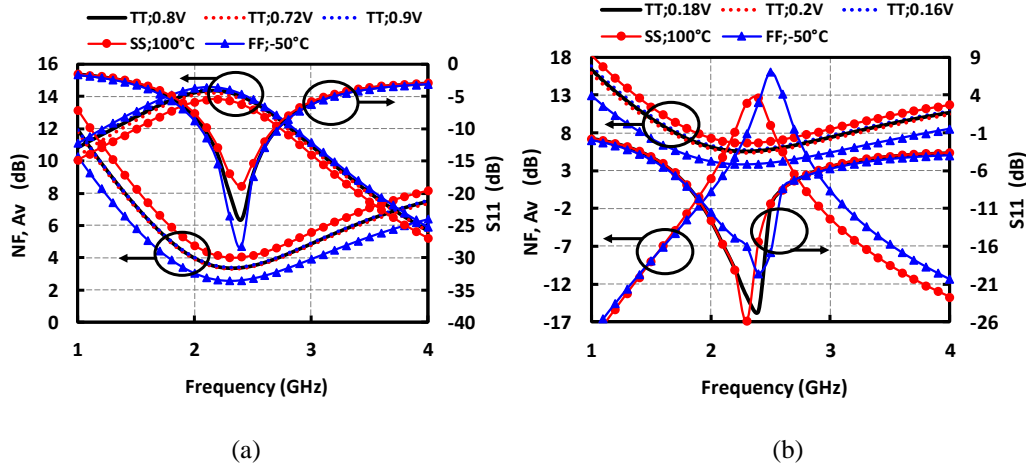
Figure 4-16: Corner simulations of (a) current-reuse LNA, (b) ULV LNA

The overall performance of the proposed LNAs is compared with that of recently published ULP LNAs in Table 4.3. The proposed LNAs consume much less power compared to state-of-the-art LNAs and far exceed the requirements of WSN standards such as BT-LE [49]. The current-reuse LNA has also a very competitive NF, while the ULV LNA has a NF comparable to other ULV designs (with supply below 0.5 V), the only exception being the LNAs in [60,61]. Using very

advanced technology of 16nm FinFET, the LNA in [60] is suppled at only 100 mV and shows NF of 3dB and it consumes just 44µW. Nonetheless, the dissipated power of the ULV LNA is 33% less and voltage gain and IIP3 are higher. Compared with [54], which is the second lowest power LNA reported, our designs exhibit equal or lower NF, better IIP3 and half the dissipated power. To evaluate the overall performance of the proposed LNAs we use a classic figure of merit (FOM), defined as:

$$FOM = \frac{IIP3(mW)\,Gain(lin)}{(F-1)\,Pdc(mW)} \qquad (4\text{-}22)$$

Due to the extremely low dissipated power and low NF, both our designs have the highest FOM compared to the all previously published works reported in Table III. For fair comparison, it should be mentioned that while [50] [51] [54] [55] and [60] report measured results, this work, together with [52] [59] [61] and [62] only report simulation results. Furthermore, on given power consumption, the proposed current-reuse LNA represents the better NF, higher sensitivity and less estimated area compare to the ULV LNA. However, if an ultra-low supply voltage is required, the proposed ULV LNA demonstrates an overall competitive performance.

Table 4-3: Performance Summary and comparison with State-of-the-art LNAs

	Current-reuse	ULV LNA	[50]	[51]	[52]	[54]	[55]	[59]	[60]	[61]	[62]
Freq(GHz)	2.4	2.4	1	0.1-1	0.1-1.6	2.4	0.6-3.1	5	2.4	2.14	3.1-10
Tech (nm)	40	40	130	130	90	130	130	180	16	65	90
Vdd (V)	0.8	0.18	1	1.2	1	0.4	0.4	0.6	0.1	0.6	0.4
Pdc (µW)	**30**	30	100	720	425	60	160	1300	44	402	410
NF (dB)	**3.3**	5.2	3.9	4	5.5	5.3	4.5	3.5	3	2.8	4.5
Gain (dB)	14.2	14	16.9	10.2	10.5	13.1	13	12.5	10.8	9.2	15
IIP3 (dBm)	-11.6	-8.6	-11.2	-13	-4.5	-12.2	-12	-2	-18	NA	-7
FOM	**10.4**	10	3.65	0.39	1.1	1.9	0.97	2.11	1.58	NA	1.5
S/M	**S**	S	M	M	S	M	M	S	M	S	S

S/M: Simulation / Measurement

5 Chapter 5

Design of Ultra-Low Power Receiver for Bluetooth Low Energy in 22 nm FD-SOI

5.1 Introduction

In the past a lot of research has gone into providing radio communication with increasing data rates, especially since the introduction of the smartphone. Lately, however, there is highly demand to provide connectivity with portable devices and sensors, that can be all around us. Such connectivity is sometimes referred to as the internet of things (IoT). Here, the challenge is to provide basic connectivity at very low power consumption. Wireless sensor networks (WSN) is an example of the application of ultra-low power radio communication. A wireless sensor network consists of small sensors combined with a radio transmitter/transceiver.

The sensor nodes are able to communicate with each other and perform together an intelligent task based on the environmental conditions obtained by a set of sensors. Sensor nodes could be placed randomly in a targeted area, which could be for example a building, a cultivation field, a road, an ocean or a forest. The sensors sense the environmental conditions (such as temperature, light, vibration, location, gas and chemical composition) and store them. A simplified WSN layout is shown in Fig.1. As shown in the figure, there is a special type of node called gateway node to collect the data from multiple sensor nodes and process them together. A sensor node communicates its data to a gateway node either directly or via another sensor node(s). For some applications, the gateway nodes collect all data and take decisions based on the data. In some other applications the gateway node transmits the data to a base station controlled by a human or a machine. The position of the sensor nodes can be either random, predetermined or dynamic, depending on the applications and the available hardware. WSNs have the potential to be applied in a variety of applications such as medical, disaster management and prevention, home automation, tracking and remote sensing. The application area is huge and one can imagine numerous new applications which will improve human life or prevent disasters in the future. These applications are possible in the future provided that low energy consuming, tiny, cheap and scalable sensor nodes with a robust sensor network are available.
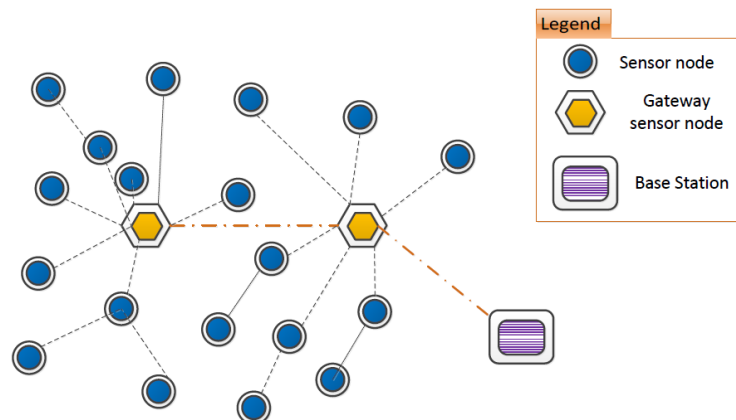
Figure 5-1: A typical wireless sensor network

5.2   Literature Review:

There has been tremendous effort to shrink the dissipated power in the receiver for Bluetooth Low Energy in the recent years [38,39,42,43,47,69]. Minimizing power can be generally categorized into following approaches or even combination of them.

1) Using ultra-low supply voltage [38-39]
2) Re-using current into different blocks [42,43,69]
3) Employing passive blocks [39,47]

One of the effective methods to reduce the power is to drastically reduce supply voltage. It is demonstrated in [38] that entire receiver chain can operate with supply voltage of 300 mV. Forward body biasing technique is utilized to perform a good functionality of MOS devices. Coupled transformer is the other interesting introduced technique to keep using low supply voltage. Fig.5.2 represents the RF blocks of the receiver. Even though it achieves very good NF of 6 dB with low supply voltage, the consumed power is still high, 1.6 mW, and linearity performance degrades heavily due to primarily using two stage LNA and also the limited headroom (IIP3 of -21dBm). Furthermore, employing 4 transformers drastically increase chip area (2.5mm^2).
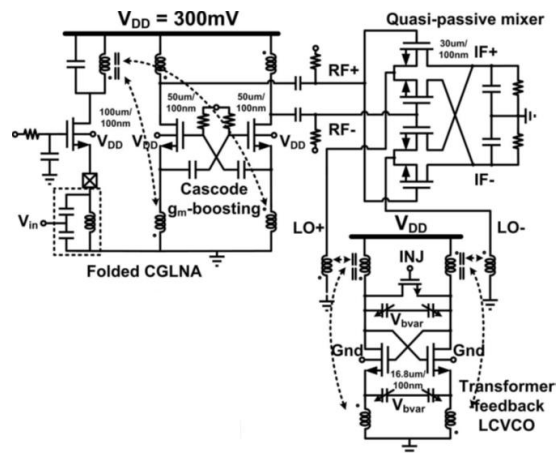
Figure 5-2: schematic of the frontend [38]

It is very interesting to use harvested energy from environment to drastically reduce the power. An ultra-low voltage and very low power receiver is demonstrated in [39]. The block diagrams of the entire receiver are represented in Fig.5.3. Power manager boosts 0.18 V supply voltage by almost factor of three and enabling to derive gate of transistors. Implementing passively quadrature generation as one of the power hungry blocks in the RX results in significantly saving power. Despite a RC-CR passive network is lossy in signal path, it does not dissipate power. The overall performance is acceptable, for instance IIP3 of around -12 dBm and NF of above 11 dB. The least

consumed power in the literature is reported and it is only 382μW, however it comes at the cost of employing 4 big inductors in the design leading to extensively high active area of 1.6mm^2.
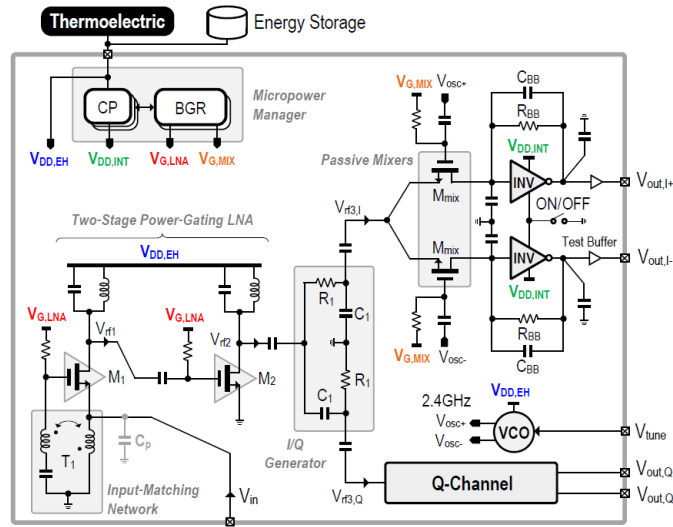
Figure 5-3: schematic of the frontend [39]

A 2.4GHz Zigbee receiver with no external component is represented in [69]. It uses current reuse approach for the main blocks (RF to BB functions) of receiver through a stacked architecture and a lower supply voltage in particular blocks. The entire receiver has an active area of 0.24mm^2, NF of 9 dB and IIP3 of -6 dBm. Even though bias current is recycled in several blocks, the power consumption is still as high as 1.7mW.
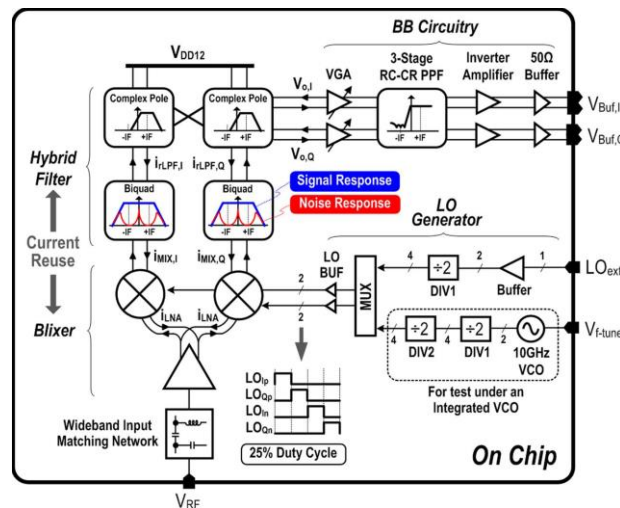
Figure 5-4: schematic of the frontend [69]

A highly linear low power Receiver for SoC coexistence application is presented in [42]. Thanks to the current reuse approach, a single shared DC bias is used between LNTA and the first stage

of both I and Q BB to save power. It shows an interesting IIP3 value of 6 dBm, however due to stacking 6 transistors, it requires supply voltage of 1.8 V and drawing 2.4 mA which makes this approach unattractive for ultra-low power application.
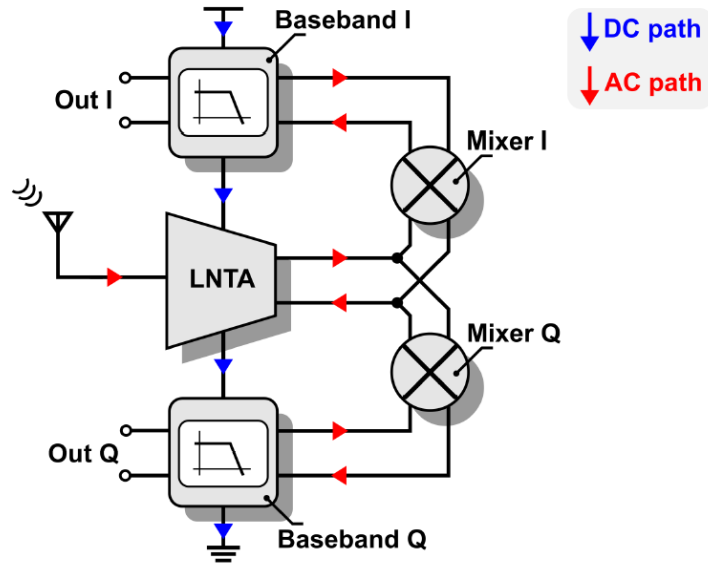
Figure 5-5: schematic of the frontend [42]
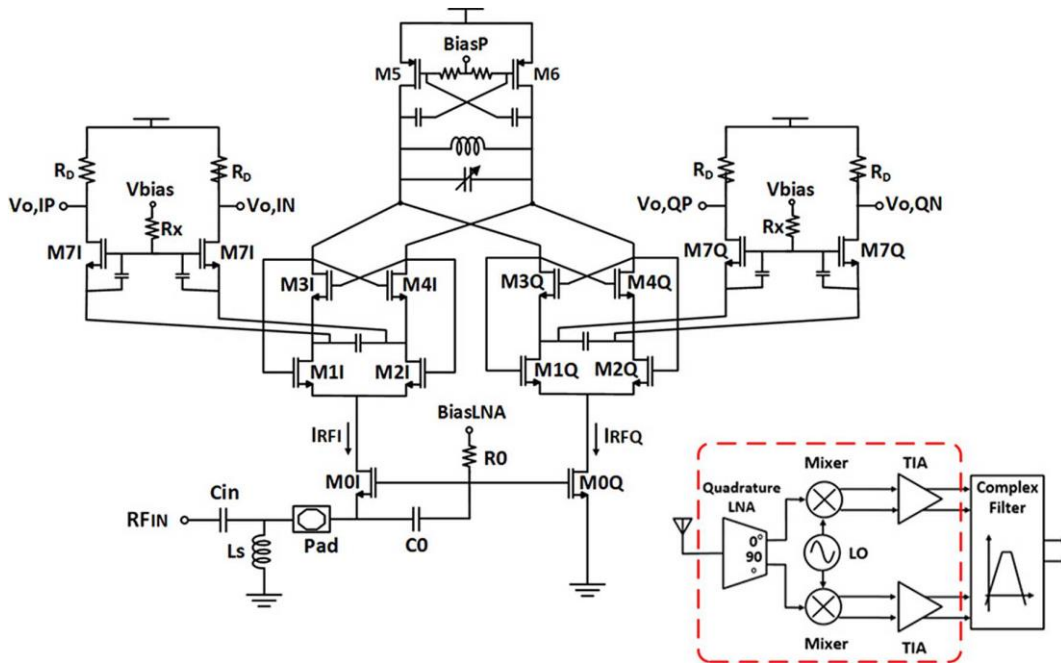
Figure 5-6: schematic of the frontend [43]

Another implementation of current reuse approach was presented in [43]. Sharing the DC bias between several blocks can potentially minimize the power consumption provided that using low supply voltage. Although in [42,69] similar concept was utilized, they required to increase the supply voltage to above 1.2V, leading to increasing power. In [43], however a sub-1V was used and results in consuming only 600μW for the whole receiver chain. Quadrature LNA was implemented and its DC bias was shared between mixer, VCO and TIAs. It is remarkable to bias all RF blocks with low supply voltage and single shared DC bias, however it causes weak isolation between stages and degrading the overall performance, for instance, NF of 15 dB and IIP3 of -16 dBm.

A mixer first receiver for ultra-low power application was proposed in [70]. In this work, LNA is removed and some voltage amplification (~10dB) is provided through passive LC network and effectively source impedance is boosted to have higher driving impedance for proper operation of passive mixer. By this technique, no power was dissipated in frond-end, however a higher power has to be consumed in baseband (BB) stage to reduce its noise contribution in the overall noise of chain. Power consumption of 550 μW under supply voltage of 0.85V was reported. IIP3 of -3 dBm was achieved thanks to the use of LNAless architecture and reporting NF of 9.6 dB.
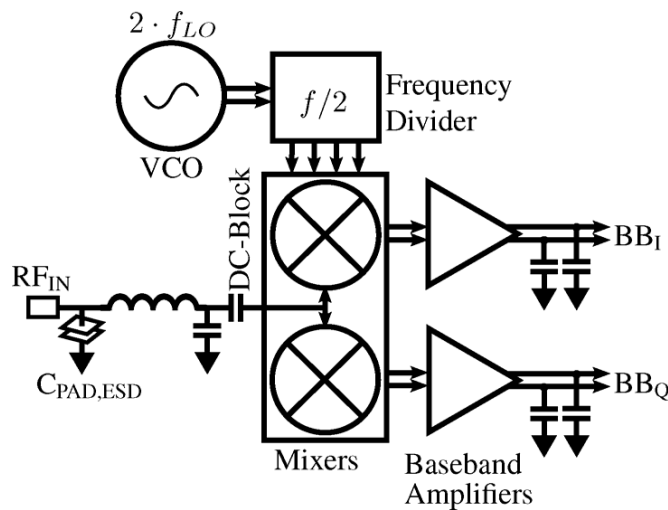
Figure 5-7: schematic of the frontend [70]

5.3   Transistor modeling and effect of body biasing on its characteristic:

To verify the feasibility of a 0.4V radio design, it is required to explore the characteristic of active device. A 22 nm FD-SOI process is chosen and due to targeting aggressively low voltage design, low-V_{TH} transistors are reasonable choice. The typical V_{TH} of nFET device is around 180 mV and it can be lowered thanks to forward biasing of back (FBB) gate. Fig.5.8(a) represents effect of V_{TH} while sweeping Vgs. As can be seen from Fig.5.8(a), biasing back gate, for instance, at V_{DD} (0.4V)

while the source is grounded, V_{TH} can be reduced by 25%. Moreover, the same argument is valid for overdrive voltage, V_{od}, of the active device and V_{od} increases from 230 mV to 260 mV while Vgs is at 0.4V and applying forward biasing, shown in Fig.5.8(b).

(a)   (b)
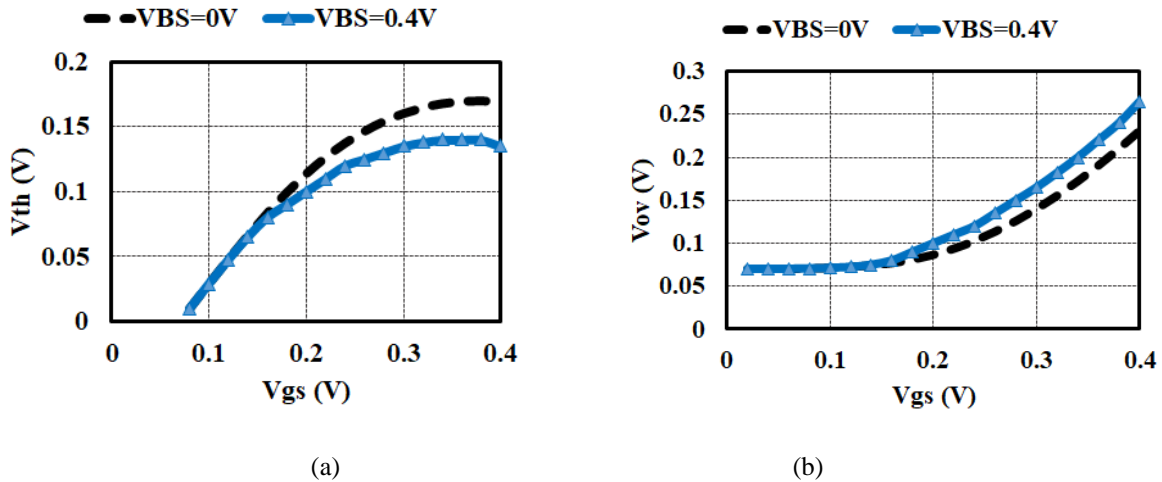
Figure 5-8: simulated (a) Vth, (b) Vov versus Vgs for different V_{BS} (Published with the permission of Global Foundries)

Fig.5.9 is extracted by varying Vgs from 0 to 400 mV while biasing V_{BS} at either 0 or 0.4V (dash and solid line respectively). Once V_{BS} is at 0.4V, V_{TH} decreases and smaller voltage is required at gate node to form the channel. In fact, with equal Vgs, applying FBB leads to increasing bias current and eventually enhancing the device g_m. The intrinsic gain of nFET device versus Vgs is shown in Fig.5.9(a) and it is almost equal at deeply inversion region compare to the employing forward back gate biasing, however it can be slightly reduced at higher Vgs. One of the important parameters of active device operating at radio frequency is cut-off frequency. As can be clearly seen from Fig.5.9(b), with constant Vgs, just by forward biasing of back gate, the device ft can be significantly enhanced, for instance, at Vgs=200 mV, from 100 GHz to 160 GHz in which makes it feasible low voltage design. By contrast, on the given Vgs, g_m/I_d of active device is slightly reduced as shown in Fig.5.9(c). It is motivating to bias transistors in deeply weak inversion to maximize current efficiency, g_m/I_d, weak inversion, however, represents relatively poor frequency response. Therefore, the product of the current efficiency and cut-off frequency can be considered as the proper Figure-of-Merit (FoM) for RF design. FoM versus Vgs is depicted in Fig.5.9(d) and the highest peak of the FoM is shifted toward lower Vgs from 320 mV to 260 mV thanks to the forward back gate biasing of active device. This phenomenon is even more appreciable at drastically lower Vgs, for instance, at Vgs=100mV, FoM is 0.9 T versus 0.35 T for V_{BS}=0V and V_{BS}=0.4V respectively which certifying the beneficial of the forward back gate biasing in this technology.
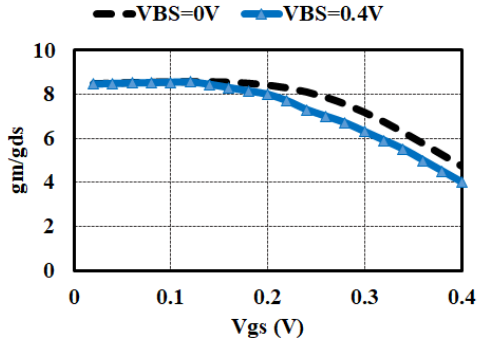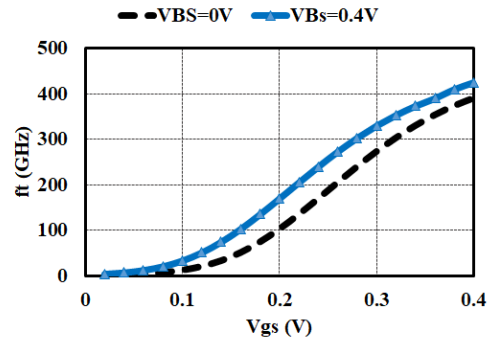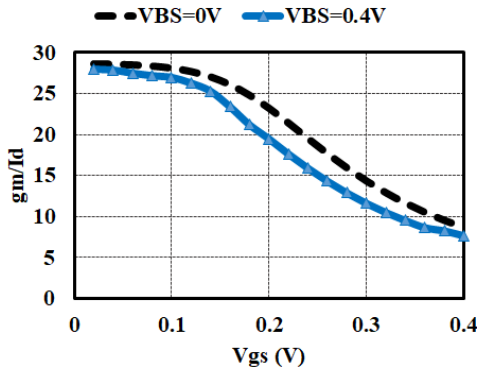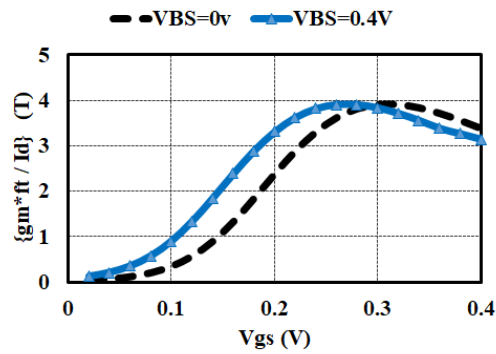
Figure 5-9: simulated (a) intrinsic gain, (b) ft, (c) g_m/I_d, (d) FoM of nFET device versus Vgs
(Published with the permission of Global Foundries)

5.4 Architecture Consideration:

One step down-conversion architecture is appropriate for low power operation. There are well known problems of higher flicker noise, even order distortion and DC-offset which makes zero IF architecture unattractive for this application, therefore low-IF is the most suitable architecture. The proposed current mode architecture is shown in Fig.5.10 and a single-ended 2.4 GHz RF input voltage is converted to the current signal by LNTA and followed by the single balance passive mixer loaded with transimpedance amplifier (TIA). To minimize the required bandwidth of IF amplifier and saving power, low IF frequency is preferable. However, the lower end of IF frequency has to be chosen above the flicker noise corner which requires higher selectivity in channel selection filter. On the other hand, to increase image rejection ratio and improving demodulator performance requires choosing high IF, for instance 3 MHz or more, at the cost of consuming further power to perform channel selection filter. Hence, according to the blocking mask for BLE standard shown in [47], a low-IF of 2 MHz is chosen leading to the smaller in band interference to be image signal and it can be easily rejected using ultra low power complex filter [43].
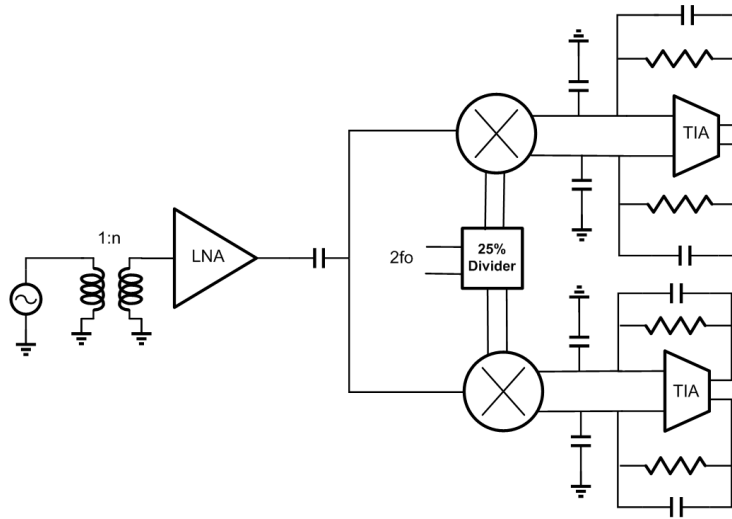
Figure 5-10: block diagram of the frontend

5.5   Frond-end Design:

The schematic of the proposed RF front-end is shown in Fig.5.10. To allow operation from only 0.4 V supply voltage, following techniques are utilized in our RF front-end. Firstly, current reuse is extensively used in each block to improve voltage efficiency. Secondly, forward back gate biasing is used to lower threshold voltage of devices. There is no considerable leakage current thanks to using small supply voltage. Thirdly, biasing transistor in the vicinity of weak and moderate inversion region to optimize g_m/I_d with an acceptable ft.

5.5.1   LNA Design and Consideration:

In CG amplifier, input power matching is restricted to the device g_m which makes this topology power hungry. However, boosting source impedance can be considered as one of the popular methods to reduce the dissipated power in CG amplifier. Basically, a step-up transformer (with a ratio of 1:T) can lower the consumed power in CG amplifier thanks to the boosting source impedance by a factor of T^2 and this impedance transformation is even more beneficial compare to the LC transformation network since transformer can be potentially wideband with a less sensitivity to the loss of inductor. Furthermore, transformer can be also utilized as a passive gain boosting between gate-source of active device and results in reducing the power.
The basic idea of proposed LNTA is to simultaneously merge scaling the source impedance and also employing passive gain boosting and shown in Fig.5.11(a). The primary of transformer (as the input of LNA) is AC coupled to the gate of active device, on the other hand, the secondary is directly connected to the source of active device. Considering an ideal transformer with K=1, the source voltage is enlarged by a factor of T, whilst the gate-source is enhanced by 1+T with respect to the input.
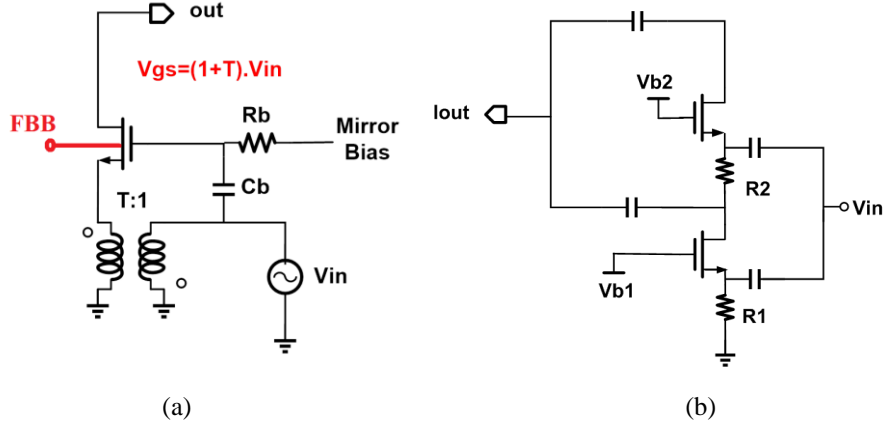
Figure 5-11: (a) gm boosting, (b) current reuse concepts of proposed LNTA

The G_m and input impedance can be computed as follows:

$$G_m = (1+T)g_m \qquad\qquad (5\text{-}1)$$

$$Z_{in} = \frac{1}{g_m T(1+T)} \qquad\qquad (5\text{-}2)$$

With a 1:1 transformer (T=1), the device g_m needs to be $1/(2R_s)$ for impedance matching and G_m is the same as with a CG amplifier and effectively doubling the current efficiency. Considering T=2, the required device g_m to perform input power matching is $1/(6R_s)$ and G_m is one half that of a CG amplifier that carries six times the current. Modelling transformer losses as a resistance R_{loss} at its secondary, the LNA noise factor is:

$$F = 1 + \frac{\gamma T}{1+T} + \frac{T^2 R_s}{R_{loss}} \qquad\qquad (5\text{-}3)$$

where γ is the MOSFET noise parameter, the second term represents thermal noise of transistor. Ignoring loss of transformer, for T=1, F=1+γ/2; for T=2, F=1+2/3γ and if T>>1, F eventually converges to 1+γ (i.e. usually less than 3dB), whilst the required device g_m (and hence power consumption) scales down as T^2. In contrast, as T enlarges, two issues should be taken into account, loss of transformer is not negligible, and simultaneously the G_m scales down (as 1/T), leading to the noise of the subsequent stages in the receive chain to be more important. Consequently, it is highly valuable to employ an additional power saving technique. To drop further power dissipation, more devices can be stacked to re-use bias current and effectively improving voltage efficiency. Fig.5.11(b) shows the current reuse technique for stacked CG amplifier. In fact, the signal is AC coupled to the both sources of NMOS transistors while they share the same bias current resulting an equivalent $G_m = g_{m,1} + g_{m,2}$. This scheme halves the DC current for the same input impedance and NF. In this scheme, the essential signal isolation is achieved by interposing

R$_2$ between two stacked CG amplifier and it has to be big enough for proper operation. Thanks to the current mode operation of receiver, the LNTA will be loaded with low impedance associated with passive mixer followed by trans-impedance amplifier, therefore the output signal current of the bottom transistor does not excursion to source of stacked transistor. The minimum supply voltage required by the voltage-stacking scheme is one of the main concerns to cope with. The value of the resistors has to be reduced once dropping the supply voltage, causing not proper functionality and also increasing NF. In the proposed LNTA, the gate and source of stacked transistors are AC coupled to the primary and secondary of transformer respectively which enables to utilize the privilege of the proposed passive gain boosting to further reducing the power. In addition, due to the driving one of the sources of active devices with transformer, it leaves plenty of voltage headroom to be utilized to further reducing the DC current by stacking more devices. One PMOS device can be added on the top of the stacked NMOS transistor resulting in reducing much further DC current. The actual schematic of proposed LNTA is depicted in Fig.5.12. The two NMOS and one PMOS share the same bias current and have the same gate-source voltage signal and all devices are biased in vicinity of weak and moderate inversion to optimize g_m/I_d with an acceptable f$_t$. Capacitive combiner adds the output signal current. Supposing all devices have the same g$_m$, the total equivalent G_m is equal to three times the device g_m. Hence, the required device g$_m$ to perform input impedance matching is only $1/(18R_s)$. Consequently, LNTA bias current can be drastically reduced with small dropped voltage across the bias and isolated resistor. For a given headroom for both resistors, the isolated resistor is considered to be larger than the bias resistor to significantly enhance the driving impedance of the TIA due to the lack of cascode devices in LNTA. This enables to consume much less power in the first stage of TIA with an acceptable noise degradation. On the other hand, since the source impedance is boosted to 200Ω, the bias resistor is chosen 1KΩ (i.e., only 5 time bigger), leading to an acceptable noise degradation at the input. Thanks to applying forward back gate biasing to all devices, threshold voltage can be reduced and the whole circuit can operate properly even with supply voltage as low as 0.4V. The noise factor of the proposed LNTA including loss of transformer is given as follows:

$$F = 1 + \frac{\gamma T}{1+T} + \frac{T^2 R_S}{R_{loss\_xfmr}} + \frac{T^2 R_S}{Rc} + \frac{T^2 R_S}{R_L}$$

(5-4)
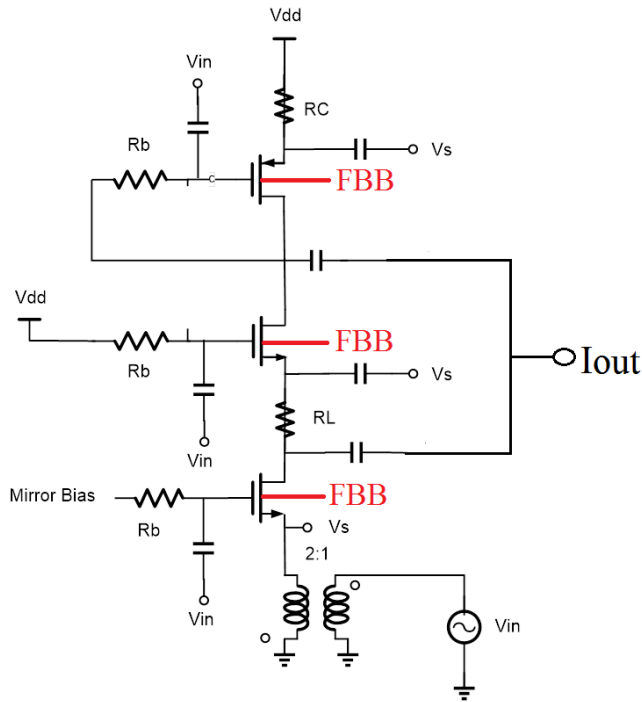
Figure 5-12: Schematic of proposed LNTA

5.5.2   Passive mixer:

A trade-off between linearity and noise is inevitable specially if it is amid to minimize the consumed power. A passive mixer is an attractive choice and consumes no DC current and representing superior noise and linearity once the LO driver is relatively large at the gate terminal. Due to the single-ended LNTA output, a single balanced mixer is used and it is also advantageous with respect to the double balance to reduce the dissipated power in LO generation path because of having smaller capacitor and leading to the less loading effect. The low pass input impedance of the BB can be frequency translated to the RF side and form band pass characteristic and reducing the interference amplitude and improving linearity. The other privilege of passive mixer is to have a slight or no flicker noise which is very desirable in direct conversion receiver.   Moreover, very low insertion loss can be achieved by quadrature sampling provided that there should be no overlapping between the conduction period of each path. This issue can be solved by providing LO signal with 25% duty cycle.

5.5.3   BB stage:

The TIA stage simultaneously serves as mixer load, converting current to the voltage and also anti-aliasing filter for the subsequent stage. In order to flow almost all current provided by the mixer into the feedback RC, the active-RC TIA stage has to provide low impedance at the mixer output. This can guarantee the linearity of the mixer due to the experiencing small voltage swing. This statement is only valid if the operational transconductance amplifier (OTA) has enough gain at the highest possible frequency. In addition, the noise of the TIA has to be small and therefore its input transconductance should be as high as possible. With limited power budget allocated to the baseband, complementary single stage inverter based OTA is preferable with twice transconductance (g_m/I_d) efficiency compare to the conventional OTA. To enhance the output impedance, the device gate length is chosen 5 time bigger the minimum value allowed with given technology. Moreover, due to using relatively large devices, it preserves the low flicker noise and also certifying good matching. A simple first order low pass RC feedback is placed around of OTA to filter unwanted interfere at higher frequency and relaxing the linearity and noise requirement of following stage, for instance, complex filter for selecting the channel. Due to creating a feedback loop, one of the issues which has to be carefully considered is the stability of common mode loop. Either common mode gain has to be less than one for unconditionally stability purpose or if it has certain gain with good phase margin, then its gain has to be low enough with respect to the differential mode. In inverter based OTA, the common mode gain is typically comparable with differential one, therefore, to drastically reducing common mode gain, the load and input transconductance has to be different in two cases, i.e., making different transfer function. The NMOS input transistors are degenerated with tail current source, therefore in common mode, its gm is heavily suppressed with big resistor, then PMOS transistors are divided into two sections such that one of them is also degenerated with resistor and acting as input transconductance and the other one acts as diode connected load with big resistor placed between its drain and gate. Hence, the output impedance is approximately 50 KΩ and $1/g_{m6}$ in differential and common mode respectively. So, it enables to attenuate common mode signal and amplifies the differential signals. To have good compromise between TIA noise and common mode rejection, all the current of NMOS transistor is almost equally recycled in both PMOS transistors. Fig.5.13 shows the schematic of the TIA and the differential and common mode gain can be computed as follows,

$$AV_{DIFF} = (g_{m2} + g_{m4}).R_L \qquad (5\text{-}5)$$

$$AV_{CM} = (\frac{g_{m2}}{1 + 2r_{o7}g_{m2}} + \frac{g_{m4}}{1 + 2R_b g_{m4}})(\frac{1}{g_{m6}}) \qquad (5\text{-}6)$$

Where the r_{o7} is output impedance of tail transistor. According to (5-6), common mode gain is always less than one and ensuring unconditionally stability purpose.
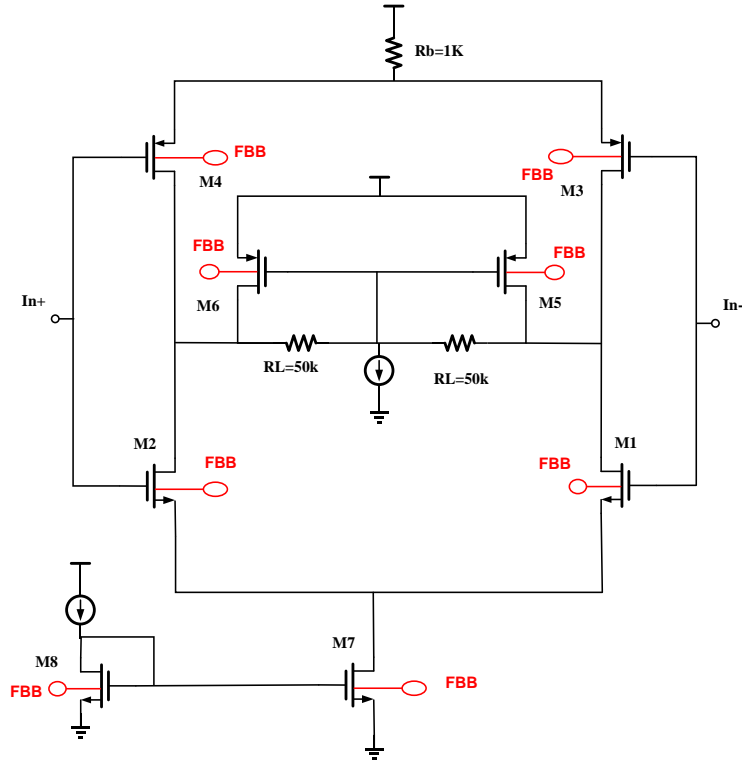
Figure 5-13: Schematic of TIA stage

5.5.4   LO Generation:

One of the most significant sources of dissipating power in RF circuit is LO generation due to the driving relatively large passive mixer. There are a two common approach to generate quadrature LO signals by means of quadrature oscillator or with single VCO operating at twice frequency followed by frequency divider. Quadrature VCO suffers from two important issues. Firstly, two VCO core is required and at least one inductor is need for each of them leading to the drastically increased chip area which is not attractive for low cost design. Secondly, strong interfere can potentially cause injection locking if there is no sufficient isolation between VCO and RF circuits, in particular in direct conversion receiver. Therefore, it is especially required to add buffer between QVCO and RF circuits leading to the consuming extra power. On the other hand, divider based solution solves drawbacks of QVCO. It requires only one core VCO operating at twice frequency leading to the smaller inductor and drastically reduced chip area and it is well immune with respect to the injection locking due to operating at the twice frequency. It is also interesting to point out the consumed power in the divider is indeed almost close to the dissipated power of buffer circuit used in the purpose of improving isolation between QVCO and RF circuits. As a consequence, divider based solution is chosen to meet all considerations of low power design.

5.5.5   VCO Design:

Voltage controlled oscillator (VCO) can be considered as one of the power hungry blocks in RF transceiver. So, it is compulsory to employ the most power efficient solution to minimize its power. Class-C and complementary Class-B VCO architectures are highly efficient and frequently being used in RF transceiver. Specifically, complementary Class-B demonstrates a double efficiency compare to the traditional single pair VCO. On the other hand, by forcing switching pair in traditional Class-B to operate in Class-C, bias current can be ideally saved as much as 36% while achieving the same phase noise performance. Hence, complementary Class-C VCO seems to be a very good choice to minimize the power. Robust start-up is one of the issues in Class-C VCO which needs to be carefully taken into consideration. One possibility is to use hybrid architecture in [71] by placing Class-B switching pair in parallel to the Class-C and forcing a robust start-up even with low gate bias voltage for the two Class-C transistors. However, it represents lower efficiency with respect to the pure Class-C VCO since the required bias for start-up is considerably higher than steady-state value. This issue is even more noticeable when VCO needs to operate with lower supply voltage. To solve the start-up issue with reduced supply voltage, an elegant approach was proposed in [72] by means of negative feedback performed by a current mirror which adjust the biasing gate of transistor to keep the current consumption at the desired value. Moreover, removing even the tail current source, the oscillator maximizes the oscillation amplitude without deteriorating the supply-pushing performance. Additionally, an improved version of that design was proposed in [73] using a complementary Class-C VCO to improve the efficiency. A high swing complementary Class-C is chosen and by applying forward back gate biasing (FBB) to the all transistor, threshold voltage of devices can be reduced, therefore it is plausible to operate with only single supply voltage as low as 0.4V for the all blocks. The schematic of the VCO is shown in Fig.5.14. The two cross-coupled pairs M1/M2 and M3/M4 operate in Class-C and provides negative resistance to restore the energy losses in the resonant load. The DC current is set by current mirror and it is composed by M1/M2 and M1b/M2b and ensuring a robust start-up, while its value drops in steady-state compare to that of in start-up value and maximizing output swing. The simulated waveforms of the gate voltage of transistors is plotted in Fig.5.15. Initially M_{1b}/M_{2b} is diode connected (at DC) and I_{bias} is mirrored by factor of N to the VCO core and facilitating safe startup. Average current of VCO core increases as the oscillator amplitude grows, hence C_B absorbs the excess current and leading to reducing V_{gateN} and forcing NMOS pair to operate in Class-C. Meanwhile, the center tap of the inductor is connected to gate of PMOS for biasing purpose. Since the common mode voltage of VCO is slightly above $V_{dd}/2$, it leads to pushing PMOS devices to the triode region in some portion of period as shown in Fig.5.15(b).
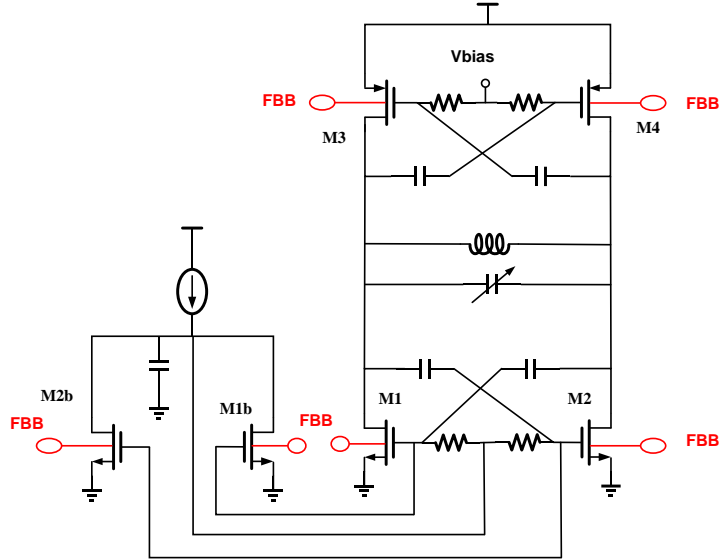
Figure 5-14: Schematic of VCO

(a)   (b)
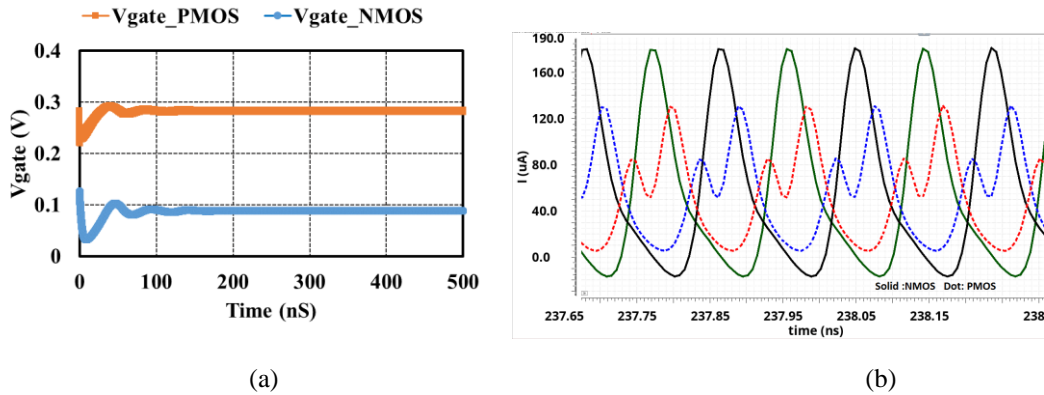
Figure 5-15: (a) Simulated the gate voltage, (b) simulated the drain current of core VCO

5.6   Simulation Results and Discussion:

The proposed receiver is designed in 22 nm FD-SOI technology and since the tape-out is scheduled to be done by early November 2017, so post layout simulation results is currently provided to validate the design. The entire receiver is designed to operate at 2.4 GHz with supply voltage as low as 0.4 V. As stated earlier, to reduce the threshold voltage of NMOS and PMOS devices, back gate is forward biased with 0.4 V and 0V respectively. The performance of the proposed LNTA is shown in Fig.5.16 while burning 28μA from 0.4 V supply voltage. As can be clearly seen in Fig.5.16(a), LNTA has NF of less than 4.5 dB at the desired frequency and its NFmin is 4.35 dB which certifying almost being noise matched. Noise circle at 2.4 GHz is plotted in Fig.5.16(b), even though the optimum source impedance corresponding to the NFmin is 75 Ω, wide variation of source impedance is acceptable to have NF of less than 5 dB. Additionally, the proposed LNTA has effective tranconductance of 6.8mS. The proposed LNTA is also relatively insensitive to the

supply voltage as shown in Fig.5.17, reducing or increasing supply voltage by 50 mV results in +/-0.2dB variation on NF while preserving very good input power matching. Due to the stacking several devices on the top of each other, stability of the LNTA needs to be investigated and as can be obviously seen from Fig.5.18, S12 is always below -24 dB and K factor is always above 2.2 and ensuring unconditionally stabile in all frequency.

(a)   (b)   (c)
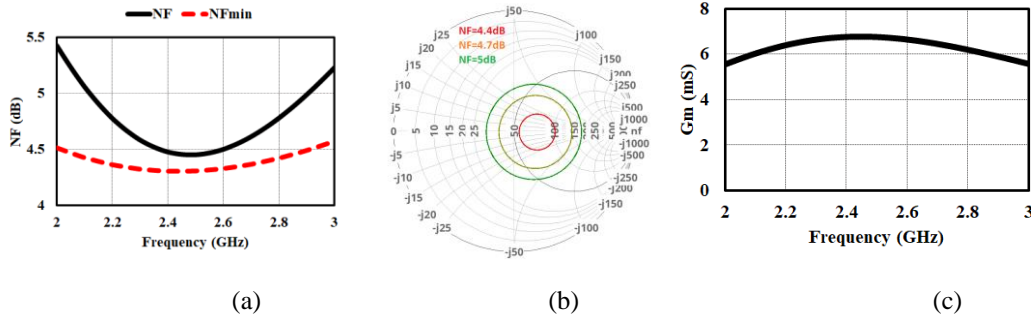
Figure 5-16: (a) Simulated the NF and NFmin, (b) simulated the Noise circle, (c) effective trans-conductance of proposed LNTA at 2.4 GHz

(a)   (b)
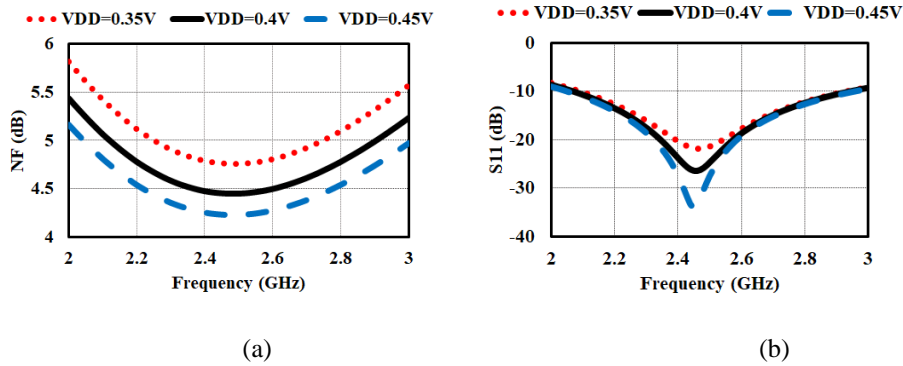
Figure 5-17: effect of Supply voltage on LNTA performance (a) NF, (b) S11

(a)   (b)
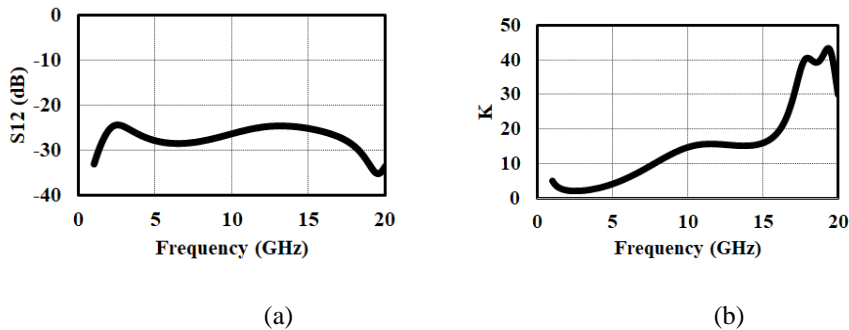
Figure 5-18: Simulated stability factor (a) S12, (b) K

Due to creating feedback loop around the TIA in the baseband stage, it is crucial to investigate the stability of loop. As can be seen in Fig.5.19(a), it has more than 10 MHz bandwidth and phase

margin of better than 100 degree in differential mode, however in the common mode, gain is always less than one and ensuring stability.
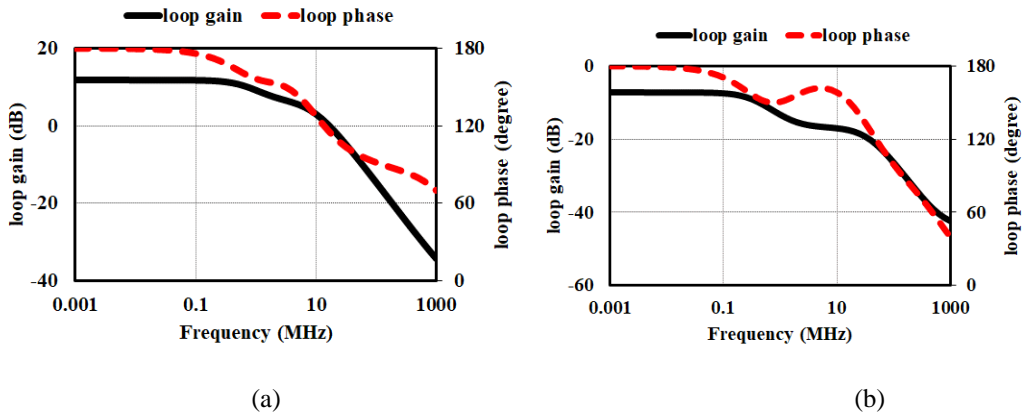
Figure 5-19: Simulated loop stability (a) Differential Mode, (b) Common Mode
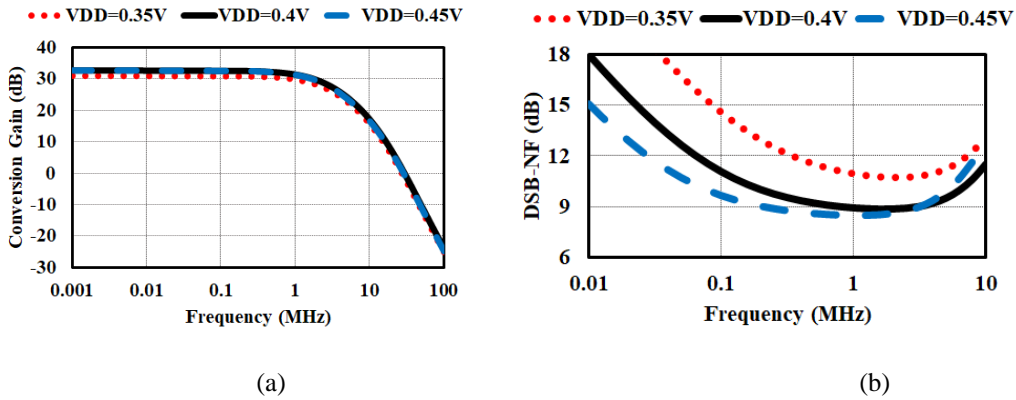
Figure 5-20: Effect of supply voltage variation (a) conversion gain, (b) DSB-NF

The proposed receiver has conversion gain of close to 33 dB and DSB-NF of 8.8 dB at IF of 2MHz while it operates at nominal supply voltage of 0.4V. Effect of supply voltage variation on conversion gain and DSB-NF is simulated and shown in Fig.5.20. As the supply voltage drops by 50 mV from the nominal value of 0.4V, 2 dB less gain is expected due to having less signal from LNTA and leading to the same degradation on DSB-NF. The performance of the proposed receiver when it operates with different supply voltage is tabulated in table 5.1.

Table 5-1: performance of proposed receiver for different supply voltage

Vdd (mV)	350	400	450
Idc_Total (uA)	190	255	335
Power (uW)	67	102	150
DSB-NF(dB)	10.8	8.8	8.5
Gain (dB)	30.9	32.7	32.7
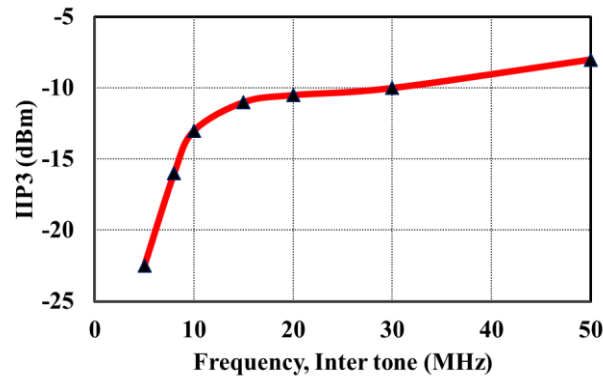
Figure 5-21: IIP3 of receiver versus offset frequency

The IIP3 simulation were performed by applying two tones at the receiver input with frequencies such that a IM3 product appears at in band frequency. In this case, the frequency of the down converted intermodulation product f_{IF} was kept constant at 1 MHz, while the two interfering tones were placed such that $f_{LO}+f_{IF}=2*f_{inner}-f_{outer}$ while varying f_{inner} and f_{outer} relative to f_{LO}. It can be observed from Fig.5.21, IIP3 is limited to the TIA nonlinearity for the in-channel and it starts to enhancing while moving further from the operating frequency and eventually it will be limited to the nonlinearity of LNTA for the out of band and will be saturated to -8 dBm for the two tones placed at 50 and 99 MHz.

To evaluate the tolerance to the strongest (-30 dBm) out of band blockers, conversion gain and noise figure simulation is performed while applying a tone at 100 MHz above the operating frequency of 2.4 GHz. As can be observed from Fig.5.22 (a), at the input power level of -25 dBm, conversion gain drops by 1 dB and the receiver will be desensitized by increasing further input power. On the other hand, to investigate the noise performance in the presence of blockers, located at 100 MHz offset, is applied to the receiver. Fig.5.22(b) represents the receiver NF with blocker for different power levels and it degrades by 1.2 dB and reaching to 10 dB for the -30 dBm input power level. According to the standard, NF has to be below 20 dB for the strangest out (-30 dBm) of band blocker and receiver NF can be degraded to 20 dB with power level of -20 dBm.
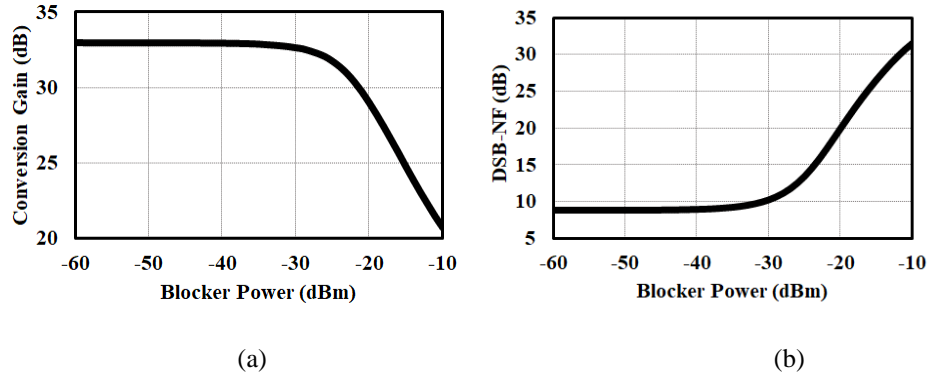
Figure 5-22: Simulated (a) conversion gain and (b) noise figure with out of band CW blocker at 100MHz above operating frequency
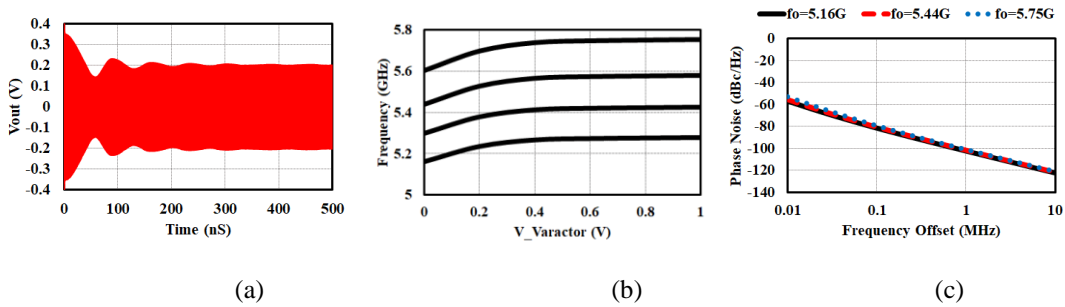
Figure 5-23: Simulated (a) output swing (b) tuning range, (c) phase noise of VCO

VCO has two bit to perform course tuning and a varactor for fine tuning. It consumes only 100 µA from supply voltage of 0.4 V. Fig.5.23(a) plots the output waveform of the VCO and it has differential peak swing of 200 mV. VCO can be tuned from 5.16 GHz to 5.75 GHz as shown in Fig.5.23(b). The minimum phase noise requirement for the BTLE application operating at 2.4 GHz is -102 dBc/Hz at offset frequency of 2.5 MHz. The simulated phase noise of VCO for different center frequency is shown in Fig.5.23(c) and its value in always better than -109.5 dBc/Hz operating at twice desired frequency which is much better the bear minimum requirement of the intended application while it operates with supply voltage as low as 0.4 V and consuming only 40 µW.

The designed VCO is centered at 5.45 GHz and has 11% tuning range. The simulated phase noise at offset frequency of 1 MHz versus RF frequency for different supply voltage is shown in Fig.5.24(a). It is expected as the supply voltage drops, due to the reducing output swing and also de-Qing tank, phase noise degrades specially at higher frequency, but it is always better than -100.5 dBc/Hz. On the other hand, considering Figure of Merit (FoM), it has very competitive FoM with respect to the high performance VCOs and its value is always better than 190 at nominal supply voltage of 0.4 V.

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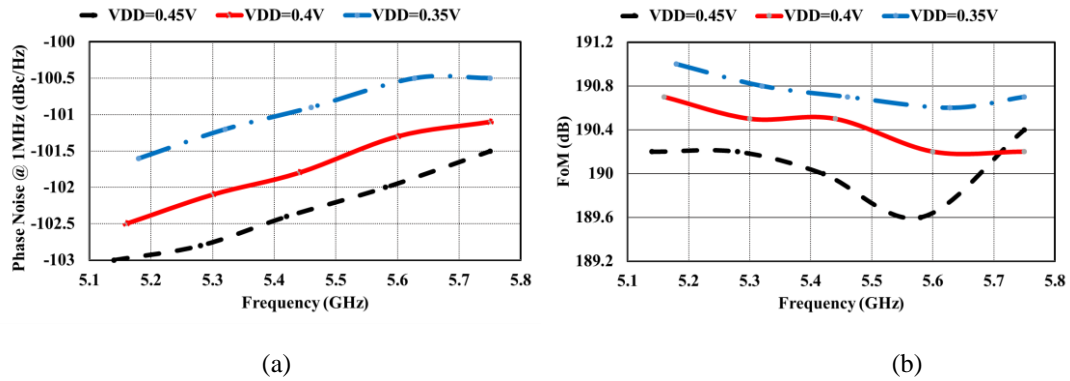
Figure 5-24: Simulated (a) phase noise at offset frequency of 1MHz and (b) FoM versus RF frequency for different supply voltage

(a)   (b)
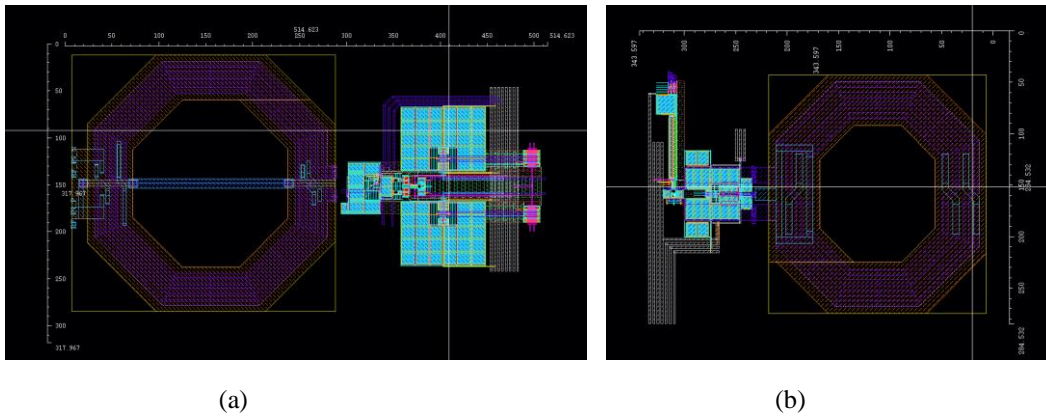
Figure 5-25: (a) layout of the proposed receiver, (b) layout of VCO

The layout of the proposed receiver excluding VCO is shown in Fig.5.25(a) and it occupies 0.15 mm^2. The VCO layout occupies 0.06 mm^2 as shown in Fig.25(b). The performance of VCO is summarized in Table 5.2 and compares it with relevant state-of-the-art for Pdc less than 500 µW. It represents the least power hungry VCO compare to the other works while it shows very competitive FoM. The designed VCO has also the lowest supply voltage with exception of [75], however our design consumes not even nearly three-time less power, but it also has almost 3 dB better FoM and much smaller occupied area.

Table 5-2: performance summary of ULP VCO and comparing with state-of-the-art

	This work	[74]	[75]	[76]	[77]
Technology (nm)	**22**	180	180	40	65
Vdd (V)	**0.4**	0.6	0.2	0.5	0.5
Power (μW)	**40**	120	114	480	330
RF freq. (GHz)	**5.16-5.75**	1.2-1.244	4.5	4-5	2.4-3.45
PN (dBc/Hz) @1MHz	**-102.5**	-121.6	-104	-139	-121.6
FoM	**190.7**	192.7	187	189.7	194.4
Area (mm^2)	**0.06**	0.55	0.29	0.14	0.2

The overall performance of the proposed receiver is compared with that of recently published ULP receiver in Table 5.3. The proposed receiver consumes much less power compared to state-of-the-art receivers and far exceed the requirements of wireless sensor network standards such as BT-LE [49]. The receiver has a lower or comparable NF to other ULP designs. It also represents better IIP3 with the exception of [70] in which using mixer first receiver solution to improve the linearity. Even though receiver in [39] operates with the lowest supply voltage (0.18V), it requires several on chip inductors to perform the functionality and biasing of active devices and leading to the drastically enhanced chip area. Thanks to employing forward back gate biasing and extensively utilizing current reuse scheme, the proposed receiver can operate with supply voltage as low as 0.4V with much smaller chip area, better NF and better linearity compares to the [39].

Table 5-3: performance summary of proposed receiver and comparing with state-of-the-art

	This work *	[43]	[70]	[53] ^	[39]
Technology (nm)	**22**	130	65	65	28
Vdd (V)	**0.4**	0.8	0.85	0.8	0.18
Power (μW)	**102**	600	550	400	382
DSB-NF (dB)	**8.8**	15	9.6	9	11.3
Gain (dB)	**32.7**	55	41	27.5	34.5
OOB-IIP3 (dBm)	**-8**	-16	-3	-21	-12.5
Area (mm^2)	**0.15**	0.25	0.15	0.1	1.6

* excluding VCO (VCO consumes 40 μW with 0.4 V supply), ^ using off-chip BB stage,

6 Conclusion

The increasing demand of speed data transfer capability in mobile smart phones is leading to more sophisticated and complex communication standards. The use of multiple bands and multiple antennas is becoming essential to satisfy the always more stringent requirements imposed by the new standards. The typical approach that uses external and bulky filters, adopted so far, is no more applicable due to the platform complexity and cost. Moreover, the scaling down technology could be potentially limited due to pins counting. A one chip wide-band transceiver able to manage all the different standards with few input-output pins would be the best solution. Generally, the out of band IIP3 of the receiver is limited to the linearity of LNTA. Hence, a high linearity LNTA is strongly required to enable removing bulky and off-chip components. A high linearity LNTA with 27 dBm IIP3 and capable of handling large blocker while requiring only 8 mA was presented. The circuit takes advantage of un-matching condition to improve both linearity and noise and requires no external components. To implement true SAW-less SDR architectures, more work is required. However, this is an important step in that direction. The proposed LNTA can be used is a SAW-less diversity receiver that includes fairly linear TX cancellation path to boost further the equivalent antenna-referred IIP3.

Internet of things (IoT) is gaining popularity as a medium of connectivity for many objects such as healthcare, weather, bio-electronic sensing, and security to provide more convenient user end services. Since large scale IoT application requires many sensor nodes to operate with limited power supply and small battery area, the total node power consumption must be kept as low as possible to maximize operation period. The wireless communication transceiver is an integral component of an IoT sensor node that tends to dissipate high power in its receiver (Rx) mode. Thus, ultra-low power (ULP) Rx can greatly extend the application of IoT technology to many areas by prolonging the IoT sensor node lifetime to several months or years with a miniature Li-Ion coin battery. A transformer-based passive g_m boosting technique for ultra-low power LNAs has been proposed. An ultra-low power ultra-low voltage LNA, powered from a 0.18 V supply, achieves in simulation 5.2 dB NF at 2.4 GHz and dissipates only 30 μW. Another design combines transformer-based passive g_m boosting with an efficient current-reuse topology. Powered from a 0.8 V supply the current-reuse LNA achieves in simulation 3.3 dB NF at 2.4 GHz and dissipates only 30 μW. Both LNAs demonstrate stable performance across +/-10% supply voltage variations. The proposed designs operate as low-noise transconductance amplifiers and are therefore suitable for integration in a passive-mixer based wireless receiver for wearable WSN applications with extend battery lifetime. Furthermore, thanks to extensively utilizing current reuse scheme and employing forward back gate biasing in advanced technology of 22 nm FD-SOI, it enables to design an ULP receiver for BTLE application. The proposed receiver consumes much less power

compared to state-of-the-art receivers and far exceed the requirements of wireless sensor network standards such as BT-LE. It can operate with supply voltage as low as 0.4V while consumes only 100 µW with much smaller chip area, better NF and better linearity compares to the-state-of-the-art.

Appendix I:

Table A.1: LTE standard operating bands

Operating Band	Uplink (User Equipment Transmits Base Station Receives)	Downlink (Base Station Transmits User Equipment Receives)	Duplex Mode
	$f_{UL,LOW} - f_{UL,HIGH}$	$f_{DL,LOW} - f_{DL,HIGH}$	
1	1920 MHz – 1980 MHz	2110 MHz – 2170 MHz	FDD
2	1850 MHz – 1910 MHz	1930 MHz – 1990 MHz	FDD
3	1710 MHz – 1785 MHz	1805 MHz – 1880 MHz	FDD
4	1710 MHz – 1755 MHz	2110 MHz – 2155 MHz	FDD
5	824 MHz – 849 MHz	869 MHz – 894MHz	FDD
6	830 MHz – 840 MHz	875 MHz – 885 MHz	FDD
7	2500 MHz – 2570 MHz	2620 MHz – 2690 MHz	FDD
8	880 MHz – 915 MHz	925 MHz – 960 MHz	FDD
9	1749.9 MHz – 1784.9,MHz	1844.9 MHz – 1879.9 MHz	FDD
10	1710 MHz – 1770 MHz	2110 MHz – 2170 MHz	FDD
11	1427.9 MHz – 1447.9 MHz	1475.9 MHz – 1495.9 MHz	FDD
12	699 MHz – 716 MHz	729 MHz – 746 MHz	FDD
13	777 MHz – 787 MHz	746 MHz – 756 MHz	FDD
14	788 MHz – 798 MHz	758 MHz – 768 MHz	FDD
15	Reserved	Reserved	FDD
16	Reserved	Reserved	FDD
17	704 MHz – 716 MHz	734 MHz – 746 MHz	FDD
18	815 MHz – 830 MHz	860 MHz – 875 MHz	FDD
19	830 MHz – 845 MHz	875 MHz – 890 MHz	FDD
20	832 MHz – 862 MHz	791 MHz – 821 MHz	FDD
21	1447.9 MHz – 1462.9 MHz	1495.9 MHz – 1510.9 MHz	FDD
22	3410 MHz – 3490 MHz	3510 MHz – 3590 MHz	FDD
23	2000 MHz – 2020 MHz	2180 MHz – 2200 MHz	FDD
24	1626.5 MHz – 1660.5 MHz	1525 MHz – 1559 MHz	FDD
25	1850 MHz – 1915 MHz	1930 MHz – 1995 MHz	FDD
26	814 MHz – 849 MHz	859 MHz – 894 MHz	FDD
27	807 MHz – 824 MHz	852 MHz – 869 MHz	FDD
28	703 MHz – 748 MHz	758 MHz – 803 MHz	FDD
29	N/A	717 MHz – 728 MHz	FDD
30	2305 MHz – 2315 MHz	2350 MHz – 2360 MHz	FDD
31	452.5 MHz – 457.5 MHz	462.5 MHz – 467.5 MHz	FDD
32	N/A	1452 MHz – 1496 MHz	FDD
33	1900 MHz – 1920 MHz	1900 MHz – 1920 MHz	TDD
34	2010 MHz – 2025 MHz	2010 MHz – 2025 MHz	TDD
35	1850 MHz – 1910 MHz	1850 MHz – 1910 MHz	TDD
36	1930 MHz – 1990 MHz	1930 MHz – 1990 MHz	TDD
37	1910 MHz – 1930 MHz	1910 MHz – 1930 MHz	TDD
38	2570 MHz – 2620 MHz	2570 MHz – 2620 MHz	TDD
39	1880 MHz – 1920 MHz	1880 MHz – 1920 MHz	TDD
40	2300 MHz – 2400 MHz	2300 MHz – 2400 MHz	TDD
41	2496 MHz 2690 MHz	2496 MHz 2690 MHz	TDD
42	3400 MHz – 3600 MHz	3400 MHz – 3600 MHz	TDD
43	3600 MHz – 3800 MHz	3600 MHz – 3800 MHz	TDD
44	703 MHz – 803 MHz	703 MHz – 803 MHz	TDD

Table A.2: Reference Sensitivity levels for some LTE bands

LTE Band	Reference Sensitivity (dBm)					
	1.4 MHz	3 MHz	5 MHz	10 MHz	15 MHz	20 MHz
1			-100	-97	-95.2	-94
2	-102.7	-99.7	-98	-95	-93.2	-92
3	-101.7	-98.7	-97	-94	-92.2	-91
4	-104.7	-101.7	-100	-97	-95.2	-94
5	-103.2	-100.2	-98	-95		
6			-100	-97		
7			-98	-95	-93.2	-92
8	-102.2	-99.2	-97	-94		
9			-99	-96	-94.2	-93
10			-100	-97	-95.2	-94
11			-100	-97		
12	-101.7	-98.7	-97	-94		
13			-97	-94		
14			-97	-94		
..						
33			-100	-97	-95.2	-94
34			-100	-97	-95.2	
35	-106.2	-102.2	-100	-97	-95.2	-94
36	-106.2	-102.2	-100	-97	-95.2	-94
37			-100	-97	-95.2	-94
..						

Appendix II:

To start analysis of linearity using Volterra series, initially defining Vs, the voltage at the source node of transistor, as the intermediate variable, and express the relation between Vs and Vin up to 3rd-order as:

$$V_s \approx A_1(s_1) \circ V_{in} + A_2(s_1, s_2) \circ V_{in}^2 + A_3(s_1, s_2, s_3) \circ V_{in}^3 \qquad (A.1)$$

Then by writing KCL equation for this circuit, we have:

$$i_d = \frac{V_S - TV_{in}}{T^2 R_s} \qquad (A.2)$$

$$V_{gs} = -\frac{1+T}{T} V_S \qquad (A.3)$$

To obtain the expressions for the 1st, 2nd-, and 3rd-order Volterra kernels $A_1(S_1)$, $A_2(S_1, S_2)$, $A_3(S_1, S_2, S_3)$, we substitute (4-21), (A.1) and (A.3) into (A.2) and cancel out Vs. To simplify calculation, it is assumed that passive components resonate at desired frequency and that the impact of parasitic capacitors is negligible, leading to frequency–independent intermodulation terms.

To get $A_1(S_1)$, we assume a single input tone and equating equations

$$-g_{m1} \frac{1+T}{T} A_1(s_1) \circ V_{in} = \frac{A_1(s_1) \circ V_{in} - TV_{in}}{T^2 R_S} \qquad (A.4)$$

Therefore, the first order Volterra kernels can be easily obtained as follows:

$$A_1(s_1) = \frac{T}{1 + (1+T) T g_{m1} R_S} \qquad (A.5)$$

Repeating previous procedure while applying two tone to the input results in,

$$-g_{m1} \frac{1+T}{T} A_2(s_1, s_2) \circ V_{in}^2 + g_{m2} \left(\frac{1+T}{T}\right)^2 A_1(s_1) A_1(s_2) \circ V_{in}^2$$
$$= \frac{A_2(s_1, s_2) \circ V_{in}^2}{T^2 R_S} \qquad (A.6)$$

and after simplifying, the second order Volterra kernels can be achieved as follows:

$$A_2(s_1, s_2) = \frac{g_{m2}(1+T)^2 R_S A_1^2(s_1)}{1 + (1+T)Tg_{m1}R_S} \tag{A.7}$$

For the third order coefficient, it is required to apply three tones to the input leading to,

$$-g_{m1}(\frac{1+T}{T})A_3(s_1, s_2, s_3) \circ V_{in}^3 + 2g_{m2}(\frac{1+T}{T})^2 \overline{A_1(s_1)A_2(s_1, s_2)} \circ V_{in}^3$$

$$-g_{m3}A_1(s_1)A_1(s_2)A_1(s_3) \circ V_{in}^3 = \frac{A_3(s_1, s_2, s_3) \circ V_{in}^3}{T^2 R_s} \tag{A.8}$$

Therefore,

$$A_3(s_1, s_2, s_3) = \frac{2g_{m2}\overline{A_1(s_1).A_2(s_1, s_2)}(1+T)^2 R_s - g_{m3}A_1^3(s_1)T^2 R_s}{1 + (1+T)Tg_{m1}R_s} \tag{A.9}$$

Now, expressing output current with respect to the input voltage as follows,

$$i_d \approx G_1 \circ V_{in} + G_2 \circ V_{in}^2 + G_3 \circ V_{in}^3 \tag{A.10}$$

By substituting (A.1) and (A.10) into (A.2), we have:

$$-g_{m1}\frac{1+T}{T}A_1(s_1)V_{in} = G_1 V_{in} \tag{A.11}$$

And the first order nonlinearity coefficient can be given as,

$$G_1 = -g_{m1}\frac{1+T}{T}A_1 \tag{A.12}$$

Applying similar procedure to obtain the second and third order nonlinear coefficients can be extracted as,

$$G_2 = -g_{m1}\frac{1+T}{T}A_2 + g_{m2}\left(\frac{1+T}{T}\right)^2 A_1^2 \tag{A.13}$$

$$G_3 = -g_{m1}(\frac{1+T}{T})A_3 + 2g_{m2}(\frac{1+T}{T})^2\overline{A_1 A_2} - g_{m3}A_1^3 \tag{A.14}$$

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