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Ph.D. Thesis

Design And Optimization Of A K-Band Low-Noise Bipolar Class-C VCO For 5G Backhaul Systems in 55nm BiCMOS Technology

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To My Family.

"Considerate la vostra semenza:
fatti non foste a viver come bruti,
ma per seguir virtute e canoscenza".

***Dante*, Divina Commedia, Inferno, Canto XXVI, vv. 118-120.**

Abstract

The demand for an enriched end-user experience and increased performance in next generation electronic applications is never ending, and it is a common trend for a wide spectrum of applications owing to different markets, like computing, mobile communication and automotive. For this reason wireless transceivers have become widespread components for nowadays electronics with a constant demand for power reduction and data-rate increase.

Data-rates in wireless communications have been steadily increasing with on-chip processing rate and logic density both in network applications and in hard-disk interconnects. The data-rates are now exceeding ***1-Gbps*** *and are expected to grow exponentially in next years as new standards are released together with the enormous amount of unlicensed bandwidth in the* ***E-Band*** *spectrum (****71-76 GHz*** *and* ***81-86 GHz*** *bands).*

The development of ***5G*** *communication systems is underway. Point-to-point wireless links in the* ***E-Band*** *can provide high data-rate, easily deployable, cheap and flexible Backhaul solutions, important enablers for the mobile network evolution towards* ***5G*** *network. The development of* ***CMOS/BiCMOS*** *integrated transceivers for* ***E-Band*** *Backhaul applications can help reducing the cost and footprint of the equipment, but presents design challenges, mostly related to the use of adaptive spectrally-efficient high-order modulations, which mandate high linearity and low Phase-Noise. In example when employing* ***64-Quadrature Amplitude Modulation*** *(****64-QAM****), very low Phase-Noise levels are required to limit* ***Error Vector Magnitude*** *(****EVM****) - i.e. less than* ***-117 dBc/Hz*** *at* ***1-MHz*** *offset from* $\boldsymbol{f = 20\ GHz}$ *carrier.*

In the frame of gigabit wireless systems, the work discussed in this thesis concerns with ***local-oscillator*** *(****LO****) generation requirements for* ***E-Band*** *Backhaul applications spanning from the concept of the circuit to its imple-*

mentation. Phase-Noise specifications for the frequency synthesizer are identified, and design and optimization of ***VCOs*** *performance is proposed. A* ***K-Band Class-C VCO*** *is proposed as key block of the frequency synthesizer. It achieves ultra-low Phase-Noise performance, while still achieving a wide Tuning-Range (****TR****), essential feature in* ***E-Band*** *communication standards. The choice between* ***CMOS*** *Versus* ***BJT*** *devices is investigated and the impact of the intrinsic Base-Resistance (*r_b*) in* ***BJT****-based* ***VCOs*** *is addressed.* ***BJT****-based* ***VCO*** *shows* $\sim$***2dB*** *better Phase-Noise when compared to* ***CMOS****-based* ***VCO*** *and low supply is employed. When higher supply is leveraged,* ***BJT****-based* ***VCO*** *advantage is kept while* ***CMOS****-based* ***VCO*** *is not able to reach the targeted Tuning-Range due to thick oxide devices parasitics. The challenges of achieving such a low Phase-Noise are discussed in detail, with particular emphasis on the minimization of* L/Q_T*, inductor versus Quality-Factor ratio. Prototypes have been realized in a* ***55nm BiCMOS*** *technology. Operated at* ***2.5 V*** *supply with the largest amplitude allowed by reliability constraints, measurements show a Phase-Noise as low as* ***-119 dBc/Hz*** *at* ***1-MHz*** *offset from a* ***20-GHz*** *carrier with a Tuning-Range of* ***19%*** *and* ***Figure of Merit*** *(****FoM****) of* ***-187 dBc/Hz****. Power consumption is* ***56 mW****. This dissertation demonstrates advances over* ***State-Of-The-Art*** *primarily in terms of low Phase-Noise performance, and shows how the proposed circuit is suitable as local-oscillator building block in direct-conversion* ***E-Band*** *Backhaul transceivers.*

The work has been performed in the ***Analog Integrated Circuits Laboratory*** *(****AICLab****) of* ***Universitá degli Studi di Pavia*** *in collaboration with* ***STMicroelectronics*** *and* ***Huawei****. The dissertation is part of broader efforts to demonstrate and design a complete* ***5G E-Band*** *transmitter.*

Overview

One of the main remarkable targets of the ***Information and Communication Technology (ICT)*** *is abridged in the ubiquity paradigm of accessing the network independently by space location: at home, at office, on the road. This vision -* ***"Connect Anytime, Anywhere, On Any Device"*** *- led to the development of multi-domain technologies, applications and architectures which allow the interaction of multiple aspects of the everyday routine. Multimedia-enabled mobile terminals, such as smartphones and tablets, are rapidly replacing personal-computers and laptops pulling alongside conventional consumer devices such as televisions and radios, which, increasingly, feature communication functions. As a result of* ***"Always and Everywhere"*** *Internet access, intelligence and smartness have also found their way into people everyday environment. Ubiquitous access to all media types - data, voice and video - has largely become a reality. This has brought to the explosion of the demand for connectivity and inter-operability together with the continuous increase of data volume through the connection networks. In the past ten years the bandwidth of the access networks has been increasing together with the computational power of* ***CPUs*** *and digital systems, while fixed and mobile networks converged.*

Transistors dimensions have been keeping on scaling at the pace expected by ***Moore's law****, leading to a consequent rise in their* ***Unity-Gain Frequency*** *(*f_T*), to the increase of the processing power of microprocessors, to the in-*

crease of the memory density and to a global improvement of the performance of integrated systems. The new applicative scenarios enabled by these innovations require an ever growing data-transferring speed. This aspect continues to resemble the infrastructural ***"bottleneck"*** *of several applications. Often, the limiting transmission speed of the communication and information systems frustrates the results achieved by the single devices alone in terms of computational power.*

If the modern communication infrastructures enabled by the ***ICTs*** *have already allowed the pervading advancement of Internet, the progressive offloading and distribution of computing tasks and services onto the network (****"Virtualization"*** *and* ***"Cloudification"****) are process still far from the end. Think about the tremendous impact of Social Networks on the network structure which had to adapt to the born of huge data-centers which need to handle enormous data-rates and incorporate huge amounts of computing power to deliver the services expected by cloud users. Concepts such as* ***Machine-to-Machine*** *(****M2M****) communication and the* ***"Internet of Things"*** *(****IoT****) will increasingly support people daily lives, enabled by innovations such as* ***"Smart Cars"****,* ***"Smart Cities"*** *and* ***"Smart Infrastructures"****. Thus, one of the crucial technological challenge, on which will depend the applications and services expansion, is represented by the design and demonstration of interconnections with higher capability and data-rate, not only along the conventional communications lines but also between boards (****inter-board*** *connection), between different chips (****inter-chip*** *communication) and also between devices integrated in the same die (****intra-chip*** *interconnection).*

O.1 Historical Overview And Future Forecasts

The rapid expansion of the *Information and Communication Technology* (**ICT**) is impacting our society. In a hundred of years, information exchange, once limited to letters and telegraphs has now reached the speed of light and

is accessible to general public. Our society, once satisfied with telephony, is now creating services to take advantage of the growing information capacity. This trend drives the demand for data-communication, which has superseded the original role of telephony networks for voice communication. With tens of millions of *direct-subscriber lines* (**DSL**) broadband access is indispensable. Business and consumer demands encourage further investments in communication infrastructures.

Since the development of **Arpanet**, the first computer network for military applications in the *1960s*, high-speed data-communication technologies have proliferated and innovation has been driven by the ubiquity paradigm of free network access *"Anytime, Anywhere, On Any Device"*. Applications started to provide not just voice links but seamless information access independently of location. Digital convergence between computing and communication devices started and smartphones are becoming the central hub of peoples digital activities.

Despite the profound changes already induced on society and people lifestyle, the **ICT** revolution is far from being fulfilled. In addition to multimedia *"infotainment"* applications a new class of energy-efficient smart devices are expected to sense, process, communicate and actuate information in a "data-centric" environment. Body-worn biometric sensors will monitor vital signs such as body temperature, pulse rate, breathing rate etc.., and alert health care or emergency services of critical events. At home, smart appliances, power meters and other home installations (e.g. lighting) are becoming controllable via mobile terminals (e.g. smartphones and tablets) communicating via a home gateway. This trend will accelerate and in the next future tiny sensor nodes are foreseen to monitor the environment, to recognize dangerous situations, single individuals as well as gestures and emotional status. Intelligence is also seen to spread in buildings and infrastructures to improve safety and energy efficiency, in vehicles for safer and more comfortable transports, all over the cities opening the way to an enormous variety of applications and services summarized

by novel visions as the *"Internet of Things"* (**IoT**), the *"Smart Vehicles"*, the *"Smart Infrastructure"*, the *"Smart Cities"* [**1**].

A complete different digital lifestyle will emerge, posing crucial challenges on devices and communication infrastructure. As devices need to be always connected, previously separated systems and networks must be integrated. Inter-operability between different networks has been developed, bridging fixed and mobile networks, public and private networks, telecommunications and **ICT** systems. The ubiquitous *"Anytime, Anywhere"* Internet access is increasingly demanding the adoption of *Software-Defined Network* (**SDN**) concepts and broadband wireless connectivity. Cognitive radio and self-organizing network functionality will be needed to improve the spectral efficiency and dynamically optimize network configurations. New concepts in cognitive radio will include spectrum agility (dynamic spectrum management) and cooperative detection. To provide broadband wireless access, new regions of the Radio-Frequency (**RF**) spectrum, notably the Millimeter-Wave (**mmW**) region (for example, short range at **80 GHz**) are being addressed by the **IEEE802.11ad** standard and by other consortia initiatives (e.g. multi-gigabit wireless systems). All these trends will challenge local processing and transceivers resources and will require the development of cheap, tunable widespread **E-Band RF-PAs**, **RF-LO** and efficient network processors in advanced **RF-CMOS** and $\mathbf{S_i/S_iG_e}$ technologies.

On the other hand, the data volume on all types of networks is going to explode with strong implications on power consumption. Today's Internet network is approaching the **ZetaByte** traffic (**Figure. O.1**) and by *2020* the energy required by the *"Information Technology"* (**IT**) traffic will exceed **10%** of the total electrical power generation in developed countries. The need to reduce the power consumption of all devices - i.e. the *"Green Policy"* - will represent one of the most relevant design constraints (e.g. deep architecture analysis with focus on ultra-low power, best in class low power technologies, advanced power management solutions, 3D packaging etc..).

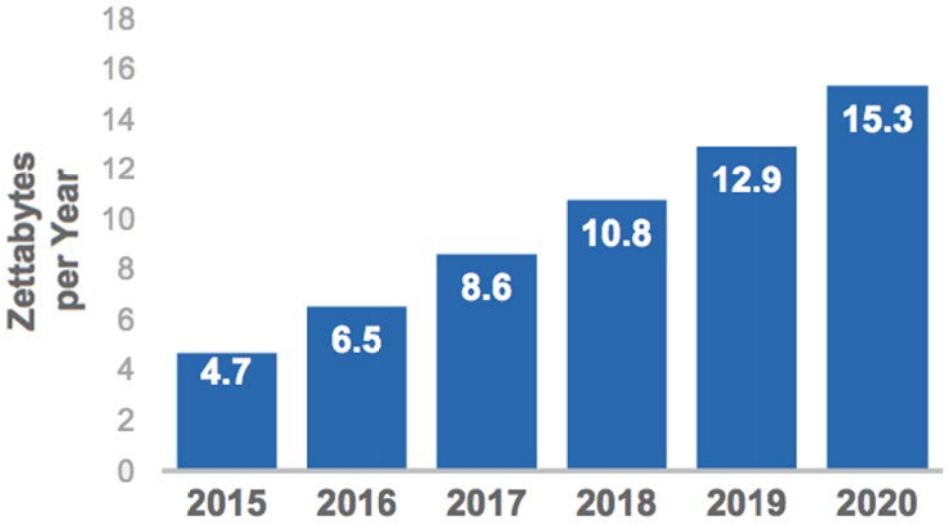


Figure O.1: Servers traffic increase per year.

The widespread access to *"Multimedia-on-Demand"* and the tremendous impact of *Social Networks* have deeply changed the network structure. Huge data-centers, at the network core, are providing the huge amounts of computing power needed to support users applications.

However, a full "data-centric" approach where information can seamlessly tunnel from any device to any destination, is still to be implemented. In this perspective the *Input/Output* (**I/O**) bandwidth requirements of systems, such as routers and servers will rapidly grow further as well as the needs of higher data-transferring speed. The transmission speed is therefore becoming the critical infrastructural *"bottleneck"* of several applications, as it frustrates the results achieved at the single devices level in terms of computational power and speed.

The design and demonstration of interconnections with higher capability and data-rate is therefore a key technological challenge that will affect the future pace of the **ICT** revolution. Higher data-rates are essential not only along the conventional communications line but also between boards (*inter-board* connection), between different chips (*inter-chip* communication) and also between devices integrated in the same die (*intra-chip* interconnection).

O.2 High-Speed Communications

Modern high-speed communication may be primarily divided among wireless and wireline channels. Wireless communication is currently comprising cellular communication for mobile telephony and broadband data communications using standards such as **IEEE 802.11b/g**. Wireless data communications are expected to grow through the deployment of **Wi-Fi** networks and data services over cellular communication.
While the focus of recent investment and consumer demand has accelerated the development of wireless infrastructure, the workhorse of data communication remains wireline technology. Wireline networking includes *Local-Area Network* (**LAN**), *Storage-Area Network* (**SAN**), *Wide-Area Network* (**WAN**), and long-haul communication. These distinctions are focused on the distance and speed of the network. Wireline communications are typically designed to support the highest data-rates over a physical channel.

O.2.1 Rise Of Wireless Communications

In recent years companies focused their efforts on emerging services like mobility, cloud and analytics. Extending battery life, lowering power consumption and maximizing power efficiency are key features to lead the market especially when referred to mobile devices. Modern mobile smartphones have to support different cellular standards from the *Global System for Mobile* communication (**GSM**) to its *Enhanced Data-rates Evolution* (**EDGE**), from the *third generation* (**3G-UMTS**), to the fourth generation *Long Term Evolution* (**4G-LTE**) together with **WiFi/WiMAX** connectivity. These significant advances in wireless devices, along with new wireless communications standards, converged to thrust the world into the *"always on, always connected"* era that we live in today.

The ever increasing mobile data traffic, expected to grow by **8X** from *2015* to *2020* [**2**], is driving continuous innovation in wireless communications, and

next generation mobile networks (i.e. *5G* and beyond) are expected to provide several **Gbps** user data-rate. Although the picture is not clear yet on how to overcome the performance limitations of the current **4G-LTE** standard, all the proposed hardware solutions involve a further increase in the *"Base-Transceiver Station"* (**BTS**) density, following the trend which has kept going in the last twenty years [**3**]. The **BTS** density increase rises the complexity of the network, and the Backhaul infrastructure, i.e. the set of links connecting the **BTS** to the network core, is emerging as a critical bottleneck in future-generation mobile networks [**3, 4**]. To push forward with the network evolution, two directions are emerging in the Backhaul industry. First, new hardware solutions are being investigated to provide high-capacity, easily-deployable, medium-range Backhaul links, suitable for dense **BTS** environments. Among the proposed competitors, **mmW** wideband wireless links, in the **E-Band** in particular, are emerging as a promising techniques [**3, 5**]. Second, as **BTS** reach high-volume productions, fully-integrated **BTS** transceivers in **CMOS** or **BiCMOS** technology can reduce the cost of Backhaul equipment. These emerging paths create new opportunities in **mmW** integrated circuit design. Unlike other **mmW** applications such as **60 GHz WLAN** or automotive radars, **E-Band** links employ high-order modulations to maximize the channel capacity. This mandates challenging specifications for integrated transceivers, especially concerning *Power-Amplifier* (**PA**) linearity and *Local-Oscillator* (**LO**) Phase-Noise.

O.3 CMOS Convergence

The success of modern *Integrated Circuits* (**IC**) is in large part due to the low-cost realization of a large-scale electronic system on a tiny semiconductor chip. Among several **IC** technologies, *Complementary Metal-Oxide System* (**CMOS**) technology has been the main driver of the exponential growth in **ICs** computing performance. The speed of **CMOS** logic gates has improved

by **13%** per year and the number of integrated transistors has increased by **50%** per year according to *Moore's law*. This continuous shrinkage of the feature size enabled higher operation speed, logic density, integration, and lower power consumption per logic function resulting in an enormous increase in the number of functionalities crammed into processing units and a **70%** growth per year of the chips computing capability. A direct consequence of this scaling process is the increase in the demand for high **IC-to-IC** wireless communication bandwidths to maximize overall system performance.

Silicon-based **ICs** play a central role in the evolution of the high-speed networks. The major advantage of silicon-based technologies is their ever increasing capacity for integration that enables realization of complex **ICs** at very low cost. For example, one consequence of integration includes doubling the number of transistors in a microprocessor every **18** months, while dropping the price of each transistor by a factor of **100** over **15** years.
The scaling trend of the silicon-based technologies, specifically the **CMOS** technologies, enables fabrication of devices with a higher frequency of operation. The latest *International Technology Roadmap for Semiconductors* (**ITRS**) projects the possibilities and challenges of integrated system design to year *2018*. For instance, the maximum *Unity-Current Gain Frequency* ($\mathbf{f_T}$), and *Unity-Power Gain Frequency* ($\mathbf{f_{MAX}}$), of a *Metal-Oxide System* (**MOS**) device with **32nm** and **22nm** gate-length are expected to be **280 GHz** and **310 GHz**, respectively.

Scaling as well as development of advanced silicon technologies such as *Silicon-Germanium* ($\mathbf{S_iG_e}$) **HBT** transistors with Germanium-doped base and *Silicon-on-Insulator* (**SOI**) technology with small device-to-substrate parasitics enables silicon technologies to meet the performance requirement of high-speed applications. In addition, along with a remarkable integration advantage, silicon-based technologies seem to be capable of delivering more functionality for a lower price and are the perfect candidate for the implementation of low-cost high-speed Integrated Circuits.

O.3.1 CMOS For mm-Wave Circuits

Electronic circuits dealing with such high data-rates will use highly sophisticated designs most probably based on the most advanced *Silicon-on-Insulator* (**SOI**) **CMOS** or even higher performing $\mathbf{S_iG_e}$ and **BiCMOS** technologies. The conflicting requirements of increased performance and reduced energy consumption are extremely demanding. If power consumption can be sufficiently reduced, harvesting energy from the environment should substantially enhance the autonomy of systems and reduce the requirements on battery charge capability (and size). The key communication technology performance metrics are:

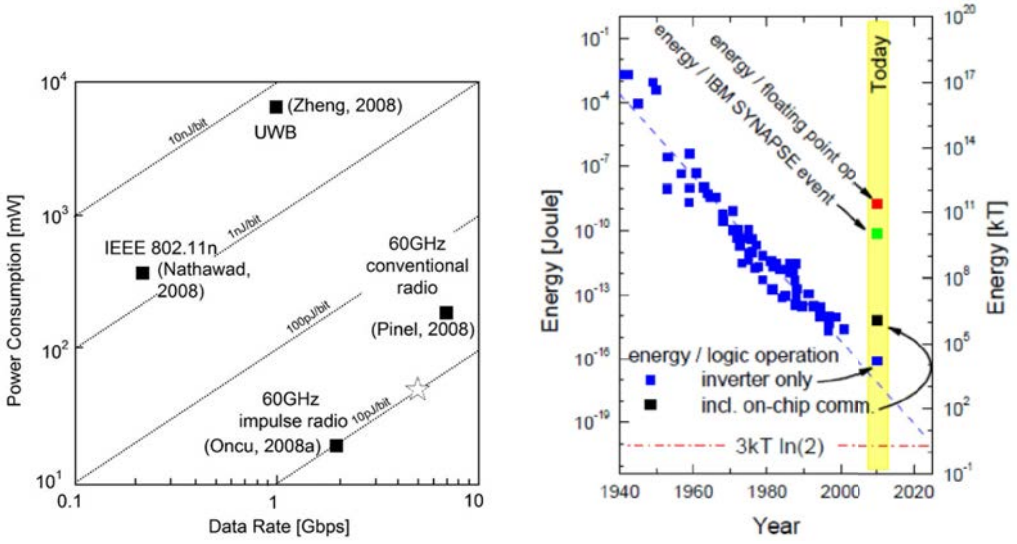
i) cost (**US$/Gbps**);

ii) power efficiency (**pico-Joule/bit**);

iii) bandwidth density (**Gbps/cm²** or **Gbps/cm**).

Traditionally, wireless systems in the **Gbps** range have been implemented in $\mathbf{G_aA_s}$ or bipolar technologies. The primary advantage provided by those technologies is faster intrinsic device speed (higher $\mathbf{f_T}$), but they suffer from the main drawback of limited level of integration. On the other hand **CMOS**, despite its slower device speed, is becoming the target technology for high-speed integrated systems due to its widespread availability and higher integration levels compared to the faster technologies. This availability makes high-speed links built in **CMOS** very attractive for large-volume applications that require such links. Furthermore with higher integration, links can be built as a macroblock in a single-chip system, allowing high throughput chips counts together with significant cost savings. Finally, the speed of **CMOS** technology is improving faster than the speed of other technologies, because of the extensive investment and momentum in **CMOS** technology developments.

The need for high-gain/high-frequency transistors able to operate in the **50** to **100 GHz** range, coupled with a suite of high-quality passive devices



(a) (b)

Figure O.2: Wireless Communication Power Trends: *(a)* - the trend is increasing power in the transmission as a consequence of the higher devices operating frequency at higher rates; *(b)* - Miniaturization leading to more energy efficient solutions: Inverters should approach the thermodynamical limit for power reduction by *2026*.

(capacitors, inductors, antennas) for the same frequency range is mandatory. These challenges will not be efficiently addressed by a single process technology. Wherever there is a need for high-power, high-efficiency and low noise, **BiCMOS** technologies will have to be deployed. The never-ending demand for new integrated functions should also be helped by the development of 3D integration techniques that allow the vertical stacking of several chips. The availability of this capability will, for example, enable the stacking of dedicated function chips (**SoC**) and *System-in-Package* (**SiP**) solutions. One of the major trends in mobile communications is multi-standard compliancy, which requires a highly integrated multi-standard **TX-RX** chain right up to the antenna, while also being low cost. New architectures, combined with silicon technologies such as *Fully-Depleted Silicon-on-Insulator* (**FDSOI**) can provide very efficient solutions able to simultaneously match the required performance and energy constraints. This approach is also important for data-centers and

High-Performance Computing (**HPC**) systems, which face the same challenge of providing more computing power and high-speed transmission capability within a limited energy budget.

Figure. O.2.a shows the actual power consumption (related to the robustness and quality of the transmission) of wireless transceivers (**Figure. O.2.b**) through the on-chip logic power consumption trend, almost exemplified by the energy requirements of a single inverter which by *2026* should approach the thermodynamical limit of **3KTln2**. Despite this reduction, the transmission architectures worsen the logic improvements of two orders of magnitude. In order to reach the performance required to support user needs, the energy efficiency of computing chips with better energy efficiency will open new opportunities in these important markets. Such results are performed also exploiting new architectures, different from the typical processor structure coming from the *Von-Neumann*'s one. Recently a great improvement has been demonstrated by the new *IBM's SYNAPSE* chip which presents a new computational architecture miming the neuronal structure reaching a **50** times improvement in energy consumption per logic operation.

O.4 Market Figures

Nowadays the hardware market for data-centers is currently worth around **US$ 100 billion**, pushed by new strategies such as *"Cloudification"* and *"Network-Function Virtualization"* (**NFV**) that can guarantee flexibility and data de-localization by reducing the local processing load and hence power consumption in end-user devices, by offloading processing tasks to the network.

Telecommunication market divides between wireline area and wireless fields. Wireline communications includes data communications as well as voice communications, with the emphasis shifting to data communications because of the growing use of smart phones and tablet computers. It is dominated by companies such as Ericsson, Huawei, Alcatel-Lucent, Cisco, and Nokia-Siemens.

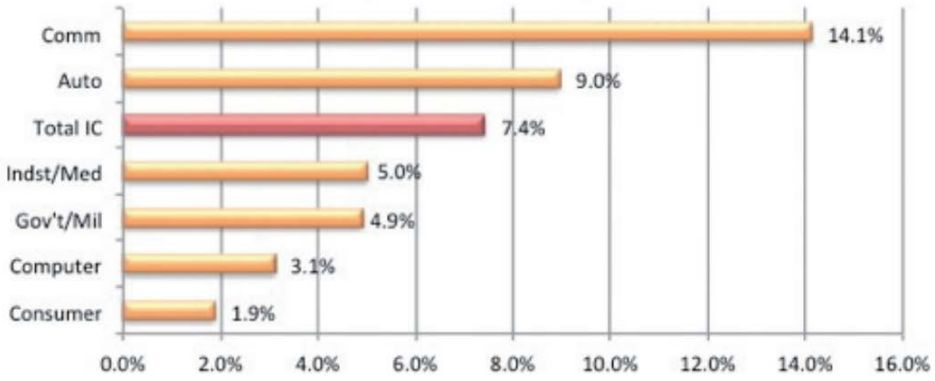


Figure O.3: ICs market growth by application **CAGR** *2011-2016*

On the other hand wireless communications includes mobile handsets, wireless communications infrastructures such as base stations, and local-area communications. The former number-one in wireless communications was *Qualcomm* but today other suppliers such as *Samsung*, *Texas Instruments*, *Mediatek*, *Broadcom*, *Infineon*, *Renesas*, and *Micron* are important market players. The market figures are still strong due to the persistent demand for smart phones and the need to support multiple protocols, e.g. **LTE**, **UMTS**, **EVDO**, **EDGE**, **GPRS** ecc...

In the past four years the market for communications chips expressed in terms of *Compound Annual Growth Rate* (**CAGR**) has increased by **14.1%** with respect to the **7.4%** of the overall semiconductor market. In *2016*, it reached a total value of **US$ 160 billion**, almost twice as large as in *2011* (**Figure. O.4**), overcoming for the first time the market share of chips for computers.

Wireless communications will be a major driver for the semiconductor industry over the next five to eight years. It will represent around **27%** of the telecommunication market over the period *2015* to *2020* compared to only **20%** in *2005*. Short-range wireless technologies (e.g. **Bluetooth**, **NFC**, **UWB** and **Wi-Fi**) are now well established in many electronic devices and rapid growth is forecast for the latest ones, such as **NFC** and **5G**.

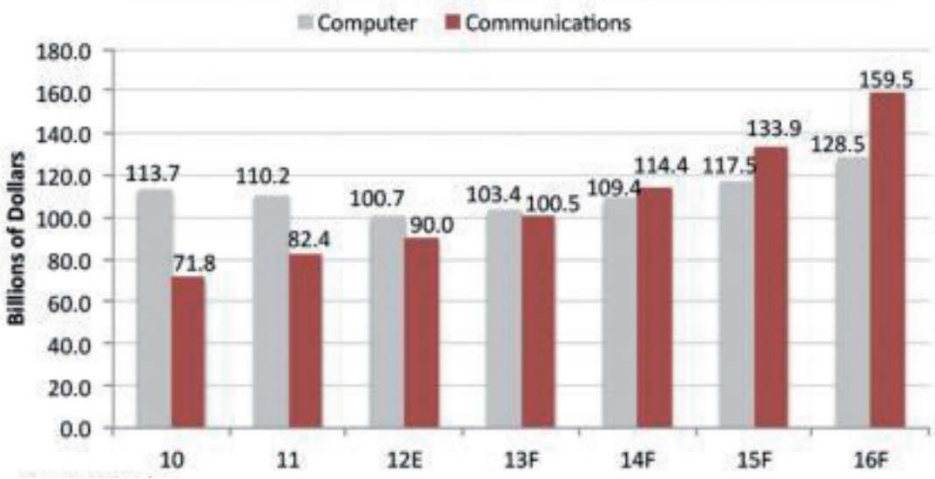


Figure O.4: Communications becoming largest market for **ICs**.

Table of Contents

List of Figures

Page

Overview

Introduction

Chapter 1: Phase-Noise In Oscillators

Chapter 2: Oscillator Topology

Chapter 3: Tank Scaling

Chapter 4: Circuit Design

Chapter 5: Measurements Results

List of Tables

Page

Glossary

Symbols | B | C | E | F | M | P | Q | R | S | T | U

Symbols

5G

5th generation mobile networks or **5th** generation wireless systems are the proposed next telecommunications standards beyond the current **4G/IMT**-Advanced standards. vii, viii, xv, xx, 6, 10

B

Backhaul

It is a portion of the network comprising the intermediate links between the core network and the small subnetworks at the "edge" of the entire network. vii, viii, xv, 6, 9–11, 15

Base-Resistance

($\mathbf{r_b}$). **BJT**'s intrinsic base-resistance. viii

C

Compound Annual Growth Rate

(**CAGR**). It is the mean annual growth rate of an investment over a specified period of time longer than one year. xx

E

E-Band

Radio Frequencies ranging from **60 GHz** to **90 GHz** in the electromagnetic spectrum. vii, viii, xii, xv, 11, 13–15, 17, 18, 21, 22, 45, 51

Error Vector Magnitude

(**EVM**). Is a vector in the I-Q plane representing the difference between actual received symbols and ideal symbols. vii

F

Figure of Merit

(**FoM**). Parameter to estimate VCO performance. The bigger (in magnitude) the better. viii

Fully-Depleted Silicon-on-Insulator

(**FDSOI**).. xviii

M

Millimeter-Wave

(**MMW**). Millimeter-length electromagnetic waves. xii

Moore's law

Empirical law stating that minimum transistor size halves every **18** months. ix

P

Phase-Noise

($\mathcal{L}$). It represents the frequency domain representation of rapid, short-term, random fluctuations in the phase of a waveform, caused by time

domain instabilities (*"jitter"*). It is measured in **dBc/Hz**. vii, viii, xv, 16–19, 21, 22, 24, 25, 27–33, 35–37, 39–42, 45, 47, 50–53, 55–58, 61, 63–65, 68–70, 73, 74, 77–80, 82–84, 86, 87, 91–94, 96, 101, 103, 106, 108, 110, 113

Q

Quadrature Amplitude Modulation

(**QAM**). It is both an analog and a digital modulation scheme. It conveys two signals by modulating the amplitudes of two carrier waves in quadrature. The modulated waves are summed and the final waveform is a combination of both **PM** and **AM**. vii, 6

Quality-Factor

(**Q**). It represents the ratio between the energy dissipated by a system and the energy stored inside. viii

R

Radio-Frequency

(**RF**). It is any of the electromagnetic wave frequencies that lie in the range extending from **3 KHz** to **300 GHz** including those frequencies used for communications or radar signals. xii

S

Silicon-on-Insulator

(**SOI**). xvi, xvii

T

Tuning-Range

(**TR**). It is the frequency range covered by a piece of equipment. viii, 33

U

Unity-Gain Frequency

($\mathbf{f_T}$). Maximum operating frequency of a device with **Gain** $\geq$ **1**. ix

Acronyms

Symbols | A | B | C | D | E | F | G | H | I | L | M | N | P | Q | R | S | T | U | V | W

Symbols

3G

3_{th} Generation. xiv

4G

4_{th} Generation. xiv, xv, 1

5G

5_{th} Generation. 2–6, 10, 17, 41

A

A_0

Oscillation Amplitude. 19, 42, 51

AC

Alternate Current. 54, 55

AM

Amplitude Modulation. 22, 23, 93

AP

AluCap. 77, 90, 99

AWGN

White Gaussian Noise. 37

B

BEOL

Back End Of The Line. 90

BER

Bit-Error Rate. 21, 33, 35–37

BiCMOS

Bipolar-CMOS Technology. vii, viii, xv, xvii, xviii, 14, 15, 19, 41, 42, 45, 52, 99, 113

BJT

Bipolar-Junction Transistor. viii, 18, 19, 31, 41, 51–54, 57, 58, 61, 64, 65, 68, 70, 74, 108, 113

BTS

Base-Transceiver Station. xv, 6–10, 14

BVCEO

Break-Down Voltage Collector-Emitter Base Open. 90

BW

Bandwidth. 37

BWCT

BW_{CT}. 37, 39

C

C

Capacitor. 25, 48

CAGR

Compound Annual Growth Rate. xx

CB

Common-Base. 47

CMOS

Complementary Metal-Oxide Systems. vii, viii, xii, xv–xvii, 14, 18, 19, 41, 42, 45, 51–55, 57, 58, 64, 65, 68, 70, 74, 75, 89, 90, 113

CPE

Carrier-Phase Estimator. 22

CPU

Central Processing Unit. ix

D

DC

Direct Current. 31, 54, 57, 69, 73, 78, 101

DSL

Digital Subscriber Line. xi

E

EDGE

Enhanced Data-Rates Evolution. xiv

EM

Electro-Magnetic. 73, 77, 85, 86, 92

ENF

Ecces Noise Factor. 33, 43

ETSI

European Telecommunications Standards Institute. 13

EVM

Error Vector Magnitude. vii, 17

F

F

Folding-Factor. 28, 51, 52

$\mathbf{f_0}$

Oscillation Frequency. 17, 42

$\mathbf{f_{Corner}}$

Noise Corner-Frequency. 17, 39, 51, 74

$\mathbf{f_{MAX}}$

Unity-Power Gain Frequency. xvi

$\mathbf{f_T}$

Unity-Current Gain Frequency. ix, xvi, xvii

FDSOI

Fully-Depleted Silicon-on-Insulator. xviii

FEOL

Front End Of The Line. 89

FET

Field Effect Transistor. 89

FM

Frequency Modulation. 23

FoM

Figure of Merit. 32, 33, 42, 43, 45, 50, 78, 79, 84, 86, 87, 92, 110, 112

$\mathbf{FoM_T}$

Figure of Merit - T. 33, 42, 43, 45, 110, 112

FSPL

Free-Space Path Loss. 9, 11

G

$\mathbf{G_aA_s}$

Gallium-Arsenide. xvii

GBW

Gain-Bandwidth Product. 90

GO2

Thick Oxide. 89

GP

General Purpose. 89, 94

GSM

Global System for Mobile. xiv

H

HBT

Heterojunction Bipolar Transistor. xvi, 89, 90, 96

HPC

High-Performance Computing. xix

I

I/O

Input/Output. xiii

IC

Integrated Circuit. xv, xvi

ICT

Information and Communication Technology. ix–xiii, 1, 2

IoT

Internet of Things. x, xii

IRR

Image-Rejection Ratio. 18

ISF

Impulse Sensitivity Function. 28–32, 51, 52

IT

Information Technology. xii

ITRS

International Technology Roadmap for Semiconductors. xvi

L

L

Inductance. viii, 18, 19, 54

LAN

Local-Area Network. xiv

LO

Local-Oscillator. vii, xii, xv, 15–18, 25, 33, 35–37, 39, 113

LoS

Line-of-Sight. 9, 11

LP

Low-Power. 89, 94

LTE

Long-Term Evolution. xiv, xv, 1–3, 6, 17

LTV

Linear Time-Variant. 25, 29, 31

M

M1

Metal-1. 90

M2M

Machine-to-Machine. x, 3, 4

M5

Metal-5. 90

M6

Metal-6. 90, 99

M7

Metal-7. 90, 99

M8

Metal-8. 77, 90, 99

MIMO

Mutiple-Input and Multiple-Output. 9, 10

mmW

Millimeter-Wave. xii, xv, 8, 9, 11, 22

MOM

Metal-Oxide-Metal Capacitor. 94, 96

MOS

Metal-Oxide Semiconductor (Field-Effect Transistor). 31, 54, 61, 64, 74, 80, 83, 93, 97

N

NFC

Near-Field Communication. xx

NFV

Network-Function Virtualization. xix

NMOS

N-Metal-Oxide-Silicon. 94

P

PA

Power-Amplifier. xii, xv, 15, 16

PLL

Phase-Locked Loop. 15, 16, 18, 22, 37, 40, 103

PM

Phase Modulation. 24, 93

PtP

Point-to-Point. 11, 13

Q

Q

Quality-Factor. 39, 84

Q_C

Capacitor Quality Factor. 48, 50, 51, 86

Q_L

Inductor Quality Factor. 47, 50, 53, 82, 86, 95

Q_T

LC-Oscillator Tank Quality Factor. viii, 18, 19, 27, 28, 32, 43, 47, 50, 51, 54, 57, 80, 82, 95

QAM

Quadrature Amplitude Modulation. vii, 6, 13, 15, 17, 22, 33, 35, 37, 39, 40, 112

QoE

Quality of Experience. 6

QPSK

Quadrature Phase-Shift Keying. 13, 39

R

r_b

Base-Resistance. viii, 19, 31, 57, 58, 70

r_{ON}

ON-Resistance. 47–50, 94, 95

R_T

Tank Resistance. 25, 31, 32, 85

RF

Radio-Frequency. xii, 17, 21, 31, 53, 57, 69, 73, 78, 83, 104

RMS

Root Mean Square. 31, 32, 43

RX

Receiver. xviii, 10, 15–17

S

S_i

Silicon. xii

S_iG_e

Silicon-Germanium. xii, xvi, xvii, 15, 52, 89

SAN

Storage-Area Network. xiv

SDN

Software-Defined Network. xii

SFDR

Spurious-Free Dynamic Range. 24

SINR

Signal-to-Interference-and-Noise Ratio. 7, 9

SiP

System-in-Package. xviii

SNR

Signal-to-Noise Ratio. 7, 10, 13, 21, 33, 35–37, 40, 42

SoC

System-on-Chip. xviii

SOI

Silicon-on-Insulator. xvi, xvii

SSCR

Single Side-Band to Carrier Ratio. 25

T

TR

Tuning-Range. viii, 18, 33, 41–43, 45, 47, 49, 50, 61, 65, 70, 74, 110

TS

Symbol Time. 37

TX

Transmitter. xviii, 10, 15, 16

U

UDN

Ultra-Dense Network. 10, 11

UMTS

Universal Mobile Telecommunications System. xiv

UTM

Ultra-Thick Metal. 90

UWB

Ultra-Wide Bandwidth. xx

V

V_{DD}

Supply Voltage. 19, 42, 45

V_{pk}

Peak-to-Peak Voltage. 25

VCO

Voltage Controlled Oscillator. viii, xxxiv, 15, 18, 19, 21, 22, 33, 37, 39–43, 45, 47, 51, 52, 58, 61, 64, 74, 75, 79, 82, 83, 85, 89, 92, 93, 96, 97, 99, 101, 103, 104, 106, 108, 110, 113

W

WAN

Wide-Area Network. xiv

WLAN

Wireless Local-Area Network. xv

Introduction

*In this **Chapter** an introduction to **mm-Wave** links suitable for backhauling is outlined. First, focus is set upon the major requirements the future-generation mobile network is asked to satisfy together with the main applications. Then, **E-Band** wireless links are briefly described, outlining the major challenges concerning the robustness of the communication and discussing the outcoming standards and regulations. Finally, the specific targets and objectives of this work are presented.*

I.5 Toward The "5G Vision"

The *Information and Communications Technologies* (**ICT**) has kept on evolving since the *1980s*, providing an increasing amount of end-user oriented applications and benefits, being **ICTs** regarded as key elements for social and economic development. As an example, the **4G** network enabled an enriched multimedial mobile experience as broadband wireless communications started to become practically equivalent to home-connections. Keeping on this trend next generation services will require to share a tremendous amount of data in a real-time response to mobile users stressing the network capacity. And some of this technological barriers to services evolution are already emerging. For example, the **4G/LTE** network is not able to provide instantaneous cloud services to mobile users which can enable people to have desktop-like experiences

Figure I.5: 5G enabling services and requirements

on the go. Furthermore, the **LTE** network can provide high quality video experience to only a limited number of mobile users simultaneously. Thus, in the future, new technologies and services (**Figure. I.5**) will enhance and change people lifestyle of future generations under many aspects. Next generation mobile network, namely the **5G**, will provide unlimited information exchange massively shared among users and objects with minimum latency powered in a self-sustained way. Through these innovations, a collective synergy of diverse services is expected to emerge enabling **ICT** industries to open new converged services. Thus, **5G** networks are currently regarded as the key infrastructure that innovates **ICT** industry.

In order to enable connectivity for a very wide range of applications with

Figure I.6: Connected Devices growth forecast in next years: The exponential increase in connected devices will seriously affect the Network Structure.

new characteristics and requirements, **LTE** wireless access capabilities must extend far beyond those of previous generations of mobile communication. The further evolution of mobile networks towards 5^{th}*-Generation* is driven by these capabilities [**6, 7**]:

i) **Huge system capacity:** Mobile data-traffic is expected to exponentially increase in next years stressing the network capacity which will evolve toward new paradigm in device-to-device management and connectivity while still preserving the overall service quality and multimedia experience for the end-user pushed by the deployment of billions of **M2M**-connected devices (**Figure. I.6**). For this evolution to be sustainable **5G** networks must deliver data with much lower cost per bit and compared to nowadays' network while facing the problem of managing a larger energy footprint requiring a much more power-friendly management of the network links than current cellular networks;

ii) **Very high Data-Rates everywhere:** A common trend in mobile network evolutions is the continuous data-rate increase from each generation to the next. This trend was driven so far by the need to provide pervasive cloud-computing and the deployment of **UHD** video streaming services. This trend is a built-in in the next network evolution step but with an important diversification with respect to the past. Instead of focusing

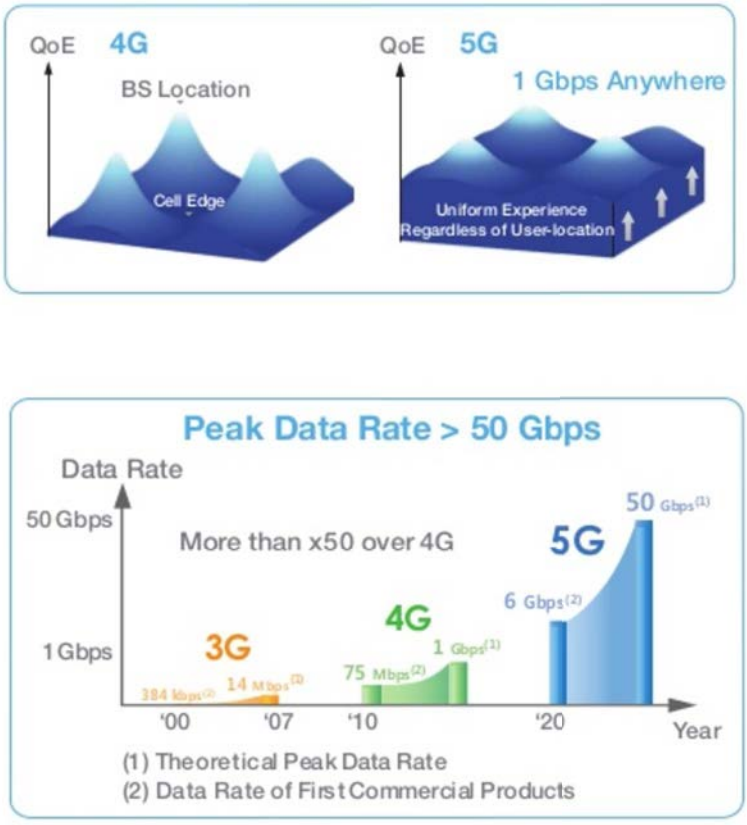


Figure I.7: Data-rates and uniformity Comparison.

uniquely on the peak data-rate, next generation connectivity puts ubiquitous access to the network and services under real-life conditions in different scenarios as specific target on the to-do list. **5G** should support data-rates exceeding **10 Gbps** in specific scenarios such as indoor and dense outdoor environments. Data-rates of several **100 Mbps** should generally be achievable in urban and suburban environments. Data-rates of at least **10 Mbps** should be accessible almost everywhere, including rural areas (**Figure. I.7**) providing uniform distribution;

iii) **Very low latency:** Specifically designed to enable **M2M** communications and applications rather than the mere multimedia expansion, a key point is represented by low latency. [**3**]. This aspect is one of the most remarkable barriers in current mobile communication systems which are

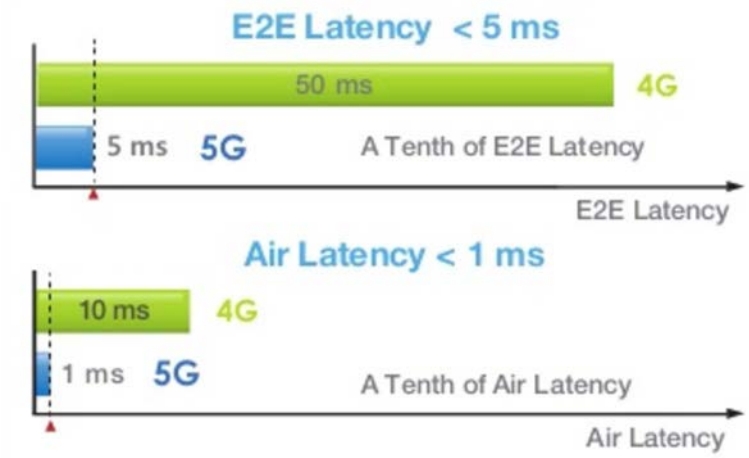


Figure I.8: Ultra-Low latency in **5G** network.

preventing some futuristic visions from being deployed such as traffic safety and control of critical infrastructure and industry processes. To support such latency-critical applications, **5G** is expected to deliver impressive data-rates with end-to-end latency of **1 ms** or less (**Figure. I.8**). This will create new capabilities for real-time communication and will allow ultra-high service reliability in a variety of scenarios, ranging from entertainment to industrial process control;

iv) **Ultra-high reliability and availability:** Being deployed in different critical scenarios, **5G** links should also enable connectivity with ultra-high proving an extremely rare quality connectivity deviation from service requirements;

v) **Very low device cost and energy consumption:** *"Green-policy"* is expected to be a key point from the energy and power dissipation point of view while "Low-cost" has been the major market driver since the early days of mobile communication. While "low-cost" is guaranteed by the technological scaling at a rate set by the well known *"Moore law"*, a smart power management and increase of the battery life (several years in example) will put to the test company R&D capacities in order to

enable the vision of billions of wirelessly connected devices;

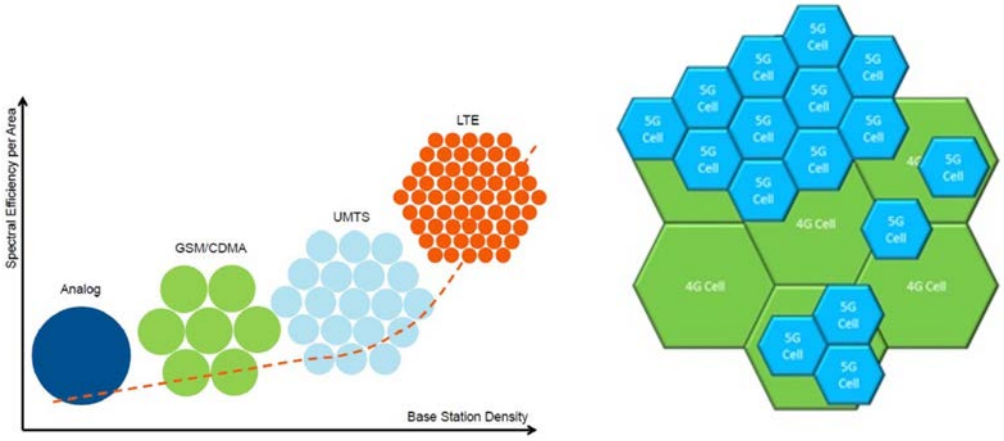
vi) **extreme efficiency:** One of the key enablers for high throughput in **5G** is densely-deployed small cells. In order to take full advantage of this massive-scale small cells, **5G** network shall be a lot more efficient in cost and energy usage.

The aforementioned requirements partly clash with each other, and will require an holistic, heterogeneous environment having to deal with multiple network layers, several co-existing access and Backhaul technologies [**3, 1, 8**].

I.5.1 5G Backhaul Challenges: The Transmission "Bottleneck"

5G targets are evidently ambitious and intensify the design challenges of the holistic **5G** network. Providing a Backhaul infrastructure to 5G and *Small-Cell* networks is complicated, and Backhaul capacity and power consumption are expected to become a major bottleneck in the network evolution [**3, 5, 9**]. As depicted before, 5G scenarios need high-capacity (**$>$ 10 Gbps**), low-latency (**$<$ 1 ms**), reliable Backhaul connections [**4**].
In order to provide the higher data-rate capacity needed by upcoming application scenario overcoming the performance limits of **LTE**, several techniques are currently under investigation [**10**]. All of them rely on adaptive coding and modulation like *Quadrature Amplitude Modulation* (**QAM**) improving the cell edge performance and combined with multi-**BTS** cooperation and dense deployment it helps in delivering the promise of *"Gbps anywhere"* and *"Uniform Quality of Experience"* **QoE**. Chief among them, three solutions are emerging as the more competitive ones:

Cell coverage area shrinking and BTS densification ((following the path which has already been traced in previous network generations, as shown in **Figure. I.9**) enable efficient spectral reuse leveraging spatial



(a) (b)

Figure I.9: Base Station densification trends: *(a)* - the trend is shrinking cell size and density while reducing energy-per-link as well; *(b)* - **5G** cells will be far smaller then **4G** cells requiring highly hierarchical network structure and coordination protocols at the edge of the cells.

diversity whilst providing superior *Signal-to-Noise Ratio* (**SNR**) at given bandwidth, thus allowing more spectrally-efficient modulations [**11, 12**];

While **SNR** benefits from **BTS** densification, interference does not scale down with cell area coverage as well resulting in *Signal-to-Interference-and-Noise Ratio* (**SINR**) worsening [**3**]. Therefore new concepts and techniques are asked to mitigate the defend link integrity from undesired out-of-channel or out-of-applications signals, both in **BTS** and user terminals [**11**].

Cell splitting will demand also an adaptive resource coordination among transmitters and advanced signal processing at the receivers. This problem proves even more urgent and critical when moving users are considered, since in dense **BTS** networks frequency of handover increases between neighboring cells. A hierarchical **BTS** infrastructure seems to be the natural answer to face this problem decoupling the resources allocation side from the mere data-providing system: wide-area macro **BTS**

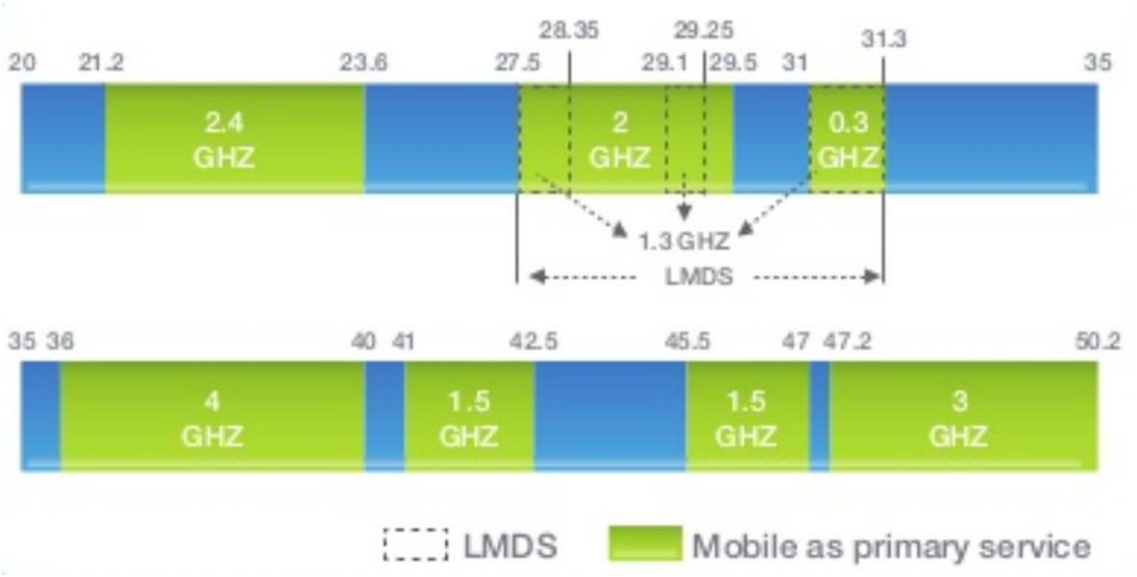


Figure I.10: Potential **5G** bands in **20-50 GHz** range.

manage control signals, allocate spectrum resources and cater for handover procedures, whereas micro cells provide data offload [**3, 4, 9**];

Millimeter-Wave (mmW) (**mmW**) links are expected to be adopted in order to give access to the huge amount of unused spectrum above **10 GHz** who can widely increase the communication bandwidth [**4, 13**]. The *mm-Wave* bands provide **10** times more bandwidth than the **4G** cellular-bands, as illustrated in **Figure. I.10**.

Several spectrum portions are under investigation by mobile operators. In the lower **mmW** domain, **28 GHz** (∼**1 GHz** spectrum available), **38 GHz** (up to ∼**4 GHz** spectrum available) and **47 GHz** (up to ∼**5 GHz** spectrum available, depending on the countries) licensed bandwidths are available [**14**]. Detailed studies on reflections and propagation in densely populated urban areas have been carried out showing promising results for mobile access [**13, 15**]. The **60 GHz** band, featuring up to **9 GHz** unlicensed spectrum, is also considered as an option for **mmW** access, although high propagation losses would require a too dense **BTS** environment [**5**]. Finally, **71-76 GHz** and **81-86 GHz** bands, featuring

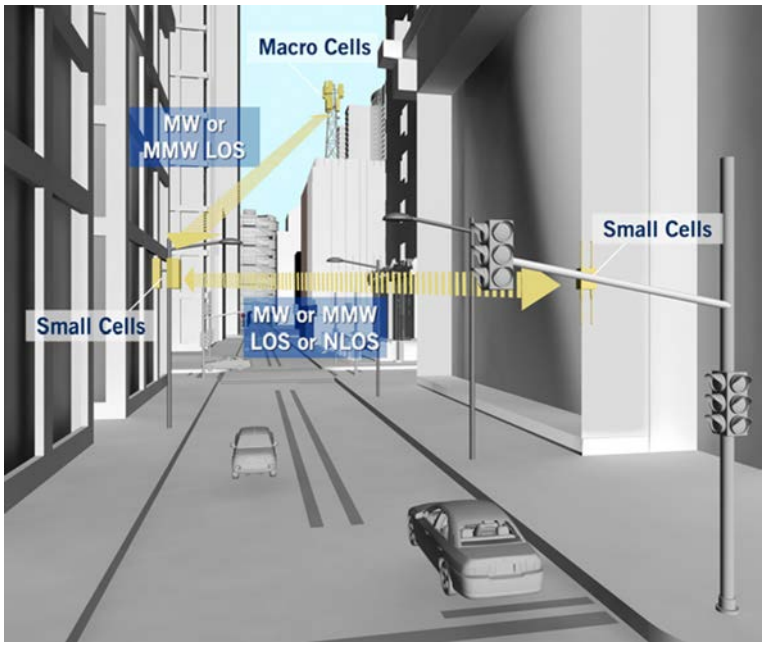


Figure I.11: Typical *Small/Macro-Cell* scenario.

lower atmospheric attenuation and currently allocated for licensed fixed Backhaul radio links, could be used for mobile service as well [**16**].

Week diffractions in the *mm-Wave* bands determine higher *free-space path loss* (**FSPL**) and a consequent more fragile link. Fortunately, the small *mm-Wave* wavelength (λ) is naturally prone to highly directional beamforms that can be obtained by means of a large number of antenna elements in a smaller form factor, benefiting from dense **BTS** environment. These adaptive directional beams with large antenna array gain are key in combating the large propagation loss in the *mm-Wave*, giving birth to *Multiple-Input-Multiple-Output* (**MIMO**) systems capable of steering different data streams to different users at the same time. As a matter of fact the shrinking of cell size brings within the reduction of the (**FSPL**) as *Line-of-Sight* (**LoS**) links become more likely, and the set of users to be covered scales down. Finally, as **mmW** links are mostly noise-limited, rather than interference-limited, the **SINR** efficiently scale with cell area shrinking [**3, 15**];

Massive MIMO systems have also been recently proposed as a way of increasing the channel capacity leveraging spatial diversity. It is based on spatial multiplexing, in which data streams from several branches are multiplexed and transmitted over several spatially separated channels [**12, 17**]. As a matter of fact path loss between **BTSs** does not depend on frequency but relies on the **TX** and **RX** antenna aperture [**18**] which does reduce in proportion to the square of the frequency. That reduction can be compensated by the use of higher antenna directivity [**15**].
The **5G** radio will employ **K** antenna elements to increase antenna aperture serving $\mathbf{N < K}$ users. In this framework, massive **MIMO** systems benefit as well from cell area shrinking, which implies having to manage a reasonable amount of users. Beamforming will be used by **BTS** to track one another and improve energy transfer and **SNR** over an instantaneously configured link. Beamforming will also improve the radio environment by limiting interference to small fractions of the entire space reducing their impact on communication quality. Coordination calibration and data-distribution will be be the major implementation challenges during the development of an hardware massive **MIMO** system while keeping array size, power and cost under acceptable values [**18**].

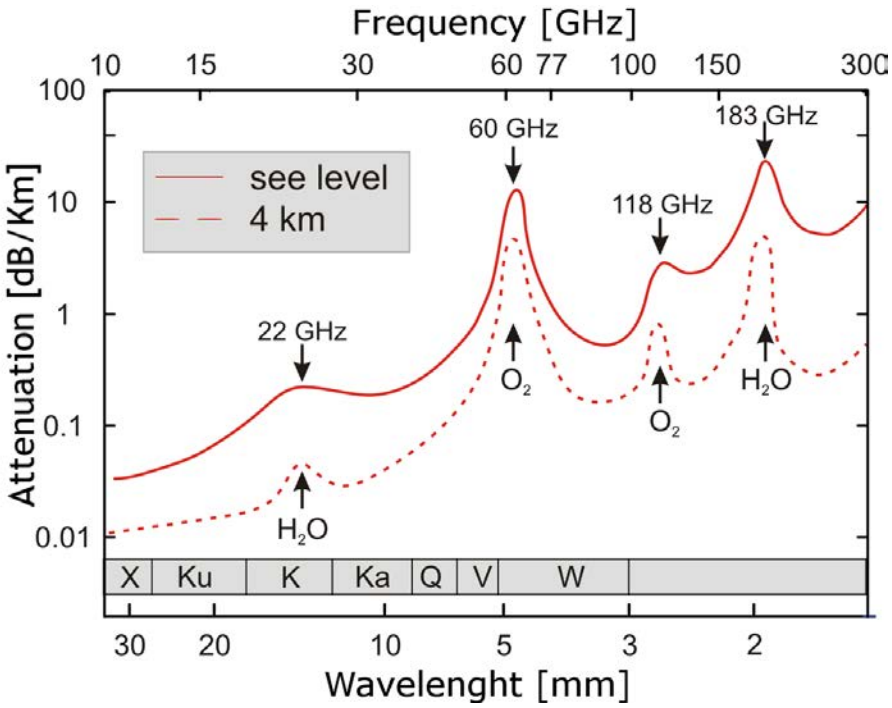
Each of the aforementioned techniques forecasts an increase in the **BTS** density. In the development towards 5G, the mobile infrastructure is expected to evolve towards *Small-Cell* (or *Pico-Cell*) *Ultra-Dense Networks* (**UDN**), where thousands of small **BTS** located at the street level provide mobile services to users, as shown in **Figure. I.11** [**9, 1, 19**].
Small-Cell Backhaul links have to be cheap, easy to deploy and reconfigure owing to the proximity of transmitters and receivers, maximise area spectral efficiency through the tight reuse of the precious spectrum, and power-friendly as the Backhaul consumption is expected to grow up to $\sim$**50%** of the **BTS** power budget [**4**]. However, as cell density rises, the Backhaul infrastructure

complexity increases.

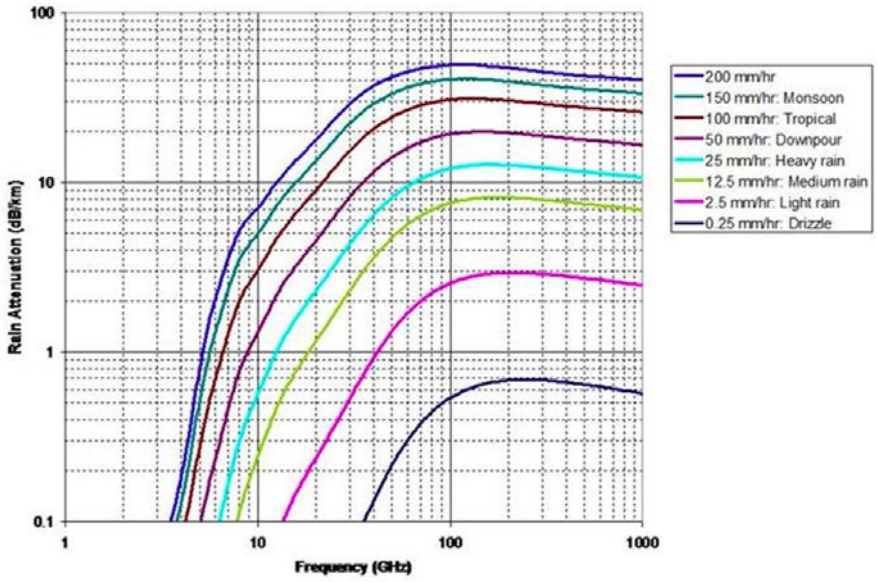
I.6 mm-Wave Wireless Point-to-Point Links

Optical connections can reach extremely high data-rates, but they are expensive and difficult to implement in ultra-dense scenarios [**3, 4, 11, 10**]. On the other hand, **PtP** *mm-Wave* links are expected to provide enough channel capacity for next-generation networks [**3, 4, 11**]. Therefore a huge interest in allocating future services in the huge amount of unlicensed spectrum above **10 GHz** has been shown by many companies and countries.
10 GHz of spectrum in the **mmW** domain, in the **E-Band** in particular, have been allocated by American and European Committee for next generation **PtP** wireless Backhaul links [**7, 20, 21, 22**]. **E-Band PtP** links are expected to provide wideband, medium-range **LoS** links, suitable for backhauling *Small-Cell* **UDN** [**4, 7**].

To **5 GHz** bandwidth (namely the **71-76 GHz** and the **81-86 GHz** portion of the spectrum) in the E-Band range have been identified to support *Point-to-Point* wireless links. Additionally, the **92-96 GHz** band is allocated in the **USA** only. As shown in **Figure. I.12.a**, atmospheric attenuation in the **E-Band** is as low as **0.5 dB/Km**, much lower than in the **60 GHz** band. By adopting high-gain, multi-array antennas (very compact at **mmW**) the significant **FSPL** (i.e. $\sim$**130 dB** over **1 Km** distance) can be easily compensated in **LoS PtP** links.// radiation absorption by water particles spread into atmosphere is another source of losses in the **E-Band** environment. While fog attenuation is negligible, rain losses can get up to tens of **dB/Km** (**Figure. I.12.b**) limiting the practical operative range of **E-Band LoS-PtP** links to **1-2 Km**, which is still suitable for *Small-Cell* backhauling [**23**]. In order to always achieve the maximum available channel capacity under any atmospheric condition, allowing the ubiquitous access to the network, proposed *mm-Wave* standards employ adaptive-modulation techniques, so as



(a)



(b)

Figure I.12: Attenuation in the *mm-Wave* spectrum: *(a)* - Air attenuation in the *mm-Wave* spectrum; *(b)* - Rain attenuation in the *mm-Wave* spectrum.

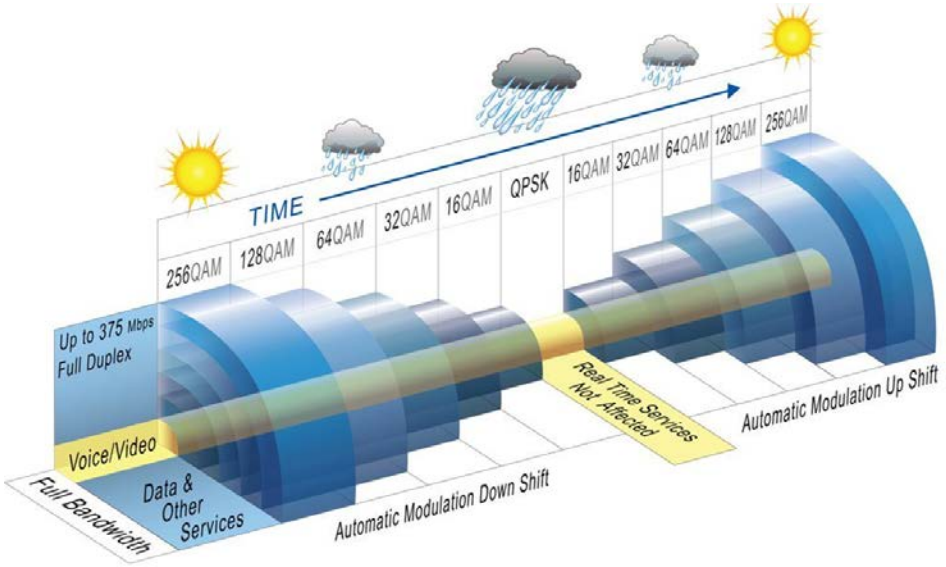


Figure I.13: Adaptive modulation according to weather conditions in **PtP** radio service.

to change the modulation order according to channel conditions, as shown in **Figure. I.13** [**24, 25**]. When high **SNR** is received, spectrally-efficient modulations like **64-QAM** and beyond are employed. Instead, if the received **SNR** is poor (e.g. during heavy rain outage), simpler modulations such as **QPSK** are used preferring a lower data throughput over link robustness.

I.6.1 E-Band PtP Links Standard

In the European Union some rules for the **E-Band PtP** communications have been already provided and included in the (*European Telecommunications Standards Institute*) **(ETSI)** standard **302-217** [**26**].

Recommended channel spacings and modulation orders are summarized in **Table. I.1**, together with the minimum required data-rate. Standard channels are **250 MHz** wide, but they can be split in two or four smaller sub-channels, or aggregated into wider channels up to **2 GHz** if required in a channel-aggregation scenario [**26**]. Modulations up to **256-QAM** are expected for standard channels, while lower-order solutions (e.g. **16-QAM**) may be used

	Channel Spacing [MHz]									
Number of Symbols	62.5	125	250	500	750	1000	1260	1500	1750	2000
2	35	71	142	285	427	570	712	855	997	1140
4	71	142	285	427	570	712	855	997	1140	//
8	106	212	425	850	1275	1700	2125	2550	2975	3400
16	142	570	1140	1710	2280	2850	//	//	//	//
32	219	438	875	1750	2625	//	//	//	//	//
64	262	525	1050	2100	3150	//	//	//	//	//
128	306	612	1225	1450	//	//	//	//	//	//
256	350	700	1400	2800	//	//	//	//	//	//

Table I.1: Minimum required data-rate (in **Mbps**) for **E-Band PtP** transceivers complying to the **ETSI** standard **302-217**, as a function of channel spacing and number of modulation symbols.

in channel-aggregation scenarios [**13**]. The data-rate should reach **∼3 Gbps** using spectrally efficient modulations. The standard explicitly allows to change both the channel bandwidth and the modulation order on the fly according to channel conditions. Other significant requirements for **E-Band** transceivers are outlined in **Table. I.2**.

Min. Bit-Error Rate (**BER**)	$\mathbf{10^{-6}}$ or $\mathbf{10^{-10}}$
Carrier frequency tolerance	**±50 ppm**
Max. EIRP	**85 dBm**
Max. **TX** power	**30 dBm**
Min. antenna gain	**38 dBi**

Table I.2: Significant requirements for **E-Band** wireless systems, according to the **ETSI** standard **302-217** and in compliance with European regulations.

I.7 E-Band Transceivers

As aforementioned above, “cheap”, “compact” and “energy-efficient” will be key words in the development of a *Small-Cell* **E-Band-BTS** network infrastructure compared to the existing **BTS** transceivers, [**3, 5**]. The need of a widespread and ubiquitous network architecture and the forecast growth in the **BTS** equipment sales, demands for a massive volume production relying on **CMOS** and **BiCMOS** technologies combined with low-power design tech-

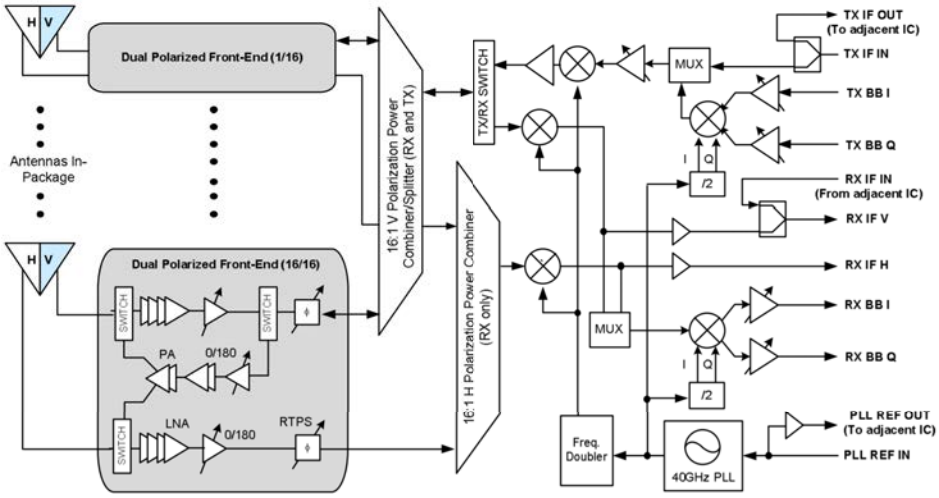


Figure I.14: Schematic of the *IBM* **E-Band** backhaul transceiver.

niques.

The stringent output power levels requirements set to power amplifiers (**PA**) motivates the frequent adoption of $\mathbf{S_iG_e}$**-BiCMOS** processes [**5**]. Development of integrated transceivers for **E-Band** Backhaul is still in an early stage. However, *IBM* has presented a $\mathbf{S_iG_e}$ **E-Band** transceiver, shown in **Figure. I.14** [**27**], supporting modulations up to **128-QAM** [**28**]. As shown in the block diagram, the transceiver features a complete analog **TX** and **RX** front-end.

LO-generation is performed using a **VCO**, embedded in a **PLL**, followed by a *frequency doubler* in parallel to a *Divider-by-2* **I** and **Q** phases. The chipset covers **83-100 GHz** band [**5**]. The prototype includes a complete **TX** and **RX** analog chain, and a complete frequency synthesizer. However, high-order-modulation transmission (i.e. **64-QAM**) was only achieved using an external **LO** [**31, 29, 30**]. *Infineon* is also working on **BiCMOS E-Band** transceiver development, and recently presented a complete system transmitting modulated data up to **64-QAM** [**32, 39, 39, 38, 37, 35, 36, 34, 33**].

Research on analog building blocks for **E-Band** integrated transceivers is

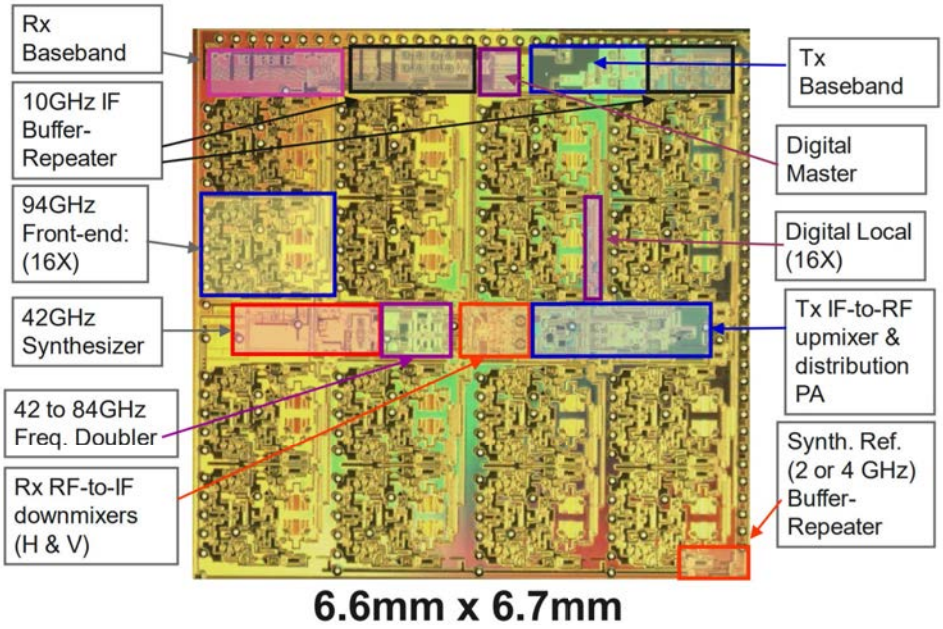


Figure I.15: Chip-Micrograph of the *IBM* **E-Band** backhaul transceiver.

mainly focused on two different tracks: transmitters **PAs** and **LO** frequency synthesizers. On the **TX** side, much efforts have been spent developing **PAs** with high saturated output power and linearity, able to support high-order symbol constellations [**34**]. In the frequency synthesis domain, solutions have been proposed to achieve wide Tuning-Range (**TR**), provide accurate quadrature generation and minimize Phase-Noise avoiding the degradation of the transmitted symbol modulation.

I.8 Objectives And Contributions

A stringent signal purity in local oscillators for **E-Band** transceivers is required. Still, power consumption has to be minimized. Since mobile services are expected to be deployed on a huge frequency range, different **PLLs** are used on chip, leading to an overall **30%** chip area occupation for **TX/RX PLLs** in single carrier scenario whereas number of **PLLs** duplicates in carrier aggregation scenarios. Oscillator spectral purity also dictates the allocation of

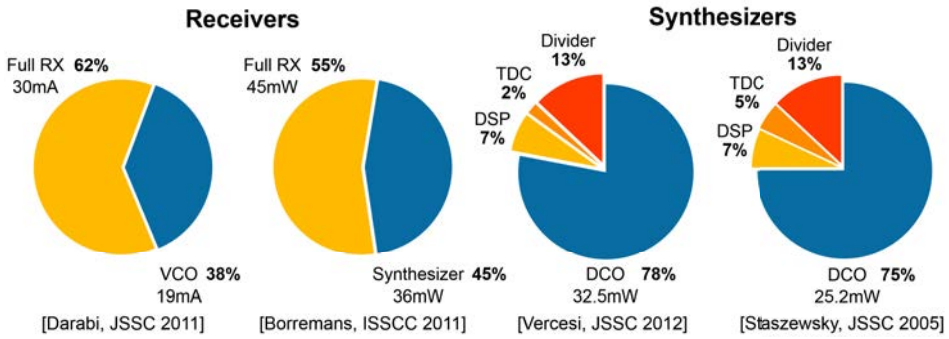


Figure I.16: Power consumption of a frequency synthesizers in transceivers.

a significant fraction of the transceiver power to the **LO**-generation building blocks. That's why frequency synthesis plays a key role when designing a transceiver architecture. When employing high-order modulation such as **64-QAM**, very low Phase-Noise levels are required to limit **EVM** - i.e. less than **-117 dBc/Hz** at **1 MHz** offset from $\mathbf{f = 20\ GHz}$. These requirements are fulfilled consuming high amount of power of an **RF** frequency-synthesizer [**40, 41**] and burning more than **30%** of the cellular **RX** power [**42, 43**] (**Figure. I.16**). High power efficiencies and low area occupation are clearly crucial, in such a scenario.

In this thesis the importance of a well-designed **LO**-generation circuitry, to achieve low Phase-Noise in the **E-Band** spectrum, is discussed. This topic is becoming significant both due to the drive to broaden the spectrum for mobile communication (in order to increase number of users per area) and the push to adopt high-order modulations to increase single channel capacity.

Almost increasing tenfold the present *State-Of-The-Art* **LTE** data-rates, no standards for a **5G** wireless link communication system are available not allowing a proper definition of the transmitters specs. The targeted **LO** requirement have been set to:

i) Fundamental oscillation frequency ($\mathbf{f_0}$) centered at **20 GHz**;

ii) $\mathbf{f_{Corner}}$ (*Noise Corner-Frequency*) $<$ **700 KHz**;

iii) $\mathcal{L}_{\text{@ 20 GHz, @ 1-MHz } \Delta f} <$ **-117 dBc/Hz**;

iv) **TR** $>$ **15%** able to cover the **E-Band** spectrum or eventually one only sub-band (and rely on the use of multiple **VCO** inside the **PLL** in order to cover the whole spectrum);

v) **IRR** (*Image-Rejection-Ratio*) $>$ **42 dB**;

vi) Suitable power consumption.

In this work, the design and measurements of a *low-noise K-Band* ***VCO*** are presented and the challenges of achieving such a low Phase-Noise are discussed in detail. We investigate the minimum Phase-Noise achievable by a *Class-C* ***VCO*** around $\mathbf{f = 20\ GHz}$, and provide design directions. In particular, we compare alternative **CMOS** and **BJT**-based solutions, showing the latter outperforms **CMOS** in this application. Emphasis is on the minimization of $\mathbf{L/Q_T}$ inductor versus quality factor ratio, to further minimize Phase-Noise. Prototypes of the **BJT**-based **VCO** have been fabricated in **55nm BiCMOS** technology by **STMicroelectronics** and were operated at the largest supply and amplitude allowed by reliability constraints to minimize Phase-Noise.

I.9 Thesis Organization

This thesis is organized as follows:

In **Chapter 1**, Phase-Noise specifications for **E-Band LO**-generators are derived. A simplified model to quantitatively estimate the effect of Phase-Noise on signal integrity degradation is described. Next, after introducing some system-level considerations, target noise specifications for the oscillator are deduced and compared with performance of the *State-of-the-Art*. Finally, the proposed frequency synthesizer architecture is discussed.

In **Chapter 2**, considerations on the most suitable topology to adopt in order to decrease Phase-Noise are presented, concentrating among the most adopted

one at *mm-Wave*, namely the *Class-B*, *Class-C* and *Colpitts* **VCO**. The choice between a **BJT**-based and **CMOS**-based implementation is addressed, pointing out the larger **BJT** supply voltage ($\mathbf{V_{DD}}$), hence larger *Oscillation Amplitude* ($\mathbf{A_0}$), and the impact of base-resistance ($\mathbf{r_b}$) on Phase-Noise.

In **Chapter 3**, a Phase-Noise-scaling technique leveraging inductor shrinking is presented. Consideration on the $\mathbf{L/Q_T}$ reduction are pointed out in order to find the ultimate limit for inductor-shrinking.

In **Chapter 4**, practical circuit design details related to the implementation of the aforementioned building blocks in **BiCMOS 55nm** technology are discussed. An overview of the realized test chips is also provided.

In **Chapter 5**, measurement results are presented, and the performance of the proposed circuits is compared with the *State-Of-The-Art*.

In the **last section** conclusions are summarized and the most significant results are presented.

Chapter 1

Phase-Noise And Frequency-Synthesizers Requirements

*Phase-Noise is a key element in many **RF** and radio communications systems as it can significantly affect the performance of systems and induce some undesired phenomena such as reciprocal mixing and noise floor increase. Additionally it can affect the **Bit-Error Rate** (**BER**) on systems using high-order modulation as the phase random fluctuations may just cause a modulation constellation rotation and therefore data corruption.*

*In this **Chapter** a brief overview of Phase-Noise theory in **VCO** is presented. The main system metrics and the sources of non-idealities limiting the system performances are considered. Focus is on the main noise sources in **LC**-oscillators, the design-dependent choices for their minimization and fundamental limits.*

*Then, system-level considerations on the design of frequency synthesizers for **E-Band** backhaul applications are considered outlining the effect of the local-oscillator Phase-Noise on **Signal-to-Noise Ratio** (**SNR**) degradation.*

*The Phase-Noise filtering operations performed by both the **Phase-Locked***

Loop (PLL) *and the baseband* ***Carrier-Phase Estimator CPE*** *is described allowing to set* ***VCO*** *Phase-Noise specifications for* ***M-QAM*** *communications in the* ***E-Band****.*

Finally, the proposed frequency synthesizer architecture is disclosed.

1.1 Introduction to Phase-Noise

In **mmW** transceivers, **PLL** are key building blocks to guarantee the quality of the transmitted and received signal. Frequency of operation and purity of the output signal in oscillators must satisfy stringent specifications set by the system itself.

The output signal produced by an ideal oscillator is perfectly periodic, namely $v(t) = A_0 \cos(\omega_0 t + \phi_0)$, where $\mathbf{A_0}$, ω_0 and ϕ_0 are the oscillation amplitude, the angular frequency and the initial phase respectively, constant over time while zero crossings occur at exact integer multiples of $\tau_0 = 2\pi/\omega_0$ [**44**].

In a real oscillator, however, due to unavoidable presence of noise sources, these quantities change over time causing modulation of the zero crossings. It is possible to divide between amplitude and phase modulation [**44**].

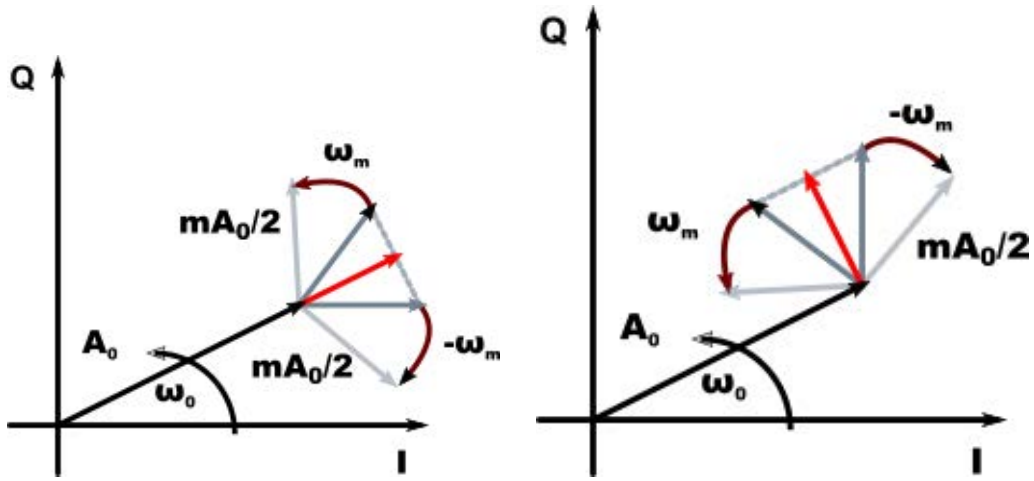
When amplitude modulation (**AM**) is considered, the oscillator output signal can be written as:

$$v(t) = A_0[1 + m \cdot \cos(\omega_m t)] \cos(\omega_0 t + \phi_0) \tag{1.1}$$

where $\mathbf{m \ll 1}$ and $\omega_m \ll \omega_0$. The output spectrum is represented by a Dirac-Delta function at ω_0 which represents the pure oscillation signal, and a couple of side-tones at angular frequencies $\omega_0 \pm \omega_m$. **Eq. 1.1** can be rewritten as:

$$v(t) = A_0 \sin(\omega_0 t) + \frac{mA_0}{2} \cos[(\omega_0 - \omega_m)t] - \frac{mA_0}{2} \cos[(\omega_0 + \omega_m)t] \tag{1.2}$$

Where $\frac{mA_0}{2} \cos[(\omega_0 - \omega_m)t]$ represents the lower side-band and $-\frac{mA_0}{2} \cos[(\omega_0 - \omega_m)t]$ is the upper side-band [**44**]. A representation of the amplitude-modulated



(a) (b)

Figure 1.1: Phasor representation of *(a)* - amplitude modulation (**AM**) *(b)* - phase modulation (**PM**).

carrier (**AM**) through rotating phasors is shown in **Figure. 1.1.a**.

When frequency modulation (**FM**) is considered, the modulated frequency can be written as: $\omega(t) = \omega_0 + \omega_m(t)$.

Since the phase is the integral of the frequency, the output signal can be written as:

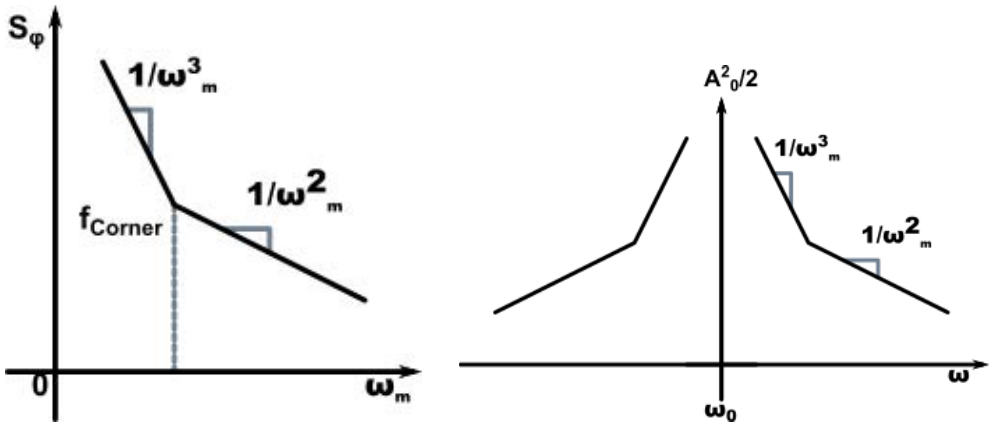
$$v(t) = A_0 \cos\left[\omega_0 t + \phi_0 + \frac{\Delta\omega_0}{\omega_m}\sin(\omega_m t)\right] \tag{1.3}$$

A corresponding phase modulation also occurs in this case, with modulation index $m = \frac{\Delta\omega_0}{\omega_m}$. The resulting phase is:

$$\phi(t) = \Delta\phi \cdot \sin(\omega_m t) \tag{1.4}$$

Where $\Delta\phi = \Delta\omega_0/\omega_m$. If $\Delta\phi \ll 1$ **rad** holds (the so called *narrow band frequency modulation*), the output signal ***v(t)*** is approximated as:

$$\begin{aligned} v(t) &\cong A_0\cos(\omega_0 t + \phi_o) - A_0\sin(\omega_0 t + \phi_0)\cdot\frac{\Delta\omega_0}{\omega_m}\sin(\omega_m t) \\ &= A_0\cos(\omega_0 t + \phi_0) - \frac{A_0}{2}\cdot\frac{\Delta\omega_0}{\omega_m}\cos[(\omega_0 - \omega_m)t] \\ &+ \frac{A_0}{2}\cdot\frac{\Delta\omega_0}{\omega_m}\cos[(\omega_0 + \omega_m)t] \end{aligned} \tag{1.5}$$



(a) (b)

Figure 1.2: *(a)* - Phase and *(b)* - voltage spectrum on a real oscillator.

Figure. 1.2.b shows the phasor representation of the two **PM** side-tones. The ratio between the power of each side-tone and the power of the carrier is known as *Spurious-Free Dynamic Range* (**SFDR**) and is given by:

$$SFDR = \frac{\frac{1}{2}\left(\frac{A_0}{2}\frac{\Delta\omega_0}{\omega_m}\right)^2}{\frac{A_0^2}{2}} = \frac{1}{4}\left(\frac{\Delta\omega_0}{\omega_m}\right)^2 = \left(\frac{\Delta\phi}{2}\right)^2 \tag{1.6}$$

The **SFDR** is equal to half the power of the modulated phase $\phi(t)$ with a spectrum S_ϕ shown in **Figure. 1.2.a**. The **SFDR** is usually expressed in **dBc**, i.e. **dB** with respect to the carrier power. The noise perturbations induced by different noise sources, whose power spreads over a certain frequency interval, are referred to as Phase-Noise. When only white noise is considered, Phase-Noise exhibits a **-20 dB/decade** slope (i.e. S_ϕ is inversely proportional to the square of the frequency offset ω_m), while a $1/\omega_m^3$ dependence (**-30 dB/decade** slope) is present when **1/f** noise occurs. The spectrum of output voltage is a scaled replica of S_ϕ folded around both sides of the carrier, as reported in **Figure. 1.2.b**. The power spectral density at $\omega_0 \pm \omega_m$ of the output voltage is given by $S_V(\omega_0 \pm \omega_m) \cong \frac{S_\phi(\omega_m)}{2}\frac{A_0^2}{2}$. The noise performance of an oscillator are quantitatively assessed, indeed, by defining a suitable *Signal-to-Noise Ratio.*

This figure is the ratio between the output noise power in a **1 Hz** bandwidth at the frequency offset from the carrier and the power of the carrier. This is defined as *Single Side-Band to Carrier Ratio* (**SSCR**).

$$SSCR(\Delta_m) = \frac{S_V(\omega_0 \pm \omega_m)}{A_0^2/2} \cong \frac{S_\phi(\omega_m)}{2} \quad [dBc/Hz] \tag{1.7}$$

When the offset frequency is equal to zero the S_ϕ diverges to ∞. This is related to the narrowband approximation that does not correspond to the real situation when ω_m approaches zero.

In some applications it is more useful to give a characterization of the time deviation of the zero crossings, the so called *jitter*, rather than the voltage spectrum. Jitter is a statistical measure of a noisy oscillation process which is characterized through a *Gaussian* distribution of the oscillation period (different at each cycle due to noise) with a mean value τ_{mean} and a standard deviation.

One of the most known dissertations on the Phase-Noise in an **LC**-oscillator (typical scenario in **LO**-generation) was presented by *Lee* and *Hajimiri* [**45**] by adopting a *Linear Time-Variant* **LTV** model to analyze devices noise injection inside the oscillator, contributing to Phase-Noise. An **LC**-oscillator can be reduced for sake of simplicity to a lossy resonator whose energy lost per cycle (represented by an equivalent parallel resistance $\mathbf{R_T}$) is restored through some active element enabling a constant amplitude oscillation as showed in **Figure. 1.3**.

The only noise contributor is represented by the resonator (assuming noiseless active devices) and can be represented by the equivalent parallel resistance. The energy stored in the Tank is:

$$E_{stored} = \frac{1}{2} C V_{pk}^2 \tag{1.8}$$

where **C** is the capacitance of the resonator and $\mathbf{V_{pk}}$ is the **0-peak** signal

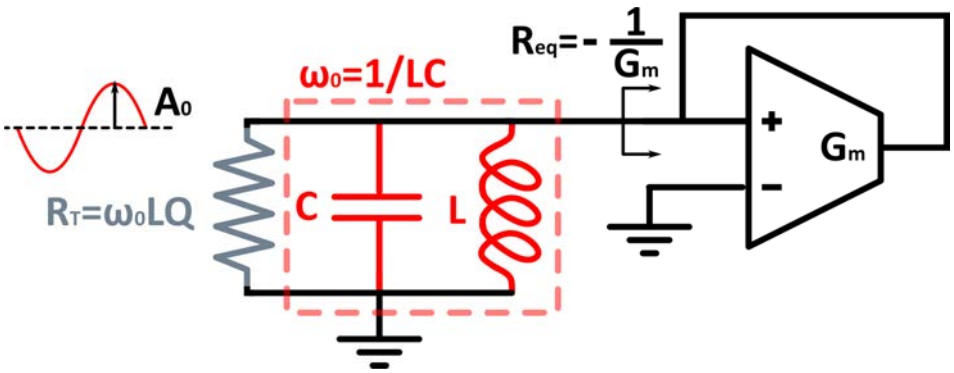


Figure 1.3: LC oscillator equivalent circuit.

voltage amplitude. Thus the mean square signal voltage, assuming a sinusoidal waveform, representing the carrier, is:

$$\bar{V}_{sig}^2 = \frac{E_{stored}}{C} \tag{1.9}$$

Integrating the resistor thermal noise density over the bandwidth of the **RLC** resonator determines the total mean square noise voltage:

$$\bar{V}_n^2 = 4k_BTR\int_0^\infty \left|\frac{Z(f)}{R}\right| df = \frac{4k_BTR}{4RC} = \frac{k_BT}{C} \tag{1.10}$$

It is possible to combine **Eq. 1.8** and **Eq. 1.10** to obtain a noise-to-signal ratio:

$$\frac{N}{S} = \frac{k_BT}{E_{Stored}} \tag{1.11}$$

Taking into account the resonator quality factor $Q = \omega E_{Stored}/P_{diss}$, **Eq. 1.11** can be always written in terms of energy stored and energy dissipated. Therefore:

$$\frac{N}{S} = \frac{\omega k_BT}{QP_{diss}} \tag{1.12}$$

The mean square spectral density of the Tank conductance is therefore:

$$\frac{i_n^2}{\Delta_f} = \frac{4k_BT}{R_T} \tag{1.13}$$

multiplying this current noise density by the effective impedance it produces a voltage noise density. In the aforementioned discussion, it was always assumed that the equivalent impedance of the restoring element is infinite, therefore it does not load the Tank and the impedance seen by the current noise density is the one of a perfect **LC** network. As stated before Phase-Noise is considered at a certain offset frequency from the carrier. Denoting $\Delta\omega$ the offset frequency from the carrier ω_0, the impedance of an **LC** Tank may be approximated by:

$$Z(\omega_0 + \Delta\omega) \sim j\frac{\omega_0 L}{2\Delta\omega/\omega_0} \tag{1.14}$$

The Tank quality factor ($\mathbf{Q_T}$) can be written as function of the parallel impedance resulting in $Q_T = R/\omega_0 L$. Using these expression into **Eq. 1.14** yields:

$$||Z(\omega_0 + \Delta\omega)|| = R\frac{\omega_0}{2Q_T\Delta\omega} \tag{1.15}$$

Multiplying eventually the spectral of the mean square noise current by the squared magnitude of the Tank impedance to obtain the voltage mean square noise spectral density:

$$\frac{\bar{v_n^2}}{\Delta f} = \frac{\bar{i_n^2}}{\Delta f} \cdot ||Z||^2 = 4k_B T R\left(\frac{\omega_0}{2Q_T\Delta\omega}\right) \tag{1.16}$$

The power spectral density of the output noise is frequency dependent because of the filtering action of the Tank, that causes the $1/f^2$ behavior as well. By means of the energy equipartition theorem it can be stated that half of this noise power is amplitude noise while half is Phase-Noise. Therefore the always present amplitude limiting mechanism removes half the noise and only Phase-Noise survives. Performing the normalization to the carrier power leads to the expression for the single sideband noise spectral density:

$$\mathcal{L}(\Delta\omega) = 10\log_{10}\left[\frac{4k_B T R}{A_0^2}\left(\frac{\omega_0}{2Q_T\Delta\omega}\right)^2\right] \tag{1.17}$$

This result states that Phase-Noise at a given offset improves as both the carrier power and **Q** increase. Of course this dependence makes sense since increasing the signal improves the signal to noise ratio, while increasing the quality factor improves quadratically because of the Tank impedance. When aggressive Phase-Noise scaling is performed through an inductance shrinking procedure (as described in **Chapter 3**), a more compact expression (yet effective in identifying the proper knobs to tune in order to address noise reduction) can be found for **Eq. 1.17**. Recalling that the equivalent Tank parallel resistance can be expressed as $R_T = \omega_0 L Q_T$ leads to:

$$\mathcal{L}(\Delta\omega) = 10\log_{10}\left[\frac{k_B T}{A_0^2}\left(\frac{L}{Q_T}\right)\left(\frac{\omega_0^3}{\Delta\omega^2}\right)\left[1+F\right]\right] \tag{1.18}$$

Where also the contribution of other noise sources from active devices and bias circuitry (topology dependent) has been put in evidence through the *Folding-Factor* **F** This result that will be extensively used hereafter shows that Phase-Noise minimization through inductance scaling is provided by reducing the term $\mathbf{L/Q}$ at constant oscillation amplitude provided that $\mathbf{Q_T}$ is constant during the inductance shrinking process (which is not guaranteed for small inductance values).

1.2 Phase-Noise Modelling

In the last decades several models to describe Phase-Noise phenomenon have been proposed, in order to give an analytical expression the the folding factor **F** in the *Leeson's* formula [**Eq. 1.18**] In particular two models have been developed.

- The *Hajimiri-Lee* model based on the so called **Impulse Sensitivity Function** (**ISF**). A linear time variant model of the oscillator;
- A Phasor-Based analysis which is the frequency domain counterpart of the **ISF** [**90**];

Here the **LTV** model of *Hajimiri* is briefly described being more intuitive as the **ISF** predicts noise conversion into Phase-Noise over time. The simple model derived proves useful in giving simple analytical expressions for Phase-Noise calculation providing design insights.

1.2.1 Hajimiri-Lee Model

Hajimiri-Lee model is presented in [**46**] as a general theory for Phase-Noise in electrical oscillators. It is a linear time-variant (**LTV**) model describing the oscillating circuit as system with **n** inputs noise source and two outputs, the instantaneous oscillation amplitude $\mathbf{A_0(t)}$ and phase $\phi\mathbf{(t)}$ of the oscillator respectively. Modelling the noise source as current or voltage generators conveniently, it is possible to define an impulse response function either for the amplitude variations or for phase variation. If a charge pulse is injected as shown in **Figure. 1.4** the amplitude and the phase will change accordingly. The instantaneous voltage change $Delta\mathbf{V}$ is given by **Eq. 1.19**:

$$\Delta V = \frac{\Delta q}{C_{tot}} \tag{1.19}$$

Where $\mathbf{\Delta q}$ is the total injected charge and $\mathbf{C_{tot}}$ is the total capacitance on the node.

The resultant impulse responses are time dependent. If the impulse is applied at the peak of the voltage across no phase shift occurs and only an amplitude is affected. On the other hand, if this impulse is applied at the zero crossing, it has the maximum effect on the excess phase and minor effect on the amplitude. Since some form of amplitude limiting mechanism is essential for stable oscillatory action, the system state will finally reach a stable cycle state. In particular non linearities of the devices act as an automatic gain control. This means that the changes in amplitudes tends to asymptotically fade with time. On the contrary any fluctuation in the phase of the oscillation persists

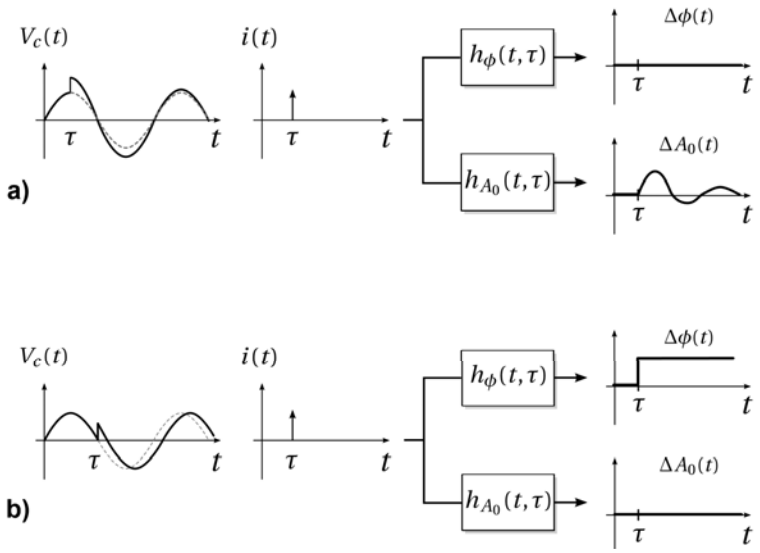


Figure 1.4: Impulse response of an oscillator voltage output waveform to a charge pulse injected *a)* at the peak of the sinusoidal voltage and *b)* at zero crossing.

indefinitely. The unit impulse response for excess phase can be expressed as:

$$h_\phi(t,\tau) = \frac{\Gamma(\omega_0\tau)}{q_{max}} u(t-\tau) \tag{1.20}$$

where $\mathbf{q_{max}}$ is the charge displacement across the capacitor on the node and $\mathbf{u(t\text{-}\tau)}$ is the unit step occurring at time τ. $\mathbf{\Gamma(\omega_0\tau)}$ is the so called *Impulse Sensitivity Function* or **ISF**. It describes how much phase shifts occurs when applying a unit impulse at time t=τ.The output excess phase is therefore:

$$\Delta\phi(t) = \frac{1}{q_{max}} \int_{-\infty}^{t} \Gamma(\tau) i_n(\tau) d\tau \tag{1.21}$$

where $\mathbf{i(t)}$ is the noise current injected into the node of interest. It is possible to state that a noise to phase analysis is twice time-variant, since the transistor noise is generated in a cyclostationary fashion, and the noise to Phase-Noise conversion is itself time-variant.

1.3 Phase-Noise in LC-Tank Oscillators

The conceptual schematic of an **LC**-oscillators is shown in **Figure. 1.3**, where the **LC**-Tank losses are represented by $R_T = Q/\omega_0 C$ and the active components by an energy-restoring block. According to the *Linear Time-Variant* (**LTV**) theory of *Hajimiri* and *Lee* [**46**], the *Impulse Sensitivity Function* (**ISF**) Γ describes the conversion of noise into Phase-Noise. The **ISF** defines the effect of noise on the oscillation phase and is a function of the phase of the Tank voltage. The general expression for the Phase-Noise is:

$$\mathcal{L}(\Delta\omega) = 10\log_{10}\left[\frac{4k_BTR}{A_0^2}\left(\frac{\omega_0}{2Q_T\Delta\omega}\right)^2(\Gamma_{T,rms}^2 + \alpha\Gamma_{M,rms}^2)\right] \tag{1.22}$$

Where k_B is the *Boltzmann*'s constant, **T** the absolute temperature, A_0^2 is the differential oscillation amplitude in the Tank, α is a noise factor that includes in general noise injected by active devices and attenuation between the Tank and **MOS/BJT** gates/bases, $\Gamma_{T,rms}^2$ and $\Gamma_{T,rms}^2$ are the **RMS ISF** for noise injected by $\mathbf{R_T}$ and transistors. Considering a **MOS** implementation, if the transistor current noise power spectral density is proportional to the derivative of the drain current with respect to the gate voltage, for a direct coupling between Tank and transistors, the excess noise factor α is just γ_{MOS}. If a **BJT** solution is adopted, the excess noise factor has a more complicated expression since it accounts for the base-resistance ($\mathbf{r_b}$) noise contribution which is not negligible. More generally, α is proportional to the inverse of the voltage gain between Tank and active devices. In **Colpitts** oscillators this factor is larger than one due to capacitance partition from drain to gate, while when using transformer coupling the factor can be either larger or smaller than one.
Noise from other sources, such as the biasing circuitry or the current source noise conversion into Phase-Noise is here not discussed. The ratio between **RF** power in the Tank $\mathbf{P_{RF}}$ and the **DC** power $\mathbf{P_{DC}}$, called power efficiency (η_P), is expressed in terms of voltage and current efficiencies η_I and η_V as showed

in **Eq. 1.23**.

$$\eta_P = \frac{P_{RF}}{P_{DC}} = \frac{I_{RF}}{I_{DC}} \frac{V_{RF}}{V_D C} = \eta_I \eta_V \tag{1.23}$$

Where $\mathbf{I_{RF}}$ and $\mathbf{V_{RF}}$ are the **RMS** values of the fundamental harmonic components of current and voltage across $\mathbf{R_T}$, $\mathbf{V_{DC}}$ and $\mathbf{I_{DC}}$ are the supply voltage and current. Using **Eq. 1.23** into **Eq. 1.22**, the oscillator's Phase-Noise can be written as:

$$\mathcal{L}(\Delta\omega) = 10 \log_{10} \left[\frac{k_B T R}{A_0^2} \left(\frac{\omega_0}{Q_T \Delta\omega} \right)^2 \frac{\Gamma_{T,rms}^2 + \alpha \Gamma_{M,rms}^2}{\eta_P} \right] \tag{1.24}$$

The main normalized metric which allows a fair comparison between different oscillators is called *Figure of Merit* (**FoM**) and is expressed as:

$$\begin{aligned} FoM &= -10 \log_{10} \left[\mathcal{L}(\Delta\omega) P_{DC,mW} (\frac{\Delta\omega}{\omega_0}) \right] \\ &= \mathcal{L}(\Delta\omega)_{dBc/Hz} + 20 \log_{10} \left(\frac{\Delta\omega}{\omega_0} \right) + 10 \log_{10} \left(\frac{P_{DC}}{1mW} \right) \end{aligned} \tag{1.25}$$

Using **Eq. 1.24** into **Eq. 1.25** leads to the handy expression:

$$FoM = -173.8 \quad dBc/Hz + 10 \log_{10} \left(\frac{\eta_P Q_T^2}{\Gamma_{T,rms}^2 + \Gamma_{M,rms}^2} \right) \tag{1.26}$$

Under the assumptions discussed in [**46**] it can be showed that $\Gamma_{T,rms}^2 = 1/2$. To improve the **FoM** we can act on three fronts. First the Tank $\mathbf{Q_T}$, getting **6 dB** for every doubling of it. Second, on the power efficiency, getting only **3 dB** for every doubling of it. Third, on the **ISF** and excess noise factor of the transistors. Assuming **100%** power efficiency, noiseless transistors and no other noise contribution, the **FoM** can be denoted as $\mathbf{FoM_{MAX}}$: Using **Eq. 1.24** into **Eq. 1.25** leads to the handy expression:

$$FoM = -173.8 \quad dBc/Hz + 10 \log_{10}(2 Q_T^2) \tag{1.27}$$

$\mathbf{FoM_{MAX}}$ is a thermodynamic limit associated with the noise and power dissipation of the unloaded Tank. Expressing the actual **FoM** in terms of $\mathbf{FoM_{MAX}}$ gives the *Excess Noise Factor* (**ENF**):

$$ENF = FoM_{MAX} - FoM = 10\log_{10}\left[\frac{2(\Gamma^2_{T,rms} + \Gamma^2_{M,rms})}{\eta_P}\right] \tag{1.28}$$

The **ENF** defines the distance from the ultimate oscillator performance limit.

Finally, it was noticed that the **FoM** in **Eq. 1.25** does not take into account a metric which is fundamental when designing voltage-controlled oscillators (**VCO**): the frequency *Tuning-Range* (**TR**) [**47**]. Therefore, another figure was introduced to take into account noise, power and Tuning-Range:

$$FoM_T = FoM - 20\log_{10}\left(\frac{TR}{10}\right) \tag{1.29}$$

Since Tuning-Range and Tank quality factor are usually (inversely) correlated, $\mathbf{FoM_T}$ is fairer metric to compare **VCO** performance. Over the last years, many works have been published deriving analytical expressions and theoretical limitations of commonly-used integrated oscillator topologies [**48, 49, 50**] and novel oscillator arrangements [**51, 52, 53, 54**]. Moreover, topology comparisons by virtue of **FoM** or **FoM**-related metrics were carried on [**52, 55, 47**].

1.4 Phase-Noise and SNR Degradation

LO signal purity requirement for **mm-Wave** transceivers, expressed in terms of Phase-Noise constraints, for the **LO** are set by **SNR** degradation concerns [**56**]. Phase-Noise produced in the **LO** impacts on the transmitted and received signal integrity by randomly rotating the symbol constellation as shown in **Figure. 1.5**, degrading **SNR**.

In even-order **M-QAM** modulations, the *Bit-Error Rate* (**BER**) is linked

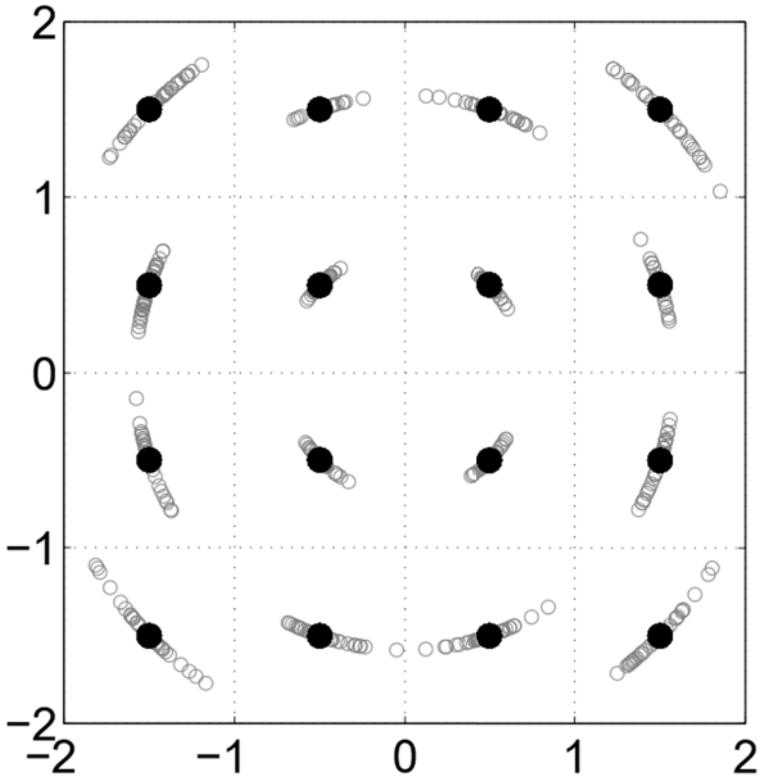


Figure 1.5: 16-QAM constellation in presence of Phase-Noise [**57**].

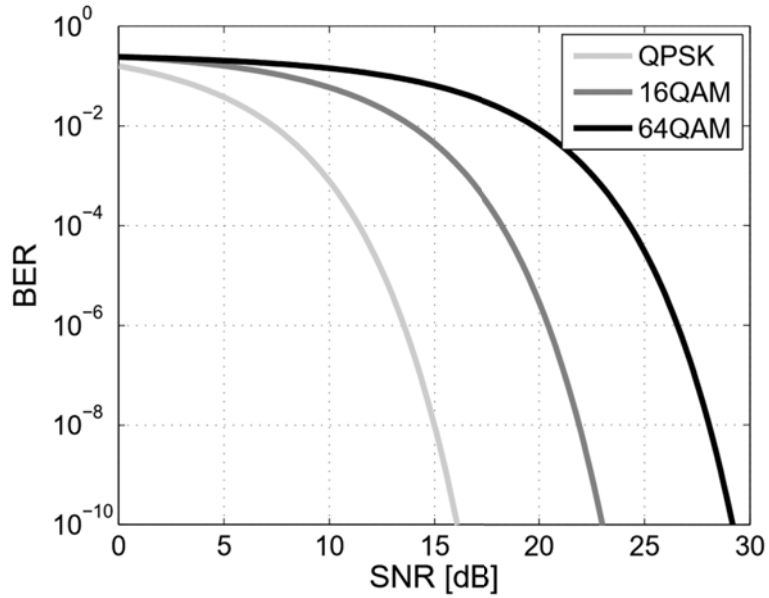


Figure 1.6: BER curves for **QPSK**, **16-QAM** and **64-QAM** modulation according to **Eq. 1.30** [**57**].

to the **SNR** at the detector (**SNRDET**) through the formula [**58**]:

$$BER \approx \frac{4}{\log_2 M}\left(\frac{1}{\sqrt{M}}\right) Q\left[\sqrt{\frac{3}{M-1} SNR_{DET}}\right] \tag{1.30}$$

where **Q** is the well-known Q-function. **BER** curves for different kind of modulations are plotted in **Figure. 1.6**.

It can be noticed that every doubling of the modulation (**M**) order yields **∼3 dB** increase in the **SNR** to achieve the same error probability. Rather complex analytical models have been derived in order to take into account the impact of Phase-Noise on the performance of a communication system **M-QAM** modulation [**59, 60**].

A simple and intuitive yet solid analysis of the correlation between **BER** and Phase-Noise requirements can be derived considering the block diagram shown in **Figure. 1.7**, where an ideal mixer and a noisy Local Oscillator have been assumed. The **LO** integrated Phase-Noise can be approximated as an uncorrelated noise process which degrades the **SNR** of the received signal

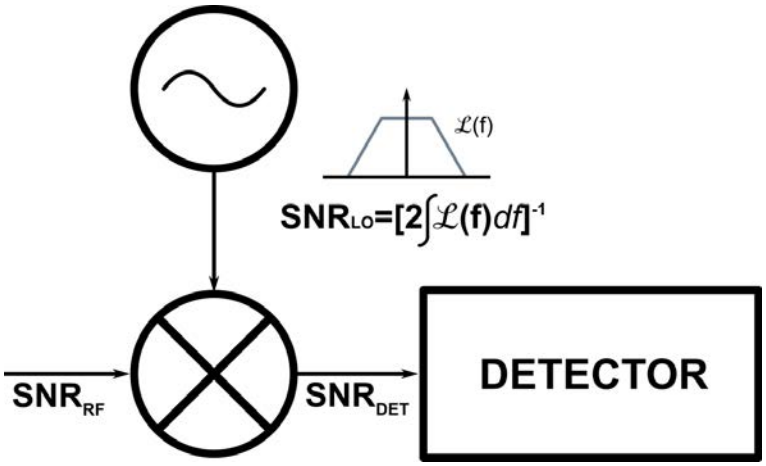


Figure 1.7: Simplified block diagram of the **RX**, stressing the **LO** noise contribution to the received **SNR**.

(**SNRRF**) according to [**62, 61**]:

$$SNR_{DET} \approx \left[\frac{1}{SNR_{RF}} + \frac{1}{SNR_{LO}}\right]^{-1} \tag{1.31}$$

where $SNR_{LO} = [2\int \mathcal{L}(f)df]^{-}1$ is the **SNR** of the local oscillator. The **SNR** degradation resulting from the mixing process can be calculated from **Eq. 1.31** as a function of $\mathbf{SNR_{LO}/SNR_{DET}}$:

$$\left[\frac{SNR_{DET}}{SNR_{RF}}\right]_{dB} = 10\log_{10}\left[1 - \frac{SNR_{DET}}{SNR_{LO}}\right] \tag{1.32}$$

As plotted in **Figure. 1.8.a**, to guarantee negligible noise degradation (i.e. $\mathbf{< 0.5\ dB}$) $\mathbf{SNR_{LO}}$ has to be at least **10 dB** higher than $\mathbf{SNR_{DET}}$. Theref ore, at given **BER**, the higher the modulation index the more challenging are the requirement for $\mathbf{SNR_{LO}}$ and Phase-Noise. To derive **LO** Phase-Noise requirements from $\mathbf{SNR_{LO}}$, the filtering operation performed over noise by both the transmitter and the receiver has to be considered.

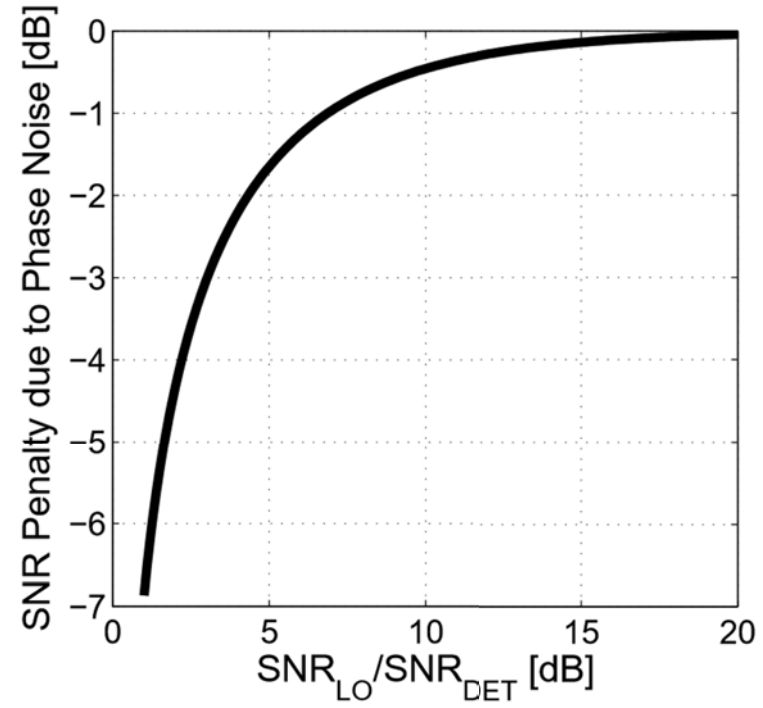
1.4.1 Phase-Noise Filtering

Noise filtering operations on the oscillator Phase-Noise spectrum is performed by two main blocks. The first is the synthesizer **PLL** while the second filtering block is the *Carrier Phase Estimator*, included in the baseband digital front-end. As shown in **Figure. 1.9**, this loop evaluates the phase error of the received constellation and counter-rotates the baseband data stream through a digital phase shifter using the received data as a phase reference. Therefore, it acts as an additional **PLL** high-pass filtering the **LO** Phase-Noise [**63**]. A wideband tracking loop is desirable to filter out most of the synthesizer Phase-Noise.

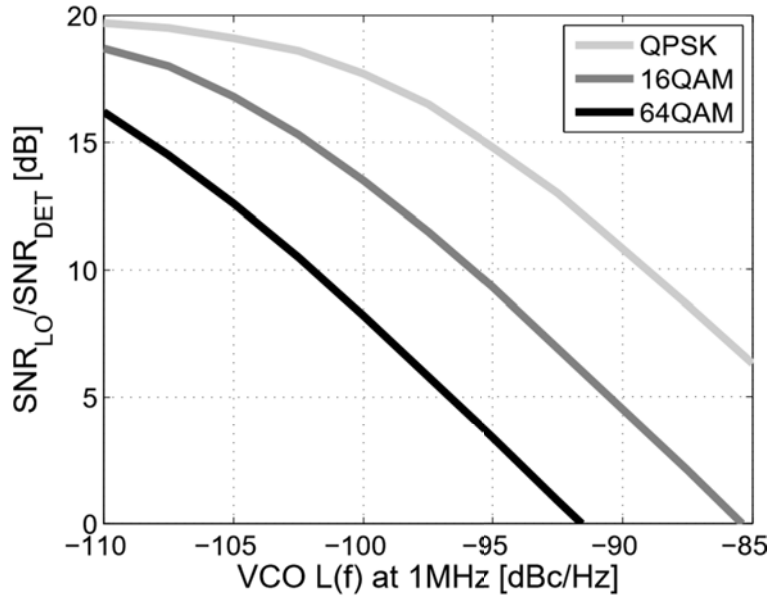
Two main issues limit the loop bandwidth (**BWCT**). First, **BWCT** has to be $\ll$ **1/TS**, where **1/TS** is the symbol rate, for proper loop operation. Also, if the bandwidth is too high, a considerable amount of the **AWGN** channel noise is converted into Phase-Noise, leading to an overall noise penalty [**63**]. According to system level simulations performed in [**64, 65**] and [**57**] **BWCT** $\approx$ **750 KHz** was chosen as a suitable value. Simulations results show that most of the Phase-Noise filtering is performed by the tracking loop and the adoption of a narrowband **PLL** (i.e. $\mathbf{BW_{PLL} < 100\ kHz}$) is beneficial. Indeed, this reduces the in-band noise contribution of loop components and crystal reference, that become significant at **mm-Waves** [**66**].

1.4.2 VCO Phase-Noise Specification

Simulated $\mathbf{SNR_{LO}/SNR_{DET}}$ is plotted in **Figure. 1.8.b** versus **VCO** Phase-Noise at **1 MHz** offset from an **80 GHz** carrier, assuming **250 MHz** channel bandwidth [**26**] for Phase-Noise integration and $\mathbf{SNR_{DET}}$ equal to the minimum **SNR** requirement for $\mathbf{BER = 10^{-6}}$ with the corresponding modulation. To keep $\mathbf{SNR_{LO}/SNR_{DET}}$ above **10 dB** so as to make the oscillator noise contribution negligible, the **VCO** Phase-Noise should be around **-102 dBc/Hz** for **64-QAM**, **-96 dBc/Hz** for **16-QAM** and **-89 dBc/Hz**



(a)



(b)

Figure 1.8: *(a)* **SNR** degradation due to Phase-Noise and *(b)* $\mathbf{SNR_{LO}/SNR_{DET}}$ as function of the oscillator Phase-Noise (at **1 MHz** $\mathbf{\Delta f}$) for different **M**-Modulations. A narrowband **PLL**, a second order tracking-loop filter at the receiver featuring $\mathbf{BW_{TL} = 750\ KHz}$ and the minimum $\mathbf{SNR_{DET}}$ required by each modulation to get $\mathbf{BER = 10^{-6}}$ have been considered in the simulation[**57**].

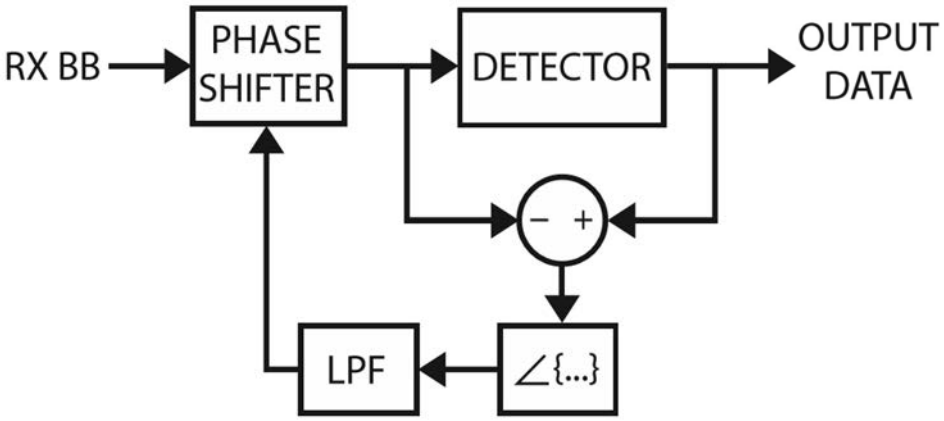


Figure 1.9: Data-aided phase tracking loop block diagram.

for **QPSK**. Therefore, also the oscillator noise specification depends on the modulation order.

The Phase-Noise specification for **64-QAM** is challenging for **mm-Wave** synthesizers, and requires to burn a significant fraction of the transceiver power in **LO** generation. Furthermore, since the **VCO** noise spectrum below **BWCT** is high-pass filtered by the tracking loop, the design of the oscillator has to focus on minimizing Phase-Noise above **1 MHz** offset. but keeping the flicker corner $\mathbf{f_{Corner}}$ below **BWCT**, where the tracking loop is effective.

1.5 Proposed Synthesizer Architecture

VCOs operating above **20 GHz** suffer from severe Phase-Noise degradations due to the poor quality factor of integrated capacitors at **mm-Wave** [**67, 68**]. Indeed, inductive quality factor rises with frequency, but it saturates to **30** above **20-30 GHz** because of skin effect losses [**69**]. Conversely, capacitive **Q** decreases while frequency increases, and becomes the main source of losses at **mm-Waves**. As a result, as shown in **Figure. 1.10** the overall quality factor of the **LC** Tank starts to significantly drop above **20 GHz**, resulting in a Phase-Noise penalty. To maximize the **LC-Tank Q**, the frequency synthesizer architecture in **Figure. 1.11** is proposed.

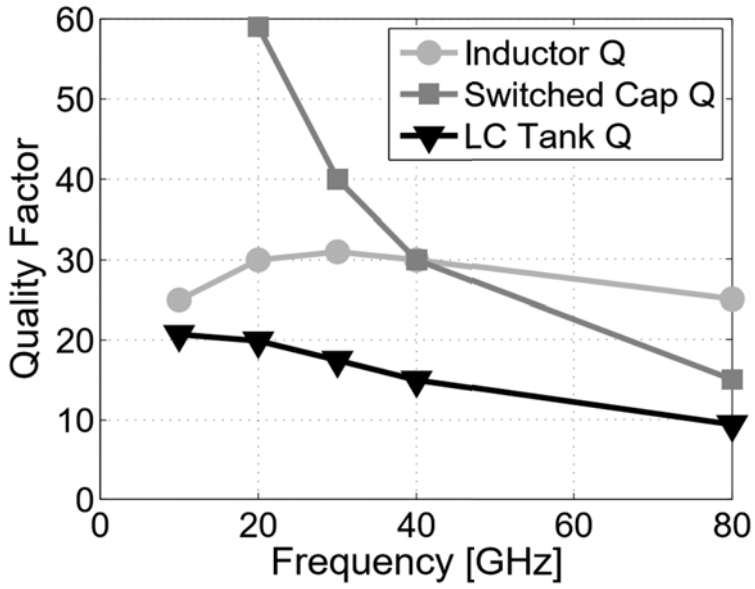


Figure 1.10: Simulated quality factor for integrated inductor, switched capacitor element and equivalent Tank in **55nm BiCMOS** technology.

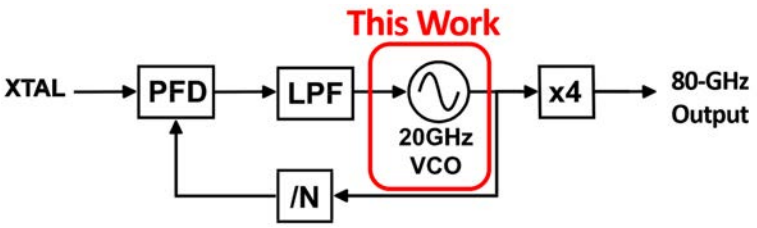


Figure 1.11: Proposed frequency synthesizer.

A **20 GHz VCO**, embedded in a **PLL**, is followed by a *frequency multiplier by 4*. This solution offers other additional advantages. First, a **20 GHz** layout considerably lowers the sensitivity to parasitics, resulting in a wider **VCO** Tuning-Range. Also, one or more power-hungry pre-scaler stages can be avoided in the **PLL** chain, compensating the additional power required by the frequency multiplier. Finally, employing a subharmonic **VCO** allows to reduce the multiplication factor of the **PLL**, resulting in less in-band noise amplification.

The **VCO** has been designed with two targets. First, ultra-low Phase-Noise to achieve negligible **SNR** degradation in **64-QAM** communication.

Chapter 2

Oscillator Topology

*Starting from a brief overview on the **State-Of-The-Art** Oscillators above **10 GHz**, this **Chapter** introduces the main knobs that may be tuned into a **VCO** in order to satisfy the stringent Phase-Noise requirements of the upcoming **5G** standards, giving to the designer some useful guidelines by focusing on the main trade-off, namely Phase-Noise $\mathcal{L}(\Delta f)$ and Tuning-Range (**TR**). The most remarkable trends are highlighted and commented based on equations provided in literature.*

*Then the discussion turns to the identification of the most suitable oscillator topology, among the most solid and robust solutions found in literature, to break the trade-offs and to fit the requirements derived in the **Introduction**. Starting from theoretical Phase-Noise equations derived in previous works on oscillators, the most promising architectures are chosen and compared, declining them in the available **55nm BiCMOS** technology.*

*Finally, focus of this **Chapter** is to compare a fully **CMOS** implementation to a **BJT**-based solution both concentrating on Phase-Noise Vs. Tuning-Range trade-off and performance.*

2.1 mm-Wave VCOs State-Of-The-Art

In the last decade much efforts have been spent to improve **mm-Wave VCOs** performance both in **CMOS** and in **BiCMOS** technologies. Three main characteristics must be emphasized when analyzing and comparing different works from literature:

a) The absolute Phase-Noise performance which is a key aspect to enable high-order modulations with negligible **SNR** degradation;

b) The oscillator power efficiency (**FoM**);

c) The Tuning-Range (**TR**) which is also evaluated through the $\mathbf{FoM_T}$ metric.

Many oscillator solutions have been reported in literature operating at different frequencies in the **mm-Wave** domain, say from **10 GHz** up to **100 GHz**. For fair Phase-Noise comparison it is useful for each oscillator to normalize their performance and derive the equivalent Phase-Noise at **1 MHz** offset from a **20 GHz** carrier, namely the target specification for the **K-Band** oscillator, through the formula:

$$\mathcal{L}_{@20GHz@1MHz-\Delta f} = \mathcal{L}_{@f_0@\Delta f} - 20log_{10}\left(\frac{20 \quad GHz}{f_0}\right) - 20log_{10}\left(\frac{\Delta f}{1 \quad MHz}\right) \tag{2.1}$$

Where $\mathcal{L}_{@f_0@\Delta f}$ is the Phase-Noise reported in literature, measured at an offset frequency Δf from a carrier frequency $\mathbf{f_0}$.

Figure. 2.1 shows the distribution of the absolute Phase-Noise performance in the whole **mm-Wave** range. Works employing similar topologies are grouped together using different colors in order to underline some trends or similar performance. In case of wide variations of the measured Phase-Noise over the Tuning-Range, an intermediate value between $\mathcal{L}_{MAX}$ and $\mathcal{L}_{min}$ has been reported. However the distribution is really sparse since the reported **VCOs** employ different supply voltage ($\mathbf{V_{DD}}$), hence oscillation amplitude ($\mathbf{A_0}$), dif-

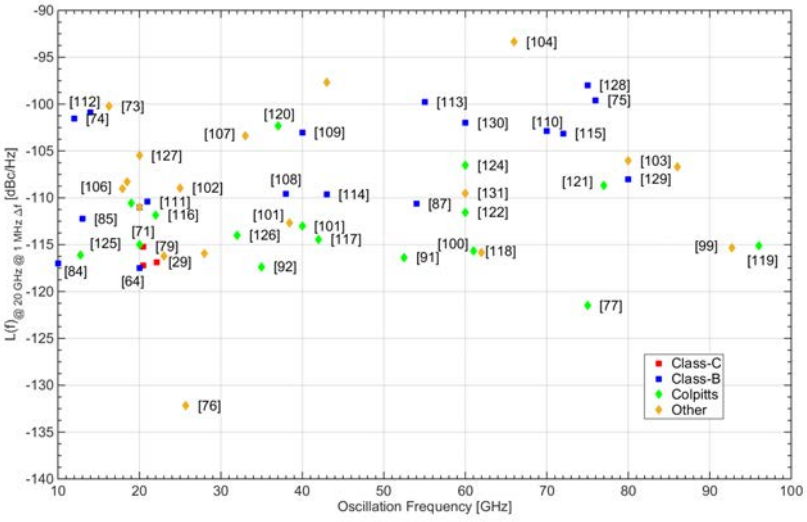


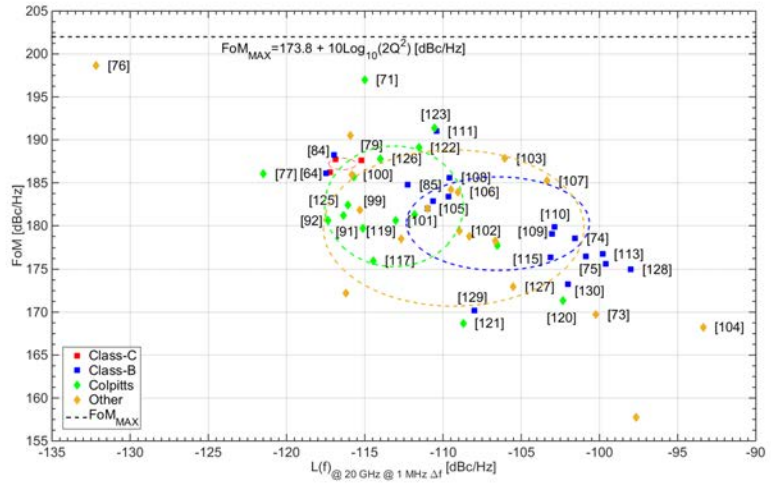
Figure 2.1: **LC**-oscillators equivalent Phase-Noise from the *State-Of-The-Art* normalized at **1 MHz** offset from **20 GHz** carrier. Works are grouped by topology.

ferent Tuning-Range (**TR**) (directly linked to the Tank-$\mathbf{Q_T}$) and different inductor size.

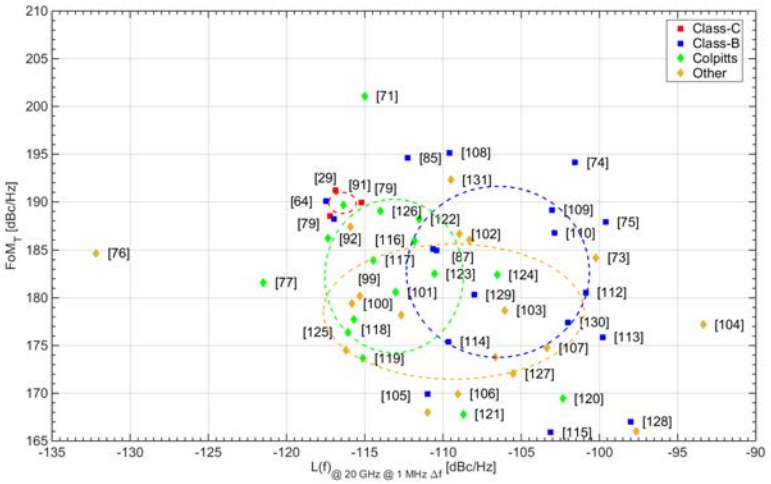
Figure. 2.2.a and **Figure. 2.2.b** show the **FoM** and $\mathbf{FoM_T}$ metric, respectively, grouped by topology, versus $\mathcal{L}_{20GHz@1MHz-\Delta f}$. The dotted ellipses represent an **RMS** performance area for each considered topology.

Bearing in mind **Eq. 1.27** and assuming that for typical inductor values adopted in **mm-Wave LC-VCOs** the Tank quality factor ($\mathbf{Q_T}$) is reasonably **∼20**, the maximum achievable $\mathbf{FoM_{MAX}}$ is in the order of **∼200 dBc/Hz** resulting in at least **10 dB ENF** for the majority of the top performing **VCOs** reported in literature.

This gap from the theoretical $\mathbf{FoM_{MAX}}$ is **5 dB** worse compared to lower frequency **VCOs** (operating below **10 GHz**) as reported in **[70]** showing that design proves critical when frequency ramps up. Indeed second order effects play a key role in determining the oscillator performance, seriously reducing passive components quality factor (i.e. through skin effect) while parasitic capacitors boost phenomena which are barely visible at low frequencies (i.e. substrate



(a)



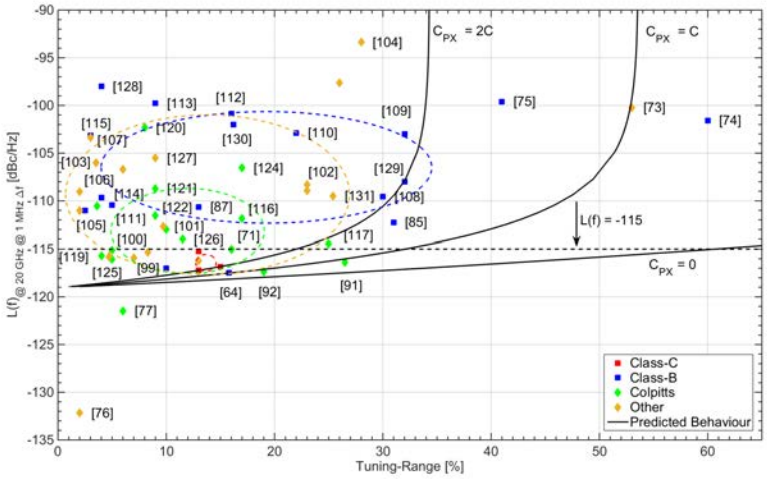
(b)

Figure 2.2: Oscillators **FoM** *(a)* and $\mathbf{FoM_T}$ *(b)* Vs. equivalent Phase-Noise at **1 MHz** offset from **20 GHz** carrier taken from literature. Works are grouped by topology. Circles represent the **RMS** performance area for each topology based on the *State-Of-The-Art* recorded works. The maximum achievable $\mathbf{FoM_{MAX}}$ is reported assuming a reasonable value for **mm-Wave** Tank-$\mathbf{Q_T}$ $\sim$**20** for typical inductance values.

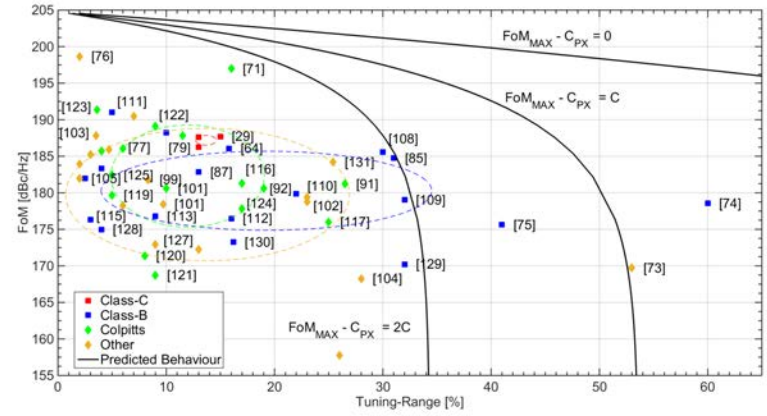
coupling) and therefore contributing to an overall performance degradation.

While absolute Phase-Noise and **FoM** are widely adopted in order to address an oscillator performance, $\mathbf{FoM_T}$ is not able to clearly identify neither an outperforming topology and/or technology nor some trends that could lead to helpful guidelines for the designer. This is because $\mathbf{FoM_T}$ mixes up too many factors and does not put in evidence the major trade-offs
More insight is provided by looking at **Figure. 2.3.a** and **Figure. 2.3.b** where equivalent Phase-Noise and **FoM** performance of oscillators from literature are plotted versus the Tuning-Range grouped by topology.

Given the targeted specs outlined in the **Introduction** (say $\mathcal{L}_{@20GHz@1MHz-\Delta f}$ **< -117 dBc/Hz, TR > 15%**), these data indicate no clear winner and a very large spread within the same architecture, although **Class-B** with tail filter and **Class-C** are the closest to the limit (also **Colpitts** which can be however assimilated to a **Class-C** [**51**]).
First, it can be observed that only a few **VCOs** achieve $\mathcal{L}_{@20GHz@1MHz-\Delta f}$ **< -115 dBc/Hz** (**Figure. 2.2.a**). Most of them are **Colpitts** oscillators in **BiCMOS** technology with high power supply (**2.5-3 V**). High $\mathbf{V_{DD}}$ can be exploited to maximize the oscillation swing, hence minimizing Phase-Noise. Apart from [**71**], the other **VCOs** feature a modest $\mathbf{FoM_T}$, as a consequence of small **TR**, which is inadequate for **E-Band** applications. [**31**], which is also a **BiCMOS VCO** with **3.3 V** supply, but based on a **Class-C** topology, achieves very competitive **FoM** and Tuning-Range. [**65**] and [**72**] are the only **CMOS VCOs** achieving $\mathcal{L}_{@20GHz@1MHz-\Delta f}$ **< -115 dBc/Hz**. The first is a **20 GHz** quad-core **Class-B VCO** exploiting oscillators coupling technique. Phase-Noise performance and **TR** are good but at the cost of large area occupation and layout complexity. The second one is a **28 GHz** oscillator exploiting a **IV**-order Tank to maximize the swing with low supply (**1.2 V**). Although noise and power efficiency are good, it only achieves **TR < 7%**, too small for **E-Band** synthesizers. Also, noise performance varies by several **dBs** over the Tuning-Range.



(a)



(b)

Figure 2.3: Oscillators $\mathcal{L}_{@20GHz@1MHz-\Delta f}$ *(a)* and **FoM** *(b)* Vs. **TR** taken from literature. Works are grouped by topology. Circles represent the **RMS** performance area for each topology based on the *State-Of-The-Art* recorded works. The black lines represent the theoretical Phase-Noise and $\mathbf{FoM_{MAX}}$ Vs. **TR** trends assuming typical **mm-Wave** values for the parameters in **Eq. 1.18** (i.e. Tank-$\mathbf{Q_T}$ $\sim$**20** for typical inductance values adopted in these works). The impact of parasitic capacitors on **TR** performance is put in evidence by changing the relative value with respect to the fixed capacitor.

As far as **TR** is concerned, it can be noticed that three works present an outstanding wide Tuning-Range compared to other solutions. These outliers rely on different mechanism to obtain such a wide Tuning-Range. [**73**] uses a **CB** topology with magnetically-coupled feedback inductor and wide Tuning-Range varactor in a $\mathbf{I_nG_aA_s}$ technology which has lower stray capacitors compared to other technologies. [**74**] and [**75**] implement inductor switching to coarsely tune the oscillator by changing the total Tank inductance and coupling coefficient. This solution however is not prone to achieve extreme low Phase-Noise through inductance shrinking since the inductor $\mathbf{Q_L}$ is preserved if the switches $\mathbf{r_{ON}}$ is negligible compared to inductor series resistance. Since the latter decreases as inductance decreases the overall $\mathbf{Q_L}$ decreases, unless switch size is increased to reduce its **ON**-resistance resulting though in increased parasitic capacitors hence lower **TR**. It should also be noticed that both [**73**] and [**75**] are **10 GHz** oscillators while other works are far beyond **20 GHz** resulting in a design much less sensitive to stray capacitors.
By looking to the top performing **VCOs** in terms of absolute Phase-Noise two works seem to be outstanding. However it must be noticed that [**76**] has a narrow **TR** as [**77**] (hence only inductive-$\mathbf{Q_L}$ counts) and employs a **9 V** supply voltage.

2.1.1 Phase-Noise Vs. Tuning-Range Trade-Off

In order to address the design of a low-Phase-Noise and wide Tuning-Range **VCO** targeting the requirements discussed in the **Introduction**, we introduce in the following equations relating the two metrics deriving a simple yet useful model. For sake of simplicity, the most general concept of **VCO** is considered in **Figure. 2.4**, intended as an **LC** lossy resonator (with Tank quality factor $\mathbf{Q_T}$) and a restoring $\mathbf{G_m}$-Cell.

It is well known that in the typical **LC**-oscillator topologies, coarse tuning to cover the **TR** is digitally performed by connecting/disconnecting portions of

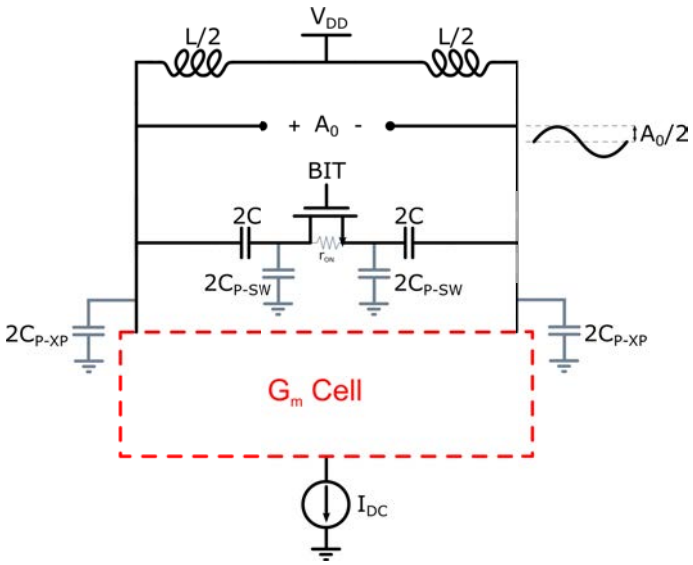


Figure 2.4: Schematic of a **VCO** highlighting the presence of parasitic capacitors affecting the **TR**. Coarse tuning is digitally performed by connecting/disconnecting portions of the capacitor-bank to the output node changing the center oscillation frequency $\mathbf{f_0}$. **2C** is the fixed capacitor while $\mathbf{2C_{P\text{-}XP}}$ and $\mathbf{2C_{P\text{-}SW}}$ are the parasitic capacitors due to the $\mathbf{G_m}$-Cell and switch size (directly trading with the Capacitor-Bank $\mathbf{Q_C}$) respectively.

the capacitor-bank to the output nodes by mean of transistors as exemplified in **Figure. 2.4**. The minimum oscillation frequency ($\mathbf{f_{min}}$) is achieved when the whole capacitor-bank is connected to the output nodes (i.e. the switch is turned on providing a finite **ON**-resistance $\mathbf{r_{ON}}$).

Parasitic capacitors $\mathbf{C_{P\text{-}XP}}$ resulting from the $\mathbf{G_m}$-Cell appear in parallel to the Tank capacitor **C** (**Figure. 2.4**) further reducing $\mathbf{f_{min}}$. The minimum oscillation frequency can be therefore written as:

$$f_{min} = \frac{1}{2\pi}\frac{1}{\sqrt{L(C + C_{P-XP})}} = \frac{1}{2\pi}\frac{1}{\sqrt{LC(1+\beta)}} \tag{2.2}$$

Where $C_{P-XP} = \beta C$. Under this conditions the capacitor-bank $\mathbf{Q_C}$ turns out to be:

$$Q_C = \frac{1}{\omega_0 C r_{ON}} = \frac{W}{\omega_0 C r_{ON \cdot \mu m}} \tag{2.3}$$

Where the switch **ON**-resistance has been linked to the transistor width (**W**

in μ**m**) by defining $r_{ON} = W \cdot r_{ON \cdot \mu m}$ where $r_{ON \cdot \mu m}$ is the $\mathbf{r_{ON}}$ of a minimum-length transistor and **1** μm width at $\mathbf{V_{DS} = 0\ V}$ and maximum $\mathbf{V_{GS}}$ (being the ideal conditions for a transistor to properly work as a switch). It is clear that $r_{ON \cdot \mu m}$ is a technology dependent parameter.

On the other side the maximum oscillation frequency ($\mathbf{f_{MAX}}$) is reached when the whole capacitor-bank is disconnected from the oscillator output nodes (i.e. the switch is in **OFF**-state providing infinite resistance). Under ideal conditions (i.e. no parasitic capacitors) the maximum oscillation frequency would be infinite. In reality it is limited by the presence of unavoidable parasitic capacitors both coming from the $\mathbf{G_m}$-Cell ($\mathbf{2C_{P\text{-}XP}}$) and the capacitor-bank switch ($\mathbf{2C_{P\text{-}SW}}$), highlighted in **Figure. 2.4**, seriously degrading the oscillator **TR**. By looking at **Figure. 2.4**, $\mathbf{2C_{P\text{-}SW}}$ appears in series to the fixed capacitance **2C** (resulting in a total capacitance $2C_H = 2\frac{C \cdot C_{P-SW}}{C + C_{P-SW}}$) when the capacitor-bank is disconnected from the output nodes ($r_{OFF} \sim \infty$), while it is bypassed by transistor $\mathbf{r_{ON}}$ during the **ON**-state provided that its impedance at the oscillation frequency is small enough compared to the parasitic capacitor impedance. Therefore the maximum oscillation frequencies can be written as:

$$f_{MAX} = \frac{1}{2\pi} \frac{1}{\sqrt{L(C_H + C_{P-XP})}} = \frac{1}{2\pi} \sqrt{\frac{\beta + \alpha}{LC[1 + \alpha(1 + \beta)]}} \tag{2.4}$$

Where $C_{P-SW} = \alpha C$ has been used. The parameter $\mathbf{C_{MAX}/C_{min}}$ can be introduced, defined as:

$$\frac{C_{MAX}}{C_{min}} = \frac{C}{C_H} = 1 + \frac{C}{C_{P-SW}} = 1 + \frac{1}{\alpha} \tag{2.5}$$

$\mathbf{C_{P\text{-}SW}}$ can be defined as function of **W** as well introducing the technology-dependent parameter $C_{P-SW/\mu m}$ accounting for the parasitic capacitors per

unit width (expressed in $\mu\mathbf{m}$):

$$C_{P-SW} = W \cdot C_{P-SW/\mu m} \tag{2.6}$$

Defining the maximum versus minimum capacitor ratio when the bank is fully connected/disconnected, accounting for its parasitic capacitors. The Tuning-Range can be expressed as:

$$\begin{aligned} TR = \frac{\Delta f}{f_0} = \frac{f_{MAX} - f_{min}}{\frac{f_{MAX}+f_{min}}{2}} = \\ = 2\frac{\sqrt{(1+\alpha)(1+\beta)} - \sqrt{\beta+\alpha(1+\beta)}}{\sqrt{(1+\alpha)(1+\beta)} + \sqrt{\beta+\alpha(1+\beta)}} \end{aligned} \tag{2.7}$$

In order to link the **TR** to the Phase-Noise and $\mathbf{FoM_{MAX}}$ in **Eq. 1.18** and **Eq. 1.27** through the Tank quality factor $\mathbf{Q_T}$, a relation linking the capacitor-bank $\mathbf{Q_C}$ to the switch parasitic capacitors $\mathbf{C_{P\text{-}SW}}$ and $\mathbf{r_{ON}}$ has to be found. By expressing **W** as function of $\mathbf{Q_C}$ in **Eq. 2.3** and substituting in **Eq. 2.6**:

$$\alpha = \frac{C_{P-SW}}{C} = \omega_0 Q_C \tau_T \tag{2.8}$$

Where $\tau_T = r_{ON\cdot\mu m} \cdot C_{P-SW/\mu m}$ has been introduced.
Reminding that losses in the Tank are both due to the inductor and capacitor-bank (so that the overall Tank quality factor is the parallel combination of the stand alone reactive elements quality factors, $\mathbf{Q_L}$ and $\mathbf{Q_C}$ respectively):

$$Q_T = \frac{Q_L Q_C}{Q_L + Q_C} \tag{2.9}$$

Given the overall observation brought so far, placing **Eq. 2.8** in **Eq. 2.7** brings out an expression linking the **TR** to $\mathbf{Q_C}$ leading to the curves in **Figure. 2.3.a** and **Figure. 2.3.b** derived assuming $\mathbf{L \sim 200\ pH}$, $\mathbf{Q_L \sim 25}$, $\mathbf{A_0 \sim 2\ V}$ and $\mathbf{F \sim 2}$ while the **55nm BiCMOS** technological parameter have been adopted for τ_T. These curves highlight the impact of parasitic capacitors over the

Tuning-Range and capacitor-bank $\mathbf{Q_C}$.

Summing up, achieving $\mathcal{L}_{@20GHz@1MHz-\Delta f}$ **< -115 dBc/Hz** with good power efficiency and wide Tuning-Range (i.e. **> 15%**), as required by high-order-modulation transceivers, is very challenging for integrated **VCOs**. In the following, the most common topologies (say **Class-B**, **Class-C** and **Colpitts**) will be investigated declining them in the **55nm BiCMOS** technology both in a fully **CMOS** and a **BJT** implementation to sort out the best one fitting the design requirements of a Phase-Noise as low as **-117 dBc/Hz**, $\mathbf{f_{Corner}}$ below **700 KHz** and Tuning-Range above **15%**.

2.2 Oscillator Topologies Comparison

By looking at **Eq. 1.18**,it is clear that the key parameter in the Phase-Noise optimization are:

i) Oscillation Amplitude ($\mathbf{A_0}$) which has to be maximized through careful topology choice and design in order not to degrade Phase-Noise performance by pushing active devices in ohmic region changing the noise transfer function and loading the Tank-$\mathbf{Q_T}$;

ii) Inductor size (**L**) must be reduced, while power consumption has to be increased in order to keep the oscillation amplitude constant;

iii) Tank quality factor ($\mathbf{Q_T}$) has to be maximized through an accurate design and optimization of both the inductor and the capacitor-bank;

iv) Folding-Factor (**F**) must be minimized through a suitable topology choice according to the design constraints. A possible way to minimize the folding factor **F** is by using the *Hajimiri* theory which indicate by calculating/simulating **ISF** the effect of different topologies on Phase-Noise.

While Phase-Noise reduction through inductance scaling will be extensively developed in **Chapter 3**, an appropriate choice of the oscillator topology can

significantly improve its performance therefore it is interesting to compare different oscillator topologies and technological implementation to identify the one which best fits the design constraints given in the **Introduction**.

The most adopted solutions (**Figure. 2.3**) for low Phase-Noise and wide Tuning-Range **mm-Wave VCO** are:

1. **a) Class-B** topology;
2. **b) Colpitts** topology;
3. **c) Class-C** topology.

They are mostly implemented in $\mathbf{S_iG_e}$ or **BiCMOS** technology rather than in **CMOS**.

Works presented in **Figure. 2.3.a** have a large performance spread corresponding to the different parameters that may be tuned in order to achieve the specific requirements of the applications or standards (i.e. ultra low Phase-Noise or low power). Therefore the comparison does not highlight a winning topology, even if, by looking at the dotted area, **Colpitts** and **Class-C** topology seem to reach the lowest Phase-Noise with larger power efficiencies.

Several papers in literature address the problem of giving an expression to the *Folding-Factor* (**F**) of **Eq. 1.18**, basing their analysis on the **ISF** calculation and coming up with some handy, closed form equations for the most common topologies both in **CMOS** and **BJT**-based implementations as reported in **Table. 2.1**. Here **k** represents the voltage partition between one

	CMOS	**BJT**	
Topology	$\mathbf{F_I}$	$\mathbf{F_I}$	$\mathbf{F_{r_b}}$
Class-B	γ/k **[48]**	1/2k **[50]**	$\frac{I_{DC}r_b}{3kV_{TH}}$ **[50]**
Class-C	γ/k **[51]**	1/2k **[50]**	$\frac{I_{DC}r_b}{3kV_{TH}}$ **[50]**
Colpitts	$\frac{1-n}{n}\gamma$ **[48]**	(1-n)/2n **[50]**	$\frac{1-n}{4n}\frac{I_{DC}}{V_{TH}}r_b \cdot \frac{B_1(\frac{nA_0}{V_{TH}})}{B_0(\frac{nA_0/2}{V_{TH}})B_1(\frac{nA_0/2}{V_{TH}})}$ **[50]**

Table 2.1: *Folding-Factor* (**F**) expressions in most common **VCOs** topologies.

Tank single-ended output node and the gate/base voltage of the **X-Paired** devices in a **Class-B/C** topology as shown in **Figure. 2.6** and **Figure. 2.15**, while **n** is the **Colpitts** voltage partition between the Tank oscillation amplitude and the emitter as it is showed in **Figure. 2.11**.

A quantitative yet simple analysis of these expressions will be showed in the following where the performance of these architecture will be presented outlining the major trade-offs. A comparison between a **CMOS** versus **BJT** implementation in the **K-Band** will be provided as well for each considered topology. The comparison is performed for a given Tank impedance (**$L = 100$ pH, $Q_L = 19$**), and supply voltage (**$V_{DD} = 1.2$ V**), with the assumption that oscillators exploit the maximum oscillation amplitude allowed by the topology without pushing it in some pathologic conditions.

2.2.1 Class-B Oscillator

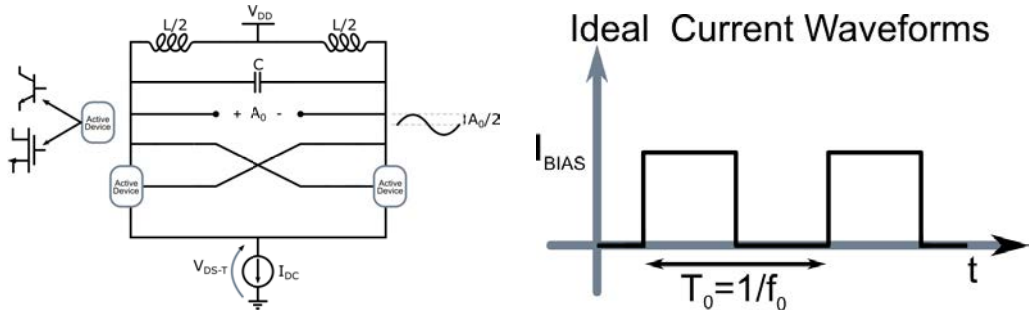
Figure. 2.5.a shows the **Class-B** oscillator and its Tank current waveform usually approximated as a square wave as reported in **Figure. 2.5.b**, assuming negligible parasitic capacitors at the tail current generator. The fundamental component of the **RF** current is $2/\pi$ resulting in a **1st-Harmonic** current of:

$$I_{\omega_0} = \frac{2}{\pi} I_D C \tag{2.10}$$

Assuming that the current generator is not contributing to any noise and that it works under proper bias conditions during the whole oscillation period, the Phase-Noise expressions for for the **CMOS/BJT Class-B** topology can be derived by looking at **Table. 2.1**, resulting in:

$$\mathcal{L}(\Delta\omega)_{CMOS} = \frac{kT}{A_0^2}\left(\frac{L}{Q_T}\right)\frac{\omega_0^3}{\Delta\omega^2}(1+\gamma) \tag{2.11}$$

$$\mathcal{L}(\Delta\omega)_{BJT} = \frac{3}{2}\frac{kT}{A_0^2}\left(\frac{L}{Q_T}\right)\frac{\omega_0^3}{\Delta\omega^2}\left(1+\frac{2}{9}\frac{I_{DC} r_b}{V_{TH}}\right) \tag{2.12}$$



(a) (b)

Figure 2.5: Class-B LC-oscillators and ideal current waveforms from the active device drain/collector.

Where $\mathbf{A_0}$ is the differential **0**-peak oscillation amplitude, **L** and $\mathbf{Q_T}$ are the total inductance and Tank quality factor respectively, and γ is the **MOS** noise factor which is assumed to be $\sim$**2** in deep sub-micron technologies.

In the basic **Class-B** topology the maximum achievable swing is limited by active devices entering ohmic region. When employing bipolars this limitation is more evident since the base-collector junctions of the **X-Pair** devices turn on and the output voltage is clipped. When this occurs, impedance from drain/collectors of the **X-Pair** devices is no more as high as that of a current-source therefore contributing to extra noise by loading the Tank and degrading the overall $\mathbf{Q_T}$. In order to prevent this phenomena the differential oscillation amplitude should be limited to $A_0 \leq V_\gamma$, where $V_{\gamma/th}$ is the built-in voltage in **BJT** or the threshold voltage in **CMOS** ($\sim$**0.5 V**).

Moreover the efficiency

2.2.1.1 AC-Coupled Class-B Oscillator

One way to increase the oscillation amplitude is to use **AC**-coupling to independently bias the gates/bases of **X-Pair** active devices as shown in **Figure. 2.6**. For simplicity **Figure. 2.6** and the followings with **AC**-coupling represent only conceptual schematics where the circuit that set the **DC** bias is not shown. In this topology variation, a fraction of the single ended output

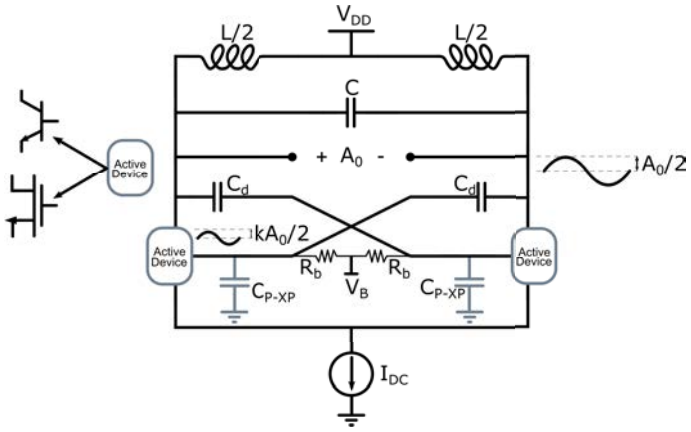


Figure 2.6: **AC**-biased **Class-B** oscillator.

signal is fed-back to the $\mathbf{G_m}$-Cell through the capacitive divider represented by the physical decoupling capacitor $\mathbf{C_d}$ and the parasitic capacitor $\mathbf{C_{P\text{-}XP}}$ on the devices gates/bases.

The feedback factor is given by $\mathbf{k} = \frac{C_d}{C_d + C_{P-XP}}$ and it is $\mathbf{k < 1}$. In this way the oscillation amplitude is decoupled from the conditions required by the active devices to properly work during the whole oscillation period. Furthermore, the gate/base bias voltage $\mathbf{V_B}$ can be set lower than $\mathbf{V_{DD}}$, provided that enough voltage room is left for the current source (i.e. **0.2 V**). Under this conditions, the maximum oscillation amplitude is set by:

$$\begin{aligned} V_{DD} - \frac{A_{0-MAX}}{2} &\geq V_B + k\frac{A_{0-MAX}}{2} - V_{\gamma/th} \\ A_{0-MAX} &\leq 2\frac{V_{DD} - V_B + V_{\gamma/th}}{1+k} \end{aligned} \tag{2.13}$$

It can be noticed that $\mathbf{A_{0\text{-}MAX}}$ depends on the feedback factor $\mathbf{k}$ since the smaller the signal on the gate/base the smaller the risk for the device to enter ohmic region of operation.

Again it is possible to derive the Phase-Noise expression for the **AC**-coupled **CMOS Class-B** topology by rewriting **Eq. 2.11** and **Eq. 2.11** by taking into

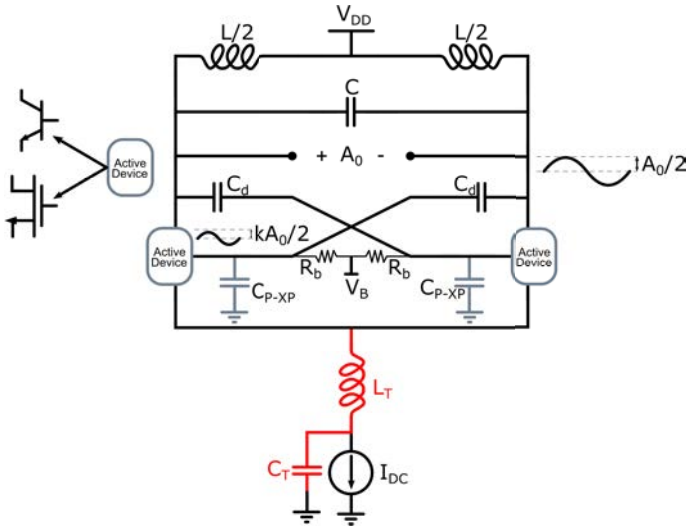


Figure 2.7: Oscillators with second-harmonic **LC** tail filter.

account the feedback factor **k**:

$$\mathcal{L}(\Delta\omega)_{CMOS} = \frac{KT}{A_0^2}\left(\frac{L}{Q}\right)\left(\frac{\omega_0^3}{\Delta\omega^2}\right)\left[1+\frac{\gamma}{k}\right] \tag{2.14}$$

$$\mathcal{L}(\Delta\omega)_{BJT} = \frac{KT}{A_0^2}\left(\frac{L}{Q}\right)\left(\frac{\omega_0^3}{\Delta\omega^2}\right)\left[1+\frac{1}{2k}+\frac{I_{DC}r_b}{3kV_{TH}}\right] \tag{2.15}$$

2.2.1.2 Class-B Oscillator With Tail Filter

While **Eq. 2.14** and **Eq. 2.15** where derived under the assumption that noise comes only from the Tank and **X-Pair** devices, a more realistic situation sees the current source as one of the major noise sources. It has been demonstrated by [**48**] that the current source contributes Phase-Noise proportionally to its $\mathbf{g_{mT}}$. Its contribution can be indeed decreased by letting the **X-Pair** devices switch more softly.

A solution to reduce this noise source is to filter it out by placing an additional **LC**-Tank, resonating at $2\omega_0$ (since the common source node oscillates at $2\omega_0$), at the tail of a **Class-B** oscillator [**78**] as showed in **Figure. 2.7**. Three remarkable advantages are obtained:

i) The common source node can swing below ground, thus increasing the

for further oscillation amplitude increase;

ii) **X-Pair** devices can deeper enter in ohmic region without loading the Tank since they see a high impedance in series with them;

iii) Noise of the current source around $2\omega_0$ (down-converted to ω_0 due to the **X-Pair** mixing) can be filtered out by using a large capacitance $\mathbf{C_T}$.

By carefully design the $\mathbf{2_{nd}}$ harmonic tail filter, noise from current source can be canceled out and **Eq. 2.14** and **Eq. 2.15** still hold.

2.2.1.3 AC-Coupled Class-B VCO: CMOS Vs. BJT

To reach low Phase-Noise a fair comparison the oscillation amplitude at given supply voltage ($\mathbf{_{DD}}$) must be maximized.

Assuming a $\mathbf{V_{DD}}$ of **1.2 V**, a reasonable value for $\mathbf{V_B}$ is **0.85 V**, leaving sufficient voltage headroom to the current source (both in the **CMOS** and in the **BJT** version) to properly operate without loading the Tank-$\mathbf{Q_T}$ factor.

The presence of the **BJT** base-resistance noise ($\mathbf{r_b}$) inside **Eq. 2.15** prevents an immediate intuition and comparison between the **BJT** and **CMOS** implementations. Indeed it cannot be neglected in Phase-Noise calculations since it contributes to a significant percentage of the total Phase-Noise. Without proper minimization, Phase-Noise may be degraded by several **dBs**.

Inserting **Eq. 2.13** in **Eq. 2.14** and **Eq. 2.15** and assuming with good approximation that the current waveform is well approximated by a square wave at ω_0 fundamental harmonic, the current **DC-to-RF** efficiency is $2/\pi$ so that $A_{0-MAX} = \frac{2}{\pi} I_{DC} R_T$, resulting in:

$$\mathcal{L}(\Delta\omega)_{CMOS} = \frac{KT}{A_0^2}\left(\frac{L}{Q}\right)\left(\frac{\omega_0^3}{\Delta\omega^2}\right)\left[1+\frac{\gamma}{k}\right] \tag{2.16}$$

$$\mathcal{L}(\Delta\omega)_{BJT} = \frac{KT}{A_0^2}\left(\frac{L}{Q}\right)\left(\frac{\omega_0^3}{\Delta\omega^2}\right)\left[1+\frac{1}{2k}+\frac{\pi(V_{DD}-V_B+V_{\gamma/th})r_b}{6kV_{TH}R_T(1+k)}\right] \tag{2.17}$$

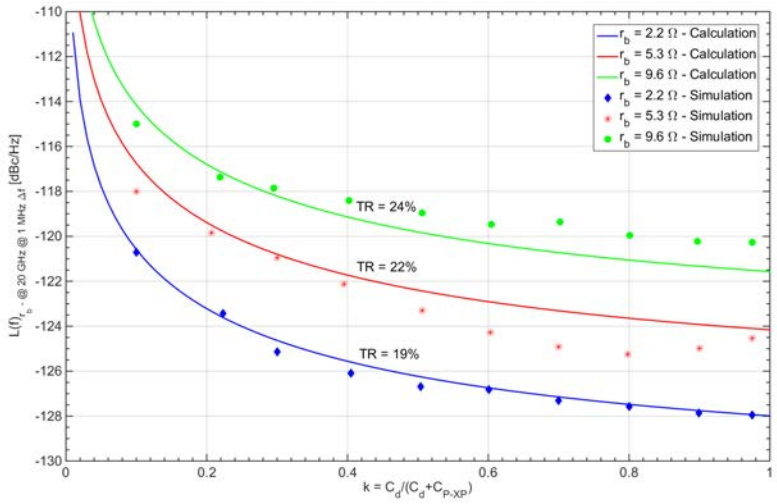
The Impact of base-resistance on Phase-Noise is highlighted in **Figure. 2.8.a**

where the Phase-Noise injected by $\mathbf{r_b}$ only in a **Class-B VCO** is showed for three different values of $\mathbf{r_b}$ corresponding to three different size of the **X-Pair** devices. For each **k** value the oscillation amplitude is maximized according to **Eq. 2.13**. Equations fit simulation results pretty well showing that as the device emitter area increases, the contribution of the base-resistance noise to the output scales down. At the same time, more parasitic capacitance is loading the Tank, penalizing the Tuning-Range.

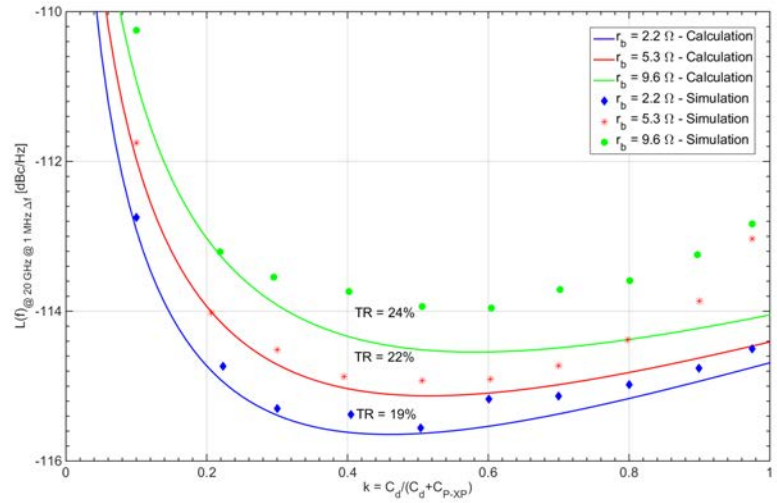
The curve plotted for $\mathbf{r_b = 2.2\ \Omega}$ in **Figure. 2.8.a** corresponds to the maximum device size allowed by the **55nm BiCMOS** technology. **Figure. 2.8.b** plots the overall **Class-B VCO** Phase-Noise in the same conditions of **Figure. 2.8.a** showing that the base-resistance noise contribution can degrade Phase-Noise by at least **2-3 dBs** and even more if not correctly addressed.

Since the **VCO** operates in **Class-B**, the capacitive divider realized by $\mathbf{C_d}$ and $\mathbf{C_{P\text{-}XP}}$ plays a very important role. If the Tank voltage swing is too large when fed to the transistors gate/base, it drives the device in ohmic region, thus degrading Phase-Noise performance. On the other hand, if the division ratio is high to attenuate the signal at gate/base input avoiding ohmic region of operation, the device current noise increases. **Figure. 2.9** shows Phase-Noise simulations versus the capacitive division ratio $\mathbf{k = C_d/(C_d+C_{P\text{-}XP})}$ both for the **CMOS** and **BJT** implementation. For low values of **k**, the voltage swing at the base is small and Phase-Noise increases. When **k** is close to **1**, the impact of the base-resistance is minimized, but Phase-Noise is increased by devices entering ohmic region. The best Phase-Noise is found around $\mathbf{k = 0.6}$ and is mildly dependent on the value of **k**.

A set of simulations have been performed for different $\mathbf{C_{MAX}/C_{min}}$ (**1.2**, **1.7** and **3.5**) capacitor-bank ratio (assuming a Capacitor-Bank structure similar to the one in **Figure. 2.4**) and by scaling the size of the active devices using $\mathbf{k = 0.6}$. Phase-Noise, as a function of the Tuning-Range, is reported in **Figure. 2.10**. If $\mathbf{C_{MAX}/C_{min}}$ is low, the quality factor of the capacitor-bank is high, and quality factor of the overall Tank is dominated by the inductor.



(a)



(b)

Figure 2.8: Base-resistance impact on Phase-Noise performance in **AC**-biased **Class-B** oscillators at maximum oscillation amplitude: *(a)* $\mathcal{L}_{r_b-@20GHz@1MHz-\Delta f}$ Vs. **k** and *(b)* $\mathcal{L}_{TOT-@20GHz@1MHz-\Delta f}$ Vs. **k** at different **X-Pair** devices size (hence $\mathbf{r_b}$ and **TR**).

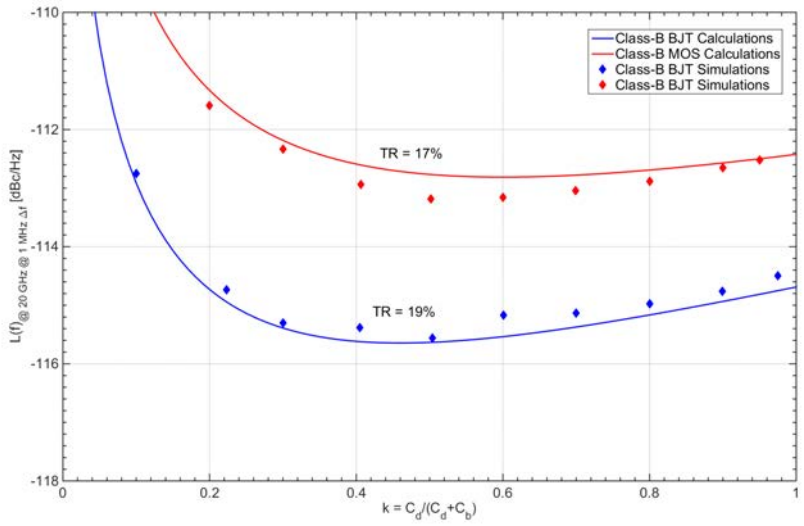


Figure 2.9: BJT Vs. CMOS $\mathcal{L}_{@20GHz@1MHz-\Delta f}$ at different **k** in **AC**-biased **Class-B** oscillators. The **BJT** dimensions are the maximum allowed by technological constraint and allows to reduce the base-resistance $\mathbf{r_b}$ to **2.2** Ω.

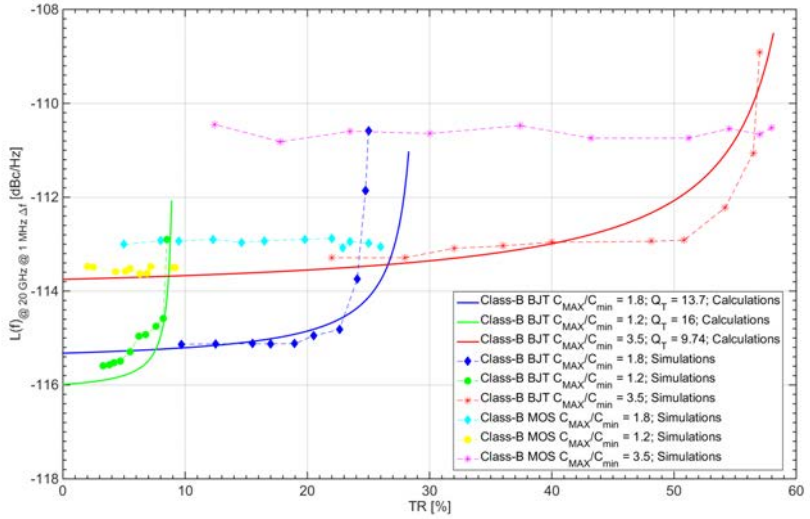


Figure 2.10: BJT Vs. CMOS $\mathcal{L}_{@20GHz@1MHz-\Delta f}$ at different **TR** in **AC**-biased **Class-B** oscillators for $\mathbf{k = 0.6}$.

On the other hand, when $\mathbf{C_{MAX}/C_{min}}$ is high, a wider Tuning-Range is achieved at the expense of Phase-Noise. By inspecting the entire **TR** at a fixed $\mathbf{C_{MAX}/C_{min}}$, the contribution of the base-resistance noise to the Phase-Noise is predominant (in the **BJT** implementation) when larger Tuning-Ranges are targeted because they require a small **BJT** device size. On the other hand, as expected, **MOS** implementation shows a Phase-Noise which is independent on the device size and therefore on **TR** remaining constant over the whole spanned Tuning-Range.

2.2.2 Colpitts Oscillator

Another oscillator topology that is commonly used, especially in the implementation of **BJT**-based oscillators above **10 GHz** (**Figure. 2.1**), is the differential **Colpitts** oscillator showed in **Figure. 2.11.a**. Positive feedback is achieved by means of a capacitive voltage divider between the drain/collector and source/emitter of the core active devices implemented through $\mathbf{C_1}$ and $\mathbf{C_2}$. The feedback factor is expressed as:

$$n = \frac{C_1}{C_1 + C_2} \tag{2.18}$$

In a **Colpitts** oscillator, at resonance, impedance of capacitor $\mathbf{C_2}$ should be far larger than the source impedance ($\sim\mathbf{1/g_m}$) to preserve the feedback. For a $\mathbf{g_m}$ in the order of **20-30 mS** and even more in ultra low Phase-Noise **K-Band VCOs**, $\mathbf{C_2 = 300\ fF}$ allows to both asses the feedback robustness and the insensitivity of the feedback factor **n** to parasitic capacitor from the active devices.

In a **Colpitts** architecture the Tank capacitor resonating with the inductor is made up by two parts:

i) The main Tank capacitor **C** between the two differential output nodes;

ii) The capacitive voltage divider consisting of an overall capacitor $\mathbf{C_H} =$

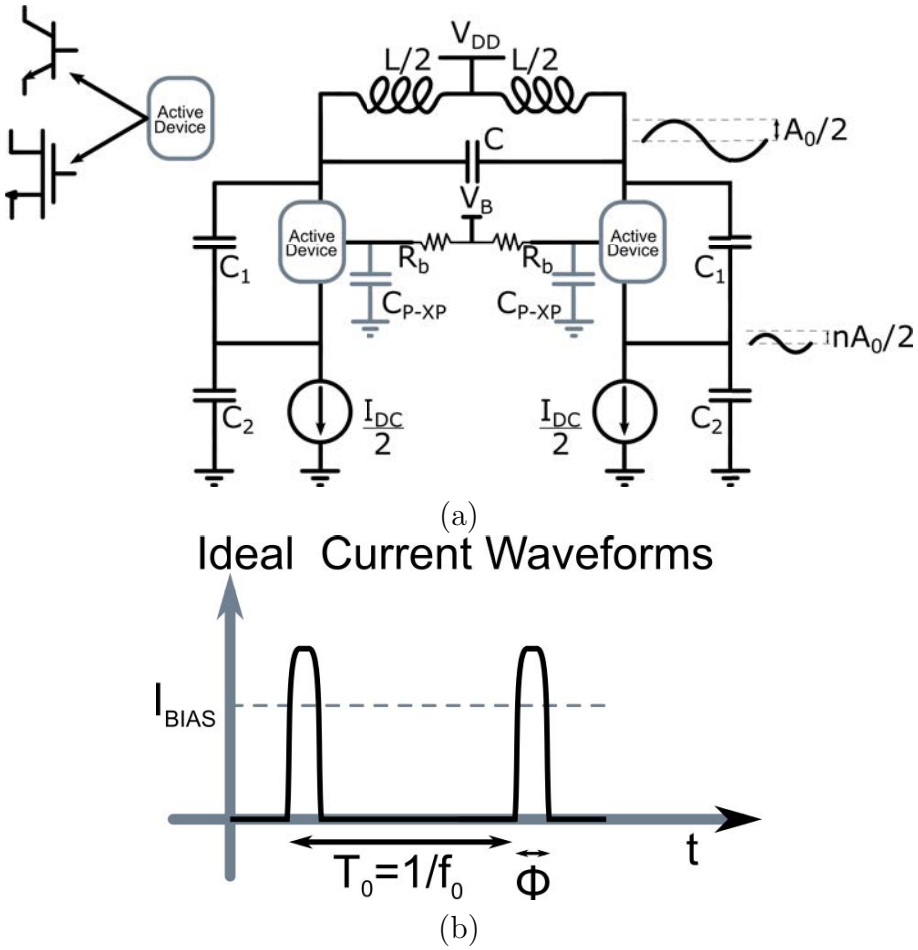


Figure 2.11: Colpitts-oscillators and ideal current waveforms from the active device drain/collector.

$\mathbf{nC_2}$.

The capacitive divider acts as a parasitic capacitor from each differential output node toward ground therefore loading the Tank and reducing the maximum attainable Tuning-Range. In principle $\mathbf{C_2}$ could be tuned as well as the main Tank capacitor through some switches. The drawback would be however a Tuning-Code dependent feedback factor **n** which would not be optimal for Phase-Noise minimization across the whole Tuning-Range.

The presence of a large capacitance at the source/emitter of the switching devices, makes current waveform resemble short and narrow pulses rather than square waves (as in the **Class-B** architecture in **Figure. 2.5.b**) as showed in **Figure. 2.11.b**. The conduction angle Φ (the portion of the oscillation period when the device injects current and noise inside the Tank) is smaller compared to **Class-B** and it defines a **Class-C** operation which will be better analyzed in the following section.
It must be however noted that, despite the **Colpitts** oscillator operates itself in **Class-C** regime, $\mathbf{V_B}$ cannot be set as low as in the **Class-C** differential **LC**-oscillator since a voltage ripple as large as $\mathbf{A_s=nA_0/2}$ exists at the source/emitter of the switching devices posing more stringent conditions for the switching devices bias conditions in order to avoid current source entering ohmic region of operation. Hence the minimum source/emitter voltage must be large enough to leave an adequate voltage headroom to the current sources. Naming $\mathbf{V_B}$, the biasing voltage at the gates/bases of the switching devices in a **Colpitts** oscillator and $\mathbf{V_B}$ the biasing voltage in a **X-Coupled Class-C** oscillator, a relation can be derived:

$$V_{B'} = V_B + \frac{nA_0}{2} \tag{2.19}$$

Meaning that for the same oscillation amplitude, $\mathbf{V_B}$, has to be at least increased by $\mathbf{nA_0/2}$ to avoid pathologic behavior of the current source. Therefore the maximum oscillation amplitude as function of the feedback factor can

be derived from the simple equation:

$$V_{DD} - \frac{A_{0-MAX}}{2} \geq V_{B'} - V_{\gamma/th} \tag{2.20}$$

Resulting in:

$$A_{0-MAX} = 2\frac{V_{DD} - V_B + V_{\gamma/V_{th}}}{1+n} \tag{2.21}$$

By looking at **Table. 2.1** and neglecting other noise sources from the bias circuitry, the Phase-Noise equations for **MOS** and **BJT Colpitts VCOs** are:

$$\mathcal{L}(\Delta\omega)_{CMOS} = \frac{kT}{A_0^2}\left(\frac{L}{Q_T}\right)\frac{\omega_0^3}{\Delta\omega^2}\left(1+\gamma\frac{1-n}{n}\right) \tag{2.22}$$

$$\begin{aligned}\mathcal{L}(\Delta\omega)_{BJT} =& \frac{kT}{A_0^2}\left(\frac{L}{Q_T}\right)\frac{\omega_0^3}{\Delta\omega^2}\left[1+\frac{1-n}{2n}+\frac{1-n}{4n}\frac{I_{DC}}{V_{TH}}r_b\cdot\right.\\ &\left.\frac{B_1(\frac{nA_0}{V_{TH}})}{B_0(\frac{nA_0/2}{V_{TH}})B_1(\frac{nA_0/2}{V_{TH}})}\right]\end{aligned} \tag{2.23}$$

Where $\mathbf{B_0(X)}$ and $\mathbf{B_1(X)}$ are the modified *Bessel* functions of order zero and one respectively.

2.2.2.1 Colpitts VCO: CMOS Vs. BJT

By expressing **Eq. 2.22** and **Eq. 2.23** as function of **n** through **Eq. 2.21**, a comparison between **CMOS** and **BJT** implementation at maximum oscillation amplitude is possible:

$$\mathcal{L}(\Delta\omega)_{CMOS} = \frac{kT}{(V_{DD}-V_B+V_{\gamma/th})^2}\left(\frac{L}{Q_T}\right)\frac{\omega_0^3}{\Delta\omega^2}(1+n)^2\left(1+\gamma\frac{1-n}{n}\right) \tag{2.24}$$

$$\begin{aligned}\mathcal{L}(\Delta\omega)_{BJT} =& \frac{kT}{(V_{DD}-V_B+V_{\gamma/th})^2}\left(\frac{L}{Q_T}\right)\frac{\omega_0^3}{\Delta\omega^2}(1+n)^2\cdot\left[1+\frac{1-n}{2n}+\right.\\ &\left.\frac{1}{4n(1+n)}\frac{(V_{DD}-V_B+V_{\gamma/th})}{V_{TH}R_T}r_b\cdot\frac{B_1(\frac{nA_0}{V_{TH}})}{B_1^2(\frac{nA_0/2}{V_{TH}})}\right]\end{aligned} \tag{2.25}$$

Firstly the problem of reducing the contribution of base resistance to the Phase-Noise is addressed in **Figure. 2.12** by increasing the size of the switching

transistors but with penalty on the Tuning-Range. A minimum is found around $\mathbf{n = 0.6}$.

As shown in **Figure. 2.13**, a marginal improvement of the Phase-Noise is achievable in the **Colpitts** oscillator at small values of **n** for a fixed amplitude of oscillation. At large values of **n CMOS** implementation outperform **BJT** implementation by **1 dB** although the increase in the current consumption, as predicted by **Eq. 2.21**, is substantial as only a fraction of the bias current (**1-n**) flows through the Tank increasing the oscillation amplitude. The rest recirculates inside the capacitive divider which enable positive feedback sustaining oscillation.

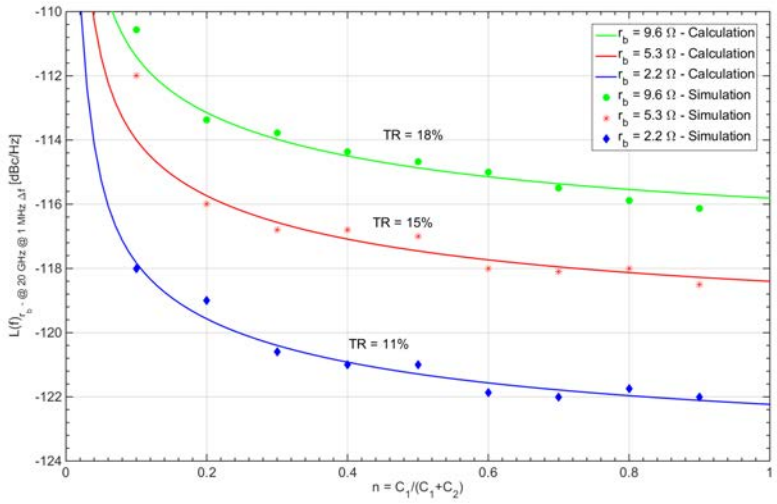
Finally as it can be seen from **Figure. 2.14** the **TR** is limited to few percentage even when a large $\mathbf{C_{MAX}/C_{min}}$ is adopted. This is mainly caused by the capacitive voltage divider which seriously loads the Tank.

2.2.3 Class-C Oscillator

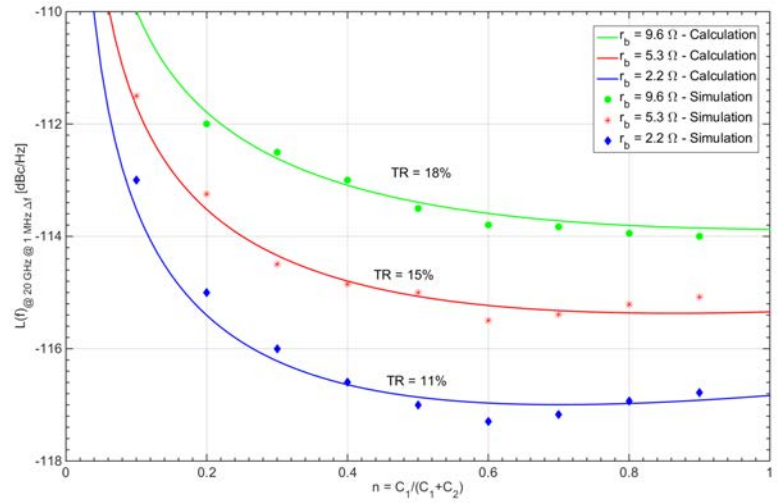
Figure. 2.15 shows the schematic of The **Class-C** oscillator. It can be viewed as the optimal evolution of the two oscillator architectures discussed in **Section 2.2.1** and **Section 2.2.2** [**51**].

Class-C schematic is the same as the **Class-B** with the addition of a large capacitance $\mathbf{C_2}$ in parallel to the current source. Despite the apparent similarity to the **Class-B**, the two topologies behave very differently. The oscillation frequency is determined by the Tank capacitance only, which is beneficial for the achievable tuning range, since there is no longer the need of a fixed loading the Tank. The Tuning-Range performance therefore should improve comparing to **Colpitts** and resemble the **Class-B** one.

Capacitor $\mathbf{C_2}$ should be chosen very large, to minimize the feedback from devices source to Tank. With large $\mathbf{C_2}$, the voltage ripple on the common-mode source (showing an oscillation at $\mathbf{2}\omega_0$) is very small since it represents a small impedance toward ground at **mm-Wave** frequencies assuming in the



(a)



(b)

Figure 2.12: Base-resistance impact on Phase-Noise performance in **Colpitts** oscillators at maximum oscillation amplitude: *(a)* $\mathcal{L}_{r_b-@20GHz@1MHz-\Delta f}$ Vs. **k** and *(b)* $\mathcal{L}_{TOT-@20GHz@1MHz-\Delta f}$ Vs. **n** at different **X-Pair** devices size (hence $\mathbf{r_b}$ and **TR**).

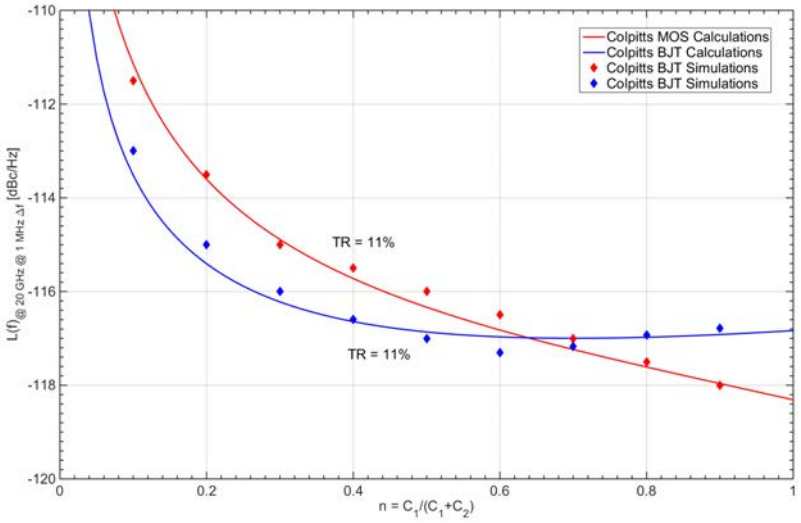


Figure 2.13: BJT Vs. CMOS $\mathcal{L}_{@20GHz@1MHz-\Delta f}$ at different **n** in **Colpitts** oscillators. The **BJT** dimensions are the maximum allowed by technological constraint and allows to reduce the base-resistance $\mathbf{r_b}$ to **2.2** Ω.

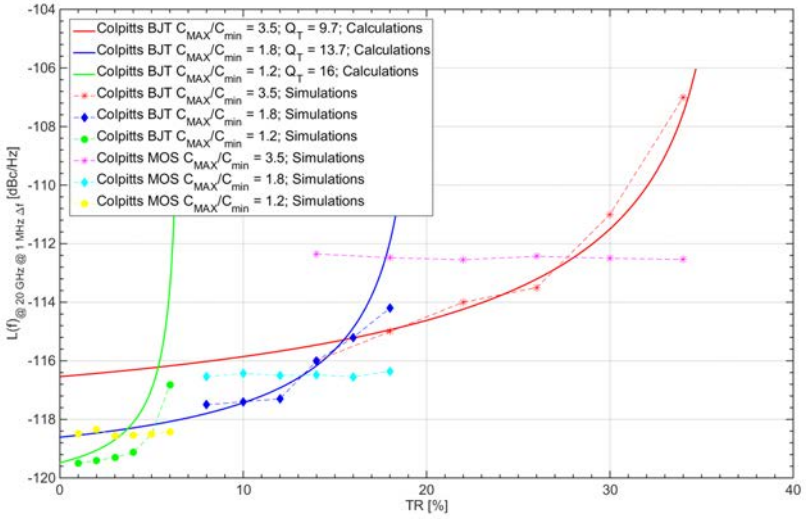


Figure 2.14: BJT Vs. CMOS $\mathcal{L}_{@20GHz@1MHz-\Delta f}$ at different **TR** in **Colpitts** oscillators for $\mathbf{n = 0.6}$.

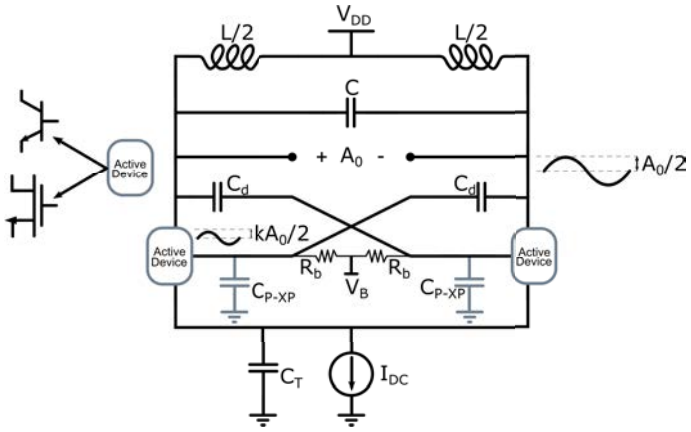


Figure 2.15: **AC**-biased **Class-C** oscillator.

analysis that its impedance at $\mathbf{2}\omega_0$ is much smaller than that from the device source ($\mathbf{g_m}$).

From [**51**] and [**79**] the Phase-Noise expression for the **CMOS** and **BJT** **Class-C** oscillator are respectively:

$$\mathcal{L}(\Delta\omega)_{CMOS} = \frac{kT}{A_0^2}\left(\frac{L}{Q_T}\right)\frac{\omega_0^3}{\Delta\omega^2}\left(1+\frac{\gamma}{k}\right) \tag{2.26}$$

$$\mathcal{L}(\Delta\omega)_{BJT} = \frac{3}{2}\frac{kT}{A_0^2}\left(\frac{L}{Q_T}\right)\frac{\omega_0^3}{\Delta\omega^2}\left(1+\frac{2}{9}\frac{I_{DC}r_b}{kV_{TH}}\right) \tag{2.27}$$

From **Eq. 2.26** and **Eq. 2.27**, and more clearly by looking at values reported in **Table. 2.1**, an important characteristic in the resulting architecture is that the contribution of the core transistors to Phase-Noise is at least as low as in the standard **Class-B** oscillator contributing an effective noise proportional to that of the Tank resistance, independently of devices dimensions and mobility of the charge carriers [**51**].

The advantage of adopting a **Class-C** architecture over a **Class-B** one is found in something different from the Phase-Noise performance.
As a matter of fact, without the tail capacitance, the topology in **Figure. 2.15** turns back to the **Class-B** one where **X-Pair** transistors are in conduction for half of the oscillation period each, and the Tank current resembles a square

wave with **50%** duty cycle, yielding a **DC-to-RF** current conversion of $\mathbf{2}/\pi$ as discussed in **Section 2.1.1**.

With a large $\mathbf{C_2}$, however, the conduction angle is much lower than half a period, a condition that in fact defines **Class-C** operations. Current waveforms are made of tall and narrow pulses, typical of **Colpitts** oscillators, and the corresponding **RF** current component is, with very good approximation, $\mathbf{I_{\omega_0}=I_{DC}}$, which is **3.9 dB** larger then the previous case. Therefore the **Class-C** operation results in a much more efficient generation of the amplitude of the fundamental current harmonic, leading to higher oscillation amplitude for a given current consumption.

From the above discussion, assuming that:

$$A_{0-MAX} = I_{\omega_0} R_T = I_{DC} R_T \tag{2.28}$$

Substituting **Eq. 2.13** in **Eq. 2.28**, by using **Eq. 2.26** and **Eq. 2.27** the Phase-Noise expressions as function of the feedback factor **k** are:

$$\mathcal{L}(\Delta\omega)_{CMOS} = \frac{KT}{A_0^2}\left(\frac{L}{Q}\right)\left(\frac{\omega_0^3}{\Delta\omega^2}\right)\left[1+\frac{\gamma}{k}\right] \tag{2.29}$$

$$\mathcal{L}(\Delta\omega)_{BJT} = \frac{KT}{A_0^2}\left(\frac{L}{Q}\right)\left(\frac{\omega_0^3}{\Delta\omega^2}\right)\left[1+\frac{1}{2k}+\frac{(V_{DD}-V_B+V_{\gamma/th})r_b}{3kV_{TH}R_T(1+k)}\right] \tag{2.30}$$

For the same power consumption, the theoretical Phase-Noise improvement, compared to the standard differential-pair **LC**-Tank oscillator, is **3.9 dB** that is the same level of Phase-Noise can be achieved with almost **60%** less power-consumption compared to the conventional **Class-B** topology.

It must be noted, however, that the average base-emitter voltage of the **X-Pair** transistors is much smaller in **Class-C** as compared to **Class-B** operation. As a matter of fact, **DC** condition for **Class-C** operation is that active device are in the **OFF**-state for most of the oscillation period. This means that $\mathbf{V_B}$ can be set to a lower value in a **Class-C** oscillator as compared to a **Class-B** oscillator (i.e. $\mathbf{V_B = 0.7}$) still providing the current source a reliable

and safe working operation during the whole oscillation period, allowing to reach higher maximum oscillation amplitudes for the same **k** value then the **Class-B** (**Eq. 2.13**). Therefore, the minimum achievable Phase-Noise with the **Class-C** oscillator could be even lower than the one achievable with the **Class-B** oscillator because of larger oscillation amplitude.

2.2.3.1 AC-Coupled Class-C VCO: CMOS Vs. BJT

The base-resistance contribution to total **BJT**-implementation Phase-Noise is highlighted in **Figure. 2.16.b** outlining the trade-off between a small base-resistance noise contribution and the **TR** since larger device size, hence parasitic capacitors, are required to reduce the $\mathbf{r_b}$ term in **Eq. 2.30**.

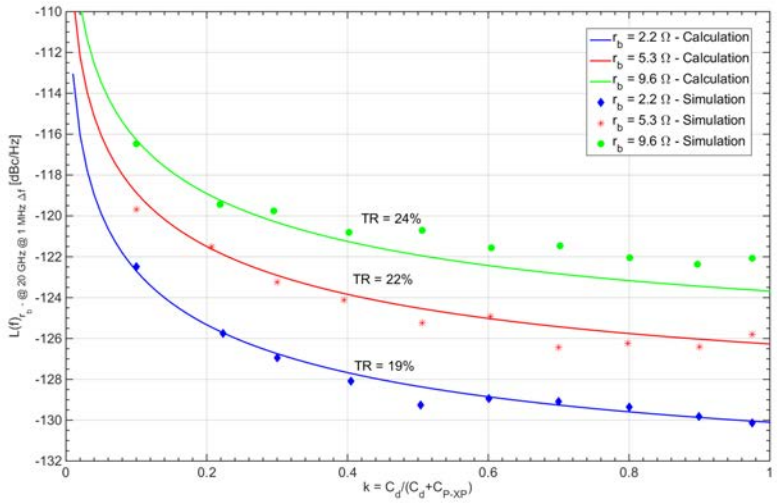
When it comes to the performance comparison between a **CMOS** and a **BJT** implementation, no great differences in **Figure. 2.17** are observed compared to **Figure. 2.9** since the equations describing the Phase-Noise and **TR** are the same (the only difference is in the absolute Phase-Noise levels since **Class-C** reaches higher oscillation amplitudes than **Class-B** as discussed above). Again an optimum is found for $\mathbf{k = 0.6}$.

The trade-off between Phase-Noise and Tuning-Range is addressed by looking at **Figure. 2.18** with practically no difference compared to **Class-B** architecture.

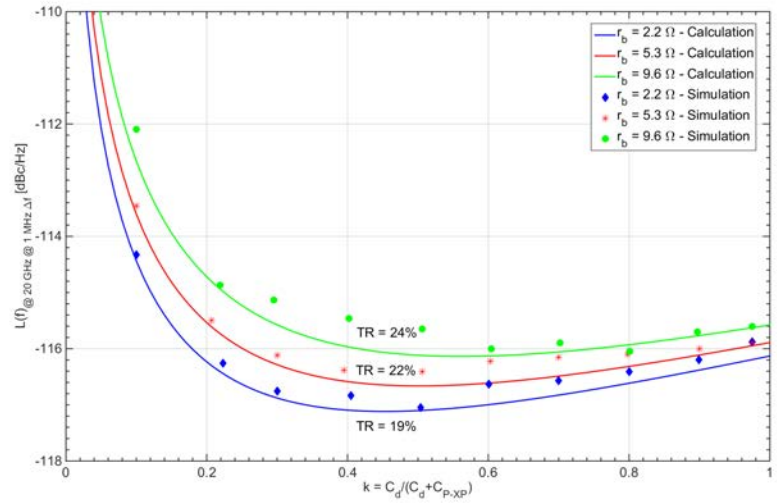
2.2.4 Comparison Conclusions

From the comparison made in previous **Sections** the main conclusions that can be drawn are:

i) The **Class-C** operation does not afford any advantage in terms of effective devices (or Tank) noise compared to **Class-B** (at same maximum oscillation amplitude $\mathbf{A_{o\text{-}MAX}}$). The topology does not change the *Folding-Factor* term of **X-Pair** devices in **Eq. 1.18** but operating the same transistors in **Class-C** maximizes the oscillation amplitude acting



(a)



(b)

Figure 2.16: Base-resistance impact on Phase-Noise performance in **AC**-biased **Class-C** oscillators at maximum oscillation amplitude: *(a)* $\mathcal{L}_{r_b-@20GHz@1MHz-\Delta f}$ Vs. **k** and *(b)* $\mathcal{L}_{TOT-@20GHz@1MHz-\Delta f}$ Vs. **k** at different **X-Pair** devices size (hence $\mathbf{r_b}$ and **TR**).

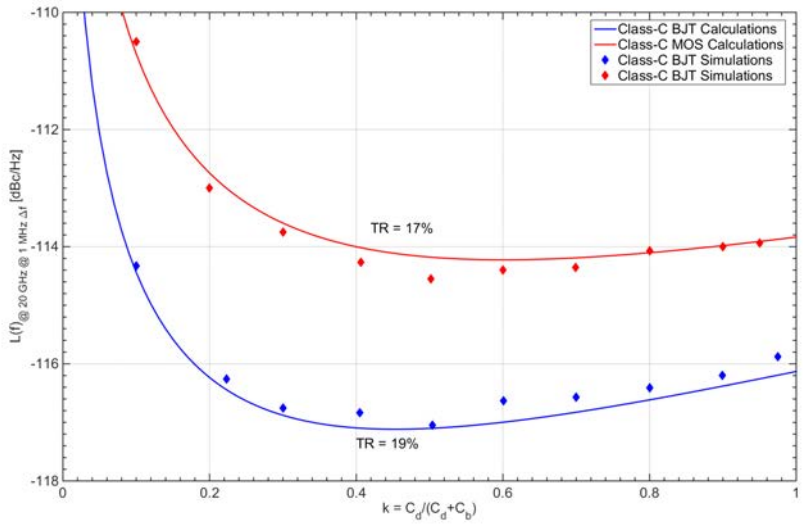


Figure 2.17: BJT Vs. CMOS $\mathcal{L}_{@20GHz@1MHz-\Delta f}$ at different **k** in **AC**-biased **Class-C** oscillators. The **BJT** dimensions are the maximum allowed by technological constraint and allows to reduce the base-resistance $\mathbf{r_b}$ to **2.2** Ω.

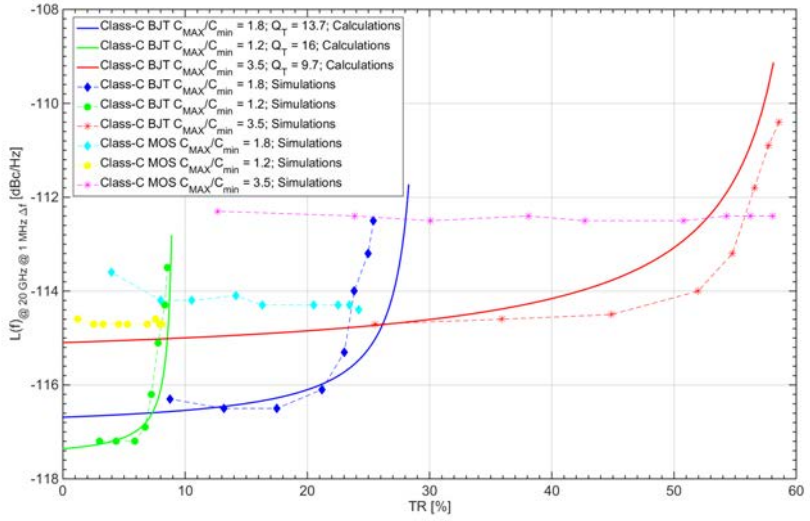


Figure 2.18: BJT Vs. CMOS $\mathcal{L}_{@20GHz@1MHz-\Delta f}$ at different **TR** in **AC**-biased **Class-C** oscillators for $\mathbf{k = 0.6}$.

on a superior **DC-to-RF** current conversion efficiency [**51**].

Furthermore by setting $\mathbf{V_B}$ at a lower value in **Class-C** operations, the maximum oscillation amplitude is increased and **Class-C** Phase-Noise improves with respect to **Class-B** by **1.5 dB** [**79**].

Actually, an even larger advantage is expected once other noise sources are considered, since the **Class-C** topology naturally filters out noise from the biasing current and current sources providing an easy implementation of a tail filter through capacitor $\mathbf{C_2}$ itself (**Figure. 2.15**), and does not introduce nodes sensitive to parasitic capacitances which may cause a large performance degradation.. On the other hand a resonant network at $\mathbf{2}\omega_0$ has to be implemented in **Class-B** topology, posing challenges in performing accurate **EM**-simulations, tuning the network together with the main Tank, finding optimal layout and in general slowing down the design.

In summary, in differential **LC**-oscillators, **Class-C** operation results in an improved performance as compared to **Class-B** biasing, both in terms of current efficiency and lower Phase-Noise, allowing to obtain larger amplitudes of oscillation for a given supply voltage;

ii) The **Colpitts** oscillator shows a comparable performance to the **Class-C** differential **LC**-oscillator in terms of Phase-Noise if the feedback factor is set for the optimal Phase-Noise versus current consumption trade-off. Even in this case, however, the current efficiency of the **Class-C** differential **LC**-oscillator is superior.

The maximum attainable value for the oscillation amplitude is the same as in the **Class-C** differential **LC**-oscillator. This is because of a non-negligible ripple on the source/emitter nodes of the switching devices in the **Colpitts** oscillator that does not allow $\mathbf{V_B}$ to be set as low as in the **Class-C** to preserve current source proper functionality. Increasing current, the **Colpitts** oscillator allows to further decrease the Phase-Noise

for a given supply voltage, but at the cost of a higher power consumption and lower efficiency. The **Class-C** differential **LC**-oscillator substantially achieves the same Phase-Noise performance of the **Colpitts** oscillator, but at a remarkably lower power consumption.

Moreover the **TR** performance of the **Colpitts** oscillator is impaired by the need for a capacitive divider ($\mathbf{C_1}$ and $\mathbf{C_2}$ in **Figure. 2.11**) which capacitively loads the Tank;

iii) As far as the **CMOS** Vs. **BJT** implementation is concerned, it is clear that, if the **BJT** devices size is large enough, Phase-Noise of **BJT**-based **VCO** outperforms **MOS**-based **VCO** due to the intrinsically lower shot noise in the **BJT** collector current versus the thermal noise in the **MOS** channel.

This important advantage is maintained also when power supply is increased to $\mathbf{V_{DD} = 2.5\ V}$ (see **Figure. 2.19**). In this case, thick-oxide **MOS** devices are required and, as an additional downside for the **MOS**-based **VCO**, it is difficult to achieve large **TR** due to the increased parasitics.

For $\mathbf{C_{MAX}/C_{min} = 1.8}$ as an example, the maximum **TR** of **CMOS** is limited to **17%** with a loop gain of **1.2** not enough for reliable operation, while the **TR** of the **BJT**-based one can go up to **25%** with a loop gain of **2.5**. At the targeted **TR** of **19%** Phase-Noise of the **BJT**-based **VCO** is already **2 dB** better than the **MOS** counterpart, which is not able to sustain the required **TR**.

Furthermore a **BJT** implementation has the advantage of a very low corner frequency ($\mathbf{f_{Corner}}$) therefore relaxing the design on the low-frequency Phase-Noise requirements presented in the **Introduction**.

The aforementioned considerations naturally lead to the choice of a **BJT** implementation of a **Class-C** oscillator. In the following it will be addressed as the chosen topology for the design of an ultra-low Phase-Noise **K-Band**

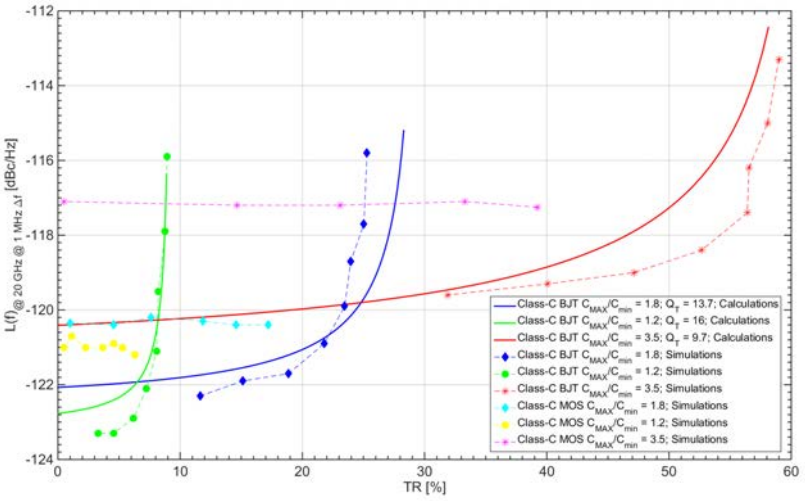


Figure 2.19: BJT Vs. CMOS $\mathcal{L}_{@20GHz@1MHz-\Delta f}$ at different **TR** in **AC**-biased **Class-C** oscillators for $\mathbf{k = 0.6}$ operated at **2.5 V** supply voltage.

VCO. The requirements could in principle be fulfilled by using a **CMOS** compatible supply voltage of **1.2 V** but in order to have some margin (since only basic **VCO** models have been considered so far neglecting noise sources here considered ideal), it has been risen to **2.5 V**.

Chapter 3

Tank Scaling

*In this **Chapter**, the minimization of the **L/Q** ratio in the **Leeson**'s formula (**Eq. 1.18**) is identified as the key factor in Phase-Noise reduction. Therefore the ultimate limits to the inductor shrinking process are discussed identifying an optimum value for the **L/Q** parameter around **L = 100 pH**. **EM** simulations have been performed over a set of progressively scaled inductors designed in the top ultra-thick metal layers of the adopted technology, including the connections to the Capacitor-Bank designed in lower metal layers. The final Tank presents a Capacitor-Bank divided in three sub-banks connected to a **M8+AP 100 pH** horseshoe-bent inductor.*

3.1 Techniques For Noise-Scaling

By looking at the *Leeson*'s formula, here reported for more clearness (**Eq. 3.1**), it is clear that as far as Phase-Noise minimization is concerned, maximizing $\mathbf{A_0}$ and minimizing $\mathbf{F}$, e.g. through topology selection and optimal biasing conditions, represents a well and broadly adopted design strategy.

$$\mathcal{L}(\Delta\omega) = 10\log_{10}\left[\frac{k_B T}{A_0^2}\left(\frac{L}{Q_T}\right)\left(\frac{\omega_0^3}{\Delta\omega^2}\right)(1+F)\right] \tag{3.1}$$

Noise scaling in oscillators can be better understood if **Eq. 3.1** is rewritten

by replacing $\mathbf{A_0 = R_T I_{\omega_0}}$, where $\mathbf{I_{\omega_0}}$ is the fundamental-harmonic component of the Tank current, and expressing $\mathbf{I_{\omega_0} = \eta_I I_{DC}}$, where $\mathbf{I_{DC}}$ is the **DC** current drawn by the oscillator and η_I is the **DC-to-RF** current-efficiency coefficient which depends on the oscillator topology [**52**]. This last relation holds as long as the transconductor works in highly non-linear regime which nevertheless is a quite common behavior in most electrical oscillators. Neglecting the flicker-noise contribution, Phase-Noise may be therefore expressed as:

$$\mathcal{L}(\Delta\omega) = 10Log_{10}\left[\frac{4K_BT}{R_T\eta_I^2 I_{DC}^2}\left(\frac{\omega_0}{2Q_T\Delta\omega}\right)^2\right](1+F) \tag{3.2}$$

Phase-Noise and power consumption do not efficiently scale straightforwardly. Aa a matter of fact, in **Eq. 3.2** Phase-Noise shows a square dependance on power consumption. Therefore a current increase by a factor **N** will lead to $\mathbf{N^2}$ better Phase-Noise. Therefore, if current consumption is doubled, the **FoM** is improved by **3 dB**.

Maximum **FoM** therefore is obtained by choosing $\mathbf{I_{DC}}$ to maximize the oscillation swing [**80**]. The maximum oscillation amplitude is related to the supply voltage $\mathbf{V_{DD}}$, and limited by the topology and reliability concerns. It can be written as $\mathbf{A_{0\text{-}MAX} = \eta_V V_{DD}}$, where η_V is a voltage-efficiency parameter that depends on topology and technology [**52**] [**80**] [**55**]. By choosing the aforementioned optimal operating conditions **Eq. 3.2** and **Eq. 1.25** can be rewritten as:

$$\mathcal{L}(\Delta\omega) = 10Log_{10}\left[\frac{4KT}{\eta_I\eta_V P_{DC}}\left(\frac{\omega_0}{2Q\Delta\omega}\right)\right](1+F) \tag{3.3}$$

$$FoM_{MAX} = 10Log_{10}\left[\frac{\eta_I\eta_V Q^2}{4KT}\right] \tag{3.4}$$

Changing the oscillator topology from **N**-only to complementary **PN** as proposed in [**81**] allows to scale noise and power by **6 dB** while preserving a constant **FoM**. Indeed, as discussed in [**49**], complementary **LC**-oscillators show different values of η_I and η_V (which are topology-dependent parameters)

and therefore achieve **6 dB** lower power and **6 dB** higher noise in optimal operating condition while maintaining the same $\mathbf{FoM_{MAX}}$ of an **N**-only **VCO**.

Another way to scale noise in **Eq. 3.1** is by reducing the Tank impedance $\mathbf{R_T}$, while keeping the oscillation swing $\mathbf{A_0}$ constant. Scaling down the inductance has always been one of the major adopted solutions to achieve low Phase-Noise levels. As a matter of fact the procedure of reducing the inductor size to lower the Phase-Noise is intuitive as it progressively reduces the noise contribution of the equivalent Tank parallel resistor ($\mathbf{R_T} = \omega_0\mathbf{LQ}$) which directly injects noise in the output nodes. $\mathcal{L}(\Delta\omega)$ is linearly proportional to $\mathbf{R_T}$, thus if the impedance is reduced by a factor of **N**, Phase-Noise is scaled down by **N**. Furthermore, all other noise sources (represented by **F** in **Eq. 3.1**) scale down as well by the same amount since their contributions to noise are referred to the one produced by the Tank.
At the same time, scaling down the equivalent Tank resistor reduces the oscillation amplitude which is proportional to $\mathbf{R_T}$. In order to restore the oscillation amplitude, current must be increased by the same shrinking factor, consuming more power. Phase-Noise minimization through inductance scaling (whatever the strategy adopted to scale it down) is achieved at the cost of larger power consumption but (and that is interesting), at constant **FoM**. As a result, Tank-impedance scaling allows to trade noise and power arbitrarily at constant **FoM** [**82**].

From literature two major methodologies have been widely implemented to perform the inductive scaling:

i) Reduce the inductance through the parallelization of multiple identical Tanks or oscillators;

ii) Physically reduce the inductance value by decreasing the physical diameter.

Each of the aforementioned techniques has pros and cons. The multi-core strategy trades noise with area occupation and Tuning-Range allowing to achieve

extremely low Phase-Noise levels without impairing Tank $\mathbf{Q_T}$. On the other hand, inductor shrinking methodology is valid until $\mathbf{Q_T}$ drops.
In the following they will be discussed to understand which are their limits and the applications in which the choice of one methodology outperforms the other one.

3.1.1 Multi-Core Oscillators

To lower $\mathbf{R_T}$ without compromising the quality factor, the whole Tank impedance, including reactive components, has to be scaled down. **Figure. 3.1** represents a simple way to implement it: the main tank is connected in parallel to an additional **LC**-Tank through switches. Provided that $\mathbf{I_{DC}}$ is doubled to keep $\mathbf{A_0}$ constant, the Tank impedance is halved by turning on the switches and therefore, according to *Leeson's Formula* in **Eq. 3.1** Phase-Noise is scaled down by **3 dB**. This solution however presents a drawback. As a matter of fact the reduction of the Tank impedance brings within the drop of the oscillators loop gain. Indeed, assuming square-law **MOS** transistors, as switching devices in the cross-coupled pair, the small-signal loop gain is given by:

$$G_{Loop} = g_m R_T = 2R_T\sqrt{k\frac{W}{L}\frac{I_{DC}}{2}} \tag{3.5}$$

where $\mathbf{g_m}$ is the cross-coupled pair devices' small-signal transconductance, $\mathbf{k_{MOS}}$ is their transconductance coefficient, and **W** and **L** are channel width and length respectively. Assuming that $\mathbf{R_T}$ is halved and conversely $\mathbf{I_{DC}}$ is doubled to keep the same oscillation amplitude, $\mathbf{G_{LOOP}}$ decreases by **3 dB**. This could lead to potential start-up issues unless the loop gain is widely oversized.

Figure. 3.2 shows a solution to the start-up issue coming from the $\mathbf{G_{LOOP}}$ reduction. The idea is to replicate the whole oscillator, including the cross-coupled pair and tail current source rather than the **LC**-Tank only. This principle can be extended to multiple oscillators. As a result, an in-phase-

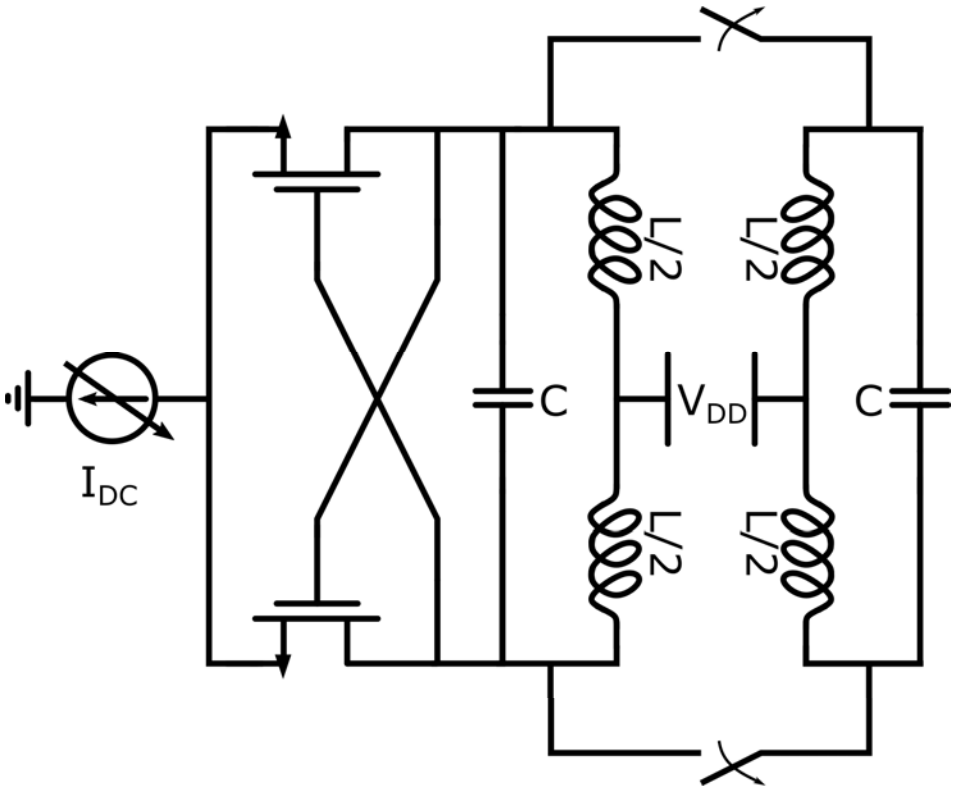


Figure 3.1: Multi-Tank Noise-scalable **VCO**.

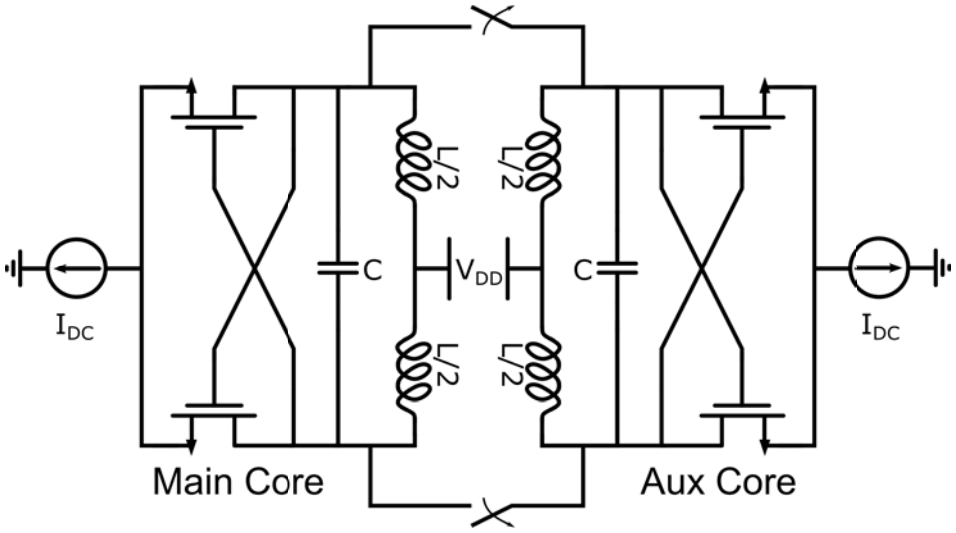


Figure 3.2: Multi-Core Noise-scalable **VCO**.

coupled multi-core oscillator is obtained. One **VCO** (namely the main core) is always switched on while the other cores (namely the auxiliary cores) can be selectively turned on and connected in parallel to the main one by mean of switches, resulting in an overall scaling of the Tank impedance and therefore Phase-Noise reduction according to **Eq. 3.1**.
This solution presents an $\mathbf{A_0}$ and $\mathbf{G_{LOOP}}$ independent by the cores number hence it does not suffers from start-up issues as previously seen for the Multi-Tank solution. As a matter of fact each core has auxiliary active devices that compensate the Tank resistance scaling.

The multi-core oscillator technique allows to overcome the limits of a single-core **VCO** reaching ultra-low Phase-Noise [**82**]. Indeed, in **Eq. 3.2** $\mathbf{Q_T}$ depends on technology parameters, $\mathbf{A_0}$ is limited to $\eta_V \mathbf{V_{DD}}$, and at given quality factor $\mathbf{R_T}$ can only be reduced by shrinking the Tank inductance **L**. However it has been observed that the inductive $\mathbf{Q_L}$ starts to drop if the Tank inductor size is shrunk below a certain size ((i.e. $\sim$**150 pH** at **20 GHz**)). This phenomena happens because of negative magnetic coupling between the two halves of the coil [**82**] as it will be further analyzed in detail in next section. Conversely, Tank impedance can be in principle arbitrarily scaled down

by leveraging the Multi-core oscillators principles of parallelizing more **VCOs** while keeping single-core Tanks optimized for maximum $\mathbf{Q_T}$.

Literature provides different works on **LC VCOs** leveraging an in-phase coupled Multi-Core architecture to target low Phase-Noise levels. Both dual- and quad-core configurations, employing resistive [**83**], capacitive [**84**], magnetic [**85**], and active [**86**] coupling, were demonstrated at **RF** frequencies. Few works demonstrated the adoption of this technique in the **mm-Wave** domain. First among them a magnetically-coupled **50 GHz** oscillator array was presented [**87**].

From theory the Phase-Noise reduction that this technique achieves is equal to $\mathbf{10Log_{10}\ N}$, where **N** is the number of cores, provided that the oscillators are coupled in phase. The theoretical Phase-Noise reduction is achieved regardless the coupling mechanism even though the type of coupling influences other factors such as stability of the in-phase mode, excess noise from the coupling devices and area. In example, area occupation could be saved by exploiting magnetic coupling since coupled Tank inductors can be overlapped. The drawback could be the low isolation achieved in a tunable **VCO** when auxiliary cores are turned off. Another technique to exploit noise scaling uses resistive switches (implemented by **MOS** devices) to establish an **VCOs** in-phase coupling. In this case a trade-off between the switches **ON**-resistance (responsible for excess noise if not carefully sized) and the Tuning-Range exists, especially at **mm-Waves**. Indeed, a low coupling resistance is beneficial to reduce the Phase-Noise penalty due to mismatches between the oscillator Tanks. However this requires large switches, resulting in capacitive parasitics and Tuning-Range reduction. Moreover, the central oscillation frequency shifts when switching from single-core to **N**-core configuration since switch capacitance changes between on and off states. As a result, the effective Tuning-Range where all the configurations overlap in frequency is further reduced.

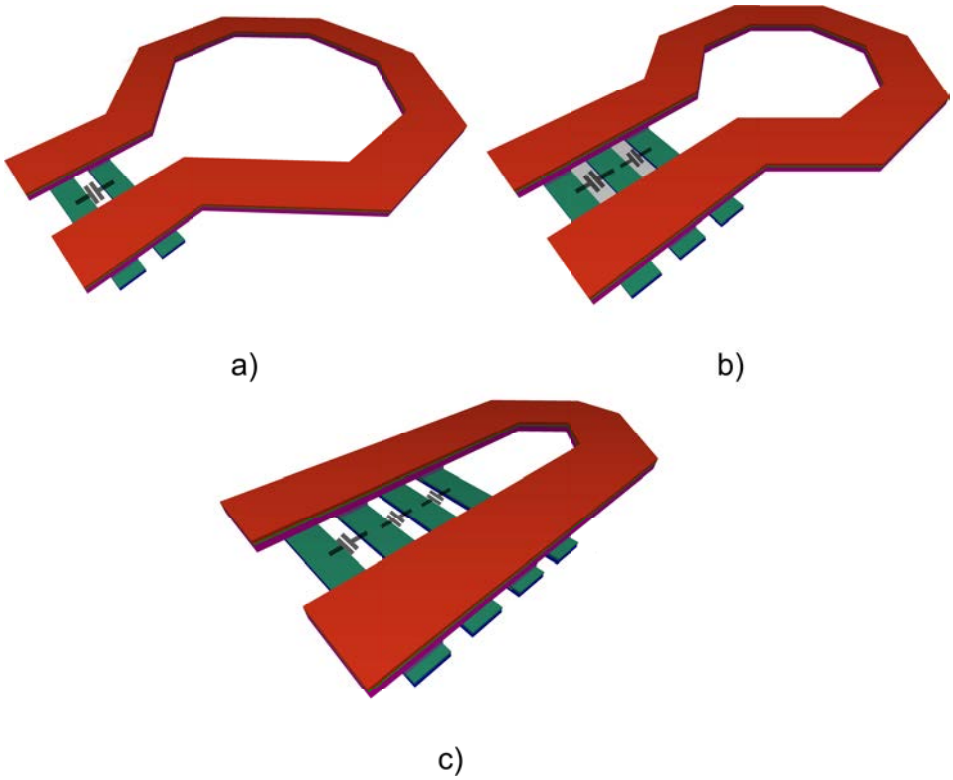


Figure 3.3: 3D view of the layout of an inductor for voltage-controlled oscillators as inductance decreases. In *a)* **L = 400 pH**, *b)* **L = 200 pH** and *c)* **L = 100 pH**.

3.1.2 Inductance Shrinking

A huge drawback when adopting Multi-Core oscillators topologies is, apart from the increased design complexity and layout, the huge area needed to accomodate **N** identical oscillators and in particular **N** high-**Q** inductors. Therefore that techniques should be employed only when the single-core oscillators limits are reached.

As highlighted before, the main limit in a single-core oscillator is scaling down the inductor while keeping constant the quality factor. By looking at **Eq. 3.1** it seems that the **L/Q** ratio parameter has to be minimized. As an example, if inductance can be halved at constant **Q** (i.e. by halving the inductor resistance as well), Phase-Noise can be improved by **3 dB** with twice the power consumption and constant **FoM**.

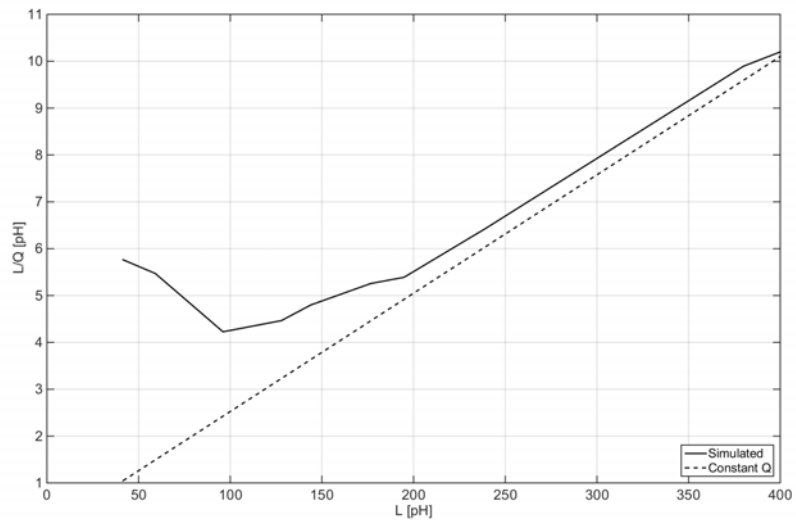


Figure 3.4: Simulation of **L/Q** as a function of **L** using **EM** simulator (solid) and assuming constant **Q** (dashed).

To gain insight, **Figure. 3.3.a** shows the **3D** view of a **400 pH** circular-shape inductor typically employed in high-**Q** integrated **VCO** designs. It is made of a sandwich of the two topmost thickest metal layers (red) to reduce the trace resistivity, while the width is $\mathbf{W = 30\ \mu m}$, the largest allowed by design rules. The transversal lines connect the inductor to the Capacitor-Bank. A **2X** down-scaling of **L**, for example, halves the inner diameter, as depicted in **Figure. 3.3.b**, where resulting inductance is **200 pH**. On the other hand, the Capacitor-Bank must double in size to keep constant frequency, thus doubling connection length. If the inner inductor diameter is still large enough so that magnetic flux around the circular shape does not cancel destructively, and the length of the connection to the Capacitor-Bank is not dominant versus the circular-shape portion, **Q** can be preserved, which is the case in our example.

Further iteration of this procedure yields the **100 pH** horseshoe-shape inductor in **Figure. 3.3.c**. Inductor traces are very close to each other, and quality factor is impaired by the negatively-coupled magnetic flux, producing an **L** reduction faster than the reduction of the corresponding $\mathbf{R_T}$. The inductor design has been optimized, through **EM** simulations, assuming as a

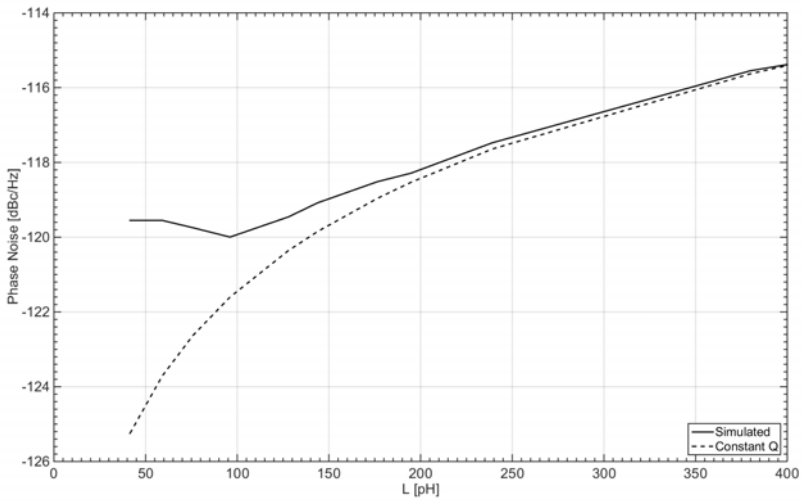


Figure 3.5: Simulation of Phase-Noise at **1 MHz** offset at **20 GHz** as a function of **L** using **EM** simulator to evaluate **L/Q** (solid) or assuming constant **Q** (dashed).

starting point a **400 pH** inductor with inner diameter of **180** μ**m** and trace width of **30** μ**m**. Results are reported in **Figure. 3.4** with inductances ranging from **400 pH** down to **30 pH**. The solid line represents the results of the **EM** simulations, while the dashed lines the expected **L/Q** ratio assuming constant **Q**. Minimum is found for a **100 pH** inductor, and **L/Q** is $\sim$**4** ($\mathbf{Q_L} \sim$ **20**). Lower inductances result in higher **L/Q** and from **Eq. 3.1** higher Phase-Noise is expected.

Based on the observations reported in **Chapter 2**, a **Class-C** topology based on bipolar devices is selected due to superior **FoM** while showing almost the same Phase-Noise performance with respect to other alternatives. The circuit is supplied at $\mathbf{V_{DD} = 2.5\ V}$. A set of simulations has been performed scaling **L** and Tank capacitor **C** ($\mathbf{Q_C = 50}$ at **20 GHz**), for constant **20 GHz** oscillation frequency. The **EM** model of **L** used in **Figure. 3.4** has been adopted. **Figure. 3.5** shows Phase-Noise results. The minimum Phase-Noise is **-120 dBc/Hz**, achieved for $\mathbf{L = 100\ pH}$. It corresponds to the minimum **L/Q**, as predicted by **Eq. 3.1**. Further **L** reduction does not lead

to any Phase-Noise improvement.

3.2 Conclusions

Noise scaling through inductance reduction is a powerful technique allowing to trade Phase-Noise with power consumption at constant **FoM**. Physically reducing the inductor allows to reduce the equivalent Tank parallel resistor and consequently scale down noise provided that more current is increased restoring the maximum oscillation amplitude allowed by the oscillator topology adopted. However as inductor shrinking procedure goes further, negative magnetic coupling and parasitic resistors in the connections to the Capacitor-Bank (becoming larger and larger as inductor scales down to allow oscillation at the same center frequency) reduce the overall quality factor.
When the **L/Q** minimum for a given technology is reached than passing from a single-core architecture to a Multi-Core solution allows to further get benefits from inductor reduction through Tank parallelization.

Adopting a Multi-Core solution using a non-minimal **L/Q** inductor would lead to a significant waste of area in a transceiver. In example instead of a **100 pH** inductor, a larger inductor, say **L = 200 pH** could be used to reach (with some margin) the Phase-Noise requirements discussed in the **Introduction**, adopting a dual-core configuration. Since the inductor diameter is proportional to the inductance value, the dual-core solution would have required at least an **8X** total occupied area with respect to the single-core one. At a first order approximation power consumption of the two solutions would be the same if the tank quality factor didn't change. Since the quality factor of the reactive components decreases indeed with at low inductance values, the power consumption of the Multi-Core solution is slightly lower than the Single-Core solution one resulting in slightly better power efficiency and **FoM**.

Chapter 4

Circuit Design

*In this chapter the design of the building blocks for frequency-synthesis is addressed. The **55nm BiCMOS** technology provided by **STMicroelectronics** has been adopted.*

*First a brief overview of the technology features is provided. Then the discussion turns on the design choices for the realization of the **VCO** and the output buffer chain. Finally, an overview of the taped out test chip is provided.*

4.1 55nm BiCMOS Technology Overview

The test chip was designed and fabricated in a **55nm BiCMOS** technology provided by **STMicroelectronics** [**88**]. The technology cross section is shown in **Figure. 4.1** highlighting the metal-stack.

The *Front-End Of The Line* (**FEOL**) features both carrier-class **55nm CMOS FET** and epitaxially-grown high-speed $\mathbf{S_iG_e}$**-npn** heterojunction bipolar transistors (**HBT**). Technology presents three type of **CMOS** transistors: *general purpose* (**GP**), operated at **1 V** supply, low power (**LP**), with **1.2 V** $\mathbf{V_{DD}}$, and thick-oxide (**GO2**), adopting **280nm** minimum channel length, as opposed to **55 nm** in the other types, pushing the operating supply voltage up to **2.5 V**. Bipolar transistors as well come in three flavors. High-speed $\mathbf{S_iG_e}$

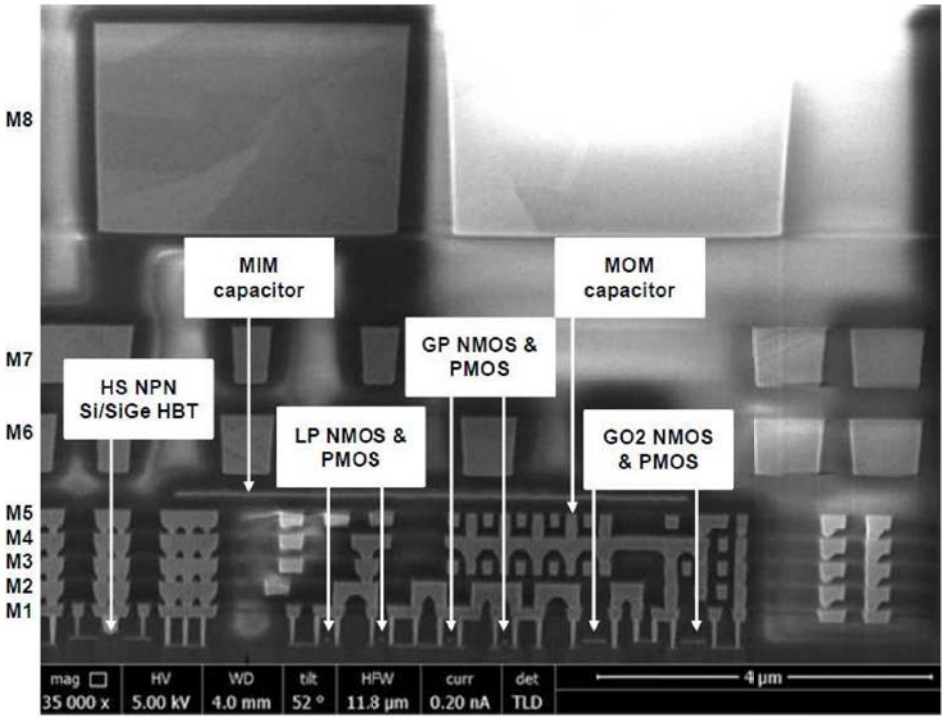


Figure 4.1: 55nm BiCMOS technology cross-section [**88**].

bipolars feature **320 GHz GBW**, with **1.5 V** *collector-emitter breakdown voltage* (**BVCEO**). The other two types (medium-voltage and high-voltage **HBTs**) achieve higher **BVCEO** with the drawback of larger parasitics and lower-speed operation.

The *Back-End Of The Line* (**BEOL**) features a stack-up made up by **8** copper metal layers. Starting from the bottom, there are: **5** thin layers **M1-M5**, **2** thick layers **M6** and **M7**, and an ultra-thick metal (**UTM**) layer **M8**, providing a very small per-square resistance therefore being suitable for the design of high quality factor reactive elements. The **3μm** thick **UTM** represents the main difference with respect to the **65nm CMOS BEOL** metal-stack. To complete, last layer in the **BEOL** is represented by a **1μm** aluminum capping layer (**AP**) covering the top.

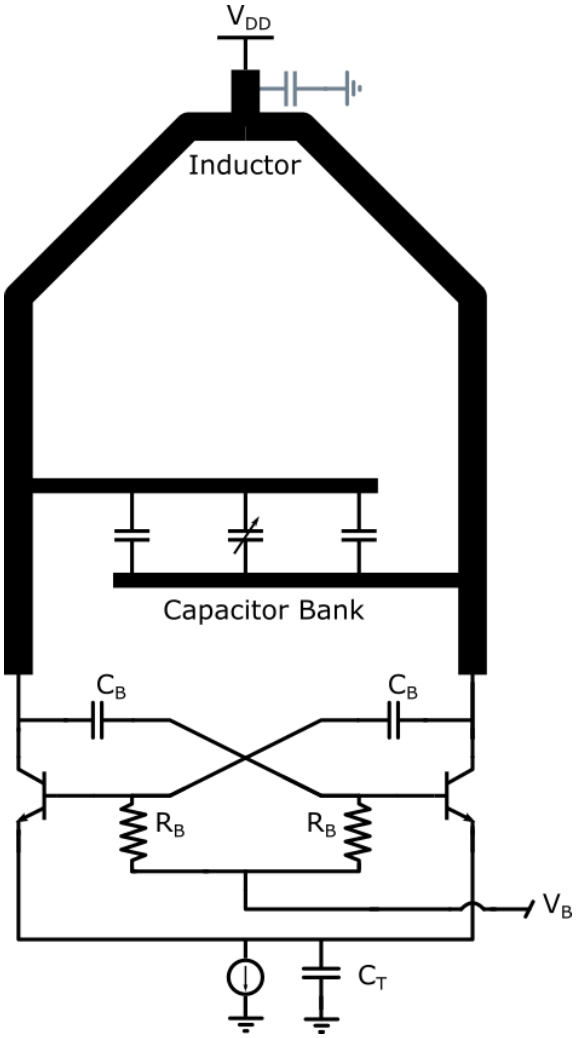


Figure 4.2: Class-C VCO sketch layout. The horseshoe-bent shape of the inductor is outlined together with the connections to the Capacitor-Bank.

4.2 VCO Design

Minimization of Phase-Noise has been the main driver of the oscillator core design. Considerations provided over the many topologies presented in **Chapter 2** pointed out that **Class-C** oscillators [**51**] and **Class-B** oscillators with tail filter [**78**] are the most performing in terms of Phase-Noise, Tuning-Range and power efficiency [**70**].

Colpitts oscillators are too much power-hungry, even if they could in principle achieve lower levels of Phase-Noise compared to **Class-B** and **Class-C** ar-

chitectures. **Class-F** oscillators [**54**] are attractive as well, but a transformer-based Tank is required, introducing unwanted capacitive parasitics at **20 GHz** impairing the Tuning-Range.

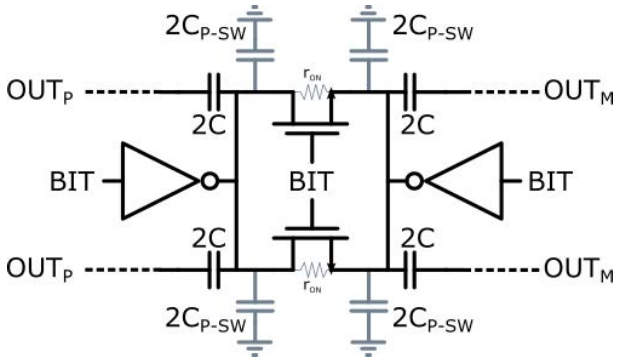
Class-B VCO with tail filter allows maximum oscillation amplitude swing (since transistors can be pushed in deep ohmic region) and Phase-Noise levels close to the theoretical limit [**89**]. On the other hand **Class-C VCOs** provide very good **FoM** and even if their oscillation swing has to be slightly limited with respect to **Class-B** operations (since topology suffers when core devices enter deep ohmic region) [**51**], core transistors bias voltage can be set to a lower level. Therefore the **Class-B** and **Class-C VCO** maximum oscillation amplitude is almost the same.
From the discussion in **Chapter 2**, since the two topologies exhibit the same absolute noise performance, **Class-C** topology has been preferred due to its superior **FoM** performance. A sketch of the **Class-C VCO** design is shown in **Figure. 4.2**.

The design and optimization of either **VCO** Tank and core will be discussed in the following.

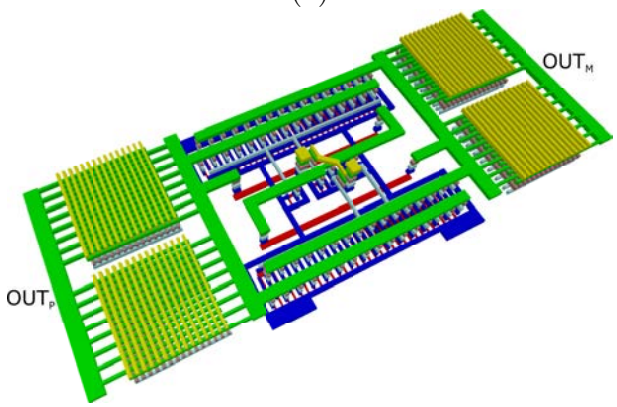
4.2.1 VCO Tank Design

Tank optimization through careful layout and accurate **EM** simulations is mandatory. While the inductor optimization and layout has been discussed in details in **Chapter 3**, identifying an optimal inductance value of **100 pH** minimizing the **L/Q** ratio and Phase-Noise, the capacitor-bank design is important too since the overall Tank quality factor is the parallel combination of both the reactive components and, as outlined in **Chapter 2**, it trades with the Tuning-Range.

The $\mathbf{C_{MAX}/C_{min}}$ needed to target the required Tuning-Range is **1.8** resulting in a total capacitance switching from **400 fF** (when only parasitic capacitors count and **VCO** oscillates at $\mathbf{f_{MAX}}$) to **720 fF** (when the whole



(a)



(b)

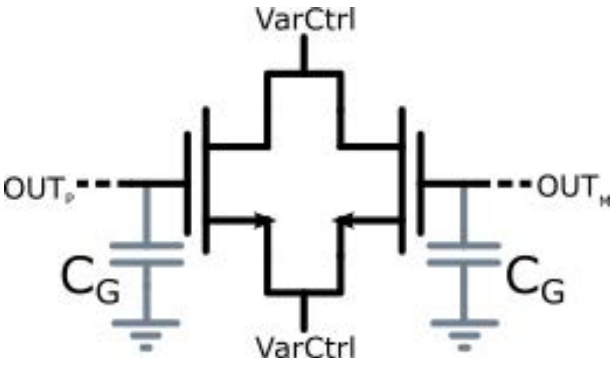
Figure 4.3: Capacitor-Bank elements: *(a)* - Capacitor unit element; *(b)* - Layout.

Capacitor-Bank is connected and **VCO** oscillates at $\mathbf{f_{min}}$).

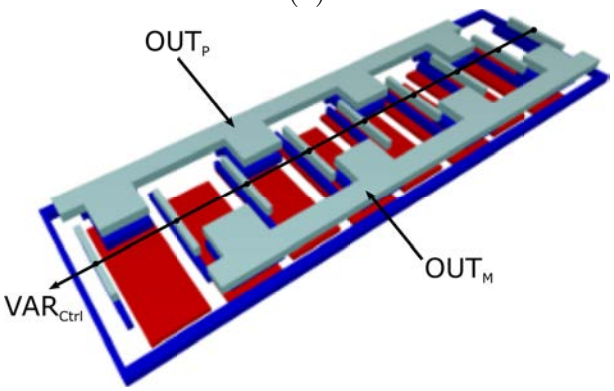
Frequency control is performed by dividing the bank in **31** equal unit capacitor element (shown in **Figure. 4.3.a**) and grouping them in binary-weighted sub-banks controlled by a **5-Bit** control word plus a small varactor for fine tuning, analogically controlled.

This solution reduces the amount of nonlinear capacity in the Tank, which would result in Phase-Noise penalties and flicker-noise up-conversion due to **AM-PM** conversion [**90**].

The **MOS**-based Varactor is made up by **8** μ**m**-width thick-oxide High-Voltage **MOS** transistors to sustain the large oscillation amplitude superimposed to the high supply-voltage. The gates are connected to the **VCO** differential outputs while drain and source are shorted and externally controlled as shown



(a)



(b)

Figure 4.4: Varactor design: *(a)* - **MOS** Varactor; *(b)* - Layout.

in **Figure. 4.4.a**. The varactor has to be properly sized so that the overall capacitance variation (by changing the analog tuning voltage **VarCtrl** from **0** to **2.5 V**) allows a frequency change large enough to cover an **LSB** variation in the digital control word in order to ensure band overlapping between two subsequent codes.

The Capacitor-Bank Element in **Figure. 4.3.a** has been designed in order to reach the required value for $\mathbf{C_{MAX}/C_{min}}$ while still preserving a reasonable quality factor not degrading the Phase-Noise performances. For this reason the smallest and more compact layout form factor for the **MOM**-capacitor has been adopted yielding a single **MOM** capacitance of **40 fF**. The layout of the single cell is center symmetric to reduce process parameter spread.
NMOS switch transistor ia a **LP** transistor which has slightly higher $\mathbf{r_{ON}}$ with respect to the **GP** transistor but can sustain larger $\mathbf{V_{GS}}$ hence being reliable

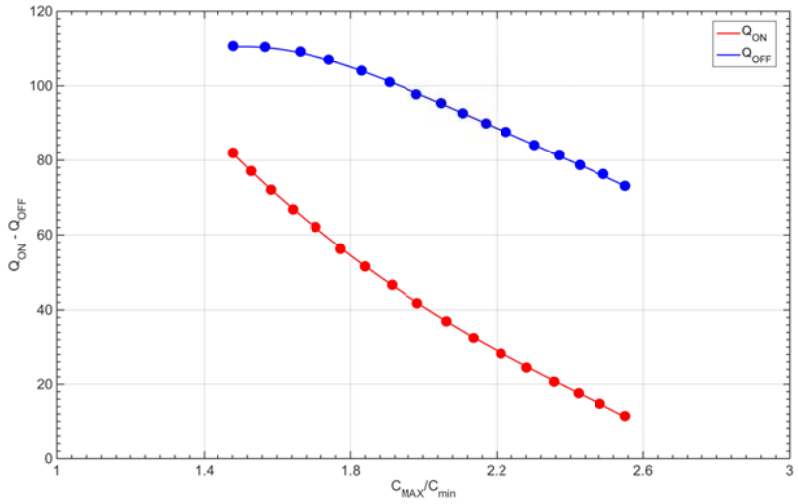


Figure 4.5: Capacitor-Bank $\mathbf{Q_{ON}}$ and $\mathbf{Q_{OFF}}$ Vs. $\mathbf{C_{MAX}/C_{min}}$.

even when large oscillation amplitudes occurs.

The trade-off between $\mathbf{C_{MAX}/C_{min}}$ and $\mathbf{Q_{ON}}$-$\mathbf{Q_{OFF}}$ is shown in **Figure. 4.5**. It can be seen that for a $\mathbf{C_{MAX}/C_{min} = 1.8}$, corresponding to $\mathbf{W = 31\ \mu m}$, the Capacitor-Bank quality factor is **100** (when the Capacitor-Bank is disconnected) and it is **50** (when the Capacitor-Bank is disconnected). $\mathbf{Q_{OFF}}$ is larger than $\mathbf{Q_{ON}}$ since when the switch is turned off it exhibits a larger resistance than $\mathbf{r_{ON}}$. The Tank quality factor however is still dominated by the inductor ($\mathbf{Q_L = 19}$) and it is only mildly influenced by the capacitor bank losses. The overall Tank quality factor is $\mathbf{Q_T \sim 14}$

4.2.2 VCO Core Design

The discussion outlined in **Chapter 2** pointed out that a supply voltage of **2.5 V** is adequate to target the specs with sufficient margin in order to take account of process variation and simulation differences with respect to silicon implementation. Referring to **Figure. 4.6**, supply voltage is connected to inductor's center tap. **Class-C** operation is guaranteed by proper biasing of the base of active devices which is set to $\mathbf{V_B = 1\ V}$ to ensure enough voltage

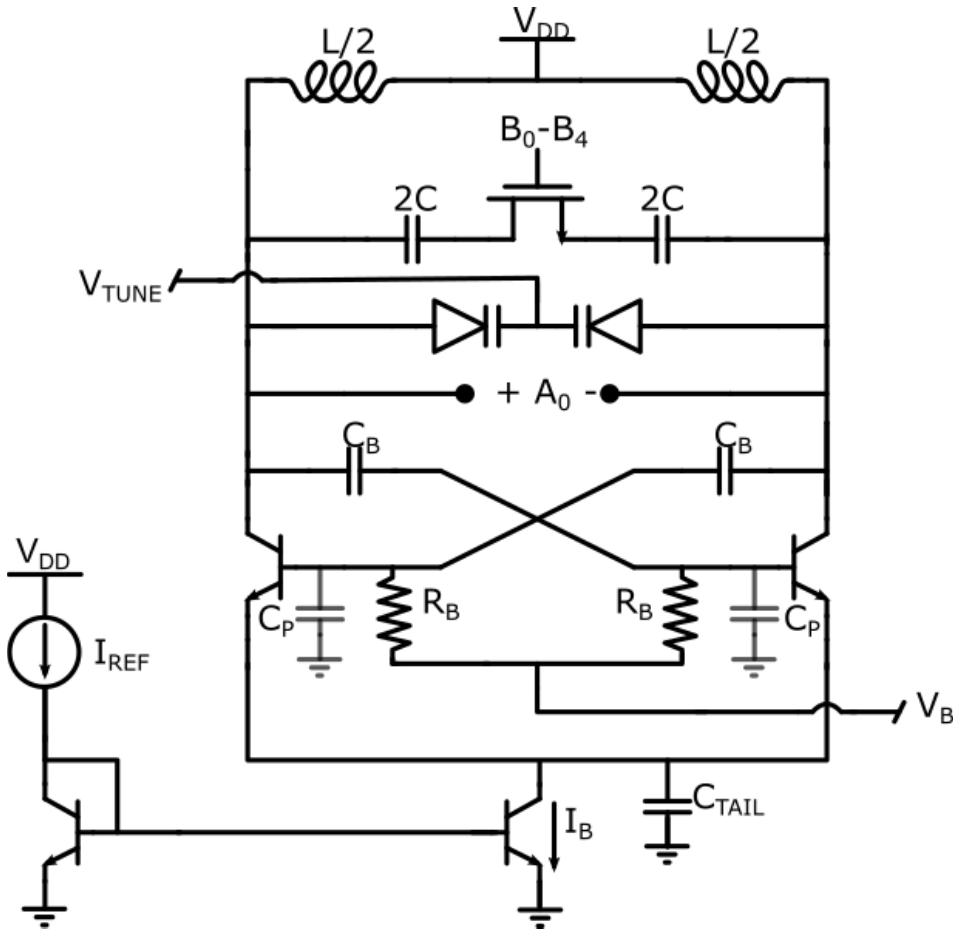


Figure 4.6: **VCO** core based on a **Class-C** topology with capacitive tail filter.

headroom to the current source. Base resistance contribution to Phase-Noise is minimized by adopting large core transistors size (**5 Emitters X 10 X 0.42** $\mu\mathbf{m^2}$). **npn-HBT** transistors were used for both cross-coupled pairs and tail current sources. The total emitter capacitance for **Class-C** operation is **2 pF**, **1.5 pF** of which is realized with an explicit **MOM** capacitor $\mathbf{C_T}$.

Since the **VCO** operates in **Class-C**, the capacitive divider realized by $\mathbf{C_P}$ and $\mathbf{C_B}$ plays a very important role as outlined in **Chapter 2**. The best Phase-Noise is found for $\mathbf{k = 0.6}$ and it is mildly dependent on the value of **k**. In this design, since $\mathbf{C_P = 200\ fF}$, $\mathbf{C_D}$ is sized to **300 fF**.

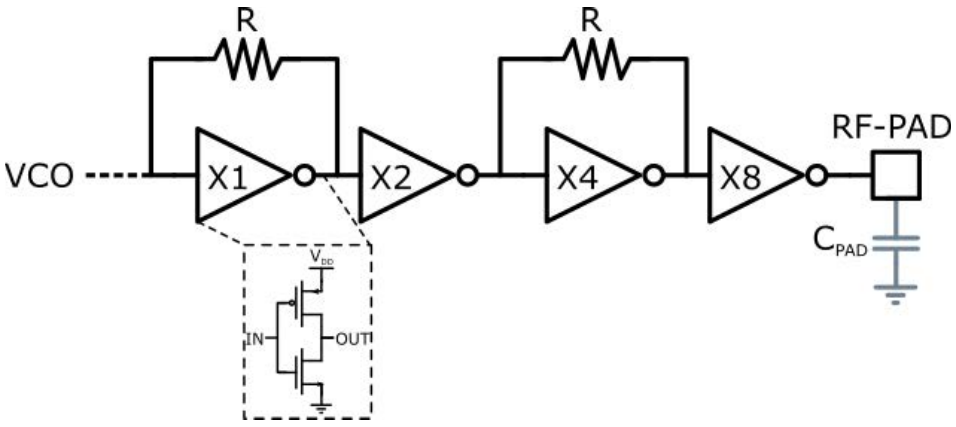


Figure 4.7: Self-biased tapered inverter output chain: The **VCO** is loaded by a small inverter in order not to degrade Tuning-Range performances by adding parasitic capacitors on sensible nodes.

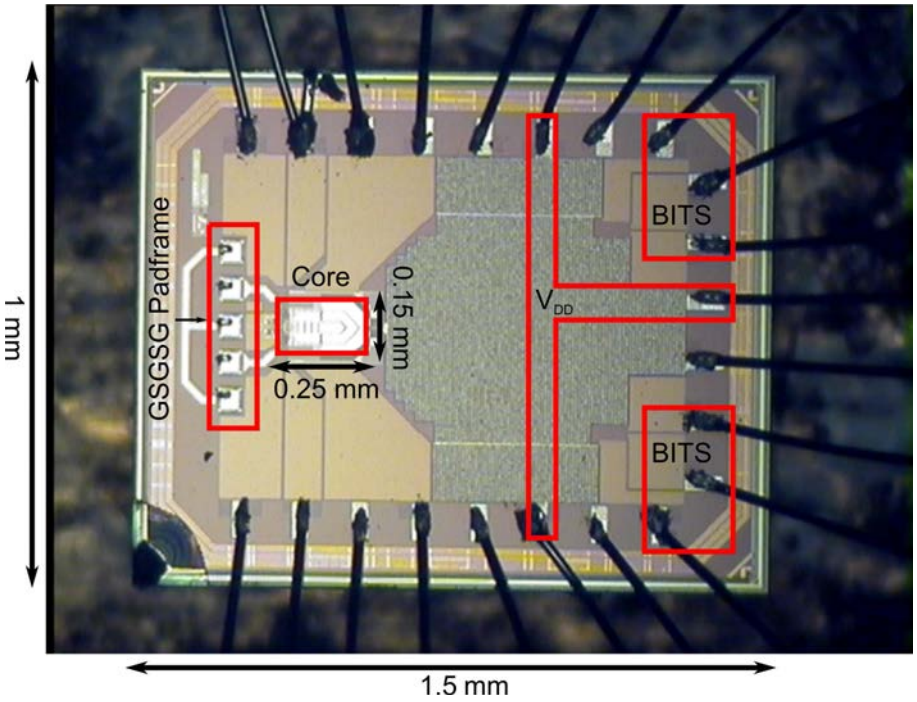
4.3 Output-Chain Design

The **VCO** is loaded by a buffer realized with the cascade of self-biased tapered inverter chain **Figure. 4.7** to drive the output Pads capacitive load and the instrumentation. The output-chain is powered with a **1.2 V** supply. **MOS** transistors have been adopted to implement the inverters building up the buffer. The first inverter is small in order not to degrade Tuning-Range performances by adding parasitic capacitors on sensible nodes. Buffer design is trivial and will not be discussed.

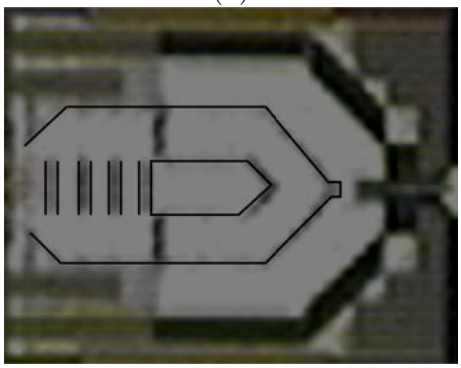
4.4 Test-Chip Overview

A test chip, named **FALCON**, has been taped out and measured. The supply voltage is **2.5 V**. The biasing current is **22 mA**. The **VCO** outputs are buffered through the output-chain to a differential **GSGSG** pad-frame for differential probing. Power-Supply, Bias currents, Bias voltages and digital and analog frequency control are provided through bonding wires. The chip micrograph is shown in **Figure. 4.8.a**.

Chip size is **1.5 X 1 mm^2** while the core area is approximately **0.25 x 0.15**



(a)



(b)

Figure 4.8: FALCON test-chip: *(a)* - **FALCON** Chip-Micrograph; *(b)* - **FALCON VCO**-core particular.

mm². in **Figure. 4.8.b** a zoom on the core area allows to clearly identify the **100 pH** horseshoe-bent shaped inductor realized through a **M8-AP** metal stack and the connection of the inductor to the underlying Capacitor-Bank realized through a stack of **M6-M7** layers.

4.5 Conclusions

In this chapter, design strategies and implementation details for the realized **20 GHz VCO** has been presented. Considerations on the optimization of the tank quality factor through careful Capacitor-Bank design are discussed in details pointing out the trade-off between quality factor and Tuning-Range. A chip has been realized in **55nm BiCMOS** technology. Measurements results are shown in the next chapter.

Chapter 5

Measurements Results

*In this chapter, measurements on the test chip described in **Chapter 4** are presented. A complete characterization and overview of the performance of the implemented oscillator is presented, and its performance is compared with other **State-Of-The-Art** works and with **E-Band** backhaul synthesizer requirements already introduced and discussed in the **Introduction** and **Chapter 2**.*

5.1 Probed VCO Measurements

The **20 GHz VCO** output signal is measured through a **GSGSG** probe, connected to a spectrum analyzer. Power supply, analog bias signals and digital controls are provided through bonding wires via an analog **DC**-Board and a digital interface programmed via **PC**. The measurement setup is shown in **Figure. 5.1**. Several On-Board capacitors ,ranging from **1** μ**F** to **1 pF**, have been placed near the chip to properly filter out noise from the bias circuitry and instrumentations.

The oscillator consumes approximately **55 mW** power from a **2.5 V** supply. Phase-Noise spectrum at **20 GHz** oscillation frequency is shown in **Figure. 5.2**.

The **VCO** suffers from drifting of the free-running center frequency. This

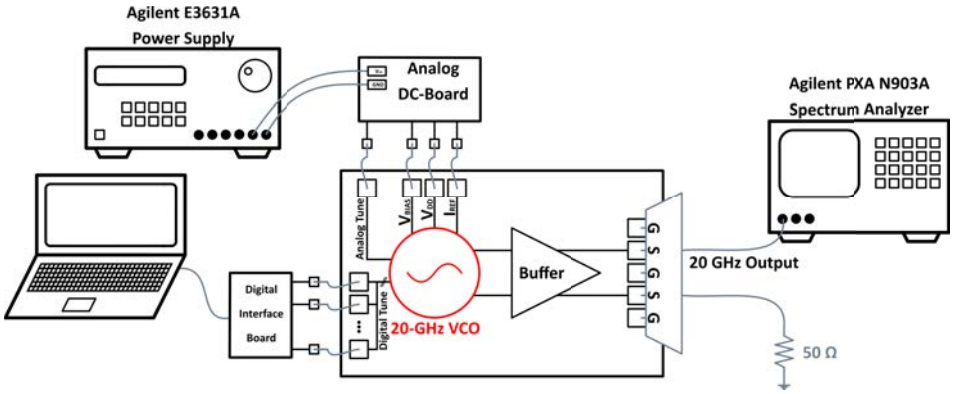


Figure 5.1: Measurement setup to characterize the **VCO** by probing it through a **GSGSG** differential high-frequencies probes.

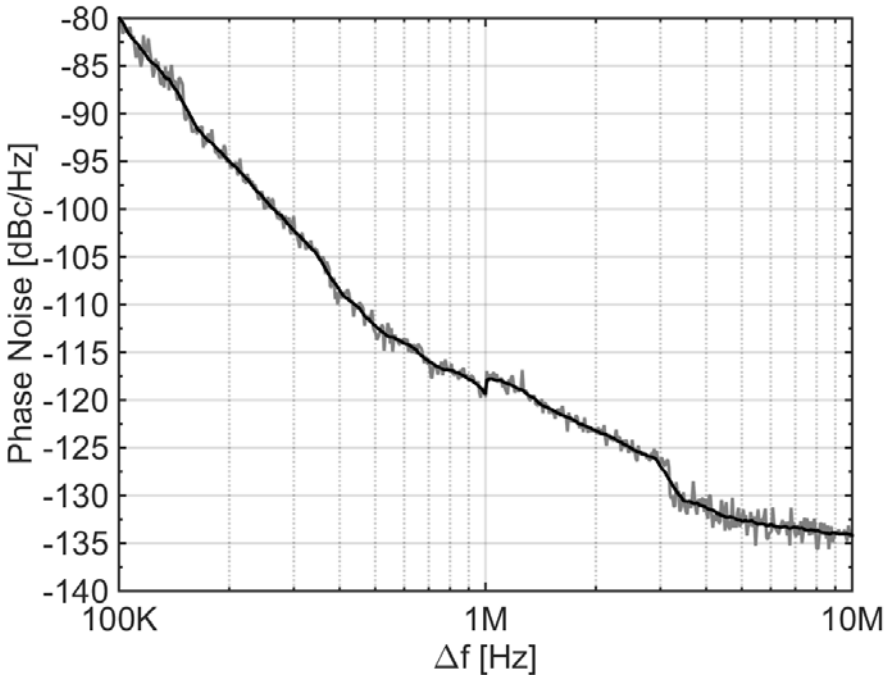


Figure 5.2: Probed **VCO** Phase-Noise measurement. The oscillator center frequency is affected by drifting impairing the Phase-Noise measurement at low frequency offset from the carrier.

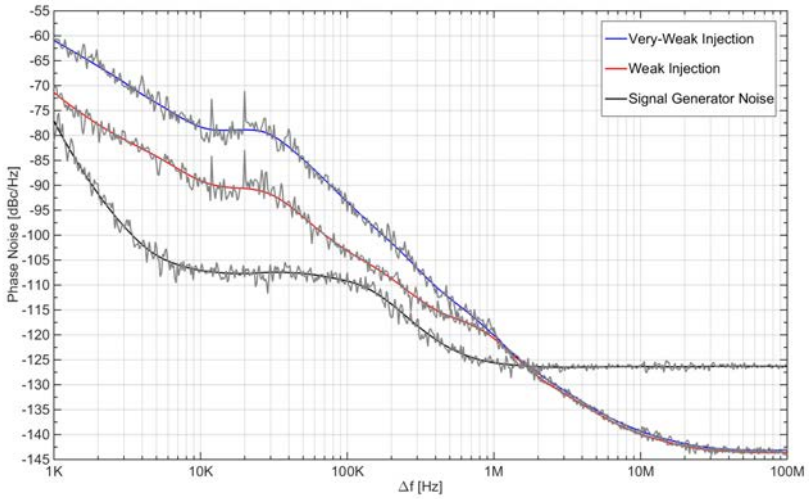


Figure 5.3: Injection-Locked oscillator spectrum. Note that under the weak-injection condition the oscillator is almost free-running and the phase noise shape starts to rise again and a $\mathbf{1/f^3}$ appears.

drift doesn't allow the spectrum analyzer to properly lock the **VCO** fundamental and correctly measure the Phase-Noise. The phenomena results into an unusual Phase-Noise behaviour between **100 KHz - 1 MHz** displacement from the carrier where a slope of **-40 dB/decade** is observed. Moreover some discontinuities appear around **1 MHz** and **3 MHz** and in general the shape of the Phase-Noise spectrum is not clean.
In order to reduce drifting, a solution would have been the adoption of a frequency divider (i.e. by **4**) through external components. It would have resulted in a reduction of the drifting phenomena by the division factor. Another widespread adopted solution consists in inserting the **VCO** in an external **PLL** in order to lock the oscillator center frequency in a stable way, provided that the locking-range of the **PLL** is smaller than the frequency displacement where Phase-Noise measurement is of interest (lower than **100 KHz** in this case).

If that is the situation than Phase-Noise measured inside the locking-range is the one provided by the external reference of the **PLL** while outside of it only the **VCO** noise counts as it can be seen in **Figure. 5.3**. The solution

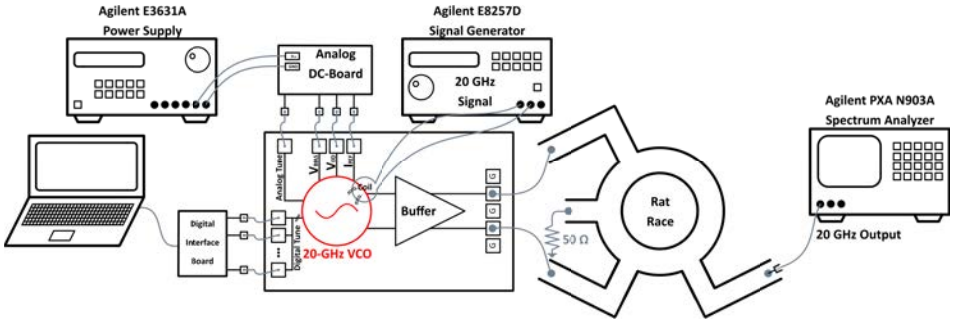


Figure 5.4: Injection-Locked **VCO** measurement setup. The **GSGSG** pads are bonded to the inputs of a **20 GHz Rat-Race** power-combiner .

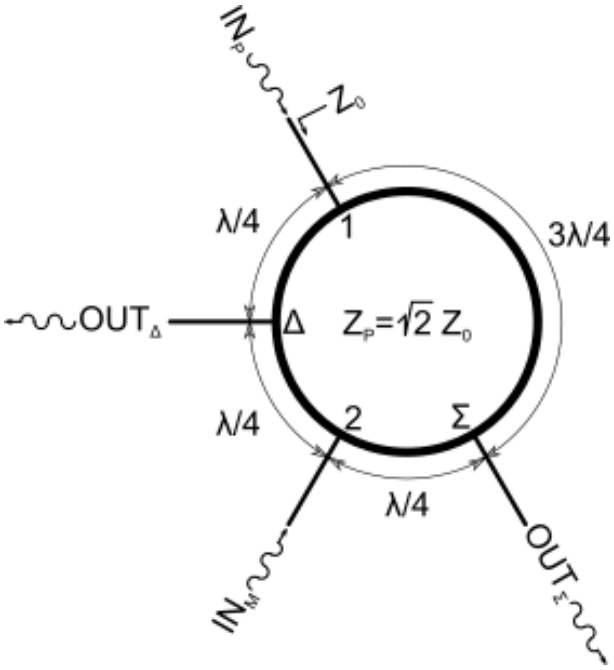
adopted to measure in a stable way the oscillator belongs to this last category as it will be discussed in next **Section**.

5.2 Injection-Locked VCO Measurements

The measurement setup shown in **Figure. 5.4** makes use of an **RF** board in **Roger**© **3003** ($\epsilon_r = 3$, $\tan(\delta) = 0.001$), able to drive high frequency signal with small losses compared to standard **FR4 PCB** layers.

A **20 GHz Rat-Race** power-combiner is designed on top of the **RF** board **Figure. 5.5**. The **Rat-Race** has been designed with the **ADS** electromagnetic tool. This solution allows to convert the differential outputs of the **VCO** in a single-ended one, easily connected to the instrumentation through a **26 GHz SMA** connector avoiding the need for a bulky probe station. Moreover, the differential to single-ended conversion allows to get rid of the common-mode components improving common-mode noise rejection and the overall measurement quality.

Differential signals coming from the chip **GSGSG** pads are fed to **Port 1** and **2** respectively through equally long path. Travelling waves in the **Rat-Race** cancel each other at **Port** Δ while add in phase at **Port** Σ provided that the ports are suitably matched to the characteristic impedance of the **Rat-Race**. The structure has been electromagnetically simulated and has a



(a)

(b)

Figure 5.5: Rat-Race power-combiner: *(a)* - Schematic; *(b)* - Layout.

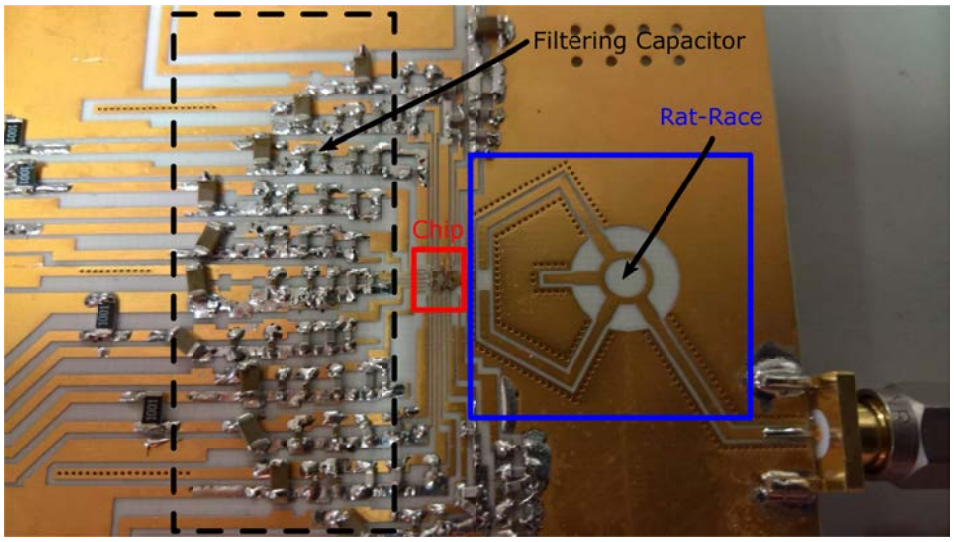


Figure 5.6: RF-board **20 GHz Rat-Race** power combiner.

bandwidth large enough to cover the **VCO** Tuning-Range.
The situation described above does not exactly happen though, since **Port 1** and **2** are not well matched to the impedance provided by the chip pads and bonding wires since they were meant for probing, not bonding. However even if some power is reflected back, the output wave feeding the spectrum analyzer has enough energy ($\mathbf{P_{Carrier}}$ **= -7 dBm**) to produce a reliable measurement of the Phase-Noise.

The injection-locking of the **VCO** is performed through a weak inductive coupling between the oscillator inductor and an external coil fed by a signal generator providing a pure harmonic exactly at the same average oscillation frequency **Figure. 5.7**. The external coil is placed on top of the oscillator inductor, some millimeter above the chip surface. The power of the signal generator is trimmed in order to achieve a locking-range of few **KHz**, small enough to avoid wrong Phase-Noise measurements in the frequency offsets of interest (**100 KHz - 10 MHz**). The frequency locking procedure is repeated for every **BIT** configuration (hence different free-running oscillation frequencies).

The measured Phase-Noise spectrum plot is reported in **Figure. 5.8** while **Figure. 5.9** shows the Phase-Noise measured at **1 MHz** Δ**f** from the carrier

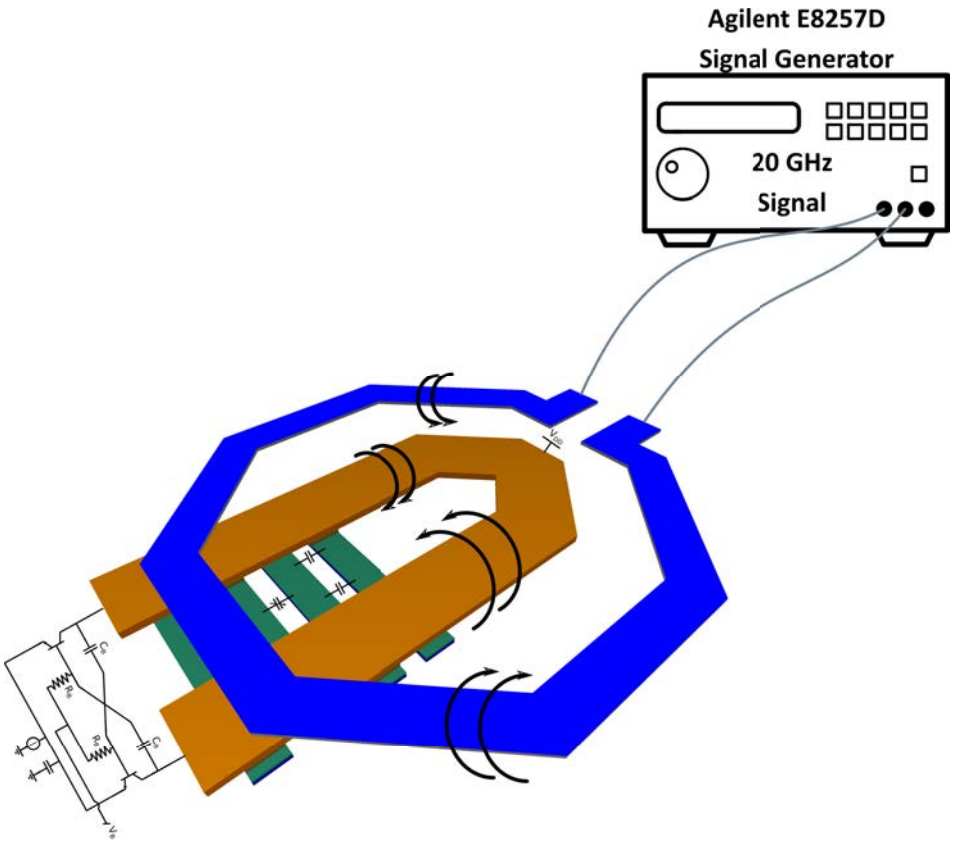


Figure 5.7: Inductive Injection-Locking. Inductor and coil dimensions are not in scale

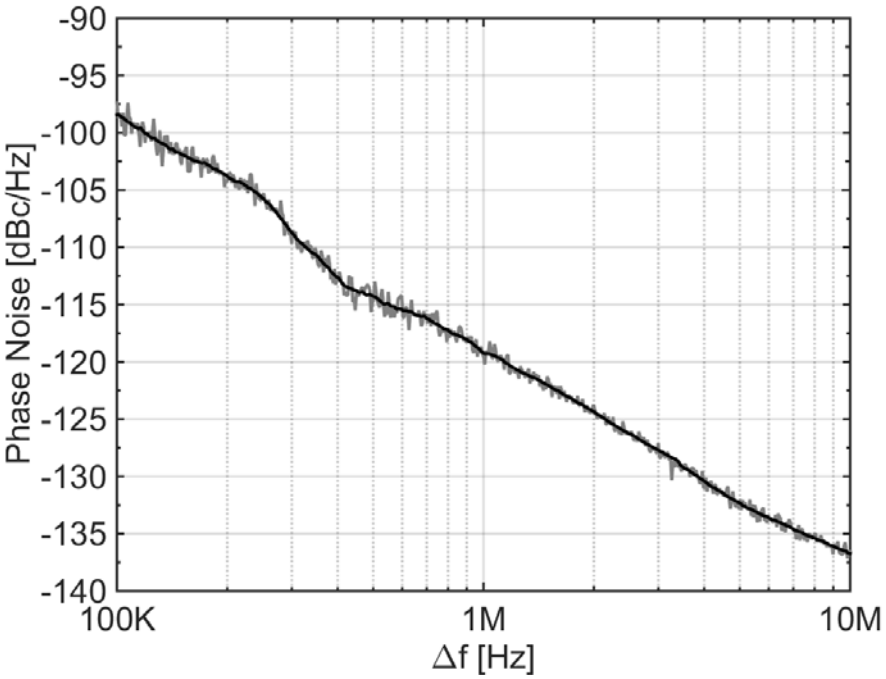


Figure 5.8: Phase-Noise spectrum plot at **20 GHz** carrier.

in each sub-band performing coarse digital tuning.

As it can be seen the Phase-Noise spectrum is much more clean compared to that in **Figure. 5.2**. No more jumps in the spectrum is observed and the slope is **-20 dBc/Hz** from **100 KHz** to **10 MHz** proving that the adoption of **BJT** as core devices in the **VCO** design allows to achieve a corner frequency well below the targeted spec of **700 KHz** pointed out in the **Introduction** of this work. The reported Phase-Noise at **1 MHz** frequency offset from a **20 GHz** carrier is as low as **-119 dBc/Hz**.

Phase-Noise changes by **1.7 dB** due to the frequency shift from a **18.7 GHz** carrier to a **22.7 GHz** carrier.

In **Figure. 5.10** the oscillation frequency is reported as function of the digital control word. The small varactor provides a $\mathbf{K_{VCO}}$ of **260 MHz/V** and allows to continuously tune the oscillation frequency ensuring band overlapping in all sub-band. The overall Tuning-Range covered through digital and analog tuning is **19%**.

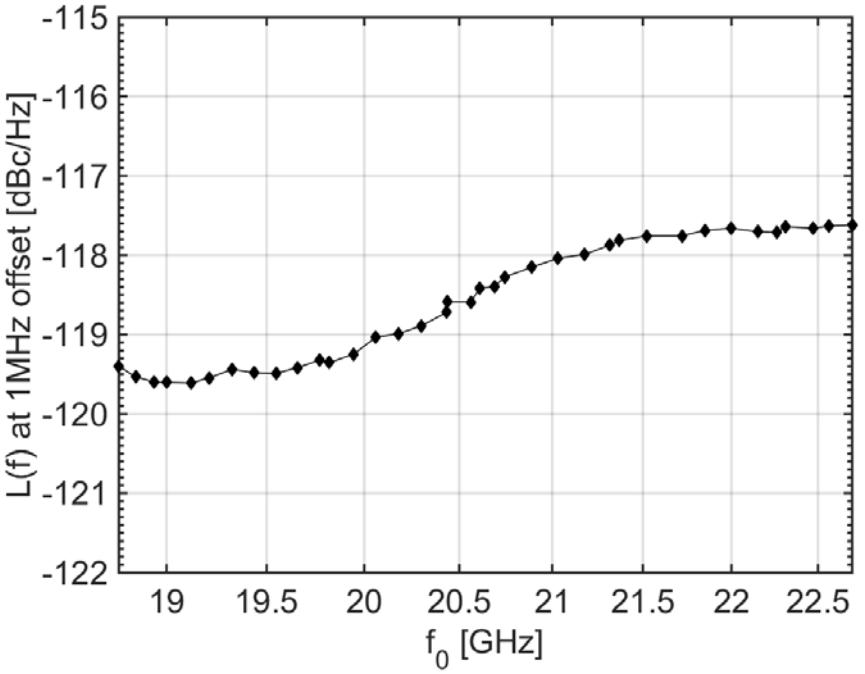


Figure 5.9: Measured Phase-Noise at **1 MHz** offset from the carrier as a function of the oscillation frequency.

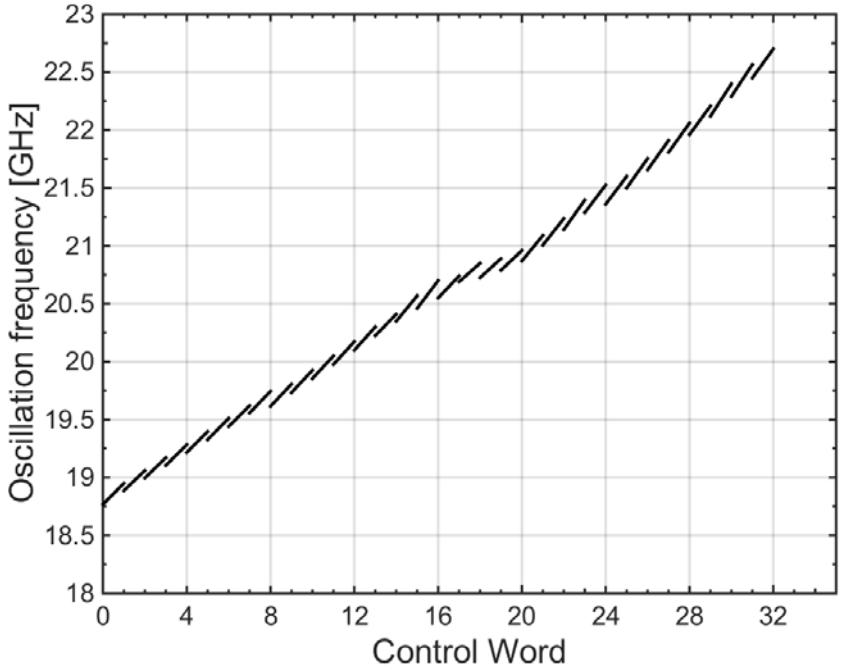


Figure 5.10: Oscillation frequency as function of control word.

5.3 Comparison with the State-Of-The-Art

Table. 5.1 reports the performance overview and comparison with *State-Of-The-Art*. As already discussed in **Chapter 1**, for fair comparison Phase-Noise performance reported in literature has been normalized to **1 MHz** offset from **20 GHz** carrier.

	[79]	[31]	[71]	[91]	[92]	This Work
Technology	S_iG_e HBT f_T = 200 GHz	S_iG_e HBT f_T = 200 GHz	180 nm BiCMOS	130 nm BiCMOS	180 nm BiCMOS	55 nm **BiCMOS**
f_0 [GHz]	20.5	22.1	20	52.5	35	**20**
Tuning-Range [%]	13	15	16	27	19	**19**
Phase-Noise$_{1\ MHz\ \Delta f}$ [dBc/Hz]	-117	-116	-115	-108	-110	**-119**
Phase-Noise$_{20\ GHz}$ [dBc/Hz]	-117.5	-116.8	-115	-116.4	-114.8	**-119**
V_{DD}	5.5	3.3	1	3	4.5	**2.5**
P_{DC}	50	33	7.5	132	190	**56**
FoM	186	188	192	181	178	**187**
FoM_T	188	191	196	189	184	192

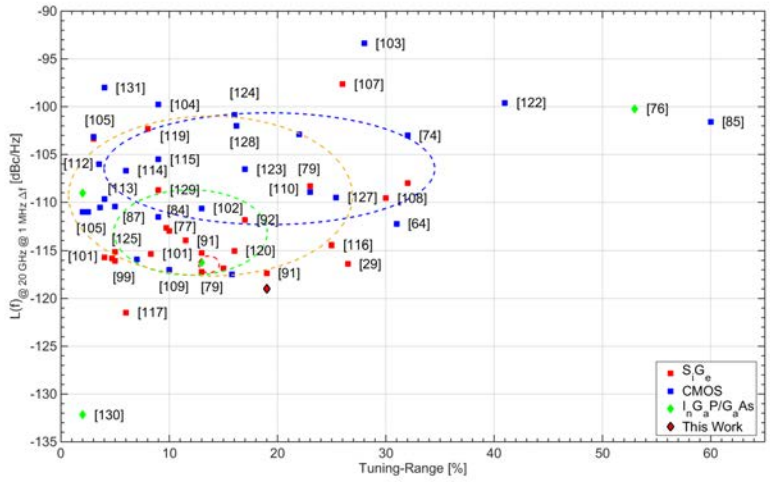
Table 5.1: mm-Wave oscillators performance overview and comparison.

Mm-Wave oscillators featuring $\mathcal{L}_{\mathbf{20\ GHz}} \leq$ **-110 dBc/Hz** are reported in the table. The proposed circuit achieves the lowest $\mathcal{L}_{\mathbf{20\ GHz}}$, with **FoM** and $\mathbf{FoM_T}$ in line with other **VCOs** from literature, and competitive Tuning-Range.

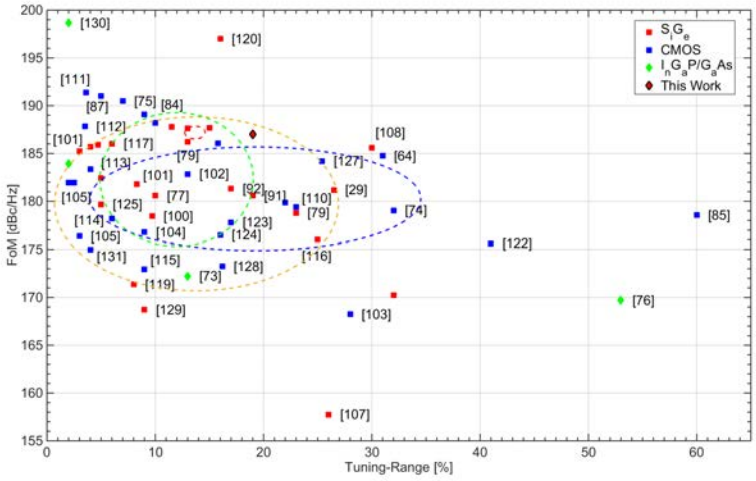
A more extensive comparison with the *State-Of-The-Art* is shown in **Figure. 5.11.a** and **Figure. 5.11.b** where, as already done in **Chapter 2**, Phase-Noise and **FoM** are plotted versus **TR** for many **mm-Wave VCO** implementations reported in literature. Measured data from the **FALCON** chip are now added to the plots.

5.4 Conclusion

In this chapter, measurement results on the proposed frequency-synthesis building blocks were presented. Leveraging inductive coupling and Injection locking techniques to reduce **VCO** drift during measurements, a Phase-Noise as low as **-119 dBc/Hz** at **1 MHz** frequency offset from a **20 GHz** carrier has been observed while the corner frequency is well below **700 KHz**. The Phase-Noise changes by **1.7 dBs** across the Tuning-Range due to the frequency shift



(a)



(b)

Figure 5.11: Oscillators $\mathcal{L}_{@20GHz@1MHz-\Delta f}$ *(a)* and **FoM** *(b)* Vs. **TR** taken from literature. Works are grouped by technology implementations. Circles represent the **RMS** performance area for each topology based on the *State-Of-The-Art* recorded works.

from a **18.7 GHz** carrier to a **22.7 GHz** carrier, resulting in an overall **19%** Tuning-Range covered through a **5-BIT** control word and an analog control voltage acting on a small varactor ($\mathbf{K_{VCO} = 260\ MHz/V}$) ensuring band overlapping in all the sub-bands. The oscillator draws **55 mW** from a **2.5 V** supply voltage.

Noise and Tuning-Range performance meet requirements for **64-QAM** transceivers derived in the **Introduction**, with several **dBs** of margin. Furthermore, the oscillator shows very competitive **FoM** and $\mathbf{FoM_T}$ values.

Conclusions

Point-to-Point wireless links in the **E-Band** (**71-76 GHz** and **81-86 GHz** bands) can provide high data-rate, easily-deployable, cheap and flexible backhaul solutions, important enablers for the mobile network evolution towards **5G**. The development of **CMOS/BiCMOS** integrated transceivers for **E-Band** backhaul applications can help reducing the cost and footprint of the equipment, but presents design challenges, mostly related to the use of spectrally-efficient high-order modulations.

In this dissertation, we addressed **LO** generation requirements for **E-Band** backhaul applications. First, we identified Phase-Noise specifications for the frequency synthesizer, and their dependence on the modulation order. Second, we designed a custom analog building block in **BiCMOS 55nm** technology, namely a **VCO**, to achieve the required performance with high power efficiency. The **VCO** leverages inductor shrinking to achieve ultra-low noise performance according to system requirements. The topology was studied in depth. A comparison between the most adopted **mm-Wave** architectures for frequency synthesis has been carried out. A **BJT Class-C** solution emerged as the most suitable candidate for an ultra-low Phase-Noise and wide Tuning-Range oscillator operating at **20 GHz**. The block provides an ultra-low noise **E-Band** frequency reference, suitable for **LO** generation in direct-conversion backhaul transceivers. The measured prototypes achieves around **-119 dBc/Hz** Phase-Noise, the lowest reported in literature at these frequencies over a **18.7-22.7**

GHz Tuning-Rrange, with **55 mW** power consumption.

Further developments will include the design of a block for frequency multiplication and generation of quadrature phases starting from the realized frequency reference (e.g. a polyphase filter or an injection-locked oscillator), as well as the integration of the blocks in a complete E-Band frequency synthesizer.

List Of Publications

Articles In Peer Reviewed Journals

- N. R. Lacaita, M. Bassi, A. Mazzanti and F. Svelto. "A Low-Noise K-Band Class-C VCO For E-Band 5G Backhaul Systems in 55nm BiCMOS Technology".™ In: *2017 IEEE Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, (Jun. 2017), Pag. 193-196.

- N. R. Lacaita, M. Bassi, A. Mazzanti and F. Svelto. "A K-Band Low-Noise Bipolar Class-C VCO For 5G Backhaul Systems in 55nm BiCMOS Technology".™ In: *2017 IEEE BCTM Conference*, (Oct. 2017). Submitted and accepted.

- N. R. Lacaita, M. Bassi, A. Mazzanti and F. Svelto. "A K-Band Low-Noise Bipolar Class-C VCO For 5G Backhaul Systems in 55nm BiCMOS Technology".™ In: *2017 IEEE Integration, the VLSI journal of*, (Dec. 2017). Invited and Submitted.

- F. Piri, M. Bassi, N. R. Lacaita, A. MAzzanti and F. Svelto. "A >40dB IRR, 44% Fractional-Bandwidth Ultra-Wideband mm-Wave Quadrature Generator for 5G Network in 55nm CMOS".™ In: *2018 International Solid-State Circuits Conference (ISSCC)*, (Feb. 2018). Accepted.

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