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Design and characterization of CMOS SPADs for charged particle detectors

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Contents

Introduction

Charged particle tracking applications at future colliders call for high granularity, low material budget, low power consumption, high spatial and time resolution and radiation hardness. In order to satisfy such severe requirements, the particle physics community, on the one hand, is trying to update well established technologies, like hybrid pixel and monolithic detectors, on the other, is exploring new solutions overcoming the intrinsic limitations of the older ones. Hybrid pixels can provide good granularity and have been and will be leveraged in the LHC (large hadron collider) experiments and in their planned upgrades. The main issue in using this kind of technology consists in the relatively large amount of material they add in the sensitive region of the experiment. Thinning them down, while reducing the material budget in the detection region, also affects the signal to noise ratio by reducing the amount of collected charge. Monolithic detectors, integrating the front-end electronics in the same substrate as the sensor, can provide a good trade-off between power dissipation, granularity and material budget. Moreover, they can be thinned down to a few tens of microns still providing good signal to noise ratio.
The properties of SPADs (single photon avalanche diodes), mostly employed in the photon detection domain in applications such as optical ranging, fluorescence lifetime imaging, positron emission tomography and Raman spectroscopy, may actually be beneficially exploited for charged particle tracking. SPADs can provide huge internal gain, with no need for pre-amplification (therefore reducing power dissipation) and high spatial resolution. Moreover, the amount of detector material can be substantially reduced, as the sensitive volume of a SPAD is limited to the very thin depleted region around the p-n junction. Use of a CMOS technology for the design and fabrication of the sensor lends itself naturally to the monolithic integration of the processing electronics with the sensing element. On the other hand, noise, in the form of random generation of dark current pulses, is one basic characteristic of avalanche diodes potentially jeopardizing their use as charged particle detectors.

This thesis work presents the development of a new type of silicon sensor for charged particle detection, with emphasis on the device characterization and on the implementation of the measurement system. The work that will be presented in the next chapters has been carried out in the framework of the APiX2 project funded by the Italian Institute for Nuclear Physics (INFN).
The aim of the APiX2 project is to develop, in a monolithic structure, an innovative position-sensitive pixelated sensor based on the vertical integration of SPADs.
The first chapter begins with a description of avalanche photodetectors (APD), discussing their working principle and their two different operating regions, focusing in particular on the Geiger-mode detector, which is another name of a SPAD. Different techniques to manage the signal provided by the sensor are presented together with a definition and discussion of the Dark Count Rate (DCR) and breakdown voltage parameters. As a final part of the chapter, more details about the APiX2 project will be provided.
The second chapter is focused on the description and characterization of a test chip designed to evaluate the features of one of the technologies investigated within the APiX2 project. First the chip, consisting of an array of SPADs with integrated front-end electronics, is described. Then, the automated measurement setup used for the chip characterization is discussed.
The third chapter is focused on the results obtained in terms of DCR curves and breakdown distribution. The data presented in the chapter will also include the outcome of an irradiation campaign performed to evaluate its radiation tolerance. The effect of temperature on the DCR has also been investigated, both before and after irradiation.
The fourth and last chapter deals with the description of a new chip designed to implement the dual tier concept proposed by the APiX2 project. The design results from the outcomes of the characterization of the first chip and of other circuits developed within the APiX2 collaboration. In particular, in this chapter, the main features of the new chip are presented together with a description of the integrated electronics, with an emphasis on the most important improvements on previous versions of SPAD arrays.

Chapter 1

SPADs and the APiX2 project

Continuous evolution and progress in science requires a costant refinement of sophisticated experimental techniques.
In photon counting applications, for many years, non solid-state vacuum-based devices, such as Micro Channel Plates (MCP) and Photo Multiplier Tubes (PMT), have been adopted owing to their very good performance in terms of noise and sensitivity, spatial resolution and timing characteristics. On the other hand they suffer from limitations mainly originating from their high operation voltage, large power consumption and high cost [1]. The turning point in photon detection applications happened when solid-state avalanche sensors were discovered and became available. Avalanche photodiode (APD) technologies introduce a way of counting photons at a microscopic scale and with the possibility to develop powerful techniques in light detection at the highest level of sensitivity: the single photon. Sensors with these properties, called *Single Photon Avalanche Diodes* (SPADs), offer an excellent timing resolution [2] and, due to this, are considered the natural candidates for the next generation of photon detectors in which high time resolution is one of the main specifications.
Charged particle tracking systems, mainly based on hybrid pixel technology, have been originally developed for physics applications in which collisions at high-energy may produce particles whose direction, identity and energy need to be measured. In these applications, hundreds of particles need to be simultaneously detected with micrometer spatial resolution and nanosecond timing precision. Use of such advanced devices is now extending to other fields, like imaging of heavy charged particles for radiography [3], biology [4] and astron-

omy [5]. The properties of SPADs can be leveraged in charged particle tracking applications, as they have the potential for providing thin, low power and highly sensitive detection systems based on commercial CMOS technology. In this chapter, after a brief presentation of the semiconductor detector operating principle, the SPAD operation is described, together with the signal processing techniques. The main characterizing parameters concerning single photon avalanche sensors are then discussed, focusing, in particular, on shot-noise and breakdown voltage. The last part of the chapter is dedicated to discussing the goal of the APiX2 project, which consists of developing a dual-layer charged particle detector based on SPAD sensors.

1.1 Operating principle of semiconductor detectors

In a radiation detection system, the sensor is that part delivering the signal to the readout electronics as a consequence of the interaction of a particle with it. Photodiodes are the most common and versatile semiconductor-based sensors used in optoelectronic systems [6]. They consist in a reverse biased p-n junction which can also be operated at high electric fields, in that case achieving an internal gain. By solving the Poisson equation at a p-n junction, it is possible to calculate the width of the depletion region, which is the actual sensitive volume of the detector, and the electric field as a function of the applied voltage. In particular, the width of the depletion region is given by

$$W = x_n + x_p = \sqrt{\frac{2\epsilon_0\epsilon_{Si}}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)(V_{bi} - V_k)}, \tag{1.1}$$

where x_n and x_p represent the width of the depletion region in the n- and p-side of the junction respectively, N_D is the concentration of donors, N_A the concentration of acceptors, V_k is the applied voltage, q is the elementary charge, ϵ_0 and ϵ_{Si} are the vacuum and silicon permittivity respectively and V_{bi} is the built-in voltage,

$$V_{bi} = \frac{kT}{q} ln\left(\frac{N_D N_A}{n_i^2}\right). \tag{1.2}$$

In the previous equation, n_i is the intrinsic carrier concentration, k is the Boltzmann constant and T is the absolute temperature. Usually, in silicon sensors, the junction is made by a highly doped and shallow p^+ diffusion in a lowly doped bulk material. Therefore, in (1.1) the term $1/N_A$ can be neglected and the depleted region is much deeper into the side of the junction with lower doping concentration (as shown in Fig .1.1). Generally the external

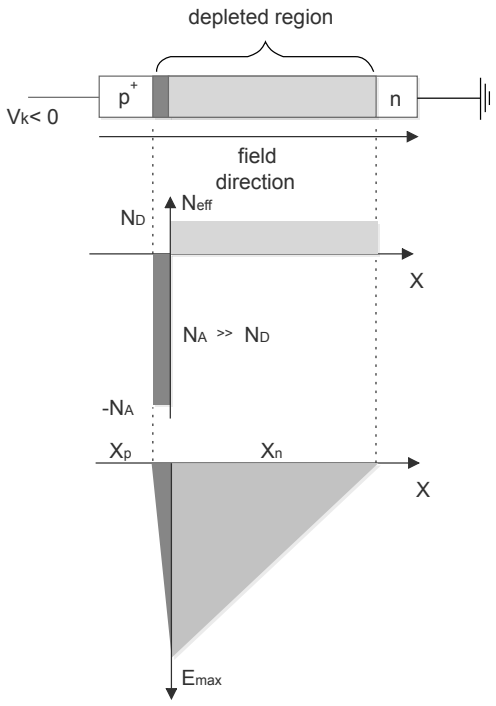


Figure 1.1: depletion region and electric field for a p-n junction with $N_A \gg N_D$.

voltage applied to the sensors is much larger than the built-in voltage, which can be neglected. Under these assumptions, the total width of the depletion region can be approximated as

$$W \approx x_n \approx \sqrt{\frac{2\epsilon_0 \epsilon_{Si}}{qN_D} V_k} \tag{1.3}$$

As it can be noticed, the dimension W of the depleted region increases proportionally to the square root of the voltage applied to the sensor terminals. By futher increasing V_k, the total width may increase over the full body of the device. As also shown in Fig. 1.1, the electric field reaches the maximum value

$$E_{max} = 2V/W \approx \sqrt{\frac{2qN_D}{\epsilon_0 \epsilon_{Si} V_k}} \tag{1.4}$$

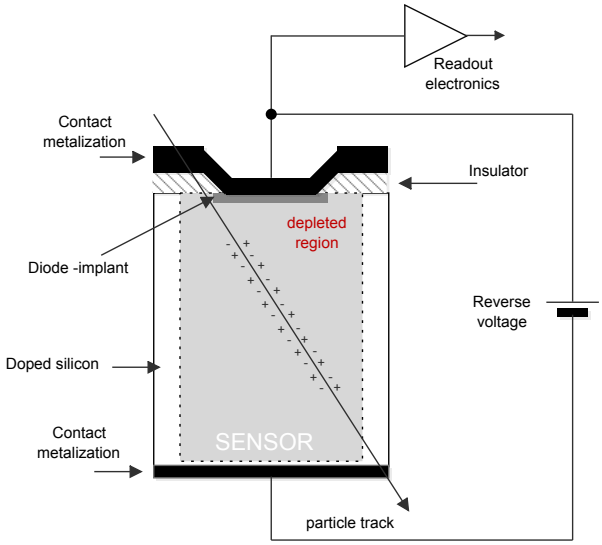


Figure 1.2: simplified cross-section of a semiconductor detector.

directly at the junction and decreases linearly till the end of the space region because of the constant doping concentration.
Fig. 1.2 shows a generic cross-section of a semiconductor sensor. The interaction of a charged particle with the silicon lattice is responsible for the generation of free carriers (electrons and holes) which are accelerated by the electric field E, perpendicular to the junction, toward the electrical contacts of the sensor. The current signal is, at a later time, processed by the readout electronics.

1.2 Avalanche sensors

Avalanche photodiodes represent a step towards higher sensitivity photon detectors as they can provide an internal gain by means of high fields at the junction. As mentioned in the previous section, a particle hitting a reverse biased p-n junction generates free carriers which, just upon generation, can be considered as free particles having a mean kinetic energy of $\frac{3}{2}kT$. Under

the effect of the electric field at the junction, an electron (or a hole) can reach an energy sufficiently high to generate new electron-hole pairs by colliding with lattice atoms. This process, called impact ionization, is responsible for the avalanche mechanism; the original carriers, together with the secondary electron-hole pairs, are accelerated by the high electric field in the junction, triggering a positive feedback in which the generation of more carriers takes place. An electron-hole pair can be generated by a particle crossing the detector or by thermal generation. Whichever the case is, the avalanche magnitude depends on two leading factors. One is related to the rate at which holes and electrons are collected at the device terminals leaving the depleted region, whereas the other concurrent factor is the carrier ionization rate. This latter parameter is related to the number of pairs generated by a carrier per unit distance travelled into the semiconductor and increases by increasing the electric field in the junction.

The concept of avalanche gain based on carrier multiplication makes it possible to push timing resolution down to tens of picoseconds. The gain is strictly dependent on the bias voltage applied to the detector. In order to have a constant gain, the field across the active area has to be uniform.

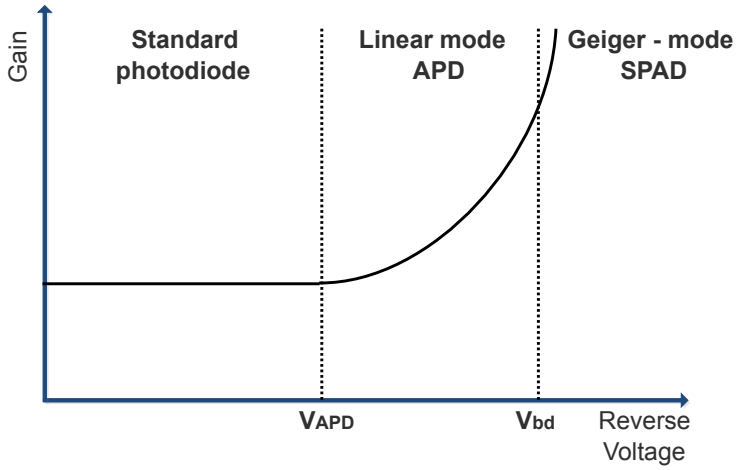


Figure 1.3: gain-voltage characteristic for photodiodes working in different operating regions.

Depending on the reverse bias voltage applied, as it is shown in Fig. 1.3, an avalanche photodiode can be used in two different operating regions, which are defined based on breakdown voltage parameter (V_{BD}): the linear mode the and Geiger-mode regions. The linear region is located below V_{BD}. Here the detector is able to provide an output current proportional to the hitting light intensity as a result of the balance between ionization and extraction rate. In the linear mode, moreover, only electrons are able to reach a sufficiently high kinetic energy capable to produce new electron-hole pairs by impact ionization. For this reason the gain reachable by multiplication is moderate and a strong excess noise may affect the APD making single photon detection difficult. The other operating region for the avalanche detectors, which is the one considered in this thesis work, is the Geiger mode. As opposed to the linear mode, in the Geiger region the device is biased well above the breakdown voltage. In this case, the electric field perpendicular to the junction is so high that also holes are able to generate new electron-hole pairs. The ionization rate becomes much greater than the extraction rate and, consequently, the output current increases to very high values, with gains that may be well in excess of 10^5. In the next section, the operating principle of the Geiger-mode avalanche diode, also known as SPAD, is discussed.

1.2.1 Single Photon Avalanche Diode (SPAD)

The characteristics of single photon avalanche diodes, such as the huge internal gain, lead to their use in photon detection applications requiring very high sensitivity, like fluorescence lifetime imaging, positron emission tomography, optical ranging and Raman spectroscopy [7], [8], [9], [10]. SPADs also represent the fundamental building block for silicon photomultipliers (SiPMs). Since they are magnetic-field insensitive, they represent a valid alternative to vacuum tube PMs, for instance, in the medical diagnostic field, in many low light level applications [11] and in gamma ray detection [12]. More recently, SPADs have been also proposed for applications to charged particle tracking due to their high spatial resolution. One other advantage of SPADs, also related to their huge internal gain, is that, in a charge measuring system, no pre-amplification is needed, therefore reducing the overall power dissipation. It is worth to notice that typical SPAD dimension depends on the application for which the detector will be used for. With reference to Fig. 1.4, in the quiescent state the sensor is biased at the voltage V_{BIAS} above the breakdown V_{BD} and no current flows through the device (the difference between V_{BIAS} and V_{BD} is usually called excess bias voltage, V_{EX}). The device is switched on as soon as a single charged carrier is injected in the high field region, generating a self-

sustaining avalanche multiplication process which allows the diode to provide a constant macroscopic current (in the milliampere range). If the charged carrier is generated by a charged particle or a photon interacting with the lattice, the fast current onset corresponds to the particle arrival. While the sensor is in the on state, it is insensitive to the arrival of other particles and, for this reason, a reset phase of the device is mandatory in order to suppress the avalanche. The reset phase (or recharge) is performed by an external quenching circuit which is able to reduce the biasing down to, or below, the breakdown voltage point, as is shown in Fig. 1.4. In this way the detector is reinitialized to its starting conditions and will be again able to detect particles. In other words, a single photon avalanche diode can be seen as a bistable circuit in which the detection may be performed by using a simple comparator and, in order to use it as a photon detector, a quenching/recharging network is needed. It is worth noticing that the reset operation takes a non zero time. This is responsible, as a primary consequence, for a dead time after the detection of a particle, that has to be considered when evaluating the detection efficiency of SPADs. Nevertheless, in the last years, quenching circuits have been developed in such a way to integrate them directly with the detector, creating a monolithic structure

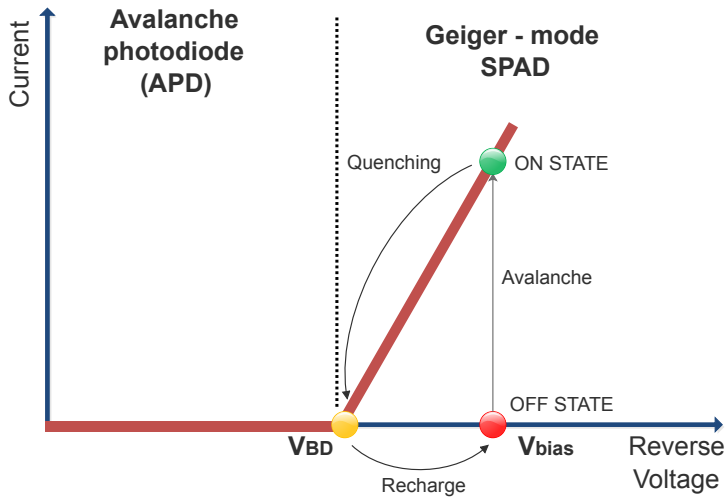


Figure 1.4: operation of a SPAD.

and leading to performance improvement. This has been made possible by the adoption of CMOS microelectronic technologies, which allows the designer to include in the same pixel both the electronics and the sensitive element, with no need for high-density interconnections between different dice.

1.2.2 Quenching circuits

Due to the working principle of the Single Photon Avalanche Diode, an additional quenching circuit is necessary for its proper operation. SPADs, as opposed to APDs, do not amplify the current linearly. As they are operated in Geiger regime, after the avalanche has been triggered they produce a current whose final value is the same whatever the number of carriers initiating the avalanche. As already mentioned, a quenching network is then needed to stop the avalanche and make the device capable of detecting a new particle. Different quenching circuits can be implemented in order to suppress the avalanche and, depending on which topology is chosen, the device performance could be affected in different ways. The choice of using one kind of quenching circuit instead of another is therefore strictly related to the application for which the

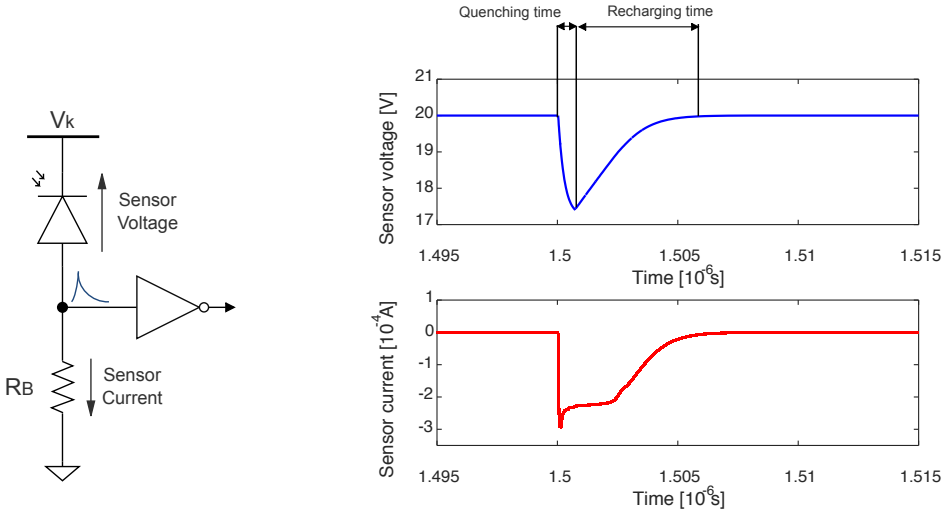


Figure 1.5: basic schematic of a passive quenching circuit and SPAD voltage and current signals when an avalanche occurs.

detector is adopted.
Since the detector is a two terminal diode, it may be connected either with a positive potential at the cathode, or with a negative potential at the anode. In any case, the SPAD should be attached to the quenching network in a way that leads to minimize its dead time and, as it will be explained later on, the charge quantity flowing in an avalanche event. These two parameters depend strongly on the parasitic capacitance associated to the diode terminal which will be connected to the quenching network [13]. SPADs fabricated in planar technology are not symmetrical and, for this reason, one terminal may feature a higher (or lower) parasitic capacitance compared to the other terminal. Two main categories of quenching circuits can be defined: passive and active quenching circuits.
Passive quenching circuit (PQC) with series resistor. This is the simplest way to bring the sensor bias voltage below breakdown once an avalanche has occurred. It consists of placing a high-value ohmic resistor (R_B) in series to the sensor, which is biased through the external voltage V_k applied to the cathode terminal, in such a way that the voltage drop on the resistor, caused by the avalanche current, lowers the bias voltage until the breakdown level is reached, as shown in Fig. 1.5. The signal produced can be detected by means of a threshold crossing logic circuit, such as a comparator or an inverter with a threshold voltage V_{TH}. As a matter of fact, the avalanche current rises very quickly to its peak value causing a voltage drop across the resistor equal to the excess bias (V_{EX}). Subsequently, the anode is discharged with an exponentially decreasing voltage and with a time constant equal to

$$\tau = C_P(R_S||R_B) \tag{1.5}$$

where C_P is the parasitic capacitance relevant to the depletion region at the junction while R_S is the space-charge resistance in the p-n junction [14]. The complete model of a SPAD device is shown in Fig. 1.6 in which a constant current generator I_A is also included to model the avalanche current. As a result, the quenching resistor affects the maximum number of detectable photons per unit time [15]. Moreover, the resistor R_B has to be chosen is such a way that the maximum value of the peak current, which is $\approx V_{EX}/R_B$, should not be too high so as to avoid that the avalanche continues due to the large number of carriers in the space charge region. On the other hand, the current should not be too small because, in this case, the avalanche may get self-quenched due to the probability that, after a random time, all the carriers have left the space charge region without further ionization [16]. Once the value of the resistor is chosen, also the maximum current is fixed and the quenching time (t_Q) can

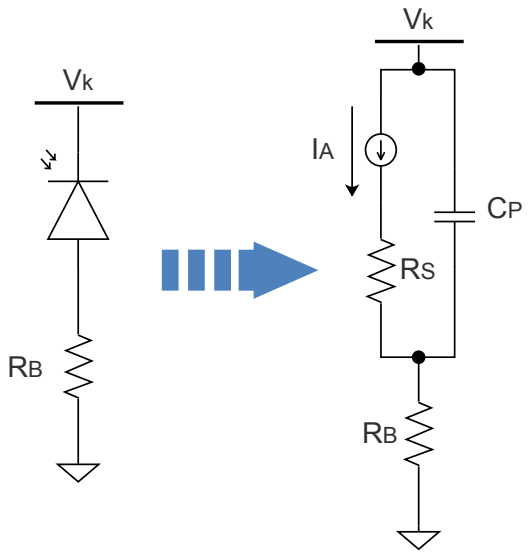


Figure 1.6: equivalent SPAD model.

be evaluated as follows

$$t_Q = \tau \ln\left(\frac{I_0 - I_F}{I_{QT} - I_F}\right) \tag{1.6}$$

in which $I_0 = V_{EX}/R_S$, $I_F \approx V_{EX}/R_B$ and I_{QT} is the quenching threshold current. The overall avalanche charge, which is given by the time integral of the current flowing from the avalanche onset until quenching and is equal to

$$Q = V_{EX} C_P \left[1 + \frac{I_F \ln\left(\frac{I_0 - I_F}{I_{QT} - I_F}\right) - I_{QT}}{I_0}\right], \tag{1.7}$$

has to be minimized. Minimization of the avalanche charge is required because the energy dissipated by the detector, during an avalanche event, is proportional to the breakdown voltage and to the amount of charge delivered [16]. Especially in the case of devices with a high breakdown voltage, minimization

of the total avalanche charge makes it possible to reduce mean power dissipation, which is defined as the product of the dissipated avalanche energy and the counting rate. For a given excess bias the only way to minimize the overall charge is by decreasing the recharging time [17] or, on the other hand, by reducing the total parasitic capacitance. A small parasitic capacitance can be obtained, for instance, by integrating the quenching electronic with the sensor. The effect on the quenching time of the resistor R_B is shown in Fig. 1.7. It is worth noticing that, decreasing the quenching time by using a smaller resistor R_B leads to a higher peak of the final current I_F.

Another reason for minimizing the avalanche current is related to the so called after-pulsing phenomenon [18]. When an avalanche is produced, some carriers can be captured by trapping centres in the space charge region and, after a random time, released. Once released they may trigger new avalanches in the junction, starting in this way a new cycle in which other carriers can be trapped again. The after-pulsing rate is related to the type and number of traps present in the silicon, but also to the total amount of charge produced during an avalanche event. A possible solution to reduce this effect consists of keeping, after the quenching operation and for a certain time interval, the bias voltage of the SPAD below its breakdown level. The time interval during

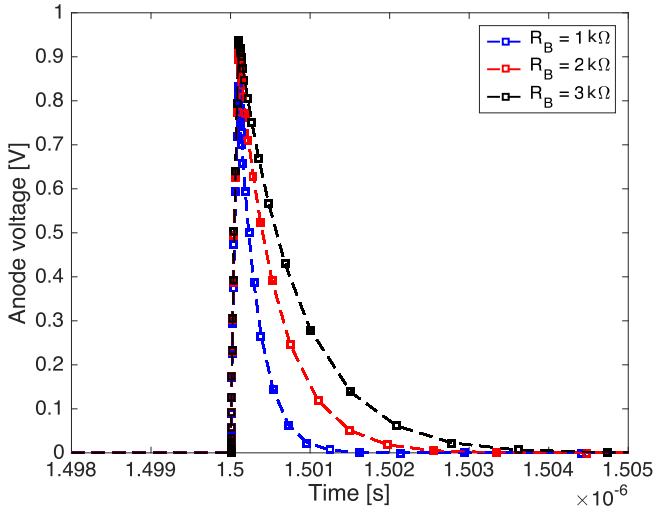


Figure 1.7: example of quenching time for different values of the resistance R_B.

which the bias voltage of the SPAD is below the breakdown level is called off-time. During this time, the trapped carriers can be released without triggering any additional avalanche. In the simplest configuration of the passive quenching, reported in Fig. 1.5, after-pulsing cannot be prevented, unless additional circuitry is implemented for this purpose. Another disadvantage of the passive quenching circuit is related to the reset time, which is the time needed to bring the bias voltage of the sensor back to its steady state after the avalanche has been quenched. In PQCs configured as in Fig. 1.5, the bias voltage starts to increase, after the quenching operation, with a time constant given by $R_B C_P$. Reset time may be some order of magnitude bigger then the quenching time. A long reset time causes, as the main drawback, a limitation in the maximum counting rate affecting the overall performance. Actually, a technique to overcome this problem consists of placing on the cell an active reset circuit [19] as the one shown in Fig. 1.8, where the anode of the sensor is discharged by means of an NMOS transistor controlled by a dedicated logic circuit.
Summarizing, passive quenching techniques based on series resistor offer simplicity, small area occupation when integrated directly with the detector and low cost with some penalty in terms of reset time and quenching time.

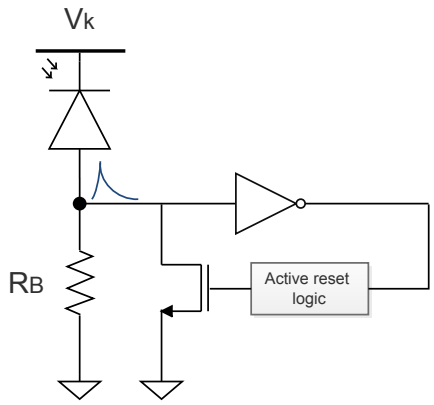


Figure 1.8: passive quenching circuit with an additional active reset control.

NMOS based passive quenching circuit. Starting from the resistor-based passive quenching configuration, another possible solution is using an NMOS transistor to quench the avalanche of the SPAD (Fig. 1.9). As in the case of the series resistor, also with the NMOS quenching transistor optimization of the circuit is required for best operation. In particular, quenching optimization is needed with respect to dead-time and jitter. As a matter of fact, if a comparator or an inverter is used to detect the anode signal, the threshold crossing should be as steeper as possible in order to minimize the crossing uncertainty, thus fast quenching time is required. This is a crucial point because the noise affecting the anode signal leads to a random variation in the dead-time period of the detector, thus affecting its performance. In particular, as shown in Fig. 1.9, if the quench transistor has a too small W/L ratio, the anode discharge will take a longer time, resulting in a longer dead-time period.

Active quenching circuit (AQC). This kind of quenching topology has been introduced in order to overcome the disadvantages of the passive one (slow reset time due to not well defined quenching time). The main difference stands in the possibility to control and change the voltage across the detector once an avalanche is detected by the readout circuit [20]. The control of the bias voltage makes it possible to keep the sensor in an operating region below the breakdown voltage for a well defined time period. As a consequence,

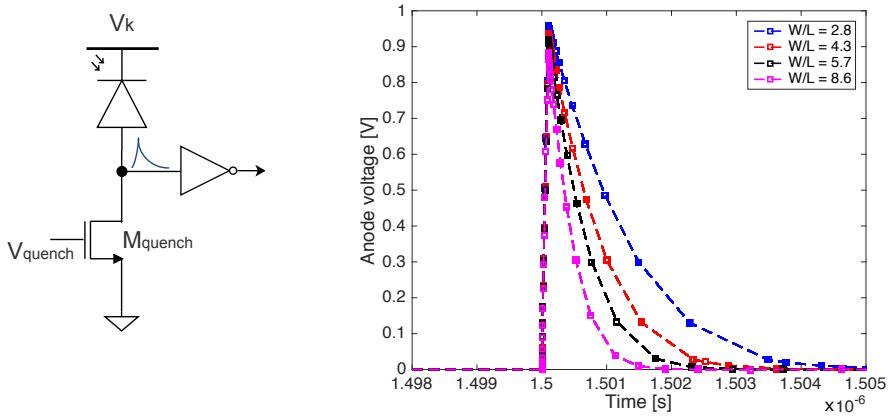
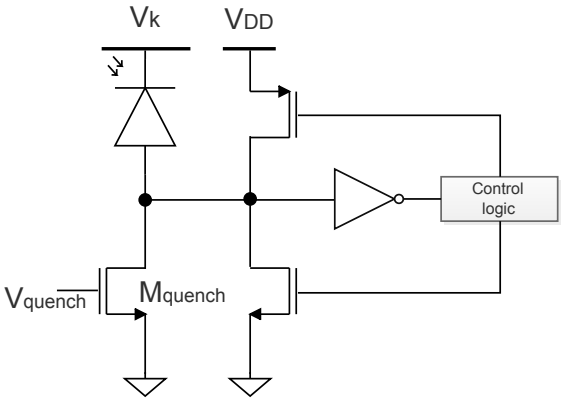
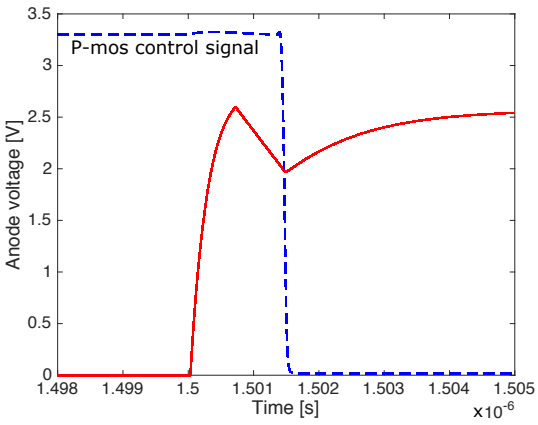


Figure 1.9: basic schematic of a passive quenching circuit with NMOS quenching transistor and quenching time variation as a function of the W/L ratio.



(a)



(b)

Figure 1.10: active quenching circuit configuration (a) and evolution of the anode signal when the PMOS control signal occurs (b).

the quenching time is less sensitive to the statistical fluctuations of the anode signal due to avalanche multiplication processes. The SPAD is configured as shown in Fig. 1.10. The AQCs quenches the avalanche by means of an NMOS transistor which makes it possible to implement also a fast reset of the sensor

(see Fig. 1.8). Therefore, when an avalanche is triggered, the current starts to flow. Then, the control logic senses the avalanche and starts the active quenching operation, keeping the SPAD off for a time interval, which can be made programmable, and restoring the initial condition and the capability of detecting new particles. In the circuit shown in Fig. 1.10, the condition in which the sensor is kept off is performed through a PMOS pull-up transistor with its gate connected to the control logic. By switching on the PMOS transistor, the anode of the SPAD is kept to V_{DD}, lowering the voltage across the sensor. Depending on the time during which the detector is kept off, the after-pulsing phenomenon is drastically reduced since the trapped carriers, released after a random time, can not trigger new avalanches by the fact that the sensor is no longer biased above its breakdown voltage. The total avalanche charge can be reduced by integrating, as in the case of PQCs, the quenching electronic with the sensor [21], thus reducing the parasitic capacitance associated to the anode terminal. The total avalanche charge also depends on the delay of the quenching activation; if this delay is too long, the avalanche charge is almost equal to that of a PQC but, if the active electronics reacts very quickly to the avalanche event, then the total charge can be limited accordingly [18].
The main disadvantage of the AQC solution is the area occupation. In particular, the AQC area occupation is larger than the area taken by the PQC, which can be a limitation for the integration process.

1.3 Dark count rate and breakdown voltage

In avalanche detectors operated in Geiger-mode, two important parameters, which have been studied in this thesis work and affecting the device operation, are the Dark Count Rate (DCR) and the breakdown voltage.
The DCR is defined as the rate of avalanche events caused by non photon-generated carriers, and is measured in Hertz. In particular, the main causes for dark count phenomena are relevant to the thermal generation of carriers, diffusion of carriers from the neutral to the high field region, band to band tunnelling and after-pulsing phenomena. In the normal operation of the detector, an avalanche caused by a hitting particle cannot be discriminated from one due to a dark count event. For this reason, the dark count rate of the sensor should be reduced as much as possible in order to minimize ambiguities in the sensor operation. Assuming that thermal generation is the only source of the DCR phenomenon, the time interval between two subsequent dark events is expected to have an exponential probability density [22]. As a consequence the probability density function of the number of dark counts in a

given time interval follows Poisson statistics [23]. In particular, the probability of n avalanche events occurring in a time interval T can be expressed as

$$P(n,T) = \frac{T^n DCR_{av}^n}{n!} \exp(-TDCR_{av}) \tag{1.8}$$

in which DCR_{av}, the average DCR, is given by the product of the average number of carriers in the multiplication region per unit of time times the probability for which a carrier triggers an avalanche. From (1.8) the probability of at least one avalanche being triggered by a carrier in the space charge region in 1 s can be written as

$$P(n \geq 1, T = 1s) = \sum_{n=1}^{\infty} \frac{DCR_{av}^n 1s^n}{n!} \exp(-DCR_{av}1s) \tag{1.9}$$

and it's equal to

$$P(n \geq 1, T = 1s) = 1 - P(0) = 1 - \exp(-DCR_{av}) \tag{1.10}$$

where DCR_{av} is assumed to be expressed in Hz. The experimental measurement of the statistical distribution of the events makes it possible to evaluate if and how other mechanisms, affect the dark count rate. For instance, the presence of after-pulsing phenomena might alter the DCR distribution, which is instead expected to be of the Poisson kind in the case where thermal carrier generation were the only underlying mechanism.
Depending on the technology and the fabrication process, the dark count rate can be found to show huge differences from one device to the other. The fabrication process for SPAD sensors may involve dedicated technologies [24] or, as more recently has been proposed, a CMOS technology in which the sensor is monolithically integrated with the front-end electronics. It is worth noticing that the integration of the front-end electronics in the same substrate as the sensitive element reduces the area available for the active region of the sensor. This results in a reduction of the fill factor (FF), which is defined as the ratio between the active area of the sensor and the total area of the pixel. Using a dedicated technology for the SPAD fabrication allows the designer to optimize the device performance in order to achieve a lower DCR, while developing a SPAD in a CMOS technology requires a trade-off between the device performance and the available process features. In order to obtain a low dark count rate, both the fabrication process and the starting material must guarantee a low concentration of impurities and defects which, potentially, could create deep levels in the active region of the junction, thus increasing the DCR. Another critical point is the electric field in the depletion region of the

junction. The field should be small enough to avoid or reduce band to band tunnelling effects and field-enhanced carriers generation. The first attempts to develop SPADs in CMOS technology gave poor results in terms of SPAD performance [25]. However, while the fast evolution of CMOS processes was mainly driven by mass market applications, not necessarily compliant with monolithic device integration, nevertheless significant performance improvements have recently been obtained in CMOS SPADs [25].
The dark count rate changes approximately in a linear fashion with the active area of the SPAD, increasing as the dimension of the sensor increases [26]. Moreover, the DCR as a function of the excess bias voltage applied at the SPAD (V_{EX}), is strictly related to the nature of the p-n junction. For instance, in some cases, the DCR was found to increase exponentially with the excess bias voltage of the SPAD (V_{EX}) [27]. A higher biasing of the detector leads to a stronger electric field in the depleted region of the junction, therefore, increasing the probability that an electron (or hole) triggers an avalanche. Fig.1.11 shows the dark count rate variation for different operating temperatures and excess voltages V_{EX} applied to the sensor. In particular it can be observed that the dark count rate increases exponentially as the temperature increase, due to thermal generation of electron-hole pairs [28]. For this reason, in some applications, a cooling system may be used to cool down the detector and reduce DCR.
The other important parameter which has to be considered when an avalanche detector is implemented, is the breakdown voltage (V_{BD}). It depends mostly on the detector fabrication process and, in particular, on the doping concentration and doping profile of the p-n junction. The uniformity of the breakdown voltage is of paramount importance for the integration of SPADs in a detection system since all the sensors will be biased at the same voltage. If the breakdown voltage is not sufficiently uniform among the SPADs in an array, for a given applied voltage SPADs in different regions of the detector will feature different sensitivity and DCR. Advanced technologies tend to use high doping levels for both sides of the junction resulting in a low breakdown voltage for the SPAD. The main drawback in the case of a low V_{BD} is that the field in the small depleted region is very high leading to an increase in the dark count rate induced by tunnelling phenomena [29]. Additional implants can be used to decrease the V_{BD} if it is too high to manage on the chip.
It is important to know the breakdown voltage of the sensor because, as mentioned in the previous section, the SPAD, in order to work as a photon-detector, has to be biased above this voltage value for a sufficiently long time. By biasing the SPAD at the breakdown voltage, the probability that

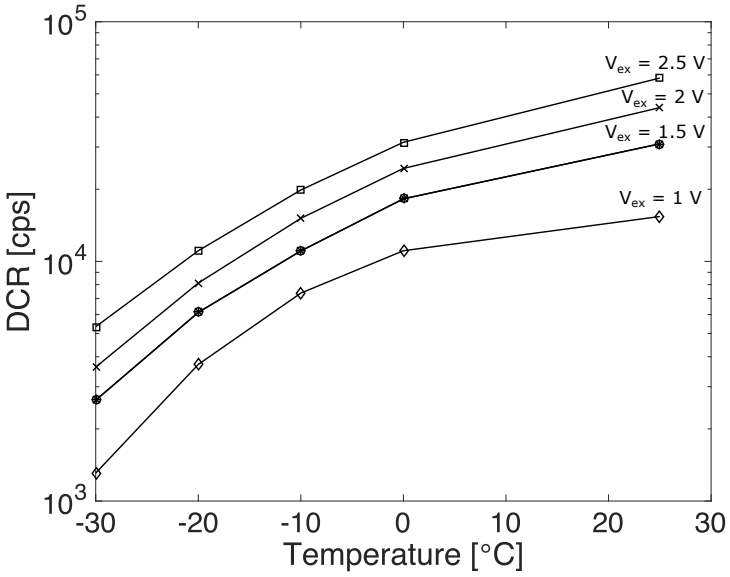


Figure 1.11: example of dark count rate as a function of temperature and excess bias voltage (V_{EX}).

an avalanche takes place due to generation-recombination phenomena in the junction is very low. Moreover, knowing the breakdown voltage of the SPAD used in a specific application, allows one to properly design the front-end electronics for optimum performance.

One important problem which may occur in the p-n junction of a SPAD is premature edge breakdown (PEB) [30]. The electrical-field at the edges of the active area may be higher than in the other regions of the junction. Therefore the probability that an avalanche is triggered may be larger there than in the center of the multiplication region. This may result in a higher level of dark count rate, consequently affecting the detector operation. Generally, guard ring structures are used to prevent this phenomenon [31]. Guard rings may consist of lowly doped regions at the periphery of the junction or shallow trench isolations (STIs) delimiting the active area, depending on the process features available for the SPADs fabrication.

Also, temperature may affect the breakdown voltage. The variation of V_{BD} with temperature can be understood as an effect of the thermal vibration of atoms. The energy of a free carrier accelerated by the electric field in the junction is proportional to the mean free path among the lattice atoms. The

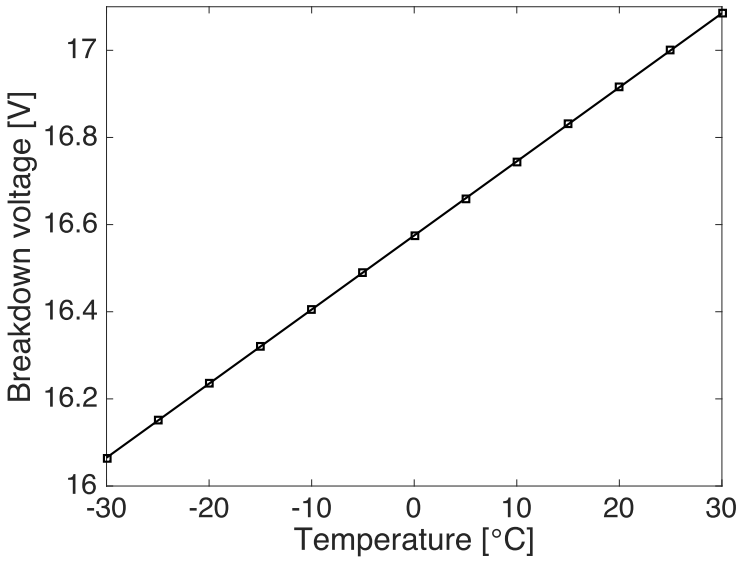


Figure 1.12: ideal breakdown voltage variations as a function of temperature.

breakdown voltage, as mentioned, is the voltage at which a free carrier reaches a sufficiently high energy to hit a lattice atom and create an electron-hole pair, which is then accelerated by the strong electric field and starts the avalanche multiplication process. As the temperature increases, the mean free path is reduced due to thermal agitation and the primary free carriers will need a higher energy in order to create electron-hole pairs. As a consequence, the breakdown voltage has to increase to satisfy this condition. The behaviour of the breakdown voltage is related to the temperature coefficient of the single photon avalanche diode, which depends on the fabrication process and, generally, varies linearly with the temperature [32] (see Fig. 1.12) according to the equation

$$V_{BD} = V_{BD0}[1 + \beta(\Delta T)]. \tag{1.11}$$

In (1.11), V_{BD0} is the SPAD breakdown voltage at room temperature, β is the breakdown voltage temperature coefficient of the sensor and ΔT is the temperature change.

1.4 The APiX2 project

The APiX2 project aims to design and fabricate a position sensitive detector based on the coincidence signal produced when a charged particle simultaneously strikes two overlapping pixels. Such a detector can be obtained by interconnecting with some technique (e.g., bump bonding) two SPAD arrays [33], [34], [35], as shown in Fig. 1.13. The project, funded by Istituto Nazionale di Fisica Nucleare (INFN) and started in 2014, involves people from University of Pavia and INFN Pavia, University of Siena, University of Pisa and INFN Pisa, University of Trento and the Trento Institute for Fundamental Physics and Applications (TIFPA). The project was proposed with the purpose of developing an innovative approach to the fabrication of charged particle detectors that could comply with the demanding specifications, in terms of material budget and noise, set by applications in the high energy physics and medical field. The design is based on commercial CMOS technologies, which, as already mentioned, can reduce the system complexity and increase its robustness. Use of CMOS technologies for SPAD fabrication, also in an array configuration, has already been demonstrated in a number of applications [36], [37], [38] .

1.4.1 Detector working principle

The APiX2 detector is implemented, as is shown in Fig. 1.14, by vertically interconnecting two layers of monolithically integrated CMOS SPADs. Each pixel includes both the sensitive area and the readout electronics. Reading out the coincidence signal of two vertically-aligned single photon avalanche detectors has the main advantage of drastically reducing the dark count rate

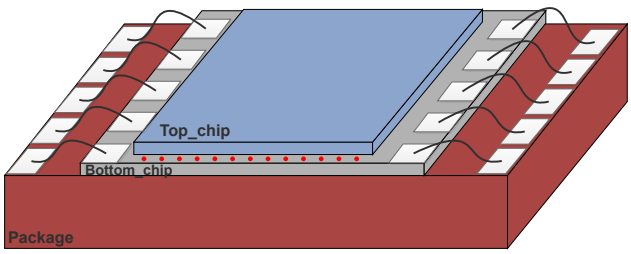


Figure 1.13: concept view of the dual-tier charged particle detector.

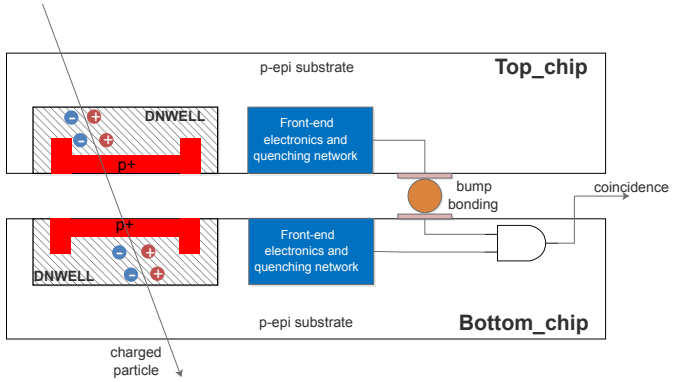


Figure 1.14: single cell of a dual-layer avalanche pixel detector according to the APiX2 approach.

of the detector. In particular, thanks to the pixel-to-pixel coincidence, the resulting dark count rate (DCR_C) of the dual-layer structure can be expressed as

$$DCR_C = 2(\Delta T) \times DCR_T \times DCR_B \tag{1.12}$$

where DCR_T and DCR_B are the dark count rates of the top and bottom pixel respectively, while ΔT represents the coincidence time window. From (1.12), if DCR_T and DCR_B are in the order of 1 kHz and ΔT in the order of 1 ns, then the coincidence DCR can be about a factor of 10^3 smaller than the DCR of the individual layers. The signal coming from the top sensor, which is propagated through the bump bonding to the bottom layer, can be degraded due to the parasitic capacitance associated to the bump connection. For this reason, the electronic channel in the top chip has to be designed properly in order to ensure minimal rise and fall times. As shown in Fig. 1.14, a true event is sensed by the electronics when a charged particle passes simultaneously through two overlapping sensors starting an avalanche in both of them. The frequency of random coincidence signals due to simultaneous dark counts in two overlapping pixels may be reduced, as already mentioned, by reducing the coincidence window duration ΔT. The effect of using different time windows is schematically shown in Fig. 1.15. For this purpose, it may be useful to design the readout electronics in such a way that it can provide a programmable coincidence time window duration, so that the best solution for improved noise

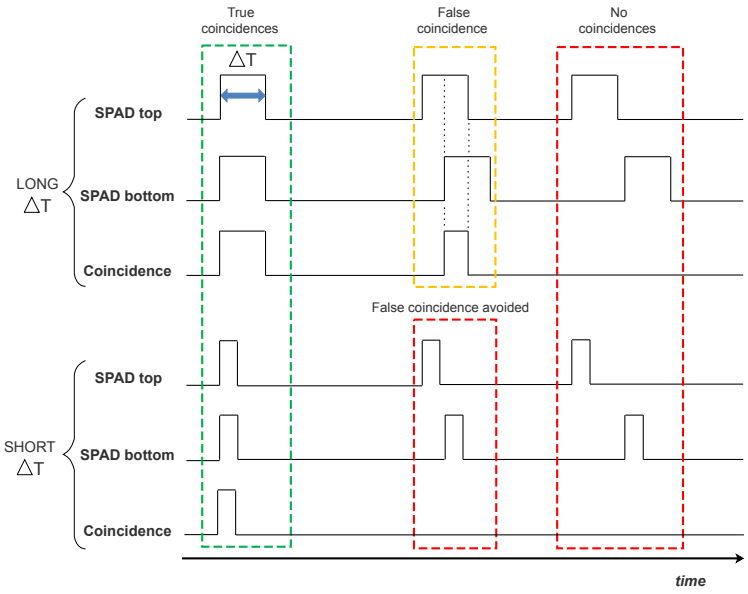


Figure 1.15: coincidence detection for different ΔT duration: in the case of a shorter ΔT, the DCR is reduced due to a higher probability of avoiding false coincidence.

rejection of the detector can be chosen. Depending on the readout electronics, the minimum time window duration may be strictly related to the features of the response of the detector to an incoming charged particle. In particular, the time jitter of the detector response, which may be in the order of several tens of picoseconds, may set a limit to the minimum ΔT [39]. The dual-tier approach demands a good alignment precision of the two overlapping layers. This characteristic is strictly correlated to the pixel dimensions and to the robustness of the technology adopted. Furthermore, interconnection through TSV (through silicon via) may be used in detectors featuring multiple layers connections.

1.4.2 APiX2 sensor prototypes

The development of a charged particle detector for tracking applications within the APiX2 collaboration was carried out through the design and the character-

	APIXFAB0	**APiX2**
Technology node	180 nm CMOS with HV (high voltage) option	150 nm CMOS standard technology
No. Layers	single layer	two layers ready for vertical integration
Total chip area	4.5 mm^2	57 mm^2 (30 mm^2 for the bottom layer + 27 mm^2 for the top layer)
Chip organization	test structures; array of SPADs	four SPAD arrays
Main purpose	study the technology features	assessment of the technology features; proving the feasibility of a dual layer sensor according to the APiX2 approach

Table 1.1: summary of the main characteristics of the two test chips designed and characterized in this work.

ization of a couple prototypes fabricated in two different CMOS technologies. The choice of two different technologies for the two prototypes was dictated by the need for exploring different solutions and evaluate which one offers the best performance in terms of DCR and breakdown voltage dispersion. The first prototype, called APIXFAB0, was designed in a 180 nm CMOS technology with high voltage option and includes a single layer SPAD array and other test structures. The main purpose of the chip was to study how the 180 nm CMOS technology behaves from the standpoint of the main SPAD features. In particular, the chip is comprised of sensors featuring different area and technology layers combined with different topologies of readout electronics. The chip was characterized in terms of dark count rate and breakdown voltage distribution. Radiation tolerance of the SPADs were also evaluated by irradiating a number of prototypes with X-rays and neutrons. Effect of the temperature on the SPAD performance was also assessed.
The second chip has been fabricated in a more scaled CMOS technology, with a minimum feature size of 150 nm, and can be seen as an evolution of another chip, fabricated in the same technology and successfully tested by the APiX2 collaboration. The new chip improves on the old one in terms of fill factor. It also explores new front-end electronics architectures and investigates the issues connected with the operation of large arrays of SPADs. In view of the fabrication of a dual layer detector, according to the APiX2 proposal, the new prototype was designed in two mirrored versions ready for vertical integration.

The features of the two chips, the one fabricated in the 180 nm CMOS technology and the one produced in the 150 nm technology are summarized in Table 1.1 and will be described and discussed in the next chapters of this thesis work.

Chapter 2

APIXFAB0: chip design and test setup

This chapter will be devoted to a detailed description of the APIXFAB0 chip, focusing on the design features of the circuit and discussing the working principle of the incorporated structures. In particular, the different topologies of quenching circuits implemented in the chip will be presented together with the description of the two different kinds of single photon avalanche diodes tested in this work. Then, the operation of the fully automated measurement system for the characterization of the chip will be presented and discussed.

2.1 Chip description

As mentioned in the previous chapter, the APIXFAB0 chip has been conceived as a platform to evaluate the properties of the XFAB xh018 CMOS technology. This was done in view of the possible design of a position sensitive detector, based on the SPAD coincidence principle. Since, to the best of our knowledge, the XFAB technology has never been used before to fabricate SPAD sensors, in this first run a single chip has been designed and submitted, with the main purpose of assessing the feasibility of SPADs with integrated electronics in the xh018 process.
In order to investigate the technology features, a test vehicle was designed and fabricated using the available high voltage (HV) option and leveraging the mini@sic prototyping concept made available by Europractice. The advantage of using a high voltage process is the possibility to obtain p-n structures with different layers combination and, therefore, the best solution can be chosen in order to get the best performance. The chip is organized as is shown in Fig. 2.1

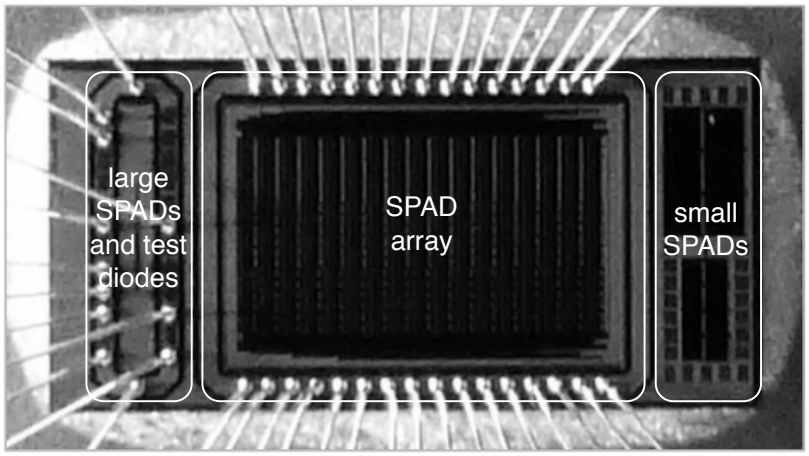


Figure 2.1: micro photograph of the APIXFAB0 test chip.

and, in particular, is subdivided as described in the following.

- Left side (large SPADs and test diodes): a set of test SPADs with pitch of 200 μm $\times$ 200 μm are implemented together with other test diodes. In addition, sensors with an active area of 100 μm $\times$ 100 μm are included. The devices can be contacted by means of dedicated probing pads.
- Right side (small SPADs): square SPADs with different dimensions (10 μm $\times$ 10 μm, 20 μm $\times$ 20 μm) with an integrated quenching resistor of 200 kOhm.
- Middle region (SPAD array): pixel array consisting of 17 rows and 18 columns in which each pixel includes both the detector and the front-end electronics.

The test vehicle takes a total area of 4.5 mm^2. This thesis work will present only the results relevant to the characterization of the structures included in the middle region. A thorough description of all of the APIXFAB0 structures will be provided in the next sections.

2.1.1 Test SPADs

SPADs of different types, using different combinations of the layers available in the XFAB technology, and with different size have been included in the test

chip. All the sensors not belonging to the SPAD array have been tested and characterized separately by people at the University of Trento, also part of the APiX collaboration, in order to extract the information needed for the test of the sensors included in the array which is one of the subjects of this thesis work.

2.1.1.1 SPAD types

Eight different SPAD types have been included in the test chip. Their reference name and active junction type are summarized in Table 2.1.

Number	Test SPAD type	Name
1	PDIFF/HVNWELL	dphnw
2	PDIFF/DNWELLMV	dpdnwellmv
3	PDIFF/ISOPWELL/DNWELLMV	dipdnwellmv
4	PDIFF/NWELL2	dp3
5	NDIFF/HVPWELL	dnhpw
6	NDIFF/PWELL2	dn3
7	NDIFF/(PWELL + HVNWELL)	dcomp
8	DNWELL/SUB	dnw

Table 2.1: test SPAD types.

2.1.1.2 SPAD size and common layers

Test SPADs with different areas were included in the chip. Test structures with an integrated 200 kOhm quenching resistance have an active area of 10 μm $\times$ 10 μm or 20 μm $\times$ 20 μm, with 45 degree corners to reduce the electric field at the edges. Test SPADs with 100 μm $\times$ 100 μm active area and no quenching resistance are also included.
The layers in Table 2.2 are used in all the SPAD test structures.

2.1.1.3 Layers and structure

The basic layers are listed in Tables from 2.3 to 2.10 for each SPAD, while a simplified cross section is shown in Fig. 2.2. Table 3.1 and Table 2.12 summarize the layers used in the different SPADs.

Layer name	Description	Purpose
SBLK	salicide block	SPAD active area (except contact)
CONT	contact	for most of the SPADs, contacts are at the periphery of the active area, only for dipdnwellmv contacts they are in the center
M1	metal 1	cathode and anode metallization
BLKALL	block all dummies	-
DIFF	no-STI	defines region without field oxide
PIMP	Np+ doping	-
NIMP	n+ doping	-

Table 2.2: common layers used in SPAD test structures.

Layer name	Description	SPAD region/purpose
PWBLK	pwell block	everywhere
DNWELLMV	medium-voltage deep nwell	everywhere
NWELL	nwell	peripheral deep nwell contact
HVPWELL	high-voltage pwell	guard ring
HVNWELL	high-voltage nwell	SPAD center doping enrichment

Table 2.3: SPAD dphnw: p+/hvnwell (same as dpdnwellmv, with additional HVNWELL).

Layer name	Description	SPAD region/purpose
PWBLK	pwell block	everywhere
DNWELLMV	medium-voltage deep nwell	everywhere
NWELL	nwell	peripheral deep nwell contact
HVPWELL	high-voltage pwell	guard ring

Table 2.4: SPAD dpdnwellmv: p+/dnwell.

Layer name	Description	SPAD region/purpose
PWBLK	pwell block	everywhere
DNWELLMV	medium-voltage deep nwell	everywhere
NWELL	nwell	peripheral deep nwell contact
ISOPW	isolated pwell	SPAD anode implant
POLY1	poly-Si gate	surrounds ISOPW (1 μm ring)

Table 2.5: SPAD dipdnwellmv: isopwell/dnwell.

Layer name	Description	SPAD region/purpose
PWBLK	pwell block	everywhere
DNWELLMV	medium-voltage deep nwell	everywhere
NWELL	nwell	peripheral deep nwell contact
MV	medium voltage	3.3V nwell
HVPWELL	high-voltage pwell	guard ring

Table 2.6: SPAD dp3: p+/mvnwell (same as dphnw, with medium voltage nwell enrichment).

Layer name	Description	SPAD region/purpose
PWBLK	pwell block	everywhere
HVPWELL	high-voltage pwell	SPAD enrichment doping

Table 2.7: SPAD dnhpw: n+/hvpwell.

Layer name	Description	SPAD region
PWBLK	pwell block	surrounds cathode
MV	medium voltage	3.3V nwell

Table 2.8: SPAD dn3: n+/mvpwell.

Layer name	Description	SPAD region/purpose
PWBLK	pwell block	everywhere
DNWELL	high voltage deep nwell	SPAD cathode
HVPWELL	high voltage pwell	SPAD anode (substrate) contact

Table 2.9: SPAD dnw: dnwell/sub.

Layer name	Description	SPAD region/purpose
PWBLK	pwell block	surrounds cathode
HVNWELL	high voltage nwell	used to compensate pwell enrichment

Table 2.10: SPAD dcomp: n+/pwell+hvnwell (enrichment region exploits compensation between standard pwell and HVNWELL).

Name	DNWELL--MV	PWBLK	HV--NWELL	NWELL
dphnw	x	x	x	x
dpdnwellmv	x	x	-	x
dipdnwellmv	x	x	-	x
dp3	x	x	-	x
dnhpw	-	x	-	-
dn3	-	x	-	-
dcomp	-	x	x	-
dnw	x	x	-	-

Table 2.11: layers used in SPAD structures: summary table 1.

Name	MV	PWELL	HV--PWELL	ISO--PWELL
dphnw	-	-	x	-
dpdnwellmv	-	-	x	-
dipdnwellmv	-	-	-	x
dp3	x	-	x	-
dnhpw	-	-	x	-
dn3	x	-	-	-
dcomp	-	-	-	-
dnw	-	-	x	-

Table 2.12: layers used in SPAD structures: summary table 2.

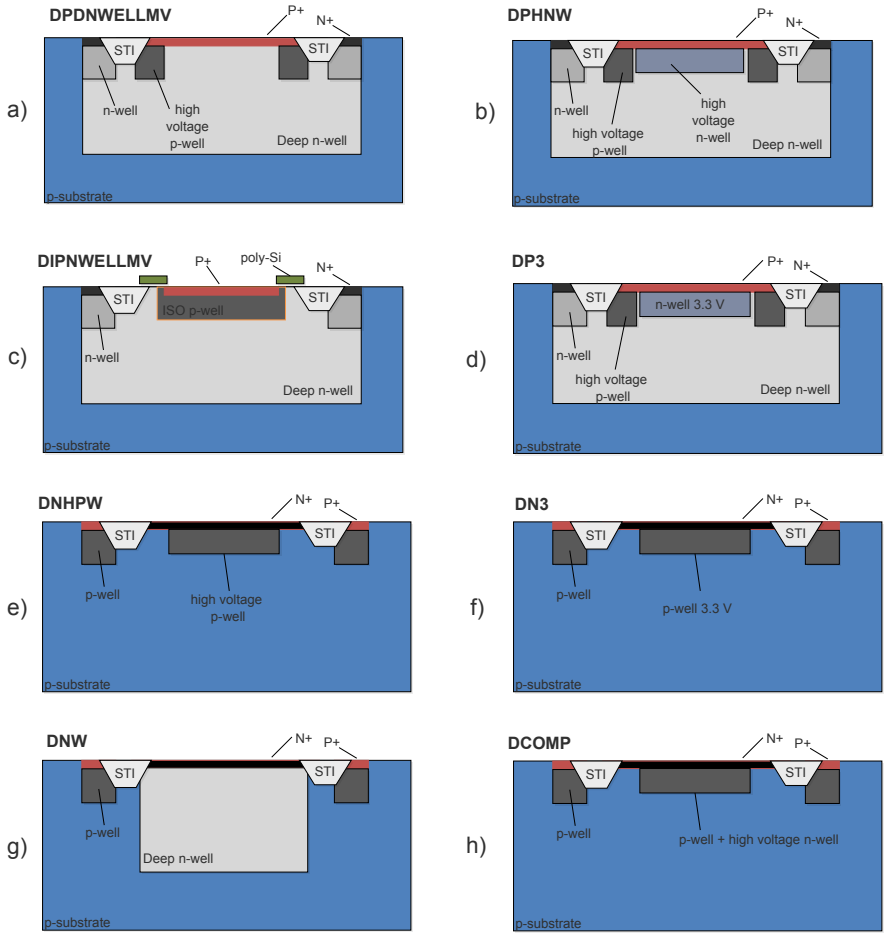


Figure 2.2: simplified cross-sections of the different SPAD types.

2.1.1.4 Test diodes

Test diodes were included to extract information on the different doping profiles through the measurement of CV curves and optical tests. The external size of the test diodes is 200 μm $\times$ 200 μm. The area exposed to light, defined by a metal shield, is 180 μm $\times$ 180 μm. The layers used in the test diodes are listed in Table 2.13.

Number	SPAD name	layers
1	ipdnwellmv	ISOPW,DNWELLMV
2	nhvpw	PWBLK, HVPWELL, DIFF, NIMP
3	npw2	MV, DIFF, NIMP
4	pdnwellmv	DNWELLMV, DIFF, PIMP
5	phvnw	PWBLK, HVNWELL, DIFF, PIMP
6	pnw2	NWELL, MV, DIFF, PIMP

Table 2.13: test diode layers.

2.1.2 SPAD array

The array includes avalanche pixels with three different sizes and three different technology layer combinations. The front-end electronics is monolithically integrated with the sensing element in the same pixel. Moreover, the three different topologies used for the readout channels (to be discussed later on in this chapter) are put together with the variety of single photon avalanche diodes in such a way that all the possible combinations are covered. In each array cell, which is 100 μm long and 50 μm wide, half of the area is dedicated to the sensor whereas the remaining part is used for the processing electronics. In Fig. 2.3, the organization of the array is shown. For a more flexible operation of the circuit, each pixel can be independently enabled or disabled by means of slow control signals. The selection of one or multiple pixels in the same row is performed by programming a shift register along each row. The choice of which row has to be programmed is implemented using 5 bits of an 8-bit shift register (Fig. 2.4). The same shift register includes three more bits to set the SPAD off time (two bits) in SPADs with active quenching readout and the output pulse width (one bit). More details will be provided later on in this chapter in the description of the individual cell operation (see 2.1.4). Once the row has been selected the pixel enable signal can be sent to the selected row together with the clock signal.

All the output signals coming from the pixels of an entire row are combined

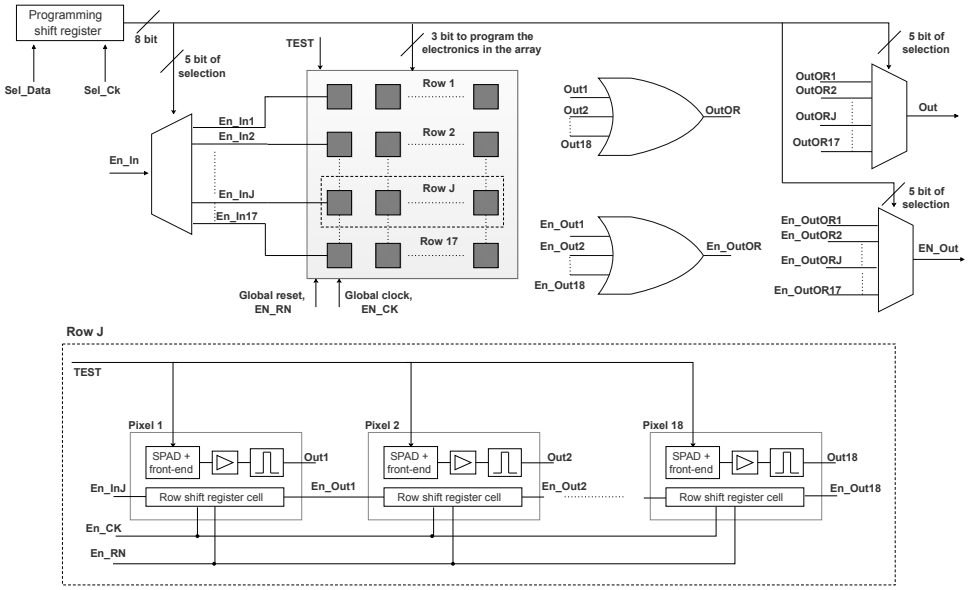


Figure 2.3: simplified internal structure of the pixel array in the APIXFAB0 chip.

with an OR gate. The OR combined signals (i.e, `Out_OR` and `EnOut_OR`), for each row, are processed through an output decoder which is controlled with the same five selection bits used for the input decoder. The `EnOut_OR` signal used to check if the row programming procedure was successful or not.
As mentioned at the beginning of this section, the array pixels were designed in such a way to cover all the possible combinations of the sensor types and readout architectures included in the chip. In particular, each row is made by 18 pixels subdivided as listed in the following:

- in pixel 1 to pixel 6, the active area of the sensor is 20 μm $\times$ 20 μm;
- in pixel 7 to pixel 12, the active area of the sensor is 30 μm $\times$ 30 μm;
- in pixel 13 to pixel 18, the active area of the sensor is 36 μm $\times$ 40 μm.

As far as the three different architectures of the front-end electronics are concerned, the array has been partitioned as follows:

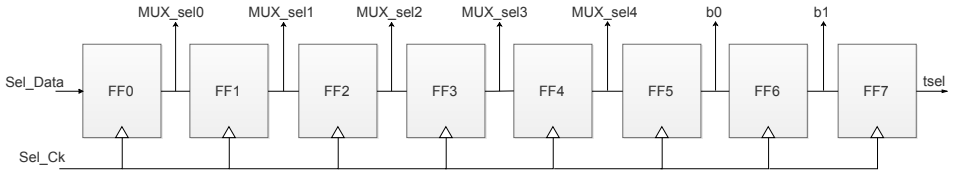


Figure 2.4: internal structure of the 8-bit programming shift register. The selection signals and the array electronics programming bits are also represented.

- column 1 to 5 are used for passive quenching readout;
- column 6 to 11 are used for active quenching readout with inverter based threshold crossing detection;
- column 12 to 17 are used for active quenching readout with comparator based threshold crossing detection.

The last partitioning is for the three kinds of single photon avalanche diodes included, called DPD, DPH and DIP (their cross-section is shown in Fig. 2.2 a), b) and c) respectively), which are based on the combination of different technology layers.
As far as the sensors of the DIP kind are concerned, their breakdown voltage was found to be quite higher, in excess of 25 V, than for the DPD and DPH sensors, as a consequence of the process layer chosen for their design. Indeed, due to such a high breakdown voltage, the minimum field at the junction needed to have an avalanche is expected to lead to excess DCR due to band-to-band tunneling [40]. This is the reason why DIP SPADs where excluded from the characterization campaign.

2.1.3 SPADs under test: DPD and DPH

The main difference between the two kinds of single photon avalanche diodes tested in this work (shown in Fig. 2.2), lies in the layers used to implement the active region of the detector. In the case of DPD sensors, the two sides of the p-n junction consists of a P^+ shallow diffusion and of the deep N-well where the P^+ diffusion is located. The second sensor structure is called DPH. As it can be noticed, the active region of the junction is obtained by using a high voltage N-well as the N-side of the junction, instead of the deep N-well.

Moreover, in both kinds of sensors, a high voltage P-well has been included as a guard-ring to avoid premature edge breakdown (PEB) effect along the perimeter of the P^+ diffusion.
Both the sensors have been implemented in the three different dimensions already mentioned in the previous section: 20 μm $\times$ 20 μm, 30 μm $\times$ 30 μm and 36 μm $\times$ 40 μm.

2.1.4 Front-end electronics

Each SPAD in the array is read out through a front-end circuit, providing a pulse with a fixed duration as a response to a signal from the sensor. In order to allow the circuitry to work properly, slow control signals are needed to configure the readout channels. The readout channels are based either on a passive or an active quenching approach. In both cases, the duration of the output pulse has a programmable duration, which can be set with a single bit in the programming shift register (see Fig. 2.3). Moreover, each cell is provided with a test terminal, enabling the test of the readout channel with an external signal.

2.1.4.1 Passive quenching readout

A passive quenching network, as explained in the previous chapter, can be implemented by using either a simple quenching resistor in series to the detector or with an N-MOS transistor. The last solution is the one implemented in the APIXFAB0 chip. Fig. 2.5 shows the block diagram of the circuit implemented in the array. After the SPAD fires, its anode is discharged through a constant current source with adjustable gate voltage V_b. Note that, if the cell is enabled, transistor M_{en} acts as a closed switch. The same ENABLE signal controlling the state of M_{en}, also controls the monostable block at the end of the channel. Signal detection is performed by using a comparator with adjustable threshold voltage V_{th}. A clamping transistor, with tunable gate voltage V_{clamp}, is used to adapt the level of the signal coming from the sensor to the comparator input. The clamping operation is mandatory because all the transistors used in the readout channel are core devices with $V_{DD} = 1.8$ V. The only exceptions are for the current source performing the quenching operation, the enable transistor and the clamping device, which are thick oxide transistors ($V_{DD} = 3.3$ V). To prevent damages in the devices with thick oxide, the excess bias at which the SPAD is biased should not exceed the voltage of 3.3 V (actually, a voltage 10% in excess of 3.3 V is allowed with no significant risk of failure for the circuit). The output signal of the pixel is provided by means of a monostable

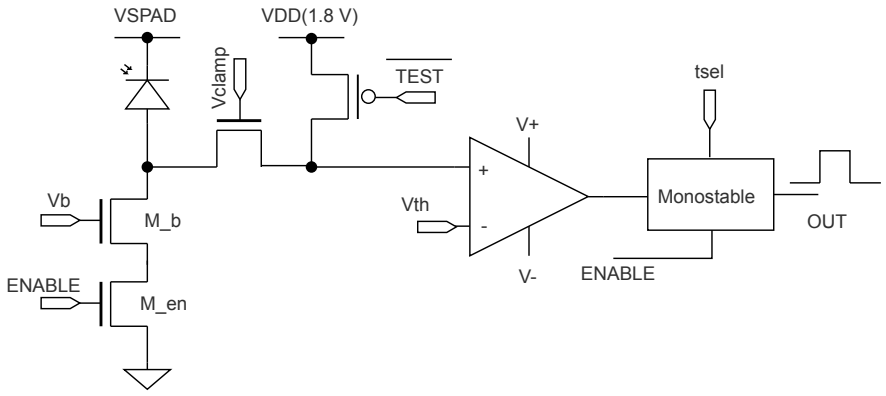


Figure 2.5: block diagram, with some transistor level detail, of the front-end circuit with passive quenching.

circuit. In particular, the monostable circuit has been designed in such a way that the duration of the output signal can be set to 2 ns or 8 ns through the t_{sel} control bit. Moreover, by switching off the relevant SPAD (this is done simply by keeping the voltage at its cathode below the breakdown voltage), proper operation of each readout channel can be evaluated by using an external test signal (`TEST`, active low), whose purpose is to emulate the signal coming from the SPAD by pulling up the non inverting input of the comparator.

2.1.4.2 Active quenching, inverter based readout

As in the passive quenching front-end channel, also in the case of the active quenching based channels the output signal consists of a pulse with programmable duration. The block diagram of the circuit is shown in Fig. 2.6. As compared to the passive quenching case, here the threshold crossing is detected through a custom designed inverter with a transition threshold smaller than $V_{DD}/2$ (about 1 V). The main feature of the active quenching technique lies in the possibility to keep the SPAD in a off state for an adjustable time interval. This feature in the APIXFAB0 chip is implemented by programming the width of the signal at the output of a monostable circuit, adding to the

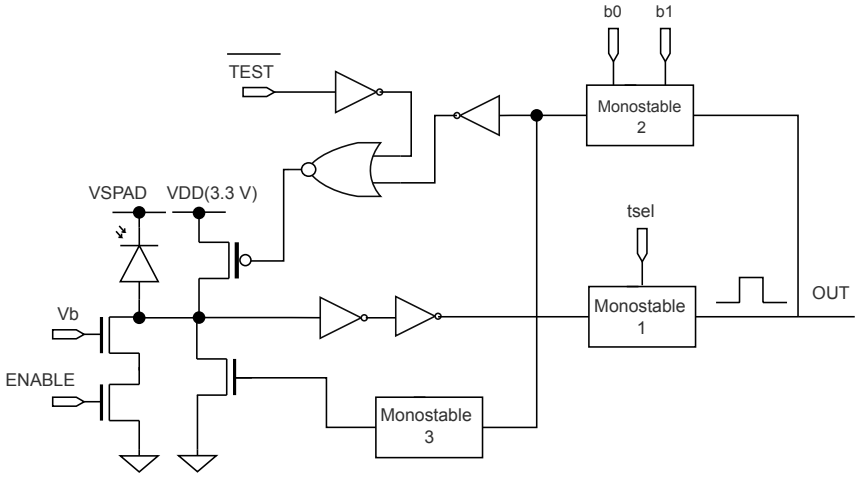


Figure 2.6: block diagram, with some transistor level detail, of the front-end circuit with active quenching. Threshold crossing is detected through an inverter with modified transition threshold.

one used for the output signal. The monostable circuit is programmed through the control bits b_0 and b_1 (see Fig. 2.6). In particular, the SPAD-off time can be set to 20 ns, 30 ns, 40 ns or 50 ns. The monostable 2 controls the gate of a P-MOS transistor which, when switched on, brings the anode terminal of the detector to $V_{DD} = 3.3$ V, lowering the voltage across the SPAD below breakdown and preventing any avalanche phenomena from occurring. Once the off-time is over, the initial conditions of the detector have to be restored as fast as possible to bring it back to operation. For this purpose, an N-MOS transistor performing a quick discharge of the SPAD anode is included in the network. In particular, the pull-down N-MOS transistor is switched on for a fixed time interval, set by monostable 3 circuit, as soon as the off-time is over. While in the passive quenching based circuit the part of the readout channel located after the clamping transistor is based on core devices, in the case of the active quenching based circuit all the devices are taken from the thick oxide library. For this reason, the clamping transistor present in the passive quench-

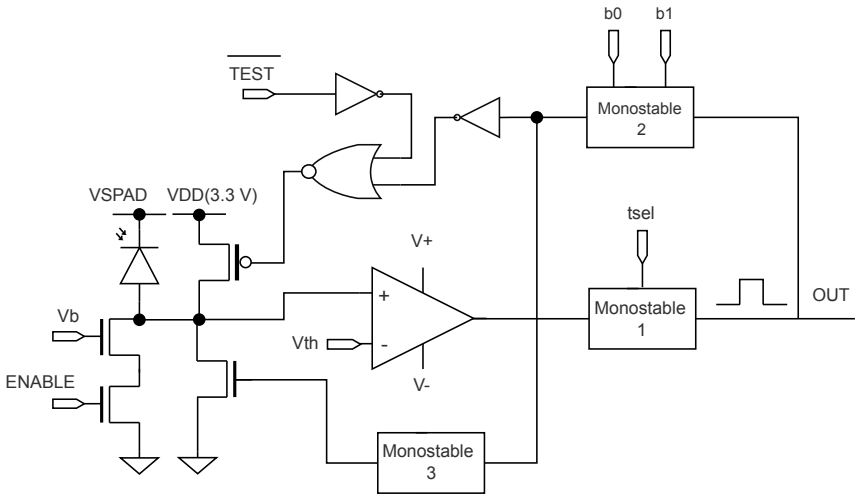


Figure 2.7: block diagram, with some transistor level detail, of the front-end circuit with active quenching. Threshold crossing is detected through a comparator with adjustable threshold.

ing circuit to adapt the signal coming from the sensor is no more needed in the circuit of Fig. 2.6. Moreover, the output signal of the channels adopting the active quenching method goes from 0 V to 3.3 V. Therefore, in order to make the pixel output signal (0 to 3.3 V) compatible with the output circuits at the chip periphery, which are based on 1.8 V CMOS logic levels, down-shifting blocks are needed. Finally, in the active quenching based front-end, the correct operation of the electronics can be evaluated by using an external test signal, as in the case of the passive quenching configuration.

2.1.4.3 Active quenching, comparator based readout

This circuit, which is shown in Fig. 2.7, is very similar to the previous one. The only difference consists of using a comparator with adjustable threshold V_{th} to detect threshold crossing instead of an asymmetric inverter.

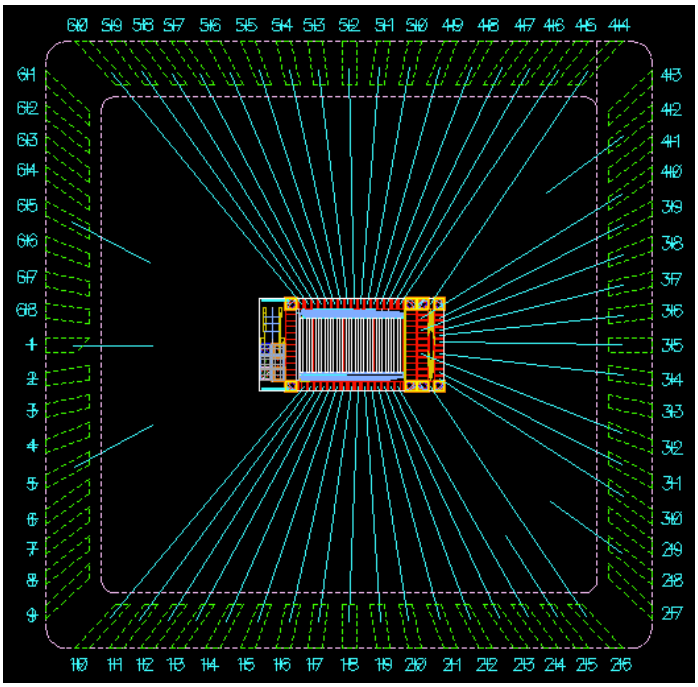


Figure 2.8: bonding diagram of the APIXFAB0 chip in a JLCC68 package.

2.1.5 Bonding diagram and pin description

For the test phase, the chip was packaged in a standard JLCC68 package with removable taped lids. The bonding diagram for the chip is shown in Fig. 2.8. The complete pin description and pin list is provided in Table 2.14.

Table 2.14: pin list.

Pad no.	Name	Function	Comment
1	SUB	substrate	backside contact (GND)
5	SUB	substrate	backside contact (GND)
10	SEL_DATA	dig. in.	slow control data
11	SEL_CK	dig. in.	slow control clock
12	VSPADC3	SPAD bias	external bias source (cols. 4, 5, 10, 11, 16, 17)
13	IOVDD33	power	3.3 V for I/O circuit
14	IOGND(33)	power	GND for I/O circuits
15	COREVDD33	power	3.3 V for circuits in the array

Table 2.14

Pad no.	Name	Function	Comment
16	COREGND(33)	power	GND for circuits in the array
17	OR_OUT	dig. out.	end of column signal
18	COREVDD18	power	1.8 V for circuits in the array
19	COREGND(18)	power	GND for circuits in the array (shorted to COREGND(33))
20	IOVDD(18)	power	1.8 V for I/O circuits
21	IOGND(18)	power	GND for I/O circuits (shorted to IOGND(33))
22	EN_OUT	dig. out.	enable output
23	VSPADC1	SPAD bias	external bias source (cols. 1, 6, 7, 12, 13)
24	VSPADC2	SPAD bias	external bias source (cols. 2, 3, 8, 9, 14, 15)
25	SUB	substrate	backside contact (GND)
26	SPAD_SUB	substrate	substrate contact for small SPADs
28	SUB	substrate	backside contact (GND)
30	DNHPW_OUT10x10	SPAD out.	10 um x 10 um DNHPW SPAD output (N side)
31	DCOMP_OUT10x10	SPAD out.	10 um x 10 um DCOMP SPAD output (N side)
32	DPDNWELLMV_CATHODE10x10	SPAD bias	10 um x 10 um DPDNWELLMV SPAD cathode (N side)
34	DPDNWELLMV_OUT10x10	SPAD out	10 um x 10 um DPDNWELLMV SPAD output (P side)
35	DNHPW_OUT20x20	SPAD out.	20 um x 20 um DNHPW SPAD output (N side)
36	DCOMP_OUT20x20	SPAD out.	20 um x 20 um DCOMP SPAD output (N side)
37	DP3_OUT	SPAD out.	SP3 SPAD output (P side)
38	DP3_CATHODE	SPAD bias	DP3 SPAD cathode (N side)
39	DPDNWELLMV_OUT20x20	SPAD out	20 um x 20 um DPDNWELLMV SPAD output (P side)
40	DPDNWELLMV_CATHODE20x20	SPAD bias	20 um x 20 um DPDNWELLMV SPAD cathode (N side)
42	SUB	substrate	backside contact (GND)
44	SPAD_SUB	substrate	substrate contact for small SPADs
45	COREGND(33)	power	GND for circuits in the array
46	COREVDD33	power	3.3 V for circuits in the array
47	VCLAMP	voltage ref.	translator clamp voltage, 1.5 V

Table 2.14

Pad no.	Name	Function	Comment
48	VBN1	voltage ref.	quenching transistor reference (passive q., 900 mV)
49	VBN2	voltage ref.	quenching transistor reference (active q., 600 mV)
50	VREF	voltage ref.	comparator threshold voltage
51	EN_IN	dig. in.	enable input
52	EN_RN	dig. in.	enable reset (active low)
53	IOGND(18)	power	GND for I/O circuits
54	IOVDD(18)	power	1.8 V for I/O circuits
55	IOGND(33)	power	GND for I/O circuits
56	IOVDD33	power	3.3 V for I/O circuit
57	EN_CK	dig. in.	enable clock
58	COREGND(18)	power	GND for circuits in the array
59	COREVDD18	power	1.8 V for circuits in the array
60	TESTN	dig. in.	test signal (active low)
65	SUB	substrate	backside contact (GND)

2.2 Measurement system

For a complete characterization of the APIXFAB0 chip, a custom measurement system had to be designed and implemented. For this purpose, a fully automated, microcontroller based measurement setup has been developed. The organization of the system is shown in Fig. 2.9. The whole setup is controlled by a program developed in the *Matlab* environment. Through a bluetooth connection, the *Matlab* program can control a microcontroller directly wired to the test board hosting the carrier board with the chip under test. The same *Matlab* program is used to set the bias voltage at the detector cathode by means of a power supply connected to the PC through a GPIO communication bus. This setup is used in particular for measuring the dark count rate as a function of the voltage applied to the SPAD. Once the cathode bias voltage is set, the program sends the starting command to the microcontroller and the measurement can be performed.
The microcontroller used in the system is the STM32F051 model by *STMicroelectronics*. It is responsible for the configuration of the chip and for providing the initialization signal with the proper timing. Moreover, the program is able to select each cell in the array recognizing which combination of SPAD and readout channel is implemented by means of a look-up table. This is important because the characterization is performed on the entire ar-

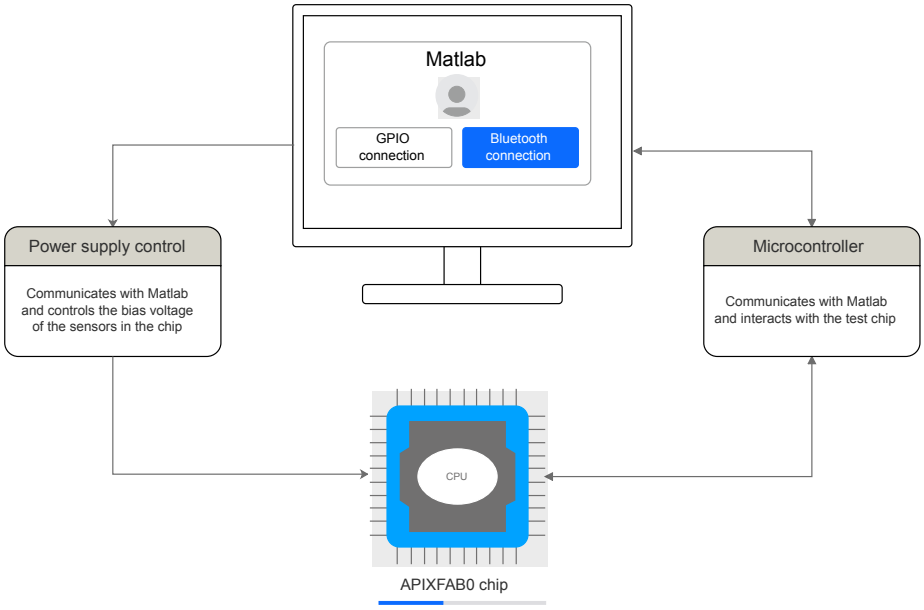


Figure 2.9: basic operation of the fully automated measurement system implemented for the characterization of the test chips.

ray, and recognizing the cell involved in the measurement can simplify data analysis and reconstruction. Furthermore, before starting with the characterization of a test vehicle, the program is able to perform a fast test of the readout electronics by taking advantage of the `TEST` signal feature. Data collected during the chip characterization are sent by the microcontroller to the *Matlab* environment through a bluetooth connection, as mentioned before. In particular, data are sent at the end of the characterization of each individual pixel. At this point, the microcontroller communicates to the *Matblab* program that the characterization of the next pixel can start.
Summarizing, the *Matlab* program sets the voltage at the cathode of the SPAD, uses the microcontroller to select the pixel to characterize, to set the SPAD-off time in the active quenching based pixels, to set the width of the pulse at the output of the cells and to perform the measurement. The measurement procedure, in particular for DCR, is described in more details later on in this chapter.

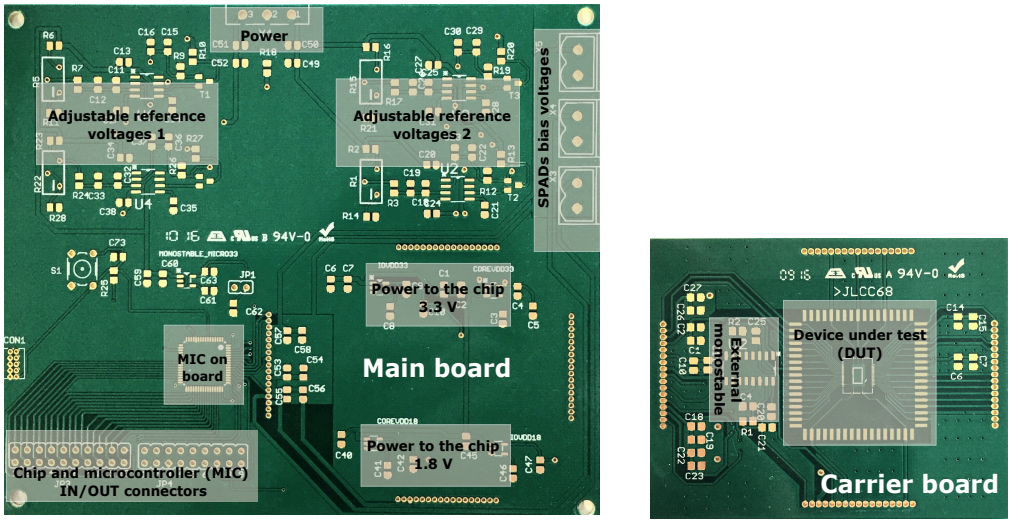


Figure 2.10: main and carrier boards for the APIXFAB0 chip measurement setup.

2.2.1 Main and carrier boards

Before starting with the measurements on different test vehicles, a printed circuit board (PCB) to bias the device under test (DUT) and to connect the chip to the measurement system has been developed. In particular, two different PCBs were designed using the *Eagle* design environment and then fabricated, as shown in Fig. 2.10.
The system is required to acquire the digital output of the chip, enable and disable all the cells in the array independently, set SPAD-off time and output pulse width for the entire array and bias each type of sensor with an adjustable voltage.
Due to the complexity of the design, a 4-layer has been chosen for the main PCB. The main board is used to generate all the reference voltages and the power supplies which are needed for the device under test. The integrated circuits (ICs) mounted on the main board require a bipolar bias voltage of ± 5 V. As mentioned during the description of the readout channels implemented in the chip, different tunable reference voltages, such as the gate voltage of the clamping transistor (V_{clamp}), the gate voltages of the quenching transistor (V_Q)

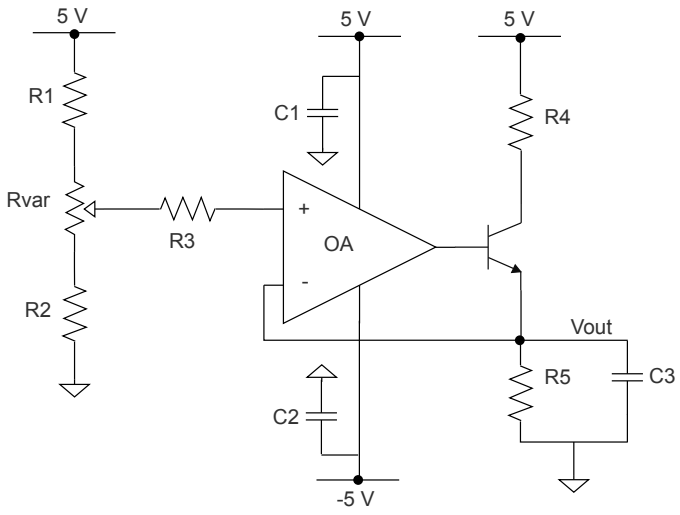


Figure 2.11: simplified block diagram of the voltage reference circuit implemented on the main board for adjustable bias references.

for the passive and active quenching readout circuits and the threshold voltage for the comparator, have to be provided with the required stability. For this reason, these four tunable reference voltages have been implemented using the scheme shown in Fig. 2.11. The output voltage V_{out} is generated by setting the voltage at the non-inverting input of the operational amplifier (OA) through the variable resistance R_{var}. The same voltage is found at the emitter terminal of the n-p-n bipolar transistor, which has its base terminal connected to the output of the operational amplifier. In this situation, the base of the bipolar transistor will assume whatever voltage is needed to make the BJT's emitter voltage equal to the input voltage applied to the non-inverting terminal.
The bias voltage for the I/O devices and the core electronics is provided by using different voltage regulators receiving as input the 5 V coming from the main power supply and providing as output the regulated voltage. In particular, the four different voltage regulators mounted on the board are listed in the following:

- one $TPS73633DBVTG4$, used to generate the 3.3 V for the I/O circuits of the chip, located under the pads;

- one $TPS73633DBVTG4$, used to generate the 3.3 V for the devices inside the chip, such as the front-end implemented in the active quenching based channels and the quenching and clamping transistors;

- one $TPS76918$, used to generate the 1.8 V for the core electronics, such as the front-end circuits implemented in the passive quenching based channels;

- one $TPS76918$ used to generate the 1.8 V for the I/O electronics under the pads in the chip periphery, such as the circuits used for down-shifting the output signal of the active quenching pixels from 3.3 V to 1.8 V.

For a more compact and portable measurement system, the microcontroller can be directly mounted on board.
The design of the carrier board (a 2-layer PCB) was carried on in such a way that the test vehicle can be accommodated on the board both as a packaged chip and as a naked die. Several capacitances are mounted on the board for power supply and reference voltage stabilization.
A critical point in the design of the carrier board was how to ensure the correct detection of the chip output signal by the microcontroller. Indeed, as mentioned previously, the time duration of the chip output signal can be set to 2 or 8 ns by programming a monostable circuit in the pixel. The microcontroller would actually be unable to detect such a fast signal. For this reason, an additional, external monostable circuit has been mounted on the carrier board in order to overcome this problem. In particular, the *Dual Retriggerable Monostable Multivibrator* $74VHC123A$ by *Fairchild* has been chosen and configured in such a way it can deliver an output signal with a duration of 300 ns, which can be easily detected by the microcontroller. The main constraint in using this external monostable IC is the minimum input signal duration, which is 5 ns. For this reason, in order to guarantee the correct operation of the system, the duration of the chip output pulse was set to 8 ns, as the other possible option, 2 ns, did not comply with the specifications of the external monostable circuit.

2.3 DUT test program for DCR evaluation

In this section a more detailed description of the program implemented for the chip characterization, and in particular for DCR measurements, is discussed in order to better understand how the results showed in the next chapter were obtained.

The microcontroller which communicates with the test chips is programmed in C language. The software used for the design of the entire C program is *Atollic TrueSTUDIO*, which is specifically adopted for the $STM32$ microcontrollers family. The flow-chart of the measurement program is shown in Fig. 2.12.

Pin configuration. Primarily, the pin configuration of the microcontroller has to be performed in order to correctly communicate with the chip under test. In particular, the pins can be configured as general purpose input/output pins or as input/output pins of peripheral structures integrated in the microcontroller. Once pin configuration is finished, the DUT can be programmed. The following lines represent a portion of the implemented code.

```
void SystemClock_Config(void);
static void MX_GPIO_Init(void);
static void MX_TIM2_Init(void);
static void MX_TIM15_Init(void);
static void MX_USART1_UART(void);
```

Each lines is referred to the initialization function implemented for each of the peripheries used (general purpose I/O pins, timer 2, timer 15 and UART module).

Chip initialization. The first part of the program provides a global reset signal `(EN_Res)` needed to disable all the cells, and configure the slow control bits to program the electronics in the different front-end channels, therefore setting the output pulse duration `(t_sel)` and the off-time for the SPAD in the cells with active quenching based readout channel `(b0, b1)`. It is worth noticing that the initialization phase of the test vehicle is mandatory to ensure its correct operation.

The following lines represent a portion of the initialization code used to reset the device and to configure the input signal.

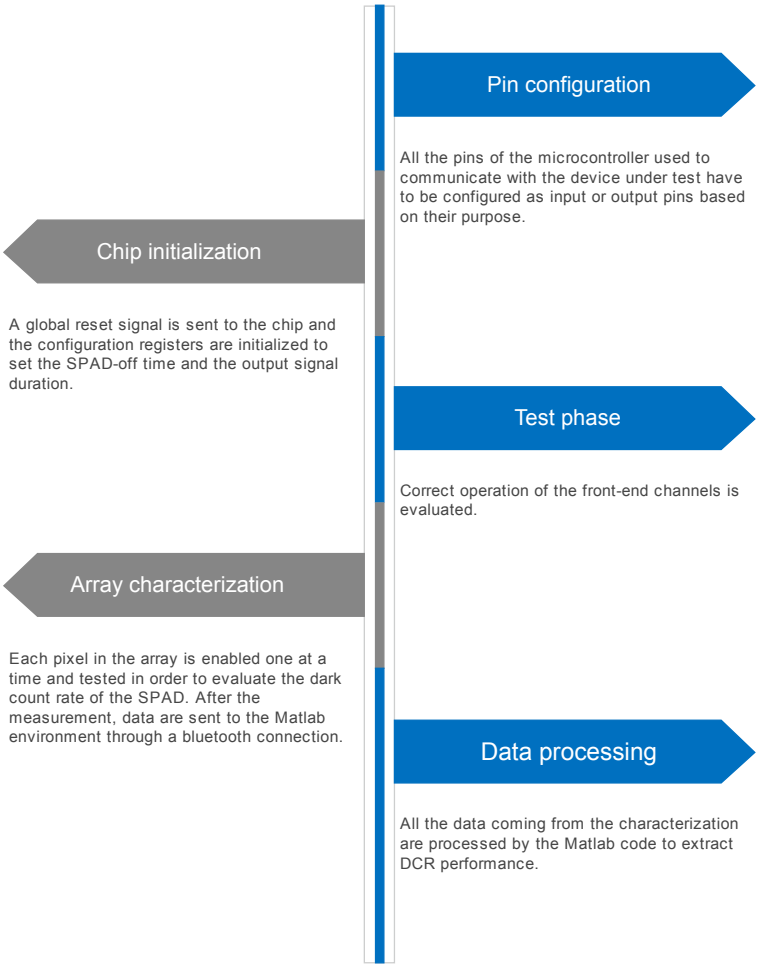


Figure 2.12: flow-chart of the measurement program used to test the APIX-FAB0 chip.

```
.
.
.
HAL_GPIO_WritePin(GPIOB, GPIO_PIN7, 1); //EN_Res
HAL_GPIO_WritePin(GPIOB, GPIO_PIN7, 0);
HAL_GPIO_WritePin(GPIOB, GPIO_PIN7, 1);
HAL_GPIO_WritePin(GPIOB, GPIO_PIN9, 1); //TEST
HAL_GPIO_WritePin(GPIOB, GPIO_PIN8, 0); //ENCK
HAL_GPIO_WritePin(GPIOB, GPIO_PIN6, 0); //EN_IN
HAL_GPIO_WritePin(GPIOB, GPIO_PIN4, 0); //SEL_DATA
HAL_GPIO_WritePin(GPIOD, GPIO_PIN2, 0); //SEL_CK
.
.
.
```

The code just reported initializes all the signals used as input to the chip and provides the reset signal needed to the chip. Depending on the signal, the pins are configured as zero logical value or as one logical value.
The following part of the code is used to configure the readout electronics in the pixels. Configuration is performed each time a new pixel is enabled.

```
.
.
.
void Pixel_Sel(int n_row, int n_col);
void configure_pixel(int t_sel, int b0, intb1);
.
.
.
```

Test phase. Before starting with the characterization, the DUT is subjected to a test phase during which the functionality of the readout electronics is evaluated. The test of the array proceeds by selecting one pixel at a time and enabling it. The selection of a row is implemented by means of the row selection bits, through which it is possible to address all the 17 rows. In particular, for a correct configuration of the shift register, the input data signal `(Sel_Data)` has to be provided together with the clock signal `(Sel_Ck)`. In this way, all the pixels in the array can be selected and, for each one of them, the test signal `(TEST)` is provided in order to evaluate if the readout circuit in that specific pixel works correctly. The result of the test is then sent to the *Matlab* environment for post processing.
If all is found to work correctly, the characterization of the array can start.
In the following a simplified version of the code performing the test of the readout electronics for two pixels in a sequence is shown.

```
.
.
.
Pixel_Sel(i, j); //i-th row and j-th column
configure_pixel (1,1,1);
test();
HAL_UART_Transmit(&huart1, data, length_data);
j++;
Pixel_Sel(i, j+1); //i-th row and j-th+1 column
configure_pixel (1,1,1);
test();
HAL_UART_Transmit(&huart1, data, length_data);
.
.
.
```

Array characterization. All the different versions of the array cells, with their combinations of active area size, readout architecture and SPAD type, are characterized.
The most critical point in the program design is to ensure correct detection

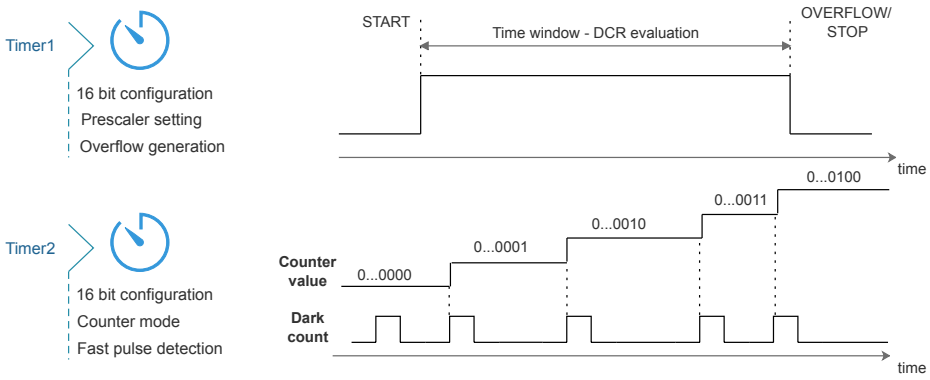


Figure 2.13: DCR evaluation using timer1 and timer2.

and counting of the dark pulses. The procedure is illustrated in Fig. 2.13. The challenge is to detect, without missing any pulse, the 300 ns long signal coming from the external monostable to the microcontroller. For this purpose, an internal *timer* of the microcontroller is used as a counter and properly set for fast signal detection. The counter is used in it 16-bit configuration for a sufficiently high counting capability.
A second internal *timer* is used to generate a time window during which the dark pulses of a SPAD are counted. This latter timer has been configured adopting a different approach. After its launch, the timer starts to counting according to a precise frequency given by the internal clock of the microcontroller. As soon as the content of the timer reaches the maximum value, an overflow signal is internally generated and the counting operation is stopped. It is worth noticing that, if the content of the timer were incremented at the internal clock frequency of the microcontroller, it would reach the maximum value very quickly, at a speed that would make it almost useless for DCR measurements. In order to be compliant with the application requirements, the *prescaler* feature of the microcontroller is used to reduce the effective counting frequency. In particular, the clock frequency is divided by a finite quantity defined in the *prescaler* registers and the resulting frequency is then used for the content increment in the second timer. In this way, a sufficiently wide time window is created for DCR evaluation.
In the following, a simplified version of the code implementing the configura-

tion of the two *timers*, the DCR calculation and, finally, the data transmission is shown.

```
.
.
.
htim1.Instance = TIM1; //TIMER1
htim1.Init.Prescaler = 0;
htim1.Init.CounterMode = TIM_COUNTERMODE_UP;
htim1.Init.Period = 65535;
htim1.Init.ClockDivision = TIM_CLOCKDIVISION_DIV1;
HAL_TIM_Base_Init(&htim1);
//External trigger
sSlaveConfig.SlaveMode = TIM_SLAVEMODE_EXTERNAL1;
sSlaveConfig.TriggerPolarity = TIM_TRIGGERPOL_RISING;
.
.
.
htim2.Instance = TIM2; //TIMER2
htim2.Init.Prescaler = 20;
htim2.Init.CounterMode = TIM_COUNTERMODE_UP;
htim2.Init.Period = 65535;
htim2.Init.ClockDivision = TIM_CLOCKDIVISION_DIV1;
htim2.Init.RepetitionCounter = 0;
HAL_TIM_Base_Init(&htim2);
.
.
.
```

```
.
.
.
//DCR evaluation
HAL_TIM_Base_Start_IT(&htim2);
HAL_TIM_Base_Start(&htim1);
__HAL_TIM_CLEAR_FLAG(&htim2,TIM_FLAG_UPDATE);
DCR = __HAL_TIM_GetCounter(&htim1);
.
.
.
//Data transmission
sprintf(data, "%d %d %d %d", row, col, ro_channel, DCR);
length_data = strlen (data);
HAL_UART_Transmit(&huart1, data, length_data);
.
.
.
```

Data processing. Finally, as mentioned in the previous section, the data are sent to the PC on which the *Matlab* code is running for further processing, and in particular to be stored on the hard drive .

2.4 Chapter related work

- M. Musacci, L. Lodola, "Single Photon Avalanche pixel for a dual-layer particle detector ", GE Conference, June 2016, Brescia, Italy.
- M. Musacci, P. Brogi, G. Collazuol, G.-F. Dalla Betta, A. Ficorella, et al., "Geiger-Mode Avalanche Pixels in a 180 nm HV CMOS Process for a Dual-Layer Particle Detector ", NSS/MIC Conference in Strasbourg, from 29 October to 6 November 2016, France.

Chapter 3

APIXFAB0 characterization results

In this chapter the results from the characterization of the APIXFAB0 test chip are presented. The results are relevant to the evaluation of the dark count rate (DCR) for the two kinds of sensors presented in the previous chapter, together with their breakdown voltage distribution. The measurements were repeated on different samples. Different sets of chips were also subjected to irradiation in two distinct campaigns involving ionizing and non-ionizing radiation sources in order to assess the radiation tolerance features of the SPAD sensors. The characterization of the irradiated chips was again particularly focused on studying radiation induced changes in the breakdown voltage and DCR. Finally, temperature tests were performed both on non irradiated and irradiated samples.

3.1 Pre-irradiation tests

In this section the results from the characterization of non irradiated (or not yet irradiated) chips will be presented. The tests were performed on four different DUTs, by evaluating the dark count rate and the breakdown voltage distribution for the two types of SPADs considered in this work.

3.1.1 DCR measurements

The non irradiated arrays were completely characterized in terms of dark count rate. Four chips were tested in order to collect a statistically meaningful set of data. The DCR characterization of the tested SPADs has been carried out

by optically shielding the chips and keeping them in "dark" conditions.

3.1.1.1 DCR vs active area

First of all, the dependence of the DCR as a function of the active SPAD area was determined for the two kinds of sensors. Fig.3.1 shows the behaviour of the dark count rate as a function of the sensitive area. In particular, data in the plot have been obtained by averaging the DCR of sensors with the same active region size at an excess bias voltage of 1 V. The readout channel is based on the passive quenching technique for both the DPD and DPH sensors in the figure, with the threshold voltage of the comparator externally set to 1 V. The DCR is observed to get larger with increasing active area, as expected, although the change is not linear. This may be ascribed to the large fluctuation in the number of DCR related defects in the device active volume, especially for SPADs of small size. The larger DCR featured by the DPH sensors as compared to DPD ones is likely due to the device structure and the

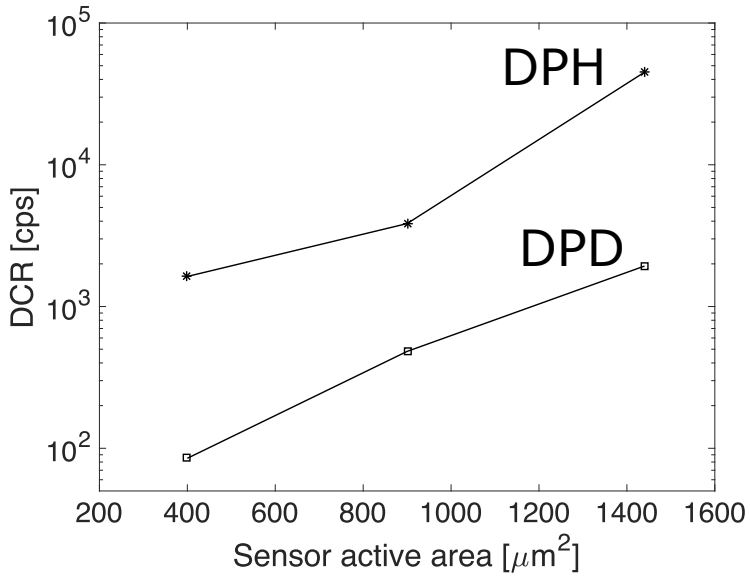


Figure 3.1: mean DCR of DPD and DPH sensors as a function of the active area for chip 4. The two curves are relevant to SPADs with passive quenching front-end electronics.

chosen process layers. Indeed, differently from SPADs of the DPD kind, the p-n junction of DPH sensors is obtained through the additional implant of a so called high voltage N-well (see Chapter 2, section 2.1.1), which may be responsible for the creation of defects in the silicon lattice acting as generation centers and contributing to DCR and after pulsing effects.
A similar behaviour of the dark count rate as a function of the active area was observed also in the SPADs with front-end channel based on the active quenching solution (see Fig.3.3). The measurements on SPADs with active quenching based readout channels were performed with a SPAD-off time of 20 ns (the shortest SPAD-off time selectable). Measurements were performed also at the longest available SPAD-off time, 50 ns. In this configuration, only for the SPADs with 20 μm $\times$ 20 μm and 30 μm $\times$ 30 μm active area, combined with the active quenching, comparator based readout channel, a significant difference was found as compared to the case of 20 ns SPAD-off time. This may indicate that the relative contribution of after pulsing to DCR becomes negligible in SPADs with large area. An example of such a measurement is provided by Fig. 3.2, showing the DCR for DPD sensors with active quenching, comparator based readout channel operated at two different SPAD-off times. The dashed lines join the mean values of the DCR.
Fig. 3.3a shows the DCR as a function of the sensor active area combined with the active quenching, comparator based readout channel, in which the threshold voltage of the comparator is set to 1 V as in the case of Fig.3.1. For a given active area, the DCR is slightly higher compared to the one obtained with the passive quenching readout. The reason for this has to be ascribed to the difference in the two readout architectures. Very likely, the dead time for the SPAD with passive quenching (which cannot be directly measured) is longer than that for the case of the active quenching configuration readout. This may be responsible both for a larger DCR and for a more significant after pulsing contribution.
Fig. 3.3b shows the DCR in pixels adopting the active quenching, inverter based readout as a function of the SPAD active area. Here, the DCR was found to be higher than both passive quenching and active quenching, comparator based configurations. The higher sensitivity to noise of the two-inverter chain used to detect threshold crossing, as compared to the comparator solution, may be responsible for the worse performance. The lower sensitivity of the comparator circuit may be related to its smaller bandwidth, which makes it less efficient in detecting small over-threshold signals.

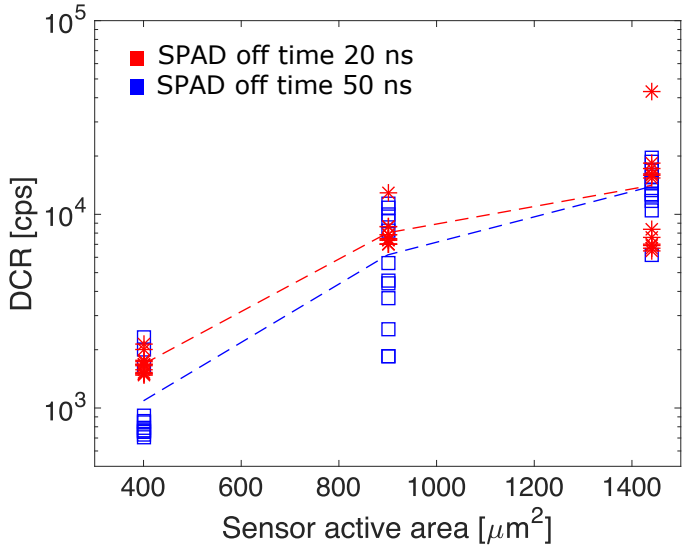
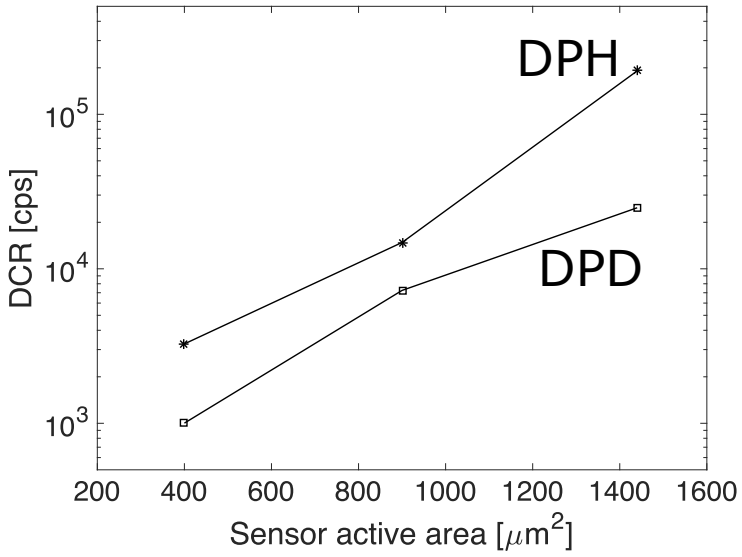


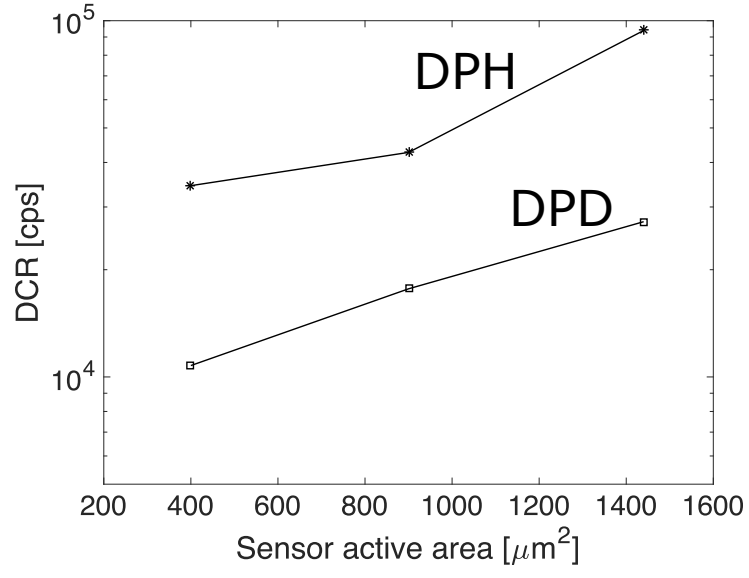
Figure 3.2: DCR as a function of the active area for two different SPAD-off times (20 ns and 50 ns). The measurements were performed on pixels adopting the active quenching, comparator based readout with DPD sensors biased at 1 V of excess bias.

3.1.1.2 DCR vs bias voltage

The dependence of DCR on the excess bias is of paramount importance to define the device performance. Breakdown voltage can also be extracted from this kind of measurements.
DCR was measured as a function of the excess bias voltage in both he DPD and DPH sensors, combined with all the available solutions for the front-end electronics. DCR was found to change more or less linearly with the excess voltage, at least in the explored voltage range.
The results from the characterization confirm the higher dark count rate of the DPH sensors as compared to the DPD ones in the entire voltage range in which the tests were performed. Moreover, for a given sensitive area, the detectors used together with the active quenching, inverter based electronics were again found to exhibit the highest DCR, higher than the SPADs based on the other two readout solutions, whatever the applied voltage was. Figures from 3.4 to 3.12 show the DCR, averaged over each of the four tested chips, of DPD and DPH sensors as a function of the excess bias. In each plot, SPADs with the



(a)



(b)

Figure 3.3: mean DCR of DPD and DPH sensors as a function of the active area for one of the four chips. Plot (a) is referred to SPADs with active quenching, comparator based readout electronics, whereas plot (b) is relevant to SPADs combined with the active quenching, inverter based readout channel.

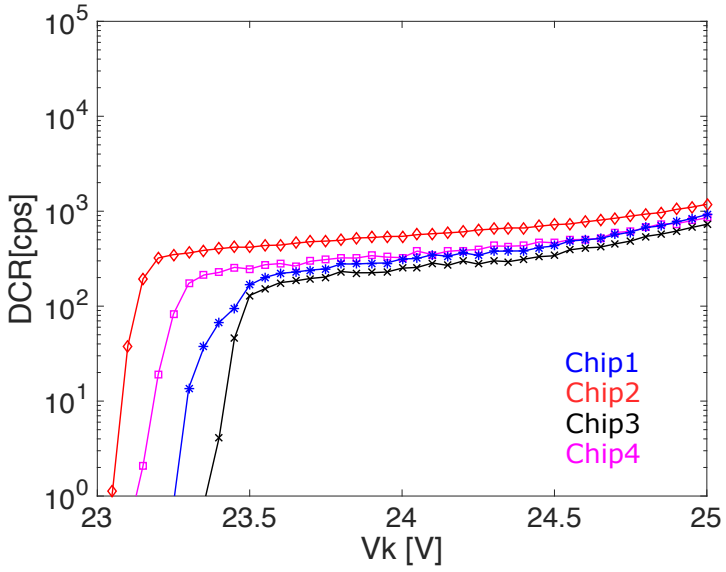
Sensor kind	Quenching topology	DCR [Hz] @ V_{ex} = 1.5 V		
		20 μm × 20 μm SPADs	30 μm × 30 μm SPADs	36 μm × 40 μm SPADs
DPD	passive	0.24×10^3	1.01×10^3	2.1×10^3
	active c.	3.6×10^3	1.14×10^4	1.88×10^4
	active i.	1.82×10^4	2.31×10^4	4.67×10^4
DPH	passive	3.1×10^3	2.01×10^4	6.5×10^4
	active c.	2.61×10^4	5.05×10^4	9.55×10^4
	active i.	6.51×10^4	7.27×10^4	2.57×10^5

Table 3.1: mean DCR, calculated by averaging over the four tested chips, at an excess bias voltage V_{ex} = 1.5 V.

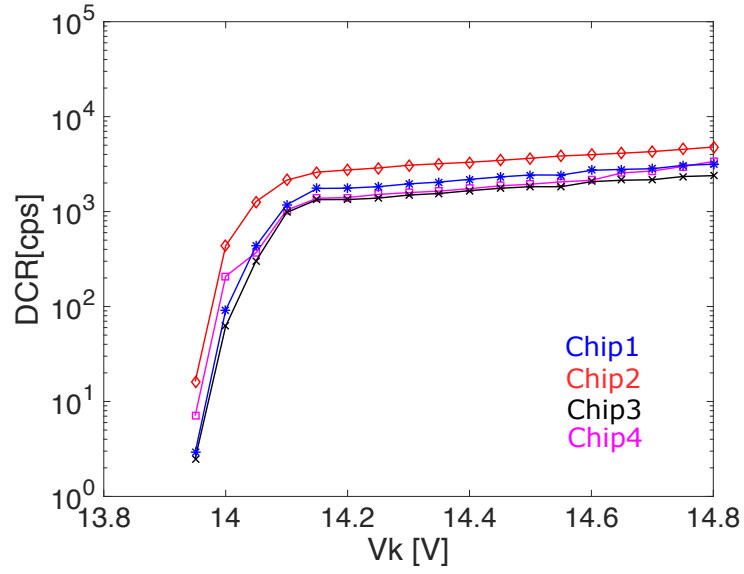
same size and read out by the same kind of front-end channel are compared. It is worth noticing that, whatever the front-end electronics topology and the dimension of the active area are, due to their internal structure, the DPD sensors exhibits a lower DCR as compared to the DPH.
Table 3.1 shows the summarizing results for the mean dark count rate obtained by averaging over all the sensors from the four characterized chips tested at an excess bias voltage of V_{ex} = 1.5 V.

3.1.2 Breakdown voltage distribution

As discussed in the first chapter, the breakdown voltage distribution is an important parameter which has to be evaluated in order to understand how the breakdown voltage of the sensor could vary in different pixels included in an array structure. A good uniformity in the distribution of the breakdown voltage ensures a more stable response of a SPAD array.
Since the avalanche detectors are monolithically integrated with the readout circuits, the anode terminal of the sensor cannot be directly contacted in order to extract the current-voltage curves and, from them, the breakdown voltage (V_{BD}). Therefore, for V_{BD} extraction, DCR vs bias voltage curves were used. Linear interpolation of the DCR vs V_k curves can be used to extract V_{BD} as the intersection point of the interpolating straight line and the x axis [41]. An example of the extraction procedure is shown in Fig. 3.13 for a DPD sensor read out with an active quenching, inverter based front-end channel. With the same procedure, the breakdown voltage has been evaluated for each sensor in the four arrays (one per chip).

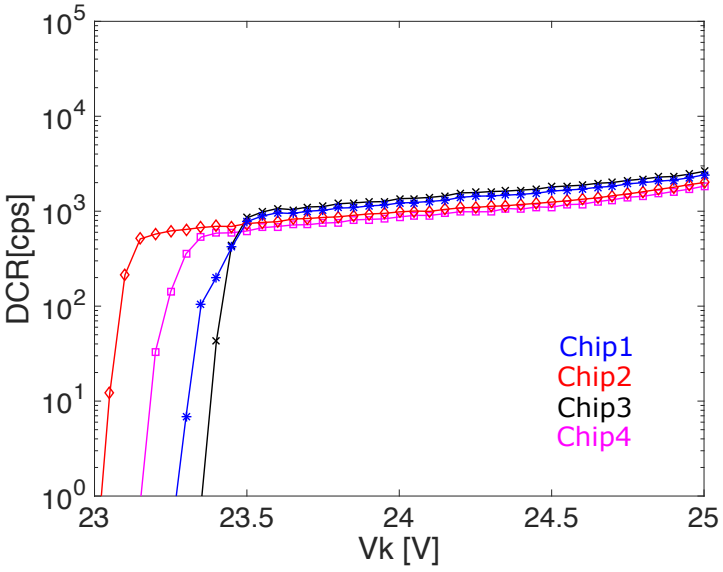


(a)

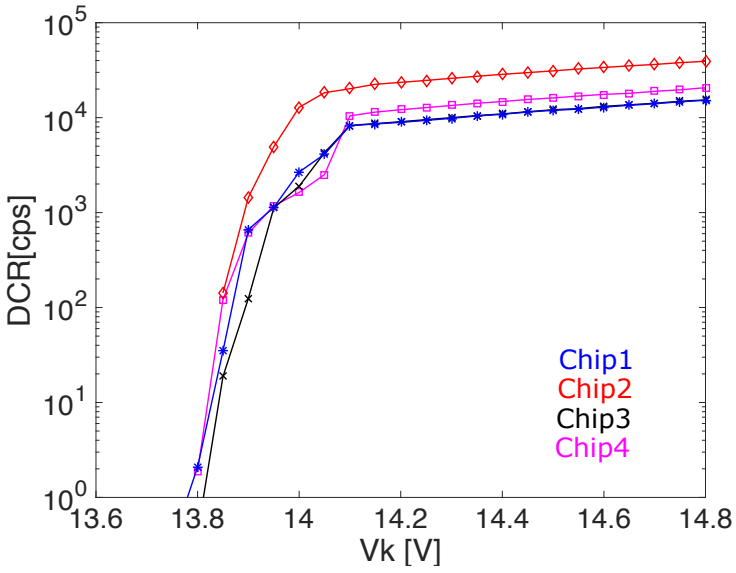


(b)

Figure 3.4: mean DCR of DPD (a) and DPH (b) sensors as a function of the applied bias voltage V_k. Each point of the curves in the two plots were obtained by averaging over all the sensors with an active area of 20 μm $\times$ 20 μm and with the passive quenching readout channel.

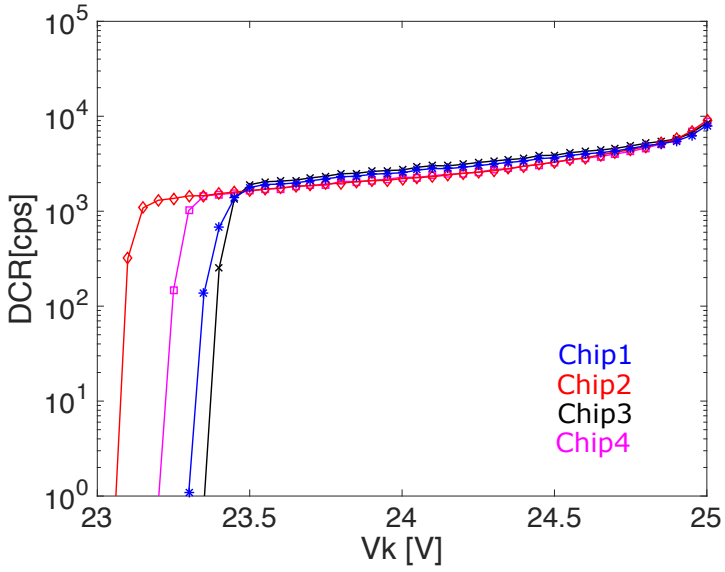


(a)

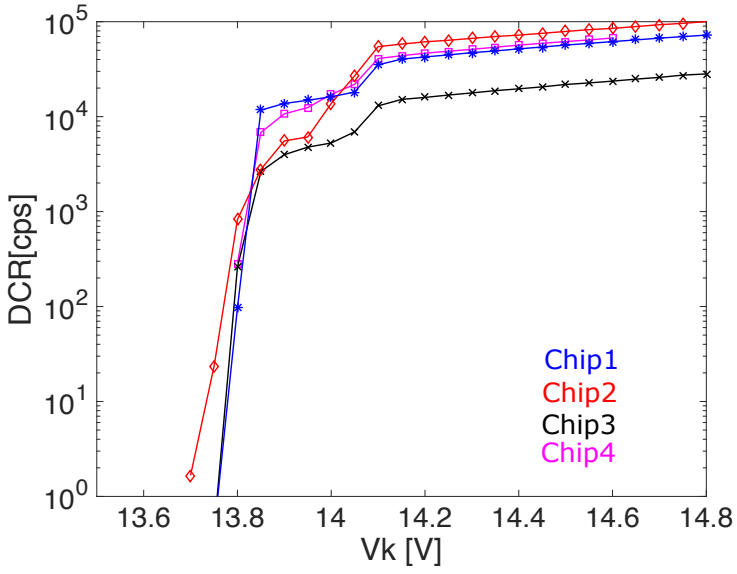


(b)

Figure 3.5: mean DCR of DPD (a) and DPH (b) sensors as a function of the applied bias voltage V_k. Each point of the curves in the two plots were obtained by averaging over all the sensors with an active area of 30 μm $\times$ 30 μm and with the passive quenching readout channel.

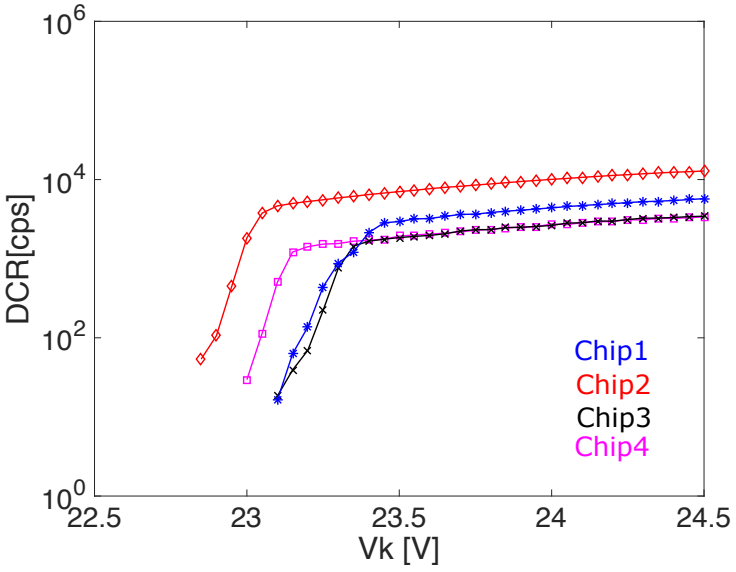


(a)

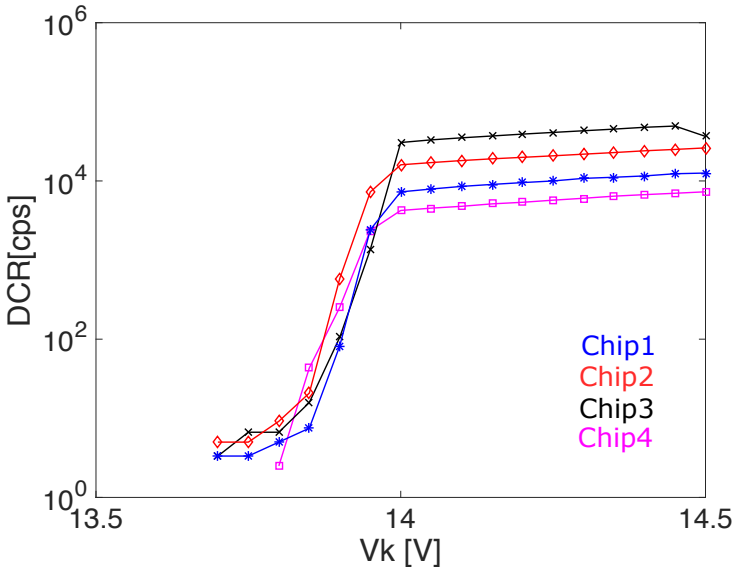


(b)

Figure 3.6: mean DCR of DPD (a) and DPH (b) sensors as a function of the applied bias voltage V_k. Each point of the curves in the two plots were obtained by averaging over all the to sensors with an active area of 36 μm $\times$ 40 μm and with the passive quenching readout channel.

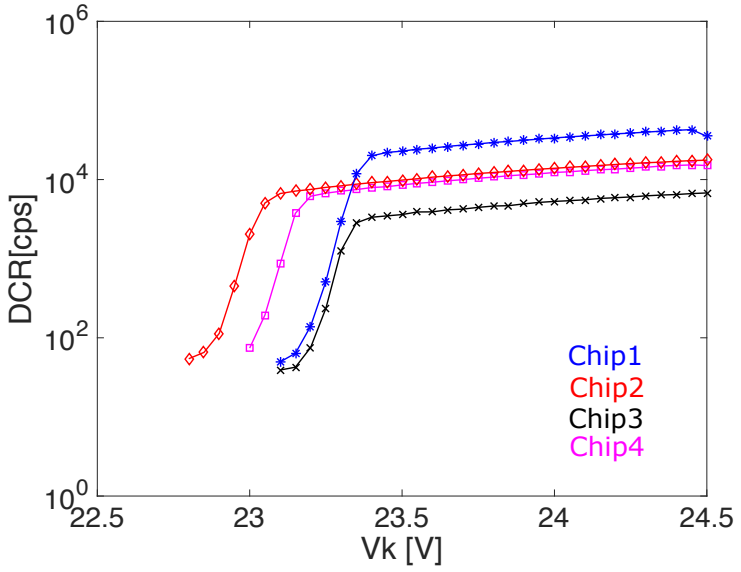


(a)

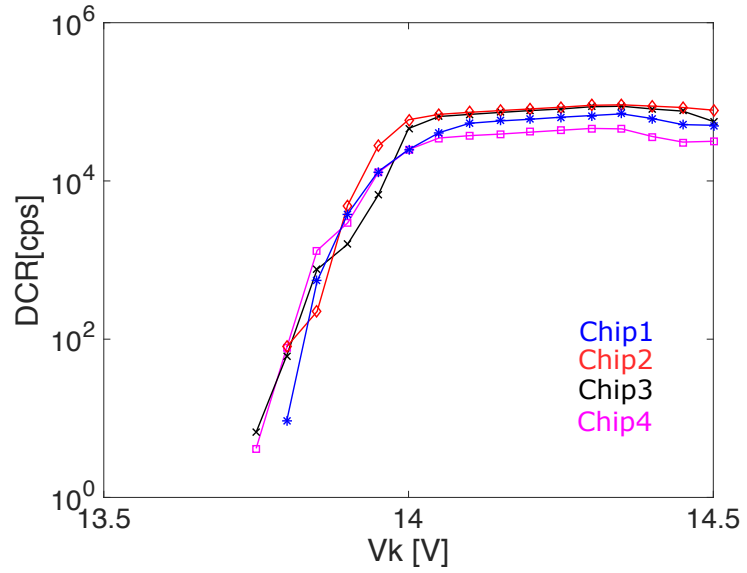


(b)

Figure 3.7: mean DCR of DPD (a) and DPH (b) sensors as a function of the applied bias voltage V_k. Each point of the curves in the two plots were obtained by averaging over all the sensors with an active area of 20 μm $\times$ 20 μm and with the active quenching, comparator based readout channel.

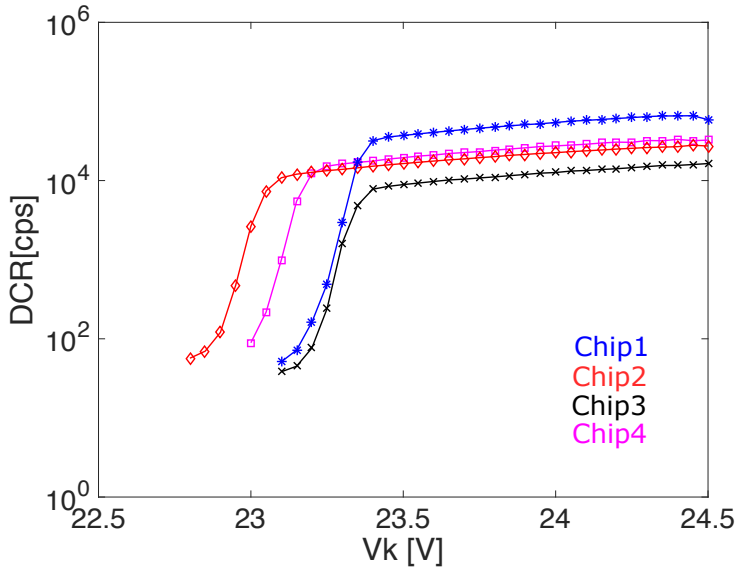


(a)

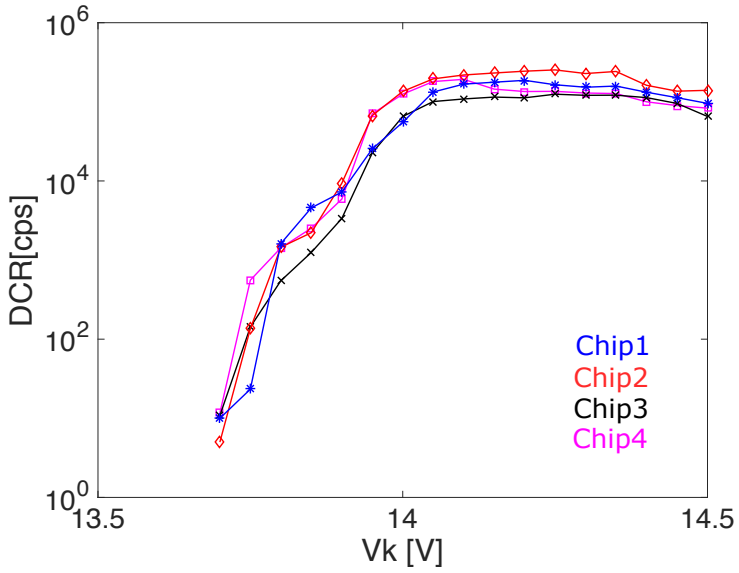


(b)

Figure 3.8: mean DCR of DPD (a) and DPH (b) sensors as a function of the applied bias voltage V_k. Each point of the curves in the two plots were obtained by averaging over all the sensors with an active area of 30 μm $\times$ 30 μm and with the active quenching, comparator based readout channel.

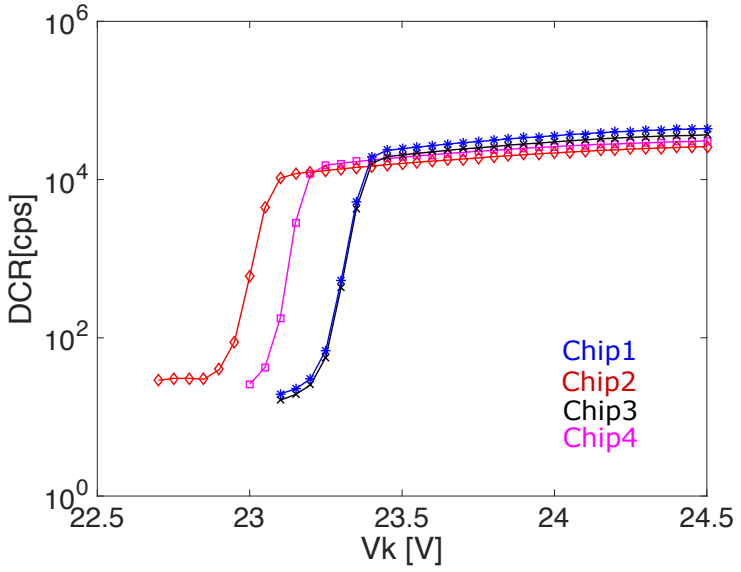


(a)

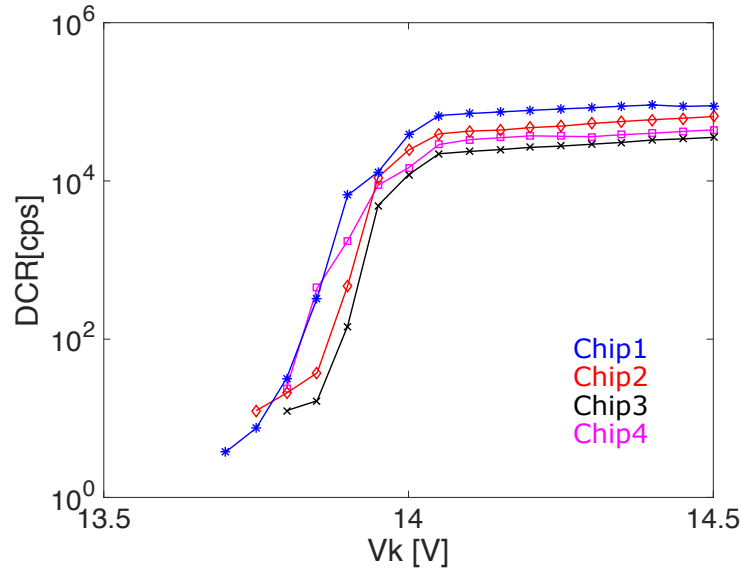


(b)

Figure 3.9: mean DCR of DPD (a) and DPH (b) sensors as a function of the applied bias voltage V_k. Each point of the curves in the two plots were obtained by averaging over all the sensors with an active area of 36 μm $\times$ 40 μm and with the active quenching, comparator based readout channel.

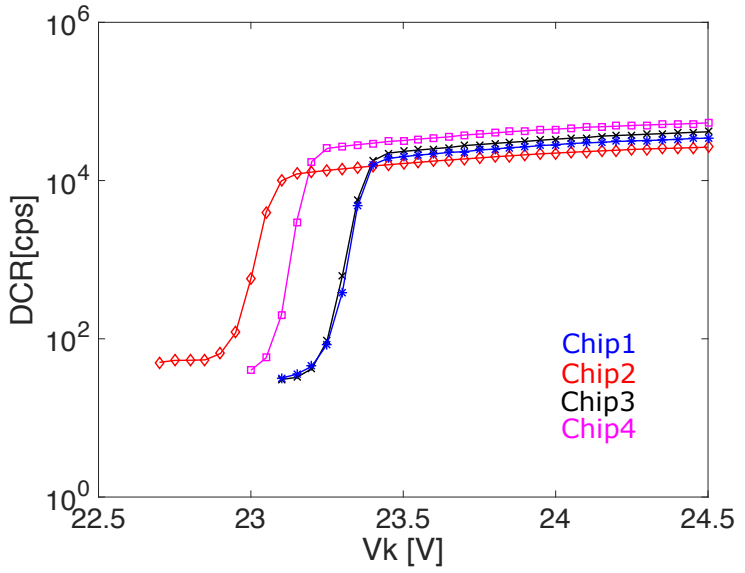


(a)

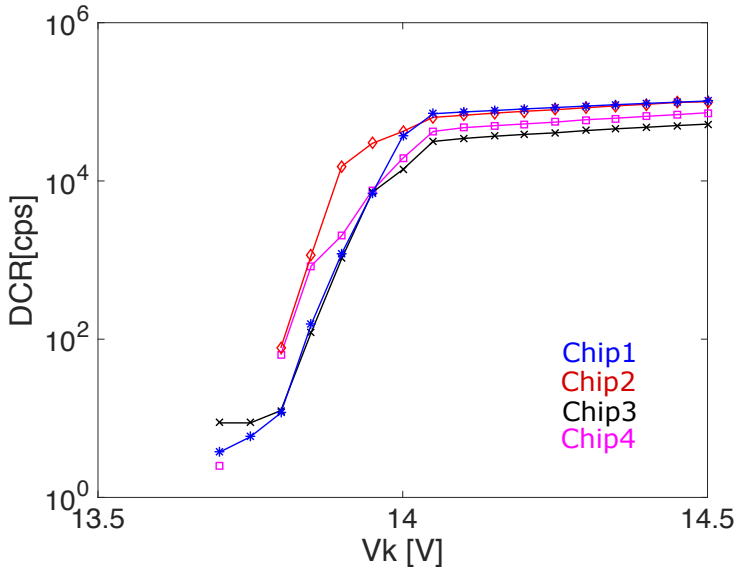


(b)

Figure 3.10: mean DCR of DPD (a) and DPH (b) sensors as a function of the applied bias voltage V_k. Each point of the curves in the two plots were obtained by averaging over all the sensors with an active area of 20 μm $\times$ 20 μm and with the active quenching, inverter based readout channel.

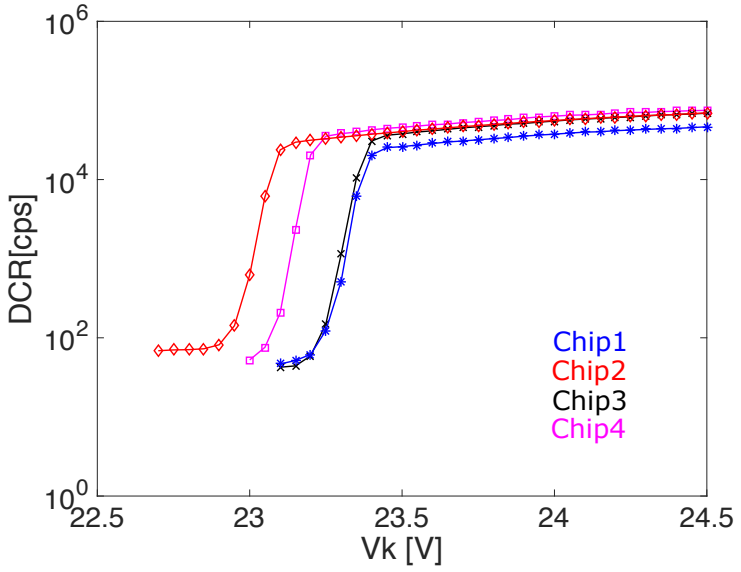


(a)

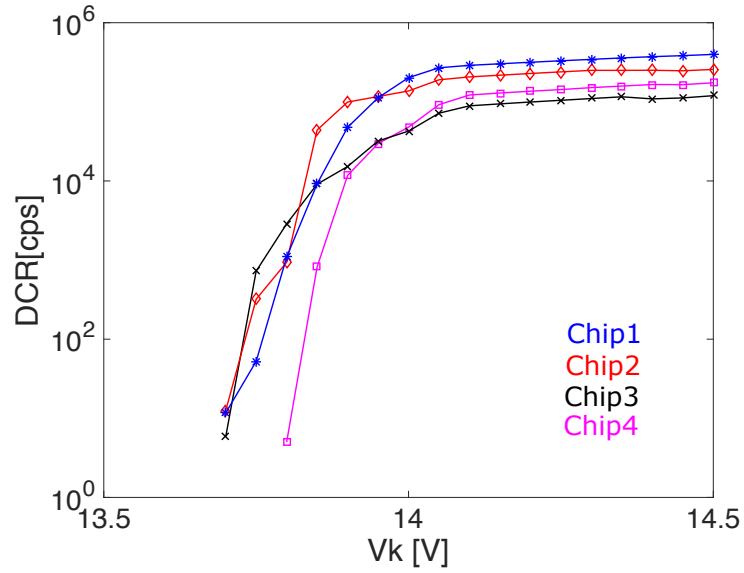


(b)

Figure 3.11: mean DCR of DPD (a) and DPH (b) sensors as a function of the applied bias voltage V_k. Each point of the curves in the two plots were obtained by averaging over all the sensors with an active area of 30 μm $\times$ 30 μm and with the active quenching, inverter based readout channel.



(a)



(b)

Figure 3.12: mean DCR of DPD (a) and DPH (b) sensors as a function of the applied bias voltage V_k. Each point of the curves in the two plots were obtained by averaging over all the sensors with an active area of 36 μm $\times$ 40 μm and with the active quenching, inverter based readout channel.

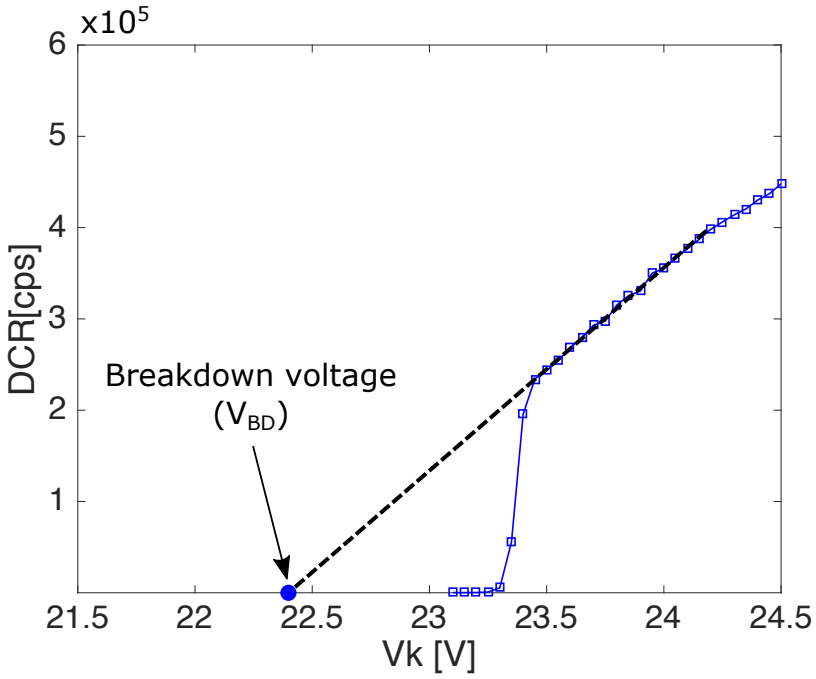
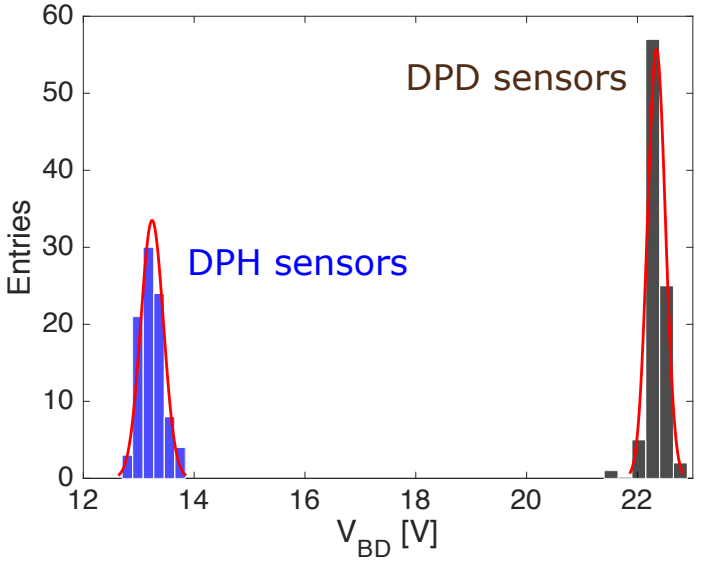
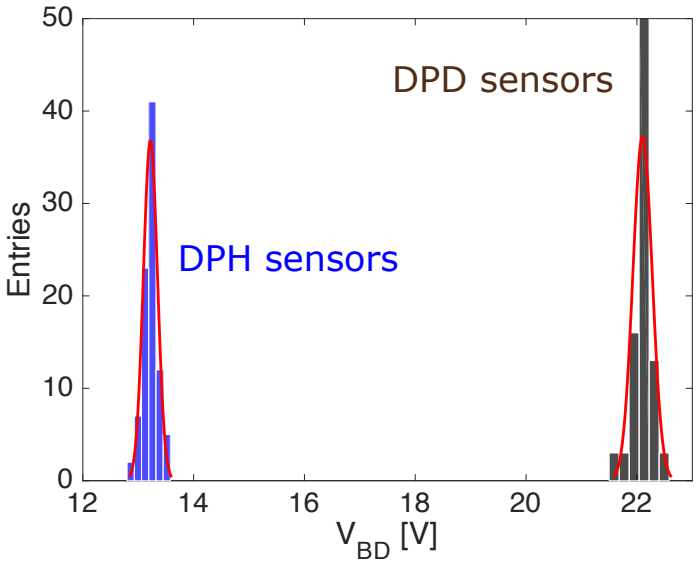


Figure 3.13: breakdown voltage extraction by interpolation of the DCR vs bias voltage curve. The curve is relevant to case of DPD sensor with active quenching, inverter based readout circuit and active area dimension of 36 μm $\times$ 40 μm.

Breakdown voltage uniformity measurements were performed for the two kinds of SPADs tested in this work, DPD and DPH sensors. Measurements include all of the three readout architectures implemented in the test chip. Fig. 3.14 shows the breakdown voltage distribution for DPD and DPH detectors obtained for chip 1 and chip 2, whereas in Fig. 3.15 the distribution obtained for the sensors in chip 3 and chip 4 are displayed. The results show a very good in chip uniformity of the breakdown voltage, both for DPD and DPH sensors. It is worth noticing that, as compared to the DPD ones, DPH devices have a slightly large breakdown voltage dispersion (the standard deviation σ of the distribution). Chip to chip dispersion was also found to be quite limited.
In Table 3.2, the average value and the standard deviation of the breakdown voltage are reported for DPD and DPH sensors. The values are relevant to SPADs in the four different tested chips.

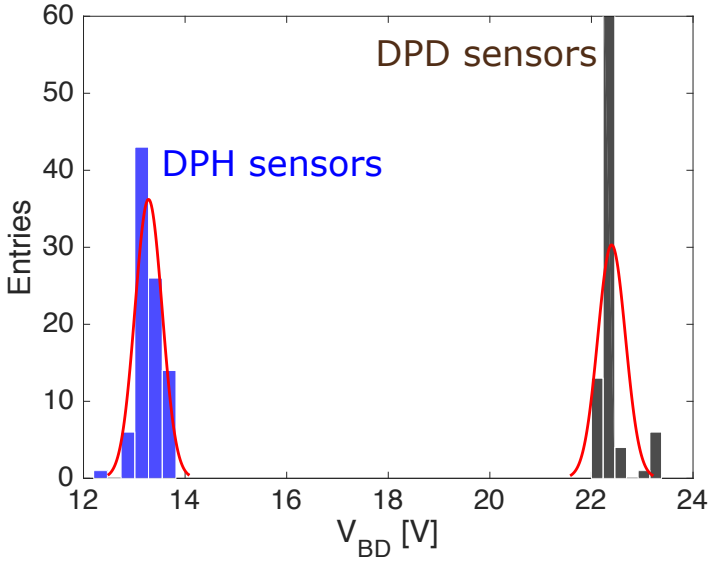


(a)

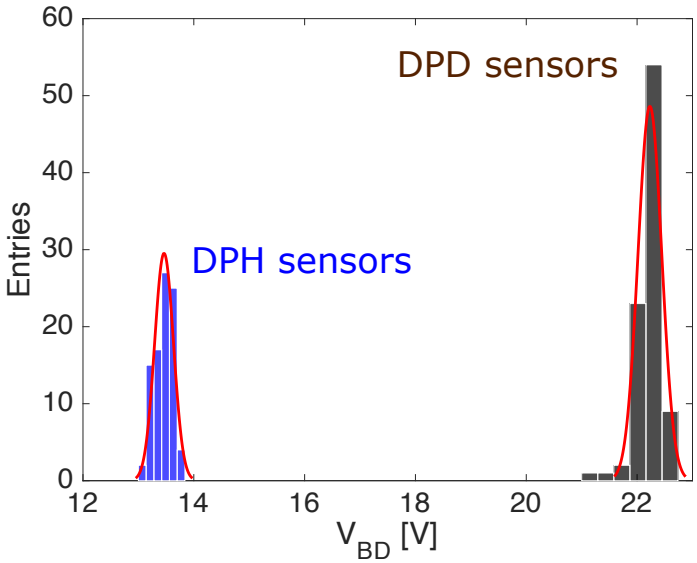


(b)

Figure 3.14: breakdown voltage distribution on chip 1 (a) and chip 2 (b) for all the DPD and DPH sensors in the relevant arrays.



(a)



(b)

Figure 3.15: breakdown voltage distribution on chip 3 (a) and chip 4 (b) for all the DPD and DPH sensors in the relevant arrays.

		Chip 1	Chip 2	Chip 3	Chip 4
DPD	mean V_{BD} [V]	22.3	22.1	22.39	22.27
	std. dev. (σ) [V]	0.161	0.174	0.265	0.142
DPH	mean V_{BD} [V]	13.2	13.22	13.26	13.3
	std. dev. (σ) [V]	0.203	0.176	0.297	0.170

Table 3.2: average value and standard deviation of the breakdown voltage for DPD and DPH sensors in the four tested chips.

3.1.3 Temperature tests

The characterization of DPD and DPH SPADs has been carried out also at different operating temperatures. In particular, one of the four available chips (chip 4) was characterized in a climatic chamber at the University of Trento. The range of temperatures at which the chip was tested goes from -5 °C to 25 °C.
The operating temperature of a SPAD is expected to have an effect on the BD voltage and on the DCR. As extensively discussed in the first chapter, thermal carrier generation not only depends on the fabrication process and the doping profiles of the sensor, but is also related to the temperature. In particular, carrier generation decreases with decreasing temperature and, consequently, also the probability of having an avalanche phenomenon is reduced when the temperature is lowered.
Also, as discussed in the first chapter, the breakdown voltage is expected to decrease with the temperature, because of the increase of the mean free path for carriers due to the lower thermal agitation. Indeed, as the mean free path increases, the energy needed by a carrier to start an avalanche multiplication gets lower. Therefore the breakdown voltage, defined as the voltage at which the free carriers reach a sufficiently high energy to create new electron-hole pairs by hitting the lattice atom, will decrease.
Fig. 3.16 shows the behaviour of the dark count rate as a function of the bias voltage at different temperatures. In particular, the case of DPD sensors with an active area of 36 μm $\times$ 40 μm and passive quenching channel is represented. As expected, the DCR is found to decrease with decreasing temperature. In particular, at an excess bias of 1.5 V, the average DCR is found to decrease by a factor of 2 for every 10 °C decrease in temperature. Also in the case of DPH detectors, a remarkable reduction of the DCR is found when the temperature is decreased. As in the case of DPD sensors, at the same excess bias voltage of 1.5 V, a reduction by a factor of about 2 of the DCR was detected for every

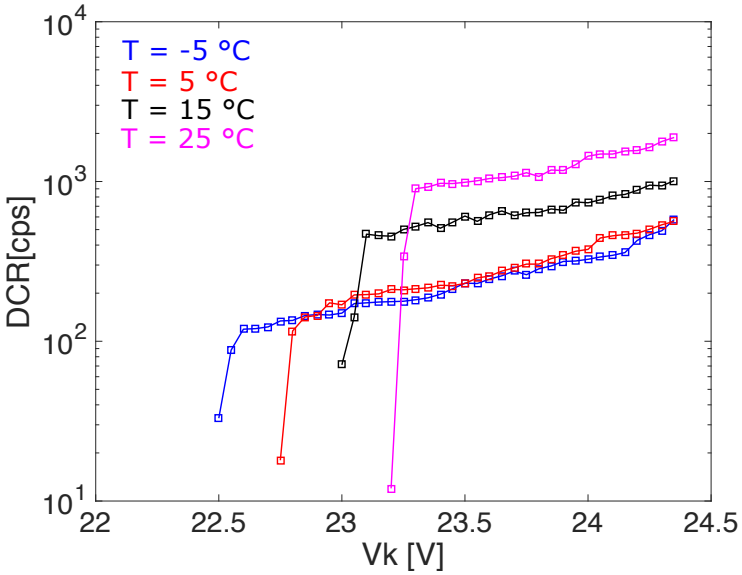
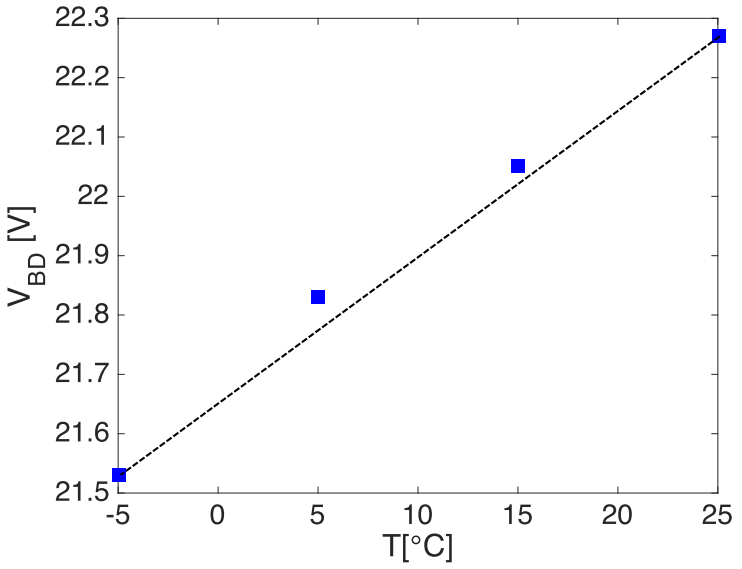


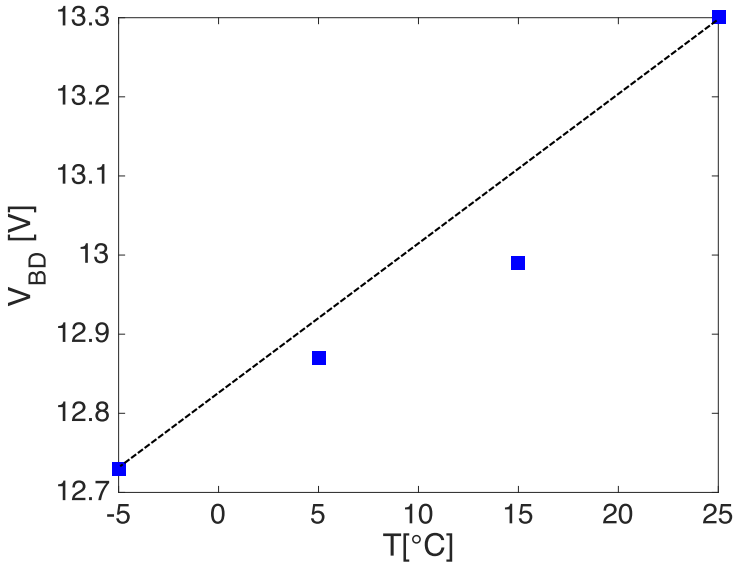
Figure 3.16: mean DCR as a function of the bias voltage at different temperatures. The plot is relevant to DPD sensors with an active area of 36 μm $\times$ 40 μm and passive quenching readout.

10 °C decrease in temperature.

Fig. 3.17a and Fig. 3.17b show the breakdown voltage as a function of the temperature for DPD and DPH SPADs respectively. In both cases, the breakdown voltage is found to change in a liner fashion with the operating temperature, as expected. From these plots, the temperature coefficient for DPD and DPH SPADs can be extracted as the slope of the relevant curves. The temperature coefficient for the DPD sensors turned out to be a little higher than for DPH SPADs (24 mV/°C for DPD sensors, 19 mV/°C for DPH ones). This different behavior may be traced back to the different structure of the two SPADs.
Finally, the breakdown voltage distribution for both sensors was evaluated for different values of the temperature. The results are shown in Fig. 3.18. In the range of temperatures at which the chip was tested, both the DPD and DPH sensors show a good breakdown voltage uniformity. Table 3.3 displays the average value and the standard deviation of the breakdown voltage measured at different temperatures for DPD and DPH sensors in chip 4.

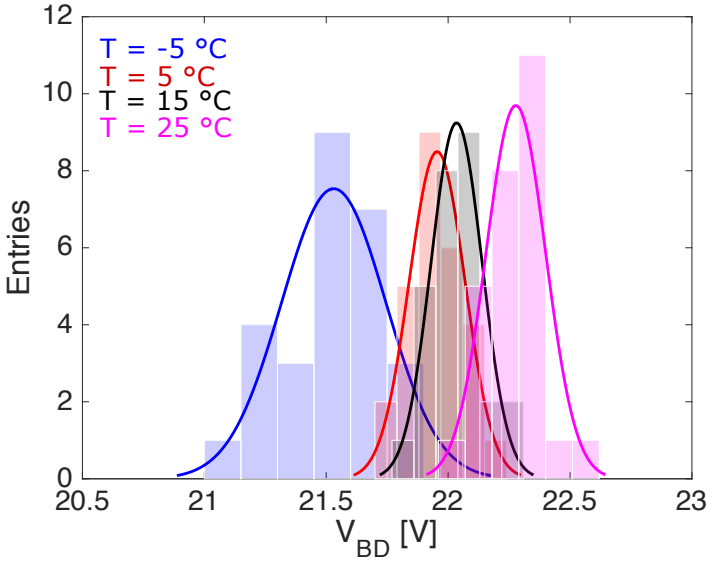


(a)

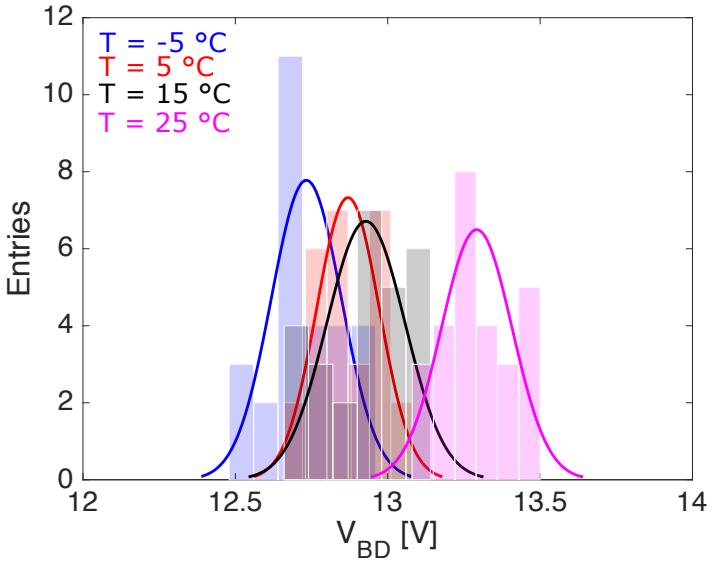


(b)

Figure 3.17: breakdown voltage V_{BD} as a function of the temperature for DPD (a) and DPH (b) sensors.



(a)



(b)

Figure 3.18: breakdown voltage distribution, relevant to DPD (a) and DPH sensors (b), measured at different temperatures.

Chip 4		-5 °C	5 °C	15 °C	25 °C
DPD	mean V_{BD} [V]	21.53	21.83	22.05	22.27
	std. dev. (σ) [V]	0.214	0.114	0.105	0.122
DPH	mean V_{BD} [V]	12.73	12.87	12.93	13.3
	std. dev. (σ) [V]	0.115	0.103	0.128	0.116

Table 3.3: average value and standard deviation of the breakdown voltage distribution measured at different temperatures for DPD and DPH sensors in chip 4.

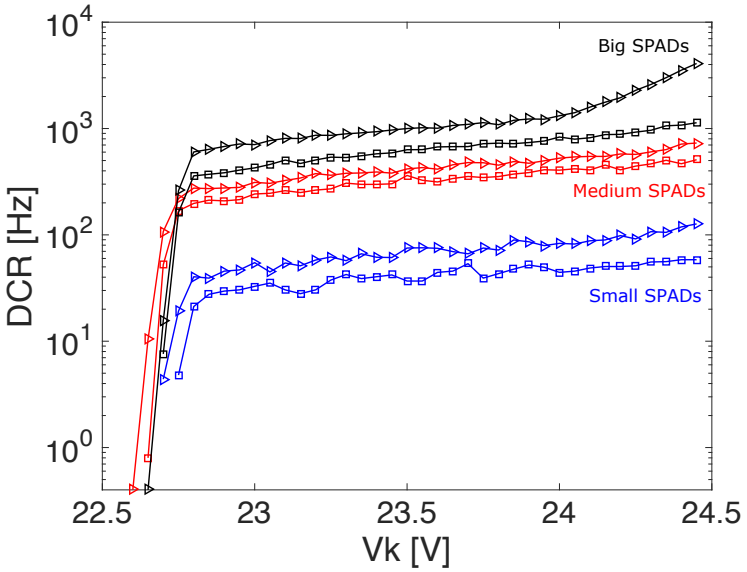
3.2 Irradiation campaigns

To evaluate the radiation tolerance of the SPAD sensors, a couple of irradiation campaigns were planned and carried out, involving exposure to ionizing and non-ionizing radiation sources. Two APIXFAB0 chips were irradiated using a 10 keV, RP-149 X-ray Semiconductor Irradiation System from Seifert available at the Physics and Astronomy Department of the University of Padova (Italy). The final total ionizing dose was 1 Mrad(SiO_2). A different set of DUTs (devices under test), four overall, was exposed to neutrons at the INFN Laboratori Nazionali di Legnaro, Italy. Neutrons were generated by bombarding a thick beryllium target with 5 MeV protons. The maximum fluence reached during the campaign was 10^{11} 1 MeV neutron equivalent cm^{-2}. Measurements on DUTs irradiated with neutrons were performed before and after annealing at 60 °C for 80 minutes. The aim of the annealing procedure was to minimize the effect coming from the short term annealing components of the damage, leaving out only the most stable ones.
It will be hereafter assumed that the performance of the front-end electronics is not significantly affected by neutron irradiation and by the relatively small ionizing doses involved in the experiments discussed in this work. Actually, no neutron induced degradation is expected for the readout circuit, since MOSFET transistors, whose operation is based on the drift of majority carriers at the device channel surface, are known to be largely insensitive to bulk damage [42]. Moreover, CMOS transistors belonging to the 180 nm and 350 nm nodes (with the same gate oxide thickness, respectively, as the core and I/O devices of the technology used here) were actually proven to be tolerant to much larger radiation levels than the 1 Mrad(SiO_2) dose eventually reached in this campaign [43].
For the two irradiation campaigns considered in this work, the radiation levels

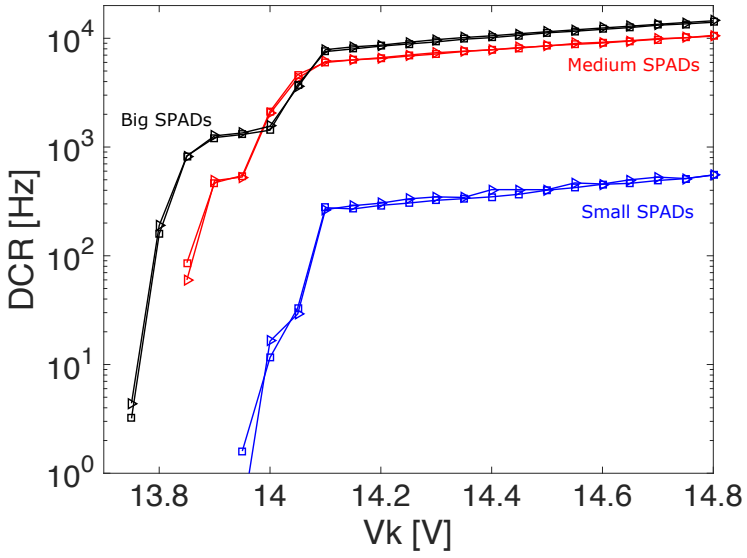
are the relatively moderate ones foreseen for the vertex detector environment of the future linear colliders.
Effects of radiation on DCR and breakdown voltage will be discussed in the following sections.

3.2.1 Total ionizing dose effects

Ionizing radiation effects have been evaluated for both DPD and DPH sensors. The DUTs were not biased during irradiation and, after irradiation, they were always kept at 0 °C while not being characterized. Both irradiation and measurements were performed at room temperature. Post-irradiation results emphasizes a different impact of ionizing radiation on the two kinds of detector in terms of DCR, as Fig. 3.19 shows. The plots in the figure represent the average dark count rate extracted for detectors read out by passive quenching front-end electronics. Triangle markers are used for DCR after X-ray irradiation, whereas square markers represent the DCR before X-ray irradiation.
Fig. 3.19a shows the dark count rate as a function of the voltage applied to the SPAD cathode for sensors of the DPD types read out with a passive quenching based front-end. Below about 24 V, a slight increase in the DCR is observed after exposure to a total ionizing dose of 1 Mrad. This change is likely due to a radiation-induced increase in the state density at the passivating oxide/silicon interface above the active area. This in turn may be responsible for an increase in the surface generation rate [44] and in the probability of the generated carriers to cross the shallow p^+ diffusion and reach the junction depleted region, where they can trigger an avalanche. When V_K gets above 24 V, a much steeper increase in the DCR with the cathode potential is observed in irradiated devices. The underlying mechanism, which is still under investigation, may be related to a radiation-induced breakdown phenomenon in a secondary junction, such as the HV P-well/N-well one, in the region close to the shallow trench isolation oxide (STI, see Fig. 2.2). Radiation-induced charge accumulation in the STI, as well as increase in trap density at or close to the Si/SiO_2 interface, may be responsible for a reduction of the breakdown voltage at that junction [45], leading to the observed sharp increase in DCR at bias voltages above about 24 V.
Fig. 3.19b shows the dark count rate as a function of the reverse voltage for SPADs of the DPH kind again read out by a passive quenching based front-end. As already mentioned, the larger pre-irradiation DCR as compared to the case of DPD sensors might be ascribed to the HV-Nwell implantation below the p^+ shallow diffusion, which is responsible for a larger density of generation centers in the reversely biased junction. Tunneling generation effects might also

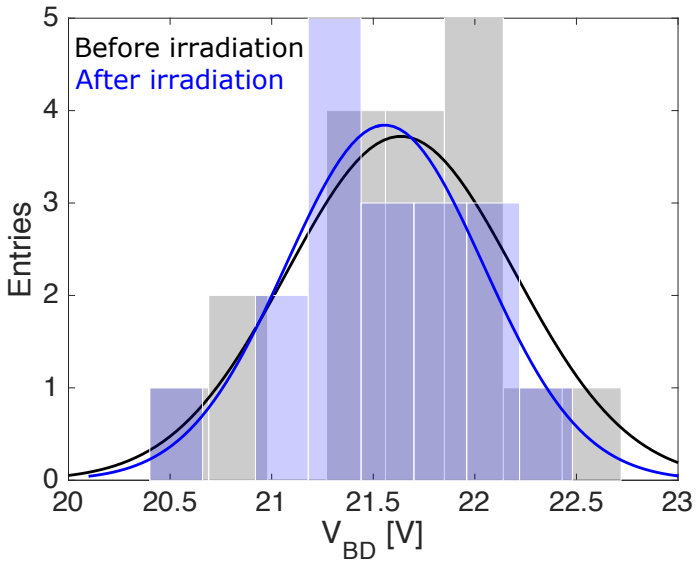


(a)

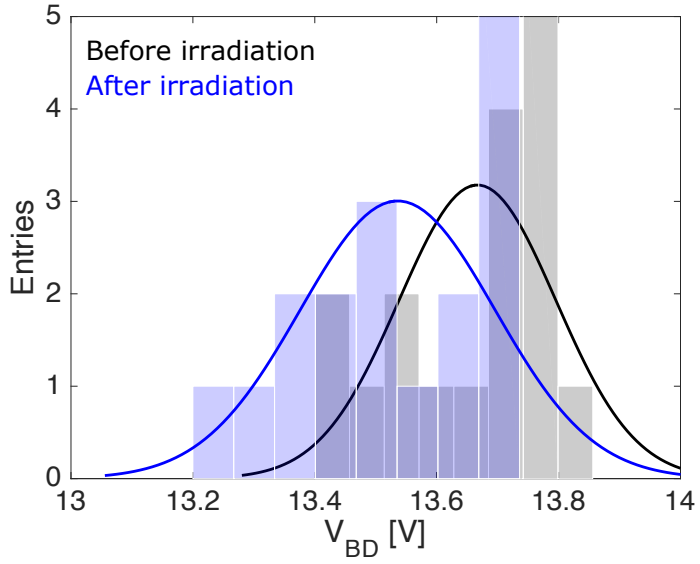


(b)

Figure 3.19: total ionizing dose effects on DPD (a) and DPH (b) sensors. The plots represent the mean value of DCR calculated for all SPADs with the passive quenching readout.



(a)



(b)

Figure 3.20: breakdown voltage distribution for DPD (a) and DPH (b) sensors. The distributions are relevant to the measurements performed before and after irradiation.

be at work here, given the relatively low breakdown voltage, around 13 V as mentioned above [46]. The little DCR change detected after irradiation can be ascribed to the same mechanism proposed in the case of the DPD devices. The smaller relative variation as compared to the SPADs of Fig. 3.19a is due to the substantially larger pre-irradiation DCR value featured by DPH sensors.
Breakdown voltage features no significant changes in the mean value and standard deviation for DPD nor for DPH sensors, as shown in Fig. 3.20. In particular, for the DPD SPAD (Fig. 3.20a), before the irradiation the distribution was found to have a mean V_{BD} of 21.63 V and a σ of 0.48 V, whereas, after exposure to ionizing radiation, the mean V_{BD} is 21.55 V with a σ of 0.55 V. A similar result is obtained with DPH SPADs (Fig. 3.19b) when pre-irradiation and post-irradiation results are compared. In this case, before the irradiation, the mean V_{BD} is 13.67 V with a σ of 0.13 V, whereas a distribution with a mean V_{BD} of 13.54 V and a σ of 0.16 V is obtained after the irradiation procedure.

3.2.2 Neutron irradiation effects

In the neutron source provided by the INFN Laboratori Nazionali di Legnaro, neutrons are generated by bombarding a thick beryllium target with 5 MeV protons. The neutron yield $Y_n(E, \Omega)$ of the source is defined as the number N of neutrons emitted by the source per unit energy E, per unit charge Q impinging on the beryllium target and per unit solid angle Ω and can be expressed as

$$Y_n(E, \Omega) = \frac{dN(E, Q, \Omega)}{dE\ dQ\ d\Omega} = \frac{1}{Q}\frac{dN(E, Q, \Omega)}{dE\ d\Omega}. \tag{3.1}$$

Note that N is proportional to Q, therefore making the right side of the equation only apparently dependent on Q.
The irradiation setup is shown in Fig. 3.21. The samples were located at a distance $r = 50$ mm from the source. Data relevant to a comprehensive characterization of the source show that the neutron yield is a function of the emission angle [47]. However, since the area A of the chips, in the order of 10 mm^2, is much smaller than r^2, the SPAD arrays cover just a small solid angle $\Delta\Omega$ around the zero degree emission angle, such that the change in the neutron yield in that solid angle can be considered negligible.
The DUTs were not biased during irradiation and, after irradiation, they were always kept at 0 °C while not being characterized. Both irradiation and measurements were performed at room temperature.

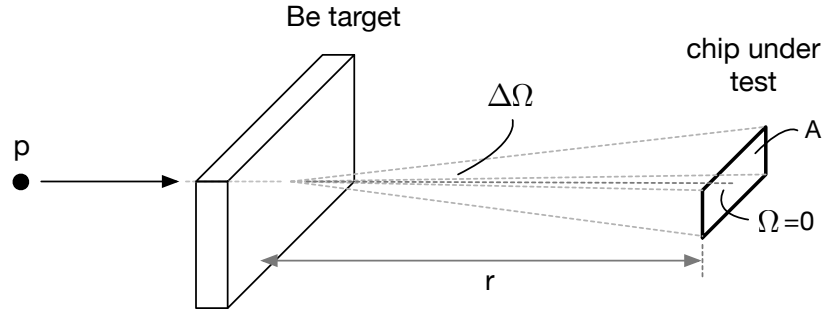


Figure 3.21: schematic representation of the irradiation setup.

3.2.2.1 Model for damage probability in neutron-irradiated SPADs

Irradiation with neutrons is responsible for the creation of deep level defects in the bulk of SPAD devices. The number of displaced atoms and the volume of the disordered region resulting from the interaction is a function of the incident neutron energy [48]. Such defects behave like Shockley-Read-Hall generation centers when they are located in the depletion region of a pn junction [49]. In the following it is assumed that, in the case of single photon avalanche diodes, these radiation-induced generation centers are responsible for an increase in DCR. The effectiveness of such centers in increasing the dark count rate may depend on their position in the depleted region of the junction (defects closer to the neutral region may be less effective as they experience a smaller electric field) and on their activation energy.

3.2.2.2 Damage probability for a single incident neutron

At the energies considered in this work, in the range of a few MeV, scattering (mostly elastic and to a smaller extent inelastic) of neutrons with silicon lattice nuclei is the fundamental mechanism responsible for the creation of radiation-induced defects in the bulk of SPADs. Besides being a function of the energy E, the probability of interaction also depends on the density of atoms N_{at} in the target material (N_{at}=5.7×10^{22} cm^{-3} in silicon). The scattering probability per unit distance travelled by a neutron through the target volume is generally expressed through the macroscopic cross-section Σ_s

$$\Sigma_s(E) = N_{at}\sigma_s(E) = N_{at}\left[\sigma_{es}(E) + \sigma_{is}(E)\right]. \tag{3.2}$$

In the previous equation, σ_s is the microscopic cross-section, or simply cross-

section, of the target nuclei for scattering interactions, resulting from the sum of the elastic scattering cross-section, σ_{es}, and of the inelastic scattering cross-section, σ_{is}.

As already mentioned, the increase of DCR in SPADs can be ascribed to neutron-induced defects in the device depleted region. Fast neutrons, i.e., neutrons with energies from tens of keV to about 10 MeV (an interval including the source used in these tests), do not lose their entire energy in a single collision, but may undergo multiple collisions before coming to a stop [50]. Therefore, neutron interaction with a nucleus in the active volume of the device might take place as the first scattering event after emission from the source (case (a) in Fig. 3.22), after one scattering event outside the depleted region (case (b) in Fig. 3.22) or after two (case (c) in Fig. 3.22) or more of them. The overall probability P_d of a neutron, with initial energy E, creating at least one defect in the SPAD depleted region will be

$$P_d(E, z_1, z_2) = \sum_{j=1}^{M} P_{d,j}(E, z_1, z_2), \tag{3.3}$$

where $P_{d,j}(E, z_1, z_2)$ is the probability of the neutron producing a defect in the depleted region upon the j-th scattering event and not in the previous j-1 collisions, M is the number of collisions after which the neutron energy gets below the threshold for displacement (around 21 eV in silicon) and z_1 and z_2 indicate the position of the upper and the lower side, respectively, of the SPAD depleted region (see Fig. 3.22). Actually, the large majority of the impinging neutrons will pass through the device bulk (as well as the package and the supporting board) without any collision. A negligibly small fraction of those interacting at least once will interact a second time. A much smaller portion of them will create a defect in the depleted region, making the probability of defect creation after one or multiple collisions insignificant. Therefore, in (3.3), all probability terms will be neglected for $j > 1$.

In the following, consistently with the setup geometry, neutrons will be assumed to hit the target perpendicularly to its surface. The probability dP_z that a neutron, upon entering the device bulk, interacts with a silicon nucleus at some generic coordinate z in an infinitesimal slice dz is given by

$$dP_z = \Sigma_s dz \left[1 - P_z(z)\right], \tag{3.4}$$

where $P_z(z)$ is the probability that a scattering event takes place between 0 and z. From (3.4)

$$P_z(z) = 1 - e^{-\Sigma_s z}. \tag{3.5}$$

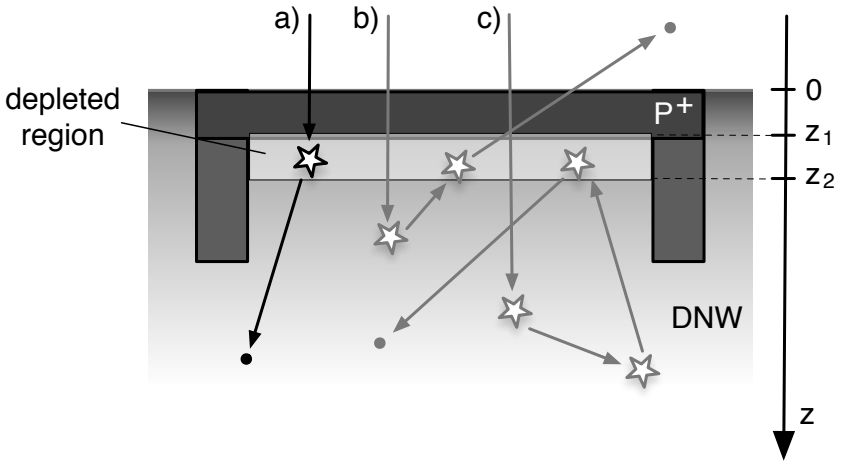


Figure 3.22: neutron interaction in the depleted region of a SPAD, taking place a) as the first scattering event after emission from the source, b) after one scattering event outside the depleted region and c) after two scattering events outside the depleted region.

By definition, the probability density function $p_z(z)$ for a neutron interacting in z is

$$p_z(z) = \frac{dP_z}{dz} = \Sigma_s e^{-\Sigma_s z}. \tag{3.6}$$

With reference to Fig. 3.22, the probability of a neutron undergoing a scattering event, for the first time after emission, in the depleted region of the SPAD is given by

$$\begin{aligned} P_{d,1}(E, z_1, z_2) &= \int_{z1}^{z2} \Sigma_s(E) e^{-\Sigma_s(E) z} dz = \\ &= e^{-\Sigma_s(E) z_1} - e^{-\Sigma_s(E) z_2} \end{aligned} \tag{3.7}$$

which, based on the above considerations about the probability of multiple collisions, is a good approximation of $P_d(E, z_1, z_2)$.

3.2.2.3 Damage probability for a given source spectrum

The source used for the neutron irradiation campaign consists of a thick beryllium target bombarded with 5 MeV protons. The total number of neutrons

N_T emerging from the source and hitting the chip under test is given by

$$N_T = Q_T \int_{E_i}^{E_f} \int_{\Delta\Omega} Y_n(E, \Omega) d\Omega dE, \tag{3.8}$$

where Q_T is the total amount of charge hitting the beryllium target and $Y_n(E, Q)$ is assumed to have support in $[E_i, E_f]$. As already mentioned, the chips cover a small solid angle $\Delta\Omega$ around the 0° emission angle, where the neutron yield can be considered constant as a function of Ω. Therefore

$$N_T \simeq Q_T \Delta\Omega \int_{E_i}^{E_f} Y'_n(E) dE, \quad Y'_n(E) = Y_n(E, 0), \tag{3.9}$$

where $\Delta\Omega \simeq \frac{A}{r^2}$. In the same solid angle, the relationship between $Y'_n(E)$ and the spectral fluence $\phi(E, r)$ at a distance r from the source is given by

$$\phi(E, r) = \frac{Q_T \Delta\Omega}{A} Y'_n(E) \simeq \frac{Q_T}{r^2} Y'_n(E). \tag{3.10}$$

The above approximations, taking advantage of the small size of the samples, can a fortiori be applied to each single SPAD sensor in the chips under irradiation. The probability of a single neutron at a given energy E_k not creating any defect in the SPAD depleted region is $1 - P_d(E_k, z_1, z_2)$. Since the scattering events are statistically independent, the probability $P_{nd}(E_k, z_1, z_2)$ of $N_n(E_k)$ neutrons at energy E_k not damaging the SPAD junction is given by

$$P_{nd}(E_k, z_1, z_2) = \left[1 - P_d(E_k, z_1, z_2)\right]^{N_n(E_k)}, \tag{3.11}$$

where

$$N_n(E_k) = Q_T Y'_n(E_k) \Delta\Omega \Delta E \simeq \frac{A_s}{r^2} Q_T Y'_n(E_k) \Delta E \tag{3.12}$$

is the number of neutrons with energy in $[E_k, E_k + \Delta E]$ hitting the SPAD active area A_s. The overall probability $P_{nd,T}$ of having no damage in the device active volume, accounting for the whole energy spectrum of the source, can be approximately calculated by subdividing the spectrum support $[E_i, E_f]$ into $M = \frac{E_f - E_i}{\Delta E}$ equal subintervals and computing the product

$$
\begin{aligned}
P_{nd,T} &\simeq \prod_{k=0}^{M} P_{nd}(E_k) = \\
&= \prod_{k=0}^{M} \left[1 - P_d(E_k, z_1, z_2)\right]^{N_n(E_k)}, \\
&E_k = E_i + k\Delta E.
\end{aligned} \tag{3.13}
$$

The probability in (3.13) can be more accurately estimated by calculating the limit for ΔE going to 0,

$$
P_{nd,T} = \lim_{\Delta E \to 0} \prod_{k=0}^{M} P_{nd}(E_k). \tag{3.14}
$$

By taking the natural logarithm of both sides, the previous equation can be rewritten as

$$
\begin{aligned}
\ln(P_{nd,T}) &= \ln\left(\lim_{\Delta E \to 0} \prod_{k=0}^{M} P_{nd}(E_k)\right) = \\
&= \lim_{\Delta E \to 0} \ln\left(\prod_{k=0}^{M} P_{nd}(E_k)\right)
\end{aligned} \tag{3.15}
$$

where the interchange between the logarithm and the limit operator is made possible by the continuity of $\ln(x)$, under the hypothesis that the limit exists. Now

$$
\begin{aligned}
\ln\left(\prod_{k=0}^{M} P_{nd}(E_k)\right) &= \sum_{k=0}^{M} \ln(P_{nd}(E_k)) = \\
&= \sum_{k=0}^{M} N_n(E_k) \ln\left(1 - P_d(E_k, z_1, z_2)\right).
\end{aligned} \tag{3.16}
$$

Therefore

$$\ln(P_{nd,T}) = \tag{3.17}$$
$$= Q_T \Delta\Omega \lim_{\Delta E \to 0} \sum_{k=0}^{M} Y'_n(E_k) \ln\left(1 - P_d(E_k, z_1, z_2)\right) \Delta E =$$
$$= \frac{Q_T A_s}{r^2} \cdot \int_{E_i}^{E_f} Y'_n(E) \ln\left(1 - e^{-\Sigma_s(E) z_1} + e^{-\Sigma_s(E) z_2}\right) dE.$$

Note that, if $\Sigma_s(E) z_1 \ll 1$ and $\Sigma_s(E) z_2 \ll 1$, as is the case with SPADs, featuring a shallow junction and a thin depleted region, then

$$e^{-\Sigma_s(E) z_1} - e^{-\Sigma_s(E) z_2} \simeq \Sigma_s(E)(z_2 - z_1) \tag{3.18}$$

and

$$\ln\left(1 - \Sigma_s(E)(z_2 - z_1)\right) \simeq -\Sigma_s(E)(z_2 - z_1). \tag{3.19}$$

Therefore

$$\ln(P_{nd,T}) \simeq -\frac{Q_T A_s \Delta z}{r^2} \int_{E_i}^{E_f} Y'_n(E) \Sigma_s(E) dE. \tag{3.20}$$

where $\Delta z = z_2 - z_1$. Eventually, the probability $P_{d,T}$ of at least one neutron undergoing a scattering event in the active volume of the SPAD is given by

$$P_{d,T} = 1 - P_{nd,T} \simeq 1 - e^{-\frac{Q_T A_s \Delta z}{r^2} \int_{E_i}^{E_f} Y'_n(E) \Sigma_s(E) dE} =$$
$$= 1 - e^{-A_s \Delta z \int_{E_i}^{E_f} \phi(E,r) \Sigma_s(E) dE}. \tag{3.21}$$

The probability $P_{d,T}$ can be expressed as a function of the 1 MeV neutron equivalent fluence $\Phi_{eq}(r)$. From (3.10),

$$\Phi_{eq}(r) = k_\phi \int_{E_i}^{E_f} \phi(E, r) dE = k_\phi \frac{Q_T}{r^2} \int_{E_i}^{E_f} Y'_n(E) dE \Rightarrow$$
$$\Rightarrow \frac{Q_T}{r^2} = \frac{\Phi_{eq}(r)}{k_\phi \int_{E_i}^{E_f} Y'_n(E) dE}. \tag{3.22}$$

In (3.22), k_ϕ is a hardness factor characteristic of the source, which can be calculated based on the displacement damage cross-section for neutrons in silicon [51]. By replacing $\frac{Q_T}{r^2}$ in (3.21), $P_{d,T}$ can be rewritten as

$$P_{d,T} \simeq 1 - e^{-\Phi_{eq}(r)\frac{A_s \Delta z}{k_\phi \int_{E_i}^{E_f} Y'_n(E)dE} \int_{E_i}^{E_f} Y'_n(E)\Sigma_s(E)dE} = 1 - e^{-\Phi_{eq}(r)\frac{A_s \Delta z}{k_\phi \int_{E_i}^{E_f} \phi(E,r)dE} \int_{E_i}^{E_f} \phi(E,r)\Sigma_s(E)dE}. \quad (3.23)$$

In the case of a monochromatic source, emitting neutrons at energy E_0, the spectral fluence $\phi(E, r)$ can be written as

$$\phi(E, r) = \Phi_0(r)\delta(E - E_0), \quad (3.24)$$

where $\Phi_0(r)$ is the neutron fluence at distance r from the source and $\delta(E)$ is the Dirac delta distribution. Then, the probability $P_{d,T}$ can be expressed as

$$P_{d,T} \simeq 1 - e^{-\Phi_{eq}(r)\frac{A_s \Delta z \Sigma_s(E_0)}{k_\phi}}. \quad (3.25)$$

3.2.2.4 Model validation

Figures 3.23 a) and b) show the theoretical damage probability $P_{d,T}$, computed based on (3.23), as a function of the device active area for DPD and DPH devices respectively (dash-dotted curves). In both figures, $P_{d,T}$ is plotted for two different values of the fluence, 10^{10} and 10^{11} 1 MeV neutron equivalent cm^{-2}. The depleted junction thickness Δz has been estimated by taking into account the measured breakdown voltage [52], 22.27 V and 13.3 V on average for DPD and DPH devices respectively, which was not affected by exposure to neutron. A value of 0.8 μm was calculated in the case of DPD SPADs assuming a linearly graded junction model, a value of 0.5 μm was found instead in the case of DPH devices under the hypothesis of one-sided step junction. The neutron yield of the source at a 0° angle, as made available in the literature [47], was used for the calculation of $P_{d,T}$. Tabulated data for elastic and inelastic scattering cross-section of neutrons in silicon as a function of energy, also needed for computing $P_{d,T}$, can be found online [53]. Both in Fig. 3.23 a) and in Fig. 3.23 b), the theoretical probability curves are compared with the experimental data, represented by empty square and full triangle markers. Each point represents the fraction of SPADs featuring a post-irradiation DCR increase of at least 5% as compared to the pre-irradiation value. The 5% threshold was chosen to account for possible dark count rate variations due to temperature fluctuations. DCR was measured at an excess voltage of 2 V

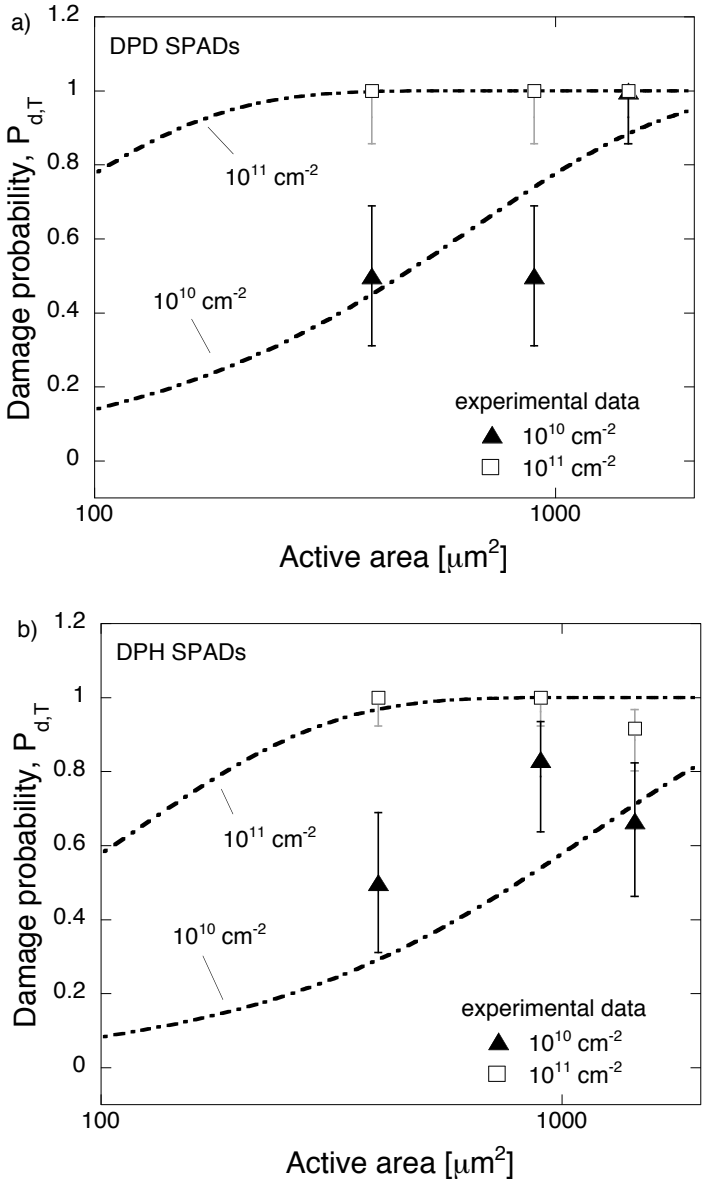
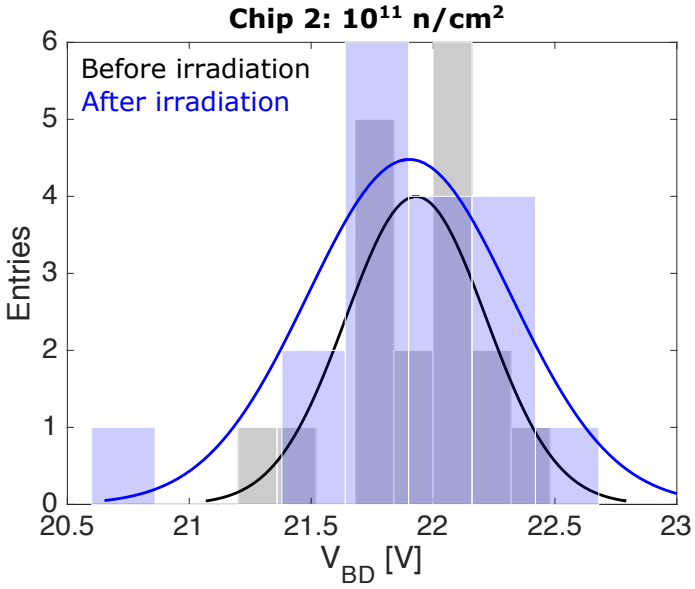


Figure 3.23: damage probability in 180 nm SPADs irradiated with different 1 MeV neutron equivalent fluences as a function of the device active area: a) DPD and b) DPH devices. Theoretical curves (lines) are compared with experimental data (symbols).

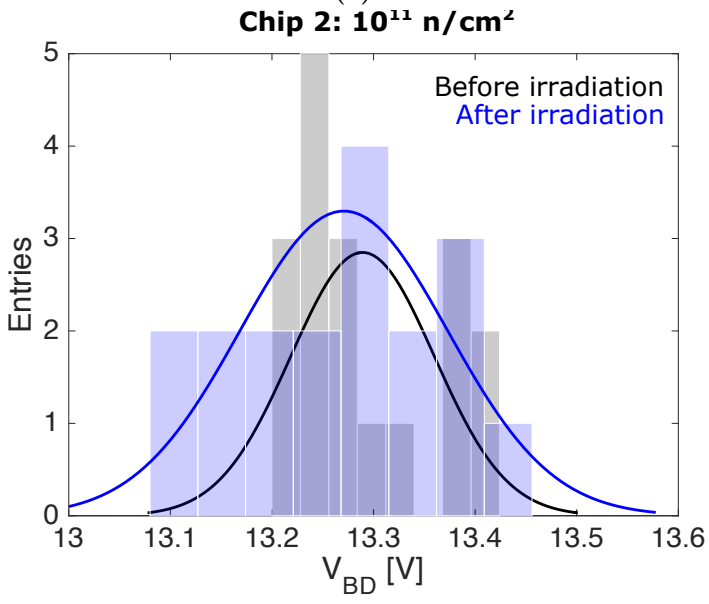
for DPD devices, of 1 V for DPH SPADs. The error bars represent the 68% confidence interval computed according to the Wilson score method [54]. This was done under the assumption that the data can be treated as a series of success-failure experiments (Bernoulli trials), where a successful experiment corresponds to a SPAD featuring a DCR increase beyond the 5% threshold. The theoretical model turns out to be in good agreement with the experimental results at the fluence of 10^{11} cm^{-2}. The less good agreement which can be detected at the smaller fluence may be ascribed to statistical fluctuations in the experimental data, due to the limited number of samples under test, only 6 for each point in the two figures, the only exception being represented by the three data points relevant to DPH devices at the fluence of 10^{11} cm^{-2}, for which 12 samples were available.

3.2.2.5 Effects on breakdown voltage and DCR

This section is devoted to presenting further results from the characterization of SPADs exposed to neutron fluences of 10^{10} n_{eq} cm^{-2} and 10^{11} n_{eq} cm^{-2}. Later in the section, the effects on the DCR and breakdown voltage of the 60 °C/80 min annealing procedure is discussed.
In the neutron irradiated chips, no substantial change in the breakdown voltages was detected. As an example, in Fig. 3.24 shows the breakdown voltage distribution for DPD sensors irradiated at the highest fluence, compared with the distribution before irradiation. The mean value and the standard deviation are not significantly changed by the exposure to neutrons. Very similar results were found in the case of DPH sensors.
The results from the characterization of the irradiated chips in terms of DCR show instead a huge increase in the rate of the dark pulses. In particular, the chip irradiated at the fluence of 10^{11} n_{eq} cm^{-2}, exhibits a DCR increase of more than three orders of magnitude in some sensors. At the 10^{10} cm^{-2} fluence, the DCR increase, as expected, is smaller. The above considerations hold both for DPD and DPH sensors.
Fig. 3.25 shows the dark count rate, before and after irradiation at the two different fluences, in the case of DPD sensors with passive quenching readout. As mentioned above, irradiation with neutrons is responsible for the creation of deep level defects in the bulk of the DUTs. The number of displaced atoms and the volume of the disordered region resulting from the interaction is a function of the incident neutron energy [55]. Such defects behave like Shockley-Read-Hall generation centers when they are located in the depletion region of a p-n junction [48] and, in the case of SPADs, are very likely responsible for the ob-

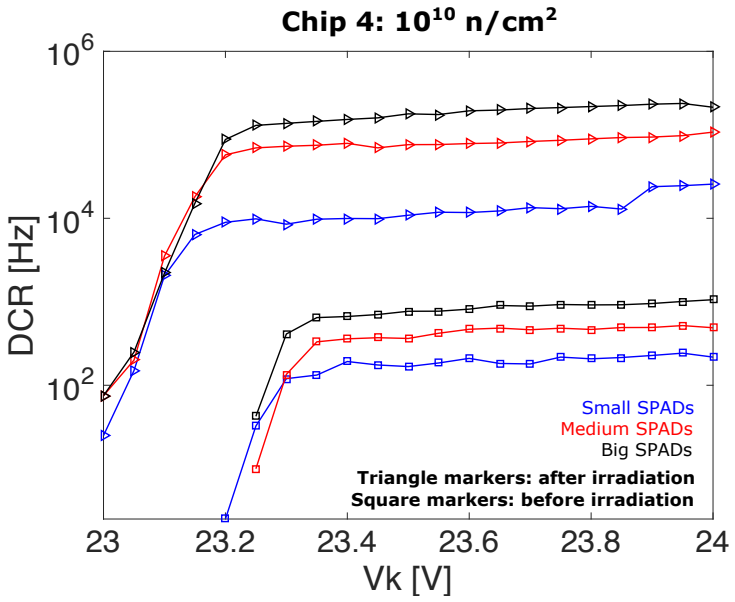


(a)

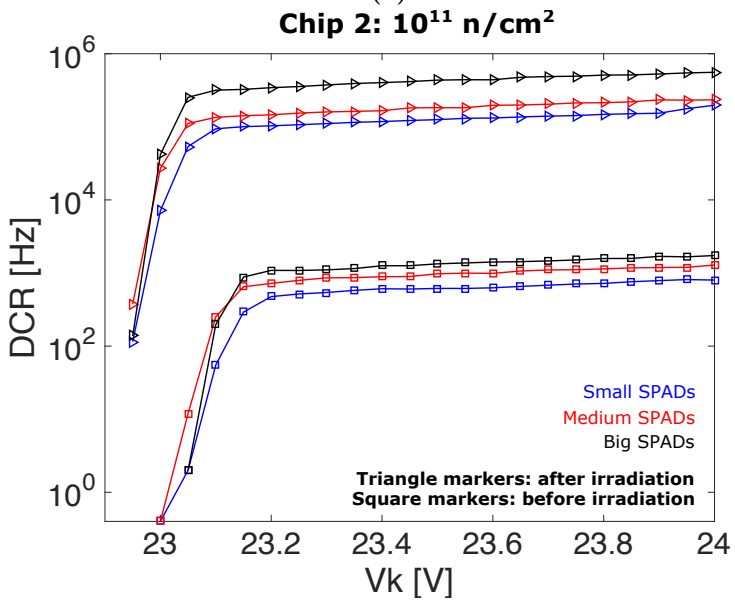


(b)

Figure 3.24: breakdown voltage distribution, relevant to DPD and DPH sensors, before and after neutron irradiation at the highest fluence.



(a)



(b)

Figure 3.25: average value of the DCR, relevant to DPD sensors with passive quenching readout, performed before and after neutron irradiation.

served increase in DCR. The amount of defects created in that region, which represents the sensitive volume of the detector, can be reasonably assumed to be proportional to the volume itself (the thickness of the depleted region times the sensor area) and to the neutron fluence. Actually, neutron-induced deep level creation is more likely to take place in sensors with larger area. At larger fluences, the probability that one or more cells are not affected by irradiation becomes smaller and defects may start cumulating in the depleted region of the single detector element, leading to a larger increase in DCR than at smaller fluences.

3.2.2.6 Annealing procedure

As already mentioned, an annealing procedure at 60 °C for 80 minutes was performed on the chips irradiated with neutrons in order to minimize the effect of the short term annealing components of the damage, keeping only the most stable ones. Subsequently, the chips were characterized in order to assess the effects on the mean DCR.

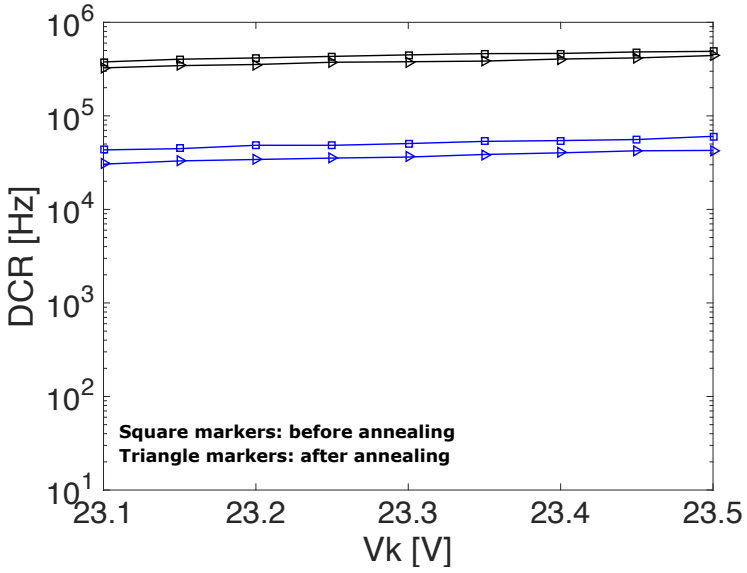
Fig. 3.26 shows two examples of the resulting DCR vs V_k curves obtained after annealing. Fig. 3.26a is relevant to two DPD sensors where a reduction in DCR was detected. Fig. 3.26b refers to the case of two DPD sensors where no change at all was observed. The different outcome depends on the stochastic nature of neutron damage in the lattice. In the case of Fig. 3.26b, no unstable defects were created by neutron irradiation. In the case of Fig. 3.26a, post-irradiation DCR increase is partly to be ascribed to unstable defects, which are then annealed through the annealing procedure.

3.2.2.7 Temperature tests

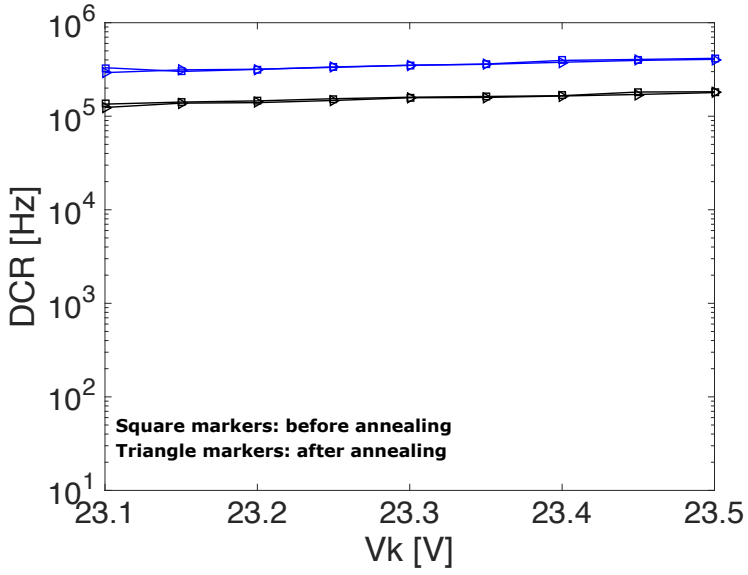
The chip irradiated at the largest fluence (chip 2) was also tested at different operating temperatures in order to evaluate how the temperature affects DCR in SPADs after neutron irradiation. The tests were performed at the Department of Physics in Pavia taking advantage of a climatic chamber.

As compared to the temperature tests performed on the non-irradiated chips, in this case a wider range of temperatures was used. In particular, the minimum temperature reached during measurements was -30 °C. Only the pixels implementing the passive quenching channels were characterized.

Fig. 3.27 shows the DCR as a function of the temperature for DPD and DPH sensors. In particular, results from the characterization of SPADs with a 30 μm $\times$ 30 μm active area and with passive quenching readout channel are displayed. In both cases, a change of about one order of magnitude is detected



(a)



(b)

Figure 3.26: DCR measured in two DPD sensors with 30 μm $\times$ 30 μm active area, irradiated with neutrons at the largest fluence, before and after the annealing procedure. Plot (a) shows the case of a reduction of the DCR after annealing, whereas plot (b) shows the case of no change.

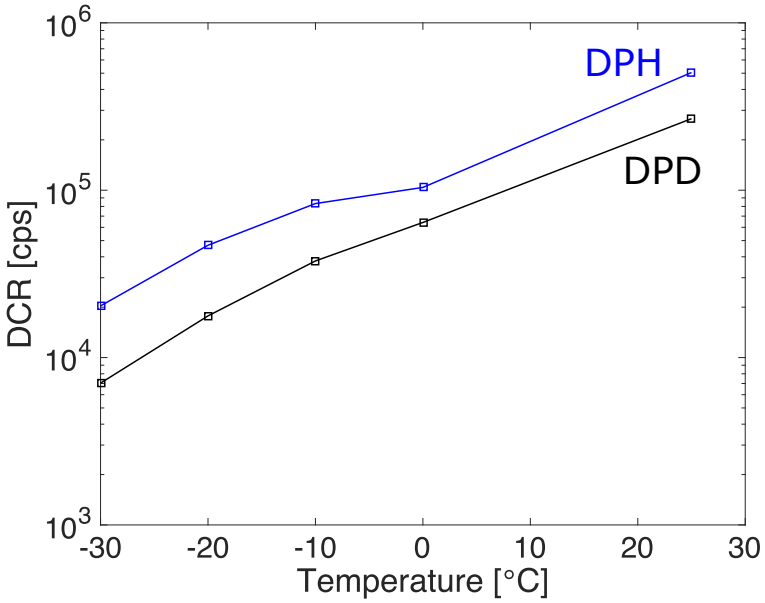
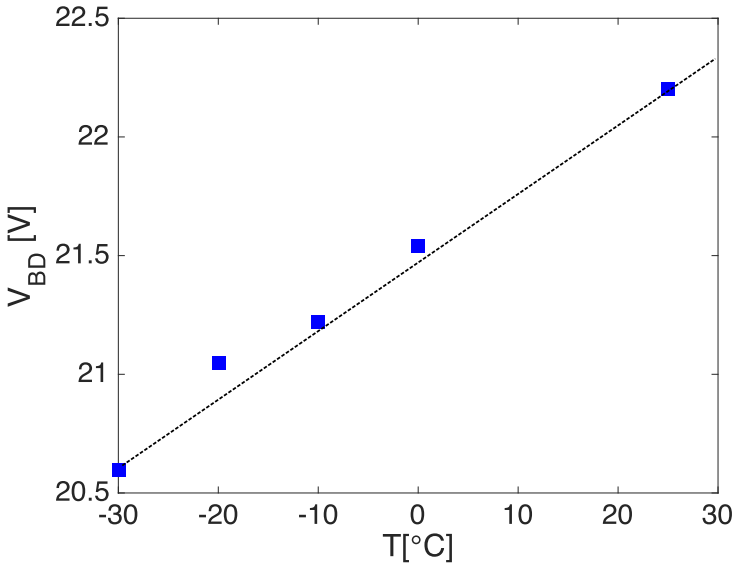
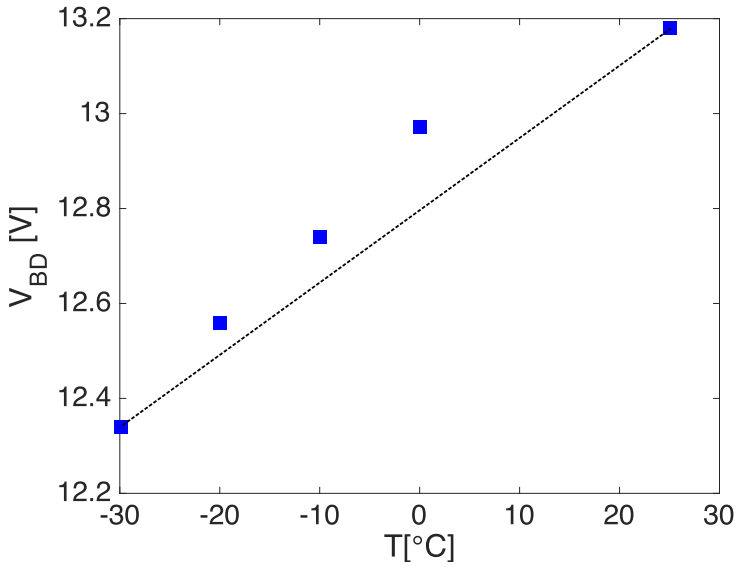


Figure 3.27: DCR as a function of the temperature for both kinds of sensors after irradiations. The results are relevant to sensors with an active area of 30 μm $\times$ 30 μm and passive quenching front-end electronics.

between the DCR measured at the lowest temperature and the one measured at the highest one (25 °C). The change in DCR is actually found to be the same regardless of the type of readout channel and of the SPAD active area.
The breakdown voltage was also evaluated, for the two kinds of detectors, at different temperatures. The breakdown voltage, extracted for each pixel, shows the same linear behaviour which was detected in the temperature tests performed before the neutron irradiation. The temperature coefficients have been extracted from the curves in Fig. 3.28, showing the breakdown voltage as a function of the temperature after the exposure to neutrons at the largest fluence. For the DPD kind of sensors, a temperature coefficient of 29 mV/°C was obtained, which is comparable with the one extracted before neutron irradiation (24 mV/°C). In the case of the DPH sensor, a temperature coefficient of 18 mV/°C was extracted, very close to the one extracted before exposure to neutrons (19 mV/°C).
As a conclusion, temperature tests performed on the chip exposed to the largest fluence feature a considerable decrease in terms of dark count rate



(a)



(b)

Figure 3.28: breakdown voltage variation for DPD (a) and DPH (b) sensors as a function of temperature.

when the temperature is lowered, as expected. The effects of the temperature can also be appreciated for the breakdown voltage, which decreases with decreasing temperature. Finally, neutron irradiation does not seem to affect the temperature coefficient, which does not change significantly in irradiated devices as compared to pre-irradiation results.

3.3 Chapter related work

- L. Ratti, P. Brogi, G. Collazuol, G.-F. Dalla Betta, A. Ficorella L. Lodola, P.S. Marrocchesi, F. Morsani, M. Musacci, et al., "CMOS SPAD sensors for particle tracking exposed to ionizing and non-ionizing radiation ", Conference on Radiation Effects on Components and Systems (RADECS 2017), Geneva, Switzerland, from 2 October to 6 October 2017

- M. Musacci, G. Bigongiari, P.Brogi, C. Checchia, G. Collazuol, et al., "Radiation tolerance characterization of Geiger-mode CMOS avalanche diodes for a dual-layer particle detector ", 14th Pisa Meeting on advanced detector, from 27 May to 2 June 2018, La Biodola, Isola dElba, Italy

- L. Ratti, P. Brogi, G. Collazuol, G. F. Dalla Betta, A. Ficorella, L. Lodola, P.S. Marrocchesi, S. Mattiazzo, F. Morsani, M. Musacci, et al., "Dark count rate degradation in CMOS SPADs exposed to X-rays and neutrons ", Transaction on Nuclear Science.

Chapter 4

APiX2: chip design

This chapter will discuss the design of a new chip, which is an evolution, in a different technology, of the one discussed in the previous chapter. The aim is to design, as mentioned in the first chapter of this thesis work, a position sensitive detector based on the coincidence signal produced when a particle simultaneously strikes two overlapping pixels on two interconnected SPAD layers. For this purpose, two sensor chips (named APiX2 Father and APiX2 Son) have been designed in such a way that they can be bump bonded on top of each other in order to make a dual-tier structure. Both chips can also be tested independently. The design explores new features relevant to in-pixel electronics, fill factor improvement and matrix complexity.

4.1 Chip overview

The APiX2 Father and Son chips were designed in a standard 150 nm CMOS technology. The Father and Son chip dimensions are 6 mm $\times$ 5 mm and 5.4 mm $\times$ 5 mm respectively. They both share the same electronics from a layout design point of view. Father and Son chips have been designed as the mirrored version of each other in such a way that they can be vertically integrated into a two-layer detector. Once they are bump bonded, all the input signals, the reference and supply voltages and the sensor bias voltages will be provided to the Father chip and delivered to the Son chip through the bump bonding contacts. Coincidence output signals will be also made available by the Father chip. As the two chips have virtually identical layout, they can be tested using the same characterization setup. As an example, the layout of the APiX2 Son chip is shown in Fig. 4.1.
The whole array is divided into four sub-matrices, listed in the following:

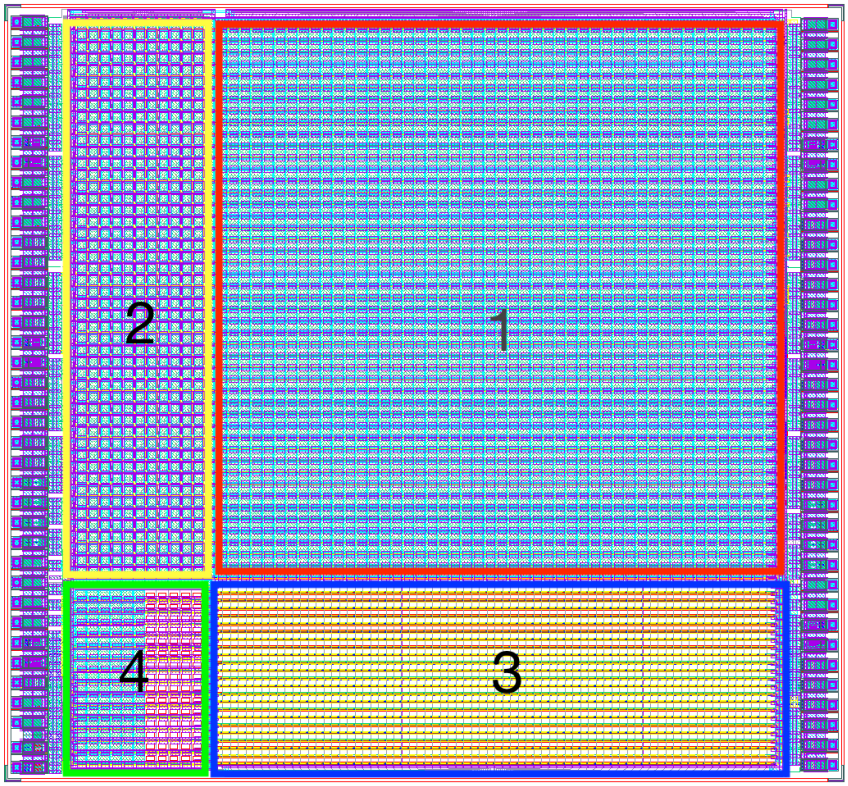


Figure 4.1: layout of the APiX2 Son chip.

- array 1: 48 × 48 square pixels with a 75 μm pitch, 1 bit memory architecture;
- array 2: 12 × 48 square pixels with a 75 μm pitch and a 10 bit ripple counter architecture;
- array 3: 24 × 72 square pixels with a 50 μm pitch, 1 bit memory architecture;
- array 4: 11 × 15 square pixels with a 75 μm pitch including different test

structures: active quenching front-end electronics, pixels with different sensitive area and different process splitting.

The pixel selection of a sub-matrix is performed by programming dedicated row and column shift registers (Fig. 4.2). Each array is powered separately from all the other. Therefore, each section of the chip can be tested with all the other sections off. Moreover, the SPAD cathode voltages (V_{SPAD}) can be set independently for the different matrices. The chip design has been carried out in such a way to improve and maximize the fill factor in the arrays 1, 2 and

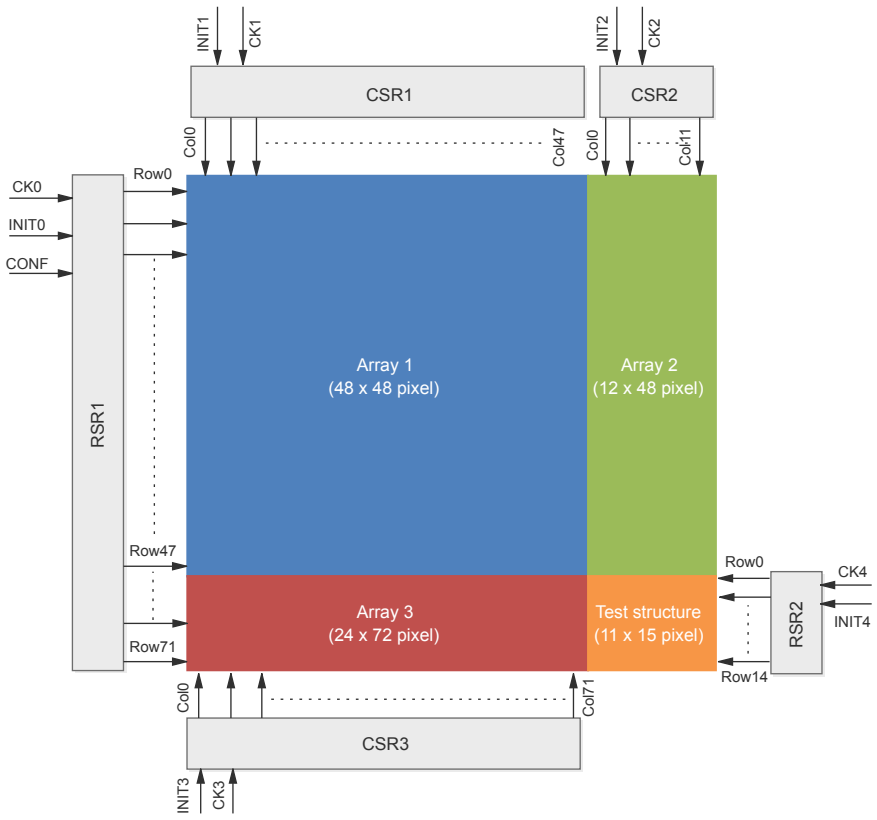


Figure 4.2: pixel selection of the APiX2 chip.

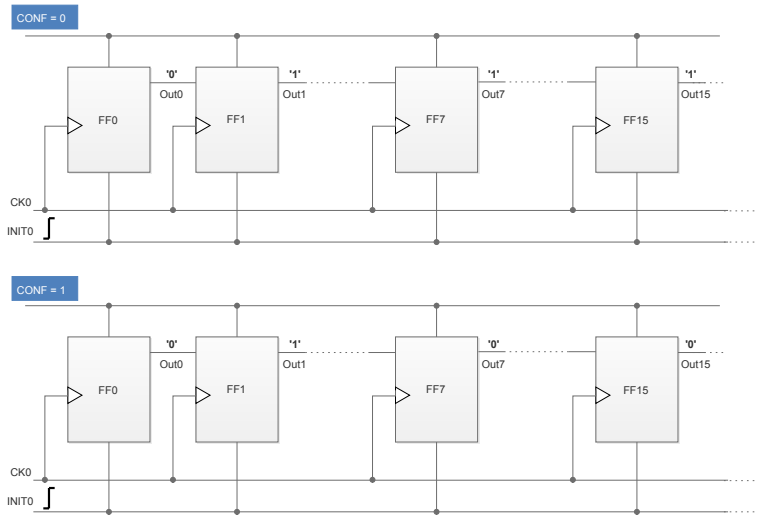


Figure 4.3: row shift register 1 initialization based on the CONF signal.

Chip section	Row selection	Column selection
Array 1	RSR1	CSR1
Array 2	RSR1	CSR2
Array 3	RSR1	CSR3
Test structure	RSR2	CSR2

Table 4.1: shift registers for pixel selection in the APiX2 SPAD array.

3. In particular, a fill factor of 66% was reached in the array 1, whereas a fill factor of 44% and 39% was obtained in the array 2 and 3 respectively. A more detailed description of the readout electronics is provided in the following.

4.2 Pixel selection and enabling

Each pixel in the chip can be individually enabled or disabled by an external slow control signal (EN). As already mentioned before, the arrays have dedicated row (RSR) and column (CSR) shift registers, which can be initialized and controlled independently. The shift register length depends on the size of the sub-matrix the shift register is used with. As shown in Fig. 4.2,

five different shift registers are included in the chip to perform as flexible as possible a pixel selection. RSR 1 can be used to select rows in the arrays 1, 2 and 3, while the other row shift register (RSR 2) is used for row selection in the test structure only. Due to the different pixel pitch, column selection in the sub-matrices 1 and 3 is performed by two independent CSRs. All the shift registers can be initialized with an external INITx (where x=0, 1, 2, 3, 4, depending on the shift register) signal setting to "0" the output of the first flip-flop in the shift register chain and to "1" the outputs of all the other cells. A pixel is selected when the corresponding cells in the column and row shift registers are set to 0. RSR 1 has two initialization signals (INIT0 and CONF) which can be used to perform single pixel selection or multiple pixel selection. In particular, if CONF is set to zero and INIT0 has a low to high transition, then only the output of the first FF is set to zero (the output of all other cells being set to one). On the other hand, if the CONF signal is set to one and INIT0 has a low to high transition, one cell every eight is set to zero, as shown in Fig.4.3 (all the other being set to one). This latter configuration can be used to perform a parallel reading of the array. Before selecting any pixel, a global reset operation is needed. Once the pixel which we are interested in is selected, an enabling operation has to be performed to allow the electronics to store events. The logic circuit implementing this operation, including a negative edge triggered latch, is shown in Fig. 4.4. As soon as the EN (active high) signal is sent, the latch output is set to one and the pixel is enabled. In order to disable it, an external global reset signal is needed (ENRB, active low).

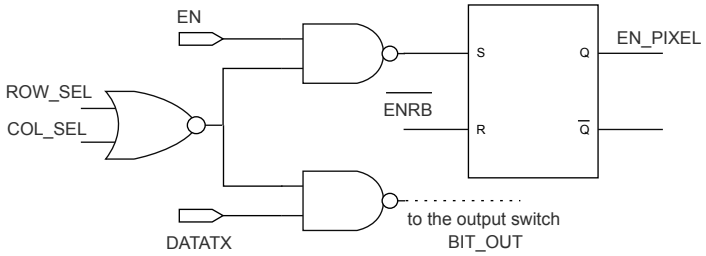


Figure 4.4: pixel selection and enabling circuits.

4.3 Front-end electronics

The APiX2 chip, featuring a relatively large area and improved fill factor, also includes cells with different readout structures such as cells with a single bit memory, cells with a 10-bit ripple counter and cells with active quenching circuits (whereas most of the SPADs in the chip are based on a passive quenching operation). In all of the cells, once the avalanche takes place, a pulse with programmable width is provided by a monostable circuit. Moreover, each channel is provided with an external test terminal, enabling the test of the readout circuits. The arrays adopting the fast readout electronics (arrays 1 and 3) have been designed to perform parallel pixel reading up to 100 MHz. The 10-bit ripple counter structure has been designed so that it can be operated also in a rolling shutter mode, in which the array is read out column by column. This readout method is usually implemented in CMOS sensors. The advantage is that, while one column is being read out, all the other sensitive elements continue collecting photons.
In test structure sub-matrix, a portion of the array has been reserved to pixels with an active quenching readout channel, in which the off-time of the single photon avalanche diode can be programmed. A more detailed description of the front-end electronics is provided in the following subsections.

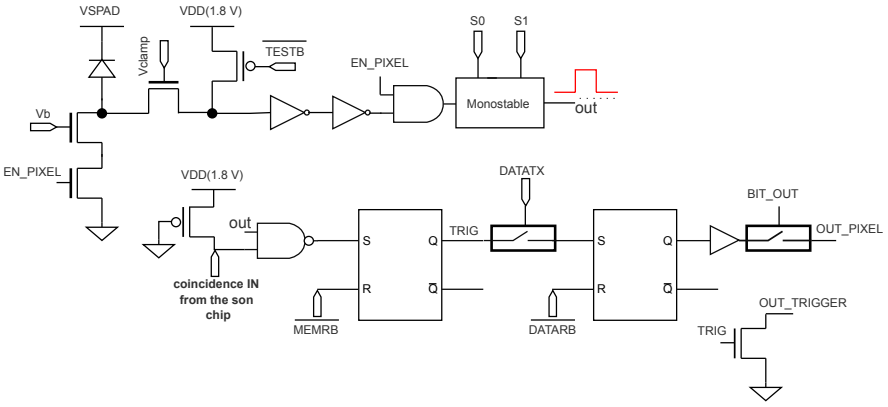


Figure 4.5: block diagram, with some transistor detail, of the 1-bit fast readout in the father chip.

4.3.1 1-bit memory cell

The complete block diagram of the circuit for the 1-bit memory cell is shown in Fig. 4.5. After the SPAD fires, the anode is discharged through a constant current source. The transistors used in the readout channel are all core devices (V_{DD}=1.8 V), except for the current source performing the quenching operation and the transistor used to adapt the signal level from the sensor to the inverters, which have a thicker oxide (V_{DD}=3.3 V). Threshold crossing is detected through a custom designed inverter, with a transition threshold larger than VDD/2 (about 1 V). Before running this part of the chip, the memory latch and the output latch have to be reset by means of the external signals MEMRB and DATARB (both active low). By acting on the control bits S0 and S1, the time duration of the signal at the monostable circuit output can be set to 400 ps (S0 = 1, S1 = 0), 750 ps (S0 = 0, S1 = 1), 2 ns (S0 = 1, S1 = 1) or configured in a transparent logic mode (S0 = 0, S1 = 0), in which

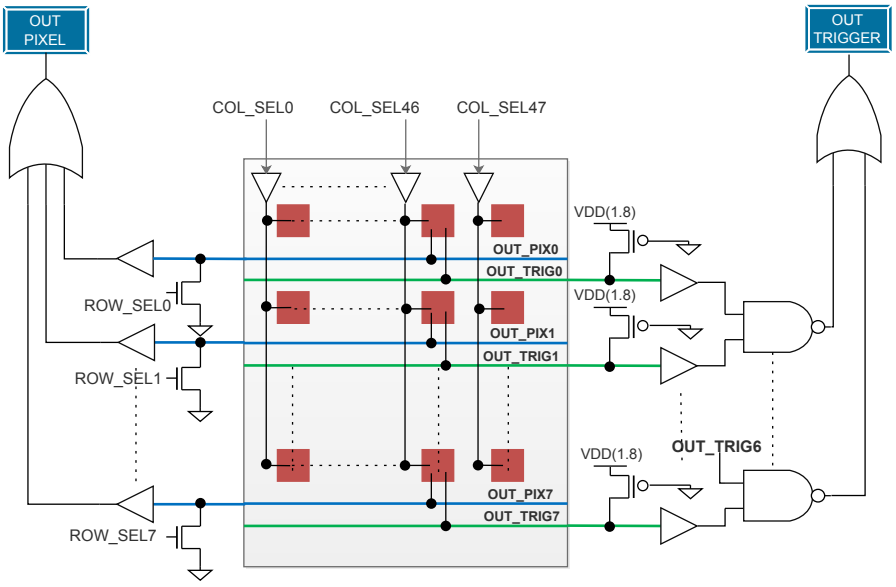


Figure 4.6: processing the pixel output (OUT_PIX) and trigger signals from 8 adjacent rows.

the signal at the comparator output (output of the two cascaded inverters) is directly sent to the output. The coincidence detection is performed by a NAND gate on the Father chip. As it can be noticed in Fig. 4.5, one input of the NAND gate is weakly pulled up by a PMOS transistor, whereas the other input is connected to the monostable circuit output. The pull-up transistor makes it possible to keep one input of the gate high so that the Father chip can be tested also as an individual layer, not connected to the Son.
All the pixels in the same row, as shown in Fig. 4.6, share two different buses. One is dedicated to the transmission of the stored bit of information and is accessible by one pixel at a time. The other bus is used for the trigger signal, which is generated when a coincidence signal is produced by at least one pixel belonging to that row. If a coincidence event is stored in the latch of one or more pixels, an NMOS pull-down transistor brings the trigger bus to a low state. Data transmission is performed by issuing a DATATX signal. Moreover, the rows which are not selected are kept to a low logic state by means of an NMOS pull-down transistor. The readout architecture shown in Fig. 4.6 is relevant to the sub-arrays 1 and 3. Each readout block includes 8 rows. The scheme in Fig. 4.6 is therefore repeated 9 times to cover the two sub-arrays, overall comprised of 72 rows. Since data and trigger buses are shared by pixels in eight adjacent rows, arrays 1 and 3 have overall 9 data output pads (6 for array 1, 3 for array 3, OUT[0;8]) and 9 trigger output pads (again 6 for array 1, 3 for array 3, TRIG[0;8]).

4.3.2 10-bit counter cell

The complete block diagram of the circuit for the 10-bit counter cells is shown in Fig. 4.7. The quenching operation and the coincidence detection are implemented using the same approach adopted in the pixels with fast readout electronics (arrays 1 and 3). The counter logic is able to detect up to 1024 coincidence events. The counter consists of a chain of ten D flip-flops. Its input becomes insensitive to coincidences in three particular cases:

- the counter control logic detects that the maximum number of events has been registered;
- the DATATX signal is provided to transmit the counter content to the output;
- the INTEG signal (active low), defining the integration time window for the detector, is high.

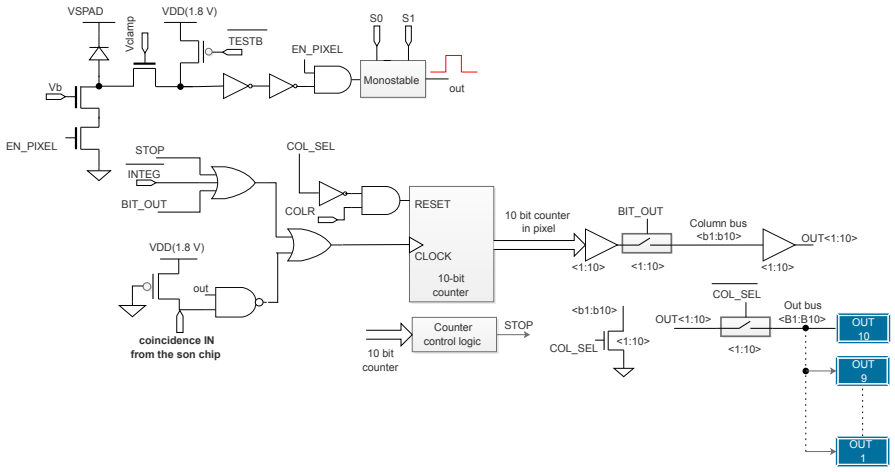


Figure 4.7: complete block diagram of the 10 bit counter front-end electronics in the Father chip.

In these cases, even if a coincidence signal is produced, the counter value is not changed. As mentioned before, array 2 can be operated in rolling shutter mode. In this case, the array is read out in a column by column fashion, with the pixels in each column being read serially (10 bits for each pixel). Once the column has been read out, the counters in the column are reset by means of the COLR signal. Fig. 4.8 shows the architecture of the 10 bit counter readout circuits. Pixel readout is performed by connecting one pixel at a time to the column bus, including 10 lines, one for each of the 10 counter bits. Only one column bus at a time is connected to the output bus by means of the *column selection* signal. The column buses which are not used are grounded by means of a set of pull-down NMOS transistors controlled by the *column selection* signal.

4.4 Test structures

A reduced portion of the chip is dedicated to the implementation of different test structures subdivided as follows:

- 5 × 15 pixels (colums 1 to 5 and rows 1 to 15): cells with different sensor

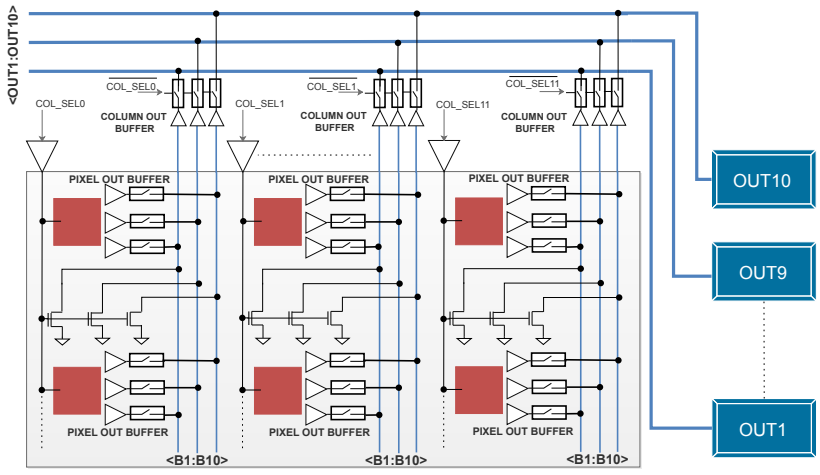


Figure 4.8: readout circuits for the 10-bit counter cells.

area;

- 6 × 7 pixels (columns 6 to 11 and rows 1 to 7): active quenching readout circuit;
- 6 × 4 pixels (columns 6 to 11 and rows 8 to 11): cells without cobalt layer;
- 6 × 4 pixels (columns 6 to 11 and rows 12 to 15): quenching front-end electronics with optimized timing.

Most of the designed cells in this sub-matrix adopt the 1-bit fast readout channel, which has been already discussed in the previous sections. In the sub-matrix dedicated to the active quenching readout channel (Fig. 4.9), avalanche detection is performed as in the passive quenching channel but, as an additional feature, the SPAD can be kept off for a given time interval (SPAD-OFF time) by acting on the SPOFF0 and SPOFF1 control bits of the monostable circuit 2. In particular, the sensor can be disabled for 70 ns (SPOFF0 = 0, SPOFF1 = 0), 90 ns (SPOFF0 = 1, SPOFF1 = 0), 110 ns (SPOFF0 = 0, SPOFF1 = 1) and 130 ns (SPOFF0 = 1, SPOFF1 = 1). The advantage of

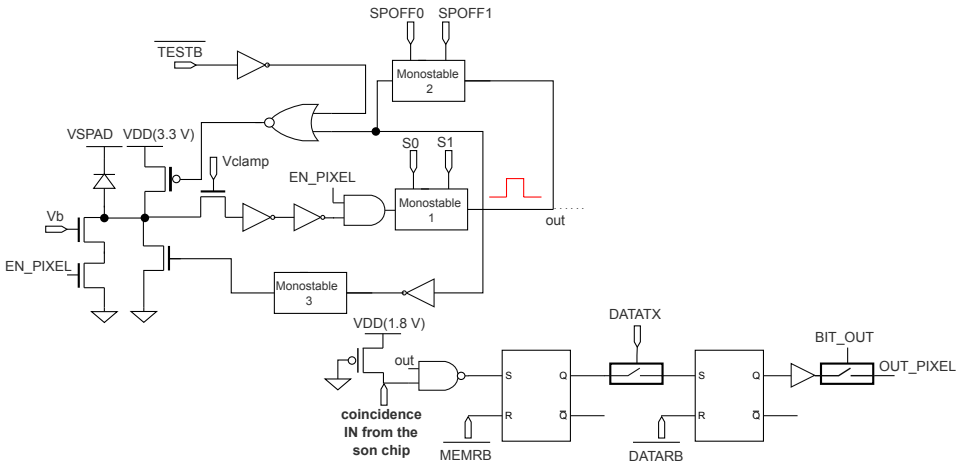


Figure 4.9: complete block diagram of a SPAD with active quenching front-end electronics form the test structure sub-array of the Father chip.

setting a well defined off-time is that of reducing the dark count pulse contribution related to the after-pulsing phenomenon. As already discussed in the first chapter of this work, after-pulsing strongly depends on the number of carriers captured during an avalanche, on the delay of the quenching operation and on the current intensity. The longer the off-time interval, the less probable after-pulsing is. At the end of the off-time interval, the SPAD anode is quickly discharged by means of an NMOS transistor controlled through the monostable circuit 3. Also in this configuration, an NMOS transistor is used to adapt the avalanche signal to the electronics implemented with core devices (V_{DD}=1.8 V). The readout of the sub-matrix is performed pixel by pixel by connecting the single cell to the row transmission bus, the logic OR of all the row buses being sent to the output pad.

4.5 Chip operation and typical signal time diagrams

Timing signals are provided for the different readout channels implemented in the chip in order to better understand their operation. In all the diagrams it is assumed that the monostable1 output duration have already been set and

the TEST signal is not active.

4.5.1 Passive quenching

Time diagrams in Fig. 4.10 are provided in order to understand how the 1-bit fast readout architecture works and how the selected pixel is enabled. A reset phase is mandatory before shift register configuration for pixel selection. In particular, with reference to the portion of the chip adopting this front-end topology (array 1 and 3), time diagrams in Fig. 4.10 are relevant to the selection of the first pixel in the rows of the sub-array. In Fig. 4.10(a) the CONF signal is set to zero and only the shift register initialization signals are provided without any clock signal. In this way, as mentioned in the previous section, a low logic state is set at the output of the first flip-flop (whereas the other outputs are set to one) therefore selecting the first pixel in the first row. The case of pixel selection with the CONF signal set to one is shown in Fig. 4.10(b). In this configuration, the outputs of the shift register cells are simultaneosly set to a low logic state every 8 flip-flops (all the other outputs being set to one), therefore performing a multiple pixel selection in the sub-array. In both cases, once the pixels are selected, the EN signal has to be provided in order to enable them.
The signal sequences, in the case of CONF = 0, to select and enable different pixels belonging to the same column or row are displayed in Fig. 4.11. Each CLK_ROW and CLK_COL pulse changes the selected row and the selected column, respectively.
Once the desired pixel is enabled, it is ready to store a single hit in the memory latch. The data transmission procedure is represented in Fig. 4.12. As soon as a photon strikes the detector of the selected pixel, the trigger bus is brought to a low level by means of the memory latch output which turns on the pull-down transistor. In order to restore the initial condition and allow the pixel to store other events, a reset phase is needed after the data transmission.

4.5.2 Counter logic

In the sub-array implementing the counter logic, as already mentioned, the rolling shutter method can be used to read the pixels. In this case, the pixel selection should be performed by setting CONF = 0 and changing the row while the column is kept unchanged, as shown in Fig. 4.11. All the column pixels have to be enabled in this way until all are operative. A column counter reset (COLR) is necessary before starting in order to ensure a correct initialization of the pixels. The reset phase is shown in Fig. 4.13 together with the

signal time evolution relevant to the case in which the counter reaches its full state. In this situation, the control logic inhibits the counter input, therefore preventing overwriting. The counter input is kept blind to other coincidence events also in other two cases (Fig. 4.14). The input has to be inhibited in order to preserve data when data are being transmitted (this is done by sending the DATATX signal). When this occurs, as soon as the transmission is over, the counter may restart counting from the value stored before the DATATX signal, unless it is disabled or reset. Moreover, by means of the external INTEG signal (active low), it is possible to define a time window during which the number of hit can be counted. In particular, when this signal is kept to a high level, the counter is made unable to register events.

4.5.3 Active quenching

Active quenching front-end is used in a sub-array of the test structure portion. As an additional feature with respect to passive quenching readout, the option of choosing the time in which the sensor is kept off is made available. Timing signals for active quenching readout are shown in Fig. 4.15. After the negative edge of the pulse at the monostable1 output, the monostable2 provides a programmable signal (the duration is set through the control bits SPOFF0 and SPOFF1) turning on the pull-up transistor that keeps the SPAD anode to 1.8 V therefore preventing the avalanche. When the sensor off-time is over, the monostable3 circuit generates a pulse with a fixed duration (about 2 ns) which very quickly discharges the anode in order to restore the SPAD operating point. The coincidence signal is stored and transmitted as in the already discussed passive quenching front-end.

4.6 Bonding diagram

For the test phase, the Father and the Son chips have been packaged in a CPGA144 (*Ceramic Pin Grid Array*) with removable taped lids. A photograph of the Son chip bonded in the package mentioned above is provided in Fig. 4.16. The Father chip has also been packaged in the same way. Fig. 4.17 and Fig. 4.18 show the bonding diagrams of the Father chip and of the Son chip respectively.

4.7 Pin description

The pin description for both the Son and the Father chips is shown in Table 4.2.

Table 4.2: Pad list

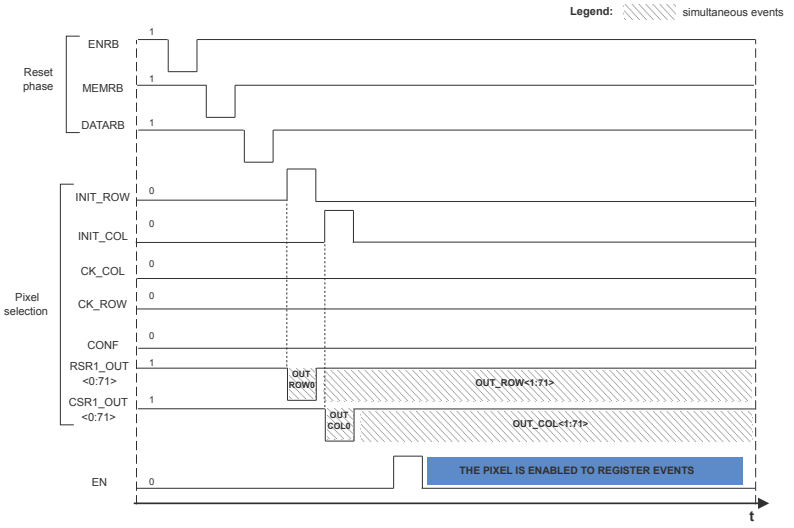
Pad no.	Name	Function	Comment
1	INIT1	Digital input	Column shift register 1 initialization signal
2	CK0	Digital input	Row shift register 1 input clock
3	INT0	Digital input	Row shift register 1 initialization signal
4	CONF	Digital input	Row shift register 1 configuration signal
5	EN	Digital input	Enable pixel input
6	VDDIO1	Power	1.8 V for I/O circuits
7	GNDIO1	Power	GND for I/O circuits
8	DATARB	Digital input	Output latch reset signal (active low)
9	MEMRB	Digital input	Memory latch reset signal (active low)
10	OUT0	Digital output	Bit0 pixel output
11	TRIG0	Digital output	Trigger0 pixel output
12	OUT1	Digital output	Bit1 pixel output
13	TRIG1	Digital output	Trigger1 pixel output
14	OUT2	Digital output	Bit2 pixel output
15	TRIG2	Digital output	Trigger2 pixel output
16	VDDIO2	Power	1.8 V for I/O circuits
17	GNDIO2	Power	GND for I/O circuits
18	OUT3	Digital output	Bit3 pixel output
19	TRIG3	Digital output	Trigger3 pixel output
20	OUT4	Digital output	Bit4 pixel output
21	TRIG4	Digital output	Trigger4 pixel output
22	OUT5	Digital output	Bit5 pixel output
23	TRIG5	Digital output	Trigger5 pixel output
24	VDD1	Power	1.8 V for circuits in the array 1
25	GND1	Power	GND for circuits in the array 1
26	GND3	Power	GND for circuits in the array 3
27	VDD3	Power	1.8 V for circuits in the array 3
28	VSPAD1	SPAD bias	external bias source for SPADs in the array 1
29	VSPAD3	SPAD bias	external bias source for SPADs in the array 3
30	VDDIO3	Power	1.8 V for I/O circuits
31	GNDIO3	Power	GND for I/O circuits
32	OUT6	Digital output	Bit6 pixel output
33	TRIG6	Digital output	Trigger6 pixel output
34	OUT7	Digital output	Bit7 pixel output

Table 4.2

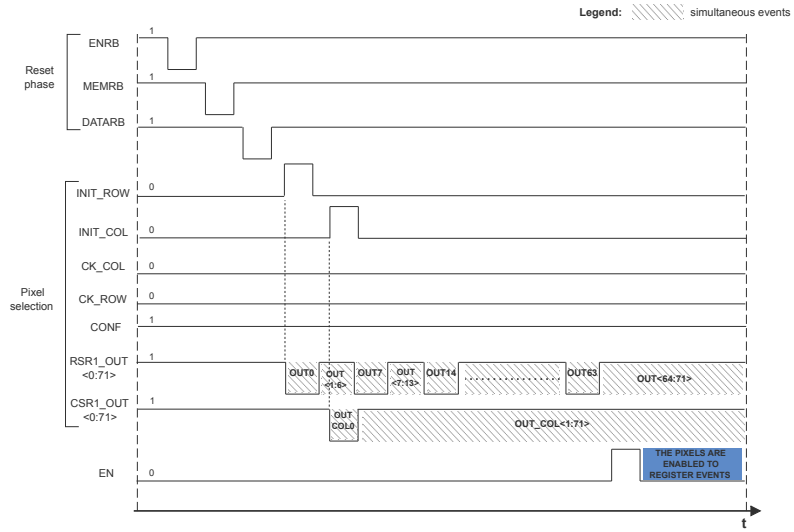
Pad no.	Name	Function	Comment
35	TRIG7	Digital output	Trigger7 pixel output
36	OUT8	Digital output	Bit8 pixel output
37	TRIG8	Digital output	Trigger8 pixel output
72	VDD33	Power	3.3 V for circuits in the test structure array
73	GND33	Power	GND for circuits in the test structure array
74	INIT3/INIT4	Digital input	Row shift register 2 and column shift register 3 initialization signals
75	CK3/CK4	Digital input	Row shift register 2 and column shift register 3 clock signals
76	OUTTS	Digital output	Test structure pixel output
77	GNDIO4	Power	GND for I/O circuits
78	VDDIO4	Power	1.8 V for I/O circuits
79	VSPAD4	SPAD bias	external bias source for SPADs in test structure array
80	VCLAMP	Voltage reference	transistor clamp voltage, 1.8 V
81	VQ	Voltage reference	quenching transistor reference, 1.8 V
82	VSPAD2	SPAD bias	external bias source for SPADs in the array 2
83	VDD4	Power	1.8 V for circuits in test structure array
84	GND4	Power	GND for circuits in test structure array
85	GND2	Power	GND for circuits in the array 2
86	VDD2	Power	1.8 V for circuits in the array 2
87	OUTC0	Digital output	Bit0 counter output
88	OUTC1	Digital output	Bit1 counter output
89	OUTC2	Digital output	Bit2 counter output
90	OUTC3	Digital output	Bit3 counter output
91	OUTC4	Digital output	Bit4 counter output
92	GNDIO5	Power	GND for I/O circuits
93	VDDIO5	Power	1.8 V for I/O circuits
94	OUTC5	Digital output	Bit5 counter output
95	OUTC6	Digital output	Bit6 counter output
96	OUTC7	Digital output	Bit7 counter output
97	OUTC8	Digital output	Bit8 counter output
98	OUTC9	Digital output	Bit9 counter output

Table 4.2

Pad no.	Name	Function	Comment
99	INTEG/SPOFF1	Digital input	Counter logic integration signal and SPAD off control bit1
100	COLR/SPOFF0	Digital input	Counter column reset signal and SPAD off control bit0
101	TESTB	Digital input	Test signal (active low)
102	GNDIO6	Power	GND for I/O circuits
103	VDDIO6	Power	1.8 V for I/O circuits
104	ENRB	Digital input	Enable reset (active low)
105	DATATX	Digital input	Data trasmission signal
106	S1	Digital input	Output pulse duration control bit1
107	S0	Digital input	Output pulse duration control bit0
108	INIT2	Digital input	Column shift register 3 initialization signal
109	CK2	Digital input	Column shift register 3 clock signal
144	CK1	Digital input	Column shift register 1 clock signal



(a)



(b)

Figure 4.10: timing signals for pixel enabling in the case of CONF = 0 (a) and CONF = 1 (b).

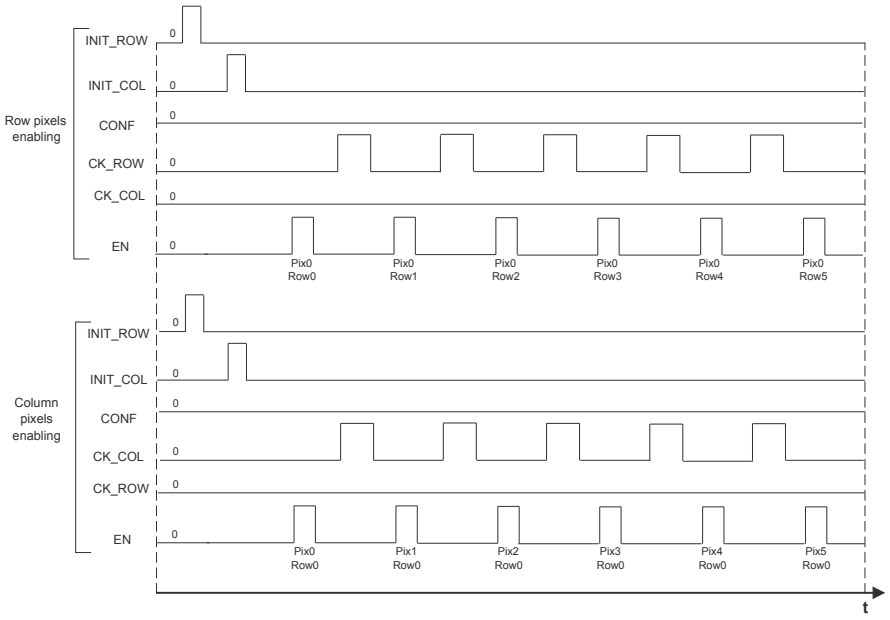


Figure 4.11: timing signals for pixel selection.

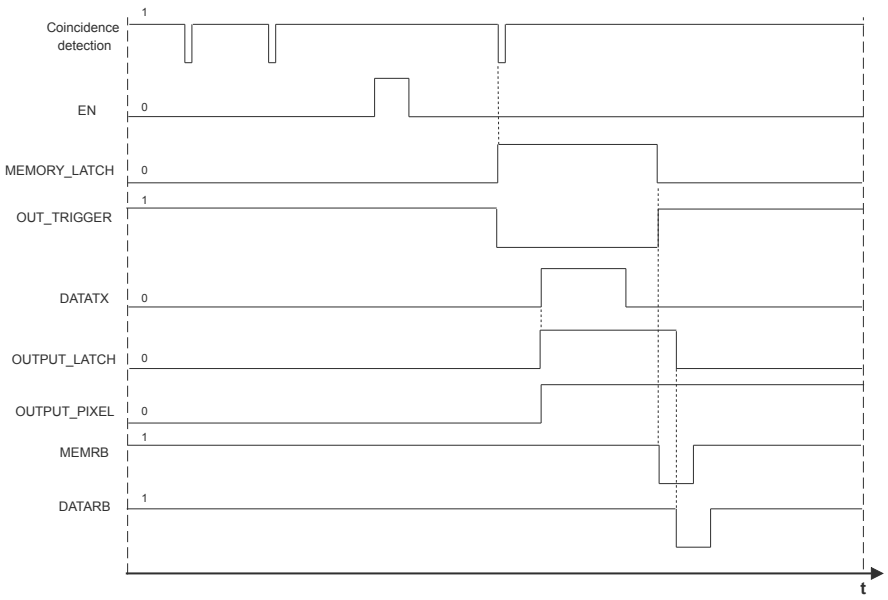


Figure 4.12: timing signals for pixel readout (1-bit memory architecture).

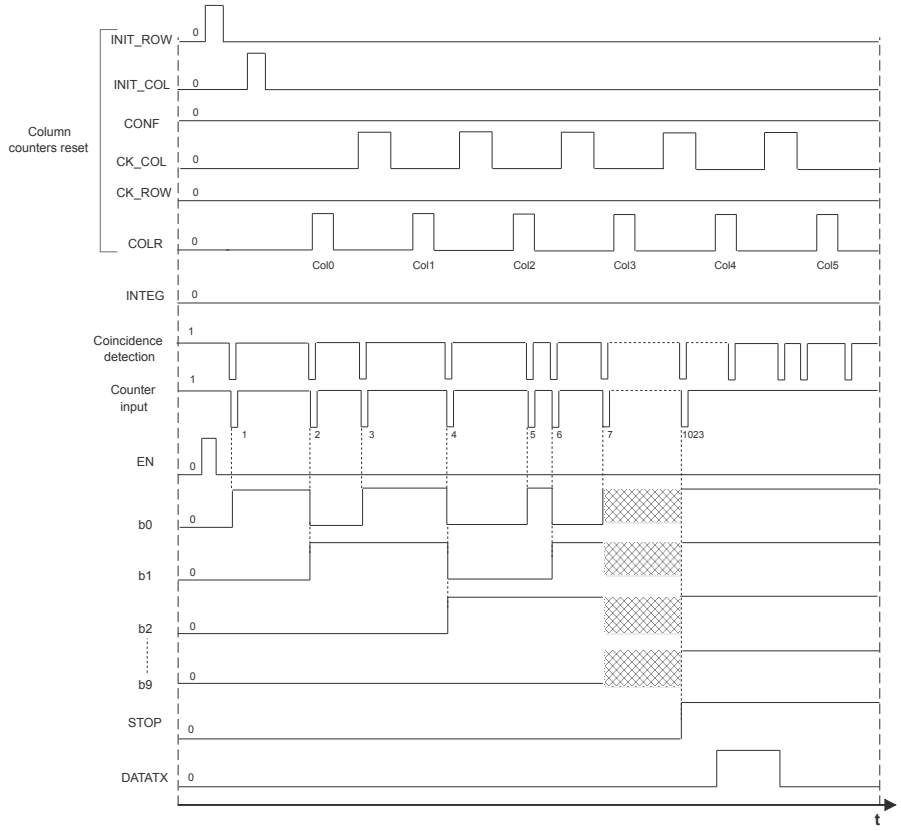


Figure 4.13: timing signals for column counter reset and data trasmission in the case of full state counter.

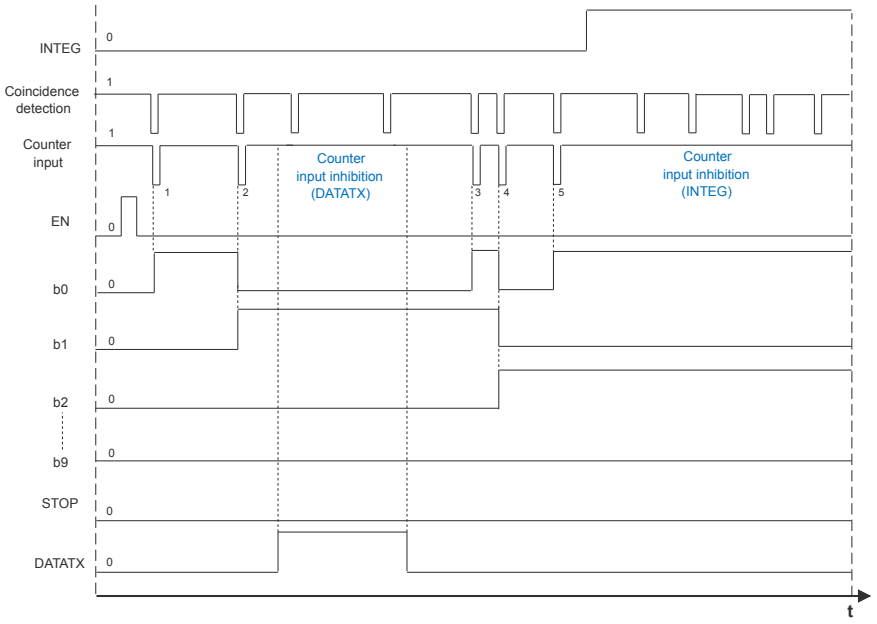


Figure 4.14: timing signals relevant to counter input inhibition.

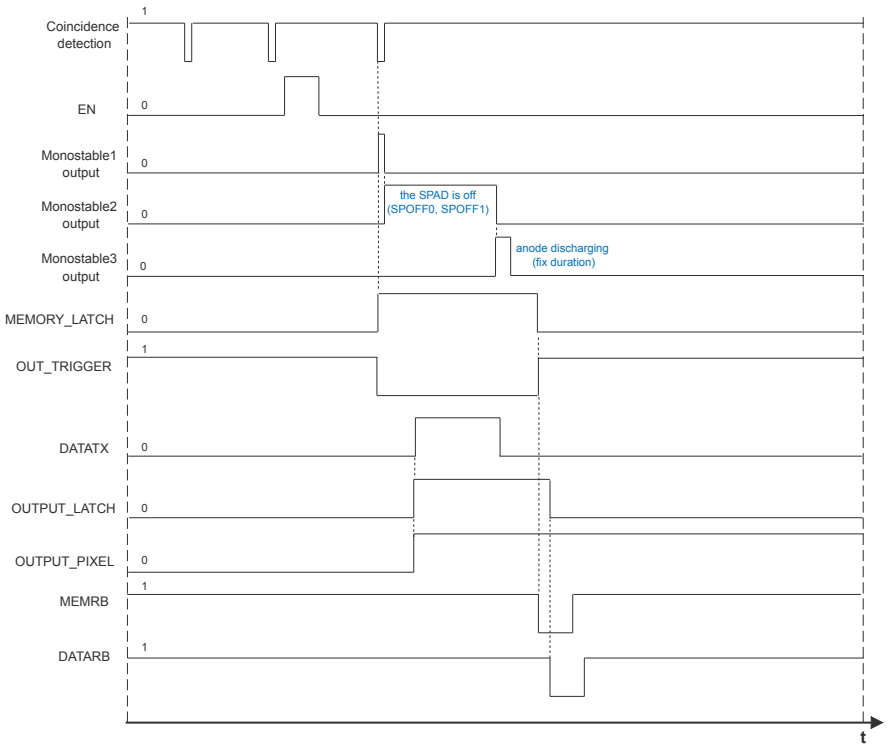


Figure 4.15: timing signals for the active quenching readout.

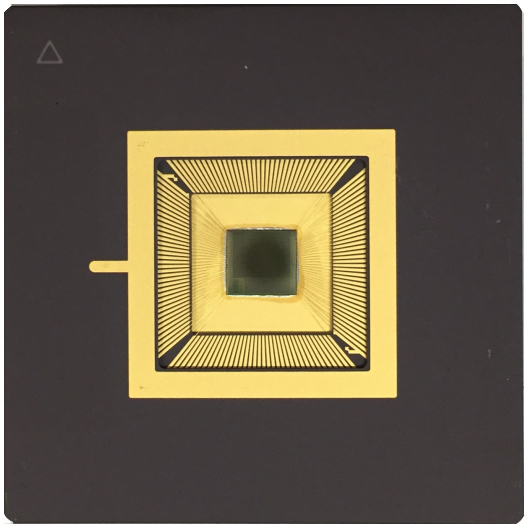


Figure 4.16: APiX2 Evo Son chip in a CPGA144 package.

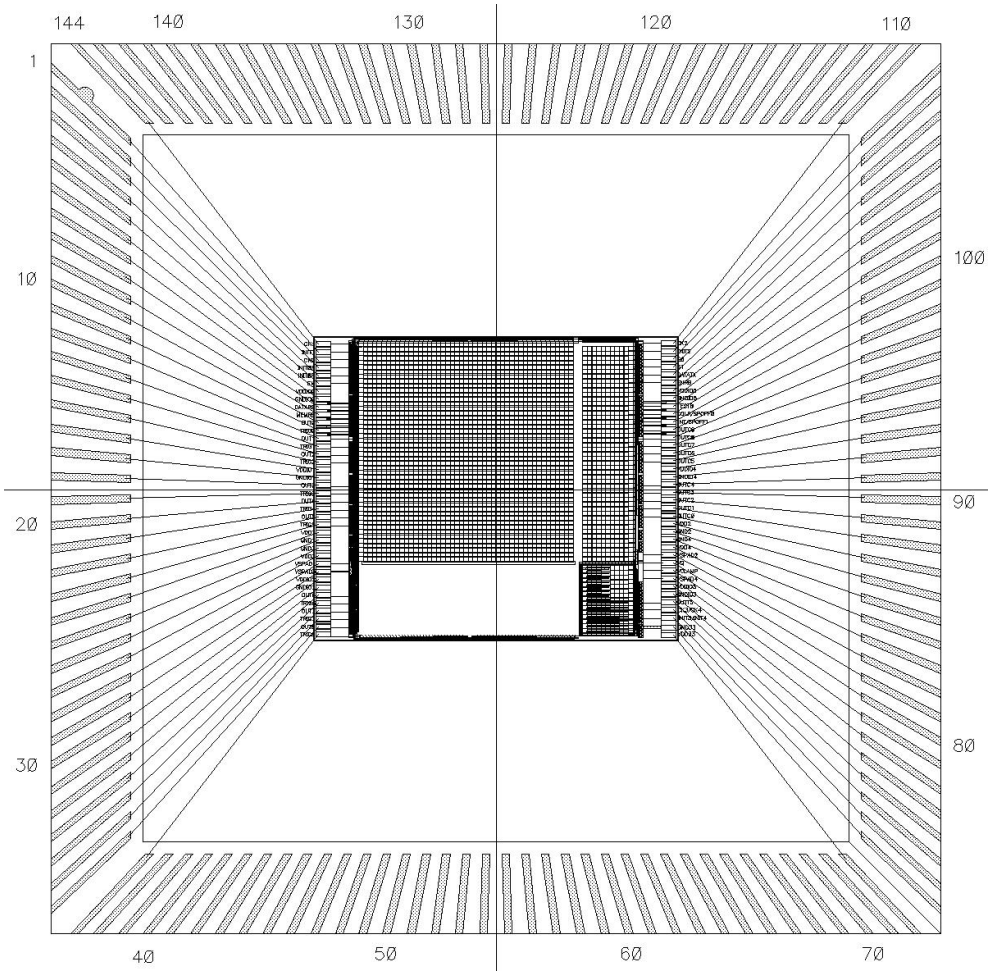


Figure 4.17: bonding diagram of the APiX2 Father chip in a CPGA144 package.

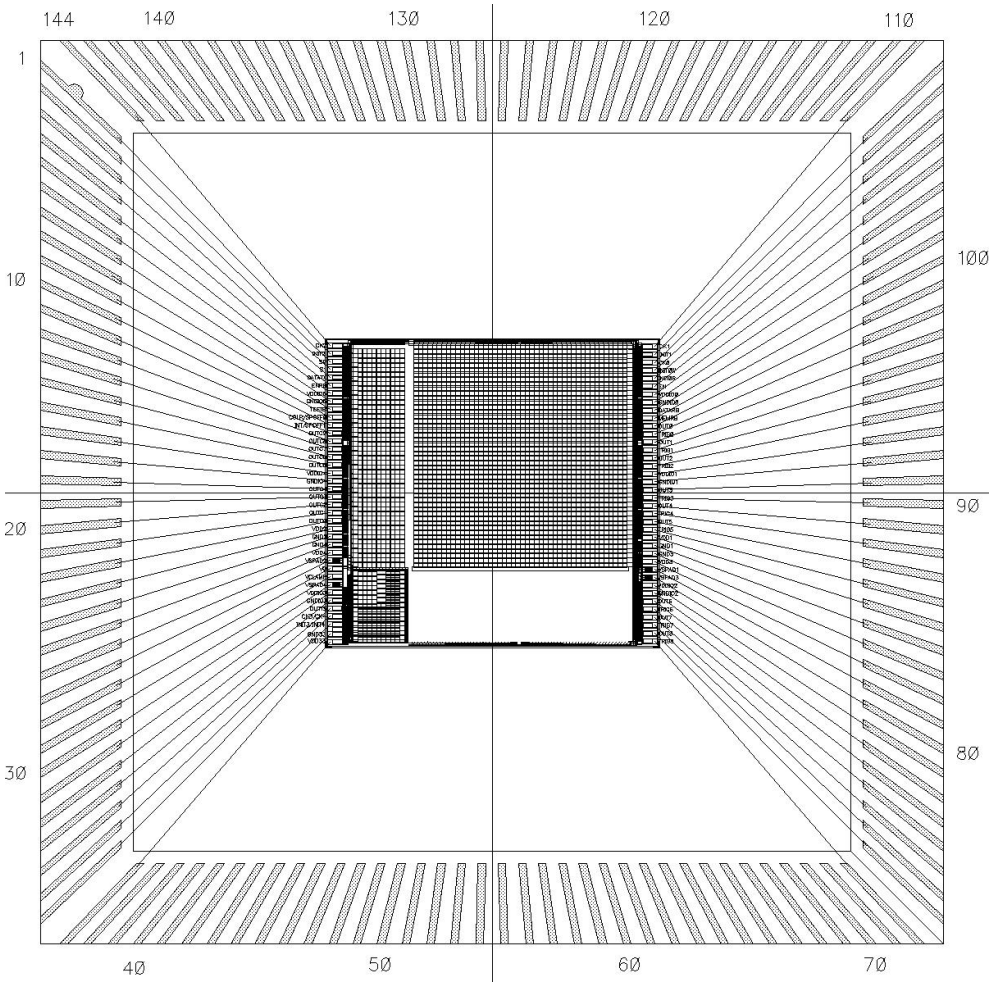


Figure 4.18: bonding diagram of the APiX2 Son chip in a CPGA144 package.

Conclusions

In this thesis work, the design of the APIXFAB0 chip, fabricated in a 180 nm CMOS technology, and its characterization in terms of dark count rate (DCR) and breakdown voltage, have been presented and discussed together with the main features of a newly designed, large scale SPAD array fabricated in a 150 nm CMOS technology. Ionizing and non-ionizing radiation effects on SPADs in the 180 nm CMOS technology have also been evaluated. Both chips have been designed in the framework of the APiX2 project, aiming at the development of a dual-tier charged particle detector based on single photon avalanche diodes read out in coincidence.
The characterization of the APIXFAB0 chip has been performed by means of a fully automated microcontroller based measurement system which is used to initialize the internal registers and configure the readout electronics, control the bias voltage which is applied to the sensor, select pixels inside the array structure and process the data. In this way, a thorough characterization of the different structures implemented in the test vehicle has been carried out. The tests were performed over a number of samples in order to collect a statistically meaningful set of data. The measurements performed on SPADs with different internal structures showed that the choice of the technology layers may have a remarkable impact on the device performance, even when a single process step is changed or added. The DCR as a function of the bias voltage has been evaluated and found to exhibit a different behaviour when different front-end electronics architectures are considered. In particular, the detectors combined with the active quenching, inverter based readout channel exhibit a higher dark count rate as compared to the case of the passive quenching, comparator based front-end circuit. This is likely due to the shorter off time obtained in the active quenching configuration and to the larger bandwidth of the designed inverter circuit than that of the comparator. Both kinds of tested sensors, called DPD and DPH in this work, were found to feature a good breakdown voltage uniformity. Tests performed in a climatic chamber showed that the average value of the dark count rate is almost reduced by half

for every 10 °C reduction.
Some test vehicles were irradiated using ionizing and non-ionizing radiation sources at the Physics and Astronomy Department of the University of Padova and at the INFN Laboratori Nazionali di Legnaro. In the ionizing radiation tests, the final total ionizing dose was 1 Mrad(SiO_2). No significant breakdown voltage variations, whereas the average DCR was found to increase sensibly due to radiation interaction with field oxides and radiation induced state density increase at the silicon dioxide/silicon interface. Also after exposure to different fluences of neutrons no substantial change in the breakdown voltage was detected. Dark count rate was instead found to sizeably increase, even by few orders of magnitude in chips irradiated with 10^{11} 1 MeV neutron equivalent cm^{-2}. The temperature tests performed on the irradiated chips confirmed the remarkable reduction of the DCR with decreasing temperature and the breakdown voltage dependence already detected in non irradiated chips. The post-irradiation temperature coefficients were measured to be very close to the ones extracted before the irradiation procedure.
A second test chip has been designed and fabricated in a 150 nm CMOS technology. The new chip is ready to be vertically integrated in a dual-layer structure implementing the coincidence logic. New features, such as pixels with different pitch (75 μm and 50 μm), in which single bit memory electronic or 10-bit counters are incorporated, have been included in the array. Moreover, the fill factor has been otpimized in some structures, with a maximum value of about 70%. The characterization of the new chip is ongoing. Preliminary tests show that the readout electronics is fully functional.
The future activity will be concerned with the complete characterization of the new SPAD array, including radiation induced damage study. Comparison with the results from the characterization of the SPAD array chip in 180 nm CMOS technology will provide indications on the best process for the development of a dual-tier, SPAD based charged particle detector.

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