UNIVERSITÀ DEGLI STUDI DI PAVIA

PH.D. COURSE IN MICROELECTRONICS

An Extended-Range Hybrid Analog-to-Digital Converter for Audio Applications

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Cycle XXXII

To my family

Acknowledgments

All glory be to the most praiseworthy who showered His countless blessings on me throughout the span of my life. With the prolific praise of the Owner of Honor, I desire to begin a limitless praise, with which He is pleased and I cite His own words; “All praise to Allah, the Lord of the worlds”. The Quran (39:75)

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Contents

List of Figures

Chapter 1

Introduction

1.1 Motivation and Background

Automotive industry is moving towards developing innovative technologies and integrated systems to meet the growing demands of the market for luxurious, safe, and smart vehicles. The advancement in semiconductor technology has aided in meeting these demands and plays an important role in developing new systems and solutions in each of the main areas of the vehicle such as powertrain, body electronics, comfort electronics and infotainment to provide better connectivity solutions, improve vehicle safety, and enhance in-vehicle user-experience . In-Vehicle infotainment (IVI) system combines information and entertainment in an integrated environment and has become an important element in all modern automotive systems. The in-vehicle infotainment market is expected to grow from USD 24.3 billion in 2019 to USD 54.8 billion by 2027, at a compound annual growth rate (CAGR) of 10.7%. during the forecast period [1].

The audio subsystem plays undoubtedly a key role in the automotive infotainment system. With the addition of more features and subsystems, the audio power pudgets are being pushed to the limits. So there is an increasing demand for providing high-performance, less-power hungry and cost-effective solutions for

audio systems. Main components of car audio system includes the radio or "head unit" that controls the entire system and generates the audio signal, amplifier that increases the strength of the audio signal so that it can drive the speakers that reproduce the sound. The audio spectrum is the audible frequency range at which humans can hear and spans from 20-20 kHz. Main goal of the audio amplifiers is the faithful reproduction of the input audio signals at the output with desired power levels and volume, but with very low distortion suppressing the in-band noise. Output power levels depend on the specific application ranging from *mW* in headphones, to a few watts in TV or PC audio, to tens of watts for "*mini*" home stereos and automotive audio, to hundreds of watts and beyond for more powerful home and commercial sound systems and to fill theaters or auditoriums with sound [2]. The Audio Amplifier Market is expected to grow from USD 3.4 billion in 2019 to USD 4.4 billion by 2024, at a CAGR of 5.6% during the forecast period [3].

A simple and straightforward solution is to provide the amplification through linear operation of the transistors where the output voltage is the amplified version of audio input. There are different reported techniques or topologies to provide this amplification phenomena and are categorized in terms of power dissipation or alternately the conversion efficiency. In Class-A amplifiers, the output transistor branch is constantly conducting the current for the entire cycle resulting in the flow of constant bias current, irrespective of the requirement of speaker. Good sound quality is achieved by this topology since there is least distortion but at the same it suffers from lowest efficiency of 20% and highest power consumption. Class-B topology eliminates the constant dc bias current in the output-stage transistors, conducting only for half the sinusoidal cycle in a push-pull manner. One transistor conducts only for positive current while the other only for negative currents. As a result the power dissipation is significantly reduced increasing

the conversion efficiency to a maximum of 50%. However this improvement in efficiency comes at the cost of linearity as it suffers from inferior sound quality due to cross-over distortion when the output-stage transistors are switching between "*on*" and "off" conditions. Class-AB technique provides a compromise between class-A and class-B [4, 5], by consuming a constant small bias current as compared to class-A but sufficient enough to prevent cross-over distortion. Both output devices conduct for more than cycle but less than full sinusoidal cycle, so the power dissipation is also between class-A and class-B limits. By reducing cross-over distortion this topology ensures better sound quality and usually achieves efficiency of 50% and at best can reach 78.5% [6]. One of the drawbacks of the CMOS class AB output stage is the limited output swing range due to headroom requirements. As compared to these above mentioned topologies using linear operation of transistors, Class-D amplifier consumes much less power with its output-stage transistors switching between "*on*" and "off" conditions to produce a train of voltage pulses. Class-D amplifiers can achieve efficiencies of 90-95%, so they are emerging as possible choice and are now being increasingly used in audio systems. "$MarketsandMarkets$" predicts that the overall class-D audio amplifier market is expected to reach USD 3.6 billion by 2024 from USD 2.3 billion in 2019 at a 9.5% CAGR [7]. This growth expected due to the increasing demand for consumer electronics and smart home devices, in-vehicle infotainment systems in automobiles, and a rise in demand for energy-efficient technologies or components in portable and compact devices. Figure. 1.1 shows the block diagram of the class-D amplifier. The input can either be in analog or digital format. The front-end of the amplifier consists of the modulator followed by the switching class-D stage. The output pulses are demodulated by a low-pass filter to reconstruct the input signal. This topology is discussed in detail in the following section.

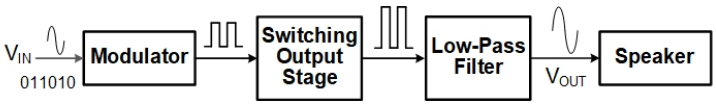

Figure 1.1: Class D open-loop-amplifier block diagram.

1.2 Class-D Audio Amplifier

A Class D audio amplifier operates in very much the same way as a switching amplifier or PWM amplifier. The switches are either fully on or fully off, significantly reducing the power losses in the output devices. The audio signal is used to modulate a PWM carrier signal which drives the output devices, with the last stage being a low pass filter to remove the high frequency PWM carrier frequency and harmonics.

1.2.1 Modulation Technique

Since class-D amplifier uses pulse modulation, where a sequence of high frequency pulses are generated in relation to the input. The two most common modulation technique used by class-D audio amplifier are pulse-width modulation (PWM) and Pulse-density modulation (PDM). In PWM, the audio signal is compared with a ramp or a triangular waveform running at a higher but fixed carrier frequency. This creates a stream of pulses at the carrier frequency, whose width is proportional to the amplitude of the audio signal. Figure. 1.2(a) shows a simple form of PWM technique also termed as natural sampling PWM (NPWM) [8] where the audio signal is compared with the triangular reference, and the output pulses are generated whose duty ratio is proportional to the input amplitude. Figure. 1.2(b) shows the PWM waveforms, where the red curve is the input analog sine wave and the blue curve represents the corresponding PWM output waveform.

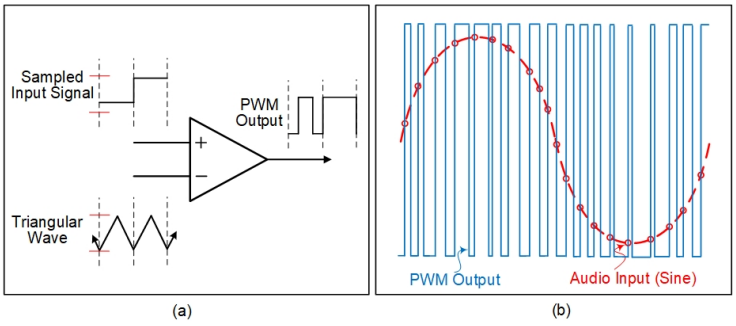

Figure 1.2: Conceptual block diagram of PWM and output waveform.

In comparison to PWM where the frequency of the pulse remain fixed, PDM also generates the stream of pulses whose density or the number of pulses in a given time is proportional to the amplitude of the audio signal. Fig. 1.3 shows a sample of the difference in the output pulse generated by PWM and PDM. Delta-Sigma modulation is a form of PDM and can be used in class D amplifiers. Depending on the oversampling ratio, the output pulses are quantized and the quantization noise is shifted to higher frequencies outside of audio band termed as noise shaping. The quantization noise decreases with increasing the oversampling ratio but at the same time the switching frequency also increases introducing switching noise. Figure. 1.4 shows the PDM waveforms, where the red curve is the input analog sine wave and the blue curve represents the corresponding PDM output waveform.

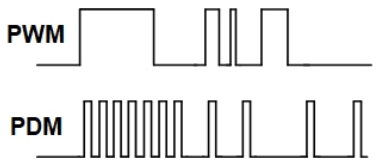

Figure 1.3: Comparison of output waveforms of PWM and PDM.

PWM is preferred because of lower switching noise as compared to PDM. Under the same conditions and clock rate, PWM has a much lower toggling rate, with

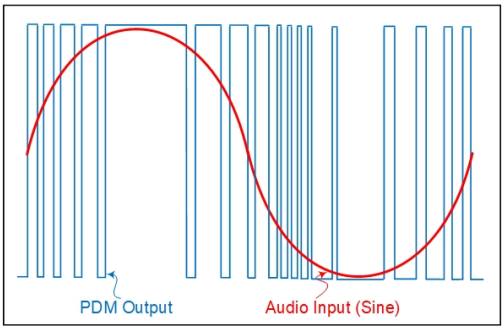

Figure 1.4: PDM output waveform in reference to analog sine wave.

fewer transitions during any given period of time, thereby reducing the impact of switching errors and dynamic power. Typically PWM modulator frequency is in the order of a few hundred kilohertz and allows 100-dB or better audio-band SNR in this range, while for PDM the sampling frequency is in the order of 100 MHz, being the root cause of higher switching losses in the output stage and higher power consumption. Another advantage of PWM amplifiers is their ability to maintain their stability up to nearly 100% modulation in some cases [8]. However PWM modulation also introduces distortion and harmonics of its carrier frequency adds EMI in the signal band, so a proper compensation and shielding is required for the speaker to minimize these unwanted frequency components. At the design level, the compensation for EMI is provided by phase staggering, frequency hopping, and AD/BD modulation [9, 10]. In addition, near full modulation the output pulse widths become too narrow causing problems for most switching output-stage gate-driver circuits that require accurate switching with very small widths at much higher frequencies. The subsequent analysis and discussion of class-D amplifiers uses only PWM for modulation.

1.2.2 Switching Output Stage

The modulated signal is amplified by the class-D switching output stage. The performance of class-D amplifier is highly dependent on the quality of this output stage. Although there are variety of techniques to amplify the modulated signal but most class-D amplifiers use half-bridge and H-bridge (full-bridge) configuration. The basic components in both configurations are MOSFETS,connected in a single-ended or differential configuration. Figure. 1.5(a) and (b) shows the schematic of output stage with both half-bridge and full-bridge configuration respectively. The full-bridge configuration uses more components, consumes more power and requires more control but have the advantage of eliminating even harmonics and DC offset because of its differential architecture [6]. For better efficiency and output power, these output power transistor devices generally have large widths, thereby increasing the parasitic capacitance [11]. These big transistors can't easily be driven by the comparator, so a gate-driving circuitry is needed to drive these transistors and ensure proper amplification by the output transistors. The efficiency of these output transistors primarily depend on the current provided to the load over time along with with other parameters that further reduces the efficiency. The optimized power efficiency of the output stage can be estimated by the following equation [12]

$$\eta = \frac{P_{out}}{P_{out} + P_s + P_c + P_r} \tag{1.1}$$

where P_{out}, P_s, P_c, P_r, are the output power delivered to the load, P_s is the power dissipated due to short-circuit current during transitions, P_c is the power dissipated due to the parasitic capacitance of large output transistors and P_r is the power dissipated by the on-resistance of the output transistors.

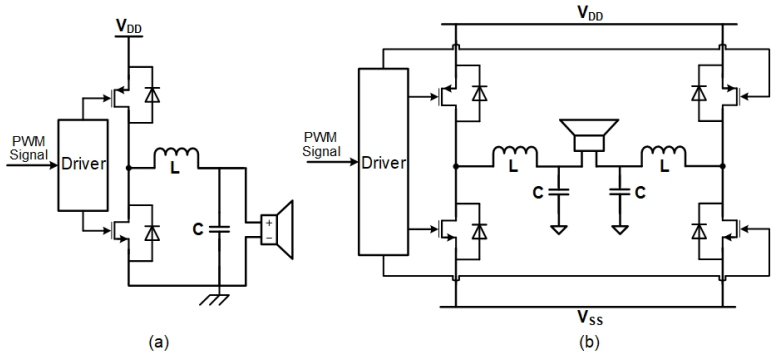

Figure 1.5: Output Stage with single-ended and differential configuration.

1.2.3 Demodulation and Filtering

Class D amplifiers are extremely susceptible to noise, as the modulation of the signal adds noise to the system which is further amplified by the output stage, so there is a need to introduce some filtering mechanism. The amplified PWM signal is generally passed through a low-pass filter to reconstruct the audio signal that serves as an input to the speaker. This low-pass filter removes the carrier frequency and high frequency components. If the high frequency components or in-band noise is not properly filtered out, it severely degrades the quality of amplifier. High frequency components require high-order filters (≥ 2), hence complicating the design. However this complexity can be traded with higher power consumption by increasing the switching frequency. Another issue with the filter design is its high sensitivity to the load variations. The impedance of the speaker is a function of frequency and can change to different values. Since the filter is designed for a specific load, load variations change the properties of the filter. Both passive and active filters can be used at the output. Passive filters use passive components i.e., resistors, inductors and capacitors and have very small losses associated with them, making them suitable for these audio applications. Active filters generally use resistors and opamps, complicating the design and increasing power

consumption and contribute more losses. However they are more accurate than their passive counterparts. The choice of the filters can be made depending on the efficiency of the system and accuracy requirements of the filter. Another option is to completely eliminate the LC filter, as inductor usually covers much space and adds much cost to the system especially in low-power applications. So a filter-less amplifier can be employed without any low-pass filtering [13, 14]. However EMI and high-frequency power dissipation increase to a high level, which could be minimized to some extent by using inductive speaker, placing the speaker in close vicinity of the amplifier and keeping the current-loops minimal.

1.2.4 Analog vs Digital class-D Amplifiers

The performance of class-D amplifiers is judged by their efficiency. Both analog class-D [15–20] and digital class-D [21–23] topologies are employed as a solution to reproduce the audio input signal and are specified as analog and digital class-D amplifiers.

A digital class-D amplifier receives a digital input $x(n)$ from its source, usually in a linear pulse code format which is digitally converted into a Pulse-Width Modulation (PWM) format. The Pulse Width Modulator then produces a high voltage signal which is filtered to replicate the original audio signal. Analog-input Class D amplifier normally requires a digital-to-analog converter (DAC) to convert into an analog signal before modulating it and then fed to the output stage for further amplification. Unfortunately, this adds die cost, power, and noise to the speaker output. These Class D amplifiers also require careful board design to avoid degradation because of signals coupling onto the analog board routes [24]. Digital-input class-D audio amplifiers are preferred because of their simpler architecture and exhibit superior performances with respect to traditional PWM analog class-D amplifiers. Generally digital class-D amplifiers are used for low-power audio

applications, however they require Analog to Digital Conversion (ADC) in the feedback to compensate for Jitter, signal distortions and power supply noise [25]. Conventionally Analog-input class-D amplifiers are used for high fidelity requirements for the input audio signal to be reproduced. Figure. 1.6 illustrates both solutions to reproduce the audio input signal at the speaker.

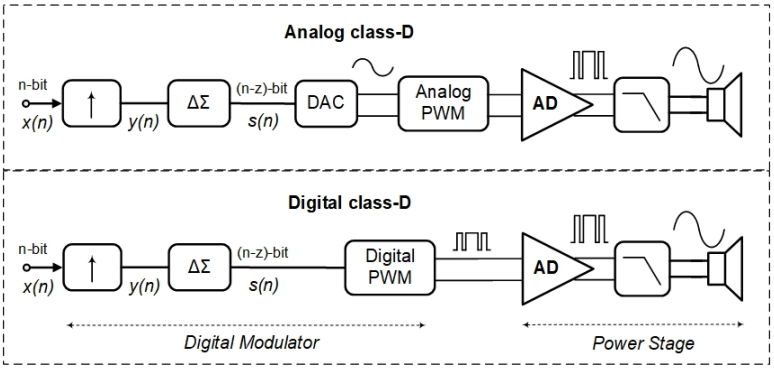

Figure 1.6: Analog and Digital solutions for class-D.

For both analog-input and digital-input class-D amplifiers, in order to create a bit stream for the output power stage, PWM signal is generated by the pulse generator based on the switching instances calculated by the sampling process. But achieving the required accuracy of the pulses is generated is quite difficult in digital PWM. One way is to use a counter to count to each switching instant, but it would require a very fast system clock. For instance, in order to sweep all the levels of 24-bit digital input word $x(n)$sampled at audio bandwidth, the minimum required frequency of PWM is given by

$$F_{PWM} = 2^n \cdot F_S = 2^{24} \cdot 48 \cdot 10^3 = 805\ GHz \tag{1.2}$$

Clearly achieving such a high frequency by the modulator in CMOS process is impossible. One solution is using a combination of a counter and a tapped delay-line which makes it possible to generate pulses with higher resolution, not

limited by the system clock [26]. Another solution is employing $\Delta\Sigma$ modulator, to quantize the input to a reduced bit-depth and through noise shaping, shift the quantization noise away from the audio band and then use a counter to produce the PWM signal [27].

1.3 Research Objectives

Since the real audio signal is in analog format, it requires an interface to convert the audio signal into a high resolution digital audio input for class-D amplifier. The performance of class-D amplifier (both analog and digital) can be enhanced, improve flexibility and made user-friendly, if an analog input-support is added eliminating the need of high resolution digital audio input. Main focus of this thesis also involves incorporating a high resolution ADC at the front-end of class-D amplifiers to

- provide analog input support to class-D audio amplifiers
- reduce the minimum required frequency of the PWM modulator

To achieve this research objective, a survey of high resolution ADCs for audio bandwidth is carried out. Conventionally $\Delta\Sigma$ ADCs have been used in audio applications because of their low-bandwidth requirements and high-medium resolution. Recently there has been a trend in using other topologies and introducing hybrid designs to take advantage of rapid growth in semiconductor technologies. In this thesis, same approach has been used and a novel hybrid architecture has been proposed by combining incremental and $\Delta\Sigma$ ADC operating sequentially targeting a dynamic range of $\geq 100\ dB$.

1.4 Thesis Organization

The thesis is organized into seven chapters as follows:

Chapter 1 gives an introduction of audio applications, class-D audio amplifiers and a brief overview of the problem. The chapter includes motivation and background of the research followed by the research objectives of this thesis.

Chapter 2 introduces ADC architectures and some basic performance metrics used to evaluate the ADCs. A detailed introduction and background of $\Delta\Sigma$ and Incremental ADCs, that are relevant to this thesis work is presented. The chapter also provides a survey and review of state-of-the-art high resolution ADCs for audio applications.

Chapter 3 introduces the proposed solution of hybrid ADC for the target audio applications that includes both incremental and $\Delta\Sigma$ ADC. Main topologies and details of the proposed solution is also discussed aided with block diagrams.

Chapter 4 presents the Matlab/Simulink model developed to validate the functionality of the proposed solution. In the first case an ideal simulink model is presented which is followed by the introduction and modeling of non-idealities including KT/C, Finite gain, slew rate and sampling jitter and their impact on the performance of proposed ADC is also discussed. The effect of mismatch in the feedback D/A converters is investigated and the compensation technique to mitigate its effect is also discussed.

Chapter 5 demonstrates the transistor-level implementation of the proposed Hybrid incremental-$\Delta\Sigma$ ADC. The chapter discusses the design of op-amps, Capacitive DAC elements, multi-bit quantizer and its compensation, other supporting blocks and their simulation results of both incremental and $\Delta\Sigma$ ADCs. One-step chopping and boostrapped switching logic is also discussed to compensate for flicker noise and switches non-linearity respectively.

Chapter 6 presents the measurement results of the prototype chip fabricated in

BCD9 process. The measurement results demonstrates the performance of the fabricated design along with other parameters including dynamic range, power consumption, SNDR. A tabulated comparison is also made with other reported ADC architectures for the same application.

Chapter 7 concludes the dissertation and suggests future research directions.

Chapter 2

Design Techniques for high resolution ADCs

The chapter discusses different topologies and techniques of ADCs to achieve high resolution especially for low-frequency applications including audio, automotive and biomedical sensing. Some performance metrics are also discussed that are generally used to compare and analyze different ADC topologies. Based on the sampling frequency (f_S), ADCs can be classified into two main categories: Nyquist-rate and oversampling. For a continuous input of range [f_B,$-f_B$], the sampling frequency f_S should be maintained as [28]

$$f_S \geq 2f_B \tag{2.1}$$

In case of oversampling ADCs, the sampling frequency f_S of an oversampling ADC is much higher than the Nyquist-rate, typically ranging from 8 to 512 [29,30] or may be higher. The ratio of the oversampling frequency $f_{S,OSR}$, to the Nyquist-rate $2f_B$, is defined as the oversampling ratio (OSR). Figure. 2.1 shows the block diagrams of two ADCs, preceded by anti-aliasing filters (AAF). As shown, in case of oversampling ADC, the analog input is sampled at the rate of $f_{S,OSR}$, followed by an additional stage i.e. digital decimator that is used to decimate the output

signal back to Nyquist rate $f_{S,NYQ}$.

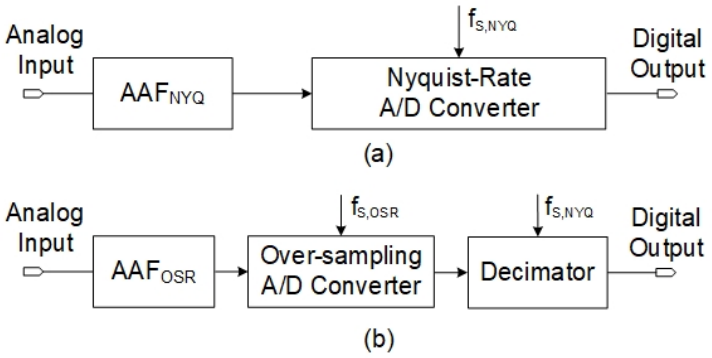

Figure 2.1: Functional block diagram of (a) Nyquist-rate and (b) oversampling ADCs.

Figure. 2.2 shows the anti-aliasing requirements for both techniques to remove the out-of-band noise and interferences, that can aliased into f_B due to the sampling process. For Nyquist-rate ADC, the aliasing frequency $f_S - f_B$ is very close to the signal band f_B, a high-order AAF with steep roll-off is required, as shown in Figure. 2.2(a). In contrast, for oversampling ADCs, the replicated spectra are far away from the signal and no frequency components of the range [f_B, $f_S - f_B$] can alias within the signal bandwidth up to f_B. As a result, the requirements of AAF are quite relaxed as it has much wider transition band with much less steep roll-off shown in Figure. 2.2(b). Since noise is removed from f_B to $f_S/2$, it has a major impact on the quantization noise by reducing its power with a factor of $f_S/(2f_B)$, leading to the following equation

$$V_{n,B}^2 = \frac{\Delta^2}{12} \cdot \frac{2f_B}{f_S} = \frac{V_{ref}^2}{12 \cdot 2^n} \cdot \frac{2f_B}{f_S} \tag{2.2}$$

where V_{ref} is the reference voltage, Δ is the LSB voltage and n is the number of bits of the quantizer. So the the quantization noise becomes independent of signal frequency [31].

The definition of the effective number of bits (ENOB) shows that oversam-

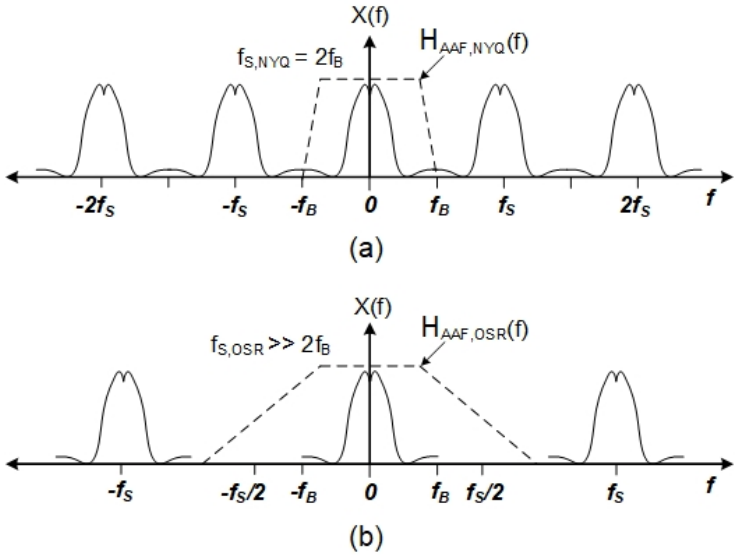

Figure 2.2: Antialiasing requirements of (a) Nyquist-rate and (b) oversampling ADCs.

pling by a factor OSR = $f_S/(2f_B)$ potentially improves the number of bits from n to

$$ENOB = n + 0.5 \cdot log_2(OSR) \tag{2.3}$$

One major advantage of oversampled ADCs over Nyquist-rate ADCs is the reduced circuit complexity and relaxed matching requirements in analog components. Nyquist-rate ADCs typically require strict matching of analog components to achieve higher resolution [32]. In case of oversampling ADCs, the additional digital processing compensates for the analog matching and complexity to some extent to achieve higher resolution. This trade-off compliments the trend of CMOS technology scaling, where it is easier to implement power- and area-efficient digital circuitry than high-resolution analog circuitry [33].

2.1 Performance Metrics

A large set of specifications describe the performance of data converters. Some specifications describe the features of either an ADC or a DAC, while others refer to the operation of both ADC and DAC. These specifications or performance metrics are generally divided into two main categories: Static which are time-independent and dynamic metrics which are time-independent and are usually analyzed in frequency-domain. The overall performance of different ADC designs is compared through variants of figure of merits (FOM).

2.1.1 Static Metrics

The static behavior of the ADC is illustrated by the input-output (I/O) transfer characteristics and is usually measured with DC or very-low frequency input signals. For an ideal case the input-output characteristic is a staircase with uniform steps over the entire dynamic range. Deviations from the ideal transfer characteristic are quantified through differential non-linearity (DNL) and Integral non-linearity (INL) as explained below.

Offset: the offset describes a shift for zero input. Offset is an error that can affect both an ADC and a DAC. The offset changes the transfer characteristics so that all the quantization steps are shifted by the ADC offset. The offset can be measured in LSB, absolute value (volts or amperes), or as % or ppm of the full scale.

Common-mode Error: is related to ADCs with differential inputs. It describes the change in the output code that occurs when the common-mode analog voltage changes by a given amount. The equal change of the two analog inputs that cause one LSB code transition is usually measured in LSBs.

Gain error: is the error on the slope of the straight line interpolating the transfer curve. For an ideal converter the slope is D_{FS}/X_{FS}, where D_{FS} and X_{FS} are the

full-scale digital code and full-scale analog range respectively. Since D_{FS} represents X_{FS}, so the ideal slope is one. The gain error defines the deviation of the slope of a data converter from the expected value. Another measure of the gain error is given by the difference between the input voltage causing a transition to the full scale and the reference (minus half LSB). When using this definition the gain error is known as the full scale error.

Differential non-linearity (DNL): is the maximum deviation of the step size of a real data converter from the ideal width of the bins Δ. Assuming that X_k is the transition point between successive codes $k-1$ and k, then the width of the bin k is $\Delta r(k)$ = (X_k+1 - X_k); the differential non-linearity is

$$DNL(k) = \frac{\Delta_r(k) - \Delta}{\Delta} \tag{2.4}$$

This function is also known as the differential linearity error (DLE). The maximum differential nonlinearity is the maximum of $|DNL(k)|$ for all k. Often the maximum differential non-linearity is simply referred to as *DNL*. The *DNL* is usually expressed in LSB, however it can also be measured in Volts (or Amperes when the input is a current) or as % or $p.p.m$ of the full scale. It measures how uniform the actual transfer function step sizes are. A large *DNL* contributes extra noise on top of quantization noise and raises the noise floor in the spectrum. A *DNL* that is greater than 1 LSB implies missing codes.

Integral non-linearity (INL): is the maximum deviation of the actual transfer function from the ideal transfer function for an ADC. Another definition of the integral non-linearity measures the deviation from the endpoint-fit line. The use of the endpoint-fit line corrects the gain and offset error. The second definition is chosen as standard since it is more informative for estimating harmonic distortion. The maximum of the *INL* is the maximum of $|INL(k)|$ for all k. Often, it is referred to as just *INL*. The *INL*, as for the *DNL*, is measured in LSB. An *INL*

that is larger than 0.5 LSB implies missing codes. It can also be measured using absolute value (Volts or Amperes), or as % or $p.p.m$ of the full scale.

2.1.2 Dynamic Metrics

The frequency response and speed of the analog components of a data converter determine its dynamic performance and are measured with time-varying input signals. The dynamic performance of ADC becomes critical when the input bandwidth and the conversion-rate are high. The dynamic performance is generally characterized by supplying a sinusoidal test signal at the ADC's input and computing its output as a function of frequency through the fast Fourier transform (FFT). A quality factor of a dynamic performance is its capability to remain unchanged within the entire range of dynamic operation.

Signal-to-Noise Ratio (SNR): is the ratio of between the power of the signal (normally a sinewave) P_{signal} and power of the total noise generated P_{noise} that includes quantization and noise of the circuit, but excluding the DC component and distortions. The *SNR* accounts for the noise in the entire Nyquist interval. The *SNR* can depend on the frequency of the input signal and it decreases proportional to the input amplitude. *SNR* is often expressed in decibel (dB) as:

$$SNR(dB) = 10log_{10}\frac{(P_{signal})}{(P_{noise})} \tag{2.5}$$

Signal-to-Noise-and-Distortion Ratio (SINAD or SNDR): is the ratio between the signal power and total noise generated excluding the DC component. It is similar in definition to *SNR* except that non-linear distortion terms are also included. Since static and dynamic limitations cause a non-linear response the *SNDR* is dependent on both the amplitude and frequency of the input sine wave. *SNDR* is also expressed in decibel (dB) as:

$$SNDR(dB) = 10log_{10} \cdot \frac{(P_{signal})}{(P_{noise} + P_{distortion})} \tag{2.6}$$

Spurious Free Dynamic Range (SFDR): is the ratio of the signal power to the highest spurious spectral component in the first Nyquist zone. The $SFDR$ provides information similar to the total harmonic distortion but focuses on the worst tone.

Dynamic Range: refers to the value of the input signal at which the corresponding *SNR* or *SNDR* is 0 dB. It is obtained by measuring the ADC's $SNDR/SNR$ variation with the input signal amplitude varied from the full-scale signal to the smallest detectable signal. This parameter is useful for some types of data converters that do not obtain their maximum $SNR\ (or\ SINAD)$ at 0 dBFS input which usually happens in sigma-delta converters.

Effective-Number-of-Bits (ENOB): indicates the ADC resolution by measuring the *SNDR* using bits. Using *SNDR* (dB), ENOB is expressed as:

$$ENOB = \frac{SNDR_{dB} - 1.76}{6.02} \tag{2.7}$$

Total Harmonic Distortion (THD): is the ratio between the total power of the harmonic components including aliased terms to the signal power of the fundamental frequency. Unless otherwise specified, THD accounts for the second through tenth harmonics: it is normally assumed that harmonic terms higher than the tenth have negligible effects. If f_{in} is the frequency of the input signal and f_S is the sampling frequency, then the $n-th$ harmonic component is at frequency $|\pm \mathrm{nf}_{in} \pm \mathrm{k}_{fs}|$, where k is a suitable number that folds the harmonic term into the first Nyquist zone. THD is also expressed in dB and is given by

$$THD(dB) = \frac{H_{D,2}^2 + H_{D,3}^2 + \cdots + H_{D,n}^2}{H_{D,1}^2} \tag{2.8}$$

A fully differential system makes the second harmonic negligible in the first two Nyquist zones. At high frequency the benefit of the fully-differential architecture vanishes and the second harmonic distortion becomes dominant [34].

Equivalent input referred noise: is a measure of the electronic noise produced by the circuits of the ADC. The result is that for a constant dc input the output is not fixed but there is a distribution of codes centered around the output code nominally encoding the input. With a large number of output samples the code histogram is approximately Gaussian. The standard deviation of the distribution defines the equivalent input referred noise. It is normally expressed in terms of LSBs or rms voltage.

Figure of Merit (FoM): is a parameter used to measure the power effectiveness of an ADC and is used as a tool to compare the performance of various ADCs which may differ widely in speed, resolution, and power consumption. FoM is used to measure the power efficiency of ADC with the assumption that the total power is consumed mainly because of the bandwidth of the converted signal (BW) and the equivalent number of bits (ENOB) and is expressed in $J/conv-step$. The Walden-FoM and Schreier-FoM are commonly used to compare the performance of ADCs. Walden FoM is given by:

$$FoM_W = \frac{P_{tot}}{2 \cdot 2^{ENOB} \cdot B.W} \tag{2.9}$$

while Schreier-FoM is commonly expressed as

$$FoM_S = DR(dB) + 10 \cdot log_{10} \frac{BW}{P_{tot}} \tag{2.10}$$

2.2 ADC Architectures

Different topologies of Nyquist-rate ADCs include Flash, Integrating, SAR and Pipelined ADCs that operate at the f_S which is either equal or slightly higher than $2f_B$. On the other hand, for oversampling ADCs an additional noise shaping phenomena is included through $\Delta\Sigma$ architecture. $\Delta\Sigma$ ADCs perform the memory-assisted operation [35] and the final output is obtained through digital filtering and decimation. Therefore, current output of the ADC depends on previous outputs and inputs. Another architecture that combines the properties of both Nyquist-rate and $\Delta\Sigma$ ADCs are Incremental ADCs. The incremental ADC achieves high-resolution due to oversampling being the property of $\Delta\Sigma$ ADCs, and sample-by-sample conversion due to periodical resetting of its memory elements being the property of Nyquist-rate ADCs. Table. 2.1 illustrates a summary of reported ADC architectures with their characteristics and targeted applications.

Architectures	**Speed**	**Resolution**	**Applications**
Flash	High	Low-Medium	RF & Microwave, Video, Telecom
SAR	Low-Medium	Medium	Biomedical, Control & Microcontrollers
Pipeline	High	Medium	RF & Microwave, Video
Cyclic	Medium	Medium	Control & Microcontrollers
Delta-Sigma	Low-Medium	Medium-High	Audio, Biomedical, Telecom
Incremental	Low	High	Instrumentation & Measurement

Table 2.1: Existing ADC architectures and their typical applications.

With the rapid advancement of technology and challenges in applications, an-

other trend that has found success is the combination of different architectures of ADCs termed as "*Hybrid Architectures*". These Hybrid ADCs are aimed to take the advantages of different architectures in a single model, albeit at the cost of higher power consumption, area and complex control logic.

In [36–44], the advantages of high-speed pipelined ADCs are combined with the oversampling and noise shaping of high resolution $\Delta\Sigma$ modulators, where in some techniques, the input signals are sampled at Nyquist rate and then oversampled in successive pipelined stage, while in some other techniques, the first pipeline stage is composed of multi-bit $\Delta\Sigma$ modulator followed by conventional pipelined stages. However these techniques consume excessive hardware and power consumption to properly avail the advantages of high speed and high resolution. Similarly in [45–49] continuous-time and discrete-time $\Delta\Sigma$ modulators have been combined with SAR ADCs for wide-band and audio applications. Because of the simpler architecture of SAR ADCs, these hybrid ADCs are less complex as compared to pipelined $\Delta\Sigma$ modulators. Recently the benefit of easier integration of SAR ADCs with advanced CMOS process is exploited by combining it with pipelined ADCs in a single hybrid architecture to achieve much higher speeds especially for telecommunication applications [50–54]. In [55–57] SAR ADC has been combined with Incremental ADC to achieve high resolution primarily for audio applications.

This thesis work is aimed at introducing design techniques to achieve high resolution A/D converters for audio applications. Conventionally, $\Delta\Sigma$ modulators with noise shaping and Incremental ADCs provide high resolution for small signal bandwidths, so the focus of the review and design is on $\Delta\Sigma$ modulators and Incremental ADCs which are discussed in following sections.

2.3 $\triangle\Sigma$ ADC

The $\Delta\Sigma$ ADC is the converter of choice for modern voice band, audio, and high-resolution precision industrial measurement applications. A $\Delta\Sigma$ ADC contains very simple analog electronics (a comparator, voltage reference, a switch, and one or more integrators and analog summing circuits), and quite complex digital computational circuitry. This digital circuitry consists of a digital signal processor (DSP) which acts as a filter (generally, but not invariably, a low pass filter). The $\Delta\Sigma$ technique, benefits from both oversampling and noise-shaping to give an optimum trade-off between speed and resolution.

2.3.1 Oversampling

As mentioned earlier, oversampling spreads out the quantization noise over a wider frequency band, so as to improve the *SQNR* in the band of interest. It is assumed that the quantization noise produced by $\Delta\Sigma$ is random and uncorrelated with the input signal. Figure. 2.3 shows the processing chain and the spectra obtained after each step of the $\Delta\Sigma$ modulator with oversampling. The scheme has a sampled-data input, with a bandwidth equal to f_B is oversampled by the A/D with sampling frequency equal to f_N = OSR $\cdot f_B$. As shown in Spectrum #1 the upper limit of this sampled analog signal is much lower than f_N. The oversampling A/D generates the quantized signal with a quantization noise spread over the entire Nyquist range as shown in Spectrum #2, however major portion of this quantization noise lies outside f_B as out-of-band noise; Spectrum #3 shows the effect of the digital filter which operates at the same frequency as of oversampling A/D and filters out the quantized signal by rejecting the Δf_R fraction lying in in the high-frequency zone. Spectrum #4, shows the effect of decimation reducing the output data rate, as required by the Nyquist theorem, f'_N.

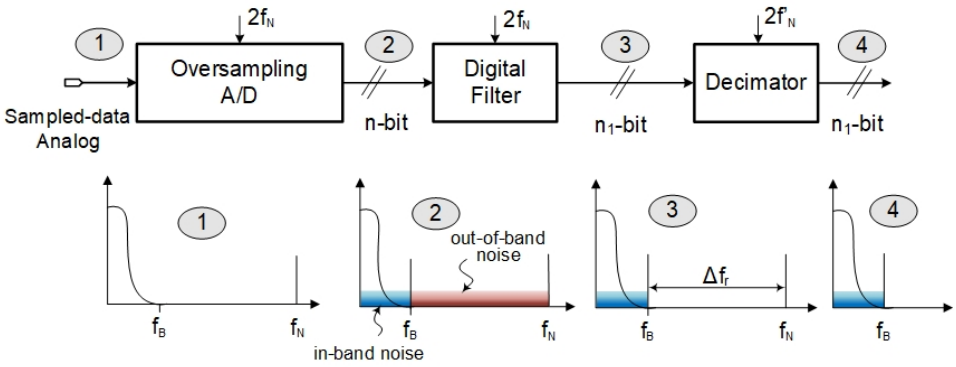

Figure 2.3: Out-of-band noise rejection and decimation of an over-sampled signal.

Although oversampling significantly relaxes the anti-aliasing filter requirements, but requires a very high oversampling ratio to achieve higher resolution. As previously shown by Eq:(2.3), a 1-bit improvement in the resolution requires increasing the OSR by a factor of 4, thereby increasing the power consumption and putting stringent speed requirements on oversampling A/D and digital filter to gain a small improvement in resolution. The oversampling method becomes more effective if the noise spectrum is lowered in the signal band, possibly at the expenses of an increase of the out- of-band portion, thereby changing the white spectrum of the quantization noise into a shaped spectrum. Having more noise in high frequency regions is not problematic as the digital filter used after the ADC (Figure. 2.3) removes it.

2.3.2 Noise-Shaping

The in-band noise reduction can be achieved by incorporating the quantizer in the feedback loop as shown in Figure. 2.4(a), termed as noise-shaping. Similar to the previous model, the scheme has a sampled data input that, after the processing block $A(z)$, is converted into digital format. For closing the loop it is necessary to generate the analog representation of the converted signal as done by the DAC. A

second processing block $A(z)$ is used before the subtracting element. The linear model of Figure. 2.4(b) represents the quantization error with the additive noise Q that is a second input of the circuit. Figure. 2.5 shows the processing chain and output spectrum with the introduction of quantizer in the feedback loop. As the output spectrum shows that the quantization error ε_Q is shaped and most of its power is pushed towards high frequency outside the signal band.

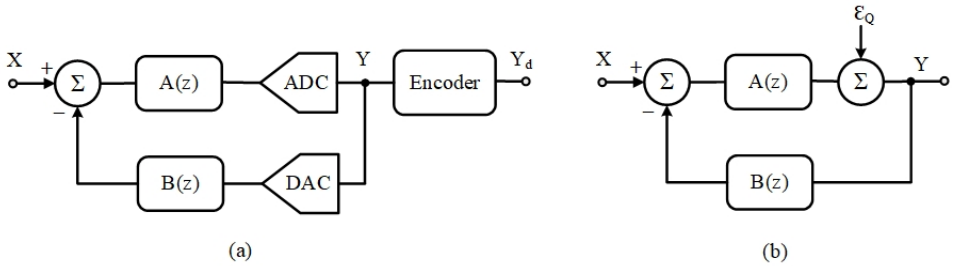

Figure 2.4: Insertion of quantizer in the feedback for noise-shaping.

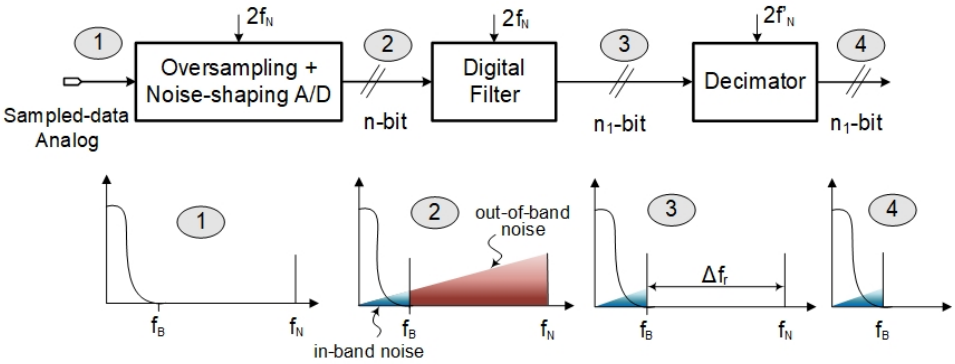

Figure 2.5: Out-of-band noise rejection and decimation of noise-shaped signal.

The goal of the system is to have different transfer functions for the input signal X and the noise signal ε_Q. These are namely Signal Transfer Function (STF) and Noise Transfer Function (NTF). By inspection of the scheme it results

$$[X - Y \cdot B(z)]A(z) + \varepsilon_Q = Y \tag{2.11}$$

The solution of this equation yields

$$\begin{aligned} Y &= \frac{X \cdot A(z)}{1 + A(z)B(z)} + \frac{\varepsilon_Q}{1 + A(z)B(z)} \\ &= X \cdot S(z) + \varepsilon_Q \cdot N(z) \end{aligned} \tag{2.12}$$

where $S(z)$ has low pass filter characteristics and $N(z)$ has high pass filter characteristics.

2.3.3 DT vs CT Modulation

The input of the modulator can be already in the sampled-and-hold format or a *S&H* is necessary before the data conversion. In the former case we have a discrete time (DT) $\Delta\Sigma$ modulator, while the latter case corresponds to a continuous-time (CT) $\Delta\Sigma$ modulator where the sampling operation takes place inside the loop. Fig. 2.6(a) corresponds to a DT implementation (DT-$\Delta\Sigma$ ADC) and Fig. 2.6(b) is a continuous-time (CT) implementation (CT-$\Delta\Sigma$ ADC). In both cases, low-pass signals are assumed to be processed. Otherwise, the filters involved must be changed from low-pass to band-pass transfer functions.

In case of CT implementation, the input signal could be fed either to AAF or directly to the modulator without preceding any filtering because the CT $\Delta\Sigma$M operation has the advantage of having an implicit anti-aliasing filter [58]. Since sampling occurs inside the loop, the sampling errors and non-idealities are also shaped by the loop reducing their impact. Moreover, the CT modulators are free from the kT/C noise. The loop filter coefficients are set by the product of a resistor and a capacitor value. However this product shifts dramatically with process variations and requires proper tuning to prevent the modulator becoming unstable. In addition, the CT modulators are also quite sensitive to the excess loop delay and jitter [59]. In DT modulators, the loop filter coefficients are set by the ratio of

capacitor values which are highly accurate in the presence of process variations. Therefore, DT $\Delta\Sigma$Ms offer advantages such as precise loop-filter coefficients and the insensitivity to the stray capacitances [60]. However to achieve high resolution, DT modulator requires large sampling capacitors. Driving large capacitors at high frequencies becomes problematic since it contributes significantly to the overall power consumption affecting the figure of merit (FoM).

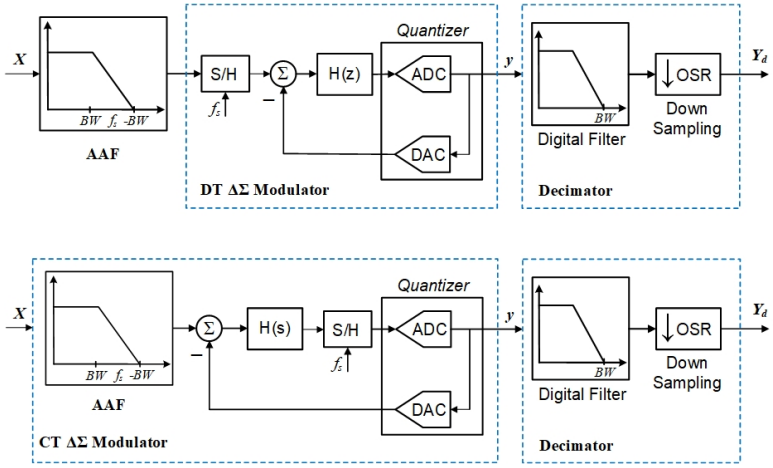

Figure 2.6: Block Diagram of (a) DT $\Delta\Sigma$ modulator (b) CT $\Delta\Sigma$ modulator.

2.3.4 Modulator Order and Multi-bit Quantizer

Considering the case of the first order sampled-data -$\Delta\Sigma$ as shown in Figure. 2.7 that uses the transfer function

$$A(z) = \frac{Z^{-1}}{1 - Z^{-1}} \tag{2.13}$$

leading to following definition of the circuit

$$Y(z) = X(z) \cdot Z^{-1} + \varepsilon_Q(z)(1 - Z^{-1}) \tag{2.14}$$

where STF = Z^{-1} and NTF = 1-Z^{-1}

The effect of the modulator is to introduce a simple delay to the input signal, while it can be proven that the noise signal is high-pass filtered. Besides, in [34] the maximum SNR of the first order $\Delta\Sigma$ modulator, in the case of an ideal filter that removes the out-of-band noise, is given as

$$SNR_{\Delta\Sigma|dB} = 6.02 \cdot n' + 1.78 - 5.17 + 9.03 log_2(OSR) \tag{2.15}$$

Where n'=$\log_2 k$, and k is number of thresholds used in the quantizer. The first term in the equation accounts for the SNR improvement due to a multi-level quantizer, while 5.17 dB is a fixed cost required to improve the SNR by 9.03 dB for every doubling of OSR. Accordingly, every doubling of the sampling frequency improves the ENOB by 1.5-bit which is given by

$$ENOB = n' - 0.86 + 1.5 log_2(OSR) \tag{2.16}$$

More complex architectures implement higher order modulators and achieve better enhancement in the SNR.

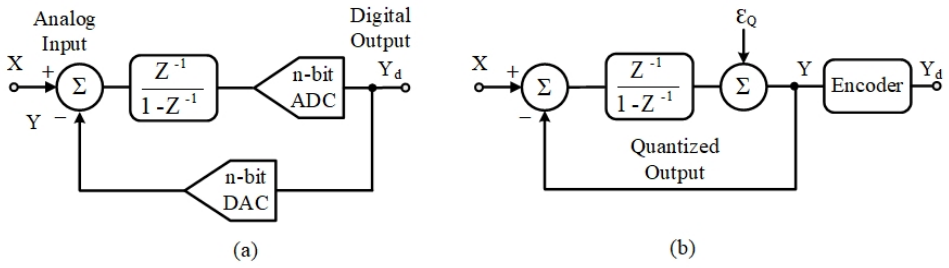

Figure 2.7: (a) Sampled-data first order sigma delta modulator and (b) its linear model.

The benefits provided by oversampling and noise-shaping enable the use of a small number of quantization levels. However, the noise-shaping technique is based on the white nature of the quantization noise. This condition applies under

a given set of circumstances:

1. all the quantization levels are exercised with equal probability;
2. a large number of quantization levels are used;
3. the quantization steps are uniform;
4. the quantization error is not correlated with the input.

Thus, the use of a small number of quantization levels does not comply with the conditions necessary for considering Q as white noise. If the signal contains a dominant DC component, the quantization noise becomes a repetitive pattern that produces spectrum tones, and also the $4th$ condition mentioned above is no longer observed. A possible solution to this problem, apart from using multi-bit quantizers, is to implement the dithering technique. Basically, an auxiliary input that eliminates the correlation between Q and the signal is added. Obviously, the dither must be effective against the tones and should not alter the signal. For this there are two possibilities: the first is to inject a sine wave whose frequency is out of the signal band. The digital filter used to cancel the out-of-band noise then removes the effect of the dither. The second method utilizes a noise-like signal whose contribution does not degrade the SNR, which can either be thermal noise of the electronics in role or an external random signal.

It is important to notice that, even with dithering, $\Delta\Sigma$ ADCs cannot provide a deterministic measurement of a DC signal, as some information of the past signals will always be present at the output of the decimator due to the nature of the converter [61].

For an $L-order$ modulator, the noise transfer function (NTF) suppressing the in-band quantization noise leads to

$$NTF = (1-Z^{-1})^{L} \tag{2.17}$$

in terms of frequency-domain it can be expressed as

$$\begin{aligned} NTF(f) = (1-Z^{-1})^L|_{z=e^{\frac{j2\pi f}{f_S}}} &= (1-Z^{e^{\frac{-j2\pi f}{f_S}}})^L \\ &= [-j2e^{j\pi f/f_S} \cdot sin(\frac{\pi f}{f_S})]^L \end{aligned} \tag{2.18}$$

The PSD of quantization noise after $L-th$ order noise-shaping is then given by [62]

$$S_{eQ}^{\Delta\Sigma}(f) = S_{eQ}(f)|NTF(f)|^2 = \frac{V_{LSB}^2}{12 \cdot f_S} \cdot 2sin(\frac{\pi f}{f_S})^{2L} \tag{2.19}$$

Assuming OSR $\gg$ 1,we have $\pi f/f_S \ll 1$, and therefore sin($\pi f/f_S$) can be approximated by $\pi f/f_S$. Then, the shaped quantization noise power in the band of interest, [-f_B, +f_B], is given by:

$$\begin{aligned} N_{\sigma_{eQ}^2}^{\Delta\Sigma}(f) = \int_{f_B}^{f_B} S_{eQ}^{\Delta\Sigma}(f)df & \\ = \int_{f_B}^{f_B} \frac{V_{LSB}^2}{12 \cdot f_S} \cdot 2^L \cdot sin(\frac{\pi f}{f_S})^{2L} &\approx \frac{V_{LSB}^2}{12 \cdot f_S} \cdot 2^L (\frac{\pi f}{f_S})^{2L} \\ = \frac{V_{LSB}^2}{12} \cdot \frac{\pi^{2L}}{2L+1} \cdot (\frac{2f_B}{f_S})^{2L+1} &= \frac{V_{LSB}^2}{12} \cdot \frac{\pi^{2L}}{2L+1} \cdot OSR^{2L+1} \end{aligned} \tag{2.20}$$

Now the *SQNR* is given by

$$SQNR_{sin}^{\Delta\Sigma}(dB) = 10log_{10}(\frac{3}{2} \cdot \frac{2L+1}{\pi^{2L}}(OSR)^{2L+1}(2^{N_B}-1)^2) \tag{2.21}$$

The above equation shows the impact of $\Delta\Sigma$ modulation in suppressing the in-band noise through oversampling and noise-shaping. By combining oversampling and noise shaping, a 9 dB improvement in *SQNR* can be achieved by doubling the OSR, which is much better than using only the oversampling, even with a first-order loop filter (L = 1).

2.4 Incremental Converters

Instrumentation and measurement applications, such as the readout of bridge transducers, battery monitoring and biomedical acquisition systems require monotonic analog-to-digital converters with high resolution, good linearity, low offset and, typically, low power. Incremental converters, directly derived from $\Delta\Sigma$ schemes, are particularly suitable for those needs. They can be considered as a combination of modulators and dual-slope A/D converters. They act like dual-slope A/D converters mixed in time, but also have the benefit of utilizing higher order architectures like modulators [63]. The architecture of an incremental A/D converter is similar to that of $\Delta\Sigma$ modulator but functionally slightly different than conventional $\Delta\Sigma$ converters since the integrators are reset at the start of each conversion. As a result, no information about past samples can be used, and so there is no need to describe the quantization error as noise and even to talk about noise shaping. Thus an incremental ADC can be regarded as a Nyquist-rate converter. The input should be constant during the entire conversion; otherwise the digital result becomes a weighted average of the analog input, in a manner similar to that of a FIR filter.

The equivalent number of bits (ENOB) of an incremental converter depends on the order of the scheme, the number of clock cycles per sample, the resolution of the quantizer and the digital post processing. Generally, to obtain a given resolution, higher order modulators are more efficient since the required number of clock periods is reduced. However, when the order of the scheme is higher than two, stability requirements can limit the effectiveness of the architecture.

An incremental ADC can use single or multi-bit quantizers. Most designs adopt single-bit quantization, [63–67]. In this case, since the DAC uses only 2 levels, it is inherently linear. Nevertheless, the relatively large output swing of integrators may result in operational amplifiers (op-amps) working in slewing mode.

In addition, when the order of the scheme is larger than two, as discussed shortly, stability of the feedback loop demands the use of fractional coefficients in the signal path, which strongly degrades the conversion efficiency.

Fig. 2.8 shows the block diagram of a first-order incremental ADC. In contrast to a dual-slope A/D converter, the integration and subtraction of the reference signal are mixed in time. It consists of a delayed-integrator, a comparator and a 2-level DAC. The operation principle is as follows: when a new conversion cycle starts, the output of the integrator, V_{RES}, is reset. Since the frequency of the input signal of incremental ADCs is usually low, V_{IN} can be regarded as a constant signal. In each clock period, V_{IN} subtracts V_{OUT} (the analog version of D_{OUT}) and the difference is accumulated by the delayed integrator. At the end of N clock cycles, the residue voltage at the output of the integrator is given by

$$V_{RES} = \sum_{i=1}^{N-1} V_{IN}(i) - \sum_{i=1}^{N-1} D_{OUT}(i) \cdot V_{ref} \tag{2.22}$$

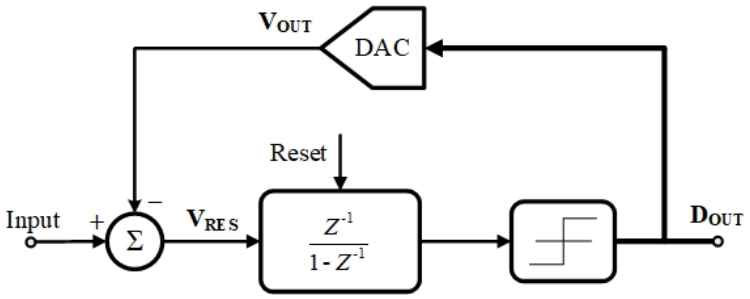

Figure 2.8: First-order incremental ADC block diagram.

Due to the stability of the feedback loop, the voltage of V_{RES} is limited, namely $-Vref < V_{RES} < Vref$, where $\pm Vref$ are the reference voltages. The input signal V_{IN} can be hence, represented as

$$V_{IN} = \frac{\sum_{i=1}^{N-1} D_{OUT}(i) \cdot V_{ref}}{N-1} + \frac{V_{RES}}{N-1} \tag{2.23}$$

and the resolution of a first-order incremental ADC can be expressed as

$$R_1 = log_2(n-1) \tag{2.24}$$

Unfortunately, the conversion efficiency of a first-order incremental ADC is low which can be improved by increasing the number of clock periods for each conversion. In addition higher order loop filters can be used to further enhance the resolution. Higher order Incremental converters and can be implemented in either a single-stage structure, or cascaded or MASH architecture. [68–74]. Moreover introduction of multi-bit quantizer directly affects the resolution. Unlike modulators at low OSRs where noise shaping increases the total quantization noise power of the system [32], incremental A/D converters always have a minimum resolution equal to the resolution of the quantizer, even at an OSR of 1, effectively making it equivalent to a pipe-line A/D converter, if implemented in a cascaded-architecture [63]. More specifically, an input feed-forward cascaded incremental A/D converter can be thought of as a higher order pipeline A/D converter.

Fig. 2.9, illustrates conventional single-stage second-order incremental ADC with feed-forward paths. The structure contains two integrators with delay. In the signal path there are two coefficients c_1 and c_2. The feed-forward paths with coefficients f_1 and f_2 are included to keep the loop stable. In addition a multi-bit quantizer is added to further enhance the resolution. Using the same mathematical approach employed for the first order scheme, the resolution of the second-order incremental converter with multi-bit quantizer can be expressed as

$$R_{2-multibit} = log_2 \frac{c_1 c_2 (N-1)(N-2)}{2!} + b_q \tag{2.25}$$

where b_q is the resolution of the quantizer.

The same approach can be generalized for an $L-th$ order architecture includes

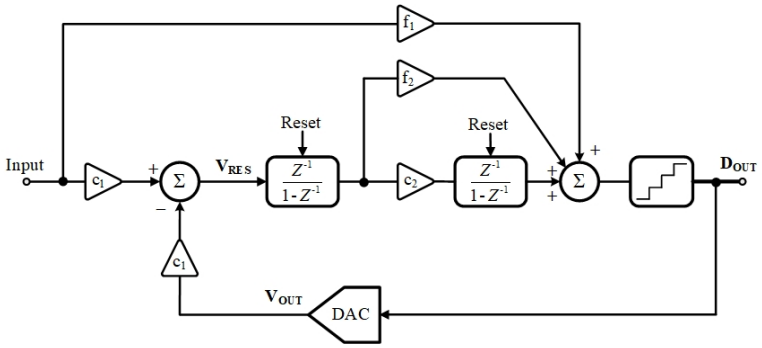

Figure 2.9: Second-order incremental ADC block diagram with multi-bit quantizer and feed-forward path.

L delayed-integrators and feed-forward paths with coefficients $f_{1,2\cdots L}$. There is only one feedback path in the scheme and L coefficients along the signal path $c_{1,2\cdots L}$. The resolution of the Lth-order incremental ADC can be estimated as

$$R_{L-multibit} = log_2 \frac{c_1 c_2 \cdots c_L (N-1)(N-2)\cdots(N-L)}{L!} \tag{2.26}$$

In order to ensure stability, coefficients $c_{1,2\cdots L}$ are generally lower than 1.

2.5 State-of-the-art Audio ADCs

Oversampling A/D converters based on sigma-delta modulation have been an attractive candidate for high-resolution CMOS A/D conversion because they avoid the need for precision components or stringent matching between constituent elements [75]. Conventionally both continuous-time (CT) and discrete-time (DT) $\Delta\Sigma$ modulators have been used for audio applications that require high resolution but have low-frequency signals 20-20 kHz. A few state-of-the-art designs intended for audio range have been discussed in the following paragraphs.

Higher-order continuous-time $\Delta\Sigma$ modulators are the most widely used tech-

niques for audio applications. In [76], a low-power 4th-order single-bit continuous-time Delta-Sigma modulator is designed for audio bandwidth. The modulator employs an input feed-forward topology to reduce internal signal swings, thus relaxing the linearity and slew rate requirements for amplifiers leading to low-voltage operation and low-power consumption. The modulator, implemented in a 0.13 μm standard CMOS technology, achieves an 82-dB DR and a 79.1 dB peak SNDR over a 20-kHz signal bandwidth. The power consumption of the modulator is 28.6 μW using a 0.6-V supply voltage and achieves a FoM of 0.0097 $pJ/conv$. In [77], a 3^{rd}-order CT $\Delta\Sigma$ ADC is implemented in 0.18 μm CMOS process. The ADC employs a 4-bit quantizer in the loop and uses a 3^{rd} order hybrid continuous-time and switched-capacitor loop filter. The mismatch in the multi-bit DAC is compensated with conventional DWA technique. The loop filter is implemented with a cascade of integrators with feed-forward paths. The effect of parasitic poles in the loop filter are mitigated by excess-delay compensated implemented through feed-in capacitor. The proposed design achieves a dynamic range (DR) of 93.5 dB by consuming 93 μW power. In [78], a 3^{rd} order continuous-time $\Delta\Sigma$ modulator (CTDSM) is designed in 0.18 μm CMOS process. The loop filter uses CIFF-B architecture, and inherits the benefits of feed-forward and feedback paths. Active-RC integrators are used for high linearity and low noise. Conventional chopping reduces the $1/f$ noise by modulating it outside of signal band, but at the same time the chopping artifacts degrade the CTDSM's SQNR by aliasing shaped quantization noise in-band. In the proposed technique, OTA in the first integrator is chopped at a low frequency and the problem of quantization noise aliasing is addressed by using an FIR feedback DAC. The circuit achieves 98.5 dB/99.3 dB/103.6 dB of $SNDR, SNR$ and DR respectively in 24 kHz bandwidth and achieves *1/f* noise corner of >10 Hz. In [79], a 3^{rd}-order continuous-time $\Delta\Sigma$ modulator using an OSR of 75 is implemented for audio

bandwidth. The modulator employs a feed-forward (CIFF) topology, multi-bit quantizer, DAC with three-level current-steering elements, and a 3^{rd}-order loop filter implemented with a low-noise, power-optimized active RC-architecture that uses only two opamps, instead of three or four as in conventional solutions. To improve linearity in the presence of mismatches in unit current-steering elements of DAC, a 1^{st} order DEM technique has been used. Designed in a 0.16 μm CMOS process, the circuit achieves DR of 103 dB, SNDR of 91.3 dB and FoM of 180 dB.

Discrete-time modulators have the advantage of having tolerance to jitter non-idealities and also simplify the specifications for the quantizers. Switched-capacitor implementation of $\Delta\Sigma$ modulator has been done to target audio applications. In [80], a 3^{rd}-order 2-1 cascade switched-capacitor (SC) $\Delta\Sigma$ with an oversampling ratio of 128 is implemented in a 0.6 μm (analog) and 0.3 μm (digital) CMOS process. The 2-1 cascade ADC comprises a 2^{nd}-order modulator followed by another 1^{st} order modulator, producing two single-bit outputs that require digital error correction to provide the 3^{rd}-order output. The design uses a programmable dynamic dither to achieve a tone free DR of 103 dB, SNDR of 96 dB in an audio bandwidth. In [81], a 2^{nd}-order switched capacitor $\Delta\Sigma$ modulator with feed-forward path followed by multi-bit quantization is implemented in a 0.18 μm CMOS process. For multi-bit quantizer, instead of conventional Flash or SAR ADC, a single comparator tracking multi-bit quantization is proposed to achieve low-power conversion. The quantizer is implemented by using an analog switch, a digital deserializer and a single operating in a time-interleaved fashion. DWA and chopper stabilization is employed to compensate for DAC mismatch and reduction of in-band flicker noise. The proposed circuit uses low supply voltage and achieves DR/SNR/SNDR of 100 dB/100 dB/95 dB respectively for audio bandwidth. In [82], a reconfigurable SC audio $\Delta\Sigma$ modulator is implemented in a 0.18 μm CMOS technology. The proposed modulator is based on

2-2 MASH architecture consisting of two cascaded 2^{nd}-order stages with a digital recombination filter. It features several different operating modes in which noise-shaping order, number of output bits, sampling rate, and signal bandwidth can be programmed. The circuit trades the overall performance with robustness and programmability, and can operate in several different modes (low-power, standard, high-resolution) depending on the target audio application. Both 2^{nd} and 4^{th}-order noise shaping can be selected for low-power and high-resolution respectively. Similarly the sampling frequency ranges from 768 kHz to 3.6 MHz. The circuit achieves a DR of 99 dB in HR mode, 96 dB in ST mode, and 85 dB in LP mode, with a peak SNDR of 80 dB in standard mode.

Recently, there has been a trend of combining different topologies of ADC to avail their advantages resulting in single hybrid designs. Same concept has also been used for audio applications. In [83] a hybrid architecture consisting of a 3^{rd}-order continuous-time $\Delta\Sigma$ modulator (CTM) and a 5-bit SAR quantizer is proposed targeting a bandwidth of 25 kHz. Noise coupling (NC) technique is used to enhance the noise transfer function instead of using cascaded OTAs. The charge redistribution 5-bit SAR uses a fully differential binary weighted CDAC with NC storage capacitors. Since the performance of SAR is highly dependent on relative capacitor values, a floating differential charge storage capacitors (FDCSC) NC scheme is proposed to mitigate the effect of capacitor mismatch. Designed in 65 nm CMOS process the circuit achieves a $DR/SNR/SNDR$ of 103.1 dB/100.1 dB/95.2 dB while dissipating 0.8 mW.

In [84], a hybrid-mode $\Delta\Sigma$ architecture is proposed to target smart phone specifications. A continuous-time first stage and a discrete-time second stage are implemented to provide second-order noise transfer function. To reduce the input swing for the second DT integrator an inner-loop voltage feedback path is established through the output of a 5-level quantizer to the input of the second

integrator. The resolution is further enhanced by using a 17-level quantizer after the second integrator. To prevent unstablity, a start-up sequence including RC calibration and signal monitoring is developed. Designed in a 40 nm CMOS process the proposed circuit achieves a dynamic range of 102 dB with 24 kHz bandwidth.

In [85], a hybrid architecture, a dynamic Zoom ADC intended for audio applications is proposed. This Zoom ADC employs a two-step architecture; a low-resolution coarse conversion is done by a synchronous 5-bit SAR ADC operating at higher speed, while fine conversion is done by a slower $\Delta\Sigma$ modulator that employs a 3^{rd}-order loop filter and 1-bit quantizer. Both these ADCs operate concurrently and their outputs are synchronized at the same frequency. Pseudo-differential Inverter-based OTAs have been used in $\Delta\Sigma$ integrators with dynamic biasing to achieve better energy efficiency. The *1/f* noise of the ADC is suppressed by the inherent autozeroing scheme of proposed inverter-based amplifiers. To compensate for the mismatch in the multi-bit feedback DAC, DWA algorithm has been employed to scramble the selection of unit capacitors. Designed in 0.16 μm CMOS process, the proposed circuit achieves 109 dB DR, 106 dB SNR, and 103 dB SNDR and a Schreier FoM of 181.5 dB for 20 kHz bandwidth.

In [86], a compact VCO-based second-order modulator is implemented in 0.13 μm CMOS process for MEMS microphone. The proposed converter is implemented using only oscillators and digital circuitry, without operational amplifiers nor other highly linear circuits. The ADC consists of two twin second-order modulators, which can work both in single-ended or in a pseudo-differential configuration. A single-bit quantizer has been used to comply with the standard digital interfaces of digital MEMS micro phones. The integration of the feedback is done in discrete-time because of its better tolerance to jitter compared to classical CT $\Delta\Sigma$ modulators. However, non-idealities including phase noise and distortion limit the achievable resolution of the circuit. The circuit uses a sampling fre-

quency of 20 MHz, and achieves SNDR, DR of 69.6 dB and 93.5 dB respectively in single-ended operation which improves to SNDR of 76.6 dB and DR of 98 dB in pseudo-differential mode.

2.6 Summary

Some basic performance metrics related to ADCs have been discussed in the beginning. A small introduction and classification of ADC architectures have been described followed by in-detail discussion of $\Delta\Sigma$ and Incremental ADCs which are generally used for low-frequency applications. A few reported state-of-the-art architectures have been reviewed that been designed for audio applications.

Chapter 3

Architectural Description of Hybrid ADC

This chapter describes the proposed architecture of the Hybrid ADC that suits the required audio application. The ADC is primarily focused to provide analog input support to a digital input Class-D audio amplifier. The ADC solution is intended to achieve a dynamic range (DR) of 100 dB for an input signal of -60 dBFs which translates into >16-bit of resolution. In addition, the ADC should also provide noise shaping with an output signal frequency of $\geq$ 576 kHz. Table. 3.1 summarizes the main target specifications of ADC.

Technology	180 nm CMOS
Supply Voltage	1.8 V
Bandwidth	24 kHz
Dynamic Range	>100 dB for -60 dBFs input
Output bits	≤ 7

Table 3.1: Summary of the available parameters and target specifications.

One of the possible architectures to achieve the targeted resolution is SAR

ADC. SAR ADC is preferred because of its simple architecture, its flexibility and coherence with modern CMOS processes [87–90]. In addition, SAR ADC offers a good match between low speed and medium-high resolution. However, the performance of SAR ADC is largely dependent on the total capacitor size, increasing by *2* times with the addition of each extra bit, hence increasing the area by the same margin. Moreover, with the increase in the number of unit capacitors and their minimum size is limited by the process variations and mismatches. A few preliminary calculations based on minimum capacitor size and mismatch were done revealing that a maximum resolution of 14-bits could be achieved with the given technology parameters, which is much less than the target resolution.

3.1 Hybrid Solution

In order to achieve the targeted specifications of >100 dB DR, a hybrid solution (extended range) has been proposed that exploits the advantages of both incremental ADC and delta-sigma modulators. Figure. 3.1 shows the conceptual block diagram of the proposed solution. In simple terms the solution includes the conversion of the input signal in two steps.

- Coarse conversion by an Incremental ADC to generate the MSBs
- Fine conversion and noise shaping by a $\Delta\Sigma$ ADC to generate the LSBs

The ultimate choice of the order and quantizer both in incremental and $\Delta\Sigma$ ADC and details of the architecture is discussed below. After the conversion, output of the incremental ADC is accumulated, delayed and combined with $\Delta\Sigma$ ADC output with proper synchronization to generate the final output.

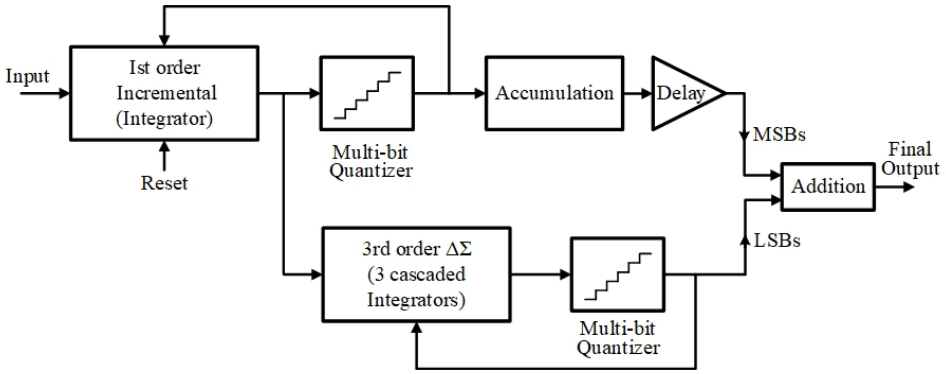

Figure 3.1: Block Diagram of proposed solution to achieve 110 dB DR.

3.2 Incremental ADC

The overall resolution of the Incremental ADC is mainly dependent on the quantizer resolution, number of clock cycles between two resets for each conversion and order of the modulator. Since the sampling frequency is fixed, increasing the number of clock cycles between two resets can help in increasing the resolution but at the same time tighten the slew rate and bandwidth requirements of the opamp in the integrator and also increases the power consumption. Similarly increasing the order of modulator results in achieving higher resolution but then the issue of the stability needs to be resolved, which is usually done using fractional coefficients in the feedback which in turn affects the conversion efficiency. Moreover, the quantizer resolution has a direct impact on resolution but increasing the quantizer bits is severely impacted by the capacitor mismatch and non-linearity requiring sophisticated approaches to compensate for these effects [91].

A small analysis was done in order to observe the effect of number of clock cycles, order of the modulator and quantizer on the overall resolution of the ADC. Figure. 3.2 shows the effect of the order of the modulator L, quantizer resolution Q and the OSR or number of clock cycles for each conversion on the overall SNR of incremental ADC. As evident, there is a tradeoff between the number

of clock cycles, the quantizer resolution and order of the modulator. In order to get the optimal performance and smaller figure of merit (FOM), it is necessary to maintain a balance between all these parameters.

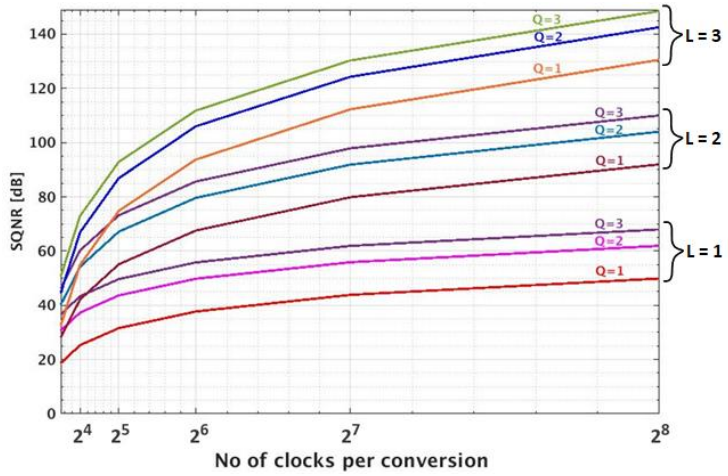

Figure 3.2: Effect of modulator order and quantizer resolution on SQNR vs OSR.

Keeping in view the above mentioned parameters and required specifications, the optimal solution for the coarse conversion is to use a single stage first order incremental ADC with a multi-bit quantizer. Advantages of using this multi-bit approach is the reduced output swing of opamp and higher conversion efficiency by using the maximum value of feedback co-efficient i.e. 1. Since the incremental ADC in the current scheme is supposed to generate the MSBs, it is important to generate a highly accurate residue. This condition puts very stringent requirements on the opamp in the integrator in terms of gain and linearity.

Resolution of the 1^{st}-order incremental ADC with multi-bit quantizer can be expressed as

$$R_{1-multibit} = log_2(n-1) + b_q \tag{3.1}$$

where n is the number of clock cycles per conversion and b_q is the resolution of converter. With a sampling frequency of 576 kHz, the number of clock cycles

selected is 28 for the audio bandwidth of 24 kHz. With a 4-bit quantizer, a maximum resolution of 8.75 bits is achieved which translates into a maximum SNR of 54.4 dB. However, the presence of non-idealities prevents to achieve the theoretical resolution. Figure. 3.3 shows a conventional 1^{st}-order incremental ADC with a multi-bit quantizer.

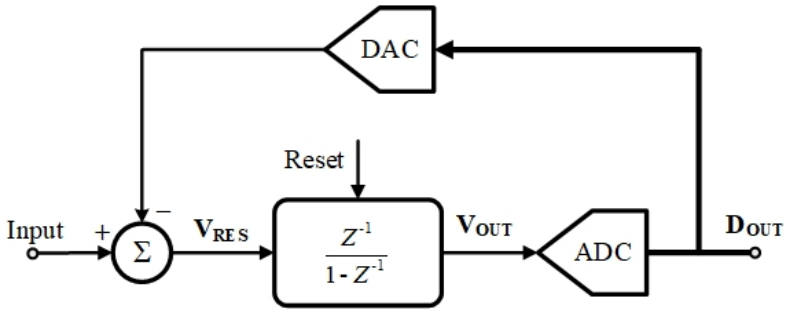

Figure 3.3: Conventional 1^{st}-order incremental ADC.

A novel approach for the 1^{st}-order incremental ADC has been proposed that reduces the output swing requirements of opamp not only in incremental block but also relaxes these requirements for the opamps in $\Delta\Sigma$ ADC. In addition it improves the conversion efficiency by employing the maximum feedback coefficients.

Figure. 3.4 shows the proposed incremental ADC to be employed at the front-end to generate the MSBs. The scheme uses an N-bit ADC (ADC2 in Figure. 3.4 used in a parallel path at the beginning of the conversion cycle (simultaneously to the reset of the integrator). The result of this initial conversion serves to generate a residual voltage which is given by the following equation

$$V_{res}(nT) = V_{in}(nT) - V_{DAC} \tag{3.2}$$

This residue is used as the input of the first-order incremental converter for all the successive cycles of the incremental section before the next reset. As a re-

sult, only the difference or the residue is processed through the incremental ADC. Consequently, the actual ADC of the incremental (ADC1 in Fig. 3.4) can use only one (DAC1 with two levels) or two (DAC1 with three levels) comparators.

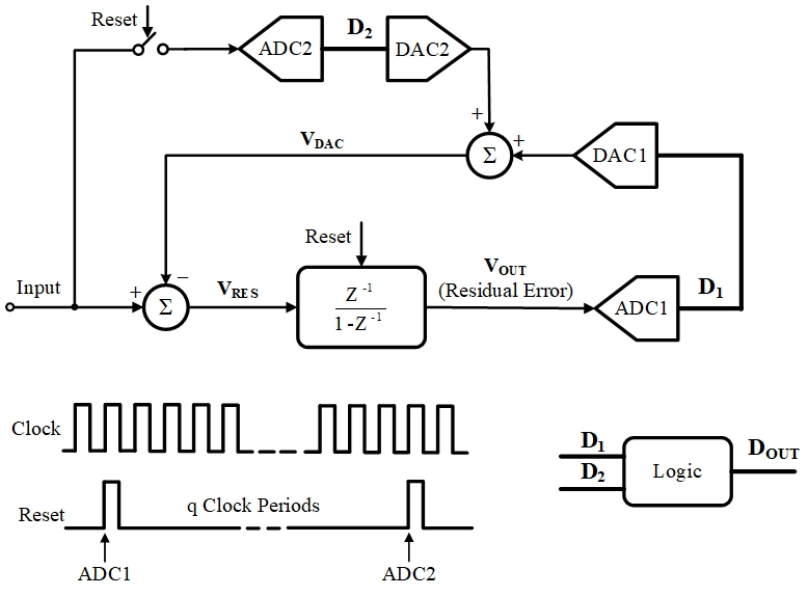

Figure 3.4: Proposed 1^{st} order Incremental ADC with multi-bit quantizer.

The scheme uses ADC2 only one time per conversion i.e. between two consecutive resets, because it is assumed that the change of the input signal during the q cycles of the conversion is much lower than $V_{FS}/2^N$ (being V_{FS} the input signal full scale). This solution requires $2^N - 1$ comparisons for the first conversion and q or $2q$ comparisons for the incremental phase. Thus, there is a lower number of comparison with respect to the conventional scheme (Fig. 3.3) that requires $q(2^N - 1)$ comparisons. Supposing $q = m2^N$, the total number of comparisons diminishes to $(2^N - 1) + q$. The value that is fed back to the input for subtraction is the addition of DAC1 and DAC2, where the output of DAC2 is constant between the two resets. The output of DAC1 may change during each cycle for each single conversion between the two resets.

With this approach the feedback error which is only a fraction of the input

signal is propagated through the incremental opamp resulting in very small output signal that is further processed by $\Delta\Sigma$ modulator. The cost of employing the parallel path is two extra comparisons in the incremental phase.

3.3 $\Delta\Sigma$ Modulator

In order to further process the small output generated by incremental opamp and perform noise shaping, a standard $\Delta\Sigma$ modulator is an optimal choice. Since the requirement of the dynamic range is quite high a 3^{rd}-order $\Delta\Sigma$ modulator with a multi-bit quantizer serves the purpose to generate the LSBs.

SQNR of a 3^{rd}-order $\Delta\Sigma$ ADC with multi-bit quantizer can be expressed as

$$SQNR = 6.02N + 1.76 + 10log2^M + 3(2L+1) \tag{3.3}$$

Where N is the resolution of the quantizer, M is the oversampling ratio and L is the order of $\Delta\Sigma$ ADC. With a sampling frequency of 576 kHz, oversampling ratio (OSR) of $\Delta\Sigma$ modulator is 12 for the audio bandwidth of 24 kHz. With a 5-bit quantizer, the resolution of the 3^{rd}-order $\Delta\Sigma$ ADC is 8.75 bits which translates into a maximum SQNR of 111 dB. However, as mentioned earlier, the presence of non-idealities prevents to achieve the theoretical resolution.

The parallel path technique employed in the incremental block also relieves the output swing requirements of the opamp of the integrators in $\Delta\Sigma$ modulator. Since the $\Delta\Sigma$ modulator is generating the LSBs, so any non-linearity or imperfection does not have a very big impact on the overall SNR of Hybrid ADC when compared with the linearity or performance of Incremetnal ADC. As a result the requirements for the opamps in the integrators of $\Delta\Sigma$ modulator are quite relaxed and do not need very high gain. Figure. 3.5 shows the proposed 3^{rd}-order $\Delta\Sigma$ modulator with a 5-bit quantizer to generate the LSBs for the digital

output. As shown the scheme employs a cascade of integrators with distributed feedback (CIFB) topology with capacitive input feedforward (CIFB-CIF). The input-feedforward path is added to increase the effective dynamic range and relax the requirements for the analog blocks in the modulator.

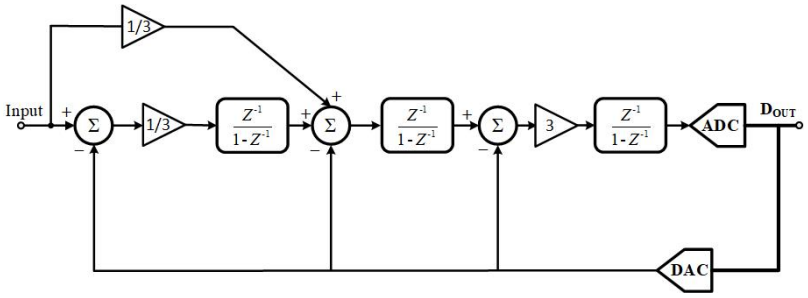

Figure 3.5: 3^{rd}-order $\Delta\Sigma$ ADC with multi-bit quantizer.

3.4 Recombination

In order to get a proper output and correct functionality, it is critical to combine the outputs of the two blocks properly and with the correct samples. Since the output from the incremental block is processed by the $\Delta\Sigma$ modulator, so there is a delay between the arrival of the outputs from both these blocks for the same input and depends on the topology of $\Delta\Sigma$ modulator. With the above mentioned topology of the $\Delta\Sigma$ modulator with feedforward path, there is a latency of two clock cycles before the outputs are combined. Moreover, before combining the outputs, the two binary outputs from the incremental block i.e. ADC1 and ADC2 needs to be accumulated for each conversion. The accumulation or the addition depends on the number of clock cycles that have been used in a single conversion. Figure. 3.6 shows the complete architecture of the proposed hybrid ADC to achieve a dynamic range of >100 dB for -60 dBFs input signal. The accumulation of the incremental binary output and combination with the $\Delta\Sigma$ modulator output can be

done off-chip.

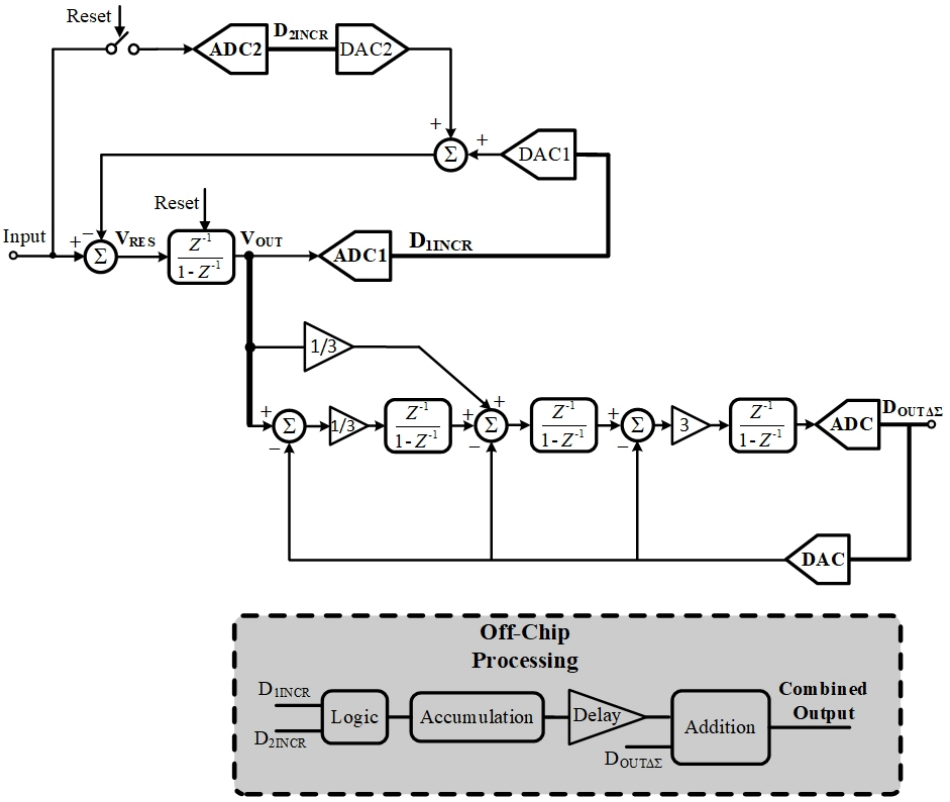

Figure 3.6: Integrated Model of the architecture of proposed Hybrid ADC.

3.5 Summary

A novel extended-range Hybrid ADC has been proposed in this chapter, that combines the advantages of both Incremental and $\Delta\Sigma$ modulators. The hybrid ADC uses a first-order Incremental ADC with multi-bit quantizer at the front-end whose residual error is further processed by a third-order $\Delta\Sigma$ ADC that also uses a multi-bit quantizer. The accumulation of the digital output from Incremental block is done off-chip and further added with the digital output of $\Delta\Sigma$ ADC after introducing proper clock delays.

Chapter 4

Behavioral modeling of proposed Hybrid ADC

In order to validate the functionality and the performance of the proposed architecture, a Matlab/Simulink model is developed before the actual implementation of the circuit. The Simulink models of the circuit should also include the possible non-idealities and limitations that are assumed to be present in the circuit and have major impact on the performance.

4.1 Ideal Integrated Simulink Model

In the first case an ideal integrated model is simulated without any non-ideality to endorse the functionality and performance of the proposed architecture. Figure. 4.1 shows an ideal Simulink model of the hybrid ADC with the specifications mentioned in the Table.4.1. An infinite gain, bandwidth and slew rate have been used for this purpose with no introduction of KT/C noise and sampling jitter. Figure. 4.2 shows the output spectrum of the combined signal at the output for an input of -1 dB, where it achieves an SNR of 123 dB, 20 dB more than the targeted specification.

Sampling Frequency	576 kHz
Input Frequency	223 Hz
Full Scale Voltage	1.8 V
No of Samples	65,536
Input Range	-1 dB$\rightarrow -60\ dB$
No of cycles/conversion in Incremental ADC	28
Quantizer-I,II in Incremental ADC	4-bit
OSR of $\Delta\Sigma$ ADC	12
Quantizer-III in $\Delta\Sigma$ ADC	5-bit

Table 4.1: Summary of the specifications used in ideal Simulink model.

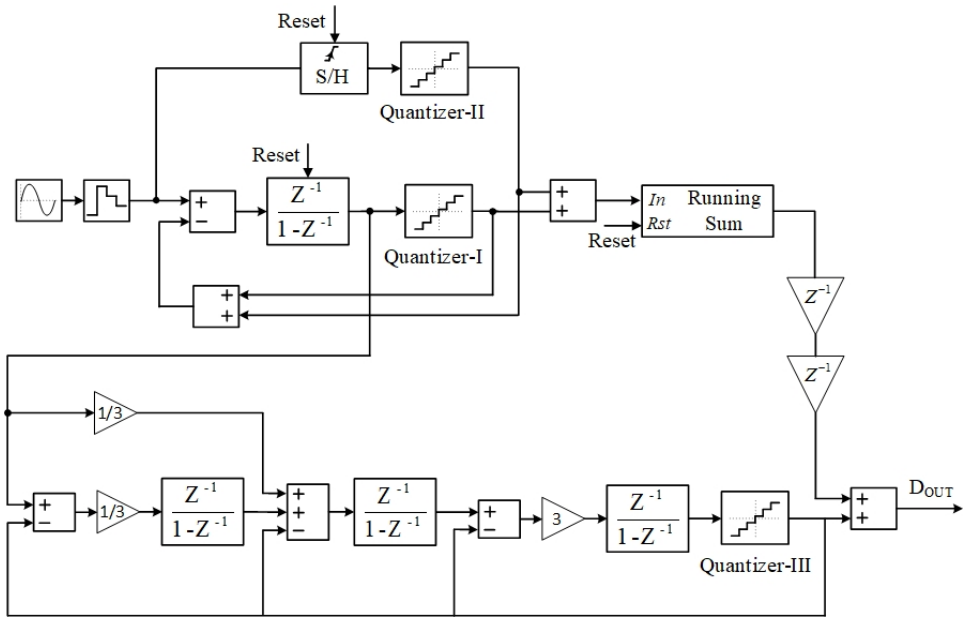

Figure 4.1: Ideal Simulink model of the proposed Hybrid ADC.

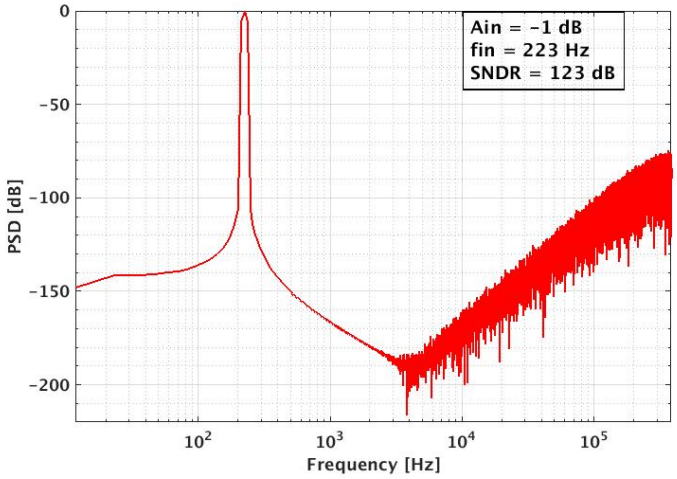

Figure 4.2: Output Spectra of the ideal model of Hybrid ADC.

4.2 Addition of Non-Idealities

4.2.1 KT/C Noise

Thermal noise is the most important noise source in switched capacitor incremental and $\Delta\Sigma$ modulators and is ever present in the system. It is caused by the random fluctuation of the carriers due to thermal energy. Thermal noise has a white spectrum independent of the frequency and wide band limited only by the time constant of the switched capacitors or the bandwidth of the operational amplifiers. The thermal noise power due to the sampling capacitor in the SC circuit is given by

$$e_T^2 = \frac{KT}{C} \tag{4.1}$$

where K is the Boltzmanns constant, T is the absolute temperature and C is the sampling capacitor.

The noise voltage e_T is directly superimposed to the input signal and poses a limit on the minimum size of the sampling capacitor to be used in the SC circuit.

In the proposed hybrid ADC topology, where the front-end is composed of the incremental ADC followed by $\Delta\Sigma$ ADC, the sampling capacitors in both blocks have an impact on total noise. For incremental ADC, the noise power is given by

$$\varepsilon^2_{rms(Incr)} = No\ of\ clock\ cycles/conv \times 2 \times KT/C_{s(Incr)} \tag{4.2}$$

Similar equation can be applied to the $\Delta\Sigma$ ADC excluding the effect of the number of clock cycles, however the noise referred to the input of $\Delta\Sigma$ ADC is reduced by a factor of OSR. The total noise power referred to the input by both blocks is given by

$$\varepsilon^2_{rms(tot)} = \frac{2 \times (\varepsilon^2_{rms(Incr)} + \varepsilon^2_{rms(\Delta\Sigma)})}{OSR} \tag{4.3}$$

with the condition that the same capacitor array is used both for sampling and in the feedback DAC alternately.

The sampling capacitor $C_{s(Incr)}$ in the SC circuit at the front end of Incremental ADC dominates the thermal noise contribution, while in $\Delta\Sigma$ ADC, since an already resolved signal is processed so the sampling capacitor $C_{s(\Delta\Sigma)}$ size does not pose a major impact on the total thermal noise.

A small analysis has been done in order to investigate the effect of the size of sampling capacitance $C_{s(Incr)}$ on the overall SNR of the system. The sampling capacitor in the $\Delta\Sigma$ ADC is fixed to 640 fF with a unit capacitance of 20 fF, since a 5-bit Flash ADC or quantizer is used for $\Delta\Sigma$ ADC. The minimum value of 20 fF is selected taking into account the process variations and amount of absolute variation in the unit capacitor value of the used CMOS process. A mismatch factor of 0.2% is targeted for the maximum variation in the unit capacitances. In addition, a somewhat higher value of the capacitance leads to lower thermal noise contribution to the system at the cost of higher area and power consumption. Figure. 4.3 represents the effect of sampling capacitor on the overall SNR for a

range of effective full scale voltages. As it is evident that the minimum sampling capacitor size that can be used to achieve 110 dB SNDR is 4 pF with effectively no margin. For all practical purposes, there needs to be a safe margin for the KT/C noise, since there is no circuit or post-processing remedy to mitigate its effect. A sampling capacitor of 8 pF is selected with a unit capacitance of 500 fF. A larger increase in the size then affects the specifications of opamps in the input stage of the incremental block by putting much more stringent requirements in terms of slew rate and bandwidth.

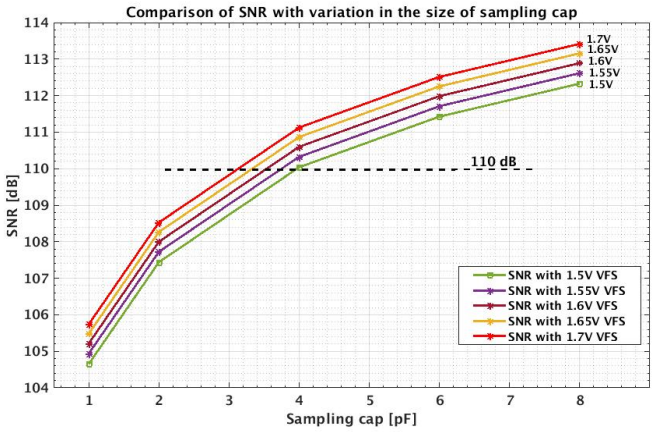

Figure 4.3: Effect of the sampling capacitor on overall SNR.

Using a sampling capacitor of 8 pF ($C_{s(Incr)}$) for the incremental and 650 fF ($C_{s(\Delta\Sigma)}$) for $\Delta\Sigma$ modulator, Figure. 4.4 shows the result of the simulation demonstrating the effect of KT/C noise on the overall SNR in comparison with the output of an ideal model for an input of -1 dB. As shown, the noise floor in the signal band increases with the insertion of KT/C noise and reduces the overall SNR from 123 dB for the ideal case to 113 dB.

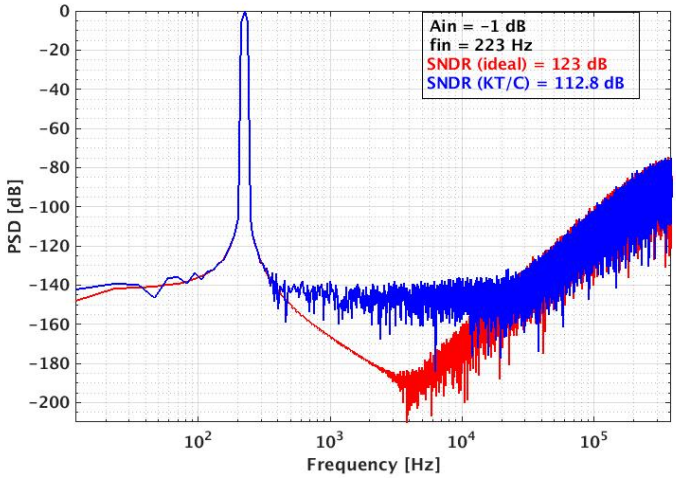

Figure 4.4: Spectra of the output with ideal and KT/C noise model for the hybrid ADC.

4.2.2 Finite DC Gain

Since for all practical cases, an opamp cannot exhibit an infinite gain and infinite bandwidth, so for a working model a known limit on the minimum gain and bandwidth of the opamp is required to achieve the required performance. The finite gain of the opamp introduces a gain error in the signal path and a phase error in the feedback path of the integrator and can be inserted in the matlab model with the following equation

$$GainError = \frac{A}{(A+2)} \tag{4.4}$$

$$PhaseError = \frac{(A+1)}{(A+2)} \tag{4.5}$$

Where A is the open-loop gain of the opamp.

The incremental opamp being at the front-end requires a high gain. In comparison, the opamps in $\Delta\Sigma$ ADC being in the second stage and processing only the residual error and operating at a much lower frequency does not require very high

gain and bandwidth. An open loop gain of 94 dB is selected for the incremental opamp, while a much less gain of 60 dB is selected for the three opamps in $\Delta\Sigma$ modulator. Figure. 4.5 shows the output spectra in the presence of finite gains in comparison with the output of ideal model with infinite gains. As shown there is an increase in the in-band noise reducing the overall SNR by 11 dB. Figure. 4.6 shows the results for the DC gain sweep of the incremental opamp. As shown the DC gain of the OTA should be higher than 90 dB to have no SNR loss.

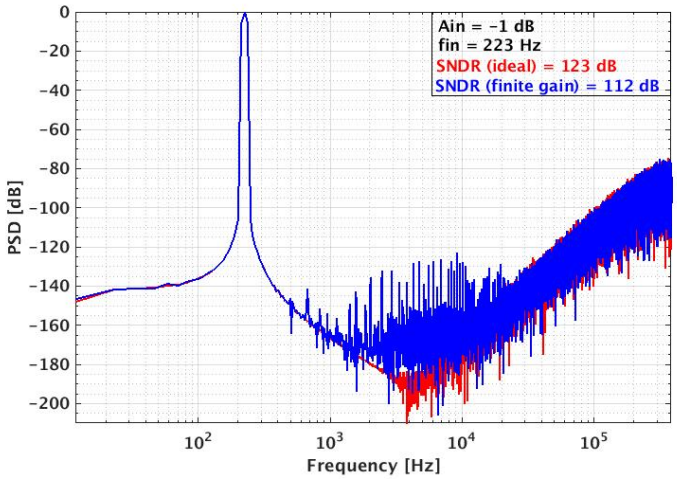

Figure 4.5: Spectra of the output with ideal and finite gain opamps for the hybrid ADC.

4.2.3 Slew Rate and Bandwidth

Both bandwidth (BW) and slew rate (SR) are related to each other and manifest their effect as a nonlinear gain [92]. Limited SR and BW result in non-ideal transient response thus leading to non-complete or inaccurate charge transfer at the output during integration phase [93]. Since both incremental and $\Delta\Sigma$ ADCs are sampling the input and operating at different frequencies, so the minimum requirements of slew rate and bandwidth are also different just like the loop gain as mentioned above. The time constant of the integrator is given by

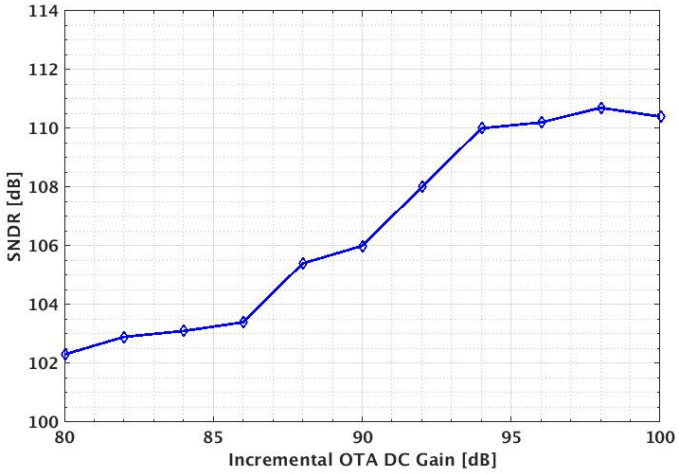

Figure 4.6: SNDR as a function of DC voltage gain of Incremental OTA.

$$\tau = \frac{1}{(2\pi \times GBW)} \tag{4.6}$$

where *GBW* is the unity gain frequency of op-amp.

While the minimum slew rate in the presence of finite gain and *GBW* is given by

$$SR > \frac{(A-1)}{A} \times \frac{Input_{(abs)}}{\tau} \tag{4.7}$$

In the proposed architecture, on one hand, the incremental block operates at a multiple of sampling frequency requiring high bandwidth and slew rate but on the other hand, since the output of the integrator in the incremental block faces another SC circuit with small output load relaxing the speed requirements, so the slew rate and bandwidth requirements for the incremental opamp are fairly in a moderate range with gain bandwidth (GBW) requirements being 100 MHz.

For $\Delta\Sigma$ block, which operates at the sampling frequency of 576 kHz, the slew rate and bandwidth requirements are quite relaxed with minimum GBW being less than 40 MHz. Figure. 4.7 shows the effect of finite gain, bandwidth and slew rate

by introducing harmonic distortions reducing the overall SNDR to 118.4 dB as compared to the ideal value of 123 dB. A unity gain frequency (UGF) value of 100 MHz and slew rate of 100 $V/\mu sec$ is selected for the incremental integrator while a UGF of 40 MHz and a slew rate of 30 $V/\mu sec$ is selected for the simulations of $\Delta\Sigma$ integrators. Figure. 4.8 shows the SNDR as a function of the GBW for incremental OTA with a DC gain of 94 dB.

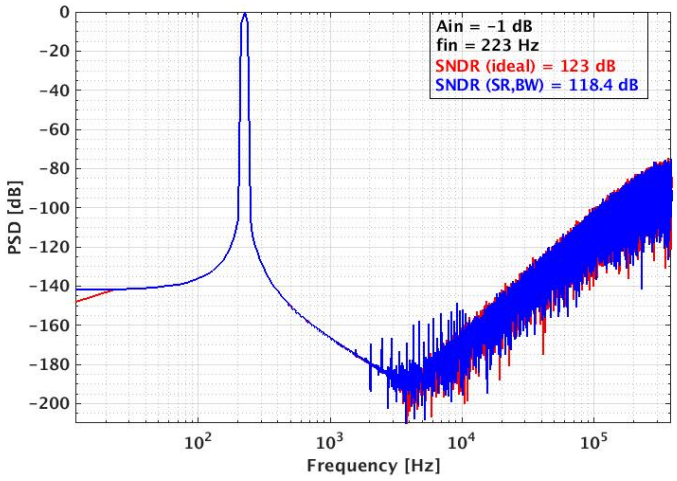

Figure 4.7: Spectra of the output with and without SR and bandwidth limits for the hybrid ADC.

4.2.4 Sampling Jitter

Generally in ADCs, the front-end is supported by a sampling circuit operating at a specific frequency to convert the CT signal into DT form. The sampling circuit is mainly comprised of a sampling switch driven by a clock signal followed by a sampling capacitor. The random variation in the timing of the clock edges is termed as clock-jitter. This variation at the sampling circuit results in errors in the sampled voltage. This error induces the noise, which is directly added to the input signal. Hence a noisy input signal is processed translating into dBs lost in

Figure 4.8: SNDR as a function of GBW for the Incremental OTA.

the signal path, thereby affecting the achievable SNR of ADC [94, 95]. The SNR degradation in the presence of jitter can be determined by the following equation

$$SNR_{jitter}[dB] = -20 \times log(2\pi \times f_{in} \times t_{jitter}) \tag{4.8}$$

where f_{in} is the input frequency and t_{jitter} is the amount of clock jitter.

As evident from the equation that with an increase in the input frequency the jitter requirements become more stringent to achieve the same SNR. For a one-decade increase in the input frequency, the achievable SNR is reduced by 20 dB in the presence of jitter. For an input frequency of 2 kHz, the SNR of 110 dB can tolerate a jitter of 250 psec.

To achieve high SNR as targeted in the proposed design, there is a need to either suppress the jitter-induced errors or make the design robust enough to tolerate these errors. One possible way is to increase the sampling frequency i.e. OSR to mitigate the jitter effect at the cost of higher power consumption. Alternatively, with a low OSR, the order of modulator or the quantizer resolution can be increased to compensate for the jitter induced noise [96]. In the targeted au-

dio application, the second option of increasing the quantizer resolution has been used to mitigate the effect of jitter along with the added advantage of reduced quantization noise.

4.2.5 Opamp Noise

Opamp noise is another important parameter that needs to be considered especially for high resolution ADCs. The noise requirements for the incremental opamp are more stringent as compared to the $\Delta\Sigma$ opamp. The opamp thermal noise is white in nature so it has the same effect as that of KT/C noise and sampling jitter. Hence it is also not noise-shaped similar to KT/C noise. An input referred noise power of 10 $\mu Vrms$ and 100 $\mu Vrms$ is assumed at the input of incremental integrator and $\Delta\Sigma$ integrator respectively. These values only include thermal noise contribution of opamps while the flicker noise and dc offset are neglected. Figure. 4.9 shows the effect of opamp thermal noise on the overall SNR in comparison with the ideal model.

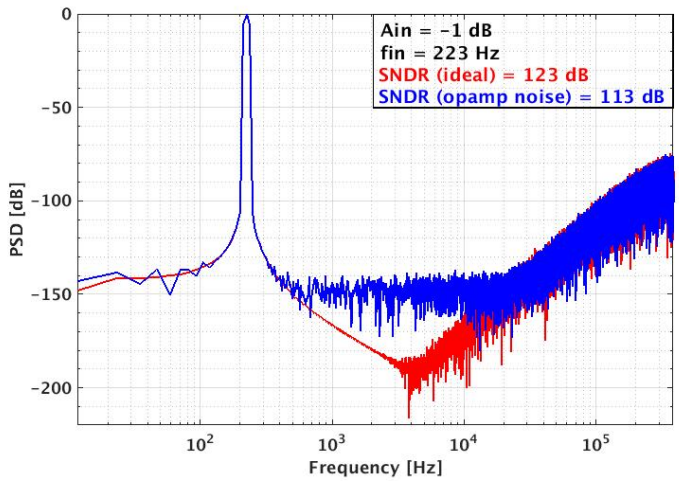

Figure 4.9: Spectra of the output with and without opamp noises for the hybrid ADC.

4.3 1^{st} Order Incremental ADC

The novel approach discussed in the previous chapter for the incremental ADC relaxes the output swing requirements. The simulink model of the proposed incremental ADC with the parallel path as shown in Figure. 4.10 has been implemented and the performance is compared with that of a standard Incremental topology under the same circumstances. The reset integrator has been implemented with the finite gain, BW and slew rate. In addition, KT/C noise has been added based on the sampling capacitor size at the front end. Table 4.2 shows the specifications of the Incremental block that has been used in the Simulink model. Figure. 4.11 shows the transient output (residual error) of the reset integrator implemented in the proposed model for an input of -1 dB, producing a very small output swing when compared with the Integrator output of a standard Incremental ADC under the same operating conditions. Figure. 4.12 shows a comparison of the output spectrum of both the topologies. It is evident that the proposed model has the comparable performance with the standard Incremental topology with the additional advantage of low output swing.

4.4 3^{rd} $\Delta\Sigma$ Modulator

The secondary phase of the processing involves the noise shaping of the residual error generated by the incremental block to further enhance the resolution and SNR. In order to achieve the accumulative dynamic range of >100 dB, a 60 dB/dec of noise shaping is enough generating the requirement of implementing a 3^{rd} order $\Delta\Sigma$ modulator. Because of the low output swing of incremental block, the maximum value of feedback coefficients can be used. Moreover, with the feedforward path, the latency of the output is reduced to *2* clock cycles. Table. 4.3 shows the specifications and non-idealities used in the Simulink model of $\Delta\Sigma$ ADC. Fig-

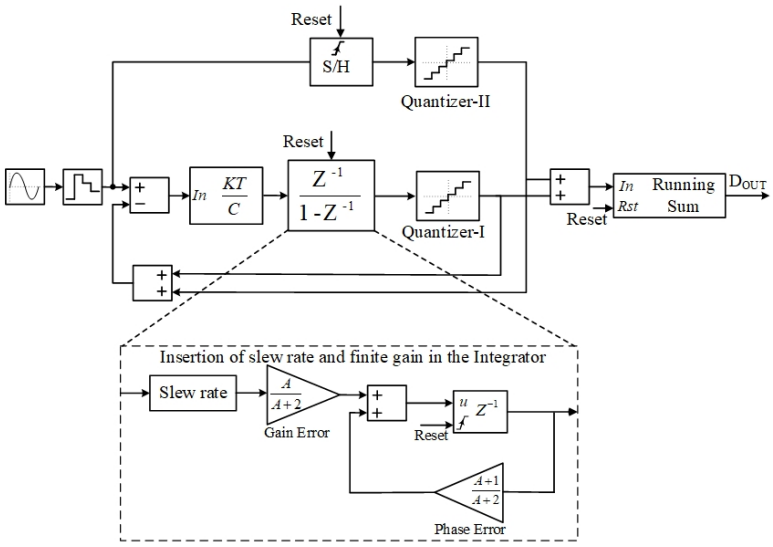

Figure 4.10: Simulink model of the parallel path Incremental ADC with the addition of non-idealities.

Input Frequency	2.4 kHz
Full Scale Voltage	1.8 V
Input	-1 dB
DC Gain	94 dB
UGF	100 MHz
Slew Rate	80 V/µ*sec*
Sampling Cap	8 pF
No of Clock cycles/conversion	28
Quantizer	4-bit

Table 4.2: Summary of the specifications used in the Simulink model of Incremental ADC.

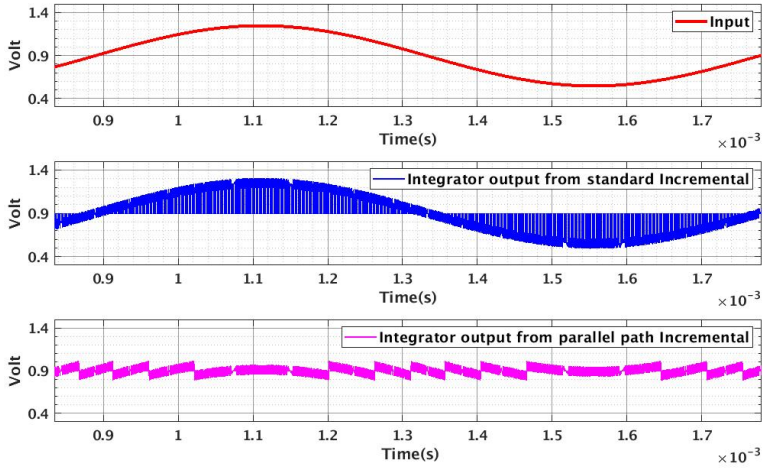

Figure 4.11: Transient outputs of the Integrators in standard(blue) and parallel path (pink) Incremental ADC.

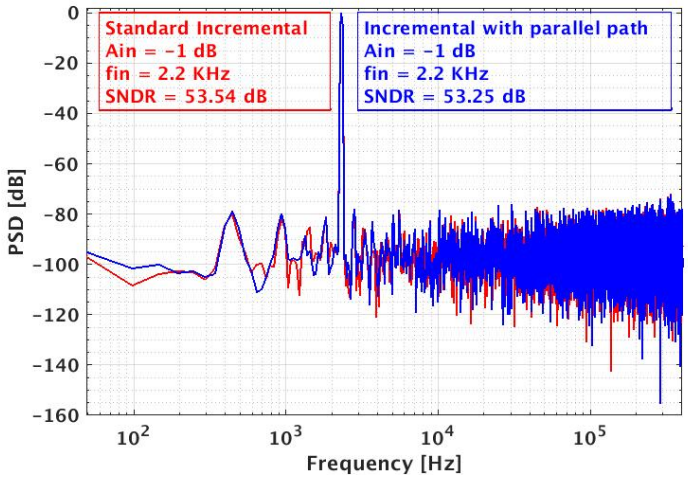

Figure 4.12: Output spectra of standard (red) and parallel path (blue) Incremental ADC.

ure. 4.13 shows the output spectrum of the output signal of $\Delta\Sigma$ modulator for an input of -1 dB. The output shows the required slope of 60 dB/dec and achieves an SNDR of 88 dB resulting in a resolution of 14.3 bits.

Input Frequency	890 Hz
Full Scale Voltage	1.8 V
Input	-1 dB
DC Gain	60 dB
UGF	40 MHz
Slew Rate	20 V/μsec
Sampling Cap	650 fF
Feedback Cap	2 pF
Sampling Frequency	576 kHz
Oversampling Ratio	12
Quantizer	5-bit

Table 4.3: Summary of the specifications used in the Simulink model of $\Delta\Sigma$ ADC.

4.5 Integrated Simulink Model

After validating the ideal integrated model and individual ADCs i.e. 1^{st} order Incremental and 3^{rd} order $\Delta\Sigma$ ADC, the integrated model is simulated with the addition of non-idealities for the opamps in the integrators of both incremental and $\Delta\Sigma$ ADC. The integrated simulink model of the proposed Hybrid ADC is shown in Figure. 4.14. The post-processing includes the accumulation of the incremental output and addition with the $\Delta\Sigma$ ADC output with two clock delays. Table. 4.4 shows the summary of the specifications used in the integrated Simulink model. Figure. 4.15 shows the output spectrum of the final output of the proposed

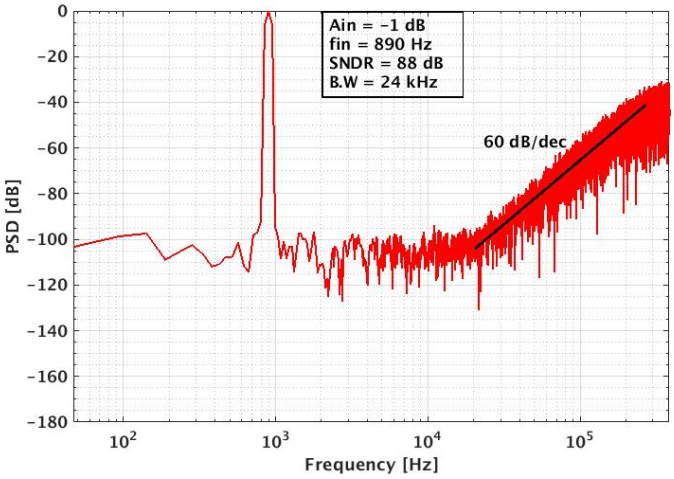

Figure 4.13: Output spectrum of 3^{rd} order $\Delta\Sigma$ ADC with feedforward path.

architecture and achieves the target DR of >100 dB. As evident, the non-idealities introduced have reduced the SNR by 14 dB.

4.6 Capacitance Mismatch

Single-bit quantizers have the advantage of being inherently linear but at the same time suffer from degradation in the conversion efficiency [91] and require much higher number of clock cycles ($\geq 2^{10}$) in each conversion to achieve a higher resolution. Multi-bit quantizers become a convenient choice in order to achieve the same resolution at reduced number of clock cycles thereby reducing the Opamp bandwidth requirements. However at the same time, these multi-bit architectures suffer from non-linearity because of the mismatches in the various DAC elements. This in turn affects the accuracy and linearity of ADCs, limiting the achievable resolution, unless properly compensated at the cost of higher power consumption.

In the current design, both incremental and $\Delta\Sigma$ employ separate multi-bit quantizers and use capacitive DACs in the feedback that uses the thermometric

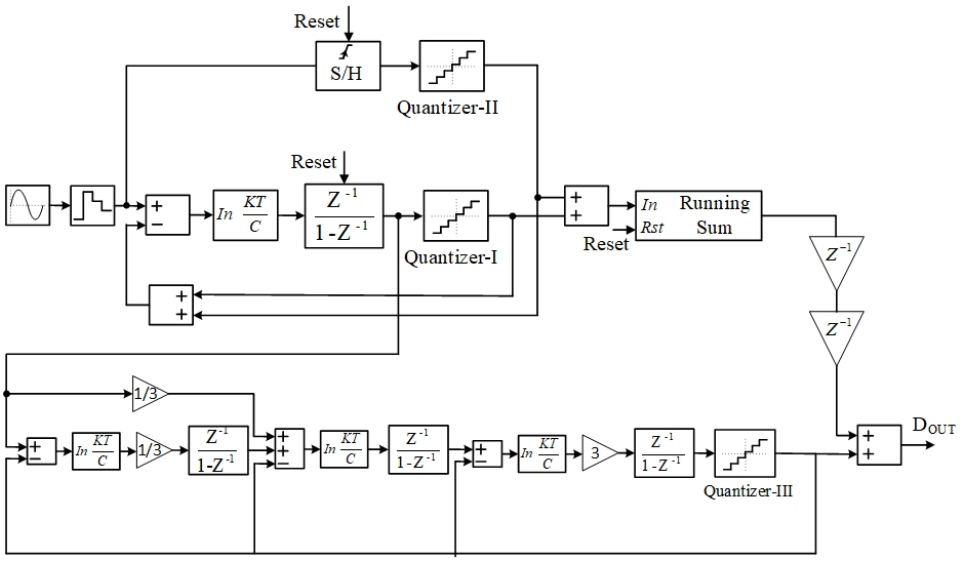

Figure 4.14: Simulink model of the proposed Hybrid ADC with the addition of non-idealities.

Input Frequency	668 Hz
No of clock cycles/conversion in Incremental ADC	28
Full-Scale Voltage	1.8 V
Input	-1 dB$\rightarrow -60\ dB$
DC Gain for Incrmetnal opamp	94 dB
UGF	100 MHz
Sampling cap in Incremetnal ADC	8 pF
Quantizer I,II in Incremental ADC	4-bit
DC Gain for $\Delta\Sigma$ opamp	60 dB
UGF	60 MHz
Sampling cap in $\Delta\Sigma$	650 fF
Oversampling Ratio	12
Quantizer	5-bit

Table 4.4: Summary of the specifications used in the Simulink model of Hybrid ADC.

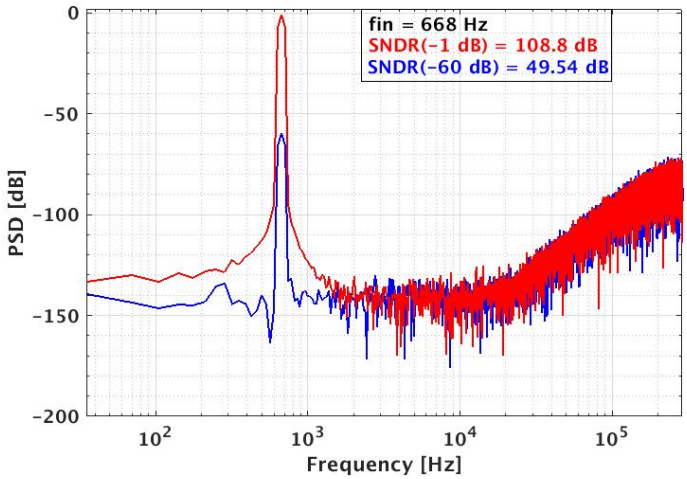

Figure 4.15: Output spectrum of Integrated Simulink Model.

code to select the number of unit capacitances. As incremental ADC generates the MSBs, so even a small mismatch in the capacitive DAC has a dominant impact on the overall SNDR of the system in comparison with the mismatch in the capacitive DACs of $\Delta\Sigma$ modulator. In addition, the usage frequency of the incremental capacitive DAC is much higher than that of $\Delta\Sigma$ capacitive DAC, so the mismatch in the unit element has higher probability to affect the SNDR. The effect of capacitance mismatch in incremental ADCs is explained as follows

Suppose to have n-bit with a capacitor array of 2^n unit elements for making the DAC. The value of each element is $C_i = C_u(1+\varepsilon_i)$, $i = 1,...,2^n$, where C_u is the unit capacitance and ε_i is the mismatch error of the i-th element of the array. Moreover, since the output voltage depends on a capacitance ratio, it is assumed the condition $\sum_{i=1}^{2^n} C_i = 2^n C_u$, making $\sum_{i=1}^{2^n} \varepsilon_i = 0$.

With a constant input V_{in} and being $D_{out,i}$ the digital output at the i-th cycle, the output of the integrator at the end of a conversion lasting q clock cycles is

$$V_{out} = kV_{in} - \frac{V_{REF}}{\sum_{i=1}^{2^n}} \sum_{i=1}^{q} \left\{ D_{out,i} + \sum_{j=1}^{D_{out,i}} \varepsilon_i \right\} \tag{4.9}$$

where V_{REF} is the flash ADC reference voltage. Equation (4.9) shows that, further to the accumulation of the digital values, the output voltage depends on the addition of the mismatch errors, ε_i.

The use of a generic element h times out of the q cycles makes the mismatch error of that element h times larger. The resulting integral non-linearity (INL) error has a statistical maximum at half of the scale where there is multiplication by q of the mismatch of the first half of the elements. If the mismatch of the capacitors is a random variable with variance σ_c, the variance of the INL at the mid-scale is

$$\sigma(INL_{mid}) = \frac{q}{2} \cdot 2^{n/2} \sigma_c. \tag{4.10}$$

For $n = 4$ achieving 12-bit resolution with a first-order incremental requires $q = 256$. The resulting variance of the INL is $512\sigma_c$. In order to keep that value lower than 1/2, the matching accuracy must be $\sigma_c < 0.1\%$. For $n = 6$, there is an equal accuracy requirement, but the number of clock periods is $q = 64$, and the number of unit elements becomes 64.

4.7 One-Shift DEM

An effective method that significantly reduces the INL is the dynamic element matching (DEM), [97–99]. It is the same method used for obtaining noise shaping in $\Delta\Sigma$ modulators. For incremental converters, being Nyquist-rate converters there is no noise shaping. Nevertheless, the method, exploiting the property $\sum_{i=1}^{2^n} \varepsilon_i = 0$, partially compensates for the mismatch error. Figure. 4.16 shows a conventional DEM algorithm based on DWA for a 4-bit DAC. The pointer logic based on the thermo-to-binary decoder, MOD-15 adder and a 4-bit register calculates the starting index of DAC elements based on the current and previous value

generated by rotational shifter [59].

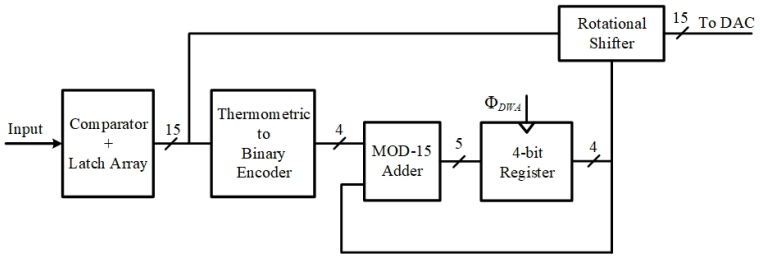

Figure 4.16: Block diagram of Conventional DEM implementation.

In the proposed architecture, since the multi-bit quantizers are used so there is a need to introduce some compensation technique to mitigate the mismatch effect that affects the accuracy particularly in incremental block since it generates the MSBs.

For the parallel path incremental ADC, since two feedback DACs are used so the limit is twofold: from DAC2 in the parallel path that generates the residual and from the elements of the incremental section (DAC1) that processes the output of reset integrator. It is possible to cancel the error caused by DAC2 by using the traditional DEM selection [30]. Since the digital control of DAC2 remains unchanged for 2^N clock period if q is an integer multiple of 2^N ($q = p2^N$), the total number of unit elements required by the q cycles is qD_{out}. The use of the DEM makes the error caused by DAC2 at the end of the conversion equal to

$$\varepsilon_{DAC2} = p\sum_{i=1}^{2^N} \varepsilon_i \tag{4.11}$$

which is zero thanks to the property of the mismatch errors.

A comparable performance can be achieved by shifting the elements by one position in the parallel path for each conversion. This shift is irrespective of the input and is performed between two resets. This proposed shift operation is more straightforward and much simpler to perform than the DEM as compared to the

conventional DEM based on DWA [97]. Figure. 4.17 shows the conceptual block diagram of proposed one-shift DEM. Therefore, using a DEM selection or the more straightforward one-step rotation cancels the first limit. The second source of error is the mismatch between the average of the unit elements of DAC2 and the one(s) of DAC1, $\varepsilon_{\bar{1},2}$. However, the use of two levels or three levels for DAC1 limits the use to one-unit element. The error caused by a single unit element is positive when the control is +1 and negative for a -1 control. Therefore, the systematic accumulation of the error ranges between +q and -q. However, since the required resolution is not that high so the mismatch from these unit elements does not have a very big impact on the performance of incremental ADC and hence this small mismatch can be tolerated without any need of compensation.

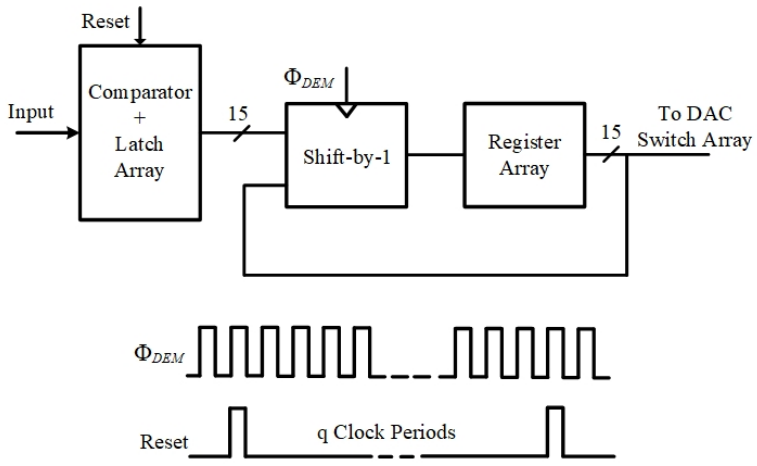

Figure 4.17: Block diagram of proposed One-shift DEM implementation.

Matlab behavioral simulations were carried out to verify the effectiveness of the proposed one-shift DEM for the proposed parallel-path incremental ADC. For all the simulated cases, the capacitor mismatch is set equal to 0.1% in order to emphasize the effectiveness of the DEM technique and the full-scale input voltage is equal to 1 V. The ADC2 is a 4-bit quantizer, while DAC1 is a three-level (+1, 0, -1) digital-to-analog converter. The considered number of clock cycles is equal

to *256* in order to obtain a theoretical resolution of *12* bit.

Figure. 4.18 shows the simulated output spectra without (top) and with (bottom) one-shift DEM enabled. The simulations use a low frequency full-scale input signal with an amplitude of -3 dB and with a capacitor mismatch of 0.1% in the unit elements. The results are compared with that of a conventional first-order incremental ADC (with no parallel path) implemented with the standard DWA-based DEM algorithm. As shown, the mismatch makes the SNDR drop down to 63.16 dB (top), equivalent to 10.2 bit of resolution. Moreover, the harmonic tones limit the achievable spurious free dynamic range. The Conventional DEM technique (blue highlighted) improves the SNR to 71.9 dB (11.6 bits of resolution) reaching close to the ideal values. Also evident is the performance of one-shift DEM for the same mismatch improving the SNR to 69.8 dB or 11.3 bits of resolution.

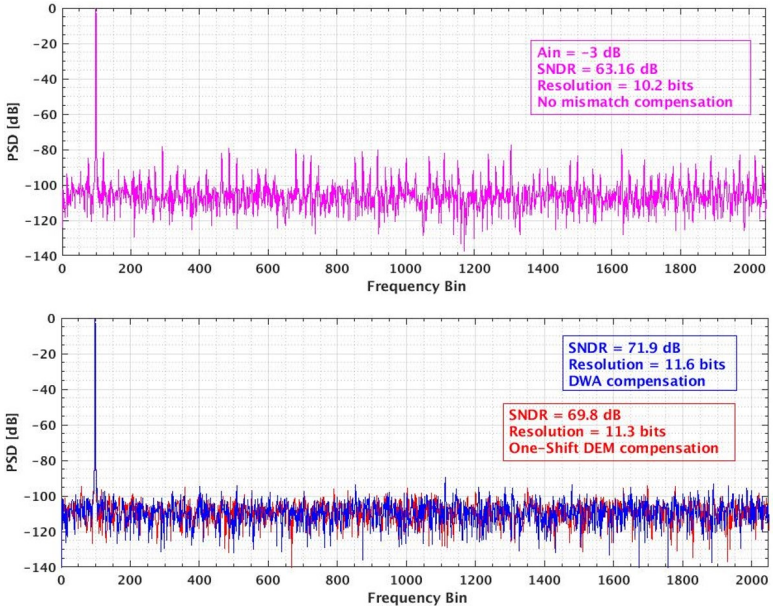

Figure 4.18: Simulated output spectra without and with (DWA, DEM) capacitance mismatch compensation.

For the integrated model, the $\Delta\Sigma$ ADC is also affected by the mismatch as it uses a 5-bit quantizer. However, since it processes the residual error from incremental block and generates the LSBs, the mismatch impact is minimal on the overall performance of ADC. Hence there is no severe need of any compensation for the DAC mismatch errors in $\Delta\Sigma$ block.

Figure. 4.19 shows the simulated output spectrum for a 1.36 kHz input signal with an amplitude of -1 dB input for the audio bandwidth of 24 kHz. The ADC model is simulated under under the condition of 0.2% random mismatch (capacitor mismatch) among the feedback DAC converter elements. The output spectrum shows the impact of that mismatch on the overall performance of ADC and its compensation through both conventional DWA and proposed one-shift DEM in the incremental block. As shown in the Figure. 4.19(top) the capacitance mismatch introduces harmonic distortion and increased noise floor reducing the overall SNDR to an average of 81 dB. With the implementation of both DWA and one-shift DEM the noise floor lowers by 15-20 dB, and also harmonic distortion reduces significantly which is compensated by both DWA and DEM separately. It is evident that one-shift DEM Figure. 4.19(bottom) demonstrates comparable performance with the conventional DWA technique by improving the SNDR to 101 dB as compared to the SNDR of 104 dB achieved by DWA.

4.8 Summary

The behavioral modeling of the hybrid ADC proposed in the previous chapter is done. Different variations and non-idealities including finite gain, limited speed and DAC variations have been introduced in the model to validate the functionality and performance of the proposed model in real-time audio application. A novel mismatch compensation technique termed as One-Shift DEM, has been in-

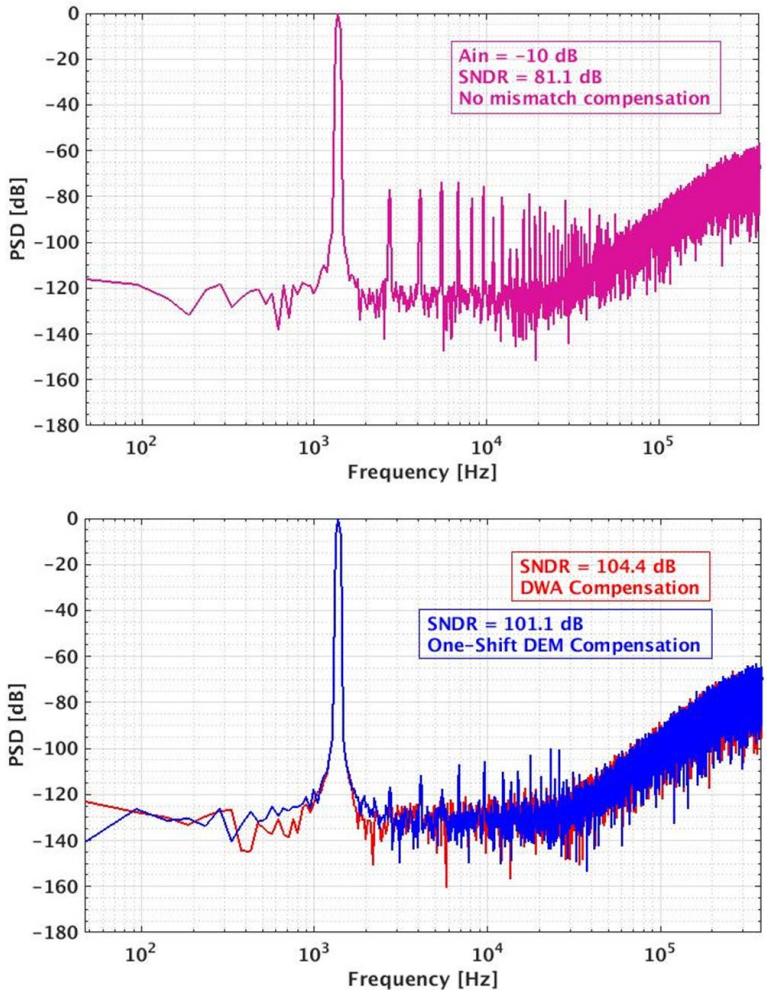

Figure 4.19: Simulated output spectra without(top) and with (DWA, DEM)(bottom) mismatch compensation for feedback DAC.

troduced in the Incremental DAC, since a small variation or mismatch has detrimental effect on the overall resolution of ADC. The performance of new compensation scheme has also been compared with that of standard DWA compensation technique to determine its effectiveness.

Chapter 5

Circuit Implementation

This chapter presents the transistor-level implementation of the Hybrid ADC, following the system-level design and Simulink model described in Chapter 4. The proposed Hybrid ADC consists of two main blocks i.e. 1^{st} order Incremental ADC and a 3^{rd} order $\Delta\Sigma$ modulator. The incremental ADC works at approximately 16 MHz while the $\Delta\Sigma$ modulator works at the sampling frequency of 576 kHz. The circuit is implemented in 0.18 μm CMOS process and targeting a DR of >100 dB at -60 dBFs input. Since Incremental ADC uses a multi-bit quantizer, a compensation technique of one-shift DEM is proposed for the parallel path to improve the DAC linearity. The chapter discusses the design of op-amps, DAC elements, multi-bit quantizer and its compensation, other supporting blocks and their simulation results of both incremental and $\Delta\Sigma$ ADCs.

5.1 Incremental ADC

This section discusses the transistor-level implementation of the 1^{st} order Incremental ADC which forms the front-end of Hybrid ADC. Figure. 5.1 shows the fully-differential schematic of the proposed Incremental ADC. A switched-capacitor design is implemented for the sampling and the feedback DAC. The

capacitors are shared by the non-overlapping clock between the input and the feedback DAC to prevent additional thermal noise. The Opamp is employed in a unity gain configuration with both sampling $C_{S(INCR)}$ and feedback capacitances $C_{FB(INCR)}$ of same value i.e. 8 pF. The thermometric code generated by the Flash ADC in both the residual and parallel path is fed back to the capacitive DAC to select the number of unit capacitances. The same thermometric bits are encoded into binary format to be combined off-chip with the binary output of $\Delta\Sigma$ ADC. The capacitor mismatch in the parallel path DAC is compensated by the DEM technique. Figure. 5.2 shows the waveform of the non-overlapping clock signals to enable the sampling and feedback network along with the reset of integrator. The integrator is reset at the sampling frequency "f_s" of 576 kHz; while the input is sampled at multiples of sampling frequency for each conversion. In addition, since the input frequency is quite low as compared to the sampling frequency so the input is assumed to be approximately constant between the two reset signal occurrences. In order to relax the slew rate and bandwidth requirements of the Incremental and $\Delta\Sigma$ Opamps, the last residue sampling/injection time that is used as an input for $\Delta\Sigma$ block is increased by two clock cycles at the cost of one less conversion. In addition, it also lowers the power consumption of the Opamp. The parallel path in the incremental ADC does not use any integrator, with the input signal being directly processed through the Flash ADC at a sampling frequency "f_s". However, the feedback operates at multiples of sampling frequency. The opamp in the integrator only sees a capacitive load and features a UGF of 100 MHz and a DC gain of 94 dB.

5.1.1 One-step Chopping

Since the opamps are affected by offset and low frequency noise which becomes more important for high gain opamps as is the case of incremental opamp. In

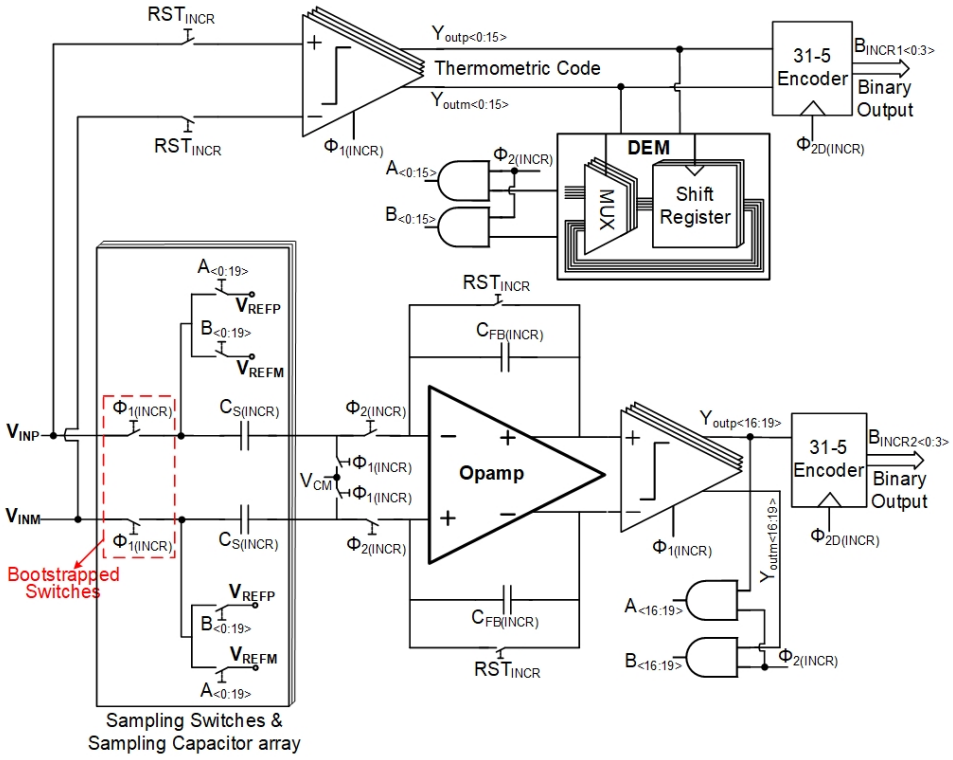

Figure 5.1: Switched-Capacitor implementation of proposed Incremental ADC.

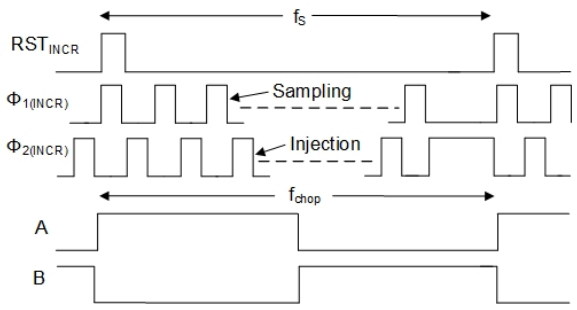

Figure 5.2: Waveform of the SC network and one-step chopping.

addition, even the low offset of the opamp gets accumulated along with the residual error until the integrator is reset. This accumulated offset may lead to an error that is greater than the LSB. So there is a need of some compensation or correction technique to reduce the opamp offset. The conventional schemes to reduce the opamp offset and low frequency noise are auto-zeroing [100], which involves sampling and canceling the offset and chopper stabilization [101–105] which involves modulating the input signal and offset to separate from each other in frequency domain. Since chopping stabilization does not use sampling and does not introduces noise folding, the resulting noise PSD is only slightly higher than the initial thermal noise floor. An efficient chopping reduces the offset over common-mode, time, temperature and die variations.

In the current scheme, the opamp offset and low frequency noise is compensated by the chopping technique that uses the polarity-reversing switches both at the input and output resulting in a ping-pong architecture [106, 107]. Figure. 5.3(a) illustrates the basic chopping technique involving the modulation of the signal to a high frequency, as done by multiplier M1 and then demodulating it to the baseband or dc at the output after multiplication, as done by multiplier M2. The modulating signal becomes a square wave signal, m(t) with a period T = $1/f_{chop}$, centered around zero for a shorted input. After the first modulation, offset and 1/f noise (Vos and Vn, respectively) corrupt the signal, but they are transposed to high frequency by the action of M2. Figure. 5.3(b)-(d) depicts the spectra of the signal involved in the relevant points of the processing chain. The frequency noise added to input of A1, modulated by M2 and replicated at multiple of f_{chop}, is lowpass filtered by the finite bandwidth of A1. Figure. 5.4 shows the Opamp architecture, in which multipliers M1 and M2 are implemented by polarity-reversing switching network "$Chop_{In}$" and "$Chop_{Out}$" operating with the non-overlapping clocks "A" and "B" in Figure. 5.2.

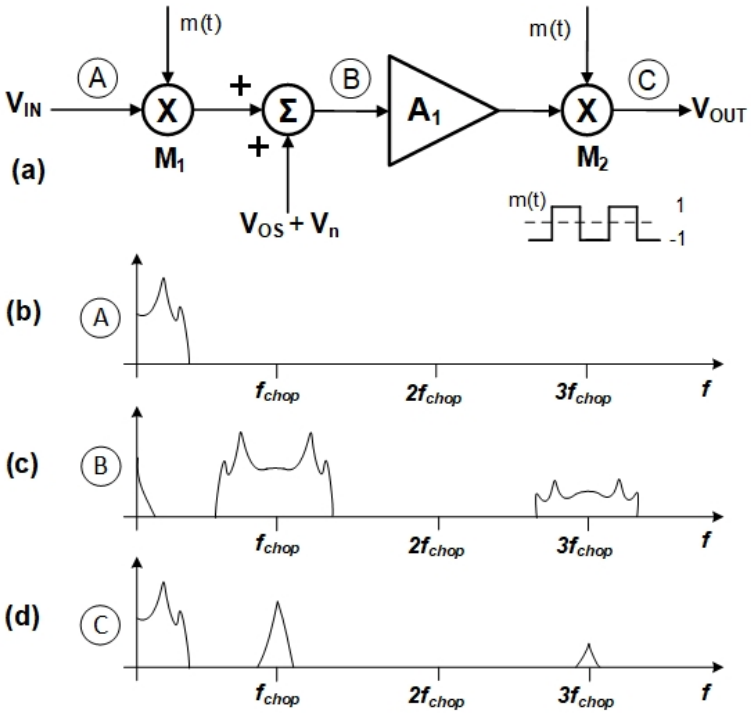

Figure 5.3: Chopper technique basic scheme.

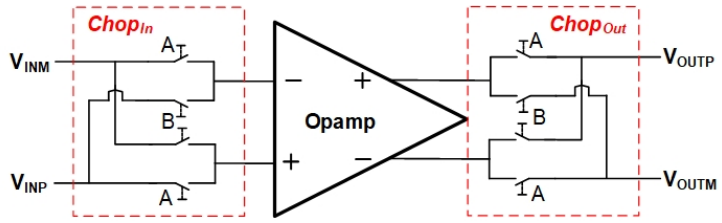

Figure 5.4: Opamp with chopping technique.

5.1.2 Bootstrapped Sampling Switch

One of the major issues in SC circuits is the designing of analog switches of the front-end sampling network. The front-end of SC circuits consists of sampling network that uses analog switches to sample the input on the sampling capacitors in discrete time. One of the major challenges in the design of analog switches is their capability to transmit full swing signals without any significant signal distortion [108, 109] which occurs because of variation in the signal-dependent on-resistance of switches. This issue becomes more severe at low-voltage operations. One of the reported techniques to overcome this problem is the implementation of switched opamp [110, 111] at the cost of either low circuit speed or higher power consumption. Another alternate is using the clock-boosting technique termed as clock bootstrapping that boost or increase the gate voltage of switch in proportion to the amplitude of input signal. This technique is usually preferred since it maintains a constant switch resistance, effectively reducing the signal distortion [112–116]. For the required specifications, the minimum signal that needs to be processed is -60 dB, so there is a need of some clock boosting circuit to reduce the signal distortion to at least -100 dB. In the current scheme, Dessouky bootstrap circuit [113]has been used to eliminate the input signal distortion. Figure. 5.5 shows the bootstrap logic that has been used and drives all the unit input switches of the sampling network.

5.1.3 Incremental Opamp

As mentioned earlier that the incremental opamp requires high gain $\geq$ 94 dB and higher UGF $\geq$ 100 MHz though can tolerate very limited output swings. One of the topologies to achieve high gain, UGF and output swing are two-stage class AB opamps [117, 118] but require a proper frequency compensation to ensure stabil-

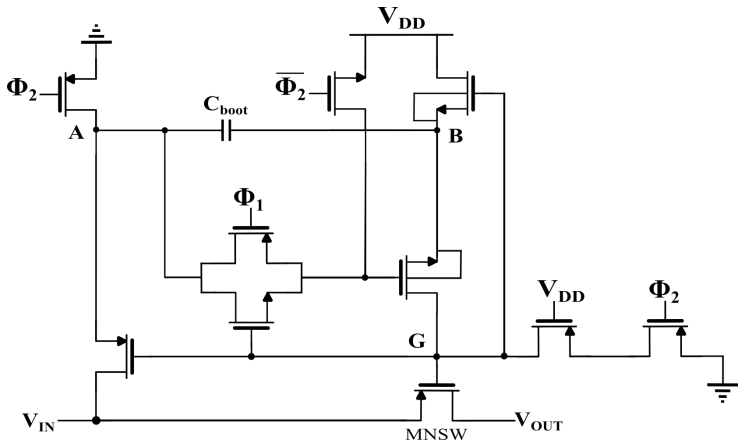

Figure 5.5: Input switch using bootstrap logic for sampling input.

ity and higher power consumption to achieve high speeds. Single-stage opamps including telescopic and folded cascade topologies are power efficient and can achieve higher UGF but can only achieve moderate gains $\leq$ 80 dB because of limited intrinsic gains of the devices. Moreover these topologies are also affected by limited output swings because of cascode devices in the output branch. Their gain can be increased by using gain-boosting techniques [119, 120] for the cascade devices without affecting the UGF, but existence of pole-zero doublet affect the settling performance of the opamp and also introduces instability if not compensated properly. The technique requires auxiliary amplifiers to provide negative feedback for the cascode devices adding much complexity and poles in the system. In the current incremental scheme, the opamp needs high gain and UGF, but requires very low output swings; thanks to the parallel architecture. To achieve the required specifications, a folded-cascode structure has been used that fulfill the bandwidth requirements but lacks the required DC gain. In order to compensate for the gain, an extra cascode device has been added in the output branch that enhances the gain by increasing the output resistance. As opposed to conventional gain-boosting technique this cascode device does not require any auxiliary

opamps for biasing and feedback; instead the extra cascodes are also biased with a constant bias voltage to keep them in saturation. The cost for this additional device is a further decrease in the output swing which can be easily tolerated since the actual output swing requirement is quite low. The advantage of this architecture is its implementation as a single-pole system in the desired frequency range, which is inherently stable as the non-dominant poles are located at very high frequencies. Figure. 5.6 shows the schematic diagram of the folded cascade opamp with the additional cascode devices. The additional cascode transistor pairs (M_7, M_8,M_9,M_{10}) adds to the output resistance of the Opamp aiding to achieve high gain. The gain expression for the folded cascode with the addition of extra cascade device biased with a fixed voltage (half-circuit) is given by

$$A_v = g_{m1}[(g_{m8}g_{m6}r_8r_6r_4)//(g_{m10}g_{m12}r_{10}r_{12}(r_1//r_{14}))] \tag{5.1}$$

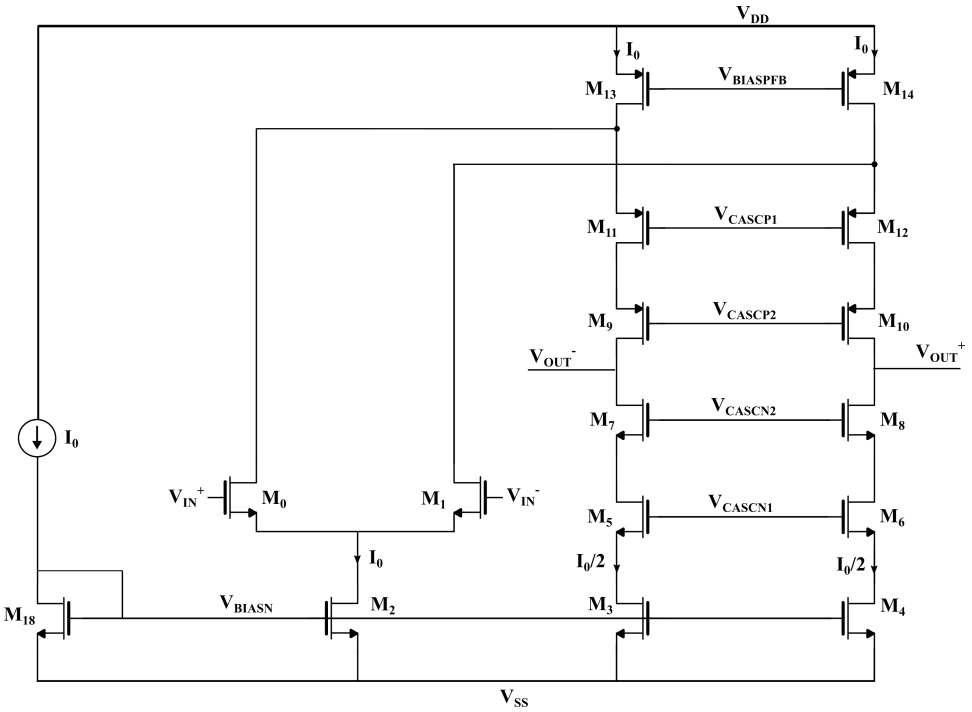

Figure 5.6: Folded-double Cascode Opamp.

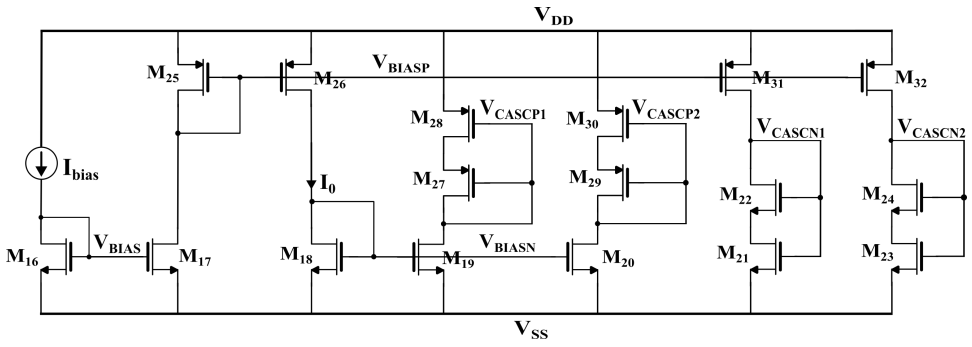

Figure 5.7: Biasing Network for Incremental Opamp.

The biasing network to generate the current and voltage biases for the cascode devices and current mirrors is shown in Figure. 5.7. The Opamp being fully differential requires common-mode feedback (CMFB) to maintain the common mode at the desired level. Figure. 5.8 shows the conventional dynamic SC-CMFB that has been used for the differential Opamp. This scheme has the advantage of saving static power consumption but provides an extra capacitive load to the Opamp along with charge injection of the CMFB switches. SC-CMFB operates at the same frequency of the incremental Opamp. The Opamp should be simulated in the actual feedback configuration in order to get its actual frequency response [121–123]. The Incremental Opamp perceives a capacitive load of 2 pF that includes the input sampling capacitance of $\Delta\Sigma$ and Quantizer. In addition it is loaded by the integration and feedback capacitance of 8 pF. Figure. 5.9 illustrates the post-layout simulated loop gain, GBW and the phase margin of the Opamp in the presence of integration and feedback capacitances. As shown, the Opamp achieves a gain of 94 dB, 54° PM and UGF of 110 MHz in the presence of all possible loads. The Opamp uses a bias current of 150 μA. The simulated slew rate (SR) of the Opamp is >60 V/μsec. The total current consumption of the Opamp including the bias circuit is <1.5 mA. For the same DC gain and slew rate, a two-stage class AB Opamp utilized 2.8 mA operated under the same conditions.

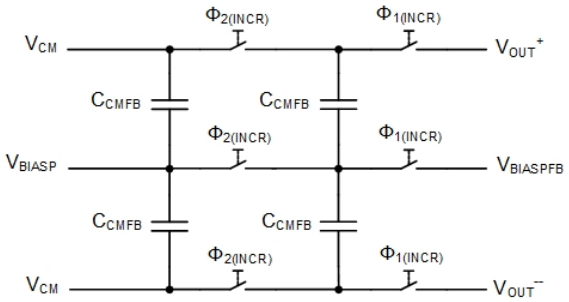

Figure 5.8: SC-CMFB network for Incremental Opamp.

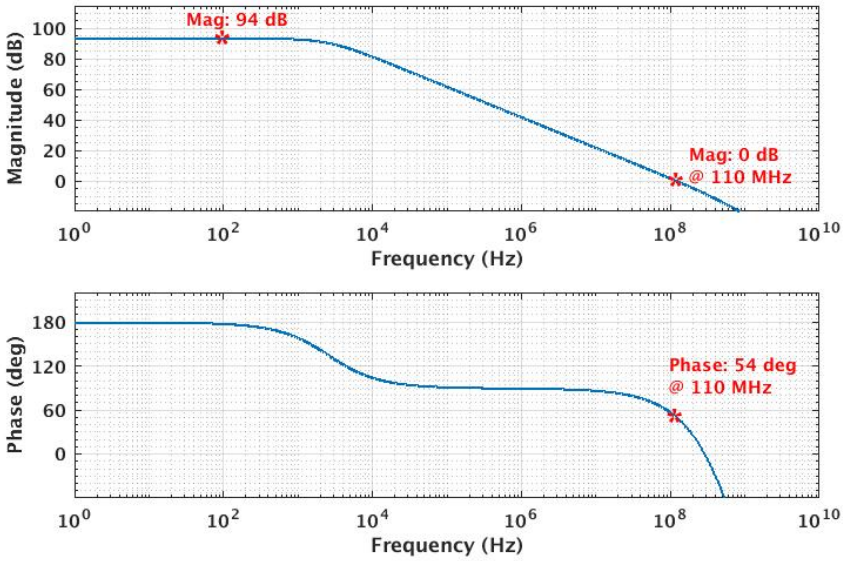

Figure 5.9: Post-layout closed loop Gain and Phase Margin of Incremental Opamp.

5.1.4 Flash ADC

Because of the additional parallel path, two Flash ADCs have been used in the Incremental ADC. The parallel path Flash ADC is composed of 15 comparators and registers to generate the thermometric code for the feedback DAC. This Flash ADC is followed by the DEM logic to compensate for the DAC non-linearity. The reference voltages are generated through a thermometric resistive ladder. Unsilicided P^+ polysilicon resistors have been used for achieving better matching accuracy in the resistive string. Compared to the silicided polysilicon, these resistors provide lower sheet resistance resulting in a lower area occupation for the references. Figure. 5.10 shows the conceptual illustration of the Flash architecture used in the design.

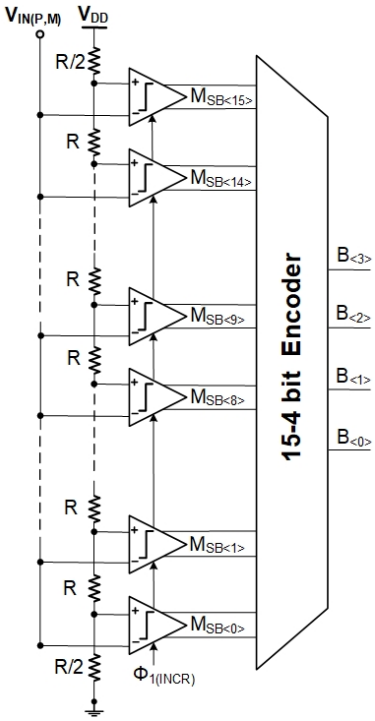

Figure 5.10: Flash ADC Architecture.

The other Flash ADC which processes the residual error from the integrator

uses the same references as that of the parallel Flash but uses only 4 comparators across the common-mode. It only digitizes the residual error which is not more than 2 bits and does not strictly need compensation for DAC non-linearity. The thermometric code generated by the two Flash ADCs is converted into binary format for post processing.

5.1.5 Comparator

Since the incremental ADC operates at multiples of sampling frequency, the quantizer has a limited decision time for the comparison and feedback. In addition, the kickback noise in the comparator distorts the input signal resulting in a wrong decision. Keeping in view these limitations, a three-stage preamplifier-based comparator followed by a latch has been used in the Flash ADC as shown in Figure. 5.11. The pre-amplifier, which is a simple differential pair with diode-connected load, improves the sensitivity to small input signals and suppresses the kick-back noise from the sampling clock. Another cascade stage is added to further enhance the gain of the preamplifier which is followed by the dynamic latch. The comparator uses NMOS input pairs because of their higher mobility as compared to their PMOS counterparts. The dynamic latch or the decision circuit consists of cross-coupled PMOS and NMOS transistors and is controlled by the clock. The circuit uses the positive feedback through this cross-coupling to increase the gain of the circuit so that it can differentiate between very small signals in the range of few mV. The pre-amplifier and the cascade stage is biased at a static current of 20 μA and as shown in Figure. 5.12, the pre-amplifier stage (1st stage) provides a DC gain of 27 dB and bandwidth of 1.2 GHz for a maximum capacitive load of 50 fF, which is an estimation of input capacitor for the 2nd stage).

The behavior of the comparator depends on the actual device parameters, especially their matching. This effect can be modeled with an error signal added to

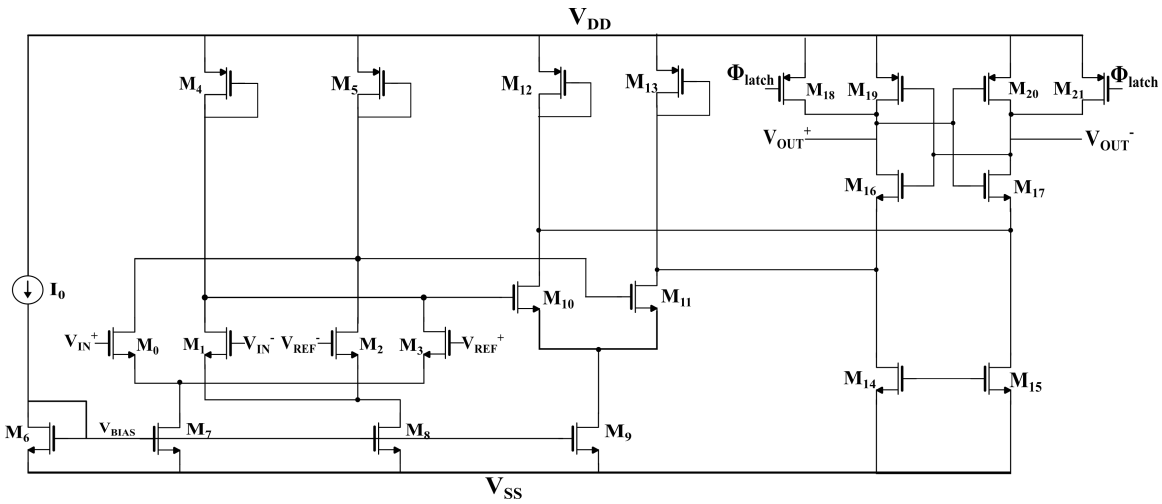

Figure 5.11: Schematic of Pre-amplifier based Comparator.

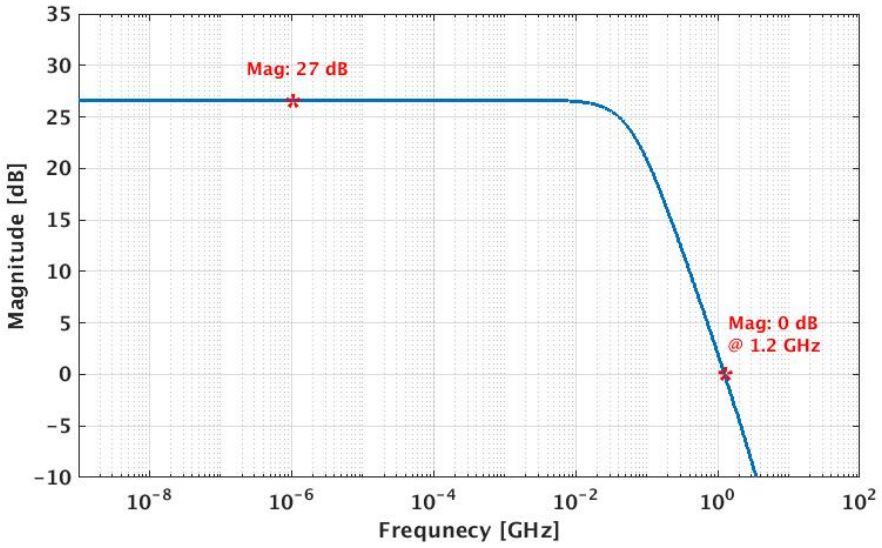

Figure 5.12: AC simulation of the preamplifer of the Comparator.

the comparator input, identified as input referred offset "V_{OS}". The comparator offset imposes a fundamental limit on the achievable performance. Monte Carlo simulations are conventionally used to estimate this static offset due to mismatch. Figure. 5.13 shows the result of 500-runs monte carlo simulation for the comparator to determine the offset.

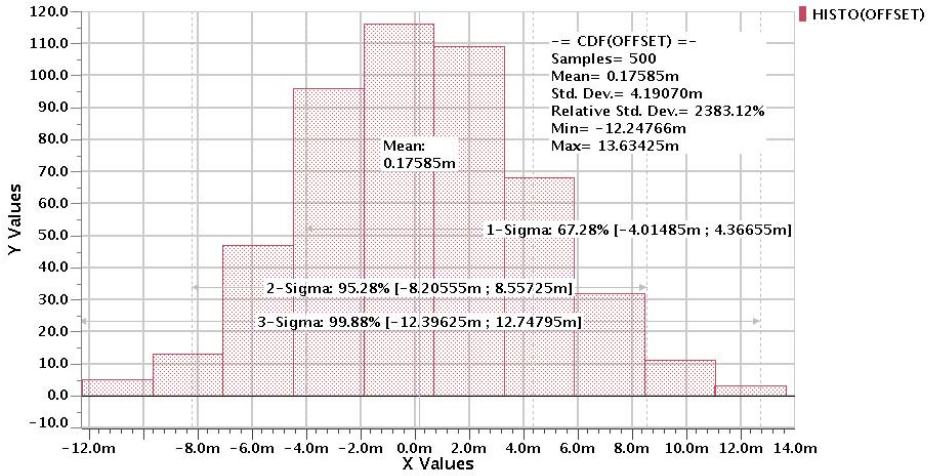

Figure 5.13: Monte Carlo simulation results for offset of Comparator.

5.1.6 Post-layout Simulation Results

Figure. 5.14 shows the layout of the Incremental ADC that includes the sampling network with bootstrap switches, Opamp, sampling and feedback capacitances and Flash ADC and is implemented in 0.18 μm CMOS process technology and occupies an area of 0.51 mm^2. Figure. 5.15 shows the post-layout simulated output spectrum results of the incremental ADC for an input of -1 dB. The circuit achieves an SNDR of 50.81 dB translating into a resolution of 8.15 bits.

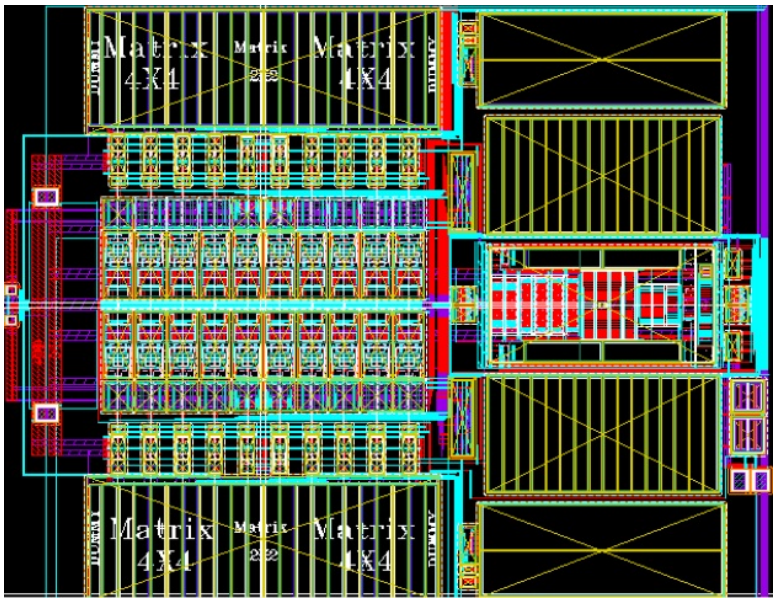

Figure 5.14: Layout of the Incremental ADC

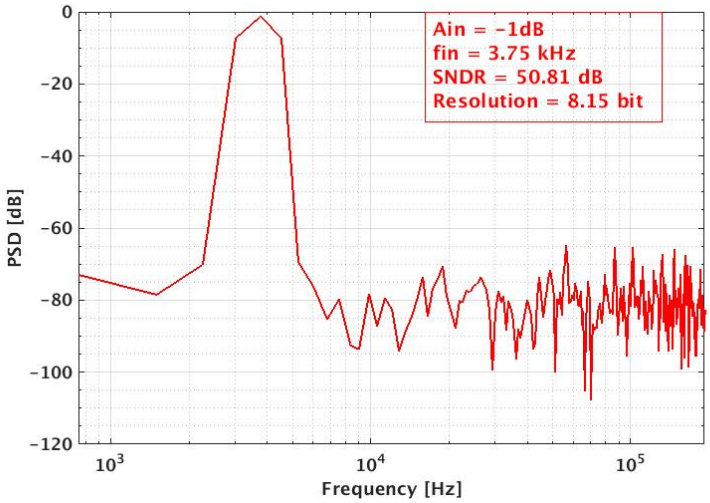

Figure 5.15: Post-layout simulated output spectra of Incremental ADC for -1 dBFs input

5.2 $\Delta\Sigma$ ADC

This section discusses the transistor-level implementation of the 3^{rd} order $\Delta\Sigma$ ADC which forms the secondary block of Hybrid ADC. As mentioned earlier, a cascade of integrators with distributed feedback (CIFB) topology with capacitive input feed-forward (CIFB-CIF) is implemented where the input is added at the input of second integrator. This summation of the input can also be done at the quantizer input but it increases the circuit complexity and power consumption [124]. The input feed-forward topologies are more attractive for low OSR designs since they impact the speed of the modulator, which is not an issue in the current case where the modulator is targeting the audio range. The STF of the modulator acts as a low-pass filter while the NTF demonstrates a third-order high-pass response. In addition the non-idealities at the output of the third integrator become less effective as they are third-order noise shaped when referred back to the input. Since the $\Delta\Sigma$ needs to process only the residual error whose maximum swing is not more than 2 incremental LSBs, so a very low input and output range is required for the Opamps. These Low op-amps swings enable relaxed slew-rate requirements, better linearity, lower power consumption, and allow operation at lower power supply voltages [125]. Figure. 5.16 shows the fully-differential schematic of the $\Delta\Sigma$ ADC used in the design while Figure 5.17 shows the timing waveforms for sampling the residue relative to the incremental waveforms. The thermometric code generated by the Flash ADC is fed back to the capacitive DAC to select the number of unit capacitances. The gain configuration is implemented by the capacitive ratio between sampling and feedback capacitances in all three stages, so each stage is implemented by a separate feedback DAC with different unit size capacitances. The same thermometric bits are encoded into a 5-bit binary format to be combined off-chip with the two 4-bit binary outputs of Incremental ADC after two clock delays. Being in the second stage of processing to generate

the LSBs, the Opamps in $\Delta\Sigma$ ADC require relatively relaxed gain and bandwidth requirements. The capacitance mismatches in the DAC does not pose a serious threat to the linearity of the system, so the Flash can be implemented without any compensation technique preserving the area and power consumption.

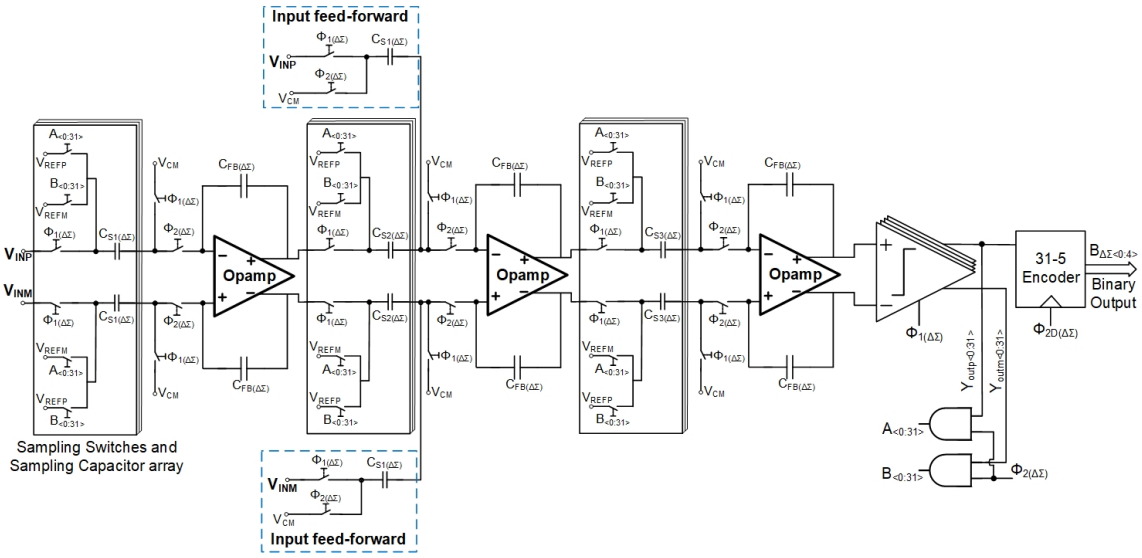

Figure 5.16: Switched-Capacitor implementation of proposed $\Delta\Sigma$ ADC.

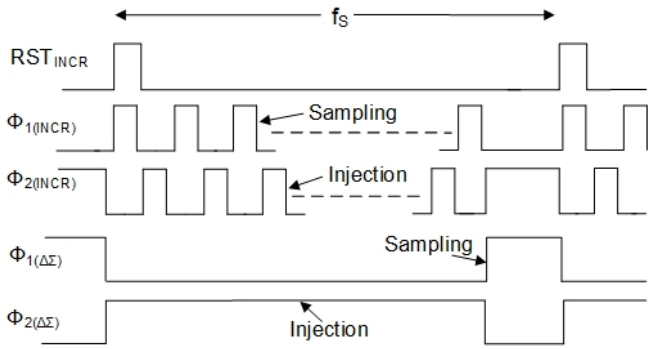

Figure 5.17: Waveform of the $\Delta\Sigma$ network.

5.2.1 $\Delta\Sigma$ Opamp

For $\Delta\Sigma$ ADC, all the three stages use the same Opamps since there is a small difference in the minimum requirements for each stage. The 3^{rd} stage Opamp requires a minimum gain of 60 dB and UGF 40 MHz. Output swing requirements are quite relaxed even for the 3^{rd} stage Opamp. In order to achieve the required specifications, single-stage Opamps can be used. Both telescopic and folded-cascode topologies qualify to fulfill the requirements. Folded cascode amplifier has the advantage of large output swing and higher gain compared to the ordinary op-amp albeit at higher power consumption. In addition, it is very suitable for deep negative feedback because of its small signal gain that can be very large. Figure. 5.18 illustrates the schematic design of the proposed folded-cascode Opamp. The Opamp uses NMOS input pair to have better mobility and achieve the speed requirements with less power consumption. The gain expression for the folded cascode biased with a fixed voltage (half-circuit) is given by

$$A_v = g_{m_1}[(g_{m_6}r_6r_4)//(g_{m_{10}}r_{10}(r_1//r_{14}))] \tag{5.2}$$

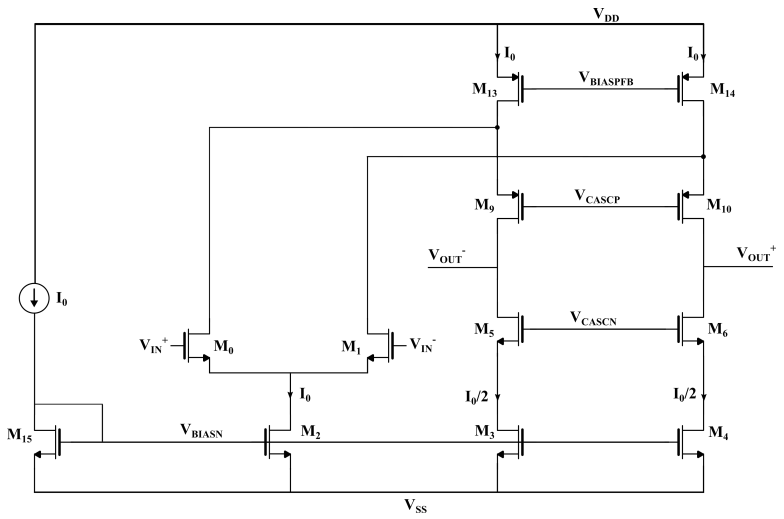

Figure 5.18: Folded cascode Opamp for $\Delta\Sigma$ ADC.

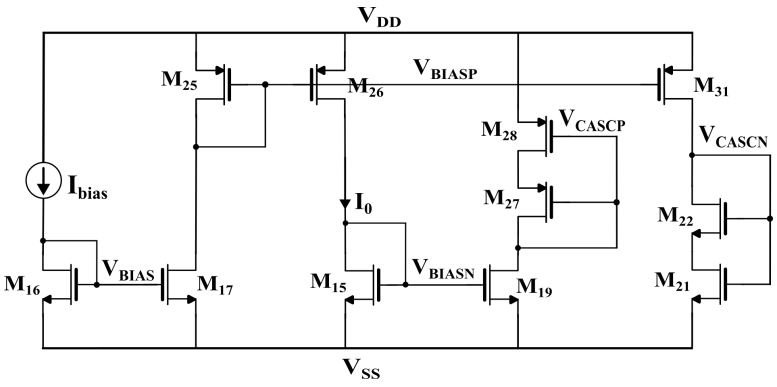

Figure 5.19: Biasing Network for $\Delta\Sigma$ Opamp.

The biasing network to generate the current and voltage biases for the cascode devices and current mirrors is shown in Figure 5.19. To maintain the common-mode of the Opamp at the desired level the same conventional dynamic SC-CMFB is employed that has been used for the incremental Opamp and illustrated it in Figure. 5.8. This SC-CMFB operates at the same frequency of the $\Delta\Sigma$ Opamp.

Each $\Delta\Sigma$ Opamp perceives a different capacitive load depending upon its position in the circuit. Combined with the feedback capacitance of 2 pF in all three stages, the maximum capacitance seen by any of the three Opamps is 2 pF, however as shown in Figure. 5.17 the Opamps require approximately 80% of the duty cycle to drive that load, so the slew rate and bandwidth requirements are quite relaxed for these Opamps. Figure 5.20 illustrates the post-layout simulated loop gain, GBW and the phase margin of the Opamp in the presence of integration and feedback capacitances. As shown the Opamp achieves a gain of 76 dB, 64° PM and UGF of 100 MHz in the presence of all possible loads. The Opamp uses a bias current of 50 μA. The simulated slew rate (SR) of the Opamp is >30 V/sec. The total current consumption of the Opamps including the bias circuit is approximately 0.9 mA.

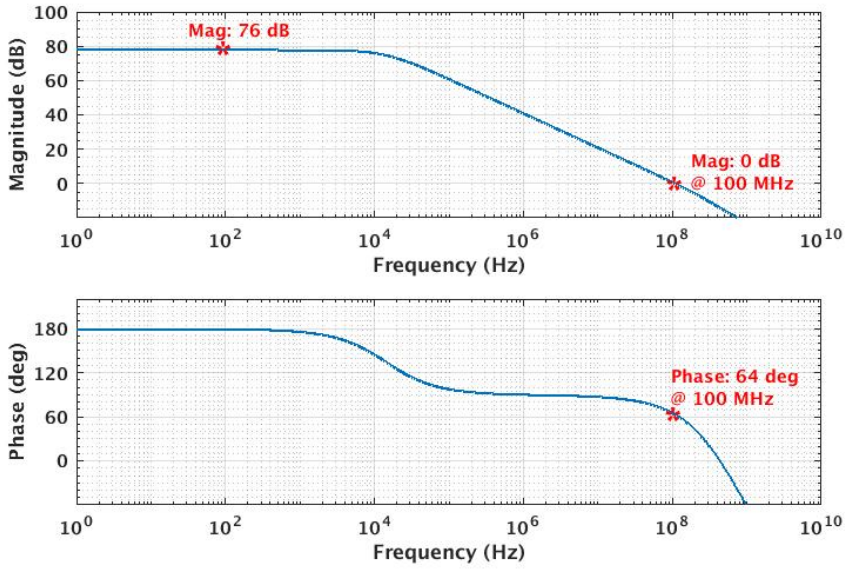

Figure 5.20: Post-layout closed loop Gain and Phase Margin of $\Delta\Sigma$ Opamp.

5.2.2 Flash ADC

The three cascaded delayed integrators are followed by a 5-bit Flash ADC which generates a 32-bit thermometric code for the three DACs in the feedback. The thermometric code is fed back to the DACs without any compensation for capacitance mismatch. The reference voltages are generated through a thermometric resistive ladder connected with the power supply i.e. V_{DD} and V_{SS}. The variations in the power supply (V_{DD}) are compensated by the introduction of voltage regulators (LDO) externally. These LDOs ensure a relatively clean supply and aids in accurate reference generation. The comparator topology used in the Flash ADCs for Incremental block is reused, but with less bias current to reduce power consumption. Instead of 32 comparators, the design uses only 16 comparators since the maximum output signal swing from the 3^{rd} cascaded integrator is less than 6-bits. 8 LSBs of the thermometric code are directly connected to "V_{DD}" since these are high in all instances of outputs, while 8 MSBs are constantly connected

to "V_{SS}" since these bits are always low for all instances of outputs. This technique saves area and power consumption by half as compared to conventional Flash ADC.

5.2.3 Post-layout Simulation Results

Figure. 5.21 shows the layout of the $\Delta\Sigma$ ADC that includes the sampling network with bootstrap switches, three Opamps, sampling and feedback capacitances and Flash ADC and implemented in 0.18 μm CMOS technology and occupies an area of 0.61 mm^2. Figure. 5.22 shows the post-layout simulated output spectrum of the $\Delta\Sigma$ ADC for a 3.75 kHz input with an amplitude of -10 dB, where it achieves an SNDR of 76 dB.

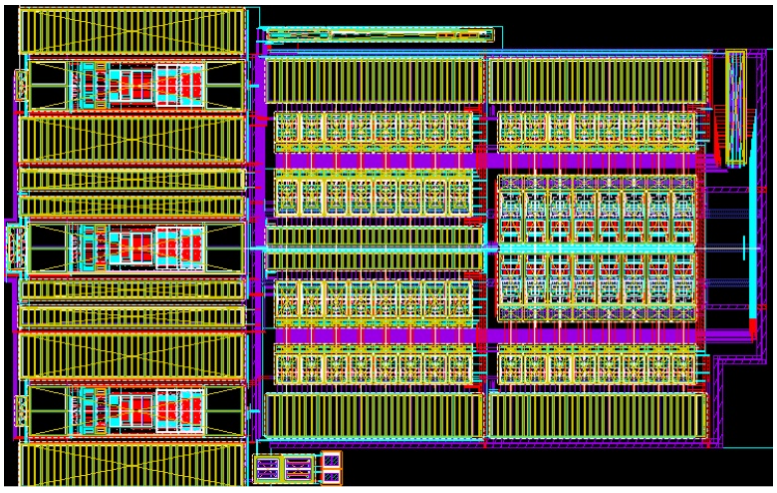

Figure 5.21: Layout of the $\Delta\Sigma$ ADC

5.3 Digital Control

The analog components of the ADC are supported by various digital blocks that control the functionality and selection of different configurations under certain

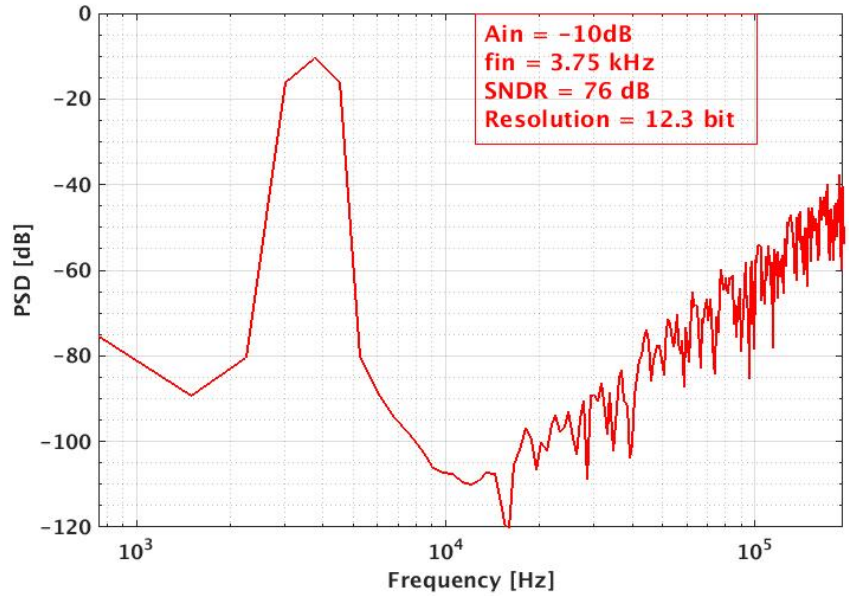

Figure 5.22: Post-layout simulated output spectra of $\Delta\Sigma$ for -10 dBFs input

operating conditions. Since both incremental and $\Delta\Sigma$ integrators are operating in discrete-time, so non-overlapping clocks are necessary for their sampling circuit. Both incremental and $\Delta\Sigma$ Opamps employ SC-CMFB to maintain common-mode, so they also need non-overlapping clocks for their proper operation. In addition the thermometric code generated by both 4-bit and 5-bit Flash ADC requires thermometric-to-binary encoders along with output buffers to drive the pins and off-chip capacitive loads. Another control circuit is added to align the sampling of the residual output of incremental integrator by the $\Delta\Sigma$ modulator. Figure. 5.23 illustrates the timing waveform generated by the digital block for control signals and data availability from both incremental and $\Delta\Sigma$ blocks.

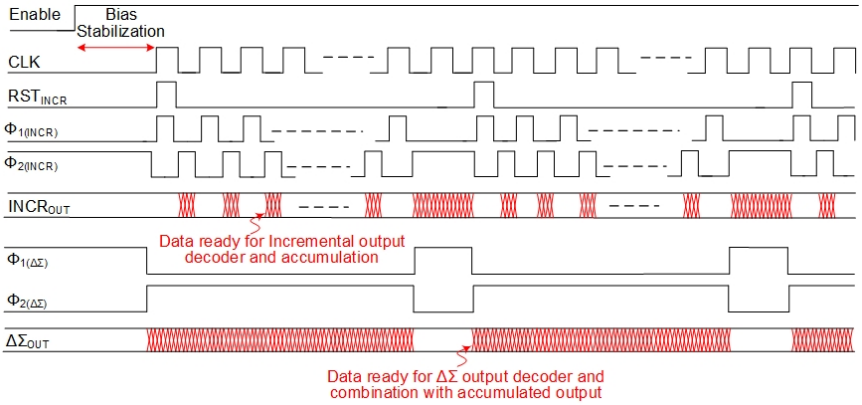

Figure 5.23: Timing signals generated by the digital control block for different functions of ADC blocks.

5.4 Post-Layout Simulation

Figure. 5.24 and Figure. 5.25 show the post-layout simulated output spectrum results of the integrated hybrid ADC for a 3.75 kHz sinusoidal input of -1 dB and -60 dB respectively. The input sinusoid is generated by an ideal source without the presence of any noise source, while a series resistance of 500 Ω is added to the power supply to include the effect of wire resistance and voltage drops. The digital output from both blocks is sampled and combined in Matlab. The circuit achieves peak SNDR of 99 dB for -1 dBFs input and an SNDR of 51 dB for -60 dBFS input over the audio bandwidth of 24 kHz. The dynamic range obtained through these simulations is 113 dB. The total simulated power consumption of the integrated circuit is 7.16 mW. Main current consuming blocks are the incremental Opamp and three $\Delta\Sigma$ Opamps with approximately 50% share of overall current consumption of the circuit.

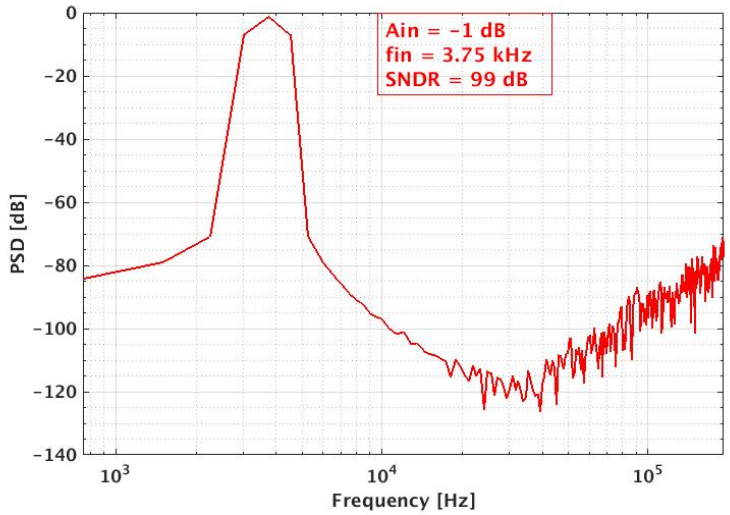

Figure 5.24: Post-layout simulated output spectra of Hybrid ADC for -1 dBFs input

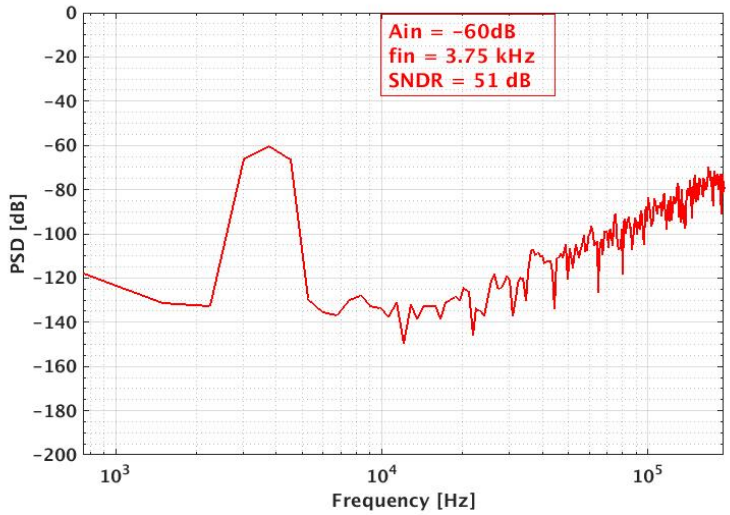

Figure 5.25: Post-layout simulated output spectra of Hybrid ADC for -60 dBFs input

5.5 Summary

The transistor-level implementation of the proposed design is discussed in this chapter. The Opamp topologies used in Incremental and $\Delta\Sigma$ blocks have been discussed in detail. Other features including, chopping and bootstrap logic that has been used in the Incremental block. The compensation technique to compensate for the DAC non-linearity in the feedback has also been discussed. The validity of the design is supported by the post-layout simulation results of Incremental, $\Delta\Sigma$ ADC and their integrated design.

Chapter 6

Measurement Results

An experimental prototype is essential for the verification of the design and investigate its functionality and suitability in the real-world environment. The chapter gives an overview of the ADC testing, measurement setup and the results obtained.

6.1 Test-chip and Board Design

The proposed extended-range Hybrid ADC, modeled and designed in the previous chapters, was fabricated in a BCD9 (0.18 μm CMOS) process offered by STMicroelectronics. The ADC has an active area of 1.2 mm^2 (1810 μm $\times$ 660 μm) excluding the I/O pads. Figure. 6.1 shows the micrograph of the integrated circuit (IC) with annotated active area of the ADC. The die of the ADC IC was packed in a TQFP package with 48 pins.

The two 4-bit binary outputs from the Incremental ADC and 5-bit binary output from $\Delta\Sigma$ along with some control signals were provided and captured at separate pins. Some voltage and current references were provided externally. Separate battery and ground connections (with sufficient bond-wire separation) were provided to noise sensitive circuit blocks on the die. The reference voltages for the Flash ADCs were internally generated in the IC.

A four layered test PCB was designed and fabricated to evaluate the performance of the ADC. The board was equipped with two LDOs to regulate and maintain a constant supply both for the board components and DUT. Ceramic capacitors with few additional SMD capacitors were used to filter the power supply and voltage references. Separate switches were provided for the digital control to allow for different configuration settings including separate testing of ADC blocks, to enable/disable DEM and chopping in incremental opamp. Off-chip bias resistors and potentiometers were used to control the bias currents for OTAs. In addition, the common-mode voltages required for the OTAs were generated using off-chip resistive dividers. The populated PCB with the mounted IC is shown in Figure. 6.2.

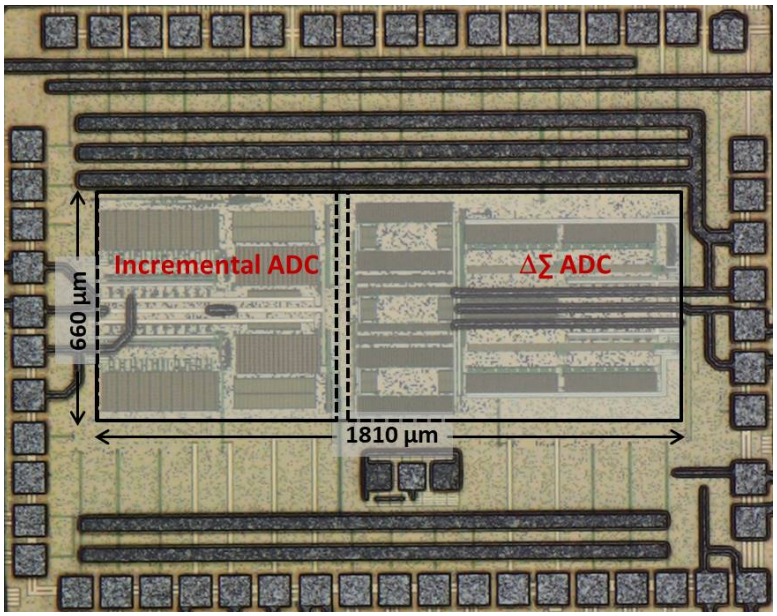

Figure 6.1: Micrograph of the chip showing the active area of the ADC

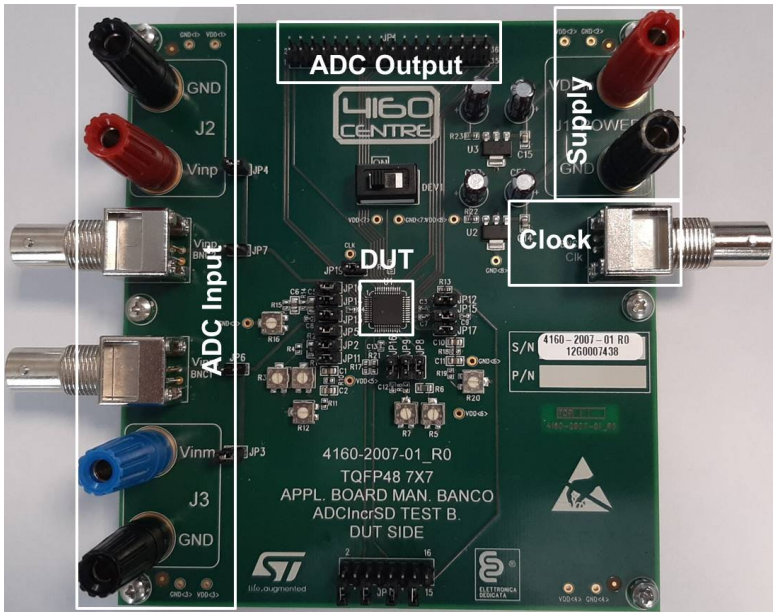

Figure 6.2: Test PCB used to evaluate the ADC

6.2 Measurement Setup

The measurement set up used for the performance evaluation of ADC is shown in Figure. 6.3. The power supply was provided using a programmable R&S supply. An external Tektronix function generator AFG-3102 was used to feed the clock signal. The differential input signal was provided by an Audio Precision source SYS-2722, while the Lecroy-WaveRunner high definition mixed-signal oscilloscope was used to capture the output bits of Hybrid ADC. External resistors and potentiometers were used for the load transient and references. The output bits captured by the oscilloscope were further processed in Matlab for the frequency response. For spectral analysis, a 2^{10}-points FFT with Hanning window has been used. Reason for using small number of points is the limited memory of mixed-signal oscilloscope.

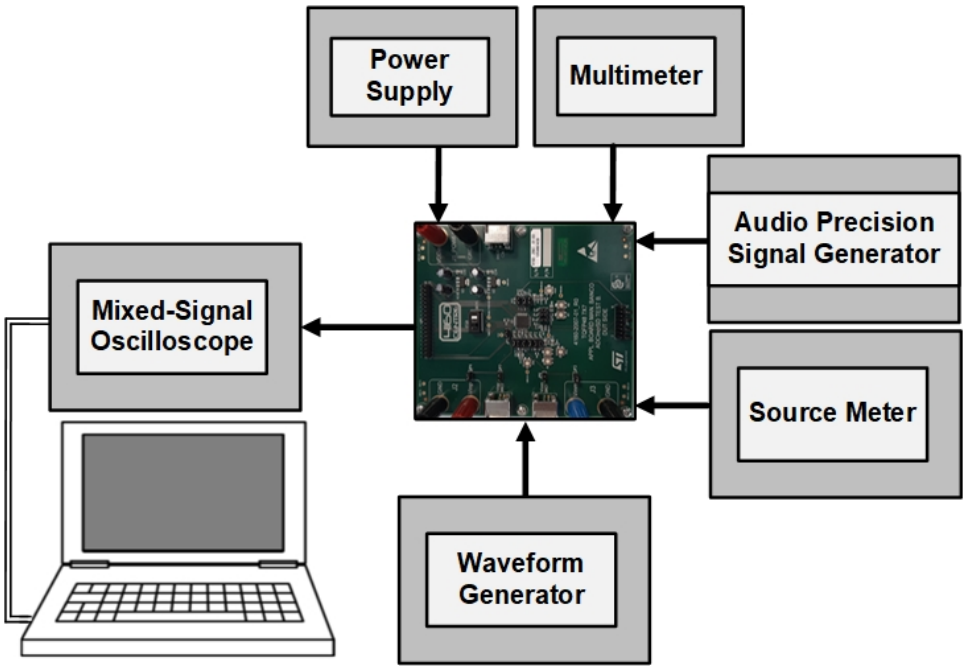

Figure 6.3: Test setup for the evaluation of the ADC

6.3 Measurement Results

Being the first prototype, both Incremental and $\Delta\Sigma$ blocks were characterized separately in order to have in-depth analysis before the integrated ADC characterization.

6.3.1 Incremental ADC

Figure. 6.4 shows the micrograph of Incremental ADC with annotated details. The standalone testing of the Incremental ADC was done by sweeping the input from -50 dB to -1 dB. Figure. 6.5 shows the measured SNDR of the Incremental ADC for a 2.8 kHz input of -2 dB amplitude. As shown, the Incremental ADC achieves SNDR of 49.72 dB translating into 7.98 bits of resolution.

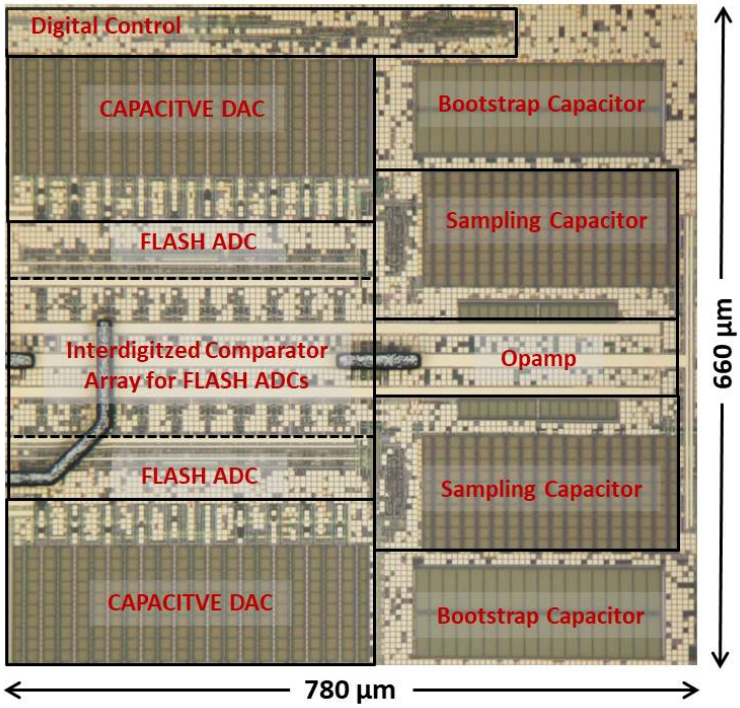

Figure 6.4: Micrograph of Incremental ADC

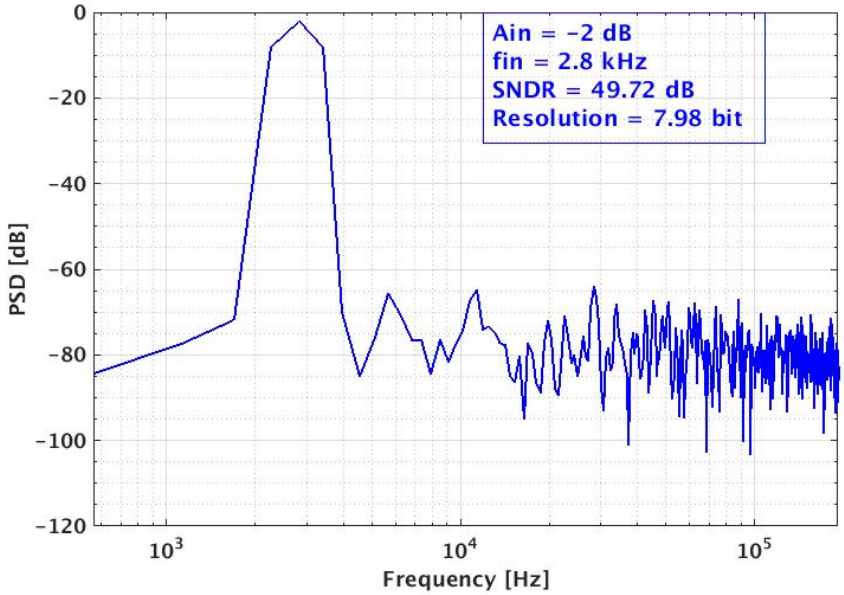

Figure 6.5: Measured output spectra of Incremental ADC for -2 dBFs input amplitude

6.3.2 Delta-Sigma ADC

Figure. 6.6 shows the micrograph of $\Delta\Sigma$ ADC with annotated details. The standalone testing of $\Delta\Sigma$ ADC was done by sweeping the input from -50 dB to -10 dB. Reason for this small input range is that since the Flash ADC in $\Delta\Sigma$ block uses only 16 comparators instead of 32. Figure. 6.7 shows the measured SNDR of the $\Delta\Sigma$ ADC for an input of -20 dB.

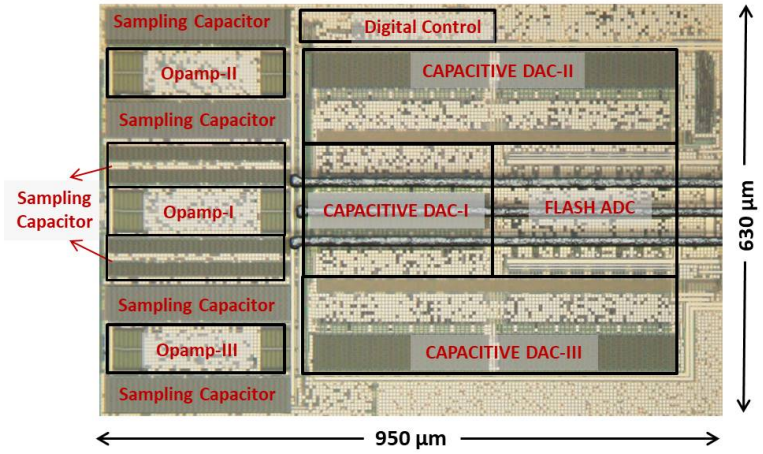

Figure 6.6: Micrograph of Delta-Sigma ADC

6.3.3 Hybrid ADC Measurements

Figure. 6.8 shows the measured power spectral density (PSD) of the combined output of hybrid ADC for a 2.8 kHz sinusoidal input of -2.4 dBFs, exhibiting a peak SNDR of 94.45 dB, SFDR of 103 dB and an ENOB of 15.4 bits, while Figure. 6.9 shows the measured SNDR for the same sinusoidal input with an amplitude of -60 dBFs. Figure. 6.10 shows the measured output SNDR for input, ranging from -2 dB to -60 dB over the intended frequency range.

Figure. 6.11 shows the SNR/SNDR as a function of input amplitude with an input frequency of 2.8 kHz. The proposed ADC achieves a dynamic range

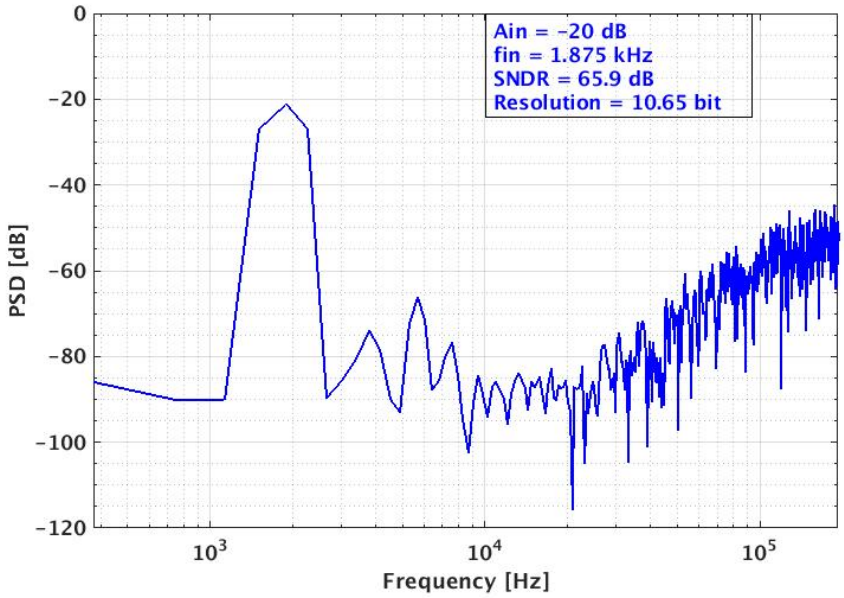

Figure 6.7: Measured output spectra of $\Delta\Sigma$ ADC for -20 dBFs input amplitude

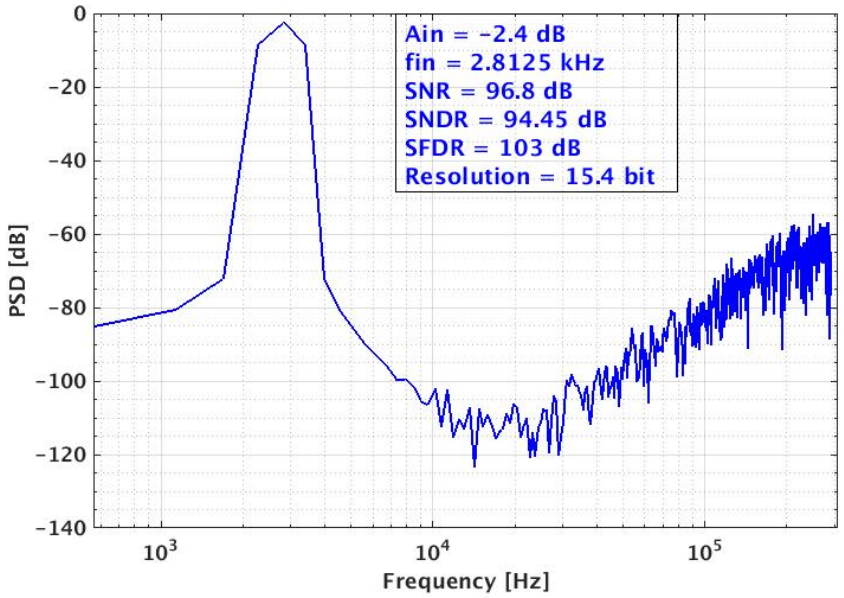

Figure 6.8: Measured output spectra of Hybrid ADC for -2.4 dBFs input amplitude

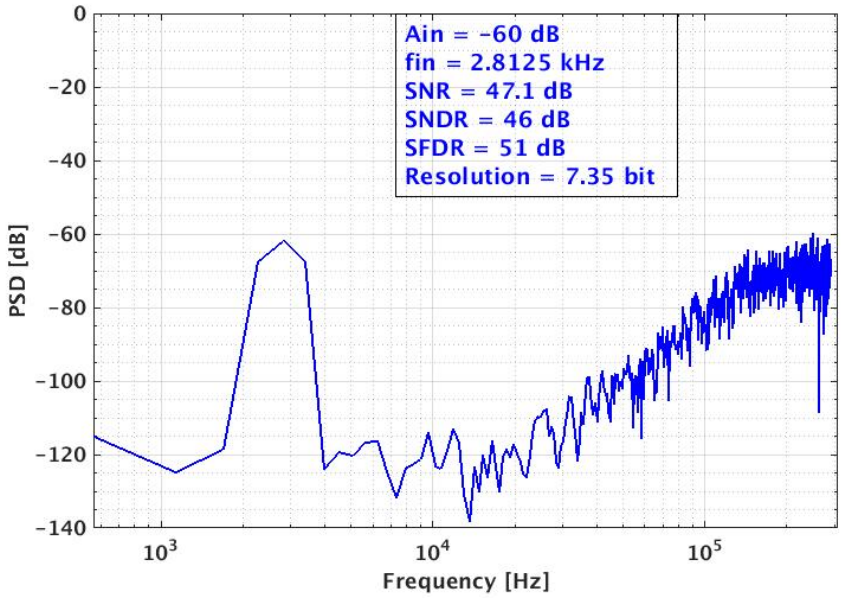

Figure 6.9: Measured output spectra of Hybrid ADC for -60 dBFs input amplitude

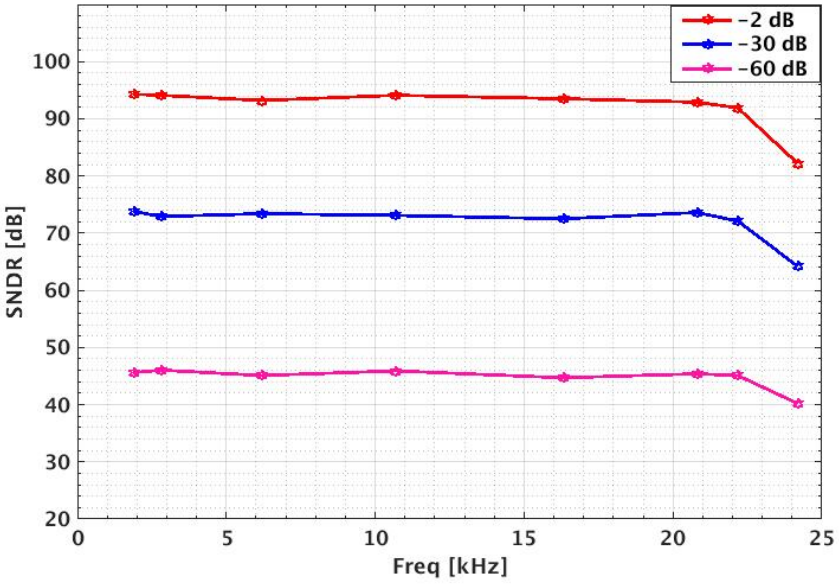

Figure 6.10: Measured output SNDR of Hybrid ADC for input frequency range.

of 106 dB, with a peak SNR and SNDR of 96.8 dB and 94.45 dB respectively. The change in the slope of the SNDR curve is mainly due to the increased error introduced in the parallel path of Incremental ADC for higher inputs. Figure. 6.12 shows the measured dynamic range over the entire input frequency range.

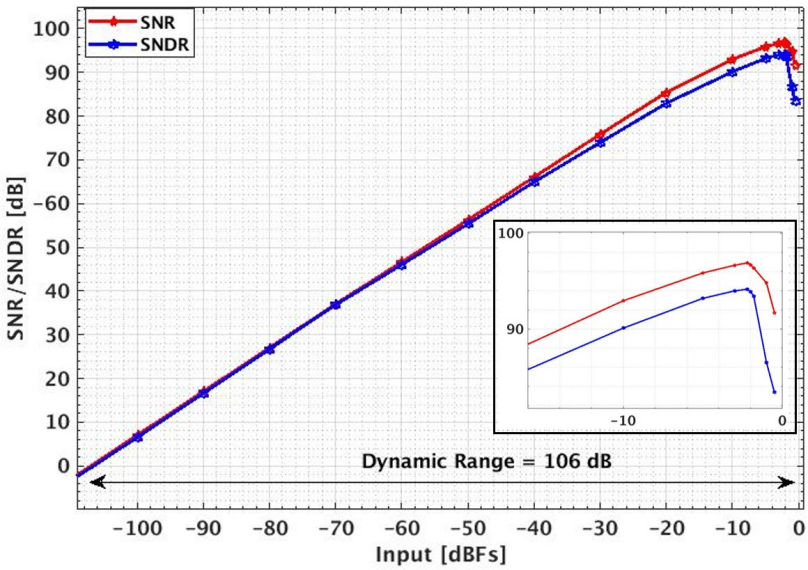

Figure 6.11: Measured SNR/SNDR of proposed Hybrid ADC as a function of input amplitude.

The power breakdown of the ADC is shown in Fig. 6.13. The Incremental Opamp and three $\Delta\Sigma$ Opamps are the main contributors to the total power consumption of 7.2 mW. The Schreier-FoM is commonly used to compare the performance of ADCs and is expressed as:

$$FOM_S = DR(dB) + 10 \cdot log_{10} \frac{BW}{Power} \tag{6.1}$$

With a dynamic range of 106 dB, and a power consumption of 7.2 mW for a bandwidth of 24 kHz, the circuit achieves an FoM of 171.23 dB. Table. 6.1 presents the performance summary of the ADC and the comparison with other reported ADCs in the literature with audio bandwidths. Reason for higher power

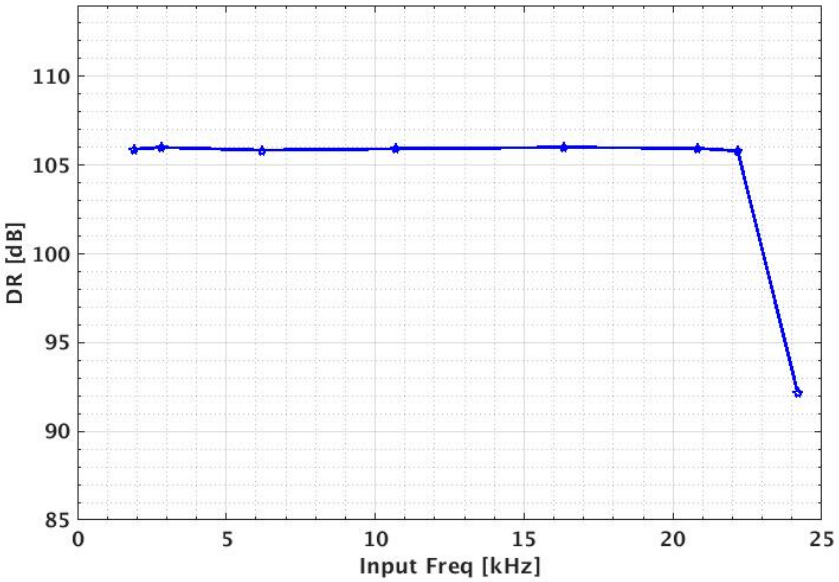

Figure 6.12: Measured dynamic range of Hybrid ADC for input frequency range.

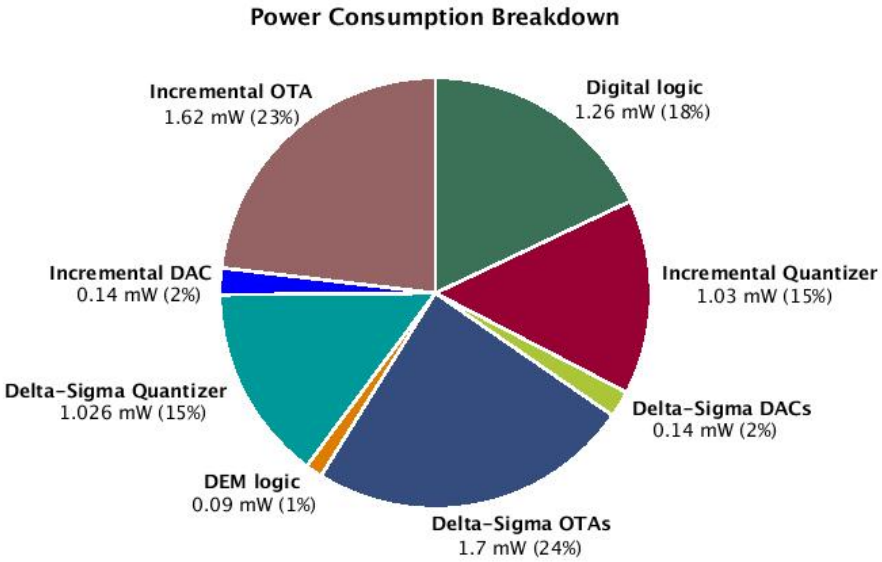

Figure 6.13: Power consumption breakdown of the ADC.

consumption and hence lower FoM is due to the fact that the output of proposed Hybrid ADC is sampled at a much higher frequency of 576 kHz instead of the audio bandwidth as is the case with other designs. This requirement directly comes from the class-D audio amplifier chain to eliminate the cost of interpolation. The discussion of interpolation phenomena in the amplifier chain and other related blocks is beyond the scope of this thesis.

Parameter	**This Work**	[81] JSSC'09	[82] ESSCIRC'16	[83] JSSC'16	[84] ASSCC'11	[85] JSSC'17
Technology (μm)	**0.18**	0.18	0.18	0.065	0.040	0.16
Active Area (mm^2)	**1.2**	2.16	0.4	0.256	0.05	0.16
Supply Voltage (V)	**1.8**	0.7	1.8	1	2.5/1.2	1.8
Input Sampling Freq. (MHz)	**16**	5	3.6	6.4	6.5	11.29
Output Sampling Freq. (KHz)	**576**	25 (BW)	20 (BW)	25 (BW)	24 (BW)	20 (BW)
SNDR$_{max}$ (dB)	**94.45**	95	80	95.2	90	103
DR (dB)	**106**	100	99	103	102	109
Power (mW)	**7.2**	0.87	1.26	0.8	0.5	1.12
FoM$_S$(dB)	**171.23**	*174.58	*171	177.9	179	181.5

*: calculated from reported DR values

Table 6.1: Performance summary and comparison table of the ADC.

Chapter 7

Conclusion and Future Work

7.1 Conclusion

An extended-range Hybrid ADC for high dynamic range is designed and implemented in 0.18 μm CMOS process for a digital input class-D audio amplifier. The design space for ADC considers harmonization and optimization with the subsequent digital chain to keep it unmodified in order to recycle completely the DAC conversion circuitry. The Hybrid ADC consists of two main blocks: first-order Incremental with 4-bit quantizer that does coarse conversion and generates the MSBs and a 3rd-order $\Delta\Sigma$ ADC with 5-bit quantizer that is used for fine conversion and generates the LSBs of the Hybrid ADC. The incremental converter uses a parallel path architecture that relaxes the output swing and slew rate requirements of the Incremental Opamp at the cost of 4 extra comparators. In addition, it also increases the dynamic range of Incremental converter, thereby also improving the dynamic range of Hybrid ADC. In order to compensate for the unit-element mismatch in the feedback DAC for the parallel path, a simpler One-Shift DEM technique is implemented that uses much lower power consumption and also does not introduce complexity in the circuit, as compared to the conventional DWA technique. A 3rd-order $\Delta\Sigma$ ADC with multi-bit quantizer is

also designed, that processes the residual error of Incremental integrator. It uses cascade of integrators with distributed capacitive feedback (CIFB) with capacitive input feed-forward path (CIFF). The Hybrid ADC achieves dynamic range of 106 dB, SNR of 96.8 dB, a maximum SNDR of 94.45 dB and SFDR of 103 dB. The performance of the Hybrid ADC and its comparison with other state of the art designs is presented.

7.2 Future Work

An improved performance of proposed Hybrid ADC can be achieved with few modifications and alternatives:

1. The Thermometric-to-Binary encoders can be implemented with registers, so that the output data can be acquired at the clock edges, eliminating any glitches.

2. The two 4-bit binary outputs from the Incremental converter can be added to generate a 5-bit binary output.

3. The SNR of Hybrid ADC can be improved further by increasing the OSR of $\Delta\Sigma$ ADC.

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