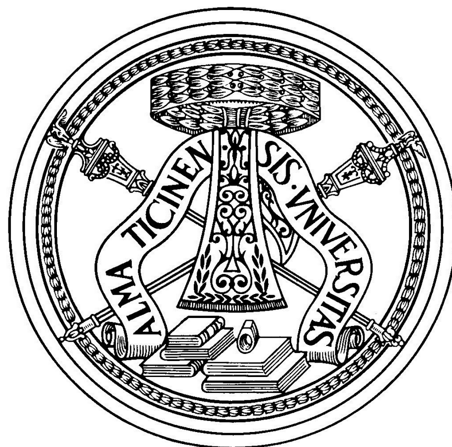
UNIVERSITY OF PAVIA



Department of Electrical, Computer and
Biomedical Engineering

Ph.D. School in Microelectronics

D-BAND AMPLIFIERS IN SiGe BiCMOS FOR WIRELESS BACKHAUL IN 5G and BEYOND

Ph.D. Thesis of
Ibrahim PETRICLI
XXXIII Cycle

Supervisor: Prof. Andrea MAZZANTI

November 2020

To my family

ACKNOWLEDGEMENTS

Arriving to this phase of my life wouldn't have been possible without the presence of certain individuals. I would like to present my humble gratitude in this page.

I would like to thank my supervisor Prof. Andrea Mazzanti for this research opportunity and also for his motivative guidance and support starting from my M.Sc. degree, which is comprising 20% of my life.

I would like to thank Ahmet Caglayan and Cansu Telkes for their life time friendship.

I would like to thank my colleagues and friends expatriate scientists Dr. Alper Akdikmen, Dr. Farshad Piri and Mustafa Oz for their presence, coffee breaks and "molto più".

I want to thank all the colleagues in Analog Integrated Circuits laboratory.

Last but not least, I want to thank each of my family member for their endless support and their belief in me.

TABLE OF CONTENTS

Page

Acknowledgements .... **v**
Table of Contents .... **vii**
List of Figures .... **ix**
Abstract .... **xiii**
1. Introduction **1**
1.1 Motivation 1
1.2 Thesis Organization 5
2. Design of Compact D-Band Amplifiers with Lumped Components **7**
2.1 Validation of Simulation Flow and Technology 8
2.2 Single-Ended Amplifier Designs 10
2.2.1 Circuit Design 10
2.2.2 Inductors and Current Return Path 12
2.2.3 Experimental Results 16
2.3 Differential Amplifier Designs 17
2.3.1 Circuit Design 17
2.3.2 Experimental Results 20
2.4 Conclusion 22
3. Analysis and Design of Wideband Amplifiers for D-Band Applications **25**
3.1 Introduction 25
3.2 Review of Common-Emitter and Cascode Gain Stages 26
3.3 Anaylsis of Cascode Output Matching Network 29
3.3.1 Lossless Matching Network 30
3.3.2 Matching Network with Lossy Components 32
3.3.3 Comparison with Simulations 34
3.4 Design of Amplifiers 36
3.5 Experimental results 42
3.6 Conclusion 44
4. Design of D-Band Power Amplifiers with Enhanced PAE **45**
4.1 Introduction 45
4.2 Current Clamping 46
4.3 Circuit Design 47
4.4 Experimental Results 50
4.5 Conclusion 53
Conclusion **55**

Appendix **57**
A.1 - A 112 Gb/s PAM-4 RX Front-End with Unclocked DFE 57
1.1 Introduction 57
1.2 RX Linear Chain and CTLE 58
1.3 Unclocked DFE 60
1.3.1 Adder 62
1.3.2 Comparators 62
1.3.3 Delay Cell 64
1.4 Results 66
1.5 Conclusion 69
References **71**

LIST OF FIGURES

Page

Figure 1.1 : Macro cell and small cells backhaul connections............................. 1
Figure 1.2 : Reserved non-contiguous spectrum blocks for fixed wireless services [8]. 2
Figure 1.3 : The challenge of fitting the ICs in the antenna array footprint [10]. . 3
Figure 1.4 : Maximum power added efficiencies for SiGe and CMOS PAs in literature. 4
Figure 2.1 : De-embedding structures for MOM Capacitor and CE HBT. 8
Figure 2.2 : (a) BEOL of the technology, (b) Simulation strategy for CE HBT. .. 8
Figure 2.3 : Comparison of EM simulation and de-embedded measurements: (a) Capacitance of MOM capacitor (top), quality factor of MOM capacitor (bottom), (b) maximum available gain of transistor in common emitter configuration. 9
Figure 2.4 : (a) 1-stage and (b) 2-stage amplifiers schematic. x_{gnd}, coupled with nearby inductors, represents current return paths. 11
Figure 2.5 : Chip microphotograph of the (a) 1-stage and (b) 2-stage amplifiers. 12
Figure 2.6 : (a) 3D View of Stacked Capacitor (b) Simplified Model (c) |Z| vs Frequency. 12
Figure 2.7 : Inductor layout with current density from EM simulations. (a) 3- terminal without shielding, (b) 3-terminal with a surrounding metal layer, (c) 4-termianl to include current return path. 13
Figure 2.8 : Equivalent circuit models reproducing EM simulations for the three situations in Fig. 2.7. 13
Figure 2.9 : Equivalent inductance from EM-simulations (dotted lines) and lumped circuit models (solid lines) for the three situations in Fig. 2.7. 15
Figure 2.10 : 1-stage amplifier measurement and comparison with simulations. (*sim.(a)*: unshielded inductors and lumped ground, *sim.(b)*: shielded inductors and lumped ground, *sim.(c)*: shielded inductors and current return paths included). 16
Figure 2.11 : 2-stage amplifier measurement and comparison with simulations. (*sim.(a)*: unshielded inductors and lumped ground, *sim.(b)*: shielded inductors and lumped ground, *sim.(c)*: shielded inductors and current return paths included). 17
Figure 2.12 : Schematic of (a) 1-stage amplifier, (b) 2-stage amplifiers................ 18
Figure 2.13 : Layout of the input matching network of one-stage amplifier........... 19
Figure 2.14 : Layout of the transformer in 2-stage amplifier. 20

Figure 2.15 : Chip microphotograph of the (a) 1-stage and (b) 2-stage differential amplifiers. 21
Figure 2.16 : S-Parameter comparison of measurement and simulation for one-stage amplifier. 21
Figure 2.17 : S-Parameter comparison of measurement and simulation for two-stage amplifier. 22
Figure 3.1 : Common emitter (a) and cascode (b) gain stages. 27
Figure 3.2 : MAG/MSG versus frequency for the common emitter and cascode active stages. 27
Figure 3.3 : Optimal source and load impedances at 150 GHz for the common emitter and cascode active stages. 28
Figure 3.4 : Equivalent circuit of the cascode stage driven by Z_{S-opt} and with matching toward the equivalent impedance at the GSG pad. 29
Figure 3.5 : Circuit schematic used to validate the analysis with simulations. 35
Figure 3.6 : Comparison of calculation with simulation for (a) lossless, (b) lossy matching network, Normalized gain and bandwidth. 35
Figure 3.7 : (a) Tline 2-port network, (b) distributed-element circuit model of a Tline 36
Figure 3.8 : (a) Cross section of the shielded microstrip TLINE, (b) characteristic impedance and quality factor vs the width of the signal trace. 38
Figure 3.9 : (a) Schematic of single-stage amplifier, (b) Peak gains at 150 GHz and bandwidths for different W values. 39
Figure 3.10 : Schematic of 2-stage amplifier. 39
Figure 3.11 : Peaking frequencies and relative positions for (a) 2-stage, (b) 3-stage amplifier. 40
Figure 3.12 : Schematic of 3-stage amplifier. 41
Figure 3.13 : Chip microphotographs of 1- (left), 2- (center) and 3-stage (right) amplifiers. 43
Figure 3.14 : S-Parameter results for 1- (top), 2- (center) and 3-stage (bottom) amplifiers. 43
Figure 4.1 : (a) Voltage-mode, (b) current-mode diode clamping circuits. 46
Figure 4.2 : The implementation of current-mode clamping on CB transistor, and current waveforms. 46
Figure 4.3 : Schematic of the single-ended PA. 47
Figure 4.4 : (a) G_P and load-pull circles, (b) dynamic load lines for the transistor in the output stage. 48
Figure 4.5 : Characteristics of T-Line and balun. 49
Figure 4.6 : Chip microphotographs of the single-ended (left) and differential (right) PAs. 50
Figure 4.7 : Measured S-parameters and stability-factors for single-ended and differential PAs. 50
Figure 4.8 : Large-signal measurement setup 51
Figure 4.9 : Measured large signal performance. 52

Figure 4.10 : The DC current of the different stages in single-ended PA. 53
Figure 4.11 : Reliability test for single-ended PA. 53
Figure 5.1 : Proposed Analog Front-end Architecture. 58
Figure 5.2 : Schematic of VGA and Continuous Time Linear Equalizer. 59
Figure 5.3 : Frequency Response of CTLE from post-layout simulations. 59
Figure 5.4 : Pulse responses of Channel, DT-tap and IIR-tap 61
Figure 5.5 : UC-DFE block diagram. 61
Figure 5.6 : Schematic of the adder. 62
Figure 5.7 : Schematic of a comparator. 63
Figure 5.8 : (a) Schematic of the amplifier used in the delay cells. (b) Transfer function and group-delay of a single stage and multi-stage amplifiers. 64
Figure 5.9 : Gain-Bandwidth product of cascaded amplifiers featuring 12 ps group delays. 65
Figure 5.10 : Eye diagrams for delay cells with a different number of stages. 66
Figure 5.11 : (a) Layout of the RX front-end with the UC-DFE. (b) The channel transfer functions. 66
Figure 5.12 : 56 Gb/s eye diagrams with 24 dB channel loss: input signal (top), CTLE output (middle), signal after UC-DFE correction (bottom). 67
Figure 5.13 : 112 Gb/s eye diagrams with 18 dB channel loss: input signal (top), CTLE output (middle), signal after UC-DFE correction (bottom) 68

ABSTRACT

The never ending demand for wider bandwidth, coupled with the evolution of technology, drives the progress of silicon ICs beyond 100 GHz. The wide available spectrum in D-band, 60 GHz centered at 140 GHz, is being considered for enhanced resolution radars and wireless transceivers with a fiber-like transport capacity, key for network deployment in 5G and beyond [1].

Amplifiers are the key building blocks in wireless transceivers, i.e., in receivers low noise amplifiers restore adequate amplitude before frequency conversion and in transmitters power amplifiers drive the antenna with sufficient power in a most efficient way. Considering the operation of transistors close to f_{max} of the technology, in D-band, design of amplifiers with sufficient performance is particularly challenging. The Ph.D. activity has been done by following three paths to address different issues:

(1) Strategies for compact designs, key for phased array systems where fitting the ICs in dedicated radiating antenna element footprint is challenging.

(2) Design approach for gain-bandwidth-product enhancement, important to ensure the full D-band operation.

(3) Techniques for efficiency enhancement for power amplifiers in D-band, essential for the most power hungry block.

To this regard, this thesis presents 9 D-band amplifiers, i.e., 7 signal amplifiers and 2 power amplifiers.

First 4 compact D-band amplifiers use lumped elements in matching networks. In the first two single ended designs, to correctly account for the effects of a non-ideal ground plane, i.e., reactances in current return paths, and coupling of inductors with nearby layout structures, a shielded 2-port, 4-terminal simulation strategy for inductors is proposed and validated by measurements. The approach allows very accurate design of compact amplifiers in D-band. The 1-stage design proves 11.8 dB gain at 152 GHz and 17.9 GHz bandwidth in 0.031 mm^2. With the 2-stage amplifier, featuring 20.1 dB gain at 150 GHz with 24.5 GHz bandwidth in 0.058 mm^2, from 2× to 5.7×

area reduction is demonstrated against similar SiGe amplifiers in the same frequency band. In the next two designs, the differential topology is developed for robustness against parasitic effects of the non-ideal ground, a key issue with lumped components at high frequency. The 1-stage amplifier reaches 8 dB gain at 156 GHz and 17.8 GHz bandwidth in 0.026 mm^2 silicon area. The 2-stage amplifier displays 17.4 dB gain at 157 GHz with 42.7 GHz bandwidth in 0.048 mm^2. Compared to previously reported SiGe amplifiers in similar frequency range, more than 2× core area reduction is demonstrated at comparable gain-bandwidth product.

The last three designs uses transmission lines in matching networks. For designed amplifiers, simple, closed-form equations for gain and bandwidth as a function of the load reflection coefficient are derived. Leveraging the results of the analysis, which can be also applied to the lumped-element approach, a single-stage and multi stage stagger-tuned amplifiers are implemented in a SiGe BiCMOS technology. Two- and three-stage amplifiers demonstrate more than 60 GHz bandwidth with 20 dB and 28 dB gain respectively, corresponding to 700 GHz and 1.7 THz gain-bandwidth product. Normalizing gain and bandwidth to the number of stages and technology f_{max}, the resulting Figure of Merit is remarkably higher than previously reported silicon amplifiers in the same band.

The power amplifiers (PAs) are designed in a single-ended and differential fashion. The PAs exploit the remarkable features of common-base stages to enhance power-added-efficiency in the linear PA operating region. A single-ended PA proves P_{1dB} =16.8 dBm with P_{SAT} = 17.6 dBm at 135 GHz. The PAE at P_{1dB} and at $P_{1dB-6dB}$ are 17.1 % and 8.5 % respectively. With a differential PA the linear output power is increased to P_{1dB} =18.5 dBm with P_{SAT} = 19.3 dBm at 135 GHz. The PAE at P_{1dB} and at $P_{1dB-6dB}$ are 12.6 % and 6.7 % respectively, an improvement of at least 3× against state of the art.

Chapter 1

Introduction

1.1 Motivation

The number of wireless devices has been increasing as a consequence of the change in our daily habits, which translates to extensive growth in data traffic. According to [2], 5G subscriptions are anticipated to surpass 849 million by 2025, which corresponds to $\sim$11 gigabytes per user per month. In other words, the mobile network traffic will be tripled by 2025 compared to today's numbers.

To cope with the aforementioned expansion, wireless infrastructures keep continue to evolve with the next generation of cellular networks. Considering the anticipated data traffic demand, 5G network standards should have 20 Gbps peak data rate, $\times$100 network energy efficiency, and 10 Mbps/m^2 area traffic capacity [3], and as a result 10^3 - 10^4 times the network capacity. To increase the spectral efficiency by means of reusing the same carrier frequency simultaneously, Massive MIMO (Multi-Input Multi-Output) and beam-forming technologies are planned to be used [3].

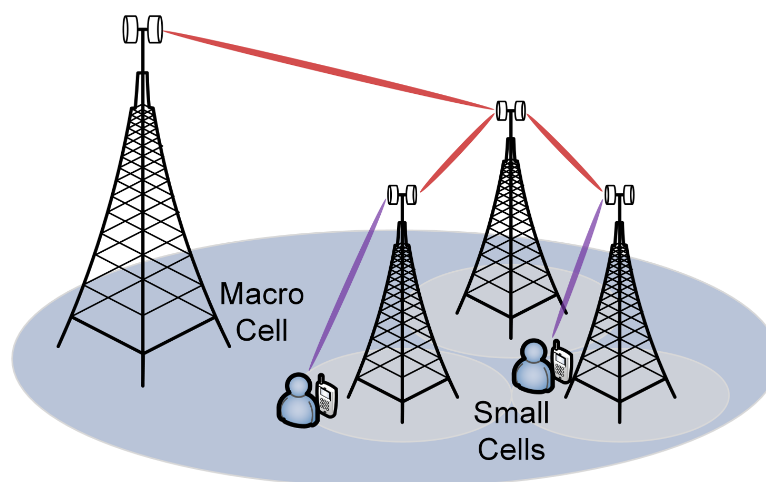


Figure 1.1: Macro cell and small cells backhaul connections

Having the major part of the world population in the urban areas necessities high number of base station deployments and smaller network cells to increase the

efficiency. To that purpose small-cell architecture has been proposed [4] (Fig.1.1). The macro cell and the small cells can be connected through optical-fiber lines. But the installation cost of fibers is extremely high, and in some areas simply it can't be laid out because of the obstructions. Therefore, the solution is simply to replace the optical-fiber connections with high data-rate wireless connections.

The availability of large bandwidth and high spectrum efficiency is essential, but even if multi-carrier techniques are used, a channel bandwidth as large as 2.5 GHz will be required [5]. This amount of bandwidth can only be provided in millimeter-wave (mmWave) frequency spectrum. To this end, mmWave frequencies have been investigated.

The wide available spectrum in D-band (100-170 GHz) is rapidly gaining interest enabling wireless communication with a fiber-like transport capacity, key for the infrastructure of future cellular networks, i.e., 5G and beyond [1, 6, 7]. Standardization and spectrum allocation are currently in progress. According to ECC recommendations, four non-contiguous spectrum blocks (Fig. 1.2), have been already reserved in the 130 GHz to 174.8 GHz frequency range for fixed wireless services [8].

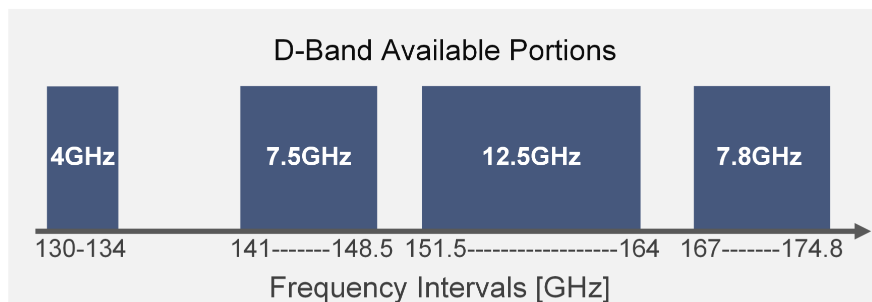


Figure 1.2: Reserved non-contiguous spectrum blocks for fixed wireless services [8].

Wireless backhaul transceivers must be energy efficient and in a compact size to simplify deployment. Moreover, in view of the increased volumes and system complexity, the adoption of a silicon technology is key. Today, the BiCMOS process, combining CMOS devices for digital functions and bipolar transistors for high-frequency building blocks represent an optimal compromise between costs and performances. Nonetheless, in D-band the implementation of transceivers with acceptable performance is very challenging because of the high operation frequency,

close to the technology limits. To this purpose, several private and public research programs are ongoing. The European projects DREAM [4] and TARANTO [9], where University of Pavia is a partner, are aimed at investigating D-band radio solutions to meet the requirements of wireless backhaul in 5G and beyond. In particular, my Ph.D. activity has been investigation of suitable D-band amplifiers in SiGe BiCMOS technology.

Taking into account transistors operate close to f_{max}, design of amplifiers with adequate performance is particularly challenging in D-band. This work followed three different paths to address different issues related to design of D-band amplifiers.

The first issue is related to the amplifier's footprint. A massive use of phased array, i.e., hundreds of radiating elements, each one driven by a dedicated front-end, is foreseen to compensate the high path loss and the limited available power from a single element [1]. To this purpose, as depicted in Fig. 1.3, a key challenge beyond 100 GHz is to fit the integrated circuits (ICs) in the area occupied by the antenna array [10]. In fact, the separation between radiating elements is set by the wavelength, but while the area of the antenna array shrinks with the square of the wavelength, the size of the ICs, dominated by the many required amplifiers, is hard to scale proportionally [10] which motivates investigations to shrink the size.

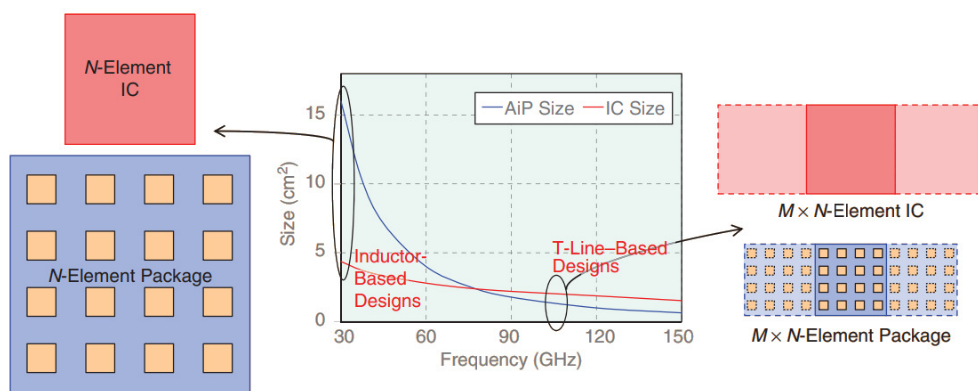


Figure 1.3: The challenge of fitting the ICs in the antenna array footprint [10].

The addressed second challenge is providing enough gain over the full bandwidth. Considering 60 GHz overall bandwidth (110-170 GHz) and gain needs of >20 dB, amplifiers must have >600 GHz gain-bandwidth-product (GBW). Distributed amplifiers in SiGe HBT technologies meet the requirement but consume excessive power.

Tuned amplifiers save power but in D-band the design is made challenging by the low available gain of transistors. To this regard, design techniques for GBW enhancement in multi-stage tuned amplifier are investigated.

Lastly, the third issue is related to the efficiency of power amplifiers (PAs) in D-band. As depicted in Fig. 1.4, evidenced by the PA survey [11] the average of maximum power added efficiency (PAE_{max}) in D-band is $\sim 6.7\%$. Moreover, this number reduces in linear operation, i.e., <5 % for P_{out}=P_{1dB}, and <2 % for P_{out}=P_{1dB}-6 dB. As an example, a PA delivering 15 dBm output power with 5 % PAE consumes approximately 620 mW DC power. Assuming PAs are employed in 8×8 phased array system, the total power consumption in $\sim 8 \times 8\,\text{mm}^2$ area would be approximately 40 W. Such a high power consumption in a very small area could cause thermal reliability issues. To overcome the problem and increase the linear operation efficiency of PAs in D-band, efficiency enhancement techniques have been proposed.

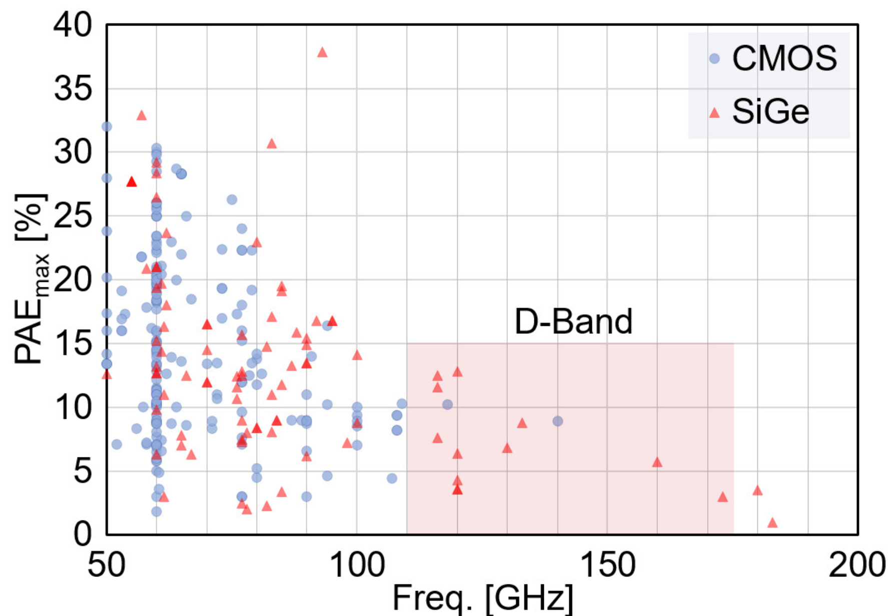


Figure 1.4: Maximum power added efficiencies for SiGe and CMOS PAs in literature.

1.2 Thesis Organization

The activity documented in the rest of the thesis was part of the TARANTO funded program and addresses the issues outlined above for the design of D-band amplifiers in the STMicroelectronics BiCMOS 55 nm tecnology.

The Chapter 2 presents a design and verification strategy for compact D-band amplifiers with matching networks implemented with lumped elements. Different test chips have been realized and measurements prove state-of-the-art performances with remarkable area reduction. The results are published in [12] and [13].

The third chapter analyses wideband amplifiers for D-band communication. A design strategy is proposed leveraging the load reflection coefficient of cascode gain stage to enhance the GBW. Measurements on implemented single and multi-stage amplifiers prove a figure of merit significantly higher than state of the art. The results are submitted to a journal publication entitled "Analysis and Design of D-Band Cascode SiGe BiCMOS Amplifiers with Gain-Bandwidth Product Enhanced by Load Reflection".

The Chapter 4 study the problem of power added efficiency in D-band power amplifiers. The remarkable properties of the common-base stage are studied and applied to the implementation of D-band power amplifiers that demonstrate 3$\times$ PAE improvement against state of the art. The results are submitted to a letter publication titled "D-band SiGe BiCMOS Power Amplifier with 16.8 dBm P_{1dB} and 17.1 % PAE Enhanced by Current-Clamping in Multiple Common-Base Stages".

As appendix of the Thesis, an activity carried out in the initial part of my PhD course is summarized. It is related to the design of a serial-link PAM-4 receiver in FinFet technology. The results of this activity are published on a journal paper titled "A 112 Gb/s PAM-4 RX Front-End with Unclocked Decision Feedback Equalizer" [14].

Chapter 2

Design of Compact D-Band Amplifiers with Lumped Components

In D-band, to maximize the gain amplifiers need conjugately matched multiple stages. Apart from few exceptions (e.g. [15]) amplifiers reported so far leverage transmission lines (Tlines) in matching networks [16–20]. The good confinement of the electromagnetic field in Tlines limits coupling and cross-talk issues with nearby components. The structured Tline models account both forward and return current paths, thus make the design robust against the effects of a non-ideal ground plane which is a critical issue at high frequency. However, despite the short wavelength in D-band, Tlines occupy large silicon area and represent the primary limit to scale the size of active circuits.

The amplifiers footprint can be drastically reduced with compact inductors in matching networks, as commonly used in the lower portion of the millimetre-wave band [21]. However, inductors are influenced from coupling with nearby structures in layout. Moreover, unless differential topology is adopted, the effects of current return paths [22, 23] must be carefully accounted in D-band to avoid unpredicted networks mistuning, responsible for frequency shift or loss of the gain.

This chapter starts with the validation of the simulation flow and technology. Even though the technology is well suited for mm-Wave design, we lacked reference measurement results above 100 GHz which brings questions about reliability of the simulation flow. Therefore, pre-validation was seemed to be necessary.

The chapter continues with compact D-band amplifiers with lumped-element matching networks. While having the small silicon area, to handle the aforementioned issue two different solutions are proposed, i.e., accurate modelling of current return paths in the lumped inductors and differential circuit topology. While the details on accurate modelling of inductors and current return paths are given in the single-ended amplifier

design section, differential amplifiers are presented in the section three. Finally, the results are summarized and compared with the state of the art in the conclusion section.

2.1 Validation of Simulation Flow and Technology

In order to verify the simulations flow against simple measurements, elementary components as well as TRL de-embedding structures (thru, reflect, and line) have been designed and fabricated in STMicroelectronics' 55 nm BiCMOS technology. As an example, Fig. 2.1 shows the microphotograph of the test structures and the 3D-layout views up to the reference planes for a MOM capacitor and a HBT in common-emitter.

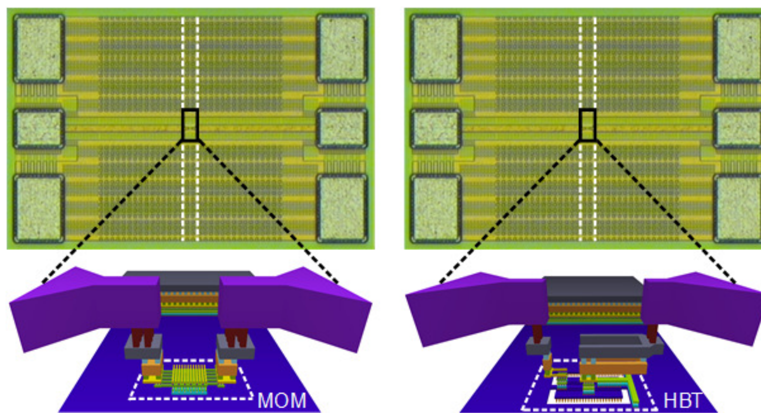
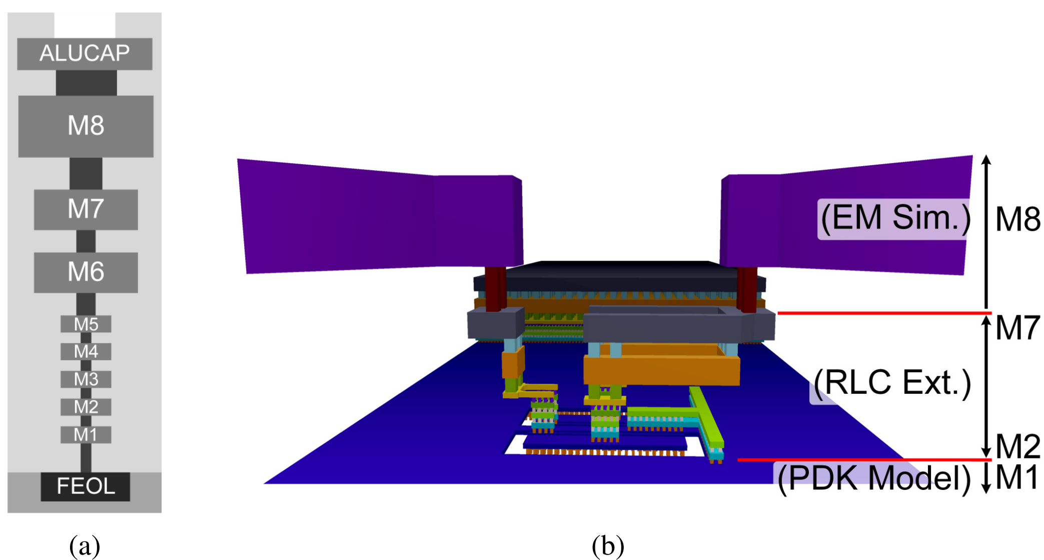


Figure 2.1: De-embedding structures for MOM Capacitor and CE HBT.



(a) (b)

Figure 2.2: (a) BEOL of the technology, (b) Simulation strategy for CE HBT.

The back-end-of-line (BEOL) of the technology is presented in Fig. 2.2(a). For the simulation of MOM capacitor only 2.5 D EM simulators (EMX and Momentum) are

used. On the other hand, as depicted in Fig. 2.2(b), the simulations of heterojunction bipolar transistor (HBT) make use of process design kit (PDK) device model, parasitic extraction tools for low level metals (M2-M7) and EM simululators for high level metals.

Fig. 2.3 plots the measured results, after de-embedding the access TLINE with the TRL method [24], in comparison with simulations. The plots in Fig. 2.3(a) show the equivalent capacitance ($C = -\text{Im}[Y_{12}]/\omega$) and the quality factor ($Q = \text{Im}[Y_{12}]/\text{Re}[Y_{12}]$) of MOM capacitor while Fig. 2.3(b) reports the Maximum Available Gain (MAG) of the HBT. After fine trimming of the many different simulation tools, the agreement between measurement and simulations is very good, thus giving high confidence level about reliability of simulations for the design of the amplifiers.

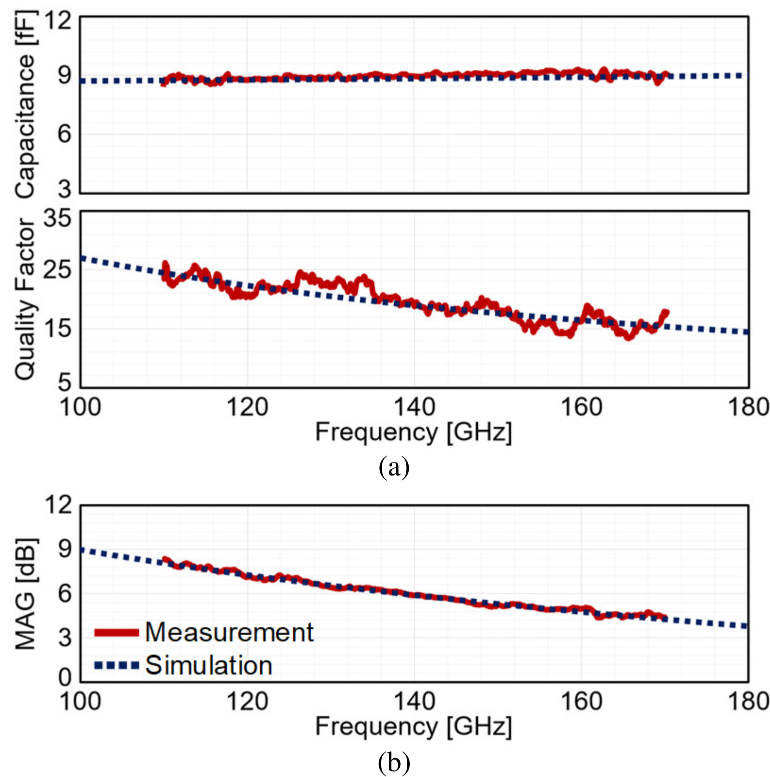


Figure 2.3: Comparison of EM simulation and de-embedded measurements: (a) Capacitance of MOM capacitor (top), quality factor of MOM capacitor (bottom), (b) maximum available gain of transistor in common emitter configuration.

2.2 Single-Ended Amplifier Designs

This section proposes an accurate, yet simple strategy for design and modelling of inductors at very high frequency without the need of performing complex electromagnetic (EM) simulations on large portions of the layout. Inductors are surrounded and co-simulated with a metal shield which ensures the component is unaffected by couplings with nearby structures. Moreover, inductors are considered as 2-port, 4-terminal devices, similar to Tlines, such that both the forward and return current paths can be accurately accounted. The approach is exploited and validated by designing 1-stage and 2-stage compact D-band amplifiers.

2.2.1 Circuit Design

The schematics of the single-stage and 2-stage amplifiers are depicted in Fig. 2.4. The two amplifiers use the same transistor with 5.1 µm×0.2 µm total emitter area. After careful layout, and biased with 7.1 mA collector current, the f_{max} is simulated as 290 GHz. A single hetero-juntion bipolar transistor (HBT) in common-emitter (CE) configuration with $V_{CE} = 1$ V displays maximum available gain (MAG) of 5.8 dB at 150 GHz while the cascode configuration, supplied at 1.9 V, performs 13.8 dB MAG. Since the minimizing the amplifiers area is essential, and considering cascode structure shows more gain than two cascaded CE stages without the need for bulky interstage matching network, in final design cascode structure was chosen for a gain stage.

Looking at the amplifiers schematic in Fig. 2.4, C_1-L_1 and C_2-L_2-L_3 form input and output matching networks respectively, identical in the one- and two-stage amplifiers. The networks are designed to provide conjugate impedance matching to 50 Ω at ∼150 GHz. C_1 and C_2, of relatively small value, are realized with M_3-M_5 metal layers as parallel plate capacitors and accurately sized with EM simulations.

Inductors L_1, L_2 and L_3 are realized in the topmost metal layer and laid out with U shape, as visible in the chip photographs in Fig. 2.5. For the largest inductors (L_2, L_3) the U shape yields ∼ 30% higher quality factor and ∼ 10% higher self-resonance frequency compared to a multi-turn layout. Because of the small footprint, metal

density rules are satisfied without adding tiles in close proximity with the inductors. No substrate shield is used, having negligible effect in this frequency range.

In the two-stage amplifier (bottom schematic of Fig. 2.4), C_3 and the magnetically coupled inductors L_4-L_5 implement the inter-stage matching network, stagger tuned to flatten the amplifier frequency response. L_4-L_5 are wounded and form a coplanar transformer with $k = 0.33$.

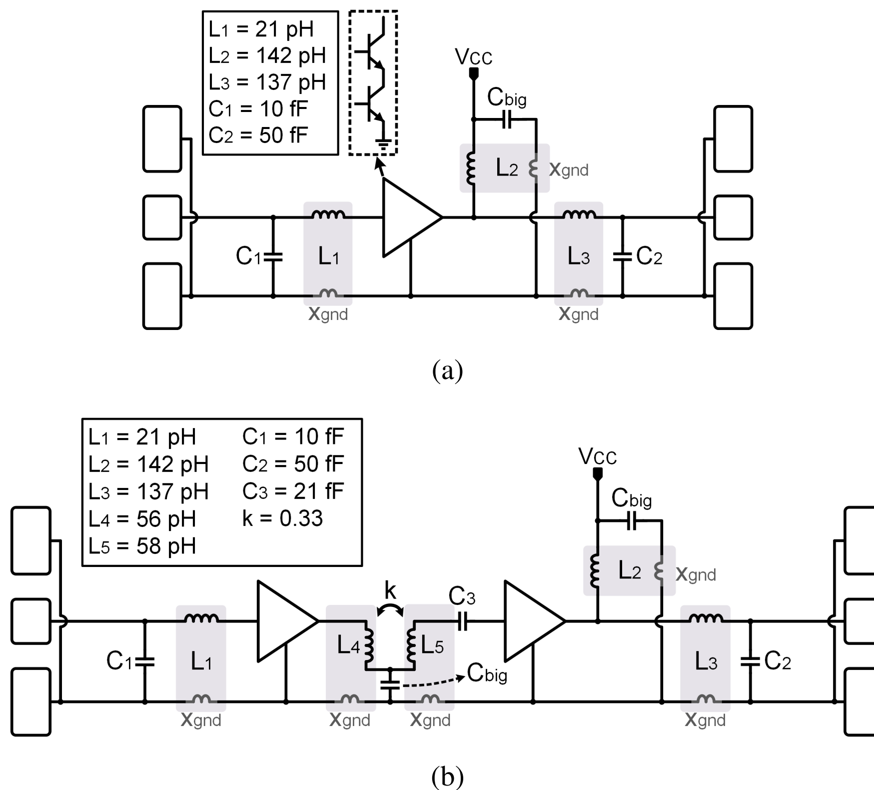
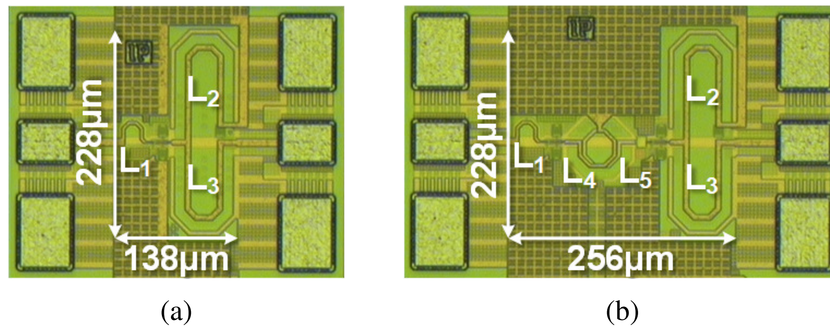


Figure 2.4: (a) 1-stage and (b) 2-stage amplifiers schematic. x_{gnd}, coupled with nearby inductors, represents current return paths.

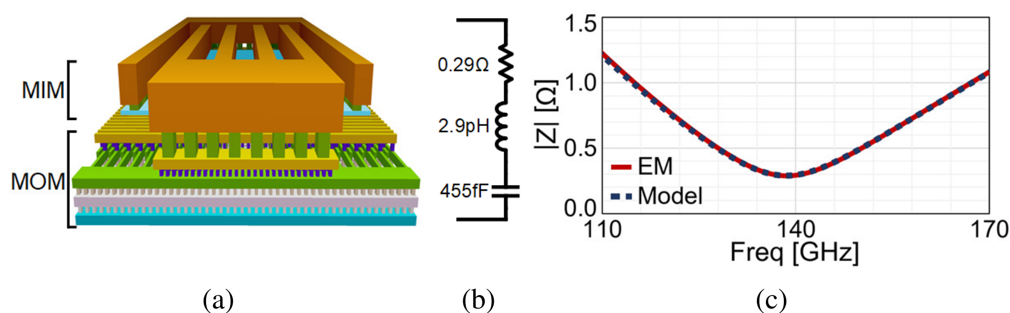
The reactances x_{gnd} in the schematics of Fig. 2.4 represent nonideal current return paths and are enclosed in a shadowed area to highlight coupling with the corresponding inductors. The approach followed for modelling inductors and x_{gnd} is deeply discussed in the next section.



(a) (b)

Figure 2.5: Chip microphotograph of the (a) 1-stage and (b) 2-stage amplifiers.

Finally, besides careful modeling of high-frequency effects in matching networks, capacitors for supply decoupling (C_{big} in Fig. 2.4) deserve attention. Being of large value, the self-resonance frequency has to be carefully accounted. The layout view of C_{big}, realized by stacking MIM and MOM capacitors, is shown in Fig. 2.6(a) while a simplified equivalent circuit, which comprises the parasitic inductance and resistance of the capacitor plates, is reported in Fig. 2.6(b). C_{big} must provide low impedance (ideally a short circuit) to the grounding point in the layout at the amplifier center frequency. The capacitor stack is therefore sized to have series resonance frequency near 150 GHz. Fig. 2.6(c) plots the impedance magnitude of C_{big}, derived from EM simulations, and from the equivalent circuit. The impedance remains below 1 Ω from 114 to 168 GHz with minimum value of 0.3 Ω at 140 GHz.



(a) (b) (c)

Figure 2.6: (a) 3D View of Stacked Capacitor (b) Simplified Model (c) |Z| vs Frequency.

2.2.2 Inductors and Current Return Path

The key issues of managing inductors in D-band is taking into account the effects of the surrounding layout (i.e., other components, metals and ground plane) and currents return path. At lower frequency, where the above effects have a minor impact, coupling

with nearby layout structures is typically neglected and a common ideal and shared reference (ground) is assumed in the model of the inductors [21].

The limitations of this approach in D-band are quantitatively analyzed in this section and a robust implementation and modeling strategy is finally proposed. We keep as an example inductor L_3, used in the output matching network. Fig. 2.7 shows the layout and the current distribution at 150 GHz, derived from EM simulations, in different cases. Fig. 2.8 presents the corresponding lumped-element models (loss resistors are included in series to each component but not shown for better readability) while Fig. 2.9 plots the simulated and modelled equivalent inductance over frequency.

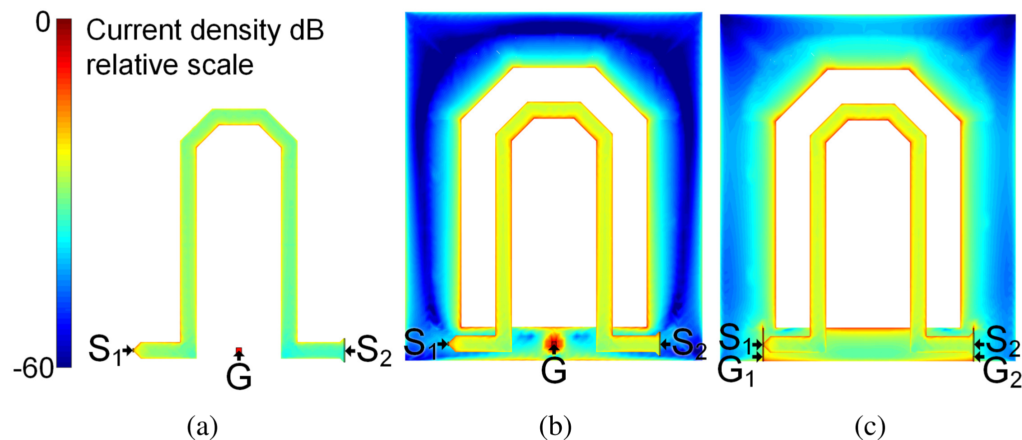


Figure 2.7: Inductor layout with current density from EM simulations. (a) 3- terminal without shielding, (b) 3-terminal with a surrounding metal layer, (c) 4-termianl to include current return path.

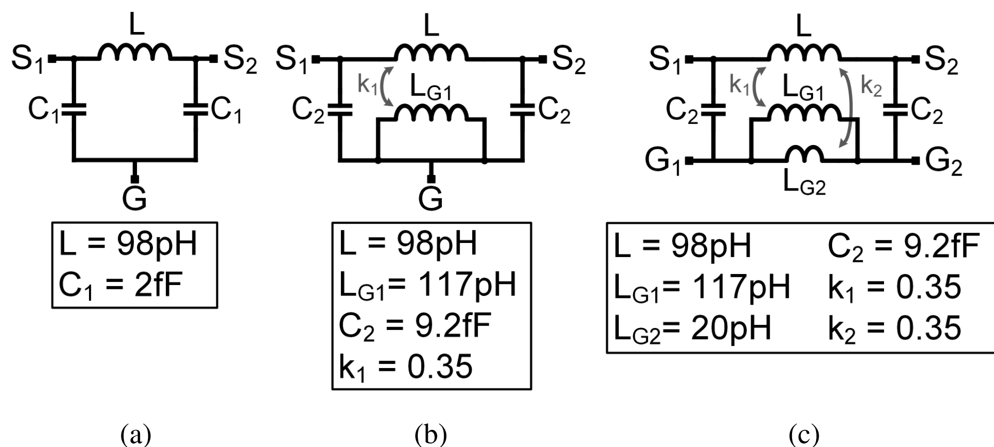


Figure 2.8: Equivalent circuit models reproducing EM simulations for the three situations in Fig. 2.7.

In Fig. 2.7(a) the inductor L_3 (realized in the top Cu metal, M_8) is simulated as a 3-terminal device: S_1, S_2 are EM-ports at the inductor ending points while G is a port on a substrate tap to account for coupling toward the substrate. This approach is accurate if no other structures or metals are close to the inductor and assumes ideal current return paths (i.e. a shared ground node). The inductor behavior is reproduced by the simple equivalent circuit in Fig. 2.8(a), where the two capacitors C_1 account for substrate coupling. The equivalent inductance, $L_{eq} = Im[Z]/\omega$ (with Z the impedance between terminal S_1 and terminal S_2 shorted to G) is plotted in Fig. 2.9 and shows a self-resonance frequency above 240 GHz. The simulated quality factor at 150 GHz (not shown) is Q = 28.

Fig. 2.7(b) shows a more realistic situation where a uniform metal is included around the inductor to mimic the effect of the ground distribution plane in final layout. The distance to the edge of the inductor is set to 3 times the width of the M_8 trace and the inductor is still considered as a 3 terminal device. As evident from the colors of the current density plot, an intense current is induced by the top M_8 trace on the edge of the surrounding metal, suggesting that coupling between the inductor and nearby structures cannot be neglected at all. On the other hand, the same plot reveals that the induced current drops very quickly moving away from the edge of the surrounding metal, suggesting the latter can be exploited to shield very well the inductor from the rest of the layout. The inductor behavior is then robust against ground plane discontinuities slightly away from the edge such as metal slots for density rules or wires for biasing and controls. In the equivalent circuit model, Fig. 2.8(b), the effect of the surrounding metal layer is captured by an additional inductor (L_{G1}) coupled to the main inductor (L) and larger capacitances to the G node (C_2). Compared to the previous case (Fig. 2.7(a) and Fig. 2.8(a)), the self-resonance frequency of the equivalent inductance, plotted in Fig. 2.9, is now reduced to around 178 GHz. The simulated quality factor at 150 GHz is 17.

By designing and simulating the inductor as in Fig. 2.7(b), the quality factor is penalized, but the component behavior will not be affected by other layout structures that may be in close proximity. However, with a single lumped reference port (G), the

parasitic reactance of the current return path (x_{gnd} in the schematics of Fig. 2.4) is not yet considered. In D-band, grounding taps located on different places in the layout cannot be assumed as perfectly short-circuited. Therefore, inductors are considered as 4-terminal devices and simulated as shown in Fig. 2.8(c). S_1, S_2 and G_1, G_2 (ports in EM simulations) are placed respectively on the inductor ending points and on the ground metal layer just below S_1, S_2. By looking at the current density in Fig. 2.7(c), a significant current flows straight in the return path, from G_2 to G_1. The 4-terminal inductor equivalent circuit is represented in Fig. 2.8(c) where, in comparison with Fig. 2.8(b) an additional coupled inductor, L_{G2}, is included to model the return path from G_2 to G_1. Curve (c) in Fig. 2.9 plots the equivalent inductance, derived from the impedance between S_1 and G_1 terminals with S_2 shorted to G_2. The self-resonance frequency is around 192 GHz and in the 140-160 GHz (the target bandwidth of the amplifiers) the equivalent inductance falls in the middle between the values predicted by the simplified simulation approaches in Fig. 2.7(a) and Fig. 2.7(b). The estimated quality factor is roughly the same as for the case in Fig. 2.7(b). The importance of careful inductors modelling and the accuracy of the 4-terminal approach is confirmed by comparing measurements of the amplifiers against circuit simulations, performed by modelling the inductors with the 3 approaches of Fig. 2.7, in the following section.

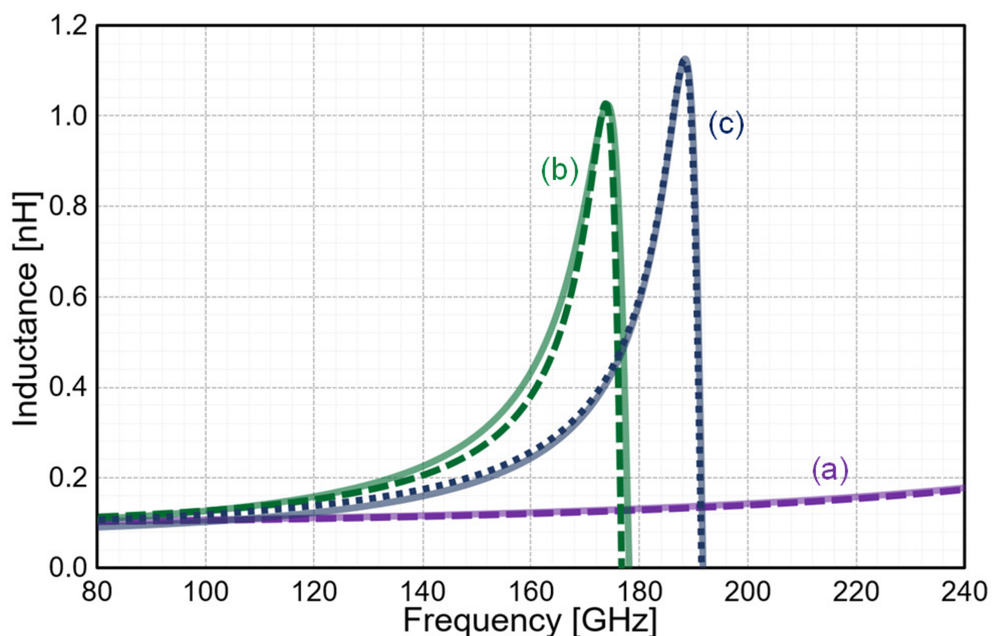


Figure 2.9: Equivalent inductance from EM-simulations (dotted lines) and lumped circuit models (solid lines) for the three situations in Fig. 2.7.

2.2.3 Experimental Results

Small-signal measurement was performed using VDI WR-6.5 D-Band Extenders with Agilent PNA-E8361C vector network analyzer (VNA) after thru-reflect-line (TRL) probe tip calibration. Fig. 2.10 plots the measured S-parameters and Rollet stability factor for the one-stage amplifier (red curves). The amplifier draws 7.1 mA from 1.9 V and displays a peak gain of 11.8 dB at 152 GHz with -3 dB bandwidth of 11.8 GHz and unconditional stability over D-band. The same plot compares measurements against simulations, performed by modelling the inductors as discussed in the previous section. *sim.(a)* neglects coupling of inductors with nearby metals and currents return path. *sim.(b)* considers a metal loop around inductors but still neglects currents return path while *sim.(c)* considers both effects. The remarkable discrepancy between measurements and *sim.(a)*, *sim.(b)* and the very good agreement with *sim.(c)* confirms the importance of careful inductors modelling and validate the proposed approach. EM simulations for the full layout (excluding HBTs) were also performed and results are in agreement with the much faster *sim.(c)* approach.

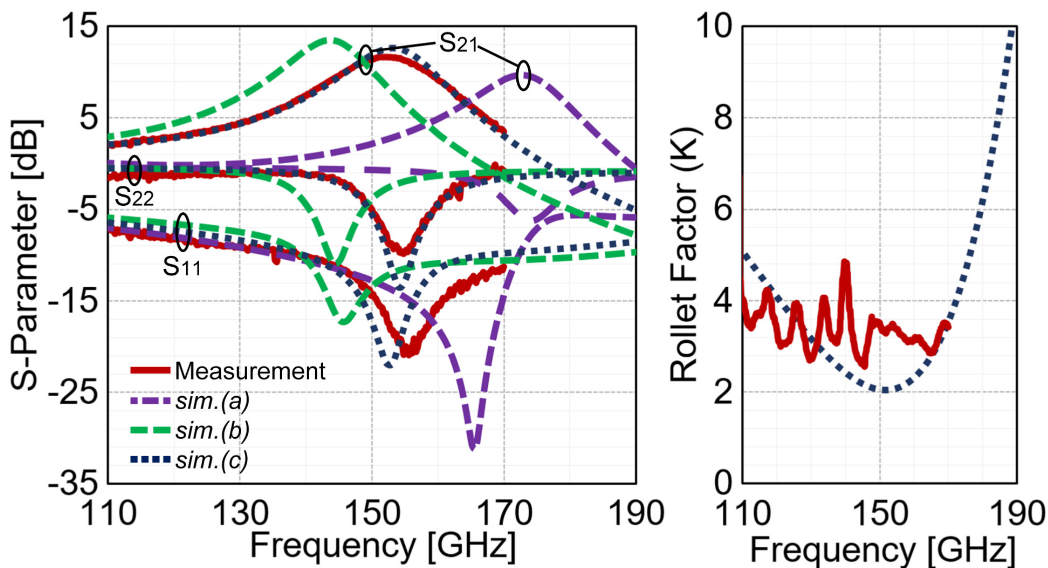


Figure 2.10: 1-stage amplifier measurement and comparison with simulations. (*sim.(a)*: unshielded inductors and lumped ground, *sim.(b)*: shielded inductors and lumped ground, *sim.(c)*: shielded inductors and current return paths included).

S-parameter measurements for the 2-stage amplifier are plotted in Fig. 2.11 (red curves). With 14.2 mA from 1.9 V supply voltage, the amplifier reaches a peak gain of 20.1 dB at 150 GHz with -3 dB bandwidth of 24.5 GHz. Also in this case measurements are in good agreement with *sim.(c)* while a remarkable discrepancy is evident with *sim.(a)* and *sim.(b)*.

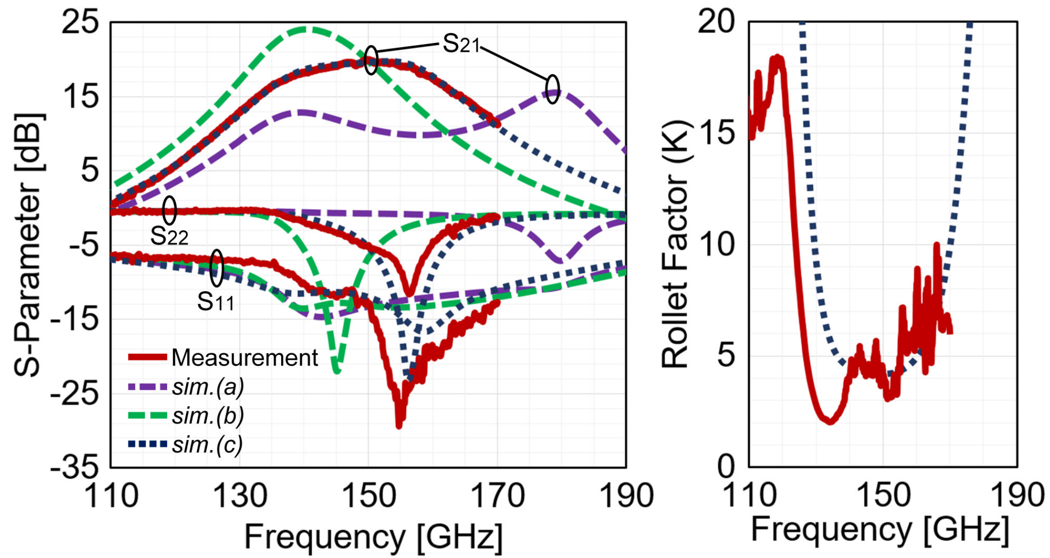


Figure 2.11: 2-stage amplifier measurement and comparison with simulations. (*sim.(a)*: unshielded inductors and lumped ground, *sim.(b)*: shielded inductors and lumped ground, *sim.(c)*: shielded inductors and current return paths included).

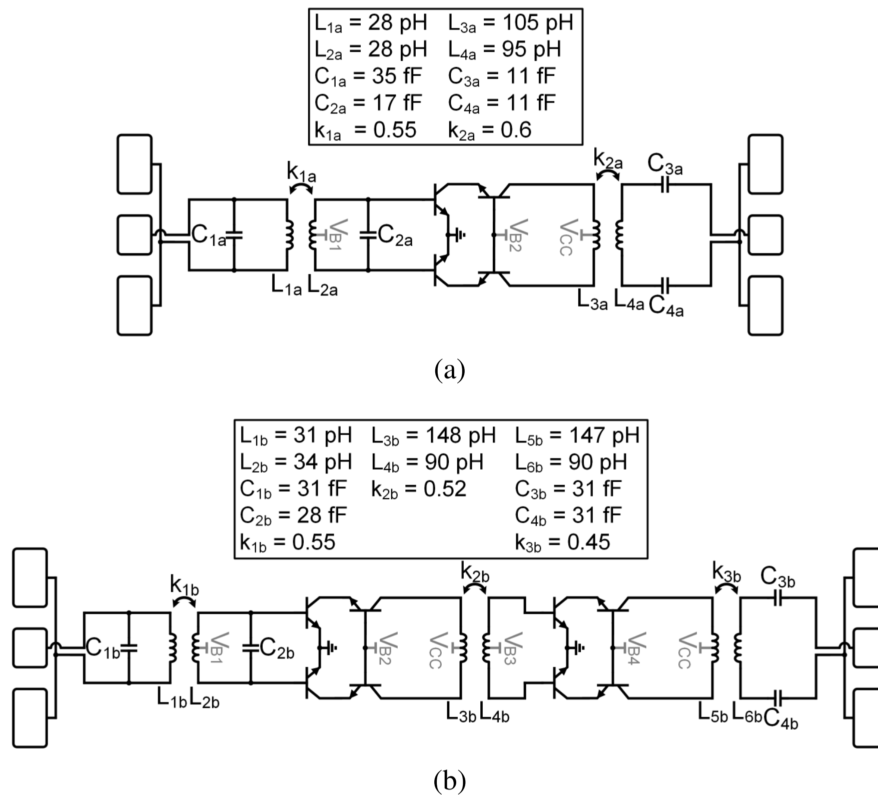
2.3 Differential Amplifier Designs

In order to circumvent the current return path issue at very high frequencies, this section proposes differential D-band amplifiers with transformers in matching networks, such that no signal current flows through the ground metal plane. The approach is exploited and validated by designing 1-stage and 2-stage compact D-band amplifiers.

2.3.1 Circuit Design

The schematics of differential D-band amplifiers are shown in Fig. 2.12. Transistors are employed in CBEBC structure with 0.2 µm×5.1 µm total emitter area, and the current density is chosen to maximize f_t at 7.1 mA / µm^2. After optimized layout of

metal layers contacting the HBT terminals, the device is unconditionally stable in D-Band, and the f_{max} of the transistor is simulated as 290 GHz. A single transistor in common-emitter configuration exhibits 5.8 dB Maximum Available Gain (MAG) at 150 GHz (consistent with the measurements in Section 2.1) while the stack of two transistors in cascode configuration, with 1.9 V voltage supply, reaches MAG of 13.8 dB. Therefore the cascode configuration which allows more gain than two cascaded common-emitter stages without the necessity of using a bulky interstage matching network, is selected.



(a)

(b)

Figure 2.12: Schematic of (a) 1-stage amplifier, (b) 2-stage amplifiers.

A differential configuration for the amplifiers is selected because, provided symmetry is maintained in layout, a well-defined virtual ground is established and ideally no signal current flows through the ground plane. This choice avoids the complex and time consuming task of accurate modelling the reactive effects of the ground metal layer in layout [22], [23]. Moreover, in view of active phased arrays with several amplifiers on the same chip, a differential configuration provides common mode noise rejection (e.g. supply and ground noise). Considering the schematic of the 1-stage amplifier

in Fig. 2.12(a), C_{1a}-C_{2a} with the coupled coils L_{1a}-L_{2a} and C_{3a}-C_{4a} with L_{3a}-L_{4a} form the input and output matching networks respectively, designed to provide conjugate impedance matching to 50 Ω at 150 GHz. The capacitors (C_{1a-4a}), of relatively small value, are implemented with a custom layout as a parallel plate structure with M_3-M_5 metal layers, and precisely sized with electromagnetic (EM) simulations. Being the input and output signals at the GSG pads single-ended, the coupled coils at the input (L_{1a}-L_{2a}) and output (L_{3a}-L_{4a}) perform single-ended to differential conversion and vice versa. The inductors are sized and simulated together with the GSG pad. As an example, Fig. 2.13 shows the 3D layout of the input transformer (L_{1a}-L_{2a}) connected to the pads. L_{1a} is realized in the two metal levels below the topmost layer (M_6-M_7) in a stack with a diameter of 42 µm and a width of 11 µm. L_{2a} is implemented in the topmost metal layer (M_8) with the same diameter and width of L_{1a}. The center of the L_{2a} is tapped for biasing of input transistors. A side-wall around the coupled inductors, acting as a shield from the surrounding structures in the final amplifier layout, is realized by stacking M_1-M_7 metal layers, and included in the EM simulations. The estimated equivalent inductances ($L_{eq} = \mathrm{Im}[Z]/\omega$) of L_{1a} and L_{2a} are 28 pH and the quality factors ($Q = \mathrm{Im}[Z]/\mathrm{Re}[Z]$) are 16 and 19 respectively at 150 GHz. The coupling coefficient, defined as $k = \mathrm{Im}[Z_{21}]/\sqrt{\mathrm{Im}[Z_{11}] \cdot \mathrm{Im}[Z_{22}]}$, is 0.55. The layout of the output transformer (L_{3a}-L_{4a}) is similar to L_{1a}-L_{2a} but the spirals are sized such that $L_{3a} = 105$ pH, $L_{4a} = 95$ pH, and k=0.6. The supply voltage for the cascode pair is fed by a center tap on L_{3a}.

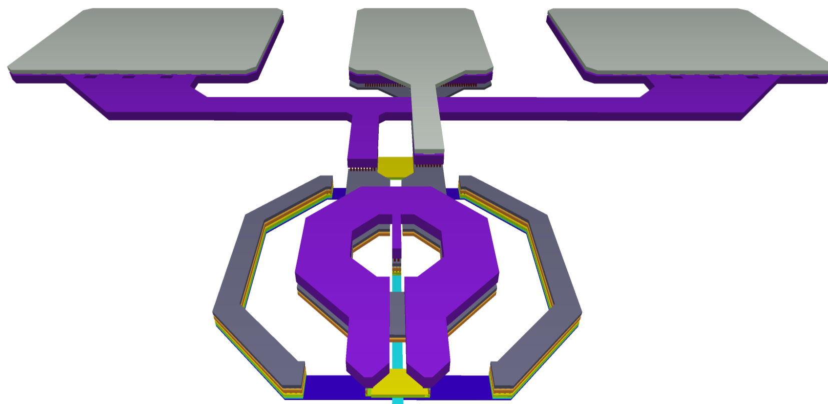


Figure 2.13: Layout of the input matching network of one-stage amplifier.

In the two-stage amplifier, the input and the output baluns are similar to the single-stage design and an additional transformer is employed as an inter-stage matching network with center taps in primary and secondary coils to provide supply and bias voltage to the first and second stage respectively. The inductors are sized to resonate with the parasitic capacitances of transistors and resonance frequencies are stagger tuned to enlarge the bandwidth. The 3D layout view of the inter-stage transformer is drawn in Fig. 2.14. Being $L_{3b} = 148$ pH, higher then $L_{4b} = 90$ pH, a planar geometry with both coils in the topmost metal layer is selected giving higher Q (∼20) and self-resonance frequency. A grounded side-wall stacking M_1-M_7 is also included to shield the component.

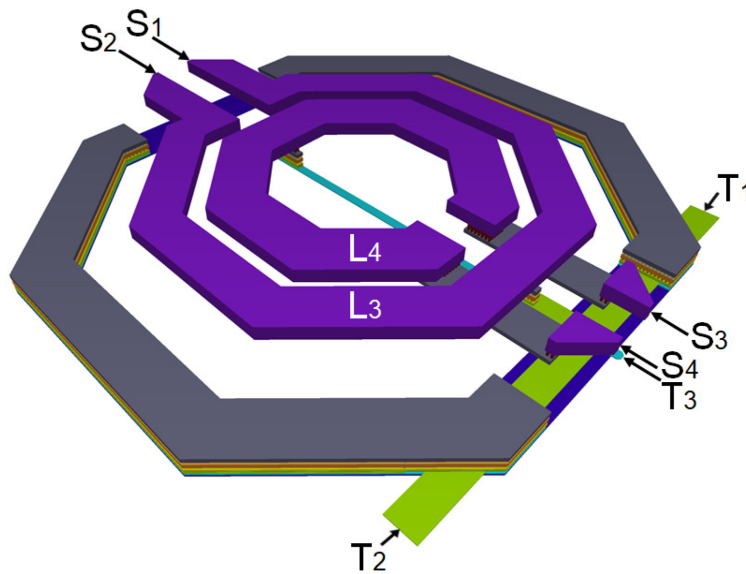


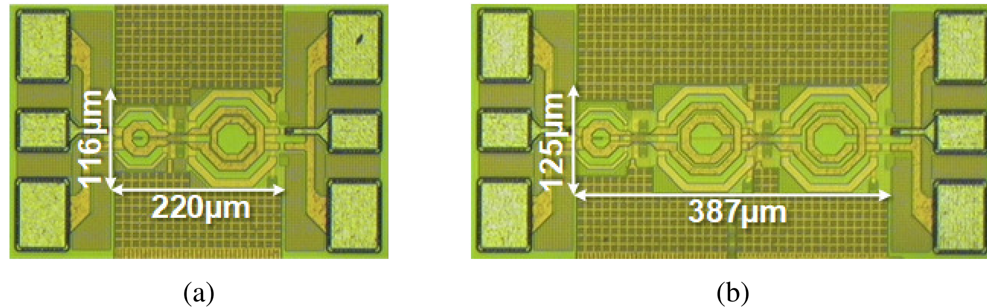
Figure 2.14: Layout of the transformer in 2-stage amplifier.

2.3.2 Experimental Results

The microphotographs of the fabricated amplifiers are shown in the Fig. 2.15. The core of the one-stage and twostage amplifier occupies very small area of 116 μm×220 μm (0.026 mm^2) and 125 μm×387 μm (0.048 mm^2) respectively.

Small-signal measurement was performed using VDI WR-6.5 D-Band Extenders with Agilent PNA-E8361C vector network analyzer (VNA) and N5260A Millimeter Head

Controller. Input and output pads were designed for 75 µm pitch GSG probes. The TRL probe tip calibration has been applied with Cascade standard substrate (138-356).



(a) (b)

Figure 2.15: Chip microphotograph of the (a) 1-stage and (b) 2-stage differential amplifiers.

Fig. 2.16 plots the measured S-parameters and Rollet stability factor for the one-stage amplifier (red curves). The amplifier draws 14.2 mA from 1.9 V and displays a peak gain of 8 dB at 156 GHz with -3 dB bandwidth of 17.8 GHz and unconditional stability over D-band. The same plot in Fig. 2.16 compares measurements against simulations proving an excellent agreement.

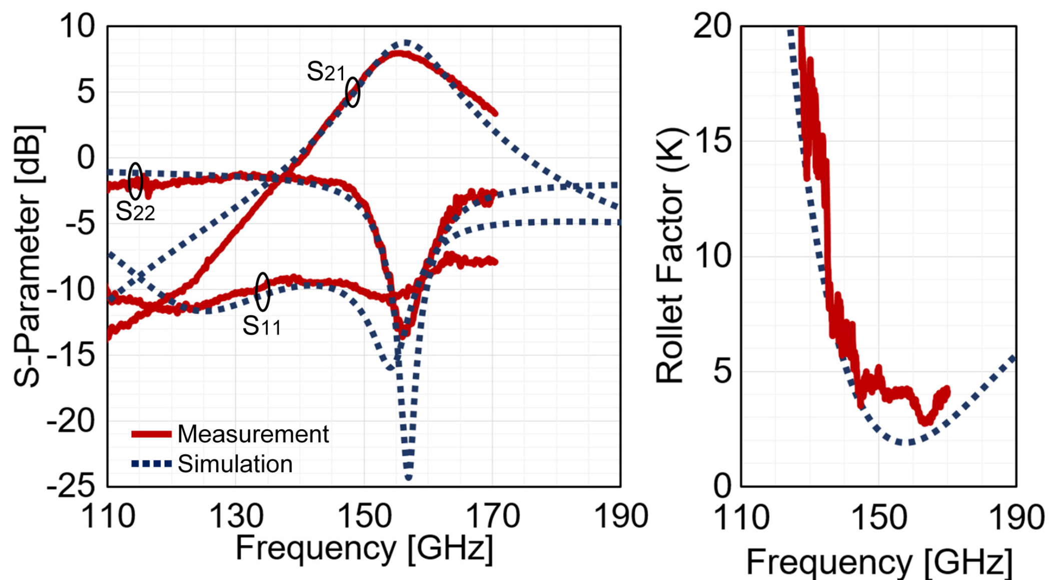


Figure 2.16: S-Parameter comparison of measurement and simulation for one-stage amplifier.

S-parameter measurements for the two-stage amplifier are plotted in Fig. 2.17 (red curves). With 28.4 mA from 1.9 V supply voltage, the amplifier reaches a peak gain of

17.4 dB at 157 GHz with -3 dB bandwidth of 42.7 GHz. Simulations, with dotted lines in the same plots, are still in very good agreement with measurements.

The noise figure (NF) at 150 GHz, derived from simulations, is 11.4 dB and 10.5 dB for the one-stage and two-stage amplifiers, respectively while the output power at 1 dB gain compression is -1.9 dBm and 1.8 dBm.

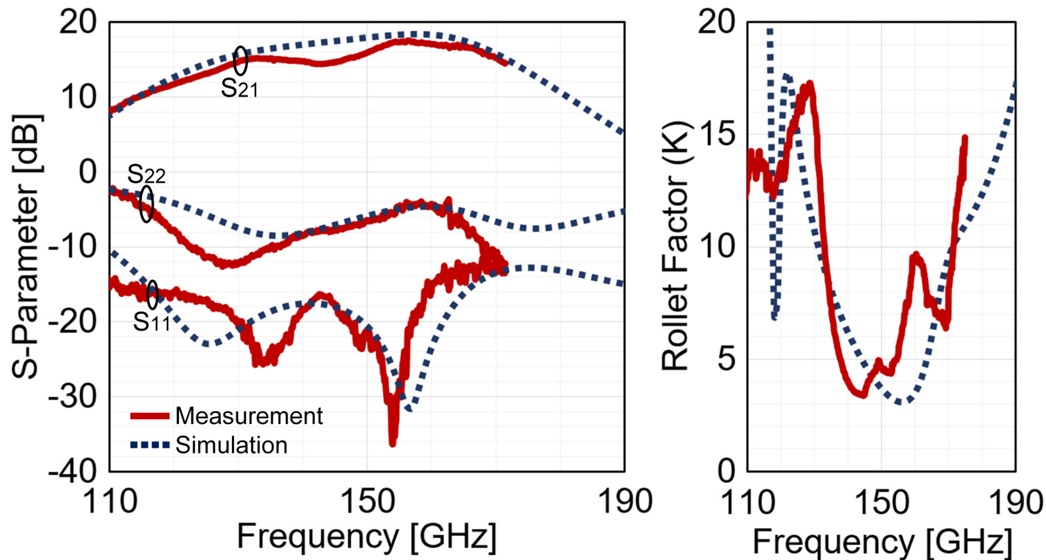


Figure 2.17: S-Parameter comparison of measurement and simulation for two-stage amplifier.

2.4 Conclusion

In this chapter compact D-band amplifiers were presented. To solve the current return path issue 2 different solutions were proposed. In the design of single-ended amplifiers, to account current return path, accurate, yet simple modelling of inductors was presented. In the Section 2, differential amplifiers made use of differential structure and symmetric layout to solve the problem.

Measurement results are summarized in Table 2.1 and compared with other SiGe HBT amplifiers operating above 100 GHz. [15] was among the first works demonstrating silicon amplifiers in D-band (to Authors knowledge). The amplifier, with 5 CE stages and based on lumped-component matching networks, features lower gain with less bandwidth and larger area occupation than the 2-stage amplifiers presented in this work. [16–19] are two-stage amplifiers with cascode HBT configuration and

transmission line matching networks. The two-stage amplifiers presented in this work has the same transistor configuration and number of stages. Therefore, a direct and fair comparison is possible. The presented amplifiers are highly compact, with 2× to 5.7× smaller area. Even though [16] and [18] have slightly higher (1.4× and 1.5× for single-ended, 1.1× and 1.2× for differential) gain-bandwidth product (GBW), which partially benefit by the lower center frequency, the area occupation is significantly larger (5.7× and 3.7× for single-ended, 6.9× and 4.5× for differential). Nevertheless, by adding one more stage to the current design the GBW can be significantly increased still maintaining advantage on area occupation.

	This Work				**[15]**	**[16]**	**[17]**	**[18]**	**[19]**
	S.E.		**DIFF.**						
Technology	55 nm				130 nm	130 nm	130 nm	130 nm	130 nm
f_t/f_{max} [GHz]	320/370				230/300	250/300	300/500	300/500	300/500
# Stages	1	2	1	2	5	2	2	2	2
Gain [dB]	11.8	20.1	8	17.4	17	25	20.5	27.5	16.1
Center Freq. [GHz]	152	150	156	150	140	120	110	125	143
-3 dB Bandwidth [GHz]	17.9	24.5	17.8	42.7	16	20	20	16	11
Gain-Bandwidth Product [GHz]	69.6	247.8	44.7	316.5	113.3	355.7	211.9	379.4	70.2
NF [dB]	9.7**	10.2**	11.4**	10.5**	-	9**	4	6.5	7.7
PDC [mW]	13.5	27	27	54	112	54	17	12	36.8
Core Area* [mm^2]	0.031	0.058	0.026	0.048	0.080	0.330	0.220	0.214	0.107

*Estimated from chip photographs excluding PADs
**Simulation

Table 2.1: Comparison with SiGe amplifiers above 100 GHz

Chapter 3

Analysis and Design of Wideband Amplifiers for D-Band Applications

3.1 Introduction

In D-band spectrum the total usable bandwidth for fixed wireless services is 31.8 GHz as mentioned in the Chapter 1. A key challenge in the design of amplifiers for such systems is providing enough gain over the full bandwidth, requiring a gain-bandwidth product (GBW) of several hundred GHz. Distributed amplifiers in SiGe HBT technology demonstrated over 500 GHz GBW in D-band, but with high power consumption [25, 26]. Tuned amplifiers save power but in D-band the design is made challenging by the low available gain of transistors, operating close to f_{max}. To boost the transistor's gain beyond the Maximum Available Gain (MAG), different strategies for device unilateralization have been investigated, but over limited bandwidth [27–29]. In general, tuned amplifiers have to be realized with several cascaded stages, conjugately matched for maximum power transfer. However, matching networks are inherently narrow-band, exacerbating the GBW issue. Several D-band multi-stage tuned amplifiers have been demonstrated in CMOS [30–33] and SiGe HBT technology [34–45], with the latter showing a significant GBW advantage. The choice of the transistor configuration also plays a key role on the amplifier performance. In fact, the achievable bandwidth of an impedance-matched gain stage is bounded by the nodal quality factor (Q_n) of the impedances to be matched, i.e., the input and output impedance presented by the active stage [46]. The most widely adopted transistor configurations for D-band amplifiers are the common-emitter and cascode. While Q_n of the impedance at the base and collector of an HBT in common emitter is relatively low, facilitating wideband matching, transistors in the cascode configuration rise substantially Q_n of the output impedance, making broadband matching difficult

[36, 38–40, 42, 45]. On the other hand, the cascode stage is typically preferred because of the remarkably higher available gain.

In this work, the common-emitter and cascode gain stages are first compared, focusing on the impedance matching issues for designing high GBW amplifiers in D-band. The non-linear relation between gain and bandwidth in resonant matching networks is then formally analyzed proving that when the gain stage displays high nodal quality factor at the output port, like the cascode, if power gain is slightly penalized by rising the load reflection coefficient the bandwidth is significantly increased, finally giving a remarkable improvement on the amplifier GBW. The analysis is further extended to derive the optimal load reflection coefficient to maximize the power gain or the GBW in the practical case of matching networks realized with lossy reactive components. D-band amplifiers with 1-, 2- and 3-stage are designed in 55 nm SiGe BiCMOS technology from STMicroelectronics to validate the analysis and to demonstrate the high achievable GBW. The 2-stage and 3-stage amplifiers prove 20.6 dB gain with 65.8 GHz bandwidth and 28.6 dB gain with 64.3 GHz bandwidth respectively. The GBW of 705 GHz and 1731 GHz are comparable or higher then distributed amplifiers with a remarkably lower power consumption. The paper is organized as follow. Section-3.2 compares in detail the differences in gain, bandwidth, input and output impedances of common emitter and cascode stages. Section-3.3 analyzes the gain-bandwidth trade-off with respect to the load reflection coefficient in resonant matching networks, and show how to apply the concept for GBW extension with a cascode amplifier. Section-3.4 describes the design of amplifiers while measurements are presented in Section-3.5. Finally, Section-3.6 compares experimental results with state of the art and concludes the paper.

3.2 Review of Common-Emitter and Cascode Gain Stages

The active gain stages in D-band amplifiers are commonly implemented with transistors in common emitter (CE) or with the cascode configuration, shown in Fig. 3.1. The two alternatives are analyzed and compared in this section, focusing on the available gain and the issues related to broad-band impedance matching. The

same transistor is used, with an emitter area of 0.2 µm × 5.1 µm, with a collector to base voltage $V_{CB} = 0$ and a current of 7 mA which provides $f_{max} = 290$ GHz.

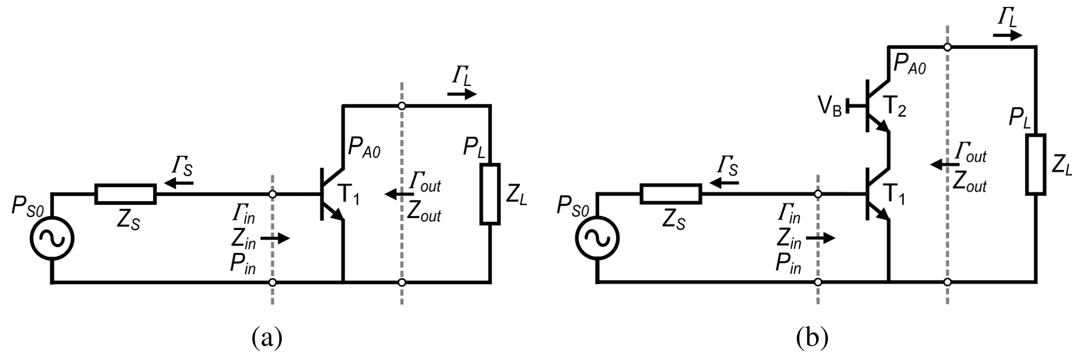


Figure 3.1: Common emitter (a) and cascode (b) gain stages.

The simulated MAG versus frequency for the two alternatives in Fig. 3.1 is shown in Fig. 3.2. Looking at Fig. 3.2, at 150 GHz the MAG of the CE stage is 5.5 dB only, while the cascode yields a remarkable improvement [43, 47]. The stacked common-base transistor (T2 in Fig. 3.1(b)) rises significantly the output impedance with a minimal penalty on the short-circuit transconductance of the stage [48]. As a result, the MAG increases to 15 dB, roughly equivalent to the cascade of three conjugately matched CE amplifiers.

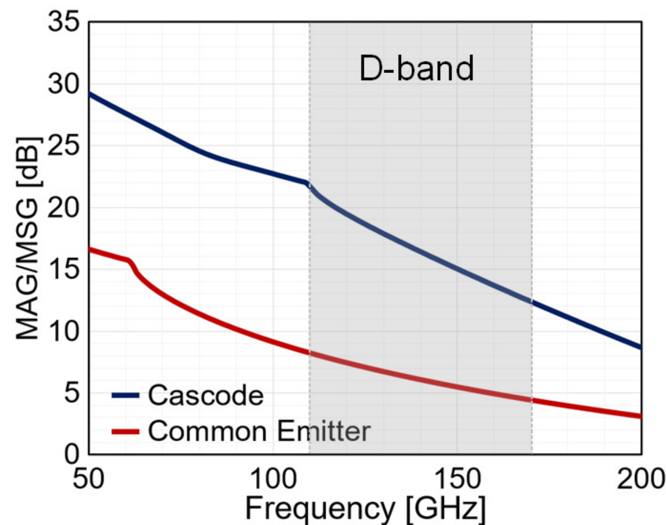


Figure 3.2: MAG/MSG versus frequency for the common emitter and cascode active stages.

The MAG is the upper bound on transducer power gain, reached with an optimal source impedance, Z_{S-opt}, which maximizes the available power gain, $G_A = P_{A0}/P_{S0}$

(being P_{A0} and P_{S0} the available power from the amplifier stage and from the source) and the optimal load impedance, Z_{L-opt}, which maximizes the operating power gain, $G_P = P_L/P_{in}$ (with P_L the power delivered to the load and P_{in} the power delivered by the source, i.e. the input power to the transistor). In this condition the active stage is also conjugately matched at the input and output, i.e. $Z_{S-opt} = Z^*_{in}$, $Z_{L-opt} = Z^*_{out}$.

The required source and load impedances influence the achievable bandwidth. Assuming a simple resonant network is used to match a 50 Ω resistance to Z_S, Z_L, the bandwidth can be approximated as $BW = 2f_0/Q_n$ where f_0 is the center frequency and $Q_n = Im[Z_n]/Re[Z_n]$ (n=S,L) [46]. The optimal source and load impedances at 150 GHz are shown on the Schmitt chart in Fig. 3.3 together with curves of constant Q_n. Z_{S-opt} and Z_{L-opt} for the CE transistor fall within the Q = 1.2 curve, thus not introducing any limitation to the amplifier bandwidth. With the cascode configuration, Q of Z_{S-opt} remains low, but because of the high resistance at the collector of T2, Z_{L-opt} is remarkably higher than for the CE transistor alone and Q of Z_{L-opt} is raised to 20.8, posing a serious bandwidth issue (BW≈14 GHz) with impedance matching.

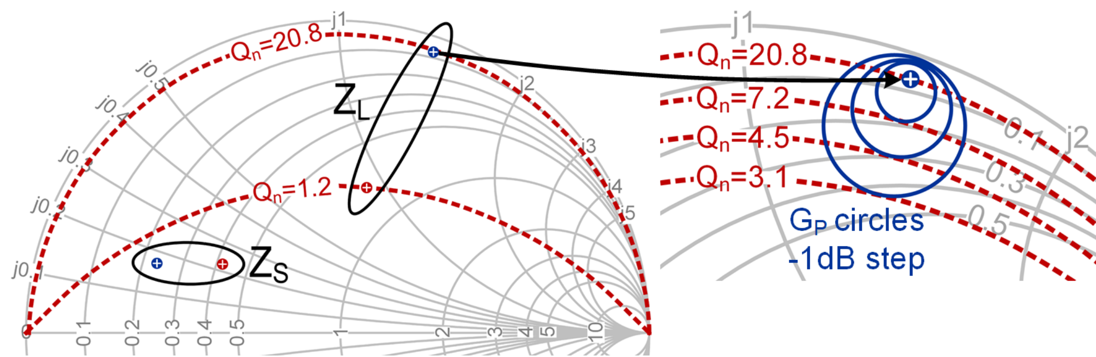


Figure 3.3: Optimal source and load impedances at 150 GHz for the common emitter and cascode active stages.

In summary, the CE transistor is penalized by a low upper bound on power gain but it allows simple wideband matching. On the opposite, the cascode features a remarkably higher MAG but rises challenges in matching networks design. It is worth noticing that cascode gain can be further increased by adding inductors at the emitter and/or base terminals of the common-base transistor (T2 in Fig. 3.1(b)) [42, 44, 45, 48, 49], still with the challenge of wideband output matching. Furthermore, although the analysis has been quantitatively performed on a specified transistor size, the conclusion remains

valid in general, being MAG and Q_n of the optimal source and load impedances nearly independent from the emitter area at fixed current density.

Considering the very low MAG in D-band of the CE transistor, the cascode remains preferable, allowing a wider design space to trade gain for bandwidth. To this purpose, a simple solution is to select a load impedance with lower Q. In the right of Fig. 3.3 constant GP circles around Z_{L-opt} are drawn, with steps of -1dB from the MAG value. Q decreases very quickly as Z_L shifts toward the center of the chart. As an example, with 3 dB of gain penalty Q is reduced from 20.8 to 3.1, yielding more than six times wider bandwidth and hence an overall improvement in the gain-bandwidth product. This trade-off is quantitatively analyzed in the next section considering first the realistic situation of matching the cascode output impedance to a general impedance (with resistive and reactive components) and, in a second step, including the impact of the losses in the matching network components.

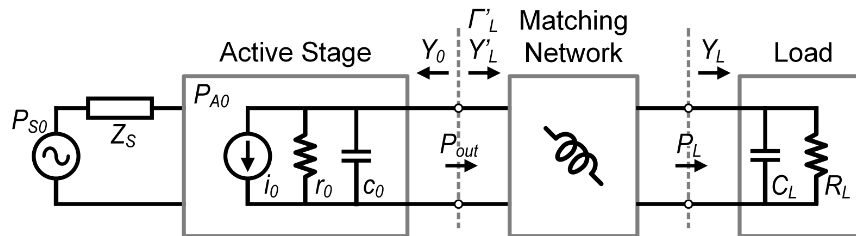


Figure 3.4: Equivalent circuit of the cascode stage driven by Z_{S-opt} and with matching toward the equivalent impedance at the GSG pad.

3.3 Anaylsis of Cascode Output Matching Network

The trade-off and optimal design of a resonant matching network at the output of the cascode stage is studied in this section considering the practical situation depicted in Fig. 3.4. We assume the cascode is terminated at the input with the source impedance Z_S. In this way the cascode output impedance, the available power gain, G_A, and the available power $P_{A0} = G_A \cdot P_{S0}$ are fixed. A matching network is placed between the output port and the load (represented by $R_L \parallel C_L$). In the neighborhood of the center frequency, f_0, the output port of the cascode can be modelled with an equivalent output resistance r_0, capacitance c_0 and the current source i_0 $(=2\sqrt{P_{A0}/r_0})$. The nodal quality factor at the cascode ouptput port, $Q_0 = 2\pi f_0 r_0 c_0$, is relatively high (from the example

in Sec. 3.2, $Q_0 = 20.8$ if $Z_S = Z_{S-opt}$). On the opposite, the nodal quality factor of the load impedance, $Q_L = 2\pi f_0 R_L C_L$, is assumed low because $R_L \parallel C_L$ represents the input impedance of a cascaded stage ($Q_L \approx 0.6$ from Sec. 3.2) or the equivalent impedance at the ground-signal-ground (GSG) pad, where the impedance of the pad parasitic capacitance is reasonably higher than the terminating resistance. Having represented equivalent circuits with parallel elements it is convenient to analyze the network with the admittance parameters. The matching network transforms the load admittance, $Y_L = R_L^{-1} + j\omega C_L$, to the admittance Y'_L seen by the cascode. Let's assume the network is designed such that the susceptance of $Y'_L(f_0)$ is the conjugate of the susceptance of $Y_0(f_0)$ ($\mathrm{Im}[Y'_L(f_0)] = -\mathrm{Im}[Y_0(f_0)]$). In this case the reflection coefficient at the output of the active stage Γ'_L is set by the real part of Y'_L and Y_0. By defining $R'_L = (Re[Y'_L(f_0)])^{-1}$ and being $r_0 = (Re[Y_0(f_0)])^{-1}$:

$$\Gamma'_L = \frac{R'_L - r_0}{R'_L + r_0} = \frac{1 - \dfrac{r_0}{R'_L}}{1 + \dfrac{r_0}{R'_L}} \tag{3.1}$$

Maintaining generality on the matching network topology we want to estimate the achievable bandwidth and how gain and bandwidth are influenced by the reflection coefficient given by (3.1). The analysis follows the law of conservation of complex power as in [50]. First, a lossless case is considered, i.e., a matching network realized with ideal reactive components. The impact of lossy components is evaluated in a second step.

3.3.1 Lossless Matching Network

Having assumed that $\mathrm{Im}[Y_0(f_0)] = -\mathrm{Im}[Y'_L(f_0)]]$, the capacitors c_0 and C_L resonate with the reactive components in the matching network, while only resistors r_0 and R_L dissipate active power. Denoting with W_t the total reactive energy stored, and with P the total dissipated active power, the loaded network quality factor is:

$$Q_{loaded} = \frac{2\pi f_0 W_t}{P} \tag{3.2}$$

and the bandwidth can be approximated with [46]:

$$BW = \frac{f_0}{Q_{loaded}} \tag{3.3}$$

Although eq. (3.2) with Q given by (3.1) is rigorously valid only for simple LC tanks, it yields a reasonably accurate estimation of the bandwidth also for a general resonator, particularly if Q is high [51].

If the matching network in Fig. 3.4 is realized only with components storing magnetic energy (i.e., inductors) the reactive energy at resonance is equal to the electrical energy stored in c_0 and C_L, denoted by W_{C_0} and W_{C_L} respectively. The nodal quality factors of Y_0 and Y_L allow to express W_{C_0} and W_{C_L} as a function of P_{r_0} and P_L, the active power dissipated on r_0 and R_L:

$$W_t = W_{c_0} + W_{C_L} = \frac{Q_0 P_{r_0} + Q_L P_L}{2\pi f_0} \tag{3.4}$$

By using (3.4), the loaded quality factor given by (3.2) can be rewritten as:

$$Q_{loaded} = \frac{Q_0 P_{r_0} + Q_L P_L}{P_{r_0} + P_L} = \frac{Q_0 \frac{P_{r_0}}{P_L} + Q_L}{\frac{P_{r_0}}{P_L} + 1} \tag{3.5}$$

Eq. (3.4) and (3.5), suggest that a matching network comprising only inductors is preferable for maximum bandwidth. In fact, any other capacitor (in addition to c_0 and C_L) would rise the reactive energy and the loaded quality factor, finally penalizing the bandwidth.

Eq. (3.5) shows that for a given active stage and load (i.e., Q_0, Q_L) the loaded Q is determined by the ratio between the power dissipated in the transistor output resistance and the active power delivered to R_L. Being $Q_0 >> Q_L$, from (3.5) the Q can be reduced (increasing the bandwidth) by reducing the P_{r_0}/P_L ratio.

From Fig. 3.4, $r_0^{-1} = \mathrm{Re}[Y_0]$ and $R'_L = \mathrm{Re}[Y'_L]$ form a current divider for i_0. Considering the available power from the active stage and with the lossless matching network assumption (i.e. $P_L = P_{out}$), the powers P_{r_0} and P_L normalized to P_{A0} are:

$$\frac{P_{r_0}}{P_{A0}} = \left(\frac{2}{1 + \frac{r_0}{R'_L}} \right)^2 = (1 + \Gamma'_L)^2 \tag{3.6}$$

$$\frac{P_{out}}{P_{A0}} = \frac{P_L}{P_{A0}} = \left(\frac{2}{1 + \frac{r_0}{R'_L}} \right)^2 \frac{r_0}{R'_L} = 1 - {\Gamma'_L}^2 \tag{3.7}$$

Eq. (3.7) represents the transducer power gain, G_{T-MN}, of the matching network. Combining (3.6), (3.7) with (3.5), the loaded quality factor can be rewritten as:

$$Q_{loaded} = \frac{Q_0 + Q_L \frac{r_0}{R'_L}}{1 + \frac{r_0}{R'_L}} = \frac{1}{2}(Q_0(1+\Gamma'_L) + Q_L(1-\Gamma'_L)) \tag{3.8}$$

If $\Gamma'_L = 0$ the amplifier is conjugately matched. From (3.7) $P_L = P_{A0}$ and from (3.8) the Q_{loaded} is the arithmetic mean of Q_0 and Q_L ($Q_{loaded} = (Q_0 + Q_L)/2$). A positive Γ'_L ($R'_L > r_0$) penalizes both power gain and bandwidth, because with $0 < \Gamma'_L < 1$, P_L is reduced and the loaded quality factor tends to be Q_0 (which is assumed $\gg Q_L$). On the other hand, if Γ'_L is negative ($R'_L < r_0$) the power gain is still reduced but the bandwidth increases. In fact, $-1 < \Gamma'_L < 0$ limits P_L but moves the loaded quality factor towards to Q_L ($\ll Q_0$). For a relatively small negative Γ'_L the bandwidth grows much faster than the gain penalty, improving the amplifier GBW.

It is worth noticing that $\Gamma'_L < 0$ is effective for GBW extension only if the nodal quality factor of the active stage is much higher than the nodal quality factor of the load to be matched, which is indeed the typical case with a cascode active stage. If $Q_0 \ll Q_L$ GBW is enhanced by $\Gamma'_L > 0$. But if $Q_0 \simeq Q_L$, from (7) and (8) $\Gamma'_L \neq 0$ penalizes gain without changing Q_{loaded} and hence the bandwidth.

3.3.2 Matching Network with Lossy Components

We now consider the practical case of lossy components in the matching network, i.e., reactances featuring a finite quality factor, Q_r. In this situation the matching network dissipates a fraction of the stored reactive energy:

$$P_{diss} = 2\pi f_0 W_t / Q_r \tag{3.9}$$

The above equation reveals that the power lost is minimized, for a given Q_r, if the matching network comprises only magnetic components resonating with c_0 and C_L, because $W_t = W_{C_0} + W_{C_L}$ is minimized. Any capacitor included in the matching network would rise the reactive energy above this minimum and consequently the power lost in the network.

From Fig. 3.4, the active power delivered by the cascode stage is:

$$P_{out} = P_{diss} + P_L \tag{3.10}$$

From (3.10), it may happen that with a lossy matching network $\mathrm{P_{diss} = P_{out}}$, hence $\mathrm{P_L = 0}$. This condition sets an upper bound on the achievable reflection coefficient, $\Gamma'_{\mathrm{L-max}}$. $\mathrm{P_L = 0}$ leads to $\mathrm{W_{C_L} = 0}$ and the total reactive energy in (3.9) corresponds only to the electrical energy stored by the output capacitance $\mathrm{c_0}$ in Fig. 3.4, $\mathrm{W_t = W_{c_0} = P_{r_0} Q_0/(2\pi f_0)}$. Using (3.6), (3.7) to express $\mathrm{P_{r_0}}$ and $\mathrm{P_{diss} = P_{out}}$ as a function of $\Gamma'_{\mathrm{L-max}}$, (3.9) can be written as:

$$1 - {\Gamma'_{L-max}}^2 = (1 + \Gamma'_{L-max})^2 \frac{Q_0}{Q_r} \tag{3.11}$$

whose solution is:

$$\Gamma'_{L-max} = \frac{1 - \dfrac{Q_0}{Q_r}}{1 + \dfrac{Q_0}{Q_r}} \tag{3.12}$$

For $\Gamma'_{\mathrm{L}} < \Gamma'_{\mathrm{L-max}}$, $\mathrm{P_L}$ and $\mathrm{W_{C_L} > 0}$. Replacing $\mathrm{P_{diss}}$ given by (3.9) in (3.10), with $\mathrm{W_t}$ given by (3.4), and making use of (3.6), (3.7) to express $\mathrm{P_{r_0}}$ and $\mathrm{P_{out}}$ as a function of Γ'_{L}, leads to:

$$(1 - {\Gamma'_L}^2) P_{A0} = \frac{(1 + \Gamma'_L)^2 P_{A0} Q_0 + P_L Q_0}{Q_r} + P_L \tag{3.13}$$

which can be solved to find the transducer gain with the lossy components in the matching network:

$$G_{T-MN} = \frac{P_L}{P_{A0}} = \frac{1}{1 + \dfrac{Q_L}{Q_r}} \left((1 - {\Gamma'_L}^2) - \frac{Q_0}{Q_r} (1 + \Gamma'_L)^2 \right) \tag{3.14}$$

The above equation highlights that an optimal reflection coefficient exists, $\Gamma'_{\mathrm{L-opt}}$ to maximize the power gain:

$$\Gamma'_{L-opt} = -\frac{Q_0}{Q_0 + Q_r} \tag{3.15}$$

and with $\Gamma'_{\mathrm{L}} = \Gamma'_{\mathrm{L-opt}}$ the maximum matching network transducer gain is:

$$G_{T-max} = \frac{1}{\left(1 + \dfrac{Q_L}{Qr}\right)\left(1 + \dfrac{Q_0}{Q_r}\right)} \tag{3.16}$$

Turning now to the bandwidth, it can still be estimated with (3.3) but with Q_{loaded} given by:

$$Q_{loaded} = \frac{2\pi f_0 W_t}{P_{r_0} + P_{diss} + P_L} \tag{3.17}$$

As intuitively expected, the lossy matching network reduces Q_{loaded} (thus increasing the bandwidth) because of the inclusion of P_{diss} in the denominator of (3.17). Replacing W_t from (3.4) and expressing the active powers in (3.17) by means of Γ_L', Q_{loaded} can be rewritten as follows:

$$Q_{loaded} = \frac{1}{2\left(1+\dfrac{Q_L}{Q_r}\right)}\left(Q_0(1+\Gamma_L') + Q_L(1-\Gamma_L')\right) \tag{3.18}$$

The dependence of Q_{loaded} on Γ_L' remains the same as for the lossless network (with Q_{loaded} given by (3.8)). In particular, with $-1 < \Gamma_L' < 0$ Q_{loaded} tends to Q_L ($\ll Q_0$) thus raising the amplifier bandwidth. The impact of the finite quality factor of the network reactances, Q_r, on Q_{loaded} is captured by the term $(1 + Q_L/Q_r)$ in the denominator of (3.18). It is interesting to note that the effect is limited in practice because $Q_L \ll Q_r$. However, the lossy network mandates selection of $\Gamma_L' < 0$ also to maximize the power gain (with Γ_{L-opt}' given by (3.15)) and this choice also increases the bandwidth by shifting Q_{loaded} towards to Q_L.

3.3.3 Comparison with Simulations

The most relevant equations from the above analyses are plotted in this section and validated against circuit simulations. The circuit schematic considered is shown in Fig. 3.5, with realistic component values. The active stage is modelled with r_0=1.45 kΩ, c_0=15.2 fF, which correspond to the output impedance at f_0=150 GHz, of the cascode active stage considered in Sec. 3.2 terminated at the input with Z_{S-opt}. The load comprises R_L=29 Ω, C_L=22 fF which represent the impedance at the GSG pad (terminated on 50 Ω employed for the design of the amplifiers described in the next section. With the above component values $Q_0 = 20.8$, $Q_L = 0.6$. The matching network is realized with the 3 inductors L_1-L_3, sized to have $\mathrm{Im}[Y_L'] = -\mathrm{Im}[Y_0]$ and different values of $R_L' = 1/\mathrm{Re}[Y_L']$ thus different values of Γ_L'.

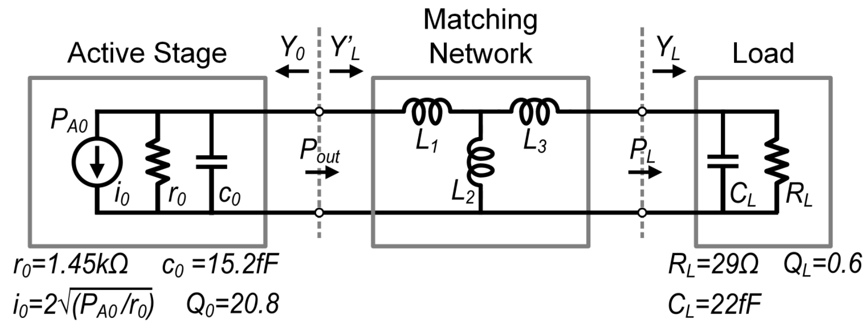


Figure 3.5: Circuit schematic used to validate the analysis with simulations.

First, inductors are assumed lossless. Fig. 3.6(a) compares the calculated transducer power gain, given by (3.7), and bandwidth given by (3.2) with Q_{loaded} in (3.8), against simulations. As previously discussed, $\Gamma'_L > 0$ penalizes gain and bandwidth while $\Gamma'_L < 0$ reduces the gain but increases the bandwidth, thus initially improving the GBW until a maximum is achieved. The calculated gain matches perfectly with simulations, because no simplifying assumptions have been made in calculations. The agreement between (3.2), (3.3) and the simulated bandwidth, measured as the frequency points at -3 dB from the maximum gain, is very good at high Q_{loaded}, (toward positive values of Γ'_L). At low Q_{loaded} a discrepancy between simulations and calculations is observed, because (3.2) and (3.3) are rigorously valid only for simple series or parallel resonators. Nevertheless, the analysis allows to explain and still predict reasonably well the dependence of bandwidth on Γ'_L.

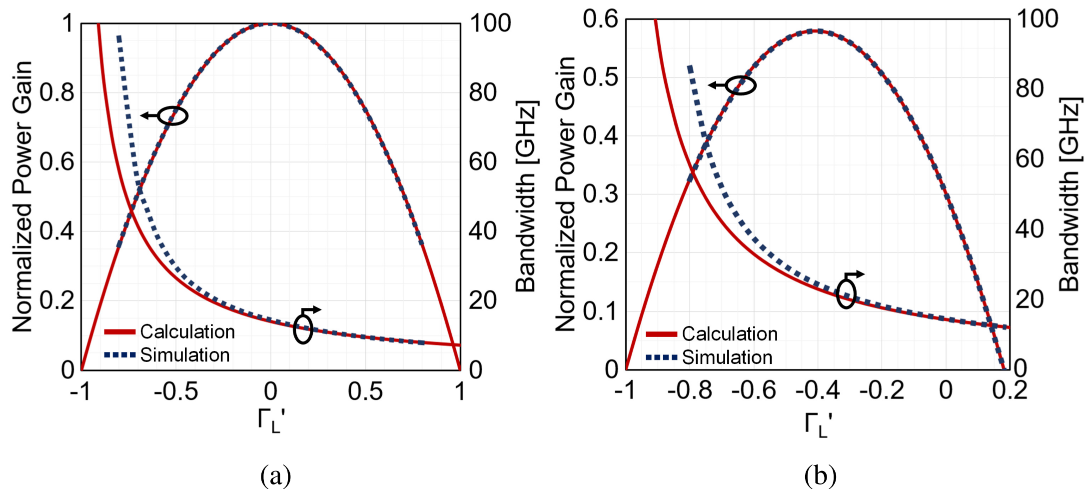


Figure 3.6: Comparison of calculation with simulation for (a) lossless, (b) lossy matching network, Normalized gain and bandwidth.

Simulations and calculations with lossy inductors are then reported in Fig. 3.6(b). In this case, a resistance in series with L_1-L_3 is included in simulations to have $Q_r = 30$ at f_0=150 GHz. Fig. 3.6(b) compares the transducer power gain, calculated with (3.14), and bandwidth, given by (3.2) with Q_{loaded} in (3.18), against simulations. From (3.12), the finite Q_r limits the maximum achievable reflection coefficient to $\Gamma'_{L-max} = 0.18$, confirmed by the simulations. As expected from (3.15), the maximum gain ($G_{T-MN-max} = 0.58$) is now achieved with a negative reflection coefficient, $\Gamma'_{L-opt} = -0.41$. With $\Gamma'_L > \Gamma'_{L-opt}$ both the gain and bandwidth are penalized while for $\Gamma'_L < \Gamma'_{L-opt}$ the gain is reduced but the bandwidth increases, enhancing the GBW.

3.4 Design of Amplifiers

D-band amplifiers have been designed in the STMicroelectronics' BiCMOS 55 nm technology leveraging the insights derived in the previous section. The active stage is the cascode structure introduced in Sec. 3.3, made of two equal HBTs of 0.2 µm × 5.1 µm emitter area and biased at 7 mA. Input and output matching networks are implemented with transmission lines (TLINEs) allowing a precise and reliable design thanks to the scalable models accounting both forward and return current paths.

The TLINE is a shielded microstrip structure, as depicted in Fig. 3.7(b), the unit length of a transmission line is often represented with a lumped elements, i.e., series resistance, series inductance, shunt conductance and shunt capacitance.

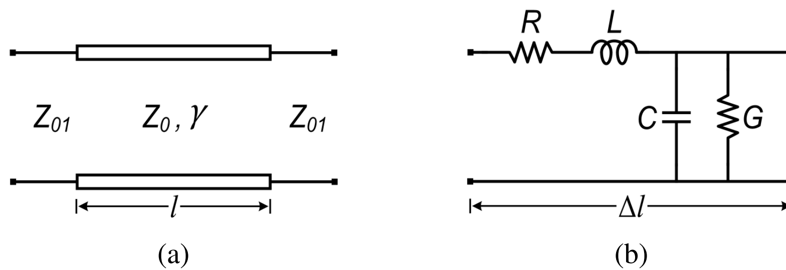


Figure 3.7: (a) Tline 2-port network, (b) distributed-element circuit model of a Tline

In order to measure the 2-port network and distributed model parameters, we make use of the relation between S-parameters and ABCD matrix [52]. The ABCD matrix of a

2-port network depicted in Fig. 3.7(b):

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh(\gamma l) & Z_C \sinh(\gamma l) \\ \dfrac{\sinh(\gamma l)}{Z_0} & \cosh(\gamma l) \end{bmatrix} \tag{3.19}$$

If we write A, B, C, D parameters with respect to S-Parameters:

$$\begin{aligned} A &= \frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{2S_{21}} \\ B &= \frac{(1+S_{11})(1+S_{22})-S_{12}S_{21}}{2S_{21}} \cdot Z_{01} \\ C &= \frac{(1-S_{11})(1-S_{22})-S_{12}S_{21}}{2S_{21}} \cdot \frac{1}{Z_{01}} \\ D &= \frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{2S_{21}} \end{aligned} \tag{3.20}$$

Due to the symmetry, Eq. (3.20) can be simplified, and substituting A, B, C and D into (3.19), the complex propagation constant (γ) and characteristic impedance (Z_0) are expressed in terms of S-parameters:

$$\begin{aligned} \gamma &= \frac{-1}{l} \cdot \ln\left(\frac{2S_{21}}{1-S_{11}^2+S_{21}^2 \pm \sqrt{(1+S_{11}^2-S_{21}^2)^2-4S_{11}^2}} \right) \\ Z_0 &= \pm Z_{01} \cdot \sqrt{\frac{(1+S_{11})^2-S_{21}^2}{1-S_{11})^2-S_{21}^2}} \end{aligned} \tag{3.21}$$

In order to derive distributed circuit parameters:

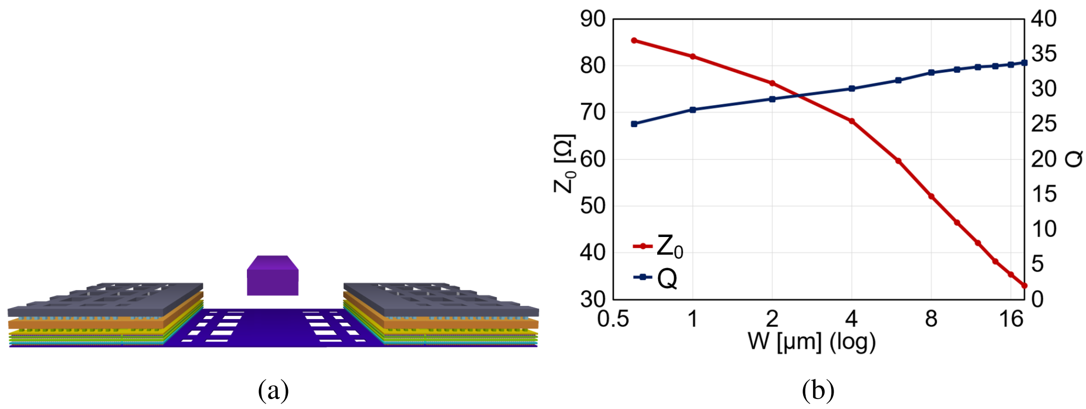
$$\begin{aligned} \gamma = \alpha + j\beta &= \sqrt{(R+j\omega L)(G+j\omega C)} \\ Z_0 &= \frac{R+j\omega L}{G+j\omega C} \end{aligned} \tag{3.22}$$

By solving (3.22):

$$\begin{aligned} R &= Re[\gamma \cdot Z_0] \\ L &= Im[\gamma \cdot Z_0]/\omega \\ G &= Re[\gamma/Z_0] \\ C &= Im[\gamma/Z_0] \cdot \omega \end{aligned} \tag{3.23}$$

The layout cross section of the TLINE is drawn in Fig. 3.8(a). The signal trace is realized in the topmost thick metal (M_8), the underneath ground plane in the first metal

(M_1) and the lateral shielding walls are made by stacking metals up to the seventh layer (M_7). The most important TLINE geometrical parameter is the width of the signal trace determining the characteristic impedance and loss. The plot in Fig. 3.8(b) shows Z_0 and Q ($\beta/2\alpha$), extracted from electromagnetic simulations for W in the range 1 μm to 18 μm. Z_0 spans from 83 Ω for the minimum W down to 33 Ω for W = 18 μm. The TLINE Q is from 25, for W = 1 μm to 35, for W = 18 μm.

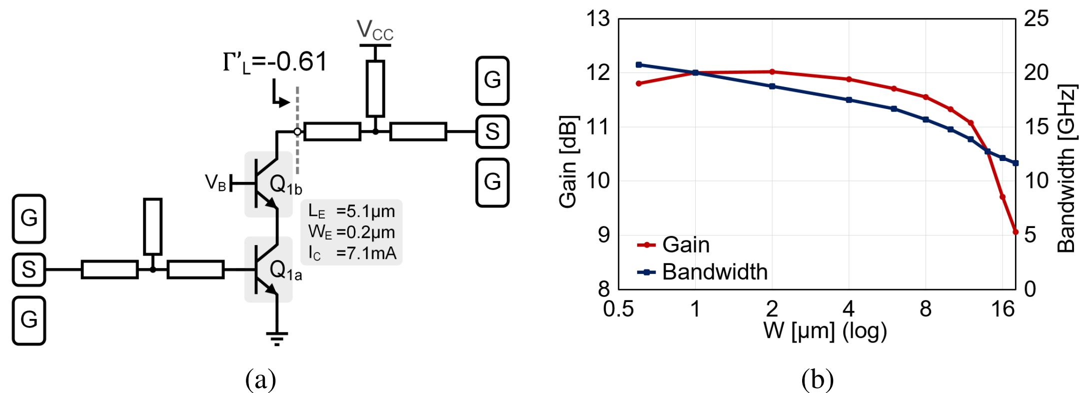


(a) (b)

Figure 3.8: (a) Cross section of the shielded microstrip TLINE, (b) characteristic impedance and quality factor vs the width of the signal trace.

The schematic of a single-stage cascode amplifier is drawn Fig. 3.9(a). The input network, not critical for amplifier performance, matches the impedance at the GSG pad to Z_{S-opt}, and it is realized with TLINE stubs of W=8 μm ($Z_0 = 50\Omega$). On the opposite, the output matching network influences significantly the gain and bandwidth. From the analysis in Sec. 3.3, high Q of the TLINE stubs is critical to avoid gain loss, suggesting selection of large TLINE W. But for maximum gain and bandwidth the network should be implemented with ideal inductors (i.e. reactances storing only magnetic energy). The condition may be approximated with TLINEs of high characteristic impedance ($Z_0 = \sqrt{L/C}$, being L and C the line inductance and capacitance for unit length) i.e. with small trace width, penalizing the TLINE Q. To gain a quantitative insight, different output matching networks are designed to achieve $\Gamma'_L = \Gamma'_{L-opt}$ given by (3.15), with TLINE stubs of different width. The simulated peak S_{21} at 150 GHz and the -3 dB bandwidth of the amplifier are shown in Fig. 3.9(b). The trend confirms the analysis in Sec. 3.3. First, increasing W rises the TLINE Q (see Fig. 3.8(b)) slightly increasing the amplifier peak gain. But increasing W decreases Z_0 of the TLINE, finally penalizing the amplifier gain due to the non-negligible electrical energy

stored in the matching network. Nonetheless, the gain variation is mild, roughly 1 dB from W=1 µm to W=12 µm. The -3 dB bandwidth monotonically decreases with W because the reduction of Z_0 rises the reactive energy stored in the network and hence the loaded network Q. In the final design, a trace width of 4 µm is selected, giving marginal bandwidth penalty but improving robustness against processing tolerances and electromigration. For W=4 µm, the Q of the TLINE is 30. Considering the nodal Q at the transistor output, $Q_0 = 20.8$, Γ'_{L-opt} given by (3.15) is -0.41 and the -3 dB bandwidth given by (3.3), neglecting the electrical energy in the network, is ~23 GHz. The final network is designed for $\Gamma'_L = -0.61$, slightly penalizing the gain for larger bandwidth.



(a) (b)

Figure 3.9: (a) Schematic of single-stage amplifier, (b) Peak gains at 150 GHz and bandwidths for different W values.

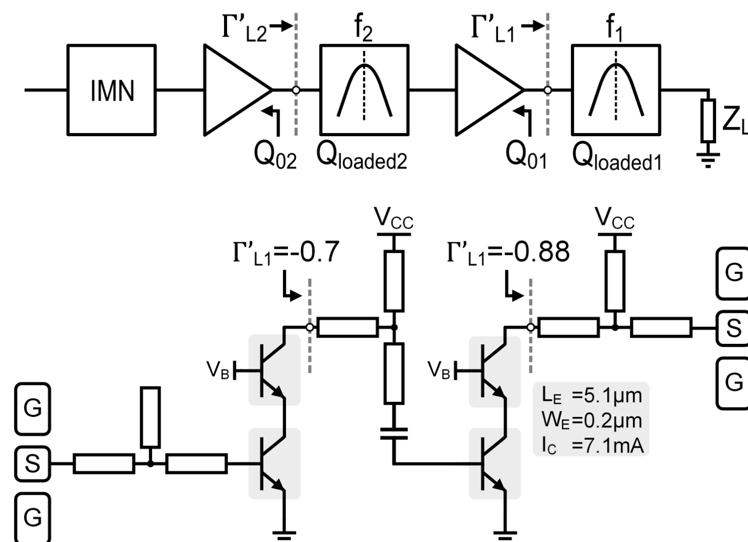


Figure 3.10: Schematic of 2-stage amplifier.

Fig. 3.10 shows the block diagram and circuit schematic of a two-stage amplifier. The input matching network is the same as in the single-stage design. Gain and bandwidth of the amplifier are primarily determined by the two output matching networks. As shown in Fig. 3.11(a), the two networks are centered at f_1, f_2 and designed with appropriate $Q_{loaded-1,2}$ to achieve flat, wide-band response.

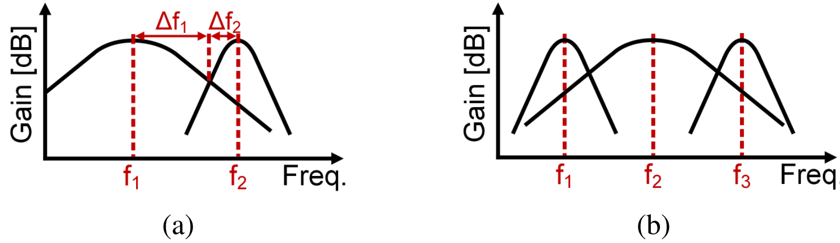


Figure 3.11: Peaking frequencies and relative positions for (a) 2-stage, (b) 3-stage amplifier.

Assuming the power gain of each stage $G_{1,2}$ follows a second-order transfer function:

$$G_{1,2}(f) = \frac{G_{1,2}}{\left[1 + 2 \cdot j \cdot Q_{loaded-1,2}\left(\frac{f - f_{1,2}}{f_{1,2}}\right)\right]^2} \tag{3.24}$$

(being $G_{1,2}$ the peak gain of each stage at its center frequency) the following condition has to be verified to have the same gain at f_1 and f_2 in the two-stage amplifier.

$$G_1(f_1) \cdot G_2(f_1) = G_1(f_2) \cdot G_2(f_2) \tag{3.25}$$

which, combined with (3.24) results into a simple relation between $f_{1,2}$ and $Q_{loaded-1,2}$:

$$\frac{Q_{loaded1}}{f_1} = \frac{Q_{loaded2}}{f_2} \tag{3.26}$$

In order to have an overall flat frequency response, without in-band ripple, the two matching networks are designed such that the two transfer functions in Fig. 3.11(a) intersect at the -3 dB point:

$$\begin{aligned} f_1 + \Delta f_1 &= f_2 - \Delta f_2 \\ f_1 + \frac{f_1}{2 \cdot Q_{loaded1}} &= f_2 - \frac{f_2}{2 \cdot Q_{loaded2}} \end{aligned} \tag{3.27}$$

Combining (3.26) in (3.27) we get the constrains on $f_{1,2}$ and $Q_{loaded-1,2}$ to be satisfied by the design of output matching networks in Fig. 3.10:

$$f_1 = f_2 \cdot \left(\frac{Q_{loaded2} - 1}{Q_{loaded2}}\right) \tag{3.28}$$

$$Q_{loaded1} = Q_{loaded2} - 1 \tag{3.29}$$

Using (3.28), (3.29) and the results of the analysis in Sec. 3.3, the design of the two-stage amplifier is as follows. First, the highest center frequency f_2 is arbitrarily selected, e.g. $f_2 = 155$ GHz. The nodal quality factor at the output of the cascode stage at frequency f_2 is $Q_{02} = 20.3$. With $Q_r = 30$, the reflection coefficient to maximize power gain, calculated with (3.15) is $\Gamma'_{L2} = \Gamma'_{L-opt} = -0.4$. The nodal quality factor of the load impedance at f_2 is $Q_{L2} = 0.63$, thus, through (3.18), $Q_{loaded-2} = 6.36$. Using now (3.28), (3.29), $f_1 = 130.6$ GHz and $Q_{loaded-1} = 5.36$. The nodal quality factor of the cascode output impedance at f_1 is $Q_{02} = 25.3$ and by using (3.18), the reflection coefficient to meet the required $Q_{loaded-1}$ is $\Gamma'_{L1} = -0.6$. With this design, the separation between f_2 and f_1 is only 24.4 GHz. To broaden the bandwidth and rise the amplifier GBW, Γ'_{L2} lower than Γ'_{L-opt} (expressed by (3.15)) can be selected. The two-stage amplifier is implemented with $f_2 = 162$ GHz and by selecting $\Gamma'_{L2} = -0.7$. Using (3.18), $Q_{loaded-2} = 3.36$ and with (3.28), (3.29) $f_1 = 113.8$ GHz, $Q_{loaded-1} = 2.36$. At 113.8 GHz, Q01 = 32.1 and QL1 = 0.5 which, inserted in (3.18), gives $\Gamma'_{L1} = -0.88$.

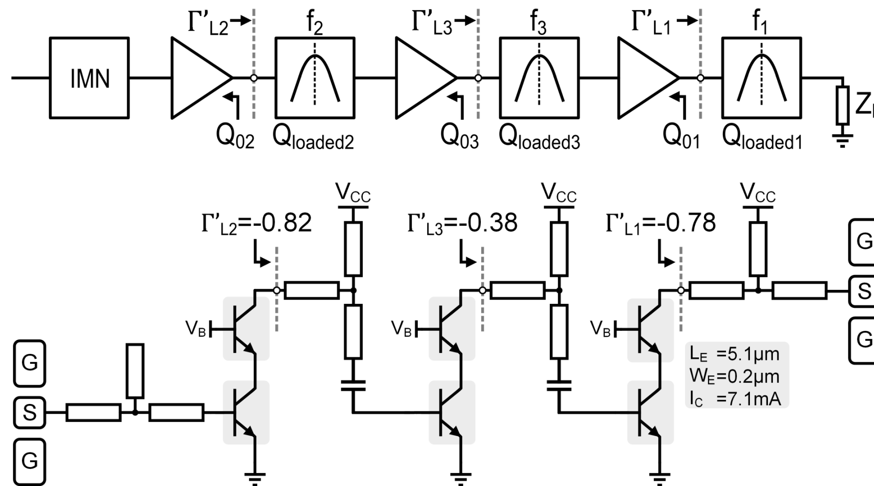


Figure 3.12: Schematic of 3-stage amplifier.

Fig. 3.12 shows the block diagram and circuit schematic of a three-stage amplifier. Still, gain and bandwidth performances are determined by the matching networks at the output of each stage. As shown in Fig. 3.11(b), the networks are stagger tuned with center frequencies f_1, f_2, f_3. With considerations similar to the previous case of two-cascaded band-pass networks, the constraints on center frequencies and

$Q_{\text{loaded}-1,2,3}$ to have flat response in the case of three stages are found:

$$f_2 = f_3 \frac{Q_{loaded-3} - 1}{Q_{loaded-3}} \tag{3.30}$$

$$Q_{loaded-2} = \frac{Q_{loaded-3} - 1}{2} \tag{3.31}$$

$$f_1 = f_3 \frac{Q_{loaded-3} - 2}{Q_{loaded-3}} \tag{3.32}$$

$$Q_{loaded-1} = Q_{loaded-3} - 2 \tag{3.33}$$

The highest center frequency f_3 is set to 167 GHz. Being $Q_{03} = 18.3$ and $Q_{L3} = 0.67$, using (3.15), $\Gamma'_{L3} = \Gamma'_{L-opt} = -0.38$. With (3.18), $Q_{\text{loaded}-3} = 6.09$ and by using (3.30), (3.31), $f_2 = 139.6$ GHz and $Q_{\text{loaded}-2} = 2.54$. With the estimated $Q_{02} = 22.6$ and $Q_{L2} = 0.59$, $\Gamma'_{L2} = -0.82$ is found using (3.18). The same procedure is adopted find finding the parameters of the matching network tuned at f_1: using (3.32), (3.33), $f_1 = 112.1$ GHz and $Q_{\text{loaded}-1} = 4.09$. With the estimated $Q_{01} = 33.1$ and $Q_{L1} = 0.49$, $\Gamma'_{L1} = -0.78$ is calculated with (3.18).

The ordering of the stages in a chain of stagger-tuned amplifiers influences the shape of the noise figure [44]. In this design, the ordering of the stages depicted in Fig. 3.12, is selected to have a pretty flat noise figure over frequency: the first stage in the chain has the output matching network tuned at center frequency, f_2, the second stage is tuned at the highest frequency, f_3, while the last stage is tuned at the lowest frequency f_1.

3.5 Experimental results

The amplifiers were fabricated in STMicroelectronics' 55nm SiGe BiCMOS technology [53], and the chip microphotographs are presented in Fig. 3.13. Small-signal measurements have been performed using Agilent PNA-E8361C vector network analyzer (VNA) with VDI WR-6.5 D-Band Extenders, after thru-reflect-line (TRL) probe tip calibration. The measured and simulated S-parameters and Rollet stability factors for the three amplifiers are reported in Fig. 3.14 The one-stage amplifier (top plot) draws ~6.3 mA current from 1.9 V supply and reaches 10.8 dB peak gain with 33.6 GHz -3 dB bandwidth. The two-stage amplifier (middle plot) achieves 20.6 dB gain with 65.8 GHz bandwidth with ~13 mA current consumption.

The gain and bandwidth of the three-stage amplifier (bottom plot) are 28.6 dB gain and 64.3 GHz with ∼19 mA current consumption. All three amplifiers are unconditionally stable over D-band.

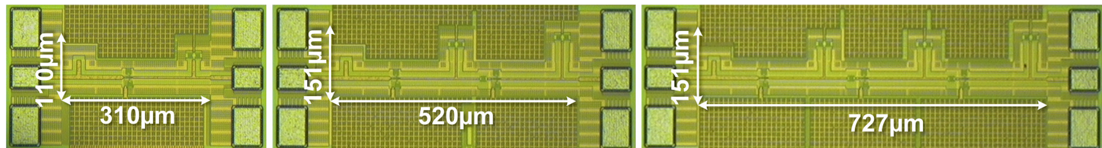


Figure 3.13: Chip microphotographs of 1- (left), 2- (center) and 3-stage (right) amplifiers.

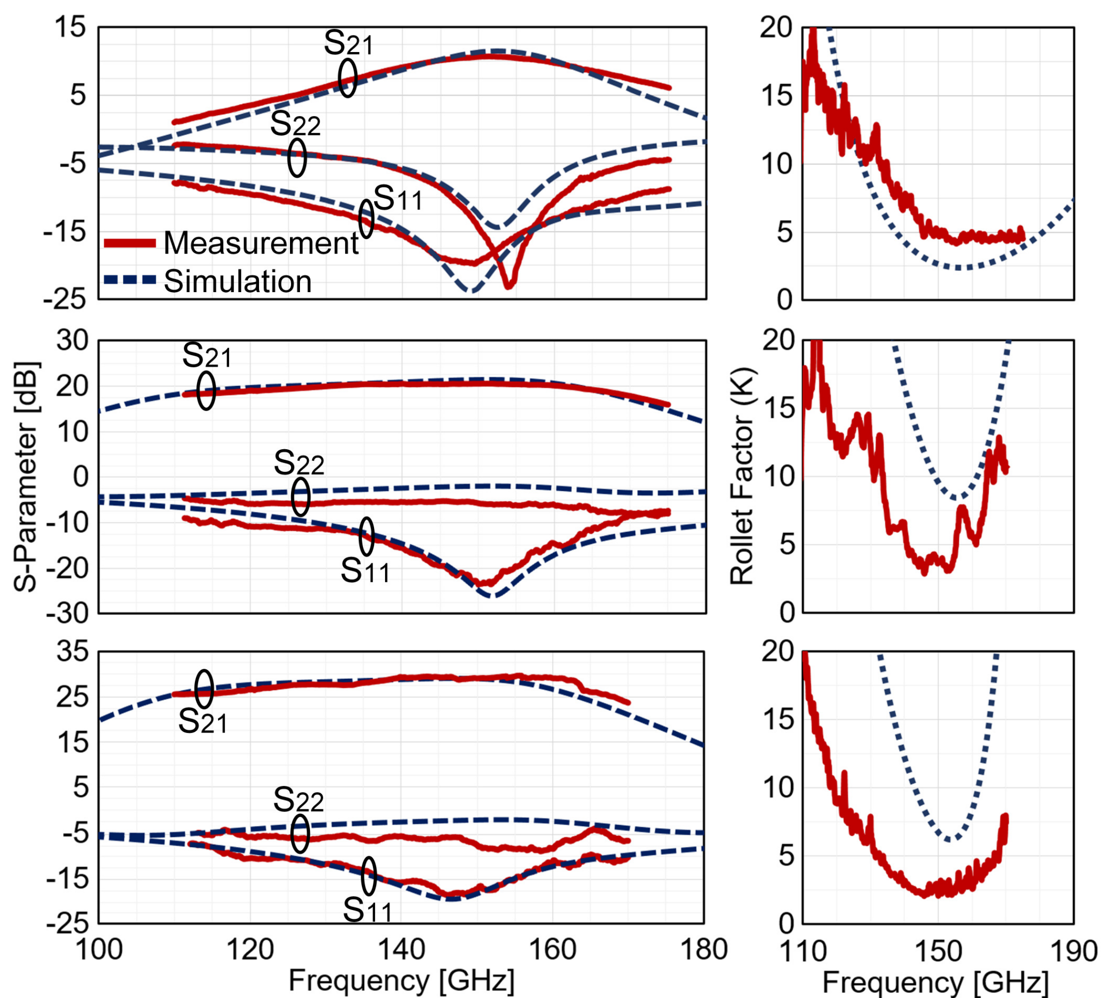


Figure 3.14: S-Parameter results for 1- (top), 2- (center) and 3-stage (bottom) amplifiers.

Measurements on the noise figure (NF) was not possible due to the lack of instrumentation. From simulations, the NF of one-stage amplifier within it's -3 dB bandwidth is from 8.6 dB to 9.6 dB. The NF of the two-stage amplifier varies from

8.1 dB to 10.2 dB while in the three-stage design, the NF is in 8.8 dB at low frequency and rises to 10.5 dB at the highest frequency.

3.6 Conclusion

The measurement results are summarized and compared with previously reported SiGe amplifiers operating above 100 GHz in Table 3.1. The third raw in the Table highlight the number of stages for each design. The presented two-stage amplifier covers more than 60 GHz bandwidth with 705 GHz GBW, rougly twice than the two-stage amplifier in [42]. The amplifier in [37] reaches 1.2 THz GBW and it is classified as two-stage, but the first stage employs four stacked transistors requiring 4.8 V supply voltage. The presented three-stage amplifier reaches over 1.7 THz GBW, a performance which is exceeded only by the amplifier in [35] with four stages. The Figure-of-Merit (FoM) from [29], with expression reported below the Table, is used to normalize the gain (G) center frequency (f_0) and the -3 dB bandwidth (BW) to the number of stages (n) and the technology f_{max}. The presented two- and three-stage amplifiers demonstrate the highest FoM, ~1.5 times than [37], which needs 4.8 V supply, and at least 3 times higher compared to the other works.

Table 3.1: Comparison with SiGe amplifiers above 100 GHz

	This Work			**[34]**	**[35]**	**[36]**	**[37]**	**[38]**	**[40]**	**[42]**
f_t/f_{max}	320/370			250/370	300/500	300/500	300/500	300/350	180/220	300/500
# Stages	1	2	3	3	4	4	2^S	4	4	2
Gain [dB]	10.8	20.6	28.6	32.8	32.6	25.3	26	30	26	27.5
Center Freq. [GHz]	150	144	140	140	140	134	150	136	130	126
-3 dB Bandwidth [GHz]	33.6	65.8	64.3	23.2	52	44	60	28	13	16
Gain-Bandwidth Product [GHz]	116.5	705.1	1730.7	1012.7	2218.2	809.9	1197.2	885.4	259.4	379.4
PDC [mW]	12	24	36	39.6	28	30	70	45	57	12
Core Area* [mm^2]	0.035	0.078	0.110	0.075	0.600	0.282	0.150	0.116	-	0.214
FoM	0.126	**0.227**	**0.248**	0.084	0.074	0.049	0.151^S	0.074	0.074	0.039

*: Estimated from chip photographs excluding PADs.

FoM=$\sqrt[n]{G_T}(f/f_{max})^2(f_{3dB}/f_c)$

^{S}: Uses 4 stacked transistor in 1st stage with 4.8 V supply.

Chapter 4

Design of D-Band Power Amplifiers with Enhanced PAE

In this chapter single-ended and differential D-Band power amplifiers (PAs) are presented. As signal amplifiers, presented PAs were fabricated in STMicroelectronics' 55 nm BiCMOS technology [53]. The proposed PAs make use of current clamping and exploit the remarkable features of common-base stages for rising the power efficiency.

4.1 Introduction

D-band PAs in silicon (both SiGe HBTs and CMOS) demonstrated a saturated output power (P_{SAT})$\geq$14 dBm [54–59]. PAs reported so far are implemented by cascading multiple Class-A common-emitter (source) or cascode stages. Due to the soft saturation, the output power at 1 dB gain compression (P_{1dB}) is remarkably lower than P_{SAT}, where the efficiency peaks, and PAE drops very sharply when $P_{out}\geq P_{1dB}$ [54–59]. Considering the peak-to-average power ratio of typical QAM modulations, PAs are operated at 5-8 dB back-off from P_{1dB} where the PAE of reported PAs is 2% or less [54–59]. The maximum available gain (MAG) of transistors in D-band is relatively low, only of few dBs. This issue limits the design options and techniques to improve PAE at power back-off, i.e., Doherty PAs or even simple Class-AB biasing are not viable.

This work proposes D-band PAs leveraging the remarkable features of common-base (CB) stages to enhance PAE. Compared to common-emitter (CE), the CB enjoys the following advantages: (1) extended breakdown, thus higher usable supply voltage, (2) linearity enhanced by the emitter degeneration impedance, leading to a sharp compression with P_{1dB} close to P_{SAT}, (3) supply current adapted to the signal amplitude by current-clamping (will be detailed in next section), with transistors nearly in Class-A, thus raising the PAE in back-off with negligible gain penalty. To the Author's

best knowledge this is the first time the advantages of CB stages are fully exploited for D-band PAs.

4.2 Current Clamping

The current clamping is the dual of well-known voltage clamping [60]. The voltage clamping circuit, depicted in Fig. 4.1(a), adds DC voltage component to input signal and clamps waveform to the reference voltage (ground). In the current-mode version (Fig. 4.1(b)) series capacitor is replaced with shunt inductor, and the diode current replaces the voltage across the diode.

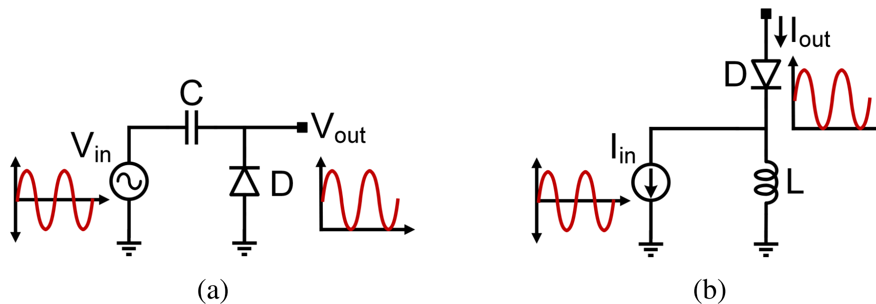


Figure 4.1: (a) Voltage-mode, (b) current-mode diode clamping circuits.

The current-mode diode clamping can be exploited in CB stage [61]. The diode and inductor in Fig. 4.1(b) are implemented with the base-emitter junction of CB transistor and emitter degeneration inductor. Neglecting parasitic capacitance C_{BE}, if the transistor is biased to have zero quiescent current, the transistor is off first half negative cycle of the input current ($I_{pk} \cdot \sin(\omega t)$), and the inductor L charges up to I_{pk}. The transistor turns on with emitter current $I_E = I_{pk} + I_{pk} \cdot \sin(\omega t)$.

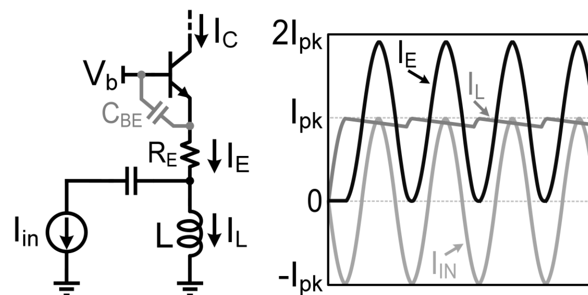


Figure 4.2: The implementation of current-mode clamping on CB transistor, and current waveforms.

Assuming the inductor L is infinite, the transistor never turns off, operates in class-A. For a large but finite value of L, non-zero emitter resistance partially discharges the inductor and the transistor turns off very short period of time in each cycle. This permits the inductor to be recharged and I_L tracks the I_{pk}. As a result, the average collector current of the transistor follows the envelope of the input signal current, similar to common-emitter with class-B biasing.

The effect of C_{BE} comes forward at high-frequencies. The C_{BE} absorbs the part of the input signal current and slows down the inductor charging during the off-state of the transistor. The charging speed and the ripple magnitude changes depending on the value of inductor. In the presence of C_{BE} the value of L doesn't change the average inductor current but sets the DC current slightly lower than I_{pk}. This infers that transistor operates more in class-AB, resulting a slight improvement of the collector efficiency.

4.3 Circuit Design

The schematic of the single-ended PA, comprising four stages, is drawn in Fig. 4.3. The transistor in the output stage, Q_4, is composed of 2 parallel HBTs each with emitter area of $A_E = 6\,\mu m^2$. Considering the breakdown voltage $BV_{CB0} = 5$ V, a supply voltage $V_{CC} = 2.2$ V is selected.

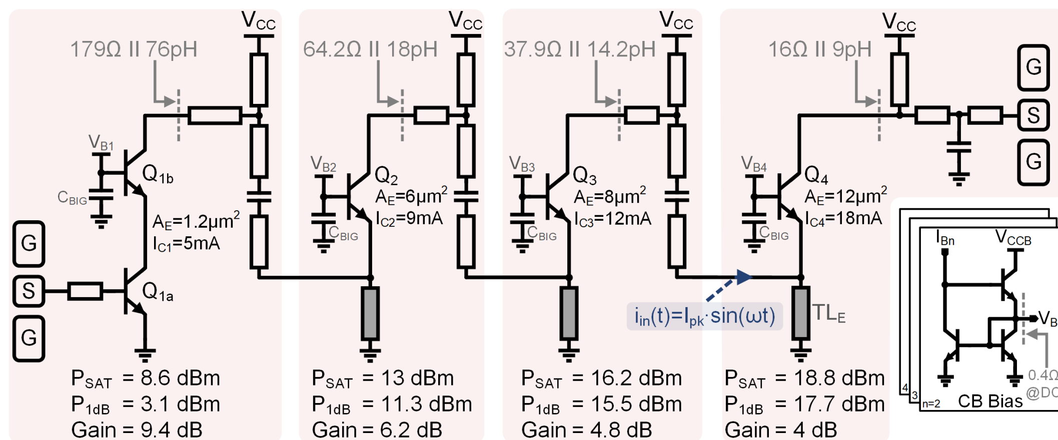
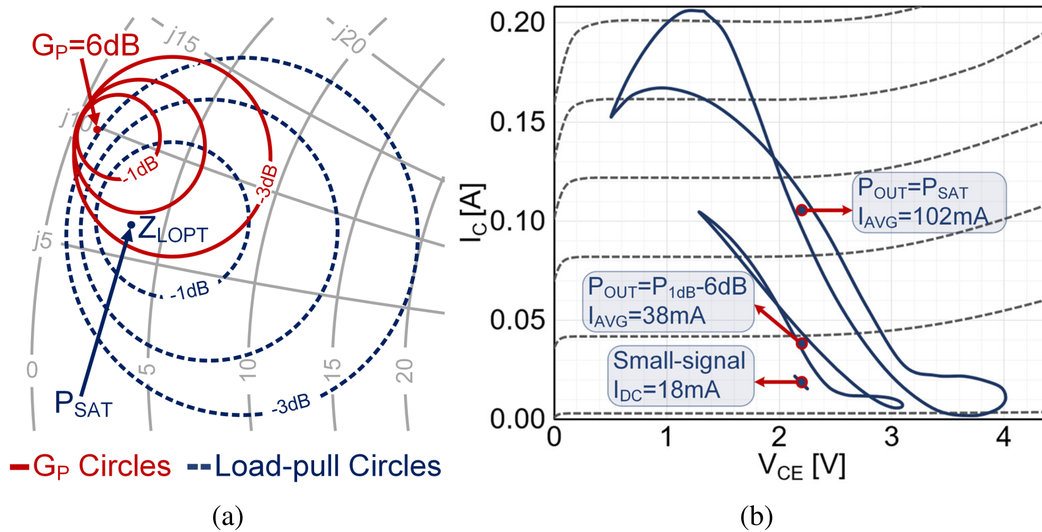


Figure 4.3: Schematic of the single-ended PA.

From load-pull simulations, drawn in Fig. 4.4, the load impedance for maximum output power is $Z_{L-opt} = 3.51 + j \cdot 6.62$ ($16\,\Omega \parallel 9$ pH) and, including the loss of he output

matching network, the device delivers $P_{1dB} = 17.7$ dBm, very close to $P_{SAT} = 18.8$ dBm. If a cascode configuration is formed with the same transistor under the same supply, $P_{SAT} = 15.2$ dBm with a substantially lower $P_{1dB} = 11.7$ dBm. Still, with the transistor in CE configuration the supply voltage must be reduced (being $BV_{CE0} = 1.5$ V) leading to $P_{1dB} = 8.9$ dBm only.



(a) (b)

Figure 4.4: (a) G_P and load-pull circles, (b) dynamic load lines for the transistor in the output stage.

Notice that from the DC viewpoint Q_4 is in CE configuration. To withstand 2.2 V supply the base voltage is set by a Wilson current mirror (drawn in Fig. 4.3) which shows a very low impedance ($< 1\Omega$). In this way impact-ionization generated holes by the collector DC voltage can flow out of the base of Q_4, rising the breakdown sufficiently above BV_{CE0} [62].

To improve the power efficiency, the quiescent current is set low, $I_{Q4} = 18$ mA, and current clamping is leveraged to adapt the supply current to the signal amplitude. If the current flowing into the emitter of Q_4, $i_{in}(t) = I_{pk}\sin(\omega t)$, exceeds I_{Q4} the BE junction turns off for a small fraction of the period and $i_{in}(t)$ charges the transmission line stub from the emitter of Q_4 to ground (TL_E), which works as an inductor. Q_4 then turns on with an average current raised roughly to I_{pk}. The effectiveness of supply current modulation performed by Q_4 is evidenced by the dynamic load-lines plotted in Fig. 4.4(b) on top of the device I-V curves. At small P_{out} the collector current of Q_4 swings around the quiescent point. But when P_{out} rises, the average current increases

and the load-line is shifted upward. Looking at the load-pull contours in Fig. 4.4(a) the selected Z_{L-opt} sacrifices 2 dB of power gain (G_P). Adding the losses of the matching network (∼1 dB) and GSG pad (∼0.5 dB), the output stage displays $G_P = 4$ dB only (it is worth noticing that the same device in CE features $G_P = 2.5$ dB, lower than CB [63]). The low G_P of the last PA stage makes the preceding stages critical for the overall performances. They have to rise gain while delivering enough power to push the last stage into compression without penalizing P_{1dB} of the complete amplifier. To meet this target CB transistors (Q_2 and Q_3 in Fig. 4.3) are still selected for the two middle stages, delivering high power with a sharp compression and allowing to exploit current clamping for efficiency improvement. The average current rising proportionally to the signal leads also to a mild (0.5 dB) gain expansion in each stage, useful to flatten the overall gain profile and maintain P_{1dB} close to P_{SAT}. Device sizes are scaled down at constant current density and the matching networks are designed favoring gradually power gain to the peak power. An input stage is finally added to rise the total power gain above 20 dB. The cascode configuration, featuring high G_P, is selected ($Q_{1a} - Q_{1b}$ in Fig. 4.3) with transistors biased in Class-A at ∼5 mA constant current.

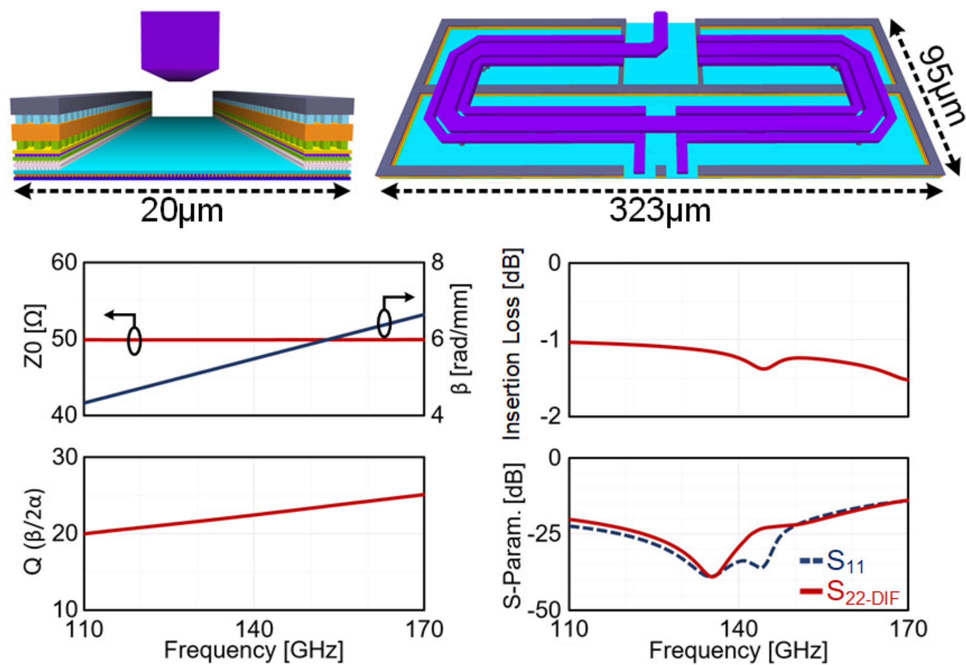


Figure 4.5: Characteristics of T-Line and balun.

Matching networks are realized with transmission lines (Tlines) and MOM capacitors. The cross section and the simulated performance of Tlines, customized for small

footprint (20 µmwidth) and low loss (Q≈23), are reported in Fig. 4.5. A differential PA has been also implemented, by using two instances of the single-ended design with Marchand baluns (shown in Fig. 4.5) introducing ∼1.1 dB simulated insertion loss.

4.4 Experimental Results

The single-ended and differential amplifiers were fabricated in STMicroelectronics' 55 nm SiGe technology with a 0.18 mm^2 and 0.26 mm^2 silicon area respectively. The chip microphotographs of designed PAs are shown in Fig. 4.6.

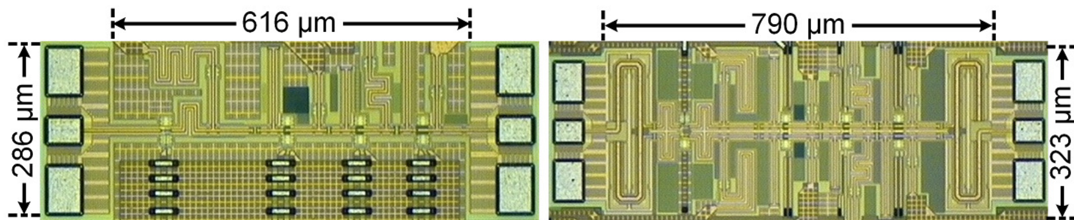


Figure 4.6: Chip microphotographs of the single-ended (left) and differential (right) PAs.

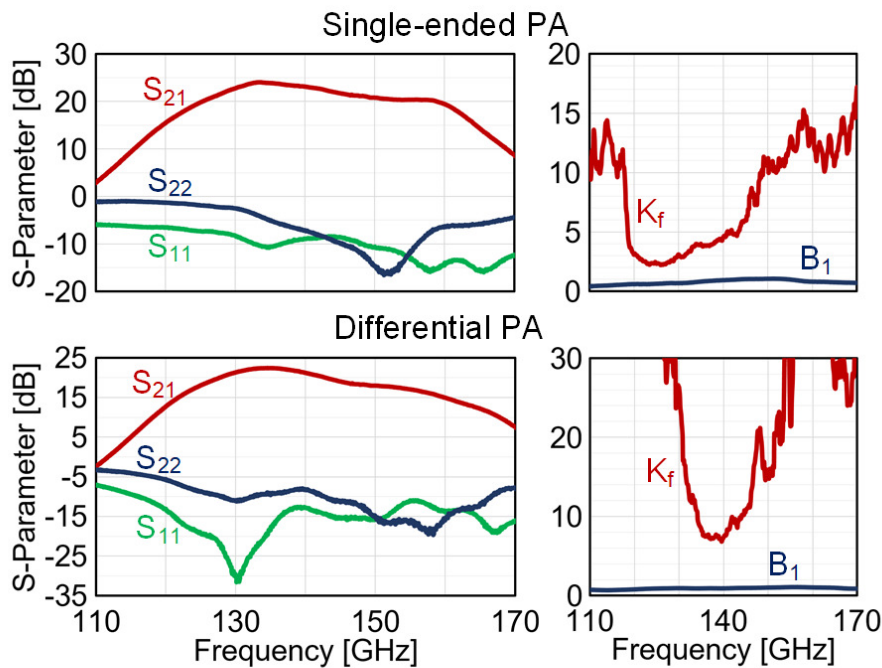


Figure 4.7: Measured S-parameters and stability-factors for single-ended and differential PAs.

The small-signal measurement was performed using VDI WR-6.5 D-Band Extenders with Agilent PNA-E8361C vector network analyzer (VNA) and N5260A Millimeter

Head Controller. The thru-reflect-line (TRL) probe tip calibration was applied with Cascade Standard Substrate 138-356. As depicted in Fig. 4.7, the PAs are unconditionally stable. The single-ended design reaches $S_{21} > 20$ dB from 125 GHz to 159 GHz with $S_{21-max} = 24$ dB at 133 GHz. The differential PA shows $S_{21} > 18$ dB from 125 GHz to 150 GHz with $S_{21-max} = 22.4$ dB at 135 GHz.

The large-signal measurement setup, comprising two Agilent E8257D signal source, VDI WR-6.5 D-Band Extender, MI-WAVE 115D Isolators, Anritsu ML2496A Power Meter, Elva D-Band Power Meter, is depicted in Fig. 4.8. Applied CW signal goes through x12 frequency multiplier and variable attenuator. Fraction of input signal is coupled and after down-conversion is monitored on power meter (P_{IN} monitor). The output signal goes through isolator and the power is measured by D-Band power meter (P_{OUT}).

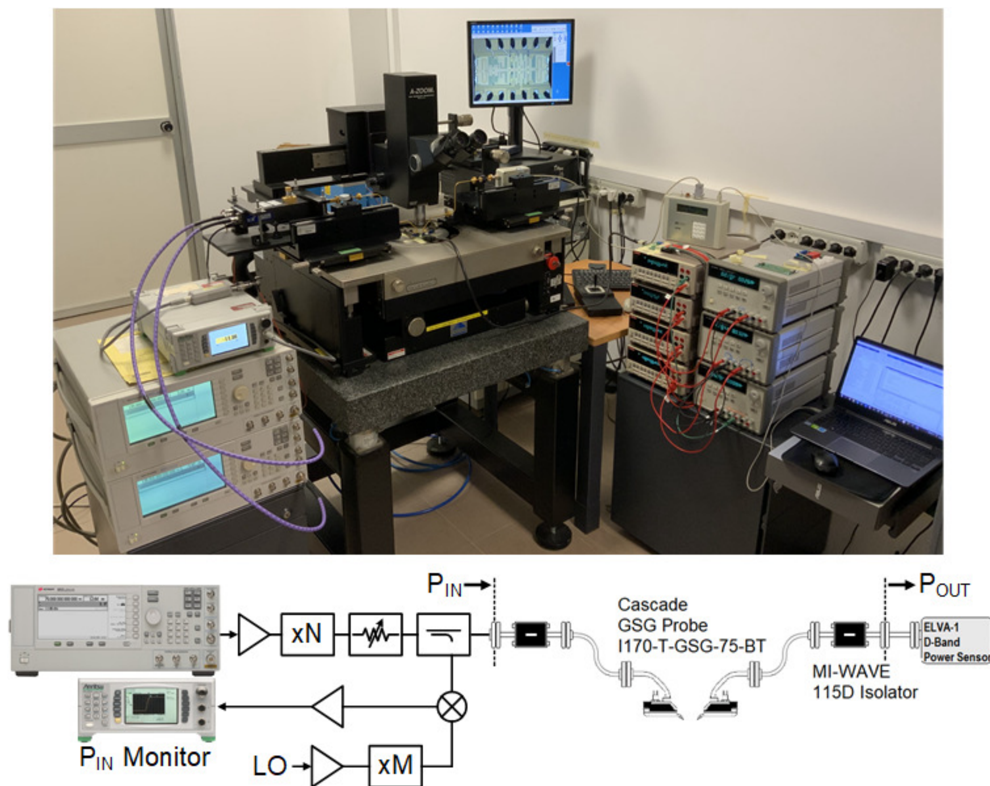


Figure 4.8: Large-signal measurement setup

The large signal measurement results are reported in Fig. 4.9. The single-ended PA displays $P_{SAT} = 17.6$ dBm and $P_{1dB} = 16.8$ dBm at 135 GHz. The PAE at P_{1dB} is 17.1 % and still 8.5 % at $P_{1dB-6dB}$. At 135 GHz the differential PA exhibits $P_{SAT} = 19.3$ dBm

and $P_{1dB} = 18.5$ dBm. The PAE at P_{1dB} and $P_{1dB-6dB}$ is 12.6 % and 6.6 %. The bottom plots report P_{out} and PAE of the amplifiers over frequency. As depicted in the bottom-left plot, from 125 GHz to 145 GHz single-ended PA performs $P_{1dB} \geq 15$ dBm. The PAE at P_{1dB} is $\geq 11\%$ and $> 6\%$ at 6 dB back-off. From 125 GHz to 140 GHz, the differential PA shows $P_{1dB} > 17$ dBm and the PAE at P_{1dB} is $\geq 9\%$ and $> 5\%$ at 6 dB back-off.

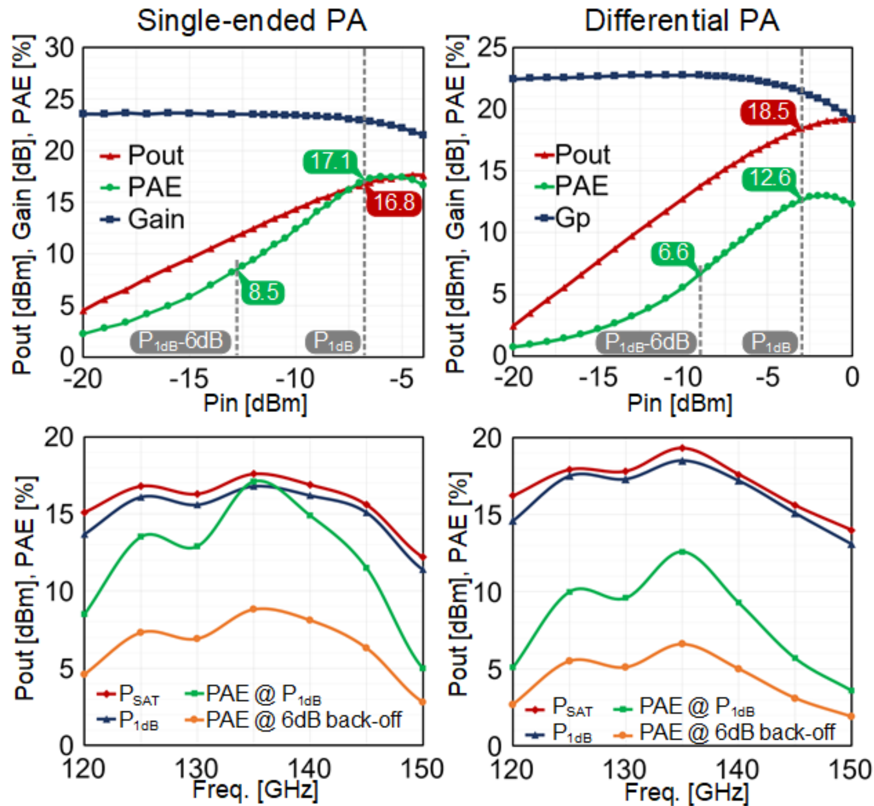


Figure 4.9: Measured large signal performance.

As shown in Fig. 4.10, the measured DC current drawn by CB stages in the single-ended PA rises with P_{out} up to 5 times of the quiescent value thanks to current-clamping. The total DC current at P_{1dB} is $\sim$130 mA, and it is nearly one-half at $P_{1dB-6dB}$, leading to a Class-B like back-off PAE profile.

The single ended PA driven at P_{1dB} has been tested with 16-hour continuous operation showing ± 0.15 dB variation around P_{out} of 16.8 dBm. The result of measurement is plotted in Fig. 4.11.

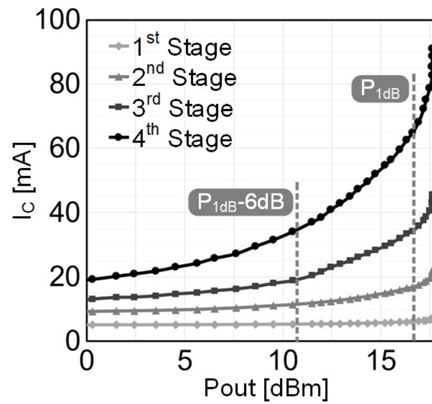


Figure 4.10: The DC current of the different stages in single-ended PA.

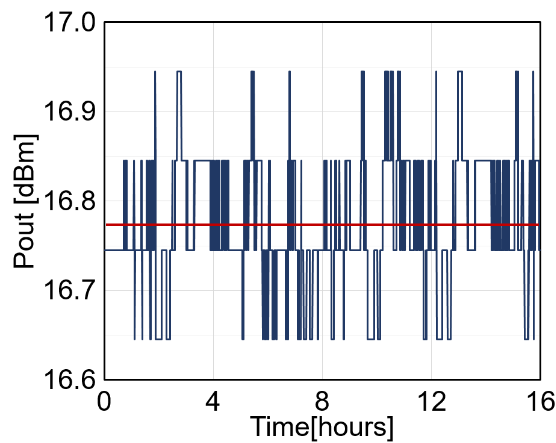


Figure 4.11: Reliability test for single-ended PA.

4.5 Conclusion

In this chapter D-band power amplifiers in 55 nm SiGe BiCMOS technology have been presented. The PAs exploit the remarkable features of common-base stages to enhance power-added-efficiency in the linear PA operating region. A single-ended PA proves P_{1dB} =16.8 dBm with P_{SAT} = 17.6 dBm at 135 GHz. The PAE at P_{1dB} and at $P_{1dB-6dB}$ are 17.1 % and 8.5 % respectively. With a differential PA the linear output power is increased to P_{1dB} =18.5 dBm with P_{SAT} = 19.3 dBm at 135 GHz. The PAE at P_{1dB} and at $P_{1dB-6dB}$ are 12.6 % and 6.7 % respectively.

The best measured performances are compared with silicon PAs at similar frequency delivering P_{SAT} >14 dBm in Table 1. P_{1dB} is aligned with [54] but from 3 to 6 dB higher than [55–59]. The efficiency at P_{1dB} and in power back-off is improved by 3× or more over state of the art. The PAs performances are compared also with the Figure of Merit

(FoM) introduced in [64] (with expression reported as foot note in Table I). The FoM, calculated at P_{1dB}, confirms the remarkable improvement against state of the art.

Table 4.1: Performance summary and comparison to prior works.

	This Work		[54]	[55]	[56]	[57]	[58]	[59]	[61]
	S.E.	DIFF.							
Technology	55nm SiGe		90nm SiGe	130nm SiGe	120nm SiGe	130nm SiGe	16nm FinFET	40nm CMOS	55nm SiGe
f_t/f_{max}	320/370		310/350	250/370	250/330	250/300	-	-	320/370
Supply [V]	2.2		1.6	1.5, 3.3	3.5	4	1	1	1.8, 2.3
Freq. [V]	135		116	130	120	160	135	140	80
Gain [dB]	24	22.4	15	28.5	32	27	20.5	20.3	18.5
$S_{21}-BW$ [GHz]	34	25	15	16	17.2	50	22	17	15
P_{SAT} [dBm]	17.6	19.3	20.8	15*	17.8	14	15	14.8	21.5
P_{1dB} [dBm]	16.8	18.5	17	12.6*	13.5	11.8	9.2	10.7	20.5
PAE_{MAX} [%]	17.5	13	7.6	8.2*	4.3	5.7	12.8	8.9	22
PAE@P_{1dB} [%]	17.1	12.6	4	5.8*	-	2.5	4.5*	4*	20
PAE @6dB backoff [%]	8.5	6.6	1.2*	2.2*	-	<1*	1.2*	<1*	7.2
FoM	37.5	28.3	0.9	12.6	-	4.9	0.8	1.0	10.2

*: Estimated from measurement plots. $FoM = 10^{-3} \cdot P_{out} \cdot G \cdot PAE \cdot f^2$

Conclusion

In the scope of the European TARANTO funded program, this PhD thesis has followed three different paths to address three different issues related to design of amplifiers in D-band. As a total, 9 D-band amplifiers were presented to solve the addressed issues.

In the first part of the thesis, design strategies for compact amplifier implementation was studied. First 4 amplifiers use lumped elements in matching networks. In the first two single ended designs, to correctly account for the effects of a non-ideal ground plane, i.e., reactances in current return paths, and coupling of inductors with nearby layout structures, a shielded 2-port, 4-terminal simulation strategy for inductors was proposed and validated by measurements. The approach allowed very accurate design of compact amplifiers in D-band. The 1-stage design proved 11.8 dB gain at 152 GHz and 17.9 GHz bandwidth in 0.031 mm^2. With the 2-stage amplifier, featuring 20.1 dB gain at 150 GHz with 24.5 GHz bandwidth in 0.058 mm^2, from 2$\times$ to 5.7$\times$ area reduction was demonstrated against similar SiGe amplifiers in the same frequency band. In the next two designs, the differential topology was developed for robustness against parasitic effects of the non-ideal ground, a key issue with lumped components at high frequency. The 1-stage amplifier reached 8 dB gain at 156 GHz and 17.8 GHz bandwidth in 0.026 mm^2 silicon area. The 2-stage amplifier displayed 17.4 dB gain at 157 GHz with 42.7 GHz bandwidth in 0.048 mm^2. Compared to previously reported SiGe amplifiers in similar frequency range, more than 2$\times$ core area reduction was demonstrated at comparable gain-bandwidth product. The results were published in [12] and [13].

The second section of the thesis analysed wideband amplifiers for D-band communication. A simple, closed-form equations for gain and bandwidth as a function of the load reflection coefficient were derived and a design strategy was proposed. Leveraging the results of the analysis, a single-stage and multi stage stagger-tuned amplifiers were implemented in a SiGe BiCMOS technology. Two- and three-stage amplifiers demonstrated more than 60 GHz bandwidth with 20 dB

and 28 dB gain respectively, corresponding to 700 GHz and 1.7 THz gain-bandwidth product. Normalizing gain and bandwidth to the number of stages and technology f_{max}, the resulting Figure of Merit was remarkably higher than previously reported silicon amplifiers in the same band. The results were submitted to a journal publication entitled "Analysis and Design of D-Band Cascode SiGe BiCMOS Amplifiers with Gain-Bandwidth Product Enhanced by Load Reflection".

The last section of the thesis studied the problem of power added efficiency in D-band power amplifiers. The power amplifiers (PAs) were designed in a single-ended and differential fashion. The PAs exploited the remarkable features of common-base stages to enhance power-added-efficiency in the linear PA operating region. A single-ended PA proved P_{1dB} =16.8 dBm with P_{SAT} = 17.6 dBm at 135 GHz. The PAE at P_{1dB} and at $P_{1dB-6dB}$ were 17.1 % and 8.5 % respectively. With a differential PA the linear output power was increased to P_{1dB} =18.5 dBm with P_{SAT} = 19.3 dBm at 135 GHz. The PAE at P_{1dB} and at $P_{1dB-6dB}$ were 12.6 % and 6.7 % respectively, an improvement of at least 3$\times$ against state of the art. The results were submitted to a letter publication titled "D-band SiGe BiCMOS Power Amplifier with 16.8 dBm P_{1dB} and 17.1 % PAE Enhanced by Current-Clamping in Multiple Common-Base Stages".

The results of an activity carried out in the initial part of the PhD program related to the design of a serial-link PAM-4 receiver in FinFet technology, is added as an appendix. The results were published on a journal paper titled "A 112 Gb/s PAM-4 RX Front-End with Unclocked Decision Feedback Equalizer" [14].

Appendix

A.1 - A 112 Gb/s PAM-4 RX Front-End with Unclocked DFE

The implementation of an unclocked DFE (UC-DFE) architecture for high-speed PAM-4 signals is investigated in this work. Instead of clocked slicers and flip-flops, data-decision and feedback delay control are performed by saturated analog delay chains. As a result, the UC-DFE, previously exploited for NRZ signals, saves power consumption and silicon area while the simple implementation allows operation at high data-rate. A receiver front-end comprising a linear equalizer and the proposed 2-tap UC-DFE scheme is designed in 7 nm FinFET technology.

1.1 Introduction

With an increasing number of internet users and the proliferation of new multimedia applications every day, the data traffic inevitably expands very fast. Furthermore, as CMOS technologies are scaled-down, the density of digital computing rises, and higher speed of interconnections is required to fully exploit the available computing power. Therefore, high-speed interfaces over optical fibers or PCB channels for system to system, rack to rack, or chip to chip communications are needed. To satisfy this demand, new standards targeting up to 112 Gb/s, such as OIF CEI-112G-VSR/XSR/USR with multilevel (PAM-4) signaling are under investigation.

The channel loss causes inter-symbol interference (ISI) which impairs the bit error rate (BER), requiring accurate and flexible equalizers in the transceivers. ADC-based receivers leverage the powerful digital signal processing for equalization and detection and demonstrated operation at 112 Gb/s over a channel with high loss (>20 dB) [65–68]. But for very-short-reach (VSR) links, i.e., 10-15 dB loss chip-to-module connections, an analog design approach saves power. In analog wireline receivers, a continuous-time linear equalizer (CTLE) mimics the inverse of the channel response. However, excessive high-frequency peaking must be avoided to limit noise and crosstalk amplification. Therefore, the CTLE is commonly followed by a decision feedback equalizer (DFE) to remove the residual post cursors without further noise and cross-talk amplification. But the implementation of high-speed DFE is challenging,

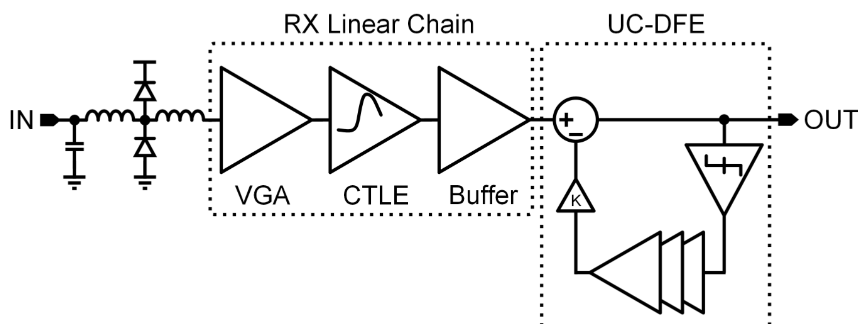


Figure 5.1: Proposed Analog Front-end Architecture.

also with advanced CMOS technology nodes, because of the critical timing constraints to be satisfied, exacerbated by the hardware complexity with PAM-4 signaling. The loop unrolling and the half- or quarter-rate DFE architectures have been proposed up to 56 Gb/s [69, 70]. This paper investigates, for the first time to Authors knowledge, the feasibility of an unclocked DFE (UC-DFE) architecture for PAM-4. Removing the clocking circuits saves power and silicon area while the simplest implementation allows a significant increase in data rate. The UC-DFE concept was initially proposed in [71, 72] and subsequently exploited at 12 Gb/s [73] and 19 Gb/s [74] for NRZ signals. In this work, an UC-DFE architecture for PAM-4 is developed. The receiver front-end in Fig. 5.1, designed in 7 nm FinFet technology, comprises a multi-stage CTLE and a 2-taps UC-DFE. It requires 53 mW maximum power and, from post-layout simulations, it supports 112 Gb/s PAM-4 over 18 dB loss channel and 56 Gb/s NRZ over 24 dB loss channel. The manuscript is organized as follows: Section 1.2 presents the linear chain of the receiver front-end of Fig. 5.1, with emphasis on the CTLE. Section 1.3 proposes the PAM-4 UC-DFE architecture and describes the most relevant circuit design aspects. Simulation results are shown in Section 1.4 while conclusions are drawn in Section 1.5.

1.2 RX Linear Chain and CTLE

The linear RX chain is shown in Fig. 5.1 and it is designed to operate with an input signal amplitude in the range of 500-800 mV_{PP} [75]. An input T-coil network absorbs pad and ESD parasitic capacitances while ensuring wideband input impedance matching. After the passive network, a differential resistor sets the 100 Ω termination

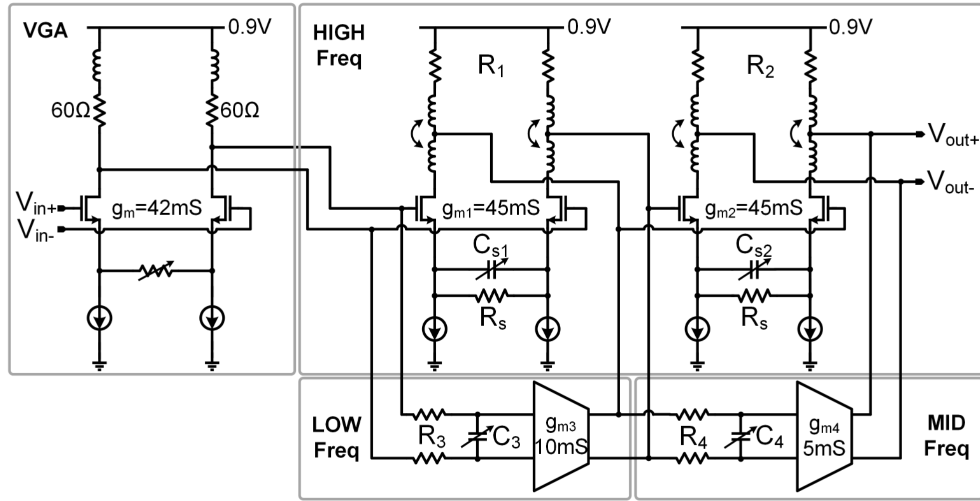


Figure 5.2: Schematic of VGA and Continuous Time Linear Equalizer.

and a VGA (shown in Fig. 5.2) provides gain programmable from -2 dB to +2 dB. The VGA draws 8 mA from 0.9 V. The CTLE (still shown in Fig. 5.2) is devised such that its transfer function can be optimally adapted at low-, mid-, and high- frequencies for accurate channel inversion. A similar concept and a possible adaptation flow is described in [69]. The CTLE draws 16 mA from 0.9 V supply and it is realized by cascading two resistive and capacitive degenerated differential pairs (g_{m1}, g_{m2}) that provide high-frequency peaking. The circuit bandwidth is limited significantly by the transistor fingers and routing parasitics and T-coil peaking networks are exploited for extending the bandwidth beyond Nyquist frequency. Two feed-forward transconductors (g_{m3}, g_{m4}) shunt the main paths for fine-tuning of the CTLE transfer function at low- and mid-frequencies.

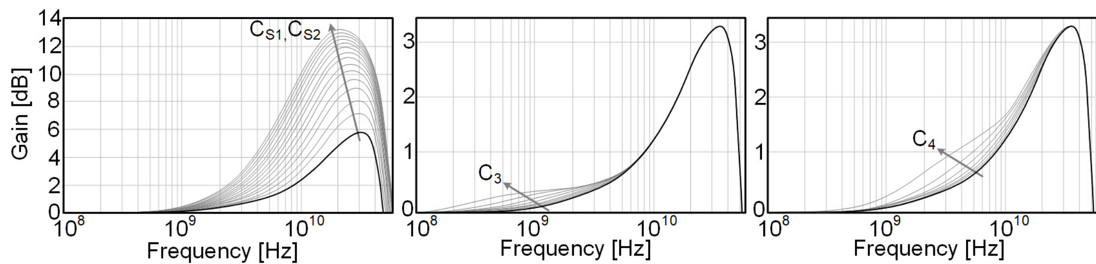


Figure 5.3: Frequency Response of CTLE from post-layout simulations.

The CTLE operation and its flexibility is proved by post-layout simulations in Fig. 5.3. The DC-gain is 0 dB. The high-frequency path can provide up to 13 dB peaking near

Nyquist frequency (28 GHz) by tuning C_{S1} and C_{S2}. The low-frequency path (g_{m3}) provides mild peaking with a pole-zero pair which can be shifted between 0.2 - 3 GHz by tuning C_3. Similarly, the mid-frequency path can provide peaking across 1 - 10 GHz by adjusting C_4. After the CTLE, a buffer with unity gain drives the subsequent UC-DFE, and draws 4 mA from 0.9 V supply. The RX linear chain draws 28 mA current from 0.9 V supply and can successfully operate with input signal amplitude up to 800 mV_{PP}.

1.3 Unclocked DFE

The latency in the feedback loop is the major obstacle for rising data-rate of the DFE. Indeed, reducing the inherent clock data delay and set-up time of the clocked slicers as well as the delay through the feedback path to be within one symbol period is challenging, and the issue is further exacerbated with PAM-4, requiring more complex hardware to manage the multi-level signal. The analog, unclocked DFE, proposed only for NRZ so far, is a promising alternative to rise speed. The latency of the first-tap feedback loop must still be equal to the symbol period. However, the latency is controlled by an adjustable and faster delay element, instead of a flip-flop. Moreover, the data decision is made in a different way. Instead of using a clocked slicer, with a delay that impacts significantly on the overall timing, data decision in the UC-DFE is performed by a saturated analog delay element. The extension of the UC-DFE architecture to PAM-4 signaling is described in this section. The presented UC-DFE implements two taps, as proposed in [76] for NRZ signals: one discrete tap (DT) and one tap with Infinite Impulse Response (IIR). As depicted in Fig. 5.4, the DT allows selective cancellation of the first post-cursor in the input pulse response while the second IIR tap provides long-tail correction. More taps can improve the equalization capability at the cost of larger power consumption. An analysis of this trade-off, for a clocked analog DFE implementation, is available in [77]. The block diagram of the PAM-4 UC-DFE is shown in Fig. 5.5 and comprises Adder, Comparators, and Delay Cells. Simulated eye diagrams in different nodes are also reported along with the block diagram. The adder combines the input with the correction signals for ISI cancellation. The 3 continuous-time comparators slice the PAM-4 input signal

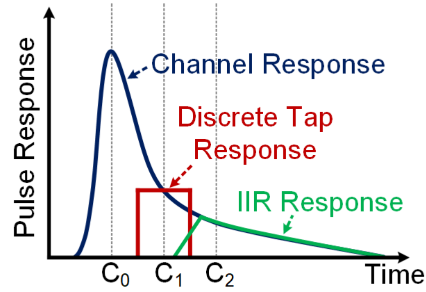


Figure 5.4: Pulse responses of Channel, DT-tap and IIR-tap

in 3 different (ideally binary) thermometric signals while the cascaded delay stages, amplifiers driven into the saturation region, take the final binary data decision and adjust the loop latency to be equal to the symbol time. Indeed, for minimal residual ISI at the center of the eye, the total delay in the feedback loop, from the input of the adder to the output of the correction taps (K_1, K_2 in Fig. 5.5), has to match the symbol period. Therefore, the delay stages after the adder are designed with a tunable delay. By setting all the 3 threshold voltages of the comparators in Fig. 5.5 to zero, maximizing the gain of the DT and disabling the IIR tap, the loop is unstable and oscillates with a period set by the feedback delay. The latter is adjusted by tuning the delay stages such that the frequency is equal to the symbol rate. In normal operation, the DFE does not show instability. Background calibration, as proposed in [73] for the NRZ UC-DFE, could also be implemented. Details on the circuits design of the PAM4 UC-DFE are presented in the following subsections.

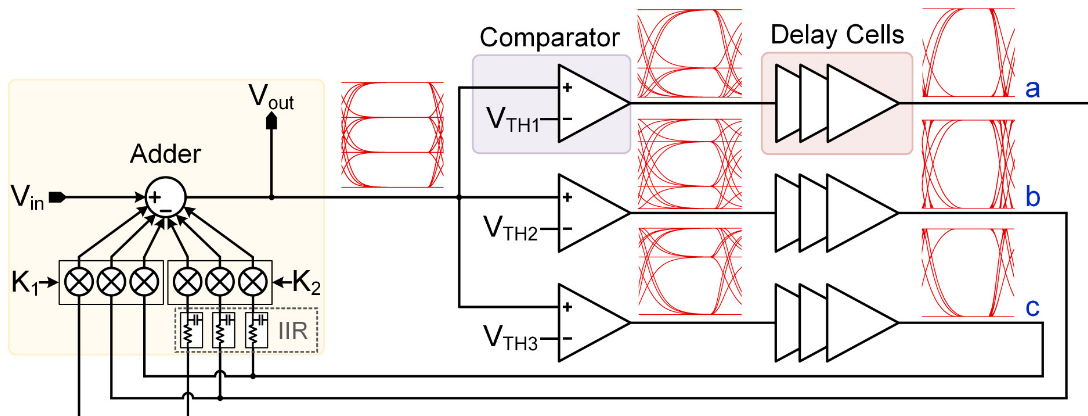


Figure 5.5: UC-DFE block diagram.

1.3.1 Adder

The adder combines the input with the correction signals from the DFE. Linearity is crucial not to distort the PAM-4 levels separation. The adder is realized as shown in Fig. 5.6. It comprises a main differential pair, driven by the input signal and linearized with resistive degeneration, and 2 sets of differential pairs, driven by the 1st (DT) and 2nd (IIR tap) DFE correction signals. The first set (K_1) is driven by the 3 binary outputs of the DFE delay paths, while the second set (K_2) is driven by a low-pass filtered version of the same signals [76, 78]. The two additional differential pairs (shown in gray in Fig. 5.6), are driven by the central DFE path in Fig. 5.5 and are used only in NRZ when the external paths are disabled to save power. The R-C low-pass filter for the IIR tap is realized with digitally programmable resistors for equalization of different channel profiles. The adder output nodes are loaded by the large drain parasitic capacitance of the several differential pairs and the input capacitance of the comparators. Because wide-bandwidth is necessary, not to introduce additional ISI, the load includes a T-coil peaking network. In this way, the bandwidth is extended beyond 40 GHz, contributing negligible ISI.

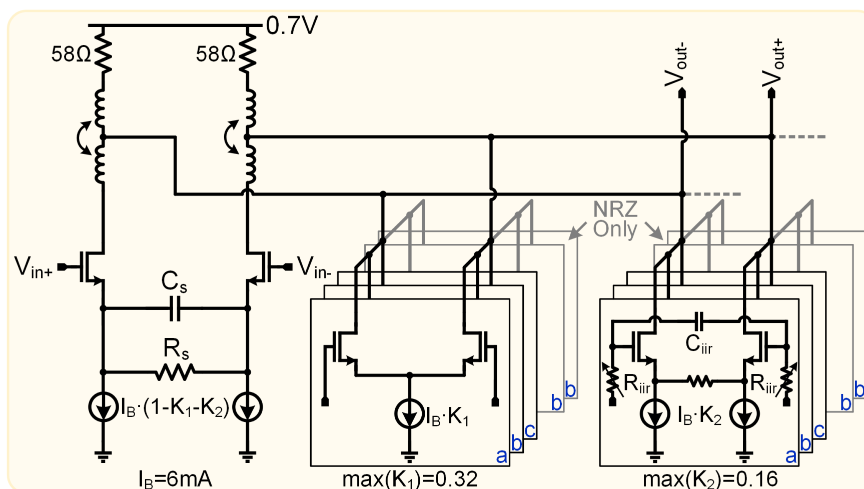


Figure 5.6: Schematic of the adder.

1.3.2 Comparators

The UC-DFE uses an array of 3 continuous-time comparators for symbol detection. The 3 comparators are driven by the PAM-4 signal provided by the adder block (of

amplitude V_{pk}) and generate a set of thermometric signals (ideally binary) that identify the received symbol. The 3 thresholds, made programmable by a DAC, should be in the middle of the 3 PAM-4 eyes, 0 for the middle comparator, and ideally $\pm 2/3 \cdot V_{pk}$ for the external comparators. With a realistic PAM-4 signal experiencing the channel attenuation and peaking from the CTLE, the optimal external thresholds may be different and are typically set by adaptation circuits [69], not considered in this work. The external thresholds are manually set close to $\pm 1/2 \cdot V_{pk}$, where the eye openings are larger, as proved by simulations in the next section.

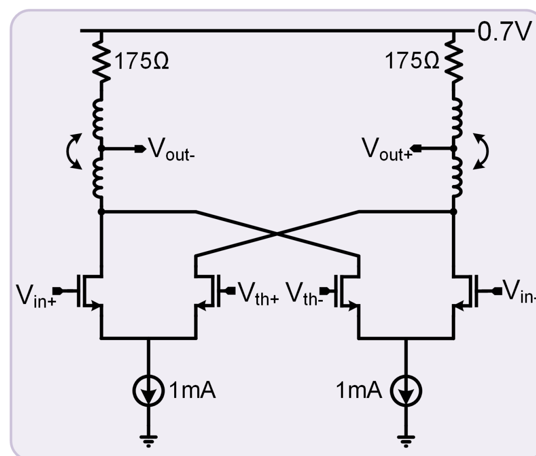


Figure 5.7: Schematic of a comparator.

The fully differential comparators are realized with the circuit topology in Fig. 5.7 and the differential threshold voltages can be set with a resistive DAC. Notably, the comparator circuit resembles the f_T doubler topology, giving the benefit of reducing the input capacitance which loads the adder stage. The design of the comparators entails a trade-off between gain and bandwidth: high gain is desirable to reach a binary (perfectly saturated) output, but high bandwidth is mandatory to settle the output in a fraction of the symbol duration. Despite the use of T-coil peaking to enlarge the bandwidth, the gain is not enough to saturate the outputs as shown by the eye diagrams at the output of the comparators in the block diagram of Fig. 5.5. However, the final symbol decision is made available in a binary fashion after passing the comparators' signals through the high-gain cascaded delay cells.

1.3.3 Delay Cell

The function of the delay cells is two fold: (1) provide the additional gain required to reach a fully saturated binary output signal and, (2) introduce the additional time delay such that the latency of the feedback loop is equal to the symbol period. Considering the target data-rate (112 Gb/s PAM-4 or 56 Gb/s NRZ), the total time delay of the feedback path must be equal to 17.9 ps. The adder and comparators introduce 5.9 ps delay thus the delay of the delay stages must be $\tau = 12$ ps.

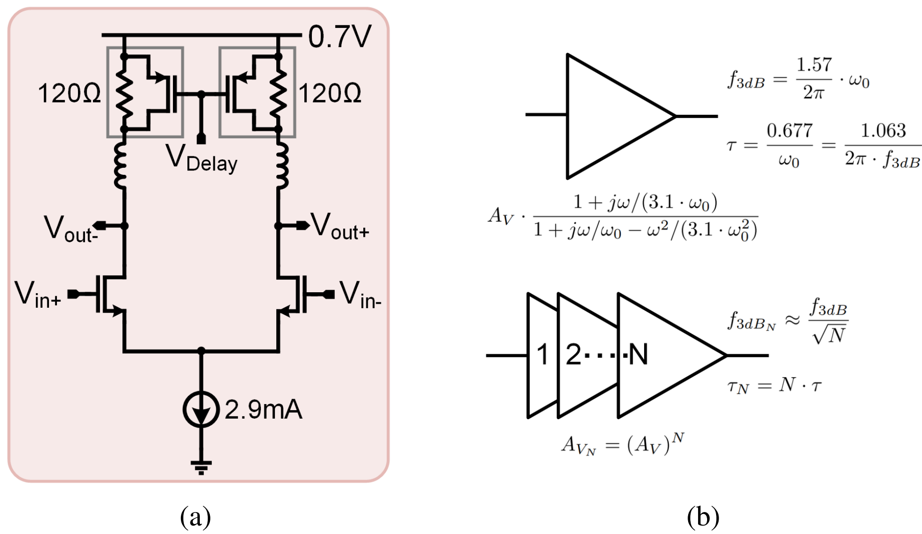


Figure 5.8: (a) Schematic of the amplifier used in the delay cells. (b) Transfer function and group-delay of a single stage and multi-stage amplifiers.

The delay cells are realized by cascading several differential-pair amplifiers with the schematic shown in Fig. 5.8(a). The load resistors are realized with PMOS in parallel, tuned by the gate voltage, allowing delay calibration. The amplifier chain has to provide simultaneously high-gain, to reach the saturated output, and wide bandwidth not to introduce ISI on the binary signal i.e. the gain-bandwidth product must be maximized. Considering the constraint on the loop delay, an optimum number of stages exists. To gain insight, Fig. 5.8(b) (top) shows a single amplifier stage with voltage gain A_V, bandwidth f_{3dB} and gain-bandwidth product $GBW = A_V \cdot f_{3dB}$. Assuming the peaking inductors are sized for maximally flat group delay [79], $\tau = 1.063/(2\pi \cdot f_{3dB})$. The resulting gain, group delay and bandwidth for the chain of N amplifiers are reported in Fig. 5.8(b). In this case the bandwidth of each amplifier has to be increased by N such that the total group delay ($\tau_N = N \cdot \tau = 1.063 \cdot N/(2\pi \cdot f_{3dB})$) remains

constant, but because of the GBW limit, the gain of each stage also decreases by N. Taking into account this constraint, the gain and bandwidth of the cascade can be written as:

$$A_{V_N} = \left(\frac{A_V}{N}\right)^N = \left(\frac{GBW}{f_{3dB} \cdot N}\right)^N = \left(\frac{2\pi \cdot \tau \cdot GBW}{1.063 \cdot N}\right)^N \tag{5.1}$$

$$f_{3dB_N} \approx \frac{N \cdot f_{3dB}}{\sqrt{N}} \tag{5.2}$$

in addition the gain-bandwidth product of the cascade, GBW_N, is

$$GBW_N = A_{V_N} \cdot f_{3dB_N} = (GBW)^N \cdot \left(\frac{2\pi \cdot \tau}{1.063 \cdot N}\right)^{N-1} \cdot \frac{1}{\sqrt{N}} \tag{5.3}$$

GBW_N (eq. (5.3)) is maximum for an optimal number of stages which depends on the target group delay, τ, and the GBW of the single stage (set by the technology and circuit topology of the amplifier). Fig. 5.9 plots eq. (5.3) considering $\tau = 12$ ps and GBW = 90 GHz, (derived from simulations on the differential pair in Fig. 5.8(a)). The optimum number of amplifiers to be used in each delay stage is 3.

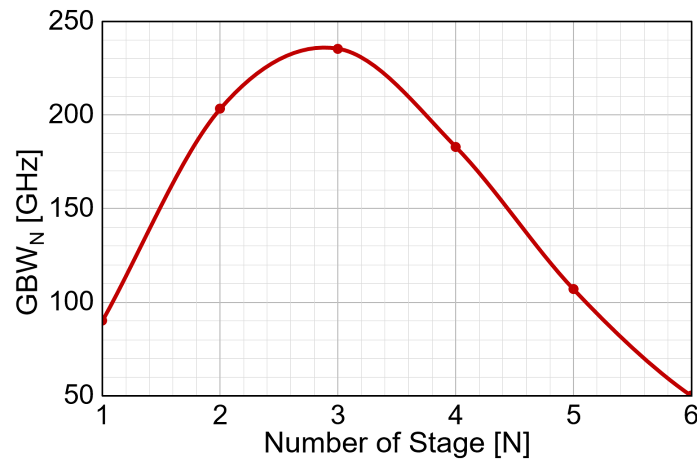


Figure 5.9: Gain-Bandwidth product of cascaded amplifiers featuring 12 ps group delays.

To gain further insight, the plots in Fig. 5.10 compare the simulated signal at the output of the delay cell driven by the middle comparator in the UC-DFE, when it is implemented with N = 1, N = 3 and N = 6 cascaded stages. All 3 cases introduce the same delay. If a single differential pair is used (N = 1), the gain (16.6 dB) is enough to saturate the output and reach a binary signal but the low bandwidth (13.3 GHz), required to meet the delay constraint, leads to excessive ISI. In the opposite case, with

N = 6 cascaded stages, each stage is designed with very wide bandwidth to reach the target delay. The overall bandwidth is wide (27.8 GHz), providing an output signal with minimal ISI, but the gain is too low (6.4 dB) to saturate the output. In the optimal situation of N = 3, the chain features 20.3 GHz bandwidth with 21.3 dB gain, and allows to reach a binary output with minimal ISI and timing jitter (middle plot in Fig. 5.10).

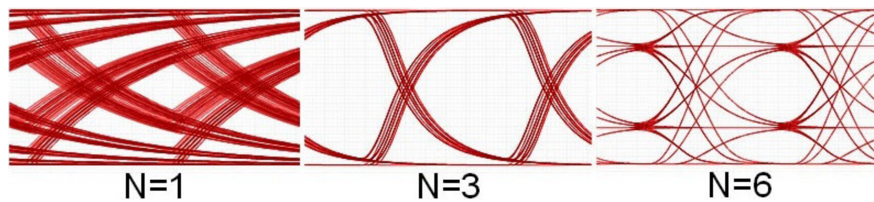
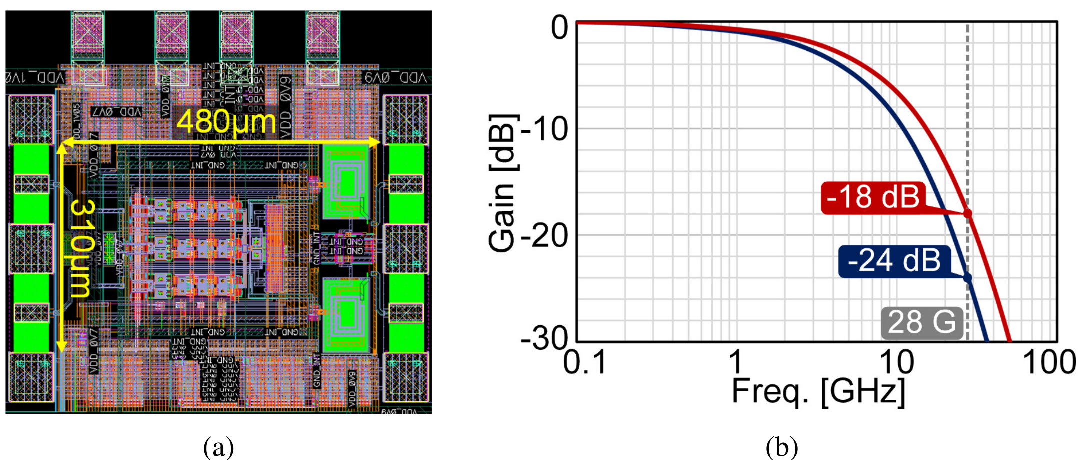


Figure 5.10: Eye diagrams for delay cells with a different number of stages.

1.4 Results

The receiver front-end has been designed in a 7 nm FinFet technology. The peaking inductors and T-coils are fully customized and modelled with an electromagnetic simulator. A picture of the layout is shown in Fig. 5.11(a). The active area, excluding pads, is 310 x 480 µm. In simulations, a worst sequence PRBS31 pattern generator feeds a realistic channel model (Fig. 5.11(b)) and the output of the channel is connected to the receiver front-end.



(a) (b)

Figure 5.11: (a) Layout of the RX front-end with the UC-DFE. (b) The channel transfer functions.

Results are presented in NRZ at 56 Gb/s and PAM-4 at 112 Gb/s with 800 mV_{PP} input signal and the VGA is configured for -2 dB gain (results with 500 mV_{PP} and the VGA

programmed for +2 dB gain are similar). In NRZ, a 24 dB channel loss at Nyquist frequency is considered and the CTLE provides 12 dB peaking. Fig. 5.12 plots the eye at the input of the analog front-end (channel output), the eye after the linear chain, and the eye after the correction from the UC-DFE. The eye after the channel (top plot) is totally closed. After the VGA and CTLE (middle plot) the eye is marginally open with vertical and horizontal openings of 27 % and 0.77 UI respectively. The effectiveness of the UC-DFE is proved by the bottom plot where vertical and horizontal openings are raised to 65 % and 0.87 UI respectively.

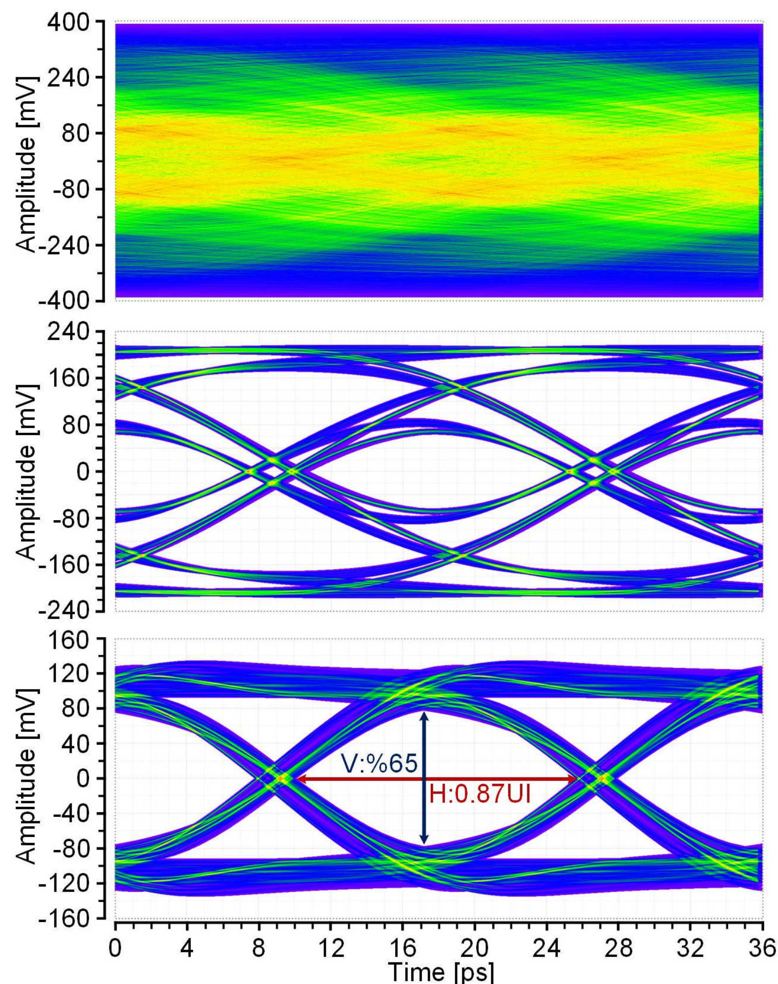


Figure 5.12: 56 Gb/s eye diagrams with 24 dB channel loss: input signal (top), CTLE output (middle), signal after UC-DFE correction (bottom).

The same simulations, but with PAM-4 input signal are presented in Fig. 5.13. In this case the channel loss is 18 dB at the Nyquist frequency with the CTLE still introducing 12 dB peaking. The signal is still totally corrupted after the channel (top

plot). The 3 PAM-4 eyes are minimally open after the linear chain, with vertical and horizontal openings of 6 % and 0.33 UI only. After the UC-DFE correction ($K_1 = 0.2$, $K_2 = 0.16$), the 3 PAM-4 eyes are clearly visible at the adder output node, with a vertical and horizontal opening of 18 % and 0.35 UI respectively. The peak-to-peak signal amplitude at the detection node, in front of the 3 comparators of the UC-DFE, is 300 mV and the amplitude of the 3 eyes is 54 mV. The estimated rms noise is 2.7 mV_{rms} (70 % of which is contributed by the RX linear chain) allowing a row bit error rate of 10^{-6} with margin. The linear chain consumes 25.2 mW from 0.9 V. The UC-DFE burns 28 mW from 0.7 V for PAM-4 and 14 mW in NRZ configuration, where two out of the 3 DFE paths are disabled. The corresponding RX power efficiency is 0.47 pJ/bit for PAM-4 and 0.70 pJ/bit in NRZ.

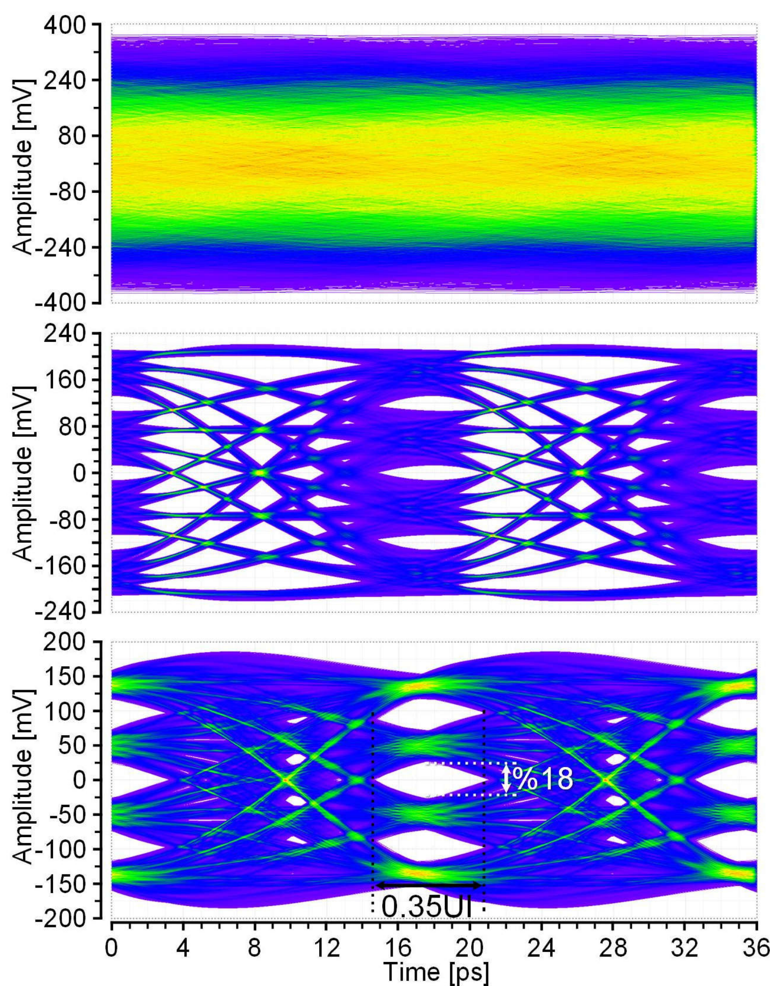


Figure 5.13: 112 Gb/s eye diagrams with 18 dB channel loss: input signal (top), CTLE output (middle), signal after UC-DFE correction (bottom).

1.5 Conclusion

An architecture for UC-DFE has been investigated for power-efficient equalization in VSR links at ultra-high speed. The operation is proved with the design of a 112 Gb/s PAM-4 receiver in 7 nm FinFet technology comprising a VGA, CTLE and the proposed UC-DFE.

Post-layout simulations proved equalization up to 18 dB and 24 dB channel losses at Nyquist frequency for PAM-4 and NRZ signals. The corresponding RX power efficiency is 0.47 pJ/bit for PAM-4 and 0.70 pJ/bit in NRZ.

References

[1] **Frecassetti, M.G.L.**, **Mazzanti, A.**, **Sevillano, J.F.**, **del Río, D. and Ermolov, V.**, 2019. D-Band Transport Solution to 5G and Beyond 5G Cellular Networks, 2019 European Conference on Networks and Communications (EuCNC), pp.214–218.

[2] **GSMA**, 2018 (accessed September 28, 2020). Mobile backhaul options, https://www.gsma.com/spectrum/wp-content/uploads/2019/04/Mobile-Backhaul-Options.pdf.

[3] **Samsung**, 2018 (accessed September 29, 2020). Who & How:Making 5G NR Standards, https://images.samsung.com/is/content/samsung/p5/global/business/networks/insights/white-paper/who-and-how_making-5g-nr-standards/who-and-how_making-5g-nr-standards.pdf.

[4] **DREAM**, 2017 (accessed September 28, 2020). D-band Radio solution Enabling up to 100 Gbps reconfigurable Approach for Meshed beyond 5G networks, http://www.h2020-dream.eu/overview/.

[5] **Ericsson**, 2017 (accessed September 28, 2020). Ericsson Microwave Outlook, https://www.ericsson.com/4adea3/assets/local/reports-papers/microwave-outlook/2017/ericsson-microwave-outlook-report-2017.pdf.

[6] **Li, Y. and Hansryd, J.**, 2018. Fixed Wireless Communication Links Beyond 100 GHZ, 2018 Asia-Pacific Microwave Conference (APMC), pp.31–33.

[7] **Ping-Heng Kuo and Mourad, A.**, 2017. Millimeter wave for 5G mobile fronthaul and backhaul, 2017 European Conference on Networks and Communications (EuCNC), pp.1–5.

[8] **ECC**, 2018 (accessed April 27, 2018). ECC Recommendation (18)01 on Radio frequency channel/block arrangements for Fixed Service systems operating in the bands 130-134 GHz, 141-148.5 GHz, 151.5-164 GHz and 167-174.8 GHz, https://docdb.cept.org/download/a5533f97-5a92/Rec1801.pdf.

[9] **TARANTO**, 2017 (accessed September 28, 2020). TowARds Advanced bicmos NanoTechnology platforms for rf to the applicatiOns, http://tima.univ-grenoble-alpes.fr/taranto/.

[10] **Sadhu, B.**, **Gu, X. and Valdes-Garcia, A.**, 2019. The More (Antennas), the Merrier: A Survey of Silicon-Based mm-Wave Phased Arrays Using Multi-IC Scaling, *IEEE Microwave Magazine*, **20(12)**, 32–50.

[11] **Wang, H.**, **Huang, T.**, **Mannem, N.S.**, **Lee, J.**, **Garay, E.**, **Munzer, D.**, **Liu, E.**, **Liu, Y.**, **Lin, B.**, **Eleraky, M.**, **Li, S.**, **Wang, F.**, **Ahmed, A.S.**, **Snyder, C.**,

Lee, S., **Nguyen, H.T.**, **and Smith, M.E.D.** Power Amplifiers Performance Survey 2000-Present, `https://gems.ece.gatech.edu/PA_survey.html`.

[12] **Petricli, I.**, **Lotfi, H. and Mazzanti, A.**, 2020. Design of Compact D-Band Amplifiers With Accurate Modeling of Inductors and Current Return Paths in 55-nm SiGe BiCMOS, *IEEE Solid-State Circuits Letters*, **3**, 250–253.

[13] **Petricli, I.**, **Lotfi, H. and Mazzanti, A.**, 2020. 150 GHz Differential Amplifiers with Lumped-Elements Matching Networks in 55 nm SiGe BiCMOS, 2020 27th IEEE International Conference on Electronics, Circuits and Systems (ICECS).

[14] **Petricli, I.**, **Zhang, H.**, **Monaco, E.**, **Albasini, G. and Mazzanti, A.**, 2020. A 112 Gb/s PAM-4 RX Front-End with Unclocked Decision Feedback Equalizer, *IEEE Transactions on Circuits and Systems II: Express Briefs*, 1–1.

[15] **Laskin, E.**, **Chevalier, P.**, **Chantre, A.**, **Sautreuil, B. and Voinigescu, S.P.**, 2007. 80/160-GHz Transceiver and 140-GHz Amplifier in SiGe Technology, 2007 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, pp.153–156.

[16] **Liu, G. and Schumacher, H.**, 2012. 47–77 GHz and 70–155 GHz LNAs in SiGe BiCMOS technologies, 2012 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), pp.1–4.

[17] **Ulusoy, A..**, **Kaynak, M.**, **Valenta, V.**, **Tillack, B. and Schumacher, H.**, 2013. A 110 GHz LNA with 20dB gain and 4dB noise figure in an 0.13μm SiGe BiCMOS technology, 2013 IEEE MTT-S International Microwave Symposium Digest (MTT), pp.1–3.

[18] **Ulusoy, A..**, **Song, P.**, **Khan, W.T.**, **Kaynak, M.**, **Tillack, B.**, **Papapolymerou, J. and Cressler, J.D.**, 2015. A SiGe D-Band Low-Noise Amplifier Utilizing Gain-Boosting Technique, *IEEE Microwave and Wireless Components Letters*, **25(1)**, 61–63.

[19] **Heredia, J.**, **Ribó, M.**, **Pradell, L.**, **Wipf, S.T.**, **Göritz, A.**, **Wietstruck, M.**, **Wipf, C. and Kaynak, M.**, 2019. A 125–143-GHz Frequency-Reconfigurable BiCMOS Compact LNA Using a Single RF-MEMS Switch, *IEEE Microwave and Wireless Components Letters*, **29(5)**, 339–341.

[20] **Turkmen, E.**, **Burak, A.**, **Guner, A.**, **Kalyoncu, I.**, **Kaynak, M. and Gurbuz, Y.**, 2018. A SiGe HBT D-Band LNA With Butterworth Response and Noise Reduction Technique, *IEEE Microwave and Wireless Components Letters*, **28(6)**, 524–526.

[21] **Dickson, T.O.**, **LaCroix, M..**, **Boret, S.**, **Gloria, D.**, **Beerkens, R. and Voinigescu, S.P.**, 2005. 30-100-GHz inductors and transformers for millimeter-wave (Bi)CMOS integrated circuits, *IEEE Transactions on Microwave Theory and Techniques*, **53(1)**, 123–133.

[22] **Wang, H.**, **Zhang, L.**, **Yang, D.**, **Zeng, D.**, **Wang, Y. and Yu, Z.**, 2011. Modeling of Current-Return-Path Effect on Single-Ended Inductor in Millimeter-Wave Regime, *IEEE Electron Device Letters*, **32(6)**, 737–739.

[23] **Zhu, Y.**, **Kang, K.**, **Wu, Y.**, **Zhao, C.**, **Ban, Y.**, **Guo, J.**, **Sun, L.L.**, **Yin, W. and Xue, Q.**, 2015. An Equivalent Circuit Model With Current Return Path Effects for ON-Chip Interconnect up to 80 GHz, *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **5(9)**, 1320–1330.

[24] **Engen, G.F. and Hoer, C.A.**, 1979. Thru-Reflect-Line: An Improved Technique for Calibrating the Dual Six-Port Automatic Network Analyzer, *IEEE Transactions on Microwave Theory and Techniques*, **27(12)**, 987–993.

[25] **Testa, P.V.**, **Belfiore, G.**, **Fritsche, D.**, **Carta, C. and Ellinger, F.**, 2014. 170 GHz SiGe-BiCMOS Loss-Compensated Distributed Amplifier, 2014 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), pp.1–4.

[26] **Testa, P.V.**, **Carta, C.**, **Jörges, U. and Ellinger, F.**, 2018. Analysis and Design of a 30- to 220-GHz Balanced Cascaded Single-Stage Distributed Amplifier in 130-nm SiGe BiCMOS, *IEEE Journal of Solid-State Circuits*, **53(5)**, 1457–1467.

[27] **Khatibi, H.**, **Khiyabani, S. and Afshari, E.**, 2018. A 173 GHz Amplifier With a 18.5 dB Power Gain in a 130 nm SiGe Process: A Systematic Design of High-Gain Amplifiers Above $f_{\mathrm{max}}/2$, *IEEE Transactions on Microwave Theory and Techniques*, **66(1)**, 201–214.

[28] **Bameri, H. and Momeni, O.**, 2017. A High-Gain mm-Wave Amplifier Design: An Analytical Approach to Power Gain Boosting, *IEEE Journal of Solid-State Circuits*, **52(2)**, 357–370.

[29] **Park, D.**, **Utomo, D.R.**, **Hong, J. and Lee, S.**, 2018. A 230–260GHz wideband amplifier in 65nm CMOS based on dual-peak Gmax-core, 2018 23rd Asia and South Pacific Design Automation Conference (ASP-DAC), pp.301–302.

[30] **Seo, M.**, **Jagannathan, B.**, **Pekarik, J. and Rodwell, M.J.W.**, 2009. A 150 GHz Amplifier With 8 dB Gain and +6 dBm P_{sat} in Digital 65 nm CMOS Using Dummy-Prefilled Microstrip Lines, *IEEE Journal of Solid-State Circuits*, **44(12)**, 3410–3421.

[31] **Xu, Z.**, **Gu, Q.J. and Chang, M.F.**, 2011. A Three Stage, Fully Differential 128–157 GHz CMOS Amplifier with Wide Band Matching, *IEEE Microwave and Wireless Components Letters*, **21(10)**, 550–552.

[32] **Kim, D.**, **Kim, D. and Rieh, J.**, 2017. A D -Band CMOS Amplifier With a New Dual-Frequency Interstage Matching Technique, *IEEE Transactions on Microwave Theory and Techniques*, **65(5)**, 1580–1588.

[33] **Parveg, D.**, **Varonen, M.**, **Karaca, D.**, **Vahdati, A.**, **Kantanen, M. and Halonen, K.A.I.**, 2018. Design of a D-Band CMOS Amplifier Utilizing Coupled Slow-Wave Coplanar Waveguides, *IEEE Transactions on Microwave Theory and Techniques*, **66(3)**, 1359–1373.

[34] **Aguilar, E.**, **Hagelauer, A.**, **Kissinger, D. and Weigel, R.**, 2018. A low-power wideband D-band LNA in a 130 nm BiCMOS technology for imaging applications, 2018 IEEE 18th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF), pp.27–29.

[35] **Turkmen, E.**, **Burak, A.**, **Guner, A.**, **Kalyoncu, I.**, **Kaynak, M. and Gurbuz, Y.**, 2018. A SiGe HBT *D* -Band LNA With Butterworth Response and Noise Reduction Technique, *IEEE Microwave and Wireless Components Letters*, **28(6)**, 524–526.

[36] **Ustundag, B.**, **Turkmen, E.**, **Cetindogan, B.**, **Guner, A.**, **Kaynak, M. and Gurbuz, Y.**, 2018. Low-Noise Amplifiers for W-Band and D-Band Passive Imaging Systems in SiGe BiCMOS Technology, 2018 Asia-Pacific Microwave Conference (APMC), pp.651–653.

[37] **Stärke, P.**, **Rieß, V.**, **Carta, C. and Ellinger, F.**, 2018. Wideband Amplifier with Integrated Power Detector for 100 GHz to 200 GHz mm-Wave Applications, 2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), pp.160–163.

[38] **Ben Yishay, R. and Elad, D.**, 2017. D-band Dicke-radiometer in 90 nm SiGe BiCMOS technology, 2017 IEEE MTT-S International Microwave Symposium (IMS), pp.1957–1960.

[39] **Yishay, R.B.**, **Shumaker, E. and Elad, D.**, 2015. A 122-150 GHz LNA with 30 dB gain and 6.2 dB noise figure in SiGe BiCMOS technology, 2015 IEEE 15th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, pp.15–17.

[40] **Shumakher, E.**, **Elkind, J. and Elad, D.**, 2013. Key components of a 130 GHz dicke-radiometer SiGe RFIC, 2013 IEEE 13th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, pp.255–257.

[41] **Liu, G. and Schumacher, H.**, 2012. 47–77 GHz and 70–155 GHz LNAs in SiGe BiCMOS technologies, 2012 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), pp.1–4.

[42] **Ulusoy, A..**, **Song, P.**, **Khan, W.T.**, **Kaynak, M.**, **Tillack, B.**, **Papapolymerou, J. and Cressler, J.D.**, 2015. A SiGe D-Band Low-Noise Amplifier Utilizing Gain-Boosting Technique, *IEEE Microwave and Wireless Components Letters*, **25(1)**, 61–63.

[43] **Coen, C.T.**, **Ulusoy, A..**, **Song, P.**, **Ildefonso, A.**, **Kaynak, M.**, **Tillack, B. and Cressler, J.D.**, 2016. Design and On-Wafer Characterization of *G* -Band SiGe HBT Low-Noise Amplifiers, *IEEE Transactions on Microwave Theory and Techniques*, **64(11)**, 3631–3642.

[44] **Turkmen, E.**, **Cetindogan, B.**, **Yazici, M. and Gurbuz, Y.**, 2020. Design and Characterization of a D-Band SiGe HBT Front-End for Dicke Radiometers, *IEEE Sensors Journal*, **20(9)**, 4694–4703.

[45] **Kanar, T. and Rebeiz, G.M.**, 2016. A Low-Power 136-GHz SiGe Total Power Radiometer With NETD of 0.25 K, *IEEE Transactions on Microwave Theory and Techniques*, **64(3)**, 906–914.

[46] **Ludwig, R. and Bogdanov, G.**, 2009. RF Circuit Design: Theory and Applications, Pearson.

[47] **Fritsche, D.**, **Tretter, G.**, **Stärke, P.**, **Carta, C. and Ellinger, F.**, 2017. A Low-Power SiGe BiCMOS 190-GHz Receiver With 47-dB Conversion Gain and 11-dB Noise Figure for Ultralarge-Bandwidth Applications, *IEEE Transactions on Microwave Theory and Techniques*, **65(10)**, 4002–4013.

[48] **Zhang, Y.**, **Liang, W.**, **Jin, X.**, **Krattenmacher, M.**, **Falk, S.**, **Sakalas, P.**, **Heinemann, B. and Schröter, M.**, 2020. 3.2-mW Ultra-Low-Power 173–207-GHz Amplifier With 130-nm SiGe HBTs Operating in Saturation, *IEEE Journal of Solid-State Circuits*, **55(6)**, 1471–1481.

[49] **Caster II, F.**, **Gilreath, L.**, **Pan, S.**, **Wang, Z.**, **Capolino, F. and Heydari, P.**, 2014. Design and Analysis of a W-band 9-Element Imaging Array Receiver Using Spatial-Overlapping Super-Pixels in Silicon, *IEEE Journal of Solid-State Circuits*, **49(6)**, 1317–1332.

[50] **Gilbert, E.**, 1975. Impedance matching with lossy components, *IEEE Transactions on Circuits and Systems*, **22(2)**, 96–100.

[51] **Capek, M.**, **Jelinek, L. and Hazdra, P.**, 2015. On the Functional Relation Between Quality Factor and Fractional Bandwidth, *IEEE Transactions on Antennas and Propagation*, **63(6)**, 2787–2790.

[52] **Pozar, D.M.**, 2011. Microwave Engineering, Wiley.

[53] **Chevalier, P.**, **Avenier, G.**, **Ribes, G.**, **Montagné, A.**, **Canderle, E.**, **Céli, D.**, **Derrier, N.**, **Deglise, C.**, **Durand, C.**, **Quémerais, T.**, **Buczko, M.**, **Gloria, D.**, **Robin, O.**, **Petitdidier, S.**, **Campidelli, Y.**, **Abbate, F.**, **Gros-Jean, M.**, **Berthier, L.**, **Chapon, J.D.**, **Leverd, F.**, **Jenny, C.**, **Richard, C.**, **Gourhant, O.**, **De-Buttet, C.**, **Beneyton, R.**, **Maury, P.**, **Joblot, S.**, **Favennec, L.**, **Guillermet, M.**, **Brun, P.**, **Courouble, K.**, **Haxaire, K.**, **Imbert, G.**, **Gourvest, E.**, **Cossalter, J.**, **Saxod, O.**, **Tavernier, C.**, **Foussadier, F.**, **Ramadout, B.**, **Bianchini, R.**, **Julien, C.**, **Ney, D.**, **Rosa, J.**, **Haendler, S.**, **Carminati, Y. and Borot, B.**, 2014. A 55 nm triple gate oxide 9 metal layers SiGe BiCMOS technology featuring 320 GHz fT / 370 GHz fMAX HBT and high-Q millimeter-wave passives, 2014 IEEE International Electron Devices Meeting, pp.3.9.1–3.9.3.

[54] **Lin, H. and Rebeiz, G.M.**, 2014. A 110–134-GHz SiGe Amplifier With Peak Output Power of 100–120 mW, *IEEE Transactions on Microwave Theory and Techniques*, **62(12)**, 2990–3000.

[55] **Visweswaran, A.**, **Vignon, B.**, **Tang, X.**, **Brebels, S.**, **Debaillie, B. and Wambacq, P.**, 2019. A 112-142GHz Power Amplifier with Regenerative Reactive Feedback

achieving 17dBm peak Psat at 1345th European Solid State Circuits Conference (ESSCIRC), pp.337–340.

[56] **Yishay, R.B. and Elad, D.**, 2015. A 17.8 dBm 110–130 GHz Power Amplifier and doubler chain in SiGe BiCMOS technology, 2015 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), pp.391–394.

[57] **Furqan, M.**, **Ahmed, F.**, **Heinemann, B. and Stelzer, A.**, 2017. A 15.5-dBm 160-GHz High-Gain Power Amplifier in SiGe BiCMOS Technology, *IEEE Microwave and Wireless Components Letters*, **27(2)**, 177–179.

[58] **Philippe, B. and Reynaert, P.**, 2020. 24.7 A 15dBm 12.8in 16nm FinFET CMOS, 2020 IEEE International Solid- State Circuits Conference - (ISSCC), pp.374–376.

[59] **Simic, D. and Reynaert, P.**, 2018. A 14.8 dBm 20.3 dB Power Amplifier for D-band Applications in 40 nm CMOS, 2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), pp.232–235.

[60] **Sedra, A. and Smith, K.**, 2010. Microelectronic Circuits, Oxford University Press.

[61] **Rahimi, E.**, **Zhao, J.**, **Svelto, F. and Mazzanti, A.**, 2019. High-Efficiency SiGe-BiCMOS E -Band Power Amplifiers Exploiting Current Clamping in the Common-Base Stage, *IEEE Journal of Solid-State Circuits*, **54(8)**, 2175–2185.

[62] **Rickelt, M.**, **Rein, H.. and Rose, E.**, 2001. Influence of impact-ionization-induced instabilities on the maximum usable output voltage of Si-bipolar transistors, *IEEE Transactions on Electron Devices*, **48(4)**, 774–783.

[63] **Zhenqiang Ma and Ningyue Jiang**, 2005. On the operation configuration of SiGe HBTs based on power gain analysis, *IEEE Transactions on Electron Devices*, **52(2)**, 248–255.

[64] **Brederlow, R.**, **Weber, W.**, **Sauerer, J.**, **Donnay, S.**, **Wambacq, P. and Vertregt, M.**, 2001. A mixed-signal design roadmap, *IEEE Design Test of Computers*, **18(6)**, 34–46.

[65] **Hudner, J.**, **Carey, D.**, **Casey, R.**, **Hearne, K.**, **de Abreu Farias Neto, P.W.**, **Chlis, I.**, **Erett, M.**, **Poon, C.F.**, **Laraba, A.**, **Zhang, H.**, **Chaitanya Ambatipudi, S.L.**, **Mahashin, D.**, **Upadhyaya, P.**, **Frans, Y. and Chang, K.**, 2018. A 112GB/S PAM4 Wireline Receiver Using a 64-Way Time-Interleaved SAR ADC in 16NM FinFET, 2018 IEEE Symposium on VLSI Circuits, pp.47–48.

[66] **Krupnik, Y.**, **Perelman, Y.**, **Levin, I.**, **Sanhedrai, Y.**, **Eitan, R.**, **Khairi, A.**, **Shifman, Y.**, **Landau, Y.**, **Virobnik, U.**, **Dolev, N.**, **Meisler, A. and Cohen, A.**, 2020. 112-Gb/s PAM4 ADC-Based SERDES Receiver With Resonant AFE for Long-Reach Channels, *IEEE Journal of Solid-State Circuits*, **55(4)**, 1077–1085.

[67] **Im, J.**, **Zheng, K.**, **Chou, A.**, **Zhou, L.**, **Kim, J.W.**, **Chen, S.**, **Wang, Y.**, **Hung, H.**, **Tan, K.**, **Lin, W.**, **Roldan, A.**, **Carey, D.**, **Chlis, I.**, **Casey, R.**, **Bekele, A.**, **Cao, Y.**, **Mahashin, D.**, **Ahn, H.**, **Zhang, H.**, **Frans, Y. and Chang, K.**,

2020. 6.1 A 112Gb/s PAM-4 Long-Reach Wireline Transceiver Using a 36-Way Time-Interleaved SAR-ADC and Inverter-Based RX Analog Front-End in 7nm FinFET, 2020 IEEE International Solid- State Circuits Conference - (ISSCC), pp.116–118.

[68] **Ali, T.**, **Chen, E.**, **Park, H.**, **Yousry, R.**, **Ying, Y.**, **Abdullatif, M.**, **Gandara, M.**, **Liu, C.**, **Weng, P.**, **Chen, H.**, **Elbadry, M.**, **Nehal, Q.**, **Tsai, K.**, **Tan, K.**, **Huang, Y.**, **Tsai, C.**, **Chang, Y. and Tung, Y.**, 2020. 6.2 A 460mW 112Gb/s DSP-Based Transceiver with 38dB Loss Compensation for Next-Generation Data Centers in 7nm FinFET Technology, 2020 IEEE International Solid- State Circuits Conference - (ISSCC), pp.118–120.

[69] **Peng, P.**, **Li, J.**, **Chen, L. and Lee, J.**, 2017. 6.1 A 56Gb/s PAM-4/NRZ transceiver in 40nm CMOS, 2017 IEEE International Solid-State Circuits Conference (ISSCC), pp.110–111.

[70] **Chandramouli, S.**, **Bien, F.**, **Hyoungsoo Kim**, **Gebara, E. and Laskar, J.**, 2007. A 10-Gb/sec unclocked current-mode logic (CML) analog decision-feedback equalizer (ADFE) in 0.18-μm CMOS, ESSCIRC 2007 - 33rd European Solid-State Circuits Conference, pp.512–515.

[71] **Chandramouli, S.**, **Bien, F.**, **Kim, H.**, **Scholz, C.**, **Gebara, E. and Laskar, J.**, 2007. 10-Gb/s Optical Fiber Transmission Using a Fully Analog Electronic Dispersion Compensator (EDC) With Unclocked Decision-Feedback Equalization, *IEEE Transactions on Microwave Theory and Techniques*, **55(12)**, 2740–2746.

[72] **Pozzoni, M.**, **Erba, S.**, **Sanzogni, D.**, **Ganzerli, M.**, **Viola, P.**, **Baldi, D.**, **Repossi, M.**, **Spelgatti, G. and Svelto, F.**, 2010. A 12Gb/s 39dB loss-recovery unclocked-DFE receiver with bi-dimensional equalization, 2010 IEEE International Solid-State Circuits Conference - (ISSCC), pp.164–165.

[73] **Gangasani, G.R. and Kinget, P.R.**, 2018. A 19Gb/s RX for VSR-C2C Links with Clock-Less DFE and High-BW CDR Based on Master-Slave ILOs in 14nm CMOS, ESSCIRC 2018 - IEEE 44th European Solid State Circuits Conference (ESSCIRC), pp.182–185.

[74] **OIF**, 2017 (accessed December 29, 2017). Common Electrical I/O (CEI) - Electrical and Jitter Interoperability agreements for 6G+ bps, 11G+ bps, 25G+ bps I/O and 56G+ bps, `https://www.oiforum.com/wp-content/uploads/2019/01/OIF-CEI-04.0.pdf`.

[75] **Shahramian, S.**, **Dehlaghi, B. and Chan Carusone, A.**, 2016. Edge-Based Adaptation for a 1 IIR + 1 Discrete-Time Tap DFE Converging in 5 μ s, *IEEE Journal of Solid-State Circuits*, **51(12)**, 3192–3203.

[76] **Thakkar, C.**, **Kong, L.**, **Jung, K.**, **Frappe, A. and Alon, E.**, 2012. A 10 Gb/s 45 mW Adaptive 60 GHz Baseband in 65 nm CMOS, *IEEE Journal of Solid-State Circuits*, **47(4)**, 952–968.

[77] **Depaoli, E.**, **Zhang, H.**, **Mazzini, M.**, **Audoglio, W.**, **Rossi, A.A.**, **Albasini, G.**, **Pozzoni, M.**, **Erba, S.**, **Temporiti, E. and Mazzanti, A.**, 2019. A 64 Gb/s Low-Power Transceiver for Short-Reach PAM-4 Electrical Links in 28-nm FDSOI CMOS, *IEEE Journal of Solid-State Circuits*, **54(1)**, 6–17.

[78] **Kim, B.**, **Liu, Y.**, **Dickson, T.O.**, **Bulzacchelli, J.F. and Friedman, D.J.**, 2009. A 10-Gb/s Compact Low-Power Serial I/O With DFE-IIR Equalization in 65-nm CMOS, *IEEE Journal of Solid-State Circuits*, **44(12)**, 3526–3538.

[79] **Shekhar, S.**, **Walling, J.S. and Allstot, D.J.**, 2006. Bandwidth Extension Techniques for CMOS Amplifiers, *IEEE Journal of Solid-State Circuits*, **41(11)**, 2424–2439.