UNIVERSITY OF PAVIA

Department of Electrical, Computer and Biomedical Engineering

PHD THESIS IN MICROELECTRONICS

XXXIII CYCLE

High-speed Time-interleaved Digital-to-Analog Converter (TI-DAC) for Self-Interference Cancellation Applications

Supervisor:
Prof. Danilo Manstreta

Co-supervisour:
Prof. Rinaldo Castello

Coordinator:
Prof. Pietro Malcovati

Author:
Mazyar Abedinkhan Eslami

November 2021

`

High-speed Time-interleaved Digital-to-Analog Converter (TI-DAC) for Self-Interference-Cancellation Applications

Mazyar Abedinkhan Eslami

A thesis submitted in partial fulfilment of the requirements for the degree of Doctor of Philosophy

UNIVERSITY OF PAVIA

NOVEMBER 2021

Declaration of Authorship

I, Mazyar Abedinkhan Eslami, declare that this thesis titled, "High-speed Time-interleaved Digital-to-Analog Converter (TI-DAC) for Self-Interference-Cancellation Applications" and the work presented in it are my own. I confirm that:

- This work was done wholly or mainly while in candidature for a research degree at the University of Pavia.
- Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated. Where I have consulted the published work of others, this is always clearly at tributed.
- Where I have quoted from the work of others, the source is always given. With exception of such quotations, this thesis is entirely my own work.
- I have acknowledged all main sources of help.

Where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself.

`

To all the people who has died because of Covid-19 and the wars across the globe.

I would like to thank God, then my family who morally and financially support me and have had vital contribution on my success, the most:

my lovely mother, deceased father, deceased grandparents, uncle, aunts, and Dr. Naserniya.

Unfortunately, some of them are not with me at this moment but their memories are always with me like my deceased father and grandparents.

Some rise by sin, and some by virtue fall.

William Shakespeare

`

UNIVERSITY OF PAVIA

Abstract

High-speed Time-interleaved Digital-to-Analog Converter (TI-DAC) for Self-Interference-Cancellation Applications

November 2021

Mazyar Abedinkhan Eslami

The need for higher data-rate is constantly growing to enhance the quality of the daily communication services. The full-duplex (FD) communication method has the potential for doubling the data-rate compared to the half-duplex one. However, part of the strong output signal of the transmitter interferes with the receiver because they share the same antenna with limited attenuation and, as a result, the receiver's performance is corrupted. Hence, it is critical to remove the leakage signal from the receiver by designing another block called self-interference cancellation (SIC). *The main goal of this dissertation is to develop the SIC block embedded in the current-mode FD receivers*.

To this end, the regenerated cancellation current signal is fed to the inputs of the base-band filter located after the mixer of a (direct-conversion) current-mode FD receiver. Since the pattern of the transmitter (the digital signal generated by the DSP) is known, a high-speed digital-to-Analog converter (DAC) with medium-resolution can suppress the main part of the leakage on the receiver path. A capacitive DAC (CDAC) is chosen among the available architectures because it is compatible with advanced CMOS technology for high-speed and the medium-resolution applications. Although

`

the main goal of the design is to perform the SI cancellation, it can also be employed as a stand-alone DAC in the Analog (I/Q) transmitter. The SIC circuitry includes a trans-impedance amplifier (TIA), two DACs, high-speed digital circuits, and built-in-self-test section (BIST).

According to the available specification for full-duplex communication system, the resolution and working frequency of the CDAC are calculated to be equal to 10-bit (3 binary+ 2 binary + 5 thermometric) and 1GHz, respectively. To relax the design of the TIA (settling time of the DAC), the CDAC is implemented using a 2-way time-interleaved (TI) approach (bringing the effective SIC frequency to 2GHz) without using any calibration technique. The CDAC is also developed with the split-capacitor technique to lower the negative effects of the conventional binary-weighted DAC. By adding one extra capacitor on the left-side of the split-capacitor, LSB-side, the value of the split-capacitor can be chosen as an integer value of the unit capacitor. This largely enhances the linearity of the CADC and cancellation performance.

When the block works as a stand-alone DAC in non-TI mode, for a digital input code representing around 10.74MHz Sinusoid with an amplitude 1dB below full-scale the ENOB, SINAD, SFDR, and output signal are 9.4-bit, 58.2dB, 68.4dBc, and -9dB, respectively. The simulated value of the $|DNL|$ (*static linearity*) is less than 0.7. When operating in the SIC mode, the capacitive-array woks in the TI mode and cancellation current is set to full-scale. For this case, the SNDR, SFDR, SNDRequ. are 51.3dB, 15.1dB, 24dBc, 66.4dB, respectively.

The layout was optimally drawn to minimize both non-linearity and power-consumption of the decoders, and to reduce the complexity of the DAC. By distributing the thermometric cells across the array and using symmetrical switching scheme, the DAC is less subjected to the linear gradient effect of the oxide. Based on the post-layout simulation results, the deviation of the design after drawing the layout is studied. To compare the results of schematic and post-layout designs, the same

`

simulation conditions are used for both cases. From post-layout simulations when the block works as a stand-alone CDAC, the ENOB, SINAD, SFDR are 8.5-bit, 52.6dB, 61.3dBc, respectively. The simulated value of the $|DNL|$ (*static linearity*) is limited to 1.3. Likewise, the SI signal at the output of the TIA, SNDR, SFDR, SNDR$_{\text{equ.}}$ are equal to 44dB, 11.7dB, 19dBc, 55.7dB, respectively.

`

Acknowledgements

I certainly have a lot of people to thank but not enough space for all of them. However few people have significantly contributed to my development and this little space is for them.

First, I want to thank my advisor and co-advisor professors Danilo Manstrertta and Rinaldo Castello, respectively, for their guidance through all these years and for the countless challenging talks about electronics.

I'm also very grateful to Gennaro Dimeo, student at University of Naples Federico II, for his great support to create the high-speed digital interface to test my chip.

I want to thank all my Ph.D. colleagues and in particular Arianna Coccia and Nicola Cordioli for helping to deal with my technical or common issues at the lab.

I am also very grateful to my family who never leave me alone and always financially and morally support me. Finally, I would like to also honour the following people

- My mother: I cannot explain *her countless support* and kindness.
- My deceased father: He could understand me, and *I heavily miss him*.
- My deceased grandparents: They trained me when I was a child and support me to have a good life.
- My uncle: He has given me great advice and *always is available*.
- My lovely aunt: She financially supported me to *finish my Doctoral degree* in the Corona era.
- My deceased Cousin: Although she was too ill, she never gave up.
- Dr. Naserniya. I could not have enough time to appreciate him because he passed away when I was younger but his contribution on my happiness is undeniable.

`

Table of Contents

List of Figures ..... **ix**

Abbreviation ..... **iv**

List of Tables ..... **viii**

1 Introduction **2**

1.1 Duplex Communication Systems **3**

1.2 Motivation **4**

1.3 Organization of this Dissertation **5**

2 The FD Transceivers and Self-Interference-Cancellation (SIC) Schemes **7**

2.1 Transceivers **7**

2.2 Linearity Definition **8**

2.2.1 One-tone Test 9

2.2.2 Two-tone Test 10

2.3 Transmitters **12**

2.3.1 Transmitter architecture 13

2.3.2 Transmitter Noise 14

2.3.3 Transmitter Linearity 15

2.4 Full-duplex Current-mode Receivers **15**

2.4.1 Current-mode Receivers 16

2.4.2 Receivers' Sensitivity 17

2.4.3 Blocking Profile 18

2.4.4 ADC Dynamic's Parameters 18

2.5 Self-interference Cancellation (SIC) **19**

2.5.1 Generic method of the SICs 21

2.5.2 SIC Practical Points 23

2.5.3 State-of-the-art SIC Scheme 25

2.6 Proposed Canceller **27**

2.6.1 RF Design's Parameters 29

2.6.2 Developed SIC 29
2.6.3 Proposed SIC Constituent Blocks 30
3 Trans-impedance Amplifier (TIA) 35
3.1 The Background Information 35
3.1.1 Feedback Network 36
3.1.2 Input RC 36
3.1.3 Frequency Domain's Issues of the TIA and OTA 38
3.2 Calculating the Frequency Domain Parameters 45
3.2.1 System-level Design 45
3.2.2 Poles and Zeros arrangement 48
3.3 Transistor-level Design of the OTA 49
3.3.1 First Stage (St1) 50
3.3.2 Second Stage (St2) 52
3.3.3 Feedforward Stage (StFF) 53
3.3.4 Third Stage (St3) 54
3.4 Simulation Results of the TIA 55
3.4.1 Testing the Stability of the TIA 56
3.4.2 Evaluating the Settling-time 58
3.4.3 Noise of the TIA 60
3.4.4 Input Impedance of the TIA 62
3.4.5 TIA operating points 62
4 Capacitive DAC (CDAC) 64
4.1 Theoretical Background 64
4.1.1 Ideal DAC Response 64
4.1.2 NRZ and RZD DAC 65
4.2 Performance Figure-of-the-merits 68
4.2.1 Quantization Noise 68
4.2.2 Oversampling Effect 68
4.3 Capacitive Array 69
4.3.1 CDAC Structure 69
4.3.2 Segmentation Technique 71
4.3.3 Switching Scheme of the CDAC 72

4.3.4 SC DAC Working Phases in the SIC Mode 74
4.3.5 Practical Points 75
4.3.6 Matching 77
4.3.7 Delay between the SI's and SIC's signals 79
4.4 Time-Interleaved (TI) 80
4.4.1 Mismatch between Sub-DACs 81
4.4.2 Analysis of the Transfer-function with non-ideality 83
4.5 Noise of the Capacitive-array 84
4.5.1 Noise Analysis 84
4.5.2 Noise Analysis of the developed CDAC 85
4.6 Digital Circuit 87
4.6.1 Using Hardware Description Language 88
4.6.2 CDAC Local Controller 88
5 The CDAC and SIC simulation and Layout 92
5.1 Manually Designed Block 92
5.1.1 Digital Interface (Pattern Generator) 94
5.1.2 Capacitive-array 94
5.1.3 TIA 94
5.1.4 Simulation Assumptions 95
5.2 Stand-Alone CDAC 96
5.2.1 CDAC Static Specification 97
5.2.2 The CDAC Dynamic Specification 98
5.3 SIC (Mode 4) 99
5.3.1 Cancellation 100
5.3.2 Loading Effect of the LNA 101
5.4 Chip Level 101
5.4.1 Extra Sub-blocks 102
5.5 Layout-level 104
5.5.1 Floor-planning 104
5.5.2 The Capacitive Array 105
5.5.3 Thermometric Configuration 106
5.5.4 MOM Capacitor 107

5.5.5 The Layout of the whole Chip 107
5.5.6 Post-layout Simulation 109
Conclusion 112
References 114

`

List of Figures

FIGURE 1-1 THE TECHNOLOGY TRENDS OF WIRELESS COMMUNICATION SYSTEMS [1]. 2
FIGURE 1-2 TRANSMISSION AND RECEPTION OF DATA IN (A) TIME DIVISION MULTIPLEXING (TDD) (B) FREQUENCY DIVISION DUPLEXING (FDD) AND (C) IN-BAND FULL-DUPLEX (IBFD). 3
FIGURE 2-1 BLOCK DIAGRAM OF A DIRECT-CONVERSION WIRELESS TRANSCEIVER [2]. 8
FIGURE 2-2 A SINGLE-TONE TEST OF A MEMORYLESS BLOCK [3]. 9
FIGURE 2-3 (A) TWO-TONE TEST OF A MEMORYLESS BLOCK (B) THE DEFINITION OF SECOND AND (IIP2) (C) THE DEFINITION OF THIRD-ORDER INTERCEPT POINTS (IIP3) [3]. 11
FIGURE 2-4 GENERIC BLOCK DIAGRAM OF A DIRECT-CONVERSION I/Q TRANSMITTER (A) ANALOG-INTENSIVE AND (B) DIGITAL-INTENSIVE [6]. 13
FIGURE 2-5 BLOCK DIAGRAM OF A SAW-LESS DIRECT-CONVERSION CURRENT-MODE RECEIVER [8]. 16
FIGURE 2-6 IB AND OOB PROFILE OF BLOCKERS FOR A 5 MHZ LTE SYSTEM [10]. 18
FIGURE 2-7 GENERIC VIEW OF A FD LINK SUBJECTED TO THE VARIOUS KINDS OF SIS [12]. 20
FIGURE 2-8 AN EXAMPLE OF DEGRADING THE PERFORMANCE OF RX DUE TO PRESENCE OF THE SI IN A FD RADIOS [4]. 21
FIGURE 2-9 GENERIC VIEW OF A SIC IN A FD LINK, SIGNAL IS TAPPED FROM VARIOUS POINTS IN THE TX PATH AND INJECTED TO DIVERSE POINTS IN THE RECEIVER [12]. 22
FIGURE 2-10 THE FD TRANSCEIVER INCLUDING THE ANALOG BASEBAND SIC A VECTOR-MODULATOR DOWN-MIXER [13]. 25
FIGURE 2-11 THE FD SIC ARCHITECTURE WITH THE DUAL-INJECTION PATHS [4]. 26
FIGURE 2-12 IMPLEMENTING THE FD RECEIVER WITH FINITE FIR AND INTEGRATED RF AND BB CANCELERS [14]. 27
FIGURE 2-13 THE PROPOSED SIC FD TRANSCEIVER USED IN THE DIRECT-CONVERSION CURRENT-MODE RECEIVER. 28
FIGURE 2-14 THE ILLUSTRATION OF THE LINK BUDGET OF A FD COMMUNICATION SYSTEM ACCORDING TO THE SPECIFICATION MENTIONED IN TABLE 2-2. 31
FIGURE 3-1 (TOP) OOB BLOCKERS (BOTTOM) CONVENTIONAL TIA STRUCTURE [21]. 36
FIGURE 3-2 AMPLIFYING NOISE OF AN OTA BY C_Z NOISE, SINGLE-ENDED MODEL [21]. 38
FIGURE 3-3 LINEAR MODEL OF THE UNITY-GAIN CONFIGURATION OF AN AMPLIFIER TO INVESTIGATE THE NEGATIVE EFFECT OF A DOUBLET ON THE SETTLING TIME [27]. 40
FIGURE 3-4 TIME DOMAIN ANSWER OF AN UNITY-GAIN AMPLIFIER, FIGURE (3-3) , TO SHOW DOUBLET SLOW AND FAST-SETTLING COMPONENTS' BEHAVIOURS [28]. 41
FIGURE 3-5 (A) CONCEPTUAL DIAGRAM OF A MULTIPATH FEEDFORWARD OTA (B) GAIN AND PHASE DEMONSTRATION [29]. 42
FIGURE 3-6 SINGLE-ENDED MODEL FOR CREATING A ZERO BY FEEDFORWARD TECHNIQUE [26]. 44
FIGURE 3-7 SINGLE-ENDED BLOCK DIAGRAM OF THE ANALOG SECTION [16]. 46
FIGURE 3-8 SINGLE-ENDED MODEL OF THE DEVELOPED OTA [16], [30]. 47
FIGURE 3-9 THE AMPLITUDE OF TRANSFER FUNCTION G-LOOP OF THE TIA EMPLOYED THE TWO POLES/ ONE ZERO COMPENSATION TECHNIQUE. 48
FIGURE 3-10 (A) FIRST STAGE OF THE DEVELOPED OTA (ST1) AND (B) THE DIMENSIONS OF THE TRANSISTORS. 50
FIGURE 3-11 (A) SECOND STAGE (ST2) OF THE DESIGNED OTA AND (B) TRANSISTORS' DIMENSIONS. 53
FIGURE 3-12 (A) FEEDFORWARD STAGE PLACED BETWEEN INPUT OF THE OTA (AC-COUPLED BIAS) AND THE OUTPUT OF THE SECOND-STAGE AND (B) THE TRANSISTORS' DIMENSIONS. 54
FIGURE 3-13 (A) THIRD STAGE OF THE OTA IMPLEMENTED AS A CLASS AB AMPLIFIER AND (B) TRANSISTORS' DIMENSIONS. 55
FIGURE 3-14 THE TEST-BENCH FOR EVALUATING THE OPEN-LOOP PERFORMANCE. 56
FIGURE 3-15 G-LOOP GRAPH OF THE TIA ACCORDING TO THE TEST-BENCH ABOVE (A) MAGNITUDE IN DB AND (B) PHASE RESPONSE IN DEGREE. 57

`

FIGURE 3-16 COMMON-MODE SIMULATION RESULT OF THE TEST-BENCH SHOWN IN FIGURE 3-14 (A) AMPLITUDE IN DB AND (B) PHASE RESPONSE IN DEGREE. 58
FIGURE 3-17 THE TEST-BENCH USED FOR MEASURING THE SETTLING TIME. 58
FIGURE 3-18 SMALL-SIGNAL SETTLING-TIME RESPONSE OF FIGURE 3-17. 59
FIGURE 3-19 LARGE-SIGNAL SETTLING-TIME RESPONSE OF FIGURE 3-17. 60
FIGURE 3-20 TIA'S OUTPUT NOISE OF THE VS. FREQUENCY RANGE LOWER THAN 100MHZ. 61
FIGURE 3-21 NOISE BREAKDOWN OF THE TIA'S INPUT-REFERRED-NOISE. 62
FIGURE 3-22 (ORANGE COLOUR) TOTAL INPUT IMPEDANCE OF THE TIA AND (BLUE COLOUR) SHOWS THE IMPEDANCE SEEN AFTER RZ INCLUDING FB. 63
FIGURE 4-1 RESPONSE OF A NRZ DAC, THE (A) TIME AND (B) FREQUENCY DOMAIN [31]. 65
FIGURE 4-2 AMPLITUDE OF A NRZ SAMPLE-AND-HOLD IN THE FREQUENCY DOMAIN [32]. 67
FIGURE 4-3 MODIFIED VERSION OF A CONVENTIONAL SPLIT-CAPACITOR CDAC, SIGNAL-ENDED SCHEMATIC [16]. 70
FIGURE 4-4 (A) SCHEMATIC OF A SC UNIT CELL (B) TWO NON-OVERLAPPING CLOCK [39]. 73
FIGURE 4-5 CHARGING PHASE, *PCHR*, OF THE CDAC (SINGLE-ENDED VERSION) [16]. 74
FIGURE 4-6 DISCHARGING PHASE, *PDISCH*, OF THE CDAC (SINGLE-ENDED VERSION) [16]. 75
FIGURE 4-7 1000-RUN MONTE-CARLO TO SHOW VARIATION OF THE UNIT CAPACITANCE. 79
FIGURE 4-8 ANALYSING THE TIMING MISMATCH IN THE SIC MODE (A) SIC WITH THE LIMITED CANCELLATION(B) PERFECTLY SIC (C) THE SI AND SIC HAVE THE SAME AMPLITUDE BUT WITH THE DELAY. 80
FIGURE 4-9 CONCEPTUAL DIAGRAM OF 2-WAY TIME-INTERLEAVED DAC (A) TWO OUT-OF-PHASE CLOCKS (B) TWO-WAY TI DACS (C) CREATING THE ANALOG OUTPUT AT F0=2/TCLK [42]. 81
FIGURE 4-10 EQUIVALENT SINGLE-ENDED NOISE MODEL OF THE CDAC IN THE CHARGING PHASE, *PCHR*. 86
FIGURE 4-11 EQUIVALENT SINGLE-ENDED NOISE MODEL OF THE CDAC IN THE DISCHARGING PHASE, *PDISCH*. 87
FIGURE 4-12 NON-OVERLAP CLOCK GENERATOR [52]. 89
FIGURE 4-13 CLOCK DISTRIBUTION INSIDE THE CHIP [52]. 90
FIGURE 4-14 THERMOMETRIC CELLS (MATRIX) DECODER INCLUDING THE HIGH-SPEED LATCH [53]. 90
FIGURE 5-1 BLOCK DIAGRAM OF THE *MANUALLY DESIGNED BLOCK* INCLUDING IN & OUT. 92
FIGURE 5-2 WORKING MODE ILLUSTRATION. 93
FIGURE 5-3 TEST-BENCH FOR MEASURING THE PARAMETERS OF THE CDAC IN MODE 2^{ND} AND 3^{RD}. 96
FIGURE 5-4 TIME-DOMAIN RESPONSE OF THE WORKING MODE 2 (2) DIFFERENTIAL VOLTAGE ACROSS THE (A) OTA'S VIRTUAL GROUND AND (B) TIA'S OUTPUT 97
FIGURE 5-5 DNL OF THE 10-BIT CDAC IN THE WORKING MODE 2^{ND}. 97
FIGURE 5-6 OUTPUT (BEFORE IDEAL LPF) SPECTRUM OF THE CDAC IN 2^{ND} MODE. 98
FIGURE 5-7 THE SIC TEST-BENCH. THE LEAKAGE SIGNAL IS FED TO THE RED ARROWS. 99
FIGURE 5-8 THE TIA'S OUTPUT SPECTRUM AFTER PERFORMING LESS THAN -40DB CANCELLATION. 100
FIGURE 5-9 FREQUENCY RESPONSE OF THE OUTPUT BUFFER (A) AMPLITUDE IN DB (B) PHASE IN (°). 102
FIGURE 5-10 PROGRAMMABLE DELAY (A) THE DELAY BETWEEN ORIGINAL CLOCK AND PREPARED DATA BY *HDL PART* AND (B) AMOUNT OF 3-BIT DELAY. 103
FIGURE 5-11 (A) TOP-LEVEL OF THE CHIP AND PADS' LOCATION (B) FLOOR-PLANNING OF THE *MANUALLY DESIGNED BLOCK*. 105
FIGURE 5-12 THE FLOOR-PLANNING OF THE 10-BIT CDAC, 3BIN-W+2BIN-W+5THCO, ALONG WITH THE EXTRA CAPACITORS AND DUMMY LOADS [53], [57]. 106
FIGURE 5-13 THERMOMETRIC CELLS DISTRIBUTION (MATRIX) TO REDUCE THE PROCESS ERRORS [53]. 106
FIGURE 5-14 ILLUSTRATION OF THERMOMETRIC CONFIGURATION FOR THE CODE EQUIVALENT 17. 107
FIGURE 5-15 M*ANUALLY DESIGNED BLOCK* OF THE CHIP INCLUDING THE TIA AND CDAC. 108
FIGURE 5-16 THE LAYOUT OF THE WHOLE CHIP INCLUDING BIST AND ANALOG PART. 108
FIGURE 5-17 THE OPEN-LOOP FREQUENCY RESPONSE OF THE TIA BEFORE (RED) AND AFTER (BLUE) DRAWING THE LAYOUT (A) PHASE IN DEGREE (B) AMPLITUDE IN DB. 109
FIGURE 5-18 DNL POST-LAYOUT SIMULATION OF THE CDAC IN 2^{ND} MODE. 110

`

Abbreviation

Vehicle-to-everything	**V2X**
Half-frequency-duplex	**HD**
Full-duplex	**FD**
Transmitter	**TX**
Receiver	**RX**
Time-division duplexing	**TDD**
Frequency domain duplex	**FDD**
Self-interference	**SI**
Signal-to-noise ratio	**SNR**
Self-interference cancellation	**SIC**
Digital-to-analog	**DAC**
Digital-signal-processor	**DSP**
In-phase	**I**
Quadrature-phase	**Q**
Sinc Function	$\frac{Sin(x)}{x}$
Baseband	**BB**
Low-noise amplifier	**LNA**
Analog-to-digital converter	**ADC**

`

Radio-frequency	**RF**
Spurious-free dynamic range	**SFDR**
Second intercept point	**IP2**
Third intercept point	**IP3**
Power amplifier	**PA**
In-band	**IB**
Out-of-band	**OOB**
Oversampling ratio	**OSR**
Bandwidth	**BW**
Surface acoustic wave	**SAW**
Low-noise transconductance amplifier	**LNTA**
Trans-impedance amplifier	**TIA**
Noise figure	**NF**
Minimum detectable signal	**MDS**
Dynamic range	**DR**
Effective-number-of-bits	**ENOB**
Signal-to-noise-distortion	**SNDR**
Printed circuit board	**PCB**
Finite impulse response	**FIR**
operational-transconductance amplifier	**OTA**
Input referred noise	**IRN**

`

Complementary-metal-oxide-semiconductor	**CMOS**
Nested-miller-compensation	**NMC**
Gain-bandwidth-product	**GBW**
No-capacitor feedforward	**NCFF**
Right-half-plane	**RHP**
Left-half-plane	**LHP**
Common-mode-feedback	**CMFB**
High-passed-filter	**HPF**
Feedback	**FB**
Non-return-to-zero	**NRZ**
Return-to-zero	**RZ**
Zero-order-hold	**ZOH**
Time-interleaved	**TI**
Most-significant-bit	**MSB**
Least-significant-bit	**LSB**
Binary-weighted	**Bin-W**
Thermometric-coded	**THco**
Switched-capacitor	**SC**
Power spectral density	**PSD**
Mean square	**MS**
Hardware description language	**HDL**

`

Built-in-self-test	**BIST**
Metal-oxide-metal	**MOM**
Metal-insulator-metal	**MIM**
Fast-Fourier-Transform	**FFT**
Continuous wave	**CW**
Low-pass filter	**LPF**

`

List of Tables

TABLE 2-1 COMPARISON TABLE BETWEEN ANALOG AND DIGITAL-INTENSIVE TRANSMITTERS [6]-[7] 14
TABLE 2-2 DESIGN (RF) PARAMETERS OF THE PROPOSED SIC. 28
TABLE 3-1 SUMMARY FORMULA OF THE NCFF TECHNIQUE. 44
TABLE 3-2 THE OPERATING POINTS AND SMALL SIGNAL PARAMETERS OF EACH STAGE OF THE OTA. 56
TABLE 3-3 SUMMARY SPECIFICATIONS OF THE TIA'S OPERATING POINTS. 63
TABLE 4-1 COMPARISON BETWEEN A NRZ AND RZ SAMPLE-AND-HOLD FUNCTION [31]-[32]. 66
TABLE 4-2 SUMMARY OF THE DEVELOPED CDAC [29], [38]. 72
TABLE 5-1 SUMMARY OF THE CHIP'S WORKING MODES. 93
TABLE 5-2 SUMMARY OF THE CDAC DYNAMIC SPECIFICATION IN WORKING MODE 2ND. THE OUTPUTS ARE REPORTED AFTER THE TA AND IDEAL LPF. 98
TABLE 5-3 SUMMARY OF SIC RESULTS WITH FULL-SCALE INPUT. 101
TABLE 5-4 SUMMARY OF SIC VS. TWO DIFFERENT LNA 'S OUTPUT IMPEDANCE. 101
TABLE 5-5 SUMMARY OF THE 2ND MODE SIMULATION WITH AND WITHOUT DELAY MODULE. 104
TABLE 5-6 SUMMARY OF THE TIA OUTPUT (BEFORE AND AFTER DRAWING THE LAYOUT) IN THE WORKING MODE 2. 110
TABLE 5-7 SUMMARY OF THE SIC BEFORE AND AFTER DRAWING THE LAYOUT, 4TH MODE. 111

`

1 Introduction

Nowadays, in 2021, it is impossible to conceive of life without advanced communication systems. Smartphones and tablets, for example, make our life different and the list of activities can be done with them are countless such as looking for the information on the Internet, consulting our emails, checking the news, watching streaming video, booking the ticket in our daily life. The evolution of wireless communication system is astoundingly fast; hence, it is generally acknowledged that the next generation of wireless communication systems enter diverse areas, from wirelessly connected vehicle-to-everything (V2X) to industrial manufacturing and health-care-sector [1]. However, these various services particularly need the data intensives ones. For example, a multimedia streaming led to a huge rise of the data traffic compared to the use of communication systems for traditional tasks like voice calls and text messages. The significant potential for the

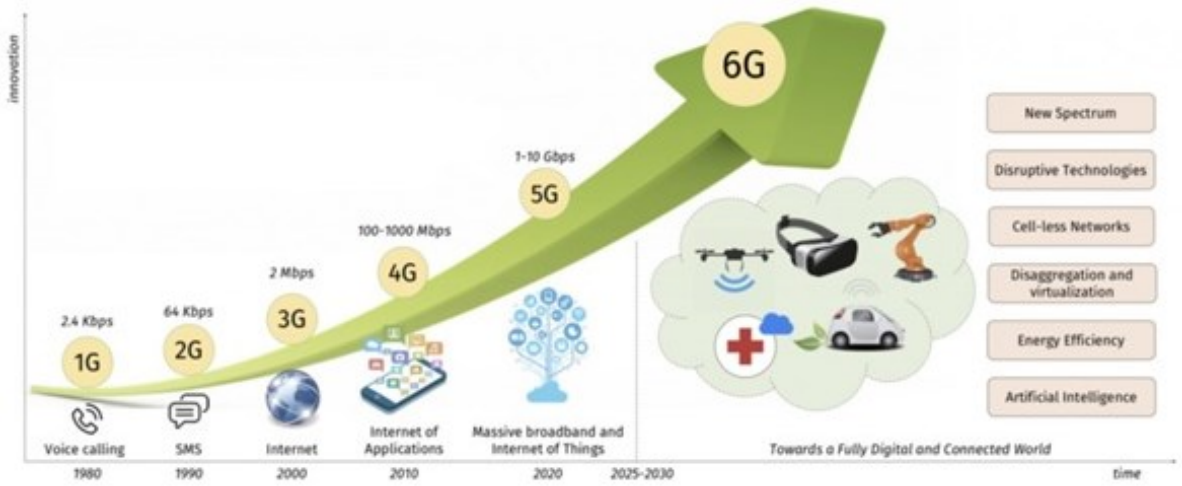


Figure 1-1 The technology trends of wireless communication systems [1].

`

speed and capacity of the wireless technology should be looked for in the somewhere else. Hence, it imposes special requirements on the communication systems' infrastructure and networks [1]. The visual technology tends of wireless communication systems, from *1G* to *6G* standards, is visually shown in Figure 1-1.

1.1 Duplex Communication Systems

The term duplex refers to the capability of a communication system to transmit and receive the data simultaneously or one at a time. There are two kinds of duplex communication systems, namely half-frequency-duplex (HD) and full-duplex (FD). With HD mode, the data can just transfer data in one direction at one time slot. Each transceiver merely has one antenna in wireless communication systems shared between transmitter (TX) and receiver (RX). On the other hand, simultaneous transmission and reception on the same channel is defined as full-duplex method. The essential characteristics of different duplexing methods are shown in Figure 1-2. Time-division duplexing (TDD) and frequency domain duplex (FDD), which is sometimes referred to as out-of-band FD and uses two different frequencies for transmission and reception, shown in Figure 1-2 (a) and (b), respectively. There is a frequency gap between the RX and TX paired to allow simultaneous transmission on two frequencies. The bands also have an enough separation to enable the transmitted

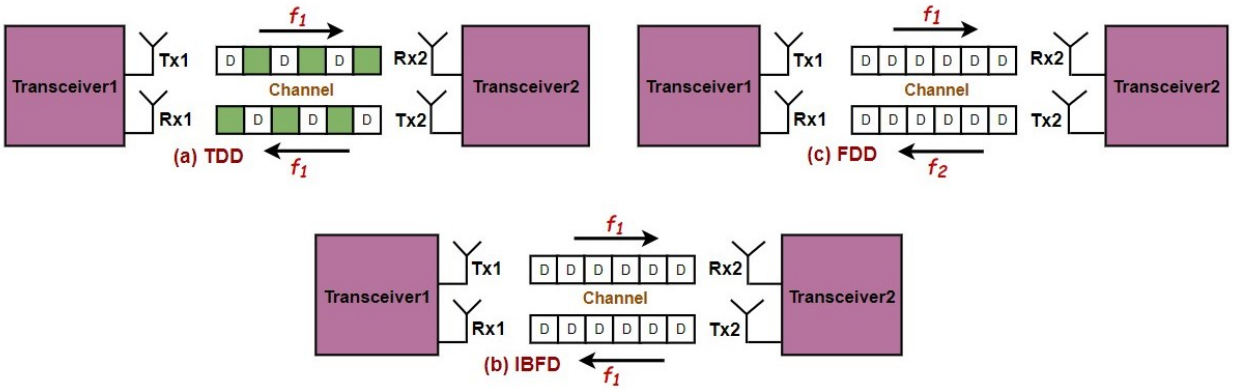


Figure 1-2 Transmission and reception of data in (a) time division multiplexing (TDD) (b) frequency division duplexing (FDD) and (c) in-band full-duplex (IBFD).

signals not to excessively impair the RX performances. The separation must be sufficient to allow the roll-off of the antenna filtering to attenuate the transmitted signal within the receive band [2]-[3]. Both schemes work in the HD mode, where the separation of the sent and received signals of a single user in either time or frequency leads to inefficient use of limited wireless resources. The out-of-band noise of TX's FDD falls into RX band, its sensitivity and noise-figure will be degraded as well [4]. By using the FD method, referred to in-band FD (IBFD) and shown in Figure 1-2 (c), the spectral efficiency obviously doubles due to simultaneous transmission and receipt of the data. Accordingly, the operators and industry are thus very willing to the IBFD technique. Besides, with a little change, it can be employed to any type of wireless standards.

1.2 Motivation

The wireless communication systems share the same medium, the air, to transmit and receive the data. The Tx signal will appear, attenuated part, at the own Rx chain, and eventually turning into a huge self-interference (SI) [3]. This SI dominates at the Rx path and all the desired signals are absolutely buried under this strong unwanted signal. Hence, it will degrade the signal-to-noise ratio (SNR) at the back end of the receiver, potentially eroding any enhancement in spectral efficiency. Without any attenuation of this SI, the IBFD operation, taking advantage of its benefit, is clearly impossible. The IBFD transceivers relies on cancellation techniques to suppress the SI. Active research has been carried out around the globe on to explore effective self-interference-cancellation (SIC) techniques. I have carried out a thorough theorical research and look for the practical realization way to remove SI in the RX side and utilize the theoretically doubling the capacity due to the full-duplex operation. By utilizing the power of modern sub-nanometer CMOS technology, a high-speed and high dynamic range capacitive digital-to-analog (DAC), a high-speed digital sequence

`

controller & built-in-self-test (BIST) circuits, and a power-full filter is developed to realize the SIC function for the current-mode FD receiver.

1.3 Organization of this Dissertation

This thesis plans to enlarge upon a new SIC method to eliminate the SI on RX to capitalize on the spectral efficiency of the FD method in current-mode receiver. The organization of the thesis is as follows.

Chapter 2 presents a background knowledge about the modern current-mode transceivers in the FD configuration. Then, the concept of the TX's signal leaks into the RX path is described, and three state-of-the-art articles are shortly mentioned. Finally, a system level analysis of the proposed SIC block is presented, some parameters are calculated, and its blocks are introduced.

Chapter 3 explains the major obstacles and the important blocks and points for developing the high-speed TIAs. Moreover, its sub-blocks, such as OTA's stages, are explained and designed. Finally, the TIA's performance, such as settling time and noise, is validated by using various kinds of simulations to satisfy the SIC block.

Chapter 4 first gives the necessary information about the DAC and its important figures-of-the-merits. Then, the used capacitive-array's structure and switching scheme are thoroughly explained. The concept of the time-interleaved method is mentioned (in this chapter) to boost the data rate. Finally, more explanations are given about the digital unit including the hardware-description-language and *manually designed logic* circuits.

Chapter 5 shortly re-explains each block, including the TIA and capacitive-array. The blocks must be connected to create the unit (design) and explore the design's simulation in the different working modes such as SIC and DAC. Next, the test-benches and simulation results of the design are presented in the schematic level.

`

Drawing the layout and special techniques to improve the performance of the design are explained in this chapter. The post-layout simulations are presented to compare the performance of the system after and before drawing the layout as a final explanation.

Conclusion explains the design achievements and how one can proceed with the results of the dissertation.

`

2 The FD Transceivers and Self-Interference-Cancellation (SIC) Schemes

This section includes background information about full-duplex (FD) transceivers and preliminary information with regard to the designed self-interference-cancellation (SIC). As mentioned in the previous section, in "Motivation" sub-section, the self-interference (SI) is the major bottleneck for using the full-duplex (FD) method in the wireless communication systems. This chapter also provides a background information about a (direct-conversion) current-mode transceivers building-blocks and some of their technical parameters. Moreover, the concept of the SIC is explained in more details along with a few state-of-the-art SIC designs. Finally, the proposed SIC and its blocks are presented according to design's parameters.

2.1 Transceivers

Among the available architectures for implementing the transceivers, *the direct-conversion architecture was chosen in my thesis*, and its block diagram is illustrated in Figure 2-1.

The TX block is shown in the bottom of Figure 2-1. The digital-signal-processor (DSP) unit creates the sequences of bits, and then they will be converted to Analog signal by employing the DAC. Afterwards, a low-pass filter (LPF) suppresses the high-frequency components to smooth the wanted signal. Quadrature up-conversion follows including two up-conversion paths called I/Q driven by in-phase (I) and quadrature- phase (Q) [2].

`

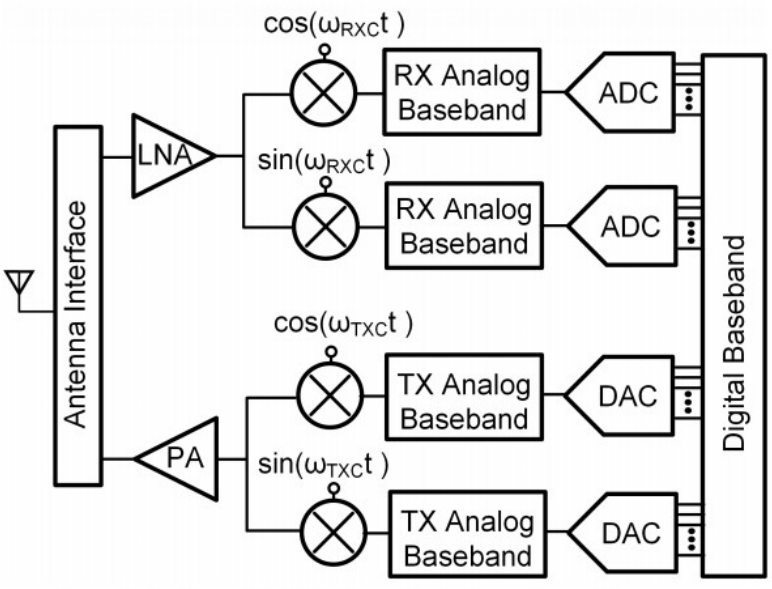


Figure 2-1 Block diagram of a direct-conversion wireless transceiver [2].

The receiver-side's functionality is reserved compared to the TX's one, as shown on the top of Figure 2-1. It is composed of a low-noise amplifier (LNA), quadrature down-conversion mixer, Analog BB circuitry involving variable-gain amplifier/ LPF, and Analog-to-digital converter (ADC) [2]. Because the local oscillator frequency is set exactly to its incoming radio-frequency (RF) signal, this architecture is called "*direct-conversion*". Likewise, the quadrature down-conversion of the receiver incorporates two down-conversion paths, namely I/Q. The received RF signal will be converted to the Analog BB, and then digitized to the digital BB, bit stream, by ADCs after passing through the consecutive stages. Hence, the Analog BB signal should not exceed the dynamic range of the ADCs.

2.2 Linearity Definition

The non-linearity of RF components plays a critical role in the communications systems, especially in the presence of interferes and large signals. To explore the linearity in more details, first the single-tone analysis is considered, and then two-tone analysis is mathematically analysed. The linearity is a broad topic which is vastly

`

discussed in the literatures for both transmitter and receiver sides, but it is out-of-scope of this thesis, and only short and useful information is presented here. To understand the effect of distortion and spectral regrowth, let us consider an amplifier with a memoryless characteristic as shown below.

2.2.1 One-tone Test

The linearity for one-tone signal is explained here. The relationship between the input and output is shown in Figure 2-2, and a memoryless block is represented by Taylor's series as follows:

$$y_o(t) = \alpha_0 + \alpha_1 x_{in}(t) + \alpha_2 x^2{}_{in}(t) + \alpha_3 x^3{}_{in}(t) + \cdots \quad \text{Eq. (2-1)}$$

where $x_{in}(t)$ is the input signal, $y_o(t)$ is the output signal ($y_o(t)$ *and* $x_{in}(t)$ are not necessarily voltage signal), α_1 can be referred to as the small signal gain of the component, and $\alpha_2, \alpha_3, \ldots, \alpha_i$ (other coefficients) represent the second and third and higher orders nonlinear coefficients. If the input signal has a small swing, we can neglect all the nonlinear coefficients such as α_2 and α_3. Increasing the amplitude of the input signal, $x_{in}(t)$, the large signal behaviour plays a key role in the characteristic of the output signal; hence, the effect of higher orders coefficients cannot be ignored anymore. The output gradually will be saturated in the certain input (voltage or power) so that the gain compression concept will be raised. For the sake of simplicity, the first three terms of Eq. (2-1) are used to study the non-linearity concept. Assuming

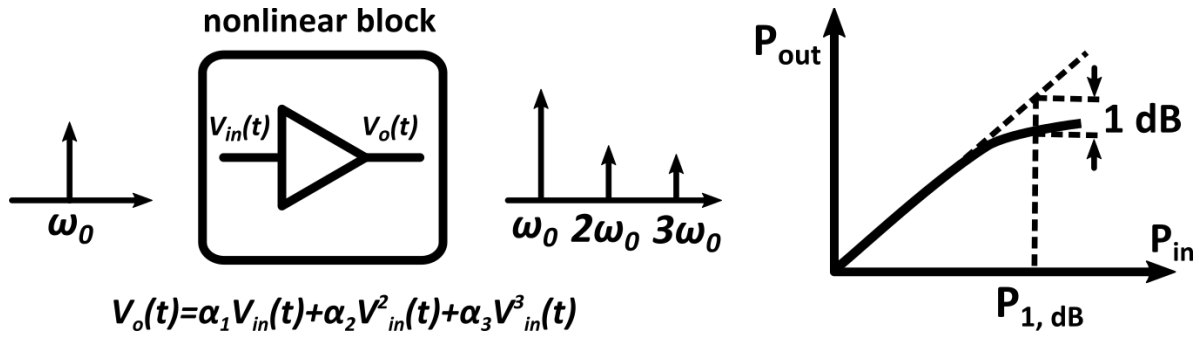


Figure 2-2 A single-tone test of a memoryless block [3].

`

a single-tone, continuous-wave, input signal, $x_{in}(t) = Acos(\omega_0 t)$, is passing through the nonlinear device, the output can be expressed as:

$$y_o(t) = \alpha_0 + \alpha_1 Acos\,\omega_0 t + \alpha_2 A^2 cos^2\omega_0 t + \alpha_3 A^3 cos^3\omega_0 t + \cdots =$$

$$\alpha_0 + \frac{\alpha_2 A^2}{2} + \left(\alpha_1 + \frac{3\alpha_3 A^2}{4}\right) \times Acos\,\omega_0 t + \frac{\alpha_2 A^2}{2} cos2\omega_0 t + \frac{\alpha_3 A^2 \times A}{4} cos3\omega_0 t \quad \text{Eq. (2-2)}$$

The output signal of the nonlinear device shows multiple harmonics of the input frequency as shown in Eq. (2-2) [3]. The linear gain of the device, $\left(\alpha_1 + \frac{3\alpha_3 A^2}{4}\right)$, will not become constant anymore in such a case. A large signal behaviour would result in amplitude compression for $\alpha_1\alpha_3 < 0$, which is usually the case for most RF cases (the case of $\alpha_1\alpha_3 > 0$ is not considered here and called expansion). To get a feeling for the gain compression, the concept of 1-dB compression point was defined by engineers and researchers, P_{1dB}, as the input level that leads to the linear small-signal gain to drop by 1dB, illustrated in Figure 2-2 [3]. The single-tone spurious-free dynamic range (SFDR) is a good parameter to compare the linearity of different blocks and be defined as the ratio of the power of the input signal to the peak spurious in dB. The spurs can be caused at the harmonics of the input frequency due to non-linearities in the device, at subharmonics of the sampling frequency due to mismatch or so on. Another way for representing the SFDR is shown below.

$$SFDR = \frac{2}{3} \times (IIP_3 - MDS) \quad \text{Eq. (2-3)}$$

Where MDS and IIP3 represent the minimum discernible signal and third-order intercept point, respectively, which will be explained in more details below.

2.2.2 Two-tone Test

In the presence of strong interferences, the receiver should be sufficiently linear to avoid masking the wanted signal, for example, with the intermodulation products. When two interferes accompany the wanted signal at the input of one device such as mixer, LNA, or amplifier, the intermodulation products will be produced at the

`

output due to non-linearity effect of the device. If two interfere signals, in-band (IB) or out-of-band (OOB), at frequencies ω_1 and ω_2 are sensed by the nonlinear system, they will mix and make spurious signals at the output, that are not necessarily harmonics of these two frequencies, called intermodulation distortion (IMd). We assume a two-tone signal with the same amplitudes, A, shown in Figure 2-3 (a), appear at the input of a nonlinear amplifier, $V_{in}(t) = Acos(\omega_1 t) + Acos(\omega_2 t)$. To get a feeling, three first terms of formula Eq. (2-1) are considered like the one-tone test case; hence, $y_o(t)$ is calculated as shown below:

$$y_o(t) = \alpha_1 A_1 cos(\omega_1 t) + \alpha_1 A_1 cos(\omega_2 t) + \cdots + \alpha_2 {A_1}^2 cos(\omega_1 - \omega_2)\, t + \cdots$$

$$+ \cdots + \frac{3\alpha_3 A_1^3}{4} cos(2\omega_2 - \omega_1)\, t + \frac{3\alpha_3 A_1^3}{4} cos(2\omega_1 - \omega_2)\, t + \cdots \qquad \text{Eq. (2-4)}$$

Where some terms are neglected such as $2\omega_2 + \omega_1$ component since it is located out-of-band, the tones at $2\omega_2 - \omega_1$ and $2\omega_1 - \omega_2$ are called the third order intermodulation products (IM3) and the tone at $\omega_1 - \omega_2$ is the second order intermodulation product (IM2) [3]. Intermodulation products are problematic in RF

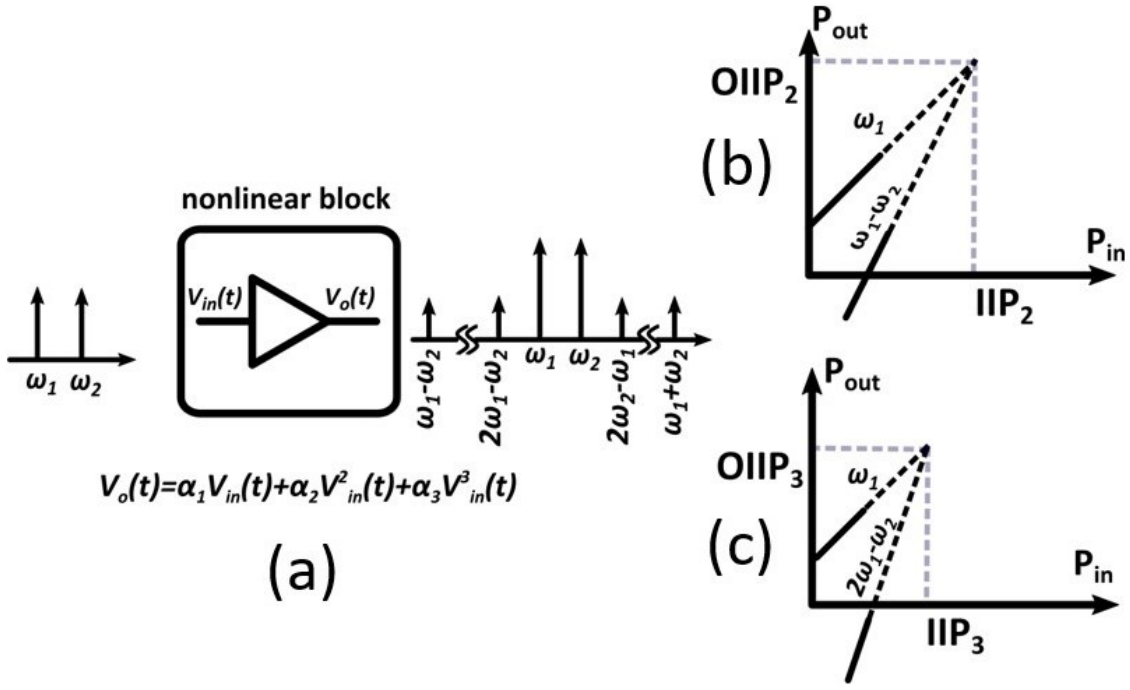


Figure 2-3 (a) two-tone test of a memoryless block (b) the definition of second and (IIP2) (c) the definition of third-order intercept points (IIP3) [3].

`

system for various kinds of reasons. The IM3 product, for example, gives additional in-band frequency content, called "spectral regrowth", which is close to the modulated signal, and will corrupt the quality of desire signal in the RX side. The designers make their effort to keep the IM3 level lower than a level defined by the communication standard and protocols during the circuit design. As shown in Figure 2-3 (c), the (figurative) point at which the IM3 intersects with the fundamental is referred to as third intercept point (IP3), expressed in Eq. (2-5) below [3].

$$P_{IIP3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|} \quad \text{Eq. (2-5)}$$

When it is referred to the input signal (power), is called Input IP3 (IIP3), however, if it is defined to the output one it is called Output IP3 (OIP3). Note that the third-order intercept point is achieved from an extrapolation, and it is an imaginary point since the input of the system cannot operated at that point (at relatively high-voltage or high-power levels). IP3 generally is around 10dB more than 1dB compression point. While the input signal rise by A, the IM3 will rise by A^3 in Figure 2-3. The IIP2 plot is also shown in Figure 2-3 (b). The extrapolated (figurative) point at which the second order distortion product meets the fundamental is called the Intercept point (IP2) and expressed as below [3].

$$P_{IIP2} = \frac{\alpha_1}{\alpha_2} \quad \text{Eq. (2-6)}$$

2.3 Transmitters

The function of the transmitter is to perform the Analog or digital modulation, frequency up-conversion, and act as an RF driver between the Analog BB and the antenna. The power amplifier (PA) is located at the end of TX chain, which amplifies the transmitted signal to the desired power level and provide necessary output matching between the antenna and PA. The TX should be capable of adjusting its output power to have relatively high peak-power along with a good efficiency. For example, the 802.11b WiFi standard delivers an output power up to level of +20dBm [

`

4]. Another important issue with regards to the transmitter is the non-linearity due to large signal operation.

Some important parameters of the transmitters are explained in the following sub-sections, there are still many other parameters which are out-of-scope of this dissertation.

2.3.1 Transmitter architecture

Transmitters' architecture divides up in two main categories, namely Analog (*Analog-intensive or conventional TX*) & digital-to-RF (*digital-intensive*) transmitters [5]. Their generic block diagrams (the direct-conversion I/Q architecture) are shown in Figure 2-4. The flexibility of an Analog-intensive direct-conversion transmitter, shown in Figure 2-4(a), is acquired by dividing the RF-signal generation into separate functional blocks such as DAC, Analog reconstruction filtering, up-conversion, and amplification. One of the disadvantages of the former is to take up a large silicon area, which does not necessarily comply with technology scaling. It also suffers from common issues of the Analog design in the deep sub-micro. However, it is still attractive for many designers due to its lower OOB noise compared to latter [6].

The intensive-digital transmitter, shown in Figure 2-4(b), moves one step toward the digital domain. The combining the digital signal processing and RF transmitter leads to new RF block. It is created by embedding the DAC and mixer as a one-unit cell. Table 2-1 reports the brief comparison between two architectures [6].

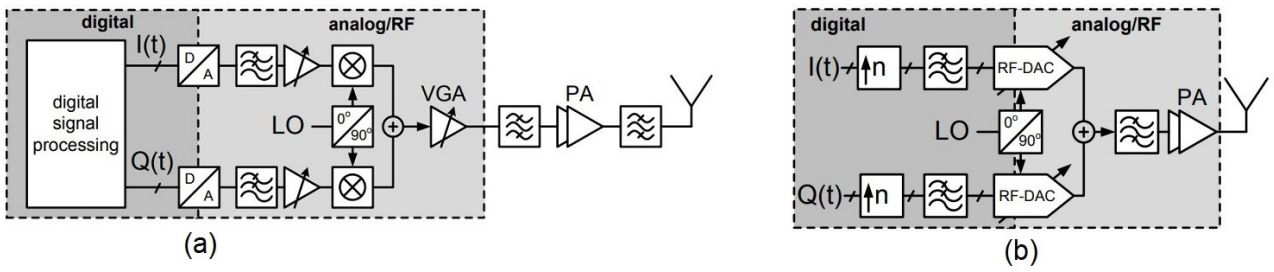


Figure 2-4 Generic block diagram of a direct-conversion I/Q transmitter (a) Analog-intensive and (b) digital-intensive [6].

If the Analog filter is removed from digital-intensive transmitter, Figure 2-4(b), the OOB emission level rise, because RF matching circuitry slightly eliminates the OOB frequency components and the digital images are just attenuated by the *zero-order-hold* characteristic of the *Sinc* $\left(\frac{\sin x}{x}\right)$ function. Besides, the quantization noise of the DAC degrades the output spectrum. The first issue will be addressed by increasing the oversampling ratio (OSR) which is not hard in the advanced CMOS technology. For tackling the second problem, raising the number of the bits of the DAC is the most straightforward way. One way to implement high-resolution DAC, whose the number of the bits is more than 14 [7], is capitalized on the delta-sigma modulator technique in the digital BB. It relaxes the design from the developing Analog power-consumed and sensitive blocks. Moreover, it is worth saying that developing such a high-speed digital BB is feasible due to the available advanced CMOS process [6].

2.3.2 *Transmitter Noise*

The noise of the TX mainly includes DAC's quantization/ thermal noise. Thermal noise of the quadrature modulator and the noise of BB's circuits also have contribution on the TX's output noise. It can degrade the performance of the RX in FDD/ FD receivers. For example, a 4G handheld device works with other radio standards, such as Bluetooth and Global Positioning System, if we desire to receive the bands of various radios the OOB noise of the LTE transmitter, as a one of restriction, must be low enough inside the RX bands in order to allow coexistence of various radios [2]. For

Table 2-1 Comparison table between Analog and digital-intensive transmitters [6]-[7]

Transmitter	Area	Flexibility	CMOS Scaling	Supply Voltage	Power Consume.	OOB noise
Analog-intensive	**High**	**Low**	**No**	**Relatively High**	**High**	**Relatively Low**
Digital-intensive	**Relatively low**	**High**	**Yes**	**Low**	**Low**	**Relatively high***

* For, example, *it can be lowered by using Delta-sigma modulator technique.*

`

giving us insight into a real system, a simple calculation is done here to obtain the noise in the output of the PA. Given a typical TX noise floor of −156dBc/Hz, the noise contribution from the PA can be ignored, and for a signal bandwidth (BW) of 20 MHz, the TX noise integrated over the signal BW is more than 80dB below the transmitted signals [2].

2.3.3 Transmitter Linearity

In high-performance wireless transceivers, transmitters can operate at a relatively high output power level and large signal mode. For example, the 802.11b WiFi standard, mentioned earlier, specifies the maximum TX output power up to +20dBm [2]. Hence, the non-linearity of transmitters is critical due to its large signal operation. The PA non-linearity causes two negative effects as follows:

1) The distorted signal is transmitted.
2) The leakage from the carrier channels into the neighbouring frequency channels because of spectral regrowth.

The transmitter's non-linearity accompanied by a wanted signal in the RX side (for instance, the LNA) leads to desensitization or it will degrade the RX's signal-to-noise ratio (SNR) , $SNR = \frac{P_{Signal}}{P_{Noise}}$ [8].

2.4 Full-duplex Current-mode Receivers

The wireless communication systems are surrounded by various kinds of RF signals and noise. The major duty of an RF receiver is to detect the desire signals among unwanted signals and noise sources without degrading the SNR of the wanted signals.

`

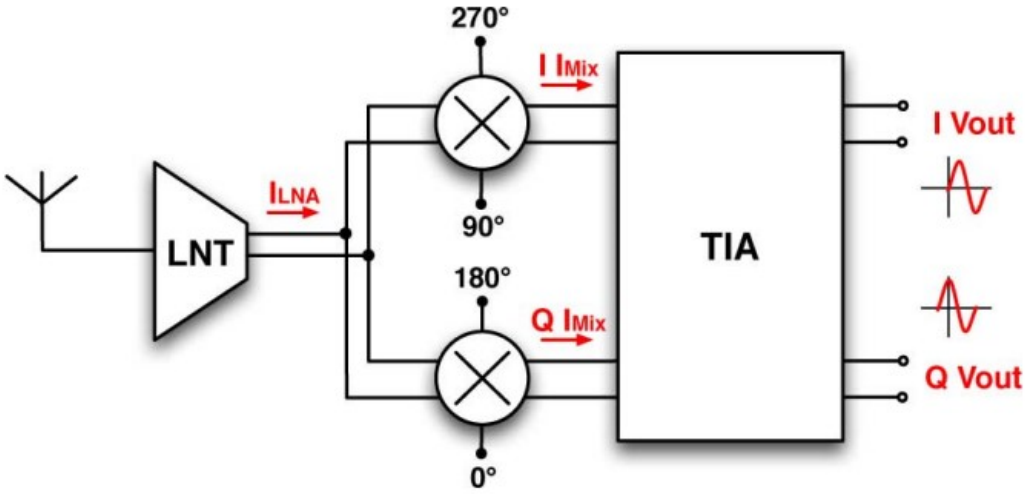


Figure 2-5 Block diagram of a SAW-less direct-conversion current-mode receiver [8].

High performance receivers employ external surface acoustic wave (SAW) filter to deal with the stringent blocking conditions in cellular radios. The SAW filters, on the other hand, are bulky and expensive, on the top of that, it is hard to implement them for the wide-band receivers [9]. Hence, the designers tend to remove the SAW filter in the RX path to implement SAW-less receivers as shown in Figure 2-5. *In the remaining chapters, it is assumed that the receiver configures like the SAW-less one*. Since the amount of OOB power exceeds the desired channel, the linearity of both front-end and digitizer generally becomes the major bottleneck for gaining the desired performance in the receivers, especially in SAW-less architectures, where there little or no RF filtering before the LNA. These non-linearities lead to cross-modulation products and some of them are folded-back into the wanted channel, which lowers the SNR. Accordingly, the excessive OOB blocking signal is a major issue in the SAW-less receivers [8]. In any case, the great benefit of the SAW-less receivers, motivates many designers and researchers to deal effectively with the mentioned issues.

2.4.1 Current-mode Receivers

The RF signal is picked up by the antenna and fed to the LNA with the output of this amplifier being current in the *current-mode receivers* instead of the voltage. Therefore, the front-end amplifier is called low noise transconductance amplifier (LNTA), some

`

of its specifications are like the LNA such as low noise, shown in Figure 2-5. The current signal, after the LNTA, passes through the 4-phase, I/Q mixer and is finally converted into voltage by the trans-impedance amplifier (TIA). The great advantages of the current-mode receivers are listed below:

1) The linearity of the LNTA, and the whole receiver, is improved due to less voltage swing on the receiver's nodes.
2) The power-consumption could be lowered.
3) The design is suitable for wide-band applications, but the power-consumption will probably be escalated in this condition.
4) This scheme can work on higher frequency compared to the voltage mode receivers.

This scheme is chosen in this dissertation due to the mentioned advantages.

2.4.2 *Receivers' Sensitivity*

In the receivers, the capability of detecting a weak signal in the presence of noise is quantified through RX's sensitivity [2]. The thermal noise is uniformly distributed across frequency spectrum and expressed in dB below.

$$P_{Thermal-Noise} = 10 \times \log_{10}(K_B \times T \times BW) \quad \text{Eq. (2-7)}$$

where K_B is the Boltzmann constant, T is the absolute temperature expressed in Kelvin, BW is the channel's BW. The IB noise of the receiver is calculated by adding the receiver noise-figure (NF) to the thermal noise's formula Eq. (2-7), defined by the Eq. (2-8) below. Then, the power of the noise floor is defined in the formula (2-9). It is important to add that the NF and $P_{Noise\text{-}floor}$ are usually expressed in dB.

$$NF = \frac{SNR_{Out}}{SNR_{in}} \quad \text{Eq. (2-8)}$$

$$P_{Noise-floor} = P_{Thermal-Noise} + NF = -174\frac{dBm}{HZ} + 10 \times Log_{10}(BW) + NF \quad \text{Eq. (2-9)}$$

`

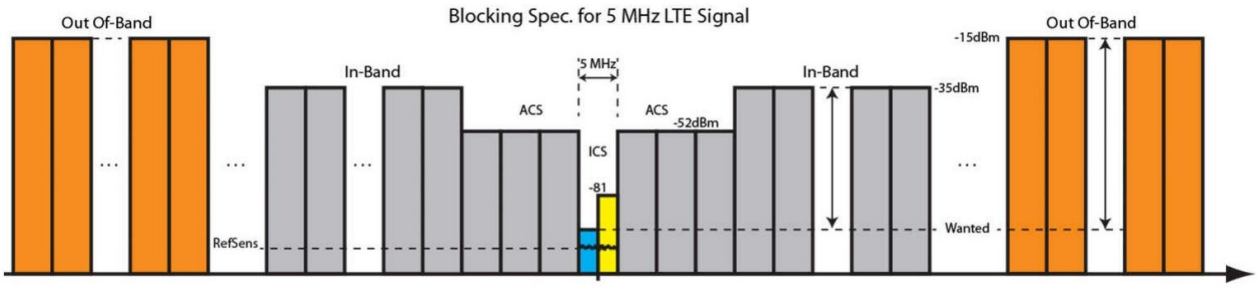


Figure 2-6 IB and OOB profile of blockers for a 5 MHz LTE system [10].

Finally, the sensitivity of the receiver is represented as the minimum detectable input (referred to antenna) power of the signal, P_{sens}, with acceptable signal quality. The minimum detectable signal (MSD) is given by formula (2-10).

$$P_{Sens} = MDS = P_{Noise-floor} + SNR_{min} \quad \text{Eq. (2-10)}$$

Where SNR_{min} is referred to a given output SNR approved by the communication standard and modulation's type to detect the signal [3].

2.4.3 Blocking Profile

The blocking characteristics describes the RX capability to detect a wanted signal at its allocated channel in the presence of an interferer. While OOB blockers' power are high, can be up to 0dBm, the IB blockers are generally very low power modulated signal. The blocking profile for a 5 MHz LTE is provided by the 3GPP and shown in Figure 2-6 [10].

2.4.4 ADC Dynamic's Parameters

In the noisy environment with many unwanted signals, the dynamic range (DR) of the ADC plays a key role to quantize the desired signal. As an example, a dynamic range of 60dB is needed for an ADC to detect 64-QAM signal in a WiFi transceiver, of which about 30dB is for SNR and another 30dB for various kinds of the margins [2].

The DR is defined as a difference between minimum and maximum input signal of a block, represented with Eq. (2-11).

`

$$DR = P_{Max} - P_{Min} \qquad \text{Eq. (2-11)}$$

The upper (P_{Max}) and lower (P_{Min}) are expressed as the maximum power in a block without clipping and the minimum detectable signal such as the minimum detectable signal (MDS) in the RX side, respectively. As an example, the LTE's signal profile is shown in Figure 2-6. The DR of the receiver should be high enough to detect a desired signal in presence of the IB and OOB blockers.

The SNR defines the performance of an ADC when the quantization noise is just considered (The SNR is expressed in dB), and other sources of noise are excluded (without any oversampling and noise shaping techniques).

$$SNR = 6.02 \times N + 1.72 \qquad \text{Eq. (2-12)}$$

Were *N* being the number of bits in the ADC. Another important parameter of an ADC is effective-number-of-bits (ENOB). It signifies the useful number of bits in the presence of noise and distortion. The ENOB to closely related to signal-to-noise-distortion (SNDR), defined below (the SNDR is expressed in dB).

$$ENOB = \frac{SNDR - 1.76}{6.02} \quad \text{Eq. (2-13)}$$

2.5 Self-interference Cancellation (SIC)

The Leakage from TX path can pass through different paths to RX chain in the FDD/FD transceivers and is called Self-Interference (SI). The similar phenomenon happens in a closed-loop stimulation and recording, in the neuroscience [11]. After stimulation of the brain tissue and cortex, the weak signals should be recorded to see the corresponding response of it, but the artifacts severely degrade recording performance due to high amplitude of the artifacts [11].

Various kinds of SI are classified [12] and are shown in Figure 2-7.

1) A direct-coupling path such as through chip's substrate or printed circuit board (PCB) lead to crosstalk between TX and RX.

`

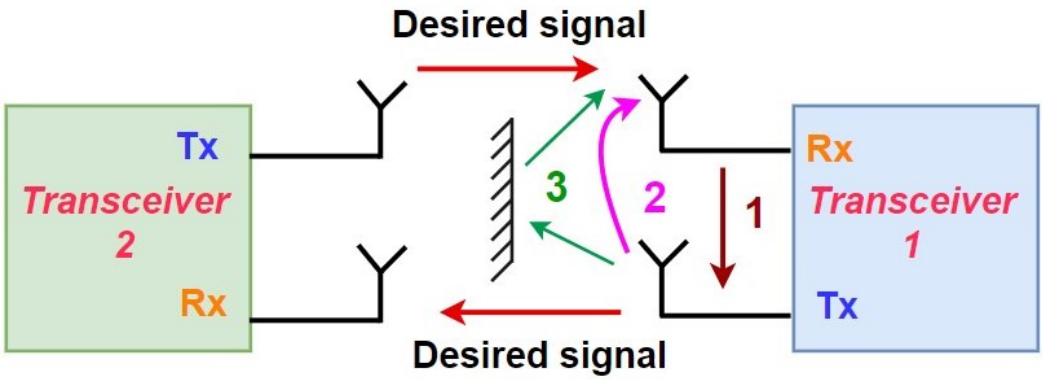


Figure 2-7 Generic view of a FD link subjected to the various kinds of SIs [12].

2) There is RF leakage due to limited antenna isolation.
3) The surrounding environment reflects part of TX's signal, so it is picked up by the RX.

In the FD link, the TX's leakage, IM2 and IM3 components, phase noise, and DAC's quantization noise leak to the RX path, and deteriorate the SNDR; hence, they corrupt the noise-floor of the RX. Unfortunately, The RX's path can even be saturated if the SI is too strong, and the RX data will be lost. Accordingly, it is hard to detect the MSD mixed with SI since the leakage signals usually are stronger than the input RF as shown in Figure 2-6. Hence, it is critical to sift the desire signal out from unwanted ones. It is worth noting an example for illustrating the SI concept. The output power of Wi-Fi can be up to +20dBm, while the RX sensitivity is as low as −90dBm, as shown in Figure 2-8 [4]. It is required more than +120dB DR to safely detect the input signal, each modulation method needs the specific SNR mentioned in the figure, it is supposed here 10dB. However, it would need a power-hungry ADC and BB's circuits which should not clip in such a high dynamic range, impossible to develop in that operating frequency by using the current technologies. As a consequence, it makes sense to look for alternative solution to overcome the negative effect of the SI.

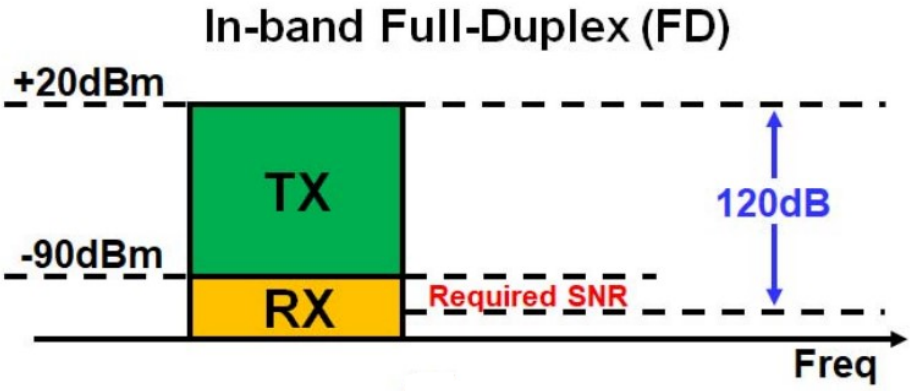


Figure 2-8 An example of degrading the performance of RX due to presence of the SI in a FD radios [4].

The important difference between the SI and blockers is that the SI is generated inside the transceiver, so we have sufficient knowledge of its pattern, compared to the blockers for which we do not have exact information. In an ideal SIC block, a copy of the SI is re-generated, and then subtracted from residue signal in the RX path to alleviate the negative effect of the SI, hence, the BB circuits and ADCs can be developed in the current technology. The SIC block must show a negative sign response compared with the sum of the leakage paths, considering each leakage path has its own transfer function, shown in Figure 2-7 [13].

2.5.1 Generic method of the SICs

From the generic point of view, the SIC utilizes the knowledge of one or different points in the TX path to cancel the SI in the following domain: 1) *the RF*, 2) *Analog BB*, 3) *digital BB domain* or 4) *combination of two or more domains* as it is shown in the state-of-the-art publications in the next sub-section. The way of implementing the SIC architectures for a transceiver can be conceptually categorized, as shown in Figure 2-9, a signal (information) is tapped from the TX output, and then injecting it to the RX chain [12]. Here, it is important to mentioned that removing the noise and linearity of

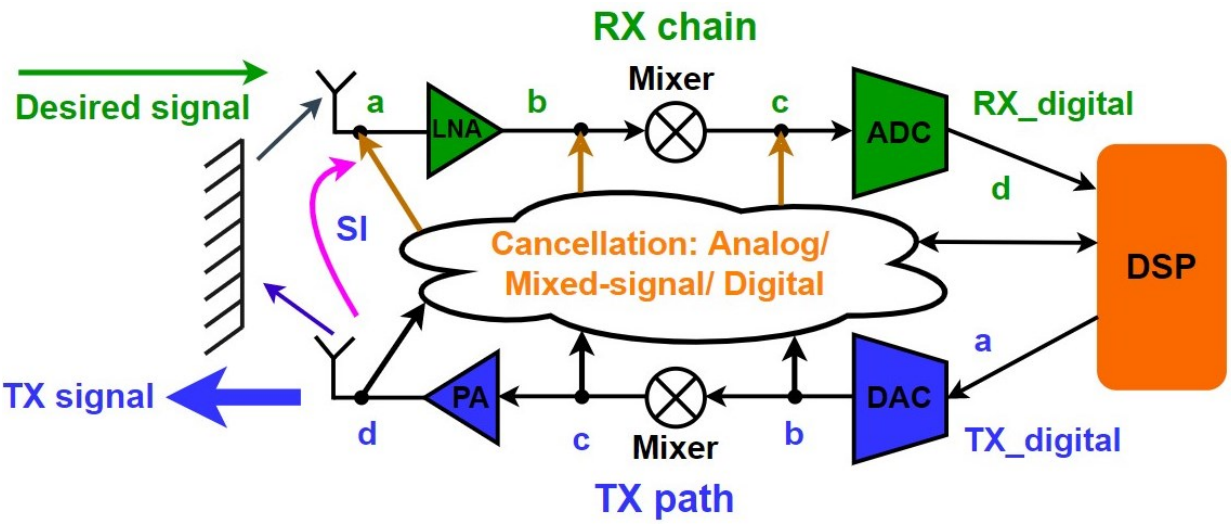


Figure 2-9 Generic view of a SIC in a FD link, signal is tapped from various points in the TX path and injected to diverse points in the receiver [12].

the leaked TX are not as simple as the main signal and it requires more complex circuits and algorithms which is out-of-scope of this thesis. For example, to lower the quantized noise leaked from the output of the digital-intensive transmitter, one way is to increase the ENOB of the RF-DAC.

Figure 2-9 shows the various nodes using information of the TX's path to re-create the cancellation signal and the diverse RX path to subtract the SI in the RX chain.

1) *The point of sampling the TX's signal*:
    a. Digital BB
    b. Analog BB
    c. RF at the input of the PA
    d. RF at the output of the PA
2) *The point of injecting the cancellation signal to the RX path*:
    a. RF at the input of the LNA
    b. RF at the output of the LNA
    c. Analog BB
    d. Digital BB
    e. Compound of the methods (a) to (d)

`

The TX signal can be tapped either from digital domain in the TX's back-end or other part after the DAC in the Analog or RF domain. As an example, it is noteworthy to give an example of one of the available options of the cancellation in Figure 2-9 for illustrating the point. A digital BB data (option (a) in the TX side) is chosen as the point to sample the TX signal. Then the option (e) (in the RX side) is used to cancel the SI. Part of the SI is cancelled at the input of the LNA (option (a) in the RX path), and the rest is removed in the digital BB (option (d) in the RX path). Two step cancellation scheme is a widespread one in state-of-art SIC such as cancellation in the RF and digital back-end.

The TX's signal leaks from the output of the PA to the RX's front-end contains most of unwanted signal including the non-linearities and noise; hence, the SIC block moved toward the antenna will shield the following blocks from the large SI alleviating their dynamic range requirements.

2.5.2 SIC Practical Points

It is worth emphasizing that developing the complete transceiver with embedded SIC block needs a lot of effort and experience. A few useful tips are shortly mentioned below to shed light on implementing the SIC's. These points are considered in more details in the following chapters.

2.5.2.1 Developing the DAC

If the signal in the back-end TX (digital one) is used as a cancellation information to remove Analog SI in the RX path it must be converted into Analog, by a DAC, before being subtracted from the SI. The design of such a high-speed DAC with relatively high dynamic range is challenging. For example, power-consumption, noise, silicon occupied area, and linearity of the added block (to the transceiver's design) can negatively affect the whole design. Removing the noise and IM component leakage are needed more complicated hard-ware and algorithm in the digital domain. *The*

`

proposed SIC block can just improve the dynamic range of the ADC without cancelling the non-linearity components and noise.

2.5.2.2 The Multi-path SIs

The TX signal can reach the RX path from multiple paths- with different delays. For example, if an object moves and become closer to the antenna the received signal will be less delay compared to the past. Since the delays in the SI paths are not equal, the SIC transfer function should follow these changes. In this case, the SIC block can be seen as an interpolator trying to regenerate and track the true SI compounds.

2.5.2.3 Closed-loop function

The change in process-voltage-temperature (PVT) degrades the performance of the chips. Accordingly, it is critical to deal with such changes. Embedding a closed-loop block in the SIC can track them and adjust the transfer function of the SIC block.

2.5.2.4 Viability of the SIC Design

Finally, on the contrary of Figure 2-8, it is also predominant to know whether the SIC block is feasible to implement or not, and what are obstacle in the way. As mentioned in [4], the DR equals +120dB (compatible with longer range radios) is not easily practicable to design. For implementing the system-level of the SIC block of such a system, the following explanation is required. The component or air interface can provide the isolation around +30dB between the TX and RX. Hence, it is inevitable to remove the remaining +90dB. If the DAC is developed to generate the replica of the leakage signal with +50dB amount of cancellation, which is feasible to design, the remaining SI (equal to +40dB) must be cancelled in the digital back-end. The mentioned example leads us to feasibly design blocks in terms of silicon occupied area and power consumption.

`

2.5.3 State-of-the-art SIC Scheme

Three advanced and modern SIC design, embedded in the transceivers, are presented in this sub-section.

2.5.3.1 Dirk-Jan van den Broek, JSCC 2015 [13]

The proposed transceiver is used the attenuated copy from the transmitted signal, and provides simultaneous tuneable phase shift, amplitude scaling and down mixing using a vector modulator down-mixer, for the SIC in the RX Analog BB. The schematic of the design is shown in Figure 2-10. The RX should have very high SNDR, so high IB linearity under cancellation of strong SI. This prevents the SI from inducing distortion that raises the RX noise floor and masks the desired signal. The SIC must take place before amplification to prevent the RX to clip under strong SI. This keeps the SI distortion low and thus maximizes the digital cancellation and link budget potential [13].

2.5.3.2 Tong Zhang, JSSC 2018 [4]

The proposed FD transceiver takes advantage of a dual-injection path SIC architecture; the schematic is shown in Figure 2-11. The SIC is performed in two different points at the RX side, the RF and BB domain. The signal is tapped from the

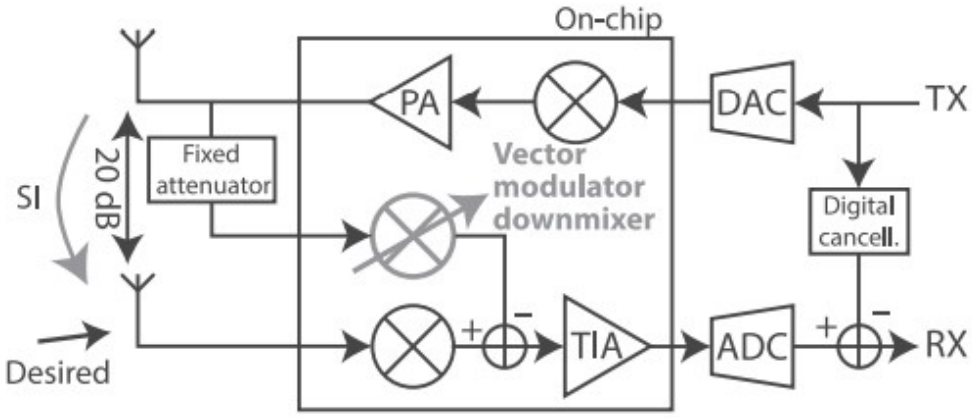


Figure 2-10 The FD transceiver including the Analog baseband SIC a vector-modulator down-mixer [13].

`

output of the PA, then the regenerated signal is injected into the mentioned locations. Part of cancellation occurs in the RF domain as follows. A copy of the TX's leakage is injected into the input of the LNA to lower the TX's leakage power. It prevents the following RX front-end from saturating. It is claimed that this technique has the positive effect of relaxing the needed linearity for the LNA and all the following RX blocks. Next, the regenerated signal is injected into the output of the BB in the RX chain with a feedforward path. Two adaptive filters (5-taps in the RF adaptive filter and 14-taps in the BB adaptive filter) are implemented to create an inverse time domain response of the leakage path while enabling the wideband SIC function [5].

2.5.3.3 Aravind Nagulu, JSCC 2021 [14]

The block diagram and die of [14] are shown in Figure 2-12. The proposed SIC technique uses finite-impulse-response (FIR) filters in the RF and BB domains. It utilizes a switched-capacitor true-time delay. The TX power is coupled capacitively to the RF canceler, and its output is connected to the LNTA input to realize the first stage of cancellation that increases the TX-induced compression of the receiver. Next, the BB canceler is capacitively coupled to the output of the down-conversion mixer, realizing the second stage of the cancellation. The wideband SIC in FD radios requires the achievement of large delay to accurately emulate the SI channel. The RF canceler

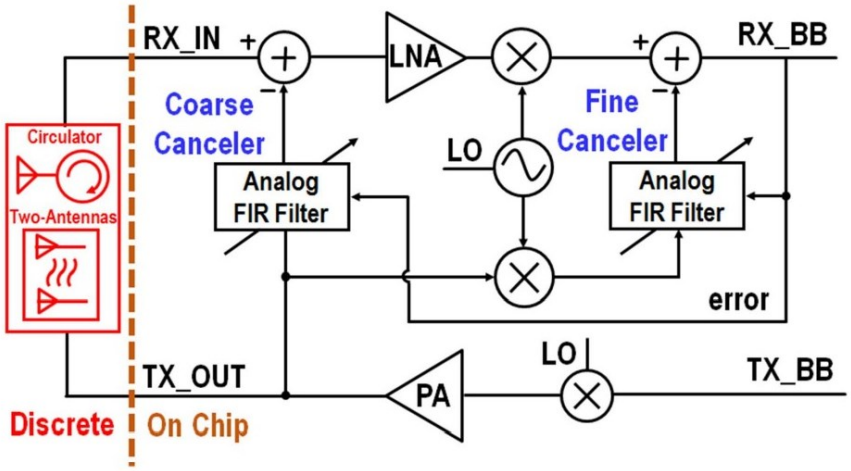


Figure 2-11 The FD SIC architecture with the dual-injection paths [4].

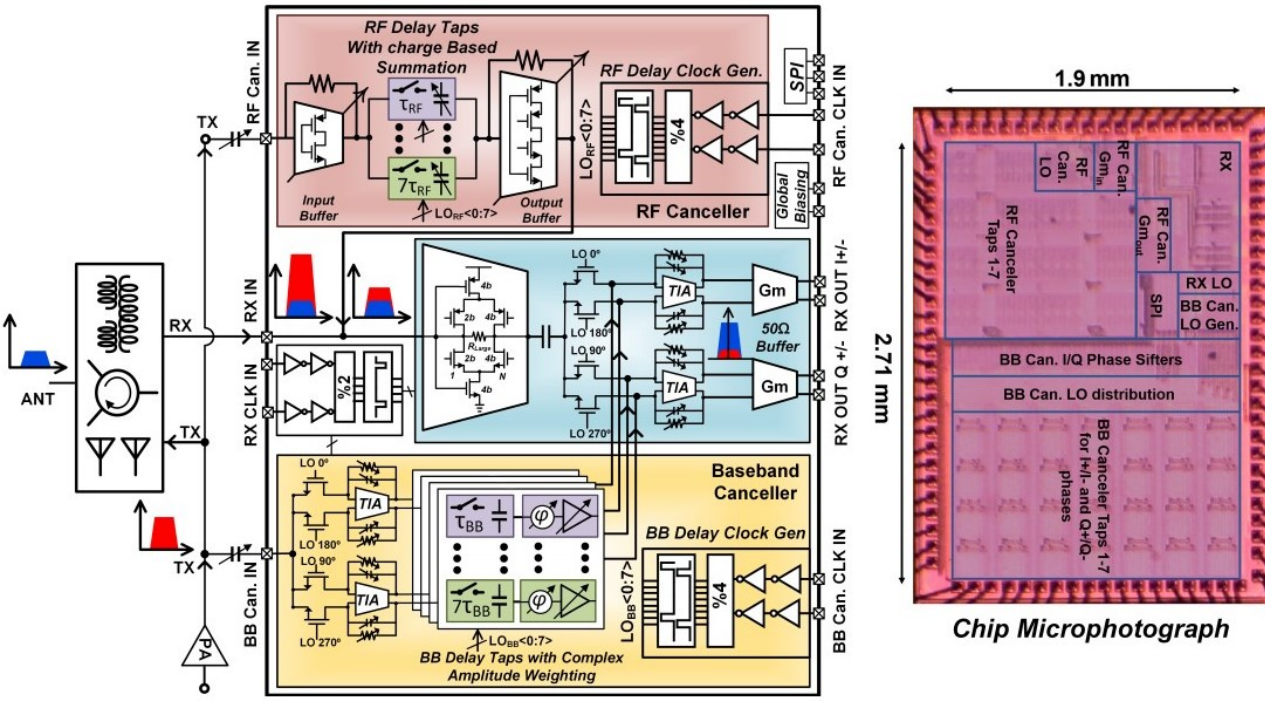


Figure 2-12 Implementing the FD receiver with finite FIR and integrated RF and BB cancelers [14].

emulates the SI channel through a set of delay taps with varying delays followed by a weighted summation. The BB canceler removes the residue from the RF canceler after the down-conversion, and therefore, the delay taps in it must exhibit a bandwidth of the order of the cancellation bandwidth. The overall cancellation and bandwidth are limited by the amount of delay obtained in the RF canceler and the gain roll-off in the BB delay taps [14].

2.6 Proposed Canceller

To enables FD operation correctly, a transceiver must be capable of attenuating the SI signal. Different SIC designs have been introduced for FD transceivers due to the importance of it. In this section, the proposed SIC method is explained at the system level to remove the SI in the BB domains according to required SIC and communication specifications mentioned in Table 2-2.

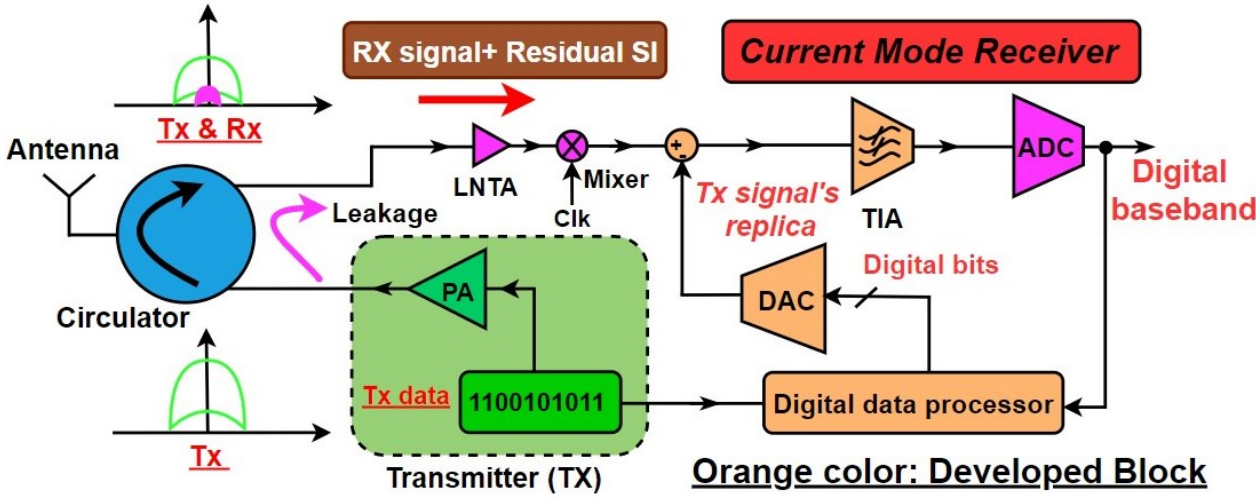


Figure 2-13 The proposed SIC FD transceiver used in the direct-conversion current-mode receiver.

The block diagram of the direct-conversion current-mode FD transceiver is shown in Figure 2-13 . The green rectangular shown at the left side of the figure below shows part of the TX side including the digital information and PA. The digital data is passed through the consecutive blocks, then the strong TX signal is sent to the antenna through *circulator*, the blue circle (three ports- in the photo) is a device typically used in the FD radios acting as a duplexer, allowing both transmitter and receiver to simultaneously work. Because of the limited attenuation of the circulator, a portion the TX signal leaks into the input of the LNTA which still can corrupt the quality of a weak signal in the receiver side. Hence, the SIC block plays a key role in the high-quality transceivers.

Table 2-2 Design (RF) parameters of the proposed SIC.

Param.	PTX (dBm)	ISO_{TXtoRX} (dB)	RF frequency (GHz)	BW_{cancl} (MHz)	NF (dB)	Margin (dB)	RF Gain (dB)	G_{mLNAT} (m℧)
Value	+20	+40	1	80	+8	+6	40-60	50

2.6.1 RF Design's Parameters

Before starting to analyse and developing the SIC, it is necessary to know the corresponding RF design's parameters. The useful and practical data have been gotten, shown in Table 2-2, from different source including the data given by my supervisor. In this Table, TX to RX isolation and cancellation bandwidth are abbreviated to ISO_{TXtoRX} and BW_{cancel}, respectively.

2.6.2 Developed SIC

As it was mentioned earlier, the SIC can be performed in the RF, Analog, mixed-signal, and/or digital domains, and can be done using either passive or active circuitry.

The active RF cancellers are compact, widely tuneable, and reconfigurable. The fundamental challenge associated with the active RF SIC is the noise and distortion of the cancellation circuitry, which can limit the receiver's performance. Then, the second limit is the cancellation BW, which is typically limited by the frequency selectivity of the antenna interface.

The signal tapped from the output of the PA has most of the necessary information for doing the SIC, such as the non-linearities and noise, but it can have negative loading effect on the PA's output and creating the delay of the RF/Analog signals. Likewise, by injecting the cancellation signal at the input of the LNTA, the SIC is done in the RF with a high-speed current DAC [15], but it introduces noise penalty being located before signal amplification. On the other hand, the digital data in the TX's BB can provide signal processing and the delay implementation in the digital domain. The downside of this method is that non-linearity and any noise of the TX's front-end will not considered in this cancellation scheme.

There are various methods to perform cancellation according to information presented in Figure 2-9. Each method has its own advantages and disadvantages, and we must also consider the practical points corresponded to each method. If the DAC

`

performs the SIC after the mixer at the input of the BB, as proposed here and shown in Figure 2-13 with orange colour, the cancellation technique can benefit from the front-end amplification and minimizing the noise degradation [16]. Moreover, by connecting the DAC to the virtual ground inputs of the TIA, immediately after the down-conversion mixer, the non-linear effects of the DAC are reduced a minimal additional power is required. Since the pattern of the SI is available, it is also possible to take advantage of the signal processing in the digital domain.

2.6.3 Proposed SIC Constituent Blocks

The blocks shown in Figure 2-13 with the orange colour are developed in this dissertation and are composed of three main blocks as follows [16].

1) Capacitive array
2) TIA
3) Digital circuits

Here, the system level parameters of the blocks are calculated according to the SIC design. *The developed design can be employed in two different modes, as follows.*

1) Minor application: As a stand-alone DAC with certain BW.
2) Main application: The SIC block.

Since the SIC is the main goal of this thesis, the parameters are calculated according to the SIC requirements. The link budget of the FD receiver is shown in Figure 2-14. It starts from the peak power in the transmitter, then the SI is attenuated by circulator, and it will end up to the noise floor in the RX side.

`

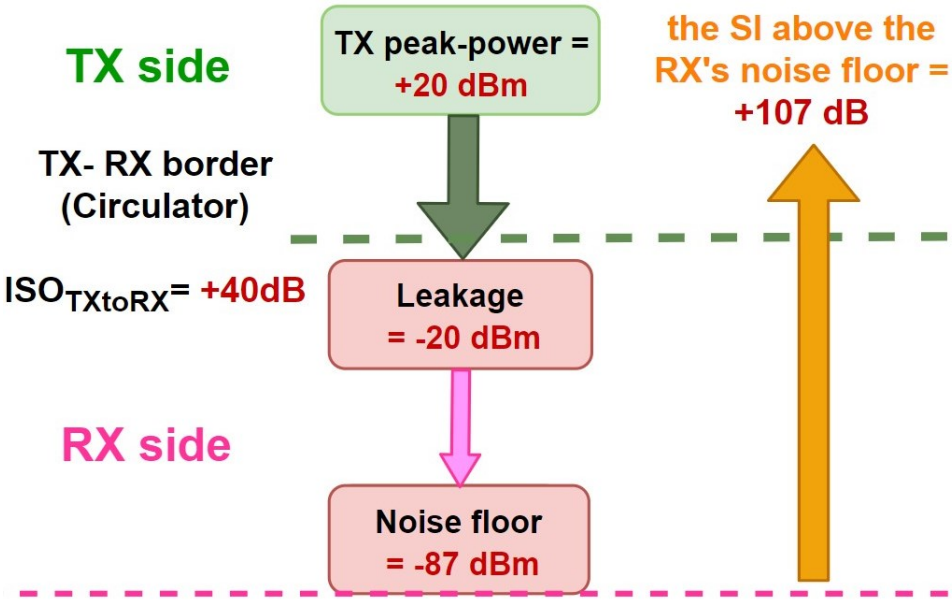


Figure 2-14 The illustration of the link budget of a FD communication system according to the specification mentioned in Table 2-2.

The calculation flow starts from here to finally achieve the amount of required cancellation represented as a different between maximum leaked transmitter's power and the receiver noise floor, represented by PTotSIC. According to Eq. (2-9), the power of the RX noise floor is calculated to be equal, $P_{Noise\ Floor} = -174 + 10 \times \log_{10}(80 \times 10^6) + 6 = -87dBm$ .Therefore, the required cancellation is equal to $P_{TotSIC} = P_{TX-peak} - P_{Noise\ Floor} = +107dB$, as it is depicted in Figure 2-14. Besides, the leakage signal is attenuated by circulator by +40dB, and the rest of the SI should be removed by proposed mixed-signal SIC block. It is equal to $P_{SIC} = P_{TotSIC} - ISO_{TXtoRX} = 67dB$.

2.6.3.1 Choosing the DAC

The next step is to choose the proper architecture for developing the DAC. There are three major topologies of the DAC in terms of the fundamental cells, we explain them in more details below [17]:

Resistive DAC (RDAC): It is comprised of resistors with different weights, switches, and sometimes an amplifier. The basic cell resistance could not be chosen too large to

`

keep the thermal noise low. The design of the RDAC is straightforward, and it causes less spike compared to the switched-capacitor. However, it burns relatively high static current. Another downside is that resistor takes up more area and its tolerance is relatively large for most of applications [17].

Current DAC (IDAC): It constitutes by several current cells with different weights. it does not need an extra amplifier to properly work. It is also the best choice for high-frequency and its occupied area is less than other kinds of the DAC. Again, it consumes static and dynamic power because current cells are continuously being switching. It is prone to have different output impedance, code-dependent error in high-frequency, because various current sources are on in the different period. Matching between current sources is also another practical problem and should be considered when drawing the layout. It is not scalable with the technology because IDAC needs minimum supply voltage to properly work [17].

Capacitive DAC (CDAC): In recent years, the use of capacitive DAC in the SAR ADCs is increasingly growing (many articles are published in this manner) because it merely includes switches, capacitors, and some logic circuits which are suitable for advanced sub-nanometre CMOS process. If it uses as a stand-alone DAC, it needs an amplifier. It works in two different modes, namely charge sharing or redistribution. In contrast to IDAC, it does not need any headroom for properly biasing current sources. Moreover, it is less sensitive to jitter compared to the IDAC. The CDAC does not consume any static power (unless it needs an amplifier). The capacitors show high impedance at the working frequency, so their loading is usually negligible. Besides, the matching between capacitor is adequate in medium resolution, 8-12 bits, ADCs, and DACs. The ratio between maximum and minimum capacitive, matching, parasitic of the capacitors, and thermal noise are the limiting factor in this topology [17].

`

2.6.3.2 System-level Parameters of the proposed DAC

Here, the CDAC was selected because of the explanation above, especially since it can operate with a lower voltage supply to create the necessary current to cancel the SI [17].

The design of CDAC is explained below:

First, we choose the best clock frequency of the CDAC to boost the performance of the SIC. To minimize mutual interference, the DAC should be synchronous with the down-conversion mixer [3]. So, the working frequency of the DAC (FS) is chosen to be twice the mixer clock i.e., 2 GHz. Thanks to over-sampling, the required SNR_{DAC} is expressed in Eq. (2-15).

$$OSR = \frac{F_S}{(2 \times BW_{Signal})} \quad \text{Eq. (2-14)}$$

$$SNR_{DAC} = 6.02 \times N + 1.72 + 10 \times \log_{10}(OSR) \quad \text{Eq. (2-15)}$$

Where N is the number of bits and OSR is the oversampling ratio. According to Eq. (2-15) and the information in Table 2-2, the number of bits is calculated equal to 9, but considering DAC non-idealities like static and dynamic non-linearity, we have added an extra bit making N=10. In principle, we can use noise and mismatch shaping to reduce N. However, the power consumption of the digital pre-processing can be too high due to the very high clock. To minimize power consumption, we avoided any noise shaping and digital signal processing at such a high frequency [18].

Before initiating the transistor level design, it is critical to calculate the total capacitance of the CDAC (CT) because it creates the necessary current for cancellation. Two parameters usually play a key role in choosing the CT as follows.

1) $\frac{KT}{C_T}$ noise
2) Matching
3) Cancellation requirement

`

Here, to compute the maximum SIC's current, the maximum TX power, ISO_{TXtoRX} and the LNTA's transconductance, as reported in Table 2-2, are equal to +20dBm, +40dB, and 20m℧, respectively. The peak's leakage voltage at the input of the LNTA is equal to -20dBm, equivalent to +31.6mV, and will be converted to an RF current of 0.63mA. Eq. (2-16) provides us with the necessary data between RF parameters and the output current of the CDAC.

$$I_{Canc} = I_{DAC}(Average) = \frac{Q_{DAC}}{T_S} = C_T \times V_{Ref} \times F_S \ (A) \quad \text{Eq. (2-16)}$$

Where Q_{DAC} is total charged transferred by the CADC to do the cancellation, V_{Ref} is the CDAC's reference voltage related to its full-swing, and T_S is period of the clock of the CDAC. V_{Ref} is chosen equal to 0.35V, as it will be explained in chapter 5, and T_S is equal to 500ns. Therefore, the total capacitance is calculated to 1pF.

The information with regards to TIA and digital parts, shown in Figure 2-13*, will be explained in the following chapters.*

`

3 Trans-impedance Amplifier (TIA)

The trans-impedance amplifier (TIA) is a first order filter removing unwanted frequency band and also converting the current to voltage at the Analog back-end of the current-mode receivers. For filtering OOB blockers, it provides low impedance path at the output of the mixer, as shown in Figure 3-1. For FD applications, to have high IB linearity, a wide bandwidth TIA is highly recommended along with low integrated IB noise, small area, and the smallest possible power-consumption [19]. In this chapter, the TIA's necessary blocks are discussed in more details. Then, by simulating the TIA's performance, it is possible to check whether the design is suitable for the SIC or not.

3.1 The Background Information

As mentioned earlier, keeping the input impedance of the TIA low (Z_{in}), not only over the BW_{BB} but also for OOB frequencies is a key point in the current-mode receiver, to ensure a small voltage swing at the output of the mixer, and to guarantee high linearity of the receivers. The whole TIA start from the shunt (relatively big capacitance), called C_Z, toward the output of Analog BB as shown in Figure 3-1. Because of the negative feedback around the TIA, its linearity performance is improved by the amount of the loop gain which is a function of the frequency [20]-[21]. The main duties of the TIA are re-listed below, as shown in Figure 3-1 [21]:

1) The attenuation of OOB interferences.
2) Maintaining a low Z_{in} up to a high frequency.

`

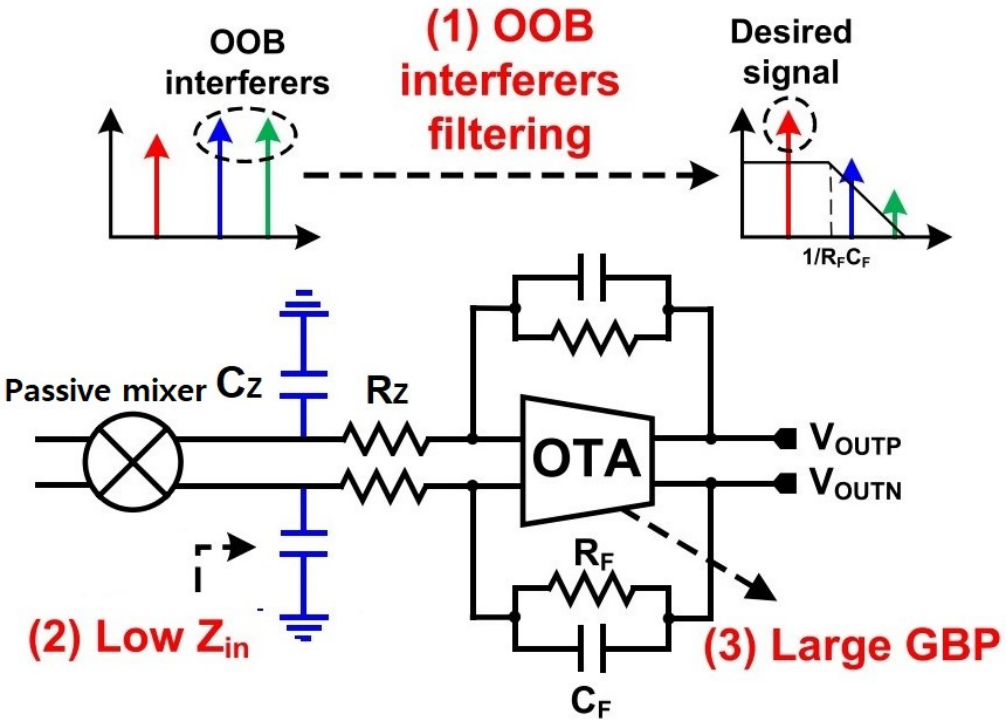


Figure 3-1 (Top) OOB blockers (bottom) conventional TIA structure [21].

3) A large GBW of the operational-transconductance amplifier (OTA) to satisfy conditions (1) and (2) above.
4) Maintain a relatively constant virtual ground at the output of the CDAC.

The TIA is composed of the three main parts as follows:

3.1.1 Feedback Network

The feedback network is composed of R_F and C_F as shown around the amplifier in Figure 3-1. The R_F amplifies the RX weak signal without any clipping at the TIA's output (assuming at least 20dB of SI cancellation). The R_F and C_F set the BW_{BB} of the receiver [20]. So, the RF specifications dictates how to select them.

3.1.2 Input RC

This sub-block includes a relatively big capacitance (normally bigger than 8pF), called C_Z, and small series resistor (less than 10Ω), defined by R_Z. They are at the input of the TIA, as shown in Figure 3-1. The combination of the C_Z in front of the TIA and the

TIA's inputs create the low impedance at the output of the mixer over the high-frequency and low-frequency. The main contribution of the Cz is to filter the high-frequency components after the mixer. It is also employed to absorb the current spikes when the CDAC discharges/charges the energy toward virtual ground. This limits the peak voltage at the inputs of the TIA. As a result, it avoids the input stage of the OTA from going into saturation decreasing the non-linearity of the system due to slewing. Furthermore, the combination of Cz and Rz also creates a high-frequency zero in the loop transfer function of the TIA boosting the small signal phase-margin [21]. The cost of adding Cz is to increase the occupied area and integrated noise. The large Cz also reduces the gain-bandwidth-product (GBW) of the TI's, degrades the low-frequency performance of it. The integrated noise, *assuming the other components of the TIA are noiseless*, is obtained by Eq. (3-1) and is approximately equal to Eq. (3-4).

$$\overline{v^2{}_{nTIAout}} = \overline{v^2{}_{nOTA}} \times \left|1 + \frac{Z_F}{Z_{nIN}}\right|^2 \quad \text{Eq. (3-1)}$$

$$Z_F = R_F \, II \left(\frac{1}{s \times C_F}\right) \quad \text{Eq. (3-2)}$$

$$Z_{nIN} = \frac{1}{R_{mix} \, II \left(\frac{1}{s \times C_Z}\right)} \quad \text{Eq. (3-3)}$$

$$\overline{v^2{}_{nTIAout}} \approx \overline{v^2{}_{nOTA}} \times \left(1 + \left(\frac{C_Z}{C_F}\right)\right)^2 \times \frac{7 \times \pi}{4} \times BW \quad \text{Eq. (3-4)}$$

Where $\overline{v^2{}_{nTIAout}}$ is the noise spectral density at the TIA's output in $(\frac{V^2}{Hz})$, $V^2{}_{nOTA}$ is the noise referred to the input of the OTA in $(\frac{V^2}{Hz})$, Z_F is the feedback impedance, R_{mix} is the impedance seen at the output of the mixer [22]. It shows the equivalent resistor seen from the input of the TIA toward the LNTA when the capacitor parasitic (C_{par}), before the mixer, is periodically switched, expressed by $R_{mix} = \frac{1}{8 \times F_{LO} \times Cpar}$. The equivalent noise model (signal ended) is shown in Figure 3-2 (the effect of the Rz is

`

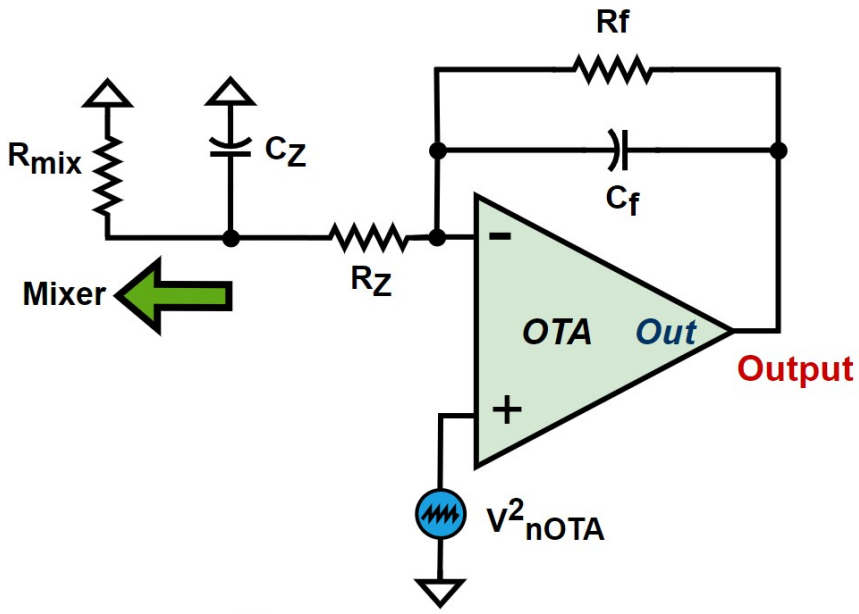


Figure 3-2 Amplifying noise of an OTA by C_Z noise, single-ended model [21].

negligible in this calculation). Thus, Eq. (3-1) explains the dependency of the output noise of the TIA with frequency [22], it includes a zero in the noise transfer function. Eq. (3-4) indicates that the integrated output noise will increase if the C_Z rises.

3.1.3 Frequency Domain's Issues of the TIA and OTA

The last part of the TIA is an active part, namely OTA. It is one of the principal building blocks in the Analog communication systems, especially filters. Both high DC-gain and high GBW (compared to the BW_{BB} of the TIA) characteristics are required to obtain high-performance. With the shrinking of the feature size of the devices in advanced complementary-metal-oxide-semiconductor (CMOS) process, the intrinsic gain of the transistors decreases. For example, it could be as low as 10dB to 20dB, depending on the bias current, for 28-nm CMOS process. We cannot stack up the transistor to raise the gain of each stage due to lower supply voltage in the advanced CMOS technology. Hence, achieving the required (high) DC-gain of the OTA is a demanding task. The available option is to cascade, some gain stages to boost the DC-gain. However, this method increases the number of the low-frequency poles and causes either to lower the GBW of the OTA or to face stability issue. As a result,

it is critical to perform a complicated frequency compensation to ensure the stability of the OTA, but it may require burning more power as well. Ref. [23] explains that there is a trade-off between the DC-gain and the stability; therefore, the use of three or four -stages can be a good candidate for low-supply voltage in advanced technologies [23]. Here, a three-stages OTA is chosen because a four-stages OTA has higher power-consumption and one more low-frequency pole. Besides, the common-mode stability of the whole OTA is a big challenge with four-stages [20].

3.1.3.1 Stabilizing Methods (Compensation schemes)

There are two well-known compensation techniques to ensure closed-loop stability as follows [24].

Pole-splitting: A simple two-stage miller compensation technique belong to this category, and Nested-miller-compensation (NMC) is employed for multi-stage OTAs as a general pole-splitting technique. In this strategy a dominant pole, which usually is at the output of first one-stage is sent to lower-frequency and the non-dominant poles move toward higher frequency. To this end, some capacitors are located around high-gain stages and Miller-effects play a key role. The pole-splitting heavily dissipates power to extend the GBW [24]-[25].

Pole-zero Cancellation: If a zero is created at the same location of a pole they can cancel each other, reducing the number of poles by one. However, imperfect pole and zero cancellation, because of different reasons such as changing in temperature, results in pole-zero doublet phenomenon. Unfortunately, this can degrade the time domain response of the closed loop of TIA due to slow settling-time component. The simplest way to improve settling-time is to send the pole-zero doublet to relatively higher-frequency. The benefit of the pole-zero cancellation motivates us to explain the doublet effect in more details showing how its negative impact can be addressed [26].

`

3.1.3.2 Doublet Analysis

Larger closed-loop GBW of the OTA does not necessarily result in a drop in the settling-time if the pole-zero doublet exists in the design. It is worthy emphasising that the doublet causes minor change in frequency response but may deteriorate the settling-time [27]. A linear model is used to study the closed-loop pole-zero doublet in the time domain response shown in Figure 3-3. For the sake of simplicity, the amplifier is in unity-gain feedback and its higher frequency poles near and after the GBW have been neglected. If the input is a step voltage with amplitude equals E, the time domain response of this model is given by the formulas below [26].

$$V_O(t) = E \times (1 - k_1 \times e^{-\omega_{GBW} \times t} + k_2 \times e^{-\omega_Z \times t}) \quad \text{Eq. (3-5)}$$

$$k_1 \approx 1 \quad \text{Eq. (3-6)}$$

$$k_2 = \frac{\omega_Z - \omega_P}{\omega_{GBW}} \quad \text{Eq. (3-7)}$$

Where ω_Z , ω_P, ω_{GBW} represent zero and pole of the doublet and GBW of the OTA, respectively. Eq. (3-5) shows the presence of a fast and slow-settling components in the response given by: the second and third exponential function, respectively. The time domain response to the step input is shown Figure 3-4. It clearly shows two different components are included in the response. The slow-component degrades the time-domain response performance of fast-circuits. A low-frequency doublet gives a

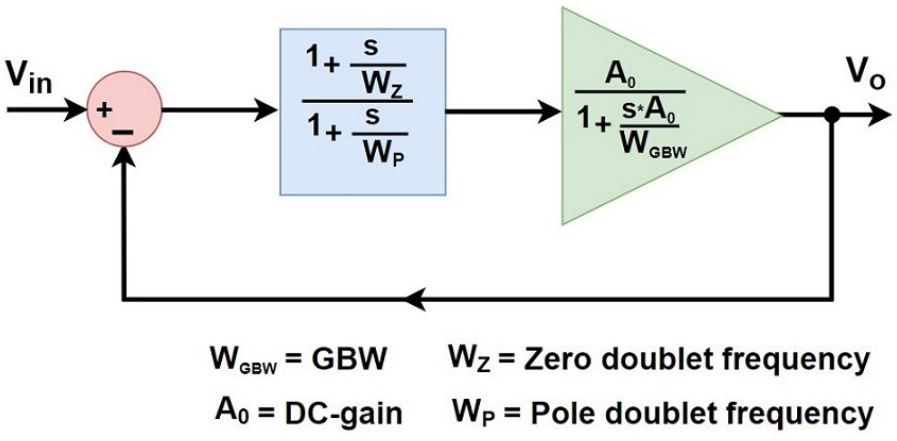


Figure 3-3 Linear model of the unity-gain configuration of an amplifier to investigate the negative effect of a doublet on the settling time [27].

`

term with a longer time-constant but with smaller amplitude, equals to $E \times k_2$. On the other hand, the high-frequency component, the second terms in Eq. (3-5), settles fast although its initial amplitude is large. The former is inversely related to the doublet frequency. The latter is proportional to the open-loop doublet separation factor, the inverse of the loop gain at the doublet frequency, and the input step amplitude [28]. As a rule of the thumb, if the 0.1% settling-time is only considered the lower-frequency term may be within the acceptable error band and thus does not deteriorate the performance of the circuit. However, if settling-time equal to 0.01% is targeted the same doublet of the previous condition may cause a large increase in the settling-time. A higher-frequency doublet is likely to produce settling-time degradation in all cases, but its effect will die away much sooner [28].

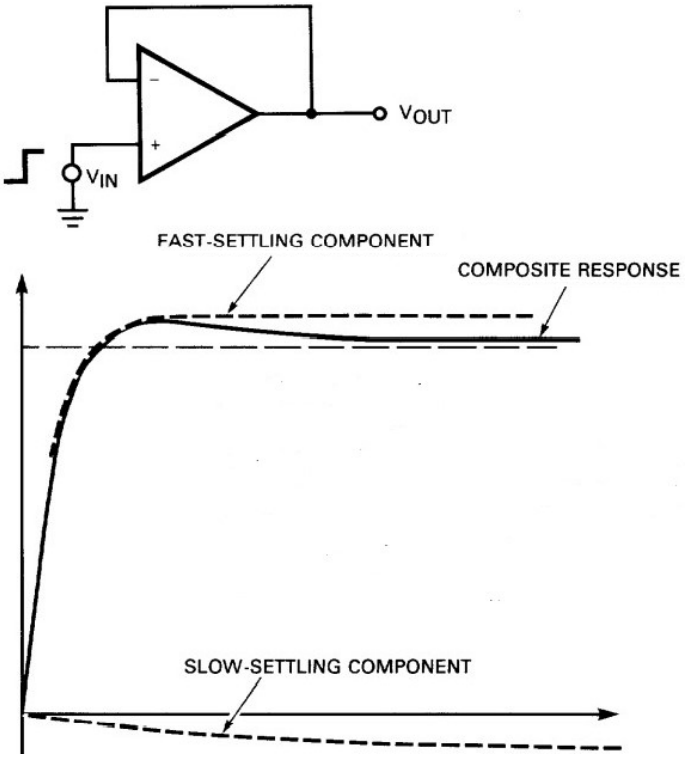


Figure 3-4 Time domain answer of an unity-gain amplifier, Figure (3-3) , to show doublet slow and fast-settling components' behaviours [28].

3.1.3.3 Creating the Required Zero

The method of pole-splitting does not work very efficient for stabilizing the amplifiers in high-speed circuit. Hence, the pole-zero cancellation technique is a useful approach in the high-frequency applications like high-speed Δ-Σ. There are two ways to create the zero as follows.

Passive: The combination of passive elements is employed to generate the zero such as a series of a resistor and a capacitor, but it always creates a pole at higher frequency as well [20], [24].

Active: Active zero is created by using the active devices, like transistors, [23]-[24], [26]. The feedforward technique is one effective way to create such a zero. Besides, it can enhance the large signal behaviour of the amplifier due to the feedforward path. The basic concept of a multistage multipath feedforward OTA is formed by the combination of single stage amplifiers as shown in Figure 3-5(a), and it creates the high gain and the high bandwidth OTA. The first-order path in this amplifier is comprised of a single stage (g_{m1}) while the third-order path consists of three stages

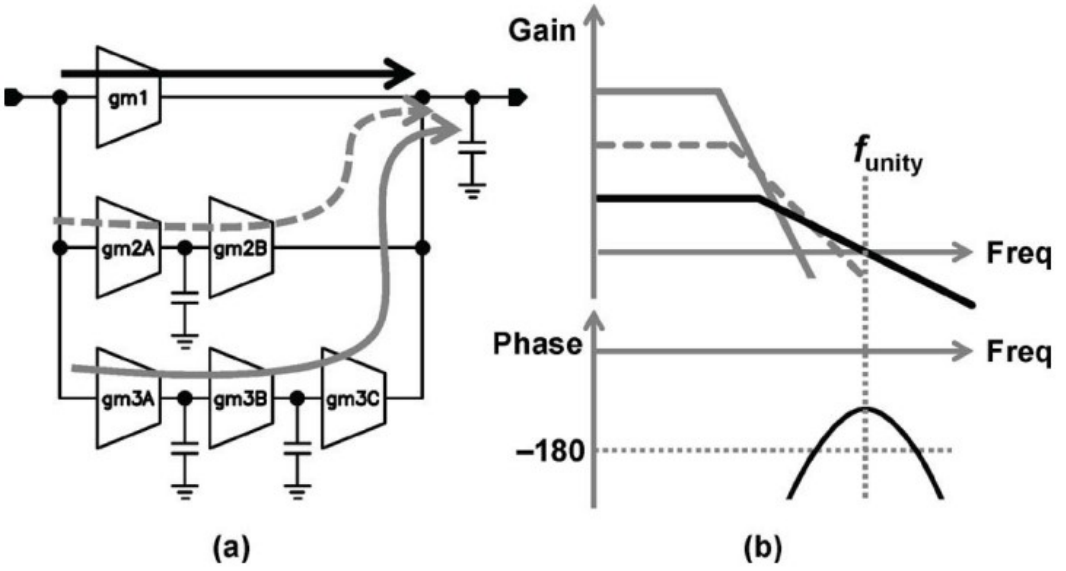


Figure 3-5 (a) Conceptual diagram of a multipath feedforward OTA (b) gain and phase demonstration [29].

`

($g_{m3A}, g_{m3B}, g_{m3C}$). A second-order path ($g_{m2A,}\ g_{m2B}$) provides a controlled transition from third- to first order behaviour. The overall gain of the amplifier is the envelope of the paths, as shown in Figure 3-5(b), because the path with the highest gain dominates the response of the amplifier [29]. To make the amplifier stable in a feedback loop, the gain must be gradually reduced from a high-order response to a first-order response around the unity gain frequency so that the phase response approaches 90 degrees as shown in Figure 3-5(b). The inter-stage capacitors shown Figure 3-5(a) models the output parasitic of each node, so this method is called no-capacitor feedforward (NCFF) scheme. The proposed NCFF compensation scheme relaxes the downsides of Miller compensation schemes, especially lowering the power consumption. However, adding capacitors to the second order and higher order paths, shown in Figure 3-5(a), can also be considered to ensure the OTA's stability in the closed-loop [29]. The NCFF technique can simply be explained by the formula presented below. Here, we suppose the blocks, shown in Figure 3-5 (a), are represented with ideal gm-cells, and it is assumed in the calculation that there is not parasitic pole before the required GBW. The linear model is shown in Figure 3-6 to give an insight about the created zero. The calculation formulas start from Eq. (3-7) to (3-12). By writing equation in the different paths, namely I_{St2} and $I_{StFF,}$ the output current, named I_{Z2}, can be calculated [26].

$$V_{o1} = V_{in} \times g_{mSt1} \times \left(R_{o1} II\ \frac{1}{s \times C_{o1}}\right) = \frac{V_{in} \times g_{mSt1} \times R_{o1}}{1 + s \times R_{o1} \times C_{o1}} \quad \text{Eq. (3-8)}$$

$$i_{ff} = V_{in} \times g_{mStFF} \quad \text{Eq. (3-9)}$$

$$i_{St2} = V_{o1} \times g_{mSt2} \quad \text{Eq. (3-10)}$$

`

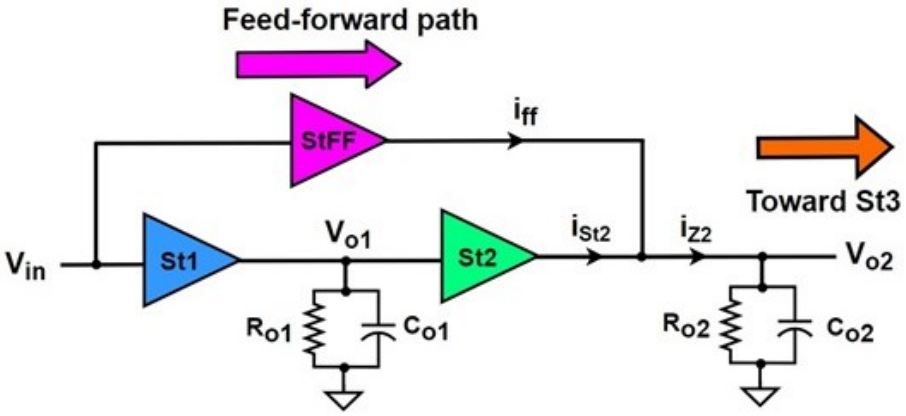


Figure 3-6 Single-ended model for creating a zero by feedforward technique [26].

$$i_{Z2} = i_{St2} + i_{ff} = \frac{V_{in} \times g_{mSt1} \times R_{o1}}{1 + s \times R_{o1} \times C_{o1}} \times g_{mSt2} + V_{in} \times g_{mStFF} \quad \text{Eq. (3-11)}$$

$$V_{o2} = V_{in} \times g_{meff} \times H_{pz}(s) \left(\frac{R_{o2}}{1 + s \times R_{o2} \times C_{o2}} \right) \quad \text{Eq. (3-12)}$$

As it is shown in Table 3-1 , by changing the feedforward, g_{mStFF}, alteration of the effective transconductance stage, g_{meff}, is negligible but the amplitude of the zero is changed. If we need to lower the amplitude of the zero it can be done either decreasing the DC-gain of the first and second stage of the OTA (by lowering A_{o1} or g_{mSt2}) or by increasing g_{mFF}. Lowering the DC-gain has negative effects in other parameters of the TIA, like precision of the final value, and increasing the g_{meff} requires more power.

Table 3-1 Summary formula of the NCFF technique.

Variable	Formula	Explanation/ Simplifying
g_{meff}	$g_{mSt1} \times R_{o1} \times g_{mSt2} + g_{mStFF}$	Gain: $A_{o1} = g_{mSt1} \times R_{o1}$ G_{m12}: $g_{meff} \approx g_{mSt1} \times A_{o1} \times g_{mSt2}$
$H_{pz}(s)$	$\frac{1+s\frac{s}{\omega_Z}}{1+\frac{s}{\omega_{p1}}}$, $\omega_{p1} = \frac{1}{s \times R_{o1} \times C_{o1}}$	$\omega_Z = \left(1 + \frac{g_{mSt1} \times R_{o1} \times g_{mSt2}}{g_{mStFF}}\right) \times \omega_{p1}$

3.2 Calculating the Frequency Domain Parameters

Before starting to develop the OTA in the transistor-level, some system-level numbers must be calculated such as RF and C_F.

3.2.1 System-level Design

Supply Voltage: The voltage supply of the OTA, Analog supply, is equal to 1.3V. The reason will be mentioned, shortly, there is a trade-off between the voltage swing at the output stage of the TIA and the amount of SIC.

Input R_Z and C_Z: The single-ended model of the TIA design is shown in Figure 3-7. This network is in the front of the OTA. As a rule of the thumb, choosing capacitance C_Z between 8pF and 15pF could be good [20]. C_Z is chosen about 10 times C_T, i.e. the total CDAC capacitance, to limit initial spike voltage at the virtual ground. Likewise, the resistance of the R_Z cannot vary too high because the low-frequency impedance seen after the mixer is equal to the series of resistance R_Z and input resistance of the TIA, Z_{inTIA}, expressed by Eq. (3-12), and should be small to fulfilling the criterion of the low-frequency linearity. On the other hand, creating a high-frequency zero, improve the phase-margin as we explain later. Hence, we need to consider both conditions when choosing R_Z. A resistance between 7 to 15Ω could be a practical number. We choose 8.5Ω according to formula (3-13) and (3-14).

$$Z_{inTIA} = \frac{Z_F}{A+1} \quad \text{Eq. (3-13)}$$

$$f_{ZhFin} = \frac{1}{2\times\pi\times R_Z\times C_Z} \quad \text{Eq. (3-14)}$$

`

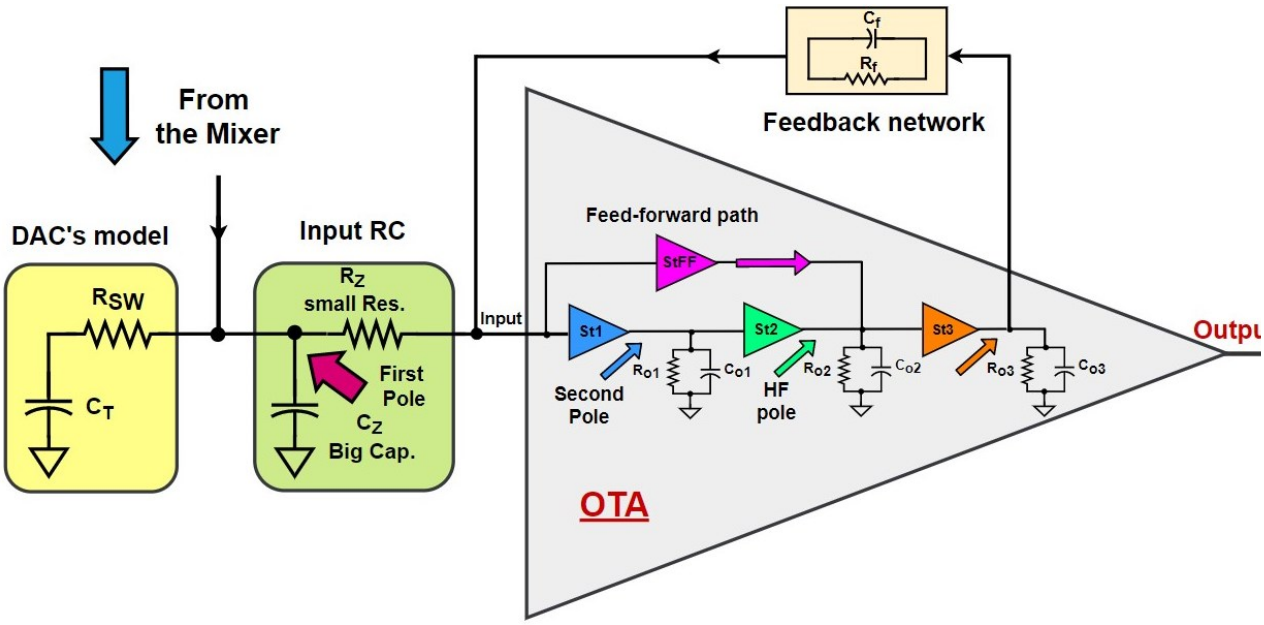


Figure 3-7 Single-ended block diagram of the Analog section [16].

Feedback Network (R_F and C_F): These two components are used in the feedback path, and the BB's current is converted into voltage by R_F [21]. Due to the specification of the project, written in Table 2-2, and Eq. (3-14), the resistance is calculated to $R_F = 2K\Omega$. Given the BW_{BB} of the RX, written in the table, capacitance C_F is calculated by formula (3-15) equal to $C_F = 2pF$.

$$A_{RX} = G_m \times R_F \qquad \text{Eq. (3-15)}$$

$$f_{BW} = \frac{1}{2\times\pi\times R_F\times C_F} \qquad \text{Eq. (3-16)}$$

OTA: To obtain the necessary DC-gain of the OTA, as mentioned in paragraph 3.1.3, s three-stages amplifier is a good start point. Each triangle in Figure 3-8 represents one transconductance stage (gm), and Roi and Coi shows the equivalent output resistor and capacitor of the previous stage, respectively [23]-[25]. The Roi contributes to generating the gain of a stage, represented by Eq. (3-17). The *dominant pole* of each stage is created at its output of it and represented by Roi and Coi in Eq. (3-18).

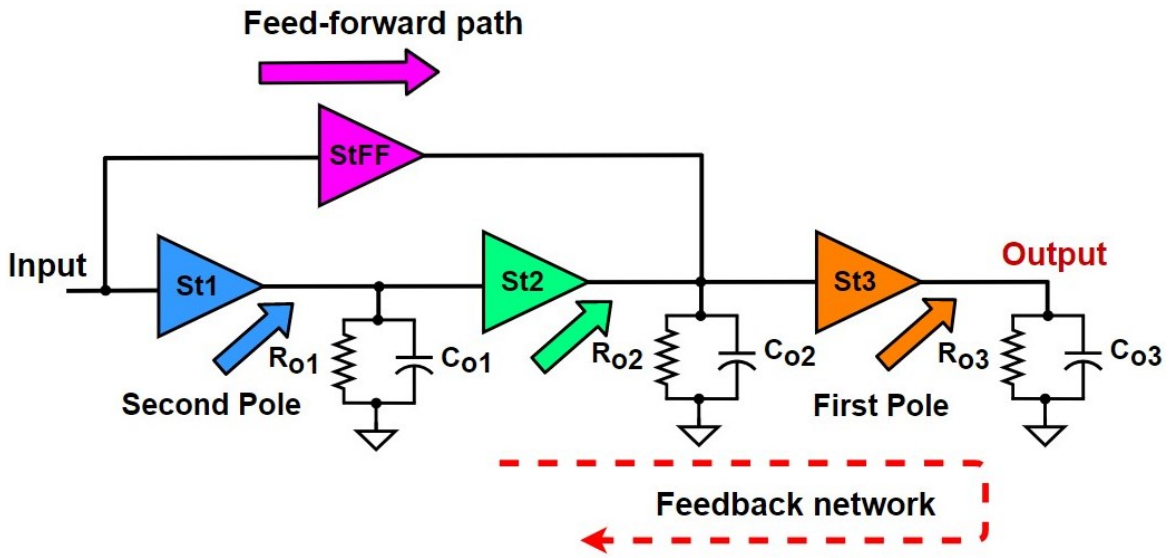


Figure 3-8 Single-ended model of the developed OTA [16], [30].

$$A_{S_{ti}} = g_{mSti} \times R_{oi} \quad \text{Eq. (3-17)}$$

$$f_{S_{tio}} = \frac{1}{2\times\pi\times R_{oi}\times C_{oi}} \quad \text{Eq. (3-18)}$$

Three dominant poles exist in Figure 3-8 due to the three-stages OTA, it is supposed that the internal non-dominant pole of each stage is negligible. In a high-frequency application, high-frequency CDAC and TIA, the pole-splitting technique is not useful because of the explaining in 3.1.3.1. Hence, it is important to have two zeros to stabilize the TIA and enhance the phase-marge, as mentioned in 3.1.3.3. From Figure 3-7, it is understandable that one of the zero can be created by the combination of RZ and CZ. The next zero is made by using feedforward sub-block, StFF, the calculation is reported in Table 3-1. In contrast to Figure 3-5 (a), for creating a zero the first transconductance, gm1, is removed because it not only decreases the output impedance of the output stage, lowering the DC-gain of the TIA, but increases the power-consumption of the whole TIA [23].

`

Gm-cell: The DC-gain and the dominant pole are usually inversely related to each other. Hence, either decreasing the gain of the amplifier or consuming more power is the way to keep the specification.

DC-gain and GBW: By simulating the system-level of thee design in the SIC mode, using the SIC's parameters of Table 2-2, and considering a cancellation of more than 67dB, the minimum acceptable DC-gain (A_{dc0}) and GBW for the OTA must be more than 70dB and 4.4GHz, respectively. Accordingly, the TIA sub-blocks should be designed to meet these criteria. Finally, it is important to check how much effect the doublet has on the performance of the SIC block.

3.2.2 *Poles and Zeros arrangement*

The arrangement of the poles and zeros effectively define the performance of the TIA. Hence, the location of them should carefully considered and studied. As mentioned earlier, there are three poles (at the end of each OTA stage) and two zeros (one created by S_{tFF} and another one by the combination of the R_Z and C_Z).

Poles and Zero Locations: The amplitude of the TIA loop transfer-function is shown in Figure 3-9. The effect of two dominant poles and a zero effect in the performance of the

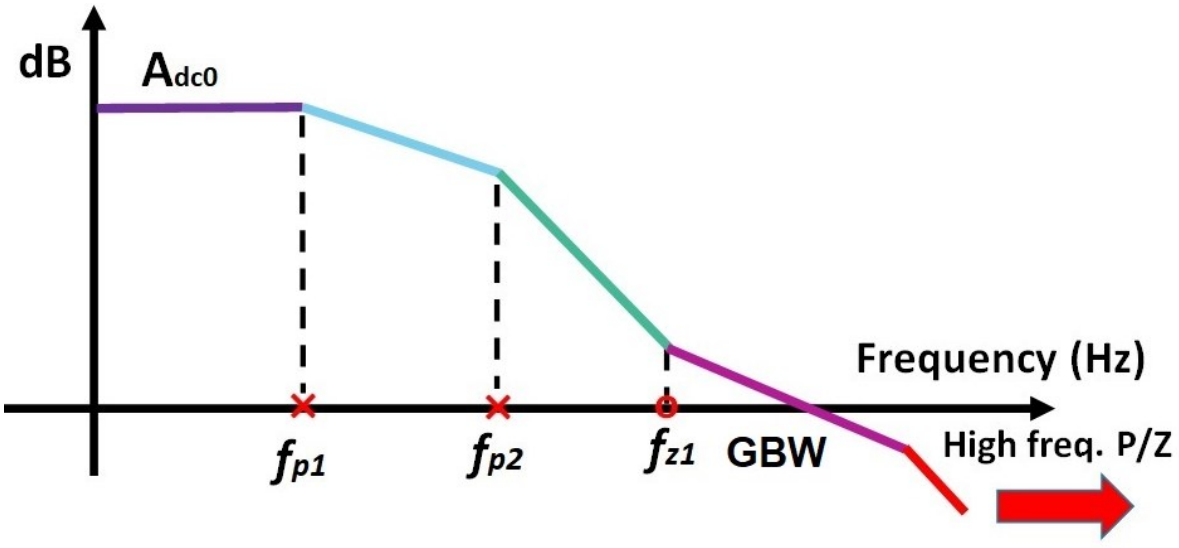


Figure 3-9 The amplitude of transfer function G-loop of the TIA employed the two poles/ one zero compensation technique.

`

TIA is visible (f_{z1} helps to adjust the phase-margin by choosing it one-third of GBW of the TIA). This method is called *two poles/ one zero compensation* [20].

High-frequency Doublet: One of the high-frequency poles, should be cancelled with one of the zeros. Among the three poles, the one at the end of the second stage has this specification in our case. Consequently, its DC-gain cannot be high as explained above. This pole-zero cancellation clearly causes a doublet but not a harmful one.

First pole: The first pole is at the end of the last stage (S_{t3}) due to large capacitor (C_Z) with moderate amount of the DC-gain.

First stage: The first stage should have higher gain to lower the input-referred-noise of the following stages. Hence, its output pole creates the second pole.

Non-dominant poles: It is important to emphasize the adverse effect of the parasitic and non-dominant poles on phase-margin, even if they are located after GBW. For example, it will be explained in the next sub-section that one of the non-dominant poles of the first stage, located at the source of the Cascode amplifier, degrades the phase-margin of the whole TIA.

3.3 Transistor-level Design of the OTA

After gaining some system-level parameters of the design in the previous section, developing in the transistor-level starts and it is important to tackle the issues in the real word such as parasitic components and mismatches [30].

Note: For simplicity, the common-mode-feedback (CMFB) and bias circuits are not shown in the transistor-level figures of the OTA's stages. The bulk pins of all PMOSs and NMOSs are connected to the Analog supply voltage (V_{ddA}) and ground (gnd_A), respectively. All the transistors are chosen from the regular (1V) RF category in the Analog part unless the opposite of it mentioned.

`

3.3.1 *First Stage (St1)*

The first is located at the input of the OTA, and it is shown with blue colour in Figure 3-8. It contributes to the DC-gain of the whole OTA. Besides, its gain should also be high enough to alleviate the input-referred-noise, V_{nOTA}, of the following stages, as shown in Figure 3-2. Hence, for lowering the noise at the output of the TIA, not only the gain of the St1 should be relatively high but also its own noise should be chosen as much as possible low. To this end, the Cascode topology is employed here, as shown in Figure 3-10. Since the supply voltage is not high enough, current reuse in both PMOS and NMOS is impossible [30]. The input common-mode voltage is set by the output of the third stage, to be equal the half of the Analog supply voltage $\frac{V_{ddA}}{2}$. The PMOS transistors are used as input ones (with ultra-low Vth) due to low input common-mode voltage (V_{cmin}=0.65V). The output pole of this stage cannot at high frequency since its

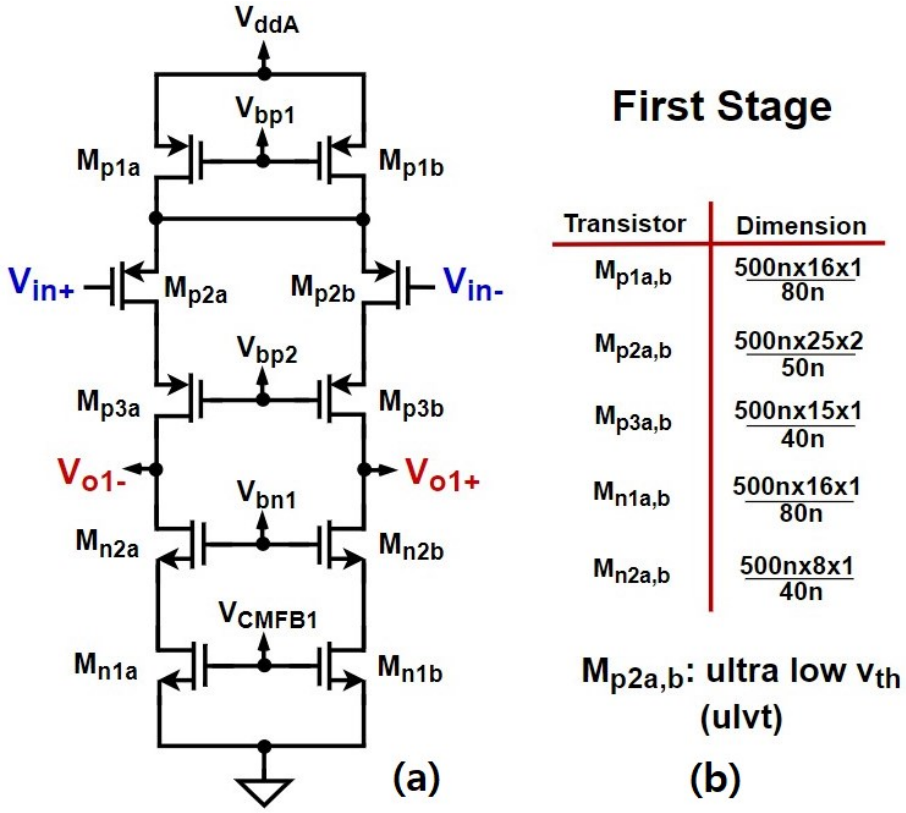


Figure 3-10 (a) First stage of the developed OTA (St1) and (b) the dimensions of the transistors.

gain is relatively high. The second pole is at the output this stage. The input-referred-noise of a PMOS or NMOS transistor is given by the formula (3-19) [30].

$$\overline{v^2}_n = \frac{4KT\times\gamma}{g_m} + \frac{k}{C_{ox}\times WL}\times\frac{1}{f} \quad \text{Eq. (3-19)}$$

Where g_m is transconductance of the transistor, $4KT \times \gamma$ is a constant, WL indicates the gate area, and f (in the second term) represents frequency. The first and second term in the Eq. (3-19) are due to Thermal and Flicker noise sources, respectively. The total input-referred-noise of St1 , with a reasonable estimation to the input-referred-noise of the following stages, is expressed by Eq. (3-20) [30].

$$\overline{v^2}_{nOTA} \approx \overline{v^2}_{nSt1} = 2\times\left(\overline{v^2}_{np2a} + \left(\frac{g_{mp1a}}{g_{mp2a}}\right)^2\times\overline{v^2}_{np1a} + \left(\frac{g_{mn1a}}{g_{mp2a}}\right)^2\times\overline{v^2}_{nn2a}\right)$$

Eq. (3-20)

Where g_{mp1a} and g_{mn1a} are transconductance of each transistor, and V^2_{np1a} and V^2_{nn1a} are the noise of the MN1a and MP1a in Figure 3-10 and given by Eq. (3-19). The input transistors, MP2a,b , are chosen PMOS type due to less Flicker noise. The dimensions of all the transistors are given on the right side of Figure 3-10. From Eq. (3-19), lowering the gate length of the top (MP1a,b) and bottom (MN1a,b) current sources will decrease the input-referred-noise of the St1 because of the reduced transconductances. The gate length of the input transistors is chosen 50-nm, there is a trade-off between its Flicker noise and parasitic pole at the source of the Cascode transistors. By choosing a large gate length for the Cascode transistors (MP3a,b – MN2a,b), St1's DC-gain rises, but the non-dominant pole at the source of the Cascode transistors decreases which leads to degradation of the phase-margin of the TIA. So, the gate length of the Cascode transistors is chosen close to the minimum, which equals 40-nm.

The DC-gain of the first stage is expressed in Eq. (3-21). Assuming that the resistance seen from the output toward the NMOS and PMOS transistors is similar the formula

`

is expressed (simplified) by Eq. (3-21). From simulations, the intrinsic gain of the transistor at low current, the technology is 28-nm CMOS technology, is around 20dB. the DC-gain of this stage is estimated around 34dB and is validated by simulation.

$$A_{St} = g_{mp2a} \times R_{o1} = g_{mp2a} \times \left[\left(r_{op2a} \times g_{mp3a} \times r_{op3a}\right) \| \left(r_{on1a} \times g_{mn2a} \times r_{on2a}\right)\right] \approx \frac{1}{2} \times \left(g_{mp2a} \times r_{op2a} \times g_{mp3a} \times r_{op3a}\right) \quad \text{Eq. (3-21)}$$

The input transconductance, $g_{mp2a,b}$, should be chosen properly for decreasing the input-referred-noise of the OTA. By simulation, the bias current and transconductance of the first stage is set to 240uA and 5m℧, respectively.

The $\frac{g_m}{I_D}$ ratio is a figure-of-merit that indicates how much power we should spend to obtain a certain transconductance. The input transistors are biased in Moderate-inversion, $\frac{g_m}{I_D} \approx 21$, which is a trade-off between efficiency, speed, and matching of the circuits. The short explanation of this stage is reported in Table 3-2 below.

3.3.2 Second Stage (St2)

The second stage, St2, is a simple one compared to other stages, and shown in Figure 3-11. This stage contributes to the overall gain but after its output is connected to the feedforward stage, StFF, the effective output impedance will decrease. As a result, the output pole will move to higher frequency. St2 should also be able to have high-swing as shown in Figure 3-8. Its noise is referred to the input by dividing it by the first stage gain, hence, it is negligible at the input. The DC-gain is mainly defined by g_{mSt2} and R_{o2}. The stage is biased at 270uA, and the DC-gain is equal to 21dB, before connecting to the StFF. The short specification is reported in Table 3-2.

`

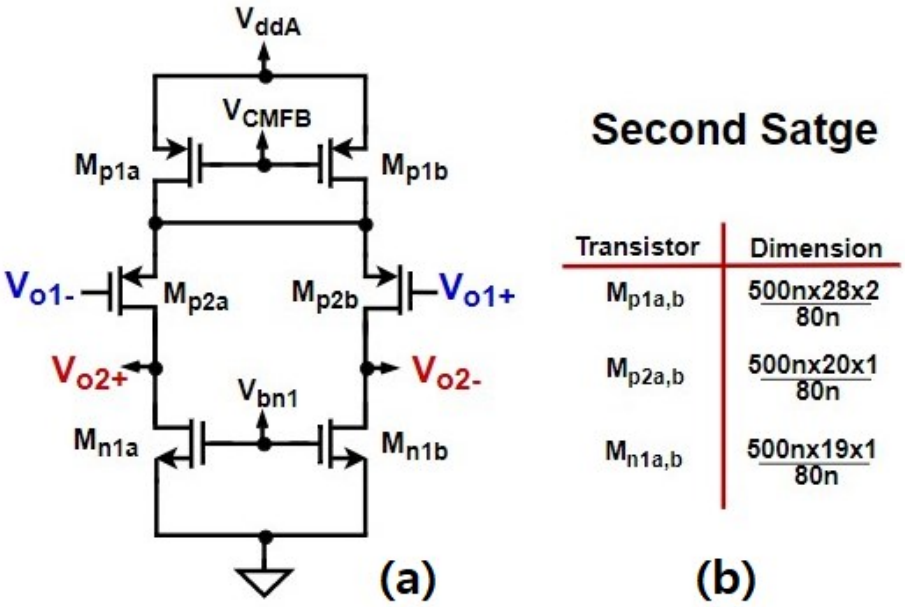


Figure 3-11 (a) Second stage ($St2$) of the designed OTA and (b) transistors' dimensions.

The dimensions of the input transistors define the capacitive load of the preceding stage; however, minimum gate length is not good choice for them because it lowers the output resistance, and the corresponding DC-gain, in Figure 3-8. Hence, the gate length is chosen 80-nm to compensate the effective output resistance seen from the parallel stages of $St2$ and $StFF$.

3.3.3 Feedforward Stage ($StFF$)

For increasing the speed and stabilizing the amplifier, it is necessary to use NCFF technique in high-speed application as explained in sub-section 3.1.3.3. To put it in another way, the $StFF$, shown in Figure 3-8, defines the high-speed operation and efficiency of the TIA. Since $StFF$ connects to the output of $St2$, the effective $Ro2$ at its output and DC-gain decrease. Accordingly, the gate length of $MP_{2a,b}$ and $MN_{1a,b}$ of $StFF$, in Figure 3-12, are chosen equal to 80-nm. The width of the transistor also increases to achieve the $gmFF$ required to implement the desired zero. However, the parasitic output capacitance of this stage should be kept low to increase the magnitude of the

`

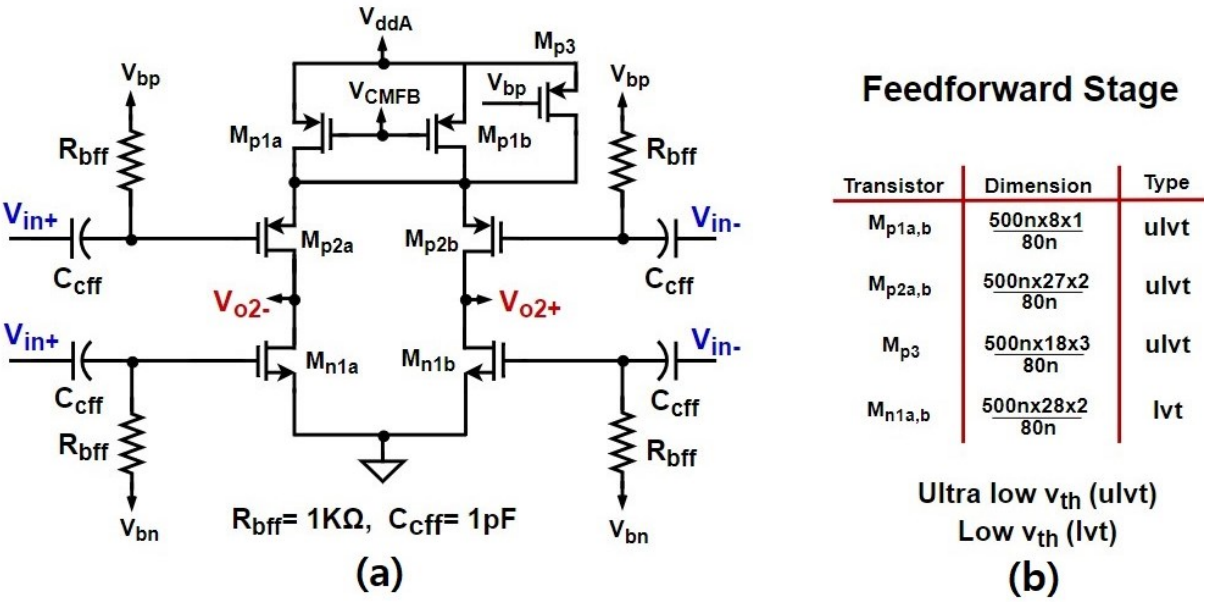


Figure 3-12 (a) Feedforward stage placed between input of the OTA (ac-coupled bias) and the output of the second-stage and (b) the transistors' dimensions.

high-speed pole. By raising the current of this stage and using the current-reuse technique, the output capacitor decreases and the necessary g_{mFF} is obtained (required zero, ω_Z) to fulfil the criteria mentioned in Table 3-1. Since the feedforward stage is connected to the input of the amplifier (its outputs are connected to the outputs of the St2) and the input common-mode voltage of the TIA is low, 0.65V, the ac-coupled bias strategy is selected to separate its bias from that of the input transistors. The PMOSs and NMOSs are selected from ultra-low Vth (ulvt) and low Vth (lvt) categories, respectively, where Vth is threshold voltage of the transistor. Since the goal is to minimize the attenuation at the input of the feedforward stage in high-frequency, after 500MHz, the 3-db frequency of the ac-coupled network is set around 160MHz by Rbff and Cceff. The amplifier is biased at 1mA, the total gmFF is equal to 26mʊ, which are reported in Table 3-2.

3.3.4 Third Stage (St3)

The output stage of the OTA is always composed of a class AB amplifier to drive the capacitive load. The developed class AB is shown in Figure 3-13. By using the current

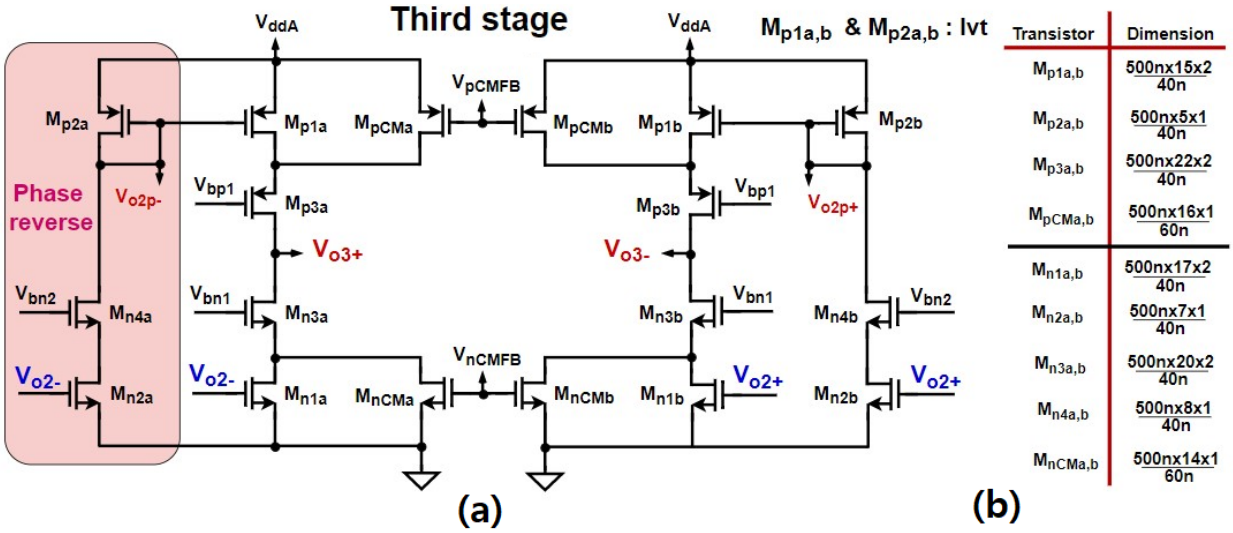


Figure 3-13 (a) Third stage of the OTA implemented as a class AB amplifier and (b) transistors' dimensions.

re-use technique, the signal is feed through both PMOSs and NMOSs, hence, the output transconductance, gm_3, is set to 25m℧ @ 1mA. The pink colour, shown in Figure 3-13, is used to indicate the reverse polarity signal for the inputs of the PMOSs. The non-dominant pole generated at the drain of $MP_{2a,b}$ (at the $V_{o2p+/-}$ nodes) can degrade the phase-margin of the TIA. It is critical to have two series transistors, in the NMOS or PMOS path, because V_{ddA}, Analog supply voltage, is more than the break-down voltage of one transistor. Its DC-gain is calculated with the formula (3-21) to be around 35dB. The dimensions of the transistor and their types are also shown in Figure 3-13. The gate length of the $MN_{1a,b}$ and $MP_{1a,b}$ are chosen low not only to decrease the loading effect on the previous stage but also to increase the speed of this stage. Finally, two CMFBs circuits are used in this stage, one for the NMOS side and another one for the PMOS side.

3.4 Simulation Results of the TIA

It is critical to have an OTA and TIA meeting the system-level specifications for cancellation. Therefore, the dynamic and static simulations' result should be considered.

Table 3-2 The operating points and small signal parameters of each stage of the OTA.

	S_{t1}	S_{t2}	S_{tFF}	$S_{t2}+S_{tFF}$	S_{t3}	R_Z/C_Z
Current consumption (mA)	0.24	0.27	1	-	1.2	-
Trans conductance (mʊ)	5	4	26	-	24	-
Output pole (MHz)	220	-	-	2000	3.6	-
Created Zero (GHz)	-	-	-	2.2	-	1.8

Before showing the results of the developed TIA, the parameters of the four stages, including current consumption, are collected from Cadence and presented in Table 3-2. The two poles/ one zero compensation concept is clearly shown and explained in the table above and Figure 3-8. There are other non-dominant poles or doublet pole–zero, such as the doublet in the feedback path created by Z_F, that are not mentioned in the table.

3.4.1 Testing the Stability of the TIA

The open-loop tests help us to evaluate the stability of the TIA. The test-bench for this simulation is shown in Figure 3-14. As it is clear in the figure, the whole TIA is shown

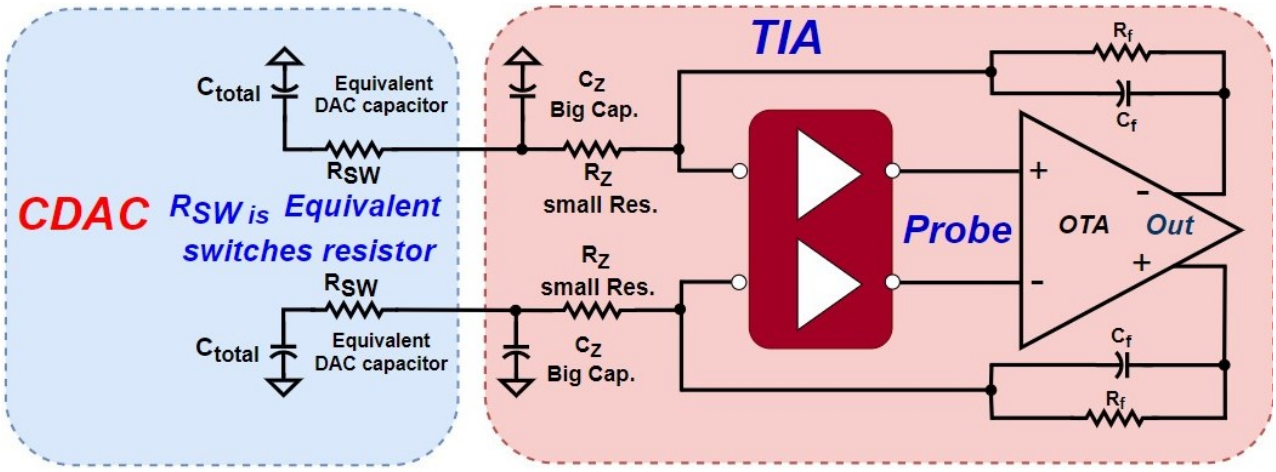


Figure 3-14 The test-bench for evaluating the open-loop performance.

in the pink box at the right-side of the figure, and probe is located at the inputs of the OTA. Plus, the equivalent circuit of the CDAC is also connected to the inputs of the TIA to have a realistic model. The model includes a series resistor and capacitor representing equivalent resistance of the switches and total capacitance of the CDAC, respectively. Figure 3-15 (a) and (b) show the open-loop magnitude and phase of the TIA. According to these graphs, the DC-gain, GBW, and phase margin are about 75dB, 4.3GHz, and 61.5°, respectively, these numbers meet the system-level specifications gained in sub-section 3.2.1. The phase margin, between 45° to 90°, guarantees a good time domain response. The effect of the zero, which aim to improve the phase-margin is shown in the figure. It is also critical to realize whether the doublet can cause a major issue or not. The main pole-zero doublet occurs around the feedback pole/ zero of the TIA (≈50MHz). The magnitude of the open-loop gain, AOL, at this frequency is critical, as mentioned in 3.1.3.2. This open- loop gain is equal to $|A_{OL}| = 51dB$ in Figure 3-15 (a) which can attenuate enough the amplitude of the slow component in the time domain response, for N=10-bit DAC, as explained in sub-section 3.1.3.2.

Finally, the common-mode stability must be checked here according to the test-bench of Figure 3-14. Because the amplitude of common-mode signal never goes beyond 0dB it cannot cause a common-mode instability issue.

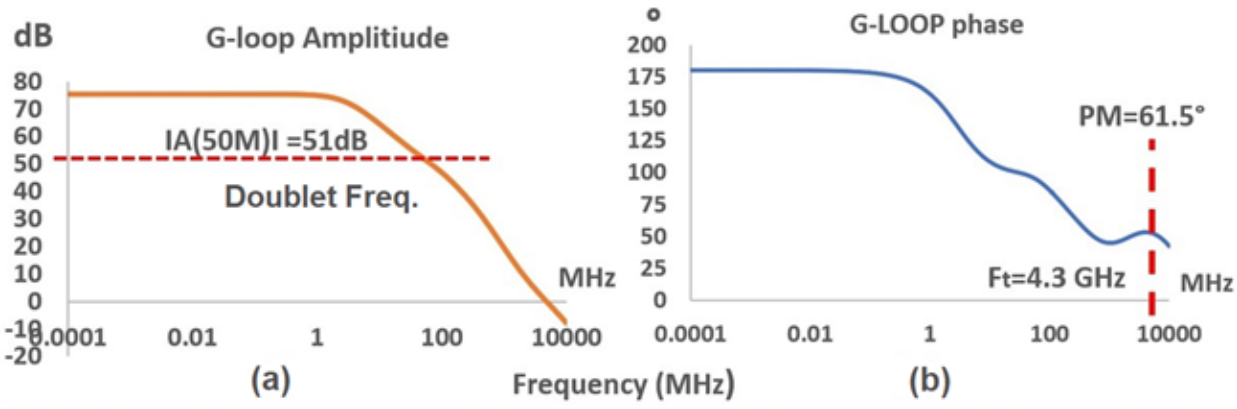


Figure 3-15 G-loop graph of the TIA according to the test-bench above (a) magnitude in dB and (b) phase response in degree.

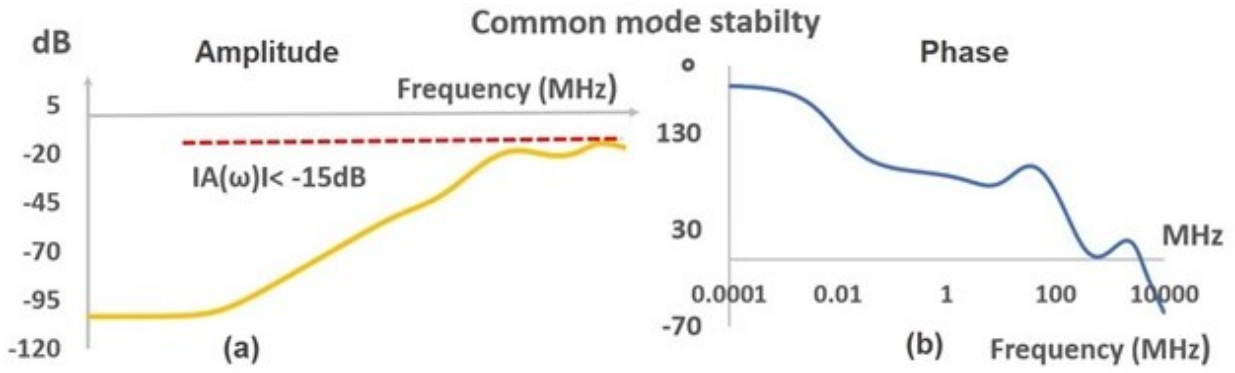


Figure 3-16 Common-mode simulation result of the test-bench shown in Figure 3-14 (a) amplitude in dB and (b) phase response in degree.

The TIA will be employed to perform cancellation by charging and discharging the CDAC. Hence, the TIA plays a key role to keep the settling-time less than half of the clock period for the CDAC. The test-bench is developed to measure the settling-time is shown in Figure 3-17. To have a real simulation, the loading effect of the CDAC is also consider in the model. The TIA is connected to the model of the CDAC via two switches. The switches are open, and capacitors are pre-charged. Then, they will be closed at the time of 1ns. The differential waveform at the top of capacitor Ctotal is shown by the green arrow in Figure 3-17. The settling-time for N=10-bit accuracy is obtained when the voltage is in a band equal to 0.1% of the voltage step.

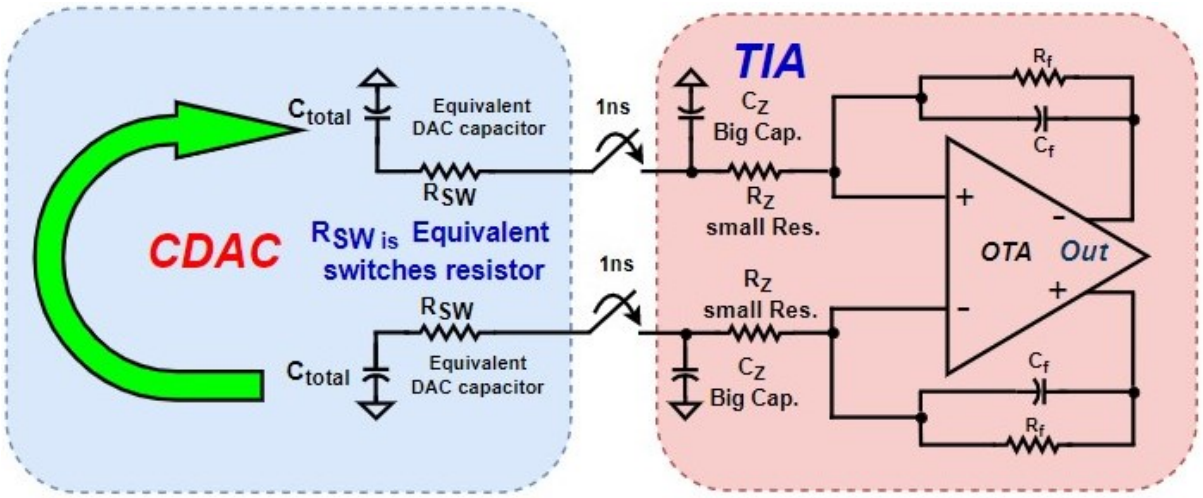


Figure 3-17 The test-bench used for measuring the settling time.

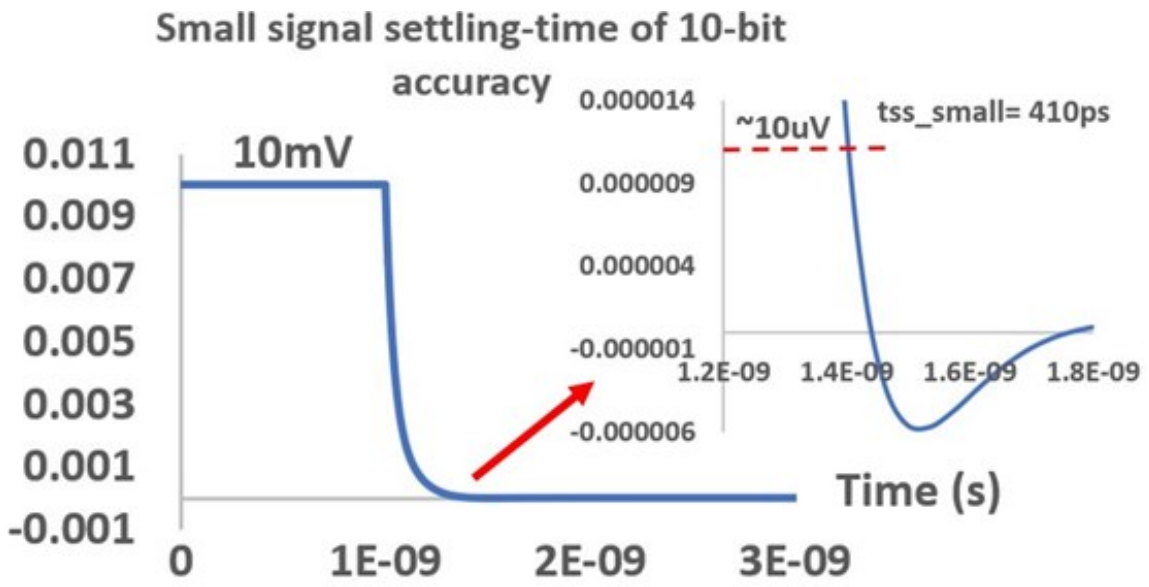


Figure 3-18 Small-signal settling-time response of Figure 3-17.

In the first simulation, the capacitors are pre-charged to 10mV differentially to measure the small-signal settling-time (T_{SMss}). The simulation result in the time domain is shown in Figure 3-18. The time required for the voltage to fall below 10uV (0.1% band) happens after T_{SMss}=410ps.

For analysing the large-signal behaviour of the system, another simulation will be done. The capacitors are initially pre-charged to 700mV differentially i.e., the full-scale voltage across the CDAC. After closing the switches at 1ns, the voltage across capacitors settles. The large-signal settling-time (T_{LGss}) is measured in Figure 3-19, for 0.1% accuracy (700µV). T_{LGss} is equal to 418ps which is close to T_{SMss} number. It is a good indication about the TIA's behaviour (linearity). The area when the voltage become lower than 700µV (equals N=10-bit) is enlarged in the right side of the figure. Figure 3-18 and Figure 3-19 have more information about the performance of the TIA. The differential voltage across the C_{total} starts decaying quickly through R_{SW} and after reaching the peak in both simulations, the waveform slowly settles via the TIA.

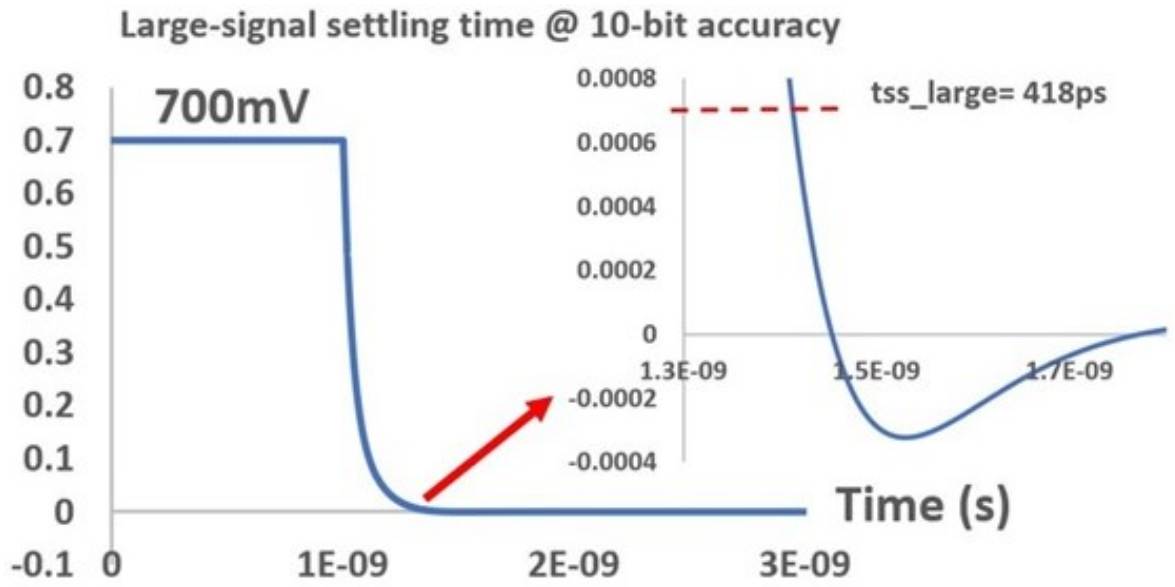


Figure 3-19 Large-signal settling-time response of Figure 3-17.

The small- and large-signal settling-time are less than 500ps; hence, the DAC's clock frequency is equal to 1GHz (FS). To relax the TIA design, it is critical to have time-interleaved (TI) to be able to support a 2GHz (clock).

3.4.3 Noise of the TIA

The noise contribution of the TIA and CADC should be analysed since they can degrade the signal-to-noise-and-distortion-ratio (SNDR) of the whole design. The noise of the TIA arises from different terms, according to Figure 3-20, the output noise of the TIA is expressed as follows:

$$\overline{v^2}_{nTIAOut} = \overline{v^2}_{nOTAOut} + \overline{v^2}_{nRFOut} \quad \text{Eq. (3-22)}$$

Where $\overline{v^2}_{nOTAOut}$ and $\overline{v^2}_{nRFOut}$ $(\frac{V^2}{Hz})$ are referred to the generated noise by the OTA and feedback resistor at the output. The major contribution of the output noise comes from the OTA [30]. For the test bench of Figure 3-2 the simulation result is shown in Figure 3-20 where the frequency varies between 100KHz to 100MHz.

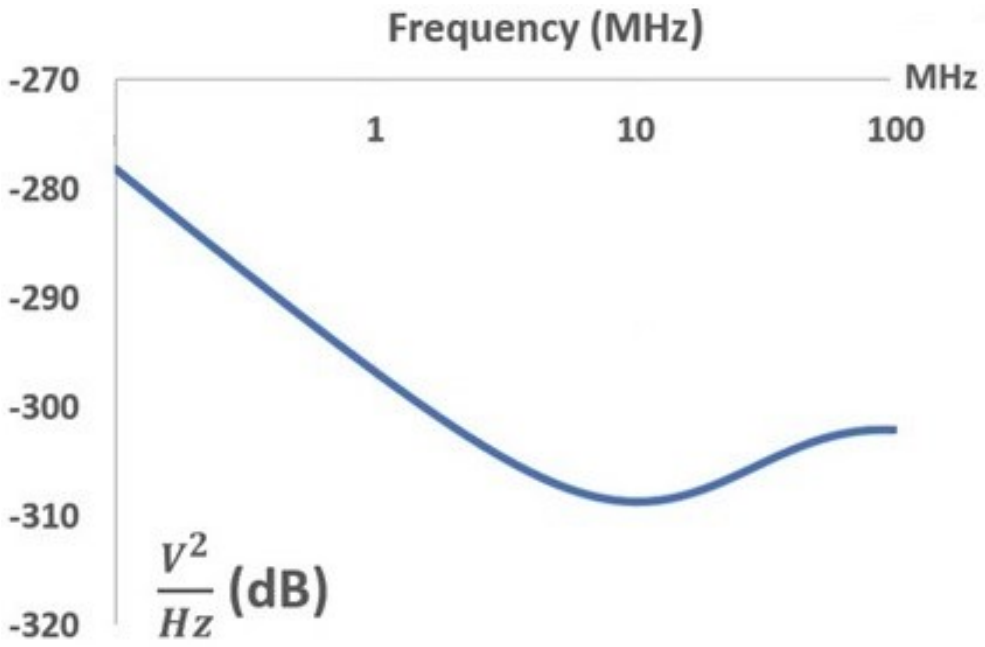


Figure 3-20 TIA's output noise of the vs. frequency range lower than 100MHz.

There is a zero shown in the waveform of Figure 3-20 around 10MHz. Eq. (3-1) also explain this effect. The total output-integrated-noise is equal to 125μV if the frequency varies between 100KHz to 40MHz (BW_{BB}).

The breakdown of the input-referred-noise of the OTA, with reference to Figure 3-2, is shown in Figure 3-21. The terms Cs and Cas correspond to current source and input transistors in the figure below, respectively. Likewise, the Therm and Flicker also indicates the noise of Thermal and Flicker, respectively. For example, Cas_Flicker, shown with blue colour in Figure 3-21, means the Flicker noise of the input transistors, and it has major share of the input-referred-noise. It can be lowered increasing the dimensions of the input transistors but with a larger input capacitor. This decreases the pole seen from the source of the Cascode transistor and degrade the phase-margin of the amplifier. Hence, this is the reason that the Flicker noise of the input transistors is dominant.

`

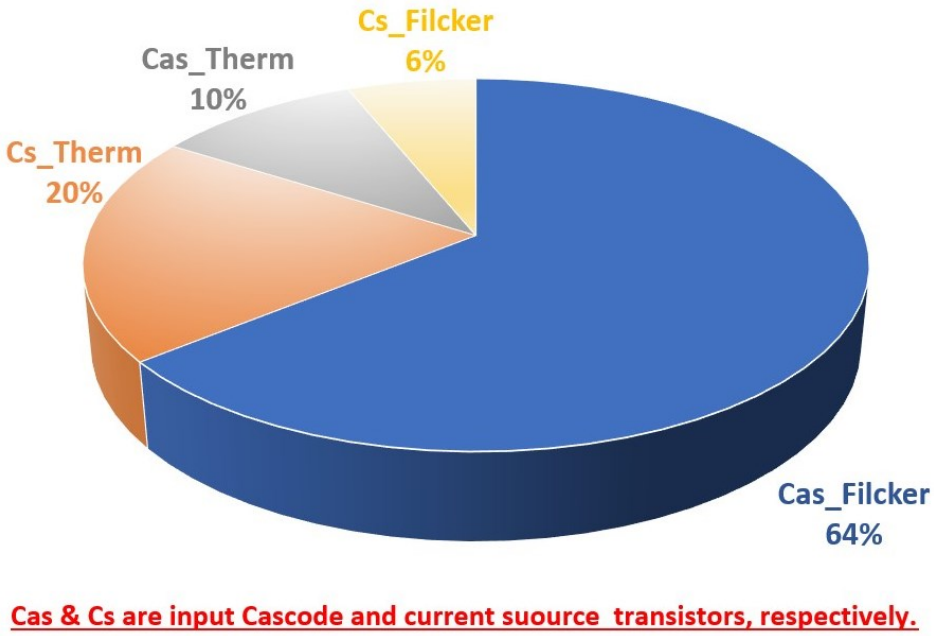


Figure 3-21 Noise breakdown of the TIA's input-referred-noise.

3.4.4 Input Impedance of the TIA

As explained earlier, the input impedance of the TIA is critical in the current-mode receivers. The orange curve, in Figure 3-22, gives to the total impedance (in dB) seen from the input of the TIA, called Zin in Figure 3-1, and its magnitude is equal to 20Ω. The blue colour represents the impedance seen after RZ toward the inputs of the OTA. Zin starts growing after 200MHz. On the other hand, the CZ has dominant effect after a few GHz. It is shown in Eq. (3-12) that the poles of the transfer function of the TIA make the value of Zin to increase.

3.4.5 TIA operating points

Some of the important features of the TIA are summarized in Table 3-3. The reported parameters are obtained by simulation and meet the system-level requirements to perform SIC.

`

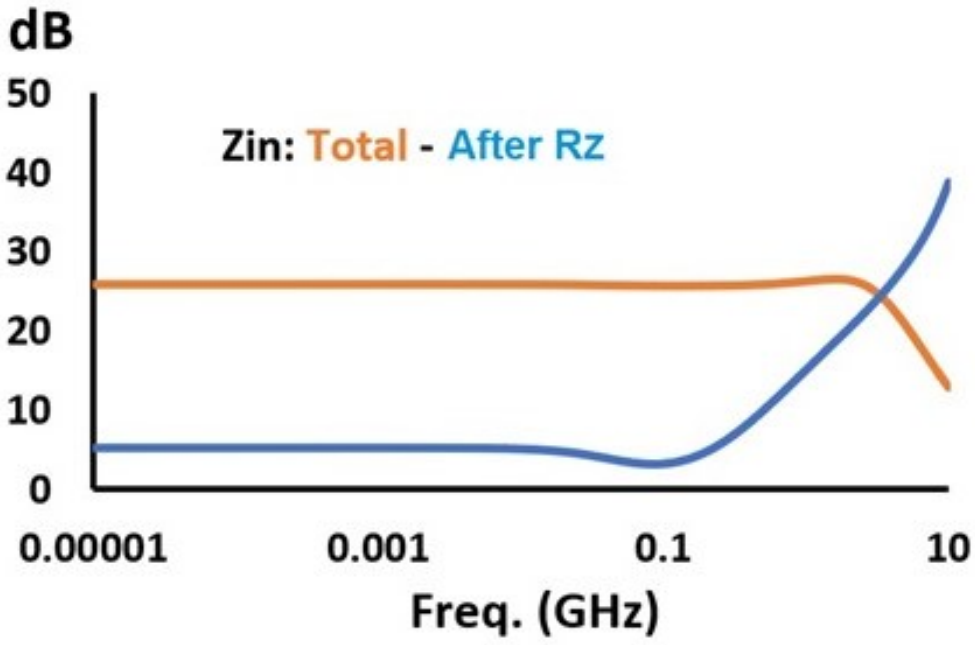


Figure 3-22 (Orange colour) total input impedance of the TIA and (blue colour) shows the impedance seen after RZ including FB.

Table 3-3 Summary specifications of the TIA's operating points.

Vdd (V)	DC Power (mW)	DC-gain (dB)	GBW (GHz)	PM* (°)	IRN+ (µV)	IB^ OIP3^ (dBm)
1.3	9	75	4.3	61.5	125	25

*PM: Phase-margin

+IRN: input-referred-noise, the frequency (integration) range: 100K to 40MHz.

^IB: In-Band.

4 Capacitive DAC (CDAC)

The main purpose of the data converters is to bridge the gap between the Analog and digital world. Signal processing is broadly utilized in various fields, such as audio, communication, and medical systems. The DACs' specifications are explained in this chapter. Then, more details are given with regards to the proposed DAC to perform the SIC such as matching, noise, and switching style. Finally, the transistor-level information of the designed CDAC is presented.

4.1 Theoretical Background

One of the main blocks of the SIC is the high-speed DAC. As argued in sub-section 3.13.1, the CDAC is a suitable kind of DAC for our application to do cancellation. Nowadays, it is commonly used to generate the Analog signals in medium-resolution designs and in various kinds of applications such as SAR ADC. It is composed of an array of capacitors, switches, and logic circuits.

4.1.1 Ideal DAC Response

In the time domain, the DAC produces the discrete-time Analog signals, either in voltage or current mode. The DAC's output value will be held constant, defined by the input code, until the end of or for a fraction of each period. Then a filter follows the DAC to re-construct the continuous-time signal by removing the high frequency components. If x(t) is a BB signal with limited-band, BW and $f_s > BW$, a sampled version of it is represented by $x_s(t)$. The small and capital letters represent time domain and Fourier transformation of the signal.

`

$$x_s(t) = x(t) \times x_\delta(t) = \sum_{n=-\infty}^{n=+\infty} x(t) \times \delta(t - nT_s) = \sum_{n=-\infty}^{n=+\infty} x(nT_s) \times \delta(t - nT_s) \quad \text{Eq. (4-1)}$$

$$X_s(f) = X(f) * X_\delta(f) = \frac{1}{T_s} \sum_{n=-\infty}^{n=+\infty} X(f - nf_s) \quad \text{Eq. (4-2)}$$

Where T_s and f_s are period and frequency of the sampling clock, n is an integer number, $\delta(t)$ is the Dirac function, and $x_\delta(t)$ is the impulse train function.

A real DAC is not able to provide ideal impulses at its output. In fact, the impulses pass to a sample-and-hold, reconstruction block, to keep the value of the impulses for one clock period or fraction of it. By using Eq. (4-1) and (4-2) and convolving $x_s(t)$ with the sample-and-hold mathematical function $p_{SH}(t)$ in the time domain and multiplying them in the frequency domain, the output signal of the DAC, called $x_{DAC}(t)$ is represented as follows [31].

$$x_{DAC}(t) = p_{SH}(t) * x_s(t) = p_{SH}(t) * [x(t) \sum_{n=-\infty}^{n=+\infty} \delta(t - nT_s)] \quad \text{Eq. (4-3)}$$

$$X_{DAC}(f) = P_{SH}(f) \times \frac{1}{T_S} \sum_{n=-\infty}^{n=+\infty} X(f - nf_s) \quad \text{Eq. (4-4)}$$

4.1.2 NRZ and RZD DAC

The sample-and-hold can have various kinds of shape such as zero-order hold. Non-return-to-zero (NRZ) and return-to-zero (RZ) are two well-known types of zero-order-hold (ZOH) to implement sample-and-hold block.

The NRZ method holds the same value until the next clock, each output lasts one complete T_s , but the RZ technique keeps the output value for a faction of T_s, for example it lasts $\frac{T_s}{2}$. The time (left) and frequency (right) responses of the NRZ DAC is

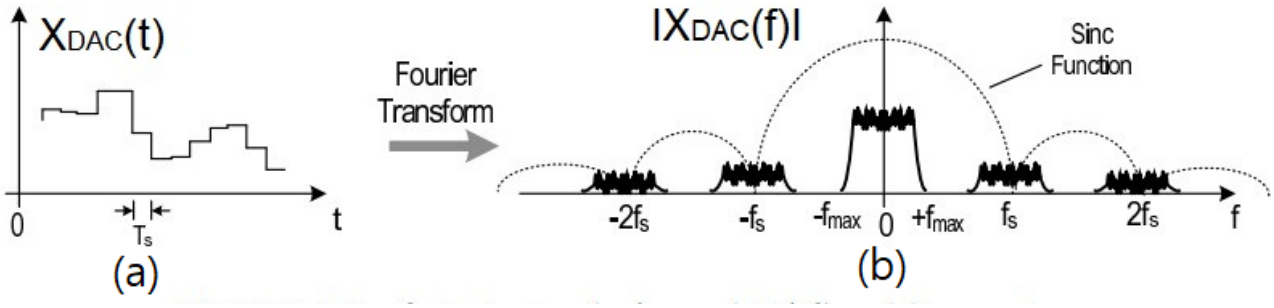


Figure 4-1 Response of a NRZ DAC, the (a) time and (b) frequency domain [31].

shown in Figure 4-1 (left) and (right) [31], respectively. The frequency response of the NRZ and RZ (the half period pulse width RZ) sample-and-hold are calculated and shown below.

$$P_{SHNRZ}(f) = \frac{T_s}{1} \times \frac{\sin\left(\frac{\pi f}{f_s}\right)}{\frac{\pi f}{f_s}} \times e^{\left(-j\frac{\pi f}{f_s}\right)} = T_s \times Sinc\left(\frac{\pi f}{f_s}\right) \times e^{\left(-j\frac{\pi f}{f_s}\right)} \quad \text{Eq. (4-5)}$$

$$P_{SHRZ}(f) = \frac{T_s}{2} \times \frac{\sin\left(\frac{\pi f}{2f_s}\right)}{\frac{\pi f}{2f_s}} \times e^{\left(-j\frac{\pi f}{2f_s}\right)} = \frac{T_s}{2} \times Sinc\left(\frac{\pi f}{2f_s}\right) \times e^{\left(-j\frac{\pi f}{2f_s}\right)} \quad \text{Eq. (4-6)}$$

Where differences between NRZ and RZ are mentioned in Table 4-1. *The designed CDAC works in RZ-mode.*

By combining the Eq. (4-4) and (4-5) the effect of the NRZ is also portrayed in Figure 4-1 and Figure 4-2. It includes the roll-off characteristics of the *Sinc* function which attenuates the harmonics and image frequencies [32].

It is worthy to shed more light on the NRZ frequency response. A Nyquist zone is mentioned in Figure 4-2. It corresponds to an integer number of frequency bands $\frac{f_s}{2}$ wide, where f_s is the DAC's sampling rate. For example, the 1st Nyquist zone extends from DC to $\frac{f_s}{2}$ and the 2nd Nyquist zone extends from $\frac{f_s}{2}$ to f_s and so on. Important note is that even Nyquist zones have a mirrored spectrum [33].

Table 4-1 Comparison between a NRZ and RZ sample-and-hold function [31]-[32].

	DC amplitude	Flattened Band	Filtering of the images
NRZ	1	1	sharper
RZ	0.5	x2	less

`

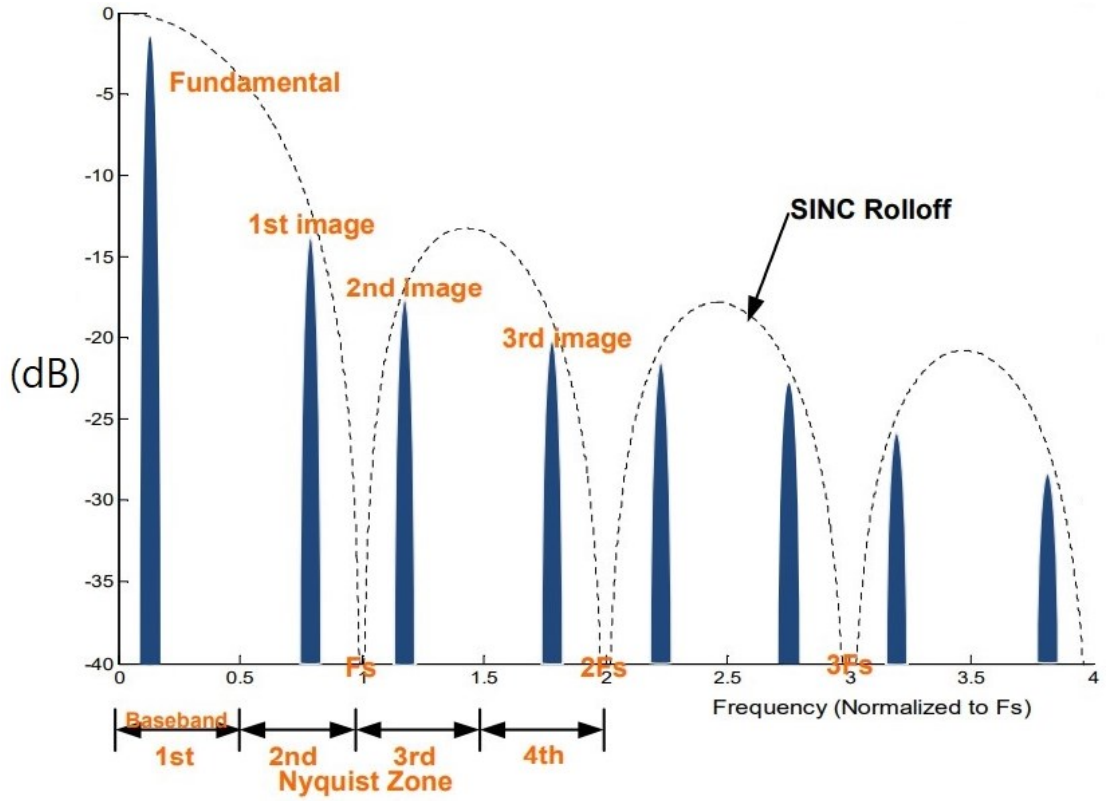


Figure 4-2 Amplitude of a NRZ sample-and-hold in the frequency domain [32].

When the DAC clock, f_s , is used to synthesize the BB signal at f_0, it results in image replicas at $f_s \pm f_0$, $2 \times f_s \pm f_0$, $3 \times f_s \pm f_0$, etc [34]. The rectangular sample-and-hold operation of the DAC results in a *Sinc* response at its output, as explained by Eq. (4-5) and illustrated in Figure 4-2 (the attenuation at $\frac{f_s}{2}$ is 2.4dB). It is observed that there are spectral nulls at multiples of f_s. As the desired signal f_0 moves near $\frac{f_s}{2}$, its sampling image replica also moves closer to $\frac{f_s}{2}$. At near-Nyquist operation, the signal and replica components close to $\frac{f_s}{2}$ are quite comparable in magnitude. Hence, the replica acts as a strong interferer to the signal of the interest. The nonlinear effects in the DAC are also well pronounced at close-to Nyquist operation, resulting in harmonic emissions and intermodulation products to occur at the output of the DAC. The combination of image replica and nonlinearity spurs results in stringent filtering

requirements or limit the instantaneous bandwidth of the DAC to well below the Nyquist frequency [34].

4.2 Performance Figure-of-the-merits

Plenty of architectures are used to convert the digital words to the Analog signals. Based on the requirements of the applications, a certain DAC architecture is chosen with a given BW_{BB}, power-consumption and area. To analyse the DACs' performance, it is vital to have the different metrics to explore various design's limitations such as speed and mismatch error. Here, some of them will be explained.

4.2.1 Quantization Noise

The theory of quantization is broadly discussed in literature. The quantization error is defined as deviation of the DAC output signal $x_R(nT_s)$ from the desire signal $x_I(nT_s)$ as follows.

$$e_Q = x_R(nT_s) - x_I(nT_s) \quad \text{Eq. (4-7)}$$

The quantization noise has Gaussian distribution and spread uniformly over the Nyquist BW, namely DC to $\frac{f_s}{2}$.

4.2.2 Oversampling Effect

From the Nyquist theorem the bandwidth of the sampled signal is constrained to half of the sampling rate. In case the sampling frequency is much higher than the Nyquist requirement, oversampling occurs. OSR is defines in sub-section 2.6.3 and Eq. (2-14), $\left(OSR = \frac{f_s}{2 \times BW_{BB}}\right)$. The amount of quantization noise power depends not only on the resolution of the DAC but also on the OSR. Since the noise power is the same in Nyquist and oversampled DAC, the height of the noise spectrum in the oversampled case must be less than the Nyquist sampled case in order to maintain the same area. As a result, the signal to noise ratio is greater in the former. By modification of Eq. (2-

`

15), the signal power to the quantization noise power metrics in dB is defined below [35].

$$SQR = 6.02b + 1.76 + 20 \times \log_{10}(FFS) + 10 \times \log_{10}(OSR) \quad \text{Eq. (4-8)}$$

Where b is the resolution of the DAC, FFS is the ratio of the DAC peak signal to the full-scale, and OSR comes from the formula (2-14). *The SNDR and SNR are also defined in section 2-2.*

4.3 Capacitive Array

The capacitive-array is the core of the CDAC and works in the return-to-zero mode. Its resolution is calculated in sub-section 2.6.3.1, being equal to 10-bit with clock frequency of 2GHz to meet the SIC criteria, however, it is very tough to design the TIA having a settling-time of less than 250ps (half of the clock frequency of 2GHz). Therefore, the clock frequency of the CDAC is kept to 1GHz and the time-interleaved (TI) technique is used here relax the design of the TIA.

4.3.1 CDAC Structure

Various kinds of topologies are available to build a CDAC. The conventional binary-weighted and C-2C technique are the simplest method to implement the DAC, but they suffer from accuracy limitations when targeting resolution between 8 to 12 bits due to parasitic capacitors and other reasons [36]. As an example, if the resolution rise, above 8-bit, in the binary-weighted array the ratio between the most-significant-bit (MSB) and the least-significant-bit (LSB) becomes too large and many critical limitations will arise. Some the negative downsides are as follows. Impossibility of scaling the switches size down to the LSB, parasitic capacitance effect, matching

`

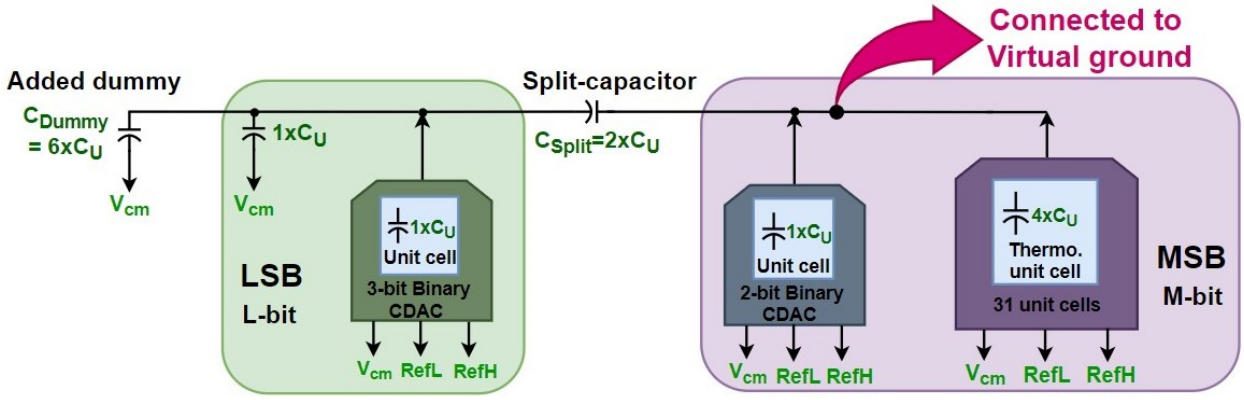


Figure 4-3 Modified version of a conventional split-capacitor CDAC, Signal-ended schematic [16].

between LSB and MSB capacitance difficult to ensure. To avoid part of the mentioned issue in a medium to high-resolution design, an array of capacitance with split-capacitor (bridge-capacitor), C_{Split}, is a good candidate. It divides the DAC into two different parts. Left-side and right-side of the split-capacitor are called LSB-side and MSB-side, respectively. The single-ended schematic of such a CDAC is shown in Figure 4-3. The LSB- and MSB-side are shown with green and pink box in the figure.

There are two critical issues i.e., non-equal bottom/ top parasitic capacitance and fractional value of the split-capacitor. The negative effect of the former is trivial in this scheme because the top-plate of split-capacitor is always connected to the virtual ground and the parasitic capacitance of the bottom-plate is negligible compared to LSB-side capacitance. It is important to give more information why the parasitic capacitance is low in the LSB-side. The ratio of the parasitic capacitance to the available one, in the used process-design kit (PDK), is less than 0.6 percentage, which is enough for the required precision according to simulations reported in Ref. [36]. To deal with the latter issue, there are ways to eliminate the negative effects of the fractional value capacitance.

All the capacitors of the array have multiple of the unit capacitor (C_U). By adding a dummy capacitor with a certain value, called C_{Dummy}, in the LSB-side of Figure 4-3, the size of the split-capacitor is made equal to an integer multiple of the C_U although

`

it reduces the dynamic range. The relationship between multiple of the dummy capacitor, the multiple of split-capacitor, and the number of bits of the sub-DAC at the LSB-side in Figure 4-3 is obtained from the formula (4-10) [37].

$$\alpha_{Split} = \left(\frac{2^L}{2^L-1} + \frac{\alpha_{Dummy}}{2^L-1}\right) \quad \text{Eq. (4-9)}$$

Where α_{Split} is the multiple of the split-capacitor, L indicates the number of bits of sub-DAC in the LSB-side of the split-capacitor and α_{Dummy} is the multiple of the dummy capacitor located in the LSB-side of the of the split-capacitor [37]. For example, in the case of Figure 4-3, the LSB-side has 3-bit, L=3, then C_{Split} and C_{Dummy} are equal to 2×C_U and 6×C_U, respectively.

4.3.2 Segmentation Technique

This sub-section argues the point of minimizing the chip area under the restriction of (10-bit CDAC) static and dynamic performances. The conventional binary-weighted (Bin-W) DAC occupied less area and need simpler coding logic circuits compared to thermometric-coded (THco) DAC. However, the former suffers from glitch and non-linearity compared to the latter. Since the THco DAC takes up a large area and requires complex and power-hunger logic (decoders) circuits, the segmentation technique is a suitable compromise. According to Ref. [38], for a 10-bit segmentation DAC an optimized architectures can be to divide it into five lower-bit (*binary-weighted*) and five higher-bit (*thermometer-coded*). The mentioned configuration, 5bit+5bit, is modified to use in the split-capacitor CDAC topology. The details of the sub-blocks of the CDAC are given in Table 4-2, including the topology of each block and its total

`

Table 4-2 Summary of the developed CDAC [29], [38].

Block	Green	Dark blue	Violet
Number of bits	3-bit	2-bit	5-bit
Architecture	Binary	Binary	Thermometric
Multiple integers of the Cu*	1+2+4	1+2	31×4

* $C_{Split}=2\times C_U$ - $C_{Dummy}=6\times C_U=(2+4)\times C_U$.

capacitance, the designed CDAC includes 3-bit conventional Bin-W in the LSB-side, 2-bit conventional Bin-W in the part of the MSB-side, and 5-bit THco in the MSB-side.

As presented in Table 4-2, the capacitive array just consists of (C_U, $2\times C_U$, $4\times C_U$). In fact, the layout and design of the CDAC is based on a thermometric cell and other cells or dummies are obtained by changing the thermometric cell. Hence, it makes drawing the layout simpler and improve linearity. More information is given about this topic in the last chapter.

4.3.3 Switching Scheme of the CDAC

Two capacitive-array are used in our design and each one is connected to one of the TIA's inputs and each one works in the TI configuration. As pointed out in the previous sub-section, the capacitive-array is comprised of 3Bin-W+ 2Bin-W+ 5THco. To build each sub-DAC, a switched-capacitor (SC) unit cell (basic cell) is defined as shown in Figure 4-4. All the cells are built by making a minor modification in this cell.

The working mode of the SC unit cell is explained as follows.

First, in *phase* $\emptyset_1$, P_{chr}, both capacitors are charged around common-mode voltage by switches named $\emptyset_1$. Second, as shown in Figure 4-4, in *phase* $\emptyset_2$, P_{disch}, both capacitors are discharged to the virtual ground. The polarity of the connection to the virtual

`

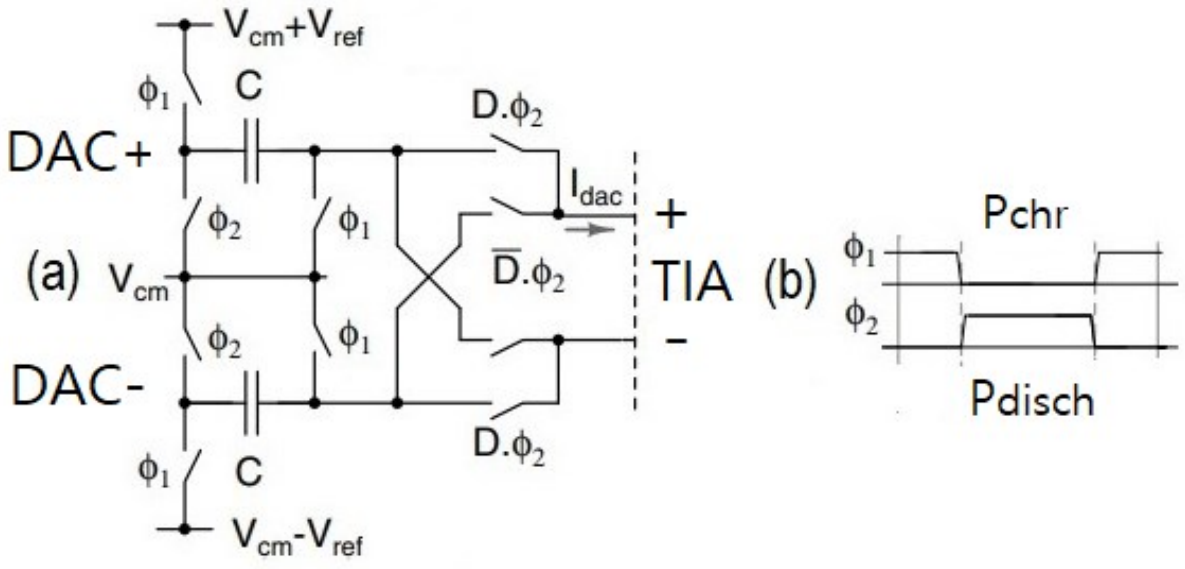


Figure 4-4 (a) Schematic of a SC unit cell (b) two non-overlapping clock [39].

grounds is chosen according to the input digital bits. The SC block works with two non-overlap clocks, shown in Figure 4-4 (b). The delay version of the clock is not used here because the switching scheme does not work in a stary insensitive mode. This reduces the number of clocks' wiring, helps distribute the clock efficiently across the chip and lowers the crosstalk.

The LSB-side has a little difference compared to the MSB-side. The capacitors are charged in the same according to the corresponding bits. Butterfly switches are not used in the LSB-side.

Before explaining the switching scheme, the following comments help understand the switching style.

1) Common-mode voltage (Vcm): It is a constant-voltage equal to the common-mode voltage of the TIA, 0.65V.
2) Low-voltage reference (RefL): It is constant reference, 0.3V, and corresponded to the zero logic. It is $-V_{ref}$ (-0.35V) below Vcm.
3) High-voltage reference (RefH): This voltage is constant (1V) and associated with the logic 1. It is $+V_{ref}$ (0.35V) above Vcm.

`

4) The top- and Bottom-plates of the two dummy capacitors in the LSB-side, 6×CU and 1×CU, are always connected to bottom-plate of the split-capacitor and Vcm, respectively.
5) The top-plate of the split capacitor is always connected to the input of the TIA, approximately virtual ground.
6) *There are two capacitive-array in the design working in the TI mode without using any calibration technique as shown in* Figure 4-9 *(This is explained in more details in the time-interleaved section and in* Table 5-1*).*
7) Each capacitor array includes two sub-DACs, namely, CA_A and CA_B. The positive plate of the split-capacitor CA_A and CA_B are always connected to the positive input (Vir+) and the negative one (Vir-) of the TIA, as shown in Figure 5-7, respectively.

4.3.4 *SC DAC Working Phases in the SIC Mode*

- *Charging phase (Pchr)*: The charging procedure of CA_A and CA_B is explained as follows. The top-plate of CA_A and CA_B are connected to $V_{cm} + V_{ref}$ and $V_{cm} - V_{ref}$ in the MSB-side, respectively, as shown in Figure 4-5. The top-plate of the capacitors in the LSB-side and bottom-plate of the split-capacitor are connected to Vcm. On the other hand, the bottom-plate of the capacitors in CA_A and CA_B are connected to the Vcm. The bottom plate of the L-bit DAC in Figure 4-3 and the two dummy capacitors are connected to the corresponding

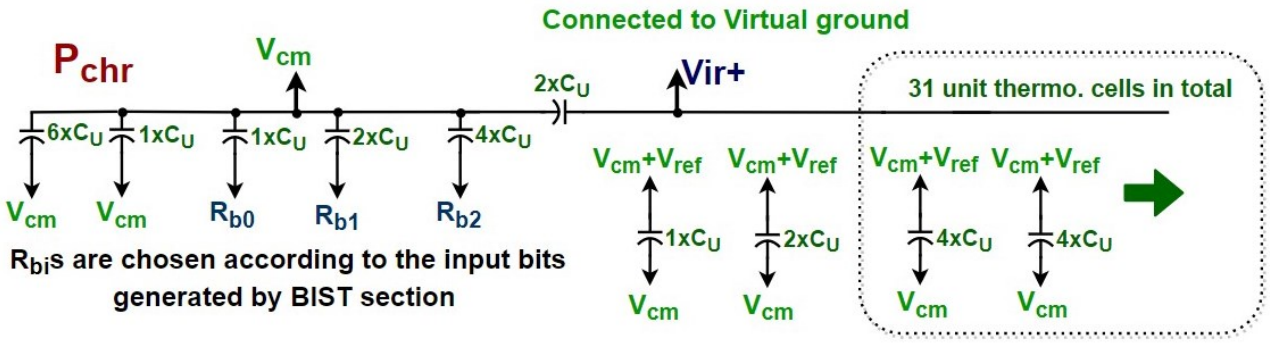


Figure 4-5 Charging phase, *Pchr*, of the CDAC (single-ended version) [16].

3 least-significant-bit ($b_2b_1b_0$), generated by the digital interface, and to V_{cm}, respectively.

- *Discharging phase (P_{disch})*: The stored charged is delivered to the TIA in the discharge phase, as shown in Figure 4-6. In the MSB-side, the top-plate of the CA_A and CA_B are connected to either Vir+ or Vir-, depending on the bits generated in the digital interface. For example, if "b_5=1" and "b_6=0", logic valuve, the corresponding capacitor are connected to the Vir+ and Vir-. The bottom-plate of all capacitors are connected to the V_{cm} except split-capacitor.

The working algorithm is slightly different in the stand-alone DAC. It will be explained later.

4.3.5 *Practical Points*

To design the capacitive-array for the SIC, the following practical points can be helpful.

4.3.5.1 *Capacitive-array Charging Formula:*

The total delivered charge for cancelling the SI depends on the input code, the unit capacitance, and the reference voltage values $\pm V_{ref}$. The formula is expressed in the formula (4-10).

$$Q_{SIC} = \frac{\Delta \times C_U}{8} \times (512d_9 + 256d_8 + 128d_7 + 64d_6 + 32d_5 + 16d_4 + 8d_3 + 4d_2 + 2d_1 + d) \quad \text{Eq. (4-10)}$$

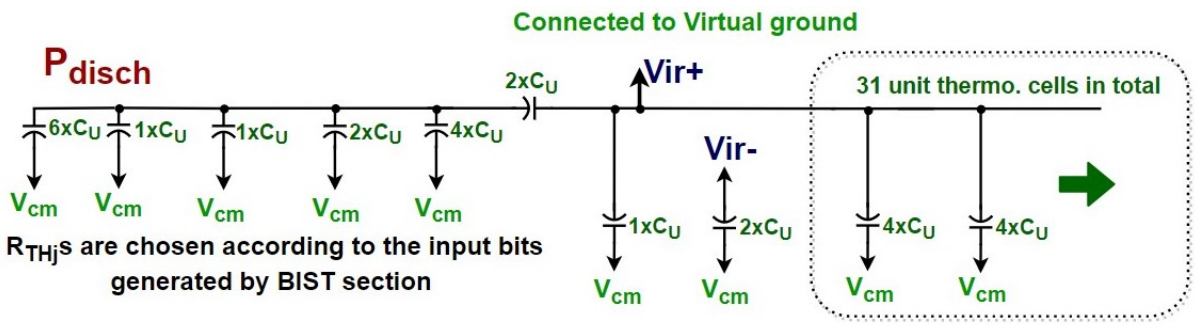


Figure 4-6 Discharging phase, *P_{disch}*, of the CDAC (single-ended version) [16].

Where Q_{SIC} is the charge delivered to the output to do SIC, V_{ref} is equal to $RefH - V_{cm} = V_{cm} - RefL$, $d_i = 2 \times b_i - 1$. Q_{SIC} can have negative and positive value, so this kind of capacitive-array works in the *bipolar mode*.

Although this method leads to a smaller gain, it boosts the linearity by removing the mismatch associated with the use of a fractional valued split-capacitor. In fact, the gain error is automatically compensated for at the system level by the (adaptive loop) that scales amplitude and phase of the output charge of the array in the digital domain. On the other hand, compensating the distortion terms would require an additional non-linear adaptation algorithm requiring much more power and area.

4.3.5.2 Choosing the Unit Capacitance

The equivalent capacitance seen from the virtual ground side towards the LSB side in Figure 4-3 is equal to C_U. The split-capacitor technique lowers the effective unit capacitor, and it is possible to explain it with an equivalent binary-weighted array with the same number of bits but a unit capacitance of $\frac{C_U}{8}$. As mentioned in sub-section 2.1.3, we need a capacitance of 1pF to provide the necessary current to remove the SI. The total capacitance seen from virtual ground node toward V_{cm} is equal to $132 \times C_U$. Hence, according to Eq. (4-11), the unit capacitance is 7.8fF. This is high enough to be slightly affected by the parasitic capacitance caused by the routing.

$$C_U = \frac{C_T}{\sum C_i} = \frac{C_T}{128} \quad \text{Eq. (4-11)}$$

4.3.5.3 Switches

The switch plays a key role in the SC circuits and can contribute to distortion of the whole design. The switches are employed in the SC schematic shown in Figure 4-4 (a) and they are made of transmission-gate configuration. Their size also highly determines design and performance. From section 3-4, we see that the first part of the settling-time is highly affects by the switches' resistance. As a rule of the thumb, if $3\tau_{CDAC} \approx 120ps$ in the first region of the discharge phase it will lead to $R_{Ton} \approx 40\Omega$

`

achieved from system-level simulation, where R_{Ton} is the total on resistance seen from virtual-ground of the TIA toward the CDAC in Figure 4-3. Enlarging the switches' size leads to faster switches but it causes more parasitic effects. On the contrary, lowering the size makes switcher relatively slower but with less charge and current leakage. Their sizes were chosen, by analysis and simulation, to decrease the distortion to an acceptable level.

Here, the process of developing the transistor-level design of the switches and choosing the RefL , RefH, and voltage supply starts. There are two kinds of transistors available in the used PDK, namely normal low-voltage (LV) and high-voltage (HV) transistors. Although the HV transistors can use a higher supply voltage (1.8V), and higher dynamic range, their parasitic is larger than the one of LV (1V) due to their minimum gate length of 150-nm. So, the DAC's distortion leads us to use LV (minimum gate length of 30-nm) and the maximum voltage supply is limited to 1V, then RefH is equal to 1V. To have maximum cancellation, V_{cm} is chosen 0.65V i.e., equals the common mode of the Analog part. RefL is made equal to 0.3V to have symmetric around V_{cm}. Accordingly, V_{ref} is equal to 0.35V, Δ.

4.3.6 Matching

The linearity determines how much the output spectrum of the DAC is far from ideal, and it degrades for larger mismatches and parasitic. Since the SIC must be used as a part of a RX chain, its linearity contributes to the linearity of the whole design as well. There are two different linearity figure-of-merit as follows: Static, such as DNL and INL, and Dynamic such as SFDR and SNDR. The SFDR is defined in chapter 2 and INL and DNL will be defined below.

INL (Integral non-linearity): It is a static metric to measure the deviation between the ideal value and the actual measured value for a certain input digital code after

`

correcting the gain and offset errors. The INL formula is defined below, and the DAC will be monotonic if its $INL < \pm 0.5$ [18].

$$INL(D) = \frac{y_R(D) - y_I(D)}{1LSB_n} \quad \text{Eq. (4-12)}$$

Where $y_R(D)$ and $y_I(D)$ are referred to the real and ideal values of the output for a certain digital code expressed by "D". $1LSB_n$ is defined for n-bit DAC as $\frac{Full-scale}{2^n}$.

DNL (Differential non-linearity): It is a static term explaining the deviation between two consecutive output Analog value of the DAC. DNL is given by the formula (4-13) below [18].

$$DNL(D) = \frac{y_R(D+1) - y_R(D)}{1LSB_n} - 1 \quad \text{Eq. (4-13)}$$

Where $y_R(D+1)$ and $y_R(D)$ represent the values of the output DAC at two digital consecutive code. The DAC will be monotonic if its $DNL < \pm 1$.

One of the major sources of error is the capacitance's mismatch, and it deteriorates the DAC linearity. By choosing the right unit capacitance, the linearity can be improved. The unit capacitance of the DAC is modelled as a CU (average value) along with a standard deviation σ_U. It is critical to find the minimum required matching accuracy, or σ_U, of the CU so that the specified INL and DNL can be obtained with an acceptable yield [41]. The maximum standard deviation of the DNL of the DAC $(\sigma_{DNL,max})$ determines the matching requirements and the required unit capacitance. By using formula (4-14) and the split-capacitor DAC equations Eq. (4-15) is obtained to guarantee high yield DAC [36], [40]-[41].

$$3\sigma_{DNL,max} \leq 0.5LSB_n \quad \text{Eq. (4-14)}$$

$$\frac{\sigma C}{C} < \frac{1}{6 \times 2^L \times \sqrt{(2^M - 1)}} \quad \text{Eq. (4-15)}$$

`

Where L and M are the number of bits in the LSB-side and MSB-side of the capacitive array. According to the specification of our design, $\frac{\sigma C}{C} < 0.27\%$ (In a fully-differential design, these results have to be divided by a factor of $\sqrt{2}$). The capacitance is chosen to be 7.8fF in the sub-section 2.6.3.1. The result of the Monte-Carlo simulation (Local variation) of the CU is shown in Figure 4-7 (1000-run). The result of the simulation indicates $\frac{\sigma C}{C} < 0.24\%$ satisfying Eq. (4-15).

4.3.7 Delay between the SI's and SIC's signals

Let us examine the condition when there is phase delay between the regenerated cancellation signal by the SIC block and SI. A limited amount of cancellation occurs in the normal condition as shown in Figure 4-8 (a) so that part of the SIC remains uncancelled. The next condition is when the two signals perfectly cancel each other which happens in an ideal canceller and shown in Figure 4-8 (b). Next, it is assumed that the two signals have the same amplitude but a small difference in phase as shown in Figure 4-8 (c), which can happen in the real words due to parasitic or PVT. Eq. (4-16) to (4-18) give the cancellation error due to the delay.

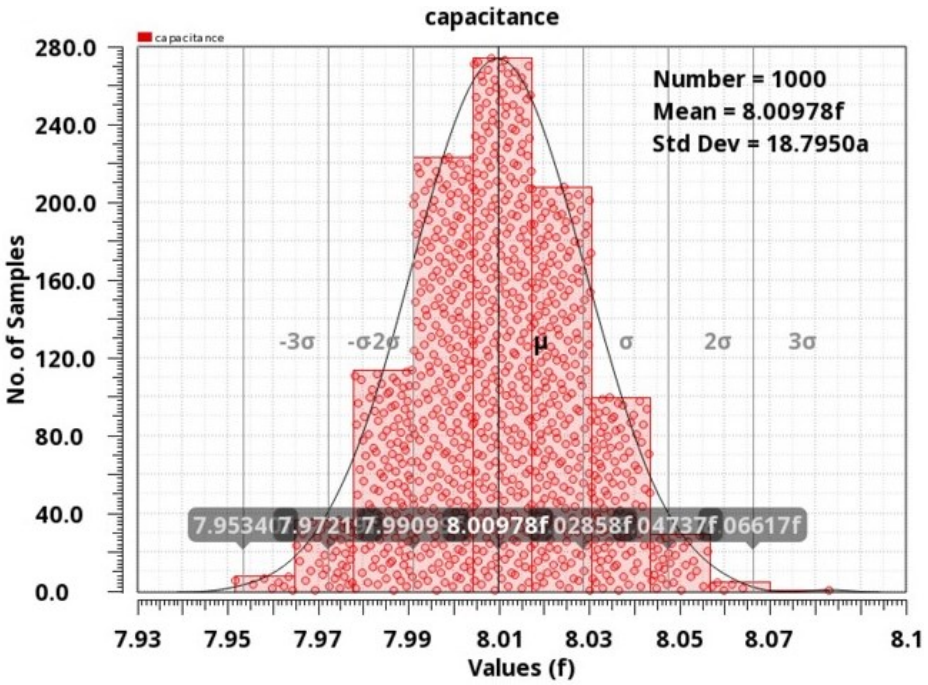


Figure 4-7 1000-run Monte-Carlo to show variation of the unit capacitance.

$$Diff.current = I_{SI} - I_{Cancel.} = I_0 - I_0 \times e^{-i\theta} = I_0 \times \left(1 - e^{-i\theta}\right) \quad \text{Eq. (4-16)}$$

$$Diff.current \approx I_0 \times i\theta \quad \text{Eq. (4-17)}$$

$$Cancellation\ error = 20 \times \log_{10}\left|\frac{I_{SI}}{Diff.current}\right| = -20 \times \log_{10}\theta = -20 \times \log_{10}\left|\frac{D}{180} \times \pi\right|$$

Eq. (4-18)

Where I_{SI} , $I_{Cancel.}$, I_0 , θ are the SI component, cancellation current, the amplitude of the SI current and their phase shift, respectively. D is the magnitude of the phase difference in degree. For instance, if a cancellation error equal -70dB is required, according to Eq. (4-18), the delay between two signals should be less than 0.018° which *shows the sensitivity of the cancellation to the delay of the SI and cancellation signal*.

4.4 Time-Interleaved (TI)

Time-interleaving technique is an architecture proposed for high-frequency operation which can make a high-speed DAC combining some slower blocks, called sub-DACs, at the cost of an increase in area and complexity. In other words, it can be a good candidate to help relax settling-time of the TIA in our application. When one of a sub-DAC is creating the Analog output, the others are preparing the data for the next

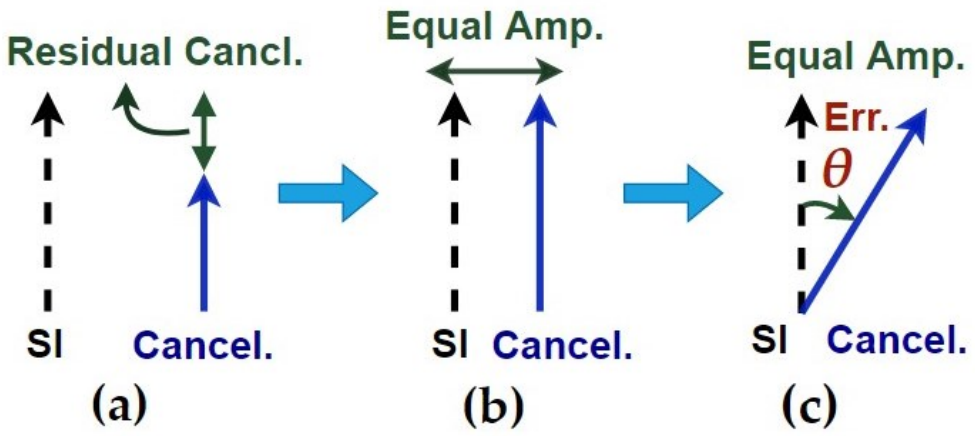


Figure 4-8 Analysing the timing mismatch in the SIC mode (a) SIC with the limited cancellation(b) perfectly SIC (c) the SI and SIC have the same amplitude but with the delay.

cycles. For example, 2-way TI is illustrated in Figure 4-9 (a). There are two clocks with 180° phase shift and the same frequency of $f_{clk} = \frac{1}{T_{clk}}$. While DAC1 updates the Analog output at $\frac{T_{clk}}{2}$, shown in Figure 4-9 (b), (c), DAC2 is processing the data to create the Analog output for the next $\frac{T_{clk}}{2}$. Hence, the effective period between two consecutive samples is $\frac{T_{clk}}{2}$, means the updating rate of the Analog output rises to $f_0 = 2 \times f_{clk}$. Of course, the main sources of the error arise from the fact that the DACs are not identical [34], [42].

To perform 2-way time-interleaved, two different DACs (sub-DACs) are used in our design without utilizing any extra calibration technique, DAC-1 and DAC-2. Each sub-DAC includes two capacitive-array (called CA_A and CA_B).

4.4.1 Mismatch between Sub-DACs

M-identical interleaved DACs (sub-DACs) working at $\frac{F_S}{M}$, under ideal conditions, produces identical output at Fs. Unfortunately, each sub- DAC have slightly different offset, gain, and delay because of device mismatch. Due to these non-idealities, alias images in the output of each sub-DAC do not exactly cancel and thus, leave behind some residual images. Depending on the source of non-ideality, these residual alias images generate spurs in the output spectrum [43]. The negative effect of the timing mismatch can be lowered in the CDAC if the whole charge is discharged in less than

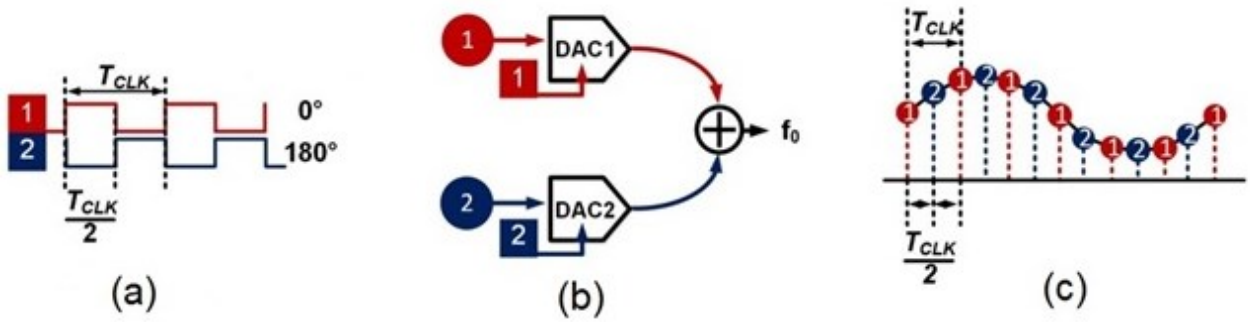


Figure 4-9 Conceptual diagram of 2-way Time-interleaved DAC (a) two out-of-phase clocks (b) two-way TI DACs (c) creating the Analog output at f0=2/Tclk [42].

half-of the period of the FS. The gain mismatch is sensitive and can appear in the output spectrum and causes non-linearity.

Offset Mismatch It is due to the variation in the DC offset between various channels. It produces a tone at DC and at half of the sampling frequency $\left(\frac{F_S}{2}\right)$ in the output spectrum of the overall DAC. The magnitude of this tone does not change with frequency, and it is independent of the input digital code. It can easily be removed by different technique such as digital filter.

Gain Mismatch If all the other characteristics are perfectly identical and ideal gain error is defined as the maximum difference between the gain of any two sub-DACs. The primary sources of gain error are the difference in reference voltages or the differences in the charging/discharging circuits, such as charge injection or clock feedthrough, between various capacitive-arrays [43]. Gain mismatch is like amplitude modulation. The input amplitude is modulated based on which DAC is active, therefore the difference in magnitude of input signal can be thought of as the carrier signal, and it's being modulated by a square wave with a frequency of $\frac{F_S}{2}$. Then the modulated signal has a tone at frequency Fmod - Fcarrier = $\frac{F_S}{2} - F_{IN}$ [44]. Unlike, the offset mismatch correction, the correction of gain mismatch is slightly involved.

Timing (phase) Mismatch the last kind of mismatch is called timing mismatch. It occurs due to jitter and time-skew in the clock. For high input signal frequencies even a small timing mismatch can cause significant error. Timing mismatch is like phase modulation, where the timing error is modulated by a square wave with a frequency of $\frac{F_S}{2}$. This results in a tone at frequency $\frac{F_S}{2} - F_{IN}$, the same as gain mismatch [44]. In practical implementation, the phase or timing errors are unavoidable due to the finite propagation of the clock signal, and variations in the clock buffers and sampling switches. The input signal effectively is phase modulated by a periodic timing error signal which has a frequency of $\frac{F_S}{M}$ [43].

`

This additional information might be exploited to separate gain error and timing error from each other. For DC input signals, timing error is zero and spurs in the output spectrum are only due to gain error. Once the gain error is calibrated or removed then, for high input frequencies, the spurs left in the output spectrum are due to timing mismatch [44].

4.4.2 Analysis of the Transfer-function with non-ideality

The output spectrum of N-way TI DAC without any non-ideality is expressed by Eq. (4-19) [34]. It is referred to *SINC* function as explained in the section (4-1).

$$Y_{Out}(f) = P_{SH}(f) \times \left[\frac{1}{T_S}\sum_{n=-\infty}^{n=+\infty} X(f - nf_s)\left(1 + e^{-j\frac{\pi}{N}} + e^{-j\frac{2\pi}{N}} + e^{-j\frac{3\pi}{N}} + \cdots\ e^{-j\frac{(N-1)\pi}{N}}\right)\right]$$

Eq. (4-19)

If there is any mismatch between two DACs this can cause non-ideality and generates spurs in the spectrum of the TI DAC [34],[42]. The output waveform of N-way TI DAC is expressed below.

$$y_{Out}(t) = x_1(t) + x_2(t) + x_3(t) \ldots + x_N(t) \qquad \text{Eq. (4-20)}$$

Where $x_i(t)$ is output signal of i^{th} sub-DAC, i varies between *0* to *N-1*, and $y_{Out}(t)$ is the output of the TI DAC. If each sub-DAC degrade from the first sub-DAC, $X_1(f)$, we can model the non-ideality with a transfer-function represented by $H_i(f)$ [34].

$$X_i(f) = P_{SH}(f) \times \left[\frac{1}{T_S}\sum_{n=-\infty}^{n=+\infty} X(f - nf_s) \times H_i(f)\right] \quad \text{Eq. (4-21)}$$

$$Y_{Out}(f) = P_{SH}(f) \times \left[\frac{1}{T_S}\sum_{n=-\infty}^{n=+\infty} X(f - nf_s)\,(1 + H_2(f) + \cdots + H_N(f))\right] \quad \text{Eq. (4-22)}$$

By using Eq. (4-4), $X_i(f)$ is calculated for the i^{th} sub-DACs. Hence, Eq. (4-22) shows how the output spectrum changes if there is deviation from the ideal characteristics. The mismatches of the *N*-way TI DAC degrade the DAC's ENOB and add spur to the

`

output response. Accordingly, it needs calibration technique or post-processing to remove the errors [43]-[47]. *But the calibration technique is not used in our design.*

4.5 Noise of the Capacitive-array

The performance of the SC circuit is limited by noise. This can come from different sources including off-chip, substrate noise, noise of the logic circuits, and power supply. As it is explained in section 3.4.3, Thermal and Flicker noise are two major sources of noise in the MOS transistors. If the transistor operates in the triode zone as a switch, its noise can be modelled by a voltage source in series with the device equivalent resistance [48]. Hence, the SC circuits works as a sample-and-hold with a resistor and capacitor, and it is explained with more details below.

4.5.1 Noise Analysis

Thermal noise of the switches, when it works in the triode region, causes serious problem in the discrete time system. The power spectral density (PSD) of a resistor is white and is expressed by

$$S_{nR} = 4KTR \left(\frac{V^2}{Hz}\right) \quad \text{Eq. (4-23)}$$

Where SnR is PSD of the noise in $\frac{V^2}{HZ}$, K is a Boltzmann constant, T is the absolute temperature, R is the resistance value. The mean square (MS) value of the noise voltage and charge stored in a capacitor is given by Eq. (4-24) and (4-25), respectively.

$$\overline{v^2{}_{nSC}} = \frac{KT}{C} \left(V^2\right) \quad \text{Eq. (4-24)}$$

$$\overline{q^2{}_{nSC}} = KT \times C \quad \text{Eq. (4-25)}$$

Where $\overline{v_{nSC}}$ and $\overline{q_{nSC}}$, C are the noise value of the voltage, charge and capacitance value of the sampled capacitor in the series RC, respectively. For example, when the

`

capacitance value is equal to 1 pF the equivalent voltage stored in the capacitor is 64.3μV. Finally, useful formulas below before staring the next sections.

$$S_{nOut} = |H_T(j\omega)|^2 \times S_{nIN} \quad \left(\frac{V^2}{HZ}\right) \quad \text{Eq. (4-26)}$$

$$\overline{v^2}_{nO} = \int_0^{\infty} S_{nOut}\, df \quad (V^2) \quad \text{Eq. (4-27)}$$

$$\overline{v^2}_{nSC} = \frac{1}{OSR}\frac{KT}{C} \quad (V^2) \quad \text{Eq. (4-28)}$$

$$\overline{v^2}_{nOut} = \overline{v^2}_{nIN1} + \overline{v^2}_{nIN2} + \overline{v^2}_{nIN3} \ldots \quad (V^2) \quad \text{Eq. (4-29)}$$

- Eq. (4-26): The PSD of the output noise of a linear system is calculated by the multiplying the input PSD by the amplitude of transfer function of the block. Where SnOut and SnIN are PSD at the output and at the input, respectively.
- Eq. (4-27): By integrating Eq. (4-26) over the frequency range, the output noise voltage is acquired. Where SnOut and $|H_T|(j\omega)$ are the PSD of the output noise and the magnitude of the transfer function of the linear system between the input and output in the frequency domain, respectively [48].
- Eq. (4-28): The MS value of the noise voltage of a SC circuit with over-sampling is calculated by this formula while OSR is defined by equation (2-14).
- Eq. (4-29): The total MS value of the noise voltage of several uncorrelated noise sources is calculated by summation the MS of noise voltage of all of them [48].

4.5.2 Noise Analysis of the developed CDAC

The designed CDAC works in two different phases, namely charge and discharge. MS value of the output noise is calculated by adding the produced noise in the charge and discharge phases.

$$\overline{v^2}_{nOut} = \overline{v^2}_{nPchr} + \overline{v^2}_{nPdısch} \quad (V^2) \quad \text{Eq. (4-30)}$$

`

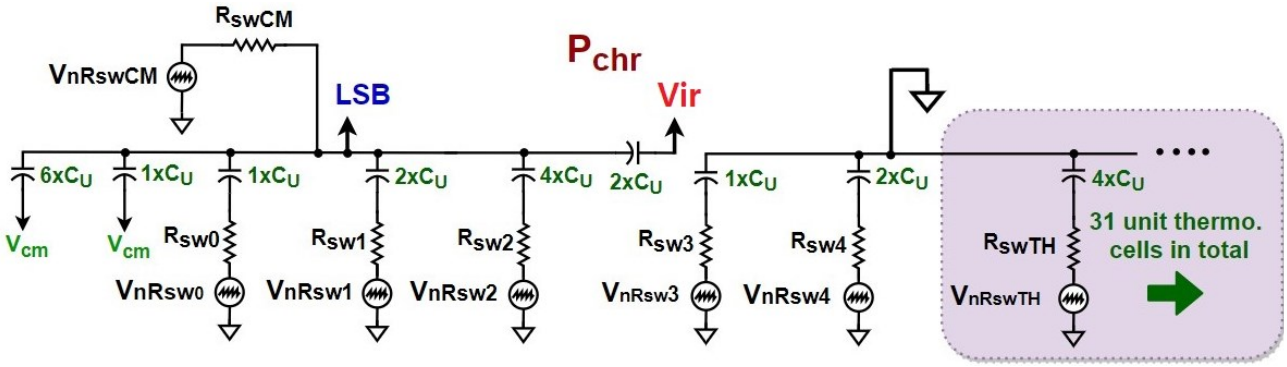


Figure 4-10 Equivalent single-ended noise model of the CDAC in the charging phase, P_{chr}.

Noise in the charging phase, $\overline{v^2}_{nPchr}$: In the charging phase, P_{chr}, the equivalent single-ended noise model of the CDAC is shown in Figure 4-10. R_{SWi} and V_{nRSWi} (i varies from 0 to 4) and R_{SWTH} and V_{nRSWTH} (31 thermometric cells) are switches resistance and equivalent noise voltage source of the binary-weighted and thermometric part, respectively. The MS value of the noise charge of the node LSB at the end of the charging phase is $\overline{q^2}_{nLSB}$ [49]-[51].

According to formula (4-26), first, it is important to find the transfer-function of each noise voltage source to node LSB, shown in the figure above. Then the different MS value of the noise voltage are calculated according to Eq. (4-27). Finally, by using Eq. (4-29), the total MS value of the noise voltage is obtained by summing them up. Because there is just three bits in the LSB-side, and the transfer-functions are complicated, an assumption is made and only the contribution of the noise voltage in MSB part is considered in the charging phase. The MS value of the noise voltage is approximately expressed by (Where C_T is total capacitive of the array)

$$\overline{v^2}_{nP_{chr}} \cong \frac{KT}{C_T} \quad \text{Eq. (4-31)}$$

Noise of discharging phase, $\overline{v^2}_{nPdisch:}$ The stored voltage at the end of the P_{chr} and the MS value of the stored thermal noise of switches in the P_{disch} phase contributes to the

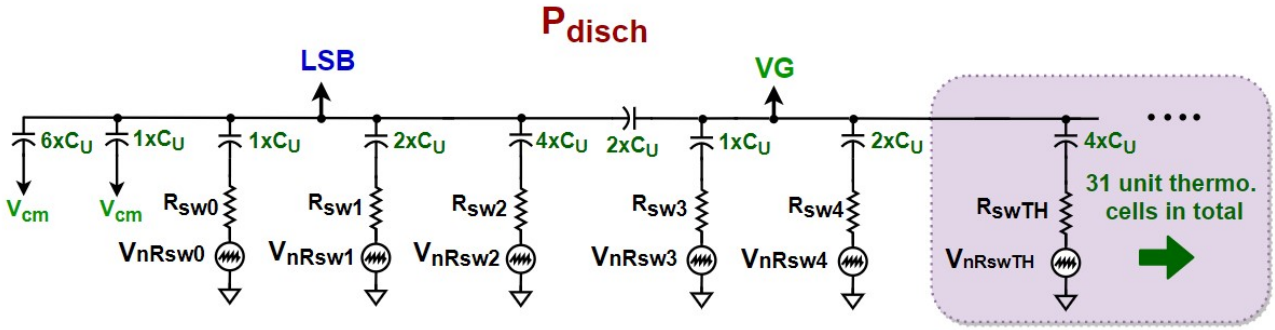


Figure 4-11 Equivalent single-ended noise model of the CDAC in the discharging phase, *Pdisch*.

noise of this phase, as shown in Figure 4-11. The capacitance and switches of a thermometric cell is supposed as base and all other switches are scaled down according to the scale factor of the capacitance. Like the previous phase, the noise contribution of the LSB-part is neglected. Hence, the MS value of total noise charge generated by the capacitive array is $\overline{q^2}_{nOut} = 2 \times KT \times C_T$ [51]. If the OSR and the fully-differential topology are considered the MS value of the noise voltage is expressed as.

$$\overline{v^2}_{nOut} = 2 \times \frac{2 \times KT \times C_T}{OSR} \quad \text{Eq. (4-32)}$$

The equivalent noise voltage, according to Eq. (4-32), is almost 50uV, which is much lower than TIA's one, 125uV. Hence, the dominant source of the noise is the TIA.

4.6 Digital Circuit

A DAC needs the digital bit stream to create a waveform. Since our design should work as a stand-alone DAC or SIC block, it required various sets of data with different BB amplitude and frequency. It also needs a unit to control the chip status like working mode or phase. Nowadays, the high-speed and high-performance digital circuit is easy to implement in advanced CMOS process to assist Analog designers. In this chapter, the digital interface is presented. It includes two parts, one developed by behavioural description software and another one developed manually (designed at the transistor-level by cadence).

`

4.6.1 *Using Hardware Description Language*

Nowadays, using hardware description language (HDL) such as Verilog or VHDL is widely recommended because they reduce design time and help test circuit precisely. By writing a description of a system, the required circuit and layout will automatically be generated by the software. It is even possible to test and verify the performance of the design after implementation. The main digital block, called *HDL part* and developed by Verilog language, works as follows.

- *Serial Interface*: Before working as a CDAC or SIC, it is necessary to load the data and control word into the chip. For saving the number of the pins, the control word and data is serially loaded into the chip at relatively low-speed (< 100MHz).
- *HDL Principle*: By using the digital interpolation technique, the serial data with slow speed is converted into high-speed digital 10-bit digital word. The resolution of the interpolator is more than 10-bits to keep the precision of our design. The *HDL part* is employed to test the design, so it is called built-in-self-test (BIST).
- *Working Mode Selection*: The serial data defines the control words of the capacitive-array and its modes. The explanation of the various working modes is mentioned in Table 5-1 in the next chapter.
- *CDAC Digital Data*: The CDAC needs 10-bit parallel digital bits, changing with 1GHz frequency, to generate continuous waveform (CW). The BB frequency can be set from 1MHz to 50MHz with the step of 12.207 KHz.

4.6.2 *CDAC Local Controller*

High-speed part of the logic circuitry is manually developed to control the function of the design including decoders. The logic block works with a supply voltage equals 1V, to minimize the parasitic and power consumption in the high-speed. This part is a *manually designed logic*, and the different section of it is explained below.

`

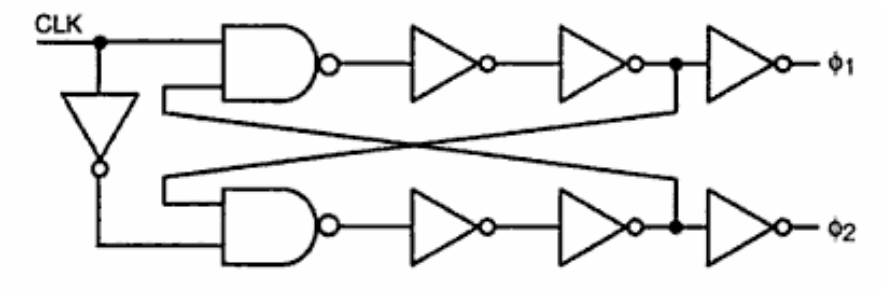


Figure 4-12 Non-overlap clock generator [52].

- *Clock with Programmable Delay*: Since the HDL's clock is provided with *manually designed logic*, the generated data, in the *HDL part*, will return to the DAC with delay (~120ps). Hence, there is not enough time for the CDAC to either charge or discharge. Using the latch is not helpful due to large delay between the clock and data. A programmable delay block is developed to create a delay from 0ps to +150ps with 3-bit resolution. The clocks that go to the capacitive-array has a certain delay compared to the clock that enters the *HDL part*.
- *Clock Generator:* Our design needs two non-overlapping and reliable clocks. They are generated from a high-speed off-chip clock, as shown in Figure 4-12. The non-overlapping between clocks should be high enough that the design could properly work in the different process of corners. However, in order not to waste the effective duty cycle, the delay should not be too high.
- *Clock Distribution*: Two non-overlap clocks are buffered and distributed across the chip. The delay of the clock should be in the acceptable range not to cause spurs in the output spectrum of the CDAC. A technique method, shown in Figure 4-13, is used in our design for distribution of the clock and the local driver to lower the negative effects of the wiring and input capacitance of each cell. Each rectangular and triangle represent one CDAC's cell and a driver in the figure below, respectively [52]. The inverters at the input nodes and inside the

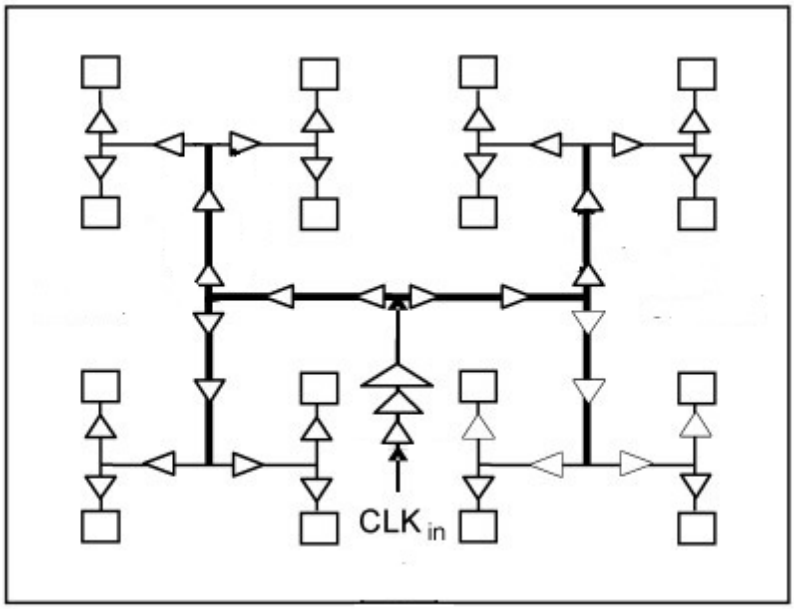


Figure 4-13 Clock distribution inside the chip [52].

current cell are used for buffering and generating the complementary signals (the thicker line shows higher current sides).

- *Matrix Decoders*: The data coming from the *HDL part* requires to enable/ disable certain cells. Hence, it is critical to have a suitable decoder to select specific cells corresponding to each code. The required decoder should be designed with high-speed and consume low power and be simple (for lowering delay and complexity). Hence, the decoder is realized by utilizing the minimum number of logic stages. The CDAC's cells are divided into three categories according to the input digital data. 1) The rows in which all the capacitive cells are turned on. 2) The rows in which all the capacitive cells are deactivated; and 3) a certain row in which some of the capacitive cells are turned on depending upon the

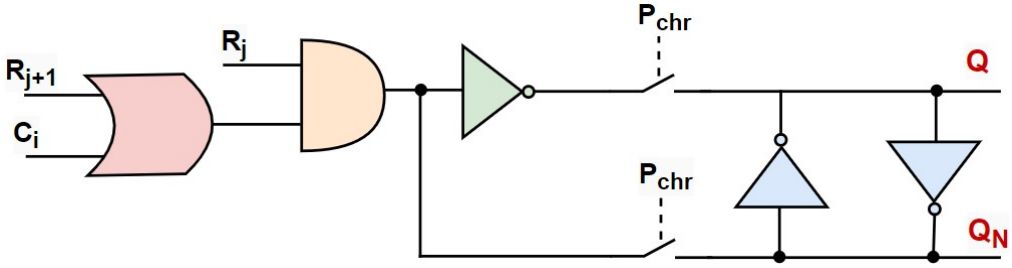


Figure 4-14 Thermometric cells (Matrix) decoder including the high-speed Latch [53].

column decoder signal [53]. Figure 4-14 shows the actual decoder circuit implemented by using *OR–AND* gates inside of each CDAC's cell as a local decoder to decrease the delay. *Rj* , *Rj+1* , and C*i* represent the signals come from the *HDL part* and represent rows of j^{th} and $(j+1)^{th}$ and column of i^{th}, respectively. First, the date is loaded in the latch and held in the charging phase. Then, the data is used in the discharge phase to suppress the glitch and to enhance the decoder speed [53].

5 The CDAC and SIC simulation and Layout

The sub-blocks of the SIC were presented in the previous chapters. So, it is important to connect them to explore the design performance for different working mode, namely stand-alone CDAC and SIC. *The chip includes two parts, namely, manually design block and HDL part*. The simulation results are also presented to give an insight about the developed block before and after drawing the layout. To improve the performance of the design, some layout techniques and floor-planning are also explained. The design will be ready for the fabrication.

5.1 Manually Designed Block

The more complete block diagram of Figure 2-13 is shown in Figure 5-1 . It illustrates in more details the design and each block. The orange colour blocks are developed in

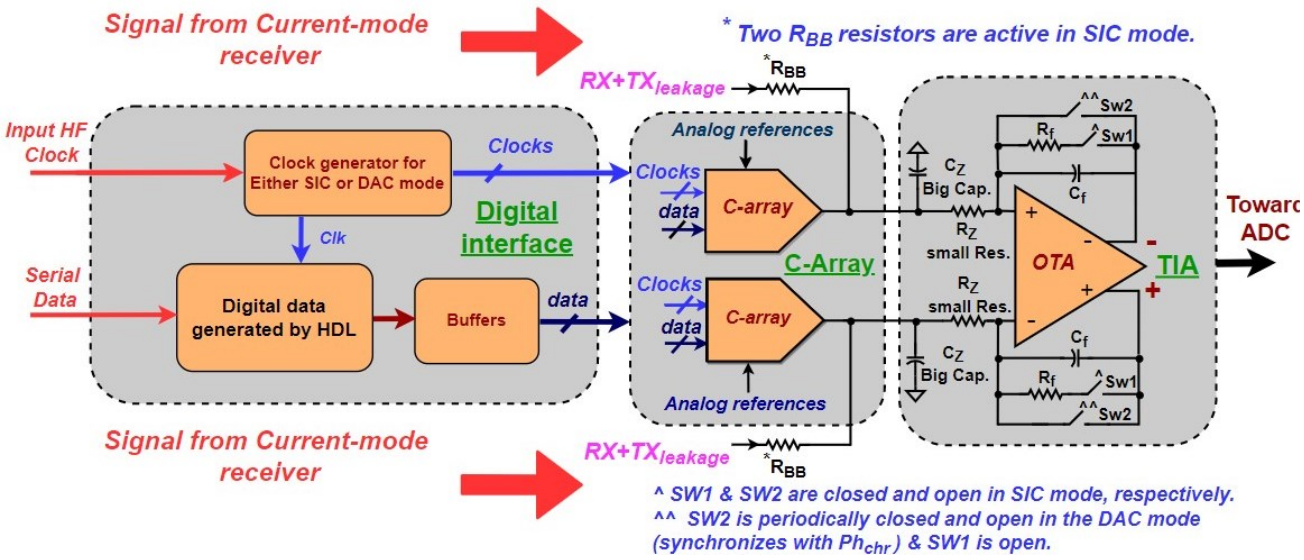


Figure 5-1 Block diagram of the *manually designed block* including In & Out.

Table 5-1 Summary of the chip's working modes.

Mode	Application	Sub-blocks	Description
1	Characterizing the TIA	TIA	Both C-arrays are off, for measuring the TIA's param.
2	Characterizing CDAC-A or CDAC-B	DAC-A or -B + TIA	Only one DAC works
3	Two-tone test of the CDAC	DAC-A and -B + TIA	Two DACs work with the same clock
4	SIC	DAC-A and -B + TIA	Two C-arrays work in the time-interleaved mode

this dissertation, and these sub-blocks are explained below to help understand the performance and test procedure of the design.

- The working mode of the chip are summarized in Table 5-1. *There are two different DACs in this design to perform 2-way TI, namely DAC-A and DAC-B, as shown in* Figure 5-2 . ***The time-interleaved is used in 4th mode, the SIC one, without using any calibration technique.***

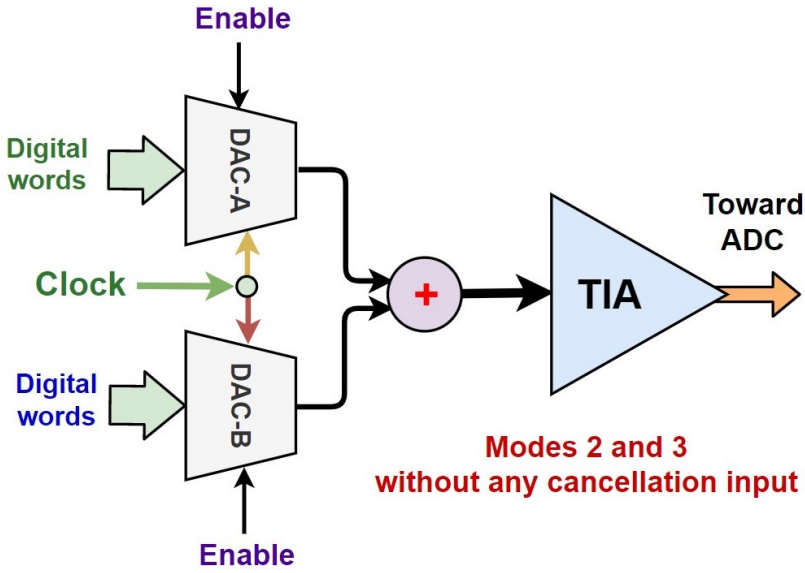


Figure 5-2 Working mode illustration.

- 1st: The capacitive array is disable in the 1st working mode to characterize the TIA.
- 2nd: In the 2nd mode, either *DAC-A* or *DAC-B* works to characterize them.
- 3rd: The block can be utilized as a part of the Analog transmitter. Two DACs simultaneously working with the same clock can be used in the I and Q paths.
- 4th: To perform the SIC, *DAC-A* and *DAC-B* work in the time-interleaved mode.

5.1.1 Digital Interface (Pattern Generator)

The high-frequency clock at 1GHa, enters the chip, from the top left side of Figure 5-1. It is fed to the clock generator to create two non-overlapping clocks for the *manually designed logic* and *HDL part* explained earlier in section 4.6. The serial input with frequency below 100MHz loads the data, from the bottom left side of Figure 5-1. The necessary set-up word is loaded to each sub-block of the chip to choose the working mode given in Table 5-1. The 10-bit Sinus digital word with variable frequency and amplitude are sent to the C-array in the middle of the figure. The frequency can be adjusted from 1MHz to 50MHz with a step of 12.207 KHz. *The HDL part unit is also called pattern generator*.

5.1.2 Capacitive-array

The sequence of the data is converted into the Analog signal that corresponds to the input words. It is in the middle of Figure 5-1.The output of this stage is connected to the output of the mixer and the input of the TIA to perform cancellation in the 4th mode.

5.1.3 TIA

This is the only truly Analog part of the design used for filtering and amplification of the signals. There are some switches in the feedback network around the TIA, on the right-side of Figure 5-1, to set the working mode. The switches are set up as follows.

In the 2nd and 3rd mode, DAC mode, SW_1 is always open but SW_2 is periodically turned on and off synchronously with charging phase clock, P_{chr}. On the other hand, if the

`

chip is used as a SIC block SW1 and SW2 are permanently closed and open, respectively, since the feedback resistor, RF, plays a key role in the SIC.

5.1.4 *Simulation Assumptions*

Here, some simulation assumptions and design parameters are mentioned since the simulations of the whole block are presented below.

- *The "HDL part" creates the digital bit steam which is sent to the "manually designed block" section to process the digital BB data and do cancellation or generate the Analog signal.*
- *High-frequency Clock*: Since the design includes the clock, the periodic steady-state analysis (PSS) could be used. It computes the periodic steady-state response and operating points of the circuit at a specified fundamental frequency. The simulation setting is explained in Ref. [54]. Although most of our simulations are done in the PSS environment, the noise analysis can be done in time domain.
- *FFT*: To obtain the dynamic parameters of a DAC, the Fast-Fourier-Transform (FFT) of the output signal is a very informative tool. When somebody want to employ the FFT, the critical point is to perform coherent or window sampling methods to get an accurate simulation result [55]. To this end, the design parameters and input frequencies should satisfy a special formula as expressed in Eq. (5-1) [56]. Where f_{BB} is the input BB test frequency, f_s is the clock frequency of the DAC, N_{Sample} is the number of the samples of the waveform, and N_{FFT} is the number of FFT points which is always a power of two such as 512 or 1024. The last point is that N_{Sample} should be either prime compared to N_{FFT} or an odd number. The BB frequency is always chosen according to the formula below in the rest of the thesis.

$$f_{BB} = \frac{N_{Sample}}{N_{FFT}} \times f_s \quad (Hz) \quad \text{Eq. (5-1)}$$

- *Constant electrical parameters*: For the simulation the clock frequency, digital supply, Analog supply, Vcm, RefH, RefL are equal to 1GHz, 1V, 1.3V, 0.65V, 1V, 0.3V, respectively. The input signal of the CDAC is a digitized sinusoidal waveform, the frequency can vary between 1MHz to 50MHz, chosen according to Coherent sampling, Eq. (5-1).

5.2 Stand-Alone CDAC

In this section, the simulations result of the stand-alone CDAC are reported at the schematic level. Hence, it is necessary to have a test-bench for measuring the CDAC's parameter, as shown in Figure 5-3. No input is feed to the two the resistors, shown with RBB in the figure below. An ideal anti-aliasing 1st order LPF follows the output of the TIA to show the oversampling effect by filtering the quantitation noise in the Nyquist band. The Nyquist band of the simulation is automatically chosen by software to $\frac{F_S}{2}$. This test-bench is used in the current section.

For demonstrating the time domain response of the CDAC, the BB digital bit stream frequency and amplitude are set around 10MHz to avoid the output voltage

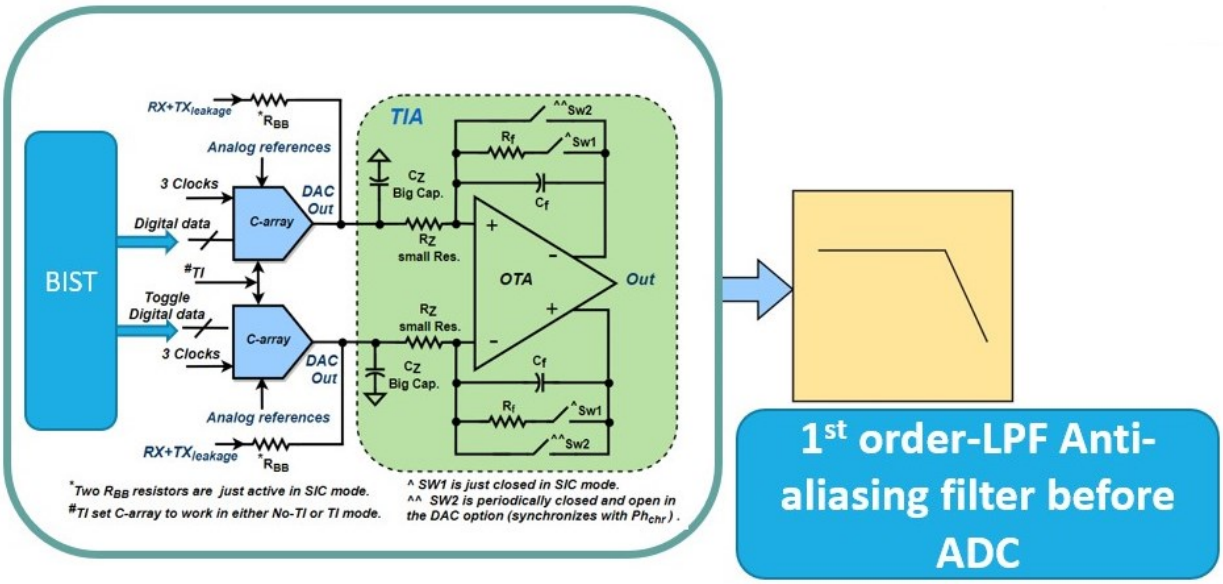


Figure 5-3 Test-bench for measuring the parameters of the CDAC in mode 2nd and 3rd.

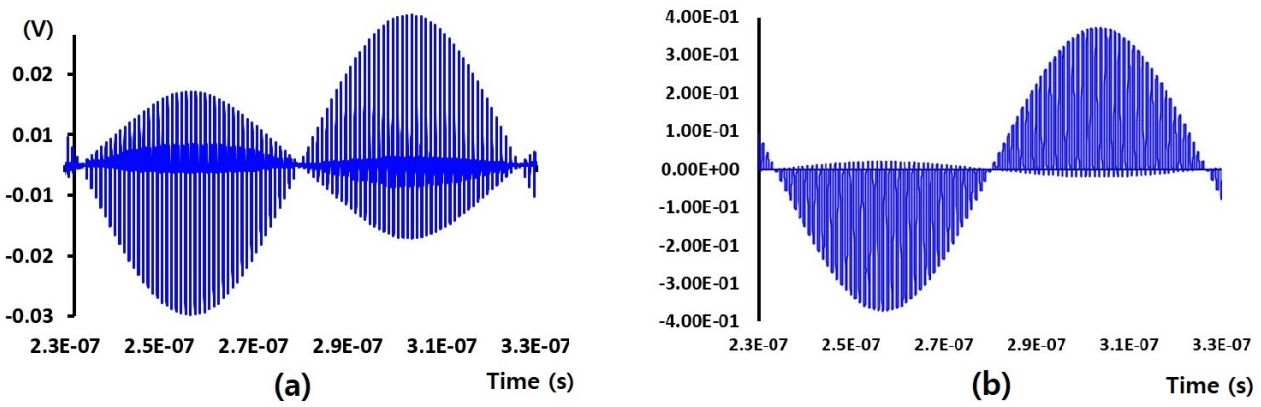


Figure 5-4 Time-domain response of the working mode 2 (2) differential voltage across the (a) OTA's virtual ground and (b) TIA's output

saturation. The time domain response of the differential voltage of the virtual ground and TIA's outputs are shown in Figure 5-4 (a) and (b), respectively. The input voltage of the OTA is kept below 30mV to have better linearity of the overall TIA, removing the slewing of the first stage. The output swing is bounded to the supply voltage.

5.2.1 CDAC Static Specification

The DNL is one of the important parameters of every type of DAC indicating the linearity of the design and it is a great figure-of-merit to compare the various designs. Although it is a static parameter, a lot can be inferred from it. After collecting information from the output of the TIA in the 2nd and 3rd working mode, the gain and offset error must first be corrected, then the DNL values are calculated by MATLAB

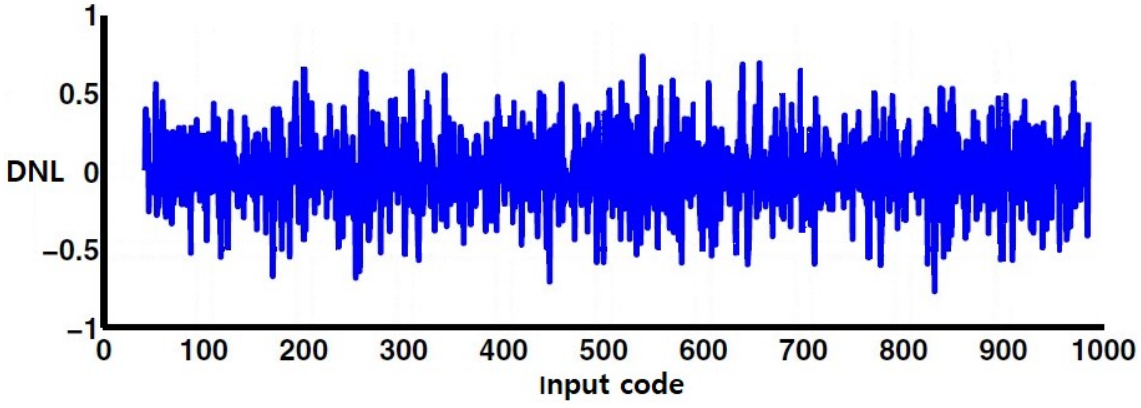


Figure 5-5 DNL of the 10-bit CDAC in the working mode 2nd.

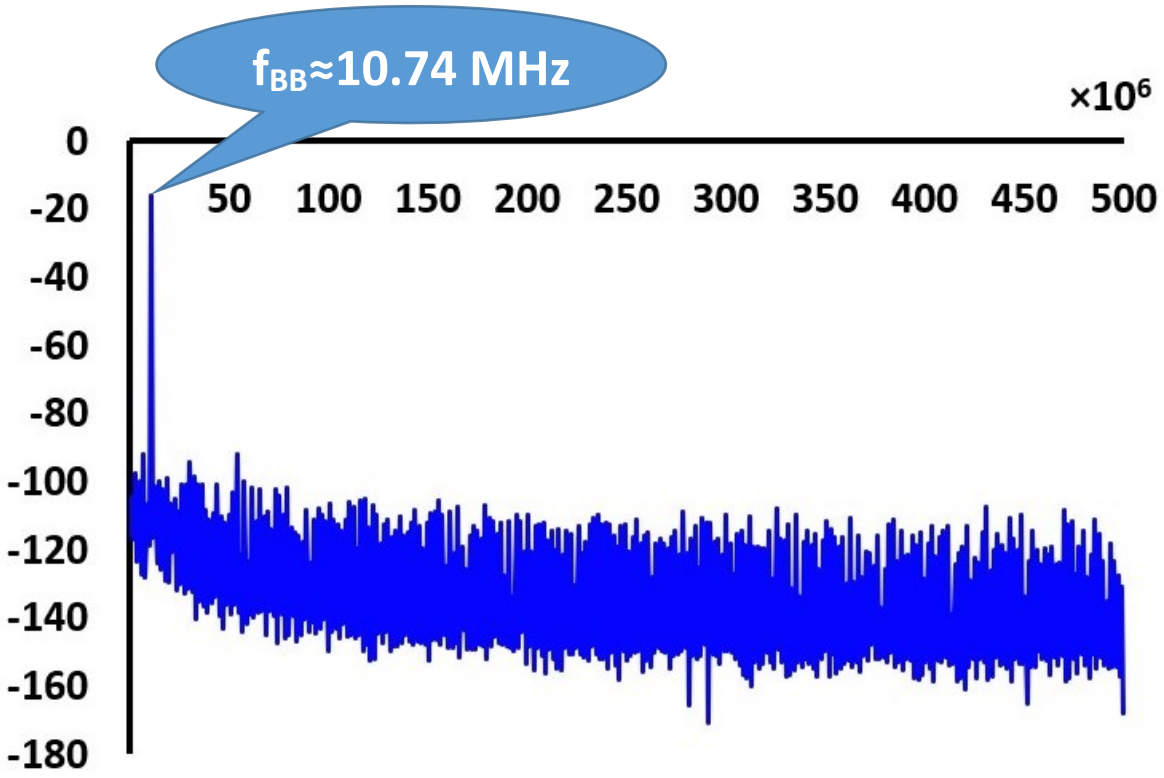


Figure 5-6 Output (before ideal LPF) spectrum of the CDAC in 2nd mode.

according to formula (4-13), as shown in Figure 5-5. From the figure, the observed $|DNL| \leq 0.7$ can guarantee that the CDAC works in a monotonic way.

5.2.2 *The CDAC Dynamic Specification*

The CDAC works in the working mode two, f_{BB} is chosen around 10.74MHz according to the coherent sampling theorem, ≈ 12× oversampling ratio, and input digital bit represents a Sinus waveform with amplitude equals 1 dB below full-scale. Hence, the TIA output spectrum is shown in Figure 5-6 and the dynamic specification before and after ideal LPF are reported in Table 5-2. After limiting the band width of

Table 5-2 Summary of the CDAC dynamic specification in working Mode 2nd. The outputs are reported after the TA and ideal LPF.

	ENOB (bit)	SINAD (dB)	SFDR (dBc)	THD (dB)	Signal power (dBV)
Output of the TIA	9.4	58.2	68.4	-69	-9
After ideal LPF	10.7	67	69	-70.5	-16

`

the output signal of the TIA, with the ideal LPF, the oversampling effect is visible in the numbers.

5.3 SIC (Mode 4)

Developing a SIC block is the main goal of this thesis. Here, the performance in the 4th working mode is reported at the schematic level. Two figures of merits are defined below in cancellation. Eq. (5-2) and (5-3) define the amount of SI cancellation and the power of the signal in the presence of non-linearity and noise after cancellation, respectively.

$$Cancel. = \left(Amplitiude\ of\ the\ fundamnetal_{\boldsymbol{Before\ Cancellation}}\right) - \left(Amplitiude\ of\ the\ fundamnetal_{\boldsymbol{After\ Cancellation}}\right) \quad (dB) \qquad \text{Eq. (5-2)}$$

$$SNDR_{\boldsymbol{equ.}} = Cancel. + SNDR_{\boldsymbol{After\ Cancelation}} \quad (dB) \qquad \text{Eq. (5-3)}$$

In Eq. (5-2), the amplitude of the fundamental BB frequency before and after SIC are in dB. For simulating the SIC, the used test-bench is shown in Figure 5-7. A differential

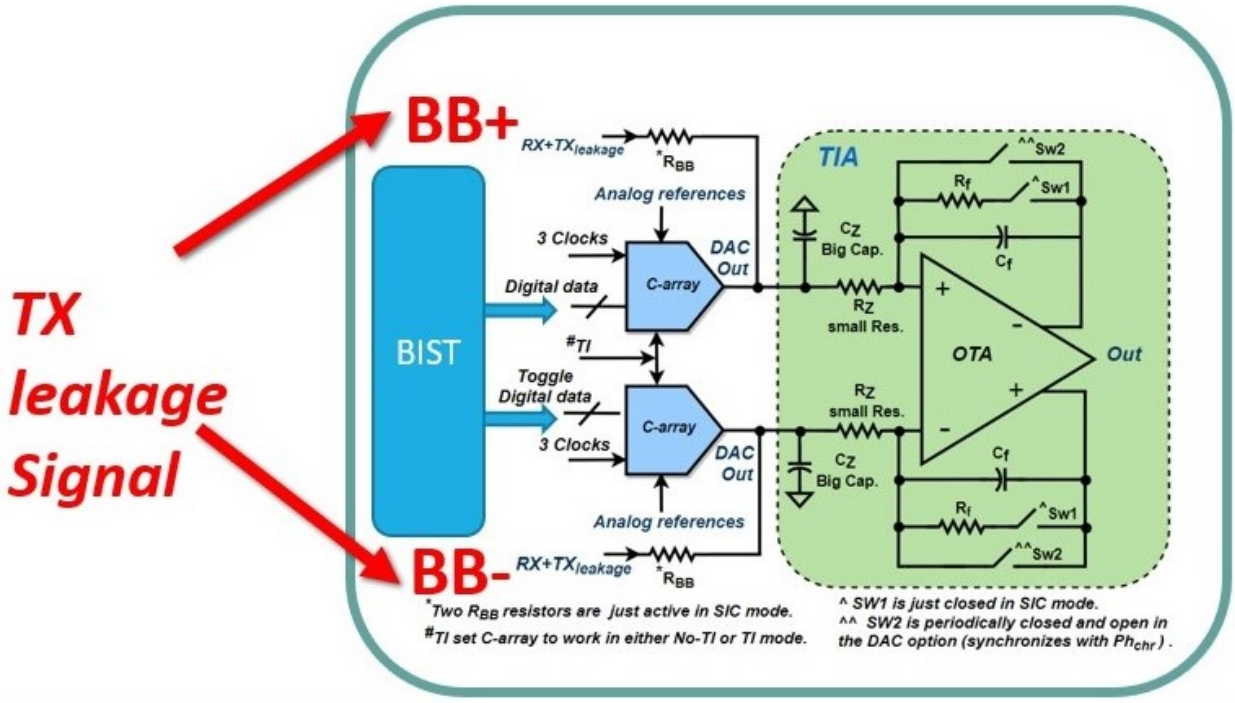


Figure 5-7 The SIC test-bench. The leakage signal is fed to the red arrows.

voltage source is connected between BB+/ BB- in the left-side of the figure below models the TX leakage. The voltage signal is fed to two R_{BB} resistors that models the output resistor of the LNA and converted into the SI current. The digital signal is generated by the BIST block, the blue part in the left-side of the figure, to remove the TX leakage signal.

5.3.1 Cancellation

Before simulating the cancellation, the input BB frequency is set to 10.7421875MHz according to the Coherent sampling. Since mode 4th works in 2-way TI, the cancellation is performed in the double cancellation way. The R_{BB} is first set to 2KΩ and the peak of the voltage amplitude between BB+ and BB- (shown with the red colour) is chosen to equal 2.6V. Then the amount of cancellation is set to -43dB by changing the digital code. The output voltage spectrum of the TIA, after cancellation, is shown in Figure 5-8. The dynamic parameters of the cancellation are reported in the Nyquist range in Table 5-3. The most important parameter is $SNDR_{equ.}$ as defined in chapter 2. It describes the amount of the signal power in the presence of the cancellation and noise. It is calculated according to Eq. (6-3) and equals 66.4dB.

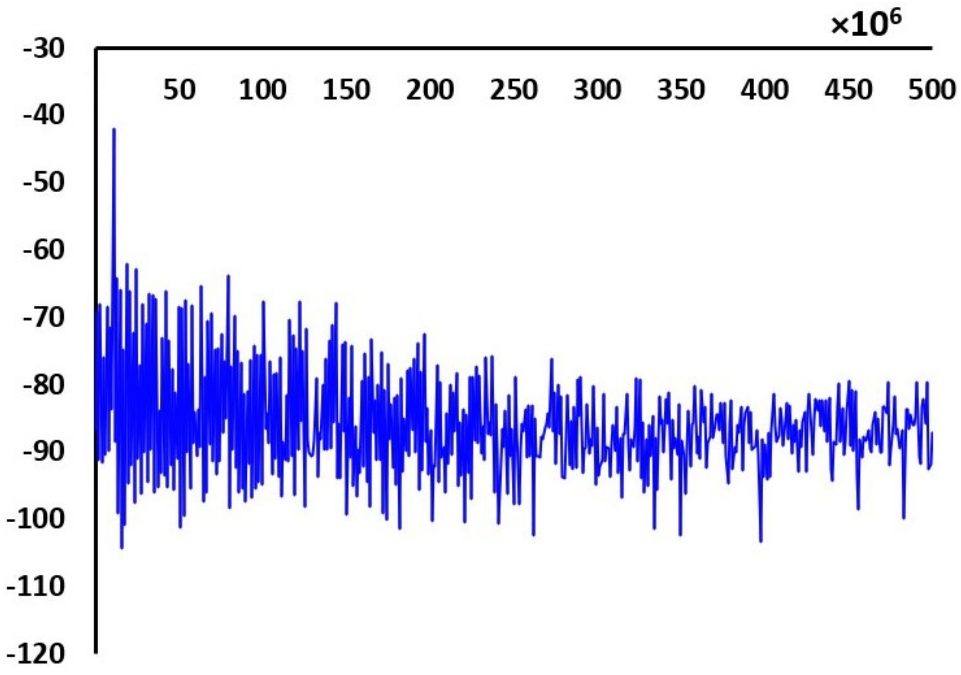


Figure 5-8 The TIA's output spectrum after performing less than -40dB cancellation.

`

Table 5-3 Summary of SIC results with full-scale input.

In. V_p (dBV)	Out. Dif. TIA V_p (dBV)	Cancel. (dB)	SNR dB	SNDR dB	SFDR dBc	THD dB	SNDRequ. dB
8.3	-43	51.3	16.3	15.1	24	-23.5	66.4

5.3.2 Loading Effect of the LNA

In the previous simulation, it is assumed the output resistor of the LNA, R_{BB}, is 2KΩ as a typical output impedance of a current-mode LNA, with a Cascode topology. However, it is critical to consider the loading effect of this resistor on the performance of the SIC. Accordingly, by choosing R_{BB} equals 8KΩ and changing the input SI voltage to achieve the same amount of cancellation of the previous test, it is possible to explore the effect of R_{BB}. The result of this test is reported in Table 5-4. By increasing the output impedance of the LNA, ×4, the dynamic parameter and SNDRequ. changes are negligible. It is also important to mention the 2KΩ resistance is close to the minimum resistance value in a typical current-mode LNA.

5.4 Chip Level

In this section, the goal is to give a better insight about the post-production's result. A few sub-blocks are added to the main design to prepare it for fabrication and test after the tape-out such as the pad's buffers. A few techniques are also mentioned for drawing the layout of the blocks in high-frequency and mixed-signal condition. Drawing the layout can negatively affect the performance of the chip if the layout is

Table 5-4 Summary of SIC vs. two different LNA 's output impedance.

R_{BB} (KΩ)	Out. Diff. TIA V_p (dBv)	Cancel. (dB)	SNR dB	SNDR dB	SFDR dBc	THD dB	SNDRequ. dB
2	-43	51.3	16.3	15.1	24	-23.5	66.4
8	-43	51.3	17.8	16.7	25.8	-25.2	68

`

not drawn well. Finally, some of the post-layout simulations are reported to complete the design process.

5.4.1 Extra Sub-blocks

After finishing the whole design in previous chapters, a few small sub-blocks must be added to the design (layout); hence, the chip can be tested without any issue.

5.4.1.1 Output (Pad) Buffer

The pad and prob capacitance are relatively high, more than 500fF in our case and can negatively impact on the performance of the TIA (SIC).Two sub-blocks are developed to address the driving issue.

First, a class-A buffer is chosen, which is made of high-voltage PMOS (1.8V) RF transistors. Its frequency response, while driving the output load, is shown in Figure 5-9. The buffer has a slight attenuation until a few hundred Mega Hz compared with a the BW_{BB}, 40MHz in our design.

Next, a LPF is used as a second method. It includes a passive 1st order RC filter placed between the TIA and the outside of the chip for monitoring the signal. The summation of the pad and probe capacitance provides the required capacitance of the RC filter

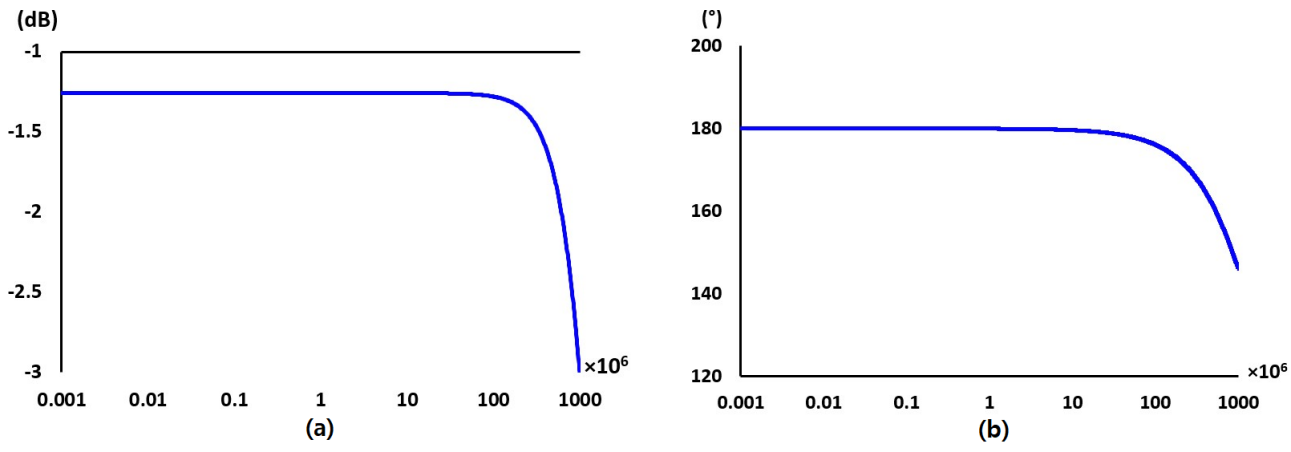


Figure 5-9 Frequency response of the output buffer (a) amplitude in dB (b) phase in (°).

(0.5pF+ 1pF). The 3-dB frequency of the filter is set at 100MHz to show the oversampling and avoid affecting the signal within the system bandwidth BW_{BB}.

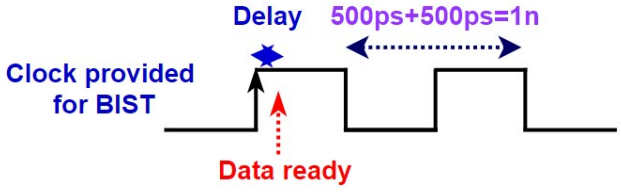
5.4.1.2 Programmable Delay generator

As explained in chapter 4, the BIST was automatically created by Verilog, called *HDL part*. The high-frequency clock of this part is provided by a *manually designed logic*. As shown in Figure 5-10 (a), there is a delay between the original clock and when the output data will be ready.

This delay is computed by simulation, Verilog, is around 120ps. It decreases the effective duty cycle of each phase.

A programmable delay generator is developed to tackle the delay's issue before sending the clock to the capacitive-array. The delay generator has three discrete delay modules, and the delay can be externally controlled. It can provide us with maximum 160ps delay, the summary of the delay is shown in Figure 5-10 (b).

By using the test-bench of the CDAC in working mode 2, Figure 5-3, the simulation is repeated by considering the 120ps delay. The new dynamic parameters at the output of the TIA are reported along with the previous numbers in Table 5-5. As it is clearly shown in the table, the ENOB decreases by 3-bit if the 120ps delay is considered. So, it is vital to have an on-chip block for adjusting fine and coarse delay.



(a)

	b0	b1	b2
Delay	~20ps	~40ps	~100ps

(b)

Figure 5-10 Programmable delay (a) the delay between original clock and prepared data by *HDL part* and (b) amount of 3-bit delay.

`

Table 5-5 Summary of the 2nd mode simulation with and without delay module.

Output of the TIA	ENOB (bit)	SINAD (dB)	SFDR (dBc)	THD (dB)	Signal power (dBV)
Without delay	9.4	58.2	68.4	-69	-9
With delay	6.7	43.2	49.5	-50.4	-11.8

5.5 Layout-level

The layout is a critical step when one develops the chip. Without carefully drawing the layout and arranging a good floor-planning the performance decreases. Two methods are employed to draw the layout, which effectively can boost the performance of the design, namely noise reduction and symmetrical drawing.

- *Noise reduction*: For lowering the noise, the sensitive Analog circuits should not be placed far from the high-frequency digital part. The bulk can also couple the digital noise to the DAC and cause negative effects on the performance of high-frequency and relatively high-resolution DAC. Plus, the high- frequency path can capacitively couple noise to other parts. Hence, it is important to arrange the block in the right location.
- *Symmetrical drawing*: The circuit was developed in the fully-differential manner due to its benefit, hence, the layout should also be symmetric otherwise the design cannot work very well.

5.5.1 Floor-planning

The top-level of the chip is shown in Figure 5-11 (a). The pads are located around the chip, and the chip is divided into two parts, namely *manually designed block* (top of the figure) and *HDL part*. *The manually designed block (Analog) and HDL part are located on the top and bottom of the chip, respectively*. Figure 5-11 (b) provides more details about the

`

Analog or *manually designed block*. It includes four main blocks, namely TIA, two DACs, high-frequency digital control logic, and two sets of coupling capacitors. As visible in the figure below, some effort was made to arrange the symmetrical layout.

The Analog and digital ground are also separated inside the chip to lower the coupling and conducted noise inside the chip, and they are connected outside the chip to have a common ground. The light blue L-shape portion, top-right of the figure, are *coupling capacitors* used for the Analog part. Likewise, the dark blue L-shape, bottom-left of Figure 5-11 (b), acts as *coupling capacitors* for the digital part.

5.5.2 *The Capacitive Array*

The capacitive-arrays are arranged like a matrix, shown in Figure 5-12, to improve the performance of the design. In other words, various kinds of layout techniques are employed to suppress the non-linearity such as symmetrical switching. The layout configuration is completely symmetric, in this dissertation, compared to the centre of the array, as shown in the figure below. In Figure 5-12 *TH*, *bi* (*i* varies from 5 to 9), *Cap*, and *D* cells represent thermometric cell, binary cell, just include capacitor cell and

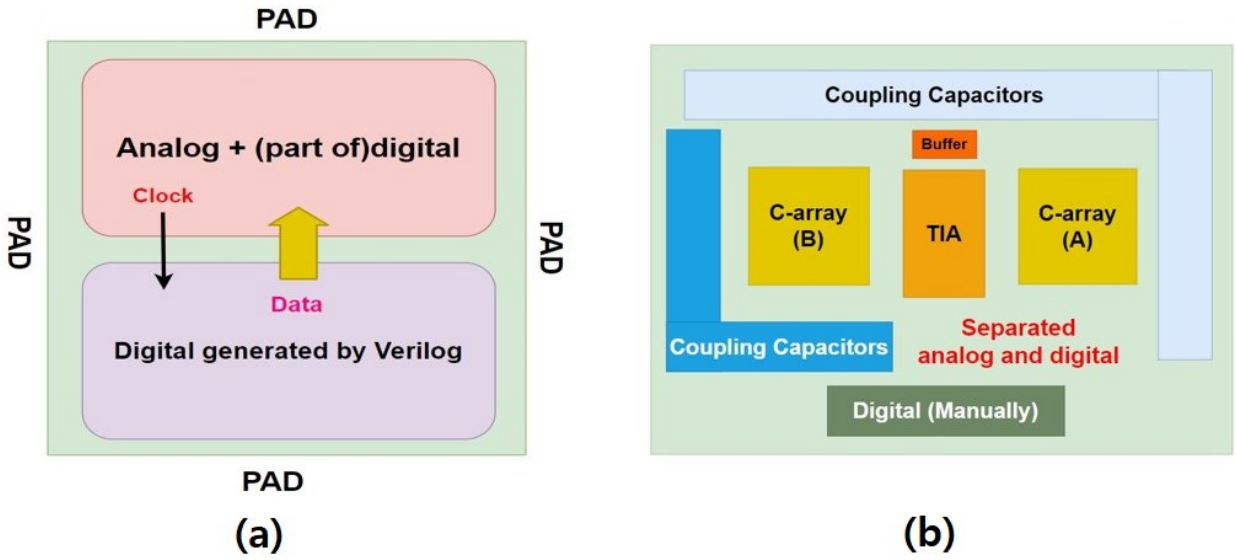


Figure 5-11 (a) Top-level of the chip and pads' location (b) floor-planning of the *manually designed block*.

D	D	D	D	D	D	D	D
D	TH	TH	TH	TH	TH	TH	D
D	TH	TH	TH	TH	TH	TH	D
D	TH	TH	TH	TH	TH	TH	D
D	b7	b8	b9	D	Cap	Cap	D
D	Cap	Cap	TH	b5	b6	D	D
D	TH	TH	TH	TH	TH	TH	D
D	TH	TH	TH	TH	TH	TH	D
D	TH	TH	TH	TH	TH	TH	D
D	D	D	D	D	D	D	D

Figure 5-12 The floor-planning of the 10-bit CDAC, 3Bin-W+2Bin-W+5THco, along with the extra capacitors and dummy loads [53], [57].

dummy cell all explained in chapter 4. The dummy cells are placed around the array to further separate the peripheral capacitors from the border.

This kind of configuration makes the capacitive-array insensitive to linear gradient in any directions, like a traditional common-centroid layout, but also to the mentioned radial gradients [53], [57].

5.5.3 Thermometric Configuration

The thermometric (cells) distribution is shown in *Ci* and *Rj* represents column and row bits, respectively. The generated bits enter the Analog part from BIST part.

	C0	C1	C2	C3	C4	C5
R0	29	27	25	26	28	30
R1	17	15	13	14	16	18
R2	5	3	1	2	4	6
R3	Not used			31	Not used	
R4	11	9	7	8	10	12
R5	23	21	19	20	22	24

Figure 5-13 Thermometric cells distribution (Matrix) to reduce the process errors [53].

`

	C0	C1	C2	C3	C4	C5
R0	29	27	25	26	28	30
R1	17	15	13	14	16	18
R2	5	3	1	2	4	6
R3	Not used			31	Not used	
R4	11	9	7	8	10	12
R5	23	21	19	20	22	24

Figure 5-14 Illustration of thermometric configuration for the code equivalent 17.

For example, as shown in Figure 5-14, if the 5 most-significant-bit are equal to 10001 (Binary), 17 (Decimal) all the column in the *R2* and *R4*, shown Figure 5-14, and part of the column *R1* (five columns) will be selected. In this way, by increasing (or decreasing) the code, the chosen cells move around the centre to alleviate the negative effects of linear and gradients in the oxide.

5.5.4 MOM Capacitor

It is worthy to give more information about the available capacitor in the PDK, namely, Metal-oxide-metal (MOM). It is very similar to the metal-insulator-metal (MIM) capacitors but with an oxide layer between metals and is usually made by interdigitating metal layers with the process oxide. So, the capacitance is created in two places: *laterally with the other fingers and vertically cwith the other layers*. The parasitic value is also 0.6 percentage of its nominal value, which is good for our design.

5.5.5 The Layout of the whole Chip

The layout of the *manually designed block* (Analog part) and the whole chip are shown in Figure 5-15 and Figure 5-16, respectively. The labels on the figure below shows the real position I the *manually designed block*. A careful look shows that the layout is completely symmetric and comply with fully differential design rule. The bottom of Figure 5-16 is developed by behavioural language (HDL). The outputs of this part enter the top part from the centre of the chip. The pins' location is arranged to have a short distance to the targeted sub-blocks, and 20 pins are assigned for *manually designed block*

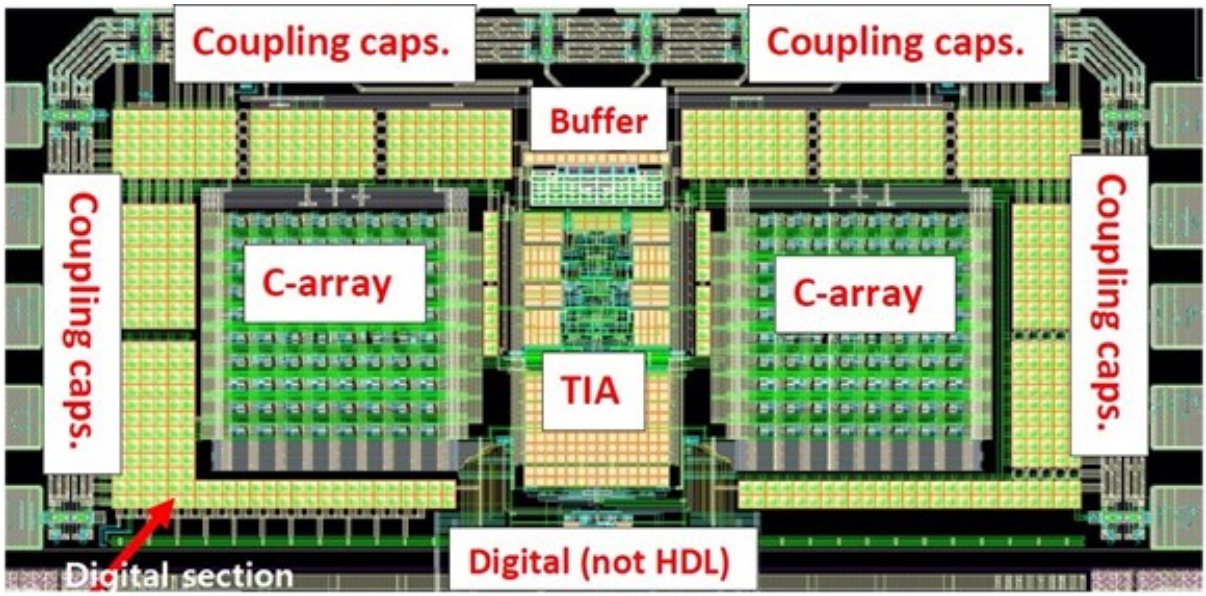


Figure 5-15 M*anually designed block* of the chip including the TIA and CDAC.

and a similar number for the *HDL part*. It is also obvious that the ground of the Analog and digital ground, even in the pad- ring, are separated.

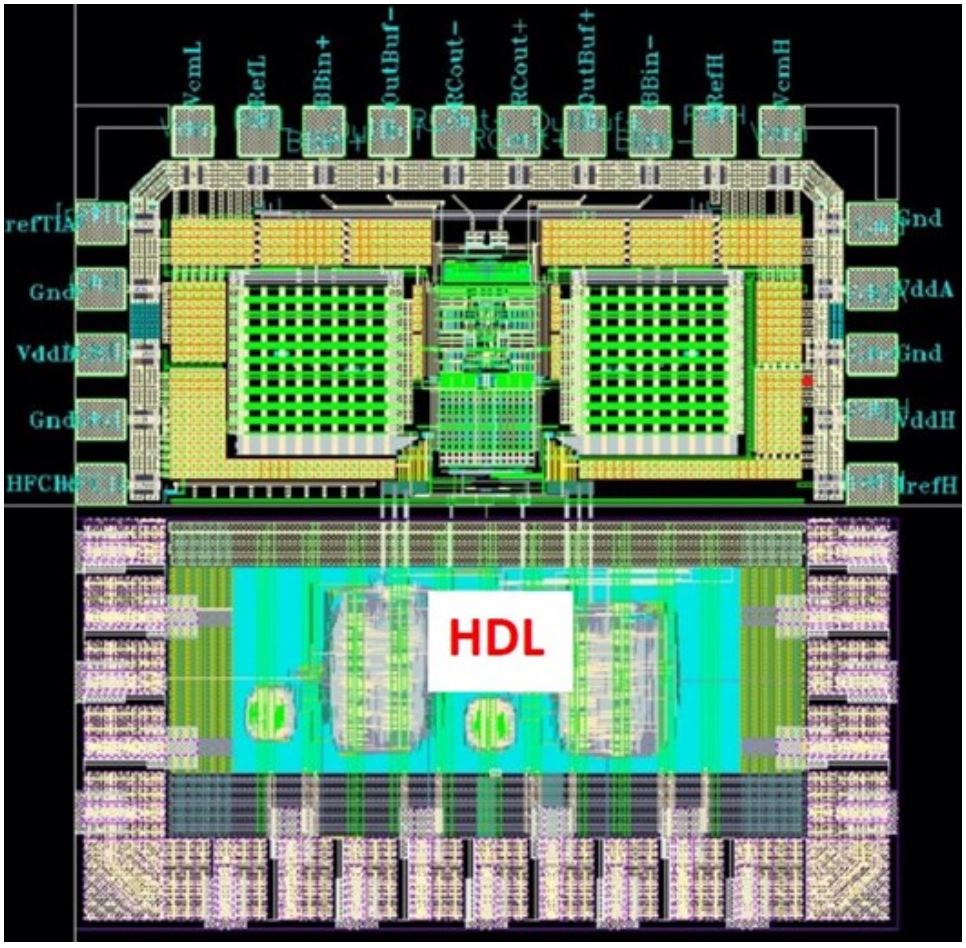


Figure 5-16 The layout of the whole chip including BIST and Analog part.

5.5.6 *Post-layout Simulation*

As a last part of this chapter, the simulation results after drawing the layout are presented. It is obvious that there should be some degradation compared to the schematic simulation due to parasitic and other non-linearities source.

5.5.6.1 TIA Open-loop:

The post-layout simulation of the open-loop TIA, using the test-bench of Figure 3-14, are shown in (a) and (b). They illustrate the phase and amplitude in degree and dB, respectively. The red and blue curves represent the simulation response before and after drawing the layout, respectively. According to these graphs, the GBW and phase-margin are changed from 4.3GHz to 3.75GHz and from 61.5° to 53° after drawing the layout.

5.5.6.2 DNL

After drawing the layout, the DNL diagram is shown in Figure 5-18. The value of the DNL after drawing the layout is $|DNL_{Post-layout}| < 1.3$ while it is $|DNL| < 0.7$ before it. It clearly shows the parasitic effect on the DNL.

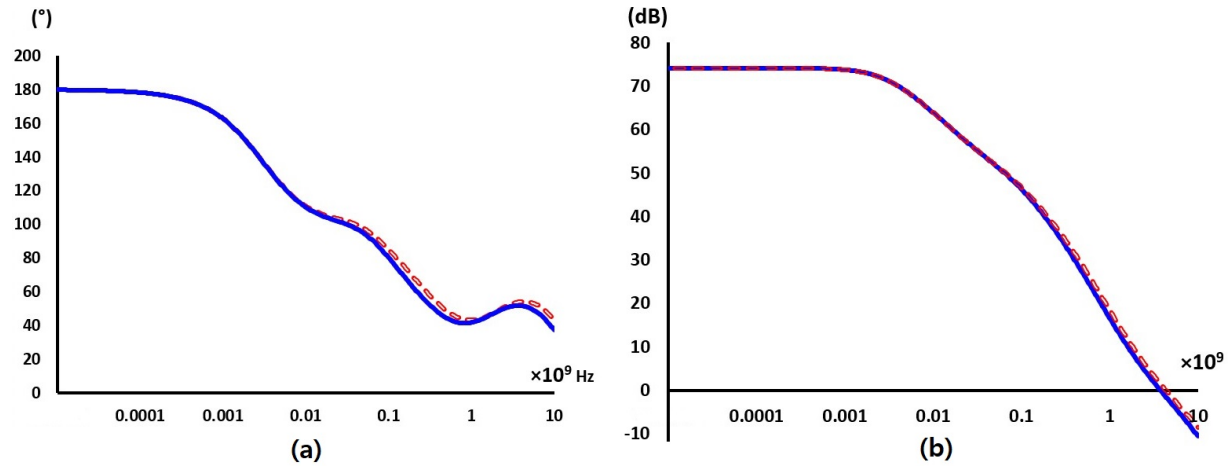


Figure 5-17 The open-loop frequency response of the TIA before (Red) and after (Blue) drawing the layout (a) phase in degree (b) amplitude in dB.

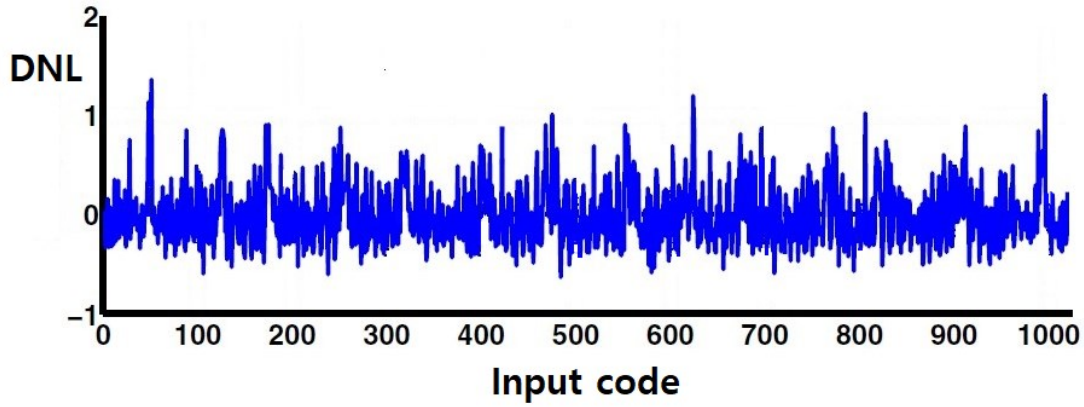


Figure 5-18 DNL post-layout simulation of the CDAC in 2nd mode.

5.5.6.3 Dynamic Parameters

To realize how much the simulation results will deviate after drawing the layout, the simulations are repeated in the similar condition of section 5.2 and 5.3 (It is supposed that delay between the clock and data is compensated). The test conditions are like in the previous simulations such as BB frequency (which is set to 10.7421875MHz). The second row of Table 5-6 is compared with the data of its first row. Table 5-7 presents the summary of the SIC result before and after drawing the layout. The information is also reported before cancellation in Table 5-3. The SNDRequ. decreases by 10.7dB. This is due to high-frequency effect of the circuit such as clock feed-though and charge injection.

Table 5-6 Summary of the TIA output (before and after drawing the layout) in the working mode 2.

SIC performance	In. Vp (dBV)	Out. Dif. TIA (dBV)	Cancel. (dB)	SNDR (dB)	SFDR (dBc)	$SNDR_{equ.}$ (dB)
Before drawing the layout	8.3	-43	51.3	15.1	24	66.4
Post-layout	8.3	-35.7	44	11.7	19	55.7

Table 5-7 Summary of the SIC before and after drawing the layout, 4th mode.

Output of the TIA	ENOB (bit)	SINAD (dB)	SFDR (dBc)	THD (dB)	Signal power (dBV)
Before drawing the layout	9.4	58.2	68.4	-69	-9
Post-layout	8.5	52.6	61.3	-60.7	-10.4

Conclusion

The demands for increasing the communication speed is currently growing. One of the alternative options is to employ full-duplex communication to double the data rate. However, this solution suffers from the leakage of the strong transmitter signal to the sensitive receiver path. Hence, it is necessary to remove this self-interference (SI) otherwise either clipping happens or a power-hungry ADC with wide-dynamic range should be designed. Accordingly, an extra block is required to remove the SI called self-interference cancellation (SIC) block. To this end, various kinds of design have been presented by researcher groups. It can occur in either RF, base-band, digital part, or a combination of them.

Here, the output of the mixer has been chosen to feed the cancellation signal at the input of the base-band of the current-mode FD receiver. Hence, the linearity improves due to connecting the cancellation signal generator, digital-to-Analog converter (DAC), to the input of base-band filter (connection to virtual ground). The capacitive DAC (CDAC) has been chosen as the DAC architecture because it just includes switches and capacitors and is compatible with advanced CMOS technology among other advantages. This design includes four main sub-blocks, namely trans-impedance amplifier (TIA), capacitive array, high-speed digital circuit, and built-in-self-test section (BIST). The developed block can act either as a stand-alone DAC or in SIC block mode.

The primary purpose of this design is to remove the TX's leakage from the current-mode receiver's path. In the SIC mode the CDAC works in the 2-way time-interleaved

`

(TI) scheme without using any calibration technique. Hence, the CADC has twice as much time for settling and it makes the design of the TIA much simpler. The clock frequency and resolution of the DAC and total capacitance is 1GHz,10-bit, and 1pF, respectively. This allows to satisfy the necessary dynamic range and create the cancellation current for performing the SIC. Although this DAC is developed to inject the required charge for cancellation, its minor application is to be used as a stand-alone DAC in the Analog (I/Q) transmitters.

If the design works in the SIC mode and cancellation current is chose close to the full-scale along with the output frequency around 10.74MHz the achieved amount of cancellation of the SI, SNDR, SFDR, SNDRequ. are obtained 51.3dB, 15.1 dB, 24dBc, 66.4dB.

The post-layout simulation results are also reported to study the deviation of the results after fabrication. The SIC test, after drawing the layout with the same condition above is as follows. The SI signal at the output of the TIA, SNDR, SFDR, SNDRequ. are equal to 44dB, 11.7dB, 19dBc, 55.7dB.

Possible future developments as the following:

- *Developing the close-loop digital circuits to control the SI dynamic changes.*
- *Developing the new design with higher the clock frequency, such as Mixer clock chosen to be 2.4GHz and boosting the value of the SNDRequ. (The quality of the signal after cancellation).*
- *Integrating the developed SIC with a full receiver or transceiver to study the performance of receiver.*

`

References

[1] http://mmwave.dei.unipd.it/research/6g/

[2] J. Zohu, “Integrated Self-Interference Cancellation for Full-Duplex and Frequency-Division Duplexing Wireless Communication Systems.” PhD thesis, Columbia University, 2017.

[3] S. Adeolu TIJANI,” Self-interference Cancellation Techniques for SAW-less Transceivers.” PhD thesis, University of Pavia, 2017.

[4] T. Zhang, C. Su, A. Najafi and J. C. Rudell, "Wideband dual-injection path self-interference cancellation architecture for full-duplex transceivers", IEEE Journal of Solid-State Circuits, vol. 53, no. 6, pp. 1563-1576, March 2018.

[5] P. Eloranta, et al., "A Multimode Transmitter in 0.13µm CMOS Using Direct-Digital RF Modulator," IEEE Journal Solid-State Circuits, vol. 42, no. 12, pp. 2774-2784, Dec. 2007.

[6] E. Roverato et al., "All-digital LTE SAW-less transmitter with DSP-based programming of RX-band noise", IEEE J. Solid-State Circuits, vol. 52, no. 12, pp. 3434-3445, Dec. 2017.

[7] N. Zimmermann," Design and Implementation of a Broadband RF-DAC Transmitter for Wireless Communications." PhD Thesis, Niklas, Rheinisch-Westfälischen Technischen Hochschule Aachen, 2011.

[8] I, Fabiaano, "2G-3G SAW-less Analog Front-End." PhD thesis, University of Pavia, 2014.

[9] E. Karegran, "High Performance Building Blocks for SAW-Less Transceivers & Design of Ultra-Low Power Receiver for Wireless Sensor Networks." PhD thesis, University of Pavia, 2014.

[10] "LTE: System Specifications and Their Impact on RF & Base Band Circuits." Application Note, Ver. 1e, Rohde & Schwarz,2013.

`

[11] J. P. Uehlin, W. A. Smith, V. R. Pamula, S. I. Perlmutter, J. C. Rudell and V. S. Sathe, " A 0.0023 mm 2 /ch. delta-encoded time-division multiplexed mixed-signal ECoG recording architecture with stimulus artifact suppression ", IEEE Transaction Biomed. Circuits Syst., vol. 14, no. 2, pp. 319-331, Apr. 2020.

[12] Dirk-Jan van den Broek, "CMOS Front-End Techniques for In-Band Full-Duplex Radio," PhD thesis, University of Twente, 2017.

[13] D. J. van den Broek, E. A. M. Klumperink and B. Nauta, "An in-band full-duplex radio receiver with a passive vector modulator downmixer for self-interference cancellation", IEEE Journal Solid-State Circuits, vol. 50, no. 12, pp. 3003-3014, Dec. 2015.

[14] A. Nagulu, A. Gaonkar, S. Ahasan, S. Garikapati, T. Chen, G. Zussman, et al., "A full-duplex receiver with true-time-delay cancelers based on switched-capacitor-networks operating beyond the delay–bandwidth limit", IEEE Journal Solid-State Circuits, vol. 56, no. 5, pp. 1398-1411, May 2021.

[15] L. Calderin, S. Ramakrishnan, A. Puglielli, E. Alon, B. Nikolić and A. M. Niknejad, "Analysis and design of integrated active cancellation transceiver for frequency division duplex systems", IEEE Journal Solid-State Circuits, vol. 52, no. 8, pp. 2038-2054, Aug. 2017.

[16] M. Abedinkhan Eslami; D. Manstretta; R. Castello"A 2GS/s 10-bit Time-Interleaved Capacitive DAC for Self-Interference-Cancellation Application"16th Conference on PRIME, July, 2021.

[17] F. Maloberti, “Data converter” Springer, 2007.

[18] E. Olieman, "Time-Interleaved High-speed D/A Converters." PhD thesis, University of Twente, 2015.

[19] D. Montanari et al., "An FDD Wireless Diversity Receiver with Transmitter Leakage Cancellation in Transmit and Receive Bands", IEEE Journal Solid-State Circuits, vol. 53, no. 7, pp. 1945-1959, July 2018.

[20] G. Pini, D. Manstretta and R. Castello, "Analysis and design of a 20-MHz bandwidth 50.5-dBm OOB-IIP3 and 5.4-mW TIA for SAW-less receivers", IEEE Journal Solid-State Circuits, vol. 53, no. 5, pp. 1468-1480, May 2018.

`

[21] H. Jung, D. R. Utomo, S.-K. Han, J. Kim and S.-G. Lee, "An 80 MHz bandwidth and 26.8 dBm OOB IIP3 transimpedance amplifier with improved nested feedforward compensation and multi-order filtering", IEEE Trans. Circuits Systems I Regular Papers, vol. 67, no. 10, pp. 3410-3421, Oct. 2020.

[22] M. Valla, G. Montagna, R. Castello, R. Tonietto and I. Bietti, "A 72-mW CMOS 802.11a direct conversion front-end with 3.5-dB NF and 200-kHz 1/f noise corner", IEEE Journal Solid-State Circuits, vol. 40, no. 4, pp. 970-977, Apr. 2005.

[23] K. N. Leung and P. K. T. Mok, "Analysis of multistage amplifier-frequency compensation," IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications, vol. 48, pp. 1041-1056, Sep. 2001.

[24] S. S. Chong and P. K. Chan, "Cross feedforward cascode compensation for low-power three-stage amplifier with large capacitive load", IEEE Journal Solid-State Circuits, vol. 47, no. 9, pp. 2277-2234, Sep. 2012.

[25] S. Pernici, G. Nicollini and R. Castello, "A CMOS low-distortion fully differential power amplifier with double nested Miller compensation", IEEE Journal Solid-State Circuits, vol. 28, no. 7, pp. 758-763, Jul. 1993.

[26] B. K. Thandri and J. Silva-Martinez, "A robust feedforward compensation scheme for multistage operational transconductance amplifiers with no Miller capacitors", IEEE Journal Solid-State Circuits, vol. 38, no. 2, pp. 237-243, Feb. 2003.

[27] B. Y. Kamath, R. G. Meyer, P. R. Gray, "Relationship between frequency response and settling Time of Operational Amplifiers", IEEE Journal Solid-state Circuits, pp. 347-352, 1974.

[28] R. Apfel, P. Gray, "A Fast-Settling Monolithic Feedforward Op-Amp Using Doublet Compression Techniques", ISSCC 74, pp. 134-135.

[29] H. Shibata et al., "A DC-to-l GHz Tunable RF ΔΣ: ADC Achieving DR=74 dB and BW=150 MHz at fo=450 MHz Using 550 mW", IEEE Journal of Solid-State Circuits, vol. 47, pp. 2888-2897, December 2012.

[30] B. Razavi, "Design of Analog CMOS Integrated Circuits." Second edition, McGraw Hill, 2017.

[31] N. Codega, "Adaptive Transmitters for Mobile Communications." PhD thesis, University of Pavia, 2013.

`

[32] Yuan-Shih Chen, "Multi-Mode Sub-Nyquist Rate D/A Converter for TV Band Cognitive Radio." PhD thesis, University of California, Berkeley, 2012.

[33] M. Guibord, "Digital-to-Analog Converter (DAC) Output Response." Application note TIPL 4705, Texas Instruments, 2017.

[34] S. Balasubramanian et al., "Ultimate transmission", IEEE Microwave Magazine, vol. 13, no. 1, pp. 64-82, Jan. 2012.

[35] K. Gentile, "Technical tutorial- DDS/ Section 4/ The Effect of DAC Resolution on Spurious Performance" Analog Devices, 1999.

[36] M. Saberi, R. Lotfi, K. Mafinezhad and W. A. Serdijn, "Analysis of power consumption and linearity in capacitive digital-to-analog converters used in successive approximation ADCs", IEEE Transaction Circuits System I: Reg. Papers, vol. 58, no. 8, pp. 1736-1748, Aug. 2011.

[37] A. Chang, H.-S. Lee and D. Boning, "A 12b 50ms/s 2.1mw SAR ADC with redundancy and digital background calibration", Proceedings of the European Solid-state Circuits Conference (ESSCIRC), pp. 109-112, Sept. 2013.

[38] C. H. Lin and K. Bult, " A 10-b 500-MSample/s CMOS DAC in 0.6 mm \$^2\$ ", IEEE J. Solid-State Circuits, vol. 33, pp. 1948-1958, Dec. 1998.

[39] Nandi, T., Boominathan, K. & Pavan, S. (2012). A continuoustime DR modulator with 87 dB dynamic range in a 2 MHz signal bandwidth using a switched-capacitor return-to-zero DAC. In 2012 IEEE on Custom Integrated Circuits Conference (CICC) (pp. 1–4), Sept 9–12, 2012.

[40] T. Wakimoto, Hongxing Li, K. Murase, "Statistical analysis on the effect of capacitance mismatch in a high-resolution successive-approximation ADC" Institute of Electrical Engineers of Japan (IEEJ), Transactions on Electrical and Electronic Engineering, p. 89-93, 2011.

[41] Z. Dai, et al., "A 53-nW 9.1-ENOB 1-kS/s SAR ADC in 0.13μm CMOS for medical implant devices" IEEE Journal Solid-State Circuits, vol. 47, no. 7, pp1585-1593, July 2012.

[42] Vipul J. Patel, "Poly-phased, Time-interleaved Radio Frequency Digital-to-Analog Converter (Poly-TI-RF-DAC)" PhD dissertation, Wright State University, 2017.

`

[43] N. Metha" Sampling Time Error Calibration for Time-Interleaved ADCs" Master of Science thesis, Delft university, 2013.

[44] Q. Wang "A 1.25GS/S 8-bit Time-interleaved C-2C SAR ADC for Wireline Receiver Applications" Master of Science thesis, University of Toronto, 2013.

[45] N. Kurosawa et al., "Explicit analysis of channel mismatch effects in time-interleaved ADC systems", IEEE Transaction on Circuits and Systems-I, vol. 48, no. 3, pp. 261-271, March 2001.

[46] J. J. McCue et al., " A time-interleaved multimode \$Delta Sigma \$ RF-DAC for direct digital-to-RF synthesis ", IEEE Journal of Solid-State Circuits, vol. 51, no. 5, pp. 1109-1124, May 2016.

[47] S. Louwsma, Ed van Tuijl, B. Nauta " Time-interleaved Analog-to-Digital Converters." Springer, ISBN 978-90-481-9715-6, 2011.

[48] R. Schreier, et al, "Design-Oriented Estimation of Thermal Noise in Switched-Capacitor Circuits," IEEE Trans. Circuits and Systems, vol. 52, no. 1, pp. 2358-2368, 2005.

[49] R. Yousry, E. Hegazi and H.F. Ragai, " A Third-Order 9-Bit 10-MHz CMOS \$DeltaSigma\$ Modulator with One Active Stage ", IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 55, no. 9, pp. 2469-2482, Oct. 2008.

[50] K. Ragab, M. Kozak and N. Sun, "Thermal noise analysis of a programmable-gain switched-capacitor amplifier with input offset cancellation.", IEEE Trans. Circuits Systems II: Express Briefs, vol. 60, no. 3, pp. 147-151, Mar. 2013.

[51] J. Xu; A. Tuan Nguyen; D. Khue Luu; M. Drealan; Z. Yang, "Noise Optimization Techniques for Switched-Capacitor Based Neural Interfaces." IEEE Transactions on Biomedical Circuits and Systems, vol. 14, no. 5, pp. 1024-1035, Oct. 2020.

[52] S. A. Tawfik and V. Kursun, "Dual supply voltages and dual clock frequencies for lower clock power and suppressed temperature-gradient-induced clock skew", IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, vol. 18, no. 3, pp. 347-355, March 2010.

[53] T. Miki, Y. Nakamura, M. Nakaya, S. Asai, Y. Akasaka and Y. Horiba, "An 80-Mhz 8-Bit CMOS D/A Converter", IEEE Journal of Solid-State Circuits, Vol. 21, N°6, pp. 983-988, December 1986.

`

[54] K. Kundert, "Simulating Switched-Capacitor Filters with SpectreRF" Designer's Guide Consulting, 2006. https://designers-guide.com/

[55] " Coherent Sampling Calculator(CSC)." Application note 3190, Maxim integrated, 2004. https://www.maximintegrated.com/en/design/technical-documents/app-notes/3/3190.html

[56] P. Athanasiadis, "FFT-tutorial/ Spectrum Analysis/ A Guide for FFT Simulations" Advance CMOS Design (5SFC0), University of Eindhoven, 2017.

[57] S. Brenna, A. Bonfanti, A. Leonardo Lacaita,"A 70.7-dB SNDR 100-kS/s 14-b SAR ADC with attenuation capacitance calibration in 0.35-um CMOS." Analog Integrated Circuit Signal Process, Springer, pp. 357-371, 2016.

`