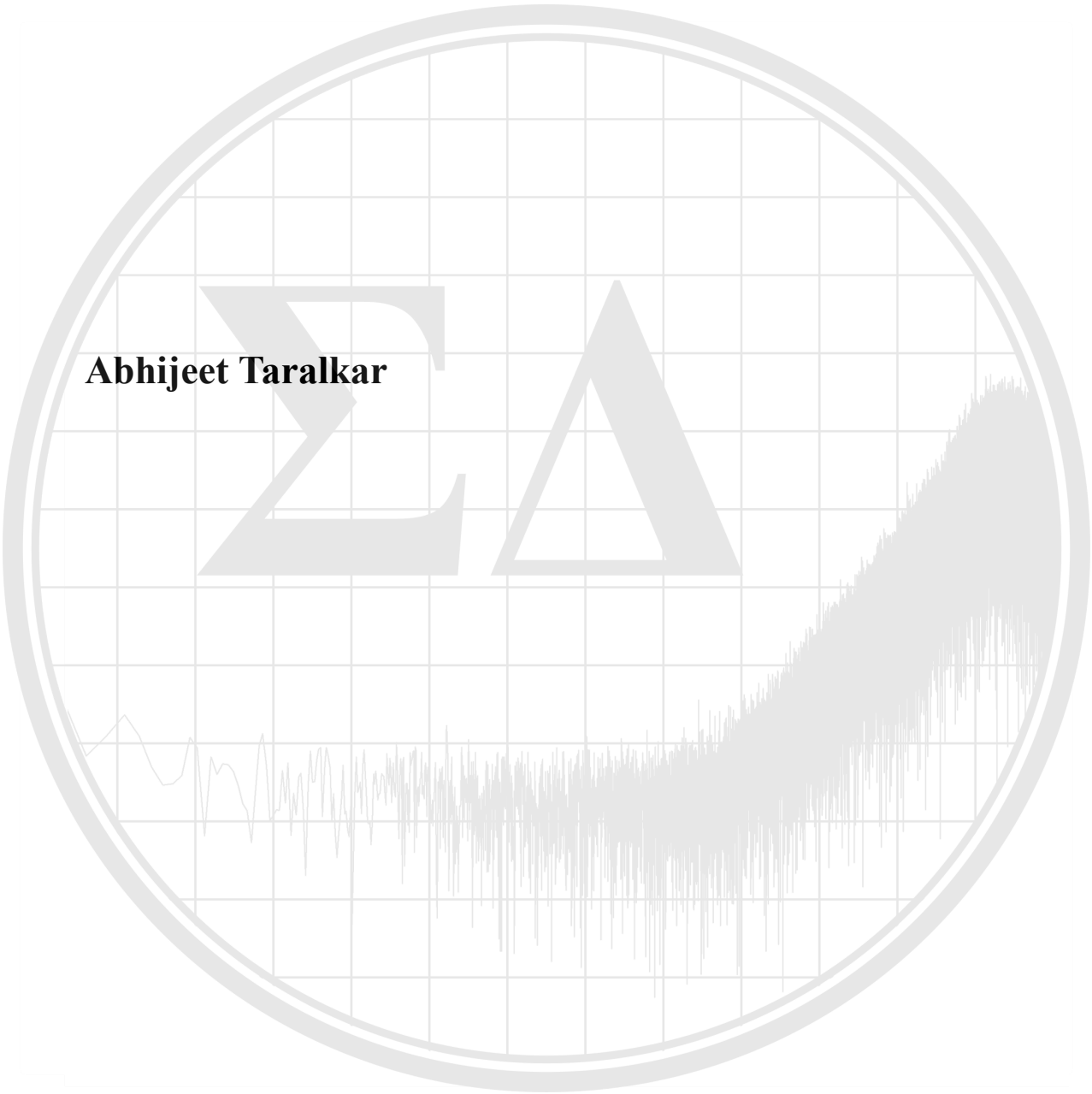
Extended-Range Second-Order Incremental Sigma-Delta ADC



Abhijeet Taralkar

Department of Electrical, Computer and Biomedical Engineering
University of Pavia

Extended-Range Second-Order Incremental Sigma-Delta ADC

Dissertation submitted in partial fulfillment

of the requirements for the degree of

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in

Microelectronics

by

Abhijeet Taralkar

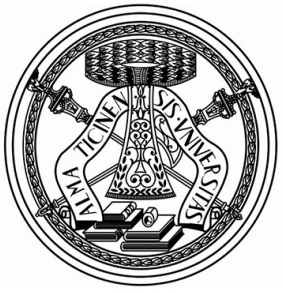
based on research carried out

under the supervision of

Prof. Piero Malcovati

and

Prof. Andrea Baschirotto



UNIVERSITA' DI PAVIA

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Department of Electrical, Computer and Biomedical Engineering
University of Pavia

To

My Beloved Family...

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Abhijeet Taralkar
University of Pavia
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Abstract

A single-stage two-steps Extended-Range Second-Order Incremental ADC in 0.13μm CMOS technology is presented here which achieves a Signal-to-Noise and Distortion Ratio (SNDR) as large as 73 dB. The proposed architecture of Extended-Range ADC based on Second-order multi-bit CIFF Incremental ADC reuses the IADC structure for coarse (input signal) as well as fine (residue) quantization without need of employment of explicit second ADC thereby minimizing power consumption and area occupancy. With a clock frequency of 80 MHz, the complete ERADC achieves in extracted simulation a peak SNDR of 73 dB at a data rate of 3.2 MS/s (25 clock cycles per conversion).

***Keywords*: *Oversampling*; *Sigma-Delta ADC*; *Incremental ADC*; *Extended-Range ADC*; *Noise Shaping*; *Decimation Filter*.**

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Chapter 1

Introduction

As the technology is advancing in the automotive field, the traditionally used mechanical motors are being replaced by the electrical motors to enable the automotive architectures that supports energy efficiency. To meet these requirements, the robust, flexible and intelligent motor driver ICs are needed, so that the size and performance of the product can be optimized. In order to serve such an application, a low power, low area, general purpose 12-bit ADC is necessary.

The obligatory requirements for such an automotive applications for the ADC encompasses a high absolute accuracy, superior linearity, very low offset and noise with low power consumption. These requisites of the automotive are well-suited to the properties of the Sigma-Delta ($\Sigma\Delta$) Modulator [1–11]. The Sigma-Delta Modulators find many applications in various fields from consumer electronics to military applications. However, exercise of the $\Sigma\Delta$M becomes impractical when multiple input sources has to be evaluated, since they retain the quantization noise memory from the previous conversions. This way, this class of ADC actually act upon the complete input signal waveform and not the individual samples. In other words, there is no one-to-one correspondence between present input sample and the digital output equivalent sample but the complete input signal and the complete digital output signal. With standard IC technologies, the performance in terms of SNDR that can be attained by employing these architectures is around 120 dB or ENOB of around 20. The implementation of $\Sigma\Delta$Ms can be done with either continuous-time technique or discrete-time technique.

The Incremental (IADC) ADCs [12–18] overcomes the limitations of the ΣΔMs. With multi-sensor platform, where the analog to digital conversion of more than one signal is desired, the exercise of the Incremental ADC is practical. In this class of ADC, all the analog and digital memory blocks are reset at the beginning of the conversion cycle thereby erasing the quantization noise memory from the previous samples' conversions. Then the next input sample is applied to IADC and the structure is iterated for M number of clock cycle. During this period, the memory blocks in the architecture do retain the noise memory, however, which is from the same sample. At the end of the conversion cycle, it delivers the digital equivalent of the input sample and next cycle starts again resetting the memory blocks. This way, IADCs have advantage of noise shaping property of ΣΔMs within the conversion cycle as well as advantage of one-to-one correspondence of the input sample and output digital equivalent property of the Nyquist ADCs. Therefore, employment of IADC for multi-sensor platform ensures the respective conversion of the input samples without contamination from each other. Nevertheless, in order to achieve high performance in terms of Signal-to-Noise Ratio (SNR) or Dynamic Range (DR), this category of the converts requires high OSR or long conversion time. In other words, the employment of the IADC for the applications with short conversion time or for the signals with large bandwidth is not suitable.

The shortcomings of IADCs can be overcome by exploiting the extended-range techniques which allows the resolution to be increased still maintaining the conversion time relatively short. The Extended Range ADCs (ERADCs) [19–29] are basically two stage ADCs where IADC conventionally serves as a first stage also known as principal ADC. The basic idea behind the extended range technique is to further digitize the residue generated from the first stage, i.e. IADC, through the second stage or supplemental ADC. Since the supplemental ADC is used to process and convert the residue, it is usually referred as Residual ADC (RADC) as well. Based on the different parameters such as power consumption, resolution in IADC, resolution required in RADC, the architecture of the residual ADC is chosen, which can be flash, SAR, pipelined, sigma-delta or even another IADC. Ultimately the two outputs from first stage and the second stage are recombined with proper coefficients which brings the digital output closer to the input signal than output of standalone IADC, thereby improving the performance.

Chapter 2

Proposed Architectures

2.1 Introduction

Sigma-delta modulators (ΣΔM) are the data converters used in most low-signal-bandwidth applications, in many different fields, from consumer electronics to military applications. This kind of A/D converters (ADCs) inherently retains a memory of the quantization noise from previous samples and uses it to push it outside the signal bandwidth, implementing noise shaping, thereby improving the resolution. Along with noise shaping, oversampling is another parameter that plays important role in improving the dynamic range of ΣΔM ADCs. However, because of the inherent memory effect, these converters are only suitable for applications with single input source. Therefore, in applications in which the same ADC has to be used for multiple different input sources, this class of converters becomes impractical.

Incremental ADCs (IADCs) are the appropriate solution to overcome this drawback of ΣΔMs . Since they are reset at the beginning of each conversion cycle, all the memory effects from previous conversions are cleared. Therefore, an IADC operates sporadically, unlike a ΣΔM, delivering the digital output with one-to-one correspondence with the input samples, thereby implying the suitability of IADCs for applications with multiple input sources. Further improvement of dynamic range in IADCs is possible at the expense of higher number of clock cycles per conversion limiting their use in applications with small signal bandwidth.

Extended-Range Incremental ADCs (ERADCs) are a promising alternative to

address high-dynamic range applications while maintaining the conversion time short. An ERADC is basically a two-stage ADC, with an IADC as first stage, a Residue ADC (RADC) as second stage and the required recombination logic [19].

2.2 Incremental A/D Converter:

Some of the crucial key features of the IADC are precise high-resolution even with the poor accuracy in the unit elements, relatively short conversion time, small bandwidth requirement and most importantly, no memory effect, since the architecture is reset after conversion of the every individual sample. This leads to the one-to-one correspondence between the input sample and the output code of the modulator.

Diverse requirements, demanded to develop the different architectures of the IADC and a particular structure need to be chosen to fulfill the given requirements. Therefore, there exists several structures of IADC, out of which some are; feedback architecture, feedforward architecture, modified feedforward architecture of IADC etc.

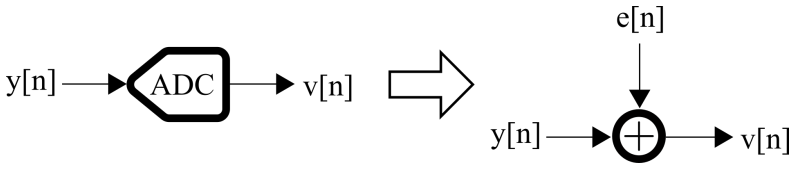


Figure 2.1: ADC modeled as an additive noise source

2.2.1 Second-Order CIFB IADC Architecture:

Feedback structure of the second-order Incremental ADC is shown in Fig.2.2. This structure is comprised of two integrators, followed by quantizer, feedback DACs and Decimation filter as shown. In order to realize the structure, the two DACs need to be implemented. That cause the circuit complexity to increase. Furthermore, the swing requirements of the op-amps are also quite high. The output of the quantizer $V(Z)$ is given by,

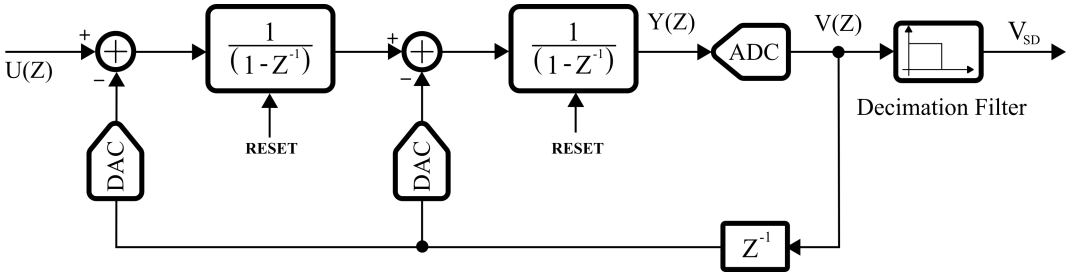


Figure 2.2: Second Order Incremental Feedback Sigma-Delta Modulator Architecture

$$V(Z) = U(Z) + (1 - Z^{-1})^2 E(Z) \tag{2.1}$$

where $E(Z)$ is the additive quantization error added by the quantizer. The input to the quantizer is $Y(Z)$ which is the output of the second integrator which can, then from eq(2.1) and fig. (2.1), be expressed as,

$$\begin{aligned} Y(Z) &= U(Z) + (1 - Z^{-1})^2 E(Z) - E(Z) \\ &= U(Z) + (Z^{-2} - 2Z^{-1}) E(Z) \end{aligned} \tag{2.2}$$

From eq(2.2), it clear that, the output of the second integrator is comprised of input signal component as well as the quantization noise with some transfer function which shows the necessity of high output swing of the op-amp.

2.2.2 Second-Order CIFF IADC Architecture:

In order to reduce the swing requirement of the op-amp, feedforward architecture is developed as shown in Fig. 2.3. The input to the loop filter is only the second order high pass filtered noise i.e. $(1-Z^{-1})^2 E(Z)$, which is passed through a series of two low pass filters, gives exclusive quantization error E(Z) at the output of the second integrator. Since the variance of the noise E(Z) is exceptionally small compared to the signal swing, the swing demand of the op-amp goes down significantly.

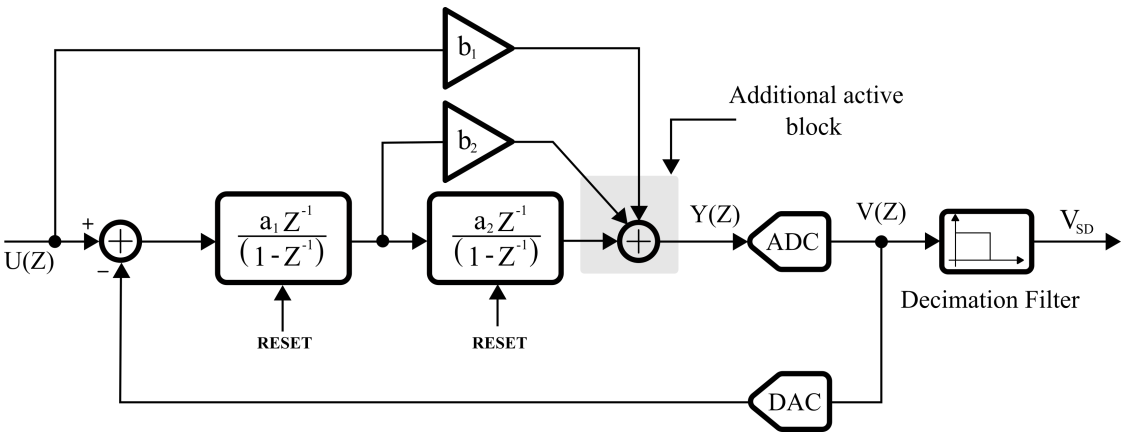


Figure 2.3: Second Order Incremental Feed-forward Architecture of Sigma-Delta Modulator

However, the input signal to the quantizer $Y(Z)$ is still the same as expressed by eq (2.2)

2.2.3 Modified Second-Order CIFF IADC Architecture:

It is explicit from the Fig. 2.3 that, the active adder is mandatory for the addition of the input signal, a signal from first integrator and a signal from second integrator and the resulting signal is provided to the quantizer. To avoid the use of this active adder

and thus to save the remarkable amount of power, the structure is modified as shown in Fig. 2.4. The summing point is moved from output to the input of the second integrator. Thus the integrator can be collaboratively used as an adder as well as an integrator. But since in this scenario, the feedforward signals has to pass through the integrator, they are differentiated prior to the addition so that the resulting input signal to the quantizer remains same.

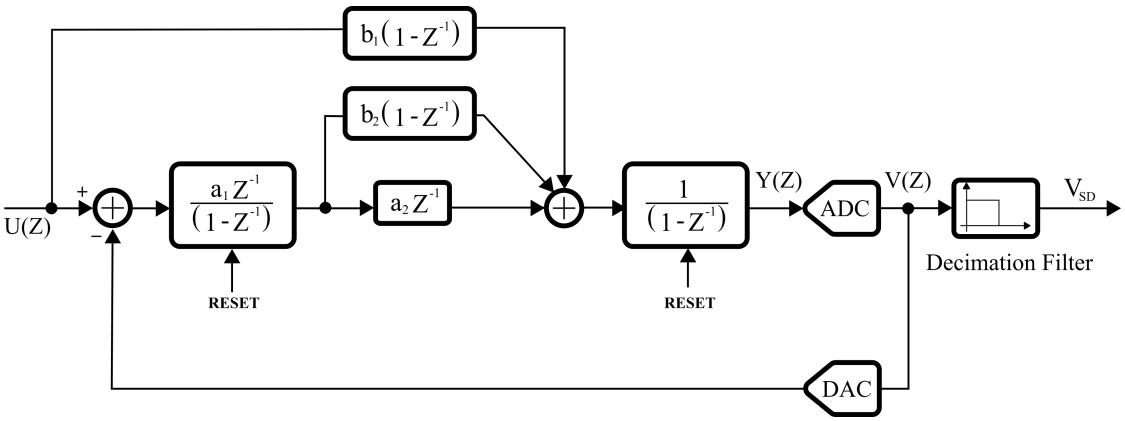


Figure 2.4: Second Order Incremental Modified Feed-forward Architecture of Sigma-Delta Modulator

The block diagram of the second order IADC is shown in Fig. 2.4. This structure is consists of two integrators followed by a multi-bit quantizer, a feedback DAC, delay block, differentiators and the decimation filter. In order to reuse the same hardware to digitize more than one analog input signals, reset feature is incorporated in $\Sigma\Delta$ modulator, hence the name Incremental Sigma-Delta Modulator. The structure is reset at the beginning of the new conversion cycle including analog and digital memory elements. Then next sample is acquired using sample and hold circuit and is applied to the input of the first integrator. If the input signal amplitude is less than or equal to the Maximum Stable Amplitude (MSA), and if the poles of the NTF are well within the unit circle i.e. the system is stable then second integrator output $y[n]$ remains bounded. Then at a given instant, the signals at the output of integrators and summing point can be expressed as,

$$w[j] = w[j-1] + a_1 u - a_1 V_{ref} v[j-1] \tag{2.3}$$

$$sum[j] = b_1 u[j-1] + a_2 w[j-1] + b_2(w[j] - w[j-1]) \tag{2.4}$$

$$y[j] = y[j-1] + sum[j] \tag{2.5}$$

Where the a_1 and a_2 are the modulation coefficients of the integrators, b_1 and b_2 are the coefficients of the feedforward input signal and the first integrator output signal paths respectively, V_{ref} is the reference voltage of the DAC and j is the index of the sampling instant. If the system run for the i number of clock cycles, then the non-iterative expressions of the signals at the output of first integrator, second integrator and the

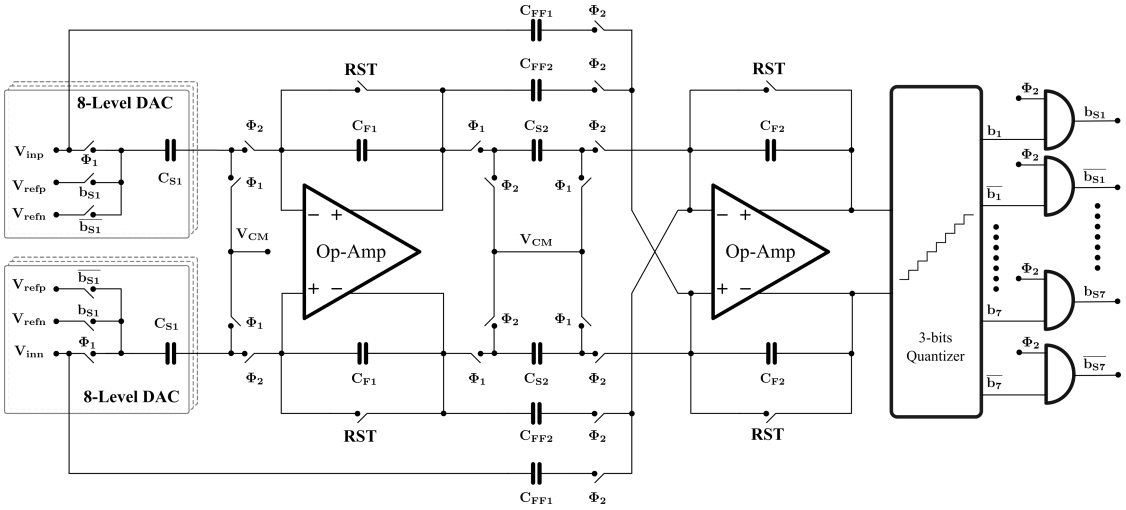


Figure 2.5: Circuit Diagram of Second Order Incremental Modified Feed-forward Architecture of Sigma-Delta Modulator

summing point are,

$$w[i] = a_1 iu - a_1 V_{ref} \sum_{j=1}^{i} v[j-1] \tag{2.6}$$

$$y[i] = b_1 u + b_2 w[i] + a_1 a_2 u \sum_{j=1}^{i} (j-1) - a_1 a_2 V_{ref} \sum_{j=1}^{i} \sum_{k=1}^{j-1} v[k-1] \tag{2.7}$$

The equation for the residue after running the structure for OSR (M) number of clock cycles yields,

$$\begin{aligned} y[M] &= b_1 u + b_2 w[M] \\ &\quad + a_1 a_2 \frac{M(M-1)}{2} u - a_1 a_2 V_{ref} \left(v[M-2] + ... + (M-1) v[0] \right) \end{aligned} \tag{2.8}$$

Since the terms $y[M]$ and $w[M]$ are negligible, it can be pronounced that the reconstruction of the input signal sample 'u' is attainable from the $(M-2)$ number of output codes of the modulator.

Provided that the oversampling ratio M is high enough, the terms $y[M]$ and $w[M]$ becomes insignificant with respect to the term '$a_1 a_2 V_{ref}(v[M-2] + ... + (M-1)v[0])$' and reconstruction can be achieved by passing this signal through a decimation filter with down sampling by a factor of M i.e. OSR. Thus can be represented as in Eq(2.9).

$$\begin{aligned} V_{SD} &= \frac{2 a_1 a_2}{2 b_1 + a_1 a_2 M(M-1)} V_{ref} \left(v[M-2] + ... + (M-1) v[0] \right) \\ &\approx \frac{2}{M(M-1)} V_{ref} \left(v[M-2] + ... + (M-1) v[0] \right) \end{aligned} \tag{2.9}$$

since $2b_1 \ll a_1 a_2 M(M-1)$, Where V_{SD} represents the close digital equivalent of the input sample.

When the conversion of one sample accomplished, the next cycle starts by resetting the analog integrators and digital memory blocks in the system, next sample is acquired by sample and hold block and cycle repeats for the conversion of the acquired sample.

For multi-bit quantizer, considering second order loop filter with oversampling ratio of M, the obtainable effective number of bit (ENOB) can be expressed approximately as,

$$ENOB = N_{SD} + 2\log_2\ (M) - 2 \tag{2.10}$$

where, N_{SD} is the resolution of the quantizer used in $\Sigma\Delta$ loop and M is the over sampling ratio.

2.3 Extended-Range Incremental ADC

2.3.1 Proposed Architecture - I

For moderate resolutions, the IADC used as a first stage of an ERADC can be based on a first-order architecture, but, when high-dynamic range is required, a second- or higher-order IADC is mandatory. Second-order IADCs can be based either on Cascade of Integrators with Feedback (CIFB) or Cascade of Integrators with Feed-forward (CIFF) architectures. The CIFF topology is typically preferable, since it relaxes the output swing and linearity requirements of the operational amplifier used in the first integrator. In any case the residue of the IADC conversion is available at the output of the second integrator at the end of each conversion cycle [19].

The block diagram of an ERADC based on a second-order CIFF IADC is shown in Fig. 2.6. The IADC, consisting of two integrators followed by an adder, a single-

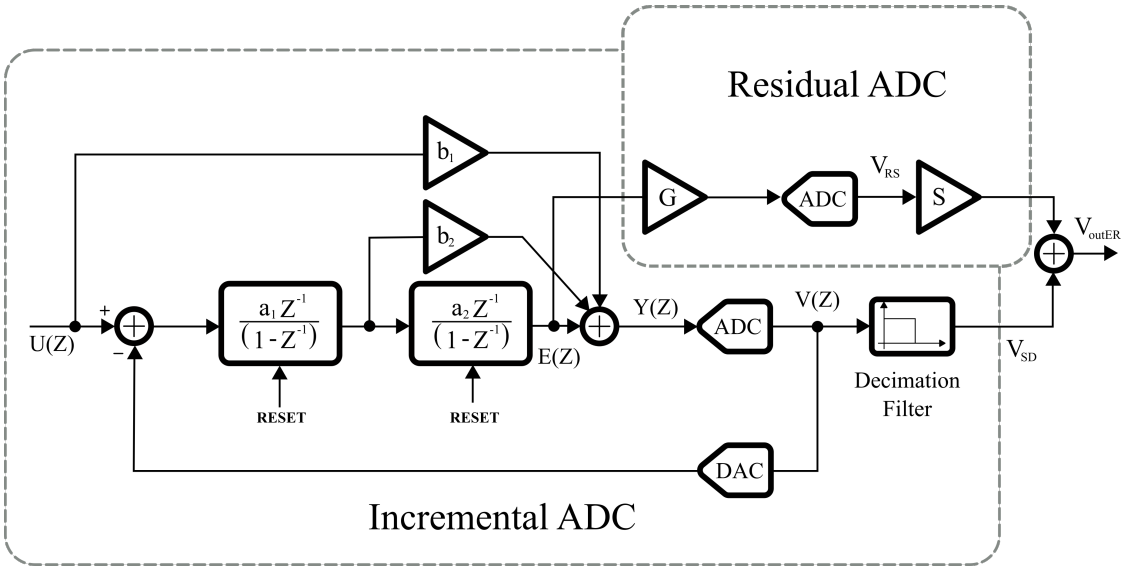


Figure 2.6: Block diagram of an ERADC based on a conventional second-order CIFF IADC topology

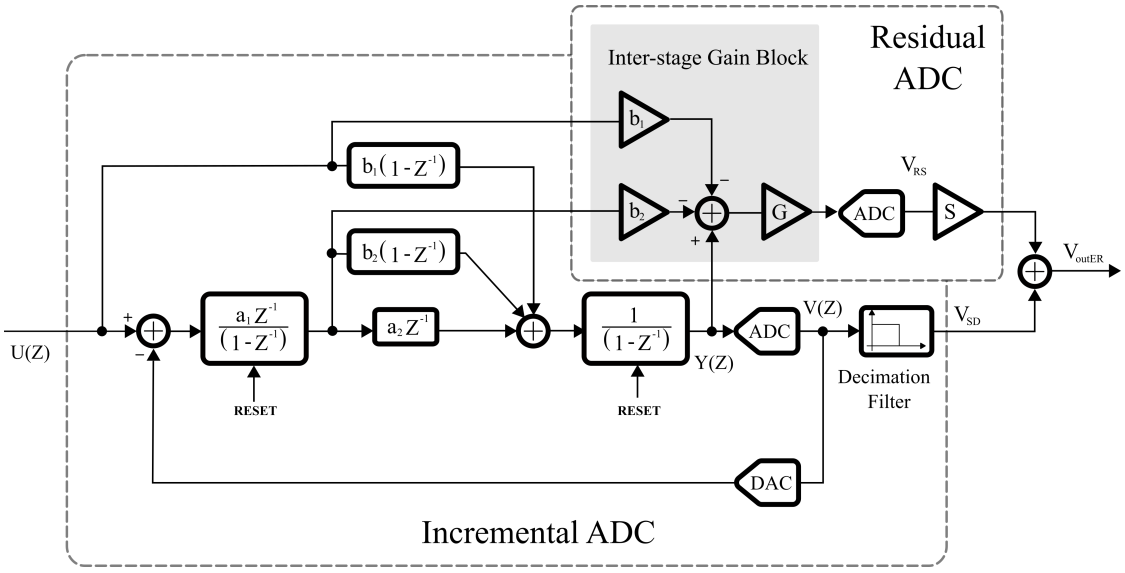


Figure 2.7: Block diagram of an ERADC based on a modified second-order CIFF IADC topology

or multi-bit quantizer, a feedback DAC and a decimation filter, performs the coarse quantization of the input sample. The residue of the coarse conversion is available at the output of second integrator at the end of each conversion cycle. In order to adapt the voltage swing of the residue to the input range of the RADC (typically the same as in the IADC), the residue has to be amplified by a factor G, through an inter-stage gain block (ISG). The amplified residue is then converted into the digital domain by the RADC, providing the fine quantization bit. The coarse and fine bit are finally combined to produce the complete ERADC output word.

It turns out that the use of an active adder in a CIFF IADC can be eliminated if the architecture is modified as shown in Fig. 2.7 [20]. The summing node is moved from the output to the input of second integrator and all the signals are differentiated. In this scheme, the second integrator collaboratively acts as an adder as well as an integrator, thus eliminating the need of an active adder. However,its output does not represents any longer the residue, but it includes also components proportional to the input signal and the first integrator output. Therefore, in order to calculate the residue to be provided to the RADC, these components have to be subtracted from second integrator output at the input of the ISG block. The ISG block, therefore, in this case collectively serves as an adder and an amplifier, avoiding the need of any additional active element for the residue calculation.

The inter-stage gain factor G can be implemented either with an actual amplifier with gain G or by scaling the RADC full-scale voltage by a factor G with respect to the IADC full-scale voltage. In the second case, the residue can be applied directly to the RADC, without the need of any active ISG block. However, in the ERADC architecture shown in Fig. 2.7, the input signal and first integrator output components present in the

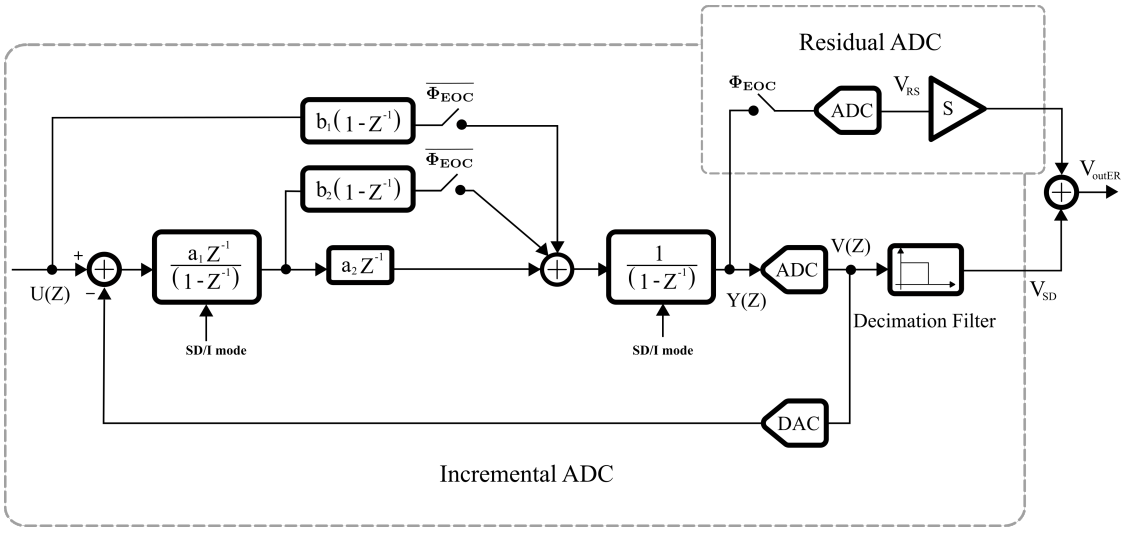


Figure 2.8: Block diagram of the proposed ERADC based on a modified second-order CIFF IADC topology

second integrator output make the use of an ISG block unavoidable, whereas the ERADC architecture shown in Fig. 2.6, does not need an ISG block, but it does need an active adder before the quantizer, leading in both case to extra power consumption.

The proposed ERADC architecture, shown in Fig. 2.8, does not require an ISG block nor an active adder in front of the quantizer of the IADC, since it performs the subtraction of the input signal and first integrator output components also at the input of the second integrator during the last clock cycle of the conversion, thus producing at the output of the second integrator directly the residue. The RADC is simply a SAR ADC, which samples the output of second integrator of the IADC during the last clock cycle of each conversion.

The implementation of the proposed architecture has been shown in more details in Fig.2.13, where RADC consists of just a quantizer, the reference voltage of which is G times smaller than that of IADC, and two switches. The decimation filtering of the output samples from IADC and the scaling the output of RADC is done in the digital domain and off-chip.

The IADC is reset before the beginning of each conversion cycle in order to clear any memory from previous samples. During the coarse conversion phase, the switches driven by $\overline{\Phi_{EOC}}$ are closed, while those driven control signal Φ_{EOC} are open, as shown in Fig. 2.9. If the IADC conversion lasts for i clock cycles, then the signal $y[i]$ at the output of second integrator can be expressed as

$$y[i] = b_1 u + b_2 w[i] + a_1 a_2 u \sum_{j=1}^{i} (j-1) - a_1 a_2 V_{ref} \sum_{j=1}^{i} \sum_{k=1}^{j-1} v[k-1] \qquad (2.11)$$

where u is the input signal (assumed constant), $w[i]$ is the output signal of the first

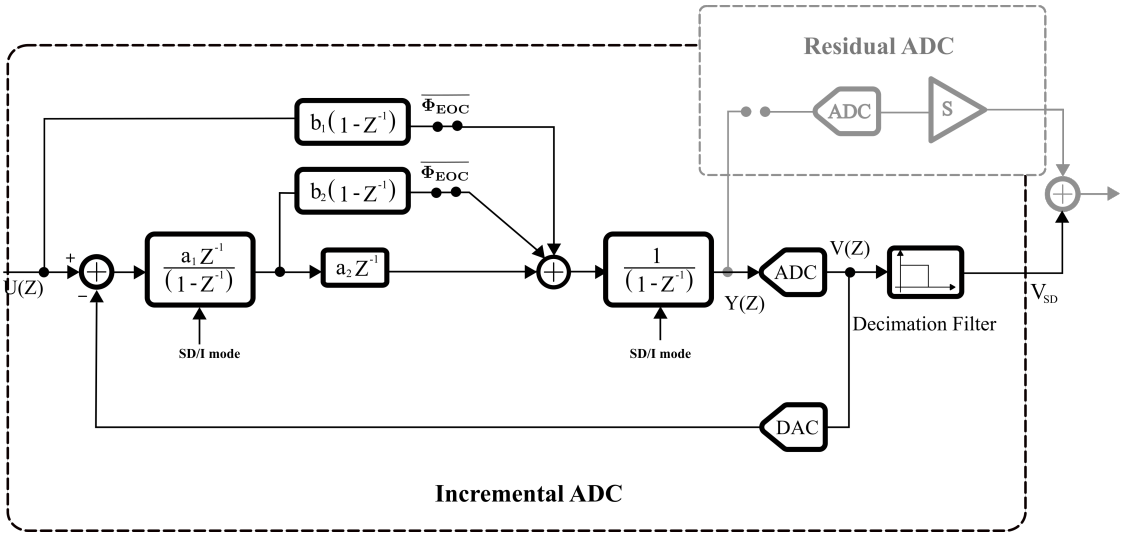


Figure 2.9: Operation of the proposed ERADC during the coarse conversion phase

integrator, a_1 and a_2 are the integrator coefficients ($a_1 = 1, a_2 = 1$) and b_1 and b_2 are the coefficients of the feedforward paths ($b_1 = 1$ and $b_2 = 2$). Parameter M represents the oversampling ratio (i. e. the number of clock cycles of each conversion). The coarse conversion is iterated for $M-1$ clock cycles with the switches driven by control signal $\overline{\Phi_{EOC}}$ closed, while in the last (M^{th}) clock cycle they are opened preventing the feedforward paths to reach the input of the second integrator. The values of $y[M-1]$ and $y[M]$ are then given by given by

$$\begin{aligned} y[M-1] = u + w[M-1] + \frac{(M-1)(M-1)}{2}u \\ - V_{ref}\left(v[M-3] + ... + (M-2)v[0]\right) \end{aligned} \tag{2.12}$$

and

$$y[M] = \frac{M(M-1)}{2}u - V_{ref}\left(v[M-2] + ... + (M-1)v[0]\right) \tag{2.13}$$

respectively.

The filtered and decimated digital output of the IADC can be expressed as

$$V_{SD} \approx \frac{2}{M(M-1)}V_{ref}\left(v[M-2] + ... + (M-1)v[0]\right) \tag{2.14}$$

For a second-order IADC with multi-bit quantizer, the obtainable effective number of bit (ENOB) is approximately given by

$$ENOB_{IADC} \approx N_{SD} + 2\log_2(M) - 2 \tag{2.15}$$

where, N_{SD} is the resolution of the IADC quantizer and M is the oversampling ratio.

Since, for $(M-1)$ clock cycles, the feedforward signals (i. e. $u[i]$ and $w[i]$) are

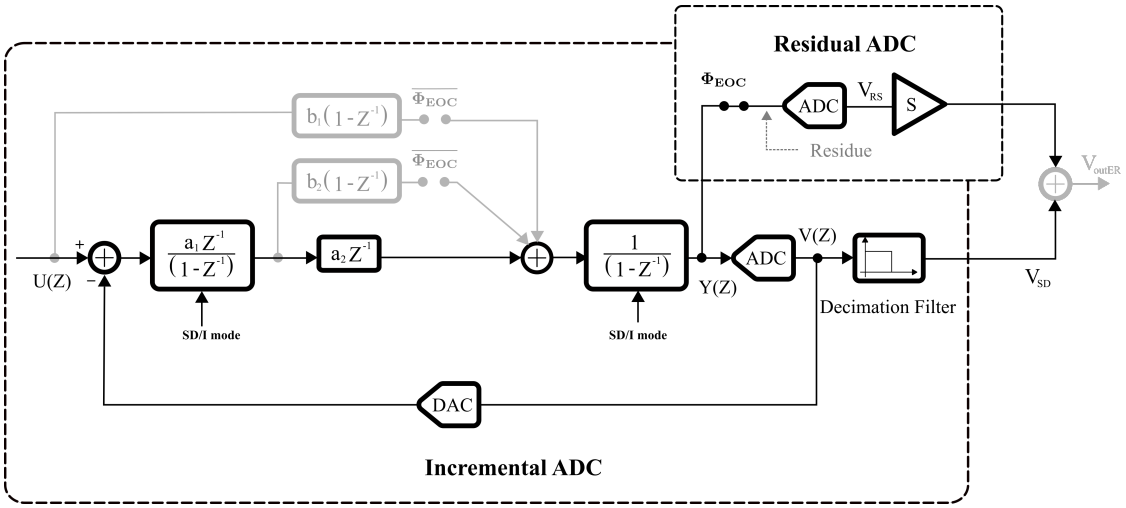


Figure 2.10: Operation of the proposed ERADC during the fine conversion phase

applied to the second integrator input, (2.11) holds. However, in the last clock cycle, these signals are blocked (i. e. $u[M] = w[M] = 0$). Therefore, the expression of the signal at the output of second integrator is given by (2.13). From (2.13), it is clear that in the last clock cycle of the conversion, the output of the second integrator represents the difference between the accumulated input signal and the digital output signal, which is indeed the residue of the IADC conversion, which can be directly applied to the RADC, as shown in Fig. 2.10.

In particular, the output voltage of the second integrator is sampled by the Sample-and-Hold (S/H) block of the SAR RADC. The reference voltages of the SAR RADC are scaled down by a factor of $G = 2^{(N_{SD}-1)}$ with respect to the IADC reference voltages, so that the residue actually covers the whole SAR RADC input range. The SAR RADC runs for N_{RS}, N_{RS} being the resolution of the SAR RADC, as illustrated in Fig. 2.11. The output of the SAR RADC V_{RS} is the digital representation of the residue. In order to recombine the RADC output with the IADC output, V_{RS} is passed through a scaling block with scaling coefficient S, given by

$$S = \frac{2}{M(M-1)} \tag{2.16}$$

The recombination of the outputs of the IADC (V_{SD}) and the RADC (V_{RS}) with proper coefficients results in the digital output V_{outER}, given by

$$V_{outER} = \frac{2}{M(M-1)} \left(V_{RS} + V_{ref}(v[M-2] + ... + (M-1)v[0])\right) \tag{2.17}$$

Therefore, the overall achievable ENOB can be expressed as

$$ENOB_{TOT} \approx N_{RS} + N_{SD} + 2\log_2(M) - 2 \tag{2.18}$$

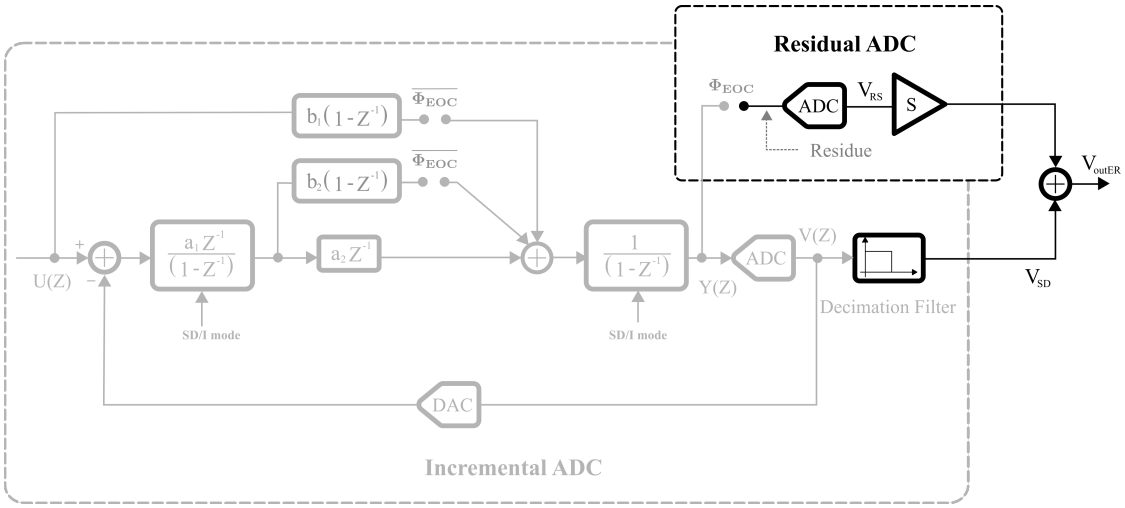


Figure 2.11: Operation of the proposed ERADC during the recombination phase

The timing diagram of the proposed ERADC is shown in Fig. 2.12. The total number of clock cycles available for the conversion is 24. Choosing $M = 18$ as oversampling ratio in the IADC, we use 19 clock cycles, since one clock cycle is needed for the reset at the beginning of each conversion cycle. Therefore, the IADC runs for 18 clock cycles, out of which, only for 17 clock cycles the feedforward paths are connected to the second integrator input, while in the 18^{th} clock cycle they are not. Therefore, the control signal $\overline{\Phi_{EOC}}$ is high for first 17 $(M-1)$ clock cycles and goes low in the last 18^{th} (M^{th}) clock cycle. Accordingly, the control signal Φ_{EOC} is high only in the 18^{th} (M^{th}) clock cycle,

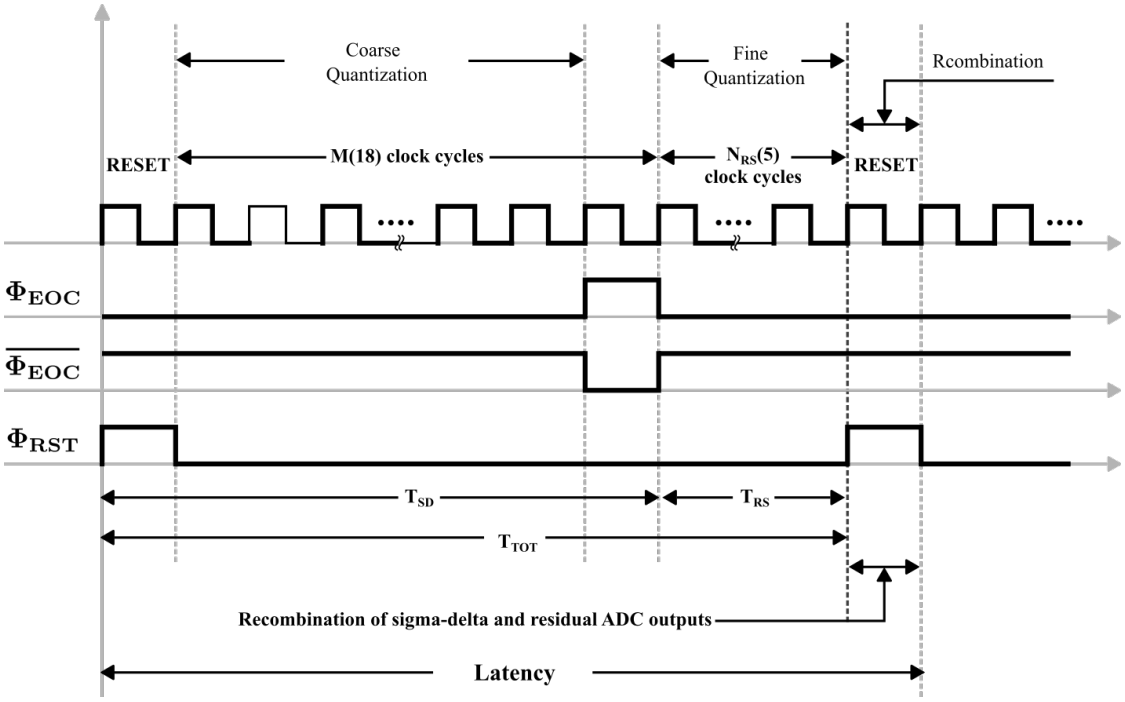


Figure 2.12: Conversion timing in an extended-range IADC

where residue is generated and applied to the RADC. Then, the SAR RADC runs next for

5 (N_{RS}) clock cycles, converting the residue. In the next clock cycle, which is in fact the reset cycle of the IADC, the available digital outputs from both stages are recombined, delivering the extended-range output (recombination phase). The total conversion time T_{TOT} is then given by

$$\begin{aligned} T_{TOT} &= T_{SD} + T_{RS} \\ &= \left(\frac{M+1}{F_{ck}}\right) + \left(\frac{N_{RS}}{F_{ck}}\right) \end{aligned} \tag{2.19}$$

whereas the latency time $T_{LATENCY}$ can be expressed as

$$T_{LATENCY} = \left(\frac{M+1}{F_{ck}}\right) + \left(\frac{N_{RS}}{F_{ck}}\right) + \left(\frac{1}{F_{ck}}\right) \tag{2.20}$$

where, T_{SD} denotes the conversion time of the IADC, T_{RS} the conversion time of the RADC and F_{ck} is the clock frequency.

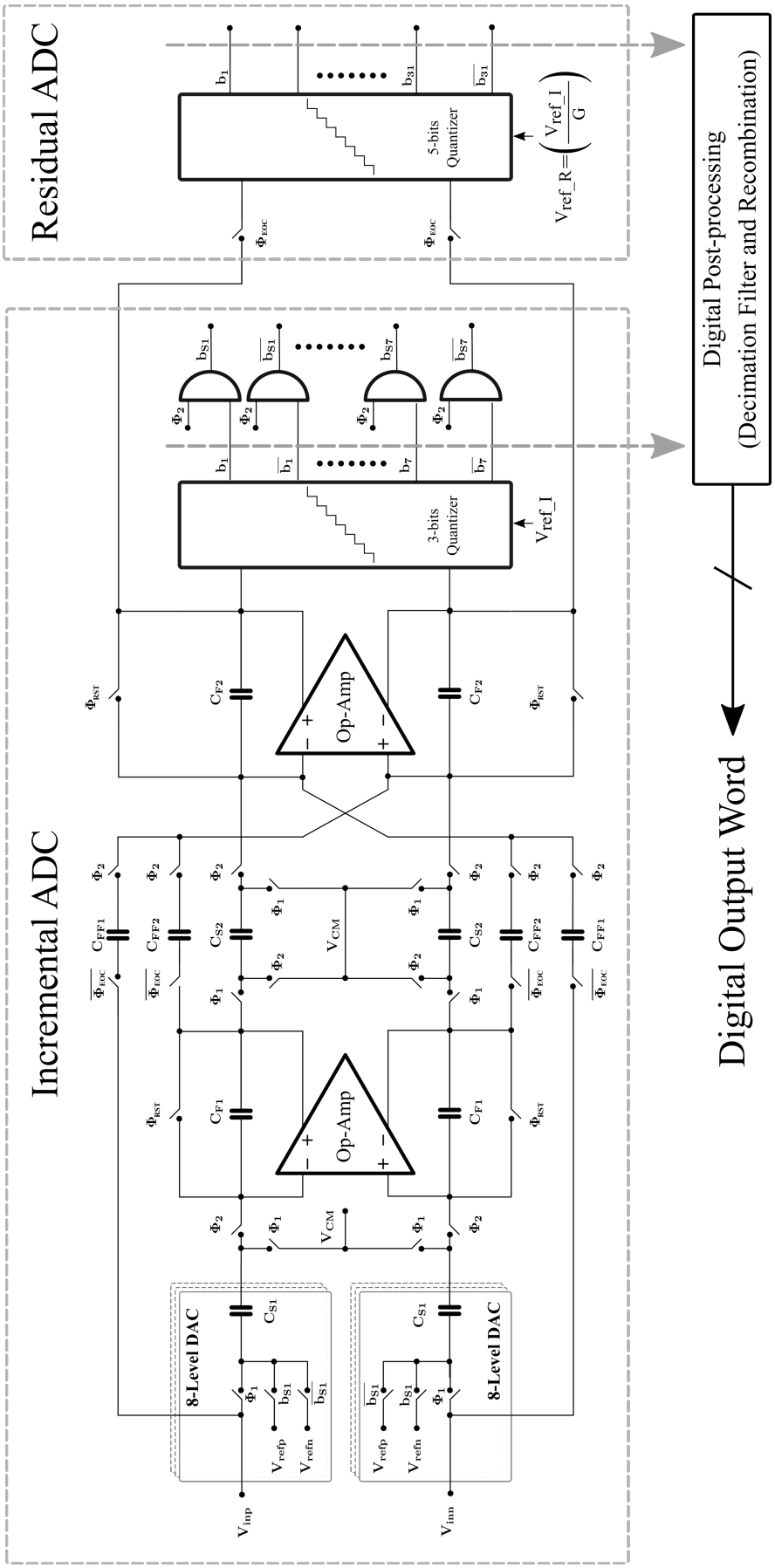
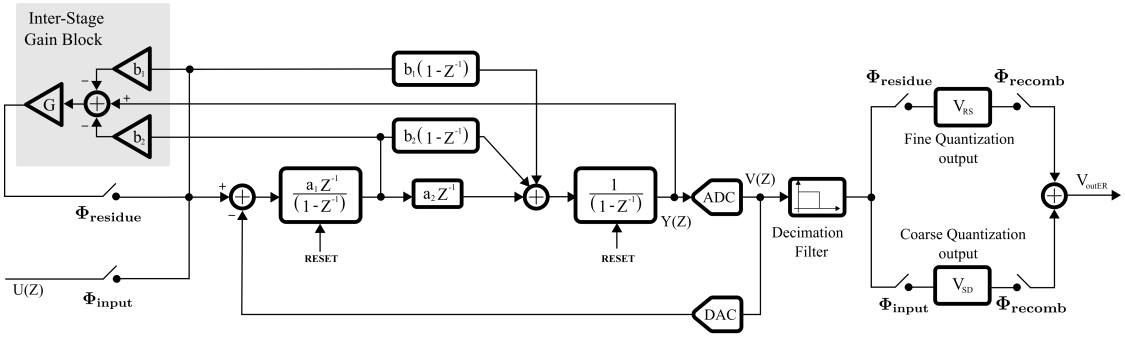


Figure 2.13: Circuit diagram of a proposed Extended-Range second-order CIFF IADC

2.3.2 Proposed Architecture - II

In a conventional Extended-Range ADCs, the implementation of the architecture is usually done with two different ADCs, i.e. first stage (or Principal ADC) and second stage ADC (or Residual ADC) where first stage is usually an Incremental ADC and the second stage could be flash ADC, SAR ADC, pipeline ADC or even incremental ADC etc. based on the quantizer resolution in IADC, quantizer resolution required in RADC, power consumption and the total available conversion time, as shown in Fig. 2.6 and Fig. 2.7.



Extended-Range ADC

Figure 2.14: Block diagram of the proposed architecture of an extended-range IADC

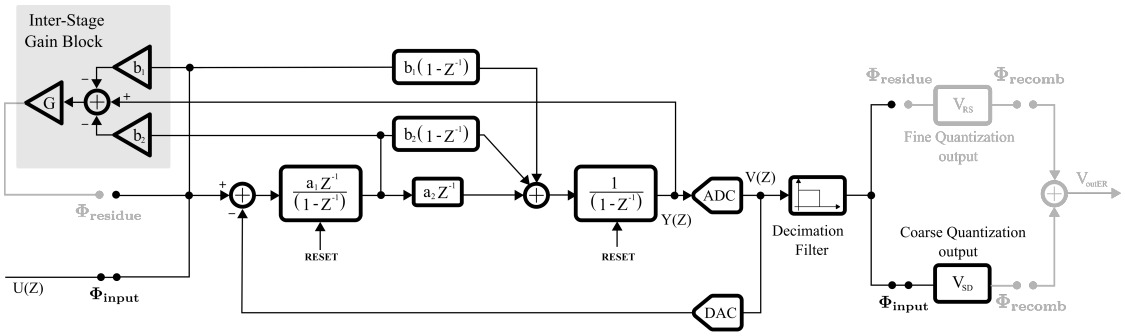
The second order IADC (first stage) consists of two integrators followed by single-bit or multi-bit quantizer, a feedback DAC and digital decimation filter, while second stage is comprised of an Inter-stage Gain block, a quantizer and digital scaling block. The implementation needs the employment of two separate ADCs which involves the designing and the layout for both the stages which in turn becomes a time consuming process. Moreover, along with necessity of more time, the architecture also occupies larger area as well as requires more power (since involves two ADCs). These shortcomings associated with Two-stage ERADCs necessitates to anticipate a solution with lesser hardware so that area, power consumption and the time for the development of the architecture is comparatively reduced.

The block diagram of the proposed architecture of the Extended-Range ADC is shown in Fig. 2.14. Unlike conventional extended range techniques, it comprised of just single-stage A/D converter and the inter-stage gain block where the ADC structure is an Incremental ADC. The IADC exercised is a second-order CIFF modified structure. It consists of two integrators, multi-bit quantizer, feedback DAC, switched-capacitive structure to realise differentiator and delay, decimation filter, memory blocks and recombination logic while ISG consists of active adder to extract the residue dealing the three signals (input sample, first integrator output and second integrator output) as shown in Fig. 2.14 and Fig. 2.20.

The operation of the proposed ERADC architecture can be divided into three sections: coarse quantization, fine quantization and recombination.

Coarse Quantization

The operation of the ADC begins with resetting the analog and digital memory blocks. The switch $\Phi_{residue}$ is opened and the switch with control signal Φ_{input} is closed connecting the input signal to the IADC structure as shown in Fig. 2.15. As long as the amplitude of the input signal $u[n]$ is less than or equal to the Maximum Stable Amplitude (MSA) and the poles of the loop filter lies within the unit circle, the input to the quantizer $y[n]$ remains bounded validating the stability of the IADC.



Extended-Range ADC

Figure 2.15: Proposed architecture of an extended-range IADC configuration in Coarse quantization phase

Then if the IADC structure is iterated for i number of clock cycles, the input to the quantizer at i^{th} clock cycles, i.e. $y[i]$ can be given as,

$$y[i] = b_1 u + b_2 w[i] + a_1 a_2 u \sum_{j=1}^{i} (j-1) - a_1 a_2 V_{ref} \sum_{j=1}^{i} \sum_{k=1}^{j-1} v[k-1] \tag{2.21}$$

where, $a_1 = 1$, $a_2 = 1$ are the integrator's coefficients while $b_1 = 1$ and $b_2 = 2$ are the coefficients of the feed-forward paths. Considering the oversampling ratio for the coarse quantization to be M_1, the non-iterative expression of input to the quantizer at the end of conversion cycle of coarse quantization can then be expressed as,

$$y[M_1] = u[M_1] + w[M_1] + \frac{M_1(M_1-1)}{2} u - V_{ref} \left(v[M_1 - 2] + ... + (M_1 - 1) v[0] \right) \tag{2.22}$$

When the OSR M_1 is very high the term $w[M_1]$ becomes insignificant with respect to the other terms. Then the filtered and decimated output from first conversion V_{SD} is

the coarse digital equivalent of the input sample, can be extracted from Eq.(2.22) and is approximately expressed as,

$$V_{SD} \approx \frac{2}{M_1(M_1-1)} V_{ref} \left(v[M_1-2] + ... + (M_1-1)v[0]\right) \tag{2.23}$$

The quantization error can be given as,

$$\Delta_{SD} = \frac{2}{M_1(M_1-1)} \frac{V_{ref}}{(2^{N_{SD}}-1)} \tag{2.24}$$

Then, the ENOB that can be achieved from the coarse quantization can be expressed as,

$$\begin{aligned} ENOB_{SD} &= \log_2\left(\frac{V_{ref}}{\Delta_{SD}}\right) \\ &\approx N_{SD} + 2\log_2(M_1) - 1 \end{aligned} \tag{2.25}$$

The Signal-to-Quantization Noise (SQNR) can be given as,

$$\begin{aligned} SQNR_{SD} &= 10\log_{10}\left(\frac{\frac{V_{ref}^2}{8}}{\frac{\Delta_{SD}^2}{12}}\right) \\ &\approx 20\log_{10}\left(\frac{V_{ref}}{\Delta_{SD}}\right) \\ &\approx 6N_{SD} + 40\log_{10}(M_1) - 6 \end{aligned} \tag{2.26}$$

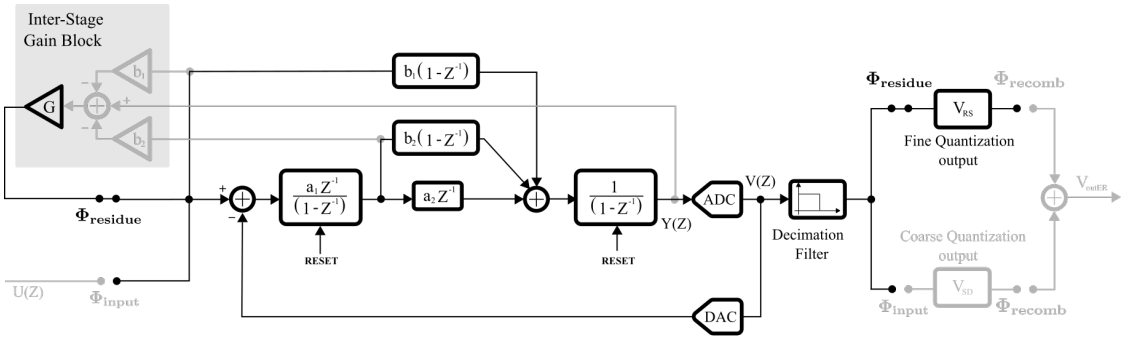
Once the coarse conversion cycle is completed, the output is stored in the digital memory block for the post-processing as shown in Fig. 2.15. It is explicit from Eq.(2.22) that the output of the second integrator in the last clock cycle does not have only the residue but also have the input signal component ($u[M_1]$) and the component of the first integrator's output($w[M_1]$). Therefore, in order to extract the residue, the input signal with coefficient b_1 and the output of the first integrator with coefficient b_2 is subtracted from the output of second integrator only in the last clock cycle.

$$\begin{aligned} e &= y[M] - b_1 u - b_2 w[M] \\ &= \frac{M_1(M_1-1)}{2} u - V_{ref}\left(v[M_1-2] + ... + (M_1-1)v[0]\right) \end{aligned} \tag{2.27}$$

Furthermore, the extracted residue need to be amplified by a factor G which makes the swing of the residue equal to the V_{ref} of the IADC to bring it to full-scale signal amplitude. However, the required amplitude for the IADC is not really the V_{ref} but the MSA of the IADC which is slightly lesser than the V_{ref}. The inter-stage gain block collectively serves as a subtractor as well as an amplifier, thus calculating the residue prepared for the further processing.

Fine Quantization

Similar to the operation of coarse quantization phase, that of fine quantization also start with resetting the analog blocks and digital decimation filter in the structure, thereby erasing the memory from the coarse quantization. The control signal Φ_{input} is pulled to zero opening the switch and disconnecting the input while the switch controlled by control signal $\Phi_{residue}$ is closed thereby connecting the residue from ISG to the IADC structure as shown in Fig. 2.16.



Extended-Range ADC

Figure 2.16: Proposed architecture of an extended-range IADC configuration in Fine quantization phase

Then, if the IADC is further iterated for M_2 (i.e. oversampling ratio considered for the conversion of residue), then the input to the quantizer at the last i.e. M_2^{th} clock cycle is given by,

$$y[M_2] = e[M_2] + w[M_2] + \frac{M_2(M_2-1)}{2}e - V_{ref}\left(v[M_2-2] + ... + (M_2-1)v[0]\right) \tag{2.28}$$

Since the OSR corresponding to the fine conversion M_2 is high enough, the term $w[M_2]$ becomes small enough compared to the other terms so that the digital equivalent of the residue filtered and decimated, can be derived as,

$$V_{RS} \approx \frac{2}{M_2(M_2-1)}V_{ref}\left(v[M_2-2] + ... + (M_2-1)v[0]\right) \tag{2.29}$$

At the end of fine quantization conversion cycle, the converted residue into digital, is stored in the memory block as shown in Fig. 2.16.

Similarly, the LSB of the IADC, $ENOB$, and the $SQNR$ in fine conversion configuration can be expressed as follows,

$$\Delta_{RS} = \frac{2}{M_2(M_2-1)}\frac{V_{ref}}{(2^{N_{SD}}-1)} \tag{2.30}$$

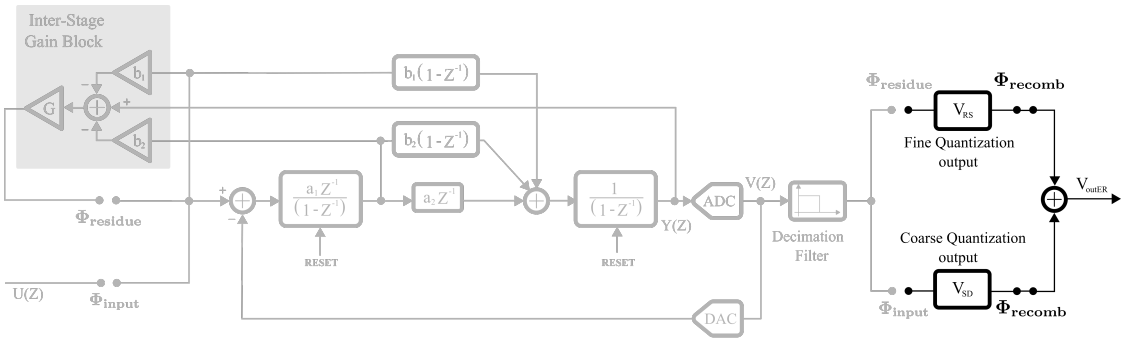
$$ENOB_{RS} \approx N_{SD} + 2\log_2(M_2) - 1 \tag{2.31}$$

$$SQNR_{RS} \approx 6N_{SD} + 40\log_{10}(M_2) - 6 \tag{2.32}$$

Recombination

At the end of the fine quantization cycle, both the outputs, i.e. digital equivalent of input sample as well as the digital equivalent of the residue are available. Then, in the recombination phase these digitized signals are recombined with proper coefficients in order to get the final output i.e. V_{outER} as shown in Fig. 2.17. Then the expression for V_{outER} can be given as,

$$\begin{aligned} V_{outER} &= V_{SD} + \frac{2}{M_1(M_1-1)}V_{RS} \\ &= \frac{2}{M_1(M_1-1)}\left[V_{RS} + V_{ref}\left(v[M_1-2] + ... + (M_1-1)v[0]\right)\right] \\ &= \frac{2}{M_1(M_1-1)}\left[\frac{2}{M_2(M_2-1)}V_{ref}\left(v[M_2-2] + ... + (M_2-1)v[0]\right)\right. \\ &\quad \left. V_{ref}\left(v[M_1-2] + ... + (M_1-1)v[0]\right)\right] \end{aligned} \tag{2.33}$$



Extended-Range ADC

Figure 2.17: Proposed architecture of an extended-range IADC configuration in Recombination phase

The LSB of the overall architecture is,

$$\Delta_{ER} = \frac{2}{M_1(M_1-1)}\frac{2}{M_2(M_2-1)}\frac{V_{ref}}{(2^{N_{SD}}-1)^2} \tag{2.34}$$

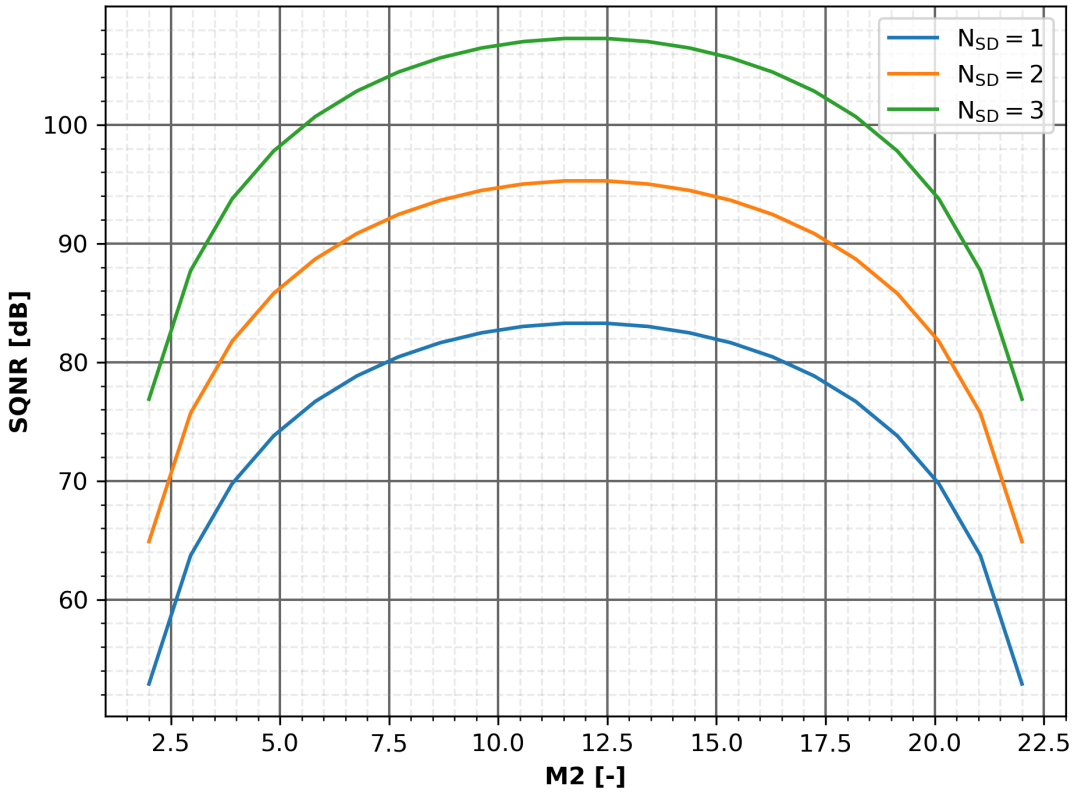


Figure 2.18: SQNR Vs M_2

From the equation above, the total ENOB that can be achieved with this architecture is,

$$\begin{aligned} ENOB_{TOT} &= \log_2\left(\frac{V_{ref}}{\Delta_{ER}}\right) \\ &\approx 2N_{SD} + 2\log_2(M_1) + 2\log_2(M_2) - 2 \\ &\approx 2(N_{SD} - 1) + 2\log_2(M_1 M_2) \end{aligned} \tag{2.35}$$

And the overall Signal-to-Quantization Noise achievable can be derived as,

$$\begin{aligned} SQNR_{TOT} &\approx 20\log_{10}\left(\frac{V_{ref}}{\Delta_{ER}}\right) \\ &\approx 12N_{SD} + 40\log_{10}(M_1) + 40\log_{10}(M_2) - 12 \\ &\approx 12(N_{SD} - 1) + 40\log_{10}(M_1 M_2) \end{aligned} \tag{2.36}$$

The total number of clock cycles required for the complete conversion are, therefore $M = M_1 + M_2$. Then for given quantizer resolution (N_{SD}) and given number of total clock cycles available for conversion (M), what would be the number of clock cycles that can be allocated for the coarse (M_1) and fine conversion (M_2) so that the maximum SQNR can be obtained. This can be found by converting the Eq.2.36 from two variables ($M_1 and M_2$) to single variable either by putting $M_1 = M - M_2$ ($M_2 = M - M_1$),

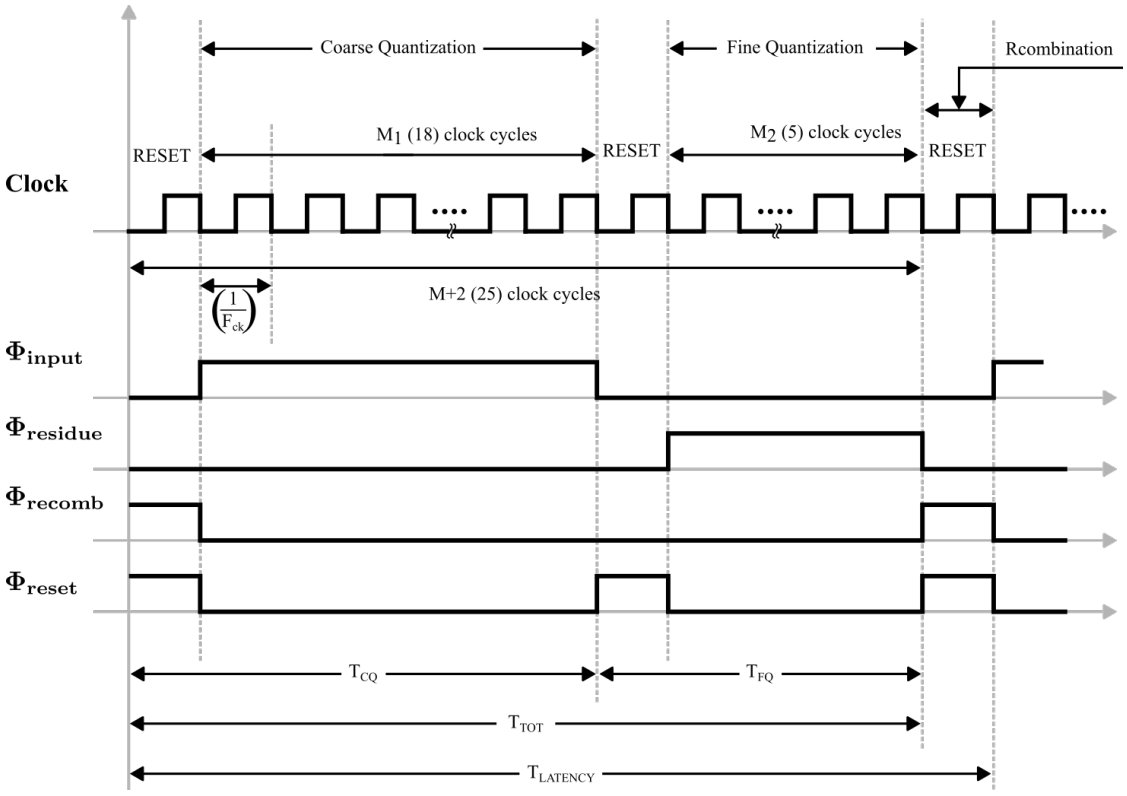


Figure 2.19: Timing Diagram with all the Phases

differentiating it w.r.t. to M_2 (M_1) and equating it to zero.

$$\frac{d}{dM_2} SQNR_{TOT} = 0 \tag{2.37}$$

$$\begin{aligned} \frac{d}{dM_2} SQNR_{TOT} &= \frac{d}{dM_2} \left\{ 12(N_{SD} - 1) + 40 \log_{10} \left[(M - M_2) M_2 \right] \right\} \\ &= 0 + 40 \frac{1}{\ln 10} \frac{M - 2M_2}{(M - M_2) M_2} \end{aligned} \tag{2.38}$$

Equation above Eq.(2.38) represents the derivative or the slope of the $SQNR_{TOT}$ characteristic for given N_{SD} and M and considering M_2 as a variable. Putting the value of Eq.(2.38) in Eq.(2.37) yields,

$$M_2 = \frac{M}{2} \tag{2.39}$$

$$M_1 = M - M_2 = \frac{M}{2} \tag{2.40}$$

This process yields that, in order to achieve maximum SNR possible $M_1 = M_2 = \frac{M}{2}$. This can also be verified from Fig. 2.18. For $M_2 = 12$ (where M is 24, i.e. $M_2 = \frac{M}{2}$), the peak SNR is obtained considering various cases with different values of N_{SD}.

The total conversion time T_{TOT} and Latency time $T_{LATENCY}$ can be given as,

$$\begin{aligned} T_{TOT} &= T_{CQ} + T_{FQ} \\ &= \left(\frac{M_1 + 1}{F_{ck}}\right) + \left(\frac{M_2 + 1}{F_{ck}}\right) \end{aligned} \tag{2.41}$$

$$T_{LATENCY} = \left(\frac{M_1 + 1}{F_{ck}}\right) + \left(\frac{M_2 + 1}{F_{ck}}\right) + \left(\frac{1}{F_{ck}}\right) \tag{2.42}$$

where T_{SD} denotes the time required for the coarse conversion, T_{RS} is the time required for the fine conversion, M_1 is the OSR for the coarse conversion, M_2 is OSR for fine conversion and F_{ck} is the clock frequency.

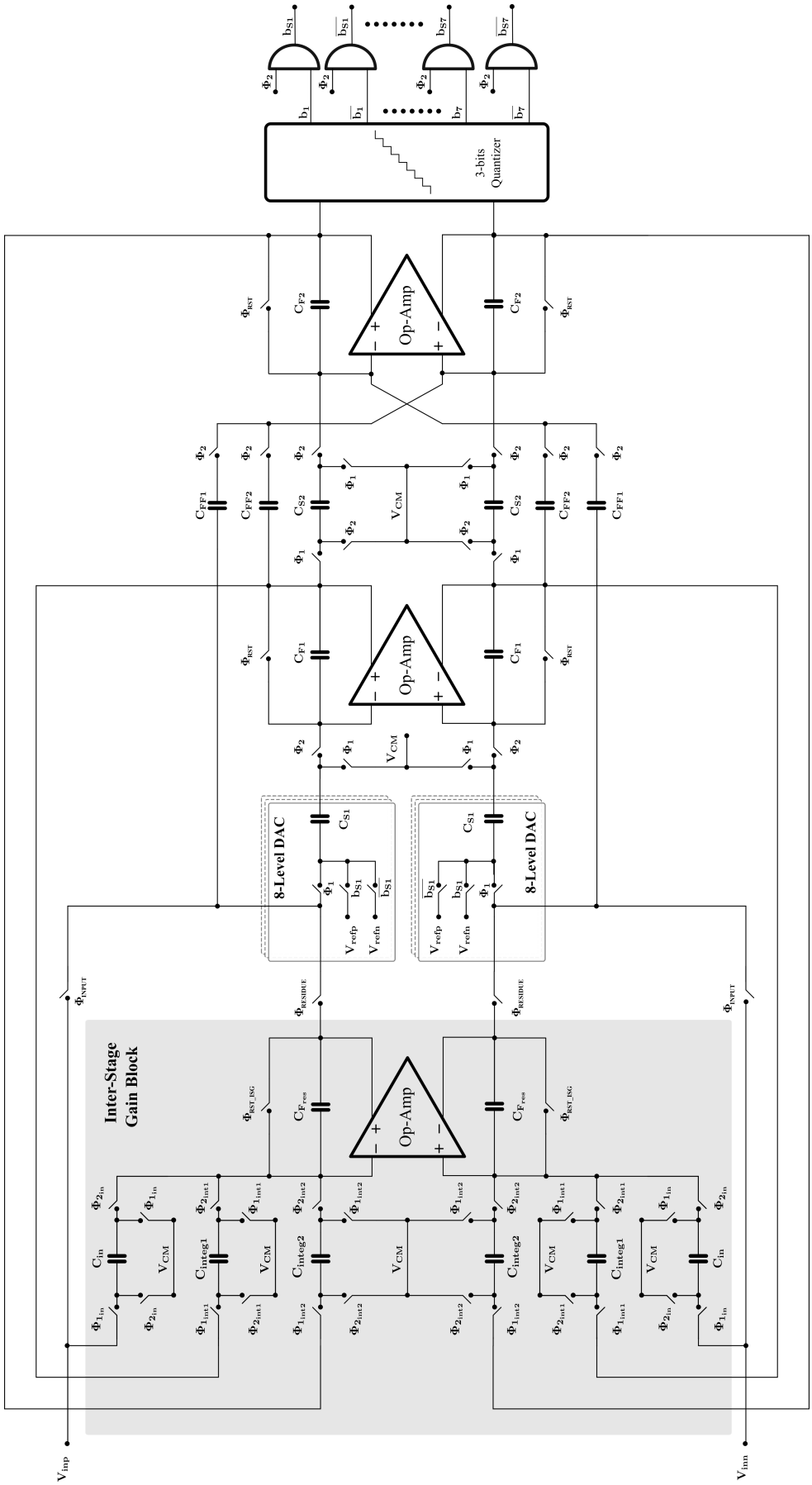


Figure 2.20: Circuit diagram of the proposed architecture of an extended-range IADC

Chapter 3

Simulink Modeling & System Verification

3.1 Introduction

Conventional sigma-delta modulators are commonly used for performing A/D conversion in several sensor read-out applications, such as automotive, consumer electronics, medical instrumentation, environmental measurements, or even live audio recording from a microphone [1]. However, these ADCs, which exhibit very high Dynamic Range (DR) thanks to oversampling and noise shaping techniques, typically feature a narrower bandwidth with respect to Nyquist rate ADCs.

Moreover, because of the memory effect inherent in sigma-delta modulation (each digital output sample somehow depends on the value of previous samples), they are not suitable for applications where single-shot events or multiple input sources with multiplexing must be evaluated. Incremental ADCs (IADCs) overcome this limitation, since they are reset at the beginning of each conversion cycle [12]. However, in IADCs high-resolution is obtained at the expense of a large number of clock cycles per conversion, preventing their use when relatively large bandwidth or short conversion time (latency) is required.

This shortcoming of IADCs can be overcome by exploiting the extended-range technique [22][23][20][19][30], which allows the resolution to be increased while maintaining the conversion time relatively short. Extended-range architectures,

however, are more susceptible than conventional IADCs to building-block non-idealities, which have then to be considered carefully. This chapter provides some insight on the effect of operational amplifier (op-amp) specifications on extended-range IADC performance, in order to allow proper choice of the design parameters.

Simulink modeling and verification of the preferred architectures is considered as crucial step in the process of the design, which enables to authenticate the feasibility of the architecture for given specifications. Therefore, a simulink model is developed for IΣΔM and residual ADC as shown in the Fig. 3.1. Developed simulink model

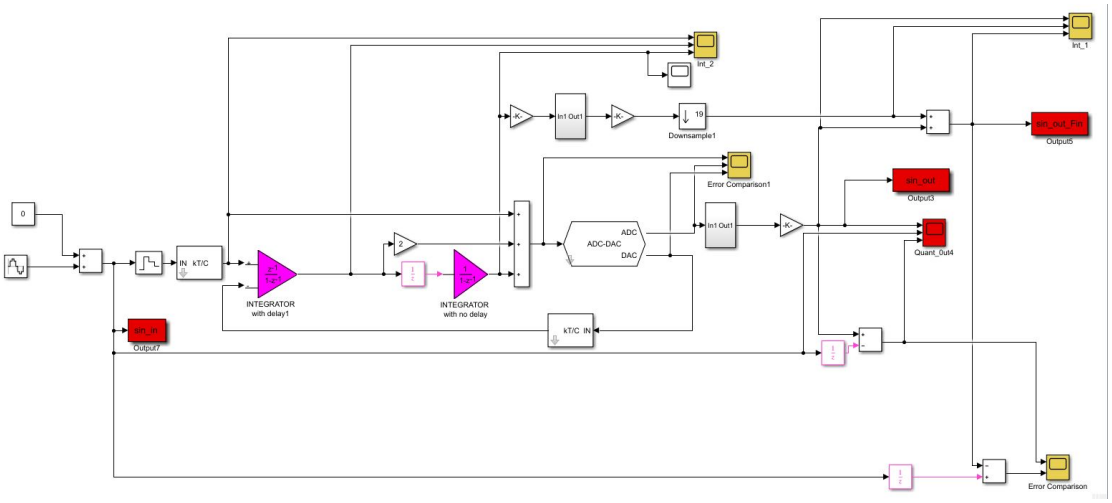


Figure 3.1: Simulink Model of Second Order Incremental Feed-forward Architecture of Sigma-Delta Modulator

architecture incorporates sample-and-hold, two delayed integrators, quantizer followed by decimation filter in the IΣΔM path, while residue signal digitization path comprised of gain block, residual quantizer and decimator as shown in the Fig. 3.1.

3.2 Block Description:

3.2.1 Integrator Block:

Integrator block has been built in order to incorporate the RESET feature to ensure the incremental function of the structure. Then a coefficient can be set with the solution of gain block. Along with this, different non-idealities of the Op-Amp needed to be consolidated, e.g. op-amp noise is included by using a block 'OpNoise' while the MATLAB functions are written to encompass other non-idealities like slew rate, loop gain and Gain-Bandwidth Product inside the 'INTEGRATOR with delay' block. The simulink model of the integrator is shown in the Fig. 3.2 For the ideal simulation, these parameters are set to, $Gain = 100\ dB$, $Slew\ Rate = 1\ V/ns$ and $GBW = 1\ GHz$ so

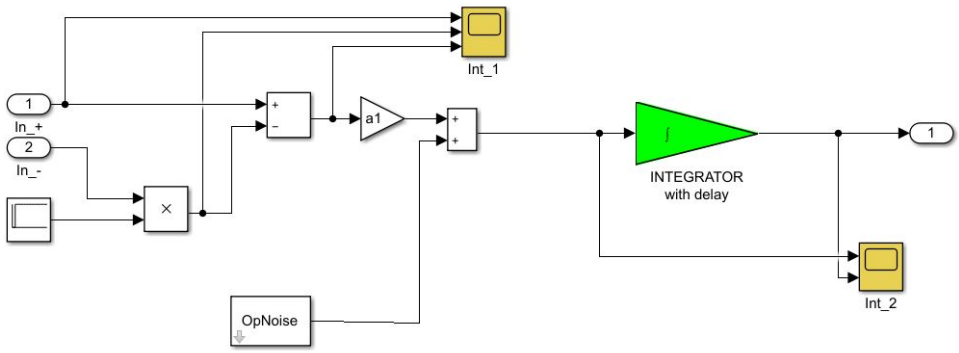


Figure 3.2: Simulink Model of the Integrators employed in the IΣΔM architecture

the integrator reflects all the ideal characteristics.

3.2.2 Quantizer:

'ADC-DAC' block from the SDtoolbox library allows to specify the number of comparators, mismatch parameter along with total capacitance to be used in the quantizer e.g. for 2 bit quantizer i.e. 4 level quantizer, the required comparators are 3, while that for 3 level quantizer are 2 and so on.

3.2.3 Decimation Filter:

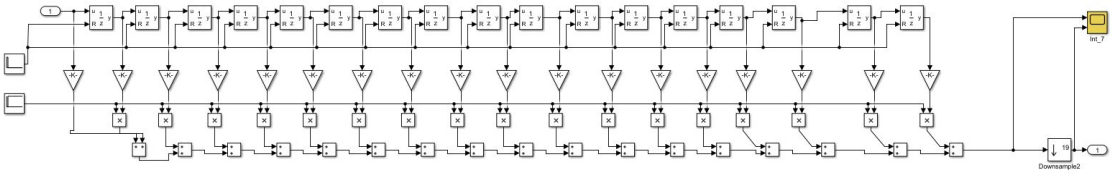


Figure 3.3: Simulink Model of the Decimation Filter

Decimation filter block is the combination of the Finite Impulse Response (FIR) filter with decimator block. The FIR filter transfer function can be expressed as,

$$H(Z) = a_0 + a_1 Z^{-1} + a_2 Z^{-2} + ... + a_{M-1} Z^{(M-1)} \tag{3.1}$$

which is implemented with M number of gain blocks, $(M-1)$ number of delay elements and $(M-1)$ number of adders as shown in Fig.3.3, where M is the over sampling ratio. The decimator block followed by FIR filter, samples the output of the filter after every M number of clock cycles.

$\mathbf{ENOB_{TOT}}$	**12**			**13**			**14**		
$\mathbf{N_{SD}}$	3	3	4	3	3	4	3	3	4
$\mathbf{ENOB_{INC}}$	12	9	10	13	9	10	14	9	10
$\mathbf{N_{RS}}$	0	3	2	0	4	3	0	5	4
M	45	18	18	64	18	18	90	18	18

Table 3.1: Parameters of the considered extended-range IADC

3.3 Analysis of Op-Amp Requirements

Different combinations of resolution in IADC with a given value of M and ERADC can fulfill a specific ENOB requirement. However, the sensitivity of each combination to the op-amp non-idealities varies, while selection of the optimum solution is necessary for robust performance. Therefore, the analysis of the op-amp specifications plays a very important role in selecting the best combination. The effects of op-amp non-idealities, such as gain and gain-bandwidth product (GBW), are, therefore, determined for an extended-range IADC with the combinations of resolution in IADC and ERADC summarized in Tab. 3.1, using a Simulink model.

A complete model of the Incremental ΣΔ Modulator with extended counting (Extended Range Incremental ΣΔ Modulator) is developed in the simulink as shown in Fig. 3.1. All the parameters of the Op-Amps are set with intention to reflect the ideal characteristics of Op-Amp and simulations are carried out. Various permutations and combinations of the resolutions of the IΣΔM and Residual ADC can be verified for given clock frequency of 80 MHz, total conversion time of 25 clock cycles to attain the ideal overall performance in terms of ENOB of 12, 13 and 14 and the other parameters considered are given in the Tab. 3.1 However the additional 12 dB margin of SNR or 2-bit of ENOB must be considered over the exact requirement of SNR or ENOB to accommodate parasitic effects and process corners degradation as a usual practice.

3.3.1 Effect of Low-Frequency Gain

The first parameter to be considered is the low-frequency gain of the op-amps used in the first and second integrator of the second-order IADC. The variation of the gain affects the integrator coefficient, as well as the location of the integrator pole. In a stand-alone IADC, the shift in the location of the pole has more significant effect than the modification of the integrator coefficient, since the integrator pole sets the zero of the IADC NTF. However, in an extended-range IADC also the variation of the integrator coefficient becomes important, since it affects the value of the residue and can cause a degradation of the overall performance after recombination. The integrator transfer

function considering finite op-amp low-frequency gain is given by [31]

$$H(Z) = \frac{C_s}{C_f}\frac{Z^{-1}}{1-\alpha Z^{-1}} \tag{3.2}$$

Parameter α is given by

$$\alpha \approx \frac{A_0 C_f}{A_0 C_f + C_s} \tag{3.3}$$

and integrator coefficient a is given by

$$\begin{aligned} a &= \frac{A_0}{1+A_0\beta} \\ &= \frac{A_0}{1+A_0\left(\frac{C_f}{C_s}\right)} \\ &= \frac{1}{\left(\frac{1}{A_0}\right)+\left(\frac{C_f}{C_s}\right)} \end{aligned} \tag{3.4}$$

where C_s is the sampling capacitance, C_f is the feedback capacitance and A_0 is the op-amp low frequency gain.

From Eq. 3.4, it is clear that, for ideal op-amp with infinite gain ($A_0 = \infty$), the integrator coefficient is simply a ratio of C_s and C_f. However, finite low-frequency gain modifies the coefficient degrading the output signal. Therefore in case of second order IADC, the residue, when passed through and processed by series of two integrators, gets corrupted. Nevertheless, since the point at which the residue is injected, is actually a point of injection of the quantization error, the change in the residue value would get high-pass filtered as quantization noise, the corrupted value should be in certain limit though. Extended-range IADC, however, rely on the accuracy of the residue signal, as it is the input to the second stage ADC. If the estimate of residue itself turns out to be inappropriate, it's digital equivalent will also get inaccurate degrading the overall response significantly. This implies that the variation of integrator coefficient has significant effect in extended-range IADC than in standalone IADC.

In case of feed-forward architecture of IADC, the output of second integrator represents the residue $e[M]$ which can be expressed as,

$$e[M]_{ideal} = a_1 a_2 \sum_{j=1}^{M}\sum_{k=1}^{j-1} u - a_1 a_2 V_{ref} \sum_{j=1}^{M}\sum_{k=1}^{j-1} v[k-1] \tag{3.5}$$

However, because of finite gain of the op-amp, the equation changes to,

$$e[M] = a_1 a_2 \sum_{j=1}^{M}\sum_{k=1}^{j-1} \alpha^{k-1} u - a_1 a_2 V_{ref} \sum_{j=1}^{M}\sum_{k=1}^{j-1} \alpha^{k-1} v[k-1]$$

$$e[M] = a_1 a_2 \left[\frac{\alpha^M - \alpha M + M - 1}{(\alpha - 1)^2}\right] u$$
$$- a_1 a_2 V_{ref} \left[\alpha^{M-2} v[M-2] + 2\alpha^{M-3} v[M-2] + ... + (M-2)\alpha v[1] + (M-1)v[0]\right] \tag{3.6}$$

$$e[M] = First\,Term - Second\,Term$$

$$First\,Term = a_1 a_2 \left[\frac{\alpha^M - \alpha M + M - 1}{(\alpha - 1)^2}\right] u$$

$$\lim_{\alpha \to 1}(First\,Term) = \lim_{\alpha \to 1} a_1 a_2 \left[\frac{\alpha^M - \alpha M + M - 1}{(\alpha - 1)^2}\right] u$$

After application of L-Hospital's Rule Two times,

$$\lim_{\alpha \to 1}(First\,Term) = \lim_{\alpha \to 1} a_1 a_2 \left[\frac{M(M-1)}{2}\alpha^{(M-2)}\right] u$$

$$First\,term\,error = First\,Term|_{\alpha=1} - First\,Term|_{\alpha}$$

$$First\,term\,error = a_1 a_2 \left[\frac{M(M-1)}{2}\right] u - a_1 a_2 \left[\frac{M(M-1)}{2}\alpha^{(M-2)}\right] u$$

$$First\,term\,error = a_1 a_2 \frac{M(M-1)}{2}\left[1 - \alpha^{(M-2)}\right] u$$

$$First\,term\,error \approx a_1 a_2 \frac{M^2}{2}\left[1 - \alpha^{(M-2)}\right] u \tag{3.7}$$

Eq. 3.7 represents the approximate error on the input signal part of the residue, due to finite low-frequency gain.

$$Second\ term = a_1 a_2 V_{ref} \left[\alpha^{M-2} v[M-2] + 2\alpha^{M-3} v[M-2] + ... \right. \\ \left. + (M-2)\alpha v[1] + (M-1)v[0]\right]$$

$$Second\ term\ error = Second\ Term|_{\alpha=1} - Second\ Term|_{\alpha}$$

$$Second\ term\ error = a_1 a_2 V_{ref} \left[(1-\alpha^{M-2}) v[M-2] + 2(1-\alpha^{M-3}) v[M-2] + ... \right. \\ \left. + (M-2)(1-\alpha)v[1]\right]$$

$$Second\ term\ error = a_1 a_2 V_{ref} \sum_{j=1}^{M} \sum_{k=1}^{j-1} \left(1-\alpha^{k-1}\right) v[k-1]$$

$$\begin{aligned} Error_{e[M]} \approx a_1 a_2 \frac{M^2}{2} \left[1-\alpha^{(M-2)}\right] u \\ - a_1 a_2 V_{ref} \sum_{j=1}^{M} \sum_{k=1}^{j-1} \left(1-\alpha^{k-1}\right) v[k-1] \end{aligned} \tag{3.8}$$

Here, the error introduced due to the Low-frequency gain of the op-amp varies sample-to-sample. However, a moderate assumption and/or approximation can be made to make the calculation simple that the residue is corrupted by $[1-\alpha^{(\frac{M-2}{2})}]$ instead, then above equation can be modified as,

$$Error_{e[M]} \approx a_1 a_2 \frac{M^2}{2} \left[1-\alpha^{\left(\frac{M}{2}-1\right)}\right] u - a_1 a_2 V_{ref} \left[1-\alpha^{\left(\frac{M}{2}-1\right)}\right] \sum_{j=1}^{M} \sum_{k=1}^{j-1} v[k-1] \tag{3.9}$$

$$Error_{e[M]} \approx \left[1-\alpha^{\left(\frac{M}{2}-1\right)}\right] \left[a_1 a_2 \frac{M^2}{2} u - a_1 a_2 V_{ref} \sum_{j=1}^{M} \sum_{k=1}^{j-1} v[k-1]\right] \tag{3.10}$$

Now the second term is actually a residue (eq.(3.5)) whose peak value is nothing but the step-size of the IADC. Then it can be expressed as,

$$e[M]_{ideal} = \left[a_1 a_2 \frac{M^2}{2} u - a_1 a_2 V_{ref} \sum_{j=1}^{M} \sum_{k=1}^{j-1} v[k-1] \right] = \frac{2}{M(M-1)} \frac{V_{ref}}{(2^{N_{SD}} - 1)}$$

$$Error_{e[M]} \approx \frac{2}{M(M-1)} \frac{V_{ref}}{(2^{N_{SD}} - 1)} \left[1 - \alpha^{\left(\frac{M}{2} - 1\right)} \right] \tag{3.11}$$

This is the peak value of the error on the residue which adds in power to the quantization noise and in turn reduces the SNR value. Assuming the distribution of this error uniform, the rms value can be given as,

$$Error_{e[M]_{rms}} \approx \frac{1}{\sqrt{3}} \frac{2}{M(M-1)} \frac{V_{ref}}{(2^{N_{SD}} - 1)} \left[1 - \alpha^{\left(\frac{M}{2} - 1\right)} \right] \tag{3.12}$$

Where, $\alpha = \left(1 - \frac{1}{A_0}\right)$,

$$Error_{e[M]_{rms}} \approx \frac{1}{\sqrt{3}} \frac{2}{M(M-1)} \frac{V_{ref}}{(2^{N_{SD}} - 1)} \left[1 - \left(1 - \frac{1}{A_0} \right)^{\left(\frac{M}{2} - 1\right)} \right] \tag{3.13}$$

Then, the Signal-to-noise Ratio accounting this error can be given as,

$$SNR = \frac{V_{sig_{rms}}^2}{Q_{eradc_{rms}}^2 + Error_{e[M]_{rms}}^2} \tag{3.14}$$

where Q_{rms} is the rms value of the quantization error of the overall architecture and V_{sigrms} is the rms value of the input signal. Ideally, the error on the residue $Error_{e[M]}$ should be zero, and in practice, it should very small compared to the overall quantization noise (i.e. Q_{eradc}) of the Extended-Range architecture, i.e.

$$Error_{e[M]_{rms}} \ll Q_{eradc_{rms}} \tag{3.15}$$

where, $Q_{eradc_{rms}}$ is given by,

$$Q_{eradc_{rms}} = \frac{1}{2\sqrt{3}} \frac{2}{M(M-1)} \frac{V_{ref}}{(2^{N_{SD}} - 1)(2^{N_{RS}} - 1)} \tag{3.16}$$

In order to validate the expression derived for $Error_{e[M]}$, a fair approach would be to plot the SNR as a function of A_0 using the equations (3.13), (3.14) and (3.16) and see how closely, the expression represents the actual simulated SNR. Fig. 3.4 sows

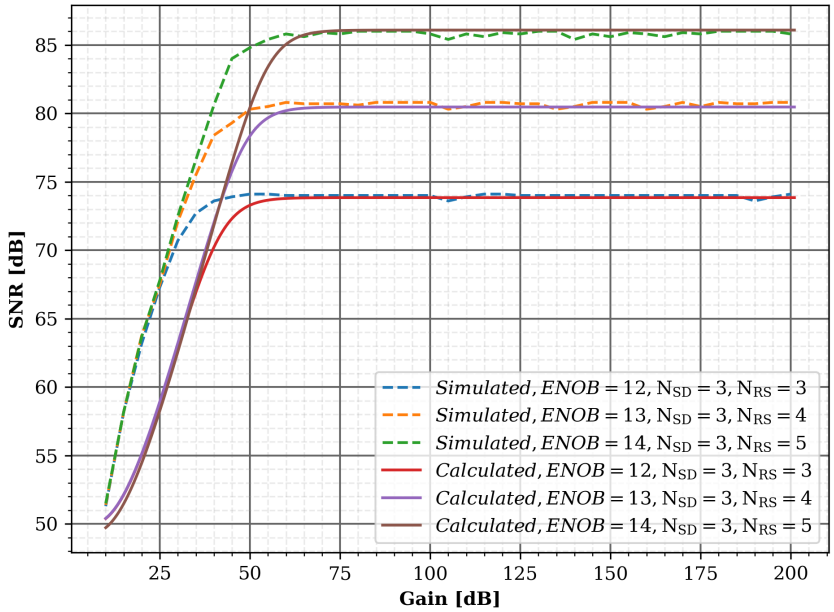


Figure 3.4: Simulated and Calculated SNR as a function of Low-frequency gain

the comparison. Various resolutions in the residual ADC (N_{RS}) are considered while keeping the resolution of the quantizer in IADC $N_{SD} = 3$, oversampling ratio $M = 18$, keeping other non-idealities to reflect the ideal behavior and varying the gain from 10 dB to 200 dB. The dotted characteristic represents simulated cases while the solid ones are plotted with the expression derived. It is clear from the plot that both the graphs are close enough within the range of nearly 1 dB at a point when simulated one just reaches it's maximum value. For example, consider a case with SNR of 86 dB or ENOB of 14. When the simulated (dotted-green) characteristic attains it's maximum value of 86 dB at a gain of 60 dB, the calculated value (solid-brown characteristic) of SNR is 85 dB. Furthermore, the value of gain at which even the expression causes SNR to reach the maximum value is 65 dB, which is higher than the simulated one (60 dB).

Further step would be to derive the expression for the Low-frequency gain of the op-amp such a that the eq.(3.15) holds. Let's assume the factor K such a that,

$$Error_{e[M]_{rms}} = \frac{Q_{eradc_{rms}}}{K} \tag{3.17}$$

where factor K is large enough so that eq.(3.15) holds. Then, putting eq.(3.13) and eq.(3.16) in eq.(3.17),

$$\frac{1}{\sqrt{3}}\frac{2}{M(M-1)}\frac{V_{ref}}{(2^{N_{SD}}-1)}\left[1-\alpha^{\left(\frac{M}{2}-1\right)}\right] = \frac{1}{2\sqrt{3}K}\frac{2}{M(M-1)}\frac{V_{ref}}{(2^{N_{SD}}-1)\,(2^{N_{RS}}-1)}$$

$$\left[1-\alpha^{\left(\frac{M}{2}-1\right)}\right]=\frac{1}{2K\left(2^{N_{RS}}-1\right)}$$

$$1-\frac{1}{2K\left(2^{N_{RS}}-1\right)}=\alpha^{\left(\frac{M}{2}-1\right)}$$

$$\alpha^{\left(\frac{M}{2}-1\right)}=1-\frac{1}{2K\left(2^{N_{RS}}-1\right)}$$

$$\alpha=\left[1-\frac{1}{2K\left(2^{N_{RS}}-1\right)}\right]^{\left(\frac{1}{\frac{M}{2}-1}\right)}$$

$$1-\frac{1}{A_0}=\left[1-\frac{1}{2K\left(2^{N_{RS}}-1\right)}\right]^{\left(\frac{2}{M-2}\right)}$$

$$1-\left[1-\frac{1}{2K\left(2^{N_{RS}}-1\right)}\right]^{\left(\frac{2}{M-2}\right)}=\frac{1}{A_0}$$

$$A_0=\frac{1}{1-\left[1-\frac{1}{2K\left(2^{N_{RS}}-1\right)}\right]^{\left(\frac{2}{M-2}\right)}}$$

$$A_0(dB)=20\log_{10}\left\{\frac{1}{1-\left[1-\frac{1}{2K\left(2^{N_{RS}}-1\right)}\right]^{\left(\frac{2}{M-2}\right)}}\right\} \tag{3.18}$$

Fig.3.5 shows the SNR Vs low-frequency gain plot for various resolutions of the RADC for different values of K. When K is 1, the error on the residue is actually half the overall quantization noise. Therefore, the Signal-to-noise ratio at that point will have a value less by 3 dB than it's maximum value (from eq(3.14)) on the calculated characteristic, however on the simulated one, it's right at the edge where it reaches it's

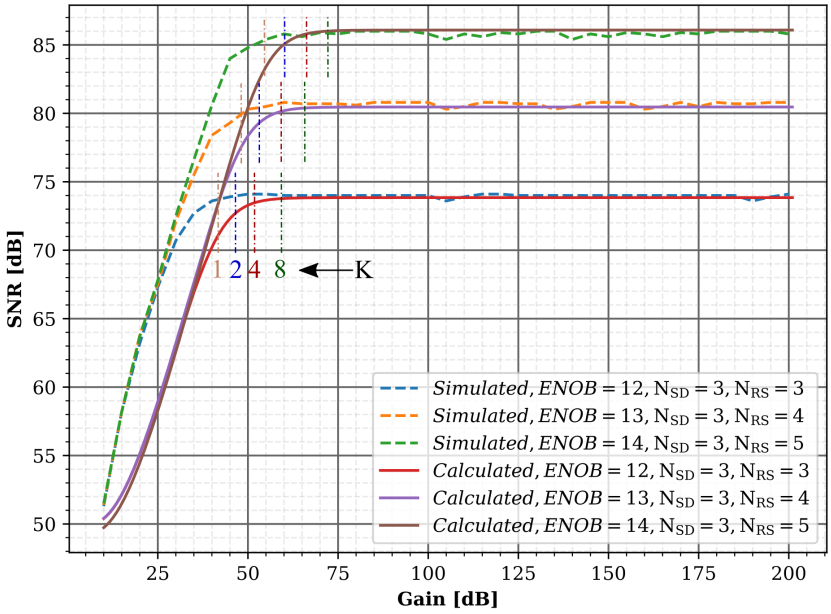


Figure 3.5: Simulated and Calculated SNR as a function of Low-frequency gain

maximum value. So, $A_{3dB_{calc}} = A_{max_{sim}}$. Nevertheless, a reasonable assumption of the factor K would be 8 where both the curves attains the maximum SNR while leaving some margin on the gain for the process corners and mismatch variation.

N_{RS}	K=1			K=2			K=4			K=8		
	Gain	SNR_{sim}	SNR_{calc}	Gain	SNR_{sim}	SNR_{calc}	Gain	SNR_{sim}	SNR_{calc}	Gain	SNR_{sim}	SNR_{calc}
3	40.7	73.5	71.2	46.87	74	72.8	52.95	74	73.5	58.89	74	74
4	47.47	80	77.6	53.56	80.5	79.5	59.61	80.9	80.1	65.65	80.9	80.8
5	53.84	85.1	82.2	59.9	85.8	85	65.93	85.7	85.5	71.96	85.8	85.8

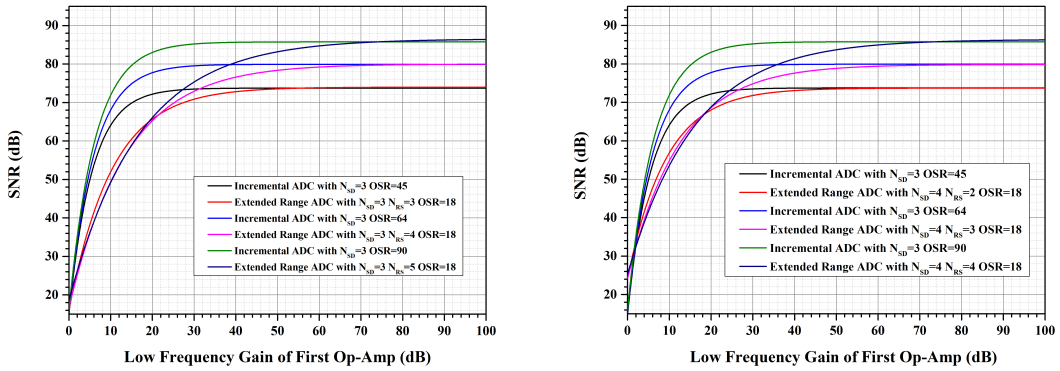
Table 3.2: Comparison between the Simulated and Calculated SNR (in dB) for different values of K as a function of Low-frequency gain in (dB)

The comparison between the simulated SNR and the SNR on the modeled characteristic at a calculated gain using eq (3.18) has been shown in the Tab. 3.2 for different values of K. For $K = 1$ the SNR on the modeled characteristic at calculated gain from eq (3.18) have the values 3 dB down the maximum SNR. Increasing K brings the calculated SNR values very close to the simulated ones while for $K = 8$ both simulated and calculated SNR values are equal. Nevertheless considering $K = 8$ for the gain calculation would be advantageous in order to account for even process variations and mismatch.

Low-Frequency Gain of the First-Integrator Op-Amp

The low-frequency gain of the first integrator op-amp in the IADC is varied from 0 dB to 100 dB considering the IADC standalone and extended-range architectures with the parameters shown in Table 3.1. In Fig. 3.6, the achieved SNR is plotted as a function of

the op-amp gain for ENOB requirement of 12, 13 and 14 bit, respectively.



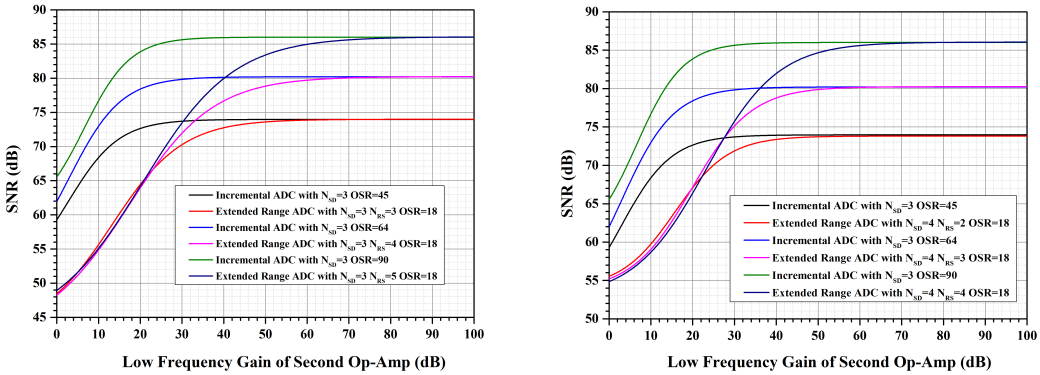
(a) (b)

Figure 3.6: Comparison of the IADC and extended-range IADC with different values of the first-integrator op-amp gain

It can be observed that for the standalone IADC, the gain requirement is low and almost equal for all the three ENOB values, while in case of extended range IADC the gain requirement is considerably higher and increases as the ENOB requirement increases. The minimum gain needed for the IADC to achieve an SNR of 86 dB is around 40 dB, while that for the extended-range IADC it is around 70 dB. Obviously the conversion time for the extended-range IADC is much shorter than for the standalone IADC (less clock cycles are required).

Low-Frequency Gain of the Second-Integrator Op-Amp

The impact of the low-frequency gain of the second-integrator op-amp on the overall performance is negligible in standalone IADCs, but it turn out to be critical for extended-range IADCs, since it affects the integrator coefficient and, hence, the residue value. Fig. 3.7 shows this effect.



(a) (b)

Figure 3.7: Comparison of the IADC and extended-range IADC with different values of the second-integrator op-amp gain

3.3.2 Effect of Finite GBW of the Op-Amps

Another major parameter which influences the ADC performance is the op-amp finite GBW. Finite GBW causes an incomplete charge transfer in the integrator at the end of each clock phase, leading to an error. A stand-alone IADC, is pretty robust against incomplete settling in the integrators. However, since the extended-range IADC performance relies on the accuracy of the residue value, which is obtained at the second integrator output, incomplete settling becomes quite detrimental for the overall ADC performance and, therefore, the op-amp GBW requirement becomes much more stringent.

In order to study the dependence of the overall Gain-Bandwidth Product (GBW) of the first Op-Amp over the SNR, all the other parameters, including the Gain, are brought back to the ideal values and GBW of the first Op-Amp is varied from 30 MHz to 300 MHz as shown in Fig. **??**(a). To achieve the maximal stable SNR, the promising value of the GBW of the first op-amp could be 250 MHz. Similar procedure is followed to observe the effect of GBW of second op-amp on the comprehensive SNR and the response is plotted as shown in the Fig.**??**(b).

In case of error due to GBW, it is equivalent of change in the integrator coefficient a by αa, then, the output of second integrator can be given as,

$$e[M] = \alpha a_1 a_2 \sum_{j=1}^{M} \sum_{k=1}^{j-1} u - \alpha a_1 a_2 V_{ref} \sum_{j=1}^{M} \sum_{k=1}^{j-1} v[k-1]$$

The error on the residue due to finite GBW can be given as,

$$Error_{e[M]} = e[M]|_{\alpha=1} - e[M]|_{\alpha}$$

$$Error_{e[M]} = (1-\alpha)\, a_1 a_2 \sum_{j=1}^{M} \sum_{k=1}^{j-1} u - (1-\alpha)\, a_1 a_2 V_{ref} \sum_{j=1}^{M} \sum_{k=1}^{j-1} v[k-1]$$

$$Error_{e[M]} = (1-\alpha) \left[a_1 a_2 \sum_{j=1}^{M} \sum_{k=1}^{j-1} u - a_1 a_2 V_{ref} \sum_{j=1}^{M} \sum_{k=1}^{j-1} v[k-1] \right]$$

$$e[M]_{ideal} = \left[a_1 a_2 \sum_{j=1}^{M} \sum_{k=1}^{j-1} u - a_1 a_2 V_{ref} \sum_{j=1}^{M} \sum_{k=1}^{j-1} v[k-1] \right] = \frac{2}{M(M-1)} \frac{V_{ref}}{(2^{N_{SD}} - 1)}$$

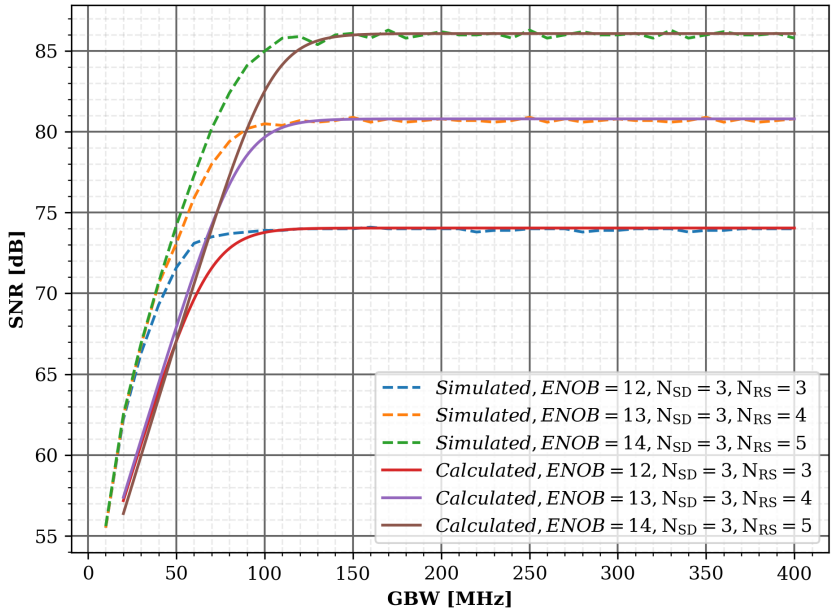


Figure 3.8: Comparison between the simulated and modeled SNR equation w.r.t. GBW

$$Error_{e[M]} = (1-\alpha)\,\frac{2}{M(M-1)}\,\frac{V_{ref}}{(2^{N_{SD}}-1)}$$

This is the peak value of the error on the residue due to finite GBW. Assuming the uniform probability distribution function for the error, it's rms value can then be given as,

$$Error_{e[M]_{rms}} = \frac{1}{\sqrt{3}}\,\frac{2}{M(M-1)}\,\frac{V_{ref}}{(2^{N_{SD}}-1)}\,(1-\alpha) \tag{3.19}$$

where $\alpha = \left(1 - e^{-\frac{t}{\tau}}\right)$ and $T = \frac{T_s}{2} = \frac{1}{2F_s}$ i.e. half the time period is allotted for the exponential change of the signal, $\tau = \frac{1}{2\pi GBW}$. Then,

$$Error_{e[M]_{rms}} = \frac{1}{\sqrt{3}}\,\frac{2}{M(M-1)}\,\frac{V_{ref}}{(2^{N_{SD}}-1)}\left[1 - \left(1 - e^{-\frac{\pi GBW}{F_s}}\right)\right] \tag{3.20}$$

$$Error_{e[M]_{rms}} = \frac{1}{\sqrt{3}}\,\frac{2}{M(M-1)}\,\frac{V_{ref}}{(2^{N_{SD}}-1)}\,e^{-\left(\frac{\pi GBW}{F_s}\right)} \tag{3.21}$$

In order to verify how closely the above equation represents the simulated curve, the graphs are plotted using the eq(3.21) by varying the GBW, along with simulated graphs as shown in fig(3.8). Three cases of ENOB of 12, 13 and 14 are considered keeping the resolution in IADC constant (3-bit) and RADC resolution of 3, 4 and 5-bit. The dotted characteristics represents simulated curves while the solid ones are plotted using eq.(3.21). Both graphs (simulated and modeled) are reasonably immediate to each

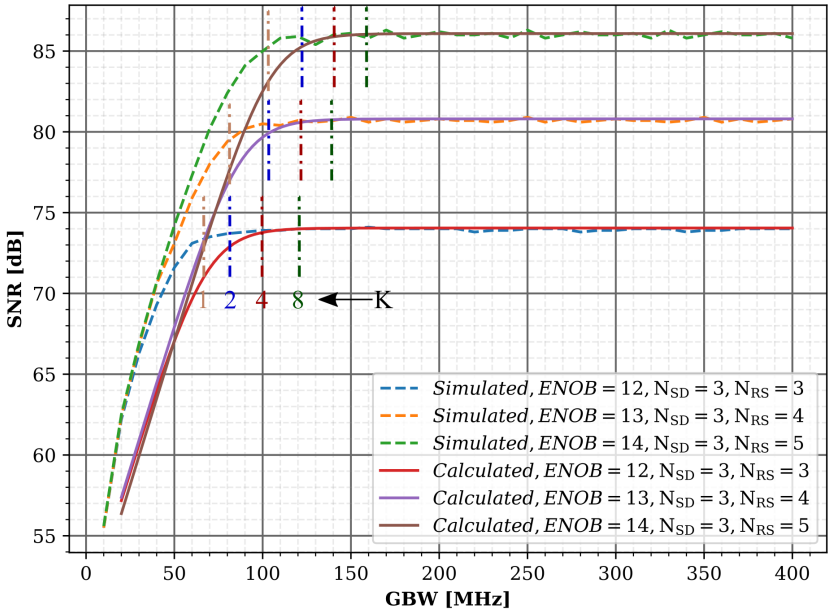


Figure 3.9: Comparison between the simulated and modeled SNR equation w.r.t. GBW

other. When the simulated characteristic reaches it's maximum, the modeled one is hardly farther by 2 dB. For example, the case with $N_{RS} = 5$, simulated (dotted green) characteristic attains it's maximum value of 86 dB at GBW of 115 dB, while modeled characteristic has an SNR value of 85 dB.

Now, as a next step, we need to find the value of GBW, such a that the error on the residue due to GBW is much smaller than the overall quantization noise of ERADC i.e. eq(3.15) holds. Then, let's assume a factor K such a that,

$$Error_{e[M]_{rms}} = \frac{Q_{eradc_{rms}}}{K}$$

Where K is large enough to hold the eq(3.15). Then, putting the values of eq(3.21) and (3.16) in the equation above,

$$\frac{1}{\sqrt{3}}\frac{2}{M(M-1)}\frac{V_{ref}}{(2^{N_{SD}}-1)}e^{-\left(\frac{\pi GBW}{F_s}\right)} = \frac{1}{2\sqrt{3}K}\frac{2}{M(M-1)}\frac{V_{ref}}{(2^{N_{SD}}-1)(2^{N_{RS}}-1)}$$

$$e^{-\left(\frac{\pi GBW}{F_s}\right)} = \frac{1}{2K\left(2^{N_{RS}}-1\right)}$$

$$e^{\left(\frac{\pi GBW}{F_s}\right)} = 2K\left(2^{N_{RS}}-1\right)$$

$$GBW = \frac{F_s}{\pi}\ln\left[2K\left(2^{N_{RS}}-1\right)\right] \tag{3.22}$$

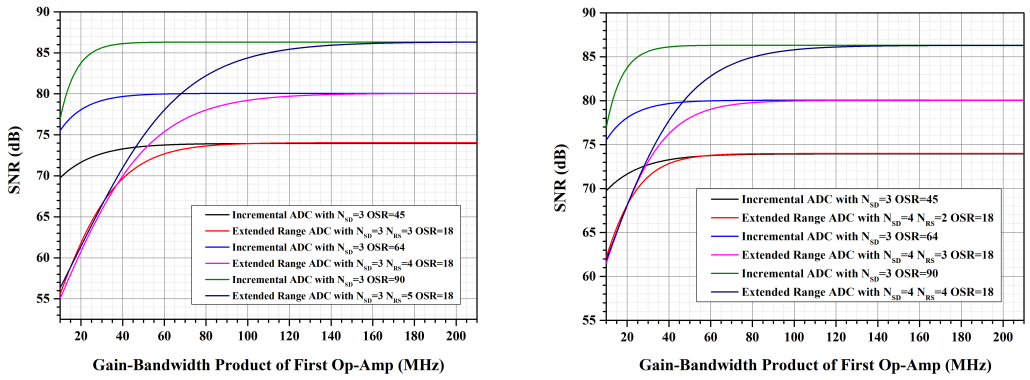
N_{RS}	K=1			K=2			K=4			K=8		
	GBW	SNR_{sim}	SNR_{calc}	GBW	SNR_{sim}	SNR_{calc}	GBW	SNR_{sim}	SNR_{calc}	GBW	SNR_{sim}	SNR_{calc}
3	67	73.5	71	85	73.9	73.1	102.5	74	74	120	74	74
4	80	79.5	77	103	80.3	79.9	122	80.8	80.8	139	80.8	80.8
5	104	85.1	83	123	85.8	85.3	140	86	86	160	86	86

Table 3.3: Comparison between the Simulated SNR and the SNR on the modeled characteristic (in dB) for different values of K as a function of calculated Finite GBW (in MHz)

Tab. 3.3 shows the comparison between the simulated SNR and the SNR on the modeled characteristic for different values of K as a function of calculated Finite GBW using eq (3.22). For $K = 1$, the value of the on the modeled characteristic is 3 dB down the maximum SNR, however, the difference w.r.t. simulated one is less than 2 dB. As K goes on increasing, the calculated values of SNR closely represents the simulated ones, furthermore $K = 4$ and $K = 8$ results in the equal values of simulated and calculated values.

GBW of the First-Integrator Op-Amp

The performance of standalone IADC and extended-range IADC as a function of the first-integrator op-amp GBW is shown in Fig. 3.10. Considering an ENOB requirement of 14 bit (SNR of 86 dB), the standalone IADC requires 60 MHz of GBW with a conversion time of 90 clock cycles, while the extended a conversion time of merely 18 clock cycles.



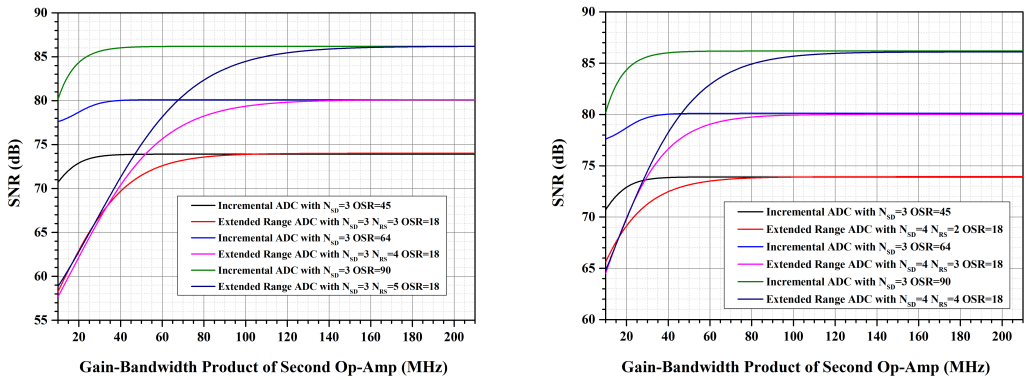
(a) (b)

Figure 3.10: Comparison of the IADC and extended-range IADC with different values of the first-integrator op-amp GBW

GBW of the Second-Integrator Op-Amp

The second-integrator op-amp GBW has negligible effect on the performance of a standalone IADC, but again it affect the overall performance of extended-range IADCs, as shown in Fig. 3.11. For an ENOB of 14 bit, the standalone IADC needs 40 MHz of

GBW, while the extended-range IADC with $N_{INC} = 9$ and $N_{RS} = 5$ requires a GBW of 160 MHz.



(a) (b)

Figure 3.11: Comparison of the IADC and extended-range IADC with different values of the second-integrator op-amp GBW

3.3.3 Performance Comparison

The results of the analysis of the effect of op-amp gain and GBW on the ADC performance are summarized in the Tab. 3.4. Basically, it turns out that, by adding extended range to an IADCs, the strong reduction of the conversion time for the same ENOB is achieved at the expense of tougher op-amp gain and GBW specifications.

$ENOB_{TOT}$	**12**			**13**			**14**		
N_{SD}	3	3	4	3	3	4	3	3	4
$ENOB_{INC}$	12	9	10	13	9	10	14	9	10
N_{RS}	0	3	2	0	4	3	0	5	4
OSR	45	18	18	64	18	18	90	18	18
Gain1 (dB)	36	58	50	38	76	70	40	80	80
Gain2 (dB)	36	58	52	38	74	60	40	80	70
GBW1 (MHz)	60	110	80	60	150	100	60	190	150
GBW2 (MHz)	40	90	80	40	130	90	40	160	130

Table 3.4: Comparison of the op-amp requirements for standalone IADC and extended-range IADC

The extended-range IADC with 3-bit quantizer and $N_{RS} = 5$ requires 18 clock cycles per conversion to achieve 86 dB of SNR (14-bit ENOB). The same ENOB can also be achieved with 4-bit quantizer and $N_{RS} = 4$ still requiring 18 clock cycles. However, it is clear that the sensitivity to op-amp non-idealities is different in the two cases. The ADC with $N_{RS} = 5$ require a gain in both op-amps of 80 dB, a GBW in first-integrator op-amp of 190 MHz and a GBW in the second-integrator op-amp of 160 MHz, while the ADC with $N_{RS} = 4$ requires more relaxed op-amp specifications (gain of 80 dB and GBW of

150 MHz, gain of 70 dB and GBW of 130 MHz in the two op-amps, respectively). This is due to the fact that a higher resolution in the ERADC requires higher accuracy in the residue value. However, the 4-bit IADC quantizer of the ADC with $N_{RS} = 4$ is twice as large and power hungry than the 3-bit quantizer of the ADC with $N_{RS} = 5$.

Chapter 4

Circuit Design

4.1 Introduction

The block specifications obtained from the Simulink model is considered as a starting point for the circuit level design in the Cadence. The core part of the architecture of the Extended-Range ADC to be implemented, as shown in Fig. 2.13, consists of two integrators, 3-bit quantizer, 3-bit DAC and Inter-Stage Gain block. While the supporting-blocks required for the complete implementation are the biasing for the op-amps in the two integrators and the ISG, timing block to generate clock phases and some control signals, the Dynamic Element Matching (DEM) block for the suppression of the harmonics due to DAC unit element mismatch and the Wallace tree encoder to convert the thermometer code to binary code which is read outside for the post-processing.

Sr. No.	Parameter	First Op-Amp	Second Op-Amp
1	Gain (dB)	50	50
2	GBW (MHz)	190	160
3	Slew Rate (V/μs)	190	160
4	Voltage Swing (V)	0.3	1.2

Table 4.1: Op-Amp specification requirements

It can be observed from Fig. 3.6 and Fig. 3.7, though the low frequency gain requirement for the case $N_{SD} = 3$ and $N_{RS} = 5$ to achieve maximum SNR of 86 dB is

around 80 dB, there is no significant degradation in SNR, if gain drops down to 50 dB. This relaxation in the gain requirement then helps to achieve the GBW value. The Table.4.1 shows the first and the second op-amp requirements for given specifications for the ADC architecture.

4.2 Integrators

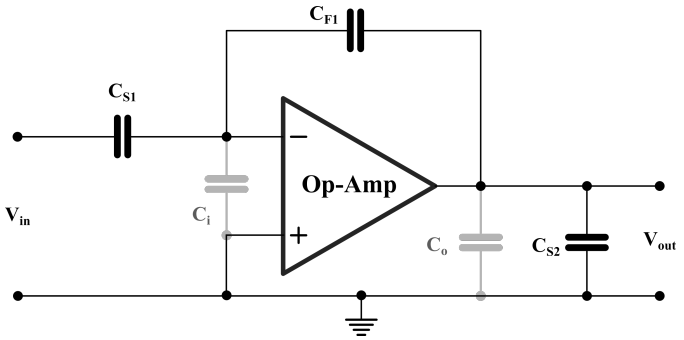


Figure 4.1: Single Ended representation of the First Integrator in the integrating phase

The choice of the architecture of the op-amps has various design constraints like power consumption, gain, GBW and slew rate, load capacitance, voltage swing etc. Two-stage op-amp is usually preferred when the gain high requirement has to be fulfilled and the power consumption is not of the concern. It also achieves high output voltage swing since at the output stage, there are just two transistors in stack. However, if along with gain the power consumption and GBW are also important, the solution could be the telescopic amplifier. Nevertheless, stack of 5 transistors between the rails in the telescopic structure limits the swing at the output. But considering the requirement, it is a good option for the op-amp in the first integrator. Swing of the signal at the output of second integrator is considerably high. Therefore, the op-amp structure or the constraints for the second integrator can be reconsidered if similar op-amp architecture has to be reused.

4.2.1 Op-Amp for the First Integrator:

In the integrating phase of the circuit of the first integrator appears like one shown in Fig. 4.1 where C_{S1} is the sampling capacitor, C_{F1} is the feedback capacitor of first integrator, C_i is the parasitic capacitor at the virtual ground node, C_o is the parasitic capacitor at the output node of the op-amp and C_{S2} is the sampling capacitor of the second integrator. The value of the sampling capacitor C_{S1} is $400\ fF$, therefore the value of the feedback capacitor is also kept $400\ fF$ for the purpose to keep coefficient of the integrator to 1.

From the setup in Fig. 4.1, the load capacitance C_L and the feedback factor β, for

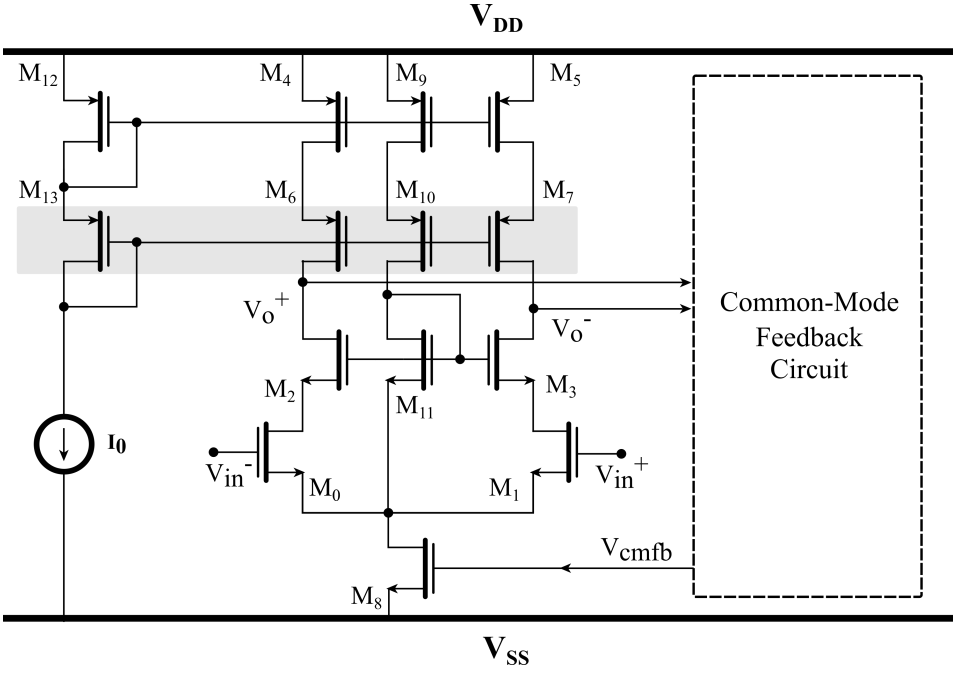


Figure 4.2: Conventional Telescopic Amplifier Circuit Diagram

the first integrator, can be estimated as,

$$C_{L1} = \frac{C_{F1}\left(C_{S1} + C_i\right)}{C_{F1} + C_{S1} + C_i} + C_o + C_{S2} \tag{4.1}$$

$$\beta_1 = \frac{C_{F1}}{C_{F1} + C_{S1} + C_i} \tag{4.2}$$

Making the use of the equations above, the load capacitance and the feedback factor turns out to be around $725\ fF$ and 0.44 respectively. Consequently, the design of the first op-amp has to be done to ensure the loop gain of $60\ dB$, loop GBW of $190\ MHz$, SR of $190\ V/\mu s$ and voltage swing of $300\ mV$ for the load of $725\ fF$ and β of 0.44.

$$Loop\ GBW = \beta_1\ GBW_{OL} = \beta_1 \frac{g_m}{2\pi C_{L1}} \tag{4.3}$$

$$Loop\ Gain = \beta_1\ A_{OL} \tag{4.4}$$

Two stage op-amps usually consumes more power compared to single stage op-amps, therefore the choice of single stage op-amp is made. But reduction in power comes with a drawback of reduced low frequency gain. Telescopic amplifier is the suitable alternative with the objective to overcome this drawback. In case of Telescopic amplifier, total five transistors are in stack from rail to rail (two transistors more compared to simple differential amplifier) which limits the output swing by two overdrives w.r.t. single stage differential amplifier as shown in Fig. 4.2. The approach to improve the output swing can be to eliminate the one transistor from the stack highlighted in conventional structure and cause to raise it by one overdrive (Fig. 4.3). However, the elimination of the transistor

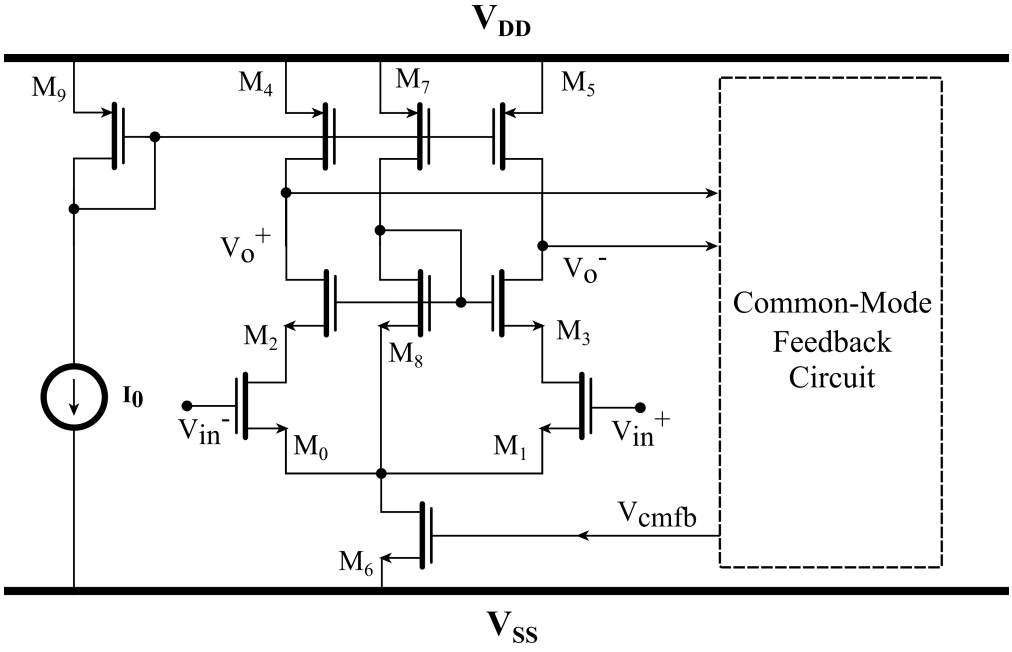


Figure 4.3: Modified Telescopic Amplifier for improved output swing

in stack leads to the lowering the gain and thus necessitates to investigate the technique to resolve this problem.

The expression for the low-frequency gain of the telescopic amplifier shown in Fig. 4.2 is given as,

$$A_0 \approx g_{m0,1}\left(g_{m2,3}r_{O2,3}r_{O0,1}||g_{m6,7}r_{O6,7}r_{O4,5}\right) \tag{4.5}$$

However, the elimination of the transistor from the stack reduces the output resistance, which in turn brings the low frequency gain, down. The expression for the low frequency gain and GBW of the modified telescopic amplifier for improved swing,

$$A_0 \approx g_{m0,1}\left(g_{m2,3}r_{O2,3}r_{O0,1}||r_{O4,5}\right) \tag{4.6}$$

$$GBW = \frac{g_{m0,1}}{2\pi C_L} \tag{4.7}$$

4.2.2 Gain and GBW Enhancement:

A technique is employed where the Auxiliary op-amp is incorporated for the purpose of gain enhancement[32] as shown in the block diagram Fig. 4.4. Auxiliary op-amp takes same inputs as the principal one and generates the signals which in turns, are used to drive the main op-amp. The power consumption of the auxiliary op-amp is significantly lower than that in the principal one.

The circuit level implementation of the architecture is as shown in the Fig. 4.5. The Auxiliary op-amp is a single stage differential amplifier with diodes as a load. The diode connected loads M_{a2} and M_{a3} in the Auxiliary op-amp are used to bias the current

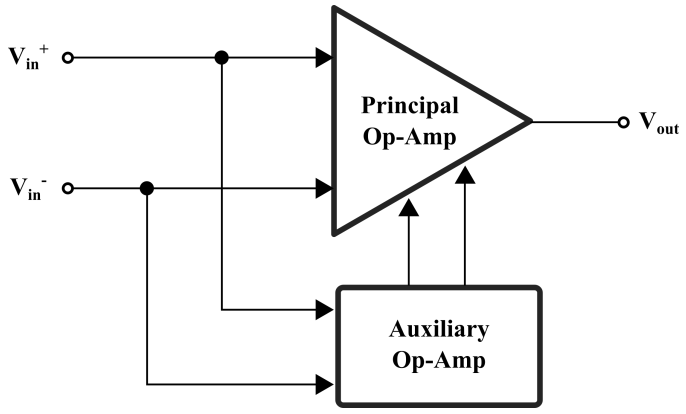


Figure 4.4: Block Diagram of Gain and GBW Enhancement

sources M_5 and M_4 in the principal op-amp respectively as shown in the Fig. 4.5. With this architecture of the amplifier, all the requirements for the first integrator are fulfilled.

The bias voltages to the current sources in modified architecture for improved swing are fixed as shown in Fig. 4.3. In case of Gain-enhanced telescopic architecture, the bias voltages v_A, v_B are generated from auxiliary op-amp and are not constant. These voltages change as the input changes and are applied to the controlled current sources. The signal voltage v_A is applied to transistor M_4 and v_B to M_5.

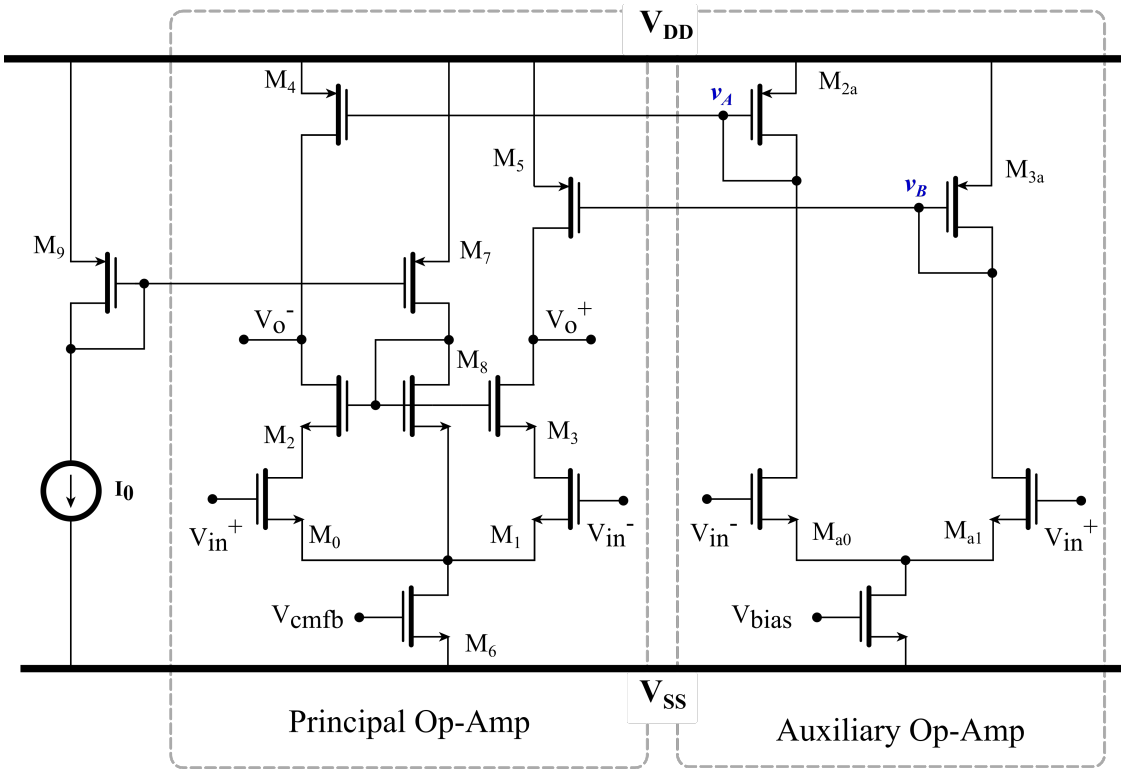


Figure 4.5: Gain enhanced Telescopic Amplifier for improved output swing with GBW boost(Common-Mode Feedback circuit not shown)

Then the expression for v_A and v_B can be given as,

$$v_A = \left(\frac{g_{ma0,a1}}{g_{ma2,a3}}\right) v_{in}^{+} \tag{4.8}$$

$$v_B = \left(\frac{g_{ma0,a1}}{g_{ma2,a3}}\right) v_{in}^{-} \tag{4.9}$$

Now, in the principal op-amp, because of the input signal v_{in}^{+} and v_{in}^{-}, the current modulation in transistor M_0 is $i_0 = g_{m0,1}v_{in}^{+}$ while that in transistor M_1 is $i_1 = g_{m0,1}v_{in}^{-}$ that flows through the output resistance, where output resistance is given by,

$$r_{out} = g_{m2,3}r_{O2,3}r_{O0,1}||r_{O4,5} \tag{4.10}$$

Furthermore, the non-constant voltages v_A and v_B also causes the further modulation in the output currents through M_4 and M_5. The expressions of these currents can be given as,

$$i_4 = g_{m4}v_A = g_{m4,5}\left(\frac{g_{ma0,a1}}{g_{ma2,a3}}\right) v_{in}^{+} \tag{4.11}$$

$$i_5 = g_{m5}v_B = g_{m4,5}\left(\frac{g_{ma0,a1}}{g_{ma2,a3}}\right) v_{in}^{-} \tag{4.12}$$

Then the output voltage of the principal op-amp is expressed as,

$$\begin{aligned} v_{out} &= v_{out}^{+} - v_{out}^{-} \\ &= (i_0 + i_4)r_{out} - (i_1 + i_5)r_{out} \\ &= \left\{\left[g_{m0,1}v_{in}^{+} + g_{m4,5}\left(\frac{g_{ma0,a1}}{g_{ma2,a3}}\right) v_{in}^{+}\right] - \left[g_{m0,1}v_{in}^{-} + g_{m4,5}\left(\frac{g_{ma0,a1}}{g_{ma2,a3}}\right) v_{in}^{-}\right]\right\} r_{out} \\ &= \left(g_{m0,1} + g_{m4,5}\frac{g_{ma0,a1}}{g_{ma2,a3}}\right) r_{out}\left(v_{in}^{+} - v_{in}^{-}\right) \end{aligned} \tag{4.13}$$

And therefore, low-frequency gain is represented as,

$$\begin{aligned} A_0 = \frac{v_{out}}{v_{in}} &= \frac{\left(v_{out}^{+} - v_{out}^{-}\right)}{\left(v_{in}^{+} - v_{in}^{-}\right)} \\ &= \left(g_{m0,1} + g_{m4,5}\frac{g_{ma0,a1}}{g_{ma2,a3}}\right) r_{out} \\ &= \left(g_{m0,1} + g_{m4,5}\frac{g_{ma0,a1}}{g_{ma2,a3}}\right) (g_{m2,3}r_{O2,3}r_{O0,1}||r_{O4,5}) \end{aligned} \tag{4.14}$$

Eq. (4.6) represents the low frequency gain of the modified telescopic amplifier for swing improvement where the transconductance of the structure is $G_m = g_{m0,1}$. While

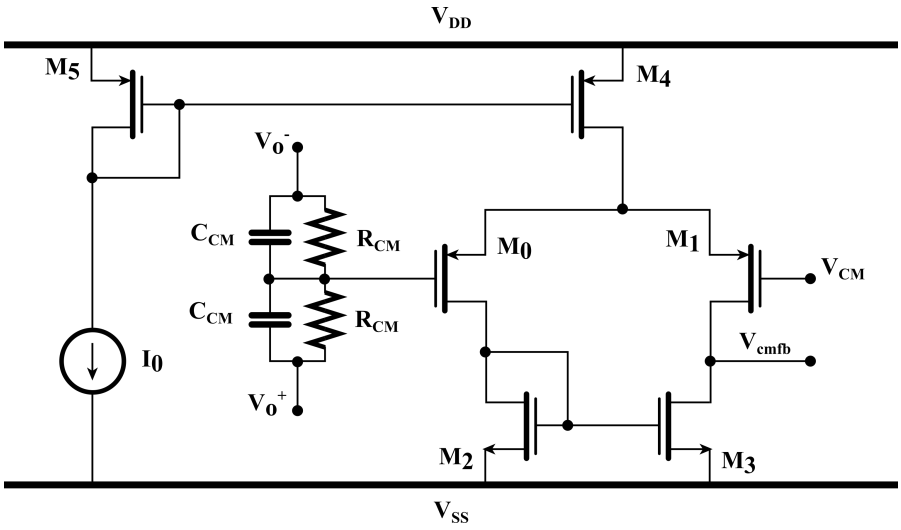


Figure 4.6: Conventional continuous time Common-Mode Feedback Circuit

that of the Gain-enhanced telescopic amplifier can be given as, from Eq.(4.14),

$$G_m = g_{m0,1} + g_{m4,5}\frac{g_{ma0,a1}}{g_{ma2,a3}} \tag{4.15}$$

It is clear from the equation above that, the scaled transconductance of transistor M_4 (M_5) is added to the $g_{m0,1}$ boosting it's gain. The GBW also gets raised as a result increase in the transconductance.

$$\begin{aligned} GBW &= \frac{\left(g_{m0,1} + g_{m4,5}\frac{g_{ma0,a1}}{g_{ma2,a3}}\right)}{2\pi C_L} \\ &= \left(1 + \frac{g_{m4,5}}{g_{m0,1}}\frac{g_{ma0,a1}}{g_{ma2,a3}}\right)\frac{g_{m0,1}}{2\pi C_L} \end{aligned} \tag{4.16}$$

The Fig.4.7 shows the schematic simulation results comparison between the architectures of the modified telescopic amplifiers without auxiliary op-amp (Fig. 4.3) and with auxiliary op-amp (Fig. 4.5). The gain characteristic and the phase characteristics are plotted as a function of frequency for the modified architecture of telescopic amplifier with and without the auxiliary op-amp.

In case of the modified architecture of telescopic amplifier for improved swing without auxiliary op-amp, the low frequency gain attained is around 43 dB, gain-bandwidth product is around 135 MHz and the phase margin is 85 ° (180-95). While, when an auxiliary op-amp is incorporated to bias the current sources of principal op-amp, the achieved low frequency gain increases to 49 dB, GBW increases to around 260 MHz with phase margin of around 67 °. For the 135 MHz of given GBW, the op-amp architecture without auxiliary op-amp consumes a current of 470 µA, while the op-amp architecture with auxiliary op-amp consumes just 500 µA of current (470 µA in

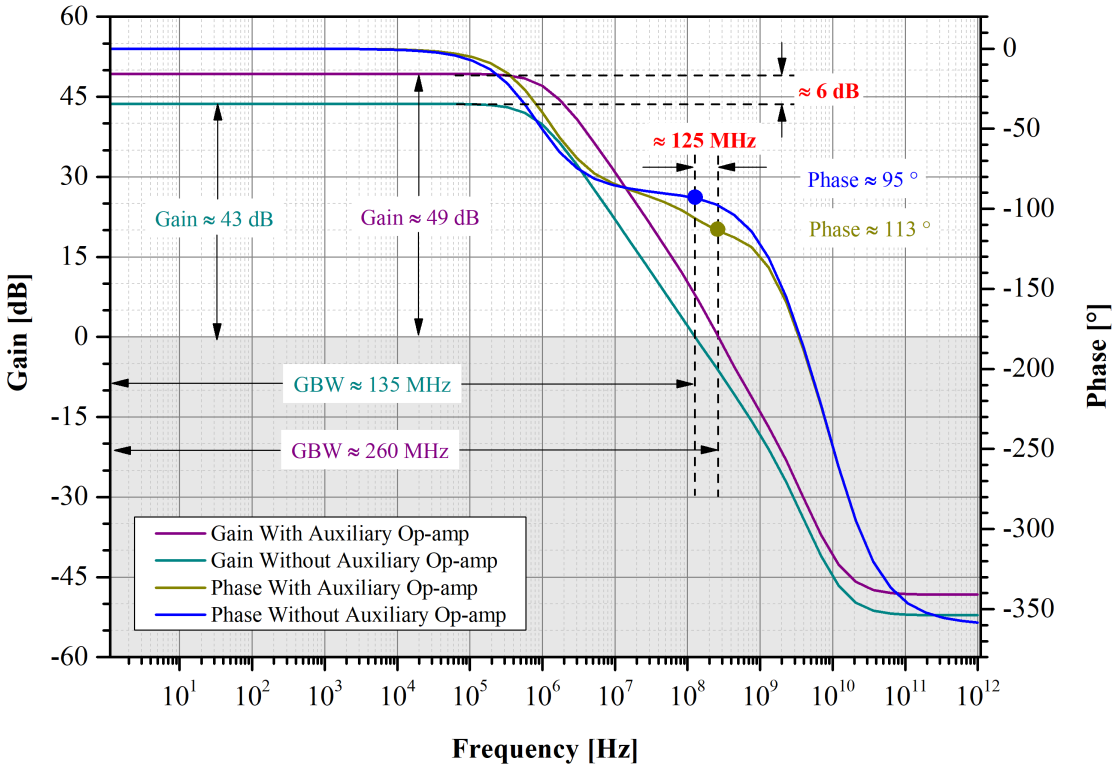


Figure 4.7: Frequency Response comparison between the modified Telescopic amplifier architectures with and without the Auxiliary op-amp for the first integrator

the principal op-amp and 30 µA in the auxiliary op-amp) boosting the gain by 6 dB and GBW by 125 MHz, i.e. there is almost 100% increase in the gain as well as GBW with just nominal amount of extra current consumption of just 6-7% (30 µA).

Next, the analysis of output voltage swing of the op-amp architecture has also been done having considered the constant voltage gain region. The low frequency gain is plotted as a function of differential output voltage swing as shown in Fig. 4.8. It is clear from the figure that the low frequency gain is around 50 dB at 0 mV differential output voltage and remains constant for output voltage from -300 mV to +300 mV exhibiting the swing of 600 mV deferentially.

4.2.3 Op-Amp for the Second Integrator:

Similar way the load for the second integrator can also be estimated in a phase where it has maximum amount of load which is again the integrating phase in this case. The second integrator in the feedforward and in the integrating phase appears as shown in Fig. 4.9. Then, from the figure, the expression for load and the feedback factor for the second integrator is pronounced in Eq. 4.17 and 4.18 respectively.

$$C_{L2} = \frac{C_{F2}\left(C_{S2} + C_{FF1} + C_{FF2} + C_i\right)}{C_{F2} + C_{S2} + C_{FF1} + C_{FF2} + C_i} + C_o \tag{4.17}$$

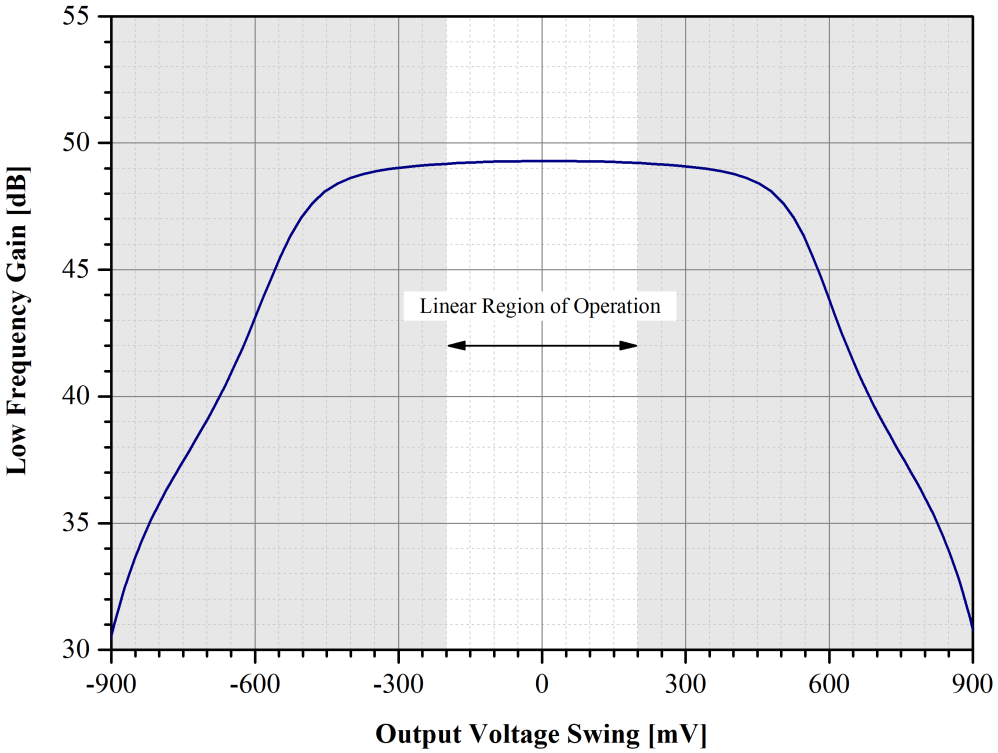


Figure 4.8: Output swing of the Op-amp Vs low frequency gain

$$\beta_2 = \frac{C_{F2}}{C_{F2} + C_{S2} + C_{FF1} + C_{FF2} + C_i} \tag{4.18}$$

However, in the architecture of Op-amp developed (Fig. 4.5), there are four transistors stacked from positive to negative rail, while the output voltage swing requirement is 1.2 V with GBW of around 200 MHz (considering PVT variations). In order to achieve such a high GBW (even with the modified structure), it is necessary to bias the transistors in the strong inversion region, and thus at higher overdrive voltage. With these restrictions, it is quite difficult to achieve the given voltage swing. Therefore, the option is to change the coefficients of the three inputs to the second integrator by

Transistor	**First Op-amp**	**Second Op-amp**	
	W (µm)	W (µm)	L (µm)
$M_{0,1}$	60	40	0.4
$M_{2,3}$	45	30	0.4
$M_{4,5}$	75	50	0.4
M_6	120	75	0.4
M_7	5	5	0.4
M_8	5	5	2.0
$M_{a0,a1}$	4	4	0.4
$M_{a2,a3}$	6	6	0.4
M_{a4}	8	8	0.4

Table 4.2: Transistor sizes in the Op-amps in the first and second integrator

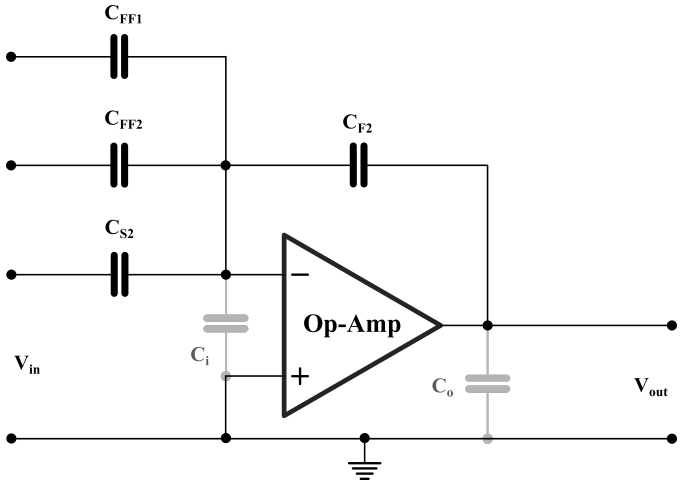


Figure 4.9: Single Ended representation of the second Integrator in the integrating phase

proper amount so as to accommodate the resulting signal within the voltage swing of the op-amp. Previously, the values of capacitors C_{FF1}, C_{F2} and C_{S2} were 400 fF and that of C_{FF2} was 800 fF setting the coefficients, $a_2 = 1$, $b_1 = 1$ and $b_2 = 2$, where $a_2 = \frac{C_{S2}}{C_{F2}}$, $b_1 = \frac{C_{FF1}}{C_{F2}}$, $b_2 = \frac{C_{FF2}}{C_{F2}}$ and as discussed, these coefficients were leading the signal swing to 1.2 V. A good scale-down coefficient could be 4 which results swing of (1.2V/4=) 300 mV and it is known that the op-amp developed for the first integrator already exhibit the same output swing, consequently which can be employed also for the op-amp in the second integrator. To do so, all the coefficients a_2, b_1 must be set to $\frac{1}{4}$ and a_2 must be set to $\frac{1}{2}$ which can simply be done by reducing the sizes of the input capacitors by 4. Then, final values of the capacitors are, $C_{FF1} = 100\ fF$, $C_{FF2} = 200\ fF$, $C_{S2} = 100\ fF$ and $C_{F2} = 400\ fF$.

Even in this case, the presumption for the parasitic capacitance at the virtual ground node (C_i) and the output node (C_o) is made to be around $100\ fF$. The overall load capacitor (C_{L2}) and the feedback factor (β_2) are computed with the help of Eq. 4.17 and Eq. 4.18 and are found to be around $300\ fF$ and 0.45 respectively. Eventually similar architecture is used for the op-amp in the second integrator as that used for op-amp in the first (Fig. 4.5) for the specifications, gain of $50\ dB$, GBW of $200\ MHz$ and SR of $200\ V/\mu s$ for estimated load and β. The expressions for loop gain and loop GBW is then expressed as,

$$Loop\ GBW = \beta_2\ GBW_{OL} = \beta_2 \frac{g_m}{2\pi C_{L2}} \tag{4.19}$$

$$Loop\ Gain = \beta_2\ A_{OL} \tag{4.20}$$

4.3 Quantizer

A quantizer block in the IADC to be employed is of the resolution of 3-bit i.e. 8 levels as extracted from the simulink simulations. Therefore the total number of comparators

needed to build a quantizer are $(2^{N_{SD}} - 1)$ i.e. 7. Each comparator has a different threshold voltage where these thresholds are generated from the switched capacitor arrangement.

4.3.1 Threshold Generator

The simplest solution to generate the thresholds of the comparator is a resistive ladder as shown in Fig.4.10. The differential threshold is the difference of the voltage generated by resistive dividers at that node, e.g. the threshold V_1 can be given as,

$$\begin{aligned} V_1 &= \frac{\left(\frac{9R}{2}\right)}{7R}\left(V_{refp} - V_{refn}\right) - \frac{\left(\frac{5R}{2}\right)}{7R}\left(V_{refp} - V_{refn}\right) \\ &= \frac{4}{14}\left(V_{refp} - V_{refn}\right) \end{aligned} \tag{4.21}$$

However, the resistors stacked between the positive and negative references tend to draw considerable amount of current, which then has to be taken into account while budgeting the power. The power consumption in the this threshold generator can be minimized by increasing the unit resistance value. But as it is known, the noise in the resistor is

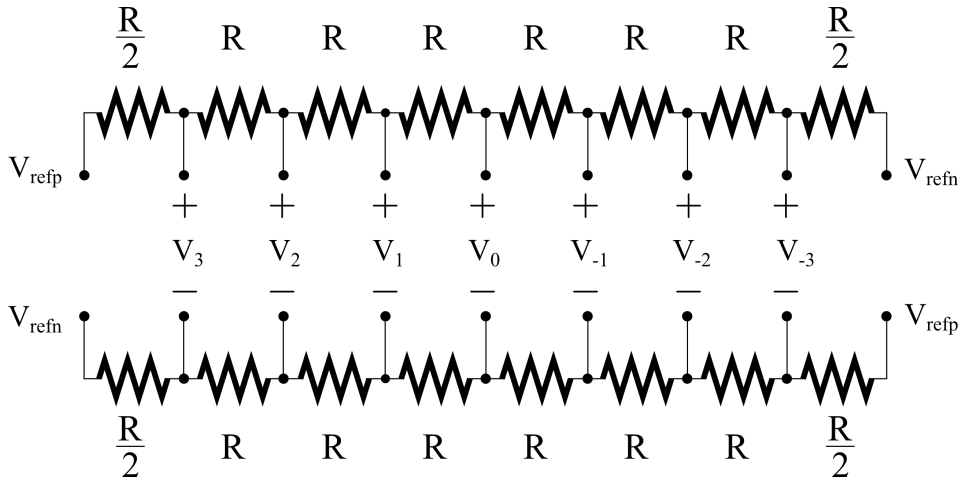


Figure 4.10: Resistive Ladder generating differential threshold voltages for comparators

proportional to it's value, i.e. $V_{noise}^2 = 4kTR$, increase in the resistance in order to save the power would end up in noisy thresholds which will then corrupt the comparator decision causing degradation in the performance.

A switched-capacitor arrangement can be employed as an option to the resistive-ladder as shown in Fig. 4.11 which saves the static power consumption. In the Fig. 4.11(a), the configuration of threshold generator is shown where the reference voltage is sampled on the capacitors with respect to the common mode voltage. Therefore, the charge stored on capacitors C_{P_U}, C_{N_U}, C_{P_L} and C_{N_L} are, (C_{P_U}=C_{P_L}=C_P,

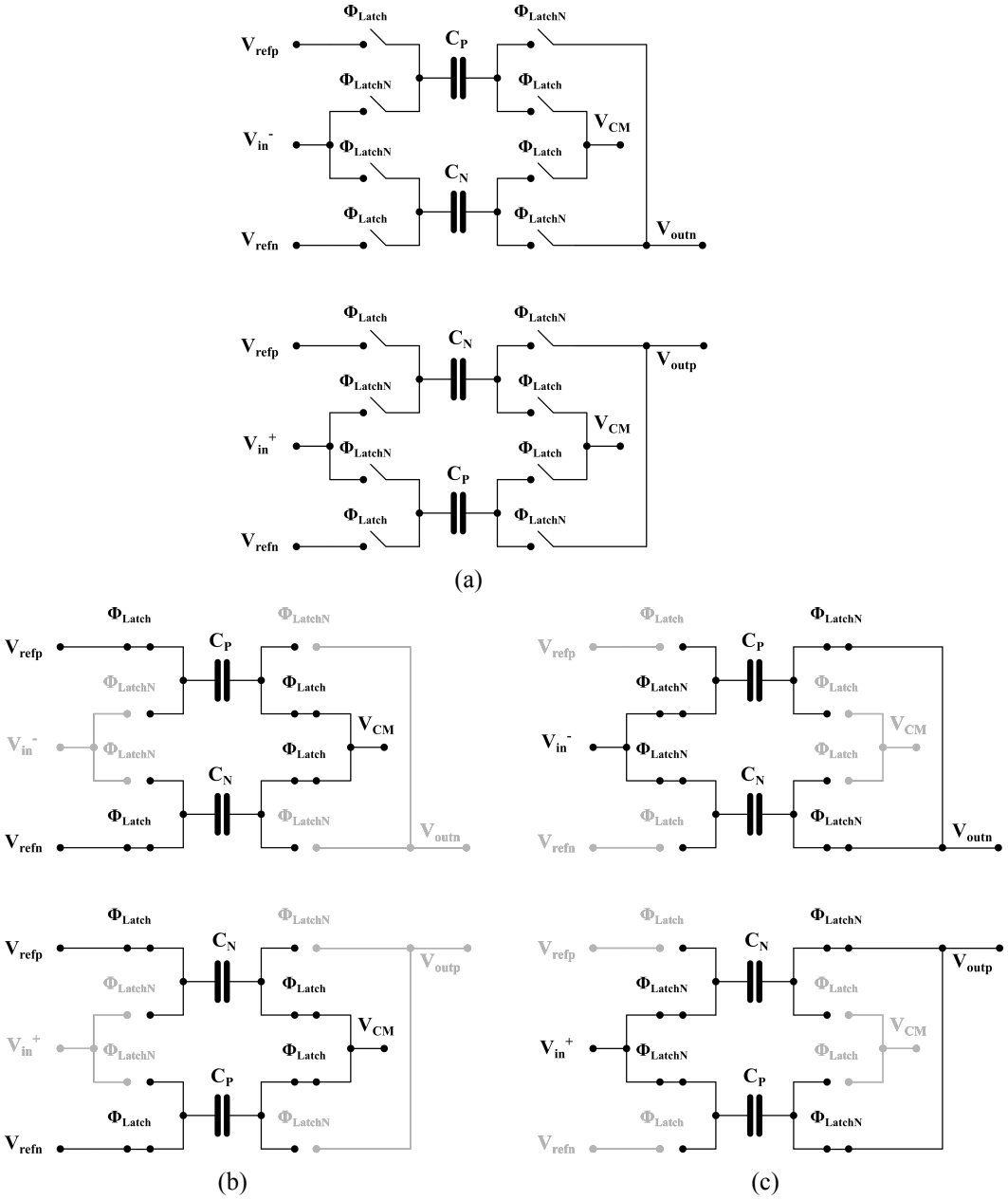


Figure 4.11: (a)Switched capacitor arrangement to generate threshold and taking difference with input sample (b)Threshold generator in a phase sampling reference voltage (c)Threshold generator in a phase sampling signal voltage

C_{N_U}=C_{N_L}=C_N)

$$\begin{aligned} Q_{CP_U} &= C_{P_U} V_{refp} = C_P V_{refp} \\ Q_{CN_U} &= C_{N_U} V_{refn} = C_N V_{refn} \\ Q_{CP_L} &= C_{P_L} V_{refn} = C_P V_{refn} \\ Q_{CN_L} &= C_{N_L} V_{refp} = C_N V_{refp} \end{aligned} \tag{4.22}$$

In the next phase where the input signal is sampled, the capacitors C_{P_U} and C_{N_U} are in parallel which makes it $C_U = C_{P_U} + C_{N_U}$. Similarly, C_{P_L} and C_{N_L} parallel combination

exhibit the total equivalent capacitance of $C_L = C_{P_L} + C_{N_L}$. Then the charge and voltage across the capacitors C_U and C_L can be given by,

$$\begin{aligned} Q_{CU} &= Q_{CP_U} + Q_{CN_U} \\ (C_P + C_N)V_{CU} &= C_P V_{refp} + C_N V_{refn} \end{aligned} \tag{4.23}$$

$$V_{CU} = \frac{C_P V_{refp} + C_N V_{refn}}{C_P + C_N} \tag{4.24}$$

similarly,

$$V_{CL} = \frac{C_P V_{refn} + C_N V_{refp}}{C_P + C_N} \tag{4.25}$$

Then the voltage difference of V_{outp} and V_{outn} can be expressed as,

$$\begin{aligned} V_{out} &= V_{outp} - V_{outn} \\ &= (V_{in}^- - V_{CU}) - (V_{in}^+ - V_{CL}) \\ &= \left(V_{in}^- - \frac{C_P V_{refp} + C_N V_{refn}}{C_P + C_N}\right) - \left(V_{in}^+ - \frac{C_P V_{refn} + C_N V_{refp}}{C_P + C_N}\right) \\ &= \left(V_{in}^+ - V_{in}^-\right) - \frac{C_P - C_N}{C_P + C_N}\left(V_{refp} - V_{refn}\right) \\ &= V_{in} - V_{thr} \end{aligned} \tag{4.26}$$

where the threshold voltage generated by the switched capacitor is,

$$V_{thr} = \frac{C_P - C_N}{C_P + C_N}\left(V_{refp} - V_{refn}\right) \tag{4.27}$$

and, $V_{ref} = V_{refp} - V_{refn}$.

For multi-bit quantizer, the different values of C_P and C_N generates the different values of the threshold voltages while the total capacitance $C_P + C_N$ is equal. The following table shows the different values of the threshold voltages created by the switched-capacitor block shown in Fig. 4.11, for 3-bit quantizer.

$\mathbf{C_P}$	$\mathbf{C_N}$	$\mathbf{V_{thr}}$ (Volts)
350 fF	50 fF	$(3/4)V_{ref}$
300 fF	100 fF	$(2/4)V_{ref}$
250 fF	150 fF	$(1/4)V_{ref}$
200 fF	200 fF	$(0/4)V_{ref}$
150 fF	250 fF	$-(1/4)V_{ref}$
100 fF	300 fF	$-(2/4)V_{ref}$
50 fF	350 fF	$-(3/4)V_{ref}$

Table 4.3: The threshold voltages generated for 3-bit quantizer

However, since the signal swing at the output of second integrator is reduced 4 times,

which is the input to the quantizer, the signal do not cover full range of the quantizer but just $1/4^{th}$ part of the full-scale. This will result in the decreased SQNR as a consequence. In order for input signal to quantizer to cover the full-scale, now, solution is to scale the quantizer thresholds down by equal amount as the signal, i.e. by a factor of 4. The ratios of the capacitors in the threshold generator has to be modified as follows considering the unit capacitance of $C_{unit} = 12.5\ fF$ which still accounts the total capacitance $C_P + C_N = 400\ fF$

C_P	C_N	V_{thr}
$19C_{unit}$ = 237.5 fF	$13C_{unit}$ = 162.5 fF	$(3/16)V_{ref}$
$18C_{unit}$ = 225 fF	$14C_{unit}$ = 175 fF	$(2/16)V_{ref}$
$17C_{unit}$ = 212.5 fF	$15C_{unit}$ = 187.5 fF	$(1/16)V_{ref}$
$16C_{unit}$ = 200 fF	$16C_{unit}$ = 200 fF	$(0/16)V_{ref}$
$15C_{unit}$ = 187.5 fF	$17C_{unit}$ = 212.5 fF	$-(1/16)V_{ref}$
$14C_{unit}$ = 175 fF	$18C_{unit}$ = 225 fF	$-(2/16)V_{ref}$
$13C_{unit}$ = 162.5 fF	$19C_{unit}$ = 237.5 fF	$-(3/16)V_{ref}$

Table 4.4: Modified threshold voltages, generated for 3-bit quantizer accommodating the signal to full scale.

4.3.2 Comparator

The architecture of the comparator used in the quantizer is as shown in the Fig. 4.12 which is designed to work with a clock frequency of $80\ MHz$. The driving transistors pair M_0 and M_1, constitutes a preamplifier. It amplifies the signal prior to the comparison and transmits it to the back-to-back connected NOT gate. This is a positive feedback

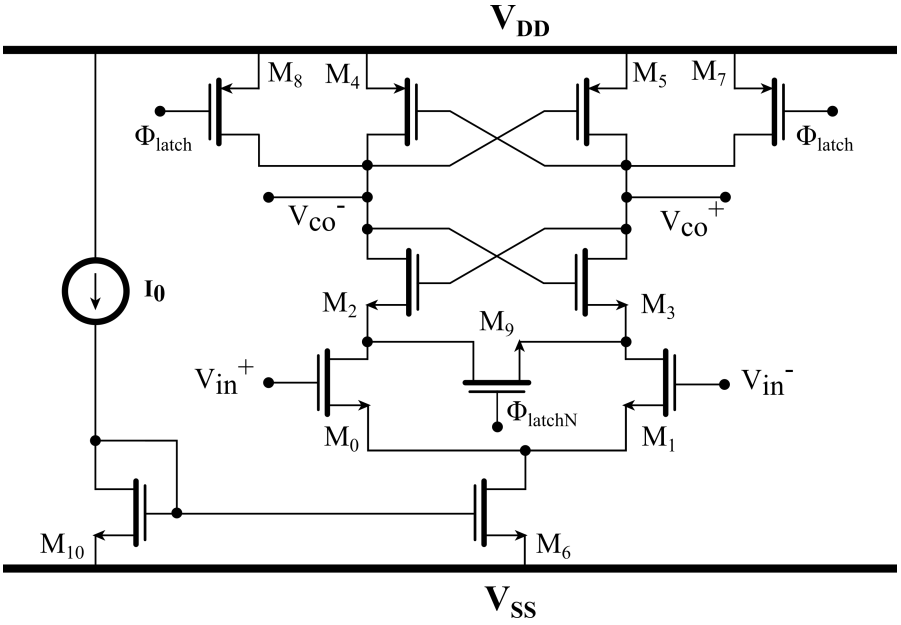


Figure 4.12: Schematic of the Comparator employed in the Quantizer

circuit which pulls up or down the output node (V_{CO}^{+} and V_{CO}^{-}) voltage depending on the signal transferred from the preamplifier and takes the decision. These comparison signals can then be stored in the latch comprised of NAND gates and then are passed through the buffers to make the signals strong enough to drive the given load as shown in the Fig. 4.13. The capacitive divider is used to generate the threshold, specific for a comparator

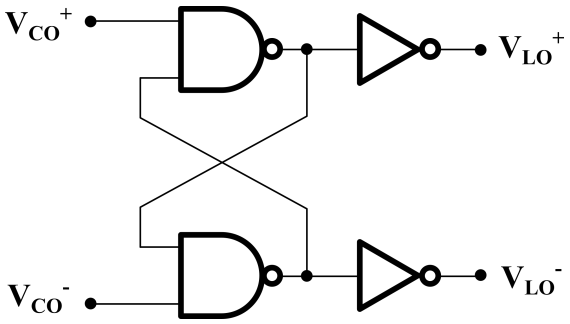


Figure 4.13: Latch Comprised of NAND gates and digital buffers

and it's value depends on the ratio of the capacitors, can be expressed as in the Eq. 4.27. The simulation results of the comparator in Fig. 4.13 are shown in the Fig. 4.14. In

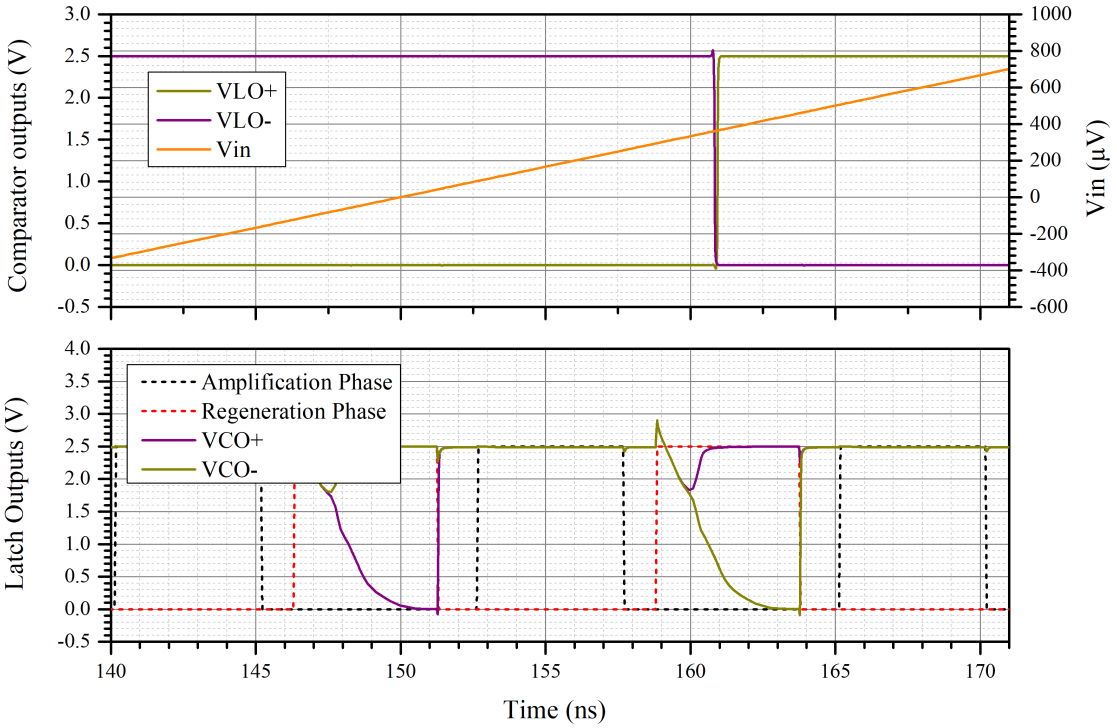


Figure 4.14: Signals at the different nodes of the Comparator

the simulation set-up the negative terminal of the comparator (V_{in}^{-}) is kept constant at the common-mode voltage ($V_{CM} = 1.25\ V$) while the positive terminal (V_{in}^{+}) is linearly varied from ($V_{CM} - 10\ mV$) to ($V_{CM} + 10\ mV$), while the comparator is clocked at the frequency of 80 MHz. The characteristic in orange in the top plot shows the differential input voltage ($V_{in}^{+} - V_{in}^{-}$) in the time frame from $140\ ns$ to $171\ ns$ which covers two

amplification phases and two regeneration phases. In the first amplification phase, from time $140\ ns$ to $145\ ns$, the differential input voltage is around $-300\ \mu V$. Therefore in the regeneration from $146\ ns$ to $151\ ns$, higher potential on the negative input causes to draw the more current through transistor M_1 than that through M_0. The rate at which the positive output node (V_{CO}^{+}) is discharging is higher than that the negative node ($V_{CO}-$) discharge rate. In turn, the node $V_{CO}+$ reaches the potential of $V_{DD} - V_{thp}$ first, which is connected to the gate of the transistor M_4 turning it on thereby connecting the V_{DD} to the negative output V_{CO}^{-}. This output is connected to the gate of NMOS transistor M_3 causing it to turn on and the gate of PMOS transistor M_5 turning it off which discharges the node to ground very fast. These outputs from comparator are then provided to the SR latch which stores the decision with outputs V_{LO}^{+} and V_{LO}^{+} as shown in the top plot of Fig. 4.14.

In the next amplification phase, the differential input is positive and is around $200\ \mu V$. Therefore exactly counter-operation in the comparator will take place in regeneration phase pulling the V_{CO}^{-} to ground and pushing V_{CO}^{+} node to V_{DD} as shown in the bottom plot of the Fig. 4.14.

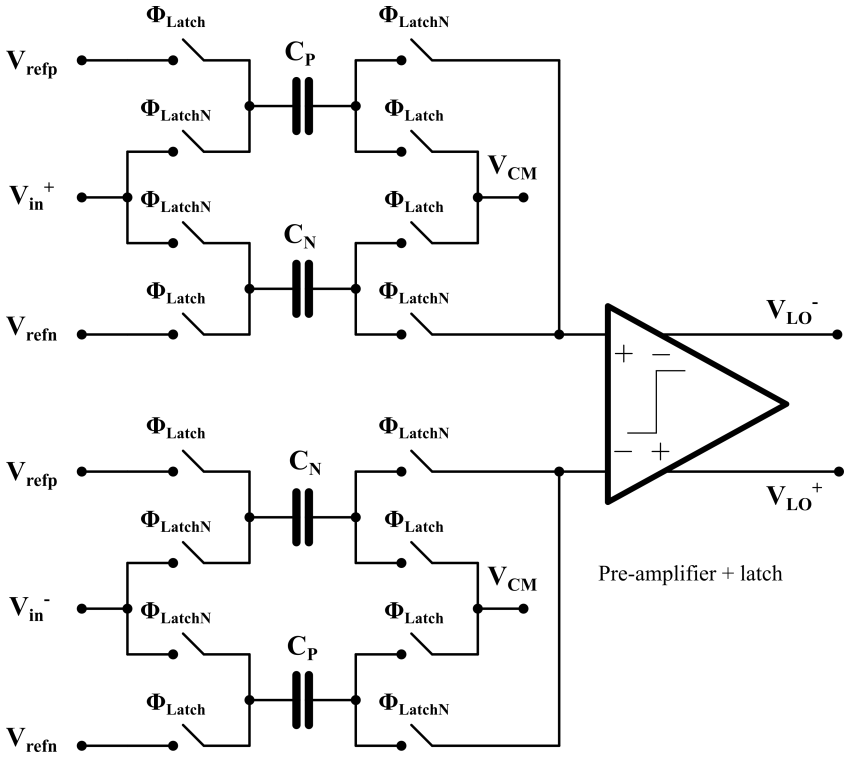


Figure 4.15: A complete structure of Comparator

A complete structure of the comparator is shown in Fig. 4.15 which consists of a switched-capacitor threshold generator and the next block is pre-amplifier and the back-to-back connected NOT for amplification and regeneration. This is the one slice of the whole quantizer. In case of 3-bit quantizer, there will be such a 7 slices with different values of C_P and C_N generating 7 different thresholds as shown in Tab. 4.4.

4.4 DAC Architecture

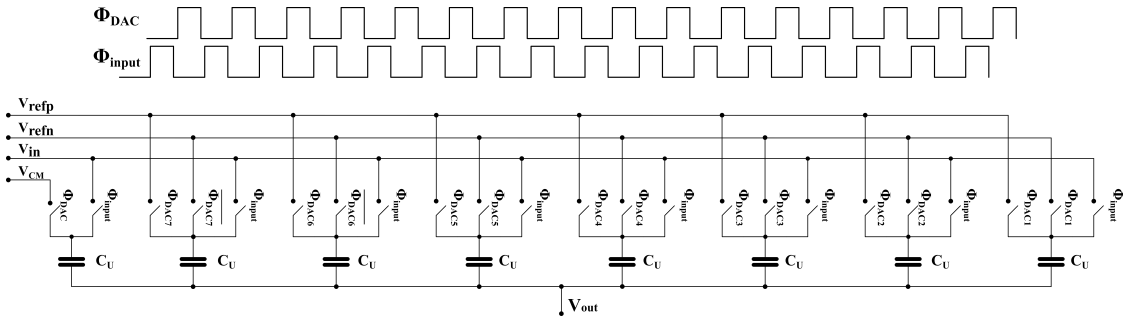


Figure 4.16: A 3-bit Thermometric Capacitive DAC at the input of First integrator

Since, the quantizer implemented in the IADC is of the resolution of 3-bit, the architecture of the DAC employed needs to be of the same resolution. Therefore the capacitive DAC with thermometric inputs is realized as shown in the Fig. 4.16. In the phase Φ_{input}, the input signal is sampled on the array of unit capacitors comprising the sampling capacitor while in the phase Φ_{DACn}, the feedback signal from the quantizer is sampled and thus a difference between input signal and the digital equivalent of the input signal i.e. residue is integrated. Here, $\Phi_{DACn} = \Phi_{DAC} * b_n$ and $\overline{\Phi_{DACn}} = \Phi_{DAC} * \overline{b_n}$ where b_n and $\overline{b_n}$ are the n^{th} thermometric output and it's complement from the quantizer and the Φ_{DAC} is the phase when feedback DAC signal should be applied.

4.5 Inter-Stage Gain Block

The circuit diagram of the Inter-stage Gain block is shown in Fig. 4.17. Since the architecture employed is the modified architecture of the Incremental ADC, the output of the second integrator contains not only the residue but the components proportional to the input signal as well as the output of the first integrator.

$$y[M] = a_1u[M]+a_2w[M]+a_1a_2\frac{M(M-1)}{2}u-a_1a_2V_{ref}\left(v[M-2]+.....+(M-1)v[0]\right)$$

Where the integrator coefficients $a_1 = 1$ and $a_2 = 1$ and the feed-forward coefficients $b_1 = 1$ and $b_2 = 2$.

Therefore the ISG block has to first extract the residue by subtracting the input signal and the output of the first integrator from the second integrator's output with proper coefficients and then amplify the residue so as to cover the full-scale of the residual ADC (RADC), i.e.

$$e[M] = y[M] - b_1u[M] - b_2w[M] \tag{4.28}$$

$$ISG\ output = Ge[M] = Gy[M] - Gb_1u[M] - Gb_2w[M] \tag{4.29}$$

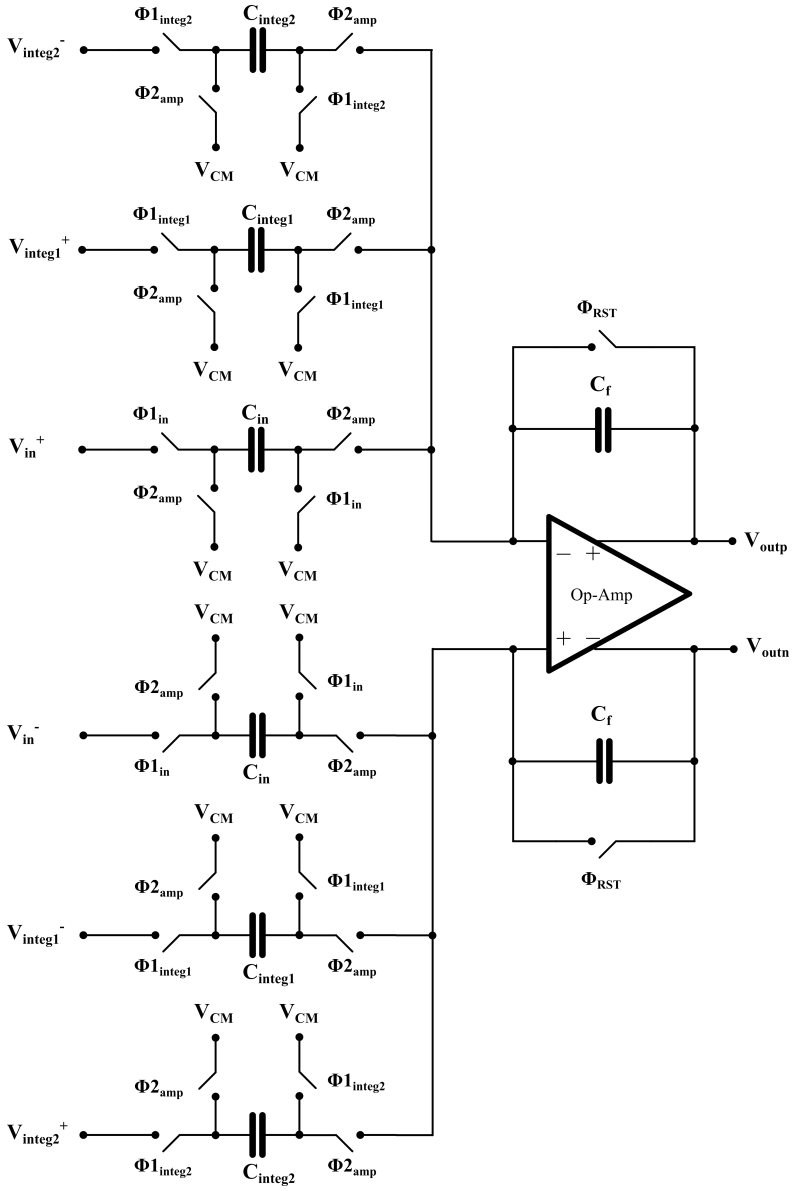


Figure 4.17: Inter-Stage Gain Block Diagram

Then, the coefficients $b_1 = 1$ and $b_2 = 2$ are set by the IADC part while the ISG gain G must be set to $2^{N_{SD}-1}$, i.e. 4, so that the amplified residue covers full-scale of RADC. Then the final coefficients of the input signal $u[M]$, output of first integrator $w[M]$ and the output of second integrator $y[M]$ for the extraction and amplification of residue are constructed by the ratio of the sampling capacitor and the feedback capacitors i.e.

$$\begin{aligned} Coeff.\ of\ y[M] &= \frac{C_{integ2}}{C_F} = 4 \\ b_1 &= \frac{C_{input}}{C_F} = 4 \\ b_2 &= \frac{C_{integ1}}{C_F} = 8 \end{aligned} \tag{4.30}$$

However, it should be noted that, the second integrator's output is already reduced by

factor of 4 in order to satisfy the swing of the op-amp. Therefore the signals $y[M]$, $u[M]$ and $w[M]$ are smaller by factor of 4. Thus, if the residue has to be amplify to the RADC full-scale (1.2V), the additional amplification factor must be incorporated in inter-stage gain G, i.e. overall gain factor will be 16 and the swing will be then 1.2V.

Nevertheless, it has been seen that achieving such a high voltage swing for given low frequency gain of 50 dB and GBW of 200 MHz is quite difficult. Hence, the ISG gain is set to 4 instead, which brings the residue swing down. Then the capacitance ratios are as shown in the Eq.(4.30)

Note that the residue swing is now $1/4^{th}$ of the reference voltage. It means the overall ERADC signal-to-quantization noise ratio will go down by 12 dB.

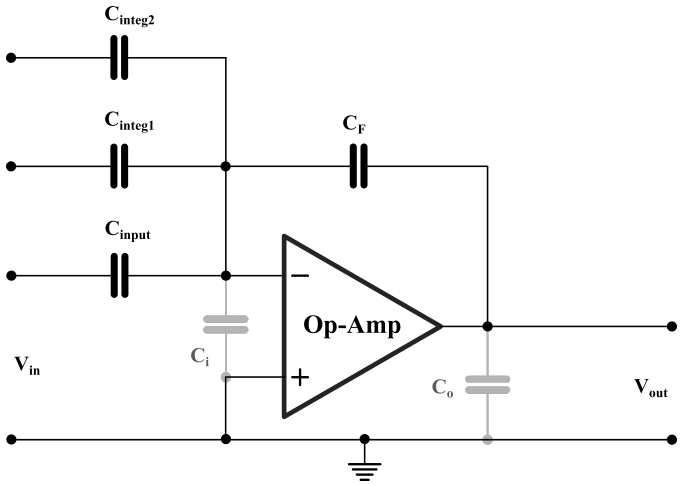


Figure 4.18: Single ended representation of the Inter-stage Gain Block in the amplification phase

After considering the parasitic capacitance at virtual ground and the output node, the configuration of ISG in the integrating phase looks like as shown in Fig. 4.18. Then the total load capacitance and the beta factor can be calculated as,

$$C_{L_{ISG}} = \frac{C_F(C_{input} + C_{integ1} + C_{integ2} + C_i)}{C_F + C_{input} + C_{integ1} + C_{integ2} + C_i} + C_o \tag{4.31}$$

$$\beta_{ISG} = \frac{C_F}{C_F + C_{input} + C_{integ1} + C_{integ2} + C_i} \tag{4.32}$$

The values of the capacitances are $C_{input} = C_{integ2} = 400fF$, $C_{integ1} = 800fF$ while $C_F = 100fF$. The parasitics considered prior to the design $C_i = 100f$ and $C_o = 100f$, which results in the total load capacitance of around $200fF$ and the feedback factor $\beta = \frac{1}{18}$. However, the op-amp requirements are quite similar to that in the first integrator. Therefore, the similar architecture is employed for the amplifier also in the ISG for the specifications of low-frequency loop gain = 60 dB, and the GBW = 200 MHz for given load and the feedback factor.

4.6 Supporting Blocks

The two integrators, multi-bit quantizer, feedback DAC and the inter-stage gain block are the core blocks of the ERADC architecture where the functionality of the structure can be verified. However, few more blocks are needed to incorporate along with core blocks such as biasing block which is used to bias the op-amps in the integrators and the inter-stage gain block as well as the comparators in the quantizer, the timing block to generate various phases such as Φ_1, Φ_2 etc and some spacial signals such as End-of-Conversion (Φ_{EOC}), reset integrators (Φ_{RST}), the Dynamic Element Matching (DEM) to improve the linearity of the feedback DAC etc.

4.6.1 Biasing

There are op-amps in the two integrators and the ISG block and the comparators in the quantizer which need the biasing current of $10\ \mu A$. Therefore a biasing circuit is developed as shown in Fig. 4.19 which does the job. It needs an external biasing current

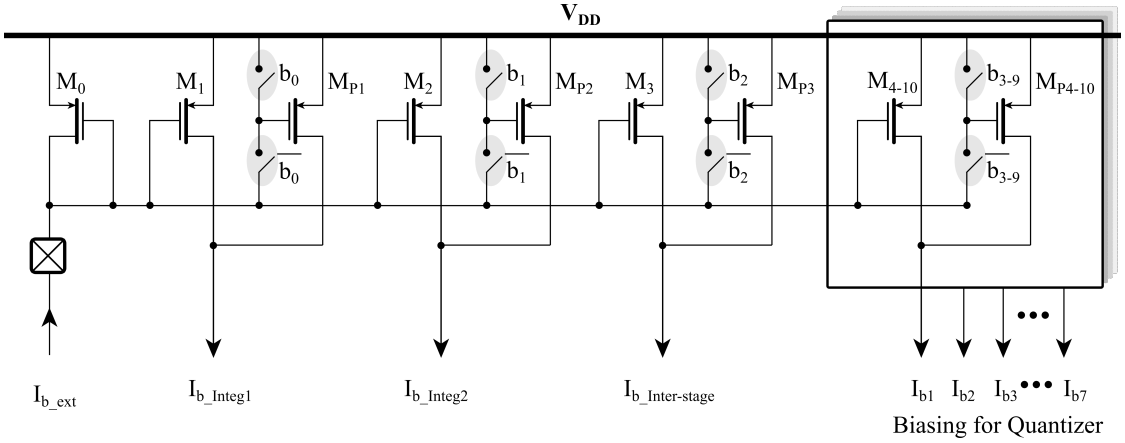


Figure 4.19: Programmable Biasing Block Diagram

of $10\ \mu A$ draining from V_{DD} through the diode connected transistor M_0 which generates the corresponding voltage V_{SG} across it's source-to-gate. This voltage is then utilized to create the multiple copies of the biasing current. The dimensions of the transistors are similar to the M_0 i.e. $\left(\frac{W}{L}\right)_0 = \left(\frac{W}{L}\right)_{1-10} = 3\left(\frac{W}{L}\right)_{P1-P10}$ Transistor M_1, M_2, M_3 is used to bias the op-amps in the first integrator, second integrator and inter-stage gain block respectively while those from M_4 to M_{10} biases the seven comparators in the quantizer. Furthermore, all the biasing current sources are made programmable through additional current source transistors M_{P1} to M_{P10} by programming bit b_0 to b_9 to have a flexibility to draw more current if needed by any particular block. When the programming bit is low, the gate of the transistors are connected to the V_{DD} bringing it's V_{SG} to $0\ V$ turning it *OFF* hence drawing zero current through the auxiliary source. Thus the nominal current is delivered.

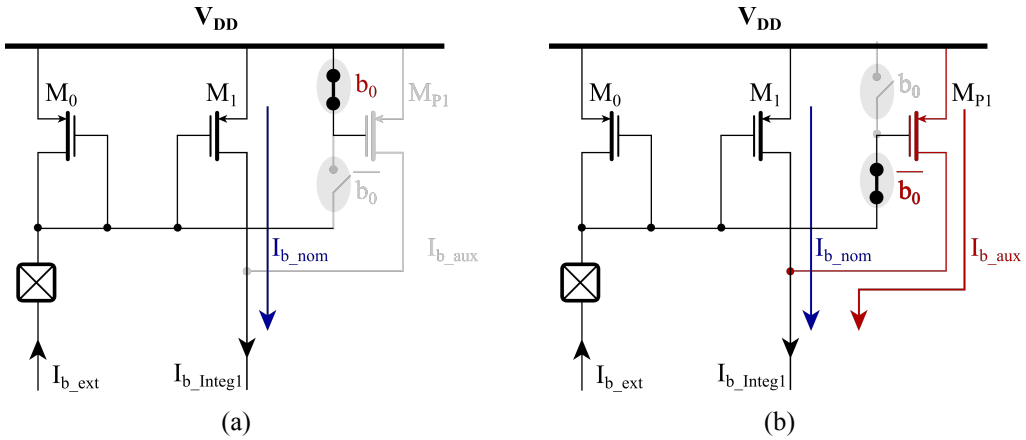


Figure 4.20: (a) Typical bias current: programming bit disables additional current (b) Higher bias Current: programming bit enables additional current

The dimensions of the auxiliary current sources ($M_{P1} - M_{P10}$) are such a that they can add 30% more current to the main current sources.

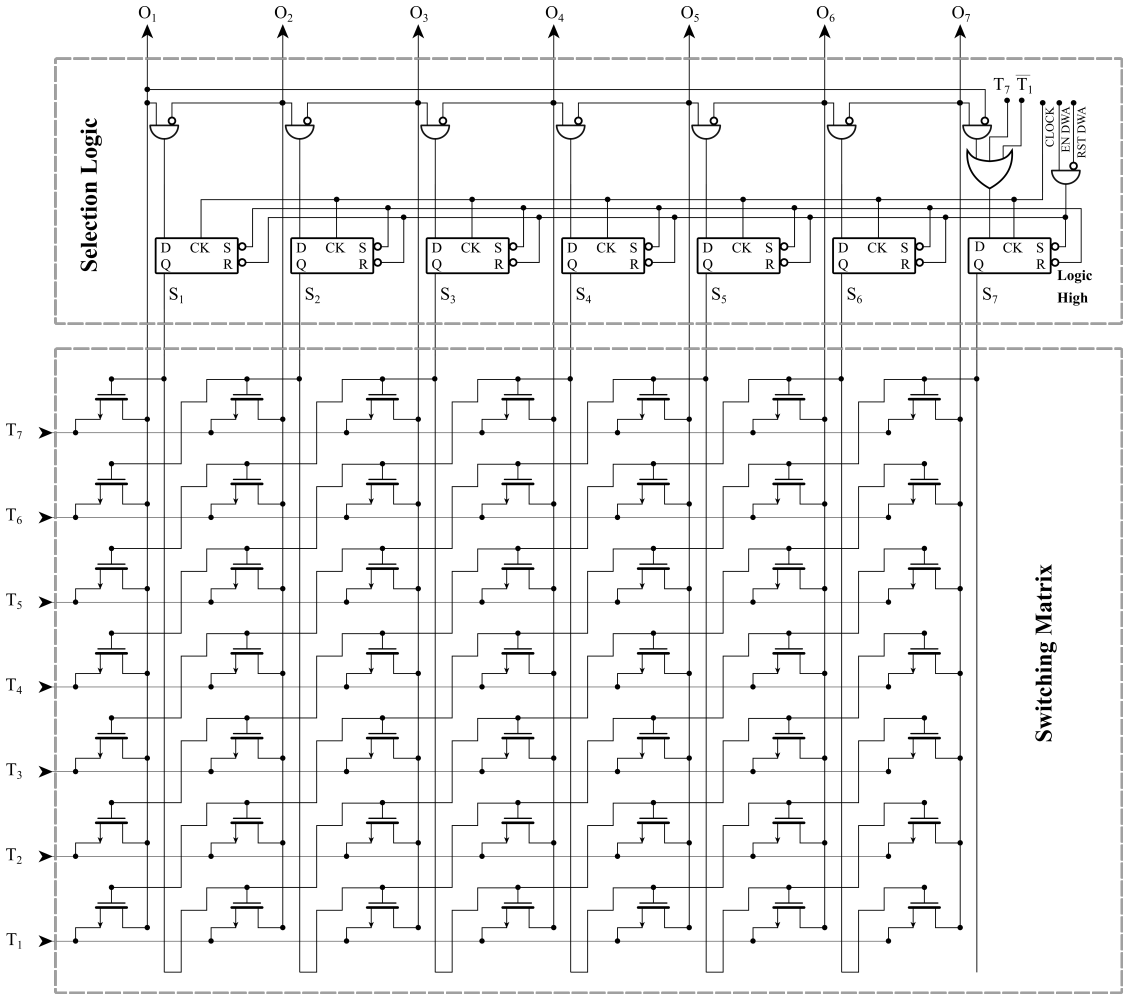


Figure 4.21: Data Weighted Averaging (DWA) implementation approach

4.6.2 Dynamic Element Matching (DEM)

In case of multi-bit digital-to-analog converter (DAC), due to the process variations, there is a mismatch between the unit elements. This mismatch causes the DAC levels to deviate from the ideal ones, which in turn makes the input-output characteristic of the DAC non-linear. Therefore, if the sinusoidal signal is passed through this non-linear function, it gives rise to the harmonics, significantly reducing the SNR, usually called signal-to-noise and distortion ratio (SNDR). Different techniques exists to solve this

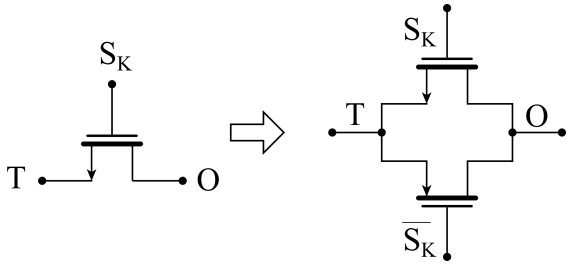


Figure 4.22: Transmission Gate

problem arising from unit element mismatch resulting into the non-linearity. The Dynamic Element Matching (DEM) technique is one of them and it's implementation is done as shown in Fig. 4.21. It it comprised of switching matrix and the selection logic. Switching matrix is shown just with NMOS switches, just for the representation, however, every switch in the design is consists of a pair of transmission gate switch, as shown in Fig. 4.22. The switching matrix acquires the thermometer code (T_7 to T_1) from the flash ADC and pass it to the outputs (O_7 to O_1) with different combination depending upon the state of the selection logic (S_7 to S_1). The Tab. 4.5 shows how the flash ADC

S_7	S_6	S_5	S_4	S_3	S_2	S_1	O_7	O_6	O_5	O_4	O_3	O_2	O_1
1	0	0	0	0	0	0	T_7	T_6	T_5	T_4	T_3	T_2	T_1
0	1	0	0	0	0	0	T_1	T_7	T_6	T_5	T_4	T_3	T_2
0	0	1	0	0	0	0	T_2	T_1	T_7	T_6	T_5	T_4	T_3
0	0	0	1	0	0	0	T_3	T_2	T_1	T_7	T_6	T_5	T_4
0	0	0	0	1	0	0	T_4	T_3	T_2	T_1	T_7	T_6	T_5
0	0	0	0	0	1	0	T_5	T_4	T_3	T_2	T_1	T_7	T_6
0	0	0	0	0	0	1	T_6	T_5	T_4	T_3	T_2	T_1	T_7

Table 4.5: The Output codes of the DEM based on the selection logic

thermometer code is passed to the output for given combination of selection logic. Extra features are also added to the DEM such as Enabling or disabling of DEM and resetting of the DEM. When DEM is disabled, the selection logic freezes the configuration to the state where S_7 is logic high and other selection bit (S_6 to S_1) are logic low. This feature helps to know the SNDR improvement.

4.6.3 Timing Block

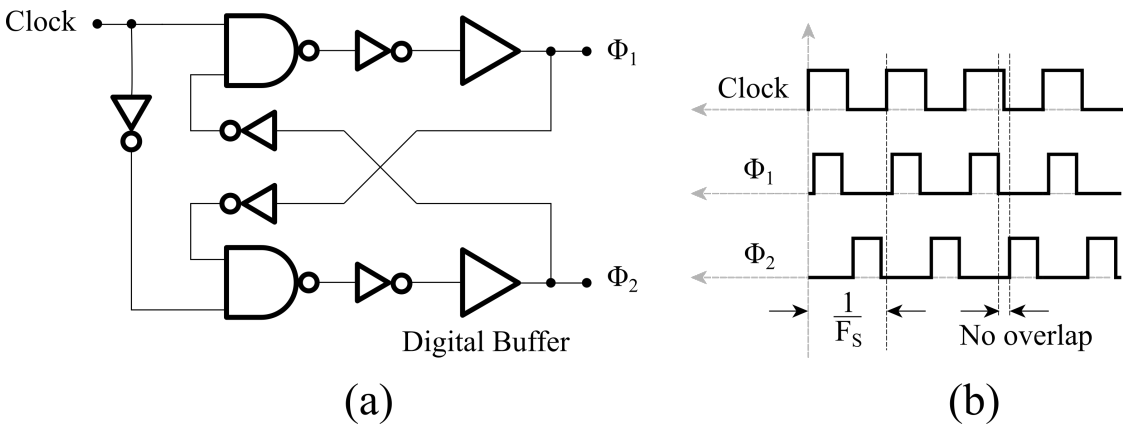


Figure 4.23: Schematic for generation of non-overlapping clock phases

The schematic of the non-overlapping phase generator is depicted in Fig. 4.23. The implementation has been done in order to derive the two non-overlapping clock phases Φ_1 and Φ_2 (and their complements $\overline{\Phi_1}$ and $\overline{\Phi_2}$, not shown in figure). It is also possible, if required, to pull-out the advanced and (or) the delayed versions of these phases through the buffers by revising the locations of the nodes through which the signals has to be pulled out. The non-overlapping time for the designed phase-generator working at 80 MHz is around 1.25 ns. After the fundamental phases are derived, some

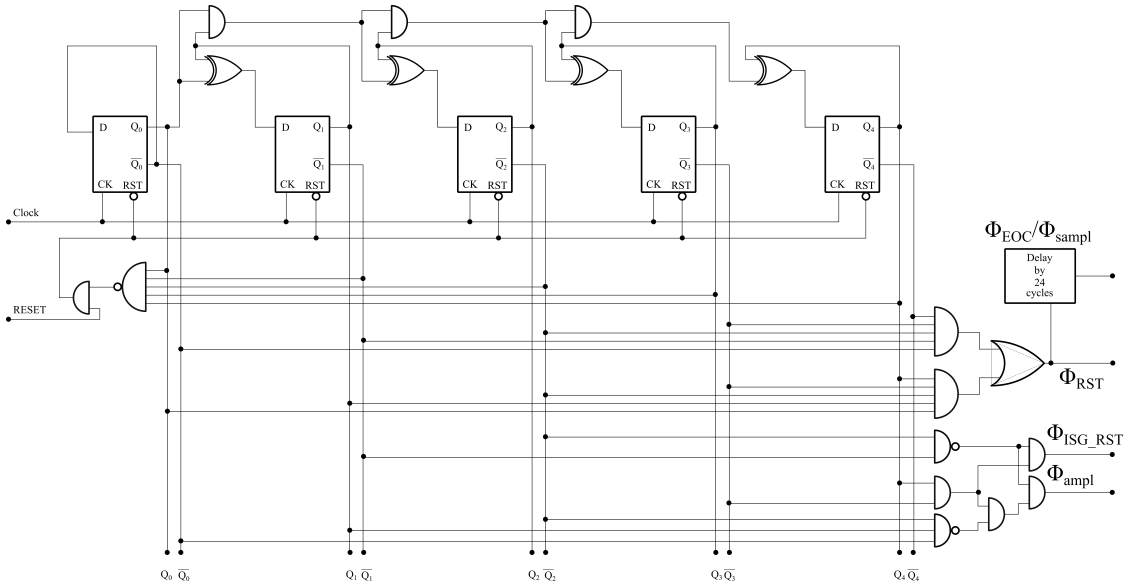


Figure 4.24: Schematic for generation of the different control signals for IADC and ISG

special control signals are required by the inter-stage gain (ISG) block such as phases for sampling the residue (Φ_{sampl}), amplifying the residue (Φ_{ampl}) and resetting the ISG (Φ_{ISGRST}) while IADC requires the signals such as Φ_{EOC} and Φ_{RST}. These signals are generated by employing MOD-24 counter and a combinational logic as shown in Fig. 4.24 and signals are depicted in Fig. 4.25.

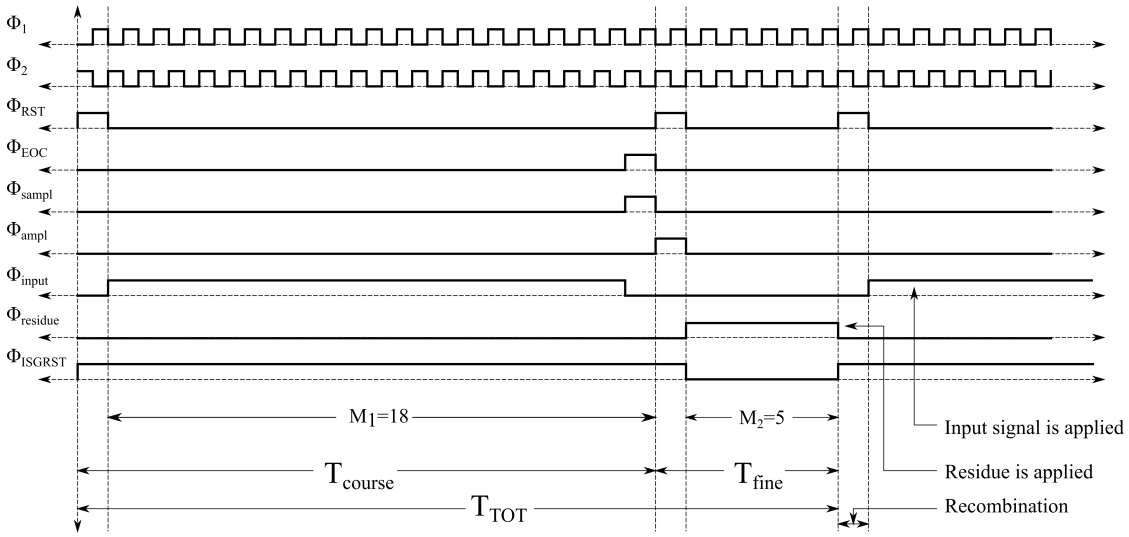


Figure 4.25: Timing diagram of the different control signals for IADC and ISG

4.6.4 Thermometer to Binary Conversion

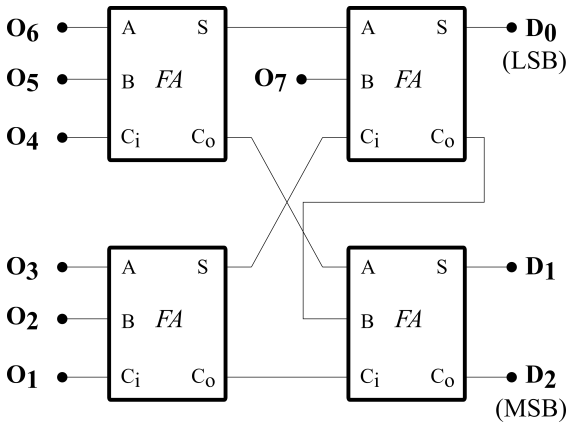


Figure 4.26: Thermometer to Binary Encoder

A 7-bit thermometer code delivered by the flash ADC must be converted into a 3-bit binary code so as to ease the interface of the chip to the instrument reading the bit during the measurements. Therefore, a thermometer-to-binary encoder is employed as depicted in Fig. 4.26. The basic building block of this encoder is a full-adder (FA). The full adder counts the number of ones present at it's input and produces the sum S and carry C_o. The encoder is also called as a ones counter since it counts the total number of 1s delivered by flash ADC and converts it into binary code. Even in presence of the bubble, this encoder works efficiently and converts into a correct binary code, this encoder is advantageous. The number of full adder cells needed for implementation of n-bit binary encoder is given as,

$$K_n = \sum_{i=1}^{n} (i-1)\, 2^{(n-i)} \tag{4.33}$$

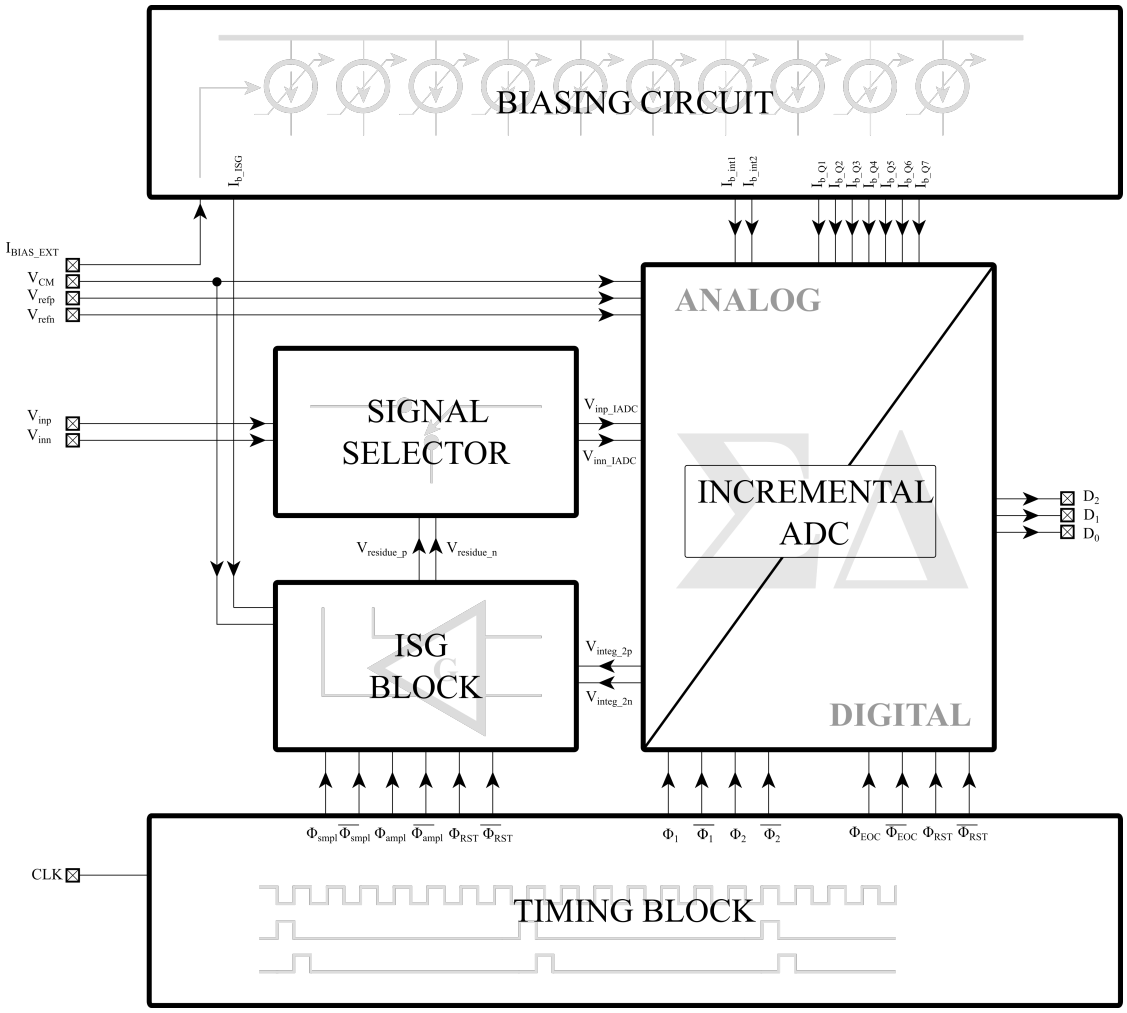


Figure 4.27: Block Diagram of full architecture of ERADC with core and the supporting blocks

Chapter 5

Simulation and Measurement Results

5.1 Introduction

After extraction of the requirements of the op-amps from the simulink simulations, it is a standard approach to design an ideal system in the cadence environment and cross-verify the functionality as well as the performance of the overall architecture. Then the process of design of the blocks at the transistor level begins. In order to keep the debugging process easier, block-by-block replacement in the ideal architecture, with transistor level blocks is done and the performance is assured with each block replacement. Once the full architecture is transformed from ideal blocks to the transistor level blocks, the blocks are laid-out one by one. A similar technique is exercised and one-by-one the transistor level blocks are replaced by the parasitic extracted blocks until the complete architecture is laid-out. With post-layout simulation, the performance is insured again.

The chapter presents the simulation results in the cadence environment with the three steps described above i.e. with ideal blocks, transistor level blocks of the whole ERADC architecture and post-layout simulation results of the extracted top level. Finally as a maiden version, the first tape-out focuses on the first-stage i.e. Incremental ADC where the characterization of the chip is accomplished with positive results and are presented.

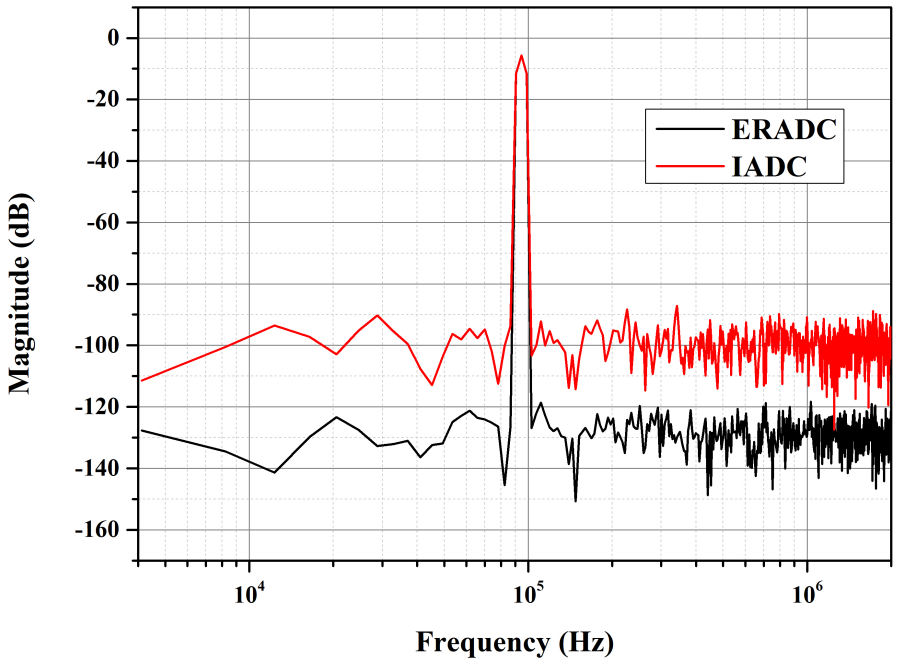


Figure 5.1: Power Spectral Density of the output of Incremental ADC and Extended Range ADC with all the blocks ideal

5.2 Simulation Results

The simulated output spectra of the IADC and of the ERADC are shown in Fig. 5.15.2 and 5.3. The input signal is a sinusoid with an amplitude of -6 dB with respect to full-scale at frequency of 100 kHz while the architecture is clocked at a frequency of 80 MHz.

In case of ERADC architecture with ideal blocks, the SNR that can be achieved from the coarse quantization is around 60 dB with a noise floor around -100 dB. However, the overall SNR delivered after the recombination of the coarse and fine quantization is 86.86 dB, i. e. 26 dB better than the IADC standalone, and the noise floor is as low as -125 dB. The overall Spurious-Free Dynamic Range (SFDR) achieved is around 96 dB as shown in Fig. 5.1.

The simulations results of the ERADC architecture with transistor level blocks are much similar to that of the ideal simulation results. The SNR from coarse conversion attained is around 60 dB while that achieved with complete ERADC structure is around 84 dB with noise floor residing at -125 dB as depicted in Fig. 5.2, SNDR, however, drops down to 70 dB on account of the harmonics. The results of the extracted simulations are depicted in Fig. 5.3. With coarse quantization, the SNDR that can be achieved remains equal as that in the ideal simulation or that in the simulation with blocks at transistor level i.e. around 60 dB. However, the SNDR in case of complete architecture of ERADC deteriorates w.r.t. ideal case, to 73 dB, still maintaining the noise floor at -125 dB, in presence of harmonics.

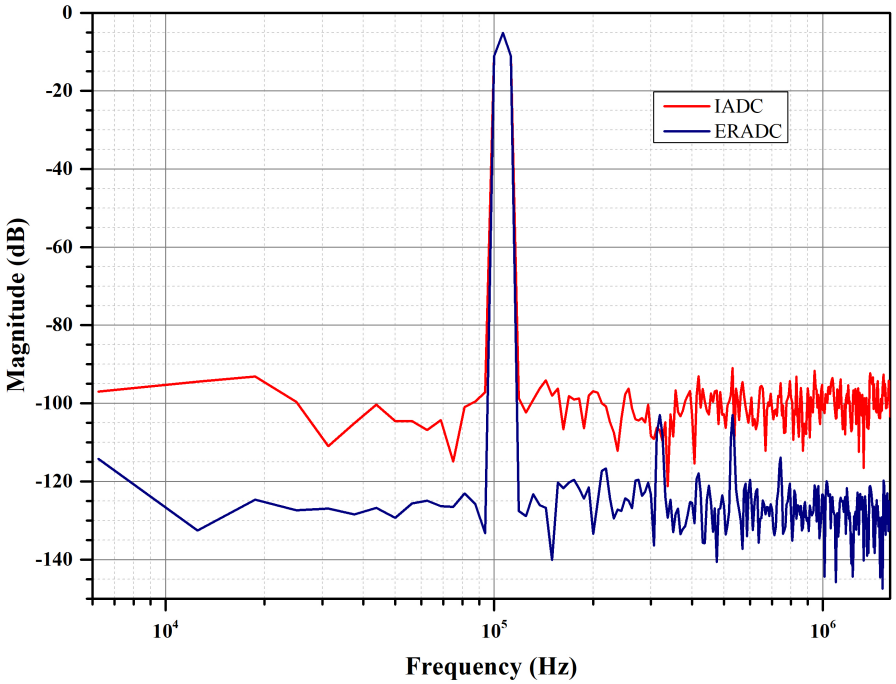


Figure 5.2: Power Spectral Density of the output of Incremental SDM and Extended Range ISDM at Transistor Level

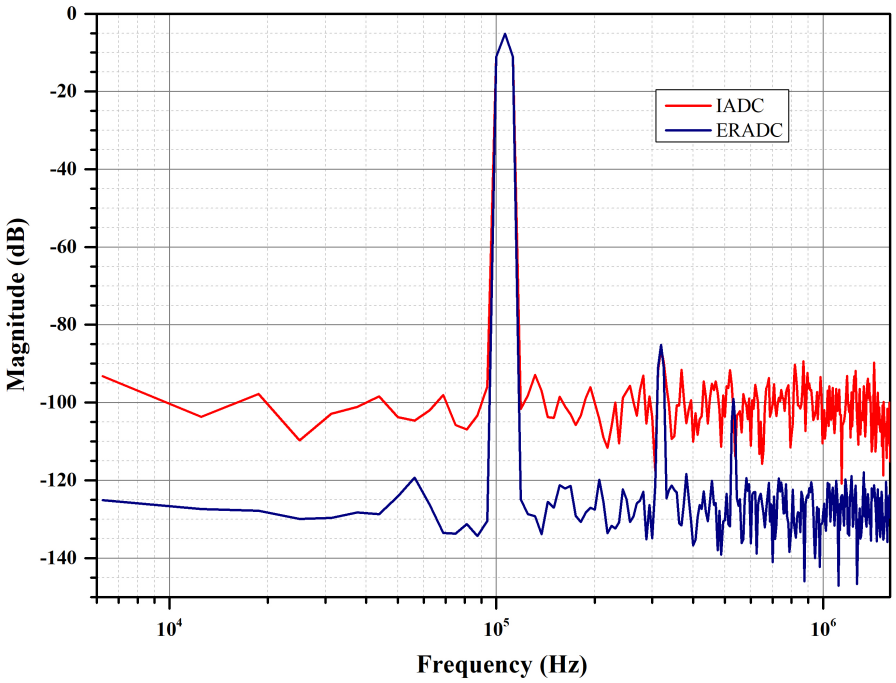


Figure 5.3: Post-Layout simulation Power Spectral Density of the Incremental SDM

5.3 Measurements Results

The Incremental ΣΔ ADC has been fabricated and it's performance has also been measured. This version of the architecture is configured in two modes, Incremental mode (I-mode) and Sigma-Delta mode (SD-mode). When I-mode is active, the structure

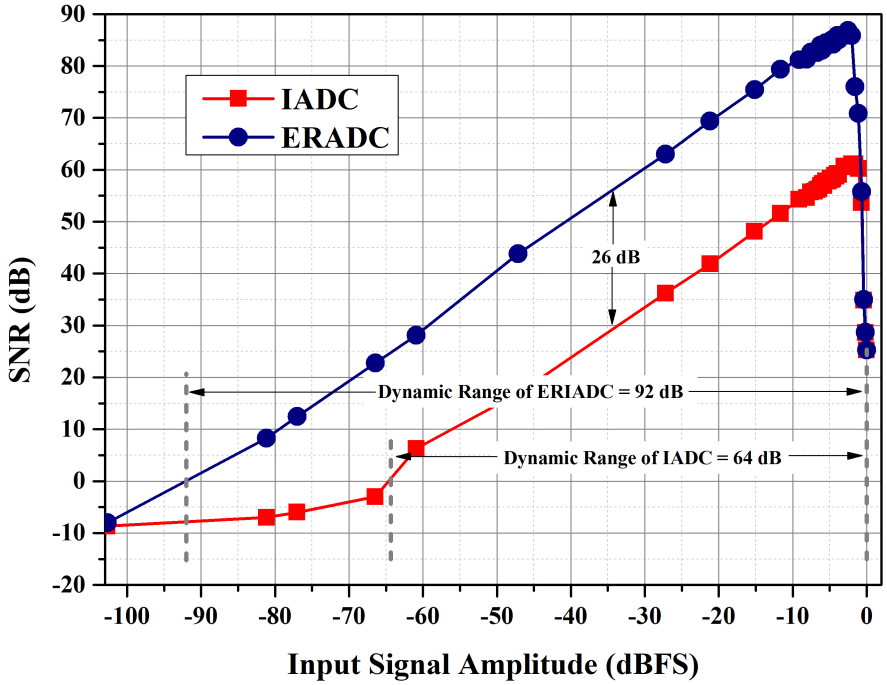


Figure 5.4: Signal-to-Noise Ratio Vs input signal amplitude of ERADC with all the blocks at transistor level design

generates the RESET signal every 19 clock cycles and resets all the memory elements while in case of SD-mode, it does not generates the RESET signal thus structure runs freely maintaining the quantization noise memory. This selection of the configuration of either of the modes is done through the JTAG programming bit.

The measurement set-up was done as shown in Fig. 5.5. For the input sinusoid, a function generator was used generating differential inputs, for square wave clock, a clock generator, a bias current drawn from the source-meter and for the DC voltages such as common-mode voltage, reference voltages, supply voltages and ground, the power supplies were used. The programming bit such as SD/I mode-selection, Power-down mode and programming bit of bias currents for op-amps and comparators in the quantizer, a JTAG programming was used. Then, once the conversion is done, the digital bit were acquired by interfacing Logic analyzer and the text file was created. Further post-processing was done in the MATLAB by importing the generated text file with output bit where the SNR, SNDR, dynamic range (DR) were calculated and FFT graphs were plotted to see the PSD of the digitized signal.

5.3.1 Sigma-Delta Mode:

Fig. 5.7, 5.7 and 5.8 shows the measurements results of the architecture when configured in the sigma-delta mode. Fig. 5.7 is the output spectrum of the signal when the input signal is applied at a frequency of 100 kHz with an amplitude of around -6 dB with respect to the full-scale and the clock frequency is 80 MHz. For the measurement of

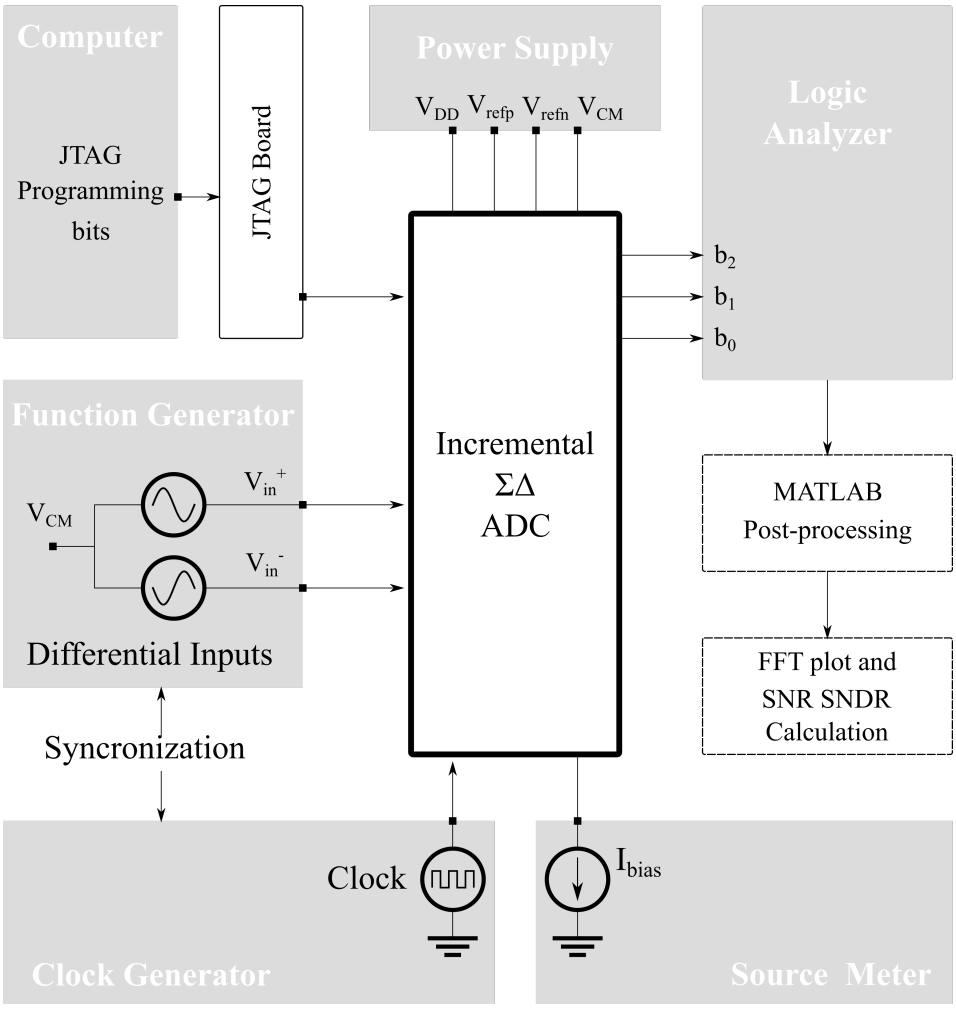


Figure 5.5: Measurement Set-up for the characterization of the Incremental (ΣΔ) ADC

the parameters like SNR, SNDR and DR, the signal bandwidth taken into account was 2 MHz. In the output spectrum, along with input tone, few harmonics are also present and the justification for the even harmonic lies in the absence of input buffer whereas for odd harmonics, it is the mismatch in the unit elements of the feedback DAC. The SNDR obtained in this case is 60.7 dB, SNR of 66.4 dB while the dynamic range is 72.8 dB.

Fig. 5.7 shows the SNDR, SNR and DR as a function of input signal amplitude. The maximum SNR obtained is 66.4 dB at an input amplitude of -6 dB hence an MAS (Maximum Stable Amplitude). When the amplitude of the signal is increased from -10 dB to -6 dB, the power of the harmonics goes on increasing causing a harmonic distortion. Therefore, SNDR characteristic starts deviating down from the SNR one. Further increase in the amplitude transgresses the MSA causing input dependent instability giving rise to nonlinear behaviour of the ADC, thus a significant drop in the performance as shown in the subplot of Fig. 5.7.

The performance of the architecture in Sigma-Delta mode is also evaluated w.r.t. the oversampling ratio and can be verified by in-band noise expression of the second-order

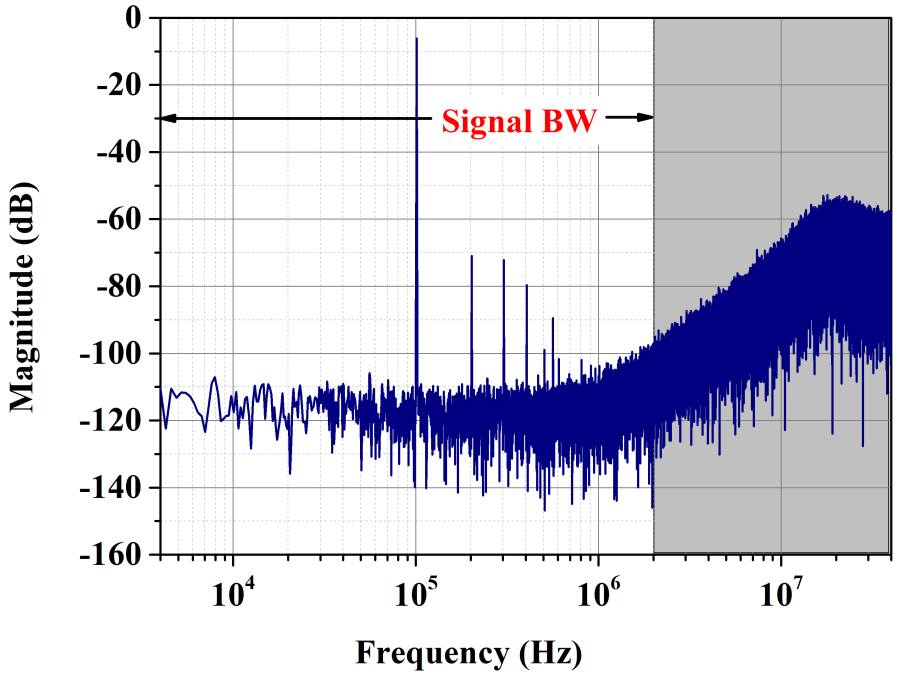


Figure 5.6: PSD of the Sigma-Delta (ΣΔ) ADC

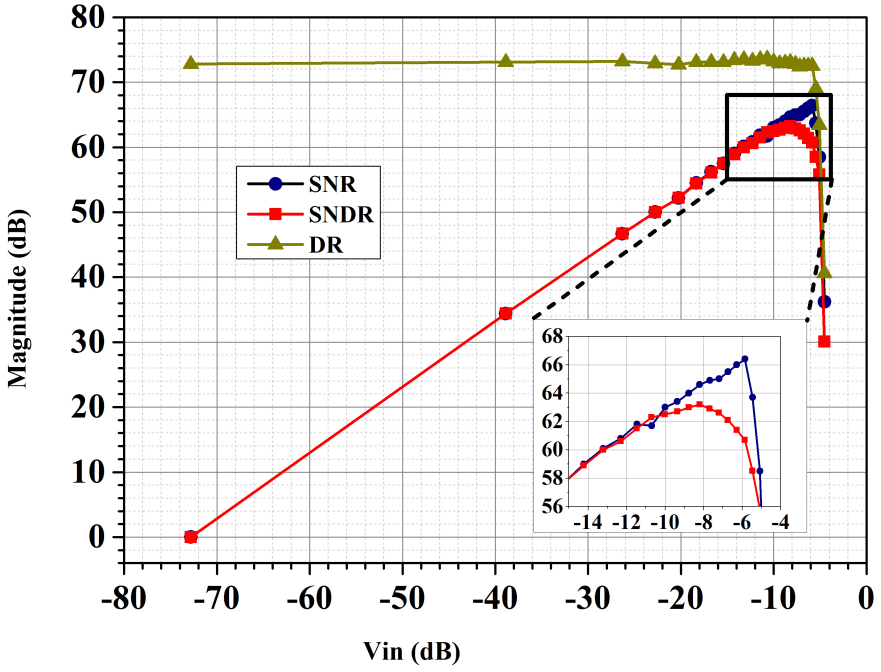


Figure 5.7: Performance of ΣΔADC as a function of input signal amplitude

ΣΔADC given by Eq. 5.1,

$$In\ Band\ Noise = \frac{\Delta^2}{12\pi}\frac{1}{5}\left(\frac{\pi}{M}\right)^5 \tag{5.1}$$

where, Δis LSB of the quantizer and M is the oversampling ratio. The above Eq. 5.1 indicates that for every doubling of the OSR i.e. M, the quantization noise goes down

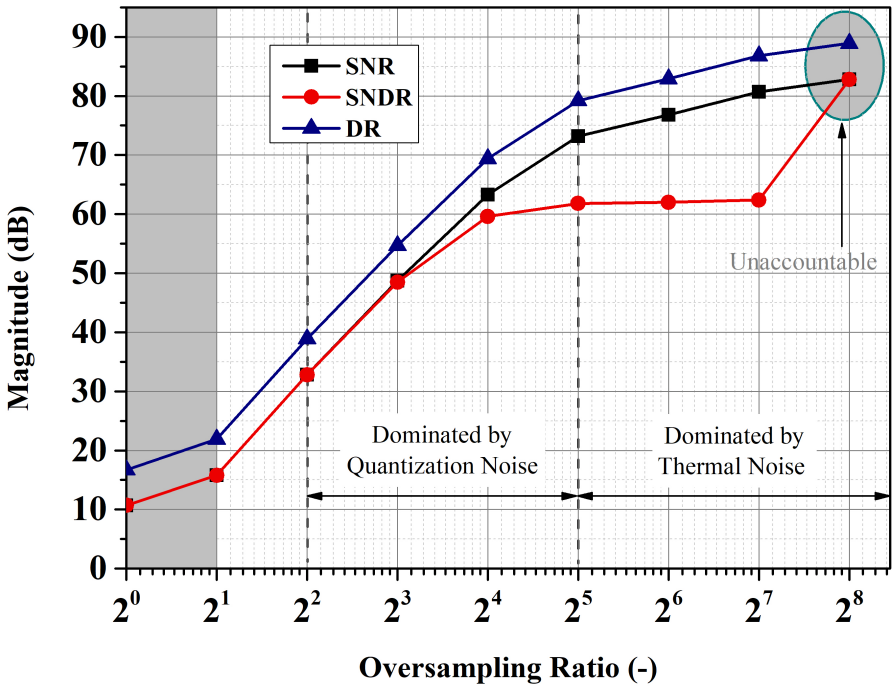


Figure 5.8: Performance of ΣΔADC as a function of input signal amplitude

by a factor of 32 i.e. 15 dB.

As depicted in Fig. 5.8, in the range from OSR value 2^2 to 2^5, the SNR is dominated by the quantization noise (i.e. region with noise shaping with slope of -40 dB/decade). This can be observed in Fig. 5.7, from frequency 1 MHz to 20 MHz. In this region, for every doubling of the OSR value, there is improvement in SNR by a factor of 15 dB, thus analysis result matches with the outcome from equation Eq. 5.1.

Further, when there is an increase in the OSR above 2^5, the bandwidth of noise integration gets limited to a region where the thermal noise is more dominant over SNR than the quantization noise. In Fig. 5.7, it extends below frequency of 1 MHz.

The measured SNDR at an OSR of 2^8 is, however, not accountable. Because, in this measurement, the bandwidth taken into account for measuring noise power is less than the 200 kHz while the input signal is at 100 kHz. Therefore, this is, in fact, masking the harmonics, though they are present in the spectrum.

5.3.2 Incremental Mode:

The output spectrum in case of Incremental mode is shown in Fig. 5.9. The RESET feature incorporated to make the ADC accessible for multiple input sources in incremental mode erases the quantization noise memory from the integrators. The reason behind the fact that IADC PSD does not exhibit the noise shaping is the reset (loss of noise memory) along with decimation filtering (Fig. 5.9).

The input signal is applied at a frequency of 100 kHz with an amplitude of -5 dB while the architecture is clocked at 80 MHz. The SNDR achieved with this setup is 55.0 dB,

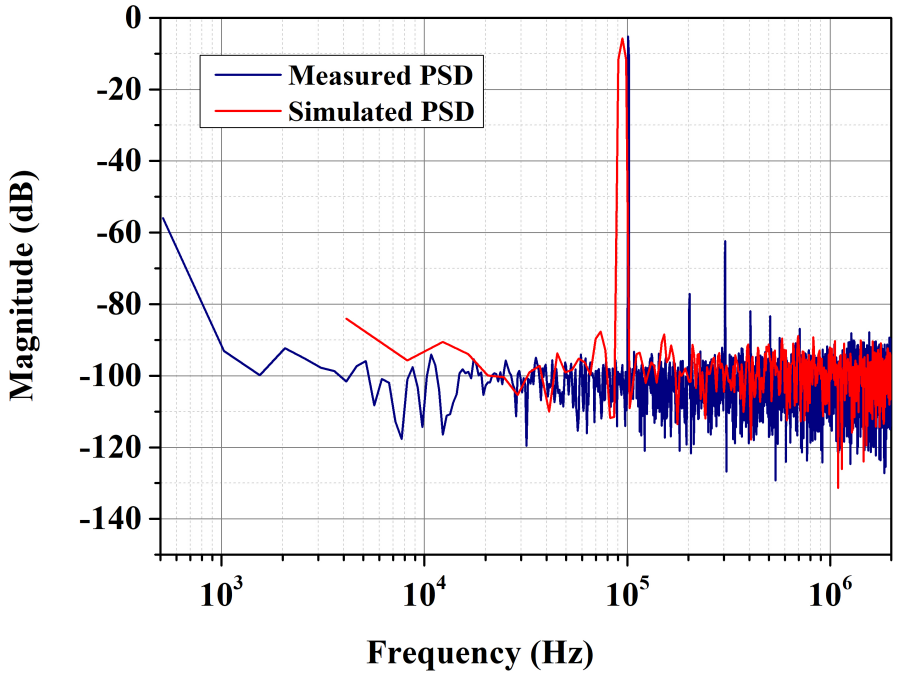


Figure 5.9: PSD of the Incremental ADC

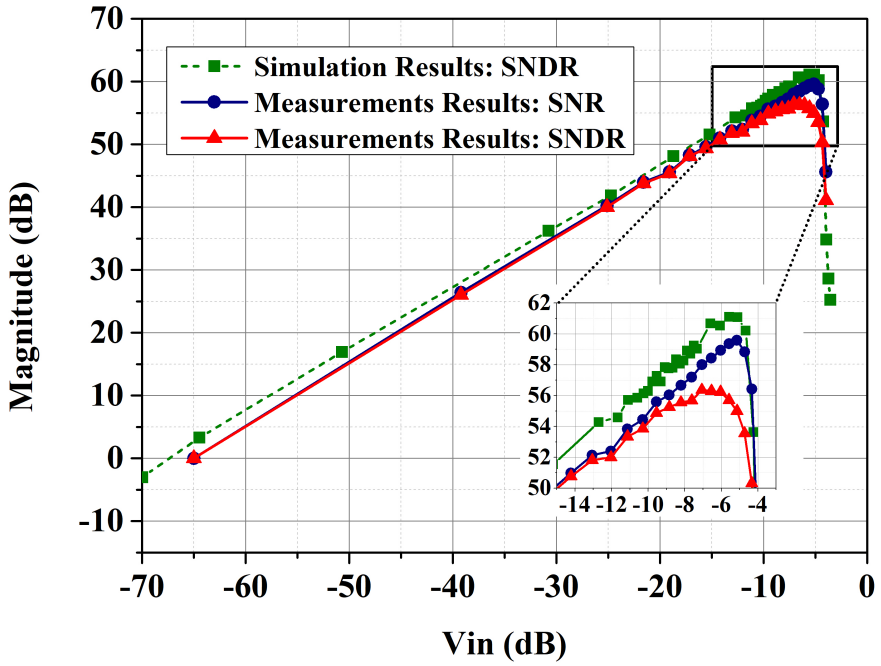


Figure 5.10: Performance of IADC as a function of input signal amplitude

SNR of 59.58 dB and the DR is around 65 dB with noise floor residing at around -100 dB. The SNDR, SNR and DR are then measured as a function of the input signal amplitude and are plotted in Fig. 5.10. From the graph it is clear that the maximum SNR that can be obtained from the IADC architecture is 59.58 dB at an input signal amplitude of -5.0 dB w.r.t. the full scale which makes it an MSA. In the subplot of the Fig. 5.10, it can be seen that, as input amplitude is increased from -15.0 dB to -5.0 dB (an MSA), the

Parameter	This Work			[33]	[23]	[34]	[35]	[36]
Architecture	**SD-Mode**		**I-Mode**	CT-MASH ΣΔ ADC	CT-ΣΔ ADC	DT-MASH ΣΔ ADC	IADC+Cyclic	Time-Interleaved IADC
Technology	**130 nm**		**130 nm**	28 nm	65 nm	130 nm	180 nm	180 nm
Supply Current	**2.6 mA**		**2.6 mA**	17 mA (A)+ 18 mA (D)	—	—	—	450 µA
Supply Voltage	**2.5 V**		**2.5 V**	1.1 V(A)/1.0(D)/1.8	0.8 V	—	—	3 V
Conversion Time	—		**237.5 ns**	250 µs	1 ms	50 µs	800 ns	5 µs
Bandwidth	2.1 MHz	**1.25 MHz**	**2.1 MHz**	15 MHz	500 Hz	10 kHz	625 kHz	100 kHz
SNR_{max}	66.4 dB	**73.2 dB**	**59.6 dB**	67.5 dB	66.2 dB	60.8 dB	96.6 dB	101.5 dB
$SNDR_{max}$	63.0 dB	**63.0 dB**	**56.4 dB**	67.5 dB	66.2 dB	60.8 dB	96.6 dB	101.5 dB
FoM	151.5 dB	**156.0 dB**	**144.7 dB**	156.5 dB	154.1 dB	154.4 dB	170.1 dB	163.8 dB

Table 5.1: Performance summary of the proposed ADC and comparison with the state-of-the-art

SNR characteristic continues to raise linearly but SNDR diverges starts shifting down progressively as a consequence of harmonic distortion. The maximum SNDR that can be obtained is 56.37 dB and corresponding SNR is 58.0 dB at an input amplitude of around -7.0 dB.

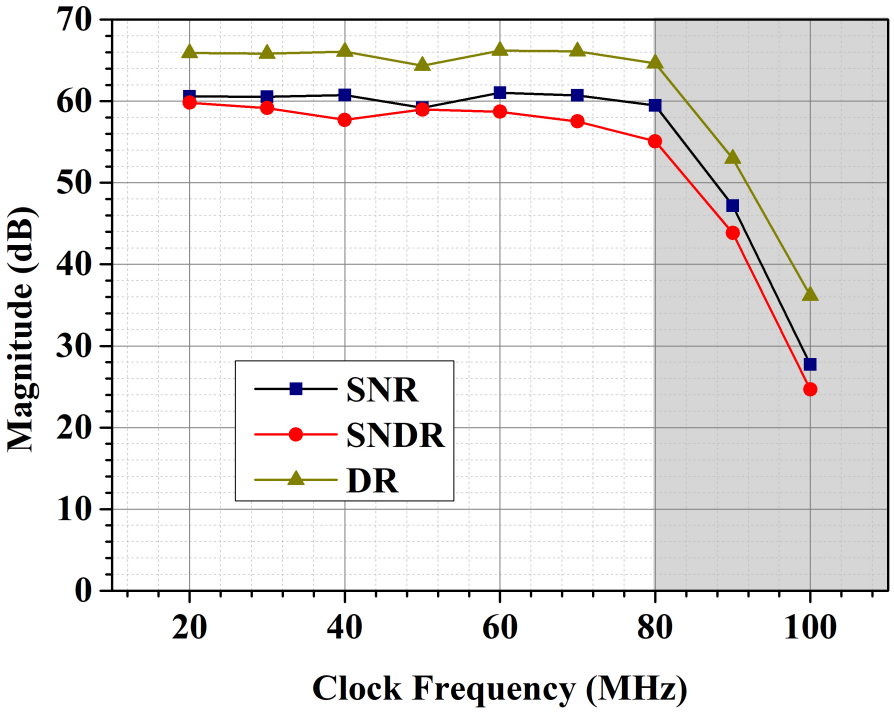


Figure 5.11: Performance of IADC as a function of clock frequency

The architecture has been designed to work in an incremental mode at a maximum speed of 80 MHz. Therefore the performance of the structure for the clock frequency is verified by varying the clock frequency from 20 MHz to 100 MHz and the parameters are plotted as shown in Fig. 5.11. SNDR, SNR and DR stays almost constant for the clock frequencies from 20 MHz to 80 MHz but later on the performance degrades significantly when running it at 90 MHz and 100 MHz.

The performances of the prototype ADC, for both SD-mode and I-mode, are summarized and compared with the state-of-the-art in Tab. 5.1. In order to have a fair platform for the comparison between different architectures, we used the Schreier figure of merit [37], defined in Eq. 5.2

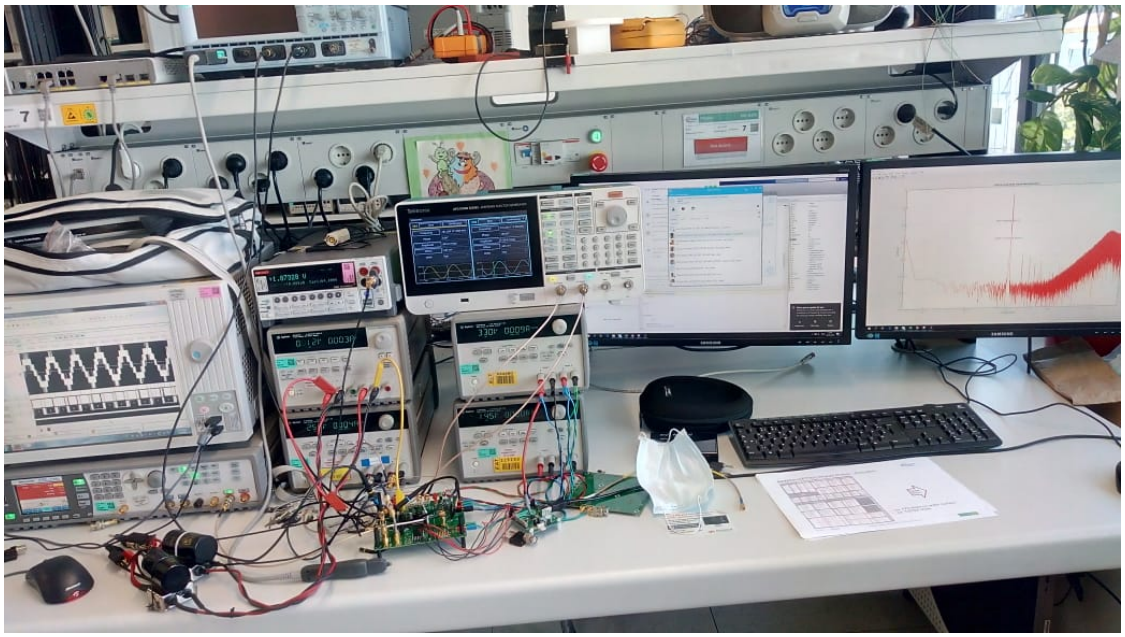


Figure 5.12: A complete Set-up in the lab for the characterization of the samples

$$FoM = SNR_{max} + 10\log_{10}\left(\frac{Bandwidth}{Power}\right). \tag{5.2}$$

Chapter 6

Conclusion

Having considered the specifications, the extended-range second-order Incremental A/D converter architecture is proposed to attain the ENOB of 12 or equivalently, an SNR of 72 dB at a sampling clock speed of 80 MHz within the 25 number of clock cycles.

The extended-range approach has been investigated, developed and verified in the Simulink. In order to decide the specifications of the operational amplifiers and the resolution in the quantizer in the $\Sigma\Delta$-loop, the sensitivity analysis is carried out where the non-idealities such as low frequency gain and finite GBW were introduced in the architecture and were swept to find out their minimum requirements.

From the analysis and comparison carried out between the standalone IADC and the extended-range IADC explicitly turns out that, in order to attain a given SNR, the extended-range IADC requires a significantly lower number of clock cycles than a conventional IADC, but the requirements of the op-amps are much more stringent. Moreover, the partitioning of the resolution between IADC and ERADC in extended-range IADCs also affects the op-amp specifications: the higher is the resolution in the ERADC, the higher are the op-amp requirements.

Blocks are then designed in the Cadence environment for the extracted specifications and the Extended-range second-order IADC architecture is developed with ideal blocks and then transistor level blocks. In simulations with architecture with ideal blocks, the SNR obtained from the coarse quantization is around 60 dB and overall it is 86 dB. At transistor level simulations, the coarse quantization offers same SNDR of 60 dB while overall SNDR drops down to 70 dB on account of the harmonics present, however, still

maintaining the noise floor at same level. In case of extracted simulations, there is no degradation in the SNDR from the coarse quantization keeping it to 60 dB, nevertheless, overall architecture of ERADC exhibits SNDR of 73 dB with presence of harmonics and SNR of 81 dB. The harmonics present in the output spectrum impels the need of further investigation.

The characterization of the first chip has been done which involves measurements of the oversampling ADC (only the first-stage of the ERADC without residual ADC) architecture which can operate either as sigma-delta modulator (SD-mode) or incremental ADC (I-mode), in order to allow reading out a single-sensor with maximum performance (SD-mode) or multiple multiplexed sensors with lower performance (I-mode). When configured in SD-mode, the ADC achieves a *SNR* of 73.2 dB with a signal bandwidth of 1.25 MHz and a *SNR* of 66.4 dB with a signal bandwidth of 2.1 MHz, while in I-mode the *SNDR* and *SNR* reduce to 56.4 dB and 59.6 dB, respectively. The *SNR* in SD-mode can be further increased by reducing the bandwidth. The ADC, with a sampling frequency of 80 MHz in both modes, consumes 2.6 mA from a 2.5 V power supply. The peak *FoM* achieved in the two modes is 156.0 dB and 144.7 dB, respectively.

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