UNIVERSITÀ
DI PAVIA

Università degli Studi di Pavia

Department of Electrical, Computer and Biomedical Engineering

Ph.D Thesis

A new topology for battery systems: Reconfigurable Cascaded Multilevel Converter

Professor:
Pericle Zanchetta

Ph.D. student:
Giulia Tresca

Academic Year 2021/2022

”E senti allora,

se pure ti ripetono che puoi

fermarti a mezza via o in alto mare,

che non c’è sosta per noi,

ma strada, ancora strada,

e che il cammino è sempre da ricominciare.”

A galla - Eugenio Montale

Acknowledgements

When I started my PhD, I was concerned about starting this challenging path two years after my Master degree; I was worried to move abroad again, without a clear return date; I was scared that, in the end, the PhD could have been the wrong choice.

Finally, almost four years later, a pandemic, five different apartments, three different countries and cities, I started to understand that life assumes its shape even without your touch and that making the wrong choices is way better than not make them at all.

I address my first thanks to Francesco. For the love, support, sharing and tenacity with which he smiled at all my doubts and fears. To the lightness that has always given to my life. Being your partner is a joy and an honor.

To my family, for their support beyond any limits. To my mother, who believed in me before I really did it; to my father, for constantly teaching me to never give up ; to my sister, for the joy she spreads.

To my old friends, who respond to my escapes with their presence.

To Giorgio, Marcella and Jacopo, for giving me your warmest hug in every moment. You made my period in Nottingham an incredible journey.

To my colleagues in Pavia, for enduring and supporting me during every working day. For lunch chatter, Friday cocktails and the time-consuming laughter at everything that doesn't work.

I would like to finally thank my two supervisors, Professor Zanchetta and Andrea Formentini. Your complementary guides were exhausting, challenging and incredibly satisfying. You have been and are a source of inspiration, every day, for the passion and tirelessness with which you

dedicate time and energy to this work.

After almost four years, my Ph.D is ended but I hope that, the light it brought into my life, will continue to shine.

Abstract

Electric vehicles cover a fundamental role for the sustainability transition of the transportation sector. In the past ten years, the investments and efforts dedicated to the developments and improvements of electric powertrain have been increasingly significant from almost all automotive companies. Battery electric vehicles are the most promising solution, guaranteeing zero local emissions and high efficiency in energy conversion.

However, the electrical architecture adopted until now, consisting in a stiff connection between a battery pack and a two-level inverter, presents two main drawbacks related to the converter topology and energy system configuration. On one hand, the two-level inverter can guarantee high efficiency only at nominal loads, showing drastic drops for partial loads operations. On the other hand, the battery pack is characterized by a fixed serial and parallel connection of battery cells, limiting the energy delivery of one string to the weakest cell. Both drawbacks are extremely critical in electric vehicles applications, since the motor is required to often work at partial loads - i.e. in city traffic - and the driving range may significantly decrease with the low efficiency operations of the battery pack.

Therefore, some research works have suggested a conceptual revision of the converter and battery pack used in electrical powertrain structures. In this regard, multilevel converters started to gain attention as valid candidates to replace conventional converters in powertrain architectures. Splitting the battery pack in several modules allows to limit the serial connection of cells and consequently decrease the probability of having multiple weak cells. Moreover, the presence of more submodules reduces the stress on the devices, permitting a theoretical indefinite increase of

the DC-link voltage.

Since an optimal battery system management relies on the possibility to access the single battery cells, other works in the scientific literature suggested the utilization of Reconfigurable Battery Systems. These systems allow to perform active management of the battery system by controlling the connection between the battery cells through a coherent placement of electronic switches.

The role of Multilevel converters in electrical powertrain is considered central in this work. This research work presents a new topology, called Reconfigurable Cascaded Multilevel converter able to simultaneously implement the power conversion and the battery management. In each submodule, battery cells are serially connected in groups of three through a pattern of switches, forming a single unit called Reconfigurable Battery Module. In this way, each battery cell can be controlled, enhancing sorting algorithms during both charging and discharging processes and fault tolerant strategies. The new topology is explained in details and then used in different case scenarios to prove its validity.

Contents

List of Figures

List of Tables

CHAPTER

1 Introduction

Climate change is recently a frequent subject of global debates. The massive human-related greenhouse gas (GHG) emissions led to the increase of the global temperature, with catastrophic effects on natural ecosystem and severe impacts on human health and economic sectors [1]. Over the past years, the fight against climate change brought political institutions to adopt several commitments: in 1997, and later re-confirmed in 2013, the Kyoto protocol was drawn up by UNFCCC (United Nations Framework Convention on Climate Change) with the aim to reduce the GHG emissions, according to customized targets for each country [2]. In 2016, the Paris agreement was signed by the 55% of UNFCC countries with three main goals: GHG emissions reduction to contain the global warming, resiliency to the climate change and investments intended to promote no emissions activities [3].

Among all pollutants sectors, the transportation is one of the largest contributors, responsible for 25% of global CO_2, with a negative record covered by road vehicles, which represent the 75% of total emissions of this cluster [4]. Internal Combustion Engine Vehicles (ICEVs) still represent the most diffuse technology used for private vehicles, thanks to high-energy density of the fuel fossils, the abundant logistic and supply network. Moreover, ICEVs market is very well established guaranteeing affordable prices both for vehicles and fuel refill.

Recognizing the absolute priority for private transportation, as fundamental aspect of the economic growth of the last century, the electrification of road transportation is an important

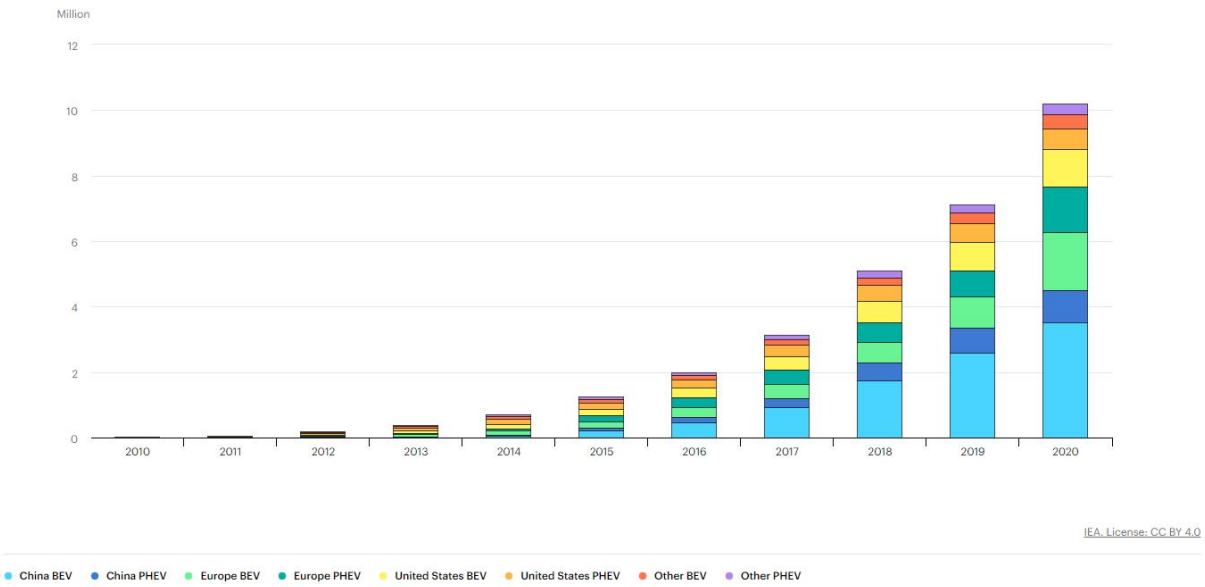


Figure 1.1: Stock of electric vehicles in the year range 2010-2020 [6].

target for many countries, to contribute to emissions mitigation. In this scenario, electric vehicles (EVs) have gained an increased attention as sustainable alternative to the ICEVs, thanks to their independence from petroleum, absence of emissions and high efficiency [5]. As shown in Fig.1.1, EVs market has grown exponentially in the last ten years: by the end of 2020, the stock of EVs was around 10 million; this number is expected at least to double by 2050.

1.1 Electric Vehicles

The adjective electric refers to all vehicles which use electrical energy to feed the motor. However, the electrical energy may come from different sources according to which the EVs can be categorized:

- Hybrid Electric Vehicles (HEVs) have two energy sources - a primary and secondary source-, usually consisting in fossil fuels and high voltage (HV) battery. Among this category, two different technologies can be distinguished, depending on how the energy

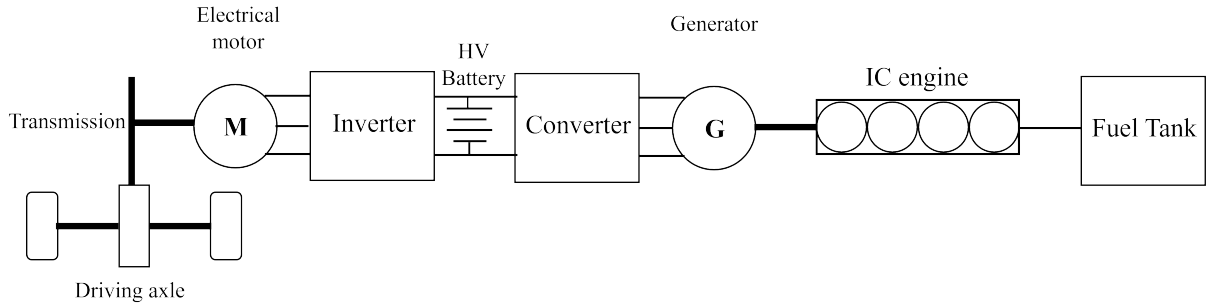


Figure 1.2: Parallel Hybrid Electric Vehicle structure.

sources are used. In Parallel HEV, whose structure is shown Fig. 1.2, the electrical motor is fed with the energy generated by an IC engine. In Series HEV, whose structure is shown Fig. 1.3, an IC engine, powered by fossil fuels, and an electrical motor, powered by a high voltage battery, co-exist and are used in complementary way. In both way, HEVs represent the combination of electrical and combustion engine traction concepts, obtaining the benefit of long driving ranges given by fossil fuels and the high efficiency of the electric powertrain.

- Fuel Cell Electric Vehicles (FCEVs) power the electrical motor with the energy obtained through the chemical process between hydrogen and oxygen in fuel cells. The operative principle of this energy sources is not the storing but the continuous generation as long as the fuel supply is kept. FCEVs promises low emission rate, guaranteed by the absence of combustion during the generation process, and long driving range, allowed by the concept of the continuos generation. Despite of the benefits, FCEVs still remain under investigation because hydrogen management is considered dangerous and extremely expensive.

- Battery Electric Vehicles (BEVs) uses the energy stored in electrochemical rechargeable battery packs. These types of vehicles are also called fully electric drives because they do not support any other source of propulsion.

BEVs are currently the product leader in the electric automotive field, because they combine the highest powertrain and Wheel-to-Wheel efficiencies [3] with the ease of energy source

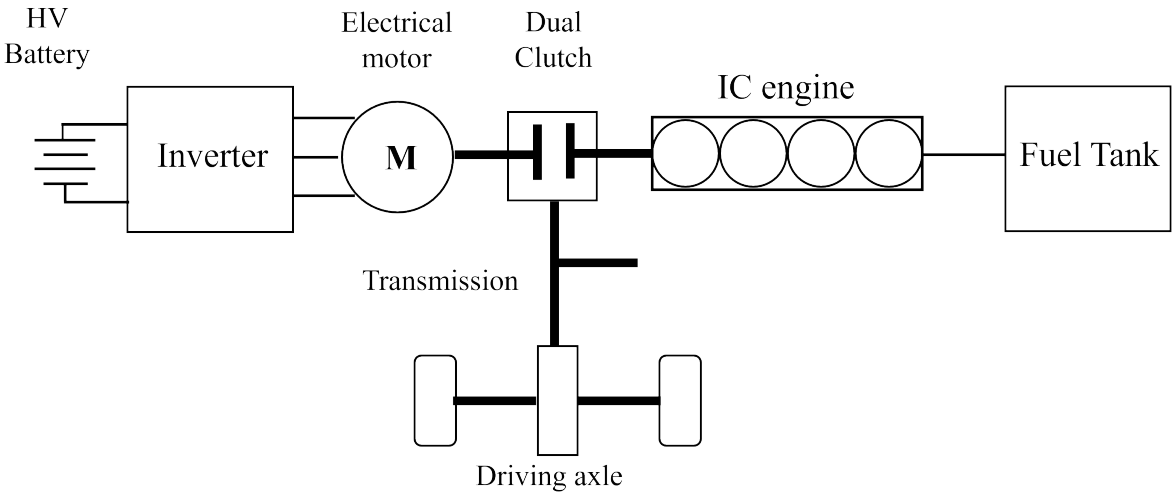


Figure 1.3: Series Hybrid Electric Vehicle structure.

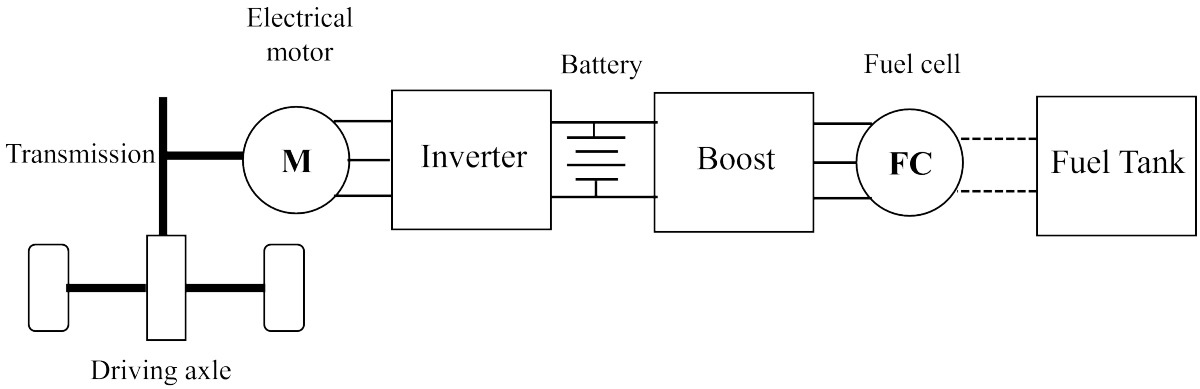


Figure 1.4: Fuel Cell Electric Vehicle structure.

management, with zero local emission. As shown in Fig. 1.1, in 2020, BEVs were the most produced with a final stock close to 9 millions.

On the other hand, BEVs spread is still hampered by several factors, the most important of which can be summarized in limited driving range autonomy, high costs for production and maintenance of the battery pack. The critical aspects are mostly related to the management of battery cells, because their energy still do not guarantee driving cycles comparable to ICEVs and the time required to charge them is not competitive compared to fuel refill.

Beside the possible improvements on the battery chemistry, important advantages can be

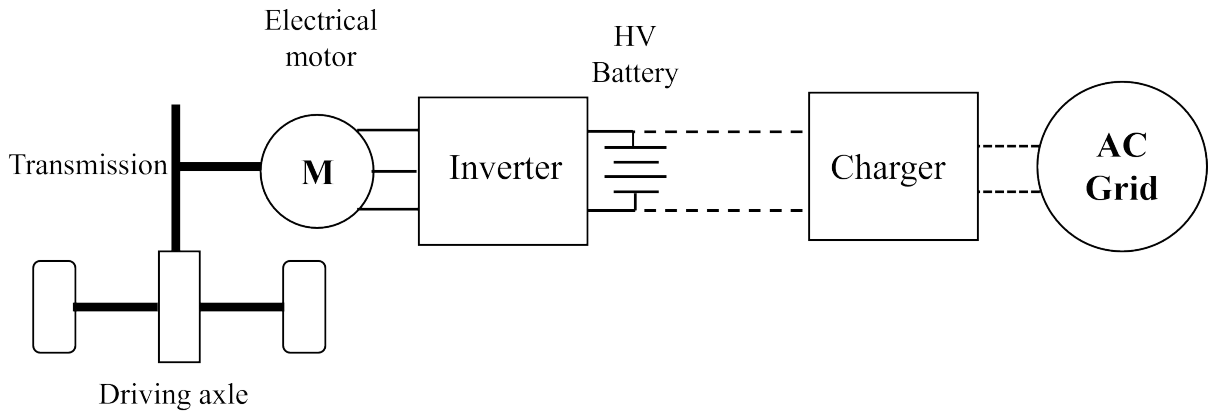


Figure 1.5: Battery Electric Vehicle structure.

obtained by optimizing the electrical circuits which regulate the energy conversion of the battery cell. As a matter of fact, for any type of EVs, an electronic converter is needed as link between the motor and the energy source. Both fuels and battery cells generate electricity in form of DC voltage, whereas the motor requires AC voltage. The conversion is performed by a DC/AC electronic converter, in charge of modifying not only the form of energy but also the voltage and current levels according to the torque and speed required from the propulsion system.

The electronic converter covers a strategic role in an electrical powertrain, by significantly affecting the overall system efficiency. Indeed, the converter operations affect the life duration of the motor - eventual high slope in output voltage bring to the reduction of the windings insulation - and the management of the energy source -, high converter losses and wrong utilization can lead to reduction of the driving range and, in case of BEVs, battery cell life cycle.

This dissertation finds its motivation in discovering new solutions in terms of converter topologies and optimization of the energy conversion process. Specifically for the BEVs, the new concepts of converter design leads to different battery cells configurations, aimed to improve the motoring phases, optimize the energy management and reduce the charging time. This research work is centred on the utilization of multilevel converters in EV powertrains. The main focus was the definition, study and realization of a new converter for a full electric BEV powertrain. The Reconfigurable Cascaded Multilevel Converter (RCMC) has been designed with the goals of

improving the management of the battery cells and increase the performance standards of the current powertrains.

1.2 Structure of the thesis

The dissertation is structured as it follows.

- The second chapter presents an excursus on power converters employed in EV powertrains. Specifically, the conventional two-level inverter topology is shown and described, in terms of architecture and possible modulations. However, the two-level inverter presents mainly two drawbacks consisting in efficiency drastic drops when working at partial load conditions and the necessity to have a fixed connection between the battery cells. Therefore, the chapter continues by describing the strategies developed to improve these aspects. The two corrective measures mostly suggested can be summarized in decreasing the overall losses due to the power devices and the insertion of a middle-stage DC-DC converter to control the battery pack voltage in a way that the two-level inverter can always work at nominal load.

  Although all developed strategies, the two-level inverter cannot accomplish with an optimum battery system management because the stiff connection within the battery pack still limits the efficiency at the weakest cell. Therefore, the studies did not only focus on the converter architecture improvements but on a general concept revision of the battery system to improve the energy conversion. New suggested topologies belong to the category of Multilevel Converters, which bring several benefits for both converter and energy system. The fixed battery pack is split in several modules, each of which is controlled by a dedicated and unique converter. The serial connection of these converters characterize one phase of Multilevel Converters. The modular structure allows to increase the DC link voltage and reduce the device stress, ensuring low current THD values and $\frac{dv}{dt}$ on the motor windings. Moreover, the disposition of the battery system over different modules and phases allows

to develop customized strategies to balance the battery modules and maintain under control the thermal distribution.

The latter approach is brought to its extreme, giving birth to the Reconfigurable Battery Systems, in which each cell can be accessed and individually managed to optimized the energy delivery and enhance fault tolerant strategies. The more is the degree of accessibility, the more is the system complexity. As matter of fact, the possibility of controlling each battery cell is guaranteed by placing a large number of switches and developing a detailed control architecture.

- The third chapter is focused on the description of the new topology - called Reconfigurable Cascaded Multilevel Converter (RCMC)- specifically developed in this Ph.D. project. The RCMC merges the functionalities of a power converter and a BMS, improving the battery system management and allowing an optimized energy conversion. Firstly, the basic operative functionalities of the converter are described and explained. The modulation strategy is described with a particular focus on the corrective actions taken for low voltage operative conditions. Then, an efficiency comparison between different architectures of the RCMC is carried out to optimize the topology and minimize the losses. Finally, the RCMC is compared with other three topologies in terms of battery and converter efficiencies to show its competitiveness with respect to the state of the art.

- The fourth chapter analyses the RCMC in three different case studies: motor drive, charging configuration and BESS application. For all three operative conditions, the applications background are explained and the simulation outputs are discussed.

- The fifth chapter faces the construction of one RCMC submodule. The new topology allows to access each cell by placing a coherent number of switches in the connection of the battery system. The high number of switches and the topology complexity significantly affect the design and concept of the RCMC. The control architecture is firstly described, followed by a detailed explanation of the PCBs design.

- The sixth chapter shows the experimental results. The RCMC is firstly used to power a RL load and, then, connected to an AC programmable power system to reproduce both motoring and regenerative phases. The battery cells voltages during discharging and charging processes are shown, to validate the features of the new converter. Moreover, voltage and current output waveforms of the converter are shown to prove the low THD values; the voltage and current of one battery cell are measured to show the insertion dynamics. Finally, the low voltage modulation is validated with experimental results.
- The seventh chapter concludes the dissertation, highlighting the results obtained and giving an overview on the future works.

CHAPTER

2 Literature Review

The powertrain assumes a key role in a vehicle, being responsible of creating power from the engine and transferring it to the wheels. In ICEVs, the powertrain is demanded to convert the thermal energy given by the fuel in kinetic energy in the engine and then deliver it via the transmission and driveshaft as torque to the wheels. In BEV powertrains, the energy is already an electrical energy whose form has to be transformed to correctly power the motor.

Fig. 2.1 shows the conventional scheme of a BEV powertrain, consisting in three main elements:

- the battery pack, intended as a fixed structure of serial and parallel connections of several battery cells, to reach the voltage and current ratings required by EVs application.
- the electronic converter, which is required to feature a bidirectional energy flow, performing both energy conversion DC/AC and AC/DC, in motoring and regenerative phases, respectively.
- the electrical motor, which usually in more modern solutions is represented by a permanent - magnet synchronous machine (PMSMs), because it fulfils the EV requirements of high power density, wide speed range and high reliability [7].

The converter topology mostly employed in traction application is the two-level Voltage Source Converter (VSC). BEVs application has inherited the two-level VSC from large drives in

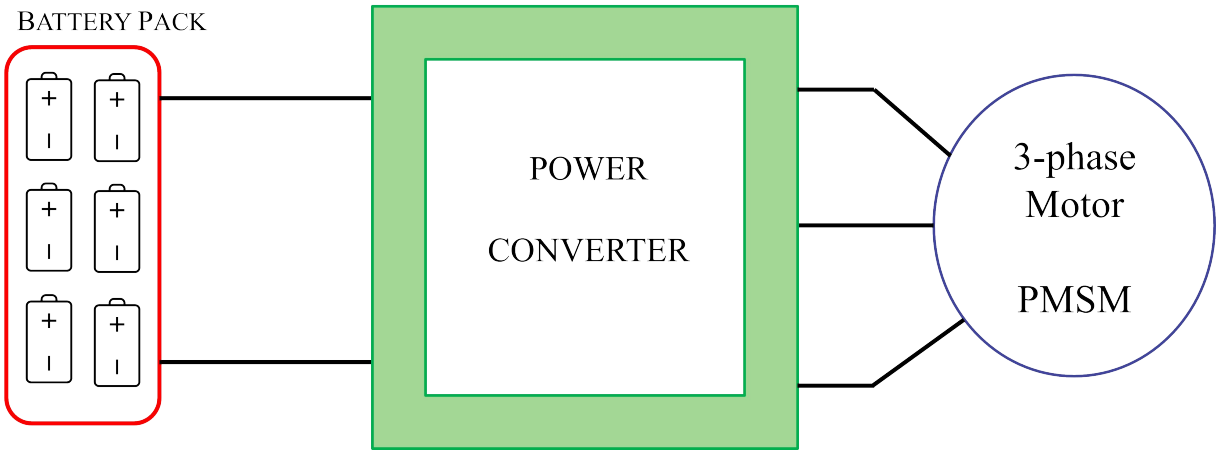


Figure 2.1: BEV powertrain scheme.

industrial applications, where this topology is widely used. The benefits of using a well-known topology are the possibility to be faster in terms of production and to have less development costs. Moreover, the two-level VSC has been widely investigated and studied under many aspects such as reliability, fault conditions, modulation strategies, etc.

2.1 Two-level VSC

The electrical schematic of the two level VSC is shown Fig. 2.2: it consists in three legs, formed by the serial connection of two switches; the AC output phase is placed between them. Each leg, also referred as pole, is connected to the positive and negative terminals of the DC source, whose voltage rating limits the output AC voltage. The term two-level identifies the two states that the AC pole voltage can assume according to the switches states, equal to 0V and the dc source voltage.

The pole voltages can be referred to the negative terminal of the DC source (N) or to the machine neutral (n), obtaining two voltage sets *vAN*, *vBN*, *vCN* and *van*, *vbn*, *vcn* respectively. The pole voltage referred to N can be either equal to V_{dc} or 0, if the upper or lower switches are turned on, respectively. Therefore, the output voltage of each pole to N can be considered DC biased of a value equal to $\frac{Vdc}{2}$; conversely, when they are applied to the three-phase motor, the net

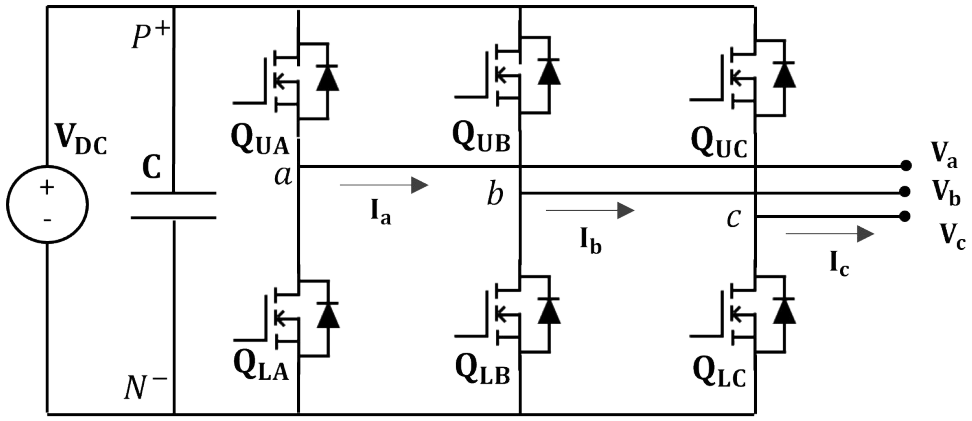


Figure 2.2: Two-level VSC.

effect cancels the dc bias and both the line and phase voltages delivered to the motor are purely AC. Each switch is paired with a body diode to permit the reverse current capability [5].

The modern electric drives are supplied with PWM waveforms, obtained with appropriates modulation strategies. In the next section, the Sinusoidal Pulse Width Modulation (SPWM) and the Space Vector Modulation (SVM) will be described.

2.1.1 Sinusoidal PWM

The SPWM uses three sine waves - usually obtained as output of a feedback control loop -, with 120° phase difference with each other, and a high frequency triangular carrier to generate constant amplitude pulses with different duty cycles. The gate signals are obtained by comparing a sinusoidal wave, one for each leg, with the triangular carrier: the switch is turned on if the sine wave voltage is greater than carrier, otherwise it is turned off. The comparison result is a stream of pulses which determines the duty cycle of the upper and lower switches. Fig. 2.3 shows the SPWM signal generation technique for three-phase VSC. The frequency of the sine waves and the triangular carrier are chosen according to the required output and switching frequency of the VSC, respectively.

The following theoretical discussion represents the average modelling of the two-level inverter and only the signal at the fundamental frequency is considered. The pole voltages referred to N

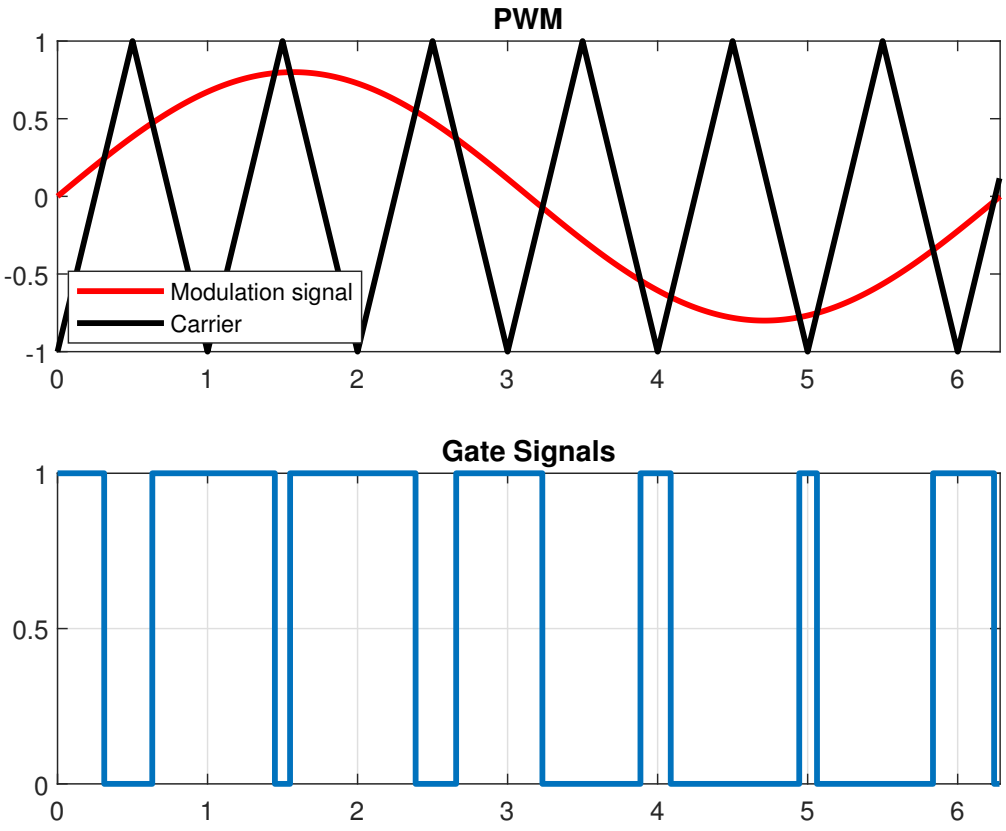


Figure 2.3: PWM modulation.

oscillate sinusoidally between $0V$ and V_{dc}:

$$v_{aN} = \frac{V_{dc}}{2} + \sqrt{2}V_p cos(\theta) \tag{2.1}$$

$$v_{bN} = \frac{V_{dc}}{2} + \sqrt{2}V_p cos(\theta - \frac{2\pi}{3}) \tag{2.2}$$

$$v_{cN} = \frac{V_{dc}}{2} + \sqrt{2}V_p cos(\theta - \frac{4\pi}{3}) \tag{2.3}$$

where V_p is the rms value of the pole voltage. In a balanced three-phase system, the neutral of the

motor is equal to half of the dc link voltage:

$$V_{Nn} = \frac{V_{dc}}{2} \tag{2.4}$$

Therefore, the phase voltages insisting on the motor are equal to:

$$v_{an}(\theta) = v_{aN}(\theta) - V_{nN} = \sqrt{2}V_p cos(\theta) \tag{2.5}$$

$$v_{bn}(\theta) = v_{bN}(\theta) - V_{nN} = \sqrt{2}V_p cos(\theta - \frac{2\pi}{3}) \tag{2.6}$$

$$v_{cn}(\theta) = v_{cN}(\theta) - V_{nN} = \sqrt{2}V_p cos(\theta - \frac{4\pi}{3}) \tag{2.7}$$

Being the phase-to-neutral peak value maximum equal to the half of the dc link voltage:

$$\sqrt{2}V_p = \frac{V_{dc}}{2} \tag{2.8}$$

The maximum phase-to-neutral voltage will be equal to:

$$V_p = \frac{V_{dc}}{2\sqrt{2}} = 0.354V_{dc} \tag{2.9}$$

The duty cycle can be written as:

$$d(\theta) = \frac{V_p(\theta)}{V_{dc}} \tag{2.10}$$

By substituting the equation of the pole voltages (2.1) -(2.3) it is possible to determine the equation of the duty cycle for each phase:

$$d_a(\theta) = \frac{1}{2} + \frac{\sqrt{2}V_p}{V_{dc}} cos(\theta) \tag{2.11}$$

$$d_b(\theta) = \frac{1}{2} + \frac{\sqrt{2}V_p}{V_{dc}} cos(\theta - \frac{2\pi}{3}) \tag{2.12}$$

$$d_c(\theta) = \frac{1}{2} + \frac{\sqrt{2}V_p}{V_{dc}} cos(\theta - \frac{4\pi}{3}) \tag{2.13}$$

The fundamental VSC output voltage can be increased by adding a third harmonic to the SPWM. The phase voltage increases of the factor $\frac{1}{cos(\frac{\pi}{3})}$, which results in 1.1547 times higher than the conventional SPWM. The key parameter used to define the peak phase voltage in relation to the half of the DC voltage is called modulation index m:

$$m = \frac{\sqrt{2}V_{ph}}{\frac{V_{dc}}{2}} = \frac{2\sqrt{2}V_{ph}}{V_{dc}} \tag{2.14}$$

2.2 Space Vector Modulation

The Space Vector Modulation (SVM) is a digital pulse-width modulation technique. The theoretical analysis starts with the assumption that any three-phase system (i.e. $a_x(t)$, $a_y(t)$, $a_z(t)$) can be represented with a unique rotating vector a_s:

$$a_s = \frac{2}{3}[a_x(t) + \underline{a}a_y(t) + \underline{a}^2 a_z(t)] \tag{2.15}$$

where $\underline{a} = e^{j\frac{2\pi}{3}}$ and $\underline{a}^2 = e^{j\frac{4\pi}{3}}$.

For a three-phase system, the vectorial representation can be written as:

$$\begin{bmatrix} A_\alpha \\ A_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{-1}{\sqrt{2}} & \frac{-1}{\sqrt{2}} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} a_x \\ a_y \\ a_z \end{bmatrix} \tag{2.16}$$

where (A_α, A_β) are the components of the representation of a vector in a complex plane, as

$\underline{a}_s = A_\alpha + j \cdot A_\beta$. The reverse transformation can be written as:

$$a_x(t) = Re|a_s| + a_0(t) \tag{2.17}$$

$$a_y(t) = Re|\underline{a}^2 \cdot a_s| + a_0(t) \tag{2.18}$$

$$a_y(t) = Re|\underline{a} \cdot a_s| + a_0(t) \tag{2.19}$$

where $a_0(t) = \frac{1}{3}[a_x(t) + a_y(t) + a_z(t)]$ represents the homopolar component. The final results is the unique correspondence between a three-phase system and a Space Vector representation. Excluding the simultaneous conduction of switches belonging to the same leg, the switching states of the two-level converter define eight configurations, shown in Table 2.1. The six vectors have a magnitude of $\frac{2}{3}V_{dc}$ and present a phase displacement equal to $\frac{\pi}{3}$, while the remaining two are equal to zero. The graph is shown in Fig. 2.4 (a). In the frame $\alpha\beta$, the voltage vectors draw a hexagon, as shown in Fig.2.4 (a). Each point within the area drawn by the hexagon represents one feasible output voltage of the two-level inverter. Taking Fig. 2.4 (b) as reference, the voltage output Vs can be obtained as result of combination and discretization of the eight known vectors.

Table 2.1: Switching state configuration.

Conf	ON	OFF	V_{aN}	V_{bN}	V_{cN}	V_{an}	V_{bn}	V_{cn}
0	QLa, QLb, QLc	QUa, QUb, QUc	0	0	0	0	0	0
1	QUa, QLb, QLc	QLa, QUb, QUc	V_{dc}	0	0	$\frac{2}{3}\ V_{dc}$	$\frac{1}{3}\ V_{dc}$	$-\frac{2}{3}\ V_{dc}$
2	QUa, QUb, QLc	QLa, QLb, QUc	V_{dc}	V_{dc}	0	$\frac{1}{3}V_{dc}$	$\frac{1}{3}V_{dc}$	0
3	QLa, QUb, QLc	QUa, QLb, QUc	0	V_{dc}	0	$-\frac{2}{3}V_{dc}$	$\frac{2}{3}V_{dc}$	$\frac{1}{3}\ V_{dc}$
4	QLa, QUb, QUc	QUa, QUb, QLc	0	V_{dc}	V_{dc}	0	$\frac{1}{3}V_{dc}$	$\frac{1}{3}V_{dc}$
5	QLa, QLb, QUc	QUa, QUb, QLc	0	0	V_{dc}	$-\frac{1}{3}V_{dc}$	$\frac{1}{3}V_{dc}$	$\frac{2}{3}V_{dc}$
6	QUa, QLb, QUc	QLa, QUb, QLc	V_{dc}	0	V_{dc}	$\frac{1}{3}V_{dc}$	$-\frac{2}{3}V_{dc}$	$\frac{1}{3}V_{dc}$
7	QUa, QUb, QUc	QUa, QUb, QUc	V_{dc}	V_{dc}	V_{dc}	0	0	0

2.3 Further improvements of 2-level VSC in electrical powertrain

The two-level VSC performance has been widely studied to investigate the topology weaknesses and, possibly, improve them. In general, the two-level VSC efficiency strictly depends on the operative power conditions. In industrial applications, where drives are required to work mostly at nominal load, a two-level inverter made of Si IGBTs reaches 97% of efficiency; the same values are obtained for BEVs powertrain application when speed and torque required coincides with the nominal system ratings [8].

However, the energy demand of an EV fluctuates with the driving cycle ranges, which often require low or medium load conditions. Being all electronic devices designed to minimize the losses at nominal loads [9], the efficiency of the VSC drops for partial loads, reaching minimum values equal to the 80% [10]. According to [11, 12], the overall efficiency of a two-level VSC ranges between 85% and 90% in comprehensive driving cycles - i.e. WLTP (Worldwide harmonized Light vehicles Test Procedure) or NEDC (New European Driving Cycle)

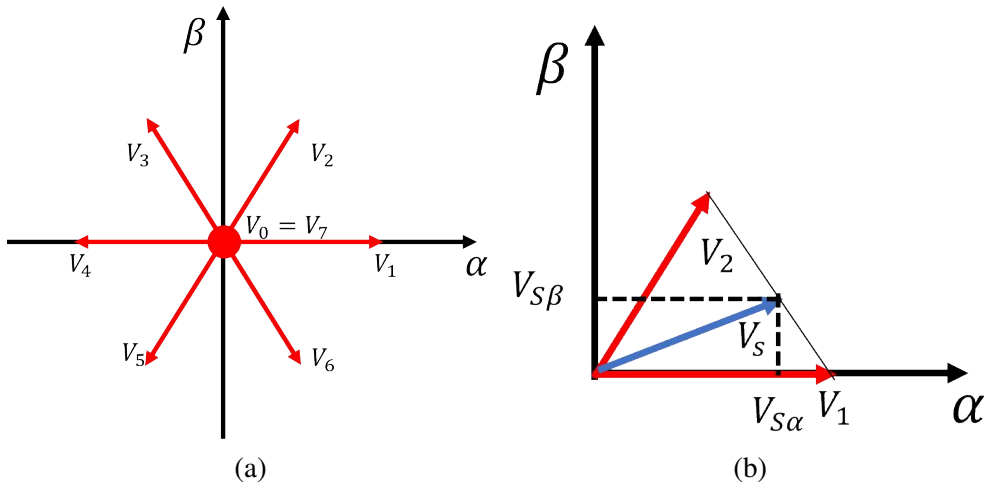


Figure 2.4: (a) The eight configurations defined by the switching states. (b) Voltage discretization with SVM.

cycles, which are the global and european standards to assess the CO_2 emissions of one vehicle, respectively [13]. Therefore, the enhancement of the two-level efficiency in BEVs powertrain has been investigated by focusing the attention on partial loads operations.

Many studies have been focused on analysing all factors contributing to the converter efficiency. The aspects mainly investigated were the reduction of the power losses due to the switches and the insertion of an extra middle stage converter to modify the operative ranges of the two-level inverter.

2.3.1 Power losses reduction

Many strategies have been developed to reduce conduction and switching losses. As an example, in [14] the authors propose to connect several IGBTs in parallel to vary the active chip area during the working operation. The losses minimization can be achieved by increasing the number of active IGBTs during the nominal load operation - when the conduction losses are prominent over the switching losses - and reduce active area during the partial load - when the switching losses outweigh the conduction losses. Other studies recommend the substitution of IGBTs with wideband gap based devices, mostly SiC MOSFETs to improve the efficiency. Indeed, [15–17], authors carried out efficiency analysis on various driving cycles claiming the reduction of the switching losses of an amount which ranges between 50% and 80%. The reduction of power losses allows to design converters with higher energy density and compact cooling systems thanks to the drop of the operating temperature. However, the utilization of SiC MOSFETs is still debated because of the high production costs and their reliability. Indeed, since the conventional qualification tests are not sufficient to determine eventual failure in SiC technology, more protocols are in definition to match the different physical properties [18].

2.3.2 Insertion of a middle stage converter

Together with the optimization of devices operation, the improvement of the efficiency at partial loads has been found to be possible by varying and controlling the inverter supply voltage.

Specifically, several studies have proposed the insertion of a middle-stage bidirectional DC/DC inverter, either a boost or buck-boost, between the battery pack and the VSC inverter, as shown in Fig. 2.5.

The majority of the research works adopts a bidirectional DC/DC boost converter to implement a variable voltage-control. In [19], the authors present the advantages of the new system consisting in the increase of the power outputs without modifying the battery pack size and the minimization of the power losses by adjusting the working point of the motor. Basically, the insertion of the DC/DC converter allows to design independently the battery pack and the inverter, gaining in system flexibility and production costs [20].

The supply voltage is strictly dependent on its back electromotive force (EMF) - the EMF is equal to the supply voltage subtracted by the voltage drop on the armature resistance -, which is proportional to the operating speed. Therefore, the voltage required to the battery pack increases with the speed range of the motor. The introduction of the DC/DC converter allows to design the battery pack to guarantee only the supply voltage for low machine speed range and boost it to manage the high speed range. For intermediate speed ranges, the DC/DC converter can be controlled in order to output a variable voltage in accordance with the motor speed. Fig. 2.6 shows the required voltage over the mechanical speed. Specifically, the variable-voltage control can be implemented to keep the modulation index equal to specific reference values, taken large enough, to reduce the harmonic distortion and increase the overall efficiency. [21] carried out an efficiency comparison between a two-level VSC and a two-level VSC connected to a DC/DC boost converter, by analysing both motoring and regenerative braking conditions in different speed ranges. The simulation results show an effective improvement on the overall system efficiency, confirmed by experimental tests.

However, the adoption of an extra DC/DC converter may create many disadvantages: the insertion of extra active and passive components - electronic devices, inductors and capacitors - leads to the generation of additional power losses, the increase of the overall size of the powertrain and eventual reliability issues. Many research works have appeared in the scientific literature

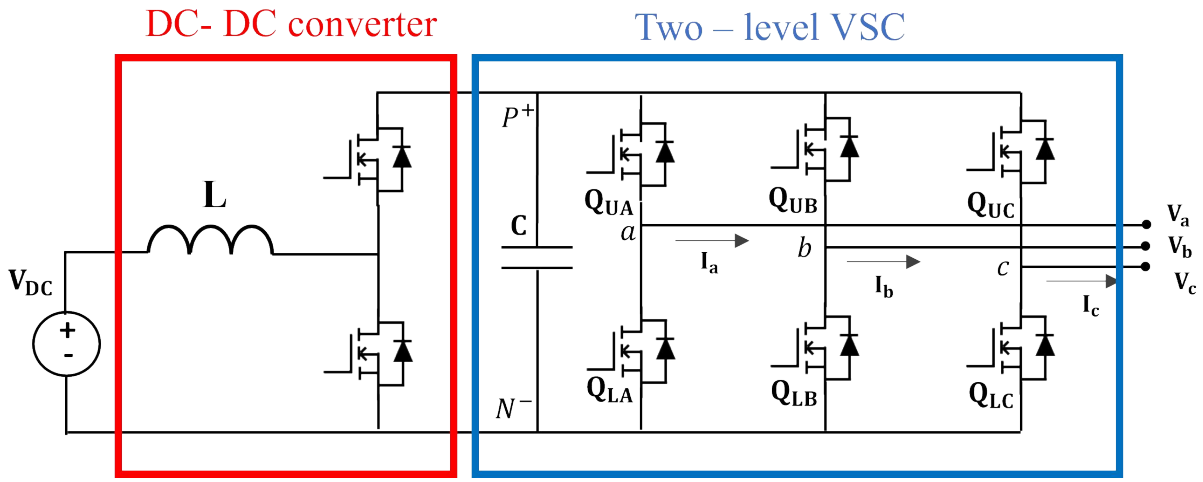


Figure 2.5: Architecture DC/DC converter connected with a two-level inverter.

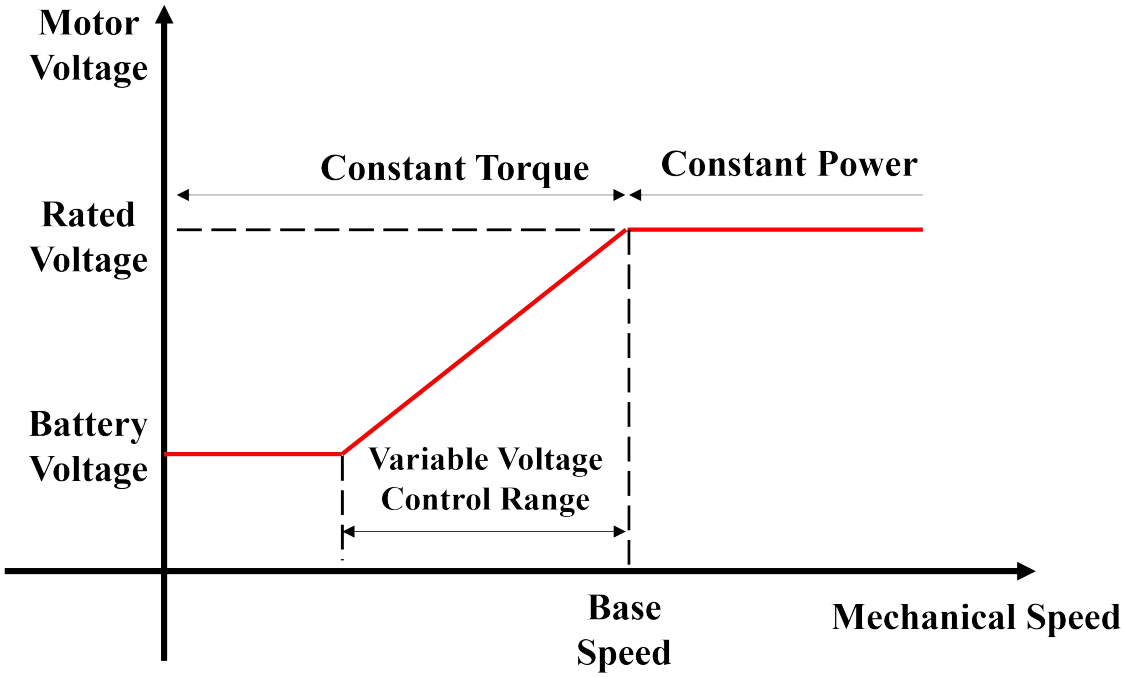


Figure 2.6: Voltage speed characteristic curve for a PMSM.

aiming the improvement of the efficiency of the DC/DC converter and they can be categorized in:

- Soft-Switching approaches, such as Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS), aiming to drastically reduce the switching losses, which represent a

substantial contribution to the overall losses. In SAZZ (Snubber Assisted Zero voltage and Zero current transition) approaches, the DC/DC converter is equipped with an auxiliary snubber circuit which nails to zero the turn on losses and significantly reduces the turnoff losses [22].

- Parallel interleaved converters and coupling inductors approaches are adopted to reduce magnetic losses and eventually switching losses [23]. Interleaving is a technique that uses multiple switching converters connected in parallel to an input and output bus. Interleaved DC/DC converter reduces the rms current flowing in the capacitors, with consequent reduction of the switching losses and passive components size and ratings.

- Three-level converters [24] approaches aim to reduce the voltage rating of the electronic devices by a factor of 2. Moreover, the reduction of inductor volt-seconds brings to halv the switching frequency. As a consequence, the inductor size can be also reduced.

- Z-source inverter [25] approaches combine the DC/DC converter and inverter functionalities. Its equivalent DC/DC stage is capable of producing higher or lower voltage outputs, allowing a wider voltage control.

- Composite Converter architecture [26] approaches are introduced to split the energy conversion process in different stages, each of them assigned to a dedicated low power converter module. All converters are cascaded connected to form the overall conversion system. The composite structure allows to optimize independently the single module, resulting in efficiency improvements over different ranges of operating conditions.

2.3.3 Management of the battery system

However, the insertion of a middle-stage converter does not completely solve the problem related to the battery pack operative conditions. Despite of the improvement of the VSC performance, the traditional multi-cell battery systems still have some significant issues. The recurring

phenomenon of the unbalanced voltages within the cells connected in series, due to internal chemical processes which determine different dynamic behaviours [27], negatively affects the energy exchange rate. Battery cells connected in series share the same charging/discharging current; the different intrinsic characteristics may lead to the case in which one battery cell is getting charged/discharged faster than the others. For safety reasons, battery cells cannot operate above/below their maximum/cut-off voltages, therefore, when one weak cell is fully charged/discharged, the entire string, to which it belong, has to be excluded from the operations. Since EV battery packs usually have several strings connected in parallel, if one cell is much weaker than the others, the exclusion of one string from the charging/discharging process means the complete interruption for the overall battery system. Furthermore, the chemical intrinsic difference of the battery cells emphasize as the utilization rate of the battery pack increases [28]. Specifically, in EV application, since discharging and charging cycles are requested on daily basis, cell unbalances phenomena cover one of the most critical aspect of energy system management.

As a result, a system control unit, also called battery management system (BMS), is used to regulate the operating conditions of the battery systems. BMSs are responsible not only for cell balancing but also for temperature monitoring, voltage and current acquisitions, ageing issues and, more in general, for detecting any abnormal conditions at infrastructure level [29]. BMSs cover a fundamental role in the energy conversion management and their architectures varies as the internal connection of the battery system varies; in [30], several examples of BMS technologies employed in EVs are presented.

In general, the basic architecture for BMSs in EVs is a master-slave scheme, where the sub-controllers directly monitors and operates on a determined group of cells and then send the information to the main controller, as shown in Fig. 2.7. According to the method used to perform the balancing process of the group of cells, the BMS structure can be categorized in passive and active [31]. Passive BMSs achieve the balancing by removing excess energy from the higher voltage cell by connecting either a fixed shunt resistor [32] or a controlled balancing resistance [33]. Active BMSs, instead, transfer the energy in excess from the most charged cells to the

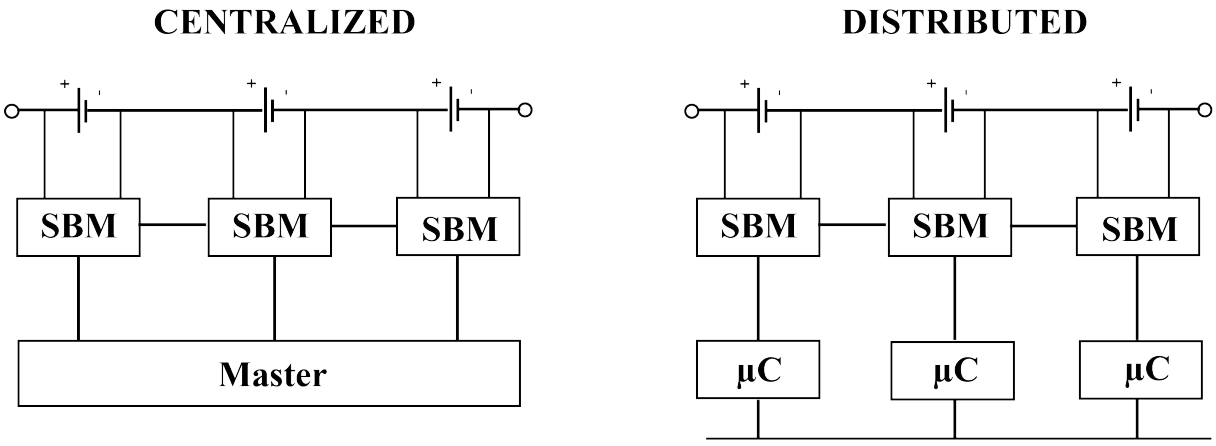


Figure 2.7: BMS architectures: centralized - implemented with one master controller and several slave controllers - and distributed - each unit is equipped with a microcontroller.

less charged ones by auxiliary circuits made of inductors and capacitors [34]. The advantages of passive BMSs consist in easy implementation and management, lower costs and smaller sizes. Nevertheless, excess charge is dissipated as heat, resulting in low energy efficiency and eventually creating hot-spot within the battery pack. Conversely, active BMSs higher efficiency is achieved by increasing the components costs and the management complexity [35]. As an example, in [36], a passive and an active BMSs are compared showing a higher efficiency for the second one at the expense of a lower equalization dynamic and a more complex structure.

The local management of battery cells is becoming increasingly important given the choice of the automotive companies to increase the voltage rating of their battery packs up to 800 V. As examples, Aston Martin E is equipped with a 800 V battery pack [37], Lucid Air will use 900 V batteries [38], while Hyundai announced that they will enable 800 V systems in their EVs [39]. Indeed, having higher voltage battery pack allows to reduce the size and weight of the power cables, the charging time [40] and the motor currents, improving the overall system efficiency [41].

However, the benefits mentioned are accompanied by new challenges regarding the power electronic and the control units. Even if the current reduction leads to lower conduction losses, higher voltage contributes to higher switching losses if the conventional two - level VSC is used

[42]. Moreover, the avoidance of cell unbalances assumes a critical role, in order to not loose the high efficiency energy delivery related to higher voltage battery and to not provoke consequent thermal issues. Indeed, abnormal increase of temperature may be caused by overcharge and overdischarge phenomena. The worst case scenario is represented by the so called thermal runaway, when the temperature increase of one battery cell generates a chain reaction for which the other battery cells start to increase the temperature too. In this conditions, the operation must be stopped. Therefore, the higher is the number of battery cells serially connected, the more sophisticated is the BMS architecture required. Furthermore, the utilization of passive BMSs may compromise the already unstable thermal situation, in case either the number of battery cells to be discharged is large or the power in excess is significant.

As a consequence, the research works, described in this thesis, started to focus on structural change of the EVs converter. The basic concept was to make the battery pack a flexible structure, dividing it in more modules. In this way, the voltage rating of the equivalent battery pack may increase without increasing the devices voltage ratings. Moreover, the battery cells management can be divided in more stages, allowing better performances and enhancing fault detection and ride-through strategies. Overall, the necessity of improving the battery management finds its motivation also in the high production and maintenance costs of the energy system, which constitutes the highest fraction of BEV powertrain cost.

In late 1990s, Multilevel Converters (MCs) started to be suggested as valid candidates for EV powertrain, because their structure allows to split the conversion processes in smaller stages keeping high efficiency standards and guaranteeing low THD current values. In automotive applications, the employment of MCs allows to divide the battery pack in several modules, each of which associated to one stage. Moreover, the equivalent DC link can be increased indefinitely without having strict necessities on the devices voltage ratings, because each device faces the power related to its own stage.

Later on, when battery system storages became strategic also for grid applications, the necessity of performing active strategies moved the research area to reconfigurable battery

systems (RBSs), which provide accessibility to each battery cell of the original battery pack. Despite of the complex structures, RBSs are providing large room for improvements in energy system management.

2.4 Multilevel Converters

The adjective ”Multilevel” is referred to the unique structure of these topologies, which are able to synthesize a desired output voltage from several levels of DC voltages. The possibility to divide the unique DC source in multiple sources makes the Multilevel Converters (MCs) highly recommended for medium and high power applications [43]. Each source is connected to a dedicated converter, whose main role is to insert or exclude it from the operation, according to the converter control. These converters are serially connected, creating a modular and redundant structure, adding the possibility to enhance the fault detection and ride-through strategies. Moreover, the multilevel structure allows to span the overall DC link voltage on the several electronic devices connected in series, decreasing in this way their required voltage rating. The more are the converters serially connected, the more are the levels and the more are the output voltage steps which generate a staircase shape.

The characteristics above described permit to reduce the $\frac{dV}{dt}$ on the output voltage and the switching frequency, usually root causes of motor bearing failures and large switching losses, respectively. The most known MC topologies employed in traction application are described in [44], with an exhaustive discussion of their advantages and disadvantages. However, the field of choice is reduced for EVs applications, where high reliability, limited size and weight and modularity are favoured. Therefore, the research works focused mainly on two topologies - Modular Multilevel Converter (MMC) and Cascaded H-Bridge (CHB) -, which will be described in details in the next subsections.

2.4.1 Modular Multilevel Converter

The basic structure of a three phase MMC is shown in Fig. 2.8. The DC source is connected in parallel to three phases; each phase, also called leg, consists in a serial connection of several submodules (SMs), distributed among two arms- the upper and the lower arms, respectively - connected via two inductors. The AC terminal is placed between the two arms. The structure of each SM can be decided according to different requirements; between all the possible SM architectures [45], the most widely adopted for traction application are the half-bridge or the H-bridge converters, shown in Fig. 2.8.

Before being considered valid candidates for electric transportation, MMCs found its core application in HVDC. In this case, each SM is equipped with a floating capacitor, which represents one elementary voltage level. The modular structure allows to extend the voltage levels without any limits, by simply adding more SMs to each leg. In practice, the maximum number is decided in accordance with power losses and control complexity requirements. Despite of these limits, the MMC is much more efficient and more reliable than the two level VSC. The efficiency improvements are related to the possibility of reducing the switching frequency and still keeping low THD current waveforms. The higher reliability is achieved thanks to the redundant design, reduced stress on electronic components and possibility to use medium voltage semiconductors for high power applications. Furthermore, the redundant structure allows to implement fault-tolerant strategies in order to not interrupt the converter operation even in case of faulty conditions.

The benefits above mentioned make the MMC a suitable topology also for EVs application. In [46] and [47], the authors propose a MMC topology with integrated battery cells: the DC voltage is not anymore connected as external source but it is synthesized directly from the appropriate management of the SMs. The new topology and the correspondent submodule are shown in Fig. 2.9. Specifically, the MMC assumes the functionalities of both the 2-level VSC and BMS, by installing one battery cell in each submodule in order to combine the energy conversion with the battery management. In [48], an efficiency assessment of the MMC is carried out by comparing its performances with the two level VSC: the final results show a predominant position for the

MMC for the light load operations. Furthermore, the MMC can balance the battery cells for an initial 30% imbalance; conversely, the two level VSC still needs the BMS actions to achieve the same result.

Neglecting the issues related to negative sequence of the circulating currents and the voltage ripple on the submodules [45], the main drawback of this topology lies on the available AC output voltage. As an example, in [46] the MMC is controlled in order to keep constant the voltage between the positive and negative busbars; therefore the two arms in each leg activates a complementary number of submodules. The two reference voltages for the top and the bottom v_{rt} and v_{rb} arms- valid for any phase- referred to the phase voltage v_p can be written as:

$$v_{rt} = \frac{V_{arm\_max}}{2} - v_p \tag{2.20}$$

$$v_{rb} = \frac{V_{arm\_max}}{2} + v_p \tag{2.21}$$

It is possible to calculate the phase voltage as:

$$\frac{V_{arm\_max}}{2} \leq v_p \leq -\frac{V_{arm\_max}}{2} \tag{2.22}$$

Therefore, the maximum phase voltage v_{p_max} is equal to half of the arm voltage. In other words, the load peak voltage is equal to one fourth of the voltage installed within one phase. In terms of costs, this limitation can be overcome considering that the battery cells capacity is halved compared to the load rating, being the current contributions equally divided between the top and bottom legs. On the other hand, under the same conditions of power and voltage, the current rating of the motor fed by the MMC may double compared to the value required by the two-level VSC.

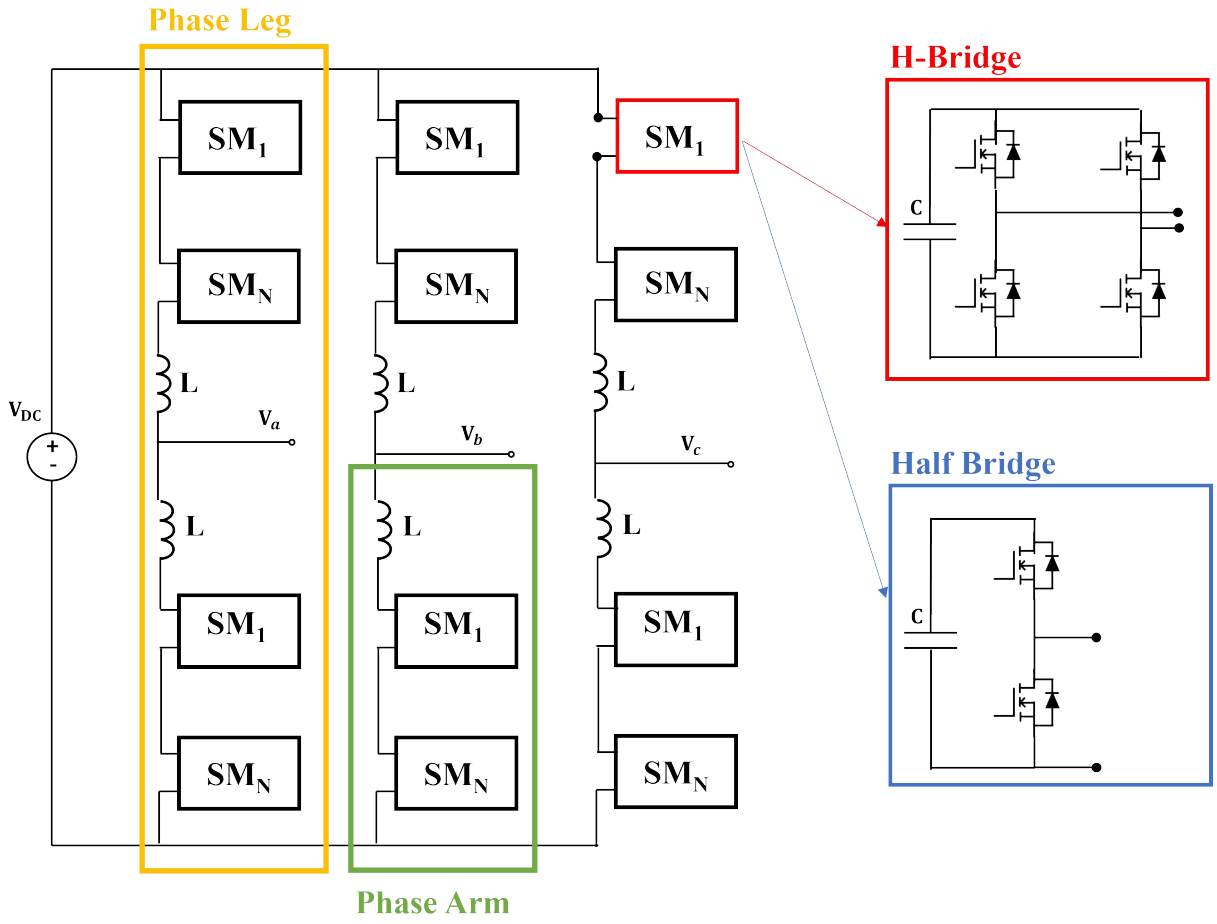


Figure 2.8: Modular Multilevel Converter with two submodules topologies: H-Bridge and Half-Bridge.

2.5 Cascaded H-Bridge

The basic structure of a three-phase CHB is shown in Fig. 2.10. Each leg is characterized by the serial connection of several SMs, which consist in full-bridge converters. The phases of the motor are directly connected to the CHB phases, without extra passive components. In this case, whether the CHB is employed for grid or EV applications, the independent DC sources are distributed among the SMs. The adoption of the bidirectional full-bridge converters allows to obtain three voltage levels for each SM, as shown in Fig. 2.11. As a consequence, in contrast to MMC, the

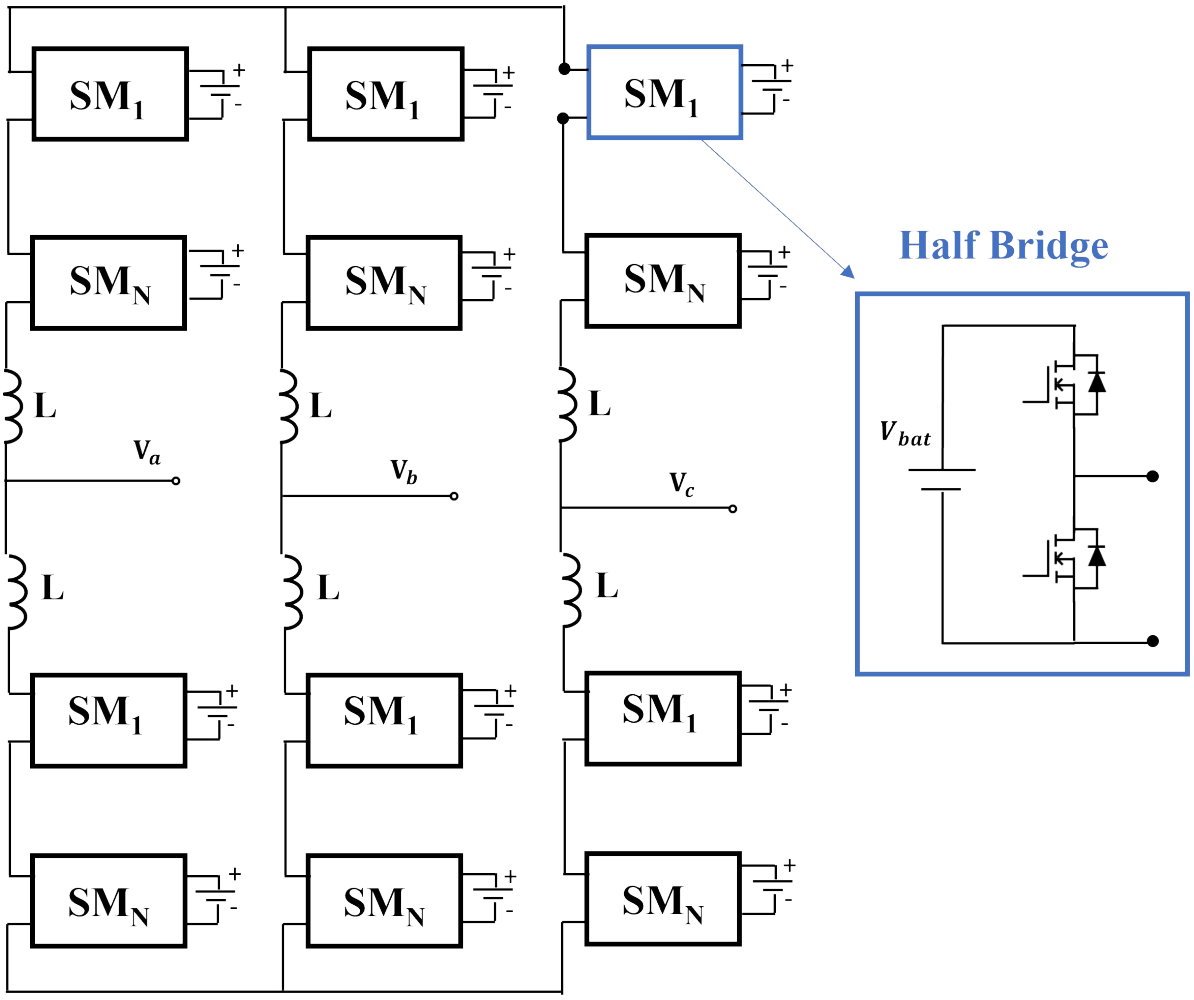


Figure 2.9: Modular Multilevel Converter used for EV powertrain.

peak of the sinusoidal output wave corresponds to the sum of the voltages installed within one phase. Specifically, if ds is the number of dc sources per phase, the CHB can synthesize an output voltage waveform with a number of levels n equal to $2ds+1$ with a peak voltage equal to nV_{dc}, where V_{dc} is the voltage of each DC source.

The CHB was suggested for large electric drives the first time in 1998, in [49]. The authors developed a 11-level converter controlled with a staircase modulation obtaining higher efficiency compared to PWM inverters, less stress for the devices and no voltage sharing problems. Since then, several research works proposed the CHB as valid candidate for traction application: in

[50], the CHB is used in a HEV powertrain and operates in order to manage the DC sources in a balanced way; in [51], a five-level CHB driver with charge equalizer functionalities is presented; in [52], the authors present a numerical and experimental analysis for the CHB in automotive application, highlighting the benefits of improving the battery management, output waveform and thermal distribution. It is important to remark the work presented in [53], where a 7-level CHB is compared with the two level VSCs - built with IGBTs and SiC MOSFETs, respectively- in terms of efficiency, costs analysis and influence on the powertrain design. The final results show that the CHB is more efficient at partial load and mantain comparable efficiency values at full load. Moreover, even if the cost of the converter may be higher compared to the two-level VSC, the better management of the battery system allows to increase the driving range, decreasing the overall cost of the powertrain. In terms of volume, the two-level VSCs are the favourite topology. On the other hand, the modular structure of the CHB allows to place the submodule on the battery module heat sink, increasing the height of the battery pack of only 1-2 cm.

However, the CHB topology have some issues which undermine its validity for EV application. First of all, the battery management improves as the number of submodules and the consequent amount of power electronics increases. Nevertheless, in [54] an optimization analysis shows that the best number of submodules per phase ranges between 3 and 4. Therefore, it is not feasible keeping high efficiency standard and completely remove the BMS functionalities. Moreover, in contrast to MMC, which allows the charging process either from AC and DC chargers [46], the three-phase CHB is preferred for charging processes from AC sources. This limitation covers a critical point, considering that many of the fast charging and ultra fast charging infrastructures provide DC voltage and current [55].

2.5.1 Modulation strategies

The modulation strategies for both MMC and CHB lies on the same concept, which are then exploited in different ways according to the topology needs. For both converters, the Space Vector PWM is feasible but the larger are the voltage levels, the more are the possible switching

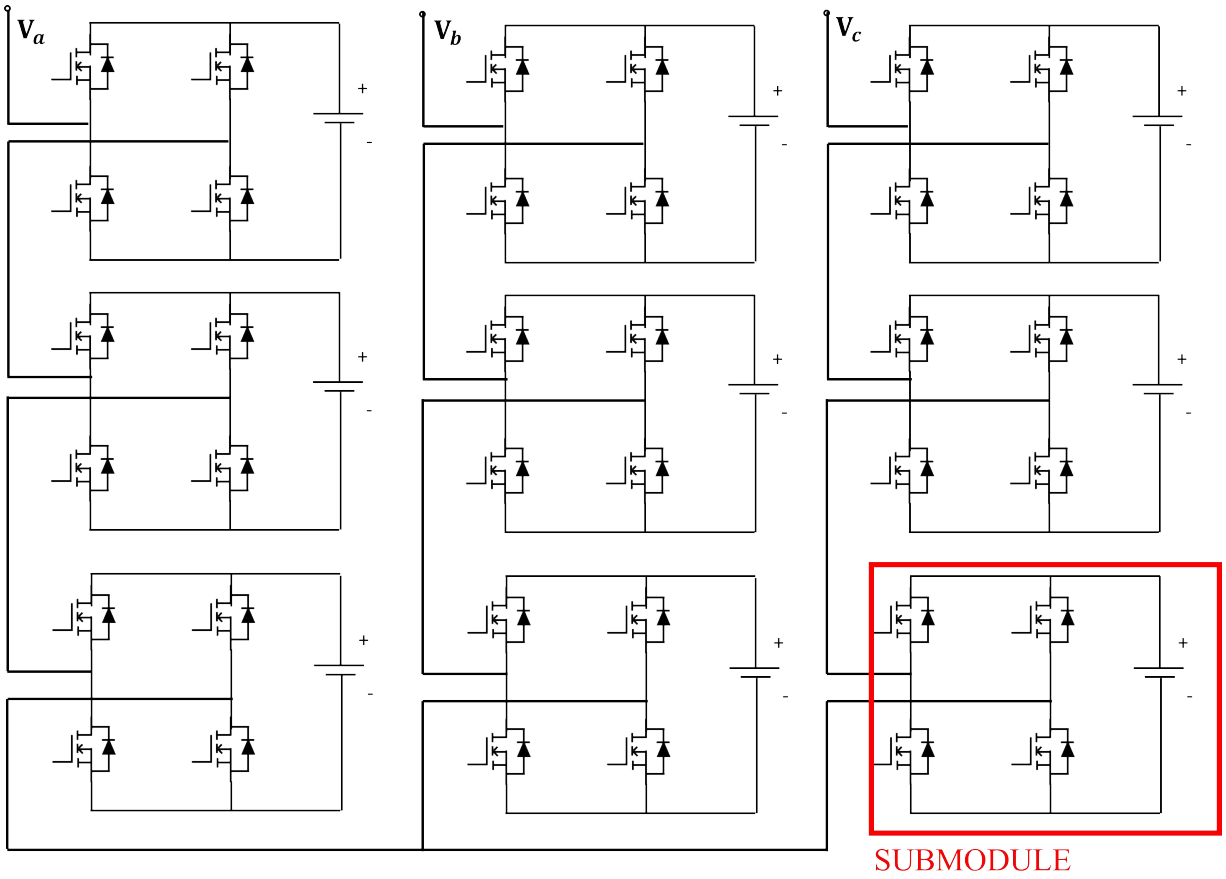


Figure 2.10: Cascaded H-Bridge topology.

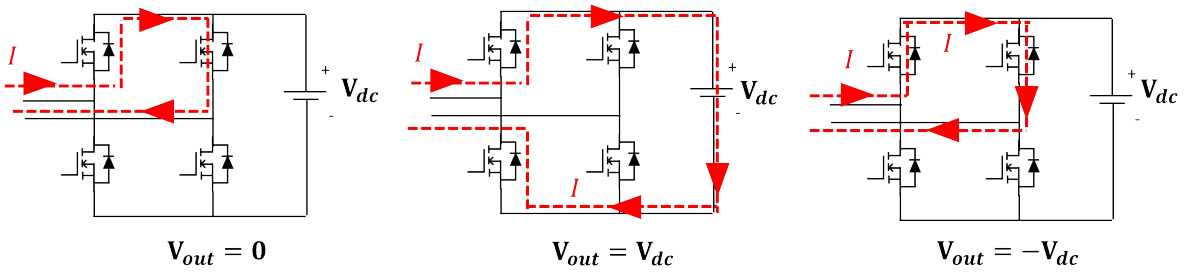


Figure 2.11: H-Bridge configurations to obtain the three output voltage levels: 0 V, + V_{dc}, - V_{dc}

states. Usually, the number of possibilities is too high, therefore, other PWM techniques and different strategies have been studied.

During 1990s, in [56] the first PWM technique suitable for multilevel converters was presented. The idea is to adopt one modulation signal - per phase - and a number of carriers equal to $N_{level} - 1$

where N_{level} is the number of the total voltage levels. The authors considered three subspecies of modulations determined by the carrier dispositions: the Alternate Phase Disposition (APOD), where the carriers are alternatively in opposition; the Phase Opposition Disposition (POD), where the carriers are in phase disposition of the positive in opposition with the phase disposed negative; the Phase Disposition (PD), where all carriers are in phase. These techniques were developed for the CHB, where the voltage sources are separated. In the MMC, instead, the SM ripples have to be distributed equally within the leg: therefore, the above techniques were modified by adding the rotation of the carriers [57]. Another PWM technique based on multiple carriers is the phase-shifted (PS) strategy [58]. A number of carriers equal to $N_{level} - 1$ are shifted of an angle equal to $\frac{2\pi}{N_{level}-1}$ and compared to one modulation signal - per phase. This technique does not reduce the switching losses, since the carrier frequency corresponds to the SM switching frequency, but it has the lowest harmonic content compared to the techniques above mentioned. The four modulation techniques are shown in Fig. 2.12.

To further reduce the switching losses, the Nearest Level Modulation (NLM) is presented in [59]. This modulation strategy determines the voltage levels by approximating the voltage modulation demand V_m*:

$$N_{level} = \frac{V_m*}{V_{dc}} \tag{2.23}$$

The mathematical approximation introduces low frequency harmonics, particularly visible with a limited number of SMs. However, this solution is specifically adequate for application with a large number of submodules because it is easy to be implemented and reduces drastically the switching losses. The NLM is shown in Fig. 2.13.

2.6 Reconfigurable Battery Systems

Reconfigurable Battery Systems were created with the aim of changing the battery interconnection pattern according to the cell characteristics and load demand. As shown in Fig. 2.14, the

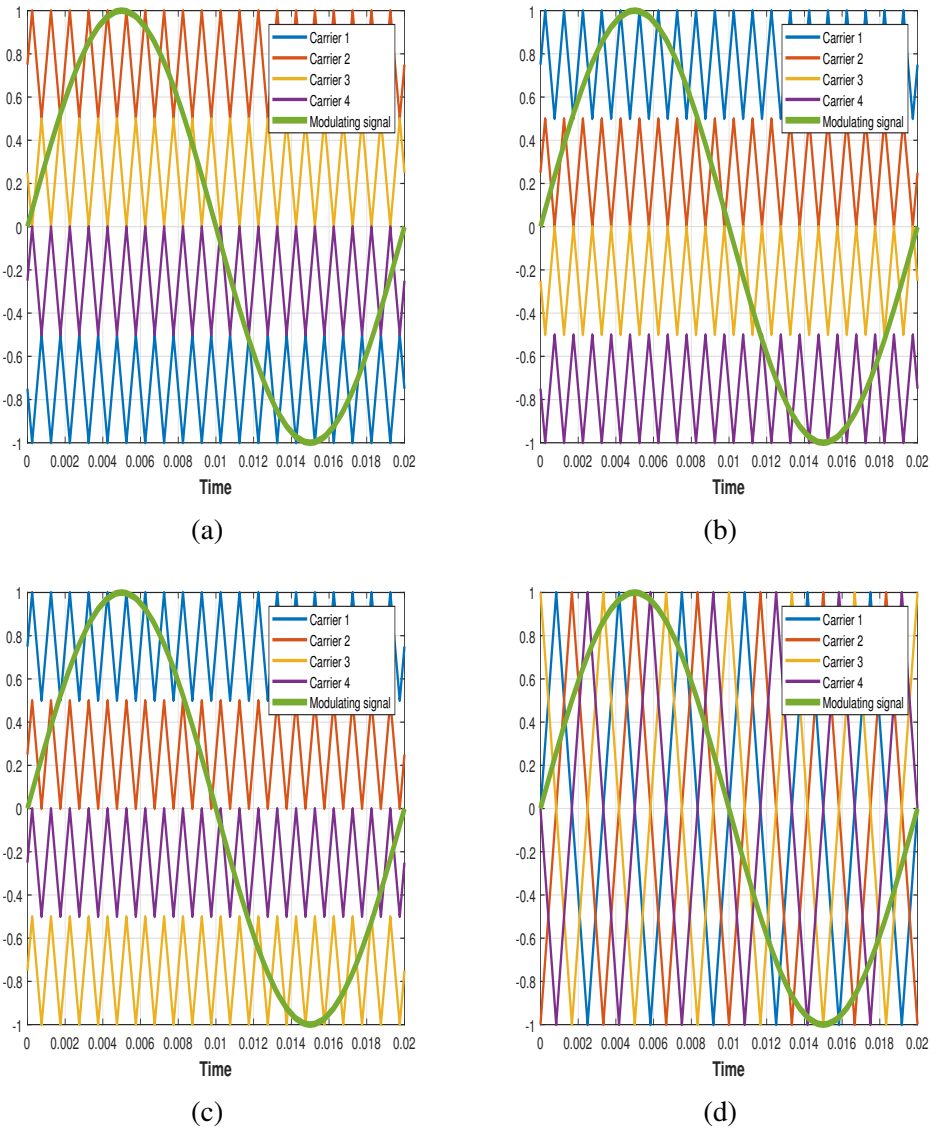


Figure 2.12: (a) APOD, (b) POD, (c) PD, (d) PS modulations.

modification of the battery pack topology is achieved by surrounding each cell with a pattern of switches to be controlled according various control schemes. The main benefits of the RBSs are widely explained in [60] and can be summarized as:

- fault tolerant strategies can be drastically enhanced. In fixed battery packs, faulty conditions force the stop of the operations and, if not detect on time, they may lead to waste of energy

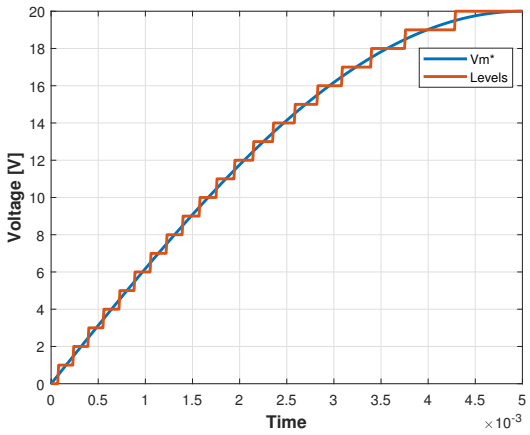


Figure 2.13: Nearest level modulation.

and materials; in RBSs, the dynamic reconfiguration allows to isolate the local faults and perform quick disconnections/connections of the damaged/healthy cells.

- Charge and temperature balancing can be performed in faster and easier way, compared to battery packs. As already explained above, charge and temperature disparity between the cells seriously affect the energy delivery and reduce the longevity of the battery system, respectively. By adequate reconfiguration strategies, the state of charge (SOC) equalization can be achieved in half of the time [61] and the temperature monitoring can be done in a capillary way.

  Moreover, battery cells experience ageing processes, which increases with the utilization rates. In EVs application, battery cells with less than 80% of their rated capacity are then moved to other applications, where the requirements are less strict [62]. A correct management of RBSs allows to increase the first-life usage, by allowing customizable balancing algorithm and thermal control routine to reduce the battery cells stress. RBSs can even cover a more strategic role during the second-life usage, where the battery cells are weaker and they do really need a careful control routine to be correctly exploited.

- The energy absorbed and delivered by the battery system can be extended. During the

charging/discharging process, the cells already fully charged/discharged can be disconnected from the system to allow the rating charge/discharge for the not charged/discharged cells. By planning the battery operation, the range of the energy delivery can be easily extended [63, 64].

- Inclusion of different chemistry batteries is possible by appropriately implementing control algorithms. The idea of mixing various technologies was proposed in [65], supporting the idea that the points of strength and weakness of different chemistries can be exploited over the operating condition ranges.

However, there are many technical challenges to be addressed for RBSs design [66]. The most important is finding a trade-off between the system complexity and the maximum reconfiguration patterns. The more are the possible interconnection paths between the cells, the more flexibility can be achieved in RBSs management; on the other hand, this will increase the control complexity, costs and size. Therefore, RBSs design should be assessed according to the application requirements, to ensure scalability, reliability and cost-effectiveness.

In EVs application, the adoption of RBSs may mitigate the issues related to the battery system mismanagement. Nevertheless, reconfigurable systems do not perform any conversion between DC and AC voltage; therefore, RBSs still need the connection to a DC/AC converter to power the motor. Depending on the reconfigurability options, RBSs may have significant losses to be added to the ones due to the DC/AC stage, affecting the overall efficiency system.

Therefore some other hybrid solutions have been developed. The latest trend is proposing the concept of ”Smart batteries”: in [67], cells are autonomously able to evaluate the optimal switching pattern, reducing the voltage ripple and equalizing their SOC according to the average values; in [68], each cell is connected to a half-bridge converter with an embedded microprocessor, responsible for the control algorithms of balancing and monitoring; in [69] BMS functionalities are integrated at cell level by inserting radio-frequency identification (RFID) to perform cell-to-cell communication; in [70], the monitoring system is performed by a battery-wireless system.

Finally, RBSs and smart battery cells are in their early stage of concept and definition. As

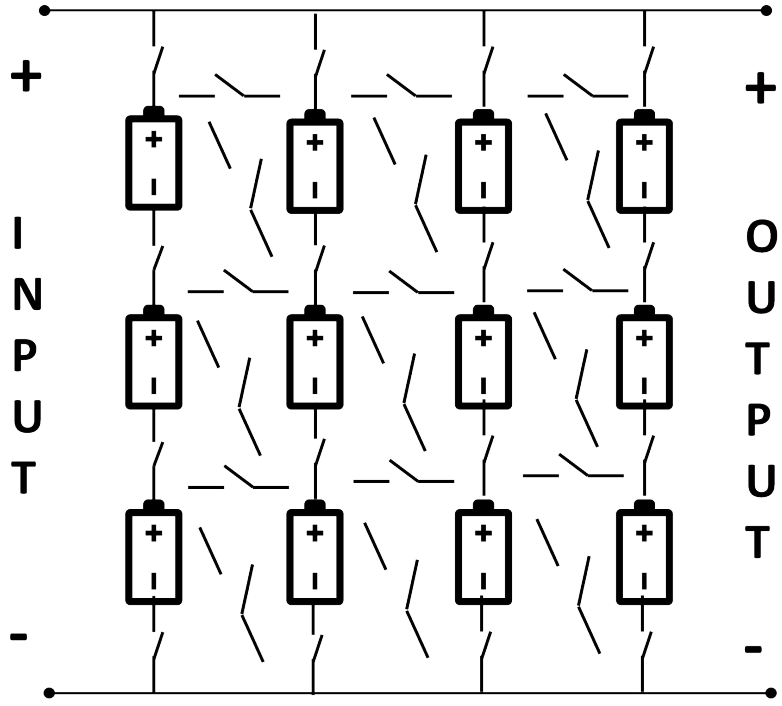


Figure 2.14: An example of a Reconfigurable Battery System.

an example, mathematical models to describe and/ or optimize RBSs and possible strategies are still under investigations, due to the difficulties of finding a working trade-off between the high computational burden and good results.

The new topology presented in this dissertation, called Reconfigurable Cascaded Multilevel Converter, combines the RBSs and MCs concepts. The structure is formed by the serial connection of several submodules per phase, in which the battery cells are inserted in a new structure called Reconfigurable Battery Module. Their role is to perform the insertion and/or exclusion of each cell by controlling a pattern of seven switches, coherently placed. The Reconfigurable Cascaded Multilevel Converter allows to merge the features of the BMS and DC/AC conversion, giving also the possibility to design its architecture according to customizable requirements.

CHAPTER

3 Reconfigurable Cascaded Multilevel Converter

The Reconfigurable Cascaded Multilevel converter (RCMC) is shown in Fig. 3.1 [71]. Each phase is characterized by the serial connection of several submodules (SMs). In each submodule, the cells are organized in fixed structures called Reconfigurable Battery Modules (RBMs), which permit to implement an individual management of the battery cells. The RBM architecture does not allow a bidirectional voltage output, therefore, its terminals are connected to a H-Bridge, which accomplishes two main roles: on one side, it is responsible of inverting the voltage output when required, and, on the other side, it allows to completely bypass the SM. The SM rated voltage can be decided according to customized requirements, by simply adding more RBMs in series.

Through the appropriate selection of the switches, the RBM structure facilitates the implementation of sorting algorithm for an optimized battery management. During both discharging and charging phases, the battery cells may be selected according to SOC requirements, in ascending and descending way respectively. Moreover, if a faulty behaviour is detected, the modular structure can guarantee a hierarchical action: it is possible to disable a single battery cell or an entire RBM or, even, one SM without the necessity to stop the normal operation of the drive train.

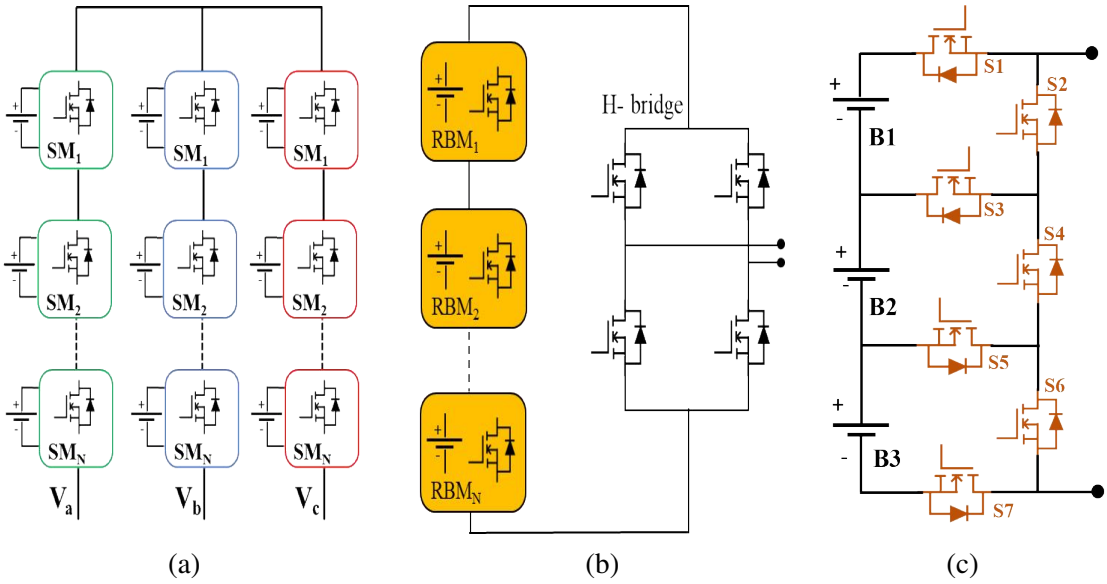


Figure 3.1: (a) Reconfigurable Cascaded Multilevel converter. (b) Submodule structure. (c) Reconfigurable Battery Module structure.

3.1 Reconfigurable Battery Module

The innovative core of the topology lies on the Reconfigurable Battery Module. Each module consists of three battery cells and seven switches coherently connected, in order to flexibly select one or more cells. The conduction path may entail a varying number of switches depending on the quantity of battery cells to be connected and where they are located within the RBM. Table 3.1 shows the device combinations for all possible battery cells selection. With reference to Fig. 3.2, the more are the battery cells to be inserted, the less are the switches in conduction: four switches must be turned on for one battery cells, three switches for two cells, two switches for three battery cells. When all three cells have to be bypassed, the three lateral switches are turned on. The RBM has only one prohibited configuration: it is not possible to turn on both the battery cells in first and third positions, without shorting out the second battery cell, as shown in Fig. 3.3.

Different analysis have been carried out to evaluate if the number of battery cells could be increased within one RBM. The benefits could have been the reduction of switches per battery

cell with a consequent mitigation of conduction losses and size. As an indicator, the ratio between the number of switches and battery cells for a three-battery cells RBM is equal $\frac{7}{3} = 2.33$. This value decreases as the battery cells per RBM increases: as an example, the ratio for ten battery cells would be equal to $\frac{21}{10} = 2.1$.

However, a larger number of battery cells increases the prohibited configurations. Considering a four- battery cells RBM, five are the prohibited combinations leading to short circuits, shown in Fig. 3.4.

The limited number of configurations not only adds a significant computational burden of the control architecture - a check algorithm is needed to avoid faulty conditions - but also reduces the effectiveness of the sorting algorithms, which can work properly only when the selection does not concern an intermediate number of battery cells. In general, a larger number of battery cells would mean reducing the flexibility of battery cells insertion.

3.1.1 Modulation strategy

The number of voltage levels available L_v for the RCMC corresponds to the number of battery cells installed within the phase. It can be written as:

$$L_v = 2 \cdot N_{\text{cell}} + 1 = 2 \cdot (3N_{\text{RBM}}) + 1 \tag{3.1}$$

Table 3.1: Device combination for battery selection

Connected batteries	Switches turned on
B1	S1,S3,S4,S6
B2	S2,S3,S5,S6
B3	S2,S4,S5,S7
B1 & B2	S1,S5,S6
B2 & B3	S2, S3, S7
B1 & B3	Not allowed
B1 & B2 & B3	S1,S7
None	S2,S4,S6

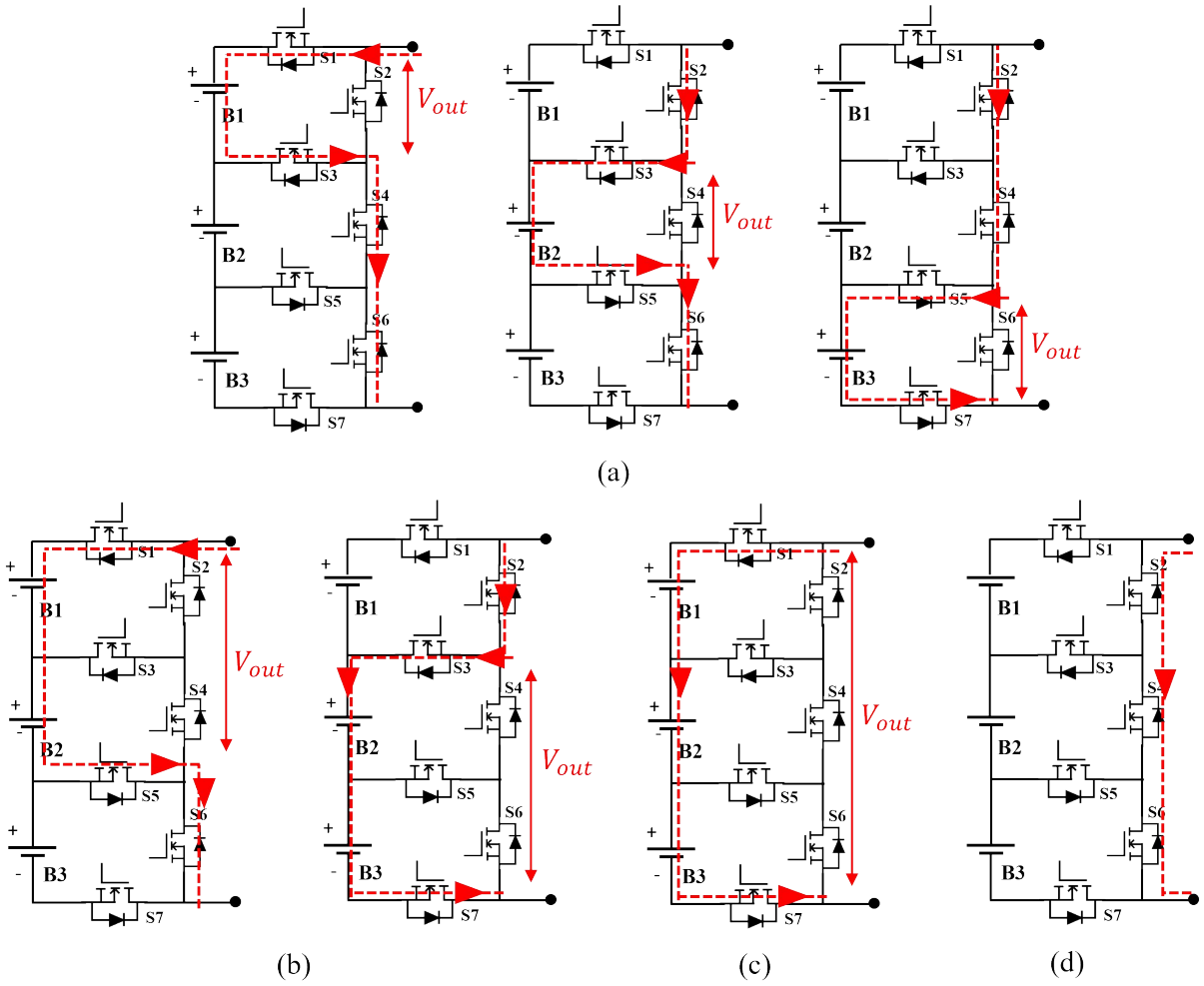


Figure 3.2: Switches combinations for the insertion of a different number of battery cells: (a) one battery cell, (b) two battery cells and (c) three battery cells.

where N_{cell} and N_{RBM} are the number of battery cells and RBM per phase, respectively. Considering a drive train application with a motor nominal voltage of hundreds of volts, the large number of battery cells serially connected are sufficient to justify the utilization of the digital Nearest Level Modulation (NLM). The latter permits to obtain low THD values for the output current, low $\frac{dV}{dt}$ and allowing a consequent reduction of EMI [18]. Furthermore, the large number of levels and the adoption of the NLM ensures low switching frequency for all the devices of the converter. Indeed, each DSP cycle, only the devices connected to the requested battery cells are

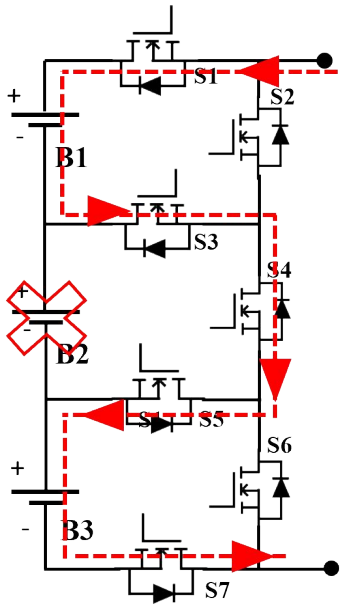


Figure 3.3: Prohibited combination for the RBM.

switched on or off while the H-bridge devices have an equivalent switching frequency equal to the one of the fundamental output voltage. As validation, in the next chapter, the THD current values will be shown for different working points.

Different considerations have to be made when the converter works at low voltage conditions. In that case, the NLM resembles a PWM because the requested output voltage is so low that the control computes an oscillating number of battery cells around the zero. Therefore, each DSP cycle, the same pattern of devices is asked to switch, until the sorting algorithms updates the batteries to be inserted. Especially when the converter works at low voltage conditions, the sorting algorithm may change the battery order with dynamics close to the minutes. Therefore, the same pattern of switches are asked to switch at the DSP frequency for a significant amount of time.

Therefore, a control strategy has been developed in order to distribute the switching pattern over the different levels, decreasing the equivalent switching frequency for all the devices. The algorithm can be properly tuned in order to fix the final switching frequency. Fig. 3.5 (a) shows a

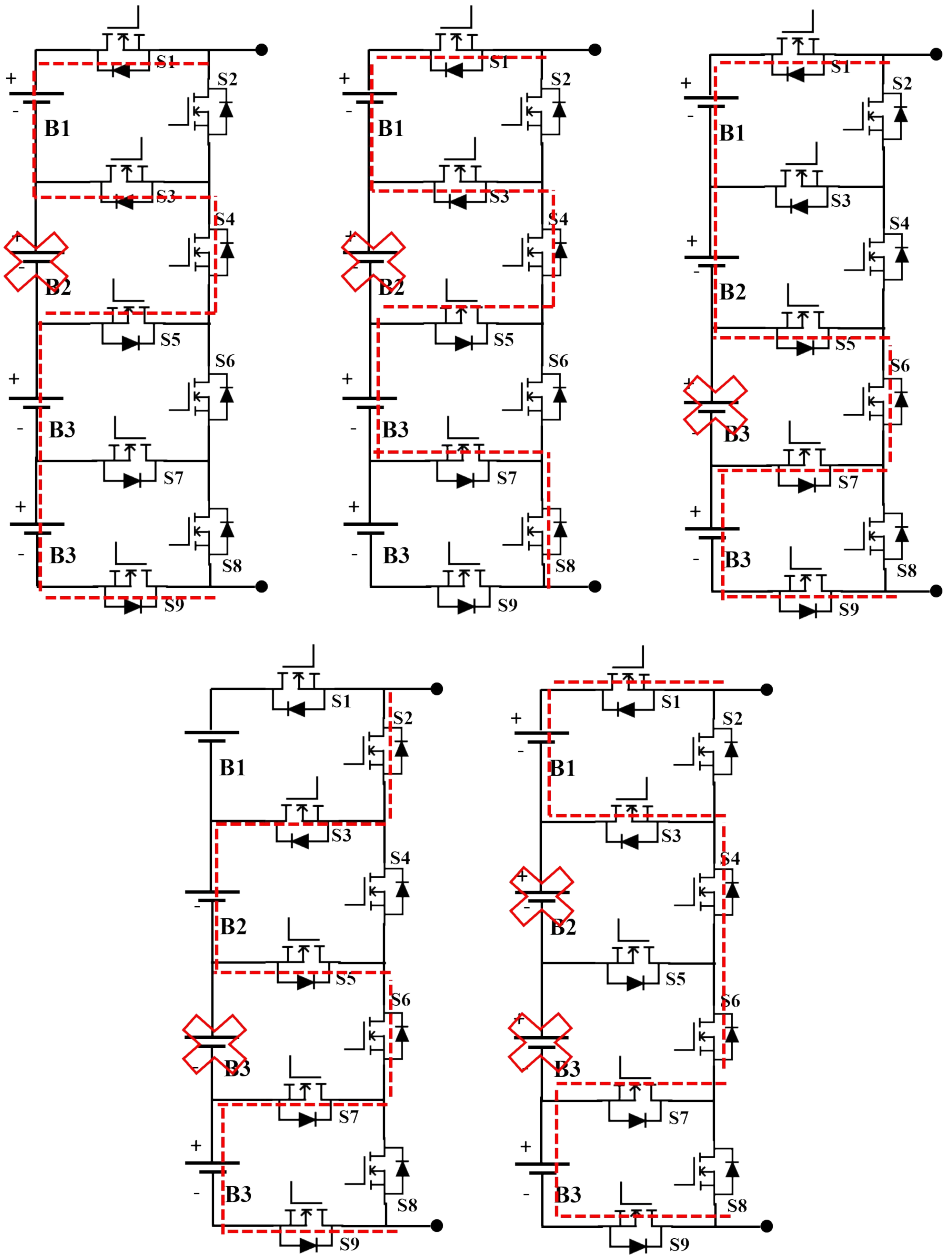


Figure 3.4: Prohibited configurations for a RBM with four battery cells.

typical situation at low voltage operation: the number of battery cells requested ranges between one and zero. Without any kind of algorithm, the most charged cell would be alternatively turned on, increasing the switching frequency for a determined number of devices up to the DSP

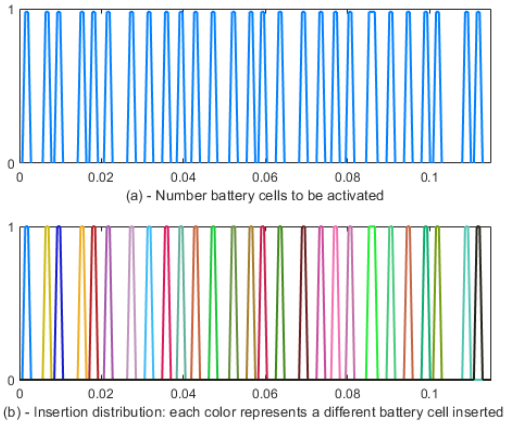


Figure 3.5: Insertion order for operative condition at low voltage loads.

frequency. On the other hand, the developed algorithm associates a red flag to the cell which has been already turned on and off consecutively in a certain period and forces the the insertion of the next more charged cell. Therefore, as shown in Fig. 3.5 (b), each time the requested number of battery cells is equal to 0-1-0, different battery cells are inserted. The period after which these cells can be inserted again it is completely customizable.

3.2 RCMC design optimization

Defined the voltage and current nominal ratings, the RCMC structure is fully customizable. The number of SMs per phase and RBMs in each SM can be decided according to different criteria such as energy density, volume optimization, etc. In this section, the converter losses are evaluated and then used as prior parameter to find the best architecture. The converter efficiencies are computed by modelling the switching and conduction losses of the devices on PLECS.

The optimization here shown will be carried out assuming that the RCMC powers a three-phase Permanent Magnet Synchronous Motor (PMSM), whose parameters are listed in Table 3.2. The PMSM torque-speed characteristic is shown in Fig. 3.6 .

The RCMC losses are mainly due to the conduction contributions while the switching losses are considered negligible, as already discussed above. The HB losses contribution can be written

Table 3.2: Motor parameters

Parameter	Value	Unit
Stator Resistance	0.037	mΩ
Flux constant	0.22075	Wb
Pole Pairs	4	
Inductance ($L_d = L_q$)	730	μH
Max Torque	320	N·m
Max phase current peak	240	A
Max phase voltage peak	388	V
Max speed	1050	rad/s

as:

$$P_{\text{condHB}} = 3 \cdot 2 \cdot N_{\text{SM}} \cdot R_{\text{dson}} \cdot I^2{}_{\text{rms}} \tag{3.2}$$

where R_{dson} is the internal HB MOSFET resistance, I_{rms} is the rms value of the load current, 3 is the number of the phases, 2 is the number of switches in conduction and N_{SM} is the number of SMs per phase. The conduction losses analysis for the RBMs cannot be performed in analytical way because they strictly depend on the instantaneous output voltage and current values. According to the voltage requirement, the NLM computes a different number of battery cells to be inserted at each DSP cycle. Therefore, the number of switches in conduction is not

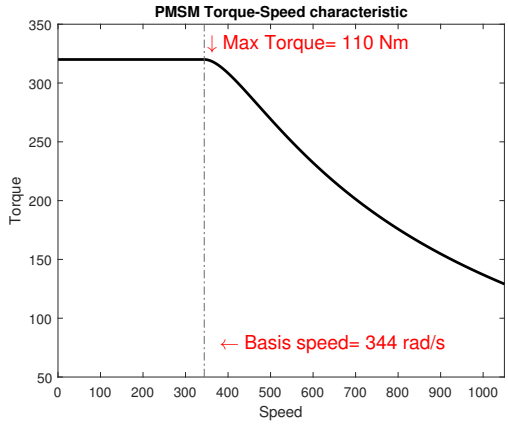


Figure 3.6: Torque -speed characteristic curve of the PMSM, used in this dissertation.

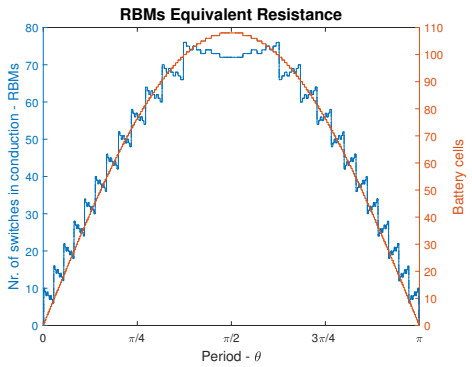


Figure 3.7: Equivalent phase resistance when the battery cells are inserted in progressive order.

constant and the conduction losses must be calculated by averaging the sum of the instantaneous losses contributions on a period of the output fundamental frequency. Moreover, the equivalent resistance strictly depends on the insertion order of the battery cells. For the same number of battery cells to be inserted, the conduction path designed by the switches may drastically change whether the battery cells belong to the same RBM or/and the same submodule. For this analysis, it is assumed to select the battery cell in progressive order from the first RBM till the last one. Fig. 3.7 shows the trend of the RBM switches in conduction, which resembles the equivalent resistance trend, on half period of output fundamental frequency assuming all battery cells are inserted consecutively.

Assuming a desired output phase voltage of $388V$ and a nominal battery cell voltage of $3.6V$, the system requires 108 cells connected in series resulting in 36 RBMs per each phase. Qualitatively, as the total number of RBMs remains the same across the different configurations, the number of SM is in reality responsible for the overall efficiency. As N_{SM} increases, more devices are present in the output current path with the risk of increasing conduction losses. On the other hand, having more SMs leads to a lower HB devices rate voltage resulting, in turn, in a lower R_{dson}. Another important characteristic that affects system losses is the possibility of bypassing all the RBMs in a submodule when they are not needed because of a low output reference voltage. The bypass of a SM eliminates all RBM switches from the output current path reducing conduction losses. The effect of this phenomenon is strongly conditioned by the number

Table 3.3: RCMC architectures parameters.

Architecture	N_{RBM}	N_{SM}	Voltage Ratings [V]	R_{dson} [mΩ]	Device
A	36	1	1000	51.4	APTM100UM45DAG
B	12	3	300	4.6	IXFN210N30X3
C	6	6	150	2.5	IXFN400N15X3
D	4	9	100	1.28	IRF100P218
E	3	12	60	0.68	NTMTS0D7N06CL
F	1	36	30	0.40	IPT004N03L

of RBM per SM.

To evaluate quantitatively these aspects, a simulative analysis is carried out by comparing six RCMC architectures. For each configuration, Table 3.3 shows the voltage rating and the internal resistance of the devices employed for the six architectures. The voltage ratings and the R_{dson} are listed only for the HB devices because their voltage ratings change according to the architecture. On the contrary, in any configurations, the RBMs devices must face at maximum three times the voltage of one battery cell. Assuming to use the Li-Ion cells, the maximum voltage seen by one device is equal to

$$V_{\mathrm{RBM}} = 3 \cdot 4.2V = 12.6V \tag{3.3}$$

Therefore, the low voltage MOSFET IPT004N03L is chosen with 30 V as V_{ds} and 0.4mΩ as R_{dson}. All R_{dson} reported are valid for a gate-source voltage V_{gs} equal to 10V, a load current I_D equal to 50 A and a operative temperature T_c equal to 25°C.

Fig. 3.8 shows the efficiency maps for the six RCMC architectures analysed. The first group of architecture, A, B and C - with the largest number of RBMs installed within each submodule -, are the less efficient. The main reasons are the higher internal resistance of the devices of the HB and the necessity to bypass several RBMs within the SM for the most of the operative condition. Indeed, architecture A does not bypass any RBMs only when the voltage requested by the control is equal to the nominal value. On the other hand, it is the most efficient within the first group because the contribution of the RBMs devices needed in bypass configuration

is less significant compared to the losses due to the HB switches of the architectures B and C. The second group of architectures, D, E and F, shows a better efficiency in the overall operative conditions. In this case, the number of RBMs within each submodule is decreased so that, even at low power conditions, the devices needed to bypass the RBMs are negligible. Moreover, the H-bridges conduction losses decrease because the switches used have an internal resistance at least one order of magnitude lower than the first group of architectures. Overall, architecture *E* has been selected for further investigation as presents a better overall efficiency on the whole operative range synthesizing a successful trade-off between the number of RBMs within each submodule and the internal resistance of the H-bridge devices.

3.3 Comparison with other converter topologies

The RCMC performance is here compared to two other multilevel topologies - the Hybrid Cascaded Multilevel Converter (HCMC) proposed in [72] and the Cascaded H-Bridge (CHB) - and a SiC two-level inverter, in terms of converter and battery efficiency, assuming they power the three-phase motor presented in the previous section. The equivalent battery pack installed within the three converters is assumed to be 80 kWh, using MOLICEL INR-18650-P26A as battery cell, with nominal voltage V_{bat} and capacity C_{bat} equal to 3.6V and 2.6 Ah, respectively.

3.3.1 RCMC design

The number of battery cells needed in each phase of the RCMC is equal to:

$$N_{\text{bt}} = \frac{V_{\text{mot}}}{V_{\text{bat}}} = \frac{388V}{3.6V} = 108 \tag{3.4}$$

where V_{mot} is the nominal phase voltage of the motor. The number of RBMs N_{RBM} for the RCMC is equal to:

$$N_{\text{RBM}} = \frac{L_{\text{v}}}{3} = \frac{108}{3} = 36 \tag{3.5}$$

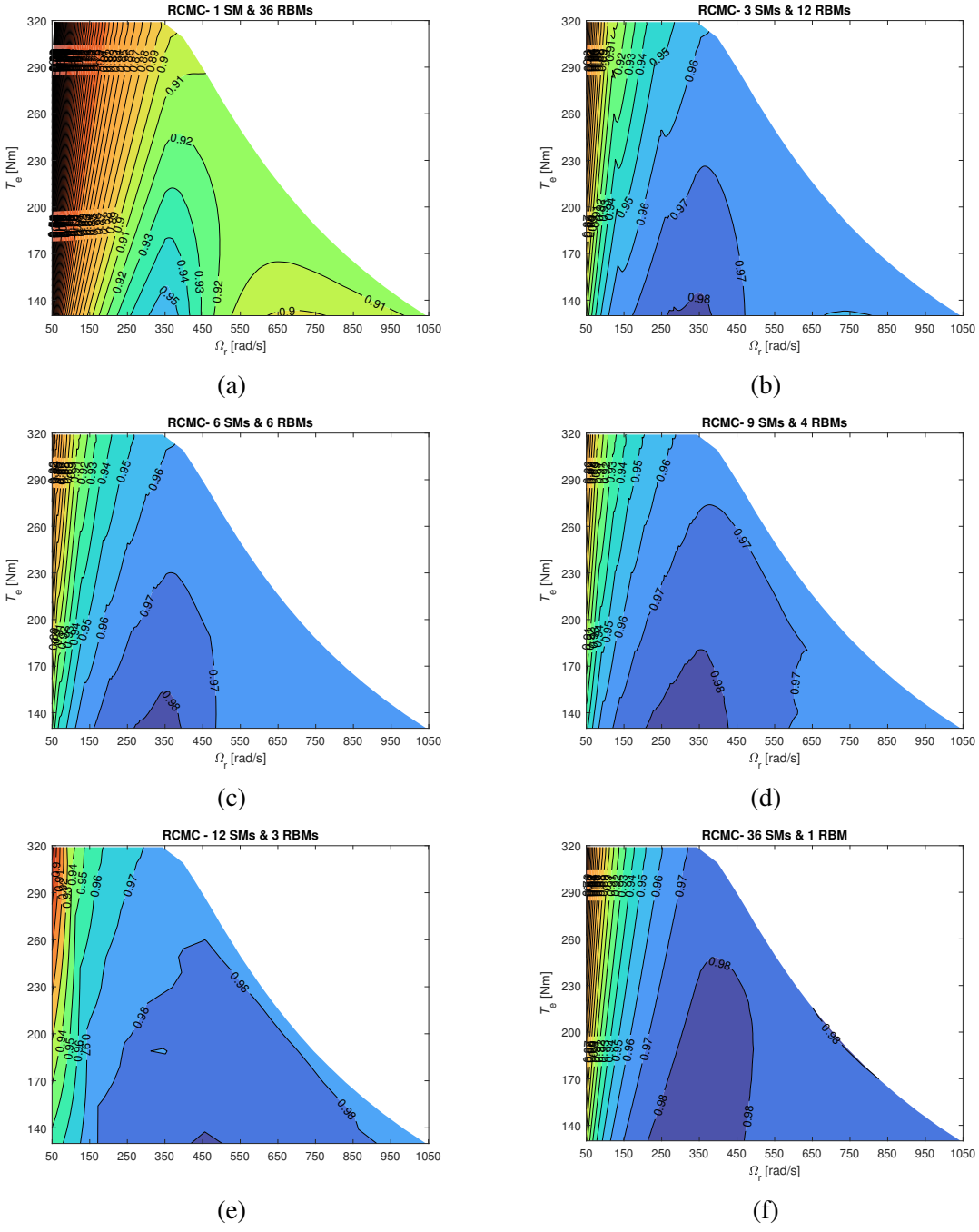


Figure 3.8: Efficiency plot for the six RCMC architectures: (a) 1 SM and 36 RBMs, (b) 3 SMs and 12 RBMs, (c) 6 SMs and 6 RBMs, (d) 9 SMs and 4 RBMs, (e) 12 SMs and 3 RBMs and (f) 36 RBMs and 1 RBM.

According to the optimization reported above, the RCMC is composed by 12 submodules with 3 RBMs and 9 battery cells each. The high number of voltage levels, equal to 217, makes convenient the utilization of the NLM. The equivalent capacity C_{lv} of the battery installed within each converter level is equal to:

$$C_{\text{lv}} = \frac{E_{\text{eq\_bat}}}{V_{\text{conv}}} = \frac{80kWh}{3 \cdot 108 \cdot 3.6} = 68Ah \tag{3.6}$$

where E_{eq_bat} is the energy of the equivalent battery pack and V_{conv} is the voltage installed within one phase of the converter. The number N_p of battery cells connected in parallel for each level can be calculated as:

$$N_{\text{p}} = \frac{C_{\text{lv}}}{C_{\text{bat}}} = \frac{68Ah}{2.6Ah} = 26 \tag{3.7}$$

The devices used for the HB of the converters is NTMTS0D7N06CL and for the RBM is the IPT004N03L.

3.3.2 HCMC design

The HCMC topology is shown in Fig. 3.9: each battery cell is connected to a Half-Bridge converter used to select or bypass it. As for the RCMC, in each SM there is a H-Bridge to invert the output voltage polarity when it is required.

Since the concept of the HCMC design is the accessibility to each battery cell, the design analysis carried out for the RCMC can be reiterated for the HCMC. The number of battery cells needed per phase is computed as in (3.4) and it is still equal to 108. In order to have a coherent comparison, each battery cell is connected to one Half-Bridge; nine Half-Bridges units are serially connected in each SM. Being the battery cells distribution identical, the parameters C_{lv} and N_p coincides with the values calculated above in (3.6) and (3.7), respectively. Finally, NTMTS0D7N06CL and IPT004N03L are used as devices for the HB and the Half-Bridges, respectively.

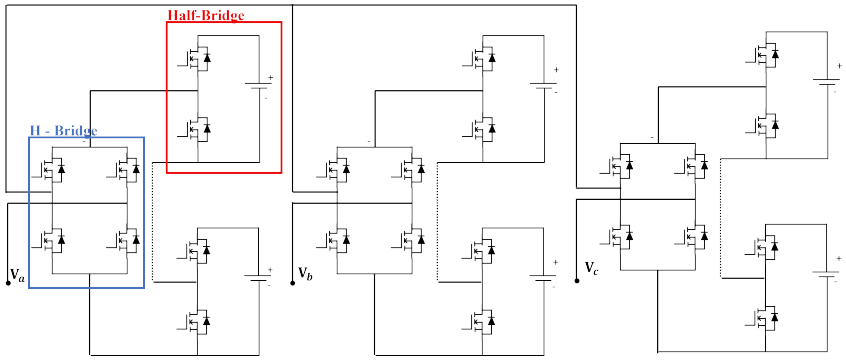


Figure 3.9: Hybrid Cascaded Multilevel Converter topology.

3.3.3 CHB design

The comparison would be inconsistent with a CHB with 108 levels because the number of switches in conduction would be at least double compared to the other two converters. Therefore, the CHB has been designed according to [12], with three SMs per phase. Each SM has an equivalent battery module equal to:

$$V_{\text{mCHB}} = \frac{V_{\text{motor}}}{3} = \frac{388V}{3} = 129V \tag{3.8}$$

Therefore, the number of battery cells serially connected in each battery module will be:

$$N_{\text{sCHB}} = \frac{V_{\text{mCHB}}}{V_{\text{bat}}} = \frac{119V}{3.6V} = 33 \tag{3.9}$$

The number of battery cells connected in parallel is the same for the RCMC and the HCMC. The final battery module for each SM of the CHB will be 33s26p. The limited number of levels of the CHB makes the utilization of the NLM inconvenient; the modulation adopted is the Phase Shift Carrier (PSC). The carrier frequency is set to 3.3 kHz, with an equivalent switching frequency equal 9.9 kHz. The device used for the simulation is IXFT150N30X3HV.

3.3.4 SiC 2 - level inverter design

The modulation technique chosen for the 2-level inverter is the Sinusoidal PWM (SPWM), with a carrier frequency equal to 20 kHz. The 2-level inverter is implemented with the power module FS03MR12A6MA1B, made of SiC MOSFETs.

In order to have a peak phase voltage V_{ph} equal to $388V$, the DC link voltage V_{dc} required is equal to [5]:

$$V_{\text{dc}} = 2 \cdot V_{\text{ph}} = 2 \cdot 388V = 776V \tag{3.10}$$

Therefore, the number of battery cells serially connected within the battery pack will be:

$$N_{\text{sINV}} = \frac{V_{\text{dc}}}{V_{\text{bat}}} = \frac{776V}{3.6V} = 215 \tag{3.11}$$

The DC link voltage value computed in (3.10) fits with the latest trend of increasing the battery pack rating voltage up to 800 V, as already explained in the previous chapter. The overall capacity of the battery pack can be written as:

$$C_{\text{inv}} = \frac{E_{\text{eq\_bat}}}{V_{\text{dc}}} = \frac{80kWh}{776} = 103Ah \tag{3.12}$$

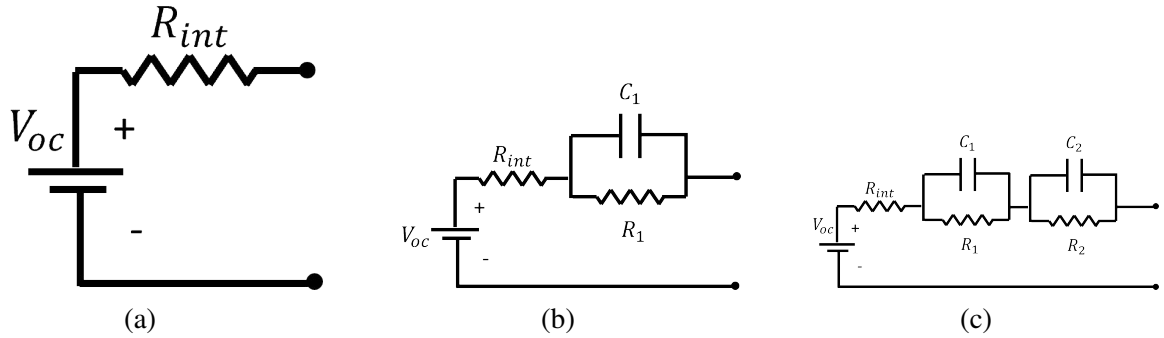
and the number of battery cells to be connected in parallel is equal to:

$$N_{\text{p\_inv}} = \frac{C_{\text{inv}}}{C_{\text{bat}}} = \frac{103Ah}{2.6Ah} = 39 \tag{3.13}$$

3.3.5 Battery efficiency

Battery model

The efficiency evaluation is carried out by firstly adopting a suitable battery cell model for the aim of this analysis. In literature, many models have been presented searching for the right trade-off



(a) (b) (c)

Figure 3.10: Battery cell models: (a) R_{int} (b) first-order resistor-capacitor (RC) (c) second-order resistor-capacitor (RC).

between the accuracy and the computational weight:

- in [73], the R_{int} model is presented. It consists in the serial connection of an ideal voltage source with a resistor: this model does not take into account the polarization and diffusion phenomena but is widely used when the static behaviour of the battery cell has to be simulated;
- in [74], the authors suggested a first-order resistor-capacitor (RC) model which can simulate the real behaviour with high fidelity;
- in [75], a second-order resistor-capacitor (RC) model is presented. This model approximates the dynamic response of the battery cell with a voltage error less than 40 mV [76].

The three models are shown in Fig. 3.10: R_{int} represents the immediate responses of the terminal voltage to the flowing current and it is the responsible of the battery losses; the first and second order RC networks are used to model the dynamic response polarization voltages, associated to the charge transfer within the cell, in short-tem and long-term components.

Since the aim of this analysis is the losses evaluation and not the dynamic responses, the R_{int} model has been chosen to have valid results with low computational weight.

Battery losses computation

It is assumed that the battery cell is fixed to the 80% of SOC and its losses are due only to the resistive element. The evaluation of the internal resistance has been done experimentally. Given the nominal motor current, the parallel connection N_p and the nominal capacity of the battery C_{bat}, the maximum C-rate which the battery will operate is equal to:

$$C_{\text{rate\_max}} = \frac{I_{\text{nom}}}{N_{\text{p}} \cdot C_{\text{battery}}} = \frac{240A}{26 \cdot 2.6Ah} = 3.5 \tag{3.14}$$

Firstly, the MOLICEL INR-18650-P26A has been characterized by doing the HPPC test [77]. The goal of this test is to determine the V_{oc} - SOC curve, which represents the correspondence between the open circuit voltage of the battery cells and its SOC value. Since this curve is strictly affected by the discharging current value, this test has been performed for six different C-rates values (C1, C1.5, C2, C2.5, C3, C3.5). Between all approaches presented in literature [78], the Current-Off method test has been chosen to estimate the internal resistance of battery cells. The test consists in discharging the battery cells from 90% to 80% of SOC and measure its internal voltage drop right before the battery is disconnected from the circuit. This value is subtracted by the battery voltage value in open circuit and then divided by the discharging current value. The test dynamic is shown in Fig. 3.11. The obtained values are interpolated to obtain the dependence between the resistance over the current flowing, as shown in Fig. 3.12.

The efficiency plots of the equivalent battery packs installed within the three converters and the two-level inverter are reported in Fig. 3.13. The three multilevel converters share the same efficiency trend, due to the similar design in terms of phase voltage ratings and battery system capacity. Therefore, under the same condition of load current and voltage, not only the number of battery cells to be inserted coincides but also the operating C-rates. Thus, in each point of the efficiency map, the equivalent battery pack resistance assumes the same value for all three converters. The two-level inverter has the most efficient battery system. The gap of 1% compared to the multilevel architectures can be explained by considering the current flowing inside the

battery cells. The current flowing in the battery cells within the multilevel converters in each phase coincides with the load current, so it is possible to write:

$$I_{mc} = 3 \cdot I_l \tag{3.15}$$

where I_{mc} is the rms value of the overall current flowing in the converter, 3 is the number of the

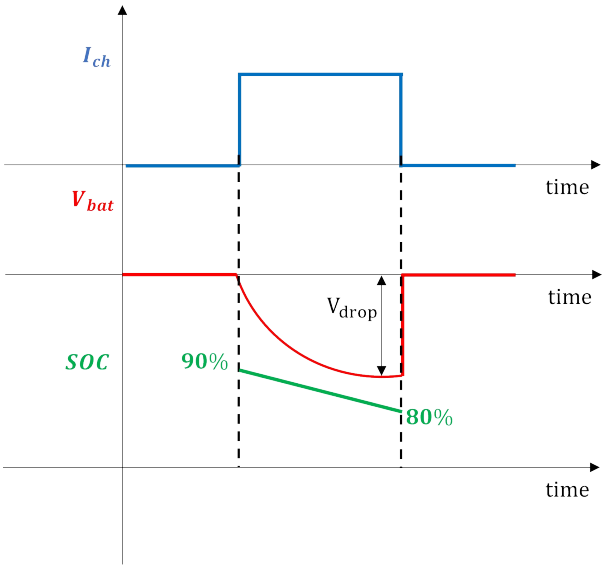


Figure 3.11: Current- OFF method test.

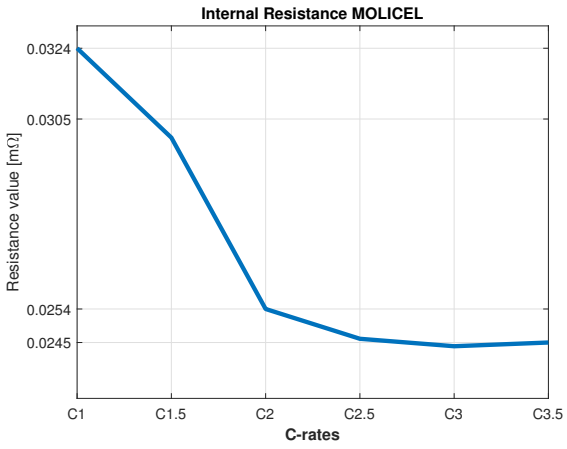


Figure 3.12: Internal resistance of MOLICEL INR-18650-P26A for operative C-rates.

phases and I_l is the load current. The DC current I_{dc_inv} of the two-level inverter can be written as:

$$I_{dc\_inv} = \frac{\sqrt{3}}{2} \cdot I_l \tag{3.16}$$

By expressing I_l as function of I_{mc} and I_{dc_inv} in (3.15) and (3.16) respectively, the relation between the two-level and multilevel converters current is obtained:

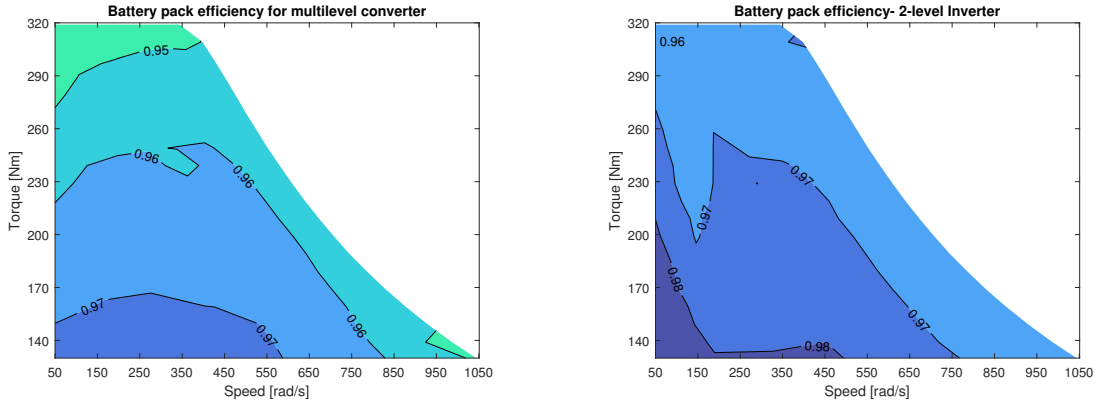
$$I_{mc} = 2\sqrt{3} I_{dc\_inv} \tag{3.17}$$

Finally, the current flowing in the battery cells in multilevel converters is 3.5 times larger than in the two-level inverter.

On the other hand, a large DC-link voltage value here considered requires effective balancing actions. BMSs should be accurately designed to not loose the advantage of the high voltage and to avoid any faulty conditions, whose occurrence probability increases as the number of battery cells in series increases. Moreover, the utilization of conventional passive BMSs may decrease the overall efficiency of the battery system [36]. The same analysis can be extended to the CHB that, with only 3 SMs per phase, requires the BMS employment as well. Conversely, the RCMC and the HCMC structure merges the power converter and BMS functionalities. The benefits are not longer limited to the active balancing strategies but involve also the possibility to perform a capillar thermal management, in order to avoid run-away phenomena. Overall, the two-level inverter has the best efficiency as long as the mantainance of the battery system is adequately performed.

3.3.6 Efficiency results discussion

As can be noted, the proposed topology outperform the more classical HCMC structure, in particular in the central region in which fall most of the driving cycles trajectories. This is justified by the following. A RBM has only two switches conducting when all cells are connected, 3 switches when two or zero cells are connected and 4 switches when only one cell is connected.



(a) (b)

Figure 3.13: Efficiency plot for (a) battery pack in multilevel converters, (b) battery pack in the two- level inverter.

On average, the latter condition happens less often compared to the first one, making the average conductive resistance of a single RBM smaller than $3R_{\text{dson}}$. For example, at speed $344rad/s$ and torque $320Nm$ the equivalent RBM conductive resistance is of $85R_{\text{dson}}$. On the contrary, the HCMC has always one switch conducting for each cell, making the equivalent conductive resistance always equal to $108R_{\text{dson}}$, which corresponds to the number of Half-Bridges installed within one phase. Fig.3.14 (c) and (d) show the efficiency map of the CHB and two level SiC configurations respectively. Both the topology outperform the proposed configuration. However, as already previously mentioned, the latter comes with all the advantages of controlling the connection of single cells independently. The slightly lower efficiency is compensated by a better management of the battery system possibly resulting, in turn, in a bigger mileage range. Especially in the two-level inverter configuration, the high number of serial connected cells requires a intensive BMS effort in order to keep balanced cell voltage levels. This become more and more critical as the battery ages and the differences between the single cells increase. Moreover, the utilization of conventional passive BMSs may decrease the overall efficiency of the battery system [36]. These drawbacks are partially mitigated in the CHB configurations. The single submodules, however, still require an additional BMS system and don't offer the flexibility

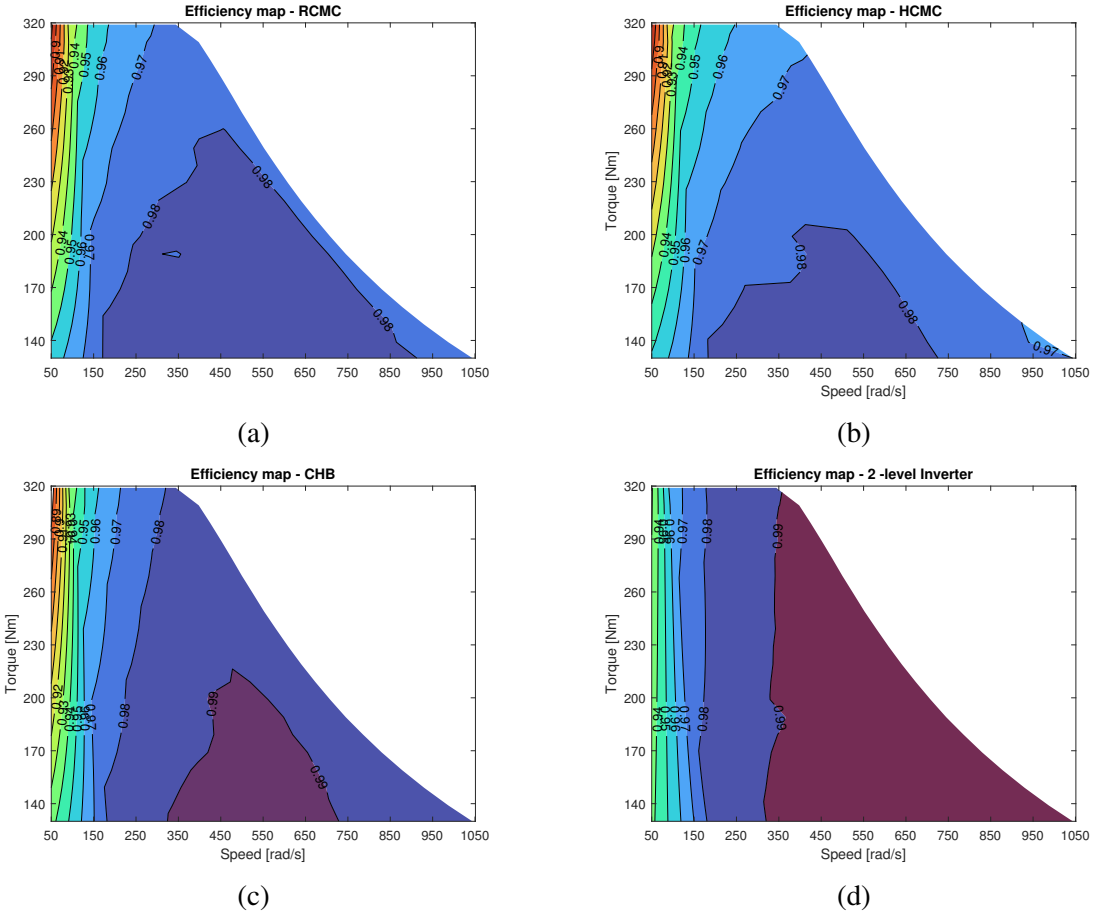


Figure 3.14: Efficiency plot for (a) RCMC, (b) HCMC and (c) CHB and (d) two- level inverter.

of having a full battery control at single cell level.

CHAPTER

4 Converter modelling and control

The RCMC has been studied in three different operative conditions:

- Motor drive. The RCMC is employed to power a motor.
- Charging setup. The RCMC is directly connected to an AC grid to perform different charging strategies for the battery cells installed.
- Battery Energy Storage System (BESS) application. The RCMC is here directly connected to a low-voltage grid to storage or deliver power, according to the grid needs.

Each of the three case studies requires a different control strategy with customized battery system management algorithms to ensure the standards of the specified application. In the following sections, each setup will be described and the simulation results will be shown to validate the RCMC topology.

4.1 RCMC in Motor Drive

Fig. 4.1 shows the circuital setup of a motor drive application consisting in five main elements: (1) speed and torque control loops, (2) sorting algorithm block, (3) gate signals evaluation block, (4) converter and (5) PMSM motor. By following the block enumeration, the features of the motor drive are explained.

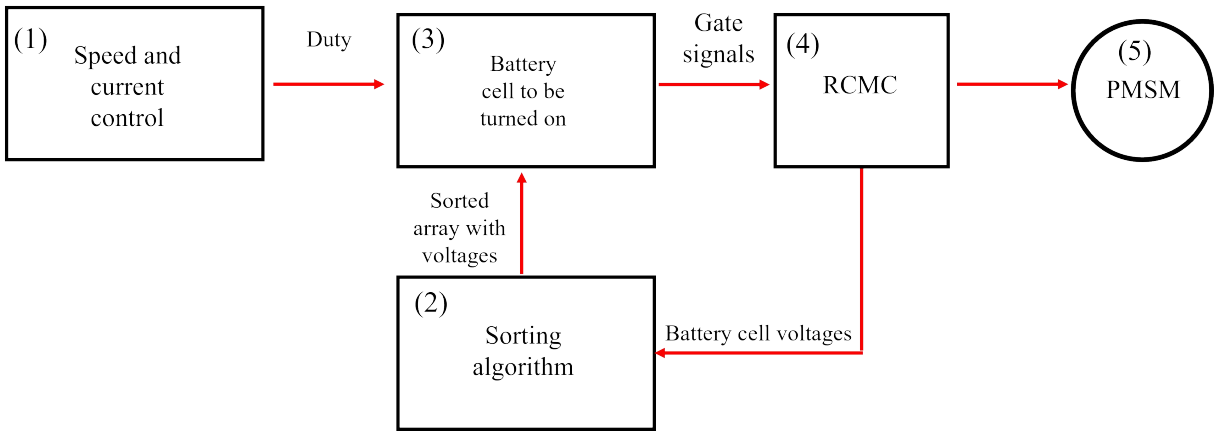


Figure 4.1: Motor drive scheme.

(1) The speed and torque control loops are responsible for evaluating the reference voltage signals for the three phases of the converter. They are implemented by a cascaded placement of two PI controllers in the dq reference frame, as shown in Fig. 4.2. The outer and inner loops are responsible for the speed and torque controls, respectively. Depending on the motor speed reference value - greater or less than the basis speed - the field weakening control is activated. The voltage references computed by the internal PIs are then transformed in abc reference and divided by the average battery voltage value to obtain the required number of cells to be inserted. (2) The sorting algorithm block receives as input all the battery cell voltages and returns as output an array with the position of the battery cells to be activated in each submodule of the three phases. This block does not only implements various sorting algorithms but also double-checks that the prohibited configuration is not selected. In other words, this block allows a double layer control: on one side, the battery cells are sorted according to customized requirements (i.e. SOC and thermal management); on the other side, the result of the previous algorithms is always checked in order to avoid the shorting out of the battery cell in second position in any of the RBMs installed. (3) The gate evaluation block merges the results of the control loops and the sorting algorithms. Indeed, the function implemented in this block activates the number of cells required by the control loops in the position decided by the sorting block. (4) The converter receives the gate signals and (5) drives the motor according to the reference signals of speed and

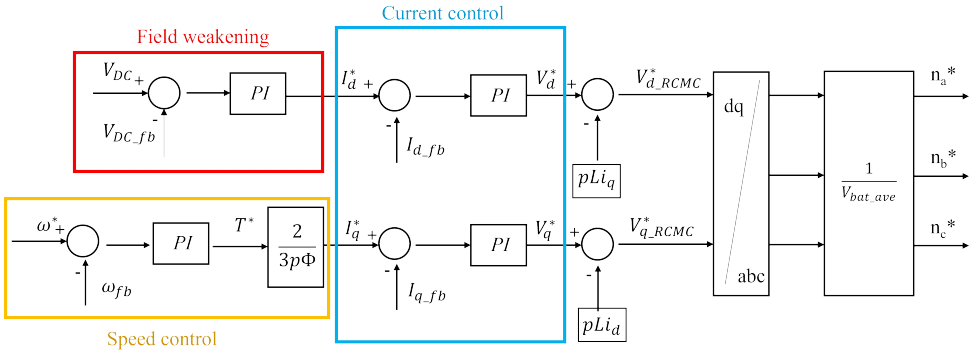


Figure 4.2: Speed and torque control scheme.

torque.

4.1.1 Speed and torque control modeling

The voltage equations of a PMSM motor in dq axis can be written as:

$$V_d = Ri_d + L_d\frac{di_d}{dt} + pwL_di_q \tag{4.1}$$

$$V_q = Ri_q + L_q\frac{di_q}{dt} + pwL_qi_d + pw\phi \tag{4.2}$$

where R is the stator resistance, ω is the motor speed, p is the number of pole pairs, ϕ is the motor flux and $V_{d,q}$, $L_{d,q}$, $i_{d,q}$ are the voltages, inductances and currents along the d and q axis, respectively. Specifically, for the isotropic PMSM, the inductances along the dq axis are equal, therefore:

$$L_d = L_q = L \tag{4.3}$$

The torque equation is equal to:

$$T = \frac{3\ i_q\ p\ \phi}{2} \tag{4.4}$$

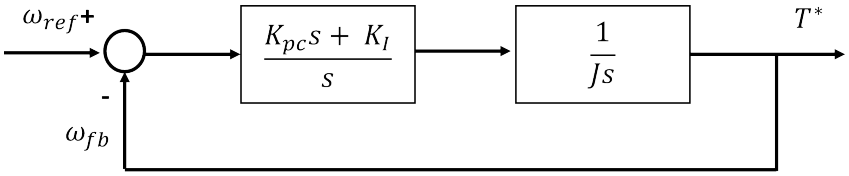


Figure 4.3: Speed loop diagram.

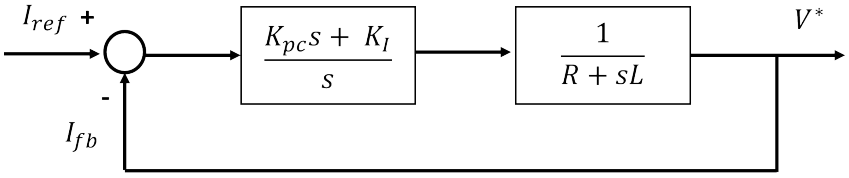


Figure 4.4: Current loop diagram.

PI design for operative conditions $\omega \leq \omega_{basis}$

In this subsection, the tuning procedure for the current and speed - for $\omega \leq \omega_{base}$ - PI controllers is explained. The calculation of the proportional and integral gains starts with the evaluation of the plants:

- for the current loop, the plant consists in the stator resistor R and inductance L;
- for the speed loop, the plant consists in the motor inertia J.

In Fig. 4.3 and 4.4, the current and speed loops are shown, respectively. As it can be noticed, the coupling terms $pwLi_q$ and $pwLi_d$, for the d and q axis respectively, are added after the PI controllers action, as shown in Fig. 4.2.

With reference to Fig. 4.3, the transfer function in open loop can be written as:

$$G_s(s) = \frac{K_{ps}s + K_{is}}{Js^2} \tag{4.5}$$

where K_{ps} and K_{is} are the proportional and integral gains of the speed control PI. The inner current control loop is not considered because the dynamic is much faster than the speed one. The transfer function for the closed loop can be written as:

$$H_s(s) = \frac{H_s(s)}{1 + H_s(s)} = \frac{1}{s^2 + \frac{sK_{ps}}{J} + \frac{K_{is}}{J}} \tag{4.6}$$

K_{ps} and K_{is} can be decided by comparing term by term the denominators of (4.6) and of the transfer function of a second order system:

$$C(s) = \frac{1}{s^2 + 2\omega_n\xi + \omega_n^2} \tag{4.7}$$

where ξ is the damping ratio and ω_n is the natural frequency of the system. Therefore:

$$K_{ps} = 2\xi\,\omega_n J \tag{4.8}$$

$$K_{is} = \omega_n^2 J \tag{4.9}$$

The output value of the speed control loop is the reference Torque $T*$ signal, which is divided for the constant $\frac{1}{\frac{3}{2}\ p\ \phi}$ to obtain the reference value for the $i*_q$, according to (4.4). Regarding the d-axis, the optimum control of a PMSM forces the reference signal $i*_d$ equal to 0.

The PI controller gains K_{pc} and K_{ic} for the current control can be tuned with the same procedure described above. The transfer function in open loop for the current control is equal to:

$$G_i(s) = \frac{K_{pc}s + K_{ic}}{s(R + sL)} \tag{4.10}$$

In closed loop, the transfer function can be written as:

$$H_i(s) = \frac{H(s)}{1 + H(s)} = \frac{1}{s^2 + \frac{s(K_{pc}+R)}{L} + \frac{K_{ic}}{L}} \tag{4.11}$$

K_{pc} and K_{ic} can be decided by comparing term by term the denominators of (4.11) and of the transfer function of a second order system (4.7), obtaining:

$$K_{pc} = 2\xi\omega_n L - R \tag{4.12}$$

$$K_{ic} = \omega_n^2 L \tag{4.13}$$

PI design for operative conditions $\omega > \omega_{base}$

When the motor is required to work in a speed range greater than its basis speed, the field-weakening control is enabled. Basically, the d-axis flux is reduced by lowering the air-gap flux linkage of the permanent magnets. This effect is obtained by de-magnetizing the d-axis stator current, forcing a negative reference value. In terms of control, this action is done by placing a PI controller on the d-axis, forming an outer control loop whose output becomes the reference signal for the inner current control. The tuning procedure for the field-weakening PI starts with finding the relationship between the stator voltage and the d-axis current. Assuming that:

$$v_s^2 = v_d^2 + v_q^2 \tag{4.14}$$

and replacing (4.1) and (4.2) - the transient terms $L\frac{di_d}{dt}$ and $L\frac{di_q}{dt}$ are neglected - and placing $p\omega = \omega_e$ - being ω_e the electrical speed -, in (4.14), it is possible to write:

$$v_s^2 = (\omega_e L i_q)^2 + (\omega_e L i_d + \omega_e \phi)^2 \tag{4.15}$$

By solving the products and dividing for $\omega_e L$:

$$(\frac{v_s}{\omega_e L})^2 = i_q^2 + i_d^2 + (\frac{\phi}{L})^2 + 2(\frac{i_d \phi}{L}) = i_q^2 + (i_d + \frac{\phi}{L})^2 \tag{4.16}$$

Solving the equation for v_s, the non-linear relation with i_d is found:

$$(\frac{v_s}{\omega_e L}) = \sqrt{(i_q^2 + i_d^2 + (\frac{\phi}{L})^2 + 2(\frac{i_d \phi}{L})} \tag{4.17}$$

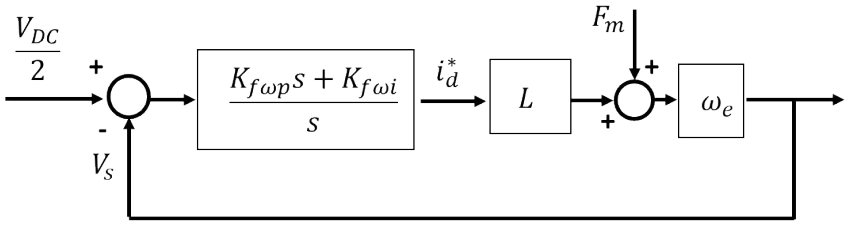


Figure 4.5: Field weakening loop.

At this point, the field weakening dynamic is assumed much slower than the current one; therefore, i_d and i_q can be considered independent and (4.17) can be written as:

$$\frac{(\frac{\delta v_s}{\omega_e L})}{\delta i_d} = 0.5(2 \cdot i_d + 2 \cdot \frac{\phi}{L}) = i_d + \frac{\phi}{L} \tag{4.18}$$

Finally, the derivative of v_s on i_d is equal to:

$$\frac{\delta v_s}{\delta i_d} = \omega_e(L i_d + \phi) \tag{4.19}$$

Once the plant is found, a PI controller is inserted in the chain loop; Fig. 4.5 shows the field weakening control loop diagram. The closed loop transfer function can be written as:

$$H_{fw} = \frac{L\omega_e(K_{fwp})s + K_{fwi}}{(1 + L\omega_e K_{fwp})s + L\omega_e K_{fwi}} \tag{4.20}$$

By placing K_{fwp} equal to 0, the control loop can be reduced to a first order system, with one pole in $\frac{-1}{K_{fwi} L\omega_e}$ [79]. The K_{fwi} value is set according to the required time response of the loop.

4.1.2 Sorting algorithm

The main feature of the RCMC is the possibility to directly access each battery cell, allowing a continuos monitoring of the working conditions of the battery cells. Several control algorithms may be developed, depending to the priority given to the battery cell parameters. For example, the SOC balancing may be preferred to the thermal management and vice versa. Furthermore, the algorithm may be structured in different layers and prioritize both thermal management and

SOC balancing with different timings.

For the motor drive application, two algorithms have been developed categorized as it follows:

- SOC balancing prioritization: battery cells are inserted according to their state of charge, in descending order.
- Losses reduction prioritization: the average state of charge of the battery modules within each submodule is computed. The insertion is performed placing in progressive order the battery cells belonging to the less charged submodules.

As it was specified in the previous chapter, the number of switches in conduction decreases as the number of battery cells inserted increases. To explain why the second criterium has better performance in terms of converter efficiency, let's assume to have nine battery cells to be inserted. The first criterium chooses the nine cells according to their SOC values, with no clue to which submodules they may belong. In the worst case scenario, the criterium may insert one battery cell belonging to nine different submodules. In that case, the number N_{Isw} the RBMs switches in conduction would be:

$$N_{Isw} = N_{SM} \cdot N_{sw} \tag{4.21}$$

Where N_{SM} is the number of submodules with one inserted battery module and N_{sw} is the number of RBMs switches in conduction. Taking as reference the architecture E defined in the previous chapter, in each submodule there are 3 RBMs: one of them has four switches in conduction to insert one battery module, while the other two are in bypass configuration by turning on the three lateral switches. Therefore, in each submodule there are 10 switches in conduction and the total number can be calculated as:

$$N_{Isw} = 9 \cdot 10 = 90 \tag{4.22}$$

On the contrary, the second criterium inserts the battery cells according to the average SOC value of the whole submodule. Therefore, the nine battery cells will be inserted by completing

the submodule before moving to the next one. Therefore, the number of RBMs switches in conduction would be:

$$N_{IIsw} = N_{SM} \cdot N_{sw} = 1 \cdot 6 = 6 \tag{4.23}$$

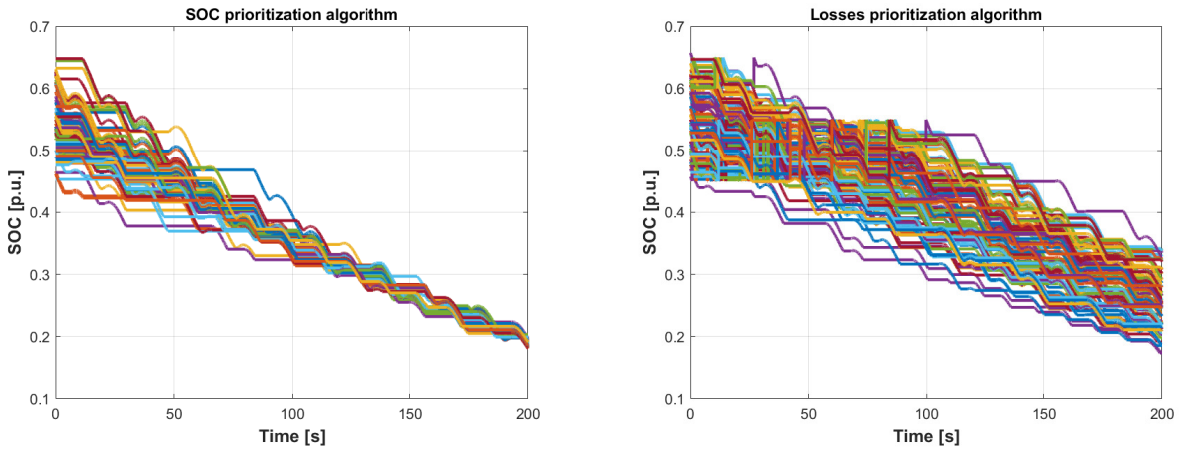
Indeed, all RBMs are inserted and the number of switches in conduction drastically decreases.

According to the SOC values of the battery modules installed within the RCMC, the two algorithms return different range of power losses. In the worst-case scenario above described, the second method provides a reduction R_{cl} of the conduction losses equal to the 93% compared with the first method, calculated as:

$$R_{cl} = 100 \cdot \frac{N_{IIsw}}{N_{Isw}} = 100 \cdot \frac{6}{90} = 93\% \tag{4.24}$$

As an example, the two algorithms have been tested with a group of 108 cells with initial SOC values in the range between 0.45 and 0.65. The test is carried out under the same condition of current and number of battery cells simultaneously inserted. In Fig. 4.6, the SOC values of all battery modules are reported for the two algorithms, respectively. By using the SOC balancing prioritization method, the final difference between all battery modules SOC values is less than 3%. After half of the discharging time, the SOC values converge and prosecute the working conditions in balanced way. On the other hand, the loss reduction prioritization method requires more time for the SOC values to converge. Under the same condition of discharging time, the final difference between the battery cells is less than the 13%. The main drawback of this method is that the accuracy of the final SOC values range is strictly dependent on the position of the less charged battery modules.

Finally, both methods are valid options according to different application requirements. If the battery modules within the phases are quite balanced, the second algorithm may be a good solution to reduce the overall losses. On the contrary, when the battery cells have unbalanced SOC values within the submodule, the first method would be a preferred solution to prioritize the



(a) (b)

Figure 4.6: (a)SOC and (b) Losses prioritization sorting algorithms.

balancing dynamic.

4.1.3 Simulation results

The motor drive setup has been simulated to test the RCMC features over the operative conditions of the PMSM motor. The motor parameters are listed in Table 3.2 and its torque speed is shown in Fig. 3.6. The RCMC architecture chosen is the E, already discussed in the previous chapter. The system has been simulated over all torque-speed area; as indicator of the converter performance, three working points are here presented:

- Working point 1 - Torque = 129Nm and speed= 50rad/s - represents the lowest power operative condition. In this scenario, the validation mainly concerns the motor current THD values.
- Working point 2 - Torque = 320Nm and speed= 344rad/s - represents the nominal power condition. In this scenario, the focus is addressed to the sorting algorithm performance.
- Working point 3 -Torque = 129Nm and speed= 1050rad/s - represents the last field-weakening working point. In this scenario, the converter works at his nominal voltage and

current ratings with the maximum output frequency, given by the motor speed.

In the following, each working point will be analysed together with the performance of the two sorting algorithms described above.

Working point 1

In Fig. 4.7 the RCMC voltages and currents are shown. The voltage waveforms resemble a PWM shape at the top: the reference signals oscillate because the required voltage is at the minimum power working conditions. In this case, the low voltage condition algorithm is activated. However, although the motor works at the minimum value of torque and speed, the number of voltage levels is enough to guarantee a satisfying THD current value. In Fig. 4.8, the THD value and the harmonics diagram computed by the fft tool in Matlab powergui are shown. In Fig. 4.9, the torque and speed waveforms are shown with their reference values.

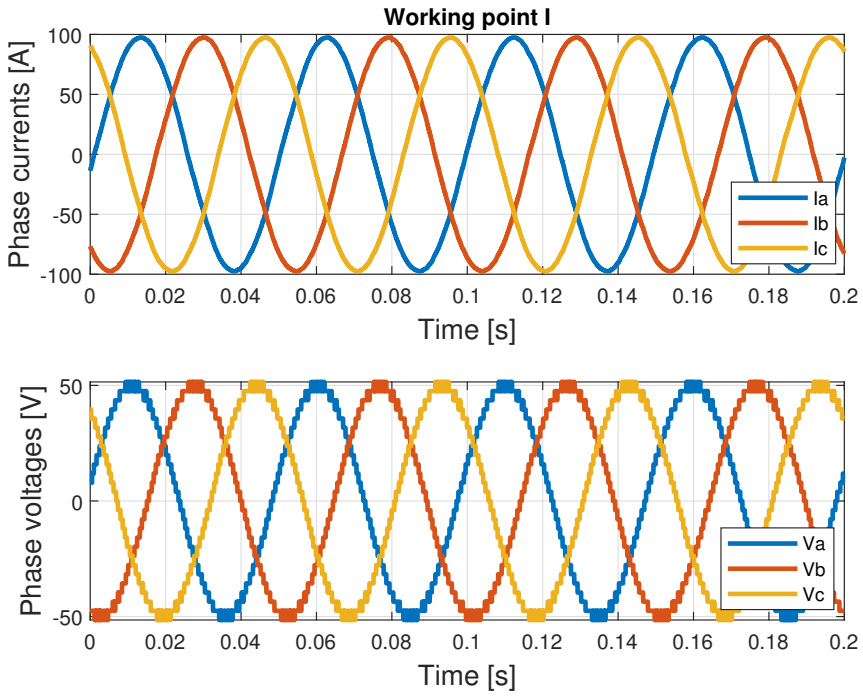


Figure 4.7: Working point I: three-phase voltages and currents.

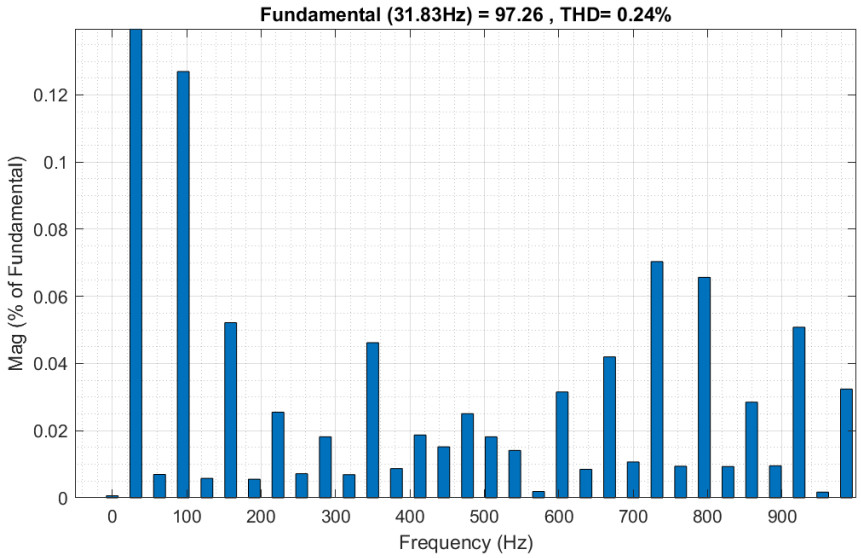
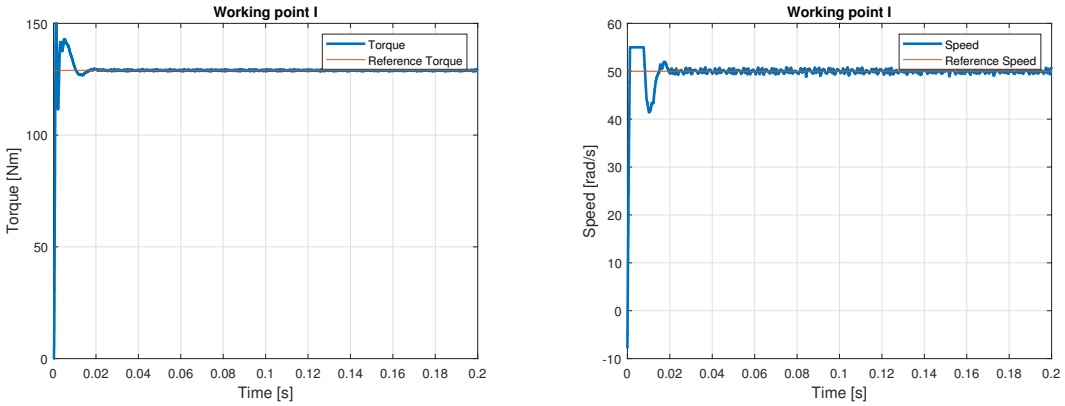


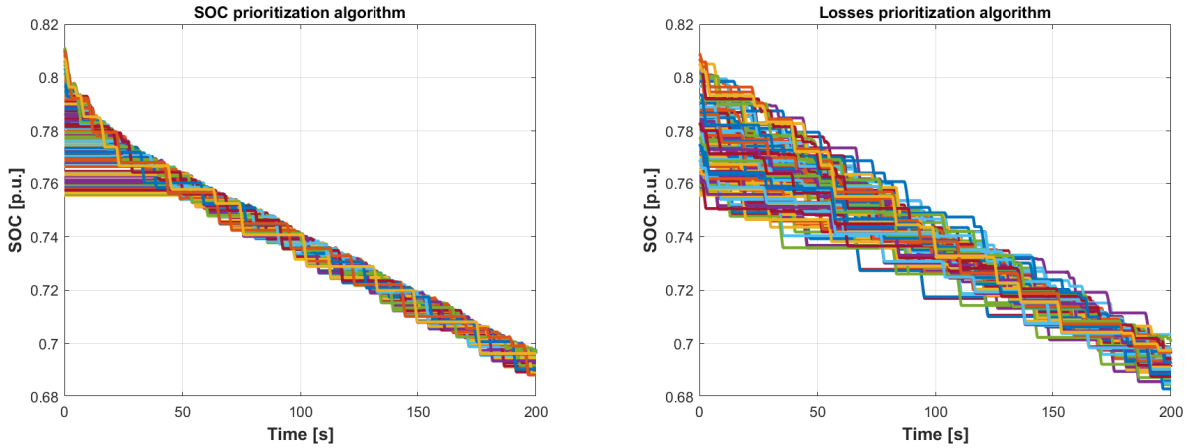
Figure 4.8: Working point I: THD value and harmonics diagram.



(a) (b)

Figure 4.9: Working point I: (a) Torque, (b) Speed reference and feedback values.

As shown in Fig. 4.10, both sorting algorithms have efficient results because the number of battery cells to be inserted at each cycle is low enough to guarantee effective rotation in the battery cells insertion. Therefore, in this scenario, even if the SOC prioritization algorithm is more effective in terms of balancing, the losses prioritization algorithm has satisfying results.



(a) (b)

Figure 4.10: Working point I: SOC trend for the battery cells according to the (a) SOC and (b) Losses prioritization sorting algorithms.

Working point 2

The three-phase voltages and currents are shown in Fig. 4.11. In steady-state, the three-phase voltages assume a sinusoidal shape, discretized in 217 levels, which brings the current THD value equal to 0.12%. In Fig. 4.12, the THD value and the harmonics diagram computed by the fft tool in Matlab powergui are shown. In Fig. 4.13, the torque and electrical speed are shown compared with the reference signals. After a small transient dynamic, the torque and electrical speed stick to the reference values.

The effectiveness of the sorting algorithms is a crucial point in this working conditions: during half period of the fundamental frequency all the battery cells are selected, increasing the time needed to balance the SOC values. As shown in Fig. 4.14, the SOC prioritization is more efficient than the losses one, making the usage of the latter one discouraged in case of significant unbalanced initial SOC values.

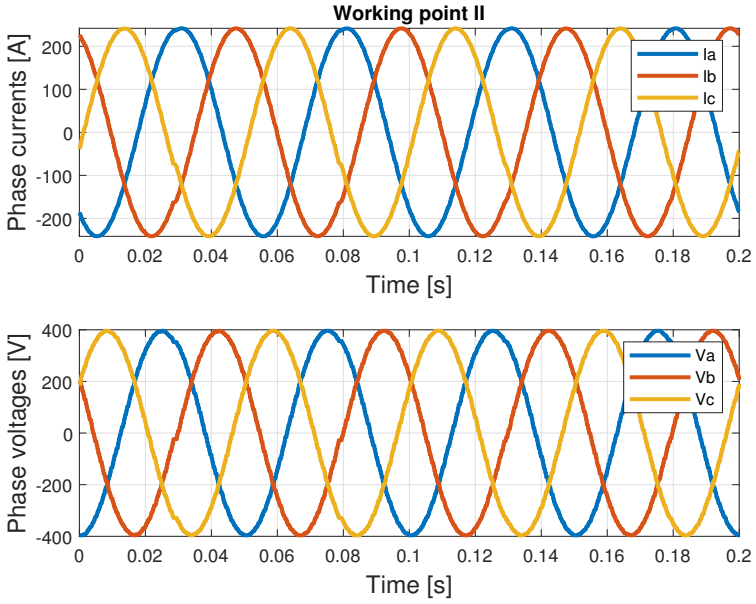


Figure 4.11: Working point II: three-phase voltages and currents.

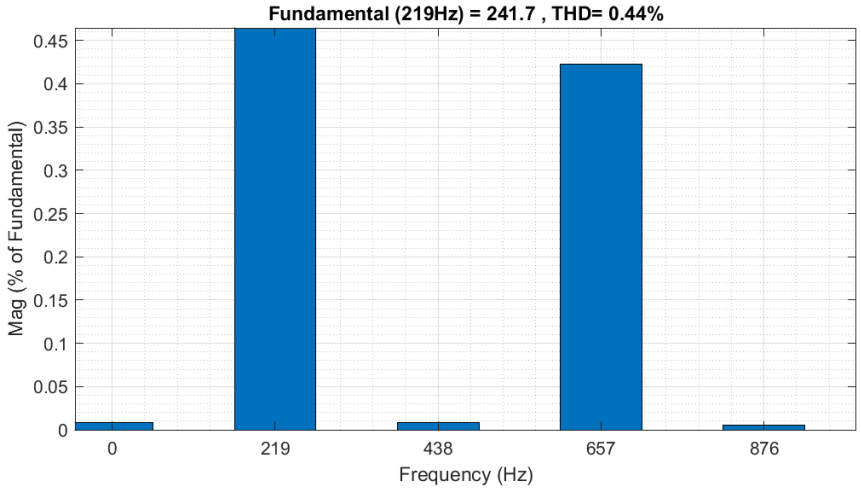
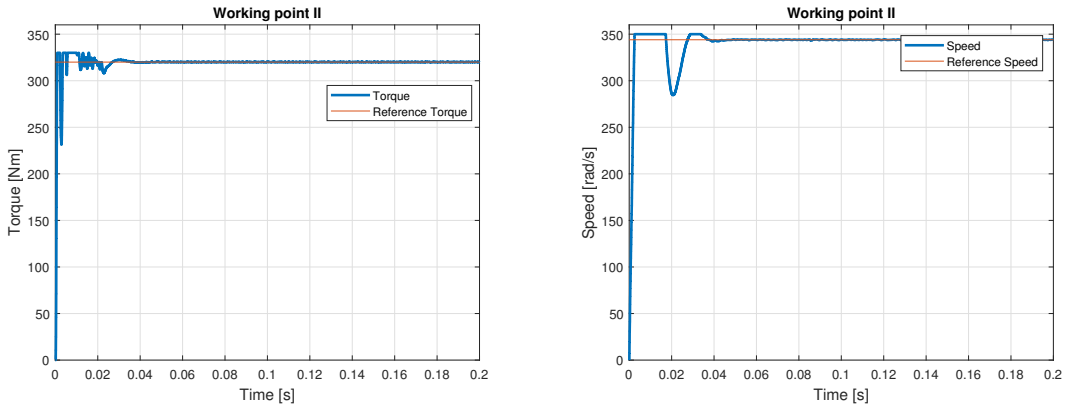


Figure 4.12: Working point II: THD value and harmonics diagram.

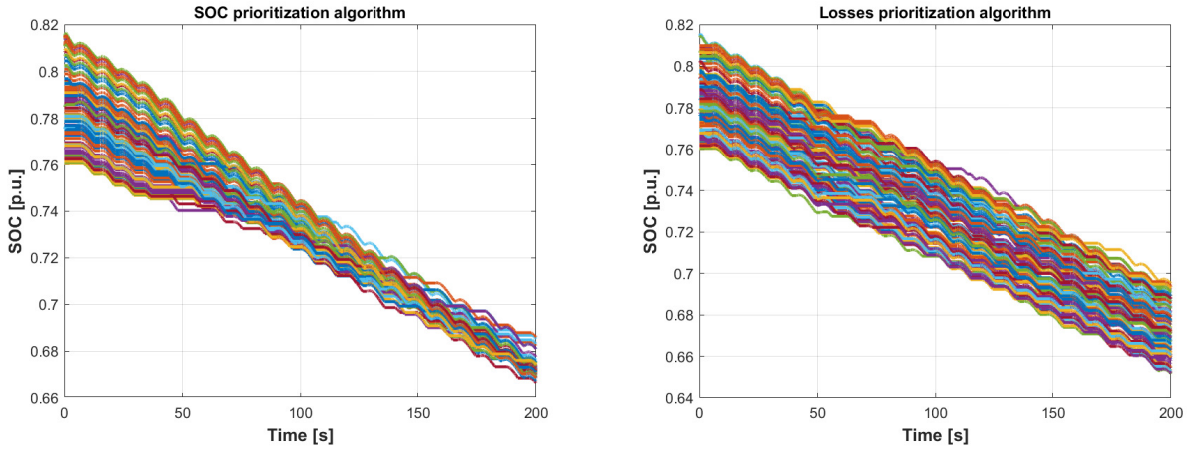
Working point 3

In Fig. 4.15 the RCMC voltages and currents are shown. As for the previous working point, the voltage and current waveforms assume a sinusoidal shape, with a THD value equal to 0.32%, reported in Fig. 4.16. In Fig. 4.17, the torque and speed waveforms are shown with their reference



(a) (b)

Figure 4.13: Working point II: (a) Torque, (b) Speed reference and feedback values.



(a) (b)

Figure 4.14: Working point II: SOC trend for the battery cells according to the (a) SOC and (b) Losses prioritization sorting algorithms.

values: the field-weakening control drives the motor at its maximum speed.

Even in this case, the SOC prioritization algorithm is more encouraged compared to the losses one because the number of battery cells inserted in half period of the fundamental frequency corresponds to the maximum number. Therefore, the sorting algorithm can only work on the insertion order which is less effective than rotating the battery cell activation over different fundamental periods. Both sorting algorithms results are shown in Fig. 4.18.

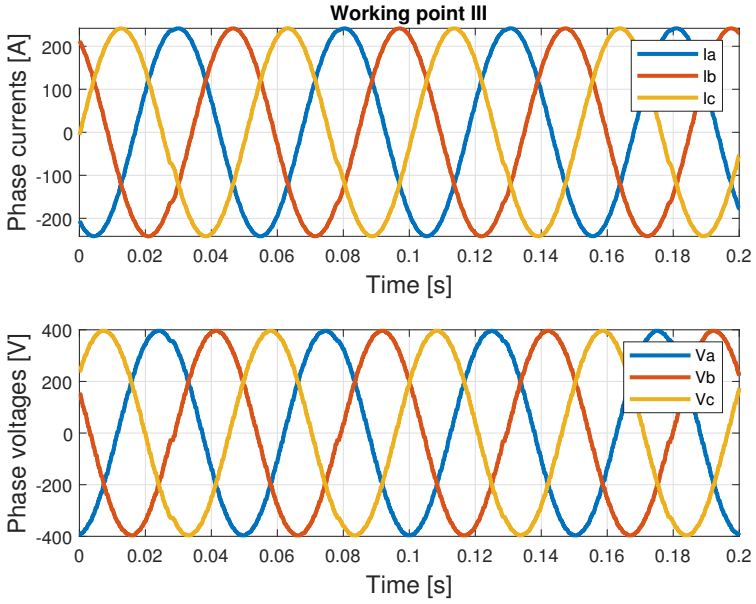


Figure 4.15: Working point III: three-phase voltage and currents.

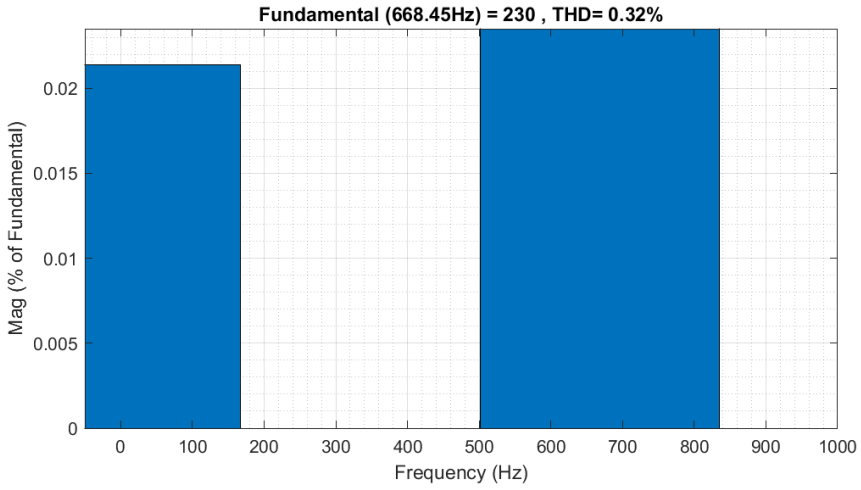
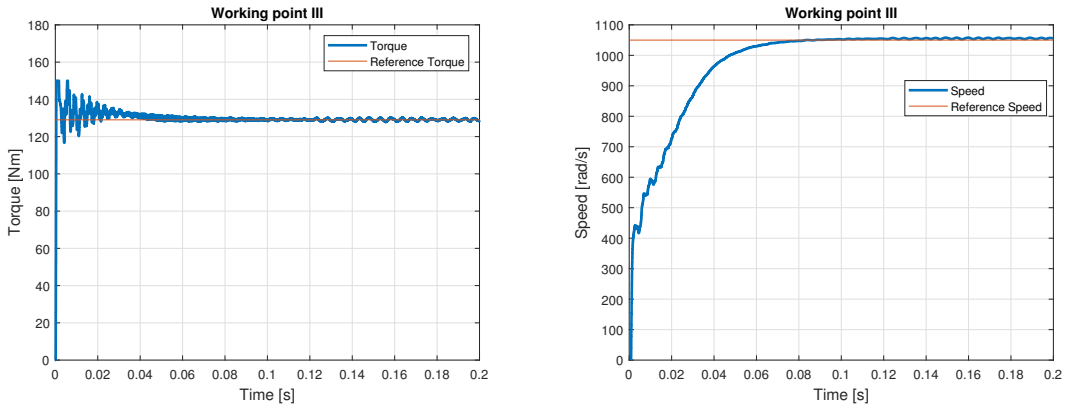


Figure 4.16: Working point III: THD value and harmonics diagram.

4.2 RCMC in charging configuration

This section analyses the three-phases RCMC in charging configuration [80]. This case study assumes to charge the battery cells within one EV RCMC, by connecting it to an AC three-phase

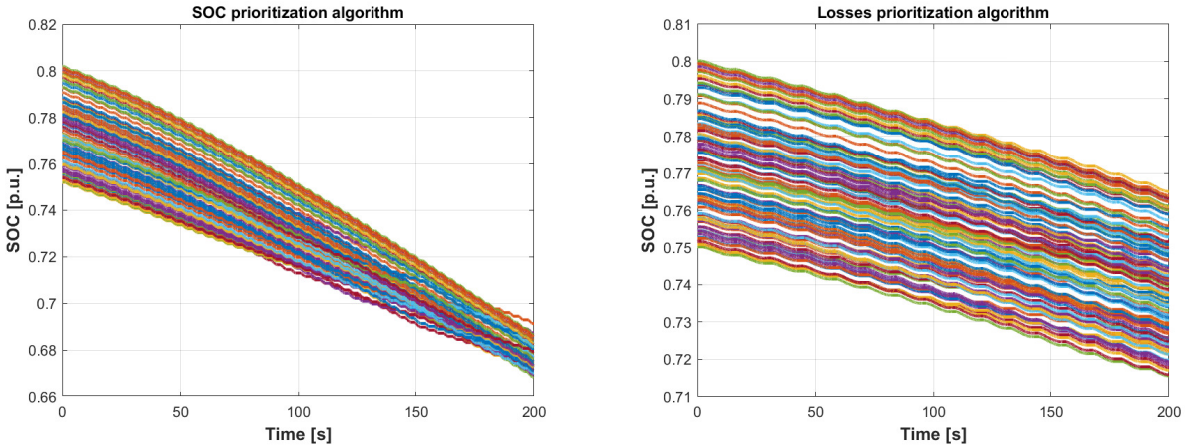


(a) (b)

Figure 4.17: Working point III: (a) Torque, (b) Speed reference and feedback values.

power system, which can be identified in the AC grid or in any other dedicated system. In contrast to the current charging infrastructures, which may require middle-stage converter – "on - board charger" or AC/DC power conversions -, the configuration here investigated permits a direct connection between the RCMC and the power system.

This application study requires firstly the study of the AC system requirements and the control.



(a) (b)

Figure 4.18: Working point III: SOC trend for the battery cells according to the (a) SOC and (b) Losses prioritization sorting algorithms.

Once the system parameters are described, the filter design calculations are carried out with a new method, fitted for converters modulated with the Nearest Level Modulation. Finally, to validate the presented system, a time comparison for charging process, assuming to connect a battery pack and the RCMC to a 2-level AC charging station, is performed.

4.2.1 AC system requirements and control

The AC power system needs to be rated according to the nominal values of current and voltage required for the charging process. Taking Fig. 4.19 as reference and assuming to have a symmetrical three-phase system, the charging current I_{ch} can be approximated as:

$$I_{ch} = \frac{V_{ps} - V_{RCMC}}{Z} \tag{4.25}$$

Given the maximum value of the charging current I_{ch_max} and considering that V_{RCMC} depends on the state of charge of each battery module,V_{ps} must respect the following constraint:

$$V_{ps} \leq ZI_{ch\_max} + V_{RCMC} \tag{4.26}$$

where

$$V_{RCMC} = 3 \cdot N_{RBM} \cdot V_{batmin} \tag{4.27}$$

where N_{RBM} is the overall number of RBMs installed in one phase and V_{batmin} is the minimum admitted voltage of battery cells.

For this case study, it has been assumed to connect the RCMC to a 2-level AC charging station, whose ratings are 400 Vac and 80 A rms value as charging current [81]; the RCMC architecture is the same as for the Motor Drive application. Table 4.1 describes the RCMC characteristics and the AC system nominal ratings.

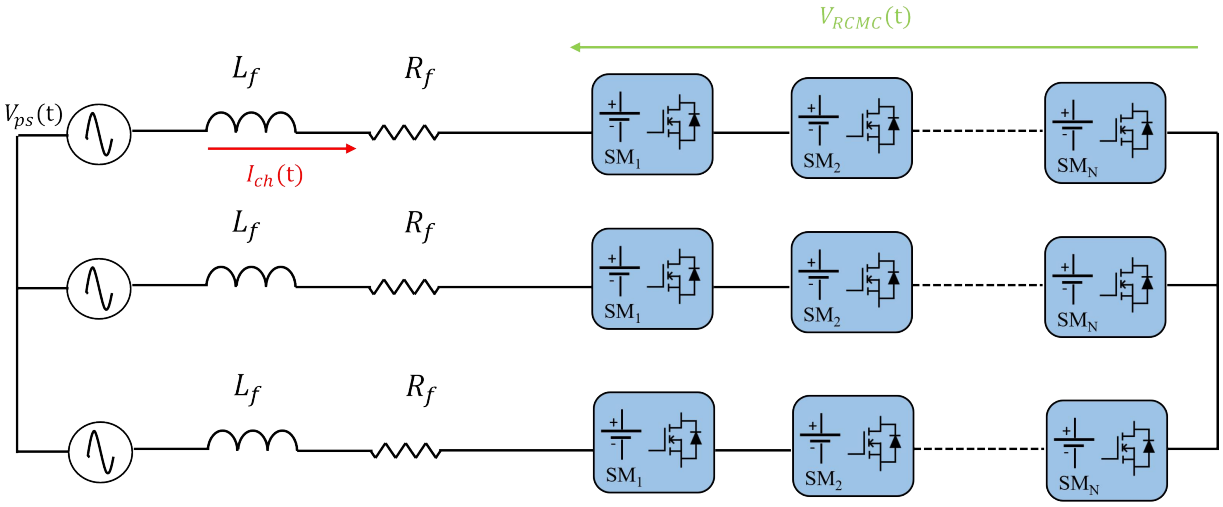


Figure 4.19: RCMC connected to an AC power system.

Table 4.1: RCMC and AC system characteristics.

Parameter	Value	Measurement Unit
AC system peak voltage	325	V
AC system nominal current	80	A
Frequency	50	Hz
Number RBM per SM	3	-
Number SM per phase	12	-
DSP frequency	7	kHz
Modulation	Nearest Level Modulation	-

4.2.2 Filter design

The number of battery cells to be inserted simultaneously during the charging process is obtained by estimating the voltage drop on the filter. Therefore, an analysis to evaluate the required value for the inductance value has been carried out. It is important to highlight that the computation considers that the converter generates the exact value of the reference sine wave voltage. In reality, the converter output voltage follows the reference voltage with a precision depending on the number of levels and their amplitude. For the RCMC, the error between the reference voltage and the converter output voltage can be considered negligible thanks to its high number of levels and the small amplitude of the voltage of each battery module compared to the AC system

voltage rating. In this case, the number of levels is 108 and the maximum value of each level corresponds to the maximum Li-Ion battery voltage equal to 4.2V. Compared to the AC system peak voltage, the maximum amplitude of the voltage level corresponds to the 1%.

The filter impedance is designed using the current ripple method. The inductor value is decided allowing a 5% of ripple on the nominal current value, calculated as:

$$\Delta I_L = 0.05 \cdot \sqrt{2} \cdot I_{chmax} = 5.7A \tag{4.28}$$

The calculation of the filter inductance for multilevel converters modulated with the Nearest Level Modulation is approached differently compared to the ones controlled by the Phase Shift PWM [82]. With NLM, the maximum voltage ripple seen from the filter inductance coincides with the maximum step amplitude computed by the modulation. Assuming T_{sw} as the switching period and T_{fp} as the period of the AC voltage, each quarter of T_{fp} the peak voltage is reached. In order to compute the maximum amplitude of the voltage step, it is firstly calculated the number of DSP cycles in one quarter of period:

$$N_{DSP} = \frac{T_{fp}}{4T_{sw}} \tag{4.29}$$

The sine voltage value computed by the DSP in each cycle can be calculated discretizing the sine wave as it follows:

$$V(i) = V_{ps} \cdot sin(\omega\ i\ T_{sw}) \text{ for } i = 1,2,...N_{DSP} \tag{4.30}$$

The amplitude of V_i is strictly dependent on T_{sw}: the faster is the DSP, the more are the intervals within one quarter of period and the smaller is the amplitude of the voltage intervals. The maximum voltage step is found where the sine slope is maximum and, therefore, where its derivative is maximum:

$$max(\frac{d[sin(\omega t)]}{dt}) = max(cos(\omega t)) \text{ when } t = 0 \tag{4.31}$$

The maximum voltage step can be then found as:

$$\Delta V_{max} = V_{ps} \cdot [sin(\omega t_1) - sin(\omega t_0)] \tag{4.32}$$

Where t_0 and t_1 are the extremes of the first interval of the DSP, as shown in Fig. 4.20. For the AC system here considered, N_{DSP} is equal to 35 and the maximum voltage ripple is equal to $15V$. Finally, the filter inductance value can be calculated as:

$$L_f = \frac{\Delta V_{max} T_{sw}}{\Delta I_L} = 375\mu H \tag{4.33}$$

The voltage drop on the inductance filter is equal to:

$$V_f = ZI_{chmax} = 2\pi f L I_{chmax} = 2\pi \cdot 50 \cdot 375\mu \cdot 80 = 9V \tag{4.34}$$

V_f is equal to the 3% of the nominal voltage installed within the RCMC, therefore it can be neglected and (4.26) can be rewritten as:

$$V_{ps} \leq ZI_{chmax} + V_{RCMC} \approx V_{RCMC} \tag{4.35}$$

Once defined the maximum value for V_{ps}, the charging current is controlled by implementing a conventional power control in dq coordinates [83], shown in Fig. 4.21. The control loops along the dq axis take as reference values the active and reactive power.

In the case of charging process, the power exchange concerns only the active power, related to the d - axis for the convention used. The reference values are then divided by the peak voltage of the AC system V_{ps}, to obtain a reference current value. Finally, a current control loop is developed where $ZI_{ch\_q} - V_{ps\_d}$ and $ZI_{ch\_d} - V_{ps\_q}$ are the decoupling terms for the d and q axis, respectively.

The PI controller gains are tuned according to the eq. 4.12 and eq. 4.13, since the plant structure is the same as the one shown in Fig. 4.4, where R and L are the filter resistance and inductance values, respectively.

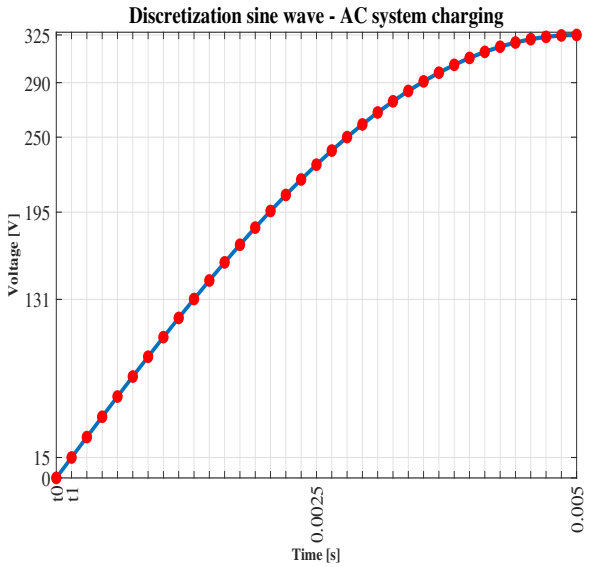


Figure 4.20: The red dots represent the voltage values for each Vi. The zoom in shows the maximum voltage ripple correspondent to the interval t0 - t1.

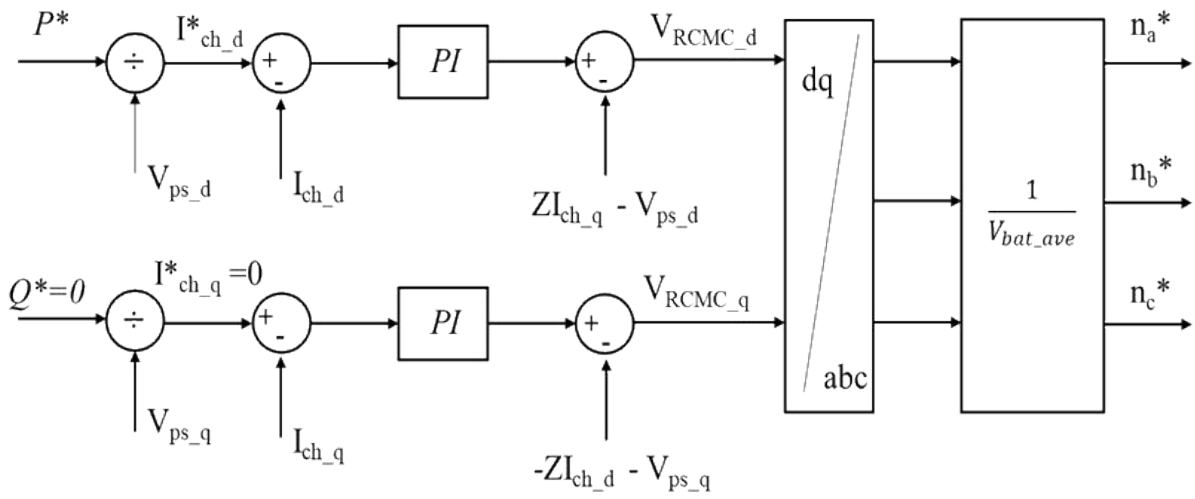
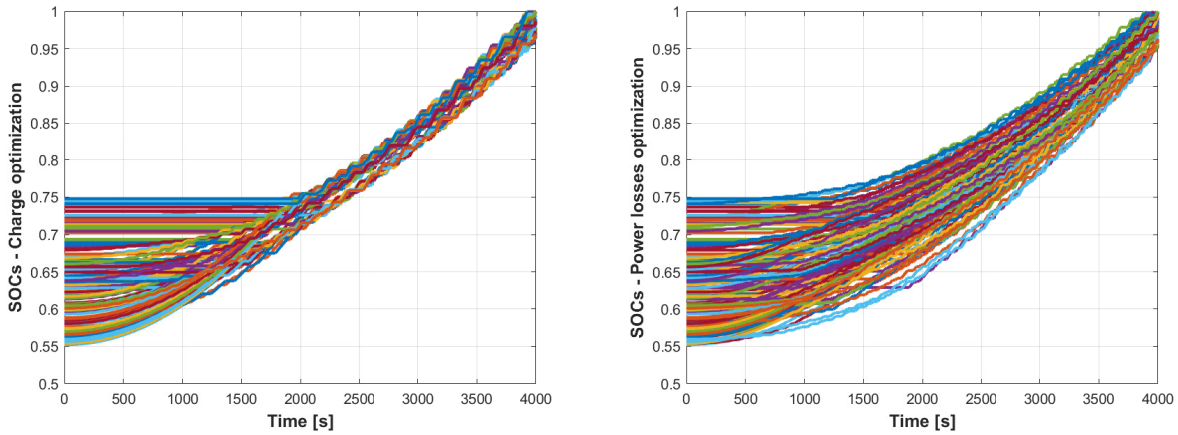


Figure 4.21: Current control in dq framework.

Sorting algorithms

The two sorting algorithms, described for the motor drive application, are also tested for the charging configuration. The initial SOC values of the battery cells are set in a range between 0.55



(a) (b)

Figure 4.22: SOC values trend for the (a) SOC and (b) loss reduction prioritization sorting algorithms.

and 0.75. As shown in Fig. 4.22 (a), the SOC prioritization algorithm is more effective in terms of voltage balancing: the difference between the SOC values is completely reduced after half charging time. On the other hand, as shown in Fig. 4.22 (b), the losses prioritization algorithm requires more time to converge the SOC values. As an indicator of performance between the two algorithms, starting with an initial SOC unbalance of 20%, the first algorithm obtains a final difference of 3%, while the second one reaches the 6%.

4.2.3 Charging time estimation

The aim of this section is the time estimation to charge the battery modules installed within the RCMC and a conventional battery pack. The charging architecture considered for the RCMC is depicted in Fig. 4.19, according to which the charging process can be performed by only controlling the converter itself; while the battery pack needs an on-board converter to perform an AC/DC conversion. It has been considered to install 80 kWh of energy within the RCMC and the battery pack and to have a primitive battery cell with 3.6V as nominal voltage and 2.6Ah as capacity. This analysis estimates the charging time needed to increase by 20% the SOC, assuming

all battery modules and the battery pack start with the same SOC value. In the following, the design and charging time estimation calculations for the battery pack and RCMC are described.

Battery pack

The most common voltage value for a classic battery pack ranges between 350 V and 500V. Therefore, a nominal voltage of 400 V has been chosen. The number of battery cells to be connected in series is equal to:

$$N_s = \frac{V_{bat\,pack}}{V_{bat}} = \frac{400V}{3.6V} = 111 \tag{4.36}$$

The overall capacity of the battery pack is calculated as:

$$C_{bp} = \frac{E_{bat\,pack}}{V_{bat\,pack}} = \frac{80kWh}{400V} = 200Ah \tag{4.37}$$

Therefore, the number of battery cells to be connected in parallel is equal to:

$$N_p = \frac{C_{bp}}{C_{bc}} = \frac{200Ah}{2.6Ah} = 77 \tag{4.38}$$

and the total number of battery cells within the battery pack would be:

$$N_{bp} = \frac{N_s}{N_p} = 8547 \tag{4.39}$$

The charging time for the battery pack can be calculated by applying the Coulomb counting [84]:

$$T_{chbp} = \Delta SOC \frac{3600 \cdot C_{bat}}{I_{ch}} = 0.2 \frac{3600 \cdot 200Ah}{80A} = 1800s \tag{4.40}$$

RCMC

The overall number of battery modules within each phase of the RCMC is equal to:

$$N_{b\_RBM} = 3N_{SM\_RBM}N_{SM} = 3 \cdot (12 \cdot 3) = 108 \tag{4.41}$$

The voltage installed per phase is equal to $388.8V$ and it is calculated as:

$$V_{phase} = N_{chbp}V_{bat} = 108 \cdot 3.6 = 388.8V \tag{4.42}$$

In this case, there is no serial connection between the battery cells because they are inserted within each RBM in groups of three. The overall capacity of the battery pack installed within the RCMC is calculated as:

$$C_{bpRCMC} = \frac{E_{bat\,pack}}{3V_{phase}} = \frac{80kWh}{3 \cdot 388.8} = 68Ah \tag{4.43}$$

Therefore, the number of battery cells to be connected in parallel is equal to:

$$N_{pRCMC} = \frac{C_{bpRCMC}}{C_{bc}} = \frac{68Ah}{2.6Ah} = 26Ah \tag{4.44}$$

Therefore, the total number of battery cells within the battery pack would be:

$$N_{bpRCMC} = \frac{N_{pRCMC}}{N_{sRCMC}} = 1 \cdot 26 \cdot 108 = 8424 \tag{4.45}$$

The RCMC charging time computation needs to consider that the SOC increment varies for each battery module, depending on the insertion order during the charging process. As shown in Fig. 4.23, the SOC increment has a parabolic trend, according to which the first battery module inserted has a greater SOC raise compared to the last one. Therefore, the estimation is implemented with an algorithm which calculates the SOC increment in each placement position and progressively alternates the insertion of the battery modules to perform a balanced charging. For the RCMC architecture, the charging time is strictly dependent on the voltage amplitude of the AC system and the voltage value of the battery modules. Indeed, assuming to have all the battery modules with same voltage values, the maximum number of them that can be charged

during one half period of the fundamental frequency:

$$N_{maxbat} = \frac{V_{ps}}{V_{bat}} \tag{4.46}$$

Therefore, the higher is V_{ps} and the lower is V_{bat},the more is the N_{maxbat}. For this analysis is assumed to consider the battery modules with the nominal voltage equal to $3.6V$. In this way, the flat part of the characteristic $SOC - V_{ocp}$ curve is considered and the module voltages do not significantly change over the charging process. Therefore, it is acceptable to assume that N_{maxbat} remains constant.

By applying (4.46), the maximum number of battery modules that can be charged simultaneously is equal to 90. The time estimation algorithm assumes to change the insertion position for each battery cell each second: i.e. the battery module n is inserted in first position for one second, then in second position for the next second and so on. The battery cell $n+1$ is inserted as second in the first second, as third in the next second and so on. When the number of seconds equals N_{maxbat}, the battery module $N_{maxbat}+1$ is used for the first insertion, until the first insertion is on the 90th battery module. This mechanism allows to perform a balanced charging dynamic taking into account the non-linear SOC increment trend over the insertion order.

Fig. 4.24 shows a SOC increment profile for one battery module and the zoom in during one charging interval respectively. The module is charged for 90s, in which recovers 90 insertion positions, and then it is excluded from the process for 17s. The overall time to perform 20% of SOC increment is equal to 1050s, which turns out to be more than 40% less than the time computed for the battery pack. Fig. 4.25 shows the SOC increment profiles for all battery modules. By varying the insertion position each second, the final charging dynamic results balanced and fast.

Finally, the RCMC can perform a faster charging process compared to the conventional battery pack, without the employment of external converters. Moreover, in case of different initial SOC values within the cells, the RCMC does not need the action of any BMSs, instead required for battery pack equalization processes.

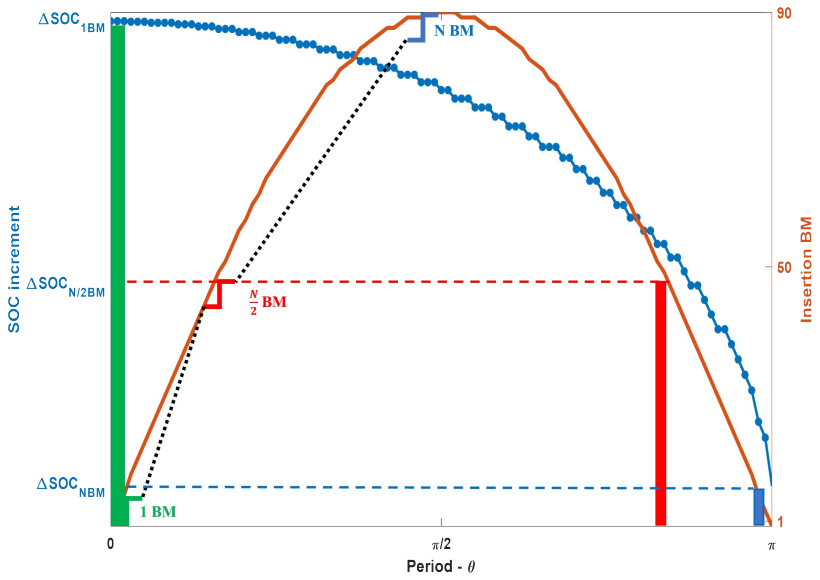
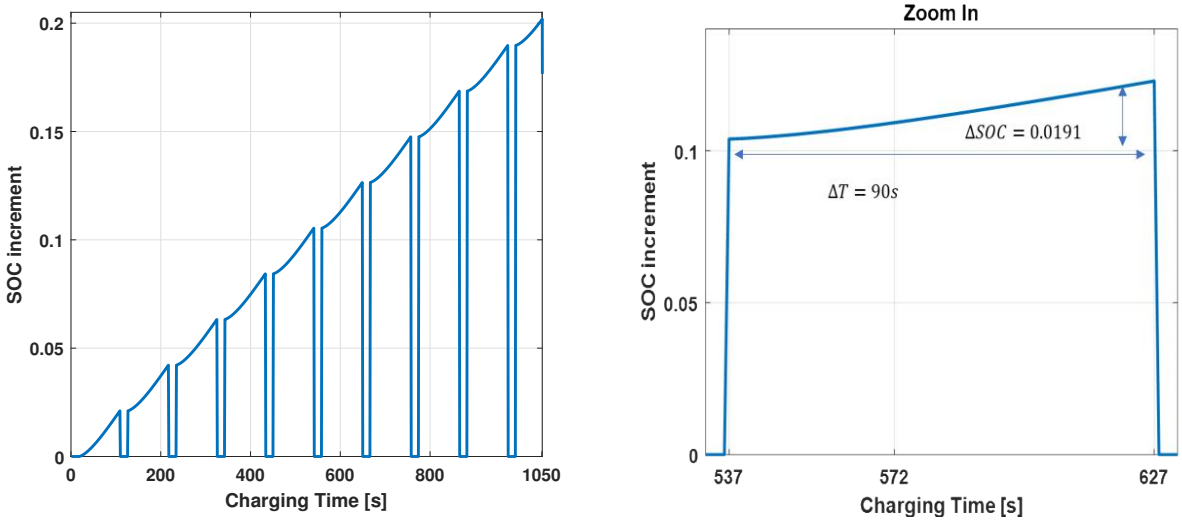


Figure 4.23: SOC increment according to the insertion order.



(a) (b)

Figure 4.24: (a) SOC increment for one battery module within the time. (b) Zoom in of the SOC increment in one charging interval: the battery module is inserted for 90s with a SOC increment equal to 0.00191.

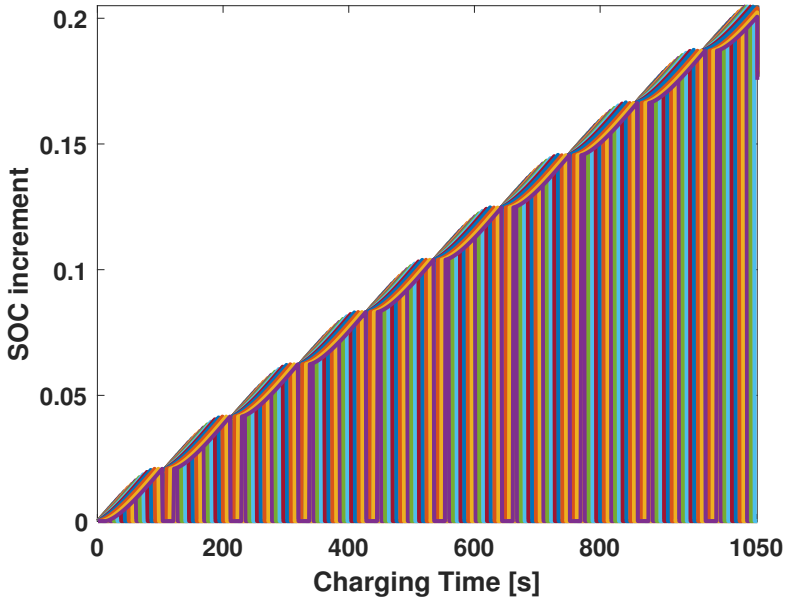


Figure 4.25: SOC increment trend for all battery modules within the charging time.

4.3 RCMC in BESS application

The scalable and modular structure of the RCMC makes it suitable for other applications beside the automotive field [85]. The possibility to separately access the battery cells in any moment of the operative conditions makes the RCMC advantageous for battery energy storage system (BESS) applications.

BESS has gained a fundamental role for the integration of renewable sources in the grid. Indeed, energy generated from photovoltaics and wind-turbine generators may be intermittent, creating undesired effects on voltage and frequency grid. Therefore, energy storage systems are usually installed close to renewable energy source to solve the consequent power-quality issues [86]. Initially, storage systems consisted in a unique battery pack whose voltage was converted in AC and then stepped up to the grid voltage to be connected. This structure presented the main disadvantages to be expensive – the step-up transformer costs are significant - and not efficient in terms of battery utilization. Therefore, in the last years, the majority of BESS have

been realized with multilevel converter topologies [87–89]. More specifically, the most used is the Cascaded H-Bridge (CHB), which permits different advantages. The storage system is divided in different battery packs, which are inter-connected and controlled by single H-Bridge converters. Its modular structure, then, allows to avoid the interface step-up transformer between the grid and the converter, to reduce the switching frequency and to obtain high quality output voltage waveform. Moreover, the CHB structure fits completely the BESS application thanks to the possibility to fully control the battery unit within one submodule, enhancing the fault tolerant and the implementation of balancing schemes, without the need of extra components. In this framework, the utilization of the RCMC would allow to exploit the battery cells potential at maximum, performing the balancing process always in active way and, in case of fault, the operation could continue by isolating the damaged part. Since the battery represents the 30%-50% of the cost of the overall structure, improving the management of the storage system would mean a significant saving. Considering that the batteries employed for BESS application are usually reconditioned from a previous applications, the necessity to efficiently manage their life cycle and operation acquires even more importance.

The feasibility and the beneficial impact of the RCMC in BESS application is validated by comparing it with a two-level inverter and a CHB - both described in detail in [82] -, in terms of filter design, power and battery losses.

4.3.1 RCMC design

The application taken in consideration requires a low voltage grid tie converter, therefore the voltage rating requested is equal to:

$$V_{phRCMC} = \sqrt{2} \cdot V_{AC} = \sqrt{2} \cdot 230V = 325V \tag{4.47}$$

Assuming to use $LiFePo_4$ battery cells - to be coherent with the reference citation [82]-, whose minimum voltage is equal to 2.8 V, the overall number of RBMs is:

Table 4.2: System BESS

System parameters	
Grid line to line voltage	325 V
Nominal current rms	51.96 A
Maximal battery voltage LiFePo4	3.6 V
Frequency	50 Hz
Two-level inverter	
Maximal DC link voltage	750 V
IGBT devices	FS100R12KT4G
Modulation	PWM
Switching frequency	8 kHz
CHB	
Maximal battery unit voltage	57.7 V
Submodules per phase	8
Mosfet devices	IPB036N12N3GATMA1
Modulation	Phase Shift PWM
Switching frequency	1 kHz
RCMC	
Maximal battery unit voltage	3.6 V
Submodules per phase	13
Mosfet devices per RBM	IPT004N03LATMA1
Mosfet device for H-bridge	NTMTS0D7N06CLTXG
Modulation	Nearest level modulation
DSP frequency	5 kHz

$$N_{RBM} = \frac{V_{RCMC}}{3 \cdot V_{batmin}} = \frac{325V}{3 \cdot 2.8V} = 39 \tag{4.48}$$

where 3 is the number of battery cells in each RBM. Assuming to use always the architecture E - characterized by 3 RBMs per submodule -, the number of submodules per phase will be equal to:

$$N_{SM} = \frac{N_{RBM}}{3} = \frac{39}{3} = 13 \tag{4.49}$$

Table 4.2 summarizes the key features of the converters and system simulated.

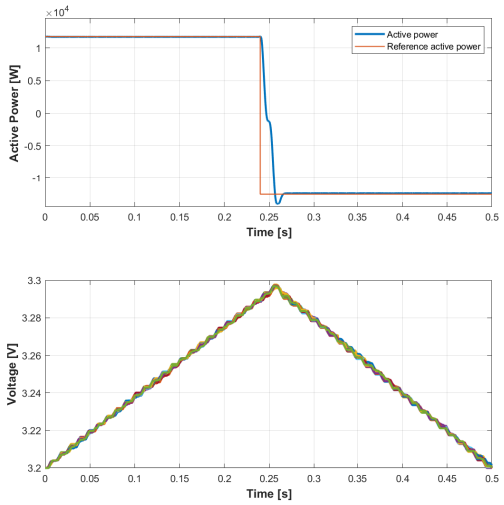


Figure 4.26: (a) Reference active power signal vs real active power. (b) Voltage battery cells when the converter is required to absorb power and to deliver power, respectively.

Control strategy

The control strategy requested for a converter used in BESS application should implement a power control which operates on top level, to supply the power fluctuations of the grid, and on local level, to guarantee the state of charge (SOC) balancing of the battery cells. Indeed, particular working conditions may affect the capacity of the battery units and it is important to compensate the differences between them through an accurate control. Therefore, the RCMC is controlled with a power control loop, shown in Fig. 4.21, combined with a sorting strategy in order to provide or absorb power keeping the system balanced. Fig. 4.26 shows the battery cells voltages in absorption and delivering phases, when the active power exchanged is assumed, by convention, positive and negative, respectively. The power control is implemented by modulating the converter with the Nearest Level Modulation. Indeed, the high number of levels of the RCMC, equal to 235, permits to have a negligible harmonic content in the output current even with low values of filter inductance.

4.3.2 Filter design

The filter inductance is designed according to the current ripple method. Allowing a 5% of maximum current ripple, equal to:

$$\Delta I = 0.05 \cdot \sqrt{2} \cdot I = 0.05 \cdot \sqrt{2} \cdot 51.96A = 3.67A \tag{4.50}$$

the CHB and the two-level inverter need an inductive filter of 3.9 mH and 6.4 mH. The inductive filter for the RCMC is computed by following the procedure explained in the previous section. By discretizing the sine wave in N_{DSP} cycles, obtained applying (4.29), it is possible to determine the maximum step voltage faced by the filter. Fig. 4.27 shows the intervals in which the sine wave is divided according to N_{DSP} with the maximum amplitude equal to 21 V. Therefore, the filter inductance can be calculated as:

$$L_{f\_BESS} = \frac{\Delta V_{max} T_{sw}}{\Delta I_L} = \frac{21V \cdot 200\mu s}{3.67A} = 1.2mH \tag{4.51}$$

The inductive filter required for the RCMC is 70% and 80% smaller than the two-level inverter and CHB, respectively. Moreover, the quality of the output power quality results to be extremely high even for low values of current. Fig. 4.28 shows the current waveforms for the RCMC, CHB and two-level inverter for the 10% of the nominal operative conditions. The RCMC guarantees the lowest THD in both conditions, even with the lowest inductive filter and switching frequency.

4.3.3 Power losses comparison

The three converters are compared in terms of power losses, consisting in converter and battery losses. The first ones are the result of the sum of conduction and switching losses. The second ones are due to the internal resistance of each battery cell. For BESS application, where battery cells work with a low value of C-rate, it is acceptable to assume that each battery cell has the same internal resistance, as stated in [90]. Assuming to not have any parallel connection between

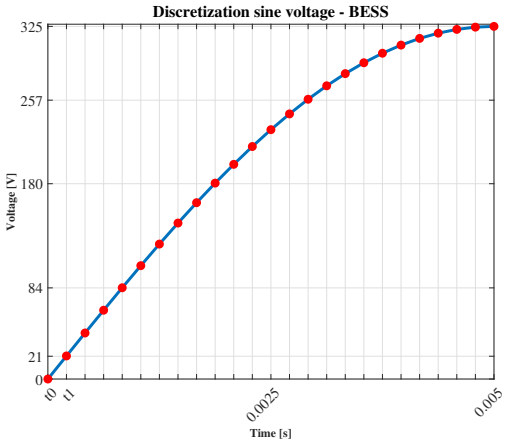


Figure 4.27: Sine wave discretization for filter design.

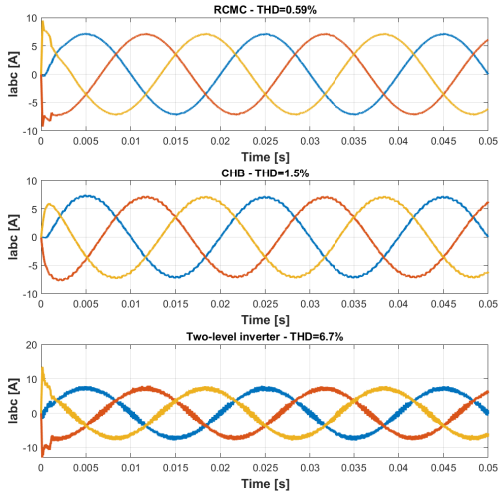


Figure 4.28: Current waveforms for the 10% of the nominal operative conditions. The RCMC provides the lowest THD.

the cells, but only one serial string, battery losses can be written as:

$$P_{bat} = N_s \cdot R_{int} \cdot I_{rms}^2 \tag{4.52}$$

where N_s is the number of cells connected in series within the battery pack, R_{int} is the internal resistance of each cell and I_{rms}^2 is the current flowing through the cells. The calculation method

of the power losses for the three converters is described in the following.

Two-level inverter

The IGBTs conduction and switching losses are evaluated with the Infineon software IPOSIM [91], designed to determine the power losses for Infineon components by deciding the voltage and current ratings, the operative temperature and modulation and the cooling system. The battery losses can be calculated with 4.52 , placing N_s equal to 208.

CHB

Switching losses are computed with PLECS, by modelling the thermal behaviour through the datasheet parameters [92]. Conduction losses can be written as:

$$P_{cond\_CHB} = 3 \cdot 2 \cdot N_{SM} \cdot R_{dson} \cdot I_{rms}^2 \tag{4.53}$$

Where 3 is the number of the converter phases, 2 is the number of switches always in conduction, N_{SM} is the number of submodules per phase and R_{dson} is the internal resistance of the MOSFETs. The battery losses cannot be calculated directly as in the two-level inverter. In the CHB, indeed, the battery units crossed by the flowing current depends on the number of active submodules in each moment. Therefore, battery losses must be computed by evaluating the instantaneous values of active submodules and current. The sum of the instantaneous contribution of the battery losses are then averaged on a period of the output fundamental frequency. Discretizing the computation, the battery losses can be written as:

$$P_{bat\_HB} = \frac{1}{k} \sum_{i=1}^{k} N_{SM}(i) \cdot N_s \cdot R_{int} \cdot I(i)^2 = \frac{1}{k} \sum_{i=1}^{k} N_{bat}(i) \cdot N_s \cdot R_{int} \cdot I(i)^2 \tag{4.54}$$

where k is the number of intervals in which is divided one period of fundamental frequency and N_s is the number of cells connected in one battery module.

RCMC

Switching losses can be neglected and conduction losses are calculated as stated in described in the previous section. Battery losses – as for the CHB – are computed by evaluating the instantaneous number of active battery cells within the RBMs and current values– and then, averaged on a period of the output fundamental frequency. The battery losses can be still written as:

$$P_{bat\_RCMC} = \frac{1}{k}\sum_{i=1}^{k} N_{bat}(i) \cdot R_{int} \cdot I(i)^2 \tag{4.55}$$

4.3.4 Results discussion

Fig. 4.29, 4.30 and 4.31 shows the converters, battery and overall systems efficiencies respectively. Fig. 4.29 shows that the two-level inverter has the largest power losses, but its efficiency increases with increasing power of the operative conditions. The CHB and the RCMC, instead, show a decreasing efficiency trend: the more is the power, the more is the current flowing in the power electronics converter. The two converters show comparable efficiency values, but the RCMC appears to be the most efficient for all operative conditions. Fig. 4.30 confirms the worst performance for the two-level inverter. The losses are significant because the fixed structure of the battery pack forces the load current to flow in each cell. Therefore, the higher is the current, the higher are the losses due to the internal resistance of each battery cell. On the other hand, the modular structure of the multilevel converters allows to activate only the necessary battery modules or cells, for the CHB and the RCMC, respectively, reducing the overall battery losses. Finally, the CHB has the highest efficiency, followed by the RCMC, whose efficiency decreases with the increase of the current. Fig. 4.31 (c) shows the overall system efficiency. The two-level inverter has the lowest efficiency, while the two multilevel converters have similar behaviour. The RCMC is more efficient for the lower current values, while the CHB reaches the top position for the highest values. Fig. 4.32 shows the three efficiency curves along the entire power spectrum.

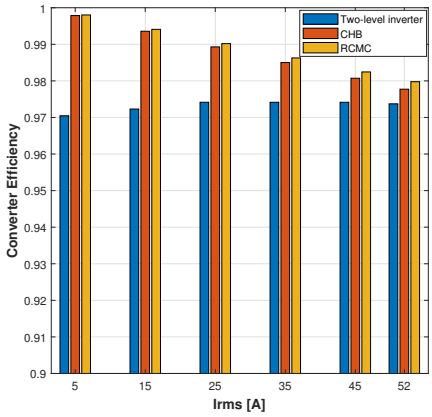


Figure 4.29: Comparison between converter efficiencies.

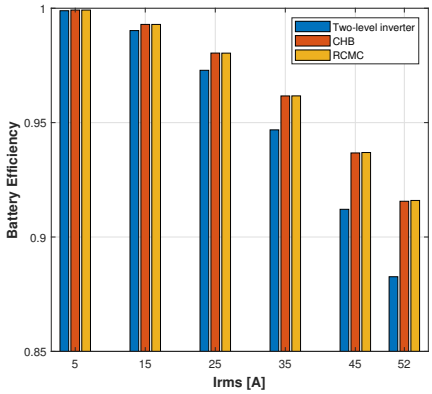


Figure 4.30: Comparison between battery system efficiencies.

The three curves decrease proportionally to the power. This behaviour is well-known for the two multilevel converters, for which more submodules are activated at higher power ratings . On the other hand, the two-level inverter is more performant for high power operative conditions, but its overall inverter efficiency trend is strongly affected by the significant battery losses, which determine the descendent trend.

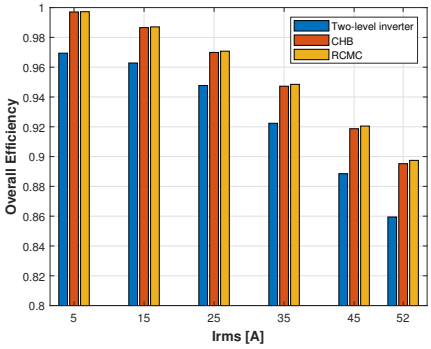


Figure 4.31: Comparison between overall system efficiencies.

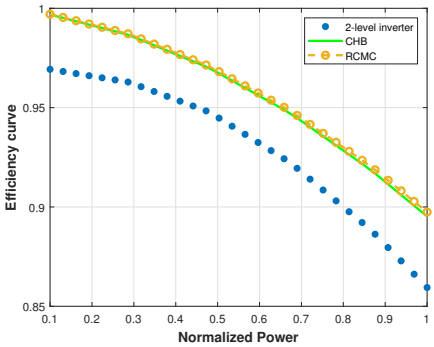


Figure 4.32: Overall efficiency on the normalized power.

CHAPTER

5 Experimental set-up

The most challenging part of the research work has been the implementation of a laboratory prototype. Being the RCMC a new topology, the development process concerned the design of the power converter, control architecture and data acquisition systems.

For the scope of this dissertation, a single submodule of the RCMC has been realized, inspired to the architecture E described in Chapter 2: it consists of 3 RBMs serially connected with a H-bridge. The installation of 9 battery cells allows to adequately validate the balancing feature of the RCMC and the 19 voltage levels, calculated with (3.1), are a sufficient number to implement the Nearest Level Modulation. Moreover, the decision of implementing one submodule allows to print other PCBs in the future in order to obtain a scalable and modular design, depending on the load requirements.

This chapter is structured in order to firstly give a detailed overview on the control architecture and then the explanation of the electrical design of the converter PCBs. Especially for the logic signals management, the control architecture significantly influences the electrical features required from the converter. For both topics, the concept design will be described, giving an overview on the technical issues encountered and how they have been solved.

5.1 Control Architecture

The first important consideration for the the control architecture design has been the management of the switches. Indeed, in terms of number of switches, the implementation of 3 RBMs and one H-Bridge requires:

$$N_{tot\_sw} = N_{RBM} \cdot N_{sw\_RBM} + N_{HB} = 3 \cdot 7 + 4 = 25 \tag{5.1}$$

where N_{RBM} is the number of RBM implemented, N_{sw_RBM} and N_{HB} are the number of switches required to implement one RBM and one H-bridge, respectively. Each device is driven by a gate signal, which needs to be transferred from the controller to the device itself. Assuming to use a conventional point-to-point link to each device - with electrical or optical cables -, the implementation of a dedicated conditioning circuit for each device would be problematic in terms of PCB layout. Moreover, assuming to extend the number of submodules to 12, the point-to-point communication may result unfeasible not only in terms of size but also in costs. As an example, the cost of an optical point-to-point link communication for 25 devices amounts to:

$$Cost = N_{tot\_sw} \cdot (cost_{RX} + cost_{TX}) = 25 \cdot (12€ + 12€) = 600€ \tag{5.2}$$

where $cost_{RX}$ and $cost_{TX}$ are the unitary cost of the receiving and transfer optical fibres. The cost is extremely high, considering that the estimation does not take into account cables and any other conditioning circuit components.

Therefore, the control architecture has been chosen to be based on a master-slave scheme. Each submodule is identified as slave and it is equipped with a dedicated controller, responsible of three tasks: (1) management of the gate signals for its devices, (2) measurements of the battery cells voltage installed and (3) communication with the master controller. In this way, assuming to have more submodules per phase, the battery voltage measurements are performed in decentralized way, without weighing down the master controller and having extra sensors.

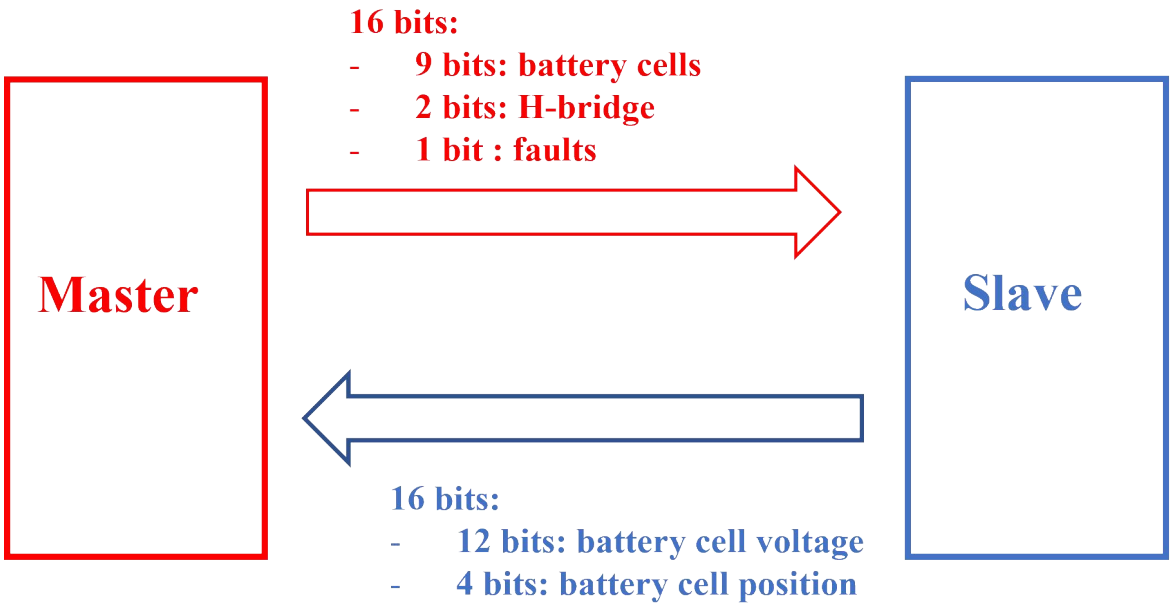


Figure 5.1: Master- slave communication scheme.

The master communicates with the slaves using a 1Mb asynchronous serial communication over optic fibre. Every sample time the master sends a 16 bits frame, containing the gate signal information for the RBMs and HB switches and fault flags. The slave decodes the message received transforming it in gate signals for each MOSFET, managing also the required dead-time. Finally, the slave measures the battery cells voltage and send the measurement data to the master with a 16 bits frame. Fig. 5.1 shows the communication scheme. In the following subsections, the master and slave features are explained in details.

5.1.1 Master controller

The master controller used for this prototype is the uCube platform [93], which integrates a dual-core ARM Cortex-A9 based Processing System (PS) and a Field Programmable Gate Array (FPGA) Programmable Logic (PL). With reference to Fig. 5.2, the functionalities required to the master controller and sequentially implemented on the dual-core ARM are listed below.

1. The current control is implemented with a classic PI controller, whose parameters are tuned

according to the procedure described in the previous chapter. The current control output is a reference voltage signal $V*$.

2. The sorting algorithm comprehends different steps. Firstly, the measurements data of the battery cell voltage are retrieved and arranged in an array, in which the voltage value of the $n-th$ battery cell is put in the $n-th$ position. Secondly, the computed array is given as input to a second function which sorts the battery cells voltage in descendent/ascendant way, for a discharging/charging process. Finally, the last algorithm checks that the prohibited configuration - first and third battery in the same RBM must not be inserted simultaneously - is not selected. Moreover, the average value of the battery cell voltage V_{mnbat} is computed.

3. The number of voltage levels is calculated knowing $V*$ and V_{mbat} as:

$$N_{lev} = \frac{V*}{V_{mbat}} \tag{5.3}$$

It is important to highlight that the reference signal is divided for the average value because, depending on process, the number of levels may change with the time. As an example, if the RCMC is used to power a motor, the same reference voltage value may require the insertion of an increasing number of battery cells, as they discharge over the time.

4. The gate signals are computed by merging the information of the sorting algorithm and the number of voltage levels. The implemented function returns a 16 bits frame structured as it follows: the first 9 bits corresponds to the 9 battery cells and specify which cell has to be connected, the next 2 bits indicate the HB configuration, another bit is used as flag to detect any fault situation.

5.1.2 Slave controller

The slave controller is responsible of decoding the gate information and performing the battery cell voltage measurements. Anytime the slave receives a 16 bits frame from the master, it

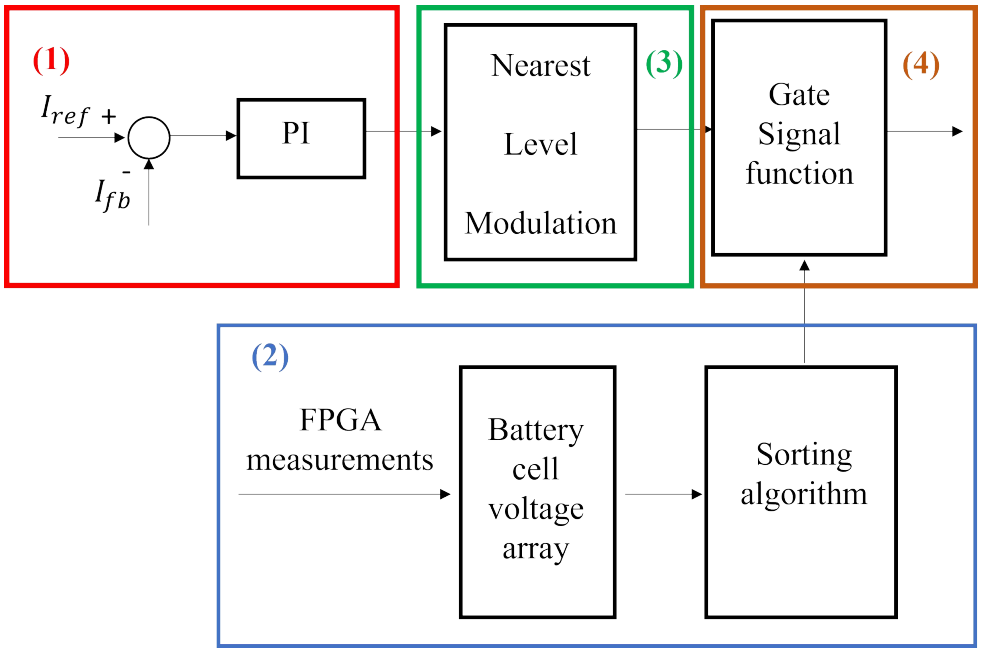


Figure 5.2: Control scheme implemented on the uCube.

performs the two functionalities and sends back a 16 bits package with the battery cell voltage information.

For the RCMC prototype, the Digilent Cmod A7-15T, a development board, designed around the Xilinx Artix-7, has been chosen as slave controller. In Fig. 5.3, the pinout of the board and the pins assignment are shown: 25 I/O pins are used as output to drive the MOSFET gate signals, 4 I/O pins are used for the measurements conditioning circuit - the functionalities will be explained later - and 1 of the 2 analog pins is used to perform the measurement of the battery cells voltage.

Gate signal elaboration

The slave controller receives a 16 bits frame from the master controller. The decoding process is structured as it follows:

- the first 9 bits are divided in three groups, each of which represents the three battery cells installed within one RBM. Each group is sent as input to a function which elaborates the correct gate signals for the RBM MOSFETs.

- the 10th and 11th bits are sent to a function dedicated to the elaboration of the H-Bridge MOSFETs gate signals.

- the 12th bit is a fault flag, active low. Therefore, if the master sends it equal to 0, all gate signals are put to 0 and no battery voltage measurement is performed.

Once, the gate signals are elaborated by the correspondent functions, they are sent as input the dead-time function. The dead time is applied to the turn on transient: therefore, all gate signals changing from 0 to 1 are delayed of 100 ns. In Fig. 5.4 an example of decodification process is shown.

Battery cells voltage measurement

The battery cell voltage measurements are performed with the internal ADC of the Artix - 7 FPGA. The ADC block can operate in two different timing modes, continuos or event driven modes [94]. In this case, the ADC acquisition and conversion is controlled by a flag, sent every time the master sends a bit frame. Each sample time, only one battery cell voltage is measured and the result is packed in 16 bits, in which the first 12 bits represent the voltage value and the remaining four bits indicates the battery cell position. This bit frame is then sent to the master control.

5.2 PCBs design

The RCMC prototype construction deals with two main aspects:

- the management of logic signals and local measurements, both responsible for the correct MOSFETs driving and control implementation.

- the DC/AC and AC/DC power conversions, for which a precise and adequate design is essential to avoid electrical faults;

The RCMC prototype realization follows the concept of the previous categorization: on one side, the low power features - gate signals elaboration and measurements - are built in the hereinafter called Logic PCB, while the high power features - DC/AC and AC/DC conversions - are implemented in the hereinafter called Power PCB. The two PCBs are vertically stacked and the electrical communication is realized via vertical headers.

5.2.1 Logic PCB

The Logic PCB is structured in order to accomplish the slave controller functionalities, implementing conditioning circuits for the gate signals and the measurement of the battery voltage.

Gate signal

The gate signals coming as output from the 25 pins of the slave controller must be driven to the Power PCB. Therefore, the Logic PCB has 5 vertical headers - one dedicated to the RBMs gate signals consisting in 21 pins, and four dedicated to each H-bridge device - directly connected to the Cmod A7-15T board. The division in five headers has been decided to reduce at minimum the length of the PCB tracks both in the Logic and the Power PCBs.

Voltage measurements of the battery cells

The utilization of the internal ADC of the Digilent Cmod A7-15T leads to the following considerations:

- the battery cells voltage are floating, while the signal given as input to the ADC has to be referred to the same ground of the Cmod A7;
- the two analog pins are not sufficient to perform the voltage measurements of nine battery cells simultaneously; therefore, a conditioning circuit is necessary to determine a timing strategy for the voltage measurements;

- the integrated ADC of the Artix-7 accepts as input voltage range 0 - 1V. A scale down circuit is already implemented on the Cmod A7 [95], allowing a maximum input voltage on the analog pins equal to 3.3 V. However, since the battery cells voltage range between 2.8 V and 4.2 V, another conditioning circuit is needed on the Logic PCB to scale down the voltage.

The conditioning circuit implemented on the Logical PCB takes into account the three technical constraints reported above. With reference to Fig. 5.6, it is possible to sequentially describe the implemented features:

1. An operational amplifier (op amp) in differential configuration is employed to measure the battery cells voltage. The op amps are powered by an isolated DC/DC converter which gives in output +15/-15 V and whose ground is shorted with the Cmod A7 ground: in this way, the measured signal and Cmod A7 grounds coincides, solving the first technical issue.

   Moreover, the choice of a bipolar supply voltage is not accidental. Indeed, from the op-amp perspective, the battery cells are serially connected and their voltage is floating. Therefore, the voltage distribution over the positive and negative pins of the op-amps has been simulated and validate experimentally to identify the correct supply strategy. With reference to Fig. 5.5, the positive pin of the first op-amp and the negative pin of the ninth op-amp face 10.8 V and -6 V respectively. The correct working conditions for any op-amp assume that their positive and negative pins cannot be connected to a voltage greater or less than their supply voltage, respectively. Therefore, if a unipolar supply voltage would have been adopted, the voltage measurement of the last battery cells could not have been performed. On the other hand, the +15/-15 V allows the correct measurement setup, accomplishing the op-amps working conditions.

   The output voltage of the op-amp in differential configuration is equal to:

$$V_{out} = \frac{R_2}{R_1}(V_+ - V_-) \tag{5.4}$$

Table 5.1: Current harmonic component

Pin 1	Pin 2	Pin 3	Pin 4	# battery cell
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9

For this prototype, it has been decided to have $R_2 = R_1$, in order to not loose any measurement information at the first stage.

2. Instead of using two analog inputs, which would still be not enough to perform all measurements simultaneously, it has been decided to use a multiplexer to have sequential battery voltage measurements. Four I/O pins of the Com A7 are programmed in order to send 9 combinations, each of which corresponds to the position of the battery cells installed. In Table 5.1, the correspondence between the four pins combinations and the battery cells is described.

3. The output of the multiplexer is connected to a low-pass active Sallen-Key filter, responsible for scaling down the voltage measurement and canceling eventual high frequency noise. With reference to Fig. 5.7, the filter gain is equal to

$$G = 1 + \frac{R_4}{R_5} \tag{5.5}$$

By using only R_4 and R_5, it is not possible to obtain a gain less than one: for this aim, the voltage divider made of R_1 and R_2 is added. The values of the two resistors are chosen according to the cut-off frequency f_c and the scale ratio S_r required; the two constraints can be written as:

$$f_c = \frac{1}{2\pi\sqrt{[(\frac{R_1R_2}{R_1+R_2})R_3C_1C_2]}} \tag{5.6}$$

$$S_r = \frac{R_2}{R_1+R_2} \tag{5.7}$$

Assuming a $f = 20kHz$, $S_r = 0.2364$, $R_3 = 10k\Omega$, $C_1 = C_2 = 1nF$, R_1 and R_2 are equal to $42.2k\Omega$ and $13k\Omega$, respectively. With these values, the maximum voltage measurement equal to $4.2V$ is scaled to $1V$. Assuming $R_4 = R_5 = 10k\Omega$, the maximum output voltage will be equal to $2V$.

4. The filtered and scaled signal reaches the analog input (AI) of the Cmod A7, in order to be measured from the integrated ADC. Finally the measured data are sent to the master.

In conclusion, the picture of the realized Logic PCB is shown in Fig. 5.8: in (1) there are the op-amp in differential configuration, in (2) the DC/DC with $\mp$ 15 V as output voltage, in (3) the multiplexer, in (4) the Sallen-Key filter and in (5) the Cmod A7.

5.2.2 Power PCB

The first feasibility check in the Power PCB realization is the design of the Reconfigurable Battery Module. As already mentioned in the previous chapters, RBMs are intentionally implemented with low voltage MOSFETs, to ensure low conduction losses and guarantee fast switching dynamics. Their driving circuits have to be designed accurately, evaluating the power ground of each switch.

As it can be seen in Fig. 5.9, the source pins - which usually identify the device power ground - are either connected to a positive/negative terminal of a battery cell or to another switch pin. Therefore, each MOSFET must have an isolated ground, to avoid the shorting out of any device or battery cell. This design is obtained by employing one DC/DC converter to power the driving circuit of each MOSFET. The adoption of dedicated DC/DC converter for each device leads to consequent constraints on gate driver choice:

- Since MOSFET and gate driver share the same power ground, each device has a dedicated gate driver. For this reason, a single channel gate driver is selected.
- Since the gate signals coming from the Cmod A7 will have a common ground, different from each MOSFET power ground, the utilization of either an isolated or differential gate driver is required. The second solution has been adopted: the input signal is referred to the Cmod A7 ground, while the output gate signal is referred to the power ground of the related MOSFET.

Finally, in Fig. 5.10 the driving circuit of the MOSFETs is shown. All DC/DC are powered with the 5 V, referred to the common ground of the Cmod A7. The DC/DC output is an unipolar voltage 15V, used to power the gate driver, and an isolated power ground (PGND) to refer the power gate signal and the source pin of the MOSFETs. As it can be seen from Fig 5.9, even if the source pins S2& S3, S4& S5 and S6& S7 shares the same potential with the consequent possibility of using a unique DC/DC for the couple of switches 2& 3, 4& 5 and 6& 7, each switch has still one dedicated driving circuit.

The same driving architecture is used to drive the H-Bridge devices. Although different strategies could have been used - i.e. a single gate driver with the Boot strap strategy- two considerations led to adopt the same driving circuit shown in Fig. 5.10:

- compared to other driving strategies, having four driving circuits removes any limitation related to the switching frequency. Indeed, using two boost strap capacitors to drive the high side MOSFETs requires a minimum switching frequency of the order of magnitude of kHz. The H-Bridge placed in the RCMC switches at the load fundamental frequency, which can be really low compared to the one required by the boost strap strategy.
- Having the same pattern of driving circuit is easier in terms of layout placing.

Finally, the picture of the Power PCB is shown in Fig. 5.11: in (1) the MOSFETs pattern of the RBMs, in (2) the nine connector needed to connect the battery cells, in (3) there is the H-Bridge, in (4) the output connector are shown.

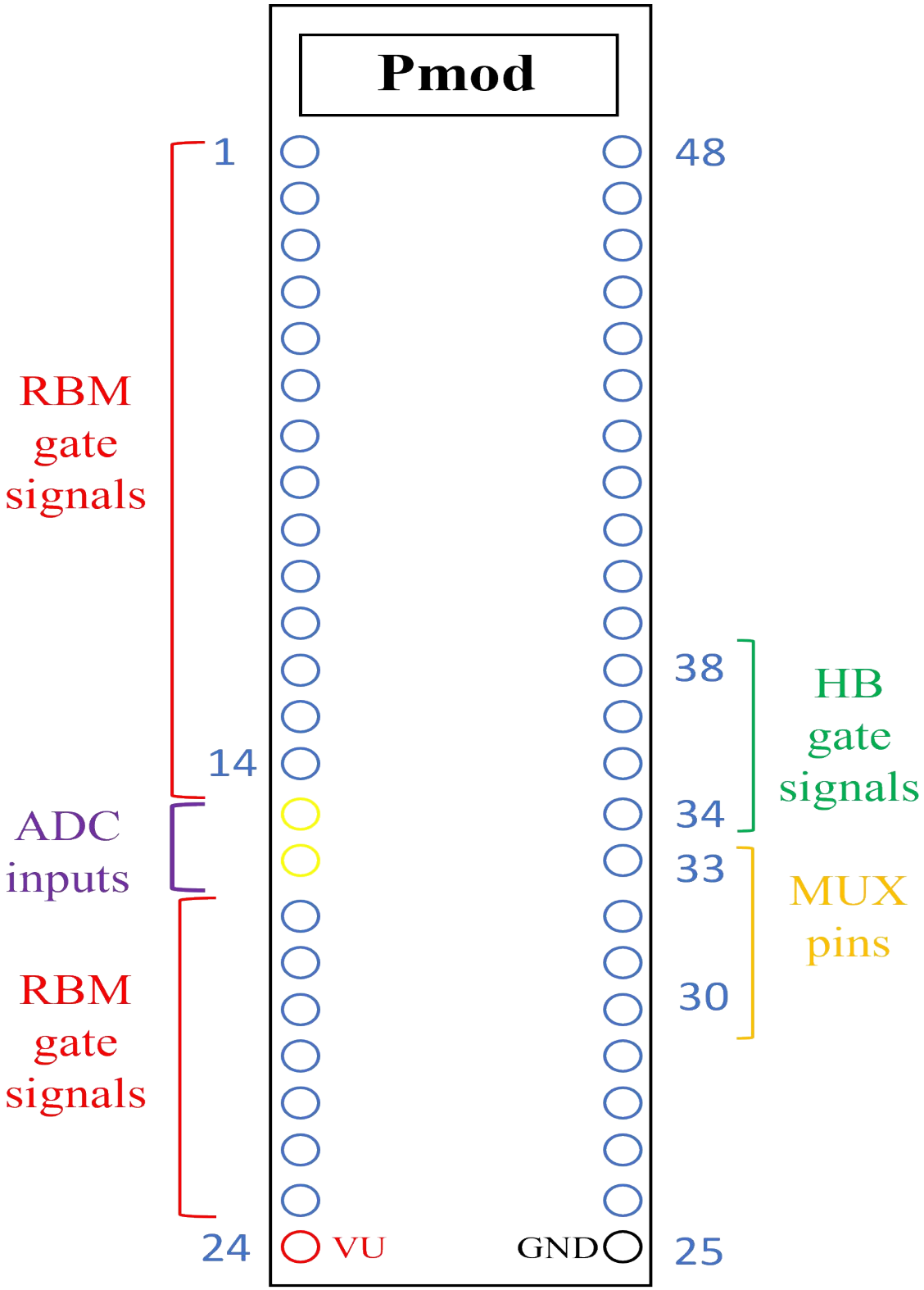


Figure 5.3: Digilent Com A7.
105

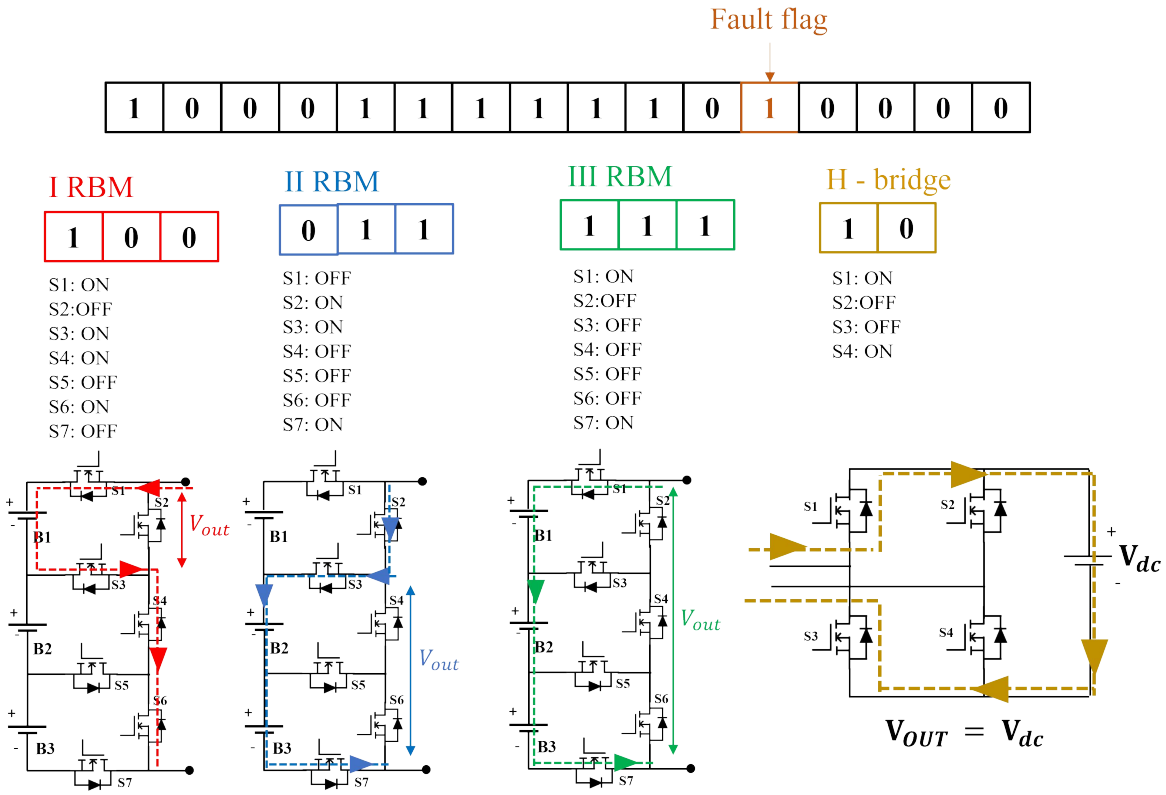


Figure 5.4: An example of decoding process computed by the slave controller.

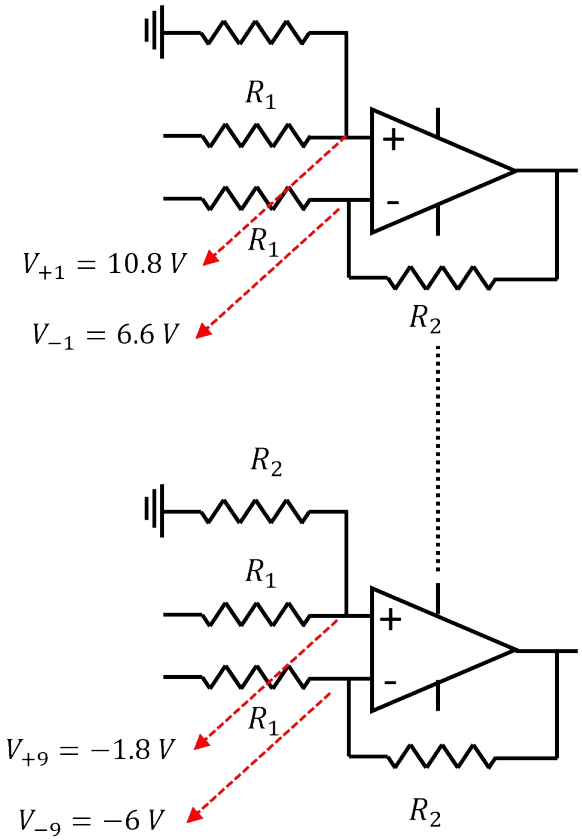


Figure 5.5: Voltage distribution over the op-amp pins.

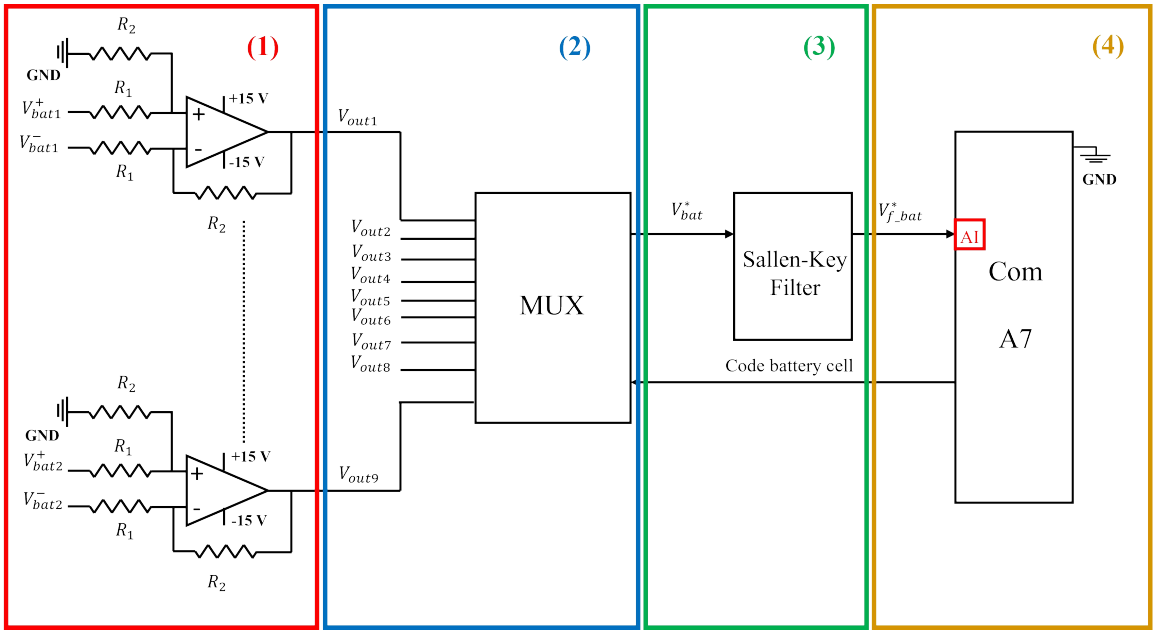


Figure 5.6: Conditioning circuit implemented on the Logic PCB.

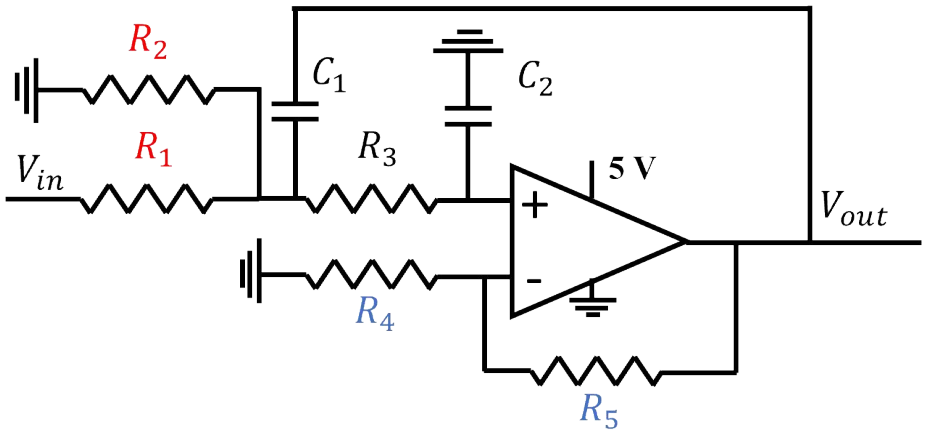


Figure 5.7: Sallen Key filter.

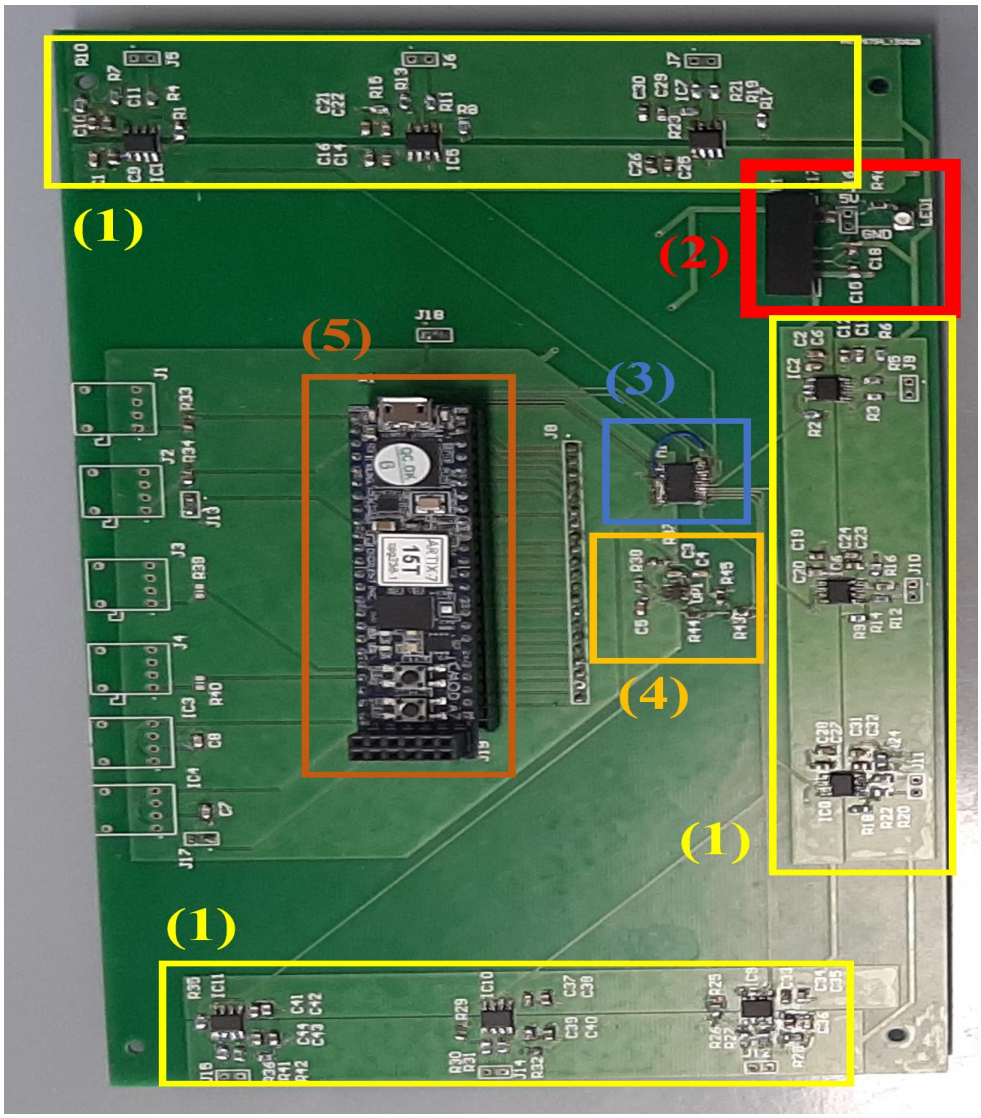


Figure 5.8: Logic PCB

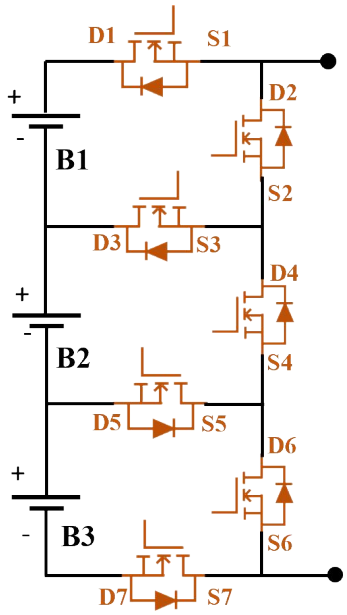


Figure 5.9: RBM architecture with the MOSFETs pins highlighted.

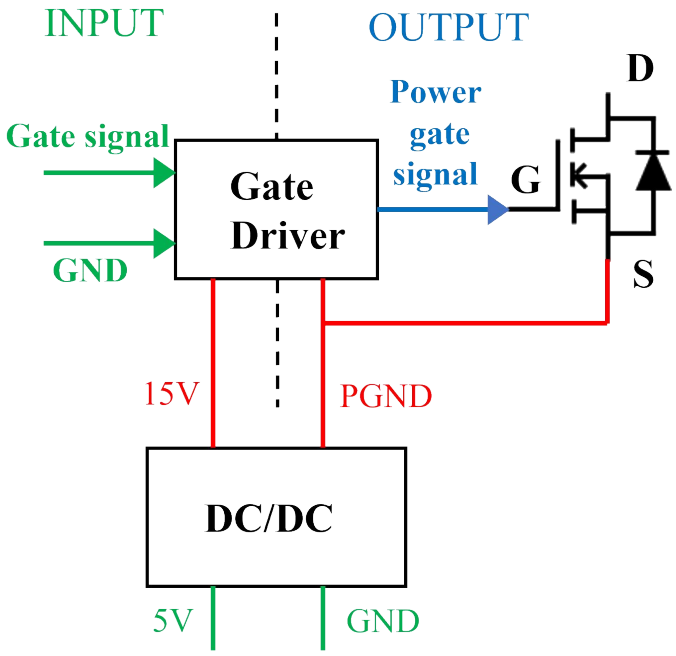


Figure 5.10: Driving circuit implemented for all MOSFETs.

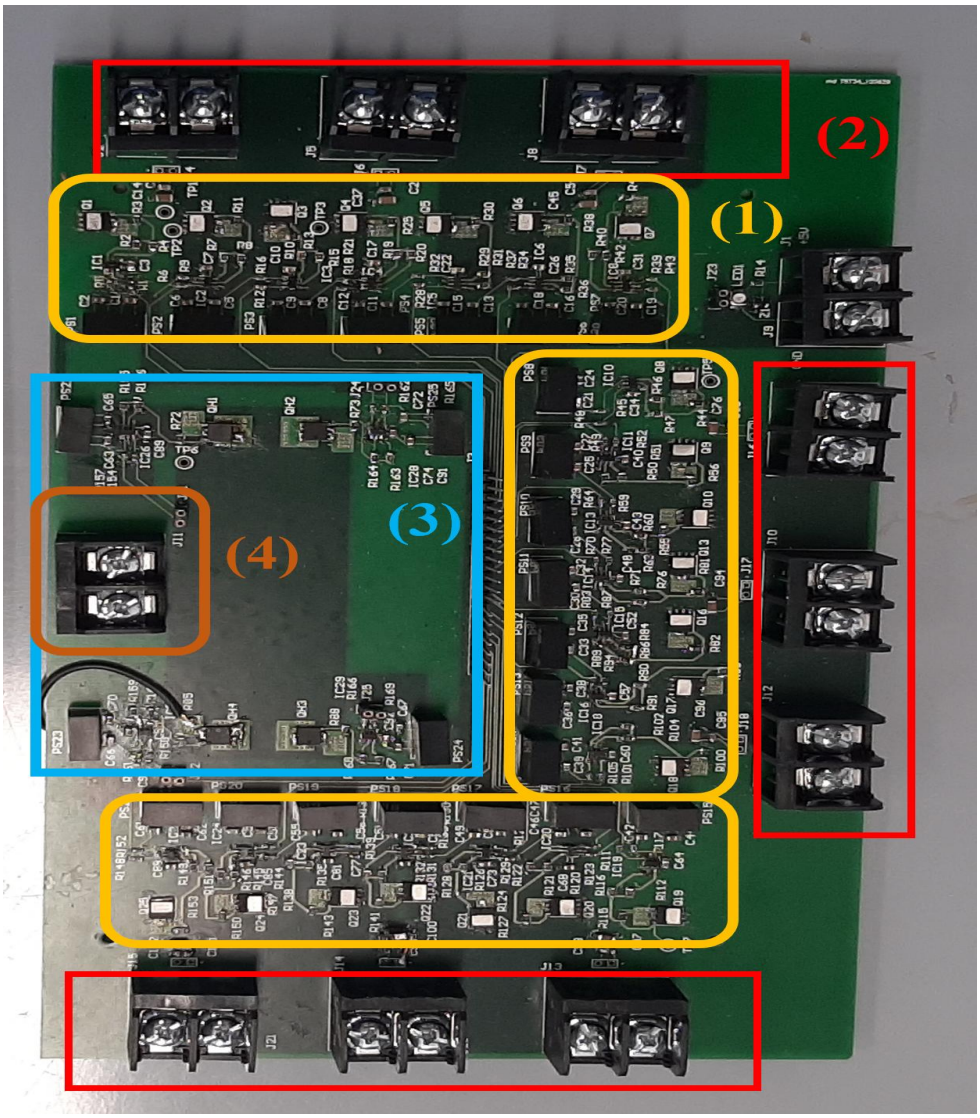


Figure 5.11: Power PCB.

CHAPTER

6 Experimental results

This chapter shows the experimental validation of the RCMC prototype. The first experimental activities were carried out to verify that both the control architecture and the PCBs were working as expected. Before assembling the whole converter, the tests listed below were carried out to verify that the control architecture, the logic PCB and the Power PCB work separately as expected.

- Control architecture
  - Sending and reception of the 16 bits frames, from both master and slave sides. Specifically, it has been checked that the asynchronous communication was feasible for 16 bits and there was no mismatch in terms of transferred data.
  - Gate signal decoding process from slave side. It has been checked that there was the correct correspondence between the 16 bits frame received and the gate signals delivered by the slave controller.
  - Battery cell voltage reading, master side. The slave controller sends digital raw data to the master, responsible of doing the conversion from binary number to a voltage value.
- Logic PCB

  - Measurements of the battery cells voltage. Specifically, it is checked that the nine op-amps can perform the voltage measurement simultaneously.
  - Sending and reception of the digital signals to/from the Multiplexer. The slave controller has been programmed in order to read sequentially the voltage measurements.
  - Filtering and scaling down actions done by the Sallen-Key filter. The input and output signals of the Sallen-Key filter have been compared to check the filtering action and the scaling ratio.
  - Parallelization of the gate signals. It has been checked that, after the gate signal decoding process, each of the 25 I/O pins had the correspondent gate signal.

- Power PCB

  - Gate signals. Specifically, different tests have been carried out to determine the optimum value of the gate resistor, in order to avoid voltage spykes, ringing and have smooth and fast turn on/off dynamics for the H-bridge and RBMs MOSFETs.
  - RBMs output voltages. Specifically, it has been checked that, given the correct gate signals, the RBM was able to insert one, two or three cells with all possible combinations.
  - H-Bridge output voltages. The four switches have been driven to obtain a positive, negative or null output voltage.

Once the previous tests gave the correct results, the RCMC prototype has been tested firstly with a RL load, to reproduce a motor drive setup, and then connected to an AC programmable power supply, in order to perform a charging process.

6.1 Preliminary details for the experimental activities

The battery cell used is the MOLICEL INR-18650-P26A; the RCMC prototype with the battery cells connected is shown in Fig. 6.1. Beside the battery cells voltage measurements computed

Table 6.1: Circuit setup

Parameter	Value	Unit
Battery cell nominal voltage	3.6	V
Battery cell nominal capacity	2.6	Ah
Resistor	1 - 11	Ω
Inductor	1	mH
Nominal Voltage RCMC	32.4	V
Nominal Current RCMC	10	A
Sample Time	200	μ s

by the slave controller, a list of the instrumentation used to measure and acquire the remaining parameter is reported below.

- The RCMC current is measured with a current Transducer LA 55-P/SP1. The measured data is then sent to the uCube controller, which is equipped with dedicated ADC.
- the data acquisition systems used for the experimental activities are mainly a Tektronix oscilloscope and the specific Matlab Graphical User Interface (GUI) developed for the uCube controller.

6.2 RCMC powering a RL load

The circuit setup is shown in Fig. 6.2 and its parameters are listed in Table 6.1. To test different current values, the load is characterized by a fixed inductance and a variable resistor.

The main functionalities to be tested were the voltage and current waveforms and the effectiveness of the current control - with a focus on the correct tuning of the PI gains. Indeed, the shape of the voltage and current waveforms is strictly connected to the control bandwidth allowed: if the natural frequency of the PI controller is set too high, the reference voltage signal may vary too fast and the Nearest Level Modulation may create oscillations during the transition from one voltage level to another. In Fig. 6.3, two case studies are shown: two different working points are taken to prove that the wrong PI tuning may generate oscillations when a new voltage

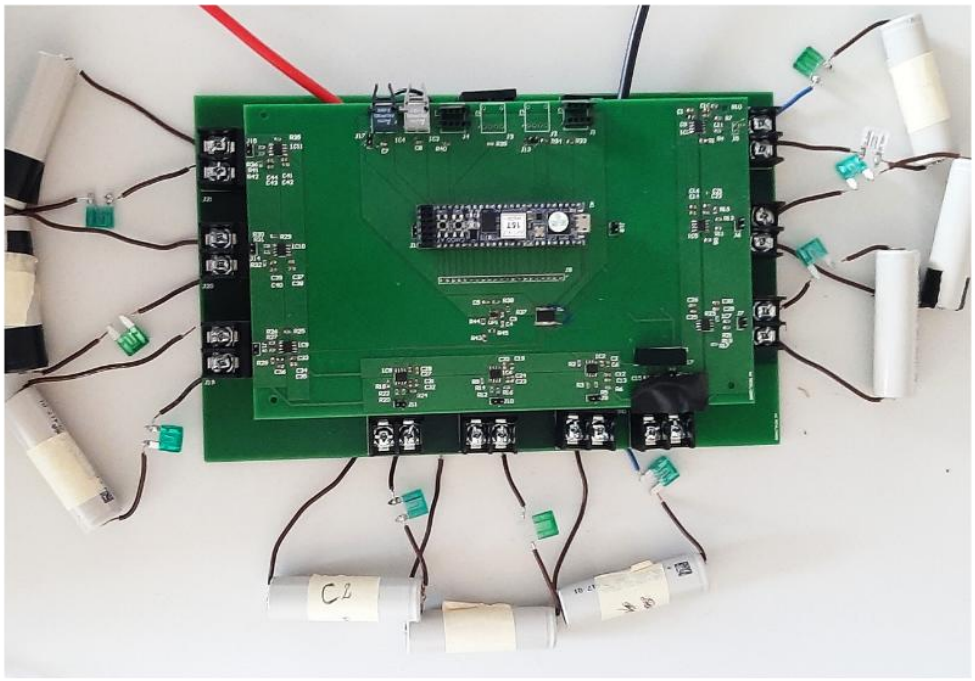


Figure 6.1: RCMC experimental setup.

level is computed, regardless of the entity of the power conditions. On the other hand, in Fig. 6.4 are reported the same working points but with a correct PI tuning: in both situations the transition between different voltage levels is computed in smooth way, with a consequent improvement of the current waveform.

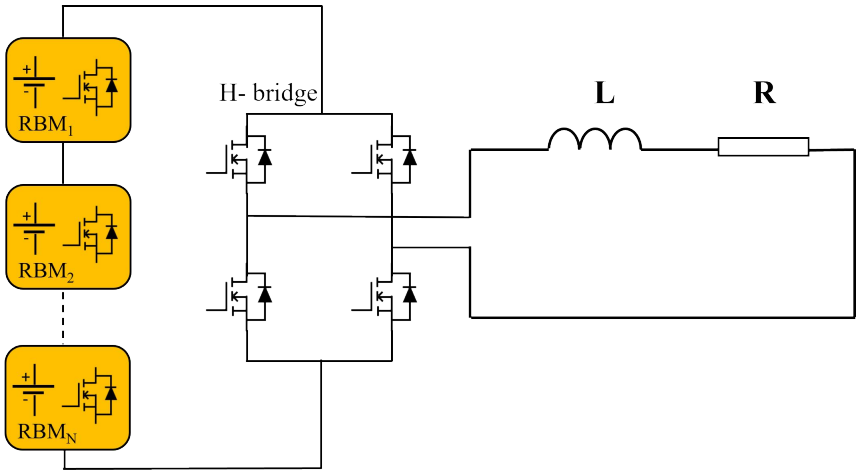
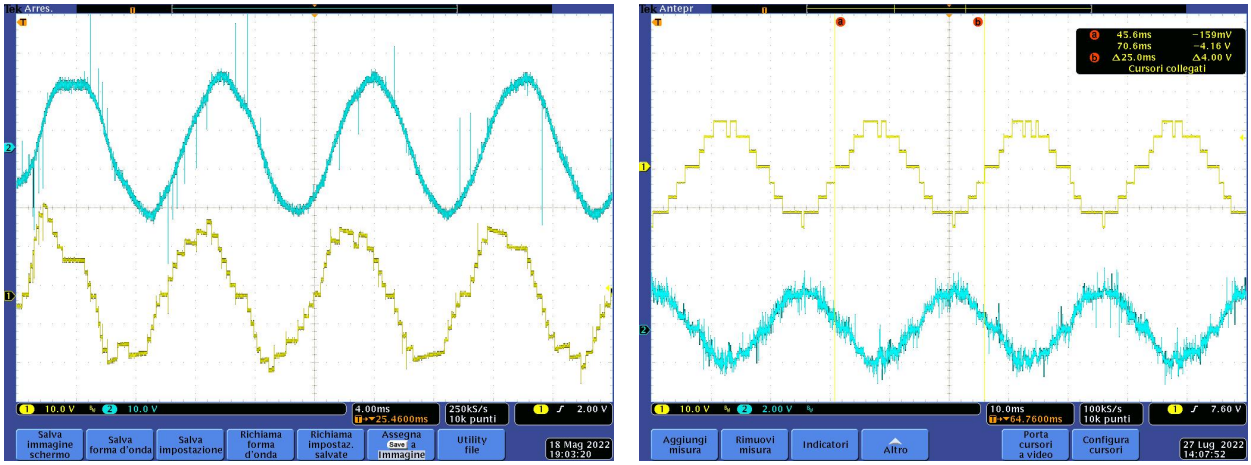


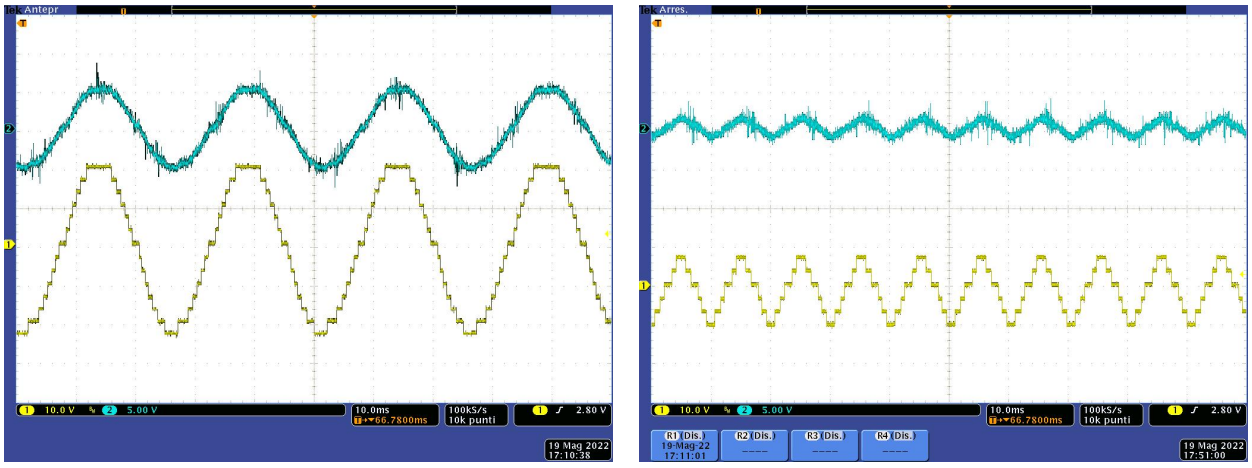
Figure 6.2: RCMC used to power a RL load.



(a) (b)

Figure 6.3: The RCMC output voltage is shown in blu, while the current is shown in yellow: (a) and (b) represent the waveforms for high and low power conditions, respectively. The wrong tuning of the PI controller gains create oscillations in the computation of the voltage levels.

Finally, the sorting algorithm is tested. The battery cells voltage is initially set in an unbalanced situation, to validate the algorithm. In Fig. 6.5, the trend of the battery cells voltage is shown: the sorting algorithm works in order to insert the battery cells when their voltage reaches the average value. In this way, not only the voltages converge to a unique value but the dynamics remains balanced during the whole working conditions.



(a) (b)

Figure 6.4: The RCMC output voltage is shown in blu, while the current is shown in yellow: (a) and (b) represent the waveforms for high and low power conditions, respectively. The correct tuning of the PI controller gains allows a smooth computation of the voltage levels.

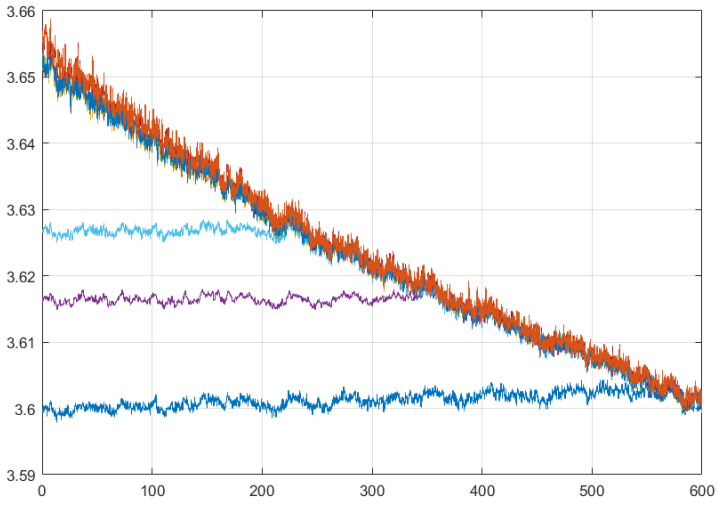


Figure 6.5: Battery cells voltage during a discharging process.

6.3 RCMC connected to an AC programmable source

The RCMC prototype is connected to an AC programmable source to validate the topology in all three operative conditions described in chapter IV, performing both the discharging and charging

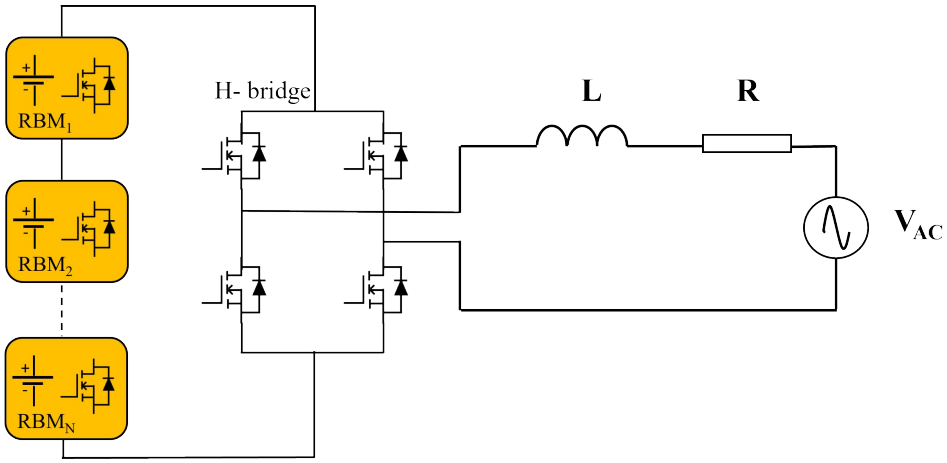


Figure 6.6: RCMC connected to an AC programmable power supply.

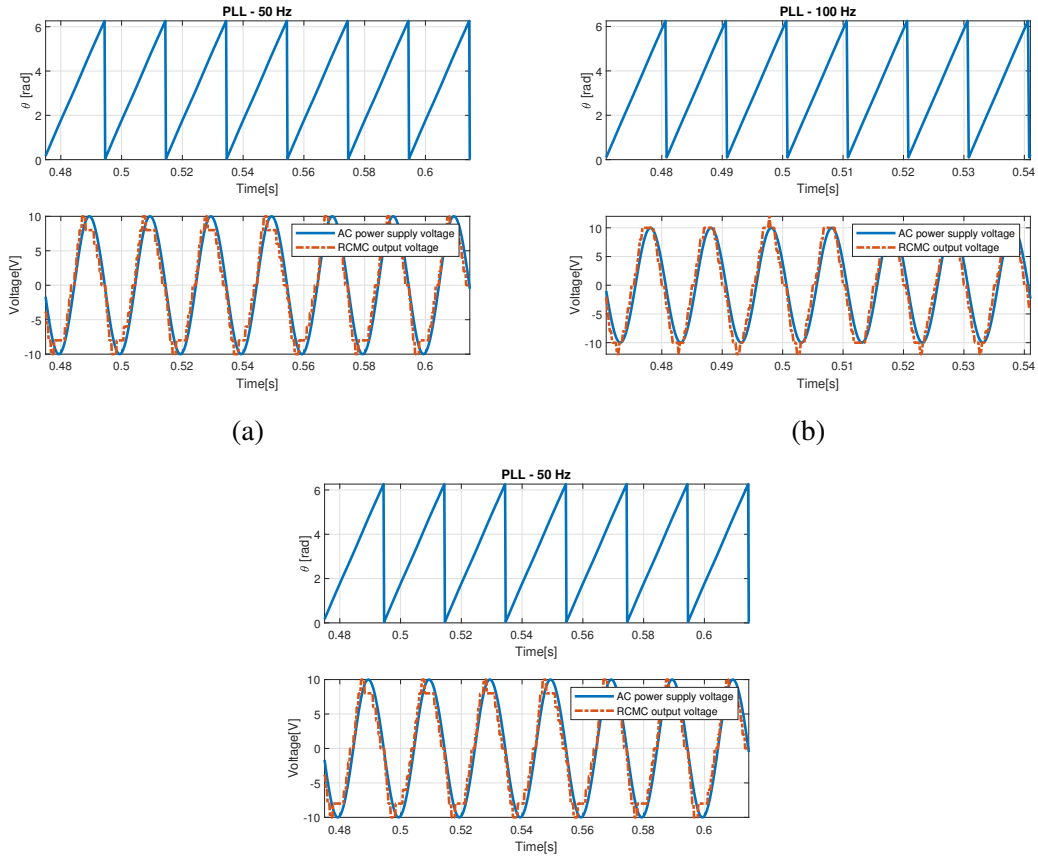
processes. The circuit setup is shown in Fig. 6.6.

6.3.1 PLL and Power tests

To perform any test with an AC power supply, it is necessary to lock the converter output voltage to the source voltage. First of all, the output voltage of the AC power supply has been measured by an op-amp in differential setup and then sent single phase PLL, implemented in the master controller. The PLL scheme has been implemented according to [96]. The PLL validation has been carried out by setting the output frequency of the AC power supply at different values. In Fig. 6.7, there are the results at 50 Hz, 100 Hz and 200 Hz.

The RCMC prototype has been tested for different phase displacement, compared to the AC power supply output voltage. In Fig. 6.8, both active and reactive power exchanges are implemented by displacing the AC power supply and the RCMC voltages of 0 and 90 degrees, respectively.

Finally, the transient dynamic has been tested. Specifically, two scenarios have been considered: the reference current increases its peak each following period and a sudden change during the working conditions. As shown in Fig. 6.9, the RCMC follows the control reference signals without any particular risky condition to be reported.



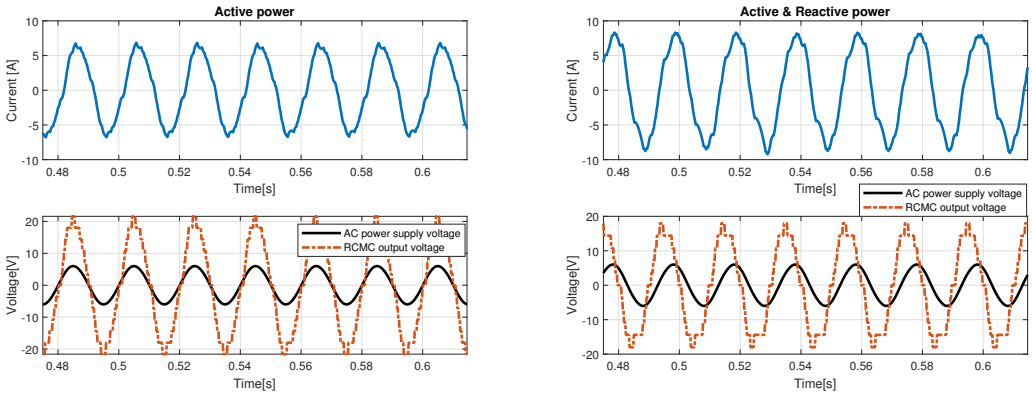
(a) (b)

(c)

Figure 6.7: The angle, the AC system and RCMC output voltages are shown for three frequency values: 50 Hz, 100 Hz, 200 Hz.

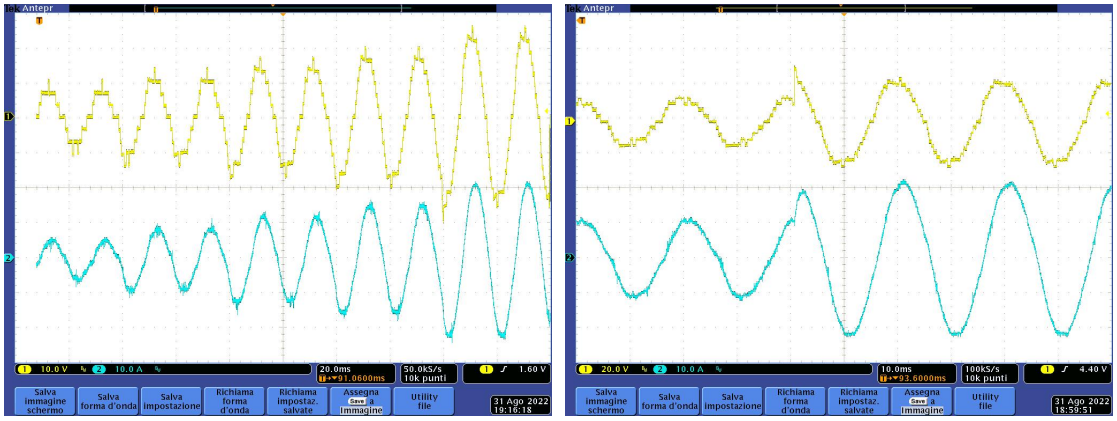
6.3.2 Sorting algorithm in discharging and charging processes

The RCMC prototype is tested in both discharging and charging phases, in which the AC power supply is used to generate a variable voltage waveform representing the load in motoring and regenerative conditions, respectively. Fig. 6.10 shows the AC voltage from the power supply and the output voltage and current of the RCMC, for different power factors. In Fig. 6.10 (a), the RCMC is feeding the load with the battery cells in discharging phase; in Fig. 6.10 (b), the load is in regenerative mode and the battery cells are in charging phase. The AC power supply generates a 4 V and 20 V peak voltage sinusoidal waveforms, for the discharging and charging processes,



(a) (b)

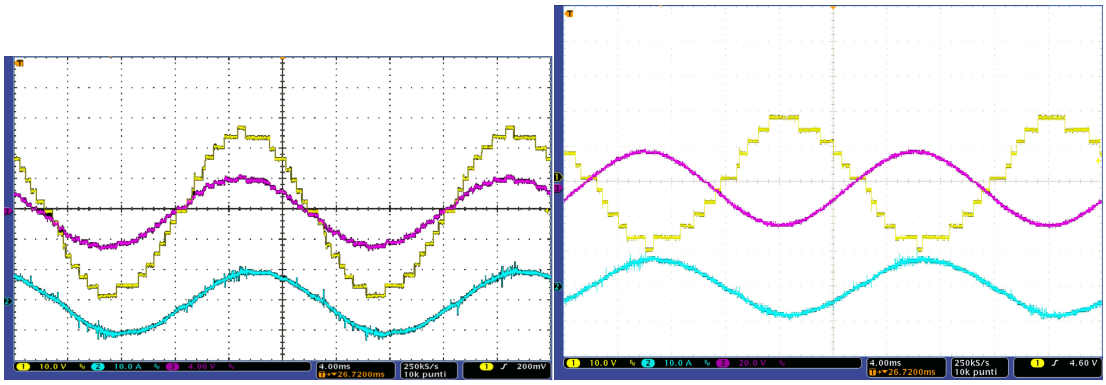
Figure 6.8: RCMC test for exchanging (a) active power and (b) reactive power.



(a) (b)

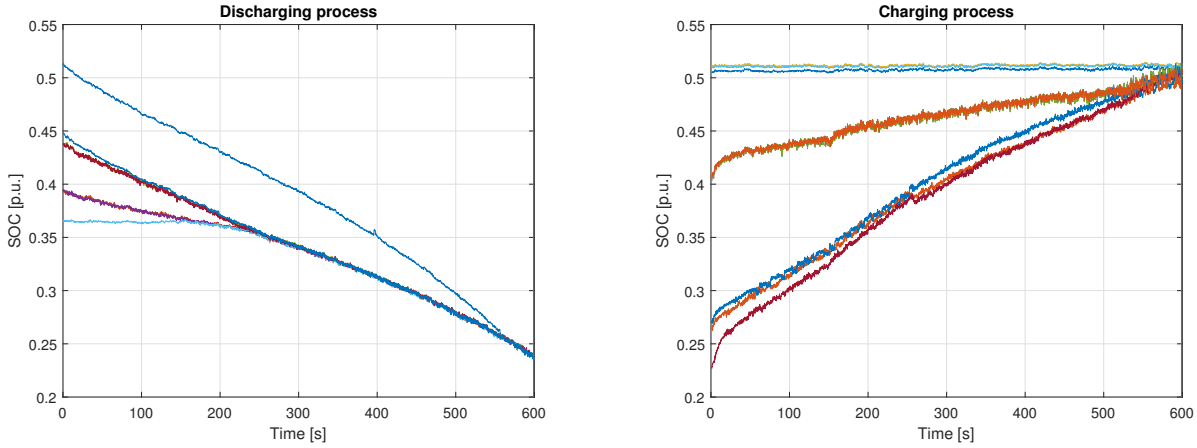
Figure 6.9: (a) Variable reference current every two periods and (b) a sudden change of the current reference.

respectively. Despite of the low frequency employed by the master, equal to 5 kHz, the high number of voltage levels provided by the RCMC ensures a pure sinusoidal current. In the same case scenarios, the battery cells voltage has been measured and then reported in SOC values in Fig. 6.11. During the discharging (charging) processes, the most (less) charged cells are selected until they reach the less (most) charged ones. The implemented sorting algorithm guarantees a final balanced situation, even starting with very different SOC values, as shown in Fig. 6.11.



(a) (b)

Figure 6.10: RCMC output voltage (yellow), current (blue) and the load (purple), in (a) discharging and (b) charging processes.

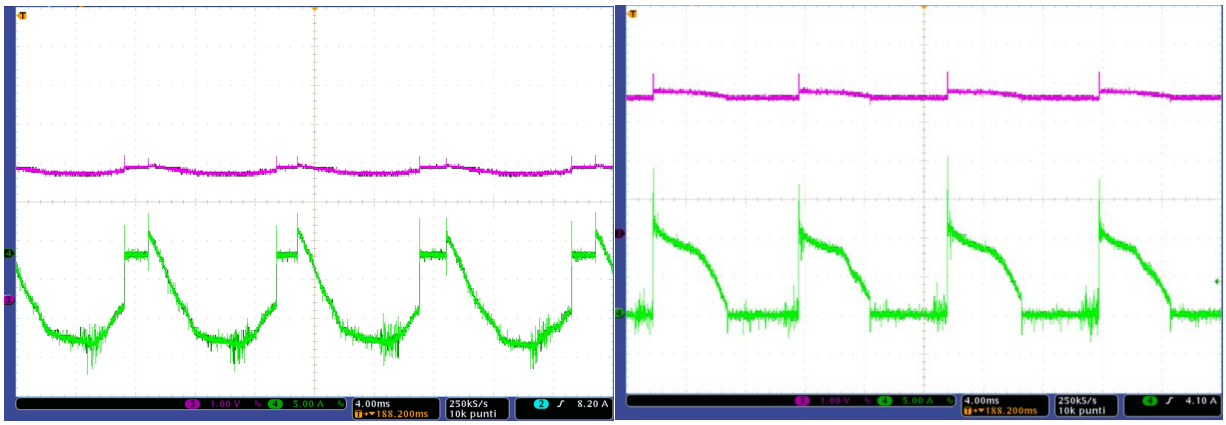


(a) (b)

Figure 6.11: SOC of the nine battery cells during the (a) discharging and (b) charging processes.

6.3.3 Battery cell measurements

Moreover, the voltage and the current of one battery cell have been measured and reported in Fig. 6.12, for both processes. When the battery cell is inserted, its voltage changes according to the current direction: in Fig. 6.12 (a) the battery is supplying current to the load and its voltage slightly decreases, while in Fig. 6.12 (b) the battery is charged and its voltage slightly increases. In Fig. 6.13, the flowing current is shown together with the RCMC output voltage: it is possible



(a) (b)

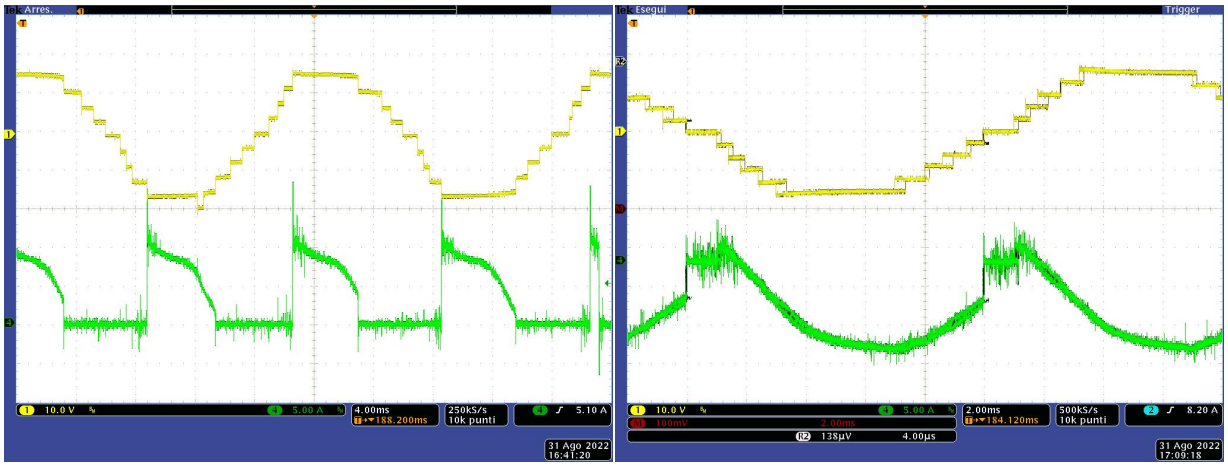
Figure 6.12: Current (green) and voltage (purple) of one battery cell, in (c) discharging and (d) charging processes.

to notice the exact insertion time of the battery cell and the step contribution that it gives to the RCMC output voltage.

During both charging and discharging processes, the flowing current follows a sinusoidal shape without being pulsant: the high number of levels permits to discretize the requested voltage with high accuracy, avoiding the continuos insertion/disconnection typical of the PWM. Therefore, battery cells work in safer conditions and there is less risk of capacity reduction [97].

6.4 Algorithm at light loads

When the converter works at light loads, the NLM resembles a PWM because the requested output voltage is so low that the control computes an oscillating number of battery cells for each level. Therefore, each DSP cycle, the same pattern of devices is asked to switch, until the sorting algorithms updates the batteries to be inserted. Therefore, an algorithm has been developed in order to distribute the switching pattern over the different levels, decreasing the equivalent switching frequency for all the devices. The algorithm can be properly tuned in order to fix the final switching frequency. The experimental tests have been carried out considering the worst



(a) (b)

Figure 6.13: Battery cell current (green) and RCMC output voltage (yellow).

case scenario: the reference voltage is less than one battery cell voltage, therefore the insertion required oscillates between 1 and 0. In this case, the nine cells are inserted in progressive way according to the sorting algorithm. Fig. 6.14 shows the number of battery cells computed by the DSP and the evolution of the array with the insertion order. Since the number oscillates between 0 and 1 and the aim is to distribute the switching pattern within the 3 RBMs, the array of the insertion order updates each time a cell has to be turned on. Fig. 6.15 shows the voltages of the nine battery cells: the measurement is performed without any low pass filter action in order to make more visible the voltage drop due to the internal resistance, which corresponds to the cell insertion. The sequence of the voltage drops completely matches the insertion array shown in Fig.6.14.

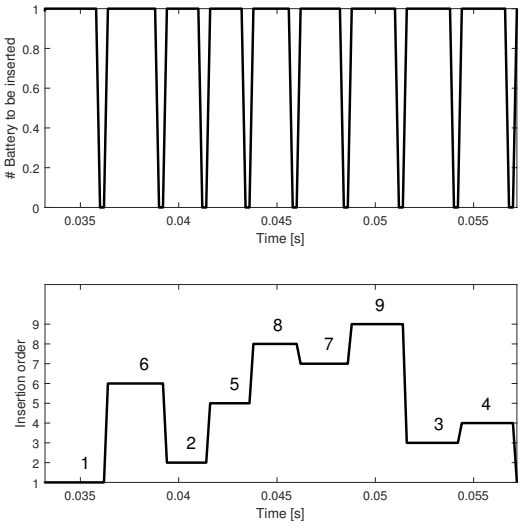


Figure 6.14: Battery cell requested and insertion order evolution.

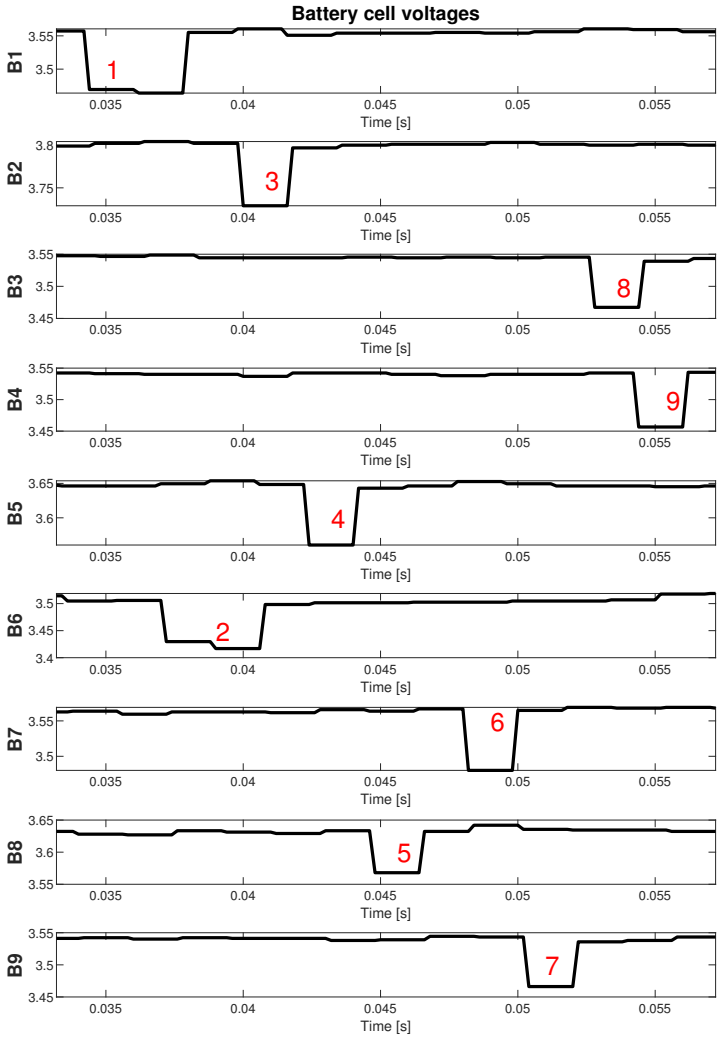


Figure 6.15: Battery cells voltage without low pass filter action: the voltage drop means the insertion of the battery cell. The number in red indicates the insertion position.

CHAPTER

7 Conclusions

The conventional two-level inverter has demonstrated its limits when employed in EV powertrain application: the efficiency drops for partial loads ranges, the energy delivery from the battery pack is not optimized and the battery cells must be managed by a Battery System Management to avoid over charge or over discharge phenomena. As widely discussed in Chapter II, even if several research works studied enhancement actions to reduce its drawbacks, the next step is changing the powertrain concept. Although the transition from a two-level inverter to a multilevel and reconfigurable structure increases the overall system complexity, the optimization of the battery system and the consequent energy conversion in EV powertrains is an important step to boost the employment of electric vehicles.

7.1 Reconfigurable Cascaded Multilevel Converter

In this work, a new topology called Reconfigurable Cascaded Multilevel Converter has been presented. The RCMC is a three-phase converter, characterized by the serial connection of several submodules. In each submodule, the energy conversion is performed by the connection of several Reconfigurable Battery Modules (RBMs) with a H-Bridge, used only to invert the voltage polarity. The real novelty lies on the Reconfigurable Battery Modules, which consist in groups of three battery cells individually accessible through a coherent selection of the switches placed between

their connections.

This work carried out an efficiency analysis comparing six different RCMC architectures to establish the most suitable one, according to given voltage and current requirements. The conduction losses - the switching losses are negligible - are used as key parameter to evaluate the most efficient topology. Furthermore, the RCMC topology is completely customizable in terms of number of RBMs per submodules and submodules per phase, so that any other key parameter can be used to establish the most suitable architecture in any application.

Moreover, its feasibility and competitiveness have been studied by comparing the new topology with a HCMC, CHB and a SiC two-level inverter, in terms of converter and battery efficiency. The simulation results show that the RCMC is completely suitable for powertrain application, being more efficient or comparable with the other topologies. Moreover, as confirmed by the experimental activities, the direct access to each cell allows to develop several algorithms to keep the state of charge of the battery cells balanced.

From charging point of view, the three-phase structure permits the direct connection to an AC system, without the need of extra components. Low THD current values are obtained also with small values of filter inductance and the charging time estimation gives satisfying results, showing a reduction of 40% compared to a conventional battery pack.

Finally, this dissertation explains in details all the challenges faced during the converter construction. The important features of the new topology correspond to a high complexity levels in terms of control architecture and PCB designs. Moreover, the high number of switches and parameters to be measured increase the converter cost and size. To overcome these issues, the control architecture has been designed according to a master-slave scheme, in which each submodule is equipped with its own controller. In this way, the gate signals conditioning and the battery cell voltage measurements can be executed by using a single device and without increase the computational burden of the master controller, already responsible of performing the current control and sorting algorithms.

The PCB are designed in order to accomplish the control architecture: the so-called Logic

PCB is responsible for the gate signal elaboration and implements the conditioning circuits for the battery cell voltage measurements; the so-called Power PCB perform the DC/AC and AC/DC energy conversions, hosting the driving circuits for each MOSFET.

The laboratory prototype is validated by showing the results of the experimental activities: in Chapter VI, both charging and discharging processes are performed and the battery cell voltages are measured to show the efficiency of the developed sorting algorithm. The output voltage and current of the converter are reported to validate the Nearest Level Modulation, both in nominal and low power conditions. Moreover, current and voltages of the converter are shown in steady-state and during transients to prove the low THD current values and the fast response to reference changes, respectively.

7.1.1 Future works

The work shown in this dissertation is only the first step in the exploitation of the RCMC features. The works planned in the future can be summarized in:

- Development of a three-phase topology to power a three-phase motor and carry out the experimental activities related to the charging configuration;
- Efficiency validation of the simulation analysis presented in Chapter III and IV;
- Implementation of customized managing battery cell algorithms, according to priority parameter. In this dissertation, two algorithms of SOC balancing are presented, according to which the battery cells are inserted. In the future, the goal is the integration of the balancing algorithms with thermal management control routines in order to have a complete overview of the battery system status. As an example, the insertion of the battery cells may be evaluated either according to the thermal distribution or their SOC values or considering both aspects. The priority can be timely decided, according to the operating conditions;
- Development of fault tolerant strategies;

- Development of recursive algorithm to reduce the number of conditioning circuits needed to perform the measurements;
- Development of a PWM modulation for low-power applications.

Bibliography

[1] G. S. Malhi, M. Kaur, and P. Kaushik, "Impact of climate change on agriculture and its mitigation strategies: A review," *Sustainability*, vol. 13, no. 3, 2021.

[2] K. Protocol, "Kyoto protocol," *UNFCCC Website. Available online: http://unfccc. int/kyoto_protocol/items/2830. php (accessed on 1 January 2011)*, 1997.

[3] "Paris agreement," in *Report of the Conference of the Parties to the United Nations Framework Convention on Climate Change (21st Session, 2015: Paris). Retrived December*, HeinOnline, vol. 4, 2015, p. 2017.

[4] I. E. Agency, "Tracking clean energy progress 2017," *Energy Technology Perspectives 2017*, 2017.

[5] G. J. Hayes and A. G. Goodarzi, *Electric Powertrain*. John Wiley & Sons Ltd, 2018.

[6] IEA, "Global electric passenger car stock," *https://www.iea.org/data-and-statistics/charts/global-electric-passenger-car-stock-2010-2020*, 2021.

[7] K. T. Chau, C. C. Chan, and C. Liu, "Overview of permanent-magnet brushless drives for electric and hybrid electric vehicles," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 6, pp. 2246–2257, 2008.

[8] S. S. Williamson, A. Emadi, and K. Rajashekara, "Comprehensive efficiency modeling of electric traction motor drives for hybrid electric vehicle propulsion applications," *IEEE Transactions on Vehicular Technology*, vol. 56, no. 4, pp. 1561–1572, 2007.

[9] E. Knischourek, K. Muehlbauer, and D. Gerling, "Power losses reduction in an electric traction drive at partial load operation," in *2012 IEEE International Electric Vehicle Conference*, 2012, pp. 1–5.

[10] E. Knischourek and D. Gerling, "Analysis of electric vehicle driving cycles for inverter efficiency improvement at partial load," in *2015 IEEE 11th International Conference on Power Electronics and Drive Systems*, 2015, pp. 503–508.

[11] E. A. Grunditz and T. Thiringer, "Characterizing bev powertrain energy consumption, efficiency, and range during official and drive cycles from gothenburg, sweden," *IEEE Transactions on Vehicular Technology*, vol. 65, no. 6, pp. 3964–3980, 2015.

[12] J. O. Estima and A. J. Marques Cardoso, "Efficiency analysis of drive train topologies applied to electric/hybrid vehicles," *IEEE Transactions on Vehicular Technology*, vol. 61, no. 3, pp. 1021–1031, 2012.

[13] J. Pavlovic, A. Marotta, and B. Ciuffo, "Co2 emissions and energy demands of vehicles tested under the nedc and the new wltp type approval test procedures," *Applied Energy*, vol. 177, pp. 661–670, 2016.

[14] K. Muehlbauer and D. Gerling, "Improvement of energy efficiency in power electronics at partial load," in *IECON 2011 - 37th Annual Conference of the IEEE Industrial Electronics Society*, 2011, pp. 2775–2779.

[15] S. Jahdi, O. Alatise, C. Fisher, L. Ran, and P. Mawby, "An evaluation of silicon carbide unipolar technologies for electric vehicle drive-trains," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 3, pp. 517–528, 2014.

[16] K. Emori, J. Niida, A. Okubo, K. Numakura, T. Hayashi, and T. Hara, "Sic inverter for electric vehicles with improved trade-off between reduced switching losses and increased radiation noise," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 4058–4062.

[17] T. Shimomura, T. Ikari, A. Okubo, R. Yamada, K. Numakura, and T. Hayashi, "High speed dv/dt control technology for sic power module for ev/hev inverters," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 5483–5486.

[18] M. Su, C. Chen, S. Sharma, and J. Kikuchi, "Performance and cost considerations for sic-based hev traction inverter systems," in *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2015, pp. 347–350.

[19] Kawahashi, "A new-generation hybrid electric vehicle and its supporting power semiconductor devices," in *2004 Proceedings of the 16th International Symposium on Power Semiconductor Devices and ICs*, 2004, pp. 23–29.

[20] T. Schoenen, M. S. Kunter, M. D. Hennen, and R. W. De Doncker, "Advantages of a variable dc-link voltage by using a dc-dc converter in hybrid-electric vehicles," in *2010 IEEE Vehicle Power and Propulsion Conference*, 2010, pp. 1–5.

[21] J. O. Estima and A. J. Marques Cardoso, "Efficiency analysis of drive train topologies applied to electric/hybrid vehicles," *IEEE Transactions on Vehicular Technology*, vol. 61, no. 3, pp. 1021–1031, 2012.

[22] Y. Ito, Y. Tsuruta, M. Bando, and A. Kawamura, "Bilateral sazz chopper circuit for hev," in *2006 37th IEEE Power Electronics Specialists Conference*, 2006, pp. 1–6.

[23] K. Kono, Y. Nakamura, and M. Yamamoto, "Optimal design of digital control system for interleaved boost chopper circuit with the coupled inductor," in *2011 IEEE Ninth International Conference on Power Electronics and Drive Systems*, IEEE, 2011, pp. 995–998.

[24] T. A. Meynard and H. Foch, "Multi-level conversion: High voltage choppers and voltage-source inverters," in *PESC'92 Record. 23rd Annual IEEE Power Electronics Specialists Conference*, IEEE, 1992, pp. 397–403.

[25] F. Z. Peng, "Z-source inverter," *IEEE Transactions on Industry Applications*, vol. 39, no. 2, pp. 504–510, 2003.

[26] H. Chen, H. Kim, R. Erickson, and D. Maksimović, "Electrified automotive powertrain architecture using composite dc–dc converters," *IEEE Transactions on Power Electronics*, vol. 32, no. 1, pp. 98–116, 2017.

[27] Y. Barsukov, "Battery cell balancing: What to balance and how," *Texas Instruments*, pp. 2–1, 2009.

[28] W. Bentley, "Cell balancing considerations for lithium-ion battery systems," in *The Twelfth Annual Battery Conference on Applications and Advances*, 1997, pp. 223–226.

[29] H. A. Gabbar, A. M. Othman, and M. R. Abdussami, "Review of battery management systems (bms) development and industrial standards," *Technologies*, vol. 9, no. 2, 2021, ISSN: 2227-7080.

[30] M. Lelie *et al.*, "Battery management system hardware concepts: An overview," *Applied Sciences*, vol. 8, no. 4, 2018.

[31] M. Daowd, N. Omar, P. Van Den Bossche, and J. Van Mierlo, "Passive and active battery balancing comparison based on matlab simulation," in *2011 IEEE Vehicle Power and Propulsion Conference*, 2011, pp. 1–7.

[32] N. Kutkut and D. Divan, "Dynamic equalization techniques for series battery stacks," in *Proceedings of Intelec'96 - International Telecommunications Energy Conference*, 1996, pp. 514–521.

[33] G. Landrum, T. A. Stuart, and W. Zhu, "Fast equalization for large lithium ion batteries," in *OCEANS 2008*, 2008, pp. 1–6.

[34] S. Kıvrak, T. Özer, Y. Oğuz, and M. M. Kelek, "Novel active and passive balancing method-based battery management system design and implementation," *Journal of Power Electronics*, vol. 21, no. 12, pp. 1855–1865, 2021.

[35] M. Einhorn, W. Roessler, and J. Fleig, "Improved performance of serially connected li-ion batteries with active cell balancing in electric vehicles," *IEEE Transactions on Vehicular Technology*, vol. 60, no. 6, pp. 2448–2457, 2011.

[36] F. Porpora *et al.*, "Performance analysis of active and passive equalizer circuits for lithium-ion cells," in *PCIM Europe digital days 2020; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2020, pp. 1–8.

[37] P. Harrop, *Electric vehicles go high voltage*, Jun. 2019.

[38] C. Hampel, *Lucid air to sport a 900-volt system*, [Online]. Available:https://www.electrive.com/2020/ 02/06/lucid-airto-sport-a-900-volt-system/, Feb. 2020.

[39] H. M. Group, *Hyundai motor invests in ionity to democratize highpower ev charging network*, [Online]. Available:https://www.hyundai.news/eu/brand, Sep. 2019.

[40] H. Tu, H. Feng, S. Srdic, and S. Lukic, "Extreme fast charging of electric vehicles: A technology overview," *IEEE Transactions on Transportation Electrification*, vol. 5, no. 4, pp. 861–878, 2019.

[41] J. de Santiago *et al.*, "Electrical motor drivelines in commercial all-electric vehicles: A review," *IEEE Transactions on Vehicular Technology*, vol. 61, no. 2, pp. 475–484, 2012.

[42] A. Bubert, K. Oberdieck, H. Xu, and R. W. De Doncker, "Experimental validation of design concepts for future ev-traction inverters," in *2018 IEEE Transportation Electrification Conference and Expo (ITEC)*, 2018, pp. 795–802.

[43] S. Khomfoi and L. M. Tolbert, "Multilevel power converters," in *Power electronics handbook*, Elsevier, 2011, pp. 455–486.

[44] A. Poorfakhraei, M. Narimani, and A. Emadi, "A review of multilevel inverter topologies in electric vehicles: Current status and future trends," *IEEE Open Journal of Power Electronics*, vol. 2, pp. 155–170, 2021.

[45] D. Ronanki and S. S. Williamson, "Modular multilevel converters for transportation electrification: Challenges and opportunities," *IEEE Transactions on Transportation Electrification*, vol. 4, no. 2, pp. 399–407, 2018.

[46] M. Quraan, T. Yeo, and P. Tricoli, "Design and control of modular multilevel converters for battery electric vehicles," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 507–517, 2016.

[47] M. Luh, T. Blank, and M. Weber, "Comparison and evaluation of modular multilevel converter topologies for li-ion battery systems," in *PCIM Europe 2017; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2017, pp. 1–8.

[48] M. Quraan, P. Tricoli, S. D'Arco, and L. Piegari, "Efficiency assessment of modular multilevel converters for battery electric vehicles," *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 2041–2051, 2017.

[49] L. Tolbert and F. Peng, "Multilevel converters for large electric drives," in *APEC '98 Thirteenth Annual Applied Power Electronics Conference and Exposition*, vol. 2, 1998, 530–536 vol.2.

[50] L. Tolbert, F. Z. Peng, T. Cunnyngham, and J. Chiasson, "Charge balance control schemes for cascade multilevel converter in hybrid electric vehicles," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 5, pp. 1058–1064, 2002.

[51] K. Ding, K. W. E. Cheng, S. X. Wang, D. H. Wang, and Z. Shi, "Five-level cascaded multilevel motor driver for electrical vehicle with battery charge management," in *2008 Australasian Universities Power Engineering Conference*, 2008, pp. 1–6.

[52] B. Sarrazin, N. Rouger, J. Ferrieux, and Y. Avenas, "Benefits of cascaded inverters for electrical vehicles' drive-trains," in *2011 IEEE Energy Conversion Congress and Exposition*, 2011, pp. 1441–1448.

[53] F. Chang, O. Ilina, M. Lienkamp, and L. Voss, "Improving the overall efficiency of automotive inverters using a multilevel converter composed of low voltage si mosfets," *IEEE Transactions on Power Electronics*, vol. 34, no. 4, pp. 3586–3602, 2019.

[54] F. Roemer, M. Ahmad, F. Chang, and M. Lienkamp, "Optimization of a cascaded h-bridge inverter for electric vehicle applications including cost consideration," *Energies*, vol. 12, no. 22, 2019. [Online]. Available: https://www.mdpi.com/1996-1073/12/22/4272.

[55] M. Safayatullah, M. T. Elrais, S. Ghosh, R. Rezaii, and I. Batarseh, "A comprehensive review of power converter topologies and control methods for electric vehicle fast charging applications," *IEEE Access*, vol. 10, pp. 40 753–40 793, 2022.

[56] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, and G. Sciutto, "A new multilevel pwm method: A theoretical analysis," in *21st Annual IEEE Conference on Power Electronics Specialists*, 1990, pp. 363–371.

[57] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 37–53, 2015.

[58] G. S. Konstantinou and V. G. Agelidis, "Performance evaluation of half-bridge cascaded multilevel converters operated with multicarrier sinusoidal pwm techniques," in *2009 4th IEEE Conference on Industrial Electronics and Applications*, 2009, pp. 3399–3404.

[59] Q. Tu and Z. Xu, "Impact of sampling frequency on harmonic distortion for modular multilevel converter," *IEEE Transactions on Power Delivery*, vol. 26, no. 1, pp. 298–306, 2011. DOI: 10.1109/TPWRD.2010.2078837.

[60] W. Han, T. Wik, A. Kersten, G. Dong, and C. Zou, "Next-generation battery management systems: Dynamic reconfiguration," *IEEE Industrial Electronics Magazine*, vol. 14, no. 4, pp. 20–31, 2020.

[61] W. Han, C. Zou, L. Zhang, Q. Ouyang, and T. Wik, "Near-fastest battery balancing by cell/module reconfiguration," *IEEE Transactions on Smart Grid*, vol. 10, no. 6, pp. 6954–6964, 2019.

[62] L. C. Casals, B. A. Garcia, and C. Canal, "Second life batteries lifespan: Rest of useful life and environmental analysis," *Journal of environmental management*, vol. 232, pp. 354–363, 2019.

[63] Z. Zhang, Y.-Y. Cai, Y. Zhang, D.-J. Gu, and Y.-F. Liu, "A distributed architecture based on microbank modules with self-reconfiguration control to improve the energy efficiency in the battery energy storage system," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 304–317, 2016. DOI: 10.1109/TPEL.2015.2406773.

[64] S. K. Mandal, P. S. Bhojwani, S. P. Mohanty, and R. N. Mahapatra, "Intellbatt: Towards smarter battery design," in *2008 45th ACM/IEEE Design Automation Conference*, 2008, pp. 872–877.

[65] A. Badam *et al.*, "Software defined batteries," in *Proceedings of the 25th Symposium on Operating Systems Principles*, 2015, pp. 215–229.

[66] S. Ci, N. Lin, and D. Wu, "Reconfigurable battery techniques and systems: A survey," *IEEE Access*, vol. 4, pp. 1175–1189, 2016.

[67] D. F. Frost and D. A. Howey, "Completely decentralized active balancing battery management system," *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 729–738, 2018.

[68] M. Ricco, J. Meng, T. Gherman, G. Grandi, and R. Teodorescu, "Smart battery pack for electric vehicles based on active balancing with wireless communication feedback," *Energies*, vol. 12, no. 20, 2019. [Online]. Available: https://www.mdpi.com/1996-1073/12/20/3862.

[69] A. Otto *et al.*, "Battery management network for fully electrical vehicles featuring smart systems at cell and pack level," in *Advanced Microsystems for Automotive Applications 2012*, Springer Berlin Heidelberg, 2012.

[70] S. A. Mathew, R. Prakash, and P. C. John, "A smart wireless battery monitoring system for electric vehicles," in *2012 12th International Conference on Intelligent Systems Design and Applications (ISDA)*, 2012, pp. 189–193.

[71] G. Tresca, R. Leuzzi, A. Formentini, L. Rovere, N. Anglani, and P. Zanchetta, "Reconfigurable cascaded multilevel converter: A new topology for ev powertrain," in *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2021, pp. 1454–1460.

[72] Z. Zheng, K. Wang, L. Xu, and Y. Li, "A hybrid cascaded multilevel converter for battery energy management applied in electric vehicles," *IEEE Transactions on Power Electronics*, vol. 29, no. 7, pp. 3537–3546, 2014.

[73] V. Johnson, "Battery performance models in advisor," *Journal of power sources*, vol. 110, no. 2, pp. 321–329, 2002.

[74] B. Y. Liaw, G. Nagasubramanian, R. G. Jungst, and D. H. Doughty, "Modeling of lithium ion cells—a simple equivalent-circuit model approach," *Solid state ionics*, vol. 175, no. 1-4, pp. 835–839, 2004.

[75] B. Xia, Z. Sun, R. Zhang, and Z. Lao, "A cubature particle filter algorithm to estimate the state of the charge of lithium-ion batteries based on a second-order equivalent circuit model," *Energies*, vol. 10, no. 4, p. 457, 2017.

[76] Y. Wang *et al.*, "A comprehensive review of battery modeling and state estimation approaches for advanced battery management systems," *Renewable and Sustainable Energy Reviews*, vol. 131, p. 110 015, 2020, ISSN: 1364-0321.

[77] T. R. B. Grandjean, J. Groenewald, A. McGordon, W. D. Widanage, and J. Marco, "Accelerated internal resistance measurements of lithium-ion cells to support future end-of-life strategies for electric vehicles," *Batteries*, vol. 4, no. 4, 2018.

[78] H.-G. Schweiger *et al.*, "Comparison of several methods for determining the internal resistance of lithium ion cells," *Sensors (Basel, Switzerland)*, vol. 10, pp. 5604–25, Jun. 2010.

[79] M. Tang, Y. Chen, and T. Yang, "Field weakening design for a high speed nine-phase permanent magnet synchronous machine in more electric aircraft," in *2022 IEEE Transportation Electrification Conference & Expo (ITEC)*, 2022, pp. 1093–1096.

[80] G. Tresca, A. Formentini, S. Granata, R. Leuzzi, and P. Zanchetta, "Direct ac charging of ev reconfigurable cascaded multilevel converter," in *2022 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2022, pp. 1–8. DOI: 10.1109/ECCE50734.2022.9947306.

[81] M. Nassary, M. Orabi, and M. Ghoneima, "Discussion of single-stage isolated unidirectional ac-dc on-board battery charger for electric vehicle," in *2018 IEEE 4th Southern Power Electronics Conference (SPEC)*, 2018, pp. 1–7.

[82] T. Lahlou, M. Abdelrahem, S. Valdes, and H.-G. Herzog, "Filter design for grid-connected multilevel chb inverter for battery energy storage systems," in *2016 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM)*, 2016, pp. 831–836.

[83] Z. Ling, Z. Zhang, Z. Li, and Y. Li, "State-of-charge balancing control of battery energy storage system based on cascaded h-bridge multilevel inverter," in *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, 2016, pp. 2310–2314.

[84] W.-Y. Chang, "The state of charge estimating methods for battery: A review," *International Scholarly Research Notices*, vol. 2013, 2013.

[85] G. Tresca, A. Formentini, S. Di Salvo, R. Leuzzi, N. Anglani, and P. Zanchetta, "Reconfigurable cascaded multilevel converter design for battery energy system storage," in *2022 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM)*, 2022, pp. 725–729.

[86] J. Dragoun, J. Talla, and T. Košan, "Control of multilevel chb converter for battery energy storage system," in *2021 IEEE 19th International Power Electronics and Motion Control Conference (PEMC)*, 2021, pp. 836–842.

[87] N. Kawakami *et al.*, "Development of a 500-kw modular multilevel cascade converter for battery energy storage systems," *IEEE Transactions on Industry Applications*, vol. 50, no. 6, pp. 3902–3910, 2014.

[88] J. Wang, X. Tang, and Z. Yin, "Research on medium voltage battery energy storage system based on rt-lab," in *2014 IEEE Conference and Expo Transportation Electrification Asia-Pacific (ITEC Asia-Pacific)*, 2014, pp. 1–5.

[89] L. Maharjan, S. Inoue, and H. Akagi, "A transformerless energy storage system based on a cascade multilevel pwm converter with star configuration," *IEEE Transactions on Industry Applications*, vol. 44, no. 5, pp. 1621–1630, 2008.

[90] E. Chatzinikolaou and D. J. Rogers, "A comparison of grid-connected battery energy storage system designs," *IEEE Transactions on Power Electronics*, vol. 32, no. 9, pp. 6913–6923, 2017.

[91] Infineon, *Iposim*. [Online]. Available: `http://iposim.infineon.com`.

[92] D. Graovac, M. Purschel, and A. Kiep, "Mosfet power losses calculation using the data-sheet parameters," *Infineon application note*, vol. 1, pp. 1–23, 2006.

[93] A. Galassini, G. Lo Calzo, A. Formentini, C. Gerada, P. Zanchetta, and A. Costabeber, "Ucube: Control platform for power electronics," in *2017 IEEE Workshop on Electrical Machines Design, Control and Diagnosis (WEMDCD)*, 2017, pp. 216–221.

[94] Xilinx, "7 series fpgas and zynq-7000 soc xadc dual 12-bit 1 msps analog-to-digital converter," *https://www. xilinx. com/support/documentation/user_guides/ug480_7Series_XADC. pdf*, 2018.

[95] C. Diligent, "A7 reference manual, rev," *B, Jun*, vol. 24, 2016.

[96] M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "A new single-phase pll structure based on second order generalized integrator," in *2006 37th IEEE Power Electronics Specialists Conference*, 2006, pp. 1–6.

[97] F. Chang, F. Roemer, and M. Lienkamp, "Influence of current ripples in cascaded multilevel topologies on the aging of lithium batteries," *IEEE Transactions on Power Electronics*, vol. 35, no. 11, pp. 11 879–11 890, 2020.