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Mm-Wave Quadrature Signal Generation for 5G Wireless Communication Networks

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Abstract

The demand for an enriched end-user experience and increased performance in next generation electronic applications is never ending, and it is a common trend for a wide spectrum of applications owing to different markets, like computing, mobile communication and automotive. For this reason, wireless transceivers have become widespread components for nowadays electronics with a constant demand for power reduction and data-rate increase.

Data-rates in wireless communications have been steadily increasing with on-chip processing rate and logic density both in network applications and in hard disk interconnects. The data-rates are now exceeding 1-Gbps and expected to grow exponentially in next years as new standards are going to release together with the enormous amount of unlicensed bandwidth in the mm-Wave spectrum like Ka-Band and E-Band.

The development of 5G communication systems is underway. Point-to-point wireless links in the E-Band can provide high data-rate, easily deployable, cheap and exible Backhaul solutions, important enablers for the mobile network evolution towards 5G network. The development of CMOS/BiCMOS integrated transceivers for E-Band Backhaul applications can help reducing the cost and footprint of the equipment, but presents design challenges, mostly related to the use of adaptive spectrally efficient high-order modulations, which mandate high linearity and low Phase-Noise and precise Quadrature LO waveforms. In example when employing 64-Quadrature Amplitude Modulation (64-QAM), very high Image Rejection Ratio (IRR) >35dB levels are required to limit Error Vector Magnitude (EVM).

In the frame of gigabit wireless systems, the work discussed in this thesis concerns with local-oscillator (LO) generation requirements for Ka-Band and E-Band, Access and Backhaul applications spanning from the concept of the circuit to its implementation. Quadrature LO specifications for the Transmitters

identified, and design and realization of quadrature generation structure is proposed. A Ka-Band Polyphase Filter (PPF) implemented as key block of the Quadrature LO generation. It achieves ultra-low phase and amplitude imbalance, while still achieving a very low Phase noise level. Phase error detection feedback structure used to maintain the performance across wide bandwidth and PVT variations discussed in detail. Finally, same circuit technique of Ka-Band design used in higher frequency range (E-band) with some improvements to implement a transmitter accompanying a full TX project.

Ka-Band Prototype realized in a 55nm CMOS technology. Measurements show an IRR >40 dB across the 28-44 GHz, 44% fractional bandwidth and Phase-Noise as low as input phase noise level of -138 dBc/Hz at 1MHz offset from 36GHz carrier. Power consumption is 39 mW overall.

E-Band Prototype realized in a 55nm BiCMOS technology. Measurements show an IRR >40 dB across the 66-88 GHz bandwidth covering full E-band spectrum. Power consumption is 186 mW.

This dissertation demonstrates advances over State-Of-The-Art primarily in terms of IRR and bandwidth performance, and shows how the proposed circuit technique is suitable as critical LO building block in IQ modulators and direct-conversion transceivers.

The work has performed in the Analog Integrated Circuits Laboratory (AICLab) of Universita degli Studi di Pavia in collaboration with STMicroelectronics and Huawei. The dissertation is part of broader system to demonstrate and design a complete 5G E-Band transmitter.

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List of Acronyms

3G – 3rd Generation

4G – 4th Generation

5G – 5th Generation

AC – Alternate Current

AM – Amplitude Modulation

AP – AluCap

BEOL – Back End Of The Line

BER – Bith Error Rate

BiCMOS – Bipolar-CMOS Technology

BJT – Bipolar Junction Transistor

BTS – Base Tranceiver Station

BW – Bandwidth

CMOS – Complementary Metal-Oxide Semiconductor

DC- Direct Current

EDGE- Enhanced Data-Rates Evolution

EM- Electro-Magnetic

EVM- Error Vector Magnitude

fT – Unity Current Gain frequency

FDSOI – Fully depleted Silicon-On-Insulator

FEOL – Front End Of the Line

FET – Filed Effect Transistor

FM-Frequency Modulation

FoM – Figure Of Merit

GBW- Gain Bandwidth Product

GO2 – Thick Oxide

GP- General Purpose

GSM – Global System for Mobile

HBT – Hetrojunction Bipolar Transistor

I/O – Input/Output

IC- Integrated Circuit

ICT – Information and Communication Technology

IoT – Internet of Things

IRR- Image Rejection Ratio

L – Inductance

LAN – Locak Area Network

LO – Local Oscilator

LoS – Line-of-Sight

LP – Low Power

LTE- Long-Term Evolution

M - Metal

MIMO – Multiple-Input and Multiple-Output

mm-Wave – Millimiter Wave

MOM – Metal-Oxide-Metal Capacitor

MOS – Metal-Oxide Semiconductor

PA – Power Amplifier

PLL – Phased Locked Loop

PtP – Point-to-Point

Q – Quality Factor

QC – Capacitor Quality Factor

QL – Inductor Quality Factor

QAM – Quadrature Amplitude Modulation

QPSK – Quadrature Phase-Shift Keying

RF – Radio Frequency

RMS – Root Mean Square

RX - Receiver

Si – Silicon

SiGe – Silicon Germanium

TX – Transmitter

UWB – Ultra Wide Band

VDD – Supply Voltage

VCO – Voltage Controlled Oscilator

WAN – Wide Area Network

WLAN – Wireless Local Area Network

To,

My Mother, My Father My Sisters, My Brother and All of My lovely Familly.

This Would not be possible without being away for almost six years from my family for the Master and Ph.D. educations but still getting warm and strong support and motıvation which kept me going.

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Introduction

The ever-increasing mobile data traffic and consumer experience requirements, promptly rising multimedia communication, home entertainment, high-resolution video sharing etc. increases the load on 3G/4G systems in particular in terms of communication capacity and speed. Considering above-mentioned points, the expectation to grow by >8x from 2015 to 2020 [1], is driving continuous innovation in wireless communications, and next generation mobile networks (i.e. 5G and beyond) are foreseen to provide several Gbps data rates per each user. Although the picture is not clear yet on how to overcome the performance limitations of the current 4G-LTE standard, all the proposed hardware solutions anticipate a further increase in the base-transceiver-station (BTS) density, the trend that has kept going in the last twenty years [2]. To achieve the above targets, several key technologies (e.g., massive MIMO (Multiple-Input Multiple-Output), ultra-dense networks, and all-spectrum access) will be used.

The BTS density increase, rises the complexity of the network, both in access side and the backhaul infrastructure, i.e. the wide-bandwidth link connecting the user to the BTS, plus the set of links connecting the BTS to the network core, is emerging as a critical bottleneck in future-generation mobile networks [2, 3]. To push forward with the network evolution, two directions are emerging in the industry. First, new hardware solutions are being investigated to provide high-capacity, easily deployable, medium-range links, suitable for dense BTS environments. Among the proposed competitors, mm-Wave wideband wireless links, in the Ka-Band for access and E-Band for backhauling in particular, are emerging as a promising solution [2, 4]. Second, as BTS reach high-volume productions, fully integrated BTS transceivers in CMOS or

BiCMOS technology can reduce the cost of backhaul equipment [4]. These emerging paths create new opportunities in mm-Wave integrated circuit design.

Unlike other mm-Wave applications such as 60GHz WLAN or automotive radars, Ka-Band and E-Band links employ higher order modulations to maximize the channel capacity. This mandates challenging specifications for integrated transceivers, especially concerning power-amplifier (PA) linearity, Quadrature LO amplitude and phase accuracy and local-oscillator (LO) phase noise.

In this work, mm-wave transmitters (Tx) requirements are addressed, proposing novel quadrature LO generation building block, namely a tunable Polyphase filter (PPF) and a phase detection feedback loop. The overall structure achieves ultra-precise quadrature LO waveforms with negligible additive phase noise at the output with CMOS-compatible power supply, and allows very high order nodulations according to the system requirements. Same technique utilized in both Ka-band and E-band frequency range and finally a full E-band transmitter is designed for demonstration. Prototypes realized in BiCMOS 55nm technology, BiCMOS being the preferred technology platform for mm-Wave transceivers [4]. The research activity carried on in collaboration with STMicroelectronics and Huawei, in the framework of the E-band transmitter project, funded by the HiSilicon. The work structured as follows.

Thesis Organisation

In Chapter 1, an overview of mm-wave wireless links suitable for 5G networks provided. The motivation for mm-Wave access and backhaul deployment in next-generation mobile scenarios outlined, propagation characteristics and spectrum regulations in the Ka-Band and E-Band mentioned.

In Chapter 2, the state of the art of integrated transceivers briefly reviewed. Major parameters and non-idealities of transmitters and their effect on Tx performance are mentioned.

In Chapter 3, an mm-wave quadrature signal generation circuit leveraging tunable Polyphase filter presented. After outlining the operating principle of the circuit, an analytical model describing system behavior and image rejection ratio (IRR) in presence of Amplitude and phase imbalance provided. A transformer-coupled solution proposed for Inter-stage matching network and measurement results on the test chip provided.

Chapter 4 deals with design techniques for wideband E-band Tx including Quadrature LO generation, up conversion mixer and power amplifier (PA) [which is in collaboration inside a broader Project] utilizing the tunable PPF to maximize the IRR. Measurements and comparison with state-of-the-art presented.

Chapter 1: mmWave Links for future Generation Wireless Networks

In this Chapter, an introduction to mm-Wave links suitable for future generation (5G etc.) wireless telecommunication networks including access and backhauling outlined. Firstly, major specifications and requirements of the next-generation mobile network is focused together with the main applications, then, Ka-Band and E-Band wireless links are briefly described, outlining the challenges concerning the robustness of the communication and discussing the outcoming standards and regulations.

1.1 5G Vision

Since 1980s the Information and Communications Technologies (ICT) has kept growing, providing an increasing amount of end-user oriented applications and benefits. During the past years, both mobile and fixed data traffic has grown exponentially due to the impressive growth of the smartphones, tablets, laptops etc. The demand for the wireless connectivity will be even larger in the future [1-3]. As an example, the 4G network enabled a hugely improved multimedia experience as broadband wireless networks started to takeover wired connections. Following this trend next generation networks will require sharing an enormous amount of data in a real-time response to wireless users stressing the network capacity. In order to enable connectivity for a very wide range of applications with new characteristics and requirements, LTE wireless access capabilities must extend far beyond those of previous generations of mobile communication. The further evolution of mobile networks towards 5th-Generation driven by these capabilities [4, 5]:

i) System capacity

Mobile data-traffic is expected to exponentially increase in next years stressing the network capacity which will evolve toward new model in device-to-device

management and connectivity while still preserving the overall service quality and multimedia experience for the end-user pushed by the deployment of billions of M2M-connected devices (Figure **1.1**). For this evolution to be sustainable 5G networks must deliver data with much lower cost per bit, compared to nowadays network while facing the problem of managing a larger energy footprint, it requires a much more power-friendly management of the network links than current cellular networks.

Figure 1.1: Connected Devices growth forecast in next years: The exponential increase in connected devices will seriously affect the Network Structure.

ii) Data-Rates

A common trend in mobile network evolutions is the continuous data-rate increase from each generation to the next. This trend driven so far by the deployment of UHD video streaming services and the need to provide pervasive cloud computing. This trend is a built-in in the next network evolution step but with a prominent assortment with respect to the past. Instead of focusing uniquely on the peak data-rate, next generation connectivity puts ubiquitous access to the network and services under real-life conditions in different scenarios as specific target on the to-do list. 5G should support data-rates exceeding 10 Gbps in specific scenarios such as indoor and dense outdoor environments. Data-rates of several 100 Mbps should generally be achievable in urban and suburban environments. Data-rates of at least 10 Mbps should be

accessible almost everywhere, including rural areas (Figure **1.2**) providing uniform distribution.

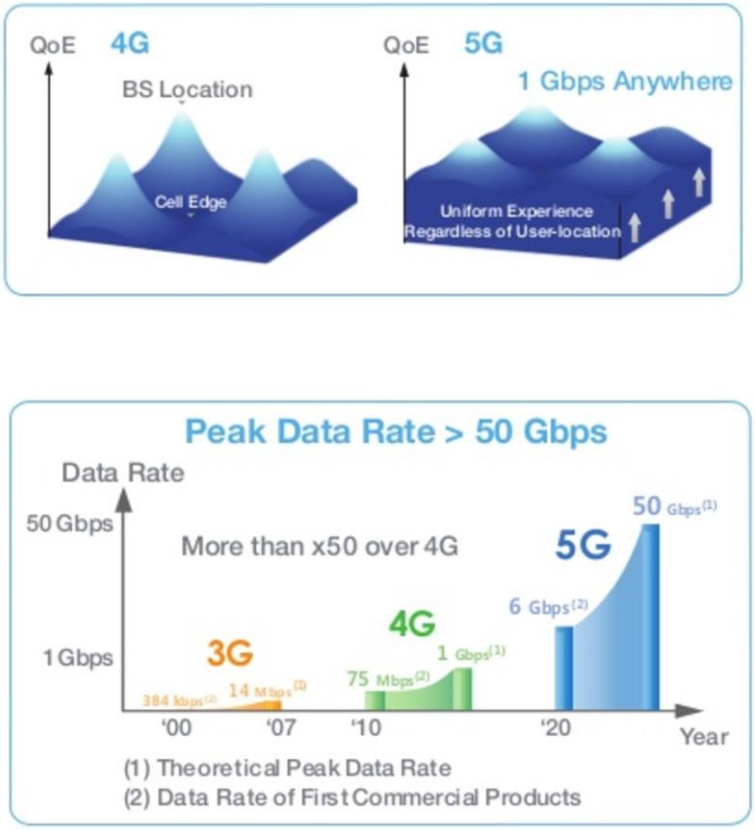

Figure 1.2: Data-rates and uniformity Comparison.

iii) Latency

Specifically designed to enable M2M communications and applications rather than the multimedia expansion, a key point represented by low latency [2]. This aspect is one of the most remarkable barriers in current mobile communication systems which are preventing some futuristic visions from being deployed such as traffic safety and control of critical infrastructure and industry processes. To support such latency-critical applications, 5G expected to deliver impressive data-rates with end-to-end latency of 1ms or less (Figure **1.3**). This will create new capabilities for real-time communication and will allow ultra-high service reliability in a variety of scenarios, ranging from entertainment to industrial process control.

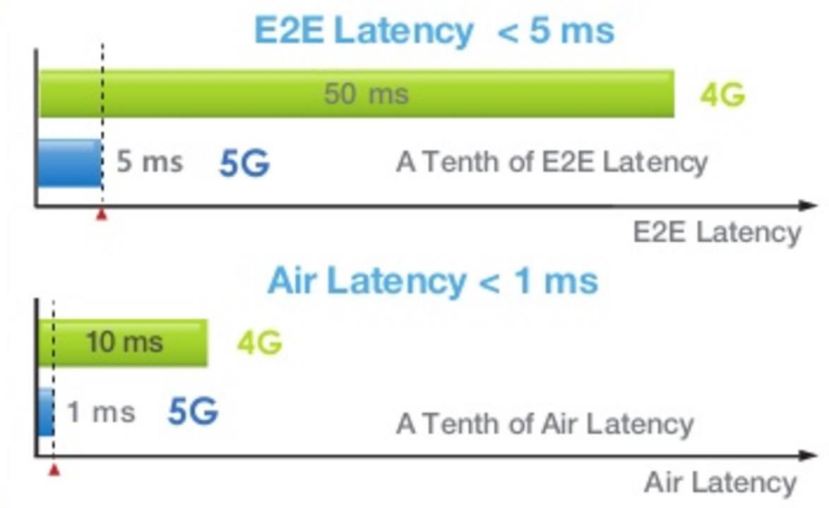

Figure 1.3: Ultra-Low latency in 5G network.

iv) Reliability and Availability

Being set up in various critical scenarios, 5G links should also enable connectivity with ultra-high proving and ultra-rare quality connectivity deviation from service specifications.

v) Cost and Energy consumption

"Green-policy" from the power dissipation and energy point of view expected to be a key point while "Low-cost" has been the major market driver since the early days of mobile communication. While “low-cost" is guaranteed by the technological scaling at a rate set by the Moore’s law, a smart power management and increase of the battery life.

vi) Efficiency

One of the key enablers for high throughput in 5G is densely deployed small cells. In order to take full advantage of these massive-scale small cells, 5G network should be a lot more efficient in cost and energy usage. The mentioned requirements partly clash with each other, and will require a holistic, heterogeneous environment having to deal with multiple network layers, several co-existing access and Backhaul technologies [2, 3, 5].

1.2 5G Challenges

5G targets are evidently ambitious and intensify the design challenges of the holistic 5G network. Providing Access and Backhaul infrastructure to 5G and Small-Cell networks is complicated, and Backhaul capacity and power consumption expected to become a major bottleneck in the network evolution [2, 6, 7]. As depicted before, 5G scenarios need high capacity (> 10 Gbps), low-latency (< 1 ms), and reliable Backhaul connections [8]. Figure 1.1 shows the demand for wireless data traffic and the number of connected devices. Global mobile data traffic is expected to increase to Zettabytes by 2020, which is about a three times increase over 2016. In addition, the number of mobile devices and connections expected to grow to more than 20 billion by 2020. New technologies should emerge in order to satisfy this demand. Related to wireless data traffic, one of the key parameters to consider is wireless throughput (bits/s) which defined as:

$$\text{Throughput} = \text{Bandwidth (Hz)} \times \text{Spectral efficiency (bits/s/Hz)}.$$

Clearly, to improve the throughput, some new technologies, which can increase the bandwidth or the spectral efficiency, or both should be exploit.

In wireless communication, the transmitted signals attenuated by fading due to multipath propagation and by shadowing due to large obstacles between the transmitter and the receiver, yielding a fundamental challenge for reliable communication. Transmission with multiple-input multiple-output (MIMO) antennas is a well-known diversity technique to enhance the reliability of the communication. Furthermore, with multiple antennas, multiple streams can have sent out and hence, we can obtain a multiplexing gain, which significantly improves the communication capacity. MIMO systems have gained significant attention for the past decades, and are now being incorporated into several new generation wireless standards (e.g., LTE-Advanced, 802.16m).

The effort to exploit the spatial multiplexing gain has shifted from MIMO to multiuser MIMO (MU-MIMO), where several users simultaneously served by a multiple-antenna base station (BS). With MU-MIMO setups, a spatial multiplexing gain could be achieved even if each user has a single antenna [9]. This is important since users cannot support many antennas due to the small physical size and low cost requirements of the terminals, whereas the BS can support many antennas. MU-MIMO does not only reap all benefits of MIMO systems, but also overcomes most of propagation limitations in MIMO such as ill-behaved channels. Specifically, by using scheduling schemes, we can reduce the limitations of ill-behaved channels. LOS propagation, which causes significant reduction of the performance of MIMO systems, is no longer a problem in MU-MIMO systems. Thus, MU-MIMO has attracted substantial interest [9-14]. There always exists a tradeoff between the system performance and the implementation complexity. The advantages of MU-MIMO come at a price:

- Multiuser interference: the performance of a given user may significantly degrade due to the interference from other users. To tackle this problem, interference reduction or cancellation techniques, such as maximum likelihood multiuser detection for the uplink [7], dirty paper coding (DPC) techniques for the downlink [9], or interference alignment [15], should be used. These techniques are complicated and have high computational complexity.
- Acquisition of channel state information: in order to achieve a high spatial multiplexing gain, the BS needs to process the received signals coherently. This requires accurate and timely acquisition of channel state information (CSI). This can be challenging, especially in high mobility scenarios.
- User scheduling: since several users are served on the same time-frequency resource, scheduling schemes that optimally select the group of users depending on the precoding/detection schemes, CSI knowledge

etc., should be considered. This increases the cost of the system implementation.

The more antennas the BS is equipped with, the more degrees of freedom are offered and hence, more users can simultaneously communicate in the same time-frequency resource. As a result, a huge sum throughput can obtained. With large antenna arrays, conventional signal processing techniques (e.g. maximum likelihood detection) become prohibitively complex due to the high signal dimensions. The main question is whether we can obtain the huge multiplexing gain with low-complexity signal processing and low-cost hardware implementation. In [16], Marzetta showed that the use of an excessive number of BS antennas compared with the number of active users makes simple linear processing nearly optimal. More precisely, even with simple maximum-ratio combining (MRC) in the uplink or maximum-ratio transmission (MRT) in the downlink, the effects of fast fading, intra-cell interference, and uncorrelated noise tend to disappear, as the number of BS station antennas grows large. MU-MIMO systems, where a BS with a hundred or more antennas simultaneously serves tens (or more) of users in the same time frequency resource, are known as Massive MIMO systems (also called very large MU-MIMO, hyper-MIMO, or full-dimension MIMO systems). In Massive MIMO, it expected that each antenna would be contained in an inexpensive module with simple processing and a low-power amplifier. The main benefits of Massive MIMO systems are:

- Huge spectral efficiency and high communication reliability: Massive MIMO inherits all gains from conventional MU-MIMO, i.e., with M-antenna BS and K single-antenna users, we can achieve a diversity of order M and a multiplexing gain of min (M, K). By increasing both M and K, we can obtain a huge spectral efficiency and very high communication reliability.
- High-energy efficiency: In the uplink Massive MIMO, coherent combining can achieve a very high array gain which allows for substantial reduction in the transmit power of each user. In the downlink,

the BS can focus the energy into the spatial directions where the terminals are located. As a result, with massive antenna arrays, an order of magnitude, or more can reduce the radiated power, and hence, we can obtain high-energy efficiency. For a fixed number of users, by doubling the number of BS antennas, while reducing the transmit power by two, we can maintain the original the spectral efficiency, and hence, the radiated energy efficiency is doubled.

- Simple signal processing: For most propagation environments, the use of an excessive number of BS antennas over the number of users yields favorable propagation where the channel vectors between the users and the BS are pair wisely (nearly) orthogonal. Under favorable propagation, the effect of inter-user interference and noise can be eliminate with simple linear signal processing (liner precoding in the downlink and linear decoding in the uplink). As a result, simple linear processing schemes are nearly optimal. Another key property of Massive MIMO is channel hardening. Under some conditions, when the number of BS antennas is large, the channel becomes (nearly) deterministic, and hence, the effect of small-scale fading averaged out. The system scheduling, power control, etc., could be done over the large-scale fading time scale instead of over the small-scale fading time scale. This simplifies the signal processing significantly.

Massive MIMO is a promising candidate technology for next-generation wireless systems. Recently, there has been a great deal of interest in this technology [17-21]. Although there is much research work on this topic, a number of issues still need to be tackled before reducing Massive MIMO to practice [22-29]. Inspired by the above discussion, in this dissertation, we study the

Moreover, Cell coverage area shrinking and BTS densification (following the path which has already been traced in previous network generations, as shown in Figure 1.4) enable efficient spectral reuse leveraging spatial diversity

whilst providing superior Signal-to-Noise Ratio (SNR) at given bandwidth, thus allowing more spectrally-efficient modulations [30, 31]. While SNR benefits from BTS densification, interference does not scale down with cell area coverage as well resulting in Signal-to-Interference-and-Noise Ratio (SINR) worsening [2]. Therefore, new concepts and techniques are asked to mitigate the defend link integrity from undesired out-of-channel or out-of-applications signals, both in BTS and user terminals [30].

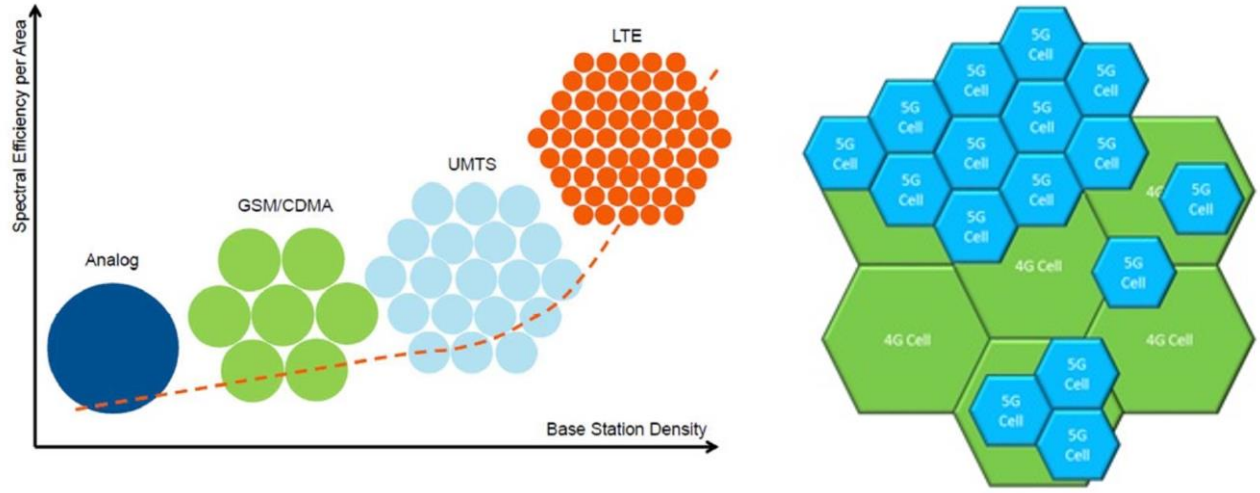

Figure 1.4: Base Station densification trends: (a) - the trend is shrinking cell size and density while reducing energy-per-link as well; (b) - 5G cells will be far smaller then 4G cells requiring highly hierarchical network structure and coordination protocols at the edge of the cells.

Millimeter-Wave (mm-Wave) links are expected to be adopted in order to give access to the huge amount of unused spectrum above 10 GHz who can widely increase the communication bandwidth [8, 32].

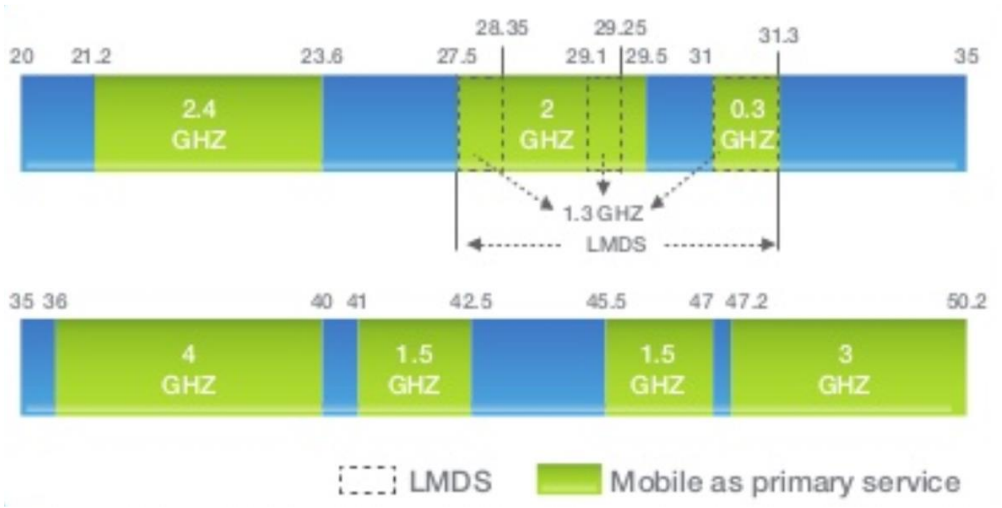

Figure 1.5: Potential 5G bands in 20-50 GHz range.

The mm-Wave bands provide 10 times more bandwidth than the 4G cellular-bands, as illustrated in Figure **1.5**. Several spectrum portions are under investigation by mobile operators.

In the lower mmW domain, 28 GHz (1 GHz spectrum available), 38 GHz (up to 4 GHz spectrum available) and 47 GHz (up to 5 GHz spectrum available, depending on the countries) licensed bandwidths are available [33]. Detailed studies on reactions and propagation in densely populated urban areas have been carried out showing promising results for mobile access [32, 34]. The 60 GHz band, featuring up to 9 GHz unlicensed spectrum, is also considered as an option for mmW access, although high propagation losses would require a too dense BTS environment [6]. Finally, 71-76 GHz and 81-86 GHz bands (E-band), featuring lower atmospheric attenuation and currently allocated for licensed fixed Backhaul radio links, could be used for mobile service as well [35].

Week diffractions in the mm-Wave bands determine higher free-space path loss (FSPL) and a consequent more fragile link. Fortunately, the small mm-Wave wavelength (λ) is naturally prone to highly directional beam forms that can be obtained by means of a large number of antenna elements in a smaller form factor, benefiting from dense BTS environment. These adaptive directional beams with large antenna array gain are key in combating the large

propagation loss in the mm-Wave, giving birth to Multiple-Input-Multiple-Output (MIMO) systems capable of steering different data streams to different users at the same time. Actually, the shrinking of cell size brings within the reduction of the (FSPL) as Line-of-Sight (LoS) links become more likely and the set of users to be covered scales down. Finally, as mmW links are mostly noise-limited, rather than interference-limited, the SINR efficiently scale with cell area shrinking [2, 34].

Massive MIMO systems have also been recently proposed as a way of increasing the channel capacity leveraging spatial diversity. It is based on spatial multiplexing, in which data streams from several branches are multiplexed and transmitted over several spatially separated channels [16, 18]. In fact, path loss between BTSs does not depend on frequency but relies on the TX and RX antenna aperture [36], which does reduce in proportion to the square of the frequency. That reduction can be compensated by the use of higher antenna directivity [34].

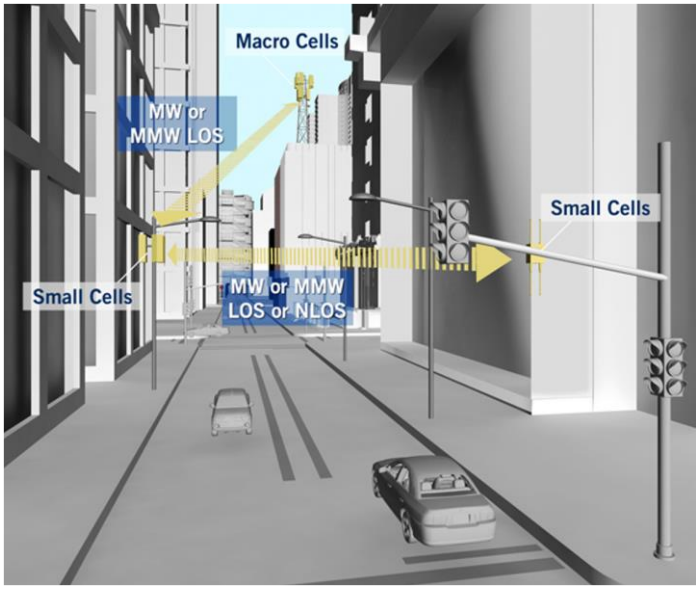

Figure 1.6: Typical Small/Macro-Cell scenario.

The 5G radio will employ K antenna elements to increase antenna aperture serving N < K users. In this framework, massive MIMO systems benefit as well from cell area shrinking, which implies having to manage a reasonable amount

of users. Beamforming will be used by BTS to track one another and improve energy transfer and SNR over an instantaneously configured link. Beamforming will also improve the radio environment by limiting interference to small fractions of the entire space reducing their impact on communication quality. Coordination calibration and data-distribution will be the major implementation challenges during the development of a hardware massive MIMO system while keeping array size, power and cost under acceptable values [36].

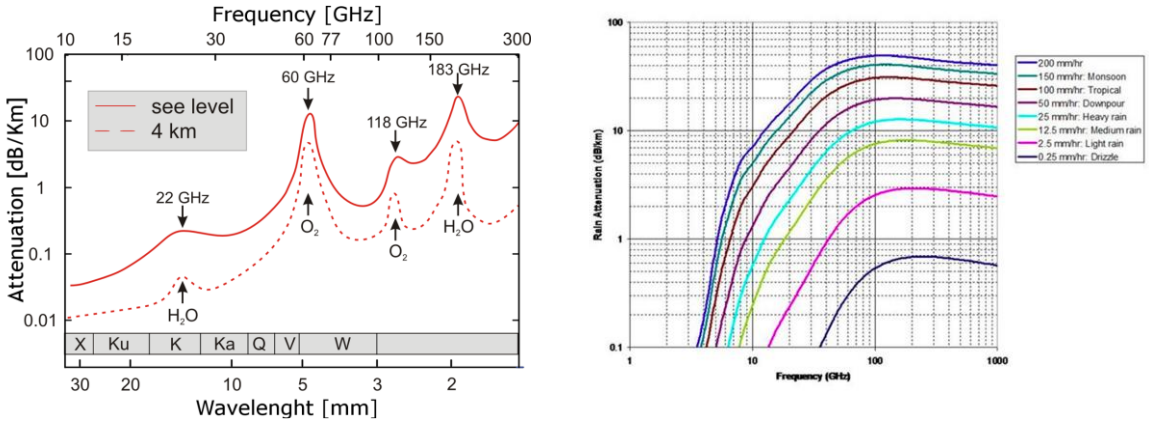

Figure 1.7: Attenuation in the mm-Wave spectrum: (a) - Air attenuation in the mm-Wave spectrum; (b) - Rain attenuation in the mm-Wave spectrum.

Each of the aforementioned techniques forecasts an increase in the BTS density. In the development towards 5G, the mobile infrastructure is expected to evolve towards Small-Cell (or Pico-Cell) Ultra-Dense Networks (UDN), where thousands of small BTS located at the street level provide mobile services to users, as shown in Figure **1.6** [3, 7, 37].

Small-Cell Backhaul links have to be cheap, easy to deploy and reconfigure owing to the proximity of transmitters and receivers, maximize area spectral efficiency through the tight reuse of the precious spectrum, and power-friendly as the Backhaul consumption is expected to grow up to ~50% of the BTS power budget [8]. However, as cell density rises, the Backhaul infrastructure complexity increases.

1.3 mm-Wave Wireless Point-to-Point Links

Optical connections can reach extremely high data-rates, but they are expensive and difficult to implement in ultra-dense scenarios [8, 30]. On the other hand, PtP mm-Wave links are expected to provide enough channel capacity for next-generation networks [8, 30]. Therefore, a huge interest in allocating future services in the huge amount of unlicensed spectrum above 10GHz has been shown by many companies and countries. 10 GHz of spectrum in the mm-Wave domain, in the E-Band in particular, have been allocated by American and European Committee for next generation PtP wireless Backhaul links [5, 38-41]. E-Band PtP links are expected to provide wideband, medium-range LoS links, suitable for backhauling Small-Cell UDN [5, 8].

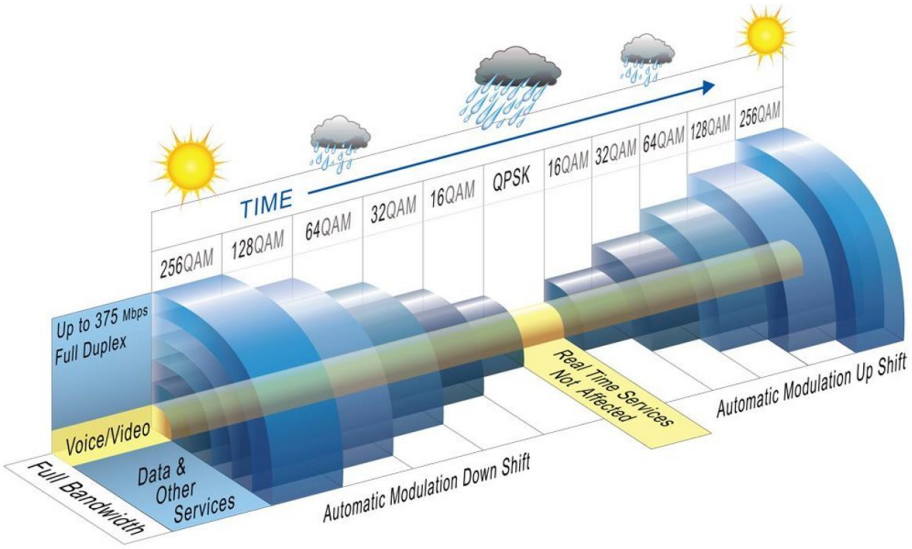

Figure 1.8: Adaptive modulation according to weather conditions in PtP radio service.

Two 5 GHz bandwidth (namely the 71-76 GHz and the 81-86 GHz portion of the spectrum) in the E-Band range have been identified to support Point-to-Point wireless links. Additionally, the 92-96 GHz band allocated in the USA only. As shown in Figure 1.7.a, atmospheric attenuation in the E-Band is as low as 0.5 dB/Km, much lower than in the 60 GHz band. By adopting high-gain, multi-array antennas (very compact at mm-Wave) the significant FSPL (i.e. ~130 dB over 1 Km distance) can be easily compensated in LoS PtP links. //

radiation absorption by water particles spread into atmosphere is another source of losses in the E-Band environment. While fog attenuation is negligible, rain losses can get up to tens of dB/Km (Figure **1.7**.b) limiting the practical operative range of E-Band LoS-PtP links to 1-2 Km, which is still suitable for Small-Cell backhauling [41]. In order to always achieve the maximum available channel capacity under any atmospheric condition, allowing the ubiquitous access to the network, proposed mm-Wave standards employ adaptive-modulation techniques, so as to change the modulation order according to channel conditions, as shown in Figure 1.8 [42, 43]. When high SNR is received, spectrally-efficient modulations like 64-QAM and beyond are employed. Instead, if the received SNR is poor (e.g. during heavy rain outage), simpler modulations such as QPSK are used preferring a lower data throughput over link robustness.

1.4 E-Band PtP Links Standard

In the European Union some rules for the E-Band PtP communications have been already provided and included in the (European Telecommunications Standards Institute) (ETSI) standard 302-217 [44].

	Channel Spacing [MHz]									
Number of Symbols	62.5	125	250	500	750	1000	1260	1500	1750	2000
2	35	71	142	285	427	570	712	855	997	1140
4	71	142	285	427	570	712	855	997	1140	//
8	106	212	425	850	1275	1700	2125	2550	2975	3400
16	142	570	1140	1710	2280	2850	//	//	//	//
32	219	438	875	1750	2625	//	//	//	//	//
64	262	525	1050	2100	3150	//	//	//	//	//
128	306	612	1225	1450	//	//	//	//	//	//
256	350	700	1400	2800	//	//	//	//	//	//

Table 1.1: Minimum required data-rate (in Mbps) for E-Band PtP transceivers complying to the ETSI standard 302-217, as a function of channel spacing and number of modulation symbols.

Recommended channel spacing and modulation orders summarized in Table 1.1, together with the minimum required data-rate. Standard channels are

250 MHz wide, but they can be split in two or four smaller sub-channels, or aggregated into wider channels up to 2 GHz if required in a channel-aggregation scenario [44]. Modulations up to 256-QAM are expected for standard channels, while lower-order solutions (e.g. 16-QAM) may be used in channel-aggregation scenarios [32]. The data-rate should reach ~3 Gbps using spectrally efficient modulations. The standard explicitly allows to change both the channel bandwidth and the modulation order on the fly according to channel conditions. Other significant requirements for E-Band transceivers are outlined in Table 1.2.

Min. Bit-Error Rate (**BER**)	10^{-6} or 10^{-10}
Carrier frequency tolerance	±50 ppm
Max. EIRP	85 dBm
Max. **TX** power	30 dBm
Min. antenna gain	38 dBi

Table 1.2: Significant requirements for E-Band wireless systems, according to the ETSI standard 302-217 and in compliance with European regulations.

1.5 E-Band Transceivers

As aforementioned above, "cheap", "compact" and "energy-efficient" will be key words in the development of a Small-Cell E-Band-BTS network infrastructure compared to the existing BTS transceivers, [2, 6, 45]. The need of a widespread and ubiquitous network architecture and the forecast growth in the BTS equipment sales, demands for a massive volume production relying on CMOS and BiCMOS technologies combined with low-power design techniques.

The stringent output power levels requirements set to power amplifiers (PA) motivates the frequent adoption of SiGe-BiCMOS processes [6]. Development of integrated transceivers for E-Band Backhaul is still in an early stage. However, IBM has presented a SiGe E-Band transceiver, shown in Figure

1.9 [46], supporting modulations up to 128-QAM [47]. As shown in the block diagram, the transceiver features a complete analog TX and RX front-end.

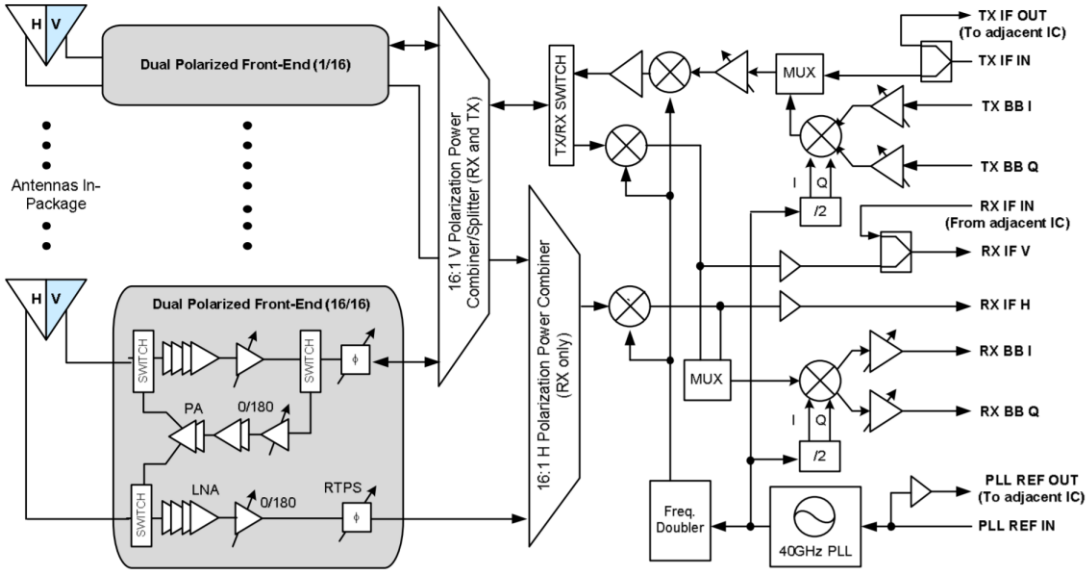

Figure 1.9: Schematic of the IBM E-Band backhaul transceiver.

LO-generation is performed using a VCO, embedded in a PLL, followed by a frequency doubler in parallel to a Divider-by-2 I and Q phases. The chipset covers 83-100 GHz band [6]. The prototype includes a complete TX and RX analog chain, and a complete frequency synthesizer. However, high-order-modulation transmission (i.e. 64-QAM) was only achieved using an external LO [48-50]. Infineon is also working on BiCMOS E-Band transceiver development, and recently presented a complete system transmitting modulated data up to 64-QAM [51]-58].

Research on analog building blocks for E-Band integrated transceivers is mainly focused on two different tracks: transmitters PAs and LO frequency synthesizers. On the TX side, much efforts have been spent developing PA's with high saturated output power and linearity, able to support high-order symbol constellations [53]. In the frequency synthesis domain, solutions have been proposed to achieve wide Tuning-Range (TR), provide accurate quadrature generation and minimize Phase-Noise avoiding the degradation of the transmitted symbol modulation.

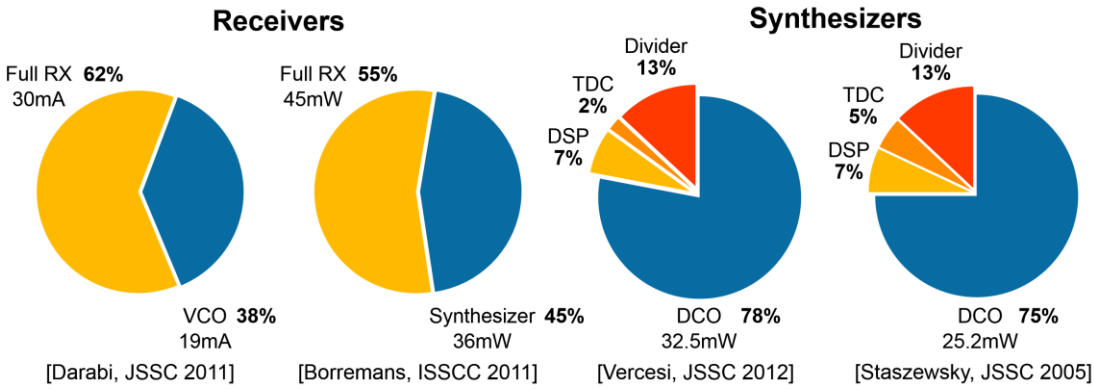

Figure 1.10: Power consumption of a frequency synthesizers in transceivers.

1.6 mmWave Communications: Architecture and Implementation

Driven by the ever-increasing consumer experience requirements, wireless communication undergoes a 10- year cycle for every generation of cellular advancement. To date, 3G and 4G wireless communication networks are widely deployed. However, rapidly expanding multimedia communication (such as large file transfer, home entertainment, gaming technology, and smart hardware) increase the burden on 3G/4G systems, particularly in terms of communication capacity and speed.

Considering the above facts, there has been much interest in 5G research from both academia and industry. It is expected that 5G wireless communication will be realized by 2020 or beyond. Compared to 4G systems, it is anticipated that 5G will achieve mobile traffic growth of 1000X, 100 billion connected devices, etc. To achieve the above targets, several key technologies (e.g., massive MIMO (Multiple-Input Multiple-Output), ultra-dense networks, and all-spectrum access) will be used.

To be more specific, 5G should meet the following specifications: 0.1~1 Gbit/s user experience data rate, tens Gbit/s peak data rate, ms-level end-to-end latency, and improvements of 100 times in terms of energy efficiency and cost reduction per bit, etc.

Because of the wide bandwidth characteristics, mm-Wave systems have advantages of high data rates and communication capacity, which benefit fixed access and cellular applications [59-62].

As opposed to sub-6 GHz, mm-Wave communication has unique characteristics. Accordingly, the main challenge for mm-Wave systems is the air interface design, particularly the RF front-end and antenna array. To achieve high data rate, high capacity, large coverage, it is very important to first understand the characteristics of the mm-Wave spectrum, and then the implementation issues. In addition, we will discuss the mm-Wave system architecture in next section.

1.6.1 mmWave Spectrum

As shown in Figure 1.11, a list of 5G candidate high-frequency bands ranging from 24 GHz to 86 GHz was selected at the WRC-15 conference (including 24.25~27.5, 31.8~33.4, 37~43.5, 45.5~50.2,50.4~52.6, 66~76, and 81~86 GHz bands). To speed up 5G research in the US, the FCC recently announced several licensed and unlicensed mm-Wave spectra, i.e., 28 GHz (27.5~28.35 GHz), 38 GHz (37~40 GHz), and 64~71 GHz [63]. It should be noted that with the existing 57~64 GHz unlicensed band, the US creates a 14 GHz contiguous spectrum at the 60 GHz band, i.e., the 57~71 GHz band. In this way, a myriad of new applications for consumer, business, industrial, and government use can be guaranteed.

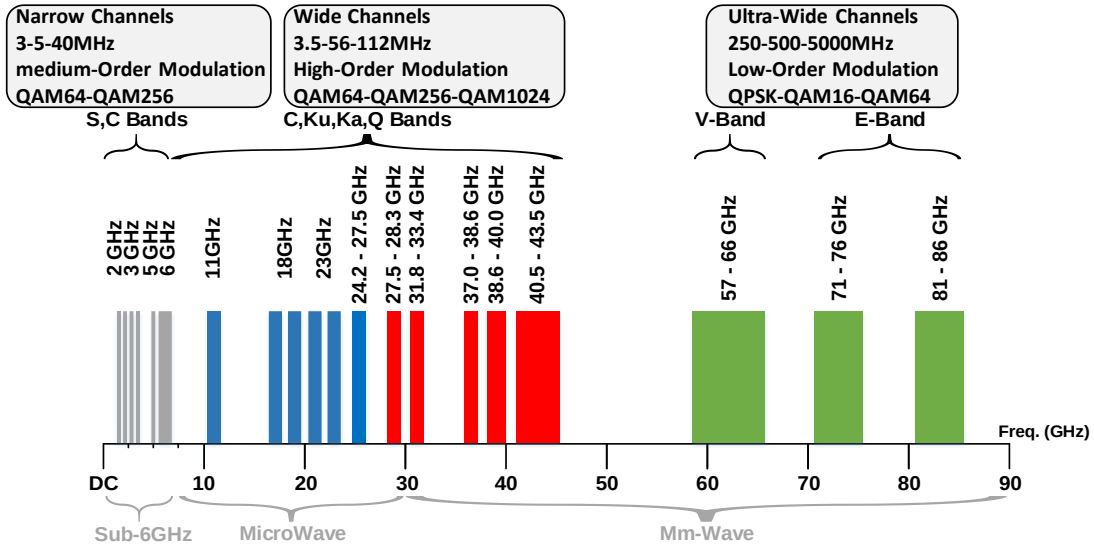

Figure 1.11: Available spectrum for wireless communication.

Compared with the traditional sub-6 GHz spectrum, the mm-Wave spectrum has several characteristics.

1) The mm-Wave spectrum is abundant, and it can easily achieve high data rates of the order of several Gbps even with low-order modulation.
2) As the free-space path-loss is proportional to the square of the link distance and carrier frequency, the mm-Wave spectrum has a very large propagation loss. In addition, the mm-Wave wavelength is very short, making it very susceptible to obstructions. To increase the coverage, considering the typical LOS (Line-of-Sight) and NLOS (Non-LOS) communication scenarios, the characterization of mm-Wave indoor and outdoor channels has been emerging as an important research topic [60]. From a system link budget perspective, the coverage can be extended by improving the system air interface performance, such as the transmitted power, receiver sensitivity, and antenna gain. However, these parameters depend largely on the implementation technology, which is to be discussed in Section 2.2.

3) Although the mm-Wave spectrum is very wide, its channel numbers are limited due to its wide bandwidth nature (500 MHz~2 GHz). In other words, the in-channel interference will become important, and interference control and mitigation techniques are needed.

1.6.2 Implementation Issues

Considering the future mass consumer market requirements, it is very critical to realize the mm-Wave system in a cost-effective and energy-efficient way, particularly in terms of the RF front-end chip, antenna, and packaging implementation aspects. In the past, the mm-Wave RF front-end chip is realized in compound process, with the penalty of high cost, high power, and low integration level. Guided by the ITRS (International Technology Roadmap for Semiconductors), the transistor feature size is reduced by Moore's law scaling, and the CMOS transistor speed and integration level are significantly improved [64]. Accordingly, the CMOS process is used to realize the mm-Wave RF front-end chip. Attracted by a potentially low cost, high integration level, and enhanced functionality, many academic and industrial groups are involved in CMOS mm-Wave circuit and system research and development for mm-Wave communication as well as for critical radar applications [65-70].

Despite the advantage of increased CMOS transistors speed due to size scaling, both the supply voltage and the ratio of the supply voltage to the transistor threshold voltage are also reduced. From the perspective of the mm-Wave circuit, this typically translates into a low signal swing and low signal dynamic range. On the other hand, the insertion loss of passive devices increases at mm-Wave frequencies, which further decreases the power gain of the active devices. Accordingly, it will result in a low output power and high phase noise for the power amplifier and oscillator, respectively [65]. These issues can be solved from a 5G system large-array architecture perspective, which is to be discussed shortly in next section.

As the interface between the RF chip and the air, the antenna and packaging plays an important role in terms of radiation pattern, efficiency, insertion loss, etc. Nowadays, because of the short wavelength at mm-Wave frequencies, antenna designs are shifting from conventional discrete designs to AoC (Antenna-on-Chip) and AiP(Antenna-in-Package) solutions. Compared with the AoC solution, AiP solutions offer a high gain, broad bandwidth, and cost-effective approach by incorporating multilayer substrate materials and chip-integration techniques. Moreover, the insertion loss between the antenna and chip can be minimized by providing a shorter interconnect.

Two kinds of interconnect techniques are available in the mainstream packaging industry: wire-bond and flip-chip techniques. The wire-bond technique, which is well established in consumer electronics, remains a very attractive solution because it is robust and inexpensive. However, if not carefully designed, the discontinuity introduced by the bond wire can significantly affect the performance of the interconnect. The flip-chip interconnect has a better performance than that of the wire bonding because of its less parasitic inductance; however, it is more expensive and complex.

1.6.3 System Architecture

Considering the unique characteristics of the mm-Wave frequency, an advanced RF transceiver architecture is needed to improve the system speed, energy efficiency, and spectral efficiency. With the high integration level in the chip and very compact antenna array, it is suitable to realize an mm-Wave system using MIMO and beamforming techniques [71-74].

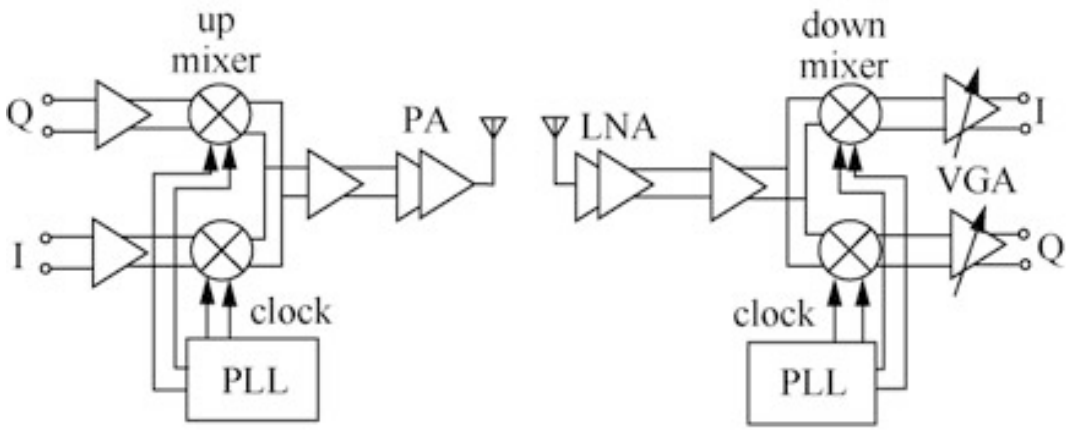

Figure 1.12: Direct-conversion architecture.

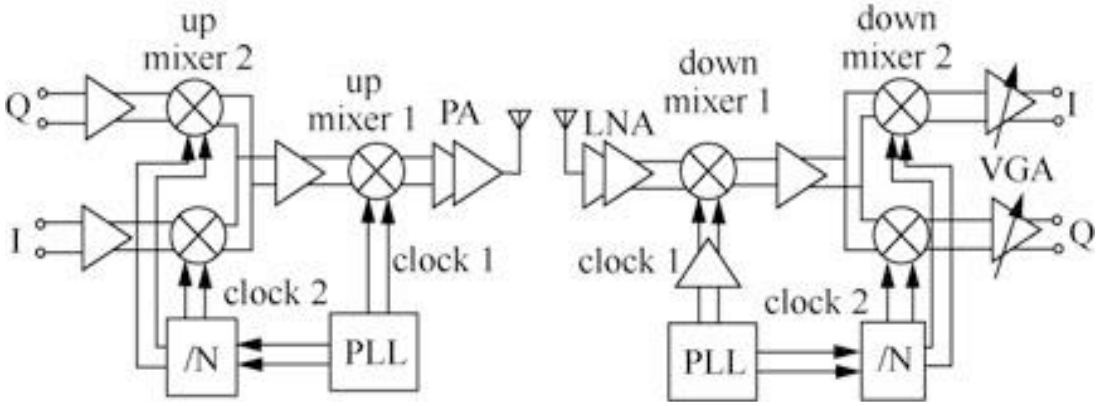

Figure 1.13: Dual-conversion architecture.

As shown in Figure 1.12 and Figure 1.13, for mm-Wave communication, there are two typical transceiver architectures, namely direct conversion and dual conversion [65, 75, and 76]. Both of these have their advantages and disadvantages. Direct conversion, which is popular in GHz RF radio, can achieve compact and low power implementation, as well as operation flexibilities. However, for mm-Wave application, its high-frequency quadrature modulation/demodulation typically gives rise to severe distortion, such as I/Q imbalance and LO feedthrough. Moreover, the indispensable quadrature PLL (Phase-Locked Loop) has introduced several implementation issues. These are the trade-off between the phase noise, tuning range, and phase error, as well as the frequency pulling/pushing caused by the power amplifier [76].

An alternative solution is to use the dual-conversion architecture (also referred to as sliding-IF), as shown in Figure 1.13. In this architecture, the quadrature modulation and demodulation working frequency is significantly reduced. Moreover, the tuning range and operating frequency of the LO are reduced, simplifying the system design. Therefore, the sliding-IF architecture is very popular in mm-Wave systems [75-79].

1.6.4 Massive MIMO and Beamfroming

Combined with the beamforming technique, based on the above transceiver architecture, we can realize the phased-array system, thus achieving beam scanning capability, which is good for LOS and NLOS communication scenarios. With the above features, mm-Wave wireless access and wireless backhaul can be simultaneously supported, increasing the system flexibility [2-4]. Moreover, with a large-scale antenna array, we can realize a large antenna array gain, compensating the large path loss associated with high frequency and increasing the coverage Accordingly, we can establish a stable wireless link.

To be more specific, from an implementation perspective, mm-Wave can achieve a high directivity using a large array antenna, and the actual power that is required to deliver a certain EIRP (Equivalent Isotropic Radiated Power) is significantly reduced. Accordingly, the requirements on each RF frontend component, such as the antenna gain and PA output power, can be relaxed, thereby increasing the system energy efficiency. On the other hand, we can achieve a small beam, increasing the signal spatial isolation and simultaneously accommodating many co-channel users. In other words, a kind of spatial filtering on the co-channel signal is achieved, and the spectrum efficiency can be improved. Combined with the mm-Wave large path loss feature, the interference can be relaxed and the frequency can be reused by using small-cell techniques, as well as increasing the spectrum efficiency and communication capacity.

These characteristics make mm-Wave communication very attractive for ultra-dense networks with a range of 10~200 m. It should be noted that because of the small beam, large-array systems are very sensitive to channel amplitude and phase mismatch in terms of aging, environment variation, and fabrication tolerance. To maintain a stable wireless link, macro assistant small cells, beam tracking, and channel calibration techniques are essential.

In 4G LTE (Long-Term Evolution) MIMO systems, each antenna has its own transmitter and receiver chain. Doing so in mm-Wave systems will cause the power consumption to be too large as the number of antennas exceeds 100. To deal with these issues, the hybrid beamforming architecture can be used, as shown in Figure 1.14. In this architecture, RF-path beamforming is selected. It should be noted that with respect to the MIMO and beamforming operation, TDD (Time-Division Duplexing) is a good alternative to FDD (Frequency-Division Duplexing) because of the ability to leverage uplink/downlink reciprocity.

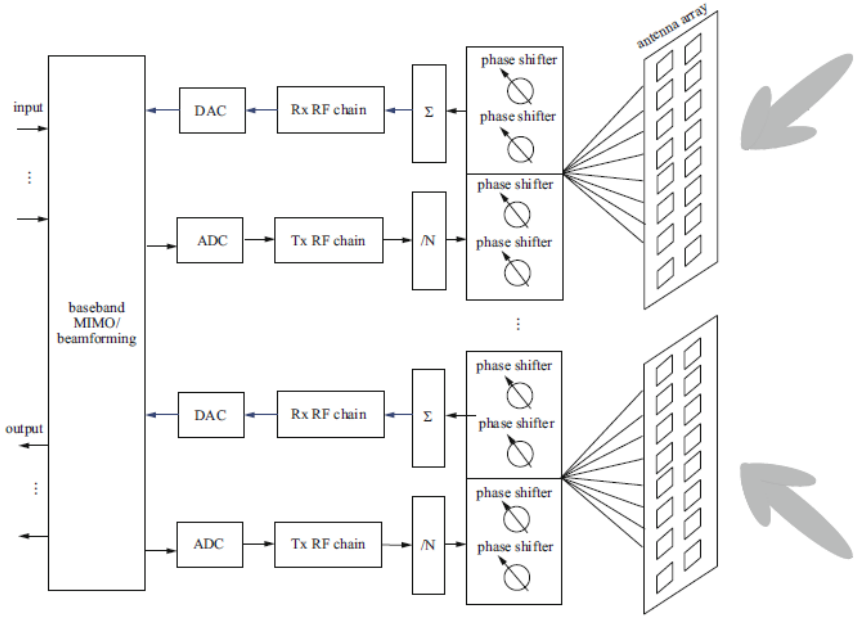

Figure 1.14: Hybrid RF/baseband MIMO architecture

Chapter 2 : mmWave Transmitters

2.1 Introduction

This chapter will focus on the architectures used to implement mm-Wave transmitter, these architectures will be discussed with respect to three important criteria: the potential to fully integrate the device on a single CMOS substrate, the ability to achieve the high performance that is necessary in modern wireless communications and the ability to operate with multiple wideband standards. The radio standards may employ different types of modulation and varying bandwidth, require a flexible architecture.

2.2 Transmitter Architecture

2.2.1 Direct Conversion Architecture

The direct-conversion architecture, shown in Figure 2.1, is interesting because of the straightforward and simplicity of the signal path. After the conversion of digital baseband Quadrature signals into analog signals with two DACs, then filtering to attenuate the aliasing from the DAC happens. The signals are then modulated and up-converted to RF in a one step by the quadrature mixer. The RF signal then passes through a discrete filter before amplification by the power amplifier. This pre-PA filter is not always necessary and is used to reduce intermodulation in the PA and to attenuate wide-band noise. Finally, after the PA, may include a discrete bandpass filter to meet the spectral mask requirements. Only a single RF frequency synthesizer performs channel selection.

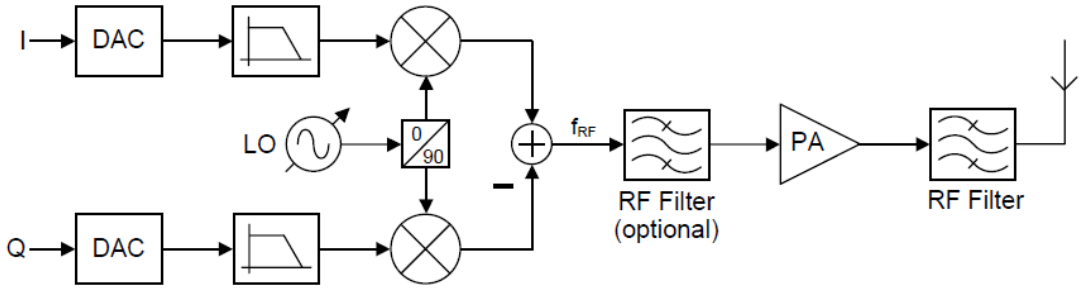

Figure 2.1: Direct-conversion transmitter block diagram.

Performance of a direct-conversion transmitter is typically limited by three factors. First, like all quadrature modulators, direct-conversion architecture requires the quadrature LO signals generation at high frequencies. Quadrature generation at RF is less definite than at lower frequencies. Therefore, the modulation accuracy of the transmitter is limited by this effect.

The other constraint to the performance of the transmitter comprises intermodulation in the PA. Whenever the baseband signals are mixed up with the LO signal, harmonics of the LO are created. These harmonics, are inherent to switching mixers. The harmonics create intermodulation of the baseband signal which latter on inter modulate in the PA and reduce the modulation accuracy and may exceed the spectrum mask.

A different potential problem for direct-conversion architecture associate interaction between different circuit blocks. If the objective is an entirely integrated transmitter, high output power signals will be present at the output of the PA. These large signals will interfere with sensitive sub-circuits especially analog circuits by coupling through the substrate or common nodes. Precisely, mostly problem occurs between the frequency synthesizer and the PA. As shown in Figure 2.2 this effect, is called injection pulling or LO pulling [80] because the high power signal from the PA output can pull and shift the LO frequency. This is a particular problem for direct-conversion transmitters because the frequency of the RF output and the LO are so close together.

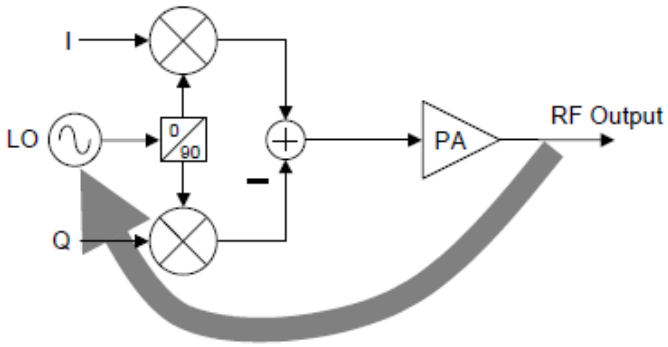

Figure 2.2: LO Pulling in a direct-conversion transmitter.

Another possible issue with direct conversion transmitters include the struggle with power control and LO feedthrough. Because of lack of IF stage, the power control must perform at baseband or RF. Baseband power control puts rigid linearity requirements on the baseband circuits. Coupling between the LO signal to the output is another potential problem due to the high frequency of the LO signal used in the quadrature modulator.

Although direct conversion transmitter has a very simple signal path and offers potential for multi-standard operation, a number of limitations associated with the architecture exist. Some of these problems can be alleviated by using circuit techniques and some could be tolerated.

2.2.2 Heterodyne Architecture

The heterodyne architecture, which uses two steps to perform up-conversion, is also a widely used topology specially in the past. This architecture, illustrated in Figure 2.3 uses a quadrature modulator to frequency translate the baseband signal to IF. An IF filter is needed to suppress harmonics created in the mixer output, IF signal then up-converted to RF. Finally, the RF signal is applied to the PA and typically filtered again to meet the spectral mask requirements.

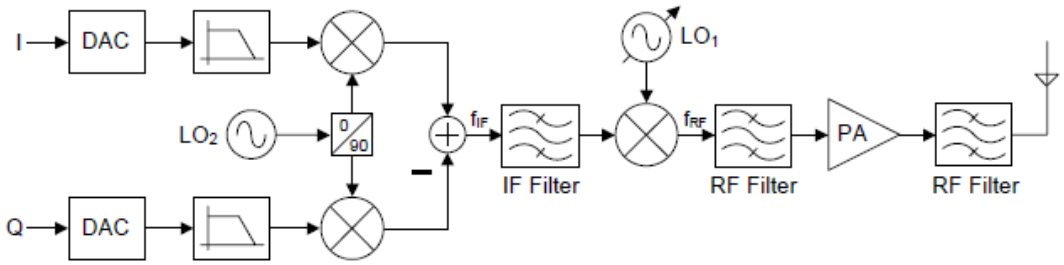

Figure 2.3: Conventional two-step or heterodyne transmitter block diagram.

The heterodyne architecture has some advantages, it avoids the LO pulling problem because up-conversion is performed in two steps and therefore neither LO is operating at the transmitted frequency. Modulation accuracy in the quadrature LO generation circuit is also improved because the lower frequency LO allows for more accurate quadrature generation. Moreover, low frequency LO signal results in less LO feedthrough at the output. The issue of third order intermodulation is also eased because the spur located $3(LO_1+LO_2)$ is attenuated by the IF filter. Although the heterodyne architecture shows promise for higher performance, the architecture has drawbacks with respect to single chip integration.

To achieve the performance benefits previously mentioned two filters are needed before the PA. IF filter is needed to attenuate harmonics created in the quadrature modulator and RF filter before the PA is needed to filter the image created by the second up-conversion. Both filters are generally discrete components that are not amenable to integration on CMOS substrate. The increased power consumption of the overall structure is another disadvantage.

The direct conversion architecture is appealing for integrated RF frontends that need to provide high data rate capabilities at low power consumption and cost. Furthermore, it is not limited to a specific modulation scheme. Nevertheless, its design provides some specific challenges that will be discus in next sections.

2.3 Transmitters Non-idealities

Along with reaching a certain power level, the signal transmitted by the TX must satisfy some other requirements. (These requirements are usually specified by a certain wireless standard, such as IEEE 802.11ad or IEEE standard 802.15.3c.) First, to guarantee the transmitted signal quality, the "error vector magnitude" (EVM) is specified, which is defined as the rms magnitude of error vectors (i.e., the deviation of the constellation points from their ideal positions) normalized to the signal rms voltage. Second, the TX "spectral mask" is defined to ensure the out-of-channel emissions remain sufficiently small. Figure 2.4 shows a typical transmitted signal constellation and spectrum with 16-QAM modulation. While the spectral mask requirement is mainly violated due to the TX nonlinearity, the EVM depends on a couple of other TX non-idealities [81, 82] that will be covered in this section.

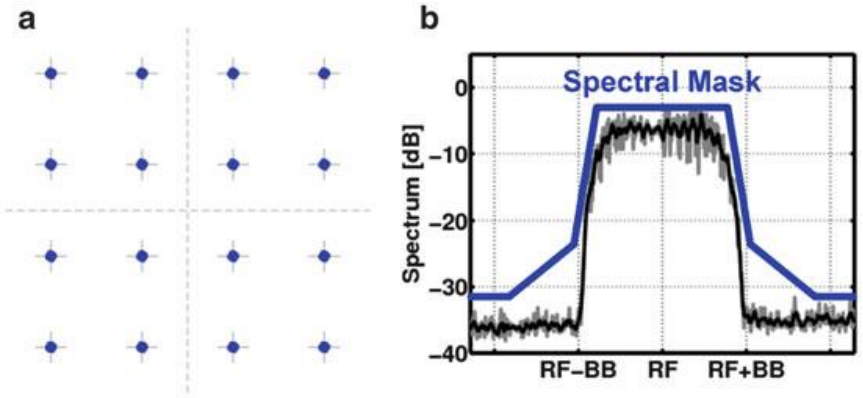

Figure 2.4: Typical Transmitter (a) Constellation (b) Spectrum

2.3.1 Linearity

The linearity sets the upper limit of the system dynamic range. Various measures have been defined to quantify the nonlinear effect, including gain compression and intermodulation distortion. The signal constellation and EVM are mainly limited by the gain compression. Under large signal level, both the amplitude and phase of the signal will be distorted and thus deteriorate the EVM

(referred as AM-AM and AM-PM distortions). The violation of the requirement for spectrum mask is usually owing to intermodulation distortions (e.g., third-order or fifth-order intermodulations). The signal power in the adjacent channel is increased as a result of spectral regrowth. In wireless standards, the adjacent channel leakage ratio (ACLR) [83] is normally specified for this purpose. In Figure 2.5a, it can be seen that four outmost points get close to the center due to the gain compression. In Figure 2.5b, the TX spectrum out of the signal band is raised due to the third-order and fifth-order intermodulations. Note that it is usually difficult to evaluate if the spectral mask or ACLR requirements are satisfied in a circuit-level simulator. Instead, a two-tone test can be performed to simulate the intermodulation distortions [81].

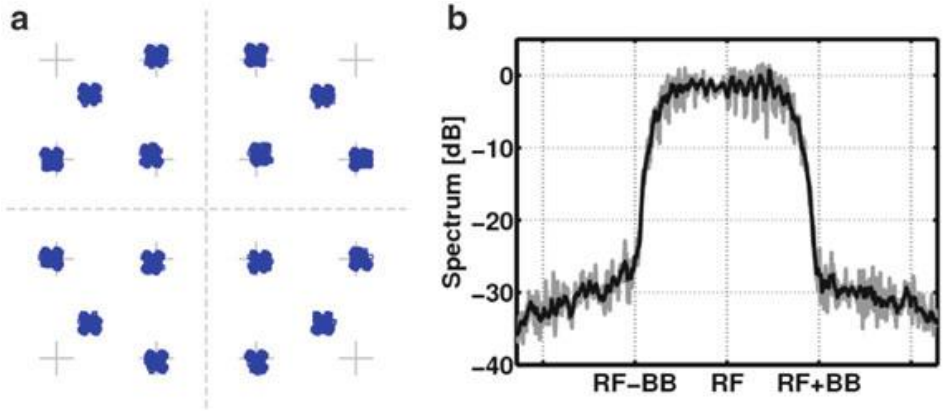

Figure 2.5: Influence of nonlinearity on the (a) constellation and (b) spectrum

2.3.2 Phase Noise

An oscillator with low phase noise is important to Gb/s complex digital modulations. The work in [84,85] shows that the phase noise should be lower than -90 dBc/Hz at 1-MHz offset frequency for 16-QAM to avoid serious package error rate degradation in i.e. 60-GHz radio. For the phase-modulated signals, the constellation will be corrupted by the phase noise (see Figure 2.6a) as you cannot distinguish the phase noise with the actual phase modulation. In addition, as shown in Figure 2.6b, a strong transmitted signal at f_1 with the phase

noise skirt may mask the weak signal in the adjacent channel at f_2. As a result, the signal at f_2 might not be correctly detected.

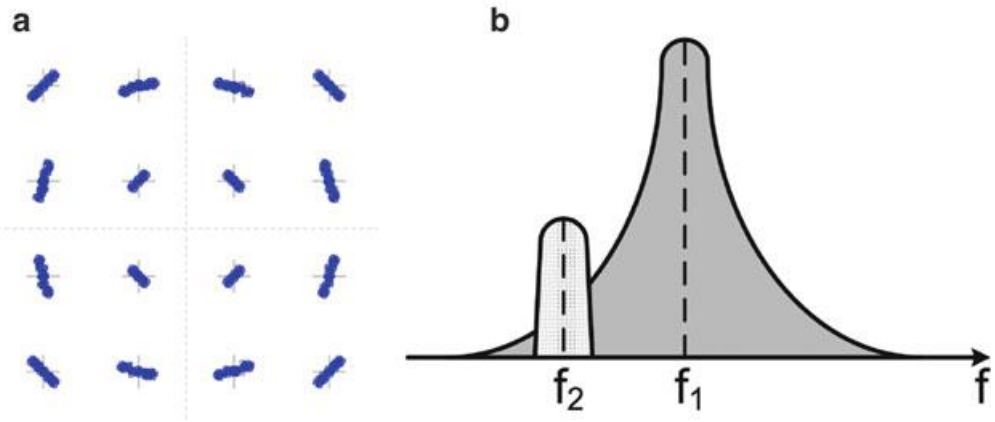

Figure 2.6: Influence of phase noise on the (a) constellation and (b) adjacent channel

2.3.3 LO Leakage

The effect of LO leakage (also known as carrier feedthrough) shifts the signal constellation in both horizontal and vertical directions by certain offsets, and appears on top of the transmitted spectrum. The LO leakage is mainly caused by dc offsets existing in the analog baseband circuits as a result of the component mismatches. It is usually not a problem when the signal power is sufficiently high. However, when the transmitter and receiver is close, the signal power has to be reduced in order not to saturate the receiver input stage. In such scenario, the signal power may not be accurately measured in the presence of LO leakage. Therefore, the LO leakage also determines the minimum power level and affects the dynamic range of the system, which has to be maintained below the noise floor in the TX design.

2.3.4 I/Q Amplitude and Phase Imbalances

Quadrature amplitude modulation (QAM) is widely used in modern wireless transceivers. Any amplitude or phase mismatch in the baseband and LO paths will directly affect the construction of QAM signals. As shown in Figure 2.7, the gain mismatch between I and Q paths will compress the

constellation in either vertical or horizontal way, and the phase mismatch will rotate the signal constellation. The work in [82] analyzes the influence of gain/phase imbalance and phase noise on the EVM in a mathematical way. At mm-Wave, transistors with minimum channel-length have to be used for high speed. As a result, the matching between devices becomes worse, which makes the LO leakage and I/Q imbalance more problematic. In next part, the influence and the cause of LO leakage and I/Q imbalance will be discussed in detail.

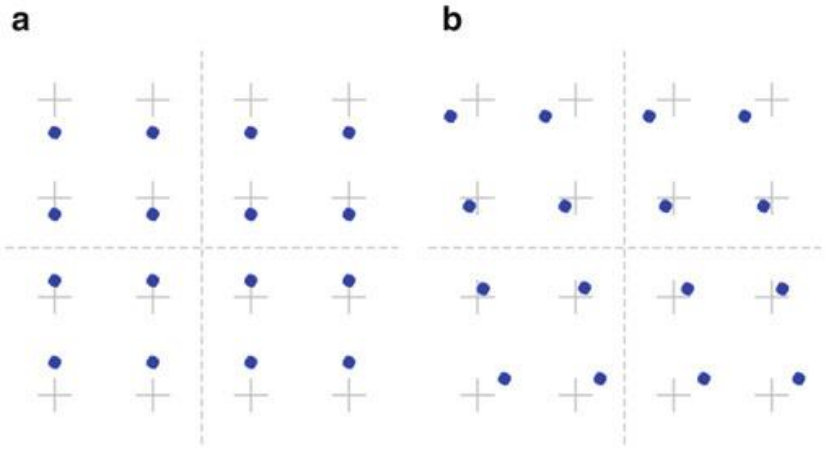

Figure 2.7: Influence of I/Q imbalances on the constellation diagrams. (**a**) Gain imbalance (**b**) phase imbalance

2.3.5 Noise

System performance is mainly limited by the noise. At TX side, it determines the dynamic range at the lower end. The signal power should be larger than the noise power with a certain margin to ensure a reliable

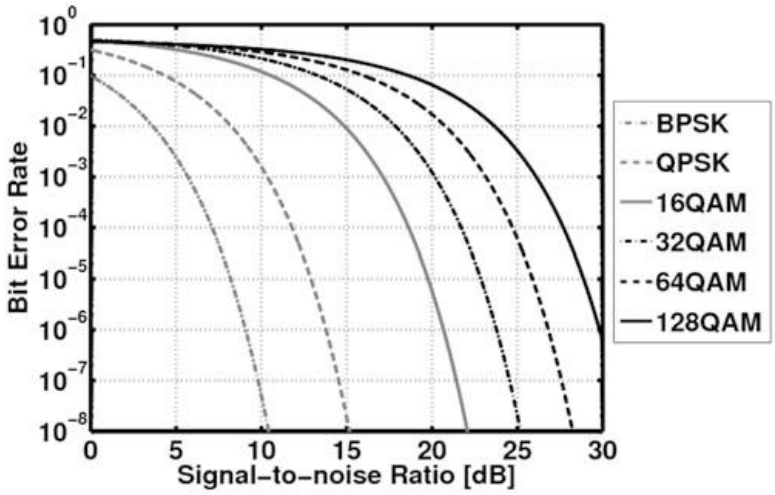

Figure 2.8: Bit error rate versus signal-to-noise ratio for different modulation schemes

link, which is defined by the signal-to- noise ratio (SNR). The wireless standard usually specifies the maximum bit error rate (BER) allowed in a system. Figure 2.8 plots the relationship between BER and SNR for different modulation schemes. The TX EVM can also be easily calculated according to [86]:

$$EVM \approx \sqrt{\frac{1}{SNR}} \tag{2.1}$$

For a certain BER, SNR and EVM requirements are tighter for a complex modulation. This is understandable as the allowed error vector is smaller, assuming the system has the same dynamic range. When the signal power is relatively low, a “cloud” forms around each point in the constellation and the signal spectrum gets close to the noise floor.

2.3.6 EVM

The error vector magnitude (EVM), is a measure used to quantify the performance of a transmitters or receivers. A signal sent by an ideal transmitter or received by a receiver would have all constellation points precisely at the ideal locations, however various imperfections in the implementation. cause the

actual constellation points to deviate from the ideal locations. EVM is a measure of how far the points are from the ideal locations. The relationship between TX EVM and other TX impairments can be expressed as [87]

$$EVM \approx \sqrt{EVM_{LOFT}^2 + EVM_{IQ}^2 + EVM_{GF}^2} \tag{2.2}$$

Where EVM_{LOFT}, EVM_{IQ} and EVM_{GF} represent the EVM degradation due to LO feed-through, I/Q imbalance, and gain flatness, respectively. The LOFT and I/Q imbalance in low-GHz TXs are mainly caused by device mismatches, which can be mitigated by sizing up the device or using common-centroid layout scheme [88]. At mm-Wave, the device mismatch has a more detrimental impact as transistors with minimum channel-length have to be used for fast speed. In addition, a common-centroid layout scheme is generally not used at mm-Wave as mismatches between interconnects play an equally important role as device mismatches. The requirements, already stringent for high-order modulations, become further challenging when considering channel bonding [89].

Techniques proposed in the literature include architectures using digital calibration. The drawback is represented by power-hungry baseband (BB) ADCs for sufficient image suppression [90]. Furthermore, continuous calibration to ensure performance over a wide temperature range is desirable. Therefore, PVT-tolerant I/Q calibration schemes such as [91] and [92] have been proposed. However, data transmission must be interrupted to allow for intermittent calibration tracking voltage and temperature variations. In this scenario, advances in circuit-level techniques to produce precise I/Q signals are key to reduce the calibration macro requirements [93]. For the mm-wave target frequency range, solutions leveraging single-phase VCOs followed by quadrature generators prove to be the best strategy. Still, the challenging phase noise required to support higher order modulations trading with tuning range mandates at least two VCOs covering half bandwidth each. For quadrature

generation, distributed couplers, e.g. Lange Couplers, are bulky and not amenable to integration. Hybrid couplers based on coupled inductors offer a compact footprint with low loss, but they are disregarded because a few percentage variation of coupling coefficient k leads to unacceptable amplitude deviations. Polyphase Filters (PPF) and their evolutions are widely adopted at RF [94]. In [95], PPF operation at mm-waves is proven through careful layout techniques. Still, wideband operation can be achieved only cascading several stages, severely increasing signal loss and power consumption.

Chapter 3: mm-Wave Quadrature LO Generation

This chapter deals with the design of the Quadrature LO building blocks in the BiCMOS 55nm technology. After a brief overview of the technology features, design choices for the PPF, inter-stage matching networks, LO buffers and phase detection/feedback loop are discussed. Finally, an overview and measurement results of the test chis is provided.

3.1 Technology Overview

All the test chips were designed and fabricated in a 55nm BiCMOS technology provided by STMicroelectronics. The technology cross section is shown in Figure 3.1. The Front End of the Line (FEOL) features both carrier-class 55nm CMOS FETs and epitaxially-grown high-speed SiGe npn heterojunction bipolar transistors(HBT). CMOS transistors come in three flavors: general purpose (GP), with1V supply, low power (LP), with 1.2V VDD, and thick-oxide (GO2), featuring 280nm minimum channel length and supply up to 2.5 V. High-speed SiGe bipolars achieve 320GHz GBW, with 1.5V collector-emitter breakdown voltage (BVCEO). Medium voltage and high-voltage HBTs featuring higher BVCEO, at expense of lower-speed operation, are also available.

The Back End of the Line (BEOL) features 8 copper metal layers: 5 thin layers M1-M5, two thick layers M6 and M7, and an ultra-thick metal (UTM) layer M8. The 3μm thick UTM represents the main difference with respect to the 65nm CMOS BEOL stack up. An aluminum capping layer is also available on top.

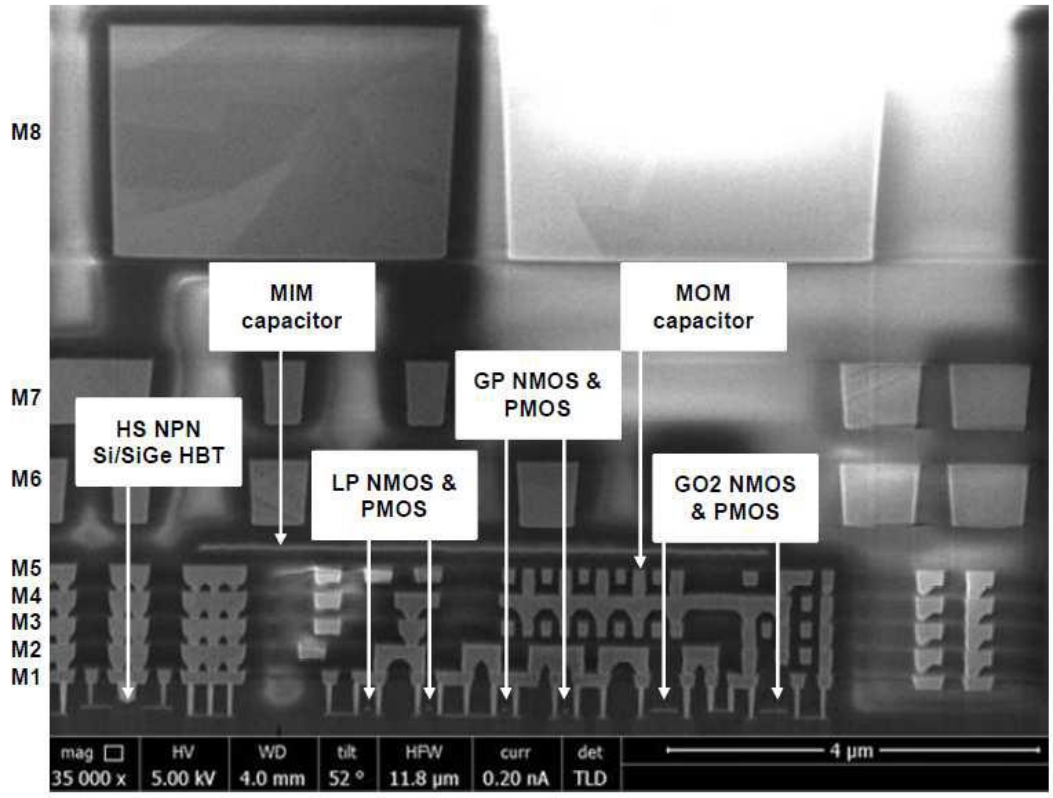

Figure 3.1: BiCMOS 55nm technology cross-section [98].

3.2 Challenges and State-of-the-Art

I/Q mismatches in signal path and LO, normally evaluated by the image rejection ration (IRR), impact the EVM performance of any communication system. The IRR can be expressed as:

$$IRR = \left| \frac{10^{\frac{\Delta A}{20}} + 2.10^{\frac{\Delta A}{20}} cos\,\Delta\theta + 1}{10^{\frac{\Delta A}{20}} - 2.10^{\frac{\Delta A}{20}} cos\,\Delta\theta + 1} \right| \tag{3.1}$$

where ΔA is the gain error in decibel and Δθ is the phase error in radians between I and Q paths [81]. As an example, when targeting 64-QAM modulation, the most critical contributions to EVM degradation are LO phase noise, LO leakage, flatness of BB to RF gain response and I/Q mismatches in signal path and LO. From [91] to achieve BER=1e-3 on 64-QAM modulation,

I/Q LO accuracy must provide IRR >35dBc, setting target to 40dB. As shown in Figure 3.2, a 40dB target corresponds to either 0.1dB amplitude mismatch and less than 1° phase error, or 1° phase error if only phase mismatch is considered, which is challenging considering it has to be ensured over all the operation bandwidth and PVT variations.

Figure 3.3 shows the typical block diagram of a wireless transmitter, where quadrature paths are shown along with calibration circuits. Two conceptually different but not mutually exclusive approaches are possible to minimize I/Q paths errors: digital calibration techniques and precise I/Q LO generation circuits. In this section we provide an overview of the state-of-the-art of the above, showing pro and cons for each one.

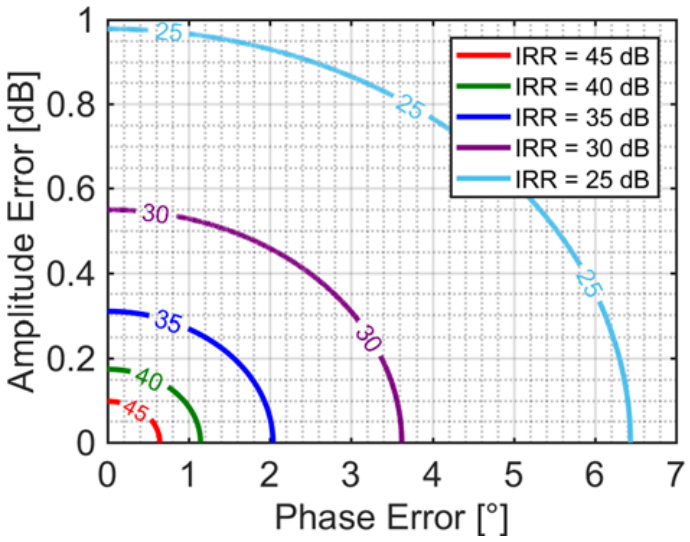

Figure 3.2: Image Rejection Ratio (IRR) contour plot

Well-established methods to perform calibration use an ADC and FFT logic to process the signal, coupling a small fraction of TX power through a dedicated detector. An ADC used for I/Q demodulation is usually re-used for calibration, whereas millimeter wave transceivers employ ADCs in the receiver paths that are not accurate enough. In fact, more than 9b ADC is required to achieve an image suppression of 50dB [92]. However, 5-to-7b ADC is usually employed for millimeter-wave transceivers due to power saving, which is not

enough to perform the calibration when modulations equal or higher than 64QAM are targeted.

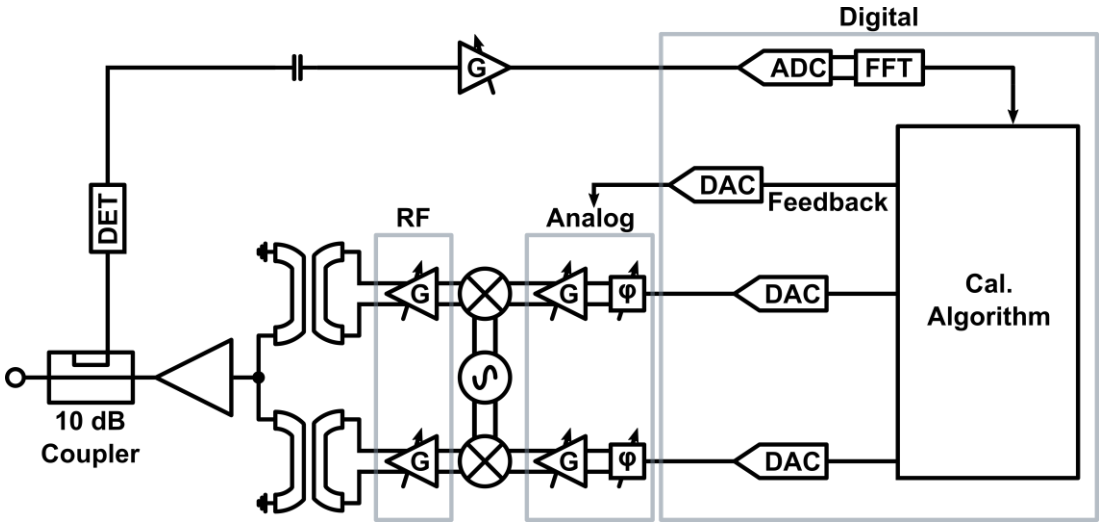

Figure 3.3: Block diagram of a wireless transmitter, where I/Q generation and calibration circuits are highlighted.

A simple and elegant solution is proposed by Pang et al in [96], where a quadrature mixer is employed to down-convert image signal to DC. Therefore, low sampling rate but high resolution dedicated ADCs can be used for accurate calibration with low power consumption. The digital macro performs the calibration by acting on variable-gain amplifiers on signal path and phase shifters on the LO This technique can simultaneously compensate LO and signal-path I/Q errors at the center of each channel frequency, but it is less effective under voltage and, mostly, temperature variations, because the block generating I/Q signals often has temperature-sensitive circuits parameters [91]. This is a serious issue, and [91] reports a I/Q phase error raising to 5° degrees (which corresponds to an IRR reduced to 29 dB only) when the temperature is swept from -40° to 85° after the system is calibrated at room temperature for 0° I/Q phase error. A slightly different implementation aiming to a PVT-tolerant digital calibration system is presented in [96,102], where baseband must transmit a continuous-wave (CW) sinusoid to perform calibration, thus regularly interrupting the transceiver normal operation and reducing the capacity of the link accordingly.

3.3 I/Q Signals Generation Techniques

Among the LO quadrature generation circuits, VCOs at twice the operation frequency (i.e. 56-78GHz) in combination with a divide-by-two circuit would naturally yield quadrature signals at output [103]. However stringent 5G phase noise requirements [104] suggest designing VCOs at lower frequencies, where passive quality factor is higher [105,106]. Quadrature-coupled VCOs (QVCOs) are a suitable alternative shown in Figure 3.4. However, they show a strong trade-off between phase noise and phase accuracy, especially if wide tuning ranges are involved, not lending themselves to applications where a large fractional bandwidth is required [94,107].

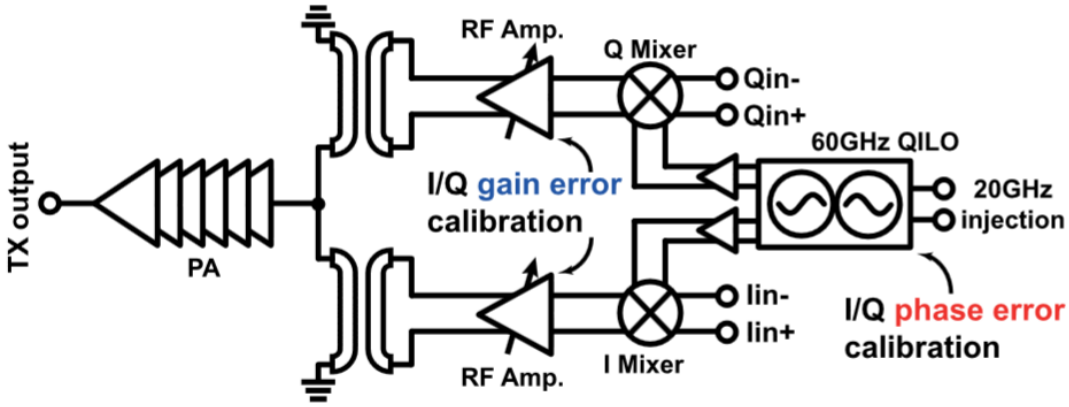

Figure 3.4: Block diagram of a wireless transmitter, where I/Q generation and calibration circuits employes Quadrature ILVCO.

In the work presented by [108, 109], a LO signal generated by a 20GHz PLL is fed to a PPF filter and injected into a 60GHz quadrature injection-locked oscillator (QILO). The free running frequency of the QILO is calibrated to be exactly 3x20GHz to reduce the I/Q phase imbalance. But still calibration is sensitive to PVT variations [91].

Lange Couplers have also been employed in several works for I/Q generation Figure 3.5. As an example, state-of-the-art implementation in [110] shows 2° phase error over a fractional bandwidth of 37%. However, given the

required λ/4 transmission lines, the whole structure, at 30GHz, is very cumbersome and with no mean of tuning for calibration.

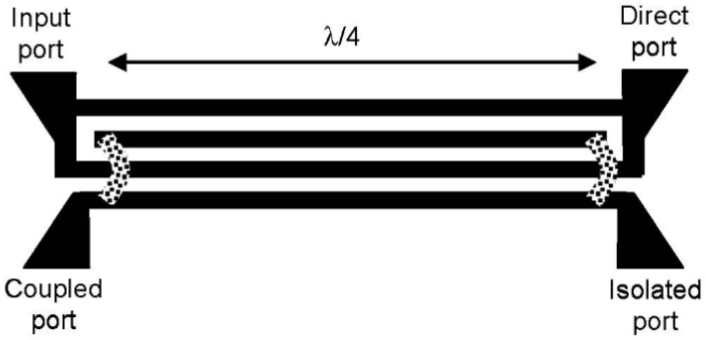

Figure 3.5: Structure of unfolded Lange coupler.

The hybrid coupler, its lumped-element counterpart, gained a lot of attention over the last years because of its small form factor (i.e. more than 10x smaller) and simple design Figure 3.6 [111, 112]. However, to minimize I/Q phase and amplitude error, the design of the transformer itself is critical, especially in presence of parasitic capacitors [113]. The required coupling coefficient is k=0.707, which is hard to realize in advanced CMOS process. Moreover, the IRR of the hybrid coupler heavily depends on the value of k. As an example, if a 35GHz hybrid coupler is designed with ideal elements, IRR is infinite at center frequency. If coupling coefficient shifts from k=0.707 to k=0.705 or k=0.708 (which is 0.28% variation, only), the IRR already drops to <40dB mainly because of the amplitude error, which is too hight to be rejected by the upconversion mixer.

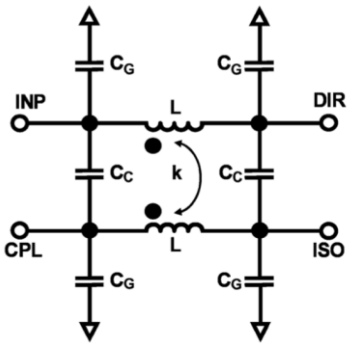

Figure 3.6: Structure of hybrid coupler. [111, 112]

A noteworthy evolution is presented by Park et al. in [100]. Here, a 3-stage poly-phase network is built on an evolution of the hybrid coupler demonstrating IRR>40dB over 82% fractional bandwidth from ~5GHz to 12GHz. Nonetheless, coupling coefficient k is as high as 0.82, which can be difficult to realize, especially when transformers must be surrounded by ground shield to have consistent and reproducible performances in mass production [114].

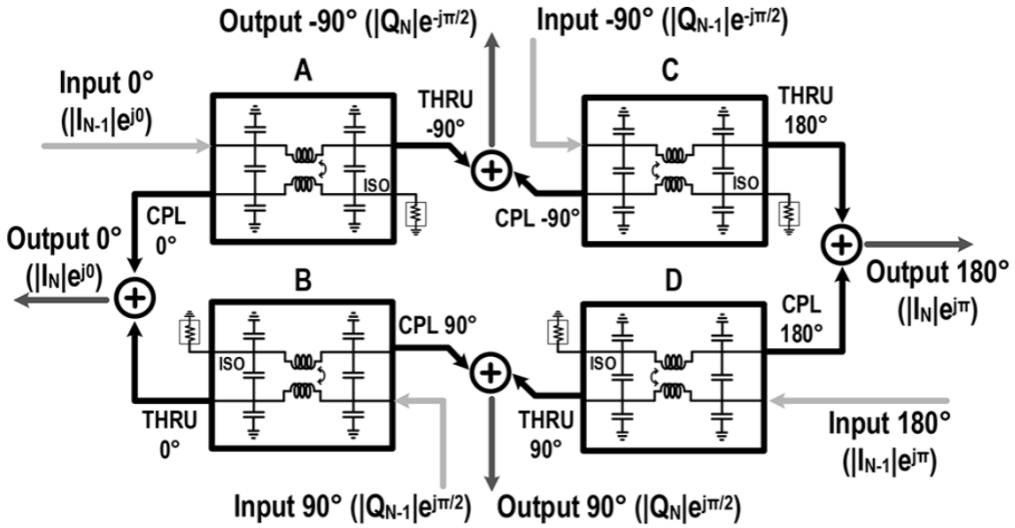

Figure 3.7: Structure of multi-stage hybrid coupler [96].

Wideband operation can be achieved even at mm-waves with careful and elegant layout using PPF and cascading several stages [93], however increasing signal loss and power consumption [115]. As an example, a 3-stage PPF was designed with 36GHz center frequency and with pole splitting factor equal to 1.84 and 3.4. The design achieves a IRR>40dB over a remarkable 94% bandwidth. However, as shown in Figure 3.8, when PVT variations are considered, IRR>40dB can be achieved on a ~11% fractional bandwidth only. Simulations show that in order to cover ~50% fractional bandwidth with 40dB IRR, at least 5 stages are required but signals are attenuated at least by 12dB, requiring power hungry inter-stage amplifiers.

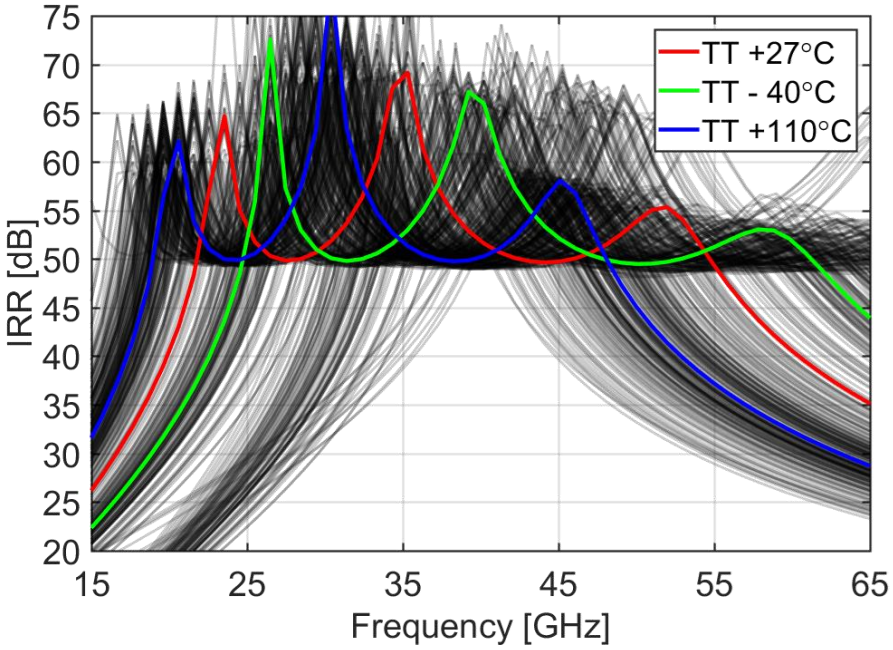

Figure 3.8: IRR Montecarlo simulation of a 3-stages polyphase filter with pole splitting for different temperatures.

To address this problem, quadrature all-pass networks (QAF) are a good alternative shown in Figure 3.9 [116]. Without any loading at their outputs, QAF has the same performance of a two-stage PPF filter, but with 6dB more gain. When loaded with parasitic capacitance of the cascaded stage, the consequent increase of I/Q mismatches can be mitigated by an additional resistor, at the expense of increased signal loss though [117].

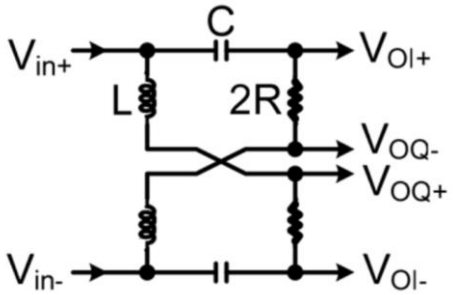

Figure 3.9: Differentail Quadrature All-pass filter(QAF) [116].

This work approaches the problem from a different perspective. Instead of looking for wide-bandwidth solutions, where lowering I/Q mismatches intrinsically trade with higher insertion loss, we propose the use of an

intrinsically narrow-bandwidth element, while continuously tuning its center frequency to cover a wide bandwidth, as discussed in detail in the next section.

3.4 Tunable Polyphase Filter

Figure 3.10 shows the block diagram of the proposed wideband quadrature LO generation architecture. A single-stage type-a PPF [118] is used to ensure zero amplitude imbalances at any frequency, and zero phase error at the center frequency only. Resistive elements are realized through four NMOS transistors biased in triode. The phase detector continuously senses the quadrature accuracy, amplifies the error, and drives all four gates of the NMOS transistors with the same voltage signal. In this way, the center frequency of the PPF is always tuned to the input LO frequency, ensuring minimum quadrature error.

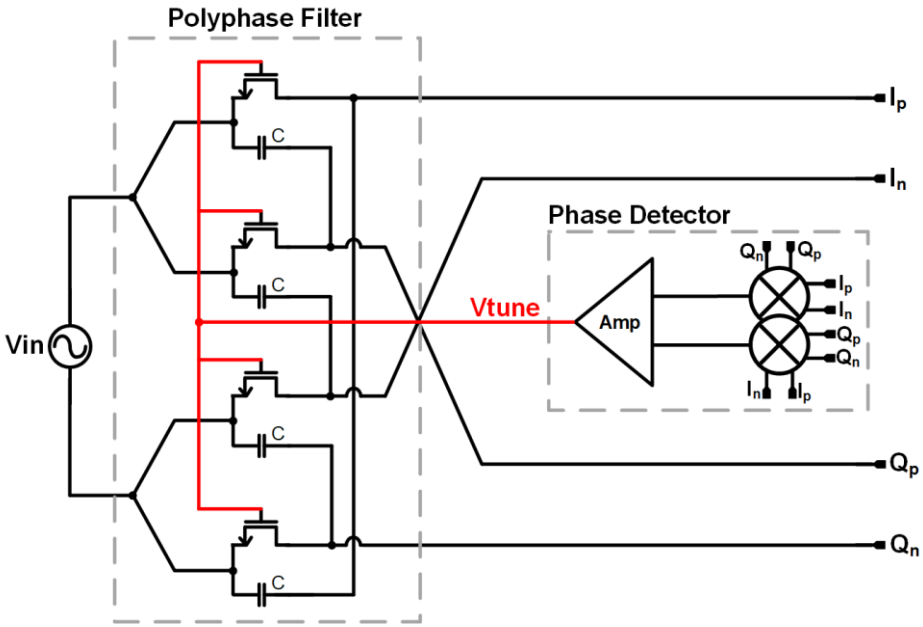

Figure 3.10: Block diagram of the proposed quadrature generator.

An example of the working principle is in Figure 3.11, where IRR is reported for three different input frequencies. If the input frequency is $f_{in,2}$=36GHz, the loop control voltage settles to V_{tune}=$V_{tune,2}$ and IRR is maximized at $f_{in,2}$. If the input frequency is higher, say $f_{in,3}$=42GHz, then the loop settles to V_{tune}=$V_{tune,3}$ and IRR is again maximized at the input frequency.

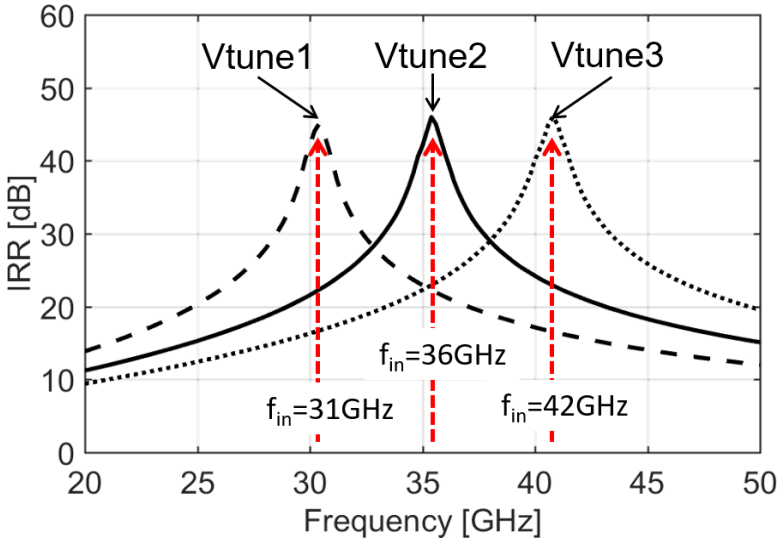

Figure 3.11: Block diagram of the proposed quadrature generator.

Figure 3.12 shows the complete schematic of the implemented test chip. A buffer is employed at the input for single-ended to differential conversion. Wideband inter-stage networks are leveraged at the input and output of the PPF to extend the operation bandwidth. At the output of the PPF, buffers in I and Q paths drive both the phase detector and the mixer, which is employed to up-convert a baseband signal provided from outside the chip and IRR measurement. All buffers are current-biased common-source stages with cross-coupled neutralization capacitances to enhance gain and stability without sacrificing PSRR. Stability of the system was checked by injection common-mode and differential-mode pulses at the input of each active/passive block- on top of large-signal and small-signal stability simulations.

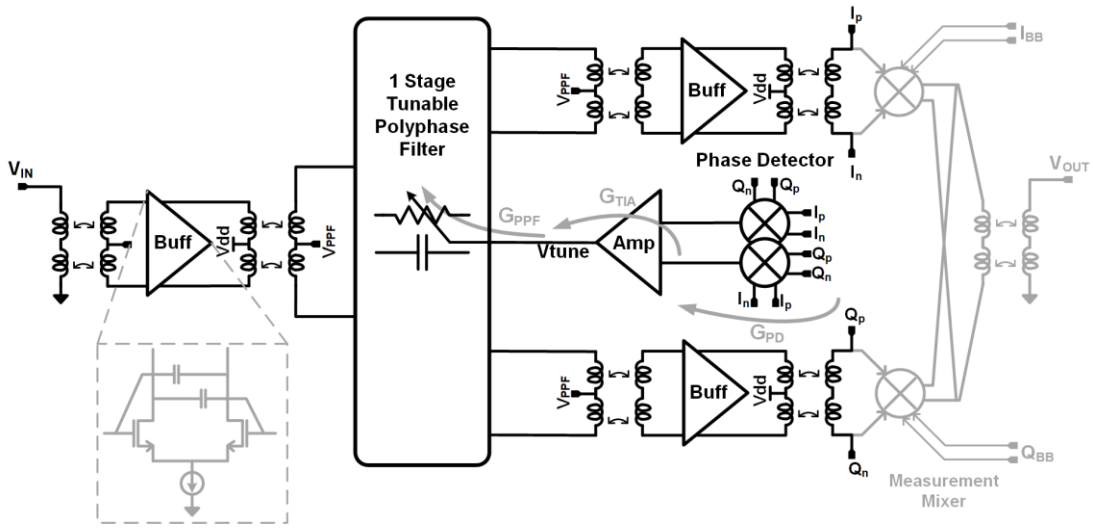

Figure 3.12: Schematic of the proposed quadrature generator.

Depending on the input feed, two types of PPF can be selected, as depicted in Figure 3.13: in type-a, quadrature phases are guaranteed only at center frequency ($H(s)=\frac{1}{sRC}$, $\omega_c=1/RC$) while amplitude imbalance is zero at any frequency [115]. Type-b is the opposite ($H(s)=\frac{1-sRC}{1+sRC}$, $\omega_c=1/RC$) [115]. Amplitude imbalance, as it will be shown later, is greatly suppressed by the mixer when driven with a large swing, while phase imbalance is not. For this reason, type-a PPF is employed. The PPF is designed such that the center frequency is f_c=33.5GHz when V_{tune}=Vdd/2. In this point, the quadrature phase error at its output is zero. At the edges of the bandwidth of interest (i.e. 28GHz-to-39GHz), the phase error in open loop θ_{ol} is about 10°~15°.

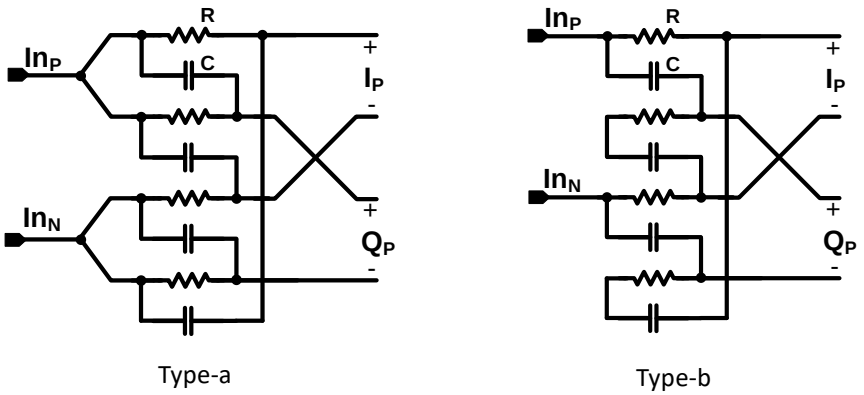

Figure 3.13: Schematic of a polyphase filter (a) Type-a (b) Type-b.

To provide an IRR better than 40dB the phase error must be reduced to less than 1°. To take into account for random mismatches on the PPF and phase detector, the targeted phase error in closed loop θ_{cl} is reduced to ~0.25°, requiring a loop gain $G_{loop} = (\theta_{ol}/\theta_{cl} - 1)$ of roughly 32dB as shown in equation 3.2. The voltage-to-phase-shift gain G_{PPF} of the PPF through V_{tune} is plotted as a function of frequency in Figure 3.14. Since the minimum value is ~150°/V and the phase detector gain G_{PD} is 20μA/°, the transimpedance amplifier is designed to provide a gain Z_{TIA}>82 [V/A] dB gain. The dominant pole at the output of the TIA is set in the 200kHz range to ensure stability over PVTs.

$$G_{Loop} = G_{PPF} \times G_{PD} \times G_{TIA} \tag{3.2}$$

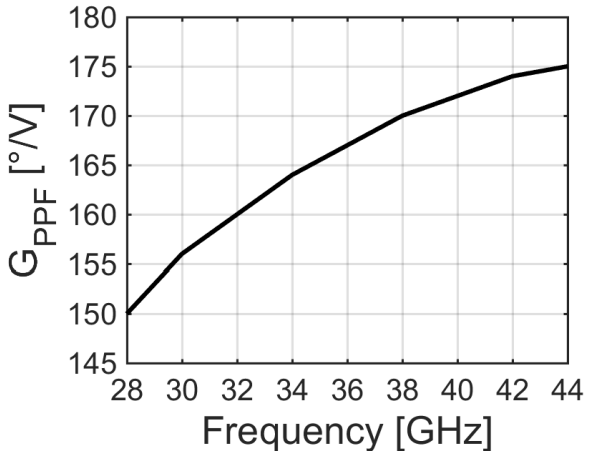

Figure 3.14: Gain of the Type-a polyphase filter over frequency.

3.5 Inter-stage Matching network design

At mm-waves, signal loss and bandwidth are the two main design concerns for PPF. A single stage is usually placed between two buffers, modeled as in Figure 3.15a, where ri, Ci, ro, Co represent the input/output impedance of the buffers, Li, Lo are inductors that may be employed to resonate out the capacitive elements, and R, C represent the resistor and capacitor of the PPF.

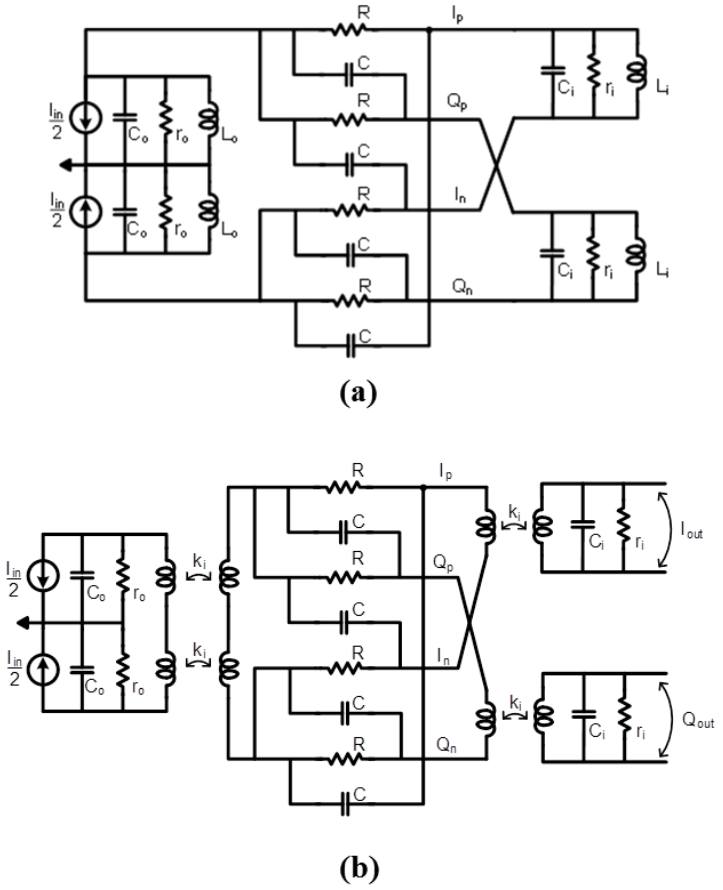

Figure 3.15: Schematic of a single-stage polyphase filter with input/output capacitances resonated out by (a) inductors (b) transformers.

The input buffer is modeled as a transconductor. With no inductors, and considering Ci,Co>0, a single-stage PPF experiences a loss at center frequency compared to the case where Ci=Co=0:

$$\left|\frac{T(j\omega_c)_{C_i,C_o>0}}{T(j\omega_c)_{C_i,C_o=0}}\right| = \frac{4}{\sqrt{\left(1+\left(1+\frac{Co}{C}\right)^2\right)\left(8+4\frac{Ci}{C}+\frac{Ci^2}{C^2}\right)}} \tag{3.3}$$

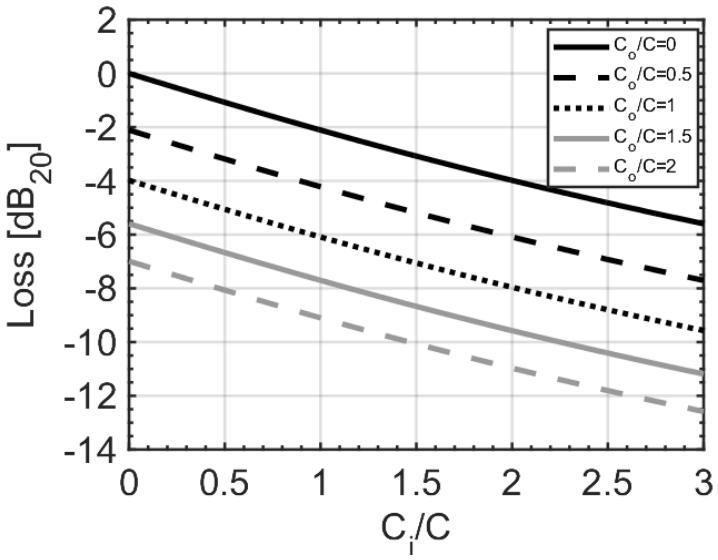

Figure 3.16: Loss of a single-stage polyphase filter as a function of the ratio of Ci/C for different values of Co/C.

where T(jω)=Vout(jω)/Iin(jω) is the transfer function from the input current Iin to the output voltage Vout=Ip-In. The calculated transfer function does not differ in amplitude if Vout=Qp-Qn, since a type-a PPF is employed. The effect of the parasitic capacitances is detrimental. The signal loss is proportional to the ratios Ci/C and Co/C, which should be therefore minimized, as highlighted by the plots in Figure 3.16. As an example, if C=Ci=Co, signal loss is already 6dB. Inductors Li and Lo can resonate out Ci+C and Co+C at center frequency. In this case, the transfer function T(jωc)=Vout/Iin is given by:

$$|T(j\omega_c)| \cong \frac{\sqrt{2}Rr_i r_o}{\sqrt{(R^2 + 4r_i r_o + 8r_i^2)(r_o^2 + (R + r_o)^2)}} \tag{3.4}$$

Interestingly, given the input/output resistance of the input/output buffers, the gain at center frequency can be maximized by setting $R = \sqrt{2r_i r_o}$ (and targeting for r_i and r_o as high as possible). Therefore, R can be selected to maximize the gain, while Ci and Co are conveniently resonated out by inductors

Li and Lo. Note that compared to using series resonance, parallel resonance yields a 33% higher gain-bandwidth product.

Second-order classic LC resonant networks are able to resonate Ci+C and Co+C, but with limited gain-bandwidth product. To meet the 40% fractional bandwidth requirement with margin, transformers can be used to couple the PPF to the input/output buffers, as depicted in Figure 3.15b. As expected, two pairs of complex poles are generated at the input and output of the PPF filter [119,120]. A higher coupling coefficient k determines a higher separation in the poles pairs, i.e. a wider bandwidth, at the expense of increased in-band ripple. The situation is depicted in Figure 3.17, where transfer function T(jω) is plotted in a normalized fashion as a function of k1=k2=k. Inductors Li and Lo were selected to resonate with Ci+C and Co+C at frequency of 36GHz, respectively. For k=0.7 ripple is limited to 1dB and bandwidth in excess of 45% is obtained. The transformers are realized with the two top thickest layers, and the quality factor at 30GHz is between 12-15, in good agreement with measurements Figure 3.18.

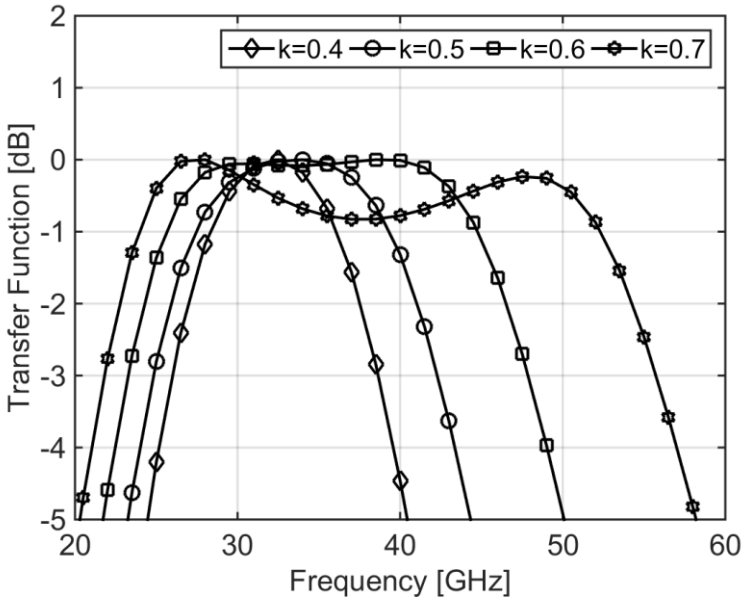

Figure 3.17: Transfer function as a function of the frequency for different k1=k2=k.

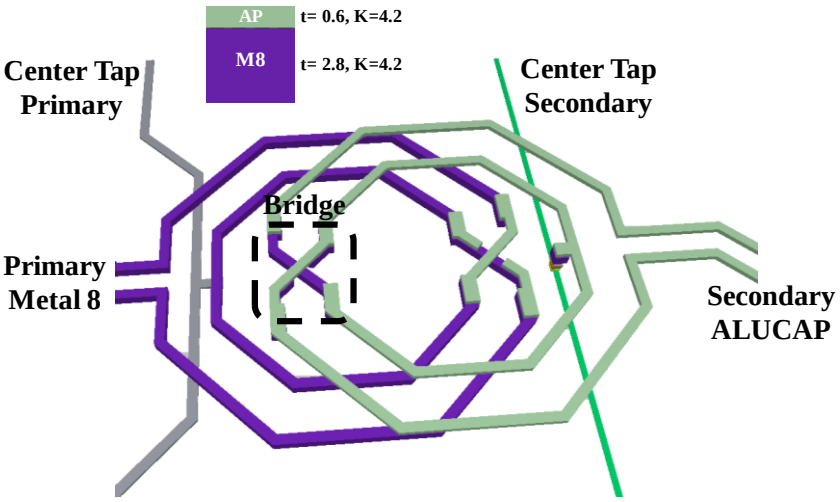

Figure 3.18: Realized transformer in top thick metal layers.

3.6 Quadrature Phase detector design

Measuring the phase difference between two signals at mm-wave frequencies is quite challenging because of the small time period and impact of parasitics. To circumvent this problem, phase difference is therefore converted to a voltage with the aim of an analog multiplier, i.e. a Gilbert cell. The injection of two sinusoids at the same frequency, with the same amplitude V but a phase difference θ, generates, after mixing and low-pass filtering, a DC output term given by:

$$V_{PD} = \alpha \, g_{mix} \, Z_{TIA} \, cos\theta \tag{3.5}$$

where α is the harmonic conversion coefficient, g_{mix} is the transconductance of transistors M1-M4 of Figure 3.19 and Z_{TIA} is the TIA transimpedance.

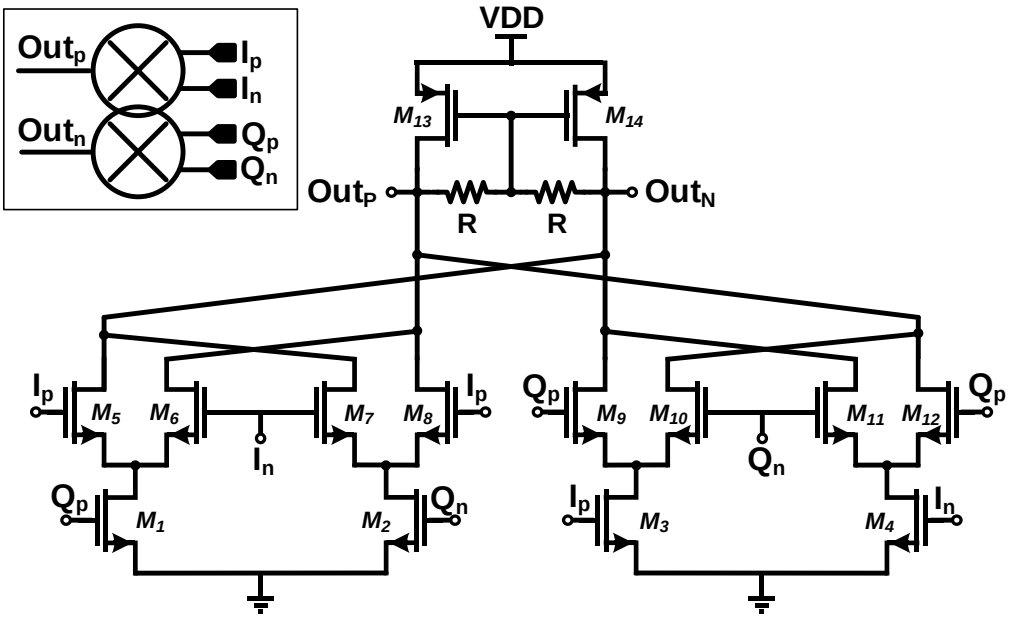

Figure 3.19: Schematic of the phase detector.

The output is proportional to the input phase difference and reaches a minimum when the phase difference θ of the input signal is exactly 90°. The mixer implementation is shown in Figure 3.19. The output of two Gilbert cells is connected together, while their input is cross connected. Inputs are DC-coupled to the switching quad through the transformer center tap, while AC-coupled to the transconductors. Being the same signals fed to the switching quad and the transconductor stage, an optimum input voltage to maximize the gain exists for Vin=700mVpk-pk. Phase detector gain G_{PD} is 20μA/° as shown in Figure 3.20.

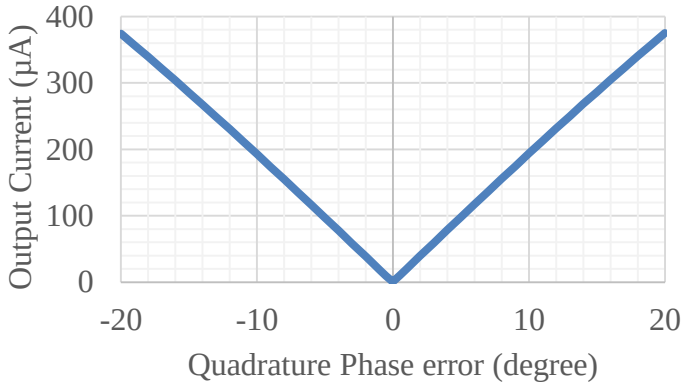

Figure 3.20: Phase Detector Gain.

Regardless the highly symmetric structure [121,122], the offset introduced by the mixer is critical, because, being the mixer the error-detector element in the loop, the quadrature phase error induced by the offset cannot be corrected anymore and results in a static quadrature phase error. This means that the output offset misleads tuning of the polyphase filter, determining an actual quadrature error at generator output. Careful design through Montecarlo simulations indicate that to keep the standard deviation of the static quadrature phase error induced by the offset under 0.15°, W/L of the 8 switching transistors must be at least 35µm/55nm, Layout shown in Figure 3.21. Simulations show that third harmonic components from the buffers, thanks to the good out-of-band attenuation provided by the second-order networks, are not impairing the performance of the phase error detector. The resulting gain from the PPF input to the input of the mixer is about 8dB achieving through LO buffers.

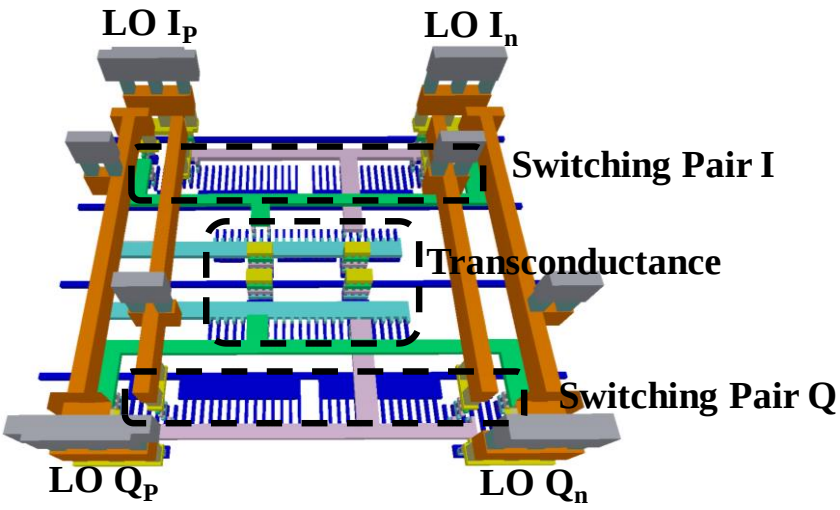

Figure 3.21: Layout of the phase detector.

Error is amplified by a two-stage Trans Impedance Amplifier (TIA). The schematic is shown in Figure 3.22 [123]. The amplifier is based on a common gate stage. The input currents are mirrored to the output branches. Eventually, resistors R perform the current-to-voltage conversion. Local feedback (transistors M3 and M8) is used around the common-gate input stage (transistors M2 and M9) to decrease the differential TIA input resistance. From Monte Carlo

simulations, the DC offset of the TIA can be tolerated without the need for calibration. Post-layout Monte Carlo simulations carried out at top level show that in the 28-42GHz frequency range the mean of IRR is 43dB with a standard deviation of 1.8dB.

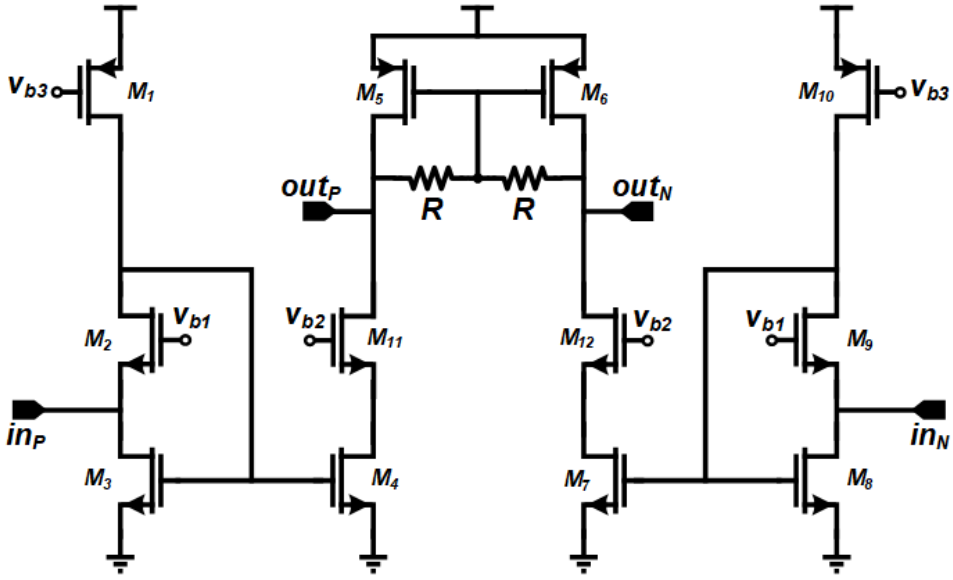

Figure 3.22: Schematic of the trans-impedance amplifier.

3.7 Layout effects on I/Q imbalance

The layout of the PPF is critical at mm-waves [118]. Serpentine interconnections, large elements and dummies to improve matching - commonly employed at the low frequency range, are not suitable because of added losses and parasitics.

In conventional low-frequency PPF design, the layout resembles the device placement of Figure 3.23a. The asymmetric red interconnect introduces a parasitic inductor Lpar, responsible for a differential phase error between the PPF outputs Ip and In, as shown in Figure 3.23b (where R=100Ω, C=40fF). Even if the parasitic inductor can be as low as 30pH, the differential phase error increases to more than 2°. This error directly converts into a quadrature phase error corresponding to half the differential phase error θ, as depicted in the phasor diagram of Figure 3.23c.

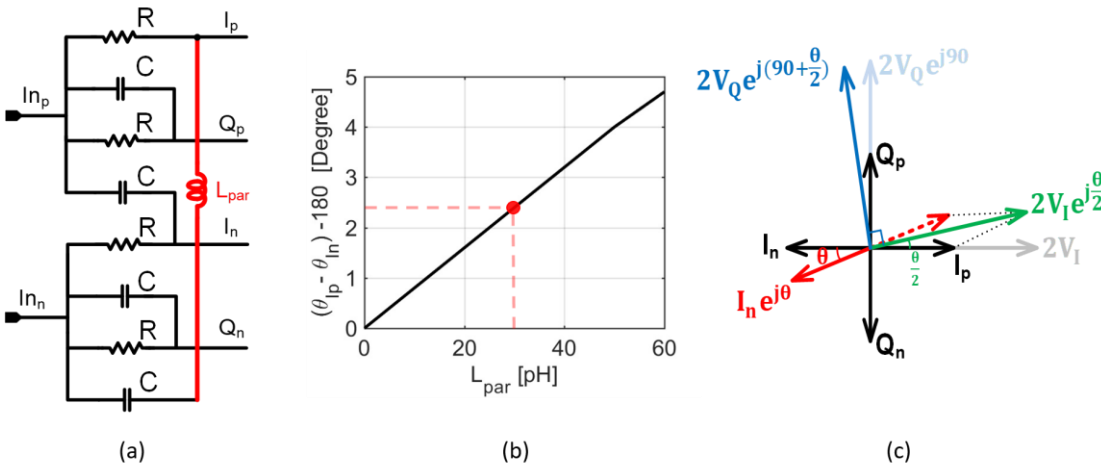

Figure 3.23: Classic PPF layout with asymmetric path highlighted (a), corresponding differential phase error between Ip and In (b) and phasor diagram (c).

Despite the fact that phase detector can minimize also this quadrature phase error, the overall error in the loop increases, requiring an accordingly increased loop gain for precise correction. Most importantly, the loop is not able to recover the remaining differential phase error, which will be directly fed to the mixer input.

To mitigate this effect, we introduced the PPF floorplan depicted in Figure 3.24, where symmetric lines connect the input and output transformers to the PPF. The dummy cross CR2 replicates the CR1 crossing, yielding symmetric routings of PPF components, greatly reducing the systematic differential phase error.

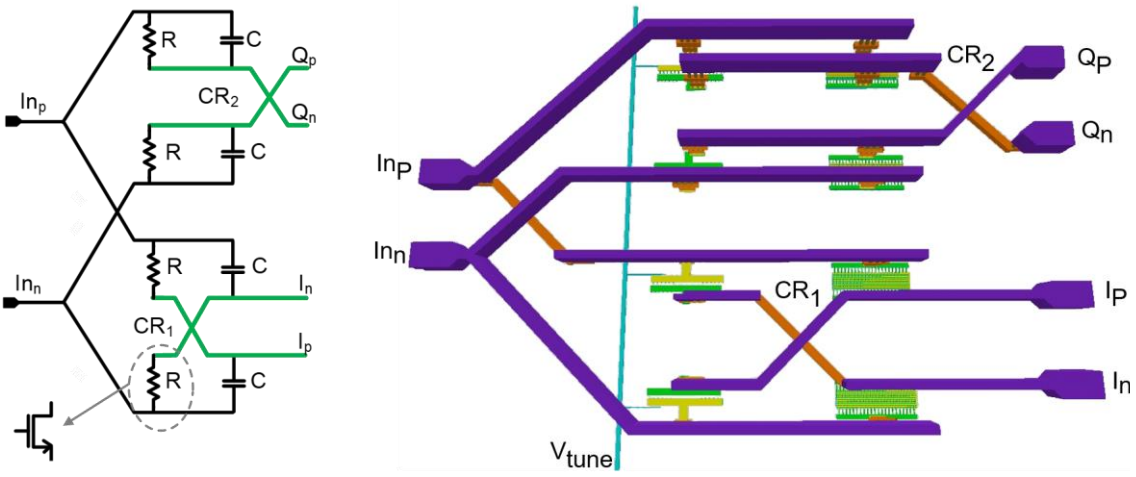

Figure 3.24: Proposed highly-symmetric PPF layout.

3.8 Up-Conversion Mixer

A Double balanced quadrature gilbert mixer shown in Figure 3.25 designed to up-convert a baseband signal provided from outside the chip employing the on-chip quadrature LO signals to perform the up-conversion and Image rejection measurements at the $f_{LO} \pm f_{BB}$ and its harmonics as shown in the spectrum in Figure 3.29.

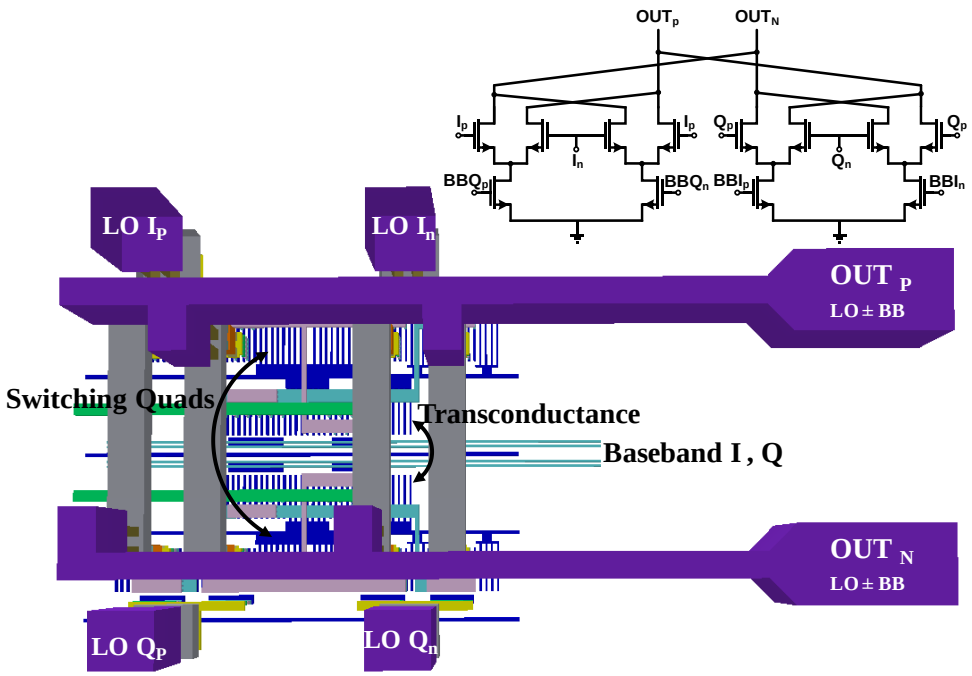

Figure 3.25: Up-Conversion Mixer layout.

Since high frequency routing will model as inductors in parallel in which will couple together and cause very high interfere tones at the output, phase detector, up-conversion mixer and output lines layout play critical role to prevent any additional imbalance at the output as shown in Figure 3.26, up-converted signal at the output of the mixer is coupled to the GSG pad through a balun. DC biasing for the drain of the mixer is provided through center tap of the output balun.

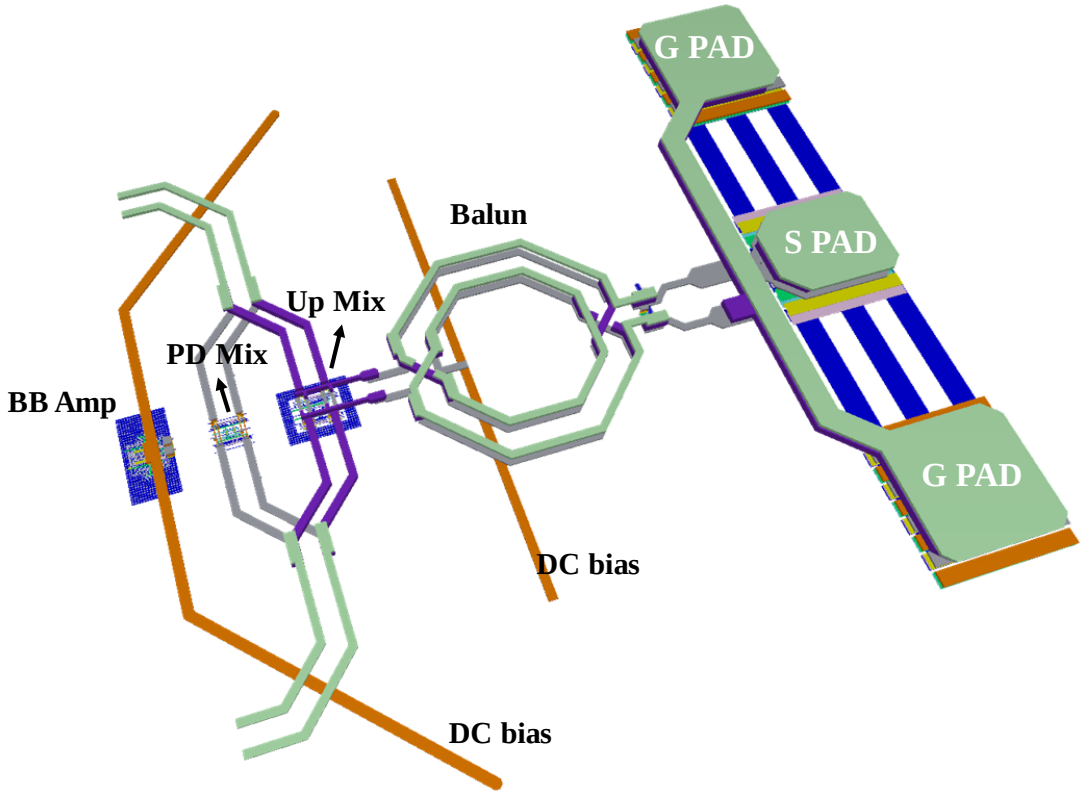

Figure 3.26: Output Layout floor plan.

3.9 Measurements results

Prototypes of the quadrature generator have been fabricated in 55nm CMOS process from STMicroelectronics. A photomicrograph of the die is shown in Figure 3.27. Full chip area is 2.3mm x 1.7mm. The core area is 590µm x 330µm. Power consumption is 36mW for PPF and input/output buffers, and 3mW for the feedback loop - both from 1.2V supply.

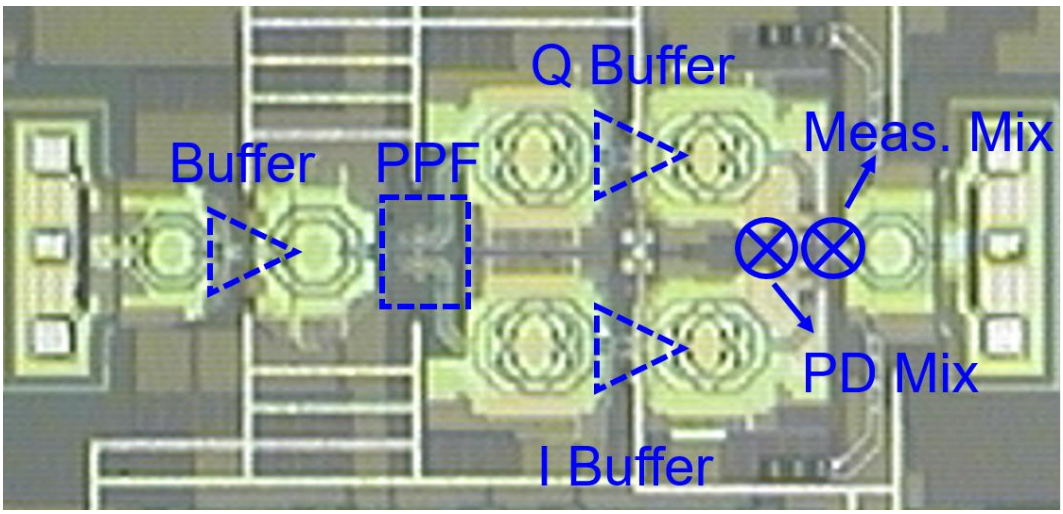

Figure 3.27: Photomicrograph of the chip.

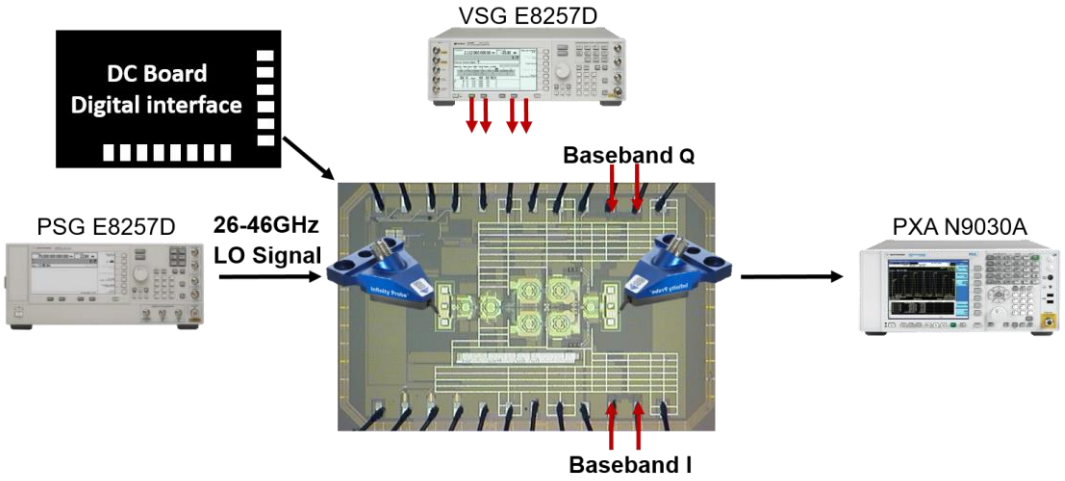

Figure 3.28: Measurement setup.

Figure 3.28 shows the measurement setup. Chip is bonded on a test board, which is connected to another board providing DC supply and digital interface. Input/output are tested with GSG probes. At the input Agilent E8257D PSG is providing 26- 46GHz input signal. To measure the IIR of the quadrature generator, baseband I/Q inputs are fed with 500kHz quadrature signals and output is connected to Agilent N9030A spectrum analyzer. LO input power is 0dBm. Figure 3.29 shows a screenshot of the output spectrum at fc=36GHz, where IRR is ~43dB and LO leakage is -23dBc.

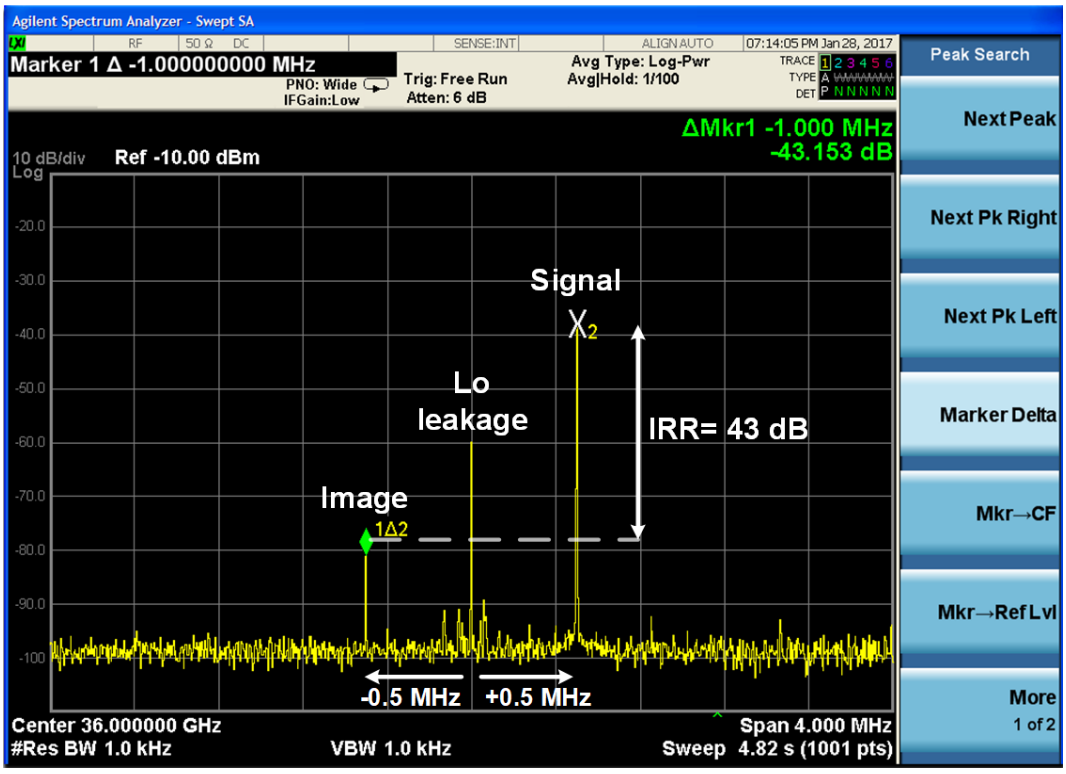

Figure 3.29: Screenshot of the IRR measurement at 36GHz input frequency.

The same measurement has been repeated over 3 different samples by sweeping the input frequency from 26GHz to 46GHz with the loop turned ON and OFF. In the latter, V_{tune} is manually set to the value at which the loop settles at f=36GHz. Results are shown Figure 3.30 and Figure 3.31, where IRR is better than 40dB from 28GHz to 44GHz and demonstrating that the loop is able to recover more than 20dB IRR with a minimum penalty in area and power consumption over a fractional bandwidth of 44%. Measurements have also been carried out by heating down/up the chip to 5°C and 120°C. IRR is well maintained with a minimum bandwidth reduction, underlying the robustness of the proposed scheme.

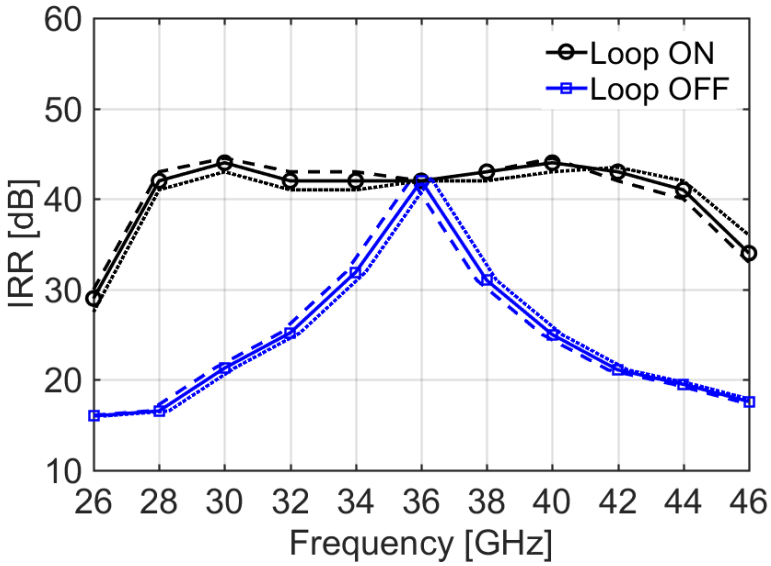

Figure 3.30: Measured Image Rejection Ratio as a function of frequency for 3 samples with the loop ON and the loop OFF with Vtune set for best IRR at 36GHz.

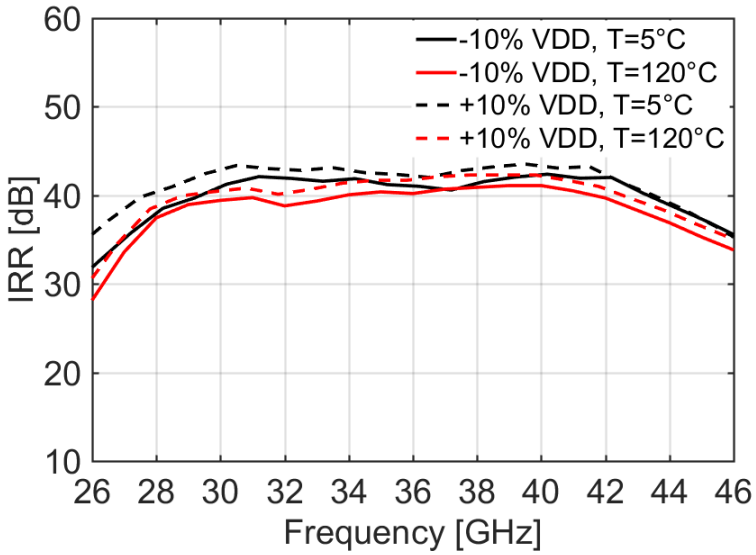

Figure 3.31: Measured Image Rejection Ratio for different supply voltages and temperatures.

Figure 3.32 shows the measured phase noise at the input and output of the quadrature generator at Fs=36GHz. Phase detector mixer and TIA are the major contributors of in-band phase noise, while buffers limit phase noise at large frequency offset from the carrier. The simulated output phase noise with a noiseless carrier of 0dBm power at the input is also shown. The integrated jitter

from 0.1kHz to Fs/2 is 33.5fs - confirming that the proposed scheme adds negligible noise to the input signal.

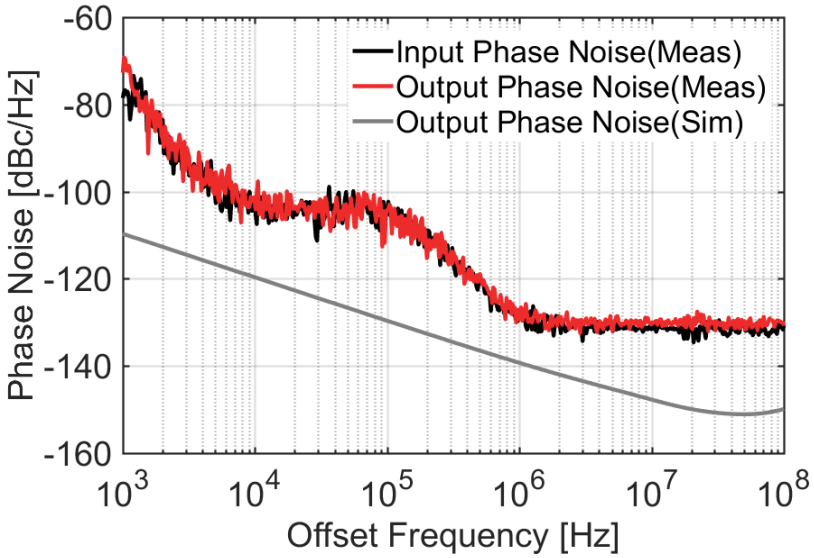

Figure 3.32: Measured phase noise spectrum at the input and output of the IQ generator at 36GHz and simulated output phase noise with a noiseless input carrier at 36GHz with 0dBm power.

Results are summarized and compared with state-of-the-art in Table I. [116] and [124] feature high fractional bandwidth but with poor minimum IRR. [100] shows a remarkable large fractional bandwidth with very good IRR. However, maximum frequency is 12GHz, where impact of parasitics is still limited. Compared to quadrature generators above 20GHz frequency, the proposed scheme yields the best quadrature accuracy (IRR >40 dB) over a remarkably large 44% fractional bandwidth.

Table 3.1: State of the Art Comparison table for Quadrature Generators

	Structure	Process	BW [GHz]	Fractional BW [%]	Phase Imbalance[°]	IRR [dB]	Power Consumption	Area [µm²]
[118]	2-Stage PPF	40nm CMOS	63 - 70	10	N/A	> 35	N/A	65 × 50
[97]	2-Stage PPF	28nm CMOS	55 - 70	24	< 2°	> 32	162 µW	20 × 40
[117]	QAF	130nm SiGe	55 - 78.5	35	< 9.5°	> 21	N/A	Core N/A 1150 × 920
[125]	ILO-ILFM	65nm CMOS	42.7 - 49.5	14	< 1.5°	> 33 [a]	Core 50mW Calibration Loop 35mW	1400 × 2000
[100]	Hybrid Coupler-PPF	65nm CMOS	5 - 12	82	< 1°	> 40	N/A	772 × 925
[124]	QAF	180nm BiCMOS	15 - 35	80	< 13°	> 17	25.2 mW	370 × 299
[126]	Hybrid Coupler	28nm CMOS	57 - 66	14	< 4.3°	> 27	0	Core N/A
[116]	QAF	130nm CMOS	15 - 26	53	< 13°	> 13	11.7 mW	330 × 430
[127]	Hybrid Coupler	40nm CMOS	54 - 67	21	< 3.5°	> 25	8mW / 12 mW	120 × 65
[95]	2-Stage PPF	40nm CMOS	62.5 - 85.5	31	N/A	> 30 [b]	N/A	500 × 450
This Work	**1-Stage PPF**	**55nm CMOS**	**28 - 44**	**44**	**< 0.7°**	**> 40**	**PPF+in/out buffers 36mW Calibration Loop 3mW**	**190 ×170 590 × 330**

[a] Off-chip Calibration Loop

[b] Including Manual Calibration

3.10 Conclusion

Precise quadrature signals over wide frequency range are key for next generation 5G communication systems. To break the trade-off between bandwidth, quadrature accuracy and loss which is typical of most of the quadrature generation blocks, a single-stage automatically-tuned PPF is proposed as precise quadrature generator at mm-waves. A phase detector senses the quadrature accuracy and drives the PPF center frequency to minimize quadrature phase error, while resonant circuits at the input and output ensure wideband operation. The prototype demonstrates state-of-the-art performances over a large fractional bandwidth.

Chapter 4: E-Band Transmitter

This chapter deals with the design of the E-Band (71-86 GHz) Transmitter Project in the BiCMOS 55nm ST Technology, My focus is on the Quadrature LO generation and distribution network following the same concept in the chapter 3 (in which the PPF with feedback loop utilized) with enhancements to overcome difficulties of E-band frequencies. Finally, the work integrated into a Transmitter project and overview and measurement results of the E-Band Transmitter test chip provided.

4.1 E-band TX Overview

The 71-76 GHz and 81-86 GHz bands (E-band) have an atmospheric attenuation of less than 0.5 dB/km at sea level and therefor enable the multi-Gb/s long-haul and back-haul wireless links for mobile and enterprise connection [128]. The work in [55] has shown the feasibility of using one single CMOS power amplifier to cover both the 70 and 80 GHz bands with uniform output power of 20.55±0.35 dBm and PAE of 20.5±1.8% by employing broadband parallel-series power combining. To facilitate the multi-Gb/s complex digital modulation (i.e., 16-QAM or 64-QAM), the remaining challenges at the transmitter side are to minimize the LO feed-through (LOFT) and I/Q imbalance over the complete E-band making higher-order modulations possible over wide-bandwidth.

The works in the literature for the E-band frequencies mainly have two different approach, first to divide entire E-band into lower and upper band and cover each one separately as [33] with the advantage of good performance over each band but in the expense of power consumption and large die area. Second approach is to cover whole 71-86 GHz band with wide bandwidth structure [52, 53, 54 and 133], which introduce challenges to keep the performance high over entire band.

For the Quadrature LO generation, In [33] a 3-dB hybrid coupler used as a core structure to have good matching and compact design, with the disadvantage of the limited bandwidth and process variations. In [52] two stage Polyphase filter followed by passive transformers and metal switch banks to tune the IQ phase imbalance has been proposed, this approach yields the sufficient BW for narrow band applications if PVT variations take into account, also loss of two stage PPF are 6dB and there is need of a Manuel calibration two reach 30dB IRR. In [53] a single stage PPF is used in both Tx and Rx paths to provide quadrature LO signals for image reject mixers, the poor IRR performance of the single stage PPF versus BW is the main limitation for the reported EVM. In [54] a passive LO power splitter of 45 degrees proposed to produce the Quadrature LO to drive the image reject mixer, utilizing the passive T-Lines and RC network to compensate the additional imperfections. It is possible to reach the high IRR but in the expense of very large footprint for overall structure since large loss of this technique compensated with additional buffers, which increase the power consumption used for IQ generation only.

This work demonstrates the circuit, layout and calibration techniques for the I/Q modulator and Polyphase filter (PPF) in the transmitter side to minimize the I/Q imbalance covering wide bandwidth and overcome the limitations of the reported works in the literature. The proposed concept and design methodology lead to the E-band direct conversion TX achieving an un-calibrated image rejection ratio (IRR) greater than 40dB from 66- 90 GHz frequency range. Overall transmitter (Figure 4.1) covers the 66-88 GHz frequency range, providing 21.5 dBm saturated output power, 21dB signal Gain and 20 dB output 1-dB compression point at center frequency. Power consumption including whole structure is 900mW at OP1-dB and 700mW at 6dB back-off.

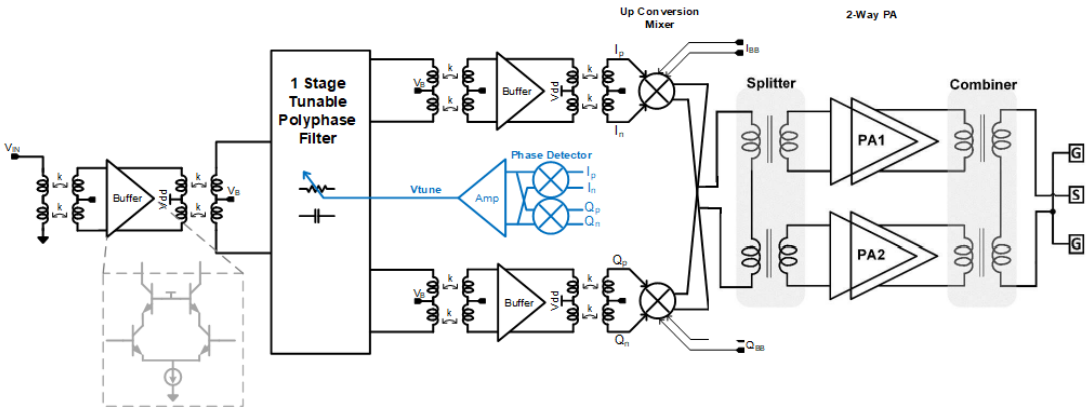

Figure 4.1: E-band Transmitter schematic.

Figure 4.1 shows the system diagram of the implemented E-band direct-conversion transmitter. It consists of an I/Q modulator, tunable poly-phase filter, LO amplifiers, feedback calibration structures to minimize the I/Q imbalance hence enhancing the EVM, Up conversion Mixer and the two-way power amplifier driving the 50 Ohm Load.

4.2 Quadrature Modulator

The E-band Quadrature signal generation follows the same concept as Ka-Band design explained in chapter 3, with main difference in phase detector and error amplifier circuit. Polyphase filter structure is single stage type-a structure with scaled elements, despite the previous design, E-band phase detector and LO buffers utilize BJT transistors to enhance the gain at higher frequencies. Increasing the frequency of the operation, there is barriers for the previous designed phase detector which will be explained in following sections with proposed techniques to overcome the difficulties at E-band.

4.2.1 PolyPhase Filter

Polyphase filter structure is single stage type-a structure with scaled capacitance and transistor values to step up the frequency range shown in Figure 4.2. Symmetrical Layout is essential to reduce the coupling effects and hence imbalances on the output signals quadrature accuracy. Capacitor values of 28

fF and resistors of 71 Ohm selected to put the center frequency at the center of the E-band.

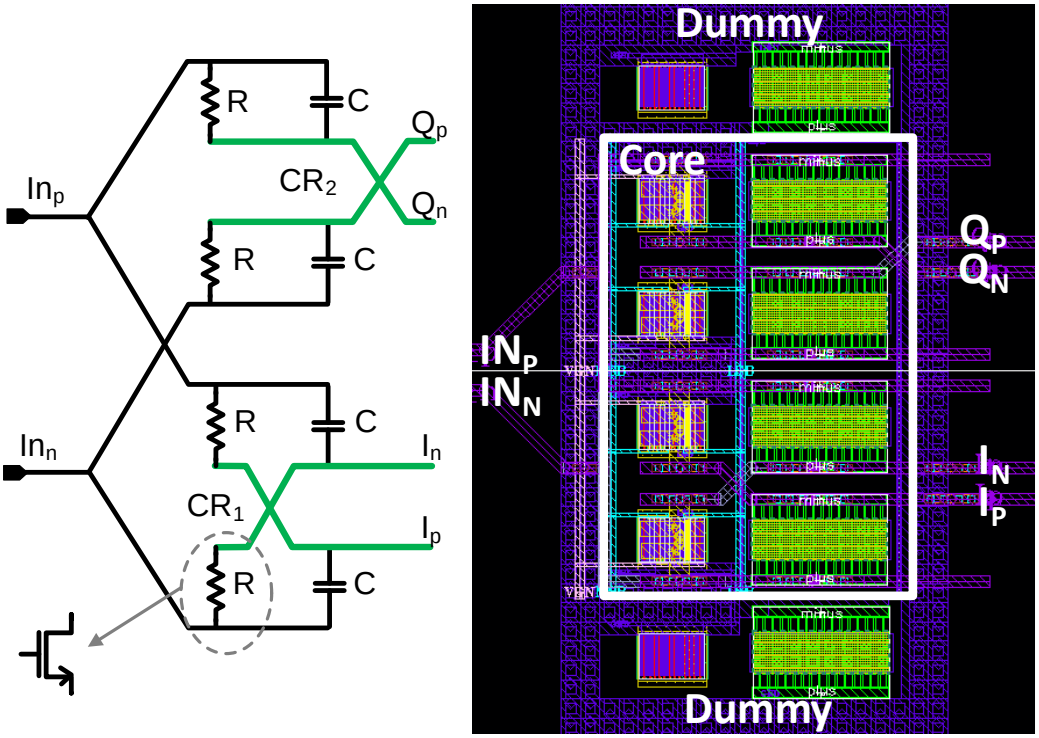

Figure 4.2: Schematic and Layout of the E-band PolyPhase Filter

4.2.2 Quadrature Phase error detector

The injection of two sinusoids at the same frequency, with the same amplitude V but a phase difference θ, generates, after mixing and low-pass filtering, a DC output term given by:

$$V_{PD} = \alpha \, g_{mix} \, Z_{AMP} \, cos\theta \tag{4.1}$$

Where α is the harmonic conversion coefficient, g_{mix} is the transconductance of transistors M1-M2 and Z_{AMP} the baseband amplifier stage trans impedance shown in Figure 4.3.

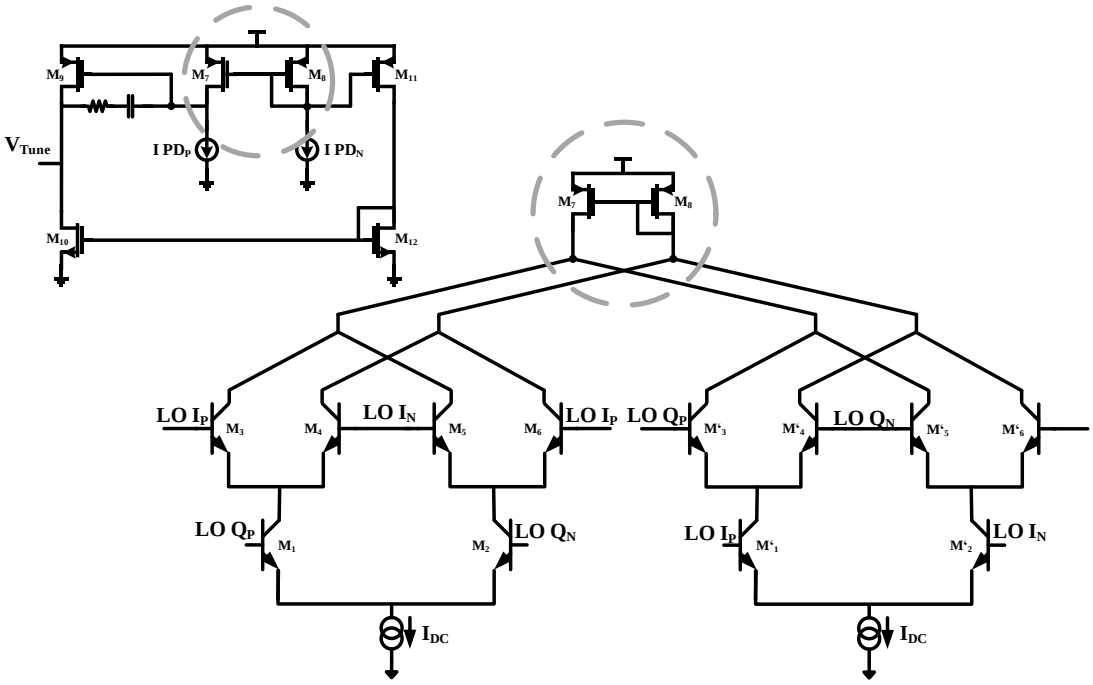

Figure 4.3: Schematic of the phase detector and baseband amplifier.

The output is proportional to the input phase difference and reaches a minimum when the phase difference θ of the input signal is exactly 90° in ideal conditions. However, by increasing the frequency of operation specially reaching the E-band, C_{BE} Capacitance (Figure 4.4) effect causes additional phase shift, which deviates the mixer output current waveforms and greatly reduces the gain. From Appendix 1 Calculations It can be shown that Gain drop due to phase shift in Transconductance path is with the factor of $\cos(\Delta\phi)$.

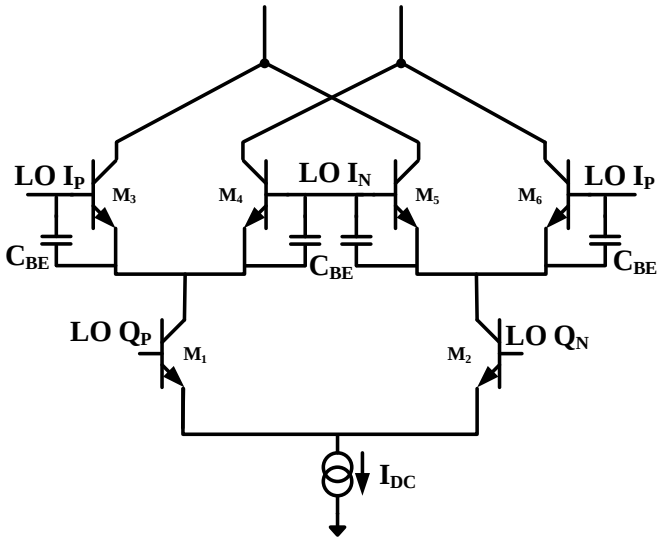

Figure 4.4: Schematic of the phase detector I branch (same for Q branch).

As it is shown in Figure 4.5a, C_{BE} Capacitance and resistance seen from emitter of the mixer switches(M_3-M_6), form a simple filter structure which cause a phase shift of –Δϕ in transconductance path current as shown in Figure 4.5b. This –Δϕ phase shift can be re-modeled as +Δϕ phase shift at the LO path of the switching quad of the phase detector mixer Figure 4.5c.

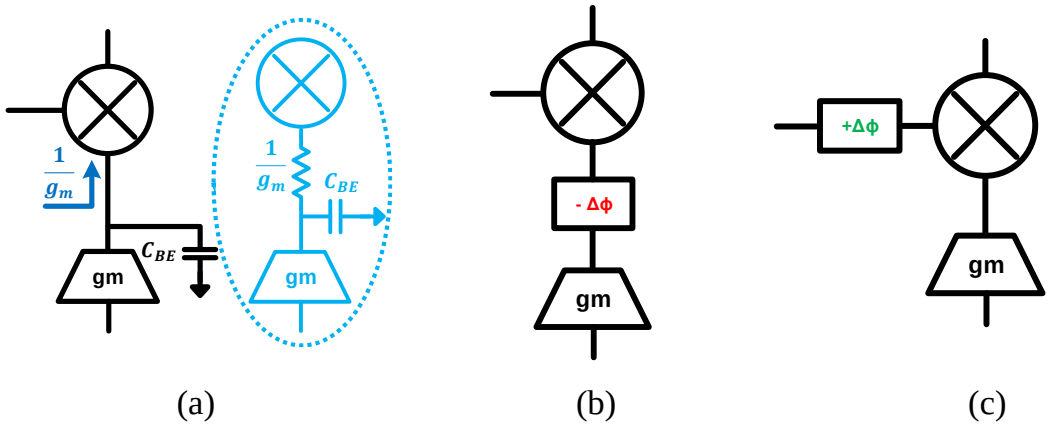

Figure 4.5: (a)C_{BE} Capacitance effect (b) modeled as –Δϕ phase shift in transconductance current path (c) modeled as +Δϕ phase shift in LO path.

Modeling the complete phase detector as a linear transconductor and an ideal multiplier as Figure 4.6 reveals the gain drop effect as shown in Figure 4.7.

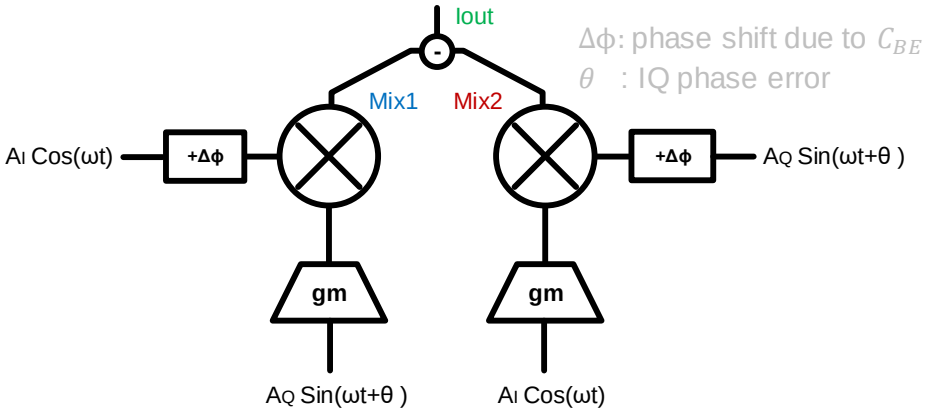

Figure 4.6: Phase detector Model.

Assuming the equal Δϕ phase shift for both I and Q paths of the LO signals, output current of each branch of the phase detector can be written as 4.3 and 4.4. Which θ is the quadrature phase error between I and Q signals, Δϕ is the phase shift due to C_{BE}, A_I and A_Q are amplitude of the LO signals and g_m is the transconductance of the mixer, overall output current will be as equation 4.5:

Assuming, $\Delta\phi_I = \Delta\phi_Q = \Delta\phi$ (4.2)

Output of Mixer 1: $\frac{1}{2} g_m . A_I . A_Q . Sin(-\theta + \Delta\phi)$ (4.3)

Output of Mixer 2: $\frac{1}{2} g_m . A_I . A_Q . Sin(\theta + \Delta\phi)$ (4.4)

Output : $\frac{1}{2} g_m . A_I . A_Q [Sin(-\theta + \Delta\phi) - Sin(\theta + \Delta\phi)]$ (4.5)

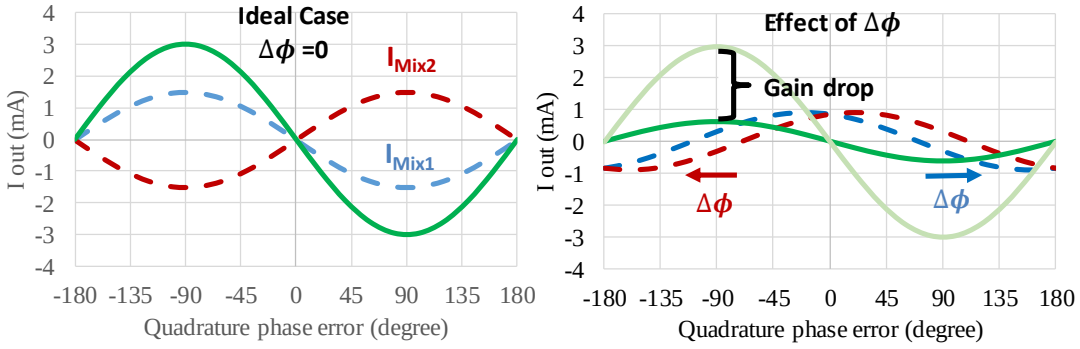

Figure 4.7: Gain drop effect in phase detector.

The immediate solution is to introduce additional phase shift with opposite sign to compensate the Δϕ phase shift effect and to recover the factor of four (12dB) in gain. therefore, adding a series resistance in the base of the switching quad of the mixer, shown in Figure 4.8, will produce additional delay (-ΔƐ) which can cancel +Δϕ caused by mentioned C_{BE} Capacitance effect and recover almost the 12dB gain as simulation result shown in Figure 4.9. This modification will recover the gain almost equal to Ideal case, which simulated in 1GHz frequency therefore; it makes a huge advantage in terms of offset of the phase detector (Output offset of the phase detector divides to the factor of four larger gain so small offset at the input overall) and loop gain depicted in Figure 4.10.

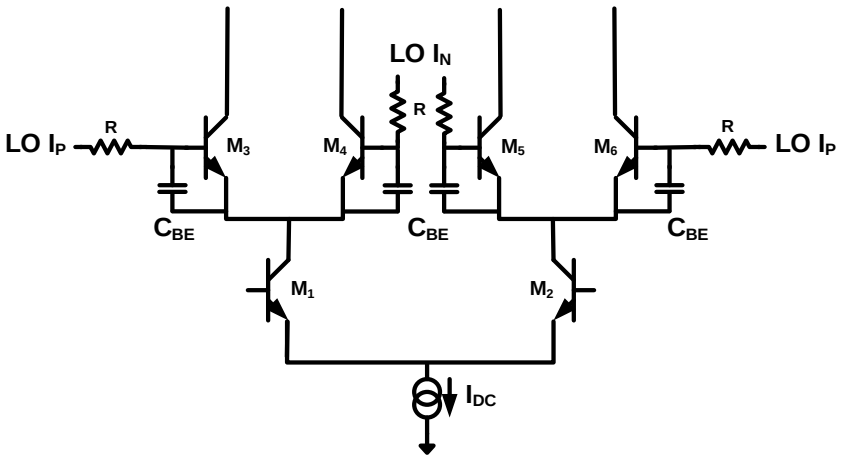

Figure 4.8: Modified phase detector to improve the gain..

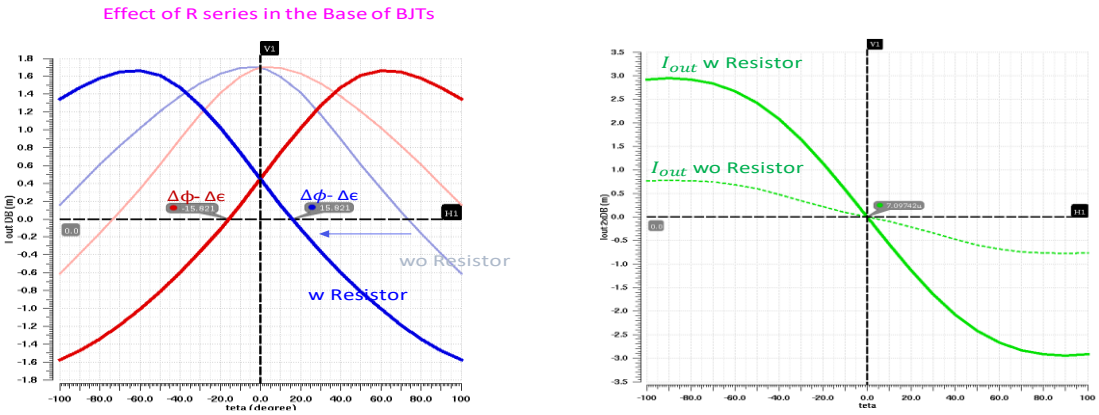

Figure 4.9: Simulation result for series resistance effect on the gain of the phase detector.

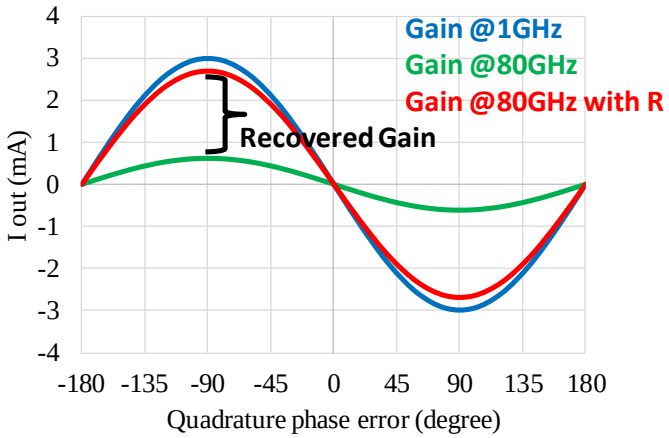

Figure 4.10: Gain of phase detector before and after explicit delay in LO signals.

4.2.3 Amplitude error effect on Phase detector

Along the quadrature LO chain, Amplitude error effect in the Up-conversion Mixer is partially rejected, basically as long as the Quad switches of the mixer are in hard switching fashion, a small variation on the amplitude will not affect the switching operation therefore, amplitude error get suppressed for the up-conversion mixer. On the contrary, phase detector at E-band frequencies is sensitive to LO amplitude error, as a result output quadrature phase error will shift from zero to larger value corresponding to amplitude error in LO I/Q paths. In order to model the amplitude error effect in the phase detector, we can parameterize phase shift introduces in the LO path to the amplitude of the LO

as shown in Figure 4.11, there will be $\Delta\phi_I \neq \Delta\phi_Q$ representing the amplitude error for I and Q waveforms. Equations of 4.2 to 4.5 could rearrange as 4.6 to 4.9 to investigate this effect as plotted in Figure 4.12.

In conclusion, Phase detector is sensitive to amplitude error due to the mechanism mentioned, therefor, residual phase error at the output of the phase detector is increasing if there is amplitude error in the quadrature LO input signals and should be controlled well. For example, amplitude error of 1dB and 2dB Cause residual phase error of 0.75° and 1.5°, respectively. It means that for unlimited close loop gain, quadrature phase error will equal to 0.75° and 1.5°.

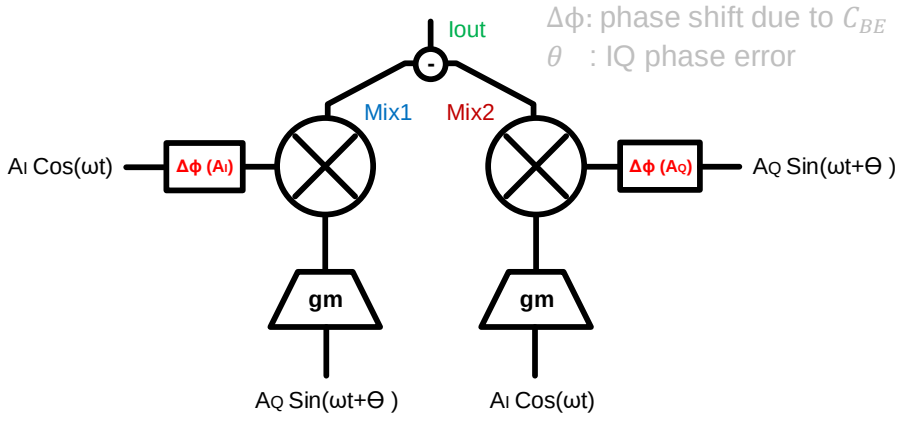

Figure 4.11: Phase detector model assuming amplitude error effect.

Assuming amplitude error, $\Delta\phi_I \neq \Delta\phi_Q$ (4.6)

Output of Mixer 1: $\frac{1}{2} g_m . A_I . A_Q . Sin(-\theta + \Delta\phi_I)$ (4.7)

Output of Mixer 2: $\frac{1}{2} g_m . A_I . A_Q . Sin(\theta + \Delta\phi_Q)$ (4.8)

Output : $\frac{1}{2} g_m . A_I . A_Q [Sin(-\theta + \Delta\phi_I) - Sin(\theta + \Delta\phi_Q)]$ (4.9)

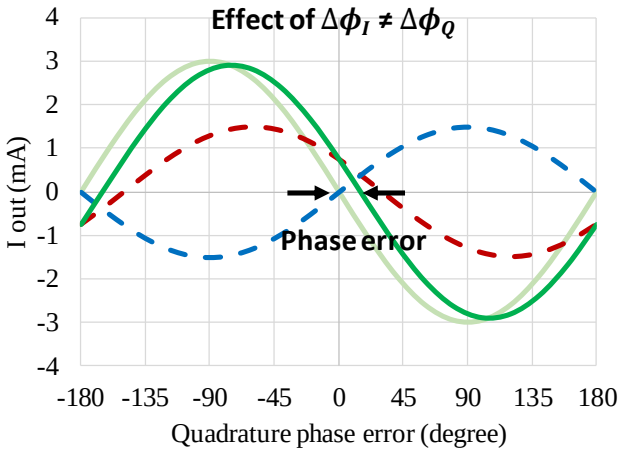

Figure 4.12: Amplitude error effect in phase detector.

Phase detector also layout plays critical role in fixed phase imbalance produced at the output because of any asymmetry or coupling in the layout paths. Keeping in mind that symmetry is key to have accuracy; the fully symmetric floorplan for phase detector depicted in Figure 4.13.

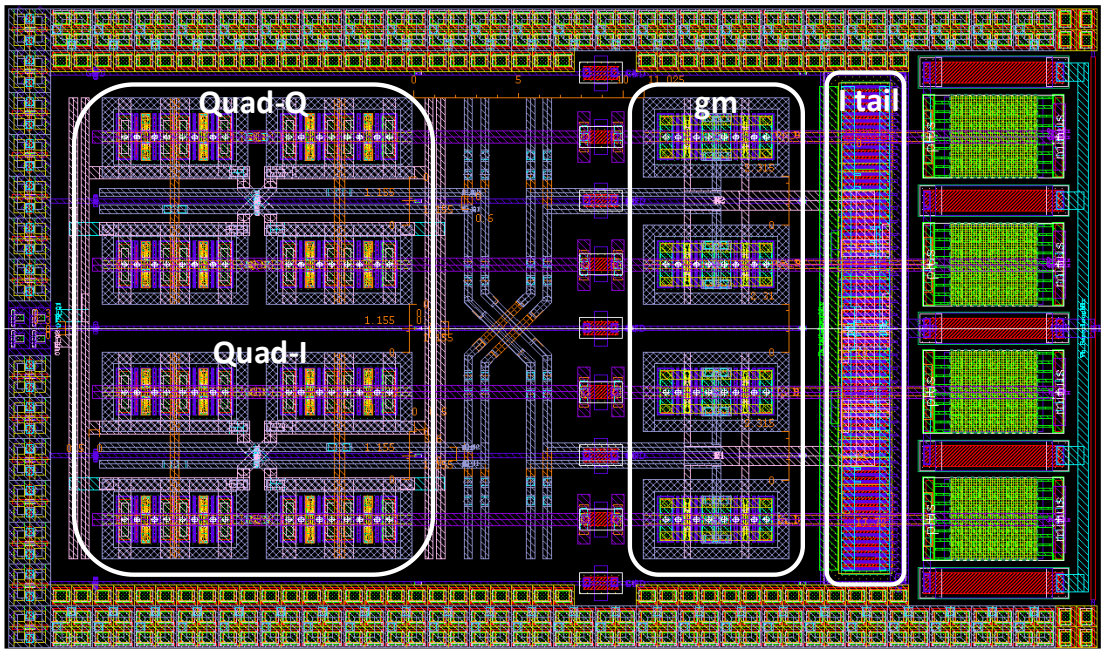

Figure 4.13: Phase detector Layout.

To come to robustness of the design versus process and corners, which is one of the main limitations for quadrature signal generation methods reported, this structure has small deviation in phase detector gain versus process corners

as it can be seen from simulations shown in Figure 4.14 and Figure 4.15. This small variation versus mismatch and process leads to have a good IRR in corners since phase detector is the most critical block in the quadrature generation feedback chain.

4.2.4 E-band LO Buffers

LO buffers utilizes Cascode differential pair structure to get better isolation between input and output (i.e. reduce miller effect) and increase stability. There is two separate buffer for I and Q path in order to properly amplify the LO signal to hard drive the up-conversion mixer and phase detector at the same time as the schematic and layout are shown in Figure 4.16 and Figure 4.17.

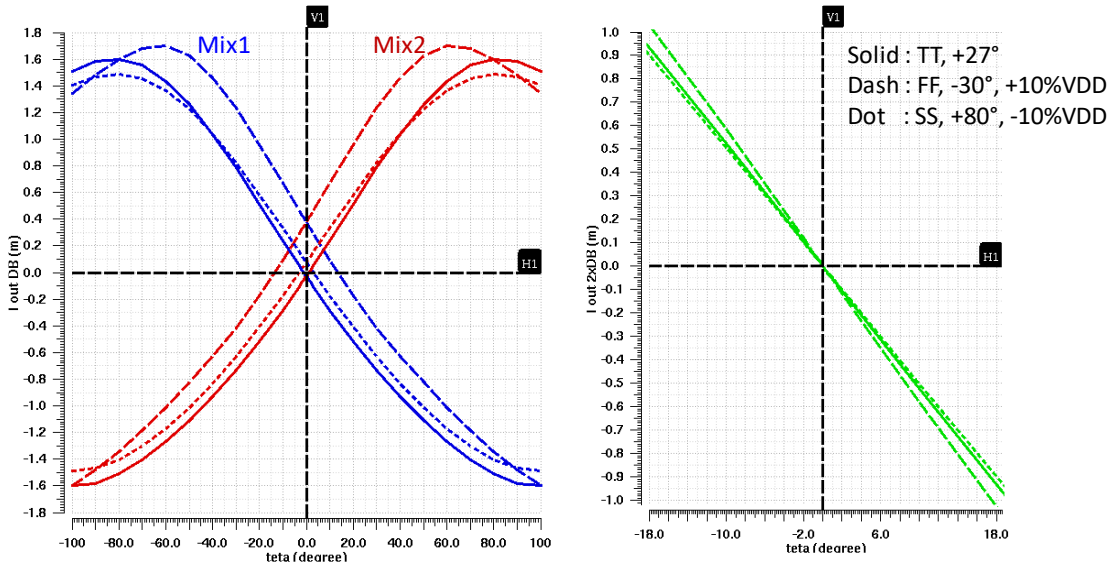

Figure 4.14: Corner simulation results for the phase detector.

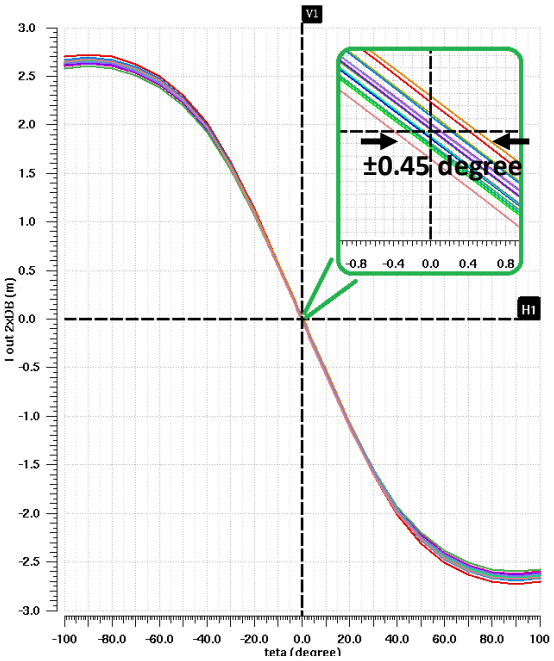

Figure 4.15: Monte-Carlo simulation of the phase detector.

Power consumption for each LO buffer is 60mW from 2.3V supply. Tail current source of the buffers are programmable through SPI interface of the chip in order to have control over the gain. Figure 4.18a shows the simulated transfer function for the LO path and Figure 4.18b shows the quadrature waveforms at the input of the up-conversion Mixer and the phase detector.

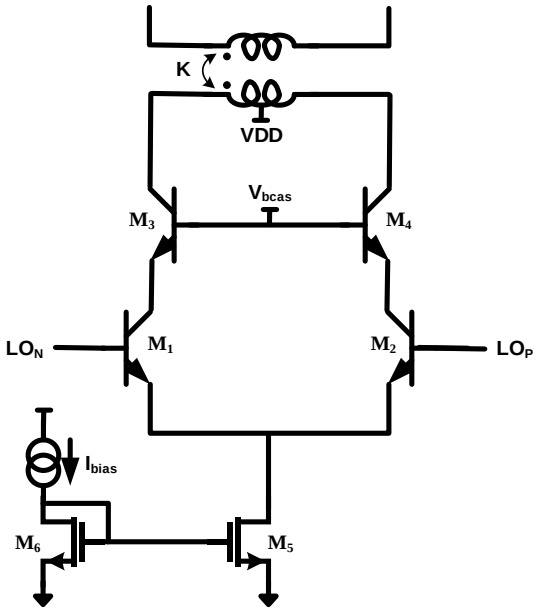

Figure 4.16: Schematic of LO Buffers.

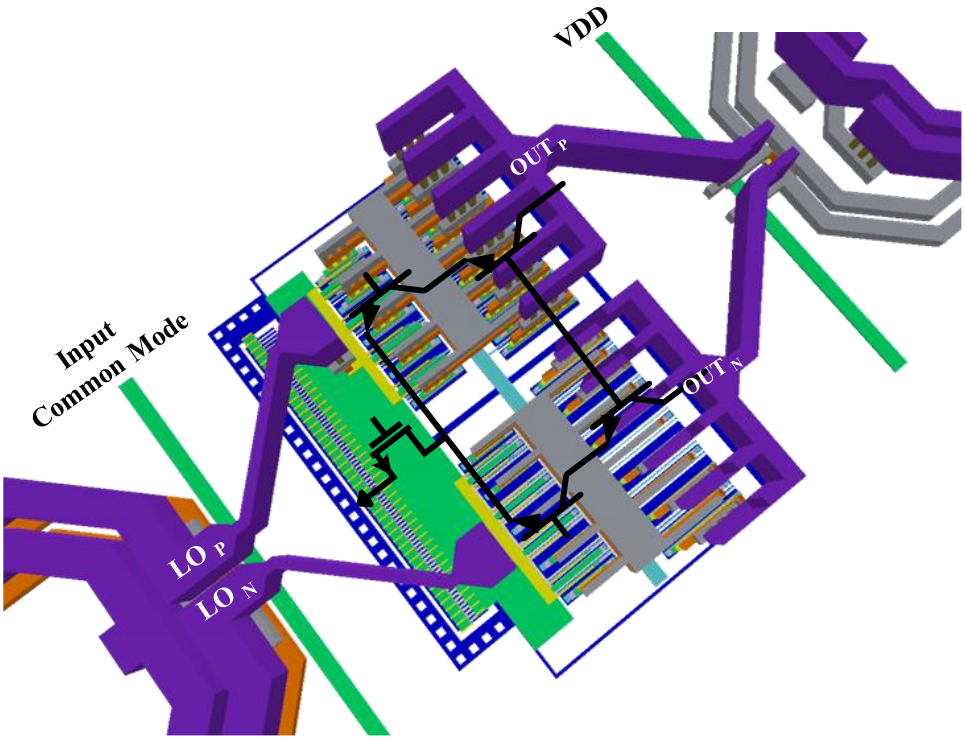

Figure 4.17: Layout of LO Buffers.

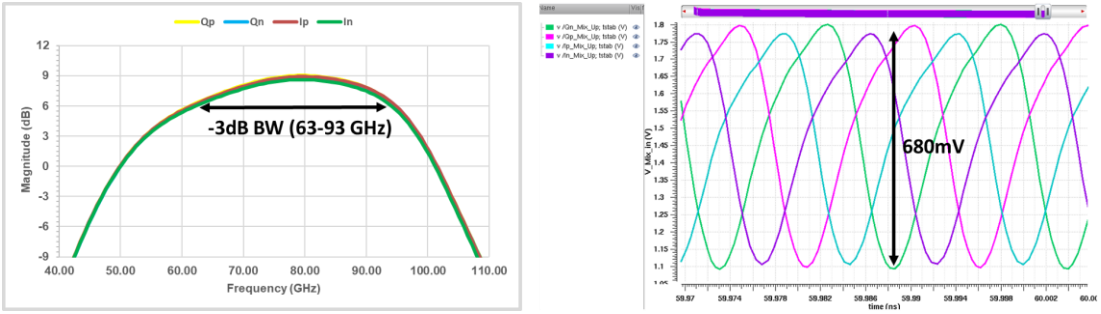

Figure 4.18: LO path transfer function.

4.2.5 Quadratue LO generation Layout

The Quadrature LO generation core size is 310um × 170um and consumes 170mW for three LO buffers and 16mW for calibration loop as shown in Figure 4.19.

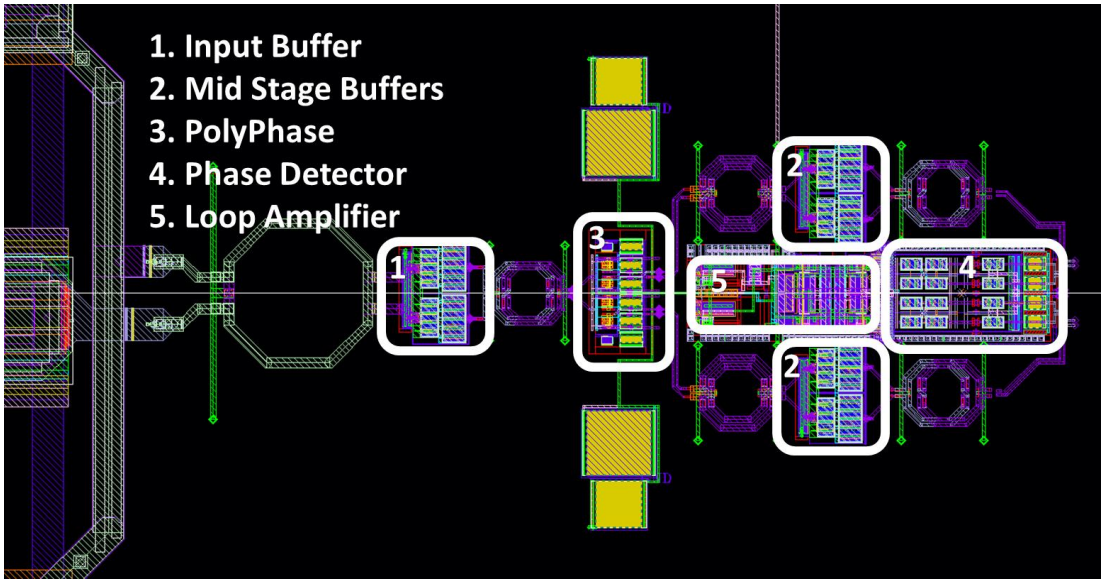

Figure 4.19: Layout of the LO generation core.

4.3 Power Amplifier

Techniques adopted at RF, such as supply modulation for envelop tracking and linearization of switch-mode PA's, do not lend themselves to high-rate mm-wave communications, suggesting further investigation of basic amplifier topologies. Most of the reported E-band PA's are based on common-source/emitter stages and suffer from soft saturation with output power at 1dB gain compression (OP1dB) remarkably lower than P_{SAT}, where efficiency peaks. Class-A biasing yields maximum gain, but efficiency drops quickly at back-off. Class-AB allows current saving at low output power, but still suffering from soft saturation. In this project, the intrinsically linear common-base stage to achieve OP1dB close to P_{SAT} has been exploited. Furthermore, the power stage implements the current-mode version of the well-known diode voltage clamper [129], so that the DC current tracks the signal current yielding a remarkable improvement of efficiency at back-off. The schematic of the single path differential amplifier including a cascode driver, output stage and matching networks is shown in Figure 4.20. The realized core PA prototype [131], in which performed by another PhD colleague, designed for 80GHz center frequency, show OP1dB=18dBm with P_{SAT}=19dBm. The efficiency at OP1dB

and 6dB back-off is 22% and 8.5%, respectively. The two-way PA shows OP1dB of 20.5dBm with P_{SAT}=21.5dBm the efficiency at OP1dB and 6dB back-off is 20% and 7.2%, respectively [131].

The driver adopts a cascode configuration, with $Q_{2a,b}$ and $Q_{3a,b}$ of $A_e=3\times2\mu m^2$,for high output impedance. For maximum gain and best linearity, transistors are biased in class-A with 2×24 mA from a V_{CC}=2.3V supply. An inter-stage matching network, realized with a transformer T_2 and transistor parasitic capacitances, introduces a current gain of ~3. The input impedance of the amplifier is matched to 50Ω with a transformer T_3, $L_{3a,b}$ and capacitance of the input pad while resistor $R_{1a,b}$ ensure unconditional stability also at low frequency[131].

Complete E-band transmitter Layout as shown in Figure 4.21 includes Quadrature LO generation and distribution network, up-conversion mixer and 2-way PA with core are of 1680µm × 2760µm.

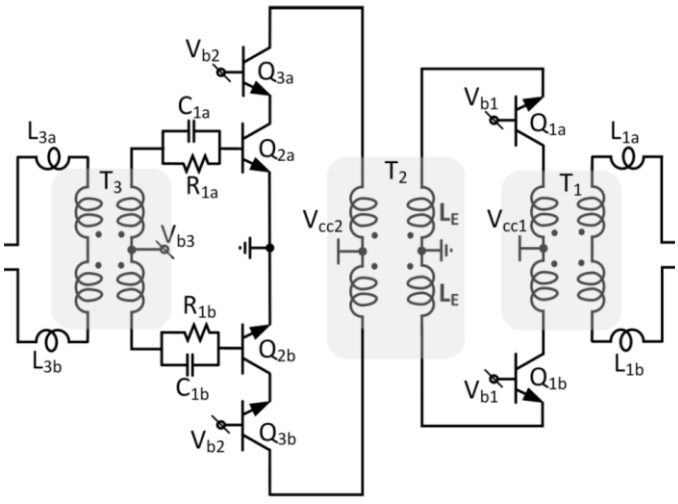

Figure 4.20: Schematic of the E-band single path power amplifier.

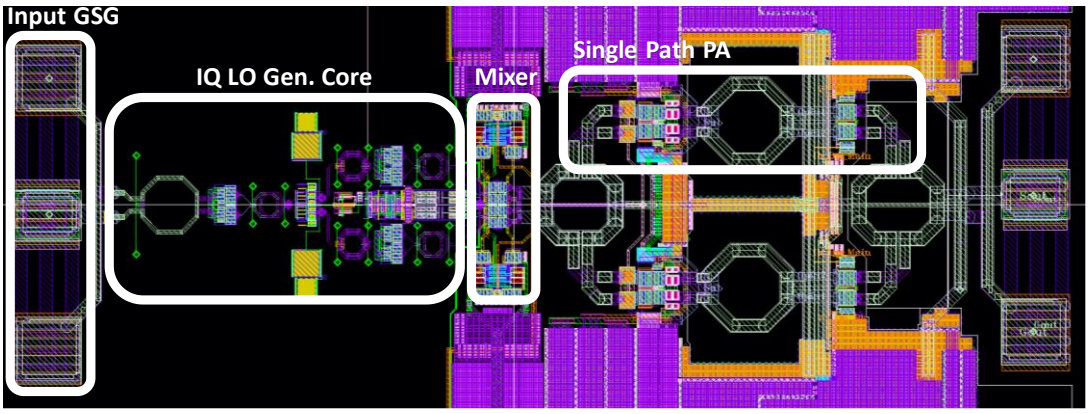

Figure 4.21: Complete E-band TX Layout.

4.4 Transmitter Measurrements

4.4.1 Measurement Setup

Input LO signal generated with Agilent E8257D PSG (Max. 67GHz) passing through multiplier by six extension kit to provide 60-90 GHz input LO signal, applied through GSG probes to the input pad. Baseband signals provided via Agilent E4438C ESG signal generator at f_{BB} frequency (I/Q Max. 1 MHz and needs to be extended). Output signal of the chip is amplified and up-converted to $f_{LO} \pm f_{BB}$, fed to the Ailent N9030A PXA (Max. 50GHz) spectrum analyzer through harmonic mixer (HM1190V Extends PXA range to 50-75GHz and HM11970W Extends PXA range to 75-110GHz range) as shown in Figure 4.22.

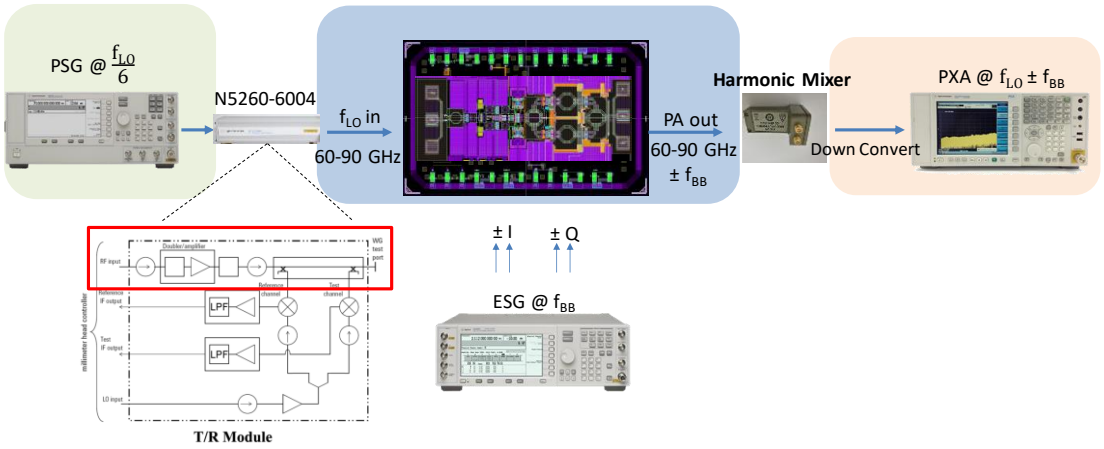

Figure 4.22: Measurement Setup.

The chip manually bonded to the copper PCB board, which will provide the baseband quadrature signals used for up-conversion through SMA connectors, another DC board used to provide voltages and currents for biasing the chip. Matlab software in combination with Arduino used to connect the PC to the chip to hand over bits needed to program serial interface as shown in Figure 4.23 and Figure 4.24.

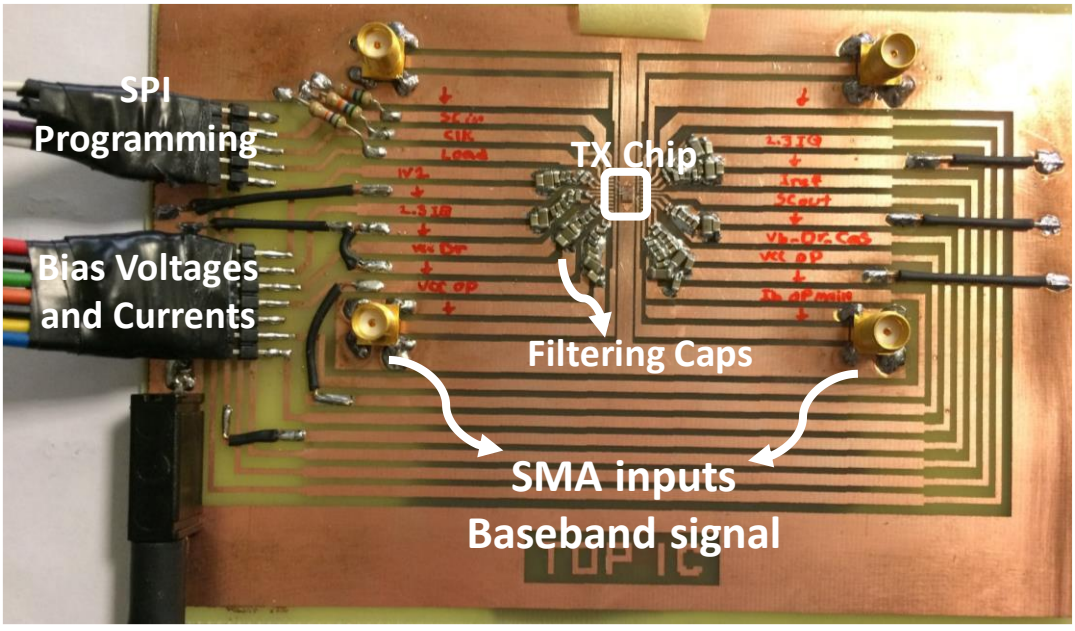

Figure 4.23: TX chip PCB for measurements.

Shift registers serial data is provided through Arduino interfaced between MATLAB and the IC board, also there is a DC board to provide DC levels required to the IC board shown in Figure 4.24.

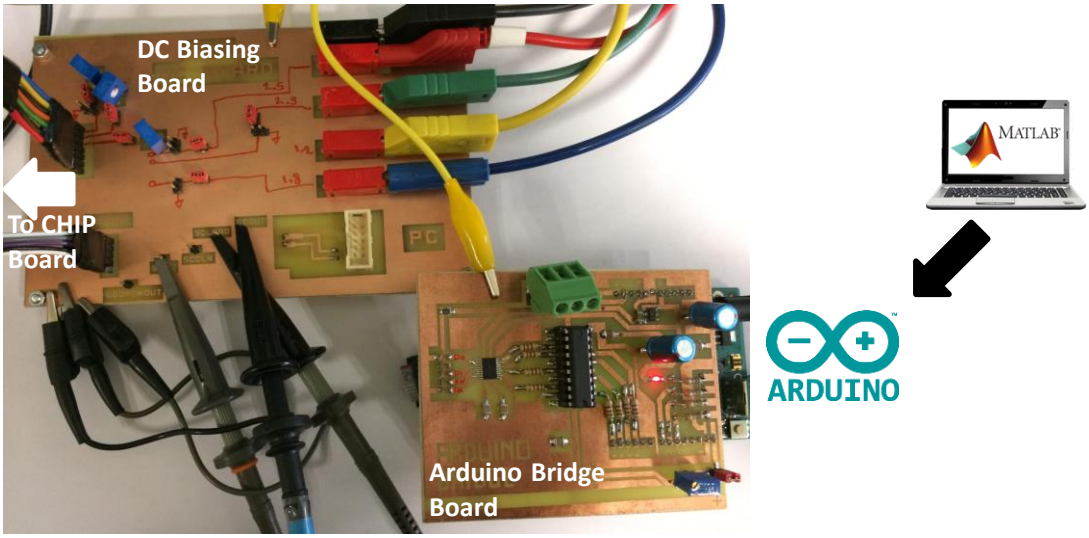

Figure 4.24: PCB for DC Biasing and SPI interface to PC.

Overall Probe station instrument setup shown in Figure 4.25 and Figure 4.26, where a high frequency probe station with probe positioners used to manage the GSG probe placement to perform the high-frequency signal tests. Agilent N1913A EPM Power meter with Power Sensors W8486A and V8486A used to measure overall power at the output of the chip.

4.4.2 Measurement Setup Calibration

To ensure proper measurement, it is essential to calibrate all the setup in order to decompose the path losses and measurement instrument losses both at the input and at the output side of the chip. The methodology performed here is to measure step by step the signal power levels along the chain and produce a calibration coefficient and plot as shown in Figure 4.27.

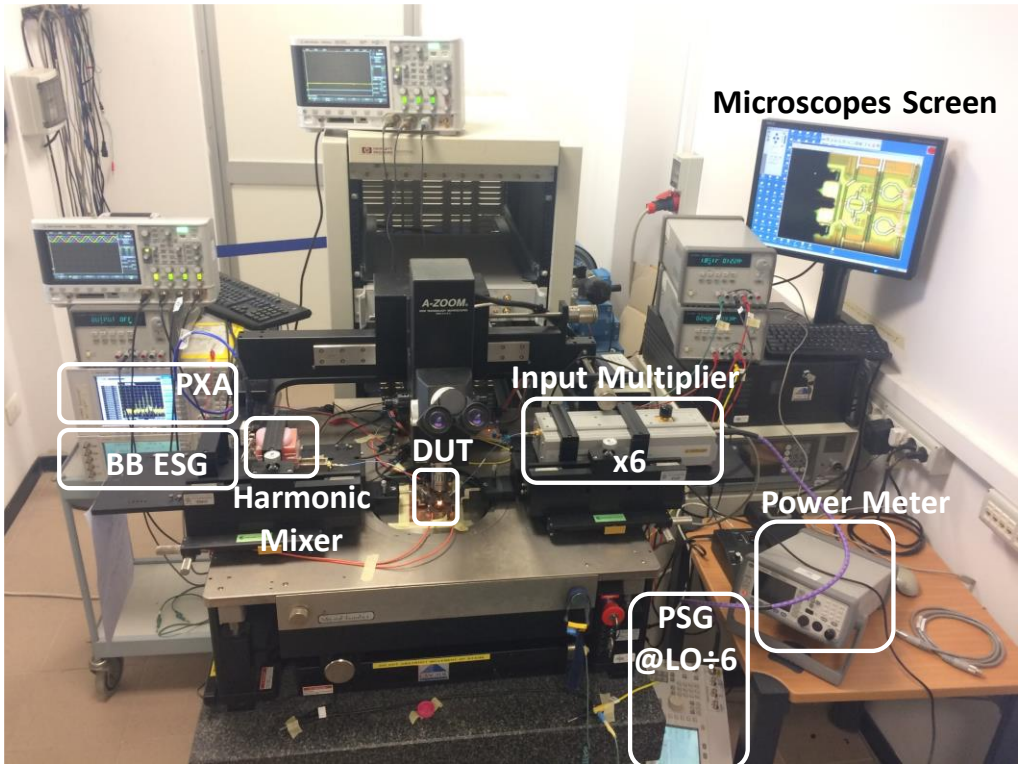

Figure 4.25: Probe station setup.

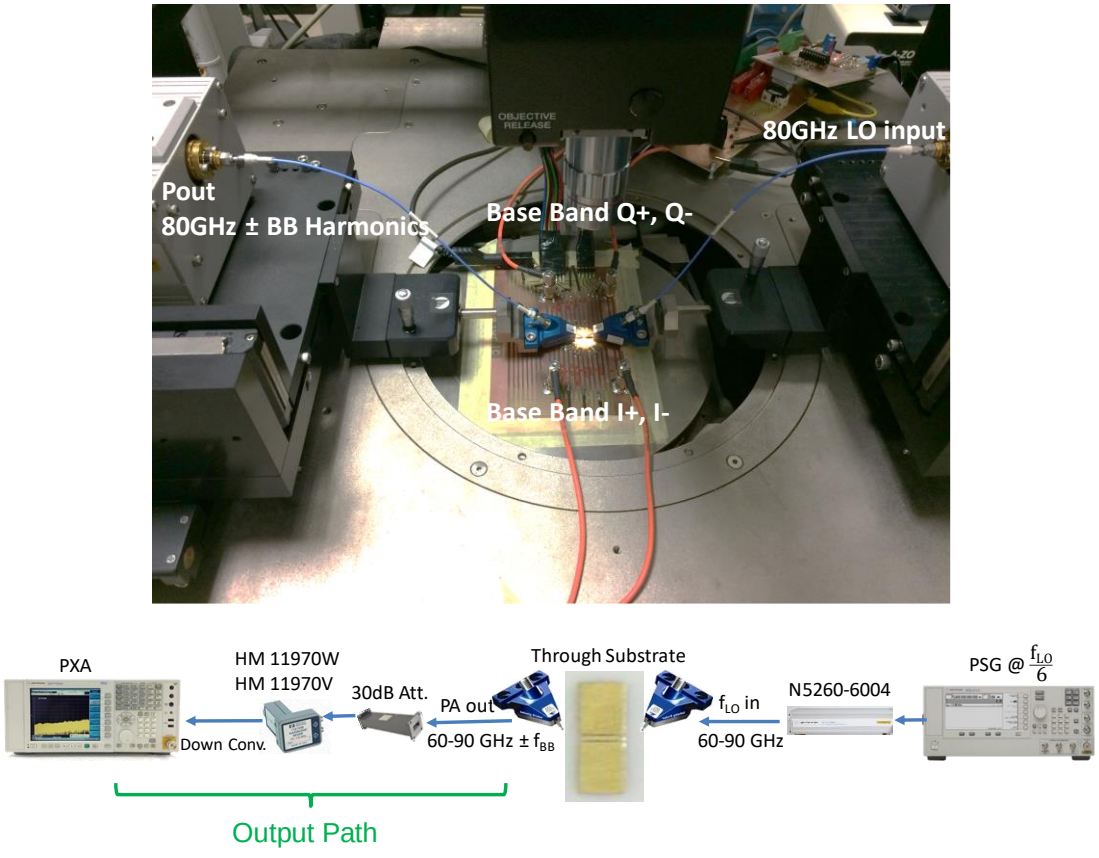

Figure 4.26: GSG Probe landing configuration.

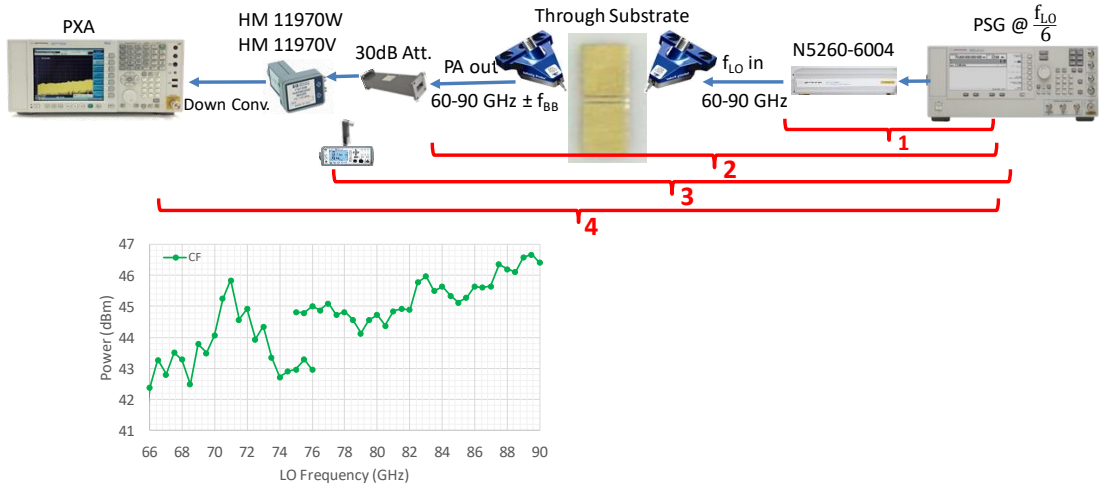

Figure 4.27: Measurement setup calibration.

4.4.3 Measurement Results

Output power, Linearity and Image rejection ratio performance of the transmitter measured by applying baseband signals, perform the full up-conversion process and measure the output harmonics through the PXA as shown in the screen shot at Figure 4.28 and Figure 4.29. For the 80GHz carrier frequency, IRR is about 43dB with the baseband signals at 100MHz. Repeating this measurement for different LO frequency we can measure the IRR performance across the bandwidth as shown in Figure 4.30, in the frequency range of 66GHz to 88GHz IRR greater than 40dB has been proved. Measurements performed at different P_{out} show negligible IRR variation.

As shown in Figure 4.31, IRR measurement versus LO frequency for different TX Gain shows negligible IRR drop in compare to 40dB reference point. In Figure 4.32, IRR measurement versus Baseband signal power for three different LO frequencies shows robustness of the design against base-band signal power level variation.

- Inputs

  LO@80 GHz

  P_{LO} = -3 dBm

  P_{BB} = 0 dBm

  f_{BB} = 100 MHz

- Outputs

  $P_{Main\ Tone}$ = 20 dBm

  IRR = 42.3 dB

  $P_{LO\ Leakage}$ = 24.4 dBc

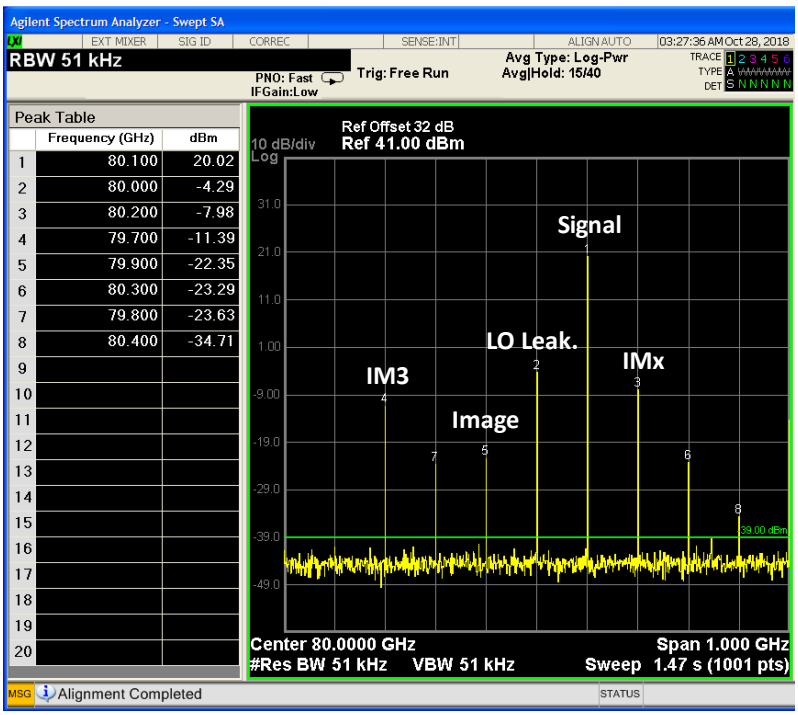

Figure 4.28: Spectrum screenshot at 80GHz carrier freq. and BB freq. of 100MHz.

- Inputs

  LO@80 GHz

  P_{LO} = -3 dBm

  P_{BB} = 0 dBm

  f_{BB} = 200 MHz

- Outputs

  $P_{Main\ Tone}$ = 19.5 dBm

  IRR = 42.7 dB

  $P_{LO\ Leakage}$ = 22.8 dBc

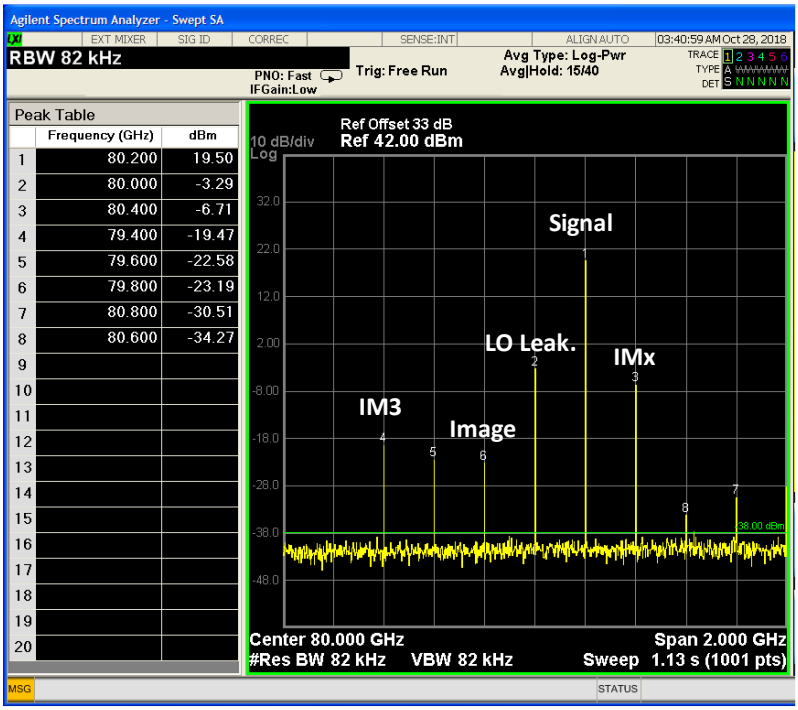

Figure 4.29: Spectrum screenshot at 80GHz carrier freq. and BB freq. of 200MHz.

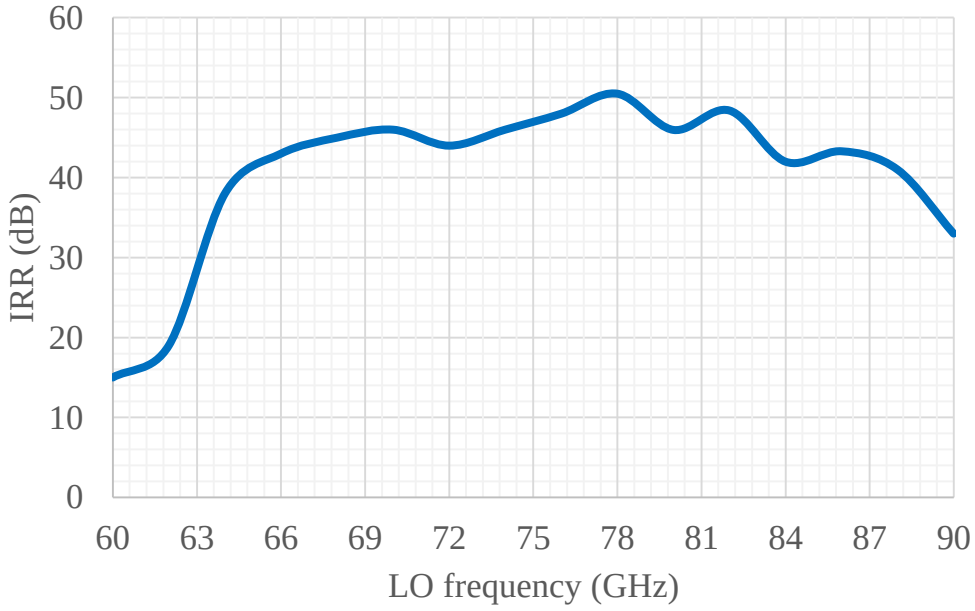

Figure 4.30: Image rejection ratio (IRR) versus LO frequency measurement.

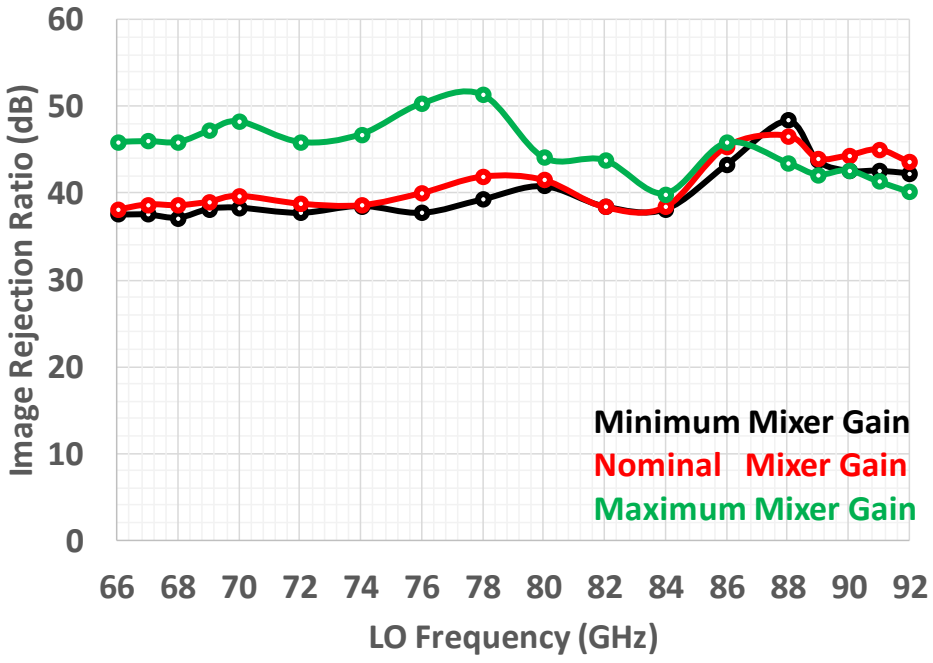

Figure 4.31: IRR measurement versus LO freq. for different TX Gains.

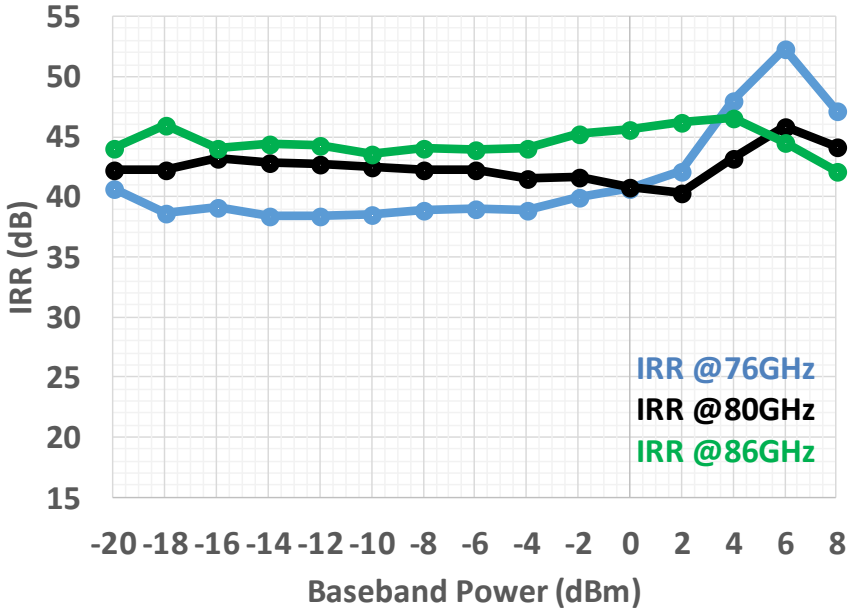

Figure 4.32: IRR measurement versus Baseband Power for different LO frequencies.

Overall transmitter shows 21 dB small signal gain in typical conditions and there is a programmability to increase/decrease by 5dB the gain by acting on the baseband transconductance degeneration bits shown in Figure 4.33. TX achieves OP1dB of 20dBm and P_{SAT}= 21.5dBm shown in Figure 4.33.

Figure 4.35 shows the output power and P_{sat} variation across the bandwidth. PAE at P_{sat} is around 18% and at OP1dB is 13% for 80GHz carrier and drops to 9% and 7% respectively at the edges of the BW. For the linearity measurements, two tone at the input is applied and as shown in Figure 4.36, OIP3 is about 28dBm.

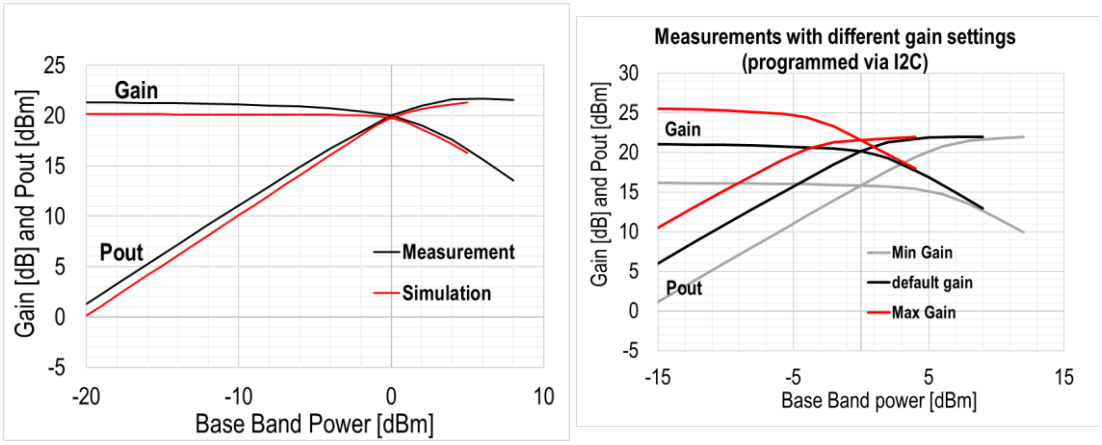

Figure 4.33: Transmitter Gain and Output Power measurement at 80GHz.

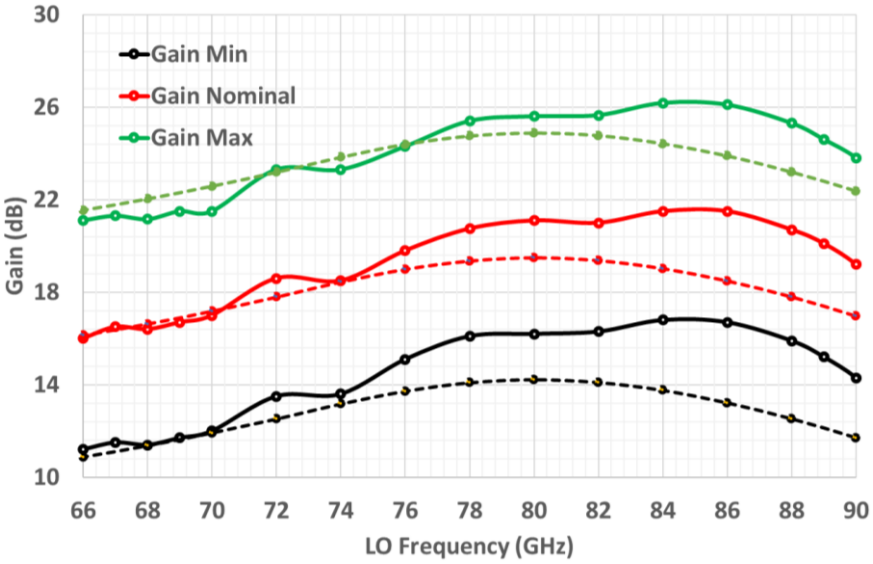

Figure 4.34: Transmitter Gain versus LO frequency for different Gain settings.

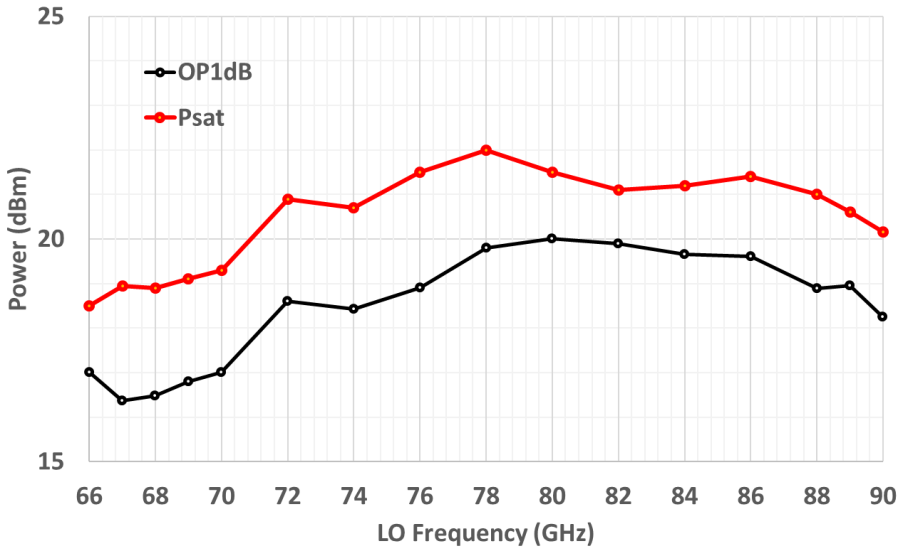

Figure 4.35: Transmitter Pout and Psat performance across bandwidth.

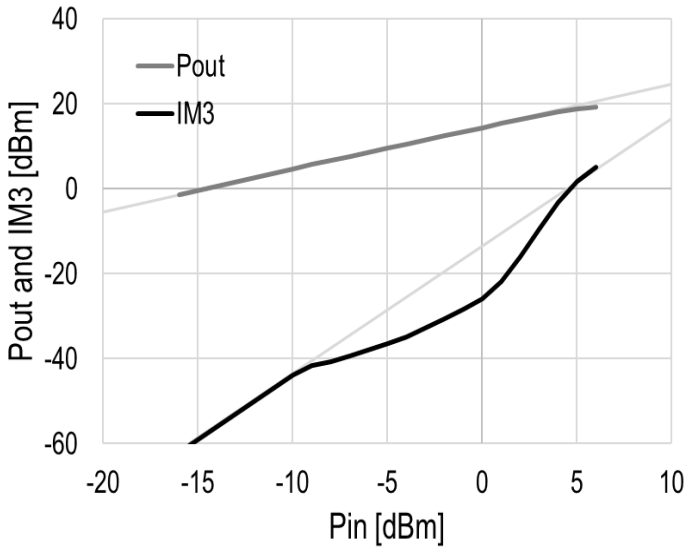

Figure 4.36: Transmitter Pout and IM3 measurement.

4.5 Conclusion

Overall performance and state of the art comparison is summarized at Table 4.1, The work in [33] shows two separate Transmitters each covering Lower (71-76 GHz) and Upper band (81-86 GHz) with 21dB Gain and maximum OP1dB of 6.9 dBm since It is very limited in the output power It has maximum IRR of 30dB and 1800mW power consumption. In [52] a Wide-band Transmitter covering 71-76/81-86 GHz band in 40nm CMOS technology with

11dB Gain, 8.8 dBm OP1dB, greater than 30dB IRR with reasonably low 102mW power consumption presented. In [53] a wideband 71-86 GHz Transmitter with 22.8dB Gain and Psat of 10dBm reported, but IRR is limited to 26dB with power consumption of 330mW. In [54] an ultra-wideband 64-84GHz IQ modulator using LO power splitting passive structures reported with limited Gain of few dBs and OP1dB of 8.3dBm, IRR of 40dB and power consumption of 114mW. In [133] a 130nm SiGe Transmitter for 71-76/81-86 GHz frequency range with high Gain of 38dB, OP1dB of 16 dBm, IRR of 25 dB and 1350mW Power consumption has been implemented. Measurements work in this thesis compares favorably against state of the art in terms of delivered output power, OP1dB and IRR covering complete E-band frequency spectrum.

Table 4.1: Comparison table of E-band Transmitter.

	This Work [Sim.]	This Work [Meas.]	[33]	[52]	[53]	[54]	[133]
Technology	55nm SiGe	55nm SiGe	SiGe	40nm CMOS	90nm SiGe	65nm CMOS	130nm SiGe
Frequency (GHz)	67 – 90	66 – 88	81 / 83 / 86	71 - 86	71-86	64-84	71-76 / 81-86
Gain (dB)	21 (Programmable)	21 (Programmable)	18.9 / 20.9 / 24	9 – 11	22.8	0 (IQM only)	38
OP1 dB (dBm)	20.5	20	3.9 / 4.9 / 6.9	7 – 8.8	NA	8,3	17.5 / 16.6
Psat (dBm)	22	21.5	8.3 / 9.2 / 10.8	11 - 12	7.4-10	11	20.5 / 18.8
IRR (dB)	> 40 (w/o Cal.)	> 40 (w/o Cal.)	> 30 (w/o Cal.)	> 30	> 26	38	> 25
LO Leakage (dBc)	< -50	< -30 < -50 (w Cal.)	-67	-27 -40 (w Cal.)	-	-	-
Power Consumption	900 mW (@ P1dB)	900 mW (@ P1dB)	1815 mW (@ Psat)	102 mW	114 mW	114 mW	1350mW

List of Publications

1. Farshad Piri, M. Bassi, N. Lacaita, A. Mazzanti and F. Svelto, "A >40dB IRR, 44% fractional-bandwidth ultra-wideband mm-wave quadrature LO generator for 5G networks in 55nm CMOS," *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, San Francisco, CA, 2018, pp. 368-370.
2. Farshad Piri, M. Bassi, N. Lacaita, A. Mazzanti and F. Svelto, "A PVT-Tolerent >40dB IRR, 44% fractional-bandwidth ultra-wideband mm-wave quadrature LO generator for 5G networks in 55nm CMOS," *IEEE International Solid - State Circuits Journal - (JSSC)*, Dec.2018.
3. Farshad Piri, N. Lacaita, M. Bassi, A. Mazzanti and F. Svelto, "A >40dB IRR, 44% fractional-bandwidth ultra-wideband mm-wave quadrature LO generator for 5G networks in 55nm CMOS," *2018 Associazione Società Italiana di Elettronica Conference - (SIE)*, Napoli, Italy, 2018.

Appendix 1 – Phase detector Gain Calculations

```
VIp=A*Cos[w t+ΔΦ]; (*ΔΦis the Quadrature Phase Error between I and Q*)
VIn=A*Cos[w t+ΔΦ+π];

IIp=gm*A*Cos[w t+ΔΦ+θ];(*θis the Additional Phase shift due to C_BE *)
IIn=gm*A*Cos[w t+ΔΦ+π+θ];

RecVI= 4*A/π (Cos[w t+ΔΦ] + 1/3 Cos[3*(w t+ΔΦ)] );
(*LO Rect waveform assuming Hard switching*)


VQp=A*Sin[w t];
VQn=A*Sin[w t+π];

IQp=gm*A*Sin[w t+θ];
IQn=gm*A*Sin[w t+π+θ];

RecVQ= 4*A/π (Sin[w t] + 1/3 Sin[3*w t] );


IV1=TrigReduce[IQp*RecVI-IQn*RecVI]
IV6=TrigReduce[IIp*RecVQ-IIn*RecVQ]
Vout=ExpandAll[IV1-IV6]
```

$$-\frac{1}{3\pi}4\,3\,A^2\,gm\,Sin[\Delta\Phi-\theta]+A^2\,gm\,Sin[2\,t\,w+3\Delta\Phi-\theta]-3\,A^2\,gm\,Sin[2\,t\,w+\Delta\Phi+\theta]-A^2\,gm\,Sin[4\,t\,w+3\Delta\Phi+\theta]$$

$$\frac{1}{3\pi}4\,A^2\,gm\,Sin[2\,t\,w-\Delta\Phi-\theta]-3\,A^2\,gm\,Sin[\Delta\Phi+\theta]+3\,A^2\,gm\,Sin[2\,t\,w+\Delta\Phi+\theta]+A^2\,gm\,Sin[4\,t\,w+\Delta\Phi+\theta]$$

$$-\frac{4\,A^2\,gm\,Sin[2\,t\,w-\Delta\Phi-\theta]}{3\pi}-\frac{4\,A^2\,gm\,Sin[\Delta\Phi-\theta]}{\pi}-\frac{4\,A^2\,gm\,Sin[2\,t\,w+3\Delta\Phi-\theta]}{3\pi}+\frac{4\,A^2\,gm\,Sin[\Delta\Phi+\theta]}{\pi}-\frac{4\,A^2\,gm\,Sin[4\,t\,w+\Delta\Phi+\theta]}{3\pi}+\frac{4\,A^2\,gm\,Sin[4\,t\,w+3\Delta\Phi+\theta]}{3\pi}$$

```
FullSimplify[- 4A^2gmSin[ΔΦ-θ]/π + 4A^2gmSin[ΔΦ+θ]/π]
```

$$\frac{8\,A^2\,gm\,Cos[\Delta\Phi]\,Sin[\theta]}{\pi}$$

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