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Design of Single-Channel Sampling-Rate Reconfigurable Asynchronous SAR and Dual-Mode Noise-Shaping SAR ADCs for Space Applications

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Dedicated To:

1. The one who happily sacrifices everything for the success of his children [My Father]
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Table 5. 1. Relationship between delay value and sampling-rate of the ASAR ADC 218

List of Abbreviations

ADC	Analog-to-Digital-Converter
ALICE	A Large Ion Collider Experiment
AMS	Austria Micro System
ASAR	Asynchronous Successive-Approximation-Register
ASIC	Application-Specific-Integrated-Circuit
BP	Bandpass
CDAC	Capacitive Digital-to-Analog-Converter
CIFF	Cascaded-Integrators-Feed-Forward
CLA	Clocked-averaged
CMR	Common Mode Rejection
CMOS	Complementary-Metal-Oxide-Semiconductors
CT	Continuous Time
DAC	Digital-to-Analog-Converter
DFF	Data Flip Flop
DNL	Differential Non-Linearity
DR	Dynamic Range
DT	Discrete Time
DWA	Data Weighted Averaging
EF	Error Feedback
ENC	Equivalent Noise Charge
ENOB	Effective-Number -of-Bits
eXTP	Enhanced X-Ray Timing and Polarimetry
FIR	Finite-Impulse-Response
FSR	Full Scale range
FoM	Figure-of-Merit
FWHM	Full Width Half maximum
GBW	Gain Bandwidth
HDL	Hardware Descriptive Language
HERMES	High Energy Rapid Modular Ensemble of Satellites
IC	Integrated Circuit
IIR	Infinite Impulse Response
INL	Integral Non-Linearity
ISI	Inter-symbol interference
LC	Inductive-capacitive
LSB	Least-Significant-Bit
LOFT	The Large Observatory For X-ray Timing
MASH	Multi-state Noise-Shaping
MDE	Modulation Dither Effect
MES	Mismatch-Error-Shaping
MSB	Most-Significant-Bit
NS	Noise-Shaping
NTF	Noise Transfer Function

OPAMP	Operational Amplifier
OSR	Oversampling Ratio
OTA	Open transconductance amplifier
PCB	Printed Circuit Board
PSD	Power Spectral Density
PSR	Power Supply Rejection
PSRR	Power Supply Rejection Ratio
PVT	Process-Voltage-Temperature
RC	Resistive-Capacitive
SAR	Successive-Approximation-Register
SDD	Silicon Drift Detector
SEEs	Single Events Effects
SFDR	Spurious-free-Dynamic-Range
SNDR	Signal-to-Noise-and-Distortion-Ratio
SR	Slew Rate
SR latch	Set reset latch
STF	Signal Transfer Function
SoC	System-on-Chip
THD	Total Harmonic Distortion
THESEUS	Transient High Energy Sky and Early Universe Surveyor (
TI	Time-Interleaved
TID	Total Ionizing Doze
VCO	Voltage Controlled Oscillator
f_s	Sampling-Rate
ΔΣM	Delta-Sigma Modulator

Abstract

Fueled by ever-escalating pursuit to demystify universe mysteries and accomplish functions impregnable in other ways, an explosive advancement has been observed in research and development activities in space field over the last two decades. This has resulted in various scientific space missions and consortiums, initiated both by small as well as large enterprises. A large majority of these space missions are accomplished by the use of large area photodetectors, accompanied by X/ɣ-rays spectroscopy and imaging technologies. Dedicated multi-channel Complementary Metal Oxide Semiconductor (CMOS) Application Specific Integrated Circuits (ASICs) are essential for a consistent and accurate readout of these photodetectors. Analog-to-Digital-Converters (ADCs) are indispensable components of these readout ASICs. Acting as a bridge between the analog front-end and digital back-end sections of the ASICs, overall performance of these ASICs primarily revolves around ADCs. Besides low-power, low-profile, low-noise, a unique set of stringent requirements and challenges are posed by these ADCs for space applications. This pushes the need for innovative ADC architectures and circuits to meet these requirements.

Instigated by this need, this thesis is devoted to the development and design of ADC architectures and circuits for activity-driven multi-channel CMOS ASICs for space applications. Selecting CMOS ASIC for Enhanced X-Ray Timing and Polarimetry (eXTP) space mission as a benchmark, this thesis presents design and characterization of two different single-channel ADC architectures, proposed for the first time for multi-channel CMOS ASICs for space applications. ADC architectures have been developed after performing rigorous review of the already proposed ADCs in the literature. Both the ADCs have been implemented and fabricated in AMS 0.35 µm CMOS technology. Each type of the proposed ADC comes with two versions: version 1, and version 2. Version 1 of each ADC is the one whose all sections operate at a supply voltage of 3.3 V. While the digital section of version 2 of each ADC operates at a supply voltage of 1.2 V.

The first proposed ADC architecture is an 8-bit ENOB sampling-rate (f_s) reconfigurable Asynchronous Successive-Approximation-Register (ASAR). The proposed ASAR ADC initiates the conversion process by a single external low duty-cycle and low-switching trigger signal 'CLKSampling' and generates all other required control signals internally. Unlike all other ASAR ADCs proposed in the literature, this ADC presents a novel rising edge only variable delay-cell to provide desired delay values to the internally generated clock signal for the comparator. The ADC is reconfigurable with respect to its sampling-rate (f_s), spanning from typical 40 kHz to 167 kHz. The f_s-reconfigurability of the ADC comes with proportionate power consumption. External trigger 'CLKSampling' signal is customizable with respect to its time-period and duty-cycle and can be tailored as per the primary requirements of the application. A simple and effective metastability watchdog circuit is part of the design for detection and self-correction of comparator's metastability events. The ADC reaches a measured ENOB and peak SNDR of 7.76-bits and 48.47 dB, respectively. Values of measured Differential Non-Linearity (DNL) and Integrated Non-Linearity (INL) lie within one LSB. Normalized figure-of-merit (FoM_{WN}) - proposed to fairly compare high voltage-based ADCs with low supply-based ADCs - of version1 of the ADC is 476 fJ/c-step at its maximum f_s. While FoM_{WN} improves to 261.7 fJ/c-step for version 2 of the ADC with power consumption of the level-shifters included. Excluding level-shifters power consumption, FoM_{WN} comes out to be only 243 fJ/c-step. Performance (ENOB and SNDR) of version 2 of the ADC is the same as of version 1.

The sampling-rate reconfigurable, dual-mode, 1st-order Noise Shaping (NS) SAR ADC is the second ADC architecture proposed in this thesis. The core of the NS-SAR ADC is 8-bit ASAR ADC, i.e., the first ADC proposed in this thesis. The NS-SAR ADC operates in two modes: NS or free running and incremental. 1st-

order Error-Feedback NS has been achieved with the use of a Finite Impulse Response (FIR) filter. To reduce power, Operational Amplifier (OP-AMP) of FIR filter operates in a duty-cycled manner. To introduce incremental mode operation, the reset and decimation functions have been added with the use of a dedicated synthesized digital logic. The dual-mode ADC can be operated either in NS mode or incremental mode with an external control. Like the ASAR ADC, the dual-mode ADC also features f_s-reconfigurability with a proportional power dissipation. The f_s of the dual-mode ADC spans from 40 kHz to 167 kHz at an OSR of 8, leading to Nyquist bandwidth of 2.5 kHz and 10.43 kHz, respectively. The dual-mode ADC supports an OSR value of 8, 16, and 32 in both operating modes, thus adjusting its f_s and bandwidth accordingly. All the sampling-rates of ADC support these three OSR values, thus offering a great deal of flexibility in ADC.

The measured ENOB, peak SNDR, and Dynamic Range (DR) of dual-mode NS-SAR ADC in NS/free running mode are 10.6-bits, 66 dB, and 67 dB, respectively at an OSR of 8. 1.3 bits rise in ENOB and 8 dB in SNDR is achieved with doubling the OSR. The ADC FoM_{WN} in NS mode is 511 fJ/c-step at its maximum f_s (167 kHz) at an OSR value of 8 for version 1, while it is 296 fJ/c-step for version 2 at an f_s of 132 kHz at OSR value of 8. In NS mode, FoM_{SN} is 157 dB at all supported sampling-rates for both the versions. The ADC performance (ENOB, SNDR, and DR) remains the same at all supported sampling-rates of version 1 of the ADC. In addition, version 2 of the ADC in NS mode exhibits the same performance (ENOB, SNDR, and DR) as version 1.

In incremental mode, the ADC secures an ENOB and peak SNDR of 10.25-bits and 63 dB, respectively at an OSR value of 8. ENOB and SNDR increase by 0.9-bits and 6 dB, respectively doubling the OSR. In incremental mode, the ADC exhibits FoM_{WN} value of 670 fJ/c-step at its maximum f_s (167 kHz) at an OSR value of 8 for version 1. FoM_{WN} improves to 334 fJ/c-step at 132 kHz f_s at an OSR value of 8 for version 2. FoM_{SN} in incremental mode is constant for all covered sampling-rates and its value is 155 dB. Performance (ENOB and NSDR) of both the versions of ADC in incremental mode is the same.

Chapter 1

INTRODUCTION

Chapter Abstract

The ever-growing quest to demystify universe mysteries has resulted in tremendous progress in research and development activities and scientific missions in the space field recently. This chapter starts with a succinct introduction on the importance of space applications and missions (section 1.1), accompanied by a brief description of the significance of small satellites for such applications (Section 1.2). Section 1.3 of the chapter is dedicated to the X/ɤ-ray imaging and spectroscopy - core technologies for a majority of the space missions- achieved with the help of Silicon Drift Detectors (SDDs) electronic device. Thus, section 1.4 is devoted to the overview and working operation of the SDDs. Dedicated multichannel CMOS ASICs are needed to read-out the SDDs signals. The relevant details to these ASICs for this application are part of sections 1.5 and 1.6. The ADCs are an essential part of these read-out ASICs. Section 1.7 outlines the significance, requirements, challenges, and specifications of the ADCs for these multi-channel CMOS ASICs, which is the primary goal and aim of this thesis. The chapter ends with the thesis outline.

1.1. Space Applications and Scientific Missions

The world has witnessed an unprecedented acceleration in research and development activities related to the space and satellite sector in the last two decades in order to achieve the functions and tasks not possible to achieve in any other way. A few of such functions include the discovery of the universe's mysteries by exploring space, remote sensing, surveillance, navigation, weather forecasting, etc. Especially, the interest in exploring space to discover universe mysteries has drawn substantial attention of large enterprises and institutions, and thus resulted in various large international space missions and projects. Some examples of such space missions include 'The Large Observatory For X-ray Timing (LOFT)' [1, 2], 'High Energy Rapid Modular Ensemble of Satellites (HERMES)' [3], 'Transient High Energy Sky and Early Universe Surveyor (THESEUS)' [4], and 'A Large Ion Collider Experiment (ALICE)' [5]. 'Enhanced X-Ray Timing and Polarimetry (eXTP)' [6, 7] is such a flagship scientific space mission, organized and coordinated by an international consortium. Being led by the Institute of High Energy Physics of Chines Academy of Sciences, the eXTP international consortium is comprised of institutions from China and eleven European countries.

The major aim of the eXTP mission, as its name indicates, is the exploration of the universe by performing X-rays studies for timing, spectroscopy, and polarimetry in the late 2020s and early 2030s. Specifically, the eXTP mission is aimed at discovering the answers to three main open challenging questions related to Astronomy and Astrophysics. The first aim is to achieve the knowledge of the properties of ultra-dense matter and discovery of its equation of state. The second goal is to unveil the behavior of matter and light in space-time in the strong-field gravity regime. The third objective is to discover the astrophysical and physical mysteries of the strongest magnetic fields in the universe. Extensive observations, timing, polarimetry, and spectroscopy of X-rays coming from deep space are vital to achieve the above-mentioned goals. The eXTP mission, by employing various techniques, methods, and instruments, will continuously examine the X/ɤ-rays coming from the sky in order to achieve its goals [7]. X/ɤ-rays spectroscopy and imaging are two such prominent and essential techniques, which also find applications in other fields, such as biomedical devices and material science. The detail of X/ɤ-rays spectroscopy and imaging is part of section 3 of this chapter. The Silicon Drift- Detector (SDD) is one of the best electronic devices used to achieve X/ɤ-rays spectroscopy and imaging. The description of SDD is part of section 1.4 of this chapter. Specially designed multi-channel Application-Specific-Integrated-Circuits (ASICs) are indispensable for a reliable and successful read-out of the signals coming from the SDDs. The details of these ASICs are included in section 1.5 and 1.6. Being a core part of such ASICs, the relevant description of the ADCs – primary goal of this thesis- is part of section 1.7.

1.2. Significance of Small Satellites for Space Applications

All space missions are accomplished with the help of satellites. As opposed to conventional large satellites with heavy payloads, the use of the small satellites (nanosatellites, pico-satellites, femto-satellites, CubeSat) for space applications and missions has become attractive these days because of their plethora of functional advantages over large satellites. Firstly, they are more compact and low-profile than large satellites, and thus occupy a small area. This results in not only their easier and convenient launching and management, but also reduced coupling problems with the satellite launch system. Secondly, they consume less power, and therefore they are power efficient. Thirdly, they are cost-effective with respect to their design, fabrication, testing, and launching overheads, and hence affordable for the small companies, research institutes, and even universities. Fourthly, they have a shorter start-to-launch cycle, which results in a rapid launch period with a high launch success-rate in comparison with the large satellites. Fifthly, they are a better candidate for performing extra functions than large satellites because of their miniaturization, power-efficiency, and cost-effectiveness. Sixthly, they open a door for the implementation of the satellite clusters because of the aforementioned advantages, and therefore promise potential for novel applications. Finally, their potential and growth have enhanced enormously owing to the recent colossal technological advancements in Integrated Circuits (ICs), fabrication processes, and digital signal processing methods. The above-mentioned advantages have made them attractive choice for variety of application areas, such as earth's remote sensing, scientific missions, radar sensing, surveillance, land deformation detection, weather forecasting, and security [8]. Because of the aforementioned advantages, mainstream modern space missions are carried out using small satellites. For example, the HERMES mission [3] uses nanosatellite [9]. Also, the eXTP space mission will use a small satellite [10]. Figure 1.1 shows an example of a small satellite with some of its core components.

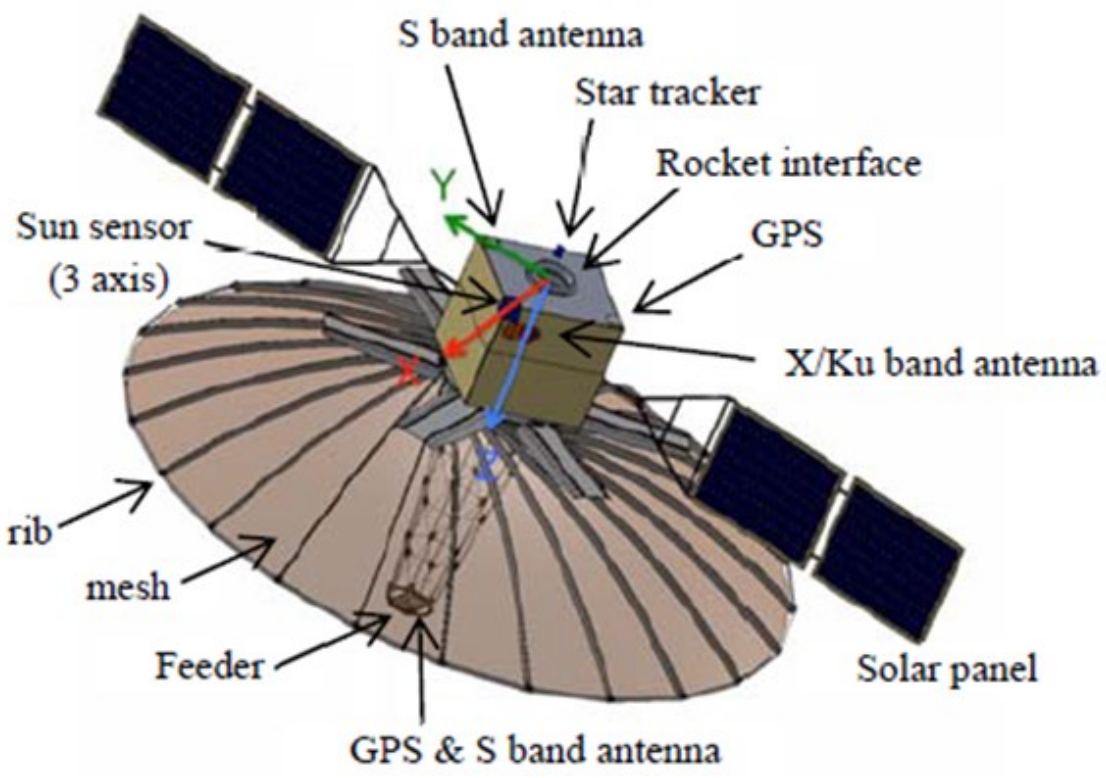

Figure 1. 1. A small satellite with some of its on-board core components [8].

1.3. Spectroscopy and Imaging Technologies for Space Applications

X/ɤ-rays spectroscopy and imaging are the core technologies for space missions. In X/ɤ-rays spectroscopy and imaging, the energy spectrum of the incident radiations (X/ɤ-rays) is determined. By analyzing and processing the energy spectrum, substantial information related to the radiation sources (X/ɤ-rays) can be achieved. For example, the evaluation and identification of the levels of different peaks in the energy spectrum is one of the key techniques to gather data relevant to the radiation sources. Example of one such energy spectrum plot is shown in Figure 1.2. However, an accurate discrimination of different peaks in the energy spectrum plot is quite a challenging task, since it requires a spectroscopic instrument with a good energy resolution. Electronic noise - a dominant noise source, especially in space environment, is a big obstacle in getting good energy resolution-based spectroscopy.

The two key performance metrics for the spectroscopy are Equivalent Noise Charge (ENC) and Full Width Half maximum (FWHM). Following equation shows relationship between these two parameters:

$$\mathrm{ENC} = \mathrm{C} \times \mathrm{FWHM} \tag{1.1}$$

Where C is a constant, whose value depends on the SDD material. For Silicon (Si), the value of C is 0.115 $e^{-}_{rms}/_{eV}$. Also,

$$\mathrm{FWHM}_{@\mathrm{Energy}} = \sqrt{\frac{\mathrm{ENC}^2}{\mathrm{C}^2} + \mathrm{FWHM}^2_{\mathrm{Fan0}}}$$

where,

$$\mathrm{FWHM}_{\mathrm{Fano}} = 1.55\sqrt{\mathrm{Energy}}\ \ [\mathrm{ev}]$$

Thus,

$$\mathrm{FWHM}_{@\mathrm{Energy}} = 119\ \mathrm{eV}\ @\ 5.9\ \mathrm{keV}\ \mathrm{in\ Si} \tag{1.2}$$

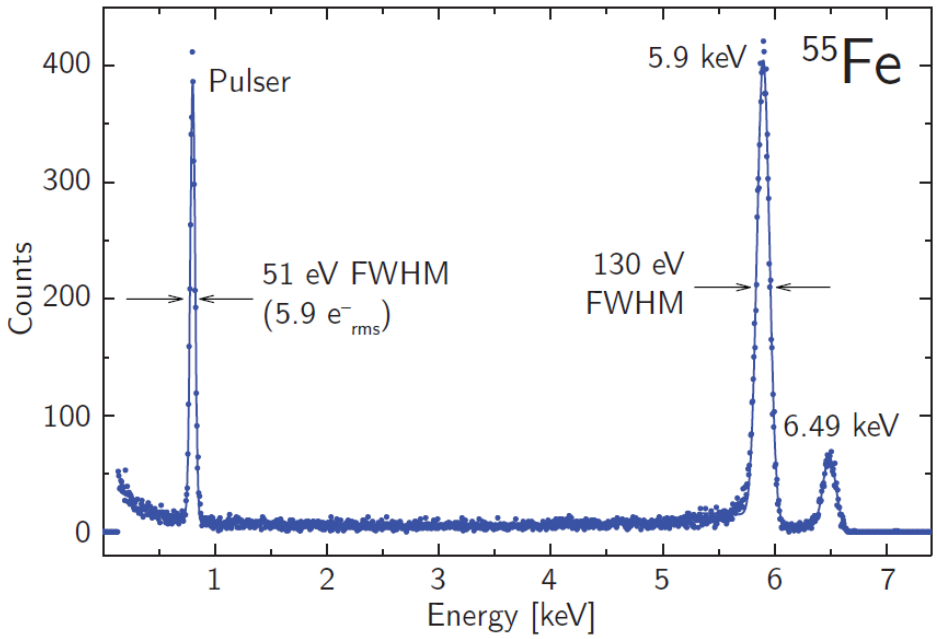

Figure 1. 2. Example of an energy spectrum graph for X/ɤ-rays spectroscopy applications [11].

1.4. The Use of Silicon Drift Detectors (SDDs) for Spectroscopy and Imaging

Generally, the systems and components onboard a small satellite for space missions can be divided into five categories: mechanical structure, electronic power system, flight controller, payload, and wireless communication system [8]. Besides other devices, wide-area spectroscopic detectors are an essential part of the satellite payload. X/ɤ-rays spectroscopy and imaging are performed by these detectors. In addition, these detectors are read-out by dedicated ASICs.

Several types of detectors are utilized for X/ɤ-rays spectroscopy. Some of these include Photodiodes, Silicon Drift Detectors (SDDs), Silicon Strip Detectors, Silicon Photomultipliers, and Photomultiplier tubes [12]. First invented in 1984, the SDDs are, however, the most auspicious candidate among these for space applications and offer several advantages. For example, they have a very small anode size. This leads to small anode capacitance (< ~ 40 fF). As a result, they exhibit very low noise performance. In addition, their structure and working principle make them attractive for an easy and hassle-free connection with the ASICs. Actually, the electrons, produced as a result of the incident photon interaction with the silicon, drift towards the anode of the SDDs. The anode of the SDDs can be connected with the read-out ASICs in such a way that reduces the parasitics, and thus enhances performance. For example, the front-end section of the ASICs can be placed very close to the anode of the SDD and can be connected by either bump or wire-bonding, thus ensuring lesser interconnects parasitics [9]. Moreover, they are cost-effective with respect to their manufacturing technology. Furthermore, they exhibit high energy resolution properties [13]. Additionally, they possess high quantum efficiency than the other similar detectors [12]. Because of these advantages, SDDs are a highly attractive choice for contemporary space missions.

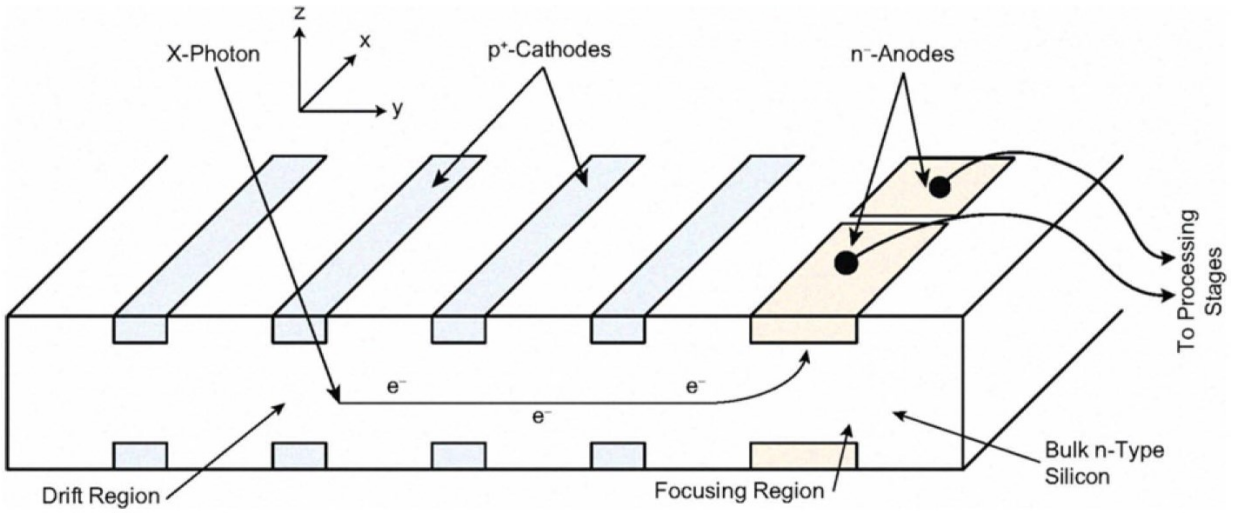

Figure 1. 3. Simple structure of an SDD [13].

1.4.1. Basic working principle of Silicon Drift Detectors (SDDs)

Figure 1.3 shows a simplified version of a typical SDD structure. It consists of a number of cathodes (p^+implants) on both sides of the silicon chip and couple of small anodes (n^+implants) located at the edge of the chip. The anodes are connected to the following processing stages, i.e., readout ASICs. In fact, the charge sensitive low noise preamplifier is the first component of the following ASIC connected with these anodes. As the capacitance of the detector is small because of the anodes' small readout geometry, the series electronic noise of the preamplifier does not contribute as much to the overall performance of the detection system as it does when used with the other large capacitance detectors. This in turn results in a high energy resolution of the system. As the incoming radiations (e.g., X/ɤ-rays) arrive at the detector, they are converted into electron-hole pairs. Because of the traversal electric field, the electrons drift towards anodes where they are collected. The horizontal (x) coordinates and vertical (y) coordinates of the incident radiations can be determined: x-coordinate are provided by the position of the anodes, and y-coordinates

are determined with the help of the drift time of the electrons. Therefore, the SDDs are capable of reconstructing the spatial position of the incident radiation in the plane (x and y coordinates). This enables the use of the linear array of the front-end electronic circuits to read-out the information, unlike the conventional pixel detectors which necessitate the matrix form front-end circuits. Consequently, the complexity level and power consumption of the entire detection system is reduced substantially [13]. Important parameters and specifications of SDDs include composition, pixel pitch, pixel size, array size, energy range, leakage current, detector capacitance, and bump/wire-bonded capacitance. The selection criteria for these values for the design of an SDD depends on the application area of the SDD.

1.5. Read-Out ASICs for Silicon Drift Detectors (SDDs)

As mentioned in section 1.4, the detector converts the incident radiation into electron-hole pair and electrons are collected on the anodes of the detector. Thus, the output signal at the anodes is in the form of a current pulse. Extracting useful information from this pulse is not possible without its further processing. Therefore, a read-out ASIC is needed for further processing [13]. There are two approaches which are employed for processing of current pulse: first is digital pulse processing, and second is analog pulse processing. Figure 1.4 shows a conceptual representation of these two approaches with output signal at different stages for a single-channel ASIC version. The ADC design requirements – main focus of this thesis - for both the solutions are quite different. For digital pulse processing solution, a fast ADC, with a typical sampling-rate of more than 100 MS/s, is required. The ADC with such a high sampling-rate essentially consumes significant power. In addition, such an ADC is highly likely to face crosstalk and interference issues because of exhibiting high switching noise caused by the use of external high-speed clock signals. The analog pulse processing solution, on the other hand, needs a slow ADC, with a typical sampling-rate of less than 10

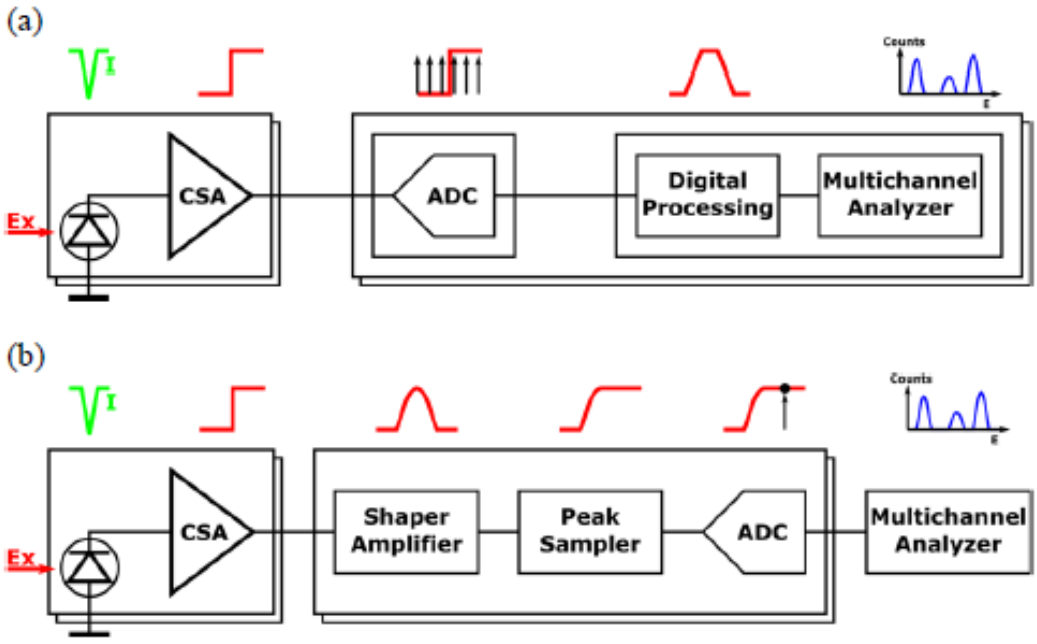

Figure 1. 4. Schematic view of two different readout chains for Silicon Drift Detectors: (a) Digital Readout Chain (DRC) and (b) Analog Readout Chain (ARC) [14].

MS/s, thus avoiding the issues faced by the high-speed ADC [15]. For the eXTP mission and for this thesis, the analog pulse processing approach has been chosen, and thus a slow ADC is adequate to serve the purpose.

Figure 1.5 shows a simple block diagram of a typical single-channel analog pulse processing readout ASIC for processing SDD output signal with the waveforms at different stages. The ASIC consists of three different sections: analog front-end, ADC, and digital processing. The analog front-end receives the current impulse from the output of the SDD and converts it into a voltage pulse shape after processing with the help of different processing blocks. This voltage pulse is then digitized using an ADC. The converted digital signal goes to the digital processing block which, with the help of digital signal processing techniques and algorithms, extracts required information from the signal.

Figure 1.6 shows a simple block level diagram of the typical analog front-end section of an ASIC for space application. A brief description of the functionality of each component of the front-end section is useful and therefore provided below:

1.5.1. Charge Sensitive Amplifier

It converts the charge signal or current impulse signal, coming from the output of the SDD, into a voltage.

1.5.2. Shaper

As the signal-to-noise ratio at the output of the charge sensitive amplifier is low, the shaper or shaping amplifier performs linear amplification as well as filtering of the signal to enhance its signal-to-noise ratio.

1.5.3. DC Stabilizer

It reduces the shift and fluctuation in the baseline of the signal which might happen because of the thermal drift and temperature variations, variable input rate, and non-linearity effects of the components. It does so by ensuring AC coupling between shaper output and the following stages.

1.5.4. Peak Stretcher

Peak stretcher performs two functions to the shaper output signal in its two different states: it behaves as a follower during the rising edge of the shaper signal; while it acts as a peak/amplitude detector of the shaper output when shaper output signal's amplitude reaches at its peak.

1.5.5. Amplitude Discriminator

It discriminates the shaper output signal by comparing it with a given threshold level. It provides a high-level signal at its output if the shaper output signal exceeds the threshold, else it gives low level signal.

1.5.6. Peak Discriminator

It acts as a discriminator for the peak of the shaper output signal. It returns a high-level signal at its output only when the peak of the shaper output signal is reached.

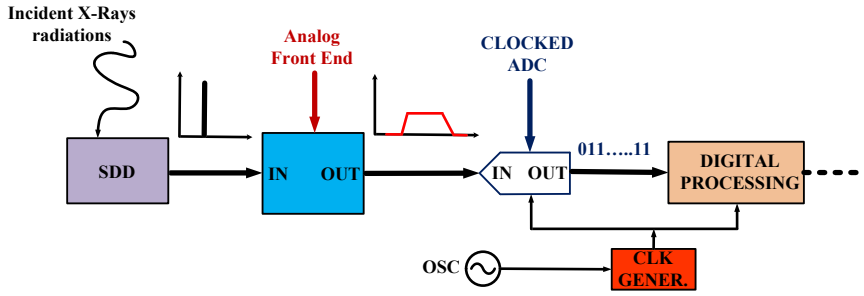

Figure 1. 5. CMOS readout ASIC for space applications: a simple illustration using only one channel.

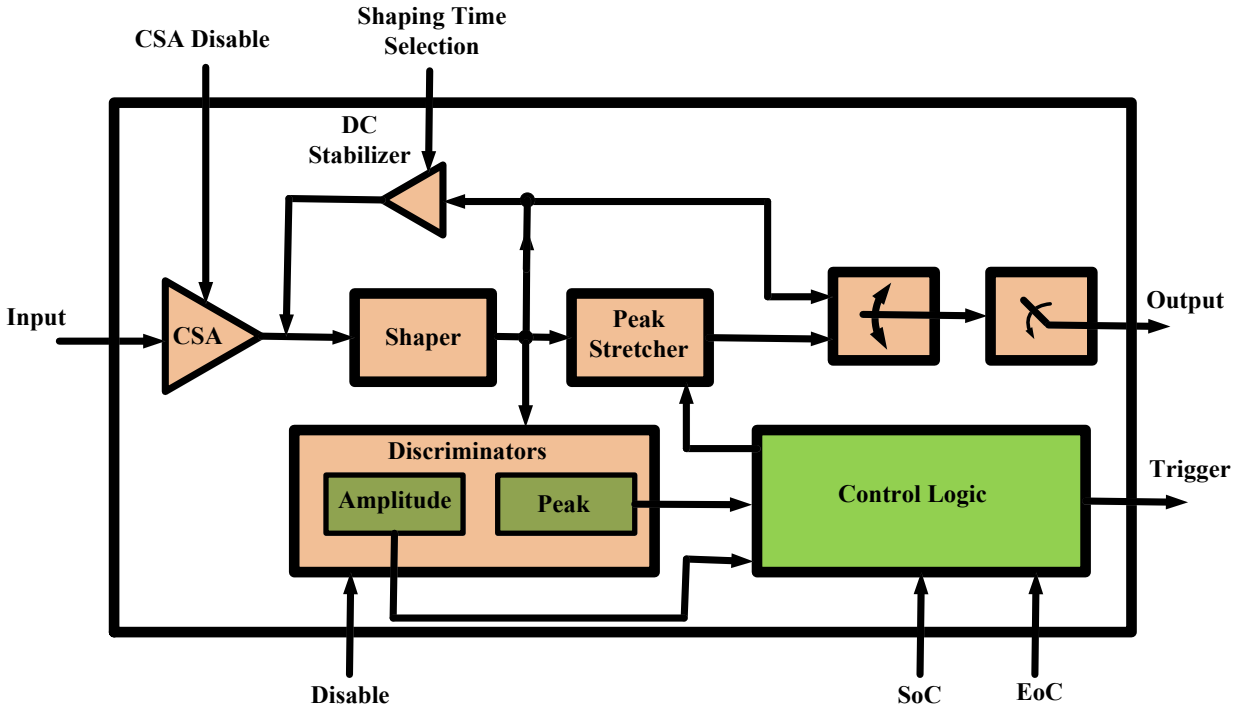

Figure 1. 6. CMOS read-out ASIC for space applications: important components of the analog front-end section.

1.5.7. Why Fully Integrated CMOS-based Read-Out ASICs for Silicon Drift Detectors (SDDs)?

Generally, the ASIC solutions for space applications proposed in the literature belong to a category where only an analog front-end section is on the chip, while the remaining sections (ADC and digital) are outside the ASIC chip. This strategy is, obviously, unfavorable for the instrument miniaturization, cost, weight, and power. This calls for an alternative approach which must ensure compact, low-cost, low-weight, and low-power functionality. The highly preferred alternative is integration of all the sections (analog front-end, ADCs, and digital) of the ASICs in a single chip. This makes the CMOS an attractive technology choice for the design of such ASICs because of its high integration, low-profile, cost-effectiveness, and power-efficiency based advantages. However, the integration of CMOS-based ASIC's all sections offer several challenges, whose detail is provided in section 1.6. Figure 1.7 depicts a conceptual illustration of all the sections of readout ASICs on a single chip with SDD connections.

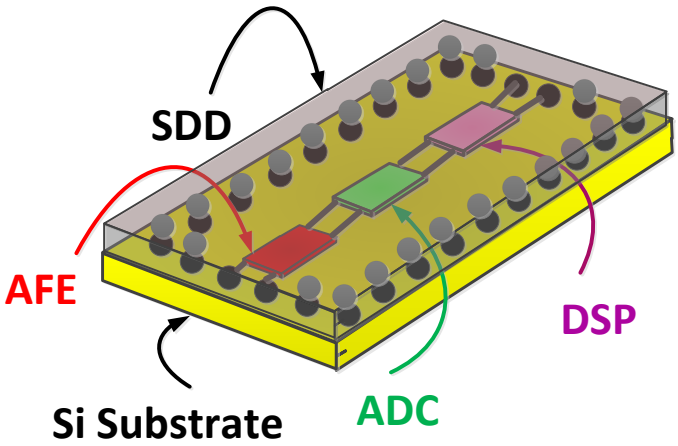

Figure 1. 7. Pictorial representation of all components of ASIC for space application on a single chip/substrate; in this example, the ASIC is wire-bonded with the multi-anode SDD.

1.6. Multi-Channel CMOS ASICs for Space Applications: Working Principle, Requirements and Challenges

Instead of single channels, multi-channel CMOS ASICs are employed to accommodate a large number of SDDs to maximize radiation acquiring from space. As the signal (radiations from space for space applications) coming from space have similar characteristics, it is highly advantageous to employ multi-channel solutions. In addition, multi-channel solutions can be cost-effective, compact, and power-efficient in CMOS technology. Figures 1.8, 1.9, and 1.10 depict simple conceptual diagrams for multi-channel ASICs for space applications in three widely used approaches with respect to the use of ADCs. Although an emerging trend of utilizing a greater number of channels in such read-out ASICs has been witnessed recently, which is likely to grow further in the near future going up-to 1024 channels and more, only 64 channels have been shown in all three figures for the sake of simplicity.

Figure 1.8 shows the first arrangement, where a single ADC is employed per ASIC channel. This approach requires a relatively low-speed (< 1 MS/s sampling-rate) ADC. This results in a better energy-efficiency per ADC. However, the use of one ADC per channel translates into a significant overall power, area, and cost of the chip. In addition, the probability of crosstalk issues between the ADCs is high. Moreover, clock synchronization and distribution to the ADC is a critical issue for this configuration. The second approach is the opposite of the first approach where only one ADC is utilized for managing the signals for all channels. Figure 1.9 illustrates a conceptual representation of this approach. The ADC here needs to be high-speed to be able to manage signals of all the channels. This leads to an ADC with significant power consumption. However, the area, cost, crosstalk, and clock synchronization issues are relaxed for this approach in comparison with the first approach. The use of a single ADC for a few numbers of channels in the ASIC is the third possible approach, which is depicted in Figure 1.10. Keeping in view the number of ADCs, this approach lies in the middle of the above-mentioned two approaches. The ADCs in this case need to have low-to-moderate conversion-rates. The design parameters and challenges such as area, power, crosstalk, and clock synchronization also lie in the middle of the above-mentioned two solutions.

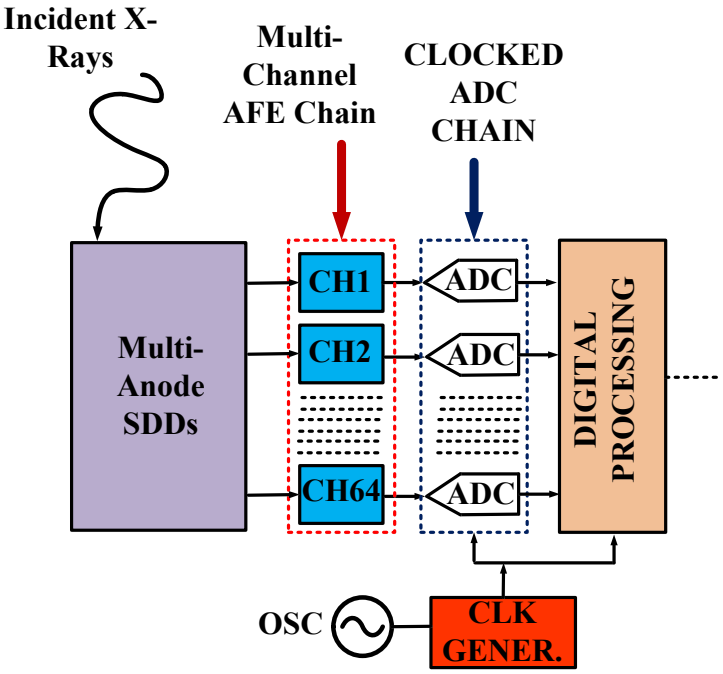

Figure 1. 8. Multi-channel CMOS read-out ASIC for space applications: example of case where a single ADC is being employed per channel.

Besides various conspicuous advantages, the large number of channels triggers a stringent set of requirements for the read-out ASICs. First, they should consume low power. Second, they must occupy a small chip-area. Third, they must ensure low-noise. Fourth, mitigation of crosstalk and interference between the analog and digital sections of such ASICs is of significance importance. Keeping in view the focus of this thesis on ADC design, section 1.7 provides a detailed description of the ADC design challenges in context of multi-channel ASICs for space applications.

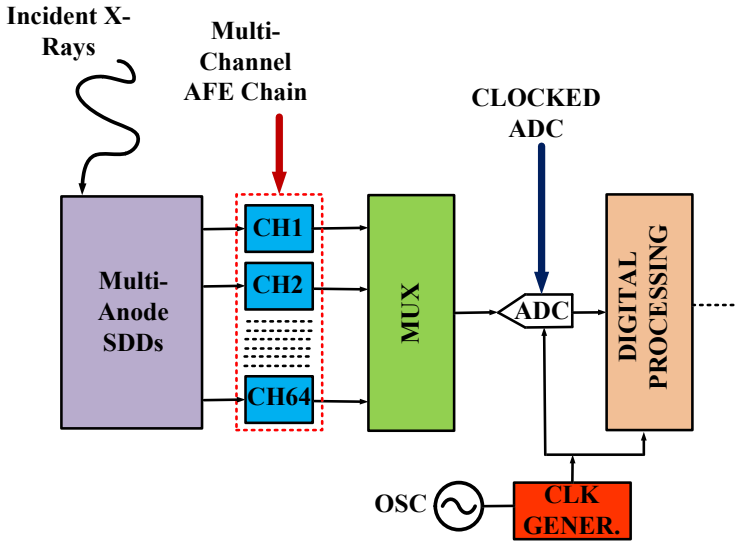

Figure 1. 9. Multi-channel CMOS read-out ASIC for space applications: example of the case where only single ADC is being used for all ASIC channels.

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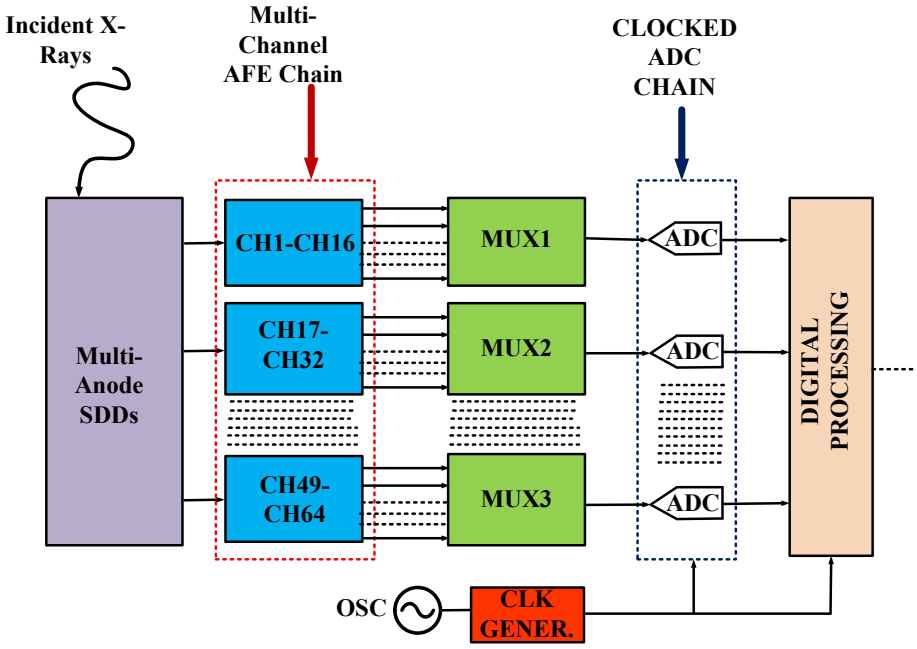


Figure 1. 10. Multi-channel CMOS read-out ASIC for space applications: example of the case where multiple ADCs are being utilized for managing signals coming from a particular set of ASIC channels.

1.7. ADCs for Multi-channel CMOS ASICs for Space Applications: Requirements, Challenges, and Specifications

Analog-to-Digital Converters (ADCs) are an essential part of these multi-channel ASICs. Usually, multiple ADCs are part of such ASICs. There are three major solutions for carrying out the analog-to-digital conversion of the analog data for multichannel ASICs for space application. First, the use of a small number of ADCs (one ADC in extreme case) operating at a very high-speed which serves the whole ASIC analog channels, as shown in Figure 1.8. Second, the employability of a large number of slow and simple ADCs, each serving a small subset of analog channels (16) [16], as shown in Figure 1.10. Third, the utilization of one ADC per channel, as shown in Figure 1.9. Each of these solutions has its own requirements, challenges, and tradeoffs. This leads to a diverse set of specifications for these ADCs besides the ones mentioned in section 1.6. A brief detail of important specifications is provided below.

1.7.1. Sufficient Large Conversion Speed

There is a growing trend in utilizing a large number of channels for space applications-based read-out ASICs. The ASICs with 1024 channels [17] have already been proposed, and this trend is likely to flourish with the passage of time. A large number of channels require ADCs to possess a sufficiently large conversion speed to be able to perform conversion of the signals coming from all the channels.

1.7.2. Adaptable Conversion Speed accompanied with adjustable power consumption

The radiations (X/ɤ-rays) in space are of sporadic nature, unlike other several applications where a continuous flow of signals is maintained, like ECG signals. Their influx ranges from large bursts of X/ɤ-rays' events to a few or no events at all. This variable and erratic radiation-flux to the SDDs demands read-out ASICs, including the ADC, to act according to the event-rate to save power. The ADC, thus, must have an adaptable conversion speed: lower conversion-rate in presence of few/less events, and high conversion rate in case of burst of events. The power consumption of the ADC should be proportional to its conversion speed for an optimized conversion-efficiency.

1.7.3. Low-Switching Noise

Crosstalk and interference are two key design challenges for read-out ASICs for any application. In the context of space applications, they become even more critical because of the large number of channels [17]. There are two types of crosstalk and interference: one between the analog and digital sections of the ASIC, and second among different channels. To get a good performance, mitigation of both of these sources is necessary. This requires a minimization of the switching-noise in the ASIC. Among other reasons, the primary cause of high switching-noise in these ASICs is external high-frequency clock signals. As shown in Figure 1.8, the ADCs need external high-frequency clock signals. In particular, the distribution of the external high-frequency clock signals among different ADCs leads to high switching-noise, and thus crosstalk issues. Special techniques are essential to lower the switching-noise to abate the crosstalk issues. A promising solution is to use an asynchronous or self-clocked ADC, which is able to generate all the high-frequency clock signals internally. This removes the need for any external high-frequency clock signals and their distributions all together, which results in low switching-noise and crosstalk issues.

1.7.4. Clock Jitter and Synchronization Issues

Besides high-switching noise caused by the external high-frequency clock signals to the ADCs, clock jitter and synchronization are other prominent design issues. Because of the large number of channels, the clock distribution to all the ADCs may result in clock jitter and asynchronization because of the parasitics associated with the long interconnects used for the clock distribution. This results in ADC performance degradation. Thus, special care and design techniques are essential to make ADC performance impervious to the issues caused by the clock ill-synchronization/jitter and distribution among the different channels. One best way to avoid these issues is to employ a set of asynchronous or self-clocked ADCs.

1.7.5. Activity-Driven Operation

As the radiation at the input of the SDD is sparse, each channel of the analog front-end utilizes a threshold detector to decide whether the incoming signal coming from the SDD is worth considering or not. Only if the signal is above the threshold value, the analog front-end alerts the relevant ADC to make a conversion. This requires the ADC to be an event-triggered or activity-driven design, i.e., it should perform conversions only when an activity or event has occurred, i.e., when intimated by the analog front-end; otherwise, it should remain idle to save its power.

1.7.6. Radiation-Hardened Design

Space is characterized by harsh environmental conditions with the presence of abundant sources of radiation, rays, etc. As a result, the ASIC including the ADC, for space applications should be capable to tolerate such harsh environments. Typical effects associated with space harsh conditions on the performance of the ASIC as well as ADC include Total Ionizing Doze (TID), Single Events Effects (SEEs), and Displacement Damage [18-21]. Besides degrading ASIC performance, these effects can permanently damage the devices.

1.7.7. Memory as well as Memory-Less Operation

In multi-channel ASIC or multi-sensor applications, the ADC can be utilized in two ways: first, it can be used for the conversion of the signals coming from a single channel or sensor; second, it can be utilized for converting signals coming from multiple channels or sensors. In the first method, the ADC is not necessarily required to be reset after the conversion of a particular set of signal samples coming from the channel or sensor. In other words, the ADC does not need to have memory-less operation. It is because the signal coming to the ADC is from the same sensor or channel, so correlation of the signals does not affect ADC accuracy. In the second approach, the ADC needs to be reset after conversion of a certain number of samples, i.e., after converting signal coming from a particular sensor or channel and before starting conversion of signal coming from another sensor or channel. Alternatively, the ADC is required to exhibit memory-less operation in order to maintain its accuracy against correlation of signals from different sensors or channels. The choice of using the ADC in memory or memory less approach depends on the desired application. However, it is highly preferred to have an ADC capable of functioning in both the modes (memory or memory-less) to achieve great flexibility and versatility in the design.

Table 1. 1. Specifications of the read-out ASIC for the eXTP space mission [11]

Sr. No.	Parameter	Value
1.	Input Photon energy range (keV)	60
2.	Electronic noise/input referred noise (e^-_{rms})	~ 12
3.	Power budget (mW)	1/channel
4.	Linearity (%)	± 2
5.	detector Leakage current (nA)	1
6.	No. of Channels	32*
7.	Peaking Time (µs)	3.6
8.	Detector Capacitance (fF)	< 40
9.	event-rate	~$10^5/sec$

* Initially at prototype stage.

1.8. Objectives and Motivations of the Thesis

The objective of this thesis is to propose and design Analog-to-Digital Converters (ADCs) suitable for spectroscopic multi-channel CMOS read-out ASICs for space applications. In this regard, the thesis is aimed at:

1. Investigating the merits and demerits of the potential ADC architectures and topologies for space applications

2. Reviewing the state-of-the-art of the ADCs for the space applications

3. Proposing novel and versatile ADC architectures, which can function as promising candidates not only for the space applications, but also other important relevant applications such as biomedical implants

4. Designing the proposed ADCs architectures in CMOS technology and getting them fabricated

5. Testing the fabricated ADCs to evaluate their performance

1.8.1. ADC Specifications

Although overall objective of the thesis is to come up with the ADC solutions which are suitable for broad range of space as well as other relevant applications, the multichannel read-out ASIC for the eXTP space mission [6, 7] has been selected as a benchmark to derive ADC targeted specifications for this thesis. Main specifications of the read-out ASIC for the eXTP space mission are provided in Table 1.1. Table 1.2 shows the targeted specifications for the ADCs to be proposed. The rationale behind each targeted parameter and specification of the ADC is provided below.

1.8.1.1. Technology Process

Austria Micro System (AMS) 0.35 µm CMOS process has been chosen for the design of the eXTP mission ASIC and thus ADCs. This technology offers four metal layers, two polysilicon layers, and high resistivity poly (1.2 kΩ/□). A range of factors come into play when it comes to the technology selection for an ASIC design and same is the case for the eXTP mission ASIC design, including the ADCs. The first crucial factor is the fact that this technology has a proven record of successful ASIC functions for several space missions. Some of these missions include 'The Large Observatory For X-ray Timing (LOFT)' [1] [2], 'High Energy Rapid Modular Ensemble of Satellites (HERMES)' [3], 'Transient High Energy Sky and Early Universe Surveyor (THESEUS)' [4], and 'A Large Ion Collider Experiment (ALICE)' [5].

The second reason is that the design implemented in this technology is robust enough to pass through the radiations' effects-a necessary requirement in the space environment. This has been validated by performing the necessary experimental tests on 'RIGEL' ASIC design in 0.35 µm CMOS process. These tests measured latch-up events, single events upsets, and total ionizing dose effects. The experiments were performed by mimicking the orbital environment/space conditions. As per the outcome of these experiments, the ASIC is safe for functioning in space environment without any additional dedicated protection mechanism or methodology [22, 23].

The third reason behind this technology selection is that this technology has a better noise performance which is highly beneficial to get low-noise analog front-end section of the ASIC. This is because of the low noise features of the MOSFETS of this technology [11]. In addition, the design criteria to minimize the noise for the circuits (such as amplifier) designed in this technology have been derived [24]. The low-noise characteristics aspect of the MOSFET of this technology is especially attractive for the low-noise design of the charge sensitive preamplifier – the first and most critical component of the analog front-end section of the ASIC.

Finally, the design cost of the technology is lower than the advanced technology nodes. Just an example, the fabrication cost of a same sized ASIC in a 0.35 µm CMOS process is approximately ten times lower than in 28 nm CMOS process.

1.8.1.2. Resolution/Effective-Number-of-Bits (ENOB)

The resolution of the ADC depends on the requirements of the spectral resolution of the SDDs, which is related to the noise requirements of the SDDs as well as accompanied ASICs. In addition, it depends on the range of the energy of the incident photons/X-rays at the input of the SDDs. Assuming a photon energy

range of 500 eV-20 keV for the SDDs, the full-scale dynamic range becomes approximately equal to 20 keV. Assuming a reasonable spectral resolution requirement of the full-scale range leads to the need of an ADC with a resolution of 9 bits. For the eXTP mission, the targeted typical resolution requirements for the ADC are 10-12 bits.

1.8.1.3. Bandwidth

As the input to the ADC is a DC signal as shown in Figure 1.5, the bandwidth is dictated by the conversion time of the ASIC**.** A small or large conversion time does have its own pros. and cons. A typical conversion time of 25 μs is chosen initially which corresponds to a sampling-rate of 40 kHz and Nyquist bandwidth of 20 kHz. However, a key design focus is to get an adaptable conversion time-based ADC with adjustable power consumption. This will automatically lead to a bandwidth reconfigurable ADC design. This adds flexibility to the ADC with respect to the decision on whether to use a small number of ADCs for the entire multichannel ASIC or considerable number of ADCs serving some sub-channels of the ASICs.

1.8.1.4. Differential Non-Linearity (DNL), Integral Non-Linearity (INL), and Total Harmonic Distortion (THD)

DNL and INL are ADC specification parameters, which are used to measure its static characteristics. These parameters dictate the linearity requirements of the ADC. For the target application, DNL and INL should be lesser than or equal to 2 Least Significant Bits (LSBs). Total harmonic distortion measures the power of harmonics in the spectrum of the ADC. It is a dynamic parameter and is measured from Power Spectral Density(PSD) plot of the ADC. For the target application, a THD of 0.2 % is adequate.

1.8.1.5. Sampling-rate (f_s)

The sampling-rate of the ADC is contingent directly on the bandwidth requirements, which in turn dictated by the conversion time requirements as described in section 1.8.1.3. As per the Nyquist criteria, the sampling-rate of an ADC must be twice its bandwidth. 20 kHz being a typical bandwidth of the ADC, a sampling-rate of 40 kHz is chosen as per this criterion.

However, sampling-rate reconfigurability is highly beneficial for the application as described in section1.8.1.3 of this chapter, an ADC design which is capable of sampling-rate reconfigurability functionality with a proportionate power consumption and thus energy-efficiency is the primary target.

1.8.1.6. Signal-to-noise-and-distortion-ration (SNDR)

Signal-to-noise-and-distortion-ratio of an ADC is related to its ENOB by following well-known relationship:

$$\mathrm{ENOB} = \frac{(\mathrm{SNDR\ (dB)} - 1.76)}{6.02}$$

With ENOB requirements of 10-12 bits, the resulting targeted SNDR becomes 62-74 dB.

1.8.1.7. Power Consumption

High spectral resolution is the primary requirement for the SDDs for the eXTP and other space missions. This cannot be achieved without sufficiently low-noise read-out ASICs for the SDDs. Low-noise ASICs design is directly proportional to their power consumption. For one channel of the eXTP ASIC, a power budget of approximately 1 mW has been allocated. Half of this budget is reserved for the analog front-end section. Out of the remaining 0.5 mW, the majority of the power budget can be reserved for the ADC design in order to be able to get high performance, i.e., required spectral resolution from the instrument.

1.8.1.8. Input Signal Swing

Because of the use of a 3.3 V supply voltage, it is highly incentivized to make use of the largest input signal swing which is achievable with a single-ended ADC architecture. Besides the targeted application, this will also make the ADC an attractive choice for a multitude of emerging applications. Thus, an input signal

swing of 2V, ranging from 0.65 V to 2.65 V centered around 1.65 V, has been chosen. 1.65 V is the common mode voltage (VCM) or analog ground (AGND) of the ADC. It is half of the supply voltage. As the majority of the analog front ends make use of half of the supply voltage as an analog ground, the selection of 1.65 V for the ADC can be beneficial in a way that it saves the need of a separate analog ground for the ADC.

1.8.1.9. Supply Voltage

3.3 V has been chosen as a supply voltage for the eXTP analog front-end design. As a result, the same supply voltage is also selected for the design of the analog and digital sections of the ADC. However, the use of lower supply voltage (e.g., 1.65 V or 1.2 V) for the design of the digital sections of the ADC is also an open avenue to explore the advantage in terms of power consumption. The design of the analog section of the ADC is not possible at a lower supply voltage because of the large input signal swing requirements as mentioned below.

Another reason for selecting 3.3 V as a supply voltage is to accommodate a large input signal swing to make the ADC insensitive to crosstalk and interference issues. It is well-known that crosstalk and interference are unavoidable in any multi-channel or multi-sensor applications and degrade the performance significantly. One of the effective ways to reduce these issues is to use high input signal swing. This obviously requires the use of a high supply voltage for the design. Just as an example, the design at a 3.3 V is more robust with respect to the crosstalk and interferences issues than a design at 1.2 V in a multi-channel or multi-sensor applications.

1.8.1.10. Offset Error and Gain Mismatch

For the targeted application, offset error and gain mismatch are not a problem at all since they can be tackled at the system level. However, both of these must be temperature insensitive. The reason is obvious: the design is intended for space application where a huge temperature variation is a normality. The change in the offset or gain of the ADC with temperature variations simply means its performance degradation, and as a result overall ASIC.

1.8.1.11. Single-ended vs. Differential Architecture

As the output coming from the eXTP analog front-end is single-ended, a single-ended ADC topology is the logical choice. In addition, it saves chip-area, power, and cost of the design in comparison with differential implementation. Moreover, it reduces the load to the preceding stage of the ADC.

1.8.1.12. Special Techniques for Radiation-hardened operation?

Usually, the ADCs for space applications should be equipped with the methods and techniques for not only withstanding the radiation impacts on their performance, but also avoiding any damage. However, no such special technique is considered for the design of the targeted ADCs because of two main reasons. First, the instruments on-board a satellite are protected from the harsh environmental and radiation effects of the space by special packages. Being part of the instrument, all the SDDs, ASICs, and ADCs are safeguarded this way. Second, previous experimental studies demonstrate [22, 23] that the ASICs, including the ADCs, designed in a 0.35 μm CMOS process pass all the radiation tests necessary to function in space condition without a need of any special protecting scheme.

1.9. Thesis Outline

The rest of the thesis is organized as follows: Background study and comprehensive literature review of the ADCs is part of chapter 2. Chapter 3 is devoted to the description of step-by-step design process of the first proposed ADC architecture, i.e., 8-bit Asynchronous SAR (ASAR) ADC with its simulation and measurement results. Details of the design, simulation, and measurement results of the second proposed ADC, i.e., dual-mode Noise-Shaping (NS) SAR ADC is part of chapter 4. The thesis ends with a brief description of the conclusions, contributions, and some future directions in chapter 5.

Table 1. 2. Targeted specifications of the ADC

Parameter/Specifications	**Value**
Technology Process (μm)	AMS 0.35
Resolution (Bits)	10-12
Typical Bandwidth (kHz)	20
ENOB (Bits)	10-12
DNL (LSB)	≤ 2
INL (LSB)	≤ 2
THD (%)	0.2
Typical $f_s(kHz)$	40
SFDR (%)	0.1
SNDR (dB)	62-72
P_{cons} (μW)	As low as possible
Input Signal Swing (V)	0.65-2.65 centered at 1.65 V
Supply (V)	3.3
Offset error	Temperature-insensitive
Gain Mismatch	Temperature-insensitive
Architecture	Single-ended
Special Techniques for Radiation-hardened operation?	No

Chapter 2

BACKGROUND STUDY AND LITERATURE REVIEW

Chapter Abstract

This chapter is devoted to a brief background study and an extensive literature review of Analog-to-Digital-Converters (ADCs). The chapter starts with a description of requirements, and specification parameters of ADCs, followed by a brief overview of ADCs architectures and topologies with a mention of pros. and cons. of each topology. The prior state-of-the-art ADC solutions for space applications is part of section 2.3. Section 2.4 provides a comprehensive literature review of the selected ADC types for this thesis, i.e., Asynchronous SAR (ASAR) and Noise-Shaping SAR (NS-SAR) ADCs.

2.1. Requirements of Analog-to-Digital Converters (ADCs)

Digital circuits have witnessed unprecedented progress over the last 50 years, owing to a relentless optimization of semiconductor technology processes to reduce the size, cost, and power consumption. This tremendous advancement in digital circuits (e.g., microprocessors) and processing has revolutionized the world by enabling a plethora of innovative applications and functions. Emergence of artificial intelligence [25-27], augmented reality [28], metaverse [29], machine learning [30], internet-of-things [31-33], wireless sensor networks [34, 35], 5G and beyond wireless technologies and systems [36-39], biomedical implants devices [40], autonomous and unmanned aerial vehicles, smart buildings [41] and city, space field and satellite sector, and smart grid are just a few such application areas and functions. As all these applications unavoidably have to deal with the real-world signals which are analog, the use of the digital signal processing is not possible without converting the real-world analog signals into digital. Thus, there is simply no way to utilize powerful digital signal processing without analog-to-digital conversion. Analog-to-Digital Converters (ADCs) are the components which perform analog-to-digital conversion. Thus, ADCs play a vital role in the modern technology-based world. ADCs can be considered as bridges between the analog world and the digital world. Like the real-world bridges on the roads, ADCs often become bottlenecks and their design is crucial for the success of the overall electronic system.

Figure 2.1. shows the conceptual representation of an ideal ADC with its working. The input to the ADC is a sine wave signal, which can either be arriving from the output of an analog front-end circuit in case of an integrated system or from a signal generator in case of a stand-alone ADC. The ADC digitizes this signal in two steps: sample & hold and quantization. As the analog signal varies continuously with time, it is necessary to keep it steady or stable for at least the duration needed for digitization. This is done by sample & hold (S & H) block. The analog input signal is first sampled at a specific sampling frequency by sample and hold (S & H) block. Sampling frequency plays a critical role in the ADC conversion process and its value depends on the system and application requirements. The famous Nyquist sampling theorem provides guidelines for determining the correct sampling-rate for the Analog-to-Digital (A/D) conversion process. The amplitude of the sample is then maintained or held by this block. It is still an analog value. The quantization block comes into play then and quantizes the hold signal into discrete values. The signal now is in digital form since it has discrete amplitude and discrete time. An encoder is utilized to convert these discrete values into binary numbers.

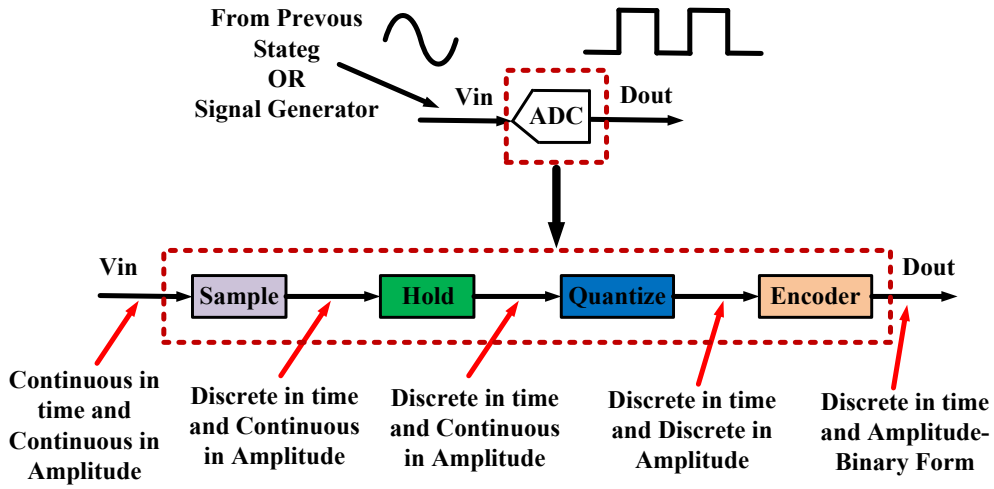


Figure 2. 1. Conceptual representation of working of an ideal ADC.

2.2. Specifications and Parameters of Analog-to-Digital Converters

ADCs performance characteristics can be divided into two categories: static/DC and dynamic/AC characteristics. A concise detail of both of these characteristics is provided below.

2.2.1. Static/DC Characteristics

2.2.1.1. Offset and Gain Error

Figure 2.2. shows the transfer function of an ideal 3-bit unipolar ADC. An ideal ADC is characterized by uniform stair-case input-output characteristics. It is well-known that straight-line model is a good approximation for an ideal ADC. However, the real ADC faces non-ideality because of several reasons, such as mismatches between internal components. This causes a deviation in the stair-case transfer function of ideal ADC. The shift or deviation can either be in horizontal direction or vertical direction. The horizontal deviation is characterized by offset error, while vertical shift is specified by gain error. Figure 2.3. depicts the offset error of a 3-bit ADC, where +1 LSB offset can be observed. However, the ADC can exhibit positive and negative offset errors. Figure 2.4. shows the ADC transfer function with a gain error of +0.5 LSB. Like offset, ADC can show positive and negative gain errors.

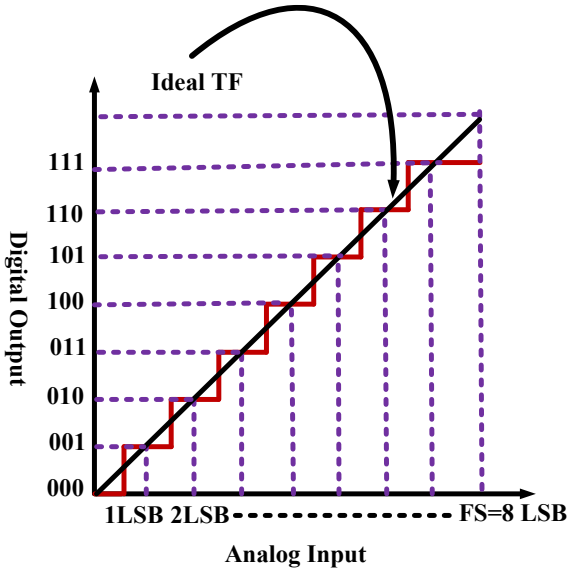


Figure 2. 2. Ideal Transfer Function (TF)/characteristics of a 3-bit ADC.

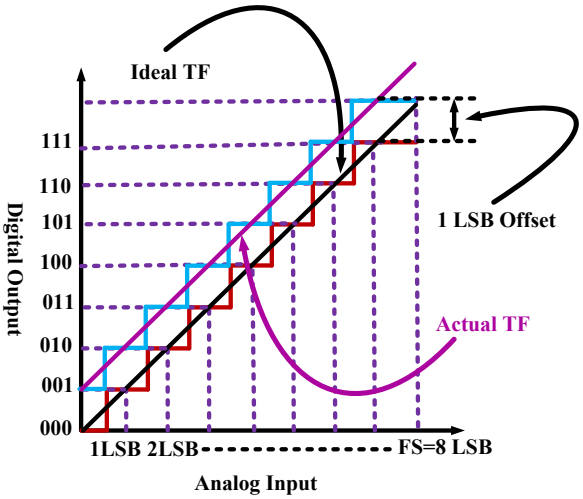


Figure 2. 3. Transfer function (TF)/characteristics of a 3-bit ADC with an offset error.

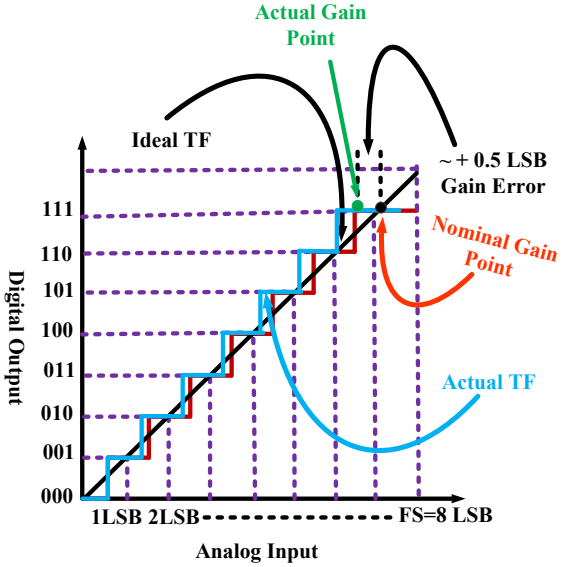


Figure 2. 4. Transfer function (TF)/characteristics of a 3-bit ADC with a gain error.

2.2.1.2. Differential Non-Linearity (DNL) and Integral Non-Linearity (INL)

The transfer function of an ADC can also deviate from its ideal behavior because of non-idealities, as described in section 2.2.1.1. The transfer function of an ideal ADC exhibits uniform stair-case input-output characteristics as shown by Figure 2.5. This means that there is a difference of exactly 1 LSB from one transition to the other, resulting in a constant step width. However, the step width can differ from this ideal behavior because of the non-ideal effects of the real ADCs. Figure 2.5 shows an example, where steps are not uniform. The width of code 010 is more than I LSB (1.25 LSB), while the subsequent code shows a smaller width of 0.5 LSB. DNL is the ADC parameter which specifies how the ADC steps deviate from the ideal values. Following expression defines the DNL of x-th code for an ADC:

$$DNL(x) = \frac{Width(x) - Width_{ideal}}{Width_{ideal}}$$

For code 010 in Figure 22.5, DNL is + 0.125 LSB, while code 011 has a DNL of -0.46 LSB.

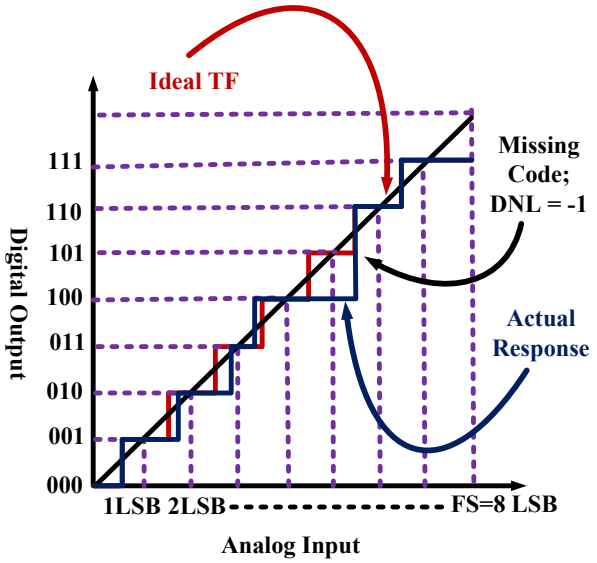


Figure 2. 5. Transfer function (TF)/characteristics of a 3-bits ADC with DNL.

2.2.1.3. Total Harmonic Distortion (THD)

The power spectral density (PSD) plot of the ADC output is a power tool to quantify ADC performance parameters. One of the most important parameters of ADC is distortion, which is characterized by the PSD plot. THD is defined as:

$$\text{THD} = \frac{\text{RMS of fundamental signal}}{\text{RMS of root-mean-square of harmonics}}$$

Generally, the first 5 harmonics are significant and thus they are considered in THD calculation. Usually, THD is measured close to full-scale input signal. However, it can be specified at any signal level. Figure 2.6 shows a sample Power Spectral Density (PSD) plot of an ADC for THD illustration point-of-view.

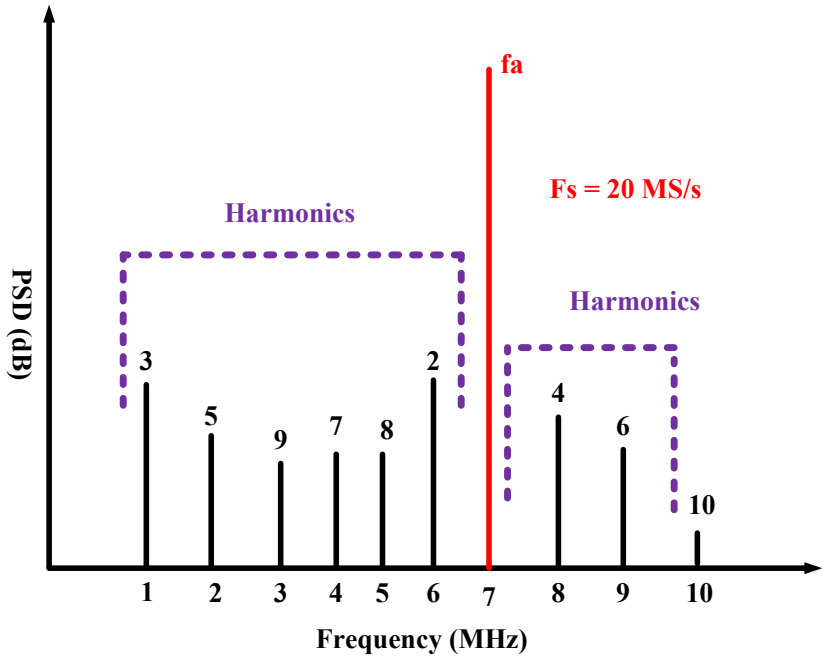


Figure 2. 6. PSD plot of an example ADC highlighting harmonics and THD.

2.2.2. Dynamic/AC Characteristics

2.2.2.1. Signal-to-Noise Ratio (SNR), Signal-to-Noise-and-Distortion Ratio (SNDR), Spurious-Free-Dynamic-Range (SFDR), Dynamic Range (DR)

SNR of an ADC is the ratio between the input signal power and the noise power, and given by:

$$\text{SNR (dB)} = 10\log_{10}\frac{P_{input}}{P_{noise}}$$

SNDR is the ratio between the input signal power and the sum of noise and distortion power, and given by:

$$\text{SNDR (dB)} = 10\log_{10}\frac{P_{input}}{P_{noise+distortion}}$$

Here, thermal and quantization noise contributions are included.

Spurious-free-dynamic-range is defined as:

$$\text{SFDR} = 10\log_{10}\frac{P_{input}}{P_{largestharmonic}}$$

Dynamic range is a ratio between the strongest and weakest signal. Figure 2.7. shows a SNR/SNDR Vs. input power plot for a sample ADC, which has a dynamic range of 70.2 dB.

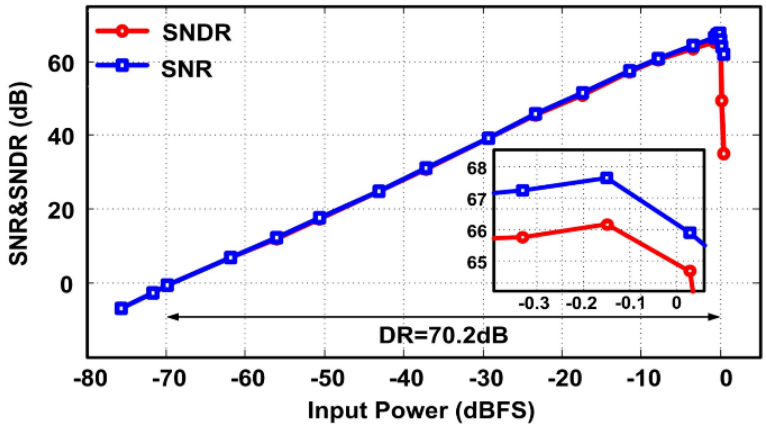


Figure 2. 7. SNR/SNDR Vs. input power plot of an example ADC with a dynamic range of 70.2 dB.

2.2.2.2. Resolution

The minimum variation in the input signal required to increase the output digital code by one Least-Significant-Bit (LSB) is defined as ADC resolution. It is expressed as follows:

$$\text{LSB} = \frac{V_{inFS}}{2^N}$$

where,

V_{inFS} = Full range of the ADC input signal

N = Number of the bits of the ADC

2.2.2.3. Effective-Number-of-Bits (ENOB)

ENOB is the actual resolution of the ADC under consideration of the circuit noise and distortion. It is determined as follows:

$$\text{ENOB (Bits)} = \frac{\text{SNDR(dB)} - 1.76}{6.02}$$

The above formula is valid for a full-scale range of the input signal. As the input signal decreases, SNDR also decreases, resulting in a decrease in ENOB. The above formula is modified as below for reduced signal swing [42]:

$$\text{ENOB (Bits)} = \frac{\text{SNDR(dB)} - 1.76 + 20\log\left(\frac{V_{INFS}}{V_{IN}}\right)}{6.02}$$

Besides input signal amplitude, ENOB may also depend on input signal frequency. It is because high frequencies introduce non-linearities and thus cause SNDR and ENOB degradation. Therefore, SNDR and ENOB vs. input signal frequency plot is normally included in order to see ADC performance at all its operating frequency range [42].

2.2.3. Other Specifications

2.2.3.1. Power Consumption

Power consumption is a key performance parameter for the ADCs. Power consumption requirement depends on the application scenario and type of the ADC. As ADC power consumption can normally be a significant percentage of total system power consumption, reducing its power consumption is highly desirable to get high energy-efficiency. Power consumption has a direct relationship with ADC speed. The higher the speed of ADC, the more is the power consumed by it. The advent of emerging applications, such as internet-of-things, biomedical implants devices and circuits, wireless sensor networks, 5G, 6G and beyond wireless technologies has made this requirement extremely important as well as challenging. Power consumption is an important specification for determining the Figure-of-Merit (FoM) of the ADCs.

2.2.3.2. Technology

The selection of a technology for ADC design depends on its application. CMOS is by far the most widely used technology for modern ADC designs because of its low-power, low-profile, and low-cost based advantages. An increasing trend in System-on-Chip (SoC) solutions, with integrated ADCs on a single chip with the other sections of the system, makes the adoption of scaled CMOS technology nodes an attractive choice. Scaled technology nodes-based ADCs benefit in terms of higher bandwidth, higher speed, and smaller chip-size. However, such ADCs face constrains in terms of dynamic range and sampling linearity due to reduced supply voltages and signal swing [43]. In addition, such ADCs are more likely to suffer from crosstalk and interference issues because of low supply and MOS threshold voltages.

2.2.3.3. Latency

The total time taken by the ADC to convert the analog input signal into digital code is called latency. Thus, low latency means high conversion speed for the ADC. The latency of the ADC depends on its architecture and type. Some applications, such as wireless transceivers for 5G and beyond applications, need ADCs with low latency, while others, such as biomedical applications, require ADCs with slow speed. Low latency comes at the cost of high-power consumption in the ADCs.

2.2.3.4. Bandwidth and Sampling-Rate

The bandwidth of ADC depends on its targetted application. For instance, the ADC bandwidth for audio applications is 20 kHz. Figure 2.8 shows the bandwidth and resolution requirements of ADC for different widespeard application areas. Sampling-rate (f_s) of ADC must be at-least twice or greater than its

bandwidth for a successful conversion of analog signal inot digital domain. This is dictated by the Nyquisite sampling-rate criteria.

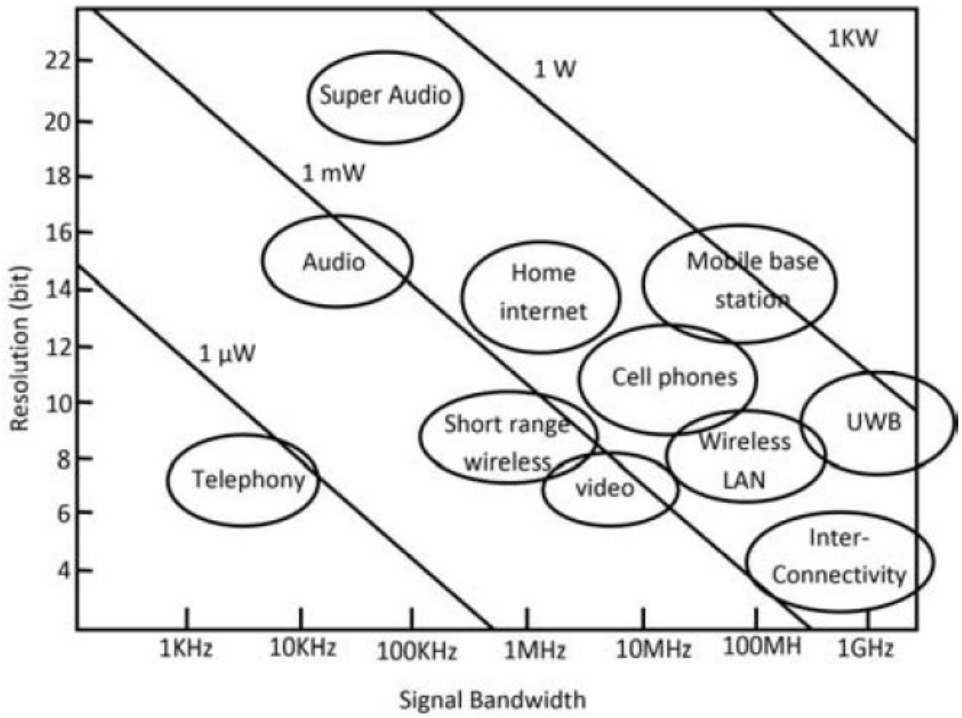


Figure 2. 8. Performance requirements (resolution and bandwidth) of ADCs for different application scenarios [44].

2.2.3.5. Chip-Area

Like power consumption, chip-area occupation is also an important specification of ADC. The primary target is always to design an ADC which occupies as small chip-area as possible, since die area occupation has a direct relationship with the chip cost. This is especially applicable to portable electronic devices, such as mobile devices, where area-efficiency is of utmost importance. Another such application is wireless network on-chip [45]. For ADCs, the area-efficiency is a strong function of resolution, technology node, and conversion-speed. In addition, area-occupation varies from one type and architecture of ADC to the other [46]. It is observed [47] that the area-efficiency of the ADC, like its conversion-efficiency, has improved with CMOS technology scaling consistently. This improvement is valid across a wide range of resolutions and frequencies.

2.2.3.6. Input Signal Swing/Voltage Range/Full Scale Input Range/Dynamic Range

The range of minimum and maximum input signal an ADC can convert into digital domain is called its input signal swing or full-scale input range or dynamic range. Any input signal exceeding this range leads ADC into saturation. The input signal swing of an ADC is related to its resolution. The definition of ADC input signal swing depends on whether ADC input is single-ended or differential. Figure 2.9 shows a pictorial representation of ADC input signal swing. Assuming a single-ended 8-bit ADC with a full-scale range of 2V,

$$\text{LSB} = \frac{\text{FSR}}{2^{\text{N}}} = \frac{2}{2^{8}} = 7.8\ \text{mV}$$

where

LSB = Least significant bit

FSR = Full scale range

As evidenced from Figure 2.9, the differential-mode ADC gets a 6 dB more dynamic range than a single-ended mode ADC.

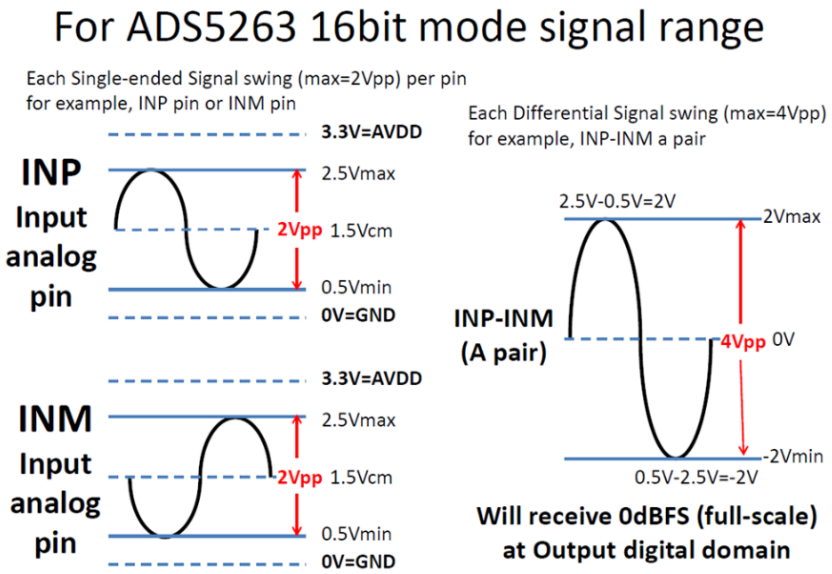


Figure 2. 9. Input signal swing of an ADC: single-ended vs differential topology.

2.2.3.7. Supply Voltage

Supply voltage to ADC is a key parameter and its selection criteria depends on numerous factors. The obvious factor is the process node in which ADC is designed. Input signal swing requirement of ADC is another factor in this regard. Another subtle but crucial factor is how pervasive is the crosstalk and interference issue for the ADC application area. For crosstalk-unavoidable applications, such as multi-channel sensors, the use of low-supply voltage usually results in a degraded performance, since the threshold voltage of the transistor is low, and crosstalk kills the performance. This requires low-supply based ADC to employ special techniques to mitigate crosstalk issues, which leads to high chip-area and design complexity. However, the downside of the use of high supply voltage is high power consumption and thus low conversion-efficiency of the ADC.

2.2.3.8. Power Supply Rejection (PSR)

Power supply ripples can couple to the ADC input to appear on the digital outputs. There is a need for a metric which measures how these ripples are coupled. Power supply rejection (PSR) is that metric. An adequate value of PSR is required for the ADC to avoid affecting its performance due to power supply noise. Usually, the noise on the power supply lines is relative to ADC input range. For an ADC with an input range of 0.7 V_{rms} and power supply noise of 20 V_{rms}, the noise on the input is -31 dBFS. Assuming the ADC with a PSR of 30 dB, the noise will appear as a -61 dBFS spectral line in the ADC output. To reduce power supply noise, decoupling and filtering of the power supply line is done. How much decoupling and fileting is needed depends on the PSR value. PSR is more critical in environments where noise is high. Some such examples include biomedical and industrial applications.

2.2.3.9. Common-Mode Rejection (CMR)

Common-mode rejection is a measure of the induced differential-mode signal in the presence of a common-mode signal. As differential input-based ADCs reject even-order distortions naturally, the use of differential-inputs is preferred for many ADCs to get high immunity against common-mode signals. There are several ways common-mode signals can be induced. Some of these include power supply ripple, high-

power signals present on the ground plane in presence of high magnetic and electric fields, and RF leakage through mixers and RF filters. The majority of the ADCs often have CMR values of 50-80 dB.

2.2.3.10. Clock Slew Rate

ADCs require a minimum slew rate to achieve targeted performance, which is called clock slew rate. This is necessary to have a well-defined sample instant for the ADCs. To achieve this, the majority of the ADCs have adequate gain on clock buffers. Slow slew rate causes a high degree of uncertainty of the sample instant, which results in excessive noise. It is, therefore, necessary to meet clock slew rate requirements.

2.2.3.11. Monotonicity

An ADC is called monotonic if its digital output codes increases with the increase of its input analog voltage and vice versa. A monotonic ADC does not guarantee that there is no missing code. A monotonic ADC can have a DNL value greater than 1 LSB which would lead to a missing code at some point in the transfer characteristics.

2.2.3.12. Figures-of-Merit (FoM)

To evaluate ADC performance and compare it with the other ADCs, well-defined Figure-of-Merits (FoMs) are essential. Although several FoMs have been proposed for the ADCs as described in [48], two FoMs have gained substantial popularity and have been well-accepted by the ADC designers and researchers worldwide. These FoMs, therefore, have become a sort of standard for ADCs evaluation and comparison. First FoM is called as 'Walden FoM' and labeled as FoM_W. This FoM is defined as:

$$\mathrm{FoM_W} = \frac{\mathrm{P_{avg}}}{2^{\mathrm{ENOB}}.\mathrm{f_s}} \text{ (J/conversion-step)}$$

where,

P_{avg}= Mean power consumption of ADC

ENOB = Effective-no-of-bits

f_s= Sampling-rate

This FoM_W measures the energy-efficiency of the ADC. As per this FoM_W metric, energy increases 2 times per bit. This FoM_W provides several insights into the ADC performance. For example, it states that ADC power consumption doubles with the doubling of its sampling-rate. Alternatively, high-speed ADCs, working at high clock rates, burn more power than low-speed ADCs. Low FoM_W means an ADC with a better performance or energy-efficiency, so the target of ADC designers is to design ADCs with low FoM_W.

For comparison of high resolution-based ADCs limited by thermal noise, there is an alternative FoM called 'Thermal FoM'. The thermal FoM is defined by:

$$\mathrm{FoM_{TH}} = \frac{\mathrm{P_{avg}}}{2^{2\mathrm{ENOB}}.\mathrm{f_s}} \text{ (J/conversion-step)}$$

Unlike FoM_W, this FoM_{TH}considers error power rather than amplitude. As per this FoM, energy increases 4 times per bit.

The second FoM is named as 'Schreier FoM' and labeled as FoM_S. According to this FoM,

$$\mathrm{FoM_S} = \mathrm{SNDR} + 20\log\left(\frac{\mathrm{BW}}{\mathrm{P_{avg}}}\right) \quad \text{(dB)}$$

This FoM also gives various insights about ADC performance. For instance, it states that energy increases 4 times per bit. ADCs with a higher FoM_W are considered high performance ADCs.

2.3. Analog-to-Digital Converter Types and Topologies: A Brief Review

The world first ADC circuit of practical importance was invented in 1974 [49]. Since then, there has been a tremendous development in the field of ADCs. Traditionally, the ADCs can be divided into two categories: Nyquist-rate and Oversampled. However, a new trend in ADCs design has been witnessed in the last 2 decades in the form of the emergence of Hybrid architectures. This section provides a brief overview of the major ADC types of each category (Nyquist-rate, Oversampled, and Hybrid). The core aim is to explore the potentials of each ADC type and evaluate their merits and demerits for multi-channel ASICs for space applications, which is the goal of this thesis. This will be done keeping in view the requirements and specifications of the ADCs for this application, which have been stated in Chapter 1 of this thesis. Besides low-power, low-profile, and low-cost, each ADC type will specifically be assessed for its capabilities in terms of:

- Sufficiently large sampling-rate

- Adaptable conversion-speed with reconfigurable power-efficiency

- Low switching-noise

- Small crosstalk and interference issues

- Event-triggered operation

- Low clock jitter

- Memory as well as memory-less operation

- Flexibility and versatility

2.3.1. Nyquist-Rate ADCs

Nyquist-rate ADCs perform conversion process following the Nyquist sampling theorem, which states that the sampling-frequency of an ADC must be at least twice the highest input-frequency to digitize a signal waveform without aliasing or distortion. The following is a brief detail of widely used Nyquist-rate ADCs.

2.3.1.1 Successive-Approximation-Register (SAR) ADC

Historically, SAR is the first invented ADC architecture in 1940s. However, first all MOS-based SAR ADC was proposed in 1974 [50]. The architecture of a basic SAR ADC is shown in Figure 2.10. It has four blocks: (1) a sample & hold (S&H), (2) a comparator, (3) a digital SAR logic, and (4) a DAC connected in feedback. The operation of the ADC starts with the sampling of the analog input signal (V_{in}). After this, conversion phase starts, where digital output code (D_{out}) of N-bits (where N is the resolution) is determined one-by-one by a binary-search algorithm action of the digital logic based on the comparator decisions. The DAC is successively adjusted towards V_{in}. V_{in} is converted into its N-bits digital representation after N cycles [51].

Charge Redistribution SAR ADC is the most widely used topology besides several other methods to implement generic SAR architecture. Figure 2.11 shows the Charge Redistribution SAR ADC with all the signals in voltage domain. As shown in Figure 2.11, the DAC is realized using an array of binary-weighted capacitors. The sampling of V_{in} is also performed by Capacitive-DAC (CDAC). After the sampling, the SAR conversion process starts. During this conversion phase, charge redistribution takes place, using switches, to iteratively govern a new residue voltage V_{res} or V_{DAC} . The comparator performs quantization of this V_{DAC} [51].

Charge Redistribution SAR ADC architecture offers various advantages. First, it is scaling-friendly since all the components can be designed in modern CMOS processes owing to the fact that the majority of the components are digital. Second, the matching of CDAC capacitors is normally good, thus leading to a good

linearity performance. Third, all the blocks can be made dynamic with respect to power consumption, which facilities adaption of power consumption with the sampling-rate [51]. However, this architecture poses constraints with respect to its speed and resolution. Inherently, SAR ADC is an attractive choice for low-to-medium speed (up to few MHz) and low-to-medium resolution (8-12 bits) and accuracy. Although a development in achieving high speed and resolution using SAR ADC can be seen recently [51], however this comes at the cost of high power and chip-area. To get higher resolution, i.e., enhancing SNDR, it is essential to improve the noise and linearity performance. This results in CDAC area increase. For one bit resolution improvement for an N-bit SAR ADC, the CDAC area and power becomes double. In addition, CDAC calibration and mismatch error shaping methods are likely to be utilized for high resolution SAR ADCs to ensure required linearity performance [52]. This again leads to an increase in the chip-area, power, and design complexity.

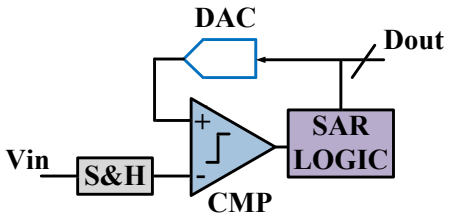


Figure 2. 10. Architecture of a basic SAR ADC [51]

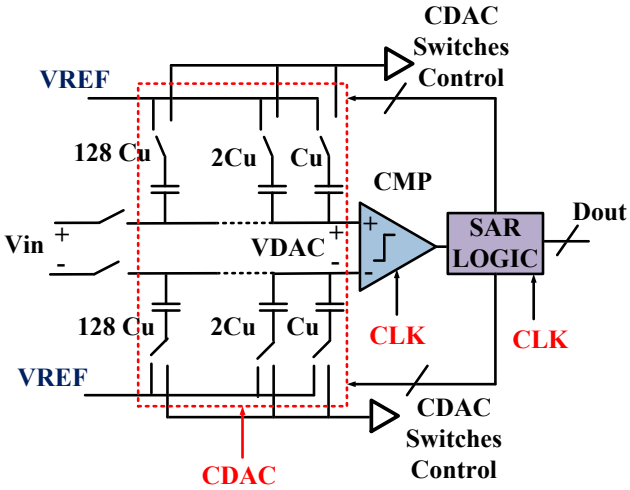


Figure 2. 11. Architecture of a Charge Redistribution SAR ADC with resolution (N= 8).

2.3.1.1.1 Asynchronous SAR

To increase conversion-speed of the conventional SAR ADC, asynchronous SAR (ASAR) ADC architecture was proposed in 2006 [53]. The ASAR ADC proposes an asynchronous scheme for the digital logic of SAR ADC, which offers some advantages over conventional/synchronous digital logic. To understand the differences between these two schemes, Figure 2.12 shows the timing waveforms of conventional SAR and ASAR ADCs. The first difference is that the ASAR ADC needs only a low-duty cycle and low-switching external clock unlike high-speed and high-switching clock in conventional SAR ADC. All the other required clock signals are generated internally inside the ASAR ADC using only a single external clock signal.

The second difference is the different lengths of the time intervals of clock for comparator. This length is fixed for each bit cycle in the case of synchronous SAR, while it is unequal for the ASAR ADC. For SAR ADC as shown by the timing waveforms of Figure 2.12, the clock for comparator (CLK_C) is generated according to the external clock signal, which forces it to be constant for each bit cycle. The comparator operates only on the positive/negative edge of the comparator clock (CLK_C), even if it is able to perform

its function (reset or regeneration) before the arrival of the next positive/negative edge of the clock. Alternatively, it waits for the arrival of the subsequent positive/negative cycles of the clock to operate. In ASAR ADC, on the other hand, the external clock governs only the time duration of the sampling phase and conversion phase. The clock for the comparator (CLK_C) is generated internally based on the comparator state. Once the comparator is done with the decision of a particular bit after a certain time duration, it enables generation of the rising edge of an internal clock signal for the SAR control logic. The comparator clock goes low right after the rising edge of the clock signal for the SAR logic, thus resetting the comparator. This forces the clock signal for the SAR logic to go low, which in turn triggers the SAR logic to generate the next rising edge of the comparator clock for the next bit decision after an adequate delay amount. It is obvious that each operation is performed immediately after completion of the previous one, the conversion speed of ASR ADC is higher than synchronous SAR ADC [54].

The third difference between these two architectures is timing constraints. In synchronous SAR ADC, the operating speed is dictated by the longest time among the comparison time, comparator reset duration, and CDAC settling time. In contrast to this, ASAR ADC timing constraints are different. The comparator clock as well as SAR logic clock are generated according to the feedback signal from the comparator. As the comparator regeneration time depends on the amplitude of the input signal, both the clocks are unequal for each bit decision. The total conversion time for ASAR ADC can be calculated using following expression:

$$\mathrm{T_{CASAR}} = \frac{1}{\mathrm{f_s}} - \mathrm{T_s}$$

The timing constraints are given below:

$$\mathrm{T_{CASAR}} \geq \sum_{\mathrm{i}}^{\mathrm{N}} [\mathrm{T_r} + \mathrm{T_{cmp,i}} + \mathrm{T_f} + \max(\mathrm{T_{DAC,i}}, \mathrm{T_{rst,i}})]$$

Here, T_r and T_f are timing constraints, while$T_{cmp,i}$ depends on the input signal to the comparator. As per the above equations, the total comparison time must be lower than the total conversion time to avoid violating the timing constraints for the ASAR ADC [54]. The advantages and disadvantages of an ASAR ADC are similar to a synchronous SAR ADC, except that ASAR ADC has high conversion-speed.

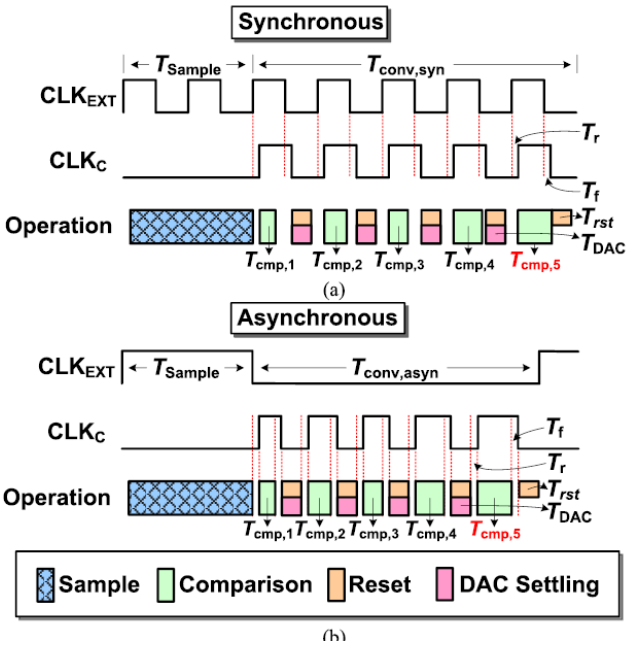


Figure 2. 12. Timing waveforms for the operation of (a) synchronous and (b) asynchronous SAR ADCs [54].

2.3.1.2. Flash ADC

The Flash ADC architecture was proposed in 1979 [55]. Figure 2.13 shows the architecture of a basic 2-bits flash ADC. An N-bits flash ADC is comprised of $2^N - 1$ comparators in parallel, fed by the same clock at the same time. To generate reference voltages for the comparators, a ladder network with 2^N identical values resistors is employed. This ladder network divides the full-scale range (V_{FS}) into 2^N regions. The working of the flash ADC can be summarized as follows:

The input signal (V_{in}) is compared with the respective reference voltage of all the comparators simultaneously. If V_{in} is greater than a reference voltage of a comparator, the output of the corresponding comparator is equal to logic 1 (high); otherwise, the output is logic 0 (low). As the comparators are connected between the low and high reference voltages, there will be a series of 1's changing to a series of 0's. This output pattern is called the thermometer code. The thermometer code facilitates deciding the quantization levels close to the input voltage amplitude. The final binary output of the ADC is generated by a thermometer-to-binary encoder [56].

Like SAR ADC, flash ADC has its own strengths and drawbacks. The conversion speed of the flash ADC is high because of the ability of its comparators to operate in parallel. However, the area and power-efficiency of flash ADC is not good for high resolution, since the number of comparators needed rises exponentially with the number of bits [57] . In addition, it is also constrained with respect to the input bandwidth, which is confined by the total parasitic capacitances at the input of the substantial number of comparators as well as routing parasitic capacitance. Moreover, the offset voltage of the comparators is a big problem in flash ADC. To suppress it, either a preamplifier or offset-calibration method is used. This results in large area, high power, and increased design complexity [56]. Furthermore, comparator metastability can also be an issue for flash ADC [57].

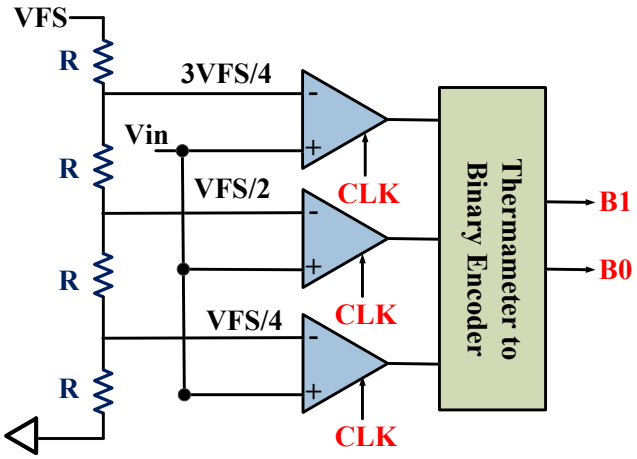


Figure 2. 13. Architecture of a traditional 2-bit flash ADC [56].

2.3.1.3. Subranging and 2-step ADC

Subranging or 2-step ADC was introduced as a solution for the key limitation of the flash ADC, i.e., the number of comparators increases exponentially with the number of bits, thus leading to high power consumption and large chip-area. In Subranging or 2-step ADC, the task of getting high resolution is divided into two low resolution-based ADCs (coarse and fine ADC) that operate sequentially. Figure 2.14 depicts architecture of a subranging or 2-step ADC. Th coarse ADC works at full-scale range and generates MSBs after performing conversion of the sampled analog input. The DAC then converts these MSBs into an analog signal. The DAC output is then subtracted from the sampled analog input and amplified to generate a residue voltage. This residue voltage is applied at the input of the second ADC, which operates at the subrange of the full-scale range. This fine ADC digitizes the residue voltage and generates LSBs. The difference between a 2-step and subranging ADC is that the former utilizes a gain stage to amplify the

residue voltage, while the latter does not use it. The order of subranging can be extended to N-bit by employing an L-bit course ADC and M-bits fine ADC, where N = L + M [56] to build an N-bit subranging ADC.

It is clear that such ADC architecture uses a significantly smaller number of comparators as compared to flash ADC. This results in a substantial reduction in power consumption and chip area. However, there are some drawbacks associated with this architecture. The one issue is of latency in final digital output code. It is because the second stage ADC needs to wait for the conversion from the first ADC and generation of residue voltage. Another problem is related to the mismatches between the generated residue voltage and input range of the fine ADC. The mismatch leads to an incorrect residue voltage by the fine ADC, causing sever linearity issues, such as missing codes. To reduce this, redundancy and calibration are employed, which results in design complexity. The DAC non-linearities also introduce errors in the LSBs generated by the fine ADC [56].

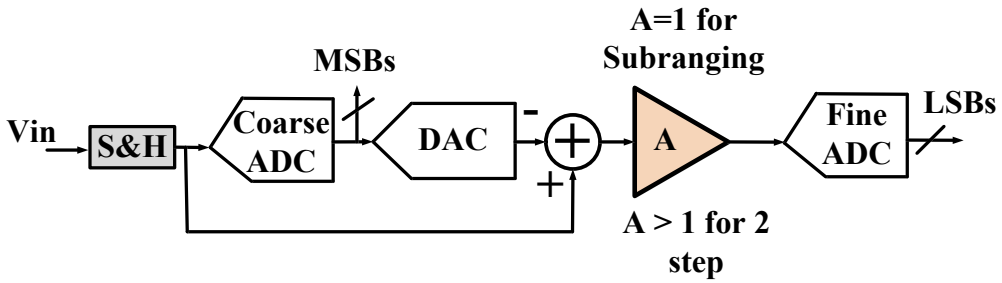


Figure 2. 14. Architecture of subranging or 2-step ADC.

2.3.1.4. Pipeline ADC

Like SAR and flash ADCs, the pipeline ADC was also proposed in the mid-1970s. Pipeline ADC is a further extension of a 2-stage ADC. It combines pipelining method with the concept of 2-step ADC to push high resolution operation to higher sampling-rates. One example of a pipeline ADC is shown in Figure 2.15. After the sampling of the input signal, the first stage commences conversion operation and generates its output bits. The same stage also generates the residue voltage and provides it to the subsequent stage after amplification to the full-scale. The same operation continuously occurs in all the subsequent stages. Thus, when one stage is performing conversion of the sample, the preceding stage is processing the next sample. The last few LSBs are usually resolved by a low-resolution flash ADC. The conversion- rate of final digital output code is the same as of only one pipeline stage [56].

As obvious from its operation, a substantial latency occurs in pipeline ADC. However, output code for each stage is generated at high speed because of pipeline operation. Comparators, operational amplifiers, and switched-capacitor circuit are needed to implement pipeline ADC. The high-power consumption of operational amplifiers for high resolution pipeline ADCs is often a key design bottleneck. In addition, the use of redundancy is common in pipeline ADCs to reduce mismatch, like 2-stage ADCs. This can also result in design complexity [56].

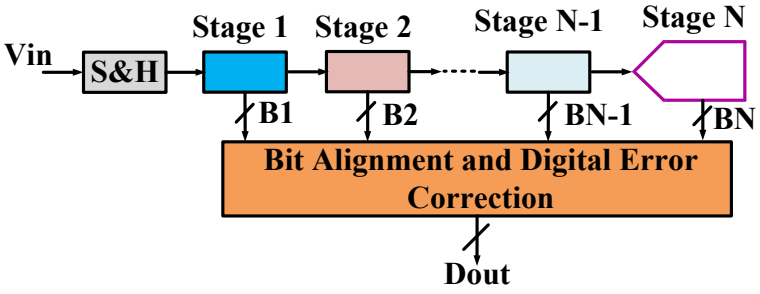


Figure 2. 15. Architecture of a Pipeline ADC.

2.3.1.5. Single and Dual-Slope ADC

In single and dual-slope ADCs also known as integrating ADCs, the output code is generated by comparing the analog signal with a sawtooth waveform, generated by an integrator. Figure 2.16 (a) shows the block diagram of a single-slope ADC. It consists of an integrator, a comparator, and an AND gate. Initially, the counter is reset to zero. The reference voltage, which is achieved after being integrated by an integrator, is compared with the input voltage by the comparator. At the start of the conversion process, the input voltage is larger than the reference voltage, resulting in a logic 1 at the comparator output. As a result, the counter is enabled and starts counting. The output of comparator changes to 0 when the integrated reference voltage becomes equal to the input voltage. Consequently, the counter stops working because of the low output of the AND gate. A reset switch is also part of the design. It is closed once the comparator output goes low to ensure avoiding any leftover charge across the capacitor. The output of the counter is proportional to the input voltage. Figure 2.16 (b) depicts a graphical representation of the time taken for the integration with respect to the applied input voltage. The slope is constant since the reference voltage and RC values are constant. The time taken for the integration depends on the input voltage, i.e., it is proportional to the input voltage. Because of the single-slope as depicted by Figure 2.16 (b), the ADC is called as single-slope ADC.

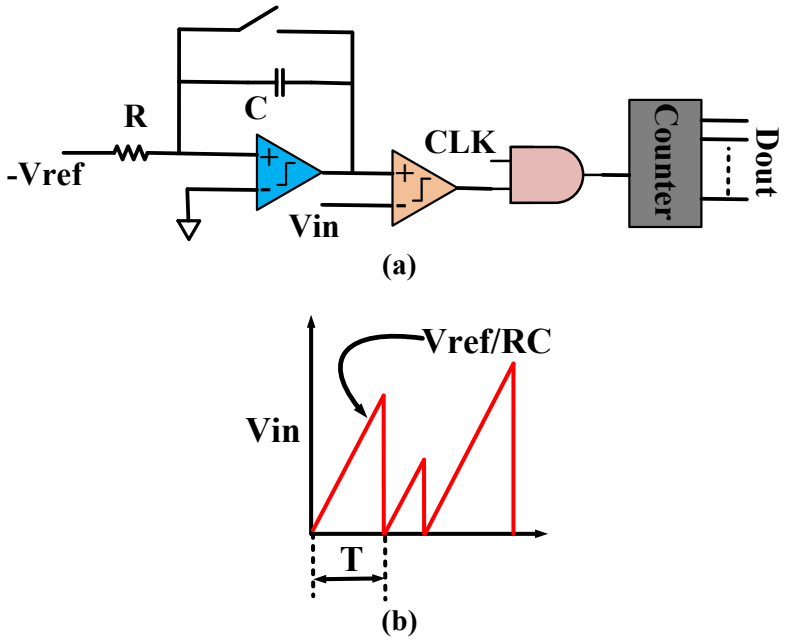


Figure 2. 16. (a) Architecture of a single-slope ADC, (b) Time taken for the integration with respect to (wrt) applied input voltage.

Figure 2.17 represents block level diagram of a dual-slope ADC. Unlike a single-slope ADC, the integrator of the dual-slope ADC is equipped with a switch at the input, which can either connect the reference voltage or the input voltage. Initially, the switch connects the input voltage. The integrator integrates the input voltage until its output is equal to the input voltage. For an output voltage V_1 and T_1 is the time taken,

$$V_o = -\frac{1}{RC} V_{in} dt$$

$$V_1 = -T_1 \frac{V_{in}}{RC}$$

After T_1, the switch is connected with the reference voltage, which is integrated. As shown by diagram 2.17 (a and b), the reference voltage is negative. The integrator integrates in a positive direction until the output voltage equals zero. The time taken for this integration is T_2. Based on the circuit and timing waveforms, after T_1,

$$V_o = -\frac{1}{RC}-V_{ref}dt + initial$$

For T_2

$$V_2 = -T_2\frac{-V_{ref}}{RC} + V_1$$

$$V_2 = T_2\frac{V_{ref}}{RC} - T_1\frac{V_{in}}{RC}$$

Also,

$$T_2 = T_1\frac{V_{in}}{V_{ref}}$$

The working of the ADC can be summarized as follows: Initially, input voltage is connected to the integrator with the help of the switch. It is integrated in negative direction by the integrator. The output of the comparator becomes high. Consequently, the counter starts counting from zero until the overflow becomes 1. The counter takes 2^N clock cycles to integrate the input signal. With overflow detection, the switch changes its position and is connected with the reference voltage. The integrator starts integrating in a positive direction and the same process is repeated. The counter stops counting at the comparator low output. At that time, the binary output is proportional to time T_2. The total conversion time of the ADC is:

$$T_{total} = 2^N T_C + NT_C$$

where T_C is the clock period.

This type of ADCs offers various advantages. First, they provide better noise immunity. Second, they offer good accuracy. Third, the input signal is averaged. Like other ADCs, this topology is also associated with some drawbacks. First, accuracy depends on the external components. Second, their conversion time increases with higher resolution, so they are slow.

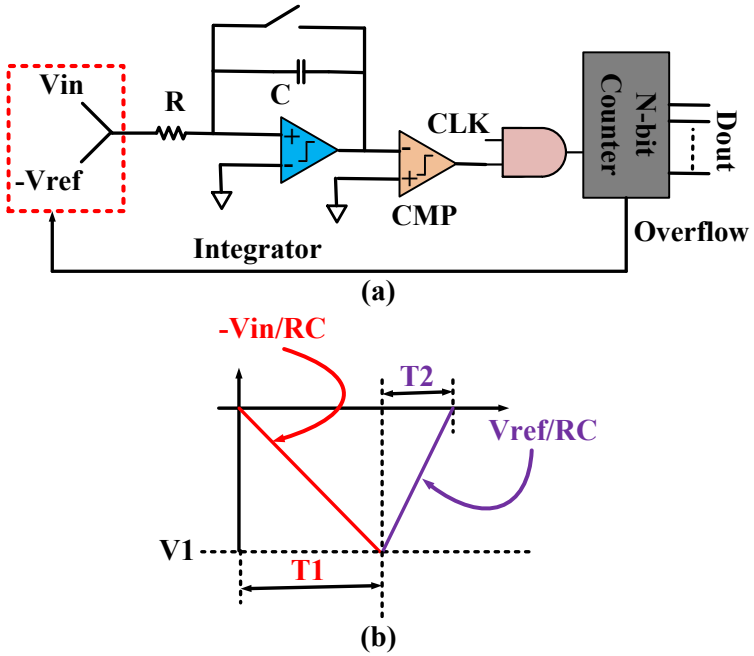


Figure 2. 17. (a) Architecture of a dual-slope ADC, (b) Time taken for the integration wrt applied input voltage.

2.3.1.6. Ramp ADC

Ramp or counter ADC is a simple ADC, which utilizes a counter for the analog to digital conversion. The bloc diagram of a simple ramp ADC is shown in Figure 2.18. It consists of a comparator, a counter, a DAC, a control circuit, AND gate, and output latches. As shown in Figure 2.18, the analog input signal (V_{in}) is applied at the positive terminal of the comparator. At the start of the conversion process, the counter is reset to zero. As a result, the output of DAC is also zero. Consequently, the output of the comparator is high (1). This leads to turning on the AND gate and its output goes high. As the AND gate output acts as a clock signal for the counter, the counter starts counting at the rising edge of the AND output signal. This changes the output of the DAC. As the counter keeps on incrementing its output, the DAC output voltage also increases in a staircase or ramp fashion. The comparator compares the input signal voltage with the DAC output voltage constantly. As long as the input voltage is greater than the DAC voltage, the output of the comparator is high, and as a result, the counter keeps on incrementing and DAC output increases in a staircase manner. When the input voltage is lesser than the DAC voltage, the output of the comparator is low, which in turn means no clock pulse to the counter. The control block is active low here, so it is activated at this stage and performs two functions: it latches the output of the counter and resets the counter to zero. The same conversion process starts again for the new input sample and continues the same process. Based on this operation, it is concluded that the output voltage is proportional to the input voltage. In addition, the ADC conversion time depends on the amplitude or magnitude of the input signal voltage. The larger the input signal amplitude is, the longer the conversion time of the ADC is. The conversion time of the ADC can be written as:

$$T_C = (2^N - 1)T_{CLK}$$

where,

N = ADC number of bits

T_{CLK}= Time period of the clock pulse

As per the above equation, the conversion time is directly proportional to the ADC resolution and clock pulse. High resolution increases the conversion time. One way to reduce the conversion time at high resolution is to increase the clock frequency. This, however, is also limited by the response time of the ADC components. The biggest advantages of this ADC architecture are its simplicity and cost-effectiveness. The downside, however, is its slow conversion speed for high resolution.

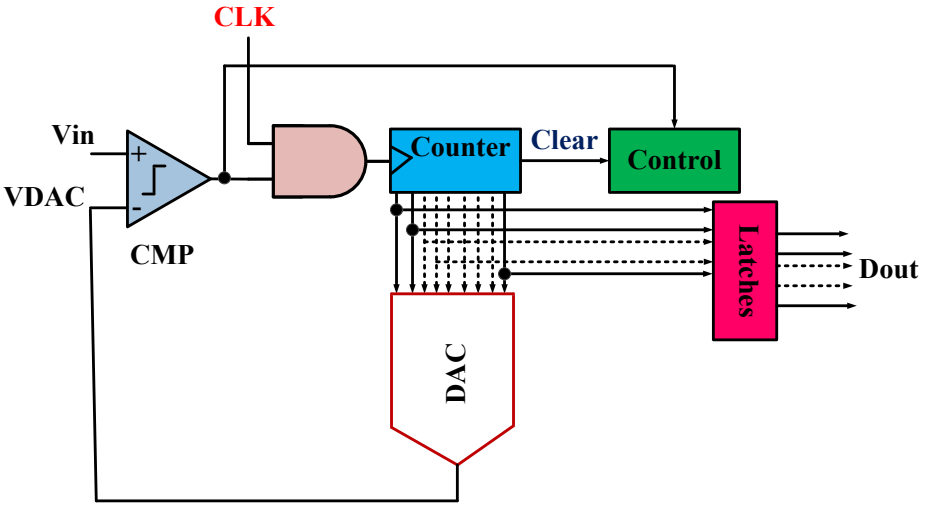


Figure 2. 18. Architecture of a ramp ADC.

2.3.1.7. Time-Interleaved ADC

Time-interleaving is a widely used method to get high conversion speed, where multiple ADC slices or channels operate in parallel. First time-interleaved ADC was proposed in 1980 [58, 59], while first product based on time-interleaved ADC was produced in 1987 [60]. Figure 2.19 displays architecture of a time-interleaved ADC with N-channels. Assuming that the sampling-rate of each ADC slice or channel is f_s, the sampling-rate of N×f_s can be achieved by using N-channel time-interleaving. Therefore, this architecture is capable of providing a conversion-rate of up to several GS/s. Sample and hold of each channel samples the analog input, and the corresponding ADC converts this signal into digital output at a sampling-rate of f_s. All channel outputs are combined using a digital multiplexer, thus resulting in a sampling-rate of N×f_s [56].

The power consumption of time-interleaving ADC is relatively lower than a flash ADC for same performance since time-interleaving ADC employs several power-efficient ADC channels in parallel. In time-interleaving ADC architecture, it is also possible to use several types of ADC slices (e.g., SAR, pipeline, and flash ADC) depending on the power-efficiency requirements of the application. Ideally, total power consumption of N-channel time-interleaved ADC is N times the power consumption of a one -channel ADC. Therefore, it is highly likely that the conversion-efficiency of N-channel time-interleaved ADC should be the same as of a single -channel ADC. However, this is not true in practice. The conversion-efficiency of time-interleaved ADC is always lesser than the single-channel ADC because of the power consumption of the blocks needed for time-interleaving. These include multiple clock phases generation and distribution, reference and input signal generation and distribution to all the channels, and mismatch calibration. Time-interleaved ADC poses several challenges. These include offset mismatch, gain mismatch, timing mismatch and bandwidth mismatch among the channels or slices. Effective calibration techniques are often necessary to reduce the effects of these issues [56].

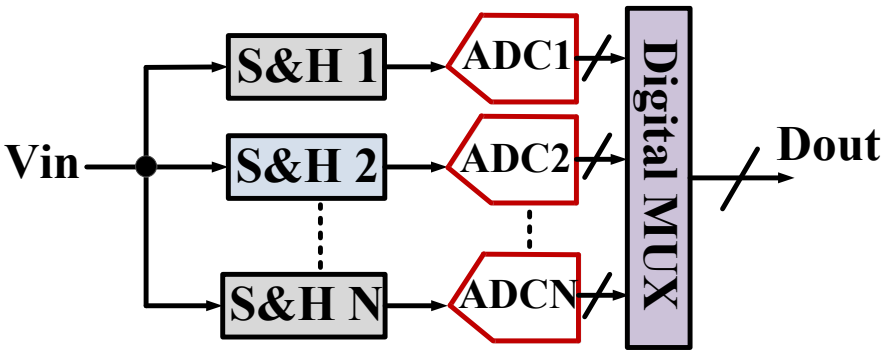


Figure 2. 19. Architecture of a time-interleaved ADC with N-channels.

2.3.2. Oversampling ADCs

Oversampling ADCs can be divided into two categories: Sigma-delta (Σ-Δ) ADCs and Incremental ADCs.

2.3.2.1 Sigma-Delta (Σ-Δ) ADCs

Sigma-delta (Σ-Δ) ADC was first proposed in 1962 [61]. Unlike Nyquist-rate ADCs whose sampling-rate is twice the maximum input frequency, Σ-Δ ADC performs sampling of the input signal at a very high sampling-rate. Figure 2.20 shows a simple architecture of Σ-Δ ADC, which consists of a sample and hold block, a Σ-Δ modulator, an anti-aliasing digital filter, and a digital decimation filter [62]. There is a one-bit ADC/quantizer inside Σ-Δ modulator, which produces a quantized, coarse output after sampling of the input

signal. A high speed and pulse-wave representation of the input signal is produced at the modulator output as a result of modulator conversion action of the input signal. This signal is noisy. The circuit has the ability to shape the noise into higher frequencies in the output spectrum. The digital/decimation filter performs two functions: first, it filters the high frequency noise; second, it solves the issue of high-sampling rate. A low-pass digital filter is utilized to attenuate high-frequency noise, while the output data-rate is slowed down by a decimation filter. A slower multi-bit code (digital output) is produced at the output owing to the sampling and filtering of modulator stream 1-bit code by the digital/decimation filter. Unlike other ADCs, Σ-Δ ADC has two different sampling-rates: input and output sampling-rate. The ratio of output to input sampling-rate is defined as decimation-ratio or oversampling-ratio (OSR).

Figure 2.21 depicts architecture of a Discrete-Time (DT) Σ-Δ ADC with inside components of Σ-Δ modulator. The Σ-Δ modulator consists of an integrator, comparator, and a DAC (1-bit or N-bit). The operation of ADC can be described in a more detailed manner using Figure 2.21. First, the difference (Δ-operation) of the input signal and the output of DAC (1-bit or N-bit) provides an analog differential signal, which is integrated (Σ-operation). These two operations are the actual reasons behind the nomenclature of this ADC. After this, the integrated signal is compared with a reference voltage to get a 1-bit or multi-bit ADC output [52]. The decimation filter performs the above-mentioned two functions, i.e., attenuation of high-frequency noise and slowing down of the output sampling-rate.

Σ-Δ ADC can be subdivide into two categories: discrete time (DT) domain and continuous time (CT) domain. Discrete time domain Σ-Δ ADCs are implemented by designing the loop resonator in discrete time domain such as switched-capacitor filters. Continuous time domain operation of Σ-Δ ADC can be achieved by designing the loop resonator in continuous time domain such as LC, RC filters, and transconductors-C. As compared to discrete tome domain, the continuous time domain Σ-Δ ADC are able to operate at higher conversion bandwidth for a given OSR because of its capability to deal with higher clock frequency. The downside, however is the performance degradation in continuous time domain Σ-Δ ADC due to non-idealities, such as loop delay and clock jitter [57]. Figure 2.22 shows a bandpass continuous time domain Σ-Δ ADC architecture.

Because of oversampling and noise-shaping characteristics, Σ-Δ ADC architecture is capable to achieve a very high resolution. But, it is achieved only with a relatively small bandwidth [52]. In addition, this architecture is not scaling-friendly because of the use of OP-AMPs.

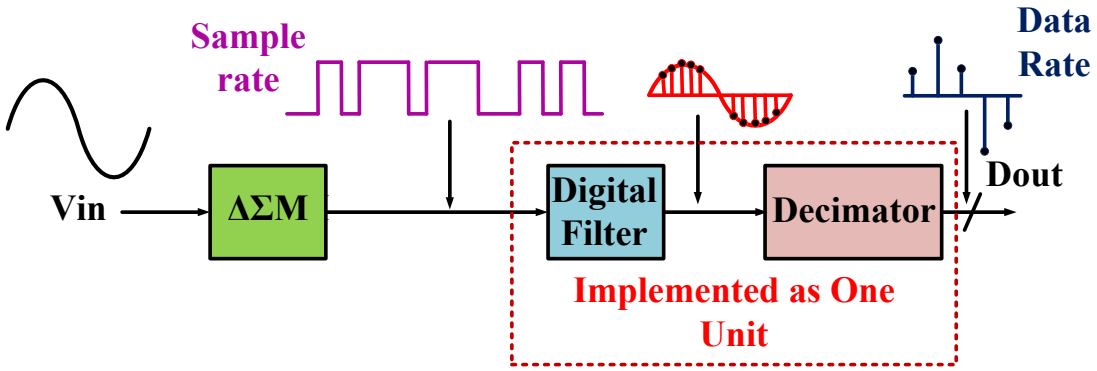


Figure 2. 20. Block Diagram of a Σ-Δ ADC.

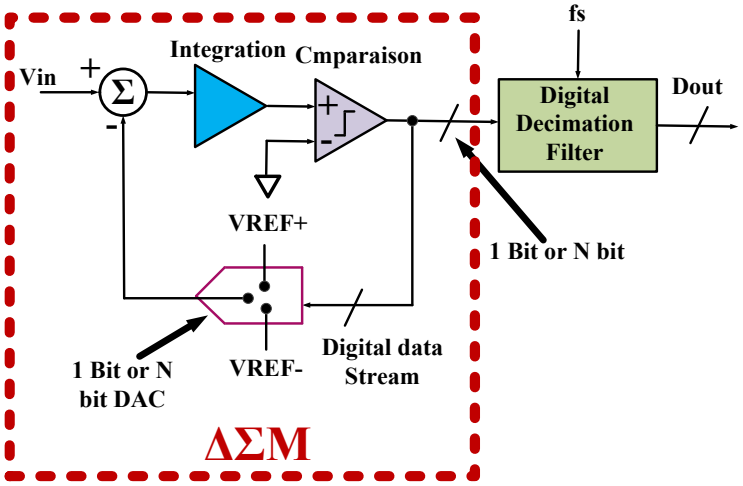


Figure 2. 21. Architecture of a basic DT Σ-Δ ADC with its major blocks [52].

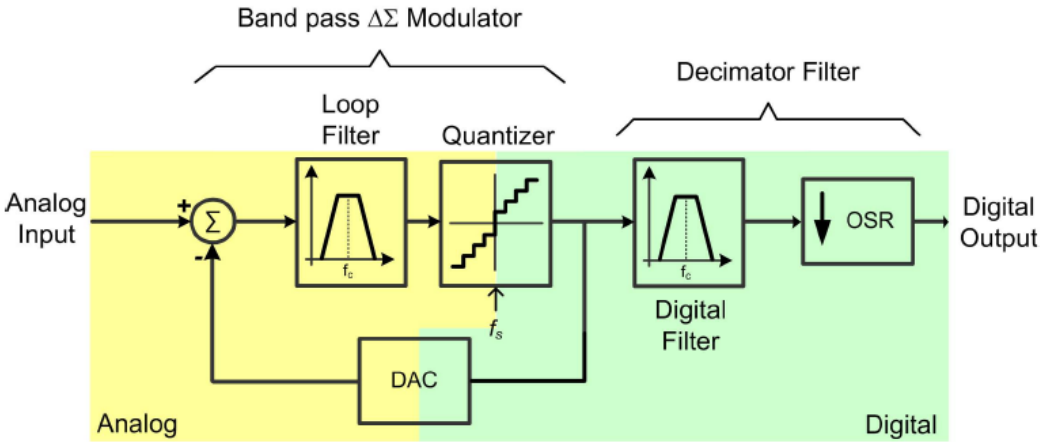


Figure 2. 22. A basic architecture of a bandpass CT Σ-Δ ADC [57].

2.3.2.2. Incremental Sigma-Delta (Σ-Δ) ADC

For multi-channel sensor applications, each channel needs to be digitized individually with low latency and to be multiplexed conveniently. Therefore, they need ADC with low latency. The latency of Σ-Δ ADC can be substantially long. Figure 2.23 (a) presents an alternative representation of a Σ-Δ ADC. It can be seen that the latency from the input to the output depends on the order of the ADC. While this ADC operating under multi-channel environment and assuming that the input signal was switched to another channel, the equivalent output estimation of the new channel will be achieved after the settling of the decimation filter, which requires (L+1) OSR clock cycles. This results in a significant latency. Incremental ADC is an alternative solution to overcome the long latency problem of Σ-Δ ADC for multi-channel sensor acquisition. Incremental Σ-Δ ADC was proposed in 1978 [63]. It is like a Σ-Δ ADC, but with a reset operation in Σ-Δ modulator and decimation filter. Σ-Δ ADC runs freely, while incremental Σ-Δ ADC is reset after a certain time interval. Figure 2.23 depicts block diagrams of Σ-Δ ADC and incremental Σ-Δ ADC. As seen by the Figure 2.23, the architecture of incremental ADC is similar to the Σ-Δ ADC and consists of a Σ-Δ modulator and digital decimation filter. In contrary to free running Σ-Δ ADC, the incremental ADC performs a periodic memory clearance by resetting both, the modulator and decimation filter. This leads to an independent sample-by-sample operation. Thanks to the reset operation, the loop continuity is broken in incremental ADC. As a result, the digital output code is contingent upon only on the input samples occurring within the conversion interval, which is highly desirable for multi-channel sensor applications. In addition, the reset operation of the incremental ADC prevents it suffering from idle tones [64].

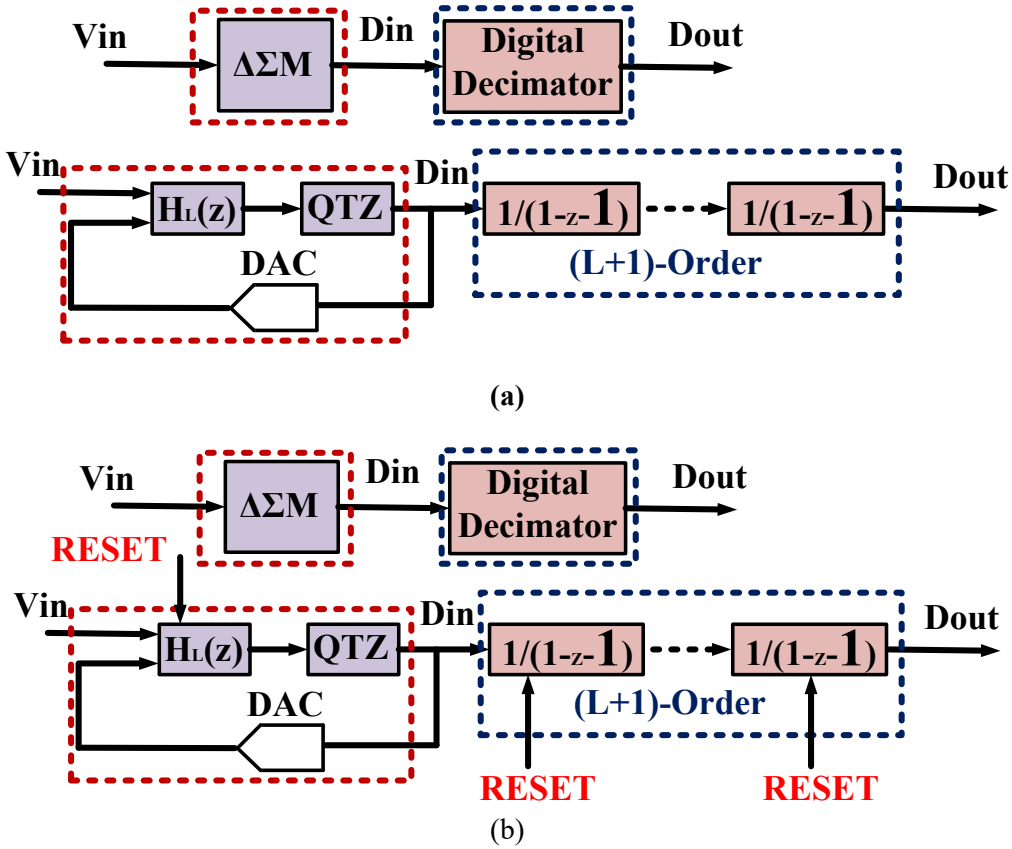


Figure 2. 23. Block diagram of (a) free running Σ-Δ ADC, and (b) incremental ADC with reset operation [64].

2.3.3. Hybrid ADCs

Nyquist-rate and oversampled ADCs have their own distinct advantages and constraints. SAR ADCs offer attractive advantages in terms of low power consumption, low profile, and low design complexity. However, they are constrained by their low-to-medium resolution and conversion-speed. Pipeline ADCs are characterized with high-speed and medium precision. However, the use of a large number of sub-stages in pipeline ADCs leads to high power consumption and design complexity. Σ-Δ ADCs are attractive candidates for achieving high accuracy and resolution. However, their use is limited to only high-precision and low-speed applications [52].

Keeping in view the advantages and limitations of the above-mentioned ADCs, a new class of hybrid ADCs has emerged recently. These ADCs are a merged version of two or more types of the above-mentioned ADCs and exhibit improved performance by exploiting the advantages and mitigating the drawbacks of the conventional ADCs. This section provides an overview of two such well-known and widely used ADC types: Noise-Shaping (NS) SAR and Zoom ADC. While numerous hybrid ADC architectures exist, the rationale behind selecting these two types is that both of these types can be attractive candidates for the space application – the focus of this thesis.

2.3.3.1 Noise-Shaping SAR ADC

With its first silicon implementation in 2012, NS-SAR ADC has drawn substantial attention from the researchers. NS-SAR ADC architecture exploits the advantages of area, and power-efficiency of a SAR ADC and high resolution of Σ-Δ ADC. This architecture emerged based on the fact that the residue voltage (V_{res}) at the CDAC node in a conventional SAR ADC (Figure 2.24) achieved at the end of the conversion

phase, based on the last comparison decision, is actually the sum of quantization error (Q_e) and comparator noise (n_{cmp}), as shown in signal flow graph of Figure 2.24. V_{res} can be defined as [65]:

$$V_{res} = Q_e + n_{cmp}$$

The digital output of a SAR ADC can be written as, using a signal-transfer-function (STF) and Noise-transfer-function (NTF),

$$D_{OUT} = NTF(Q_e + n_{cmp}) + STF.V_{in}$$

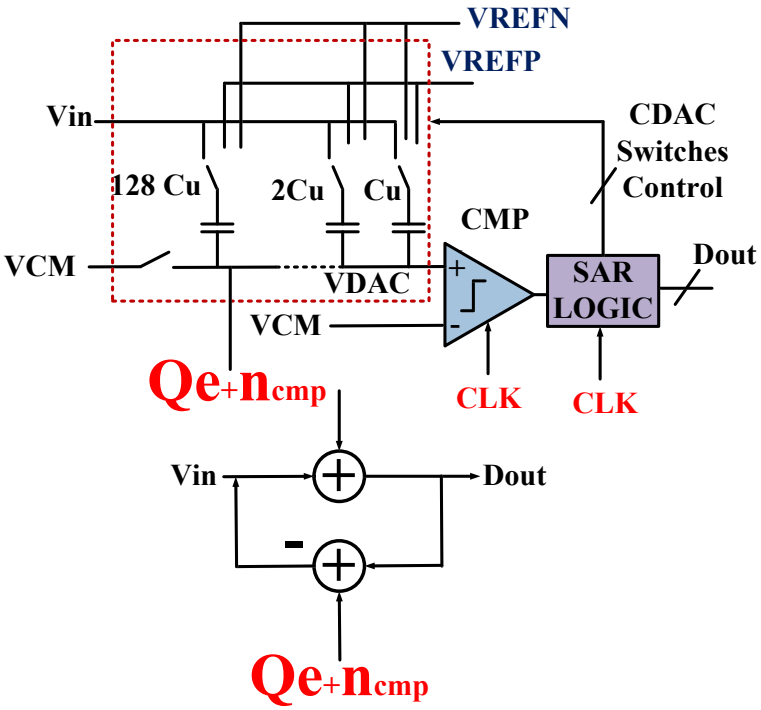


Figure 2. 24. Architecture of a SAR ADC with signal-flow-graph of V_{res} generation based on the last decision of the comparator.

There are two ways to implement NS-SAR ADC: Error-Feedback (EF) and Cascaded-Integrators-Feed-Forward (CIFF). The freely available V_{res}, if applied to the subsequent sampling phase of the SAR ADC, realizes a long-established Σ-Δ modulator with an inherent EF Noise-shaping. This, with a combination of oversampling, provides an enhanced performance (ENOB and SNDR). Besides quantization error, the NS-SAR shapes the comparator noise out of the band of interest. In addition, the $^{kT}/_{C}$ noise of CDAC is also shaped. The EF NS-SAR (Figure 2.26 (a)), is achieved by using a Finite-impulse-response- filter (FIR), which processes the V_{res} before feeding it back to the next sampling phase. With the FIR filter, it is possible to shape the noise only without the signal,

$$D_{OUT} = V_{in} + [1 - L_{EF}(z)].(Q_e + n_{cmp})$$

Where, $STF = 1$ and $NTF = 1 - L_{EF}(z)$

In CIFF NS-SAR ADC, the loop filter filters the V_{res} and feeds it forward to an additional input of the comparator, as shown in Figure 2.26 (b). Loope filter is realized by a cascade of FIR-IIR filter. For this implementation, following can be derived,

$$D_{OUT} = V_{in} + (Q_e + n_{cmp})\frac{1}{1 + L_{FF}(z)}$$

Where, STF $= 1$ and NTF $= \frac{1}{1+L_{FF}(z)}$

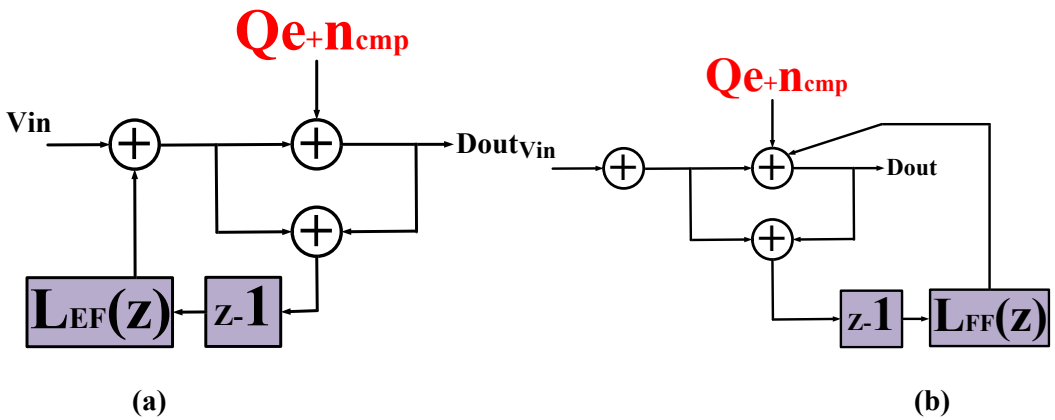


Figure 2. 25. Signal-Flow-Graph of (a) EF NS-SAR, and (b) CIFF NS-SAR ADC.

2.3.3.2 Zoom ADC

Zoom ADC is another widely used hybrid architecture, which is a combination of SAR and Σ-Δ ADCs taking advantages of both architectures. To get a high resolution, multi-bit Σ-Δ ADCs are normally utilized. The biggest drawback is that these ADCs need multi-bit quantizer, which increases area, power, and circuit complexity. The need for a new architecture emerges, which uses only a single quantizer in the Σ-Δ loop but achieves performance of a multi-bit quantizer by using some coarse ADC outside the loop. This can be achieved by the use of a two-step ADC: a low-resolution coarse ADC and a high-resolution one-bit fine Σ-ΔM, performing conversion on the residue quantization error of the coarse step. To get performance, it is important to get rid of the non-idealities of the coarse ADC and fine ADC (e.g., non-ideal DACs of both ADCs) judiciously in a new 2-step ADC architecture. Zoom ADC is such a new architecture [66].

Figure 2.27 shows a block diagram of a typical zoom ADC. To mitigate the errors caused by the non-ideal DACs as mentioned above, the zoom ADC combines two separate DACs into a single N-bit DAC. The N-input to the DAC is generated by the sum of k (output of a coarse N-bit ADC) and bs (1-bit bitstream of fine ADC). This avoids the need for an additional subtraction node to calculate the residue voltage. This multi-bit DAC has the same linearity, noise, and offset limitations as that of a DAC of a multi-bit Σ-ΔM. Consequently, techniques, such as dynamic element matching, can be applied to enhance DAC linearity. The N-bit coarse ADC has to be a SAR ADC due to its excellent energy-efficiency. However, the linearity of the coarse SAR ADC has to be of the level of final output code (N +M bits) [66].

Conceptually, zoom ADC can be thought of a 1-bit Σ-ΔM, whose DAC is tacking the signal. Alternatively, the ADC zooms-in to the small region around the signal in such a manner that the signal is always in between the positive and negative references of the DAC. Figure 2.28 shows the output voltage of the DAC of a zoom ADC for a sinusoidal input signal. The coarse ADC (5-bits SAR ADC in this example) tracks the input signal and then a modulation is performed by a 1-bit Σ-ΔM on top of the coarse quantization steps; the output accurately corresponds to the input signal after decimation. The internal signal swing of the fine Σ-ΔM is reduce because of the zoom-in operation. This results in relaxed requirements in terms of circuit performance and leads to reduced power consumption [67].

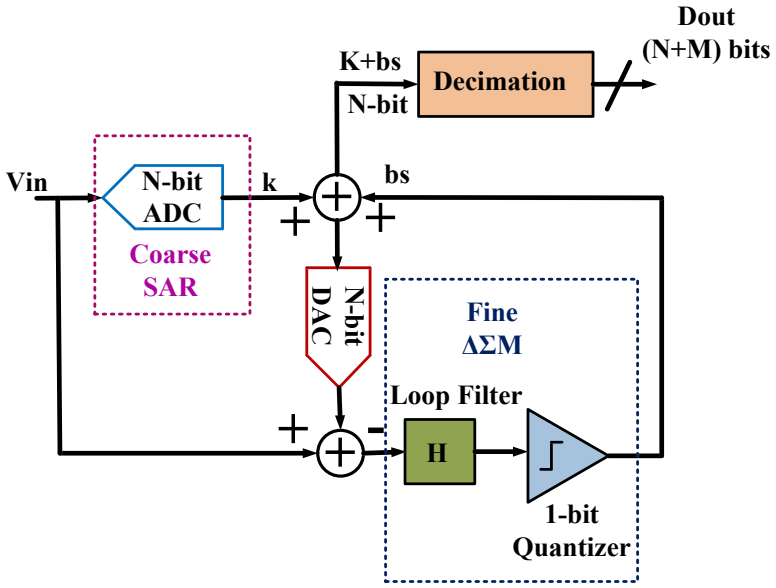


Figure 2. 26. Block diagram of a typical zoom ADC.

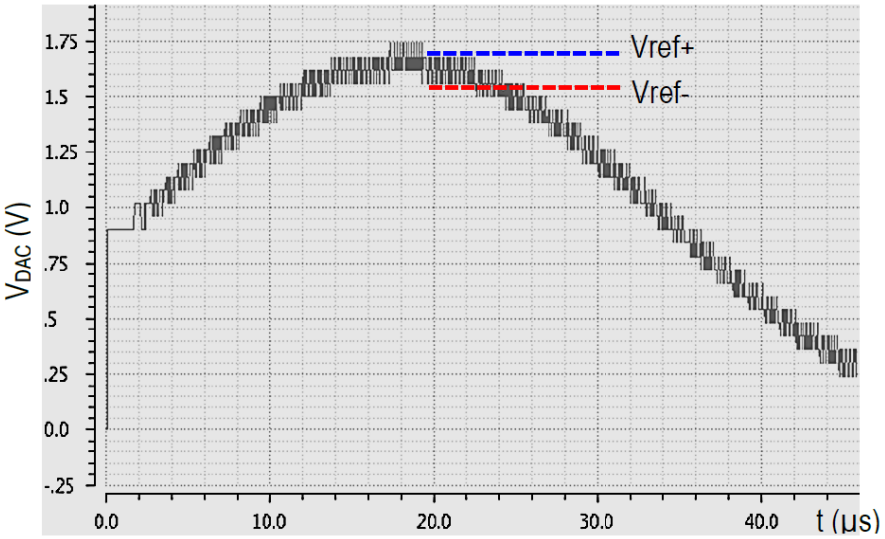


Figure 2. 27. Output voltage of a DAC part of an example zoom ADC [66].

2.3.4. A Brief Comparison of ADC Architectures with Respect to Targeted Application

Based on the literature review, Table 2.1 shows a comparative potentials and capabilities of the reviewed ADCs for the targeted application, i.e., multi-channel ASICs for space applications. It is clear from Table 2.1 that there is no single ADC type which meets all the specifications single-handedly needed for the application. Each ADC type poses its own tradeoffs for space application. Therefore, the selection of an optimized ADC topology becomes a challenging task. In addition, it becomes obvious that an innovation at architectural level is needed in one of these ADC types to enable it to accommodate the majority of the requirements for targeted application, thus clearly indicating a gap in the literature. Moreover, an extensive literature review on the already proposed ADC types for space applications is essential to explore and

examine their potentials and challenges as well as find a literature gap before a decision is made. The focus of the next section is exactly the same.

Table 2. 1. Comparison summary of ADCs keeping in view their potentials for the targeted application of the thesis

ADC Type	a	b	c	d	e	f	g	h	i	j
SAR	Low	Low-to-medium	Low-to-medium	Low	Medium-to-High	Medium-to-High	Medium-to-High	Low	Low	Medium
ASAR	Low	Low-to-medium	Low-to-medium	High	Low	Low	Low	High	Low	High
Pipeline	High	Low-to-medium	Low-to-medium	Low	High	High	High	Low	Low	Low
Flash	High	Low-to-medium	High	Low	High	High	High	Low	Low	Low
Subranging and 2-step	Medium	Low-to-medium	Low-to-medium	Low	Medium-to-High	Medium-to-High	Medium-to-High	Low	Low	Medium
Single and Dual-Slope	Medium	Low-to-medium	Low-to-medium	Low	Medium-to-High	Medium-to-High	Medium-to-High	Low	Low	Medium
Ramp	Low	Low-to-medium	Low-to-medium	Low	Medium-to-High	Medium-to-High	Medium-to-High	Low	Low	Medium
Time-interleaved	High	Low	High	Low	High	High	High	Low	Low	Low
ΔΣ	High	High	Low	Medium	High	High	High	Medium	Low	Medium
Incremental ΔΣ	High	High	Low	Medium	High	High	High	Medium	High	Medium
NS-SAR	Low	High	Low-to-medium	High	Low	Low	Low	Medium-to-High	Medium	High
Zoom	Low	High	Low-to-medium	Low	Medium-to-High	Medium-to-High	Medium-to-High	Low	Medium	Medium

a: Power; b: Resolution; c: Sampling-rate; d: Potential for sampling-rate reconfigurability; e: Switching-Noise; f: Crosstalk and interference; g: Clock Jitter; h: Event-triggered capability; i: Memory-less/Reset Operation; j: Flexibility.

2.4. ADCs for Space Applications: Prior State-of-the-art

Numerous ADC architectures have been proposed for space applications. This section provides an overview of such already proposed ADC topologies with a description of their pros. and cons.

2.4.1. Incremental ADC

In [68], the authors have proposed a single-channel, 12-bits, 2^{nd}-order incremental ADC for space exploration spectroscopy for multi-channel ASICs in a 0.35 µm CMOS technology at a supply voltage of 3.3 V. The proposed ADC is capable of performing an on-demand operation to reduce power consumption. Besides incremental mode, it also supports Σ-Δ mode operation to facilitate ADC testing. The ADC exhibits a maximum conversion-rate of 39 kHz, while it can adapt its conversion-rate as low as up to 100 Hz. This has been achieved by using different OSR values, i.e., it supports an OSR value of 128, 256, and 512. ADC secures an ENOB of 11.8 bits in measurements.

The major drawback associated with the proposed architecture is a high-switching external clock, i.e., a clock with a 10 MHz frequency is needed. Such a high-switching external clock can potentially cause high-switching noise when used in a multi-channel environment. In addition, clock distribution among different channels can lead to clock jitter and ill-synchronization issues. This can result in severe performance degradation. Another disadvantage with this solution is that it consumes a high on-conversion power, i.e., 3.64 mW for single-channel ADC. As three such ADCs are to be used per channel as per the ASIC requirements as described by the authors, this leads to a much high-power consumption contribution per channel, keeping in view the overall power consumption of the multi-channel ASIC. In addition, the input signal swing of the ADC is 1 V, i.e., 1.65 ± 0.5 V. As the ADC is using 3.3 V as its supply voltage, its input signal swing can easily be enhanced to 2 V, i.e., 1.65 ± 1 V in order to accommodate large input signal. Doing so in the proposed ADC will also result in further high-power consumption.

2.4.2. Pipeline ADC

A 10-bit, 50-MS/s pipeline ADC has been designed in 65 nm CMOS technology in [69] for high-energy cosmic rays detection. The topology consists of 5 stages: the first stage provides a resolution of 1.5 bits, while the other stages give a resolution of 2.5 bits per stage. Instead of using a dedicated sample and hold circuit, the input signal is sampled by the first stage directly to save power. The overall architecture consists of two main stages: these stages share OP-AMP to save power as well as utilized a 3-bit full-flash ADC. The ADC obtains a measured SNDR of 50.3 dB, an SNR of 52.3 dB, and SFDR of 59.2 dB.

High power consumption (12 mW at a supply voltage of 1.2 V) is the primary limitation of this architecture. Using it in a multi-channel environment will lead to substantial power consumption, which is not feasible for the majority of space applications. The need for a high-frequency external clock is its second disadvantage, which can potentially lead to high-switching noise as well as clock jitter when integrated into a multi-channel environment. This ADC solution is also not tunable with respect to its conversion-speed, which is a highly desired feature for space applications. In addition, it does not support an activity-driven operation.

2.4.3. Synchronous SAR ADC

In [70], a 12-bit synchronous/clocked SAR ADC has been presented in a 0.35 µm CMOS technology at a supply voltage of 3.3 V for Silicon drift detector read-out in space applications. The ADC input signal range is 1.7 V, while its sampling-rate is 0.87 MHz. It achieves an ENOB of 11.9 bits, SNDR of 73.8 dB, and consumes a mean power of 0.27 mW. This ADC architecture is constrained with few factors for space applications. First, the results presented are only simulation based. Second, it needs a high-frequency external clock because of its synchronous-SAR nature, which enhances chances of switching-noise. Third, its sampling-rate is fixed and cannot be tuned.

In [71, 72], the authors have proposed a 12-bit clocked charge redistribution SAR ADC, which is integrated on a multi-channel SDD readout IC. To reject common-mode noise and disturbances, a fully differential architecture has been chosen. The ADC has been implemented in a 0.35 µm CMOS process at a supply voltage of 3.3 V, and achieves a sampling-rate of 5 MS/s. The ADC achieves a good ENOB of 11 bits. The main limitations of this topology are the need for high-switching external clock, and an inability to configure its sampling-rate. The ADC with similar topology, but with slightly different specifications, has also been utilized for digitizing the data of a 16-channel readout ASIC for space applications in [12]. Also, a similar SAR ADC, with a modified specifications, is part of a 1-channel read-out ASIC for space applications in [15] and for 4-channel read-out ASIC in [14].

A 10-bit interleaved SAR ADC has been proposed in [73] for X-rays free electron lasers (FELs) detectors read-out applications- an application similar to space applications. The sampling-rate of the ADC is 2 MHz, and it is implemented in 65 nm CMOS technology at a supply voltage of 1.2 V. The ADC secures an ENOB of 9.05 bits, and SNR of 56.3 dB, consuming a power of 85 µW. Like other clocked SAR ADC, the drawbacks associated with this ADC include lack of sampling-rate reconfigurability, and high-frequency external clock. One radiation-hardened 14-bit, 50 KS/s SAR ADC has been presented in [74], which also faces the issues typical of clocked SAR ADCs for space applications, as mentioned above.

2.4.4. Wilkinson

In [16, 75], a 9-bit Wilkinson ADC architecture has been presented, which is integrated with a complete readout channel for X-ray spectroscopy in space applications. The ADC converts signals at a rate of 100-210 µs with the help of a clock frequency of 10 MHz. The ADC operates at a supply voltage of 3.3 V using a 0.35 µm CMOS process. The power consumption of the stand-alone ADC is greater than 8 mW. For a case of 16×16 array of channels with one ADC per channel, the total power consumption is 56 mW. The average power consumption of the ADC per channel is 0.4 mW. The primary drawback linked with this solution is its lack of sampling-rate reconfigurability. In addition, the power consumption of a single ADC

is high. Moreover, it uses a high-frequency external clock, which is not suitable from a switching-noise point of view for multi-channel integration.

An improved version of Wilkinson ADC has been proposed in [76], which is a 13-bit, 32-channel single-slope architecture. The conversion time of the ADC is 2.56 µs and its input signal range is 2 V. It has been implemented using a 0.35 µm CMOS process at a supply voltage of 3.3 V. A special method to mitigate the temperature effects on chip performance is also part of the design. In addition, the ADC is immune to single-events impacts owing to dedicated design methods. An on-chip Phase-Locked-Loop (PLL) generates clock with a frequency of 100 MHz using a reference clock of 1 MHz. The total power consumption of the ADC is 57 mW. The sampling-rate of the ADC can be reduced by reducing its resolution. The output data can be acquired in either serial mode or parallel mode. The major limitation of this ADC is the use of high-frequency external reference clock. In addition, its sampling-rate tuneability is coupled with its resolution, i.e., it cannot be achieved independently. Moreover, power consumption is also high.

An 8-bit Wilkinson-type ADC has been proposed in [77] for pixel-level integration, which can be a suitable candidate for multi-channel ASICs for space applications. It has been implemented in a 0.13 µm CMOS process at a supply voltage of 1.2 V. The conversion time of the ADC is 160 ns, and input signal range is 0.86 V. The ADC consumes 560 µW and secures an SNR of 65 dB. The ADC is equipped with circuitry to trim gain and offset. The limitations of this ADC for space applications are similar to previously mentioned Wilkinson ADCs. These include high-switching external clock (800 MHz), lack of conversion-speed tunability, and high-power consumption.

Table 2.2. summarizes the prior state-of-the-art ADCs for space applications. [21] provides guidelines for the selection and suitability of commercially available ADCs for space applications.

Table 2. 2. ADCs for space applications: prior state-of-the-art

Ref.	Type	Tech. (nm)	V_{DD} (V)	ENOB (Bits)	SNDR (dB)	f_s (MHz)	P_{avg} (mW)	Limitations
[68]	Incremental	350	3.3	11.86	73	0.039	3.640	1. High power; 2. External high-switching clock
[70]	SAR	350	3.3	11.9	73.8	0.870	0.270	1. External high-switching clock; 2. non-tunable f_s; 3. Only simulations
[71]	SAR	350	3.3	11		5	-	1. External high-switching clock; 2. non-tunable f_s
[12]	SAR	350	3.3	10.75	66.5	475	19	1. External high-switching clock; 2. non-tunable f_s
[14]	SAR	350	3.3	12		2	-	1. External high-switching clock; 2. non-tunable f_s
[72]	SAR	350	3.3	10.75	66.5	4	-	1. External high-switching clock; 2. non-tunable f_s
[15]	SAR	350	3.3	12		2.5	-	1. External high-switching clock; 2. non-tunable f_s
[16] [75]	Wilkinson	350	3.3	11		0.00470	11	1. External high-switching clock; 2. non-tunable f_s; 3. High power
[76]	Single slope	350	3.3	13		0.4	57	1. External high-switching clock; 2. No independent $f_s -$ turnability 3. High power
[77]	Wilkinson-type	130	1.2	8		6.25	0.560	1. External high-switching clock; 2. non-tunable f_s; 3. High power
[69]	Pipeline	65	1.2	10	50.3	50	12	1. External high-switching clock; 2. non-tunable f_s; 3. High power
[73]	SAR	65	1.2	9	56	2	85	1. External high-switching clock; 2. non-tunable f_s

2.5. Selected ADC Types

Based on the extensive literature review of ADCs in general as well ADCs for space applications in previous sections of this chapter, an asynchronous SAR ADC looks a promising candidate for the targeted application. It is well-known that the design of an ASAR ADC for a resolution of above 8-bit is extremely difficult without employing special techniques, such as calibration and mismatch shaping for the CDAC, offset cancellation of the comparator, etc. In addition, chip-area and power increases significantly with an increase in resolution. These result in a higher complexity of the design as well as a high failure probability-rate. Because of these reasons, it is judicious to design an 8-bit ASAR ADC first, and then enhance its resolution and SNDR by introducing noise-shaping into it as per the desired application. Following are the

details of the factors, reasons, and advantages behind ASAR ADC architecture selection for the targeted application.

2.5.1. Self-Clocked Topology

Unlike externally applied clocked ADCs, an asynchronous SAR ADC does not require a high-switching external clock. On the contrary, it only needs a low-switching 'start-of-conversion (SoC)' trigger signal to perform the conversion of the analog signal and generates all required clock signals internally. This feature makes it a self-clocked ADC topology. As a result, there is no need for a dedicated clock generation circuit to drive the ADC, thus saving power, area, and cost of the overall system. This advantage becomes extremely attractive while keeping in view the integration of a large number of such ASAR ADCs in a multi-channel ASIC environment.

2.5.2. Low-Switching Noise

Because of no need of a high-switching external clock, the asynchronous SAR ADC exhibits a low switching noise as compared to the ADCs who need high-switching external clock. Consequently, it does not require a circuitry devoted to mitigating switching-noise unlike clocked ADCs. This results in lesser system complexity, cost, area, and power.

2.5.3. Impervious to Clock Distribution Issues

Unlike ADCs who require external high switching clock, the asynchronous SAR ADC is largely impervious to issues associated with clock distributions, such as jitter. This feature is especially attractive in ASICs with multi-channels, where distribution of high switching external clock to all channels is not an ordinary task.

2.5.4. Sampling-Rate Tunability

The sampling-rate of an asynchronous SAR ADC is dictated by external 'end-of-conversion' trigger signal. Its duty-cycle as well as frequency can be controlled externally. This fact can be exploited to make it sampling-rate tunable. This feature becomes extremely attractive if the sampling-rate tunability is achieved along with scalable power consumption.

2.5.5. Sufficiently Large Conversion Speed

The conversion speed of an asynchronous SAR ADC is higher than a conventional clocked/synchronous SAR ADC. This is because the conversion speed of a synchronous SAR ADC is limited by external clock. Even if the comparator makes decision earlier, the speed cannot be made faster because of the operation controllability by the external clock. On the other hand, asynchronous SAR ADC does not pose this limitation because of its self-clocked nature, i.e., it is able to self-regulate its speed. In other words, its speed is limited only to the internal factors, such as CDAC settling, comparator speed, etc.

2.5.6. Event-Triggered/Activity-Driven Operation

The operation of the ASAR ADC commences with the arrival of the rising edge of the external 'start-of-conversion' signal. Without this signal, it does not perform conversion and remains idle. Thus, its operation is event-triggered. The introduction of conversion-rate tunability feature to the ASAR ADC will make it a true activity-driven ADC.

2.5.7. Low Power and Area

Asynchronous SAR ADC inherits all the benefits of a conventional clocked/synchronous SAR ADC. It is well-know that the SAR ADC topology is better in terms of power, area, and energy-efficiency than other ADC topologies for applications with low-to-medium conversion speed. In addition, it is a scaling-friendly architecture.

2.5.8. No prior Asynchronous SAR ADC for Space Applications

Besides the above-mentioned reasons, no ASAR ADC has been proposed for space application before this work as per the author's best knowledge despite its versatile benefits, as can be seen in Table 2.2. This gap in literature has also been one of the key factors behind selecting this topology for this thesis.

2.6. Asynchronous SAR ADCs: State-of-the-art

Numerous ASAR ADCs have been proposed in literature since its invention in 2006. This section summarizes some major trends in the design of ASAR ADCs and provides an outline of the state-of-the-art. The core components of an ASAR ADC include CDAC, comparator, SAR logic, Delay-cell, and Asynchronous clock generators. Some ASAR ADCs also include circuits to handle metastability issues of the comparator. This section divides the state-of-the-art of the ASAR ADCs into six different important aspects in order to achieve cohesion and coherence: (1) CDAC Switching Techniques, (2) Methods to implement SAR Logic, (3) Solutions with Metastability Watchdog Circuits, (4) The techniques to implement delay-cell, (5) Techniques to enhance speed, and (6) Others/hybrid.

2.6.1. CDAC Switching Techniques

In [78], a 10-bits ASAR ADC is presented, which uses a monotonic CDAC switching method for an improved energy-efficiency and small area. Compared to conventional switching method, the total capacitance and total switching power are reduced by 50 % and 81 %, respectively owing to the use of the proposed switching technique. Simulated in a 180 nm CMOS process, the proposed ASAR ADC achieves an ENOB of 9.9 bits, and a peak SNDR of 61.3 dB at 5 kHz f_s, consuming 1.43 µW at a supply voltage of 0.5 V. A 12-bit ASAR ADC is presented in [79], which uses a split-CDAC to reduce area and increase conversion speed. LSB dummy customized symmetrical unit capacitor is programmed to calibrate the CDAC linearity. Prototyped in a 65 nm CMOS process at a supply voltage of 1.2 V, the ADC secures a 10.17-bits ENOB at 100 MS/s f_s, while it consumes 0.8 mW. In [80], a 10-bit ASAR ADC is presented, which employs a CDAC monotonic switching scheme for an enhanced energy-efficiency. The three MSB bits of CDAC are split, which reduces the settling time of the MSB CDAC, increases ADC sampling-rate, reduces CDAC power consumption, and minimizes the comparator offset. Simulated in a 65 nm CMOS process at 1.2 V, the ADC gets an ENOB of 8.36-bits at 50 MS/s, while it consumes 2.79 mW.

A 12-bit ASAR ADC has been proposed in [81], which utilizes segmented CDAC and merged capacitor switching techniques to reduce area and power. To further reduce area and power, a floating inverter preamplifier-based comparator has been used. Simulated in a 180 nm CMOS process, the designed ADC secures 70.48 dB peak SNDR at 20 MS/s, while consumes 1.3 mW. In [82], a 12-bit ASAR ADC is presented, which employes an improved split-capacitor CDAC structure to reduce area, power and settling. The proposed CDAC consists of 2 stages, bridged by 2-unit capacitors with the high five capacitors equally divided. Simulated in a 65 nm CMOS process using a supply voltage of 1.2 V, the ADC secures a peak SNDR of 65.4 dB at 100 MS/s, while consuming 48 mW. A 7-bit ASAR ADC is presented in [83], which uses a 40 fF sampling capacitor, separate from CDAC capacitance to reduce input buffer load. In addition, it uses a non-binary-weighted split-capacitor array CDAC to relax settling and the effect of reference voltage fluctuations. Fabricated in a 28 nm CMOS process at 1 V supply, the ADC gets a peak SNDR of 36.5 dB at 430 MS/s, dissipating 2.52 mW.

A 10-bit ASAR ADC is presented in [84], which uses an improved energy-efficiency-based common mode charge redistribution algorithm for CDAC switching, reducing 12 % switching power compared to a merge capacitor switching method. To optimize energy efficiency, a 2-stage dynamic latched comparator with an adaptive power control has been proposed. A modified energy-efficient asynchronous SAR logic is also proposed to reduce digital power consumption. Designed in a 55 nm CMOS process at 1 V supply, the proposed ASAR ADC secures 9.3-bit ENOB at 8 MS/s, consuming 45 µW. In [85], a 9-bit ASAR ADC has been proposed, which uses a splitting monotonic switching method to a binary-weighted custom made unit capacitance-based CDAC to get a better switching energy-efficiency. The design proposes a dynamic

SAR memory circuitry instead of conventional SAR logic to reduce digital power. Fabricated in a 65 nm CMOS process at 1.2 V supply, the presented ASAR ADC achieves a peak SNDR of 47.6 dB at 222 MS/s, while it consumes 1.28 mW. A non-binary SAR algorithm-based 14-bit ASAR ADC is presented in [86]. Because the single voltage is present at CDAC for every DAC-code in a binary-weighted SAR algorithm, a comparison error because of the thermal noise makes it impossible to correct the wrong conversion if it happens. This issue has been solved with the utilized non-binary SAR algorithm in the proposed ADC. As the ADC uses an OSR of 4 to reduce data-rate needed for the targeted application (bio-signal acquisition-system), an on-chip low-power decimation filter is also part of the design. Fabricated in a 180 nm CMOS process at 1V supply voltage, the ADC secures a peak SNDR of 78.58 dB at 0.512 kHz, consuming 1.125 µW.

In [87], a 10-bit ASAR ADC is presented, which uses a monotonic CDAC switching method to reduce switching energy. An 81 % reduction in switching energy and 50 % reduction in CDAC capacitance have been achieved with the use of the proposed switching method in comparison with the traditional switching method. The signal-dependent offset is mitigated by the use of an improved comparator. Fabricated in a 130 nm CMOS process at 1.2 V supply, the designed ADC secures a peak SNDR of 57 dB at 50 MS/s, while it consumes 0.826 mW. A 10-bit ASAR ADC is implemented in [88], which utilizes a top-plate V_{CM}-based switching method for the CDAC to reduce switching energy. The input-dependent offset of the comparator is taken care of at the system level, thanks to the adopted switching scheme. A 90 % reduction in CDAC area has been obtained by the use of asymmetrical metal-oxide-metal capacitor for a given gain error. A modified SAR logic is also part of the design with a reduced switching activity. Fabricated in a 65 nm CMOS process at 0.9 V, the ADC secures an ENOB of 9.1 bit at 1 kS/s, while consuming 5.8 nW. An 11-bit ASAR ADC is presented in [89], which proposes a novel CDAC switching method for a single-ended SAR architecture for improved energy-efficiency. The proposed switching scheme reduces 50 % capacitance in CDAC as well as 87.5 % switching energy in comparison with traditional switching scheme. An error and offset cancelling network is part of the ADC solution. The input signal to the ADC is twice its reference voltage. The common-mode voltage of the design can also be used as its reference voltage. All the blocks have been designed in subthreshold regions to reduce power. Fabricated in a 180 nm CMOS process at 0.75 V, the ADC gets a peak SNDR of 60.5 dB at 10 kS/s, while consumes 250 nW power.

In [90], a 10-bit ASAR ADC is presented with a novel energy-efficient CDAC switching scheme. The proposed automatic algorithm-based switching scheme has been developed by exploiting the advantages of both, binary switching scheme as well as LSB-first successive approximation switching method. To mitigate the clock jitter issue for ASAR ADC, a clock-jitter compensation method is also part of the solution. In addition, the ADC is accompanied by a metastability detection and suppression circuitry. Fabricated in a 180 nm CMOS process at 1.2 V, the ADC shows a peak SNDR of 57.7 dB at 2 MHz and consumes 9.3 µW. In [91], a 9-bit ASAR ADC is presented, which adopts a top-plate based CDAC switching method for a split-capacitor CDAC. The design is implemented using low-V_t transistors in order to enable ADC's design at ultralow-supply. A fully dynamic comparator and bootstrapped circuit topologies are part of the solution. Designed in a 180 nm CMOS process at 0.5 V supply, the ADC secures an ENOB of 8.55-bits, while it consumes 48 µW. A 10-bit ASAR ADC has been proposed in [92], which proposes an energy-efficient splitting monotonic switching method for CDAC. The proposed scheme maintains the common-mode voltage during bit cycling, unlike some other CDAC switching methods. Fabricated in a 180 nm CMOS process, the ADC achieves an ENOB of 9.83-bits at 10 MHz, while consuming 98 µW.

A 12-bit ASAR ADC, presented in [93], uses a split capacitor array CDAC to reduce area and power consumption. The used comparator is equipped with an offset cancellation method. Designed in a 350 nm CMOS process, the ADC secures an ENOB of 11.05-bits at 99 kHz, while consuming 6.8 µW. A 9-bits ASAR ADC, proposed in [94], uses monotonic switching scheme to reduce switching energy. For linearity boost, a two-stage comparator with a current source has been used. A modified sample and hold circuit with a reduced body-effect is also part of the design. Simulated in a 28 nm CMOS process at 1 V, the ADC achieves an ENOB of 8.84-bit at 50 MS/s, consuming 45 µW. A 10-bit ASAR ADC of [95] uses a hybrid

R-2R/C-3C DAC to reduce area and switching power of the ADC. The ADC uses a 2b/step technique with the help of the proposed hybrid DAC to increase conversion time. To save comparator area occupation, an interpolation-assisted time-domain 2b comparison scheme has been proposed. In addition, a dual-edge comparison strategy is part of the design, which halves the comparator switching activity. Designed in a 180 nm CMOS process at 0.6 V supply, the ADC secures 9.2-bits ENOB at 100 kS/s, while consuming 390nW. An 8-bits ASAR ADC [96] adopts a resistor-capacitor DAC array to reduce area, and improve linearity. Simulated in a 65 nm CMOS process at 1.2 V, the ADC secures an ENOB of 7.8-bits at 10 MS/s.

A set-and-down switching scheme is presented for a10-bit ASAR ADC [97], which reduces CDAC total capacitance, its setting time, and power consumption. To further relax the settling requirements, a redundant tree algorithm with a sub-binary radix is proposed. The use of a dynamic comparator with a dynamic SAR logic further reduces the power. Fabricated in a 65 nm CMOS process at 1.2 V supply, the ADC gets a peak SNDR of 56.2 dB at 100 MS/s, consuming 3.1 mW. An 8-bit ASAR ADC [98] uses a split-capacitor CDAC to reduce area and power. The ADC is able to work in a single-ended as well as differential mode with the use of 3 bootstrap switches. Simulated in a 65 nm CMOS process at 1.2 V, the ADC secures a peak SNDR of 49.55 dB at 40 MHz sampling-rate, consuming 2.26 mW. A set-and-down CDAC switching method has been utilized for an 8-bit ASAR ADC [99]. Analog calibrations have been used to correct offset mismatches. In addition, the use of a double-tail dynamic comparator saves energy. Simulated in a 40 nm CMOS process at 1.1 V, the ADC secures a peak SNDR of 44.75 dB at 500 MS/s sampling-rate and consumes 0.61 mW.

2.6.1. Methods to implement SAR Logic

In [84], a 10-bit ASAR ADC proposes a modified energy-efficient SAR logic to reduce digital power consumption of the ADC. Instead of providing a fixed delay to the internal clock for each conversion cycle as in the case of conventional ASAR logic, the proposed method introduces a variable delay for MSB to LSB comparisons. The delay is controlled externally by digital bits. The proposed dynamic logic is simple and consumes lesser current. Fabricated in a 55 nm CMOS process at 1 V supply, the proposed ASAR ADC secures 9.3-bit ENOB at 8 MS/s, consuming 45 μW. The authors have proposed a SAR memory to replace conventional SAR logic in a 9-bit ASAR ADC in [85]. This has been enabled by the use of a splitting monotonic switching method of the CDAC. The SAR memory has been implemented in a state-machine based approach. Each cell of SAR memory uses dynamic logic to reduce power and improve speed. The ADC has been designed in a 65 nm CMOS technology at a supply voltage of 1.2 V and secures a peak SNDR of 47.6 dB at a sampling-rate of 222 kHz and consumes 1.28 mW.

In [100], a novel ASAR logic is presented, which is based on modelling the SAR logic using signal transition graphs, unlike the traditional SAR logic which depends on clocks to control conversion process of the ADC. Th proposed ASAR logic method is modular with the help of handshaking protocol, enabling the ASAR ADC construction based on single bit control unit. The systematic ASAR logic-based SAR ADC features low-power in comparison with the traditional SAR logic-based ADCs. Monotonic and V_{CM} switching methods based ASAR ADCs have been tested by the proposed technique. Measured results show that the proposed ASAR logic-based ADCs have power consumption which is at least one order of magnitude lesser than the traditional SAR logic-based designs. In [101], a ring-oscillator-based timing generator circuit has been proposed for data and power converters applications with an aim of reduce power in comparison with conventional logic circuits consisting of flip flops, latches, and delay-cell. The proposed timing generator has been applied to a SAR ADC to verify its efficacy. As per simulation results, the proposed timing circuit gets 5.8× reduction in SAR ADC's power consumption compared to conventional logic circuits.

2.6.3. Solutions with Metastability Watchdog Circuits

In [102], the authors have proposed a method to minimize the metastability errors in ASAR ADCs. The proposed method avoids the disadvantages associated with the traditional metastability mitigation methods, such as extra metastability errors due to detector circuit itself, reduced speed, additional delay in logic, and

detection of metastability for each bit. The proposed technique uses the outputs of comparators to detect whether a metastability event has occurred or not, instead of detecting a particular bit where metastability has occurred. Extensive simulations for an 8-bits ASAR ADC show that the proposed method eliminates the errors with half-range error amplitude and reduces the number of metastability errors for other error amplitudes. Except 1 and 2 LSB, the probability of all other error amplitudes is reduced by more than one order.

A circuit to detect the sparkle-codes, caused by the comparator metastability errors, is part of 6-bit ASAR ADC designed in [103]. The circuit also corrects the sparkle-codes errors to prevent ADC performance degradation. The proposed method detects the sparkle-codes bits and stores them in pulse latches for later correction of these codes in the digital backend. Fabricated in a 28 nm FDSOI CMOS process, the designed ADC secures a peak SNDR of 25.3 dB at 46 GS/s and consumes 381 mW from 1.05/1.6 V supply.

A metastability detection circuit is part of a 6-bit ASAR ADC in [104]. A simple logic has been utilized to track metastability occurrence by observing comparator clock. If comparator clock does not change after a certain time-threshold amount, metastability circuit comes into play and stops the conversion, forcing fixed digital 1 followed by all other bits to 0. Designed in a 40 nm CMOS technology, the ADC gets a peak SNDR of 31.2-bit at 1.33 GS/s, consuming 7.52 mW at 1.1 V.

In [105], a metastable-then-set approach is presented for a two-channel ASAR ADC. The approach sets all unresolved codes, due to metastability occurrence, on chip and completes the conversion when metastability is detected. This avoids conversion speed reduction because of metastability and eliminates unnecessary decision cycles. To minimize crosstalk between two channels, a flag synchronization method has been used. Designed in a 130 nm CMOS process at 1.2 V supply, the ADC gets a peak SNDR of 51.3 dB at 17.5 MS/s, while consuming 570 μW.

A metastability detection technique is presented for a 10-bit ASAR ADC [106]. The circuit ensures providing the internal clock to the comparator in case of metastability detection. The metastability is detected by waiting for the internal clock for the comparator for a delay amount which is equal to comparator regeneration time for an input difference of 1 LSB. Designed in a 130 nm CMOS process at 1.2 V, the ADC secures an ENOB of 9.32-bits at 20 MS/s, consuming 0.62 mW.

In [107], a metastability detection scheme is accompanied by a 10-bit ASAR ADC. A timer circuit has been used to provide extra time for the conversion in case of metastability events. Prototyped in a 180 nm CMOS process, the designed ADC achieves an ENOB of 8.95-bit for sampling-rates range of 100-500 kS/s, consuming proportionate power according to the sampling-rate because of the use of scalable supply for different sampling-rates.

2.6.4. The techniques to implement delay-cell

In [108], a tunable delay-cell has been proposed for a 10-bit ASAR ADC to cater for the PVT variations introduced by the use of a low voltage (0.9 V) for the ADC design. The delay value, provided to the internal clock going to the SAR logic, is controlled by the use of a 3-input decoder. Simulated in a 110 nm CMOS process using a 0.95 supply voltage, the ADC secures a peak SNDR of 58.4 dB at 0.2 MS/s, while it consumes 2.24 μW.

A variable delay-cell has been proposed for a 10-bit ASAR ADC [84]. This externally controlled variable delay-cell provides a variable delay to the internal clock for MSB to LSB bits comparison to reduce power consumption. The ADC has been designed in a 55 nm CMOS technology and achieves an ENOB of 9.4 bits and consumes 45 μW at 1 V supply.

In [109], an 8-bit ASAR ADC is presented without an on-chip clock generation circuit. The digital control logic has been realized using a delay line comprised of a cascade of monostable, which exhibits good PVT-

robustness. The control logic has been implemented in static CMOS logic. Simulated in a 350 nm CMOS process, the designed ADC achieves a peak SNDR of 48.2 dB at 5 kHz.

In [110], a 10-bit ASAR ADC is presented, which enables a timing-calibration-free asynchronous operation by using a clock-to-Q delay compensator with scalable supply voltages. Analog and digital sections of the ADC operate at different supplies to get a power-efficient operation. Compared to all blocks working at single 0.4 V supply, the power consumption of SAR logic has been reduced by 37 % when using 0.6 V as analog supply and 0.35 V as digital supply. The ADC uses a current-biased dynamic comparator to enhance ADC performance. Prototyped in a 180 nm CMOS process at 0.6 and 0.35 V supplies, the ADC achieves an ENOB of 9.50-bit at 20 kS/s, while it consumes 112 nW.

A variable and asymmetrical delay-line is part of a 7-bit ASAR ADC [111], which optimizes the timing for the digital and analog sections. The delay line delays only the falling edge of the input signal clock. An external voltage can control the delay value. Simulated in a 65 nm CMOS process at 1 V, the ADC secures an ENOB of 6.8-bits at 50 MS/s, consuming 157 μW.

2.6.5. Techniques to enhance speed

An 8-bits ASAR ADC is presented in [112], which performs a 2-then-1 bit/cycle conversion to enhance the ADC speed. The proposed method uses 3 comparators to get 2-then-1 bit/cycle conversion. To mitigate comparators offset, an offset mismatch calibration method has also been proposed. Simulated in a 40 nm CMOS process, the presented ADC secures an ENOB of 7.6 bits, consuming 3.95 mW.

In [113], an ASAR ADC performs a 3-bit/cycle conversion to enhance ADC speed by using an asynchronous ping-pong based quantization method. The proposed quantization method relaxes the settling requirements of reference voltages, enables the use of loop-unrolled technique to get further high-speed without an extra hardware overhead, and corrects comparator offset in background mode without an extra calibration phase. Simulated in a 22 nm CMOS process, the proposed ADC secures a peak SNDR of 33.4 dB, which can be enhanced to 47.2 dB with the use of offset calibration. The ADC consumes 2.1 mW power.

A 6-bits ASAR ADC is presented in [114], which uses a 2b/cycle conversion to increase speed. In addition, the 32-way time-interleaving has been used to get high-speed operation. The time-interleaver uses 8 sampling-and-hold amplifiers and each of these drives 4 sub-ADCs. Adjustable delay lines have been used to mitigate clock skew issues. Fabricated in a 28 nm CMOS process, the designed ADC secures an ENOB of 4.38 bits at 48 GS/s, while consuming 72.3 mW.

In [115], an ASAR ADC proposes an ASAR logic to enhance ADC speed. The logic is based on a two-phase handshaking architecture, which reduces the delay of a single conversion by 47 % compared to conventional method. The ADC uses a V_{CM}-based CDAC switching method with a 1-bit redundancy. Simulated in a 90 nm CMOS process using 1.2 V supply voltage, the presented ADC shows a peak SNDR of 36.2 dB at 500 kS/s, while it consumes 0.99 mW power.

In [116], the authors have proposed an ASAR based flash ADC to enhance conversion speed. The ADC consists of a loop-unrolled ASAR ADC and a reference-embedded 8× interpolating flash ADC. The architecture uses dynamic complementary amplifiers in a dual-edge manner to achieve 8-bits resolution with only 4 amplifiers and one CDAC, thus reducing the area and power consumption, while increasing bandwidth. Fabricated in a 28 nm CMOS process using a 1.1 V, the ADC secures a peak SNDR of 45.5 dB at 1 GS/s, while consuming 2.55 mW.

In [103], a 6-bit ASAR ADC is presented, which is 72-way time-interleaved hierarchically with the use of cascode samplers to get high-speed. The design is also accompanied by a sparkle-code, induced due to comparator metastability, detection and correction circuit. Foreground calibration has been used for gain

and offset mismatches correction. Fabricated in a 22nm FDSOI CMOS process, the designed ADC achieves a peak SNDR of 25.2 dB at 46 GS/s, while consuming 381 mW.

In [117], the authors have proposed a 12-bit ASAR ADC with a speed-enhanced comparator. The conversion speed of the comparator has been increased by introducing a positive feedback loop to it. The loading of the comparator and delay of SAR logic has been reduced by the use of a true-single-phase-clock latch. To overcome PVT variations, a variable delay-unit is also part of the design. Simulated in a 130 nm CMOS process, the ADC gets an ENOB of 11.46 bits at 16 MHz, while it consumes 4.95 mW.

A 6-bit ASAR ADC is presented in [115], which uses a two-phases handshaking architecture to enhance SAR logic speed. Each cell of the SAR logic consists of a static logic gate and a SARM-latch. The ADC uses a V_{CM}-based switching scheme for CDAC with 1-bit redundancy to reduce switching energy. Simulated in a 60 nm CMOS process at 1.2 V, the ADC gets a peak SNDR of 36.3 dB at 500 kS/s, consuming 0.99 mW.

In [104], a single-channel, 6-bit ASAR ADC is presented, which proposes an additional method to enhance conversion speed besides using asynchronous SAR logic. Instead of using only one comparator, the proposed method uses N-comparators for an N-bit conversion, which stores the comparison result of each bit within digital output of each comparator. The proposed method can enable the ADC to get a scalable resolution. The design is also equipped with a metastability detection circuit. Designed in a 40 nm CMOS technology at 1.1 V, the ADC gets a peak SNDR of 31.2-bit at 1.33 GS/s, consuming 7.52 mW.

In [118], an 8-bits ASAR ADC is presented. The ADC uses 2-b/step conversion to increase conversion speed. In addition, it utilizes a resistive-capacitive DAC to reduce loading effect and reference settling time. To further speed-up the ADC conversion, it adopts monotonic switching scheme as well as uses quartered reference. Designed in a 28 nm CMOS process at 1 V supply, the ADC secures a peak SNDR of 45.2 dB at 750 MS/s, consuming 4.5 mW.

A single-channel, 6-bit ASAR ADC is presented in [119], which introduces a technique to reduce feedback delay to enhance conversion speed. Unlike single quantizers in a traditional SAR ADC, the proposed design uses multiple quantizers for each conversion bit, which are driven by an asynchronous clock. The proposed method is attractive for time-interleaved SAR ADCs. Least Mean Square (LSM) calibration is also part of the design. Designed in a 40 nm CMOS process at 1.1 V, the ADC secures a peak SNDR of 31.3 dB at 1.33 GS/s, while it consumes 7.52 mW.

To enhance speed for a single-channel 8-bit ASAR ADC of [120, 121], the authors have proposed a method to relax comparator reset timing by using two comparators, which works in an alternative manner. A calibration method is added to mitigate comparator noise and offset. A logic stores the comparator decisions, which also servs to drive SAR logic. Fabricated in a 32 nm CMOS process, the ADC secures a peak SNDR of 38.8 dB at 1 GS/s, consuming 2 mW.

In [122], the authors have proposed a single-channel 6-bit ASAR ADC with a 3b/stage conversion scheme for speed enhancement using only 2 stages and a resistive DAC. A four-input dynamic comparator has been used for the design to accommodate differential inputs. Fabricated in a 65 nm CMOS process at 1 V supply, the ADC achieves a peak SNDR of 30.02 dB at 410 MS/s, consuming 2.03 mW.

An improved speed latched-based comparator has been proposed in [123] for ASAR ADC. The comparator removes the dead time needed for the reset phase of the comparator in the differential input stage. The proposed comparator has been used for the design of an 8-bits ASAR ADC in 180 nm CMOS process for verification purposes. The results of proposed comparator based ASAR ADC are compared with standard comparator based ASAR ADC. Simulation results show that the proposed comparator performs better than traditional comparator with respect to speed and power.

In [124], a 12-bit ASAR-based time-interleaved ADC is presented. A 2-channel time-interleaved architecture has been adopted for high conversion speed. To relax CDAC settling time, a settling-while-conversion scheme has been used. To reduce comparator noise, a gain boosting dynamic pre-amplifier has been proposed, whose speed has been increased with the help of an asynchronous decision. Internal clock generator generates clock in two modes: in mode 1, it generates a low-jitter fixed-width sampling pulse for high frequency operation, while in mode 2, it generates a low-quality clock at the benefit of low power for low frequency operation. Designed in a 65 nm CMOS process at 0.6 V, the ADC secures 10.4-bits ENOB at 10 MS/s and consumes 83 μW.

To enhance the speed, a 6-bit ASAR ADC uses a comparator-reused-based architecture [125] as an alternative of binary-search, and flash ADCs. The method ensures lesser number of comparators than binary-search and flash ADC based technique. The comparator selection and activation, one at a time, is done by the use of a selection logic. To allocate reference voltage to the selected comparators during the conversion process, a smart switching network is proposed. Simulated in a 180 nm CMOS process at 1.8 V, the ADC gets a peak SNDR of 36.02 dB at 330 MS/s, consuming 0.65 mW.

2.6.6. Others/Hybrid Solutions

In [126], a 10-bits ASAR ADC is presented, which uses a time-domain comparator to reduce the noise. To compensate for the low-sampling-rate because of the use of a time-domain comparator for 3-bit fine comparison, a double-tail comparator has been used for 7-bits coarse comparison besides asynchronous SAR logic. Simulated in a 180 nm CMOS process using a supply voltage of 0.6 V, the proposed ADC achieves an ENOB of 9.13 bits at 400 kS/s f_s.

In [127], an inverter-based 2nd-order CT bandpass Σ-Δ ADC is proposed, which utilizes a 5-bits ASAR ADC as quantizer. Inverter-based amplifier replaces the conventional OP-AMP in an integrator configuration in Σ-Δ ADC, making the architecture scaling-friendly. ASAR ADC uses monotonic switching method to reduce power and area. A current-steering CDAC has been used to minimize thermal noise. Fabricated in a 28 nm CMOS process at a supply voltage of 1 V, the proposed Σ-Δ ADC secures a peak SNDR of 58 dB at 30 MHz bandwidth, consuming 2.5 mW.

In [128], the authors have presented a 6-bit asynchronous charge-injection SAR ADC to get high-speed operation. The solution solves the major constraints faced by the traditional charge-injection SAR ADC, such as high input sampling capacitance and thus large area occupation, performance degradation due to PVT variations, and input dependent offset of the comparator. The design achieves a 95 % reduction in sampling capacitance compared to traditional charge-injection SAR ADC by the use of current reduction technique. In addition, the ADC has been made PVT-robust by introducing a replica-based feedback loop. Designed in a 28 nm CMOS process, the ADC secures a peak SNDR of 35.2 bits at 1.1 GS/s, while consuming 1.32 mW.

A semi-synchronous 8-bit SAR ADC is presented in [129] to enhance the conversion speed in comparison with an ASAR ADC. The proposed ADC employs a delay-locked-loop for clock generation. The method uses different delays for different bit decisions, leading to a variable CDAC settling time. Simulated in a 180 nm CMOS process at 1.8 V supply, the ADC secures a peak SNDR of 49 dB at 70 MS/s, consuming 2.8 mW.

In [130], a 12-bit sub-range ADC is presented which uses an ASAR ADC with a 1st-order CT incremental ADC. The aim is to get power-efficiency benefit of SAR topology and low-speed & high-accuracy advantages of incremental topology. In addition, the combination of these two architectures saves CDAC area in comparison to conventional SAR ADC for the same resolution. Simulated in a 65 nm CMOS process at 1.2 V supply, the ADC achieves a peak SNDR of 72 dB at 62.5 MHz, while it consumes 1.6 mW.

A 14-bit ASAR ADC has been proposed in [131]. To reduce the total capacitance, area and parasitics, the CDAC has bene implemented as a binary-weighted attenuation capacitor topology, featured with a

mismatch-insensitive layout arrangement as well as shielded unit-capacitance. A foreground calibration method is part of the design to compensate the CDAC mismatches. A preamplifier is used before the comparator to reduce kickback noise, which is turned on only when needed to save power. Designed in a 350 nm CMOS process using 1.8 V supply, the ADC secures an ENOB of 11.45-bits at 100 kS/s, while consuming 43.4 µW.

An 8-bit ASAR ADC is presented in [132], which offers a power-efficient solution for wide sampling-rates range, i.e., between 10 kS/s and 10 MS/s. The CDAC is binary-weighted with custom designed unit capacitor. To reduce leakage, a dynamic comparator with selectively high-V_t devices have been proposed. Fabricated in a 90 nm CMOS process at 1 V supply, the ADC secures an ENOB of 7.8-bit at 10.24 MS/s, while it dissipates 69 µW.

In [133, 134], an 8-bit ASAR ADC is proposed, whose power consumption scales proportional to its sampling-rate. All the blocks are dynamic without DC biasing for proportional power consumption with the sampling-rate. Fabricated in a 90 nm CMOS at 1 V, the ADC gets an ENOB of 7.7-bit at 10.24 MS/s, while consuming 26.3 µW.

In [135], an 8-bits conversion-speed scalable ASAR ADC, with a constant energy-efficiency across all covered conversion-speeds, is presented. Instead of a charge-distribution CDAC, a charge sharing CDAC has been utilized for a linear scale up of power with ADC speed. Designed in a 180 nm CMOS process at 1 V, the ADC secures an ENOB of 7.52-bits at 4 MS/s, while consuming 28.4 µW.

An 11-bit ASAR ADC with an embedded passive gain is presented in [136, 137]. Passive gain of 2× is embedded in sampling capacitor network as part of the SAR conversion prior to the comparator. This reduces comparator noise and improves speed and power of the overall ADC. Prototyped in a 65 nm CMOS process at 1.1 V, the proposed ADC gets an ENOB of 10.2-bit at 95 MS/s, while consuming 1.36 mW.

In [107], the authors have proposed a 10-bit ASAR ADC with a scalable conversion time. To scale power consumption accordingly, the supply voltage of the ADC is scaled according to the conversion speed. A metastability detection circuit is also part of the solution. Monotonic switching scheme has been used to get low switching power of the CDAC. Because of a low-supply voltage, a triple-latched comparator has been used. Designed in a 180 nm CMOS process, the designed ADC achieves an ENOB of 8.95-bit for sampling-rates range of 100-500 kS/s, consuming proportionate power according to the sampling-rate because of the use of scalable supply for different sampling-rates.

In [138], a 3-stage asynchronous 8× pipeline-SAR ADC is presented, which uses open-loop amplifiers in the integrators to maximize the sampling-rate, resolution, and linearity. To reduce power and rea, the design uses dynamic circuits. Foreground and background calibrations are part of each sub-ADC. Designed in a 16 nm process, the ADC secures a peak SNDR of 57.3-bits at 4 GS/s, consuming 513 mW.

A 5-bit ASAR ADC is part of a zoom ADC architecture as a coarse ADC [139, 140]. Besides ASAR ADC, zoom ADC architecture consists of a 2nd-order 1-bit Σ-ΔM as fine ADC. Both the ADC uses same sampling-rates, but separate CDACs. A pre-amplifier-based comparator is used for ASAR ADC. Fabricated in a 160 nm CMOS process at 1.8 V, the zoom ADC gets a peak SNDR of 118.1 dB at 2 MHz, consuming 280 µW.

In [141], a time-interleaved 8-bit ASAR ADC is presented. The proposed architecture does not need any sampling buffers, thus reducing significant power consumption. The architecture consists of 4 front-end sampling switches, and 8 ASAR ADCs. The design avoids static current consumption to get high energy-efficiency. Fabricated in a 130 nm CMOS process at 1.2 V supply, the ADC secures a peak SNDR of 44.6 dB at 3.2 GS/s sampling-rate, consuming 105 mW.

A 5-bit ASAR ADC has been used a as coarse ADC in a CT zoom ADC [142], which uses a 3rd-order CT 1-b Σ-ΔM as fine ADC. Fabricated in a 160 nm CMOS at 1.8 V, the CT zoom ADC gets a peak SNDR of 106.4 dB at a sampling-rate of 5.12 MHz, consuming 618 µW.

Table 2.3 provides a summary of the prior state-of-the-art ASAR ADCs.

Table 2. 3. Summary of ASAR ADCs proposed in the prior state-of-the-art

Ref.	Tech. (nm)	Supply (V)	Res./ENOB (Bits)	f_s (MHz)	DNL (LSB)	INL (LSB)	P_{avg} (µW)	FoM_S (fJ/C-step)	Area (mm^2)	Comments
[78]	180	0.5	10/9.9	0.005	-	0.4/+0.3	1.43	143.08	-	Monotonic switching technique; only simulations
[126]	180	0.6	10/9.13	0.4	-0.46/+0.4	-0.49/+0.66	-	94	-	Tome-domain comparator for 3-bits fine comparison; double -tail comparator for 7-bits coarse comparison; simulations only
[112]	40	1.1	8/7.6	500	-	-	3950	43.46	-	1-then-1 bit/cycle; background offset calibration
[113]	22	0.8	8/7.9	1000	-	-	2100	11.2	-	3b-cycle conversion; offset calibration; ping-pong-based quantization
[79]	65	1.2	12/10.17	100	-1/+2.36	-1.77/+1.43	0.8	17.6	0.029	Split-CDAC; Programable LSB dummy unit-cap for CDAC calibration
[114]	28	1/1.1	6/4.38	64000	-	-	72300		0.1265	2b-cycle; TI-ASAR; One of the highest speeds
[80]	65	1.2	10/8.36	50	-	-	2790	169	0.105	Monotonic switching; Split CDAC with 3 MSB capacitor; Simulated only
[81]	180	1.8	12/12	20	-	-	1300	-	-	Segmented CDAC with merge capacitor switching; FIA-based comparator
[82]	65	1.2	12/10.6	100	-	-	4800	31.	0.038	Improved Split-CDAC; Simulations only
[127]	28	1	10/9.34	60	-	-	2500	38.6	0.04	Inverter-based CT ΔΣ ADC with 5-bit ASAR quantizer
[83]	28	1	7/5.77	430	-0.59/+0.63	-0.4/+0.55	2520	107	0.00798	40 fF separate sampling-cap; split-CDAC
[84]	55	1	10/9.3	8	-0.9/+0.8	-1/+0.84	45	8	0.190	Improved CDAC switching method; comparator with power control; ASAR logic with variable controlled delay for LSB and MSB comparisons
[85]	65	1.2	9/7.6	222	-1/+0.5	-1.4/+1.4	1280	29.6	0.017	Split CDAC switching method; Dynamic SAR memory instead of SAR logic
[108]	110	0.95	10/9.41	0.2	-	-	2.24	16.46	0.049	Variable delay-cell to cater for PVT variations;
[115]	90	1.2	6/5.72	0.5	-0.30/+0.38	-0.34/+0.24	990	-	0.016	Two-phase handshaking-based SAR logic; V_{CM}-based CDAC switching
[116]	28	1.1	8/7.36	1000	0.59	0.82	2550	16.6	0.0056	ASAR-based 8× flash; reuse of complementary dynamic amplifiers
[128]	28	1.1	6/5.5	1100	-	-	3150	25.5	0.0024	Charge-injection ASAR ADC;
[100]	65	1	10/10	70/75	-	-	16	-	-	Editable ASAR control logic to reduce power consumption
[103]	28	1.05/1.6	6/4	46000	-	-	381000	560	0.14	72× TI ASAR; Metastability detection and correction circuit; offset and gain calibration
[86]	180	1	14/12.8	1.024e-3	-0.5/+0.6	-16.64/25.39	1.125	158.2	0.349	Non-binary SAR Algorithm;
[129]	180	1.8	8/7.9	70	-	-	2800	174	-	A semi-synchronous SAR to improve ASAR speed;
[109]	350	-	8/7.8	0.005	-0.1/+0.1	-0.1/+0.1	2	-	-	Monostable delay-based digital logic

[87]	130	1.2	10/9.18	50	-0.63/0.91	-1.36/+1.27	826	29	0.052	Monotonic CDAC switching method
[88]	65	0.9	10/9.1	0.001	-0.62/+0.59	-0.41/+0.89	0.0058	10.94	0.046	V_{CM}-based CDAC switching;
[89]	180	0.75	11/9.76	0.005	-0.37/+0.6	-0.89/+0.94	0.250	28.8	0.13	Energy-efficient CDAC switching for singe-ended architecture; Subthreshold design; error-and-offset cancelling network
[130]	65	1.2	12/11.67	62.5			1600	8.25		ASAR-Incremental sub-range ADC
[90]	180	1.2	10/9.29	2	-0.3/+0.3	-0.6/+0.6	9.3	7.5	0.21	Binary + LSB-first SA based switching method; metastability correction circuit; Clock-jitter compensation circuit
[110]	180	0.6/0.35	10/9.5	0.020	-0.2/+0.18	-0.25/+0.26	0.112	7.79	0.0468	Clock-to-Q delay compensation; supply-scale able ADC;
[91]	180	0.5	9/8.55	10	-0.5/+0.9	-0.85/+0.7	48	13	0.1215	Top-plate split-capacitor CDAC switching; Sub-threshold operation
[117]	130	3.3	12/11.46	16	-0.25/+0.25	-0.8/+1.1	4.95	101	0.189	Speed-enhanced comparator; Variable delay-unit;
[115]	90	1.2	6/5.72	0.5	-0.3/+0.38	-0.34/+0.24	990	-	0.002	Two-phase handshaking SAR logic; V_{CM}-based CDAC switching
[131]	350	1.8	14/11.45	0.1	-0.9/+0.9	-2.6/+2.1	43.4	155	1.35	Attenuation capacitance calibration; shielded unit capacitance;
[132]	90	1	8/7.8	10.24	-0.56/+0.32	-0.36/+0.29	69	30	0.0554	Power efficiency between 10 kS/s and 10 MS/s
[92]	180	1	10/9.83	10	-0.34/+0.28	-0.38/+0.23	98	11	0.086	Splitting monotonic switching scheme
[104]	40	1.1	6/4.91	1330	-	-	7520	188	0.014	N-comparators for N-conversion for speed enhancement; metastability detection circuit
[133] [134]	90	1	8/7.7	10.24	-0.84/+0.14	-0.73/+0.37	26.3	12	0.054	Scalable power wrt sampling-rate
[105]	130	1.2	9/8.3	17.5	-	-	570	103	0.0775	Two-channel ASAR; metastability-the-set algorithm for high speed; Synchronization approach between 2 channels
[135]	180	1	8/7.55	4	-0.42/+0.30	-0.62/+0.61	28.4	46	0.019	Speed-scalable ASAR with a constant energy-efficiency; Charge-sharing CDAC
[143]	180	0.4	10/9.4	0.0025			0.0065	3.98	0.097	Simulations only;
[93]	350	3.3	12/11.05	0.099	-0.1/+1.5	-1.5/+2	6.8	49	0.715	Split capacitor CDAC array
[118]	28	1	8/7.7	750	0.6	0.57	4500	41	0.004	2b/conversion; R-C DAC; Subranged ASAR
[119]	28	1.1	6/4.91	1330	-0.4/+0.6	-0.6/+0.5	7520	188	0.014	Multiple-quantizers to improve speed;
[94]	28	1	9/8.84	50	-	-	45	2.01	-	Simulated; Monotonic switching method; two-stage comparator
[120] [121]	32	0.9	8/6.15	1000	-0.3/+0.79	-0.9/+0.91	2000	28	0.0015	2 comparators working alternatively;
[136] [137]	65	1.1	11/10.2	95	-0.84/+0.7	-0.84/+0.79	1360	22	0.073	Passive gain to sampling capacitor;
[111]	65	1	8/6.8	50	-	-	157	28	0.017	Only simulations; tunable delay-line with external control

[95]	180	0.6	10/9.2	0.100	-0.2/+0.5	-0.8/+0.95	0.390	6.7	0.103	Hybrid CDAC; 2b/step conversion; time-domain comparator
[122]	65	1	6/4.69	410			2030	189.17	-	3-b/stages, R-DAC; 4-inputs comparator
[96]	65	2.5/1.2	8/7.8	10	-0.499/+0.51	-0.663/+0.798	-	-	-	R-C DAC to reduce area and linearity; Simulations only
[106]	130	1.2	10/9.32	20	-0.32/+0.34	-0.47/+0.22	620	41	0.095	Metastability detection circuit
[124]	65	0.6	12/10.4	10	0.24	0.45	83	6.2	0.1008	ASAR-based TI ADC; Settling-while-conversion method;
[107]	180	0.5-0.65	10/8.97	0.005-0.5	-0.8/+0.6	-1.3/+0.8	2.84	10.9	0.077	Sampling-rate scalable with the use of scalable supply; Metastability detection circuit
[144]	180	1.2	8/	50			750			Simulations only;
[138]	16	-	13/10.31	4000	-0.3/+0.3	-1.5/+1.5	513000	153.2	1.04	3 stages Asynchronous pipeline-SAR; foreground and background calibrations
[97]	65	1.2	10/9.04	100	-	-	3100	30.27	0.009	Set-and-down switching
[125]	180	1.2	6/5.87	330	-0.53/+0.47	-0.56/+0.53	640	36.47	0.0164	Comparator reused ASAR ADC for speed enhancement
[139] [140]	160	1.8	5/	2	-	-	-	-	-	Coarse ADC in zoom ADC
[145]	55	1	10/9.75	8	-	-	124	-	-	Simulations only
[98]	65	1.2	8/7.85	400	-0.3/+0.3	-0.25/+0.25	1940/2260	26/23		Simulations only; single as well as differential mode
[141]	130	1.2	8/7.6	3.2			105000	640	1.1	TI ASAR ADC
[99]	40	1.1	8/7.5	500			610	9.46		Set-and-down CDAC switching; Analog calibration for offset mismatch
[142]	160	1.8	5/	5.12						Coarse ADC in CT zoom ADC

2.7. Noise-Shaping SAR ADCs: State-of-the-art

From their inception in 2012, NS-SAR ADCs have drawn ample attention from the research community. As a result, numerous developments can be witnessed recently. This section provides a short overview of the recent advancements in NS-SAR ADCs by dividing them into three categories: Error-feedback topology (EF), Cascaded Integrated Feedforward (CIFF) topology, and hybrid/combined topology.

2.7.1. Error-Feedback NS-SAR ADCs

In [146], an EF NS-SAR ADC has been presented, which is the first NS-SAR ADC based on EF topology. The NS has been achieved with the help of a switched capacitor network. A dual polarity digital calibration method has been utilized to compensate for the CDAC mismatches. The proposed ADC has been designed and fabricated in a 0.5 µm CMOS process at a supply voltage of 1.8 V and secures an SNDR of 67.7 dB at a sampling-rate of 62.5 kHz. The power consumption of the ADC is 38.3 µW.

A 1st-order EF NS-SAR ADC has been presented in [147] with a rail-to-rail input. The ADC core consists of a 10-bit non-binary SAR ADC. The NS has been achieved by using a buffer and a capacitor. The design also consists of a comb decimation filter, which consists of 2 stages cascaded integrator. At a supply voltage of 1.8 V using 180-nm CMOS process, the proposed ADC secures an ENOB of 14.3-bit, and peak SNDR of 88 dB, while dissipating 20 µW.

In [148], a 2nd-order EF-based NS-SAR ADC has been proposed. The NS functionality has been achieved with the use of a passive FIR filter and a comparator-reused dynamic amplifier. In addition, the design is

accompanied by a PVT tracking background calibration technique. Designed in a 40 nm CMOS process at a supply voltage of 1.1 V, the ADC secures a peak SNDR of 79 dB, while dissipating 84 µW power.

A 1st-order EF-based NS-SAR ADC has been presented in [149]. The design uses two equal valued capacitors to implement the CDAC instead of a binary weighted CDAC in order to reduce capacitance spread and associated mismatch errors. Also, a monotonic switching method for the CDAC has been used to reduce ADC conversion time as well as switching-energy. The NS has been achieved using an active integrator. Implemented in a 180 nm CMOS process at a supply voltage of 1.5 V, the proposed design achieves an ENOB of 12.80 bits and peak SNDR of 78.8 dB at a 2 kHz bandwidth. It consumes 74.2 µW power.

In [150], a 2nd-order EF-based NS-SAR ADC has been presented. The NS has been achieved by cascade of a temperature-tolerant dynamic amplifier and a ring-amplifier to implement a low-noise and power-efficient feedback path gain. The design is accompanied by a novel digital calibration method for the CDAC mismatch errors. Designed in a 65 nm CMOS process using a supply voltage of 1 V, the proposed ADC secures a peak SNDR of 70.98 dB at a bandwidth of 625 kHz, consuming 130 µW.

A 4th-order cascaded EF-based NS-SAR ADC has been presented in [151]. The 4th-order NS has been achieved by a cascade of two 2nd-order EF NS-SAR stages in such a way that it consumes the same power and occupies same area as of a 2nd-order NS stage. A two-phase settling method has been introduced to improve the efficiency of the amplifiers. The proposed method is inherently PVT-robust. Designed in a 28 nm CMOS process at a supply voltage of 1 V, the proposed design secures a peak SNDR of 87.6 dB at a bandwidth of 100 kHz and consumes 120 µW power.

In [152], a EF-based NS-SAR ADC has been presented. The NS functionality has been obtained by an adjustable 2-tap switched-capacitor FIR filter. The design is equipped with a 2-stage clock-controlled amplifier in EF path to enable both, an enough gain and speed at the same time by allocating adequate currents in the gain stage and the driving stage separately. The design is configurable with respect to signal bandwidth and supports 8 different bands. Designed in a 65 nm CMOS technology at a supply voltage of 1 V, the ADC secures a peak SNDR of 74 dB, while consuming 70 µW.

A 1st-order EF-based NS-SAR ADC has been proposed in [153]. NS has been implemented using an integrator based on a single OP-AMP. Correlated double sampling and correlated level shifting methods have been adopted to relax the design of single OP-AMP: the former method reduces the offset and flicker noise of the integrator, while the later enhances OP-AMP gain and reduces its power. To cancel the CDAC mismatch errors and parasitic impacts, a two-step incremental ADC based digital calibration method has been utilized. Designed in a 130 nm CMOS technology with a supply voltage of 1.6 V, the design secures a peak SNDR of 82.6 dB over a bandwidth of 2 kHz and consumes 40.8 µW.

In [154], a 4th-order cascade EF-based NS-SAR ADC has been proposed. The NS functionality has been achieved by a 4th-order robust filter; filter consists of an integrator, made up of a stack of a residue capacitor with the integration capacitor. Integration capacitor stores the stacking outcome through a unity-gain dynamic buffer. Source-follower has been used as a unity-gain buffer because of its simple nature and PVT-robustness. Implemented in a 40 nm CMOS process using a supply voltage of 1.1 V, the ADC achieves a peak SNDR of 93.3 dB at 250 kHz bandwidth, while consuming 340 µW.

A 2nd-order EF-based NS-SAR ADC is presented in [155, 156]. The NS function has been achieved by the use of an FIR filter. A gain stage is applied in the residue path to compensate for the loss due to charge sharing process. To get a PVT-robust gain stage, a novel voltage-time-voltage (V-T-V) converter has been utilized. This enables the ADC to operate reliably without the use of any calibration. Designed in a 90 nm CMOS process using a supply voltage of 1 V, the ADC achieves an ENOB of 12-bits, and peak SNDR of 73.8 dB at 625 kHz bandwidth, while consuming 71 µW.

In [157], a EF-based 2nd-order NS-SAR ADC is presented. The NS function has been achieved by the use of series connections in capacitors in the loop filter in such a way that enables the use of a low-gain closed-loop dynamic amplifier in the loop path. Simulated in a 55 nm CMOS process, the presented solution obtains a peak SNDR of 98.1 dB at 1.25 MHz, while it consumes 623.6 µW.

An EF-based active NS-SAR ADC is proposed in [158]. The aim of the proposed architecture is to improve precision and speed of a NS-SAR ADC with the help of different techniques employed in the proposed solution, such as Mismatch Error Shaping (MES), Data Weighted Averaging (DWA), and Tri-level switching. Designed in a 40 nm CMOS process at a supply voltage of 1.1 V, the presented solution gets a peak SNDR of 98.2 dB at 100 kHz and consumes 1.998 mW.

In [159], an EF-based NS-SAR is presented. A 2nd-order NS function has been achieved with the use of a unity gain buffer and delay elements working in a ping-pong manner. Designed in a 65 nm CMOS process using a supply voltage of 1.2 V, the presented ADC gets a peak SNDR of 79.3 dB at 0.625 MHz, consuming 113.02 µW.

A 2nd-order EF-based NS-SAR ADC is presented in [160]. The NS function has been obtained by the use of 2 passive integrators based on a duty-cycled amplifier. A 1st-order reshaping of the CDAC errors has been obtained with the help of a two-level digital prediction method. Fabricated in a 65 nm CMOS process, the proposed ADC secures a peak SNDR of 80 dB at 31.25 kHz, consuming 7.3 µW.

A summary of EF-based NS-SAR ADCs is provided in Table 2.4.

Table 2. 4. Summary of EF topology-based NS-SAR ADCs

Ref.	Tech. (nm)	V_{DD} (V)	BW (MHz)	OSR	ENOB (Bits	SNDR (dB)	P_{avg} (µW)	FoM_S (dB)	FoM_W f.J/C-step)	Comments
[146]	500	1.8	3.125	10	-	67.7	38.3	176.9	-	First ever EF NS-SAR; uses dual-polarity digital CDAC calibration method
[147]	180	1.8	0.000040	64	14.3	88	20	151	-	Non-binary SAR; uses a decimation filter;
[148]	40	1.1	0.625	8	-	79	84	178	9	Passive FIR filter with dynamic amplifier; PVT tracking background calibration method
[149]	180	1.5	0.002	32	12.80	78.8	74.2	153.1	-	Active NS; monotonic switching; two equal-valued capacitors based CDAC
[150]	65	1	0.625	8	-	70.98	130	168	35.9	Dynamic ring amplifier; Temp-tolerant;
[151]	28	1	0.1	10	-	87.6	120	176.8	135.7	Cascaded 4th-order NS;
[152]	65	1	0.625	8	12	74	70	174	-	Bandpass NTF; configurable NS-SAR
[153]	130	1.6	0.002	32	-	82.6	40.8	160	-	Corelated double sampling and corelated level shifting methods; digital calibration
[154]	40	1.1	0.250	10	-	93.3	340	182	-	Capacitor stack; dynamic buffering
[155] [156]	90	1	0.625	8	12	73.8	71	173.2	14.2	PVT-robust V-T-V based gain stage for FIR filter; 2nd order NS
[157]	55		1.25	16	-	98.1	623.6	188	-	2nd-order; dynamic closed-loop amplifier
[158]	40	1.1	100	64	-	98.3	1998	175.3	-	Speed up the NS-SAR;
[159]	65	1.2	0.625	16	-	79.3	113.02	176.73	11.99	2nd-order; ping-pong with delay; unity-gain buffer
[160]	65	1.2	0.03125	16	-	80	7.3	176.3	14.3	Duty-cycled OP-AMP; passive; Digital predicted mismatch error shaping

2.7.2. Cascaded of Integrators with Feedforward (CIFF) NS-SAR ADCs

The firstly-proposed NS-SAR ADC [161] is based on CIFF topology. The core of the NS-SAR is an 8-bit charge redistribution CDAC array. The NS has been achieved with the help of a loop filter, which consists of a cascade of an integrator and a charge-domain FIR filter. Implemented in a 65 nm CMOS process using

a supply voltage of 1.2 V, the proposed 90 MS/s NS-SAR ADC obtains an ENOB of 10-bits, a peak SNDR of 62.1 dB, and consumes an average power of 806 μW.

A 2nd-order CIFF NS-SAR ADC has been presented in [162]. The design uses an 8-bits CDAC. The NS functionality has been achieved with the help of a fully passive gain method based on capacitive charge pumps, thus avoiding the use of any OP-AMP. Prototyped in a 65 nm CMOS process at a supply voltage of 1 V, the ADC secures an ENOB of 10.5-bits, a peak SNDR of 64.9 dB, while dissipating a power of 252.9 μW.

In [163], a CIFF-based NS-SAR ADC solution in a 130 nm CMOS process at a supply voltage of 1.2 V is presented. The ADC uses a CADC of 10-bits. The NS has been obtained using a fully passive, OP-AMP free integrator, which uses only two capacitors and one switch. The design is PVT-robust with respect to the CDAC mismatch errors. It consumes a power of 61 μW, while achieving an ENOB of 12-bits and peak SNDR of 74 dB.

A CIFF topology-based 1st-order NS-SAR ADC has been proposed. The core consists of a 12-bits SAR ADC. The NS has been achieved using a cascaded FIR-IIR based loop filter, which consists of an input buffer, a passive FIR filter, and a discrete time integrator. It also includes a CDAC mismatch error shaping (MES) method. The proposed solution works in conventional SAR as well as NS-SAR modes. Designed in a 55-nm CMOS process using a 1.2 V supply, the NS-SAR ADC obtains a peak SNDR of 101 dB and consumes 15.7 μW power.

In [164], a 3rd-order CIFF-based NS-SAR ADC has been proposed, whose core is a 12-bits SAR ADC. The NS has been achieved by using three integrators, which introduce a 3rd-order integrator behavior. In addition, dynamic element matching (DEM), and modulation dither effect (MDE) techniques have been utilized to mitigate the CDAC mismatches errors. Designed in a 28-nm CMOS process, the design ADC achieves a peak SNDR of 97.99 dB and ENOB of 16-bits. Under a 1.55 V and 0.75 V supply, it consumes 37.1 μW.

A CIFF-based NS-SAR ADC has been introduced in [165]. The NS functionality has been achieved by using a FIR-IIR filter with a fully dynamic OP-AMP. It uses active residue voltage sampling instead of passive. To enhance linearity and reduce power consumption, the proposed design uses sub-range SAR topology with aligned switching and detect-and-skip methods. It is also accompanied by a data-weighted averaging (DWA) to improve the CDAC linearity. Implemented in a 28-nm CMOS process with a supply voltage of 1 V, the ADC secures an ENOB of 10-bits and peak SNDR of 79.75 dB and consumes an average power of 460 μW.

In [166], a CIFF-based NS-SAR ADC is presented, which achieves NS function with the help of an open-loop integrator based on a dynamic amplifier. To compensate for the CDAC linearity, binary mode dynamic element matching method has been adopted. The proposed design is also clock-scalable with a sampling-rate range of 2.5 MHz to 25 MHz. Designed in a 65 nm CMOS process using a supply voltage of 1 V, the proposed design secures a peak SNDR of 82.3 dB at a sampling-rate of 2.5 MHz, while consuming 66.3 μW.

A 2nd-order CIFF-based NS-SAR ADC has been presented in [167]. It uses a 9-bits SAR as its core. The NS has been achieved with the help of passive integrators made up of switches and capacitors, thus leading to a passive and OP-AMP free solution. The design is NS-order reconfigurable (from 0 to 2). To reduce power and noise, it proposes a dynamic non-overlapping clock generator and tri-level majority voting methods. Designed in a 40-nm CMOS process at a supply voltage of 1.1 V, it secures an ENOB of 13-bits and peak SNDR of 80 dB, while dissipating 143 μW.

In [168], the authors have proposed a CIFF-based NS-SAR ADC. The NS has been obtained using a ping-pong switching based passive method. In addition, it uses a noise quantizer method to enhance SNR. The ADC works with and without noise quantizer method enabled. The ADC has been prototyped in a 14 nm

CMOS process at a supply voltage of 1V and secures a peak SNDR of 69.1 dB with noise quantizer enabled. The power consumption is 2.8 mW.

The authors have presented a CIFF-based NS-SAR ADC in [169]. The NS has been achieved by a cascaded FIR-IIR loop filter including input buffers, which has been implemented as an inverter-based switched capacitor circuit. To mitigate the CDAC mismatch errors, a least square estimation calibration method has been utilized. Designed at a supply voltage of 0.81 V using a 28 nm CMOS process, the ADC secures an ENOB of 11-bits, and peak SNDR of 68.1 dB. It consumes 70.5 µW power.

In [170], the authors have presented a 3rd-order CIFF-based NS-SAR ADC. The core of the design is a 9-bits SAR ADC with a non-binary CDAC array to enhance sampling-rate. The NS has been obtained by a passive switched capacitor network. Designed in a 65 nm CMOS technology, the proposed design achieves an ENOB of 11.08 bits and peak SNDR of 68.5 dB at a sampling-rate of 43 MHz, consuming 460 µW power.

The authors of [171] have proposed a 2nd-order CIFF-based NS-SAR ADC. The NS functionality has been achieved by a passive noise-shaping loop, which does not consume quiescent current. In addition, the design makes use of a dynamic element matching to reduce harmonic distortions. Also, a tunable majority voting method is part of the design to relax comparator noise requirements. Prototyped in a 28 nm CMOS technology at a supply voltage of 1 V, the ADC achieves an ENOB of 11.2 bit and a peak SNDR of 72 dB at a bandwidth of 100 kHz, while dissipating 118 µW.

In [172], a CIFF-based 1st-order NS-SAR ADC has been proposed. The NS has been achieved by the use of a passive signal residue summation method to achieve desired NTF without the need of a multi-input comparator. Doing so breaks the tradeoff between noise reduction in a conventional NS-SAR ADC by introducing NS and noise increase because of the introduction of the multi-input comparator. Designed in a 14 nm process at a supply voltage of 0.9 V, the proposed design secures an ENOB of 10 bits and a peak SNDR of 66.6 dB at a 40 MHz bandwidth, while consuming 1.25 mW power.

A CIFF-based 2nd-order NS-SAR ADC has been implemented in [173]. The design adds an input buffer in such a way that the CDAC is placed at the input of the buffer and the sampling capacitor is placed at the output of the buffer; both of these are separated by the input buffer in order to compensate the non-linearity of the input buffer as well as reduce sampling capacitor values, resulting in a significant power saving. The NS functionality has been achieved by using power-efficient passive integrators with the sampling capacitor. An error shaping method has been introduced to mitigate the CDAC mismatch errors. Designed in a 65 nm CMOS process at a supply voltage of 0.9 V, the ADC secures a peak SNDR of 73.8 dB at a bandwidth of 2 MHz and consumes 0.87 mW power.

In [174], a CIFF-based NS-SAR ADC has been proposed. The core of the design is a 9-bits CDAC. The design includes an on-chip foreground CDAC calibration method. The NS has been achieved by a loop filter, which consists of two integrators, a passive summer, and a local feedback path. Prototyped in a 28 nm CMOS process at a supply voltage of 0.8 V, the ADC secures a peak SNDR of 68.2 dB at a bandwidth of 5 MHz and consumes 108.7 µW.

A CIFF-based 2nd-order NS-SAR ADC has been presented in [175]. The NS function has been obtained by using a loop filter with a PVT-robust closed-loop dynamic amplifier. The design does not need any gain calibration for a sharp NTF implementation. Designed in a 40 nm CMOS process, the proposed design secures a peak SNDR of 83.8 dB at a bandwidth of 0.625 MHz, while consuming 107 µW.

In [176], a CIFF-based NS-SAR ADC has been proposed. The NS functionality has been achieved by a passive filter, which provides a 4× passive gain. In addition, the proposed architecture eliminates the need of residue sampling, thus abating the $^{kT}/_{C}$ noise. Moreover, it introduces a 2nd-order tune-free analog mismatch error shaping method to compensate the CDAC mismatch errors. Implemented in a 40 nm CMOS

process at a supply voltage of 1.1 V, the designed ADC secures a peak SNDR of 90.5 dB at a bandwidth of 40 kHz and consumes 67.4 µW.

A 2nd-order CIFF-based NS-SAR AC has been proposed in [177]. The core of the design is an 8-bits SAR ADC. The NS functionality has been achieved by a lossless integrator, which has been implemented by a ping-pong structure and two dynamic amplifiers. Prototyped in a 65 nm CMOS technology at a supply voltage of 1.2 V, the proposed design achieves a peak SNDR of 77 dB over a bandwidth of 3.125 MHz and consumes 1.24 mW.

In [178], a CIFF-based 1st-order NS-SAR ADC has been presented. The NS function has been obtained by the use of a PVT-robust passive integrator. Designed in a 65 nm CMOS process, the design secures a peak SNDR of 68 dB at a sampling-frequency of 150 MHz at an OSR of 4, while consuming a 0.5 mW power.

A CIFF-based NS-SAR ADC is presented in [179]. The core of the design is a 7-bits CDAC. The NS functionality has been achieved by using an integrator, which consists of switches, capacitors, and a dynamic amplifier. With the help of digital logic, the comparator is enabled to be reused as an amplifier three times. This saves power, area, and reduces noise. Designed in a 180 nm CMOS process at a supply voltage of 1 V, the design secures a peak SNDR of 65 dB at a sampling-rate of 10 kS/s with an OSR value of 8, while consumes 0.09 µW.

A 2nd-order CIFF-base NS-SAR ADC has been proposed in [180]. The core of the design is a 5-bits SAR ADC. The NS function has been achieved by the use of an integrator instead of a cascade of integrators. The proposed ADC overcomes the input range limitations of the conventional NS-SAR ADCs by enhancing input impedance. Instead of using multi-input comparator with a cascade of integrators, the proposed solution employs a recycling reconfigurable transconductance amplifier to perform two successive integration phases as well as a passive summation. A Clocked-averaged (CLA)-based element matching technique has been used to enhance linearity. Designed in 180 nm CMOS technology at a supply voltage of 1 V, the proposed ADC secures an ENOB of 16.2 bits and a peak SNDR of 99.1 dB at a bandwidth of 1kHz and consumes 9.29 µW power per channel.

An 2nd-order CIFF based hybrid NS-SAR ADC is presented in [181]. The core consists of an 8-bits SAR ADC. The NS function has been achieved by the use of an FIR-IIR filter. Simulated in a 65 nm CMOS process at a supply voltage of 1.2 V, the design secures an ENOB of 14.5 bits and a peak SNDR of 87.9 dB at a bandwidth of 6.25 MHz, consuming 1.78 mW.

A 1st-order CIFF-based CT NS-SAR ADC is presented in [182, 183]. A 10-bits DT SAR is the core of the design. Instead of a DT integrator, this design uses a CT $G_m - C$ integrator with an inherent anti-aliasing capability. To overcome the timing issues between DT SAR ADC and CT integrator, SAR ADC sampling switch is eliminated, and integrator is duty-cycled in such a way that it leaves a 5 % of the sampling clock period for the SAR conversion. Because of the nonexistence of the sampling-switch, redundancy has been added to track varying input to the ADC. Prototyped in a 65 nm CMOS process at a supply voltage of 1 V, the design secures a peak SNDR of 77.3 dB at 62.5 kHz, consuming 13.5 µW.

In [184], a fully passive 1st-order CIFF-based NS-SAR ADC is presented. The NS has been achieved by the use of a passive integrator with a dynamic DC offset to compensate for the path gain variation error at CDAC array at each quantization step. Path gain variation error occurs because of the use of a novel energy efficient CDAC switching technique. Simulated in a 180 nm CMOS process at a supply voltage of 0.6 V, the ADC secures a peak SNDR of 70.3 dB at 1.56 kHz bandwidth, consuming 130 nW.

A CIFF-based 2nd-order NS-SAR ADC is presented in [185]. The core of the design is a 6-bits SAR ADC. The NS functionality has been obtained by a passive gain of 4 in the passive loop filter, based on capacitor stacking and two input paired comparators. As per behavioral simulations, the proposed solution secures a peak SNDR of 70 dB at a bandwidth of 500 kHz.

In [186], a 3rd-order CIFF-based NS-SAR ADC is presented. The core consists of a 9-bits SAR ADC. The NS function has been achieved by a 3rd-order integrator with floating inverters-based amplifiers. The summation function of the loop filter has been realized using stacking capacitors. A non-binary split capacitor CDAC has been used to reduce area and power. Simulated in a 130 nm CMOS process, the design achieves a peak SNDR of 80.2 dB at 312.5 kHz bandwidth, while consuming 607 µW.

A CIFF-based 1st-order NS-SAR ADC is presented in [187]. The design uses a dual-capacitor merge-and-split CDAC switching method to improve energy-efficiency. Simulated in a 180 nm CMOS process at a supply voltage of 1 V, the ADC gets a peak SNDR of 68.13 dB at 62.5 kHz bandwidth, consuming 6.19 µ W.

In [188], a 2nd-order CIFF-based NS-SAR ADC with embedded input buffer is presented. The input buffer separates the CDAC and sampling capacitor. This improves the buffer linearity as well as reduces sampling capacitor value, thus saving power. The NS has been achieved by a passive loop filter, which consists of a sampling capacitor, a bridge capacitor, and two integration capacitors. Designed in a 65 nm CMOS technology, the proposed ADC secures a peak SNDR of 73.8 dB at 2 MHz, dissipating 2.14 mW.

A CIFF-based 1st-order NS-SAR ADC is presented in [189]. The NS function has been achieved with the help of a passive integrator in the loop filter, made up of capacitors and switches only, without the need for a multi-input comparator. A split-capacitor CDAC is used to reduce area and power of the design. Simulated in a 180 nm CMOS process, the design secures an ENOB of 13.7 bit and a peak SNDR of 84.3 dB at 8 kHz bandwidth, consuming 7.65 µW.

In [190], a CIFF-based 2nd-order NS-SAR ADC is proposed. The NS function has been obtained with the use of a 2nd-order CIFF-based passive loop filter with a three-input comparator. The design is accompanied with the last bit voting method to reduce comparator's noise. In addition, a cyclic dynamic element matching is part of the solution for the CDAC mismatches cancellation. Designed in a 28 nm CMOS process, the design obtains a peak SNDR of 72.3 dB at 50 kHz, while consuming 60 µW.

A CIFF-based 2nd-order passive NS-SAR ADC is presented in [191]. The NS function has been enabled by the use of 2 passive integrators separated by a pre-amplifier. Least mean square calibration is applied to the NS-SAR to mitigate CDAC errors. Simulated in a 130 nm CMOS process, the proposed ADC get a peak SNDR of 78.04 dB at 125 kHz, consuming 65.3 µW.

In [192], a CIFF-based 2nd-order NS-SAR ADC is presented. A 10-bits SAR ADC is the core of the design. It uses a resistor-capacitor DAC and two differential integral capacitors to reduce area. A voltage gain calibration for a 3-input comparator is included to enhance the NS performance. Simulated in a 180 nm CMOS process, the designed ADC secures a peak SNDR of 87.3 dB at 62.5 kHz, consuming 248 µW.

Table 2.5 summarizes the state-of-the-art of CIFF-base NS-SAR ADCs.

Table 2. 5. Summary of CIFF topology-based NS-SAR ADCs

Ref.	Tech. (nm)	V_{DD} (V)	BW (MHz)	OSR	ENOB (Bits)	SNDR (dB)	P_{avg} (µW)	FoM_S (dB)	FoM_W f.J/C-step)	Comments
[161]	65	1.2	11	4		62.1	806	163.5	35.8	First-ever NS-SAR ADC
[162]	65	1.0	8	4	10.5	64.9	252.9	169.9	10.9	Fully-passive; OP-AMP free
[163]	130	1.2	0.125	8	12	78	61	167	-	Fully passive integrator
[193]	55	1.2	0.001	500	-	101	15.7	178.9	-	Highest SNDR reported; Works in SAR as well as NS-SAR modes; uses CDAC MES method
[164]	28	1.55/0.75	0.002	25	16	97.99	37.1	175.3	-	Uses DEM and MDE
[165]	28	1	5	13.2	10	79.75	460	180.1	5.8	Sub-range SAR; uses DWA; uses dynamic OP-AM based FIR-IIR Filter

[166]	65	1	0.25	20	-	82.3	66.3	172	-	Utilizes dynamic amplifier-based Open-loop integrator; uses binary mode dynamic element matching method
[167]	40	1.1	0.262	16	13	80	143	173	-	Uses passive integrators
[168]	14	1	25	6	-	69.1	2800	169	20.7	Passive NS; uses noise quantizer method; First-ever NS-SAR in FinFET technology
[169]	28	0.81	1.75	8	11	68.1	70.5	172	9.8	At least square estimation CDAC calibration method
[170]	65		3.76	5.7	11.08	68.5	460	167.62	20	Passive structure;
[171]	28	1	0.05	16	11.2	72	118	161.2	180	DEM technique; tunable majority voting;
[172]	14	0.9	40	4	10	66.6	1250	171.7	8.9	Single input comparator; passive residue summation; second NS-SAR in 14 nm FinFET technology;
[173]	65	0.9	2	20	-	73.8	870	167.4	54.3	Includes input buffer; MES method;
[174]	28	0.8	5	4	-	68.2	108.7	174.8	5.2	On chip foreground CDAC calibration;
[175]	40		0.625	8	-	83.8	107	181.5	6.8	Closed-loop DA; PVT-robust
[176]	40	1.1	0.04	25	-	90.5	67.4	178.2	-	OTA-free; PVT-robust; 2nd-order MES
[177]	65	1.2	3.125	16	-	77	1240	171	-	Lossless integrator; dynamic amplifier;
[178]	65	-	18.8	4	-	68	500	172.3	-	Passive integrator
[179]	180	1	0.000625	8	10.5	65	0.09	163.5	50	Comparator reused 3 times as an amplifier; dynamic amplifier in integrator;
[180]	180	1	0.001	64	16.2	99.1	9.29/channel	179.5	-	2nd-order NS-SAR; with clocked-averaged based element matching
[181]	65	1.2	6.25	8	14.2	87.9	1780	183	-	2nd–order; only simulated
[182] [183]	65	1	0.625	1.6		77.3	13.5	174	18	1st CT NS-SAR; CT $G_m - C$ integrator; 1st CT NS-SAR
[184]	180	0.6	.00156	8	11.4	70.3	0.13	171	-	Simulated; passive integrator; energy efficient CDAC switching method
[185]	-	-	0.5	16	-	70	-	-	-	Behavioral simulation results only
[186]	130	-	0.3125	8	-	80.2	607	167.3	-	3rd-order; non-binary split CDAC
[187]	180	1	0.0625	8	11.02	68.13	6.19	168.2	23.3	1st-order; split-and-merge CDAC switching method
[188]	65	0.9/2.1	2	20	-	73.8	2130	163.6	133	Buffer-embedded 2nd order; Passive integrator
[189]	180	1.8	5	25	13.7	84.3	7.65	174.4	-	Passive loop filter without multi-input comparator; only simulations
[190]	28	0.6/1	50	16	11.7	72.3	60	161.5	178	2nd-order passive; last bit majority voting; Cyclic DEM
[191]	130	-	0.125	8	-	78.04	65.3	-	-	Simulation only; 2nd-order NS; LSM-based CDAC calibration
[192]	180	1.8	0.0625	8	14	87.3	248	-	-	Simulations only' R-C DAC;

2.7.3. Hybrid/Combined NS-SAR ADCs

A 1st-order hybrid NS-SAR ADC has been proposed in [194]. The NS has been obtained with a passive network, which is OP-AMP free. This solution uses the CDAC to store residue voltage in order to get information about error sources of the ADC, such as CDAC settling and mismatch, comparator noise, and quantization noise. The core of the ADC is an 8-bits CDAC. Designed in a 65 nm CMOS technology at a supply voltage of 0.8 V, the ADC achieves an ENOB of 9.35-bits, peak SNDR of 58 dB, while consuming a power of 120.7 μW.

In [195], an EF-based 4th-order NS-SAR ADC has been proposed, that introduces time-interleaving to overcome bandwidth limitation of the NS-SAR ADC. The NS functionality has been achieved by using a summing preamplifier and a shared feedback bus to avoid complexity. The need for a low gain for the proposed architecture enables the use of a single stage open-loop amplifier. To make the design robust to avoid quantization overload, redundancy has been introduced, as well as NTF coefficients have been optimized. Prototyped in a 40 nm CMOS process at a supply voltage of 1 V, the ADC achieves a peak SNDR of 70.4 dB at a bandwidth of 50 MHz, consuming 13 mW.

A CIFF-based NS-SAR ADC has been presented in [196], which introduces time-interleaving. The NS has been obtained by the cascade of integrators with a fully passive switched capacitor-based loop filter. The summation has been implemented by a multi-path comparator. The design uses a fully dynamic amplifier. The time-interleaving has also been achieved by fully passive switched capacitor network. The design is PVT-robust. Designed in a 40 nm CMOS process at a supply voltage of 1.1 V, the design secures a peak SNDR of 69.1 dB over a bandwidth of 50 MHz and consumes 8.5 mW.

A 3rd-order CIFF-EF-based NS-SAR ADC has been designed in [197]. The design uses only a single OP-AMP, which is fully dynamic. An open-loop self-quenching floating-inverter has been used as the amplifier. A sampling noise cancelling method, which reuses hardware implementing EF-CIFF functionality, has been used to mitigate the $^{kT}/_{C}$ noise. Designed in a 65 nm CMOS technology, the designed ADC secures a peak SNDR of 84.8 dB at a bandwidth of 625 kHz and consumes 119 µW.

A time-interleaved CIFF-based NS-SAR ADC has been proposed in [198]. The NS has been achieved by the use of a passive residue summation method without the need of a multi-input comparator. The residue sampling has been done by using two back-to-back capacitors connected across the CDAC top plates. Time-interleaving is achieved by the use of a coarse-fine structure of comparators. The coarse comparators are time-interleaved, while a single fine comparator is shared between two channels, which not only saves hardware but also reduces inter-slice offset. Designed in a 22 nm FDSOI CMOS process, the designed ADC secures a peak SNDR of 66.3 dB at a bandwidth of 80 MHz and consumes 2.56 mW.

In [199], an ADC architecture has been proposed, which is a combination of an open-loop bandpass Σ-Δ ADC and CIFF-based NS-SAR ADC in combination with N-path filter. A 2nd-order NS has been achieved by adopting CIFF topology. The NS-SAR has been used to get a sharp NTF at DC for the signals. The CDAC is shared between NS-SAR and N-path filter, which avoids signal attenuation, saves power and area, and reduces circuit complexity. Designed in a 40 nm CMOS process, the ADC achieves a peak SNDR of 78.7 dB at a 3.5 MHz and consumes 5.04 mW.

A hybrid (EF-CIFF) 3rd-order NS-SAR ADC has been proposed in [200]. The core consists of an 8-bits SAR ADC. The NS has been obtained by a hybrid error control architecture, which exploits the advantages of EF and CIFF structures, while obviating their drawbacks. The EF and CIFF summation is performed simultaneously by the hybrid error control structure. Designed in a 130 nm CMOS process at a supply voltage of 1.2 V, the ADC secures a peak SNDR of 79.57 dB at 125 kHz bandwidth, while consuming 96 µW.

A hybrid ADC architecture has been proposed in [201]. The design presented is a VCO-based CT Σ-ΔM, where a 2nd-order NS-SAR has been used as a quantizer to get a 3rd-order NTF overall. The hybrid design breaks the bandwidth-resolution tradeoff of CT Σ-Δ ADCs. A 2nd-order 5-bit NS-SAR functionality has been achieved using an EF-CIFF based topology. Designed in a 28 nm CMOS process at a supply voltage of 1 V, the proposed ADC secures a peak SNDR of 84.2 dB at a bandwidth of 1 MHz, while consuming 1.63 mW.

In [202], a passive bandpass Σ-Δ ADC is presented, which uses a high-pass NS-SAR as a quantizer. Σ-Δ ADC has been realized by the use of 2 high-pass NS-SAR ADCs, which operate in a time-interleaving manner. The architecture of the NS-SAR ADCs has been realized by the use of a 5-bit fine NS-SAR and a

4-bit coarse SAR. Data weighted averaging is part of the design for the CDAC mismatches cancellation. The NS has been obtained by a passive loop filter, which consists of capacitors, switches, and a 2nd-order integrator. The ADC is scaling-friendly because it does not need any OTA, unlike conventional 4th-order Σ-Δ ADCs. Designed in a 28 nm CMOS process, the ADC gets a peak SNDR of 69 dB at 12 MHz and consumes 2.5 mW.

In [203], a hybrid NS-Pipeline ADC architecture has been proposed. The design uses a 2nd-order fully passive CIFF-based NS-SAR ADC, which employs a floating invert-based amplifier as a residue amplifier. The NS-SAR serves as a gain-shaping stage. The hybrid ADC is also equipped with a quantization prediction unrolled method. Designed in a 28 nm CMOS process using a supply voltage of 1 V, the hybrid ADC secures a peak SNDR of 77.2 dB at a bandwidth of 25 MHz, consuming a power of 2.03 mW.

A hybrid fully dynamic incremental Zoom ADC architecture is proposed in [204], which uses a buffer embedded 2nd-order EF-based NS-SAR ADC to increase the input bandwidth of the hybrid architecture. The NS-SAR uses only one dynamic amplifier-based buffer to save power and complexity. In addition, it uses a floating inverter-based amplifier for the residue extraction. Implemented in a 28 nm CMOS process at a supply voltage of 1V, the hybrid ADC secures an ENOB of 15-bits, and a peak SNDR of 92.5 dB at a bandwidth of 150 kHz. It consumes a power of 160 µW.

A 4th-order single-channel pipeline NS-SAR ADC has been presented in [205]. The hybrid architecture uses a 3rd-order EF-CIFF based NS function incorporating a 2nd-order EF NS stage and a 1st-order FF-based NS stage. Both the NS stages are fully passive. Designed in a 28 nm CMOS process, the designed hybrid ADC secures a peak SNDR of 70.15 dB at a bandwidth of 100 MHz and consumes 4.52 mW.

In [206], a 4th-order pipeline NS-SAR ADC has been presented. The design uses a 2nd-order EF-based NS-SAR in the first stage and a 2nd-order CIFF-based NS-SAR ADC in the second stage. The proposed solution includes a $^{kT}/_{C}$ cancellation method. In addition, it uses a dynamic amplifier sharing method to reduce hardware complexity. Designed in a 65 nm CMOS process at a supply voltage of 1.2 V, the ADC achieves a peak SNDR of 83 dB at a bandwidth of 1.25 MHz, consuming 335 µW.

A 1st-order hybrid (EF-CIFF) NS-SAR ADC has been presented in [207]. The proposed NS-SAR avoids the use of a multi-input comparator as well as high gain amplifier; instead, it utilizes a ratio of the capacitances to achieve a better NTF. The design reuses a passive integrator in both NS paths to save power and area. The proposed design makes use of a unity gain buffer in the EF path. Designed in a 28 nm CMOS process at a supply voltage of 0.9 V, the ADC secures a peak SNR of 75 dB at a bandwidth of 2.5 MHz, consuming 150 µW.

In [202] , a 4th-order passive bandpass Σ-ΔM is presented with a high pass 2× time-interleaved passive NS-quantizer. NS-SAR consists of a 4-bit coarse SAR and 5-bit EF-based NS-SAR ADC with 1-bit redundancy. In addition, a data weighted averaging method has also been used for the CDAC mismatches cancellation. The loop filter of the NS-SAR consists of a 2nd-order passive integrator, capacitors, and switches. Designed in a 28 nm CMOS process, the proposed solution secures a peak SNDR of 69 dB at a bandwidth of 12 MHz, consuming 2.5 mW.

A hybrid 2nd-order 2× time-interleaved NS-SAR ADC is presented in [208, 209]. To obtain the NS, two methods have been used: first, a one-time midway EF-based NS, and second a 2nd-order CIFF-based NS. The design uses a dynamic residue amplifier shared between two channels, which lowers offset. Designed in a 28 nm CMOS process at a supply voltage of 1 V, the design secures a peak SNDR of 73.2 at 30 MHz bandwidth, consuming 3.07 mW.

In [210], a 3rd-order DT Σ-ΔM has been designed, which uses a NS-SAR combined digital noise-coupling quantizer. The Σ-ΔM consists of two dynamic integrators based on floating inverters amplifiers, and an asynchronous SAR quantizer: passive NS and digital noise coupling methods have been introduced to the

SAR quantizer to get 3rd-order function in Σ-ΔM. The NS has been achieved by using a simpler switching circuit only without any active element, which leads to an incomplete NTF order. To get complete NTF order, a 2-bit 1st-order digital noise coupling method has been introduced. The DWA is also part of the solution. Designed in a 22 nm CMOS process at a supply voltage of 1 V, the proposed ADC secures a peak SNDR of 80.4 dB at 0.5 MHz, while consuming 0.32 mW.

A hybrid 12-bits NS subranging SAR ADC has been presented in [211], which uses a 4-bits flash ADC and a 9-bits SAR ADC with 1-bit redundancy. The NS has been achieved by a 2nd-order CIFF-based topology. The ADC is embedded with an input buffer made up of the source follower. A dynamic level-shifting method is used to enhance the linearity of the input buffer. The design is also equipped with a mismatch error shaping method to cancel CDAC mismatch errors for avoiding inter-symbol-interference (ISI) errors. To mitigate ISI, an ISI correction technique is also part of the design. Background and foreground calibrations have been introduced to mitigate gain mismatch error in subrange ADC and NS filter. Designed in a 40 nm CMOS process, the design secures a peak SNDR of 84.2 dB at 5 MHz, consuming 1.84 mW.

In [212], a 3-channel TI NS-SAR ADC has been designed. The NS has been achieved by a passive 1st-order CIFF-based topology, made up of a passive integrator, without the need of a multi-input comparator. The DWA is part of the design to suppress the CDAC mismatches. Designed in an 8 nm process at a supply voltage of 1.1 V, the design secures a peak SNDR of 65.37 dB at 75 MHz, while consumes 4.015 mW.

A hybrid CT/DT 0-2 multi-stage noise-shaping (MASH) Σ-ΔM is proposed in [213] with a 2nd-order passive CIFF-based NS-SAR ADC. The first stage of the hybrid ADC operates in CT mode to perform a coarse quantization with inherent antialiasing and easy driving advantages. The second stage consists of a DT NS-SAR, which is PVT-robust and power-efficient, and scaling-adaptable. The proposed solution is better than conventional CT-MASH ADCs in terms of matching issues between analog and digital sections. Simulated behaviorally, the proposed ADC achieves a peak SNDR of 90 dB over a 10 MHz bandwidth.

In [214], a dual-residue pipeline ADC is presented with a 2nd-order NS interpolating SAR ADC. The 2nd-order EF-based passive NS-SAR has been used in a dual residue pipeline architecture in the backend to relax the accuracy requirements of the residue amplifier in the pipeline topology. The achievable resolution has been enhanced by the use of a segmentation method for capacitive interpolating DAC. Designed in a 180 nm CMOS process, the ADC secures a peak SNDR of 81.2 dB at 1.5 MHz, while consuming 1.8 mW.

A 3rd-order CT- Σ-ΔM is presented in [215], which uses a TI 1st-order CIFF-based NS-SAR as quantizer. The architecture is aimed at mitigating the speed-resolution tradeoff of NS-SAR quantizer in CT- Σ-ΔM. The technique is based on providing a delay to the NS quantizer feedback to get a complete parallel NS quantizer operation. The extra time acquired as a result of providing delay relaxes the loop filtering, residue integration and enhances quantizer resolution. Designed in a 20 nm CMOS process at a supply voltage of 1 V, the ADC gets a peak SNDR of 81.6 dB at 15.625 MHz, consuming 6.4 mW.

A hybrid 1-0 quasi MASH NS-SAR ADC is presented in [216]. The architecture has been built by merging judiciously a passive EF-based NS-SAR and an LSB repeating SAR ADC to suppress the comparator's noise by 8 times LSB repeating. The comparator's suppressed noise is extracted by an average-based virtual sub-ADC and shaped by a NTF digitally. The design is also equipped with a 12-bits bridge crossing segmented CDAC. Designed in a 40 nm CMOS process using a supply voltage of 1.2 V, the ADC achieves a peak SNDR of 84.2 dB at 625 kHz, consuming 100 µW.

In [217], a 4th-order CT Σ-ΔM is presented, which uses a 2nd-order CIFF-based CT NS-SAR ADC. The target of the proposed architecture is to avoid the need of an excessive loop delay compensation, when CT Σ-ΔM is hybridized with DT NS-SAR ADC. The excessive loop delay compensation comes at the cost of high power, power-hungry loop filter, and often poor compensation. The proposed design does so by hybridizing CT Σ-ΔM with CT NS-SAR quantizer. In addition, the design is accompanied by a single

amplifier biqaud and an AC+DC negative-R techniques. Designed in a 28 nm CMOS process, the ADC gets a peak SNDR of 75.5 dB at 20 MHz, consuming 2.78 mW.

In [218], a 1st-order NS-SAR ADC is part of a bidirectional peripheral nerve interface chip data digitization. There is an array of 64 NS-SAR ADC in the entire IC. The NS function has been achieved by a CIFF-based NS topology with an inverter-based integrator. The DEM is part of ADC to suppress the CDAC mismatch errors. Designed in a 65 nm CMOS process, the ADC secures an ENOB of 14-bits over a 2.5 kHz bandwidth with a 173 dB Schrier FoM.

A 4th-order MASH NS-SAR ADC is presented in [219]. The first stage consists of a 2nd-order EF-based NS-SAR with a ring amplifier, which provides a 32× gain in the loop path. The quantization noise of the SAR is first amplified by the ring amplifier, and then sent to the second stage, which consists of a ring amplifier based 2nd-order loop filter. The ring amplifier of stage 1 is reused by stage 2 to get the gain. As a result, the stage 2 NS circuit is relaxed with respect to accuracy and power consumption. Cascade of both stages implements a 4th-order NS function overall. Simulated in a 22 nm process, the proposed ADC achieves a peak SNDR of 78 dB at 100 MS/s, while consuming 15 mW.

In [220], a 2nd-order NS-SAR ADC is proposed. A 10-bits SAR ADC is the core of the design. The NS function has been achieved by cascading 2 identical passive IIR filters and a passive gain stage is added to enhance the loop filter gain. Also, a duty-cycled inverter-based amplifier is part of the loop filter. A 1st-order MES is also part of the design. Designed in a 65 nm CMOS process at a supply voltage of 1.2 V, the proposed ADC secures a peak SNDR of 80 dB at 31.25 kHz, consuming 7.3 µW.

A hybrid (EF-CIFF) 3rd-order NS-SAR ADC is reported in [221]. The core of the design is an 8-bit SAR ADC. The NS has been obtained by a hybrid topology: EF and CIFF. The first stage is EF-based, which consists of a residue sampling capacitor, a residue amplifier, and a passive SC FIR. The second stage is CIFF-based NS, which comprises of a first order passive integrator and a multi-input comparator. To compensate for the CDAC mismatches, a dither based digital calibration method is part of the design. Designed in a 130 nm CMOS process at a supply voltage of 1.2 V, the proposed solution secures an ENOB of 12.93 and a peak SNDR of 79.57 dB at 125 kHz, while consuming 96 µW.

In [222], a hybrid 2nd-order NS-SAR ADC is proposed. The NS is achieved by active-passive loop integrators with low-gain open-loop amplifiers. A passive-active Σ-ΔM has been used as a multi-input, feedforward loop filter to suppress phase error of the passive integrator only. The ADC uses a monotonic CDAC switching technique to get high energy-efficiency. Simulated in a 180 nm CMOS process, the solution secures a peak SNDR of 89.4 dB at 1 MHz bandwidth, while consumes 880 µW.

A 2nd-order SAR-assisted NS-SAR ADC based pipeline ADC is presented in [223]. The NS functionality has been achieved by using a 2nd-order EF-topology, based on a single amplifier, in the second stage of the structure. With a coarse SAR ADC and interleaving techniques, the architecture gets a high-speed operation with low power and strong suppression of in-band quantization noise. The ADC is equipped with gain and offset calibration. Designed in a 28 NM CMOS process, the proposed ADC achieves a peak SNDR of 79.1 dB at 20 MHz, while consumes 3.1 mW.

In [224], a NS-SAR-assisted Σ-ΔM is presented, which is equipped with a 4th-order truncation error-shaping and input impedance enhancement. The architecture consists of a 1st-order Σ-ΔM and a 2nd-order CIFF-based NS-SAR ADC to act as equalizer. The NS-SAR ADC consists of 2 passive integrating capacitors, and a multi-input comparator. A truncation error-shaping block is part of the solution, whose output is fed back to the local loop of the NS-SAR ADC. This enables further 2nd-order NS functionality, leading to a 4th-order NS overall. Designed in a 65 nm CMOS process, the proposed ADC achieves a peak SNDR of 94.5 dB at 500 Hz bandwidth, consuming 5.2 µW.

In [225], a hybrid-loop Σ-ΔM with a time-interleaved NS-SAR ADC as its quantizer is presented. The hybrid-loop Σ-ΔM is aimed at overcoming the PVT variations, sensitivity to timing errors, and sampling-

rate limitations of a CT Σ-ΔM. The purpose of time-interleaved bandpass EF-based NS-SAR ADC is to enhance sampling-rate. Designed in a 28 nm CMOS technology using 1 V supply, the presented ADC gets a peak SNDR of 67.5 dB at 100 MHz, while consumes 13.4 mW.

An analog front-end embedded EF-based 2nd-order NS-SAR ADC is proposed in [226] for direct neural recoding application. To save power and make the NS-SAR PVT-robust, the solution enables the reuse of a capacitive-feedback amplifier of the analog front-end part of the chip with the loop filter of the NS-SAR to get a reliable NS transfer function. The design is also equipped with a novel passive high-pass IIR filter with a chopper-based implementation to get an improved NTF of the NS-SAR ADC. Designed in a 180 nm CMOS process, the proposed design secures a peak SNDR of 82.7 dB at 5 kHz, while consuming 4.2 µW.

In [227], a 3rd-order hybrid NS-SAR ADC is proposed. The NS has been obtained by the use of a 1st-order CIFF-based integrator in the feedforward path of a 2nd-order EF-based NS-SAR. The integrator is passive and has been realized with switches and capacitors only. Comparator compensates for the charge sharing loss of the integrator. In behavioral simulations, the designed ADC gets a peak SNDR of 194.3 dB at 200 kHz.

A 4th-order hybrid NS-SAR ADC is presented in [228, 229]. The NS has been achieved by a merger of EF and CIFF based technique, i.e., EF-CIFF NS method facilitated by a fully dynamic amplifier assisted resonator. This enables robust and energy-efficient NS operation. The design is also equipped with a noise-mitigated push-pull buffer-in-loop method to achieve low-noise and easy-to-drive benefits. In addition, a halved-CDAC level shifting technique is part of the design, which enables the use of a push pull source follower in the buffer-in-loop technique. Designed in a 65 nm CMOS process, the proposed ADC secures a peak SNDR of 84.1 dB at 500 kHz, consuming 133.8 µW.

In [230], a NS-SAR-assisted pipeline ADC is presented. A CIFF-based passive NS-SAR is used in the first stage of the pipeline architecture, realizing a 2-0 MASH. Besides shaping quantization error and comparator's noise, the first stage also shapes inter stage nonlinearity and gain. To overcome interstage offset, a low-cost code-counter-based background offset calibration has been used. Partial interleaving has been utilized in the first stage to get high speed operation, besides sharing the integrating capacitors in CIFF NS stage to save area. Designed in a 28 nm CMOS process, the presented ADC gets a peak SNDR of 79.5 dB at 10 MHz bandwidth, while it consumes 1.26 mW.

A single Open Transconductance Amplifier (OTA)-based 4th-order CT- Σ-ΔM has been proposed in [231], which uses a PVT-robust 2nd-order passive DT CIFF-based NS-SAR ADC with multi-input comparator as quantizer. To reduce circuit complexity and power, the design incorporates excessive loop delay compensation and an input feedforward path inside NS-SAR in the charge domain. Fabricated in a 40 nm CMOS, the design secures a peak SNDR of 80.9 dB at 12.5 MHz, consuming 3.7 mW.

In [232], an OTA-free 1-1 MASH ADC is presented, which uses a passive NS-SAR in the first stage and an open-ring VCO ADC in the second stage. The target of the ADC is to drive large sampling capacitor with NS-SAR ADC. The proposed technique linearizes the VCO ADC by the residue attenuation in the low-resolution NS-SAR. Besides quantization noise and comparator noise of SAR ADC, the proposed solution also high pass-shapes the VCO ADC thermal noise. A simple foreground interstage gain calibration algorithm is also part of the solution. Designed in a 65 nm CMOS process, the presented ADC achieves a peak SNDR of 71.5 dB at 1.1 MHz, while consuming 0.16 mW.

A summary of the prior state-of-the-art of hybrid/combined topologies-based NS-SAR ADCs is presented in Table 2.6.

Table 2. 6. Summary of combined/hybrid topology-based NS-SAR ADCs.

Ref.	Tech. (nm)	V_{DD} (V)	BW (MHz)	OSR	ENOB (Bits)	SNDR (dB)	P_{avg} (µW)	FoM_S (dB)	FoM_W f.J/C-step)	Comments
[194]	65	0.8	6.25	4	9.35	58	120.7	166	14.8	Fully passive; OP-AMP free
[195]	40	1	50	4	-	70.4	13000	166.3	48.1	Calibration-free; TI EF topology; Open-loop amplifier
[196]	40	1.1	50	4	-	69.1	8500	166.8	36.3	Full dynamic; passive loop filter, TI,
[197]	65	1.1	625	8	-	84.8	119	182	6.6	EF-CIFF; only single dynamic amplifier; hardware reuse kT/C cancellation method
[198]	22	-	80	4	-	66.3	2560	171.2	9.48	Passive; Calibration-free; Amp-free
[199]	40	-	3.5	64	-	78.7	5040	167.1	-	BP ΔΣ with N-path filter and NS-SAR;
[200]	130	1.2	0.125	8	-	79.57	96	170.7	-	3rd order; EF + CIFF
[201]	28	1	1	50	-	84.2	1620	172.1	-	VCO-based continuous time ΔΣM with NS-SAR quantizer
[203]	28	1	25	8	-	77.2	2030	178.2	6.8	Pipeline SAR with CIFF-based NS-SAR quantizer; Q-prediction unrolled gain error shaping method
[204]	28	1	0.15	815	-	92.5	160	182.2	15.6	Incremental Zoom with 2ed order EF-based NS-SAR;
[205]	28		100	3.8	-	70.15	4520	173.6	8.6	4th order NS-SAR Pipeline; EF+CIFF based NS
[206]	65	1.2	1.25	8	-	83	335	178.7	11.6	4th order Pipeline; EF NS-SAR in 1st stage; 2nd order CIFF NS-SAR in second stage; Sharing of dynamic amplifier
[207]	28	0.9	2.5	8	-	75	150	177.2	6.5	1st order EF-CIFF NS-SAR; without multi-input comparator; reuse of integrator in both paths
[202]	28	-	12	10	-	69	2500	165.8	45.2	4h order ΔΣM with 2× TI high pass NS-SAR; DAW CADCA mismatch calibration
[208] [209]	28	1	30	5.5	-	73.2	3070	173.1	-	2× TI NS-SAR; Calibration free; shared dynamic amplifier;
[210]	22	1	0.2	24	-	80.4	320	172.3	-	3rd order DTΔΣM with passive NS and digital noise coupling; uses DWA
[211]	40	1.1	5	6	-	84.2	1840	178.6	13.8	With SF input buffer; DAW; ISI correction technique; 2ed order CIFF NS; foreground and background calibration
[212]	28	1.1	75	4	-	65.37	4015	168.1	17.65	3× TI 1st-order CIFF NS-SAR; DWA; fully passive integrator without multi-input comparator
[213]	-	-	10	20	-	90	-	-	-	Behavioral simulation results only; 2nd order CIFF-based passive NS-SAR
[214]	180	1.8	1.5	8	-	81.2	1800	170.4	-	Dual-residue pipeline ADC with 2ed order EF-based passive NS-SAR
[215]	28	1	15.625	16	-	81.6	6400	175.5	-	3rd order CT-ΔΣM with 1st order CIFF-based NS-SAR quantizer; no calibration
[216]	40	1.2	0.625	8	-	84.2	100	182	-	1-0 quasi–MASH NS-SAR; LSB repeating, Bridge crossing segmented CDAC
[217]	28		20	18.75	-	75.5	2780	174.1	14.3	4th order CTΔΣM with CT NS-SAR; AC-DC coupled Negative-R
[218]	65	0.4-2.5	2.5		14	84.2	5.2/channel	173.1	71.5	64 array of 1st order NS-SAR in a bidirectional peripheral nerve interface IC
[219]	22		100	3	-	78	15000	-	13	4th order MASH NS-SAR; only simulated; highest BW; Lowest OSR
[220]	65	1.2	.03125	16	-	80	7.3	176.3	14.3	2 identical passive IIR filter; duty-cycled OP-AMP; 1st order MES

[221]	130	1.2	0.125	8	12.93	79.57	96	170.7	-	Hybrid 3rd order NS; dither digital calibration for CDAC
[222]	180	1.8	1	5	14.56	89.4	880	-	-	2nd-order passive-active integrator-based loop filter; monotonic switching method
[223]	28	1	20	6.5	-	79.1	3100	177.2	10.5	SR-assisted NS-SAR Pipeline; 2nd - order EF NS in second stage; gain an offset calibration
[224]	65	1.3/0.8	1-500	100	-	94.5	5.2	174.3	-	NS-SAR assisted ΔΣM with 4th order truncation error shaping
[225]	28	1	100	8	-	67.5	13400	166.2	34.6	Hybrid-loop ΔΣM with bandpass EF NS-SAR as quantizer; one of the highest BW
[226]	180	1.2	0.5	8	-	82.7	4.3	162.5	-	AFE-embedded 2nd-order EF NS-SAR; chopper-based high-pass IIR Filter
[227]	-	-	0.200	8	-	104.3				Behavioral simulations only; 3rd order
[228] [229]	65	1.2/2/	0.5	5	-	84.1	133.8	180	10	4th order hybrid NS with fully dynamic amplifier; embedded with input buffer
[230]	28	1	0.01	20	-	79.5	1260	178.5	8.5	NS-SAR Assisted pipeline; Code-counter-based offset calibration
[231]	40	1.2	12.5	20	-	80.9	3700	176.1	-	4th order CT-ΔΣM with 2nd-order DT NS-SAR as quantizer
[232]	65	1.1	1.1	11	-	71.5	160	169.9	23.3	1-1 MASH with passive NS-SAR and VCO ADC;

Chapter 3

A SINGLE-CHANNEL 8-BIT ENOB SAMPLING-RATE RECONFIGURABLE ASYNCHRONOUS SAR ADC

Chapter Abstract

This chapter provides design detail and results of the first ADC chip, i.e., 8-bit ENOB sampling-rate reconfigurable asynchronous SAR ADC following a top-down approach. The chapter starts with a brief description of the aptness of the proposed ADC architecture for the targeted application, followed by ADC targeted specifications. ADC architecture, system level considerations, its sampling-rate reconfigurability, and versatility are illustrated after that. Verilog-A based implementation of the ADC is part of section 3.6, followed by a step-by-step design process of ADC components at schematic level with layout considerations in section 3.7. Section 3.8 is devoted to version 2 of the ADC with its delay-cell and digital section operating at 1.2 V. Schematic level, post-layout level and measurement results are part of section 3.6, 3.10, and 3.11, respectively, followed by the ADC comparison with other similar ADCs in section 3.12.

3.1. Suitability and Potential of Proposed Sampling-Rate Reconfigurable ASAR ADC for Multi-channel ASICs for Space Applications

Before describing the architecture and design procedure of the proposed ASAR ADC, this section outlines its suitability for the targeted application, i.e., multi-channel ASICs for space applications. Figure 3.1 depicts a simple pictorial representation of an architecture of a 64-channels ASIC with the proposed self-clocked ASAR ADC solution as well as with the traditional clocked ADC solutions. Unlike the clocked ADC solutions, the ASAR ADC-based solution uses only a single 'Start-of-Conversion (SOC)' signal, which is a low-frequency and low duty-cycle signal, to start the conversion process. This signal can be applied in two ways: (i) externally in form of a 'CLKsampling' signal, or (ii) by the analog front-end section of the ASIC when analog-to-digital conversion is needed. All the other required clock signals are generated internally inside the ADC, thus making the ADC self-clocked. This offers an enormous advantage in terms of crosstalk and interference issues, switching noise, and clock jitter and synchronization. There is no need for a dedicated on-chip clock generation circuit for the ADC, thus saving power, chip-area, and complexity. Low switching 'CLKsampling/SOC' signal does not cause high switching noise. In addition, it reduces the occurrence of crosstalk. Moreover, issues associated with clock distribution, such as clock jitter, are reduced. The proposed ASAR ADC is configurable with respect to its sampling-rate (f_s) with a proportional power consumption. Thus, its f_s can be tuned by the analog frond-end of the ASIC, based on the activity-rate of the events (X/ɣ-rays) on its inputs from the SDDs. The ADC activity can be stopped by the analog front-end section in case of no event detection by the SDDs, thus saving power. This makes this ADC a true event-triggered or activity-driven architecture. In summary, the proposed ADC meets all the requirements of multi-channel ASICs for space applications mentioned in section 1.7. This will be highlighted in the following sections.

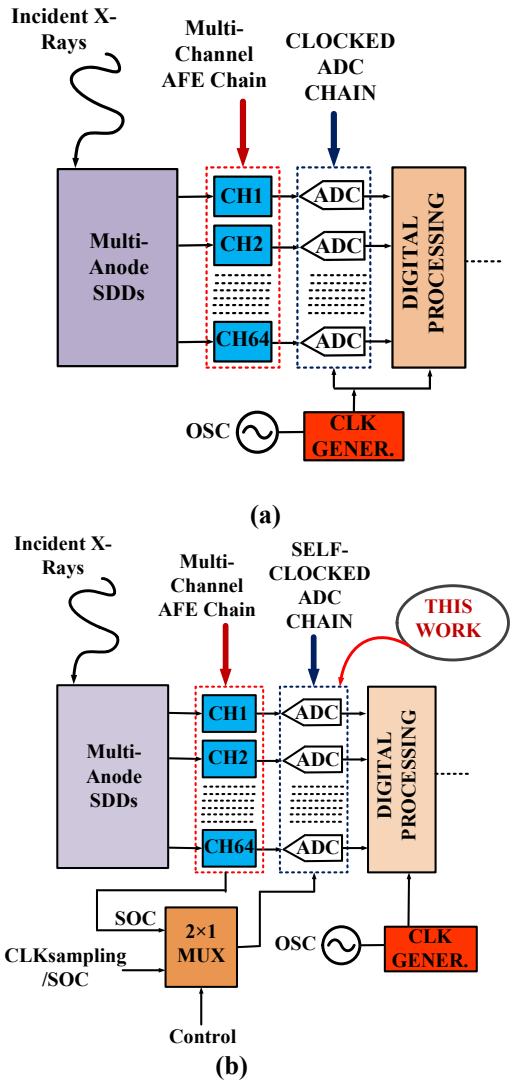


Figure 3. 1. Architecture of a 64-channels ASIC with (a) conventional ADC-based chain, and (b) proposed ASAR ADC-based chain. The use of 64 channels in the diagram is just for a simplification purpose, otherwise the total number of channels can be as high as 1024 or even more.

3.2. Proposed ASAR ADC: Specifications

Tabel 3.1 shows the targeted specifications of the ASAR ADC set initially. All the specifications are the same as mentioned in Table 1.2 of this thesis, except the ENOB and SNDR. Although required ENOB and SNDR are 10-12 bits and 72 dB, respectively, relatively low values of these metrics are set for the ASAR ADC design. To achieve such a high ENOB (10-12 bits) and SNDR (72 dB), the first obvious choice is to get these by designing a 10-12 bits ASAR ADC. However, it is well-known that getting an ENOB more than 8-bits (and SNDR more than 50 dB) is extremely challenging for an ASAR ADC without the use of special techniques, such as CDAC calibration and trimming, comparator offset cancellation, etc. The use of these techniques enhances design complexity, area, power, and failure-rate. A superior alternative approach to achieve this goal is to first design an 8-bit ASAR ADC without the use of any complicated technique, and then enhance its ENOB by introducing noise-shaping technique to 8-bit ASAR ADC. This thesis adopts the latter-mentioned approach. Thus, the first objective is the design and fabrication of an 8-bit ASAR ADC with specifications of Table 3.1. Once accomplished, the second target is to enhance performance of 8-bit ASAR ADC with the help of noise-shaping. This chapter focuses on the design detail of the first objective, while chapter 4 deals with the second objective.

Table 3. 1. Targeted Specifications of ASAR ADC

Specification	Value
Technology Process (nm)	350
Resolution/ENOB (Bits)	8
Typical Bandwidth (kHz)	20
ENOB (Bits)	8
DNL (LSB)	≤ 2
INL (LSB)	≤ 2
THD (%)	0.2
Typical $f_s(kHz)$	40
SFDR (%)	0.1
SNDR (dB)	48
P_{cons} (µW)	As low as possible (~ 100 µW)
Input Signal Swing (V)	0.65-2.65 centered at 1.65 V
Supply (V)	3.3
Offset errors	Must be Temperature-independent
Gain Mismatch errors	Must be Temperature- independent

3.3. Proposed ASAR ADC: Architecture and System-level Considerations

Figure 3.2 shows the architecture of the proposed ASAR ADC. It consists of an 8-bit binary-weighted CDAC with its switches network, a fully dynamic StrongArm latched comparator followed by an SR-latch, a SAR logic, circuitry to generate internal clock for the comparator (CLK_{CMP}) and SAR logic (CLK_{int}), and a variable rising edge only delay-cell. Four on-chip closed-loop buffers are also part of the ADC, which are not depicted in Figure 3.2 for simplicity reason. These include an input voltage (V_{IN}) buffer, a common-mode voltage (V_{CM}) buffer, an upper voltage reference (V_{REFP}) buffer, and a lower voltage reference (V_{REFN}) buffer.

3.3.1. Input Signal Swing

As evidenced from Table 3.1 and Figure 3.2 (a), the input signal swing of the ADC is 2 V (1.65 ± 1V). Thus, $V_{REFP} = 2.65\,V$ and $V_{REFN} = 0.65\,V$ have been chosen. This leads to an LSB of 7.8 mV ($\frac{V_{REFP}-V_{REFN}}{2^N}$), where N = 8. Selection of such a high input signal swing provides two advantages. First, it facilitates a direct integration of the ADC with the analog front-end section of not only the multi-channel ASIC for space applications, but also with the high voltage sensors for several other practical applications, thus making the ADC versatile, flexible, and multi-purpose. Second, it makes the ADC less sensitive to crosstalk and interference - issues inevitable in multi-channel solutions - compared to a low input signal swing-based ADC. However, the downside is high power consumption and lower energy-efficiency of the ADC in comparison with low input signal swing-based ADCs because of the use of high supply voltage to enable high input signal swing operation.

3.3.2. Single-ended Architecture

Instead of a differential architecture, a single-ended solution has been chosen because of several reasons. First, the signal arriving from the analog front-end section of the targeted eXTP ASIC is single-ended. Thus, selecting a single-ended architecture enables a direct interface of the analog front-end with the ADC without the need of any single-ended to differential conversion. Second, the single-ended solution occupies lesser chip-area than a differential implementation. The overall area of the ASAR ADC is dominated by its CDAC. The CDAC area becomes double in a differential architecture in comparison with a single-ended architecture for the same number of bits. Third, single-ended solution is more power-efficient than

differential implementation, especially with respect to power contribution form the CDAC. Fourth, single-ended architecture offers a reduced loading effect to the previous stage of the ADC, i.e., analog front-end section of the ASIC. Fifth, the design complexity of a single-ended solution is lower than a differential implementation because of the above-mentioned reasons.

3.3.3. Bottom-plate Sampling

For sampling of the input signal, two approaches are popular in ASAR ADC: top-plate and bottom-plate sampling methods. A bottom-plate sampling has been adopted for this design. The primary reason for this choice is that the bottom-plate sampling method is more robust than the top-plate sampling method with respect to the parasitic capacitances associated with the critical CDAC node, labelled as V_{DAC} in Figure 3.2 (a). The CADC node parasitic capacitances are known to significantly affect the SAR ADC performance. This is especially valid for a single-ended SAR architecture – the selected architectural choice for this design. In addition, the bottom-plate sampling eliminates the input dependent charge injection [233] unlike the top-plate sampling method.

3.3.4. Conventional CDAC Switching Scheme

Because of the use of binary-weighted CDAC, conventional CDAC switching scheme has been chosen for the design, as shown in Figure 3.2. (c). Although offering a simple implementation benefit, the chosen switching scheme is not optimized with respect to the CDAC switching energy perspective. There are various other CDAC switching schemes, which offer better energy-efficiency. Monotonic or set-and-down switching is such a widely-used scheme [87], which offers 81 % reduction in switching energy and 50 % reduction in the CDAC capacitance as compared to conventional switching scheme. However, implementation of this scheme requires a differential CDAC architecture. Another energy-efficient switching technique is V_{CM}-based switching, which saves 87 % energy as compared to conventional switching scheme. However, this is also suitable only for a differential implementation. Bidirectional switching method [233] is another such scheme, which reduces the total CDAC capacitance by 2 times compared to monotonic switching scheme and 4 times compared to conventional switching method. In addition, it secures an 86 % reduction in the CDAC reference power. However, it also needs a differential CDAC. Thus, these techniques are not applicable for the single-ended solution.

There are a few energy-efficient switching schemes which are suitable for single-ended architecture. The CDAC switching scheme proposed in [89] for a single-ended ASAR ADC reduces 50 % of the total CDAC capacitor and 87.5 % CDAC switching-energy in comparison with conventional single-ended switching method. However, these benefits come at the cost of an added design complexity, since the design needs an additional network to cancel the errors caused by the CDAC parasitics as well as comparator offset. In addition, it uses a bridge capacitor CDAC topology, which is known to be susceptible to parasitics impacts. Another switching scheme suitable for single-ended solutions has been presented in [234], which provides a 92.3 % saving in switching energy in comparison with conventional switching scheme. However, this method needs top-plate sampling topology, which is more prone to parasitics than bottom-plate method. In addition, the proposed method has only been verified using behavioral simulations, and thus does not include actual factors affecting the ADC performance.

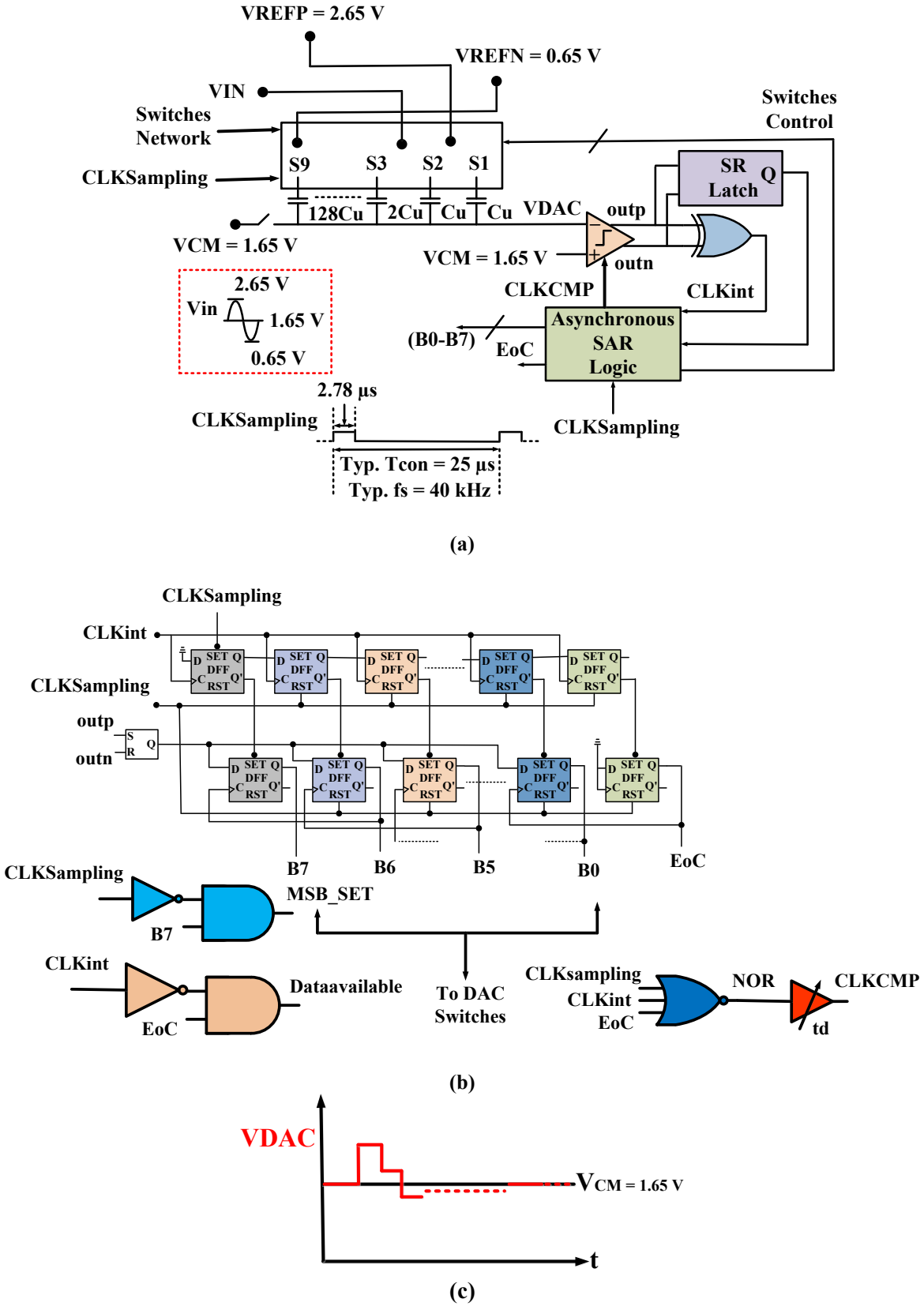


Figure 3. 2. (a) Architecture of the proposed ASAR ADC, (b) Schematic diagram of the proposed Asynchronous SAR logic with variable delay-cell, and (c) adapted CDAC switching scheme.

3.4. Proposed ASAR ADC: Operation and Working Principle

Figure 3.3 shows timing waveforms of the ADC operation. The ADC operation is divided into two phases: sampling and conversion. The ADC starts its operation with the sampling phase at the rising edge of the 'CLKSampling' signal, where the sampling of the input signal (V_{IN}) is performed. During this phase, the top plates of all CDAC capacitors are connected to the common mode voltage (V_{CM}), while the bottom plates are connected to the input signal (V_{IN}) through relevant switches (Figure 3.4). At the falling edge of the 'CLKSampling' signal, the sampling phases ends, and the conversion phase starts. At the beginning of this phase, the most significant bit (MSB) is set high with the help of the 'MSB_SET' signal. This is achieved by connecting bottom plate of the MSB capacitor of the CDAC to upper voltage reference (V_{REFP}), while bottom plates of all other capacitors are connected to low reference voltage (V_{REFN}). At the same time, top plates of all capacitors are disconnected from V_{CM}. Besides the MSB setting in the start of the conversion phase, the output of the NOR gate 'NOR' also goes high. Ideally, the 'NOR' signal is supposed to function as an internal clock for the comparator. But the CDAC needs sufficient time for the MSB settling before comparator can make its first comparison. Therefore, a delay, with an amount adequate for the CDAC settling, has been introduced to the 'NOR' signal. A unique asymmetrical variable delay-cell has been proposed for this design, which provides desired delay only to the rising edge of the 'NOR' signal. The rising edge only delayed version of the 'NOR' signal (CLK_{CMP}) acts as comparator clock.

At the arrival of the rising edge of the CLK_{CMP} signal, comparator makes its first decision by providing its outputs (outp and outn), which are stored in an SR-latch. With the comparator decision, the output of the XOR gate (CLK_{int}) goes high. The CLK_{int} acts as an asynchronous clock for the SAR logic. The rising edge of the CLK_{int} activates the relevant D flip-flops (DFF) in the SAR logic to not only generate the MSB/B7 bit decision, but also control signals for the CDAC switches to set MSB-1/B6 bit for the next bit decision. With the rising edge of the CLK_{int} signal, the 'NOR' signal goes low. This forces the CLK_{CMP} signal to turn low as well because of the rising edge only effect of the delay-cell. Lowering of the CLK_{CMP} forces the CLK_{int} to go low, which leads to the next rising edge of the 'NOR' signal. This 'NOR' signal is delayed again by the rising edge only delay-cell to generate the CLK_{CMP} to enable comparator's next decision. The same process continues until the conversion of all 8 bits is done. At this stage, the 'EoC' signal stops the conversion phase by deactivating the CLK_{int} and CLK_{CMP} signals. 8-bit output data is ready to be acquired at the rising edge of the 'dataavailable' signal. The next sampling phase starts at the rising edge of the subsequent 'CLKsampling' signal, which resumes the ADC normal operation, as described above.

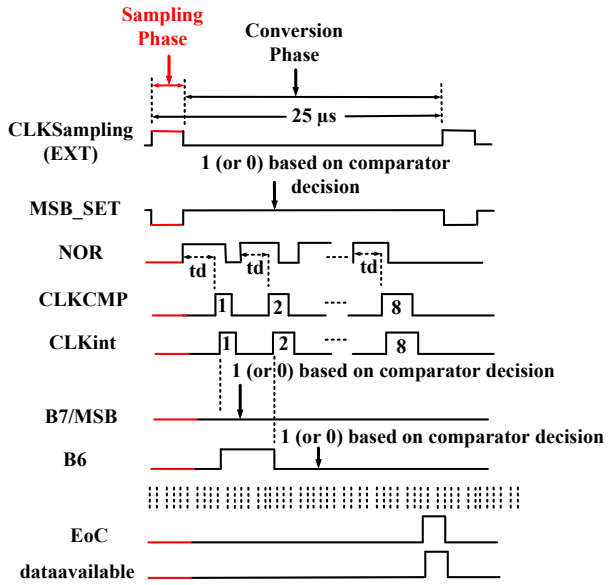


Figure 3. 3. Timing Waveforms of the ASAR ADC depicting its operation.

Figure 3.4 shows the status of the CDAC switches for the first three CDAC switching (sampling phase, MSB, and MSB-1 phases). The ADC requires 8 clock cycles of asynchronous clocks (CLK_{CMP} and CLK_{int}) to complete the conversion. Typical conversion time of the ADC is 25 µs, leading to a typical sampling-rate of 40 kHz. The ADC, however, is reconfigurable with respect to its sampling-rate and bandwidth, as described in detail in section 3.4.1.

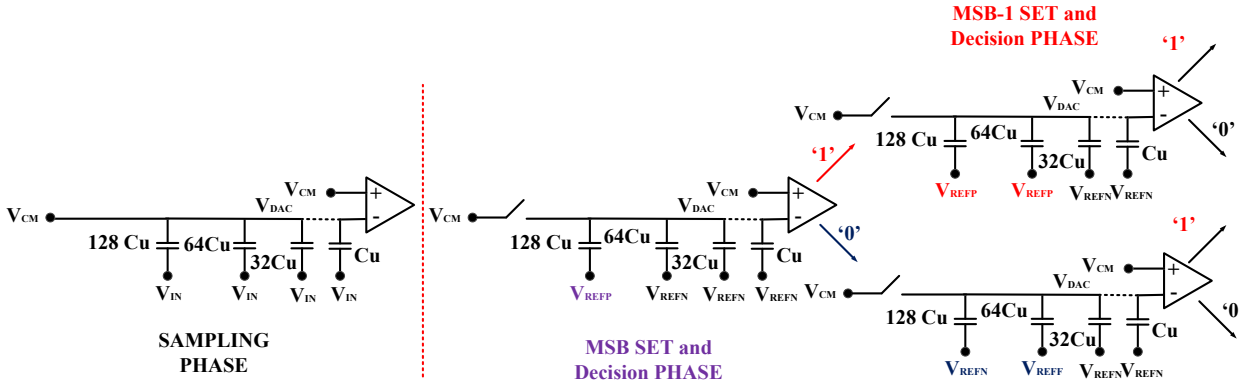


Figure 3. 4. CDAC switching status for sampling, MSB and MSB-1 decision phases.

3.4.1. Proposed ASAR ADC: Sampling-Rate Reconfigurability Operation

As evidenced by the ADC operation described in section 3.4, comparator clock CLK_{CMP} is generated by providing an adequate delay to the 'NOR' signal. Also, the CLK_{int} signal depends on the CLK_{CMP} signal since it is the output of the XOR gate with comparator outputs (outp and outn) as its inputs. Therefore, the time-period and frequency of both of these internal clock signals are dependent on the amount of the delay introduced by the delay-cell. For a minimum adequate delay, i.e., a delay amount which is adequate for the CDAC settling, the ADC finishes the conversion phase well before the arrival of the rising edge of the next 'CLKSampling' signal because of the fast switching of both the cock signals. Assuming a typical conversion time of 25 µs, the ADC completes all 8 conversions and becomes idle; it remains idle until the arrival of the rising edge of the next 'CLKSampling' signal, as shown in Figure 3.5. With a maximum delay value introduced, the ADC completes the conversion phase just before the arrival of the rising edge of the subsequent 'CLKsmapling' signal, thus finding a little idle time duration, as shown in Figure 3.5. We call it observation 1.

The sampling-rate of the ADC is dictated by the time-period/frequency of the 'CLKSampling' signal. This signal, either provided externally or by the analog front-end section of the ASIC, is well-controlled with respect to its time-period. We call it observation 2. Based on observation 1 and 2, the ADC can be made sampling-rate reconfigurable by making the delay-cell variable according to the delay range. However, this is only attractive if the power consumption of the ADC also scales accordingly without any performance degradation of the ADC. Especially, the biasing currents of the voltage reference (V_{REFP} and V_{REFN}) buffers are also change accordingly. With the help of extensive simulations, it is verified that the buffers biasing currents scale proportionally with the delay value. For halving the delay value, the biasing currents needed for the buffers double with the same performance from ADC; this alternatively means the sampling-rate of the ADC doubles by halving the time-period of the 'CLKSampling' signal. We call this observation 3. Table 3.2 shows the summary of buffers current vs delay value results got using simulations.

Based on observation 1, 2, and 3, it is concluded that the ADC is capable of exhibiting sampling-rate reconfigurability with a constant power-efficiency for each sampling-rate. Thus, the delay-cell has been made variable to facilitate sampling-rate reconfigurability. In addition, a desired number of voltage reference buffer slices of each type have been integrated on-chip. Both the delay-cell and voltage reference buffers can be controlled externally and independently.

Despite the ability of the ADC to exhibit a large range of sampling-rates with the help of delay-range and number of voltage reference buffer slices, only 8 buffer slices have been integrated in parallel to avoid chip-complexity. This results in 8 different sampling-rates supported by the ADC with constant power-efficiency. Figure 3.6 shows a pictorial representation of 8 buffer slices integrated in parallel to get sampling-rate reconfigurability with their external control logic. Delay-range (maximum and minimum delay amount) from the delay-cell has been chosen according to the selected number of buffer slices. This led to a maximum delay (t_{dmax}) amount of 2.2 µs and minimum delay (t_{dmin}) amount of 275 ns. For t_{dmax}, only 1 buffer of each type is enabled, while all 8 buffers are enabled for t_{dmin}. Figure 3.7 shows sampling-rate reconfigurability operation of the ADC with the help of its timing waveforms.

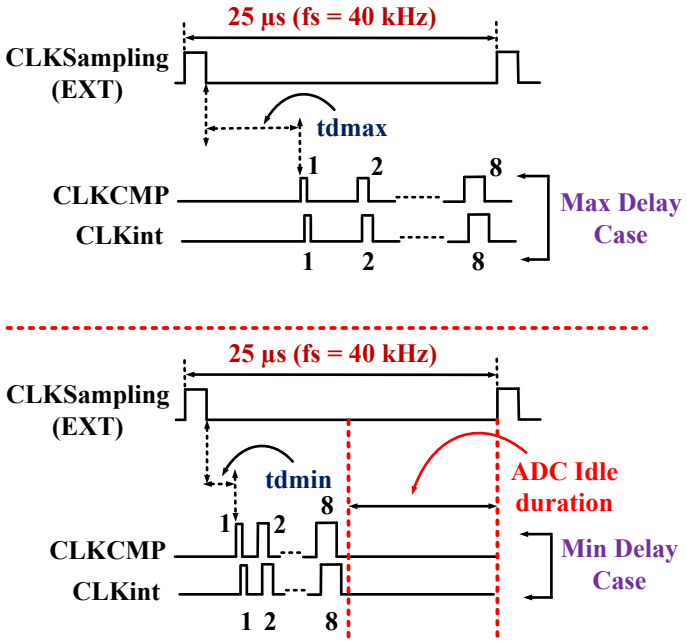


Figure 3. 5. ASAR ADC timing waveforms for maximum delay (t_{dmax}) case and minimum delay (t_{dmin}) case to illustrate its potential for sampling-rate reconfigurability.

Table 3. 2. Relationship between delay value and Biasing current of voltage reference buffers

Sr. No	Delay Value	Buffer current (µA)	ENOB (Bits)	Comments
1	2.2 µs	2	7.78	1. Maximum Delay 2. Current of a unit buffer
2	1.1 µs	4	7.81	1. 1/2 of maximum delay (double sampling-rate in comparison with maximum delay case 2. Double current wrt unit buffer
3	550 ns	8	7.86	1. 1/4 of maximum delay (4 times sampling-rate in comparison with maximum delay case 2. 4 times current wrt unit buffer
4	275 ns	16	7.91	1. 1/8 of maximum delay (8 times sampling-rate in comparison with maximum delay case 2. 8 times current wrt unit buffer

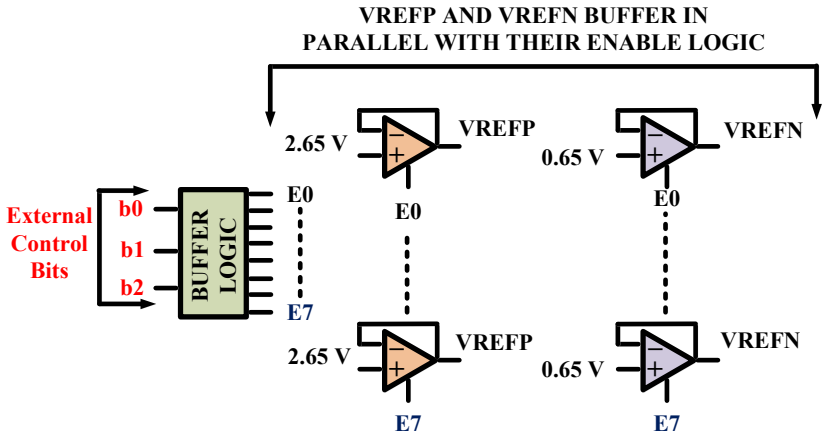


Figure 3. 6. Multiple (8 for this ADC) voltage reference buffer slices integrated in parallel with their external control to get sampling-rate reconfigurability.

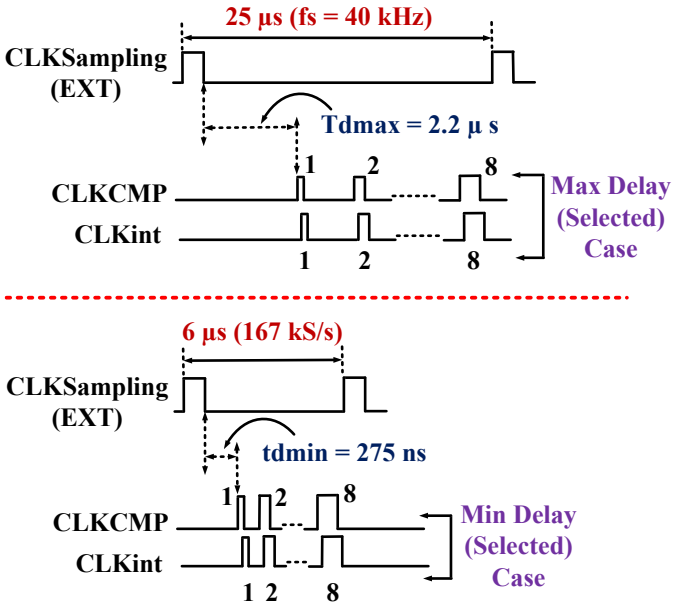


Figure 3. 7. Sampling-rate reconfigurability functionality of the ADC: Timing Waveforms. Only one reference voltage buffer is enabled for t_{dmax}, while all 8 buffers are turned on for t_{dmin}.

3.5. Proposed ASAR ADC: Flexibility and Versatility Capability

Compounded with sampling-rate reconfigurability, there is another factor which enhances flexibility and versatility of the ASAR ADC. It is also adaptable with respect to the duty-cycle of the 'CLKSampling' signal besides its frequency. For example, varying the logic high duration of the 'CLKSampling' signal has a direct effect on the settling requirements as well as power consumption of the input (V_{IN}) and common mode (V_{CM}) buffers, because these buffers are needed and thus enabled only during the sampling phase. There are scenarios where the duration of sampling phase can be reduced. The cases where input and common buffers are implemented off-chip is one such scenario. Because of off-chip buffers, the duration of sampling phase of the ADC can be reduced, which results in an enhanced time for the conversion phase. Another such situation can be the use of the ADC for analog front ends of ASICs or sensors accompanied by a sample and hold circuit by itself, such as VEGA ASIC of [11]. Figure 3.8 shows a pictorial representation of ADC working with reduced sampling phase.

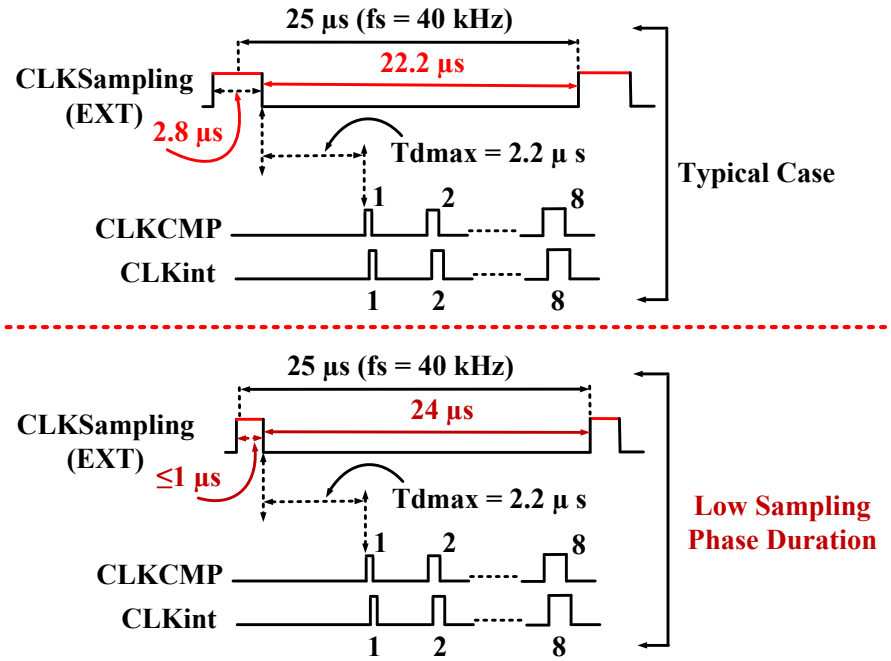


Figure 3. 8. Flexibility of ADC with respect to the 'CLKSampling' signal: ADC timing waveforms with reduced sampling phase duration, which can relax the settling time and power consumption of input and common mode buffers.

The fact that the 'CLKSampling' is tunable with respect to its frequency can also be useful for sampling-rates lower than typical (40 kHz). Considering the case of a 4 kHz sampling-rate, as shown in Figure 3.9, the 'CLKSampling' can be applied accordingly. In this case, the ADC performs all 8 conversions well before the arrival of the rising edge of the next 'CLKSampling' signal and becomes idle, thus consuming no power. This scenario is particularly attractive if the voltage refence buffers are either implemented off-chip or they are tuned off right after the completion of all 8 conversions by the ADC.

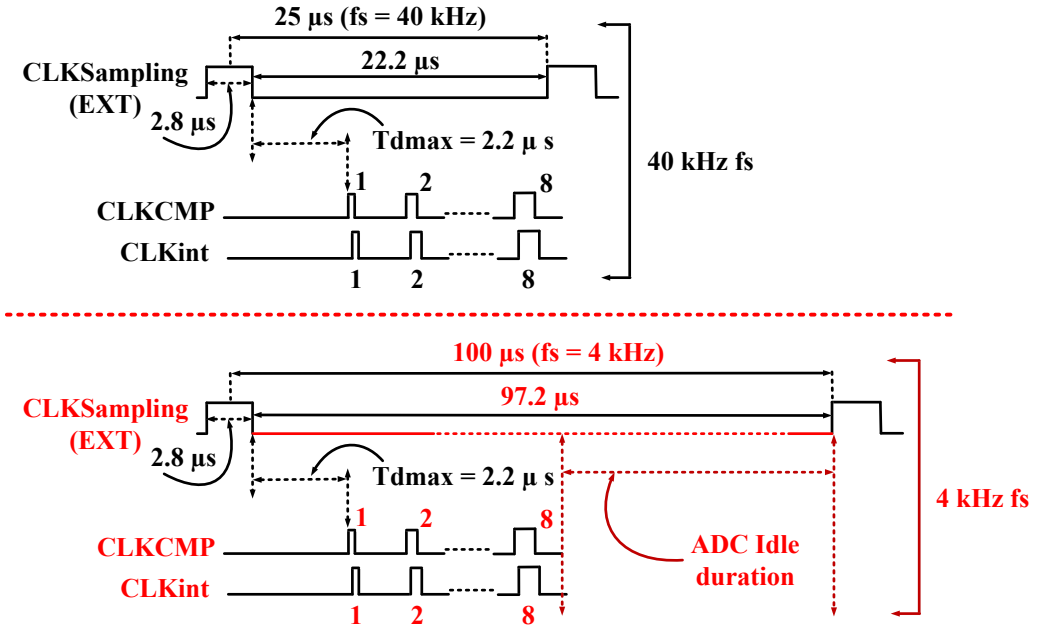


Figure 3. 9. Flexibility of ADC with respect to 'CLKSampling' signal: ADC timing waveforms with a sampling-rate lower (4 kHz) than typical (40 kHz). ADC has the ability to consume no power during its idle duration.

3.6. Proposed ASAR ADC: Verilog-A based Circuit Design

After the system level considerations and architecture study, the next step is the circuit level implementation and simulation of the ADC in Cadence Virtuoso environment. Before transistor-level design, the intermediate step is the use of Verilog-A based modeling of the ADC, which is done by creating Verilog-A based behavioral blocks of the ADC. Verilog-A based implementation enables study and optimization of the ideal behavior of whole ADC circuit. Once Verilog-A based implementation of the ADC is done successfully, the transistor level implementation is started step-by-step replacing each Verilog-A based ideal block by transistor level counterpart and verifying its functionality. This ensures a smooth and structured transition towards the real transistor level implementation.

3.6.1. 8-Bit Bottom-Plate Sampling Binary-Weighted CDAC with Switches Network

As mentioned earlier, a binary-weighted charge redistribution single-ended CDAC has been chosen for the ADC. This type of CDAC exploits the charge stored in the capacitor array to produce output voltages based on the input digital codes. For an 8-bit CDAC, 256 digital codes can be represented by as many voltages. The full-scale range of the ADC dictates the range of these voltages. As mentioned in Table 3.1, the full-scale range of the ADC is 2 V (1.65 ±1 V). This leads to an LSB value calculated below:

$$\text{LSB} = \frac{V_{FS}}{2^N} = \frac{2}{2^8} = 7.8\ \text{mV}$$

Figure 3.10 depicts the transfer characteristics of the ideal CDAC. As visible from Figure 3.10, each 256 digital values correspond to 256 equally spaced (7.8 mV) voltages. Circuit diagram of the CDAC is depicted in Figure 3.11. To get the selected full-scale range of the ADC, two reference voltages (V_{REFP} and V_{REFN}) have been chosen in following way:

$$V_{FS} = V_{REFP} - V_{REFN}$$

As the supply voltage for the ADC is 3.3 V, it is logical to define a common mode voltage ($V_{CM} = 1.65$ V) around which the input signal as well as voltage references (V_{REFP} and V_{REFN}) are centered. This leads to $V_{REFP} = 2.65$ V and $V_{REFN} = 0.65$ V, because the input signal has a full-scale of 2 V centered around $V_{CM} = 1.65$ V

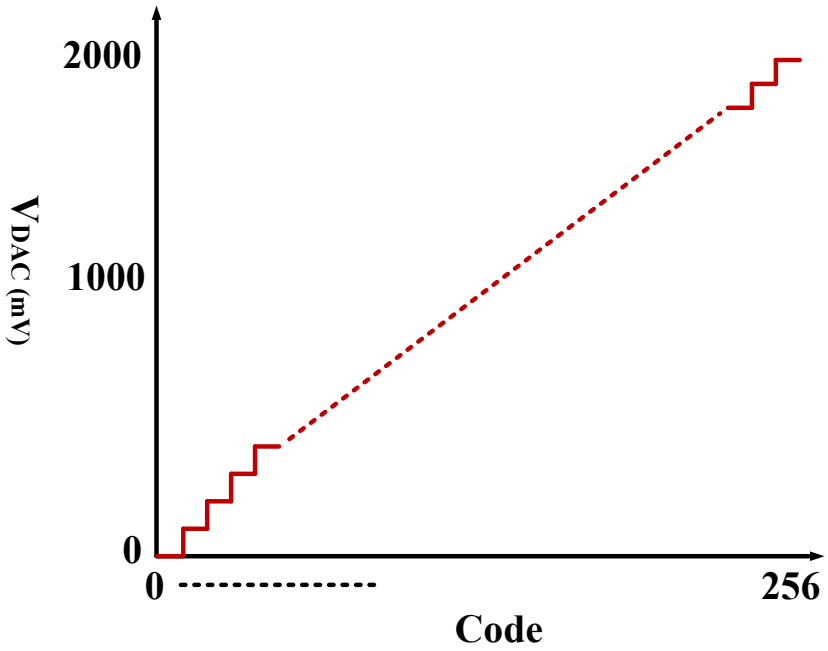


Figure 3. 10. Transfer characteristics of an 8-bit CDAC with a full-scale voltage of 2V.

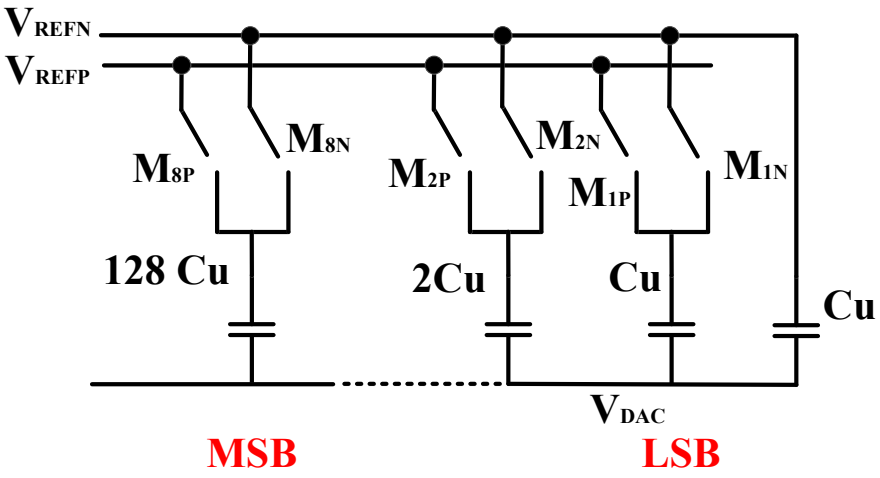


Figure 3. 11. Circuit diagram of an 8-bit binary weighted CDAC.

A switches network is part of the CDAC with various switches. These switches are driven by the bits of the digital word. The smallest capacitor (C_U) of the CDAC is for the LSB bit, while the largest ($128C_U$) is for MSB bit. For each capacitor, a PMOS has been selected as switch for V_{REFP} and an NMOS for V_{REFN}. Assuming the conversion of the digital word 11110000 into analog domain by the CDAC, the configuration of the switches will be as follows:

$M_{P8} = 1$ ($M_{N8} = 0$)

$M_{P7} = 1$ ($M_{N7} = 0$)

$M_{P6} = 1$ ($M_{N6} = 0$)

$M_{P5} = 1$ ($M_{N5} = 0$)

$M_{P4} = 0$ ($M_{N4} = 1$)

$M_{P3} = 0$ ($M_{N3} = 1$)

$M_{P2} = 0$ ($M_{N2} = 1$)

$M_{P1} = 0$ ($M_{N1} = 1$)

For Verilog-A based design, the ideal capacitors from AnalogLib of Cadence Virtuoso have been chosen for the CDAC implementation. However, all the switches have been implemented in Verilog-A with ideal behavior. Verilog-A code of the switches is provided in Appendix 1.

SAR ADC works on the basis of a binary search algorithm, where the input signal is compared with a threshold voltage generated by the CDAC. Therefore, the sampling of the input signal is necessary. This CDAC topology is inherently capable of performing the sampling of the input signal too. Figure 3.12 shows circuit diagram of the CDAC with inherent sampling of the input signal (V_{IN}). An additional switch is added for each CDAC capacitor for the input signal (V_{IN}), besides one switch for V_{CM}. All the CDAC capacitors are connected to V_{IN} through relevant switches driven by the signal M_S. After the sampling phase, the conversion phase commences, and charge is distributed across the CDAC capacitors dictated by the digital logic.

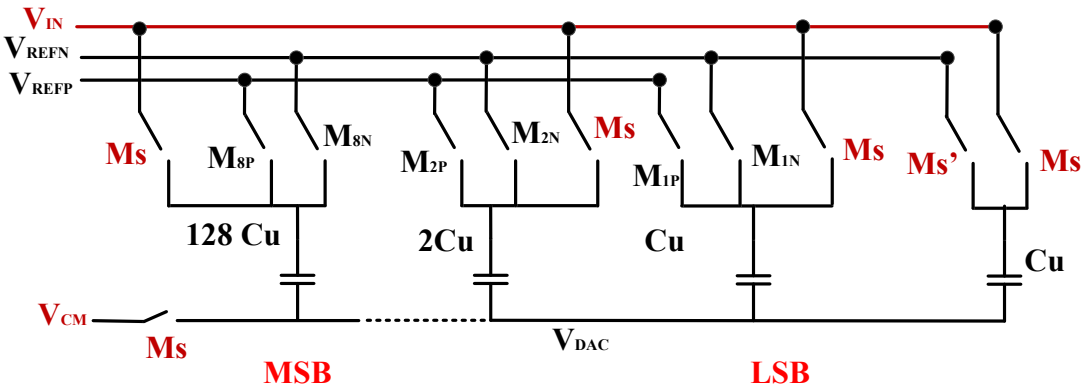


Figure 3. 12. Circuit diagram of an 8-bit CDAC with inherent sampling of the input signal.

3.6.2. Comparator with SR-Latch and Asynchronous Clock Generation for SAR Logic

During the conversion phase of the ASAR ADC, the input signal is compared with the continuously changing threshold voltage during every clock period. The comparison is performed using a comparator. The function of the comparator is to decide whether the input is larger or smaller than the generated threshold voltage. For the selected charge redistribution based CDAC with inherent sampling, the voltage at the top plate (V_{DAC}) of the CDAC capacitors is already the difference $V_{IN} - V_{th}$ once the charge distribution is completed after the CDAC settling. Thus, comparator needs to compare this voltage with the analog ground/common mode voltage (V_{CM}), thus making this process simple. The outputs of the comparator need to be stored in an SR-latch. For this design, a NAND-based SR-latch has been selected. Being an asynchronous SAR ADC, the clock for SAR logic needs to be generated internally. This is achieved by the use of an XOR gate, whose inputs are the outputs of the comparator. Figure 3.13 shows selected diagram of ASAR ADC with only comparator, SR-latch, and SAR logic clock generation circuit.

Verilog-A code of the comparator is provided in Appendix 1. SR-latch is implemented with the use of Verilog-A based NAND gates; Verilog-A code of a 2-inputs (N)AND gate is given in Appendix 1. Appendix 1 also shows Verilog-A code of an XOR gate.

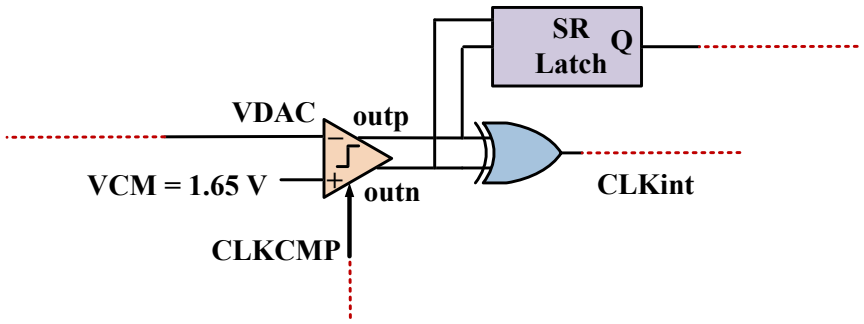


Figure 3. 13. Circuit diagram of comparator with SR-latch and XOR gate.

3.6.3. SAR Logic with Auxiliary Blocks Including Delay-Cell

The purpose of the SAR logic is to drive the CDAC switches in such a way that binary search algorithm is implemented. As shown in Figure 3.14, a shift register based SAR logic has been implemented for this design. The basic component of the SAR logic is D flip-flop. D flip-flops have been implemented using Verilog-A and then SAR logic has been realized using Verilog-A based D flip-flops. Verilog-A codes for D flip-fops used in the SAR logic are given in Appendix 1. All auxiliary gates of SAR logic have also been implemented using Verilog-A, whose codes are given in Appendix 1. Here, an ideal delay-cell from

AnalogLib of Cadence Virtuoso has been used. The working of the SAR logic, within the context of ADC working, has already been escribed in section 3.4.

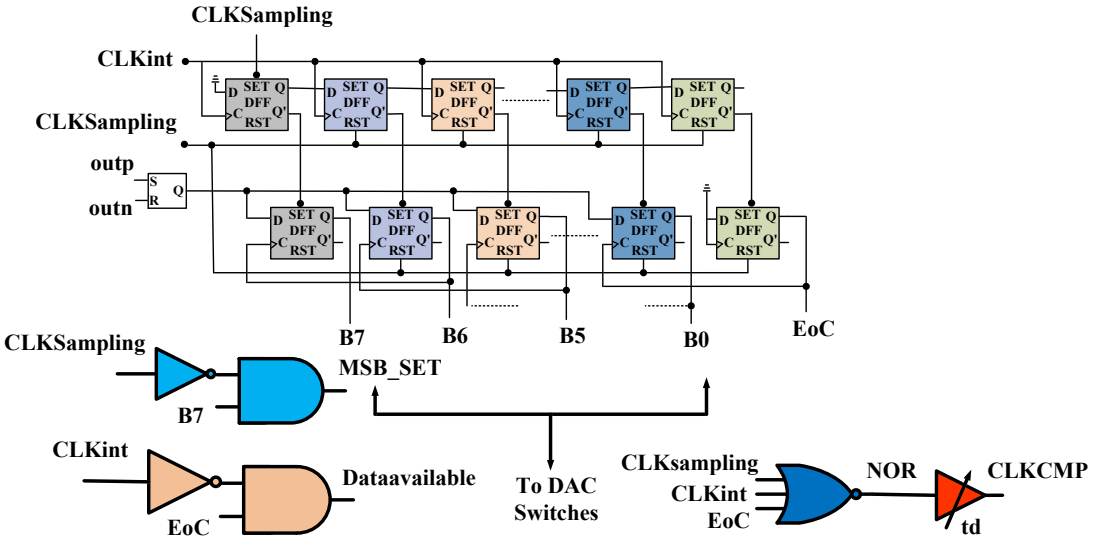


Figure 3. 14. SAR logic with auxiliary blocks and variable delay-cell.

3.6.4. Simulation Results of Verilog-A based Implementation

After complete realization of the ASAR ADC with Verilog-A, its performance has been verified by its Power Spectral Density (PSD) plot at typical sampling-rate (40 kHz), which is shown in Figure 3.15. As evident from the PSD plot, the ADC secures and ENOB of 7.84 bits, which is equivalent to 7.96 bits for a full-scale input. The SNDR of the ADC is 48. 9 dB. The achieved ENOB and SNDR confirm the correct functionality of the proposed ASAR ADC architecture.

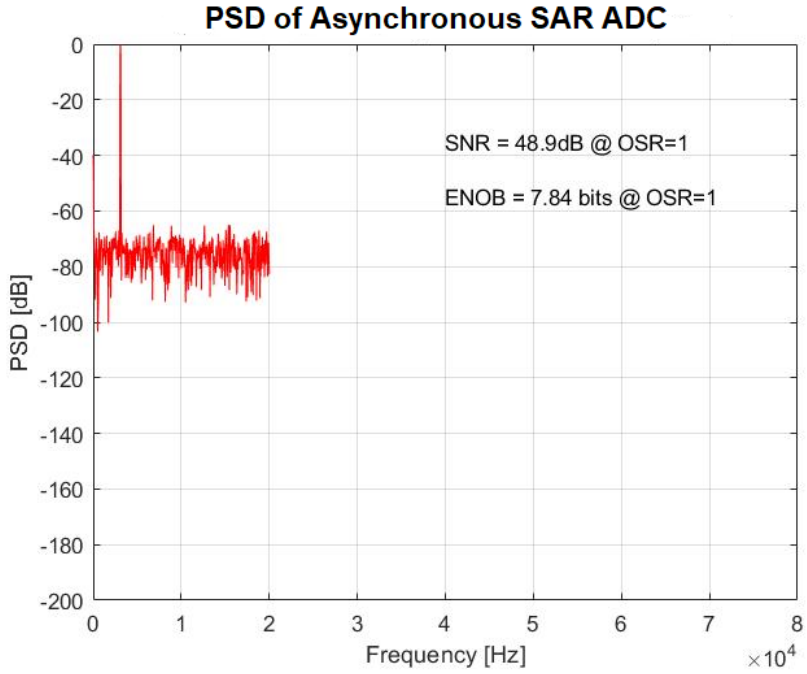


Figure 3. 15. PSD plot of ASAR ADC based on Verilog-A implementation. Here $f_s = 40\ kHz$; $f_{in} = 3\ kHz$; $V_{in} = -0.8\ dBFS$.

3.7. Proposed ASAR ADC: Transistor-Level Circuit Design with Layout Considerations

After successful Verilog-A implementation of the proposed ADC, the next step is the implementation of the ADC with real components. This section describes the step-by-step process of transistor-level development of the ADC with the design detail of each of its components. After description of the design process of each component, the Verilog-A based component will be replaced by the transistor-level component to verify ADC performance. In addition, layout design of each component is also part of this section.

3.7.1. Comparator Implementation

3.7.1.1. Selection of Comparator Circuit

As discussed in section 3.4, the asynchronous clock CLK_{CMP} is the delayed version of the NOR signal. Because of the rising edge only effect introduced to the CLK_{CMP} signal, a fully dynamic comparator architecture with a single clock-phase, and rail-to-rail output is needed. The first step is the selection of a suitable comparator circuit meeting these requirements. There are two contemporary comparator architectures, which can be a good choice: StrongArm [235], and the Miyahara latch [236]. StrongArm latch has been chosen because of its simpler and robust design-based advantages. In addition, the input-referred-noise of StrongArm comparator is slightly lower than Miyahara latch [237]. Moreover, it draws no static current. Furthermore, its offset primarily depends on its input pair. The use of StrongArm latch also offers a dedicated advantage for the proposed ADC architecture. As the duty-cycle of comparator clock CLK_{CMP} is always far lower than 50 % because of the rising edge only delayed effect to the NOR signal, the use of StrongArm is better from energy-efficiency point-of-view too because of its fully dynamic nature. Figure 3.16 shows circuit diagram of the StrongArm latched comparator.

3.7.1.2 StrongArm Comparator Circuit Operation

The circuit operation starts by precharging nodes P, O, outp, and outn to V_{DD} when the CLK_{CMP} is low. We symbolize the capacitance at these 4 nodes as C_P, C_Q, C_{outp}, and C_{outn}, respectively. Furthermore, we assume that $C_P = C_Q$ and $C_{outp} = C_{outn}$. We call this mode 1. As the CLK_{CMP} goes low, M_1 and M_2 act as a differential pair with capacitive loads. In addition, voltages at node P and Q drop from V_{DD}, while producing a differential component proportional to $V_{DAC} - V_{CM}$. We call this mode 2. Mode 2 continues until the drop of voltage at P and Q node to approximately $V_{DD} - V_{TH3,4}$. At this time, the voltage is roughly equal to $2g_{m1,2}V_{TH3,4}/I_{tail}$, where $g_{m1,2}$ represents transconductance of M_1 and M_2. M_3 and M_4 turn on at the end of mode 2. This leads to drop of voltage at node outp and outn until the activation of M_5 and M_6. At this stage, one output (outp or outn) is pulled to V_{DD} by either M_5 or M_6, while the other output node drops to zero. M_3 and M_4 plays a key role of cutting the path from V_{DD} to ground after the comparator is done with the decision.

The use of precharge phase (mode 1) of the StrongArm comparator is twofold. First, it forces voltages at node P and Q to start from V_{DD}, which keeps M_1 or M_2 in saturation for some time, which enables these transistors to provide gain. Second, all 4 internal nodes are equalized after each comparison, regardless of in which state each node was before. This suppresses the dynamic offset by ensuring that the state in one clock cycle is not inherited by the other cycle.

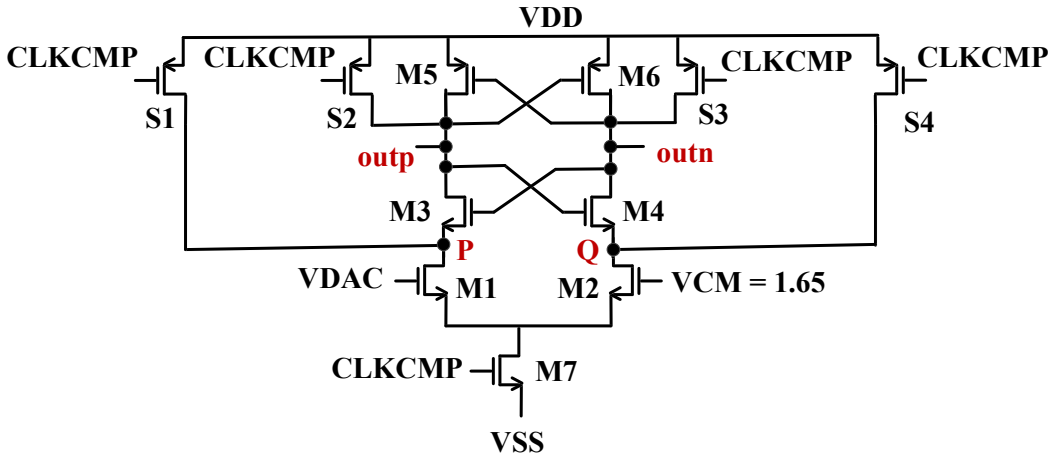


Figure 3. 16. StrongArm latched comparator circuit diagram.

Table 3. 3. Comparator target specifications

Sr. No.	Parameter	Min. Acceptable Target	Comments
1	Input offset	≤ 1/10 LSB ≤ 10 LSB	1. Not a major issue 2. Should be temperature-independent
2	Speed	Based on timing budget	
3	Power consumption	As low as possible	As low as possible for other target specifications
4	Sensitivity	< 1/4 LSB	Important
	Metastability	Important	Add metastability watchdog circuitry if needed
5	Kickback noise	< 1/4 LSB	1. Critical 2. If kickback noise occurs after the comparison decision, no issue; otherwise, use of a pre-amplifier.
6	Input-referred electronic noise	< 1/4 LSB	1. Critical 2. The use of a pre-amplifier if needed

3.7.1.3. Comparator Design (Calculation of Transistor Dimensions)

The design of comparator for the proposed ADC has been done by following a systematic method proposed in [235], keeping in view the targeted specifications. Table 3.3 shows the target specifications for the comparator circuit. The following method has been adopted to determine the circuit transistor dimensions.

We start design with the following target values of some parameters initially:

Input offset: < ½ LSB (≤ 3.9 mV= 4 mV)

Clock rate: $T_{CLK} = \frac{1}{f_{CLK}} = 2.4\ \mu s$; duty cycle = 50 %; $t_r = t_f = 100\ ps$

Power consumption: $P_{cons} \sim 10\ \mu W$

Tail current: $I_{tail} \sim 5\ \mu A$

Supply: $V_{DD} = 3.3\ V$

Temperature: $T = 27\ ^{\circ}C$

Technology: 350 nm CMOS

Corner for simulation: Typical

Next step is estimating the transistors dimensions.

Pairs in the signal path include M_1 and M_2; M_3 and M_4; M_5 and M_6. The dimensions of these transistors must be estimated first.

Let us start with the dimensions of the input differential-pair transistors (M_1 and M_2). We will select their dimensions keeping in view the input offset requirement.

From the literature,

$$\Delta V_{TH1,2} = \frac{A_{VTH}}{\sqrt{(WL)_{1,2}}} \tag{3.1}$$

where,

$\Delta V_{TH1,2} = \text{Threshold voltage mismatch of } M_{1,2}$

$A_{VTH} = \text{Technology} - \text{dependent parameter} = \sim 6 - 8\text{m V}\mu\text{m for 350 nm CMOS process.}$

Let,

$A_{VTH} = 7 \text{ mV } \mu\text{m}$

Let,

$$L_1 = L_2 = 0.6 \ \mu\text{m}$$

From our desired specifications,

$$\Delta V_{TH1,2} \leq 4 \text{ mV}$$

To be on a safe side from an offset contribution of the other transistors, let

$$\Delta V_{TH1,2} = 3.5 \text{ mV}$$

Putting values in (3.1), we get

$$W_1 = W_2 = 6.67 \ \mu\text{m} = 7 \ \mu\text{m}$$

Coming to the tail transistor (M_7). It must draw sufficient current and must operate in deep triode region when turned ON.

$$V_{GS7} = V_{DD}$$

$$V_{DS7} = V_{in,CM} - V_{GS1,2}$$

In our case,

$$V_{in,CM} = 1.65 \text{ V}$$

Let

$$V_{GS1,2} = 1.15 \text{ V}$$

$$V_{DS7} = 0.5\ V$$

Now we estimate its dimensions.

Let

$$L_7 = 0.6\ \mu m$$

We calculate W from the following equation for M7:

$$I_D = \mu_n C_{ox} \frac{W}{L}[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}]$$

We have,

$$I_D = 5\ \mu A$$

$$\mu_n C_{ox} = 170\ x\ 10^{-6}$$

$$V_{GS} - V_{TH} = 3.3 - 0.6 = 2.7\ V$$

$$V_{DS7} = 0.5\ V$$

So,

$$\frac{W}{L} = \frac{I_D}{\mu_n C_{ox}[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}]}$$

After evaluating, we get

$$\frac{W}{L} = 0.9 = 1$$

Since the offset introduced by the M_3 and M_4 pair is reduced because of the gain of M_1-M_2 pair, we select initially following values for their dimensions:

$$W_{3,4} = 7\ \mu m$$

$$L_{3,4} = 0.6\ \mu m$$

Also, the offset contribution from M_5-M_6 pair is even smaller, so

$$W_{5,6} = 2\ \mu m$$

$$L_{5,6} = 0.6\ \mu m$$

But we need to keep in mind that these transistors are critical for speed.

The reset switches (S1-S4) should pull their drains to M_1-V_{DD} within approximately 0.6 μs (1/4 of the clock period time). We expect that following values are OK for this:

$$W_{S1-4} = 1\ \mu m$$

$$L_{S1-4} = 0.6\ \mu m$$

$$L_{S1-4} = 0.6\ \mu m$$

The circuit was simulated with the calculated values and dimensions of a few transistors were slightly changed to either optimize the specifications or facilitate layout design. Table 3.4 displays the final dimensions of the comparator transistors.

Table 3. 4. Final Transistor dimensions for StrongArm Comparator circuit (all in µm)

Transistor	Calculated	Final based on Simulated Results
M_1, M_2	W = 7; L = 0.6	W = 8; L = 0.6
M_3, M_4	W = 7; L = 0.6	W = 8; L = 0.6
M_5, M_6	W = 2; L = 0.6	W = 4; L = 0.6
M_7		W = 1; L = 0.6
S_1-S_4	W = 1; L = 0.6	W = 1; L = 0.6

3.7.1.4. Simulation Results

Figures 3.17-3.24 and Table 3.5 show Monte Carlo simulation results of the offset voltage of the designed comparator with respect to Process-Voltage-Temperature (PVT) variations effect. As can be witnessed, the offset of the comparator is less than one LSB. In addition, it is temperature insensitive as desired.

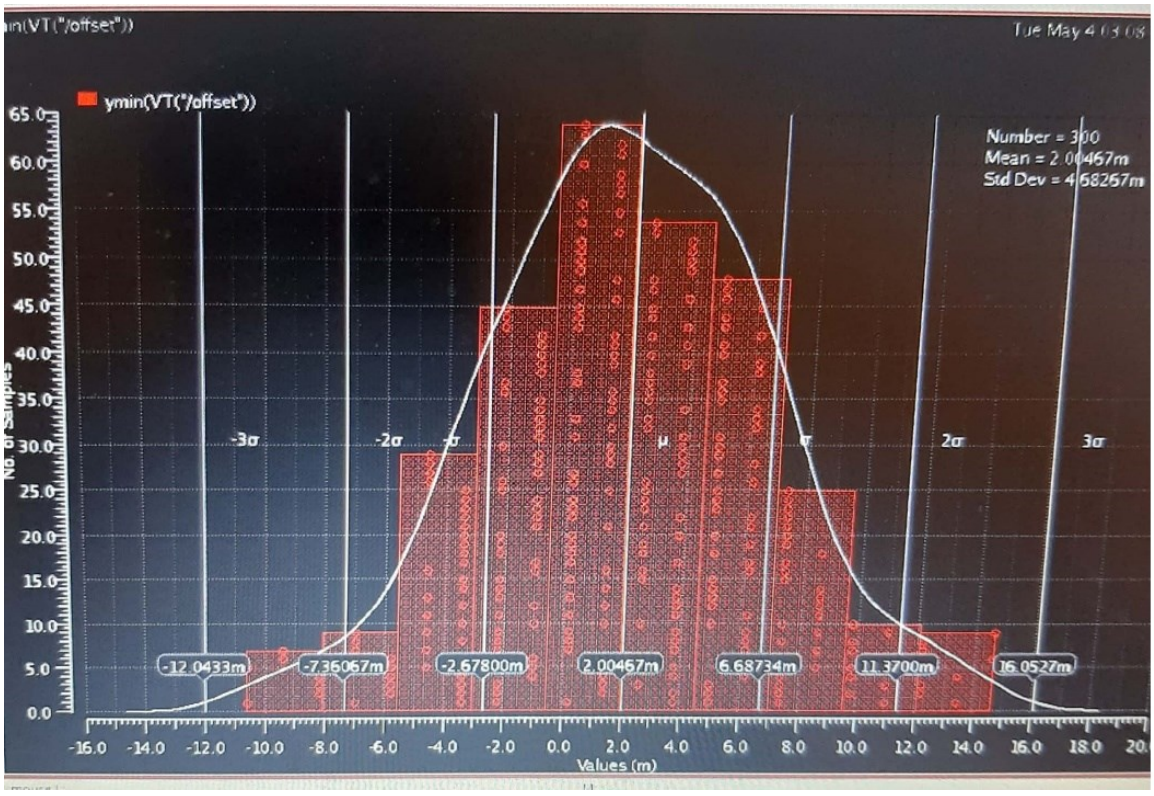


Figure 3. 17. Comparator offset voltage at $V_{DD} = 3\ V$, and T= 0 °C.

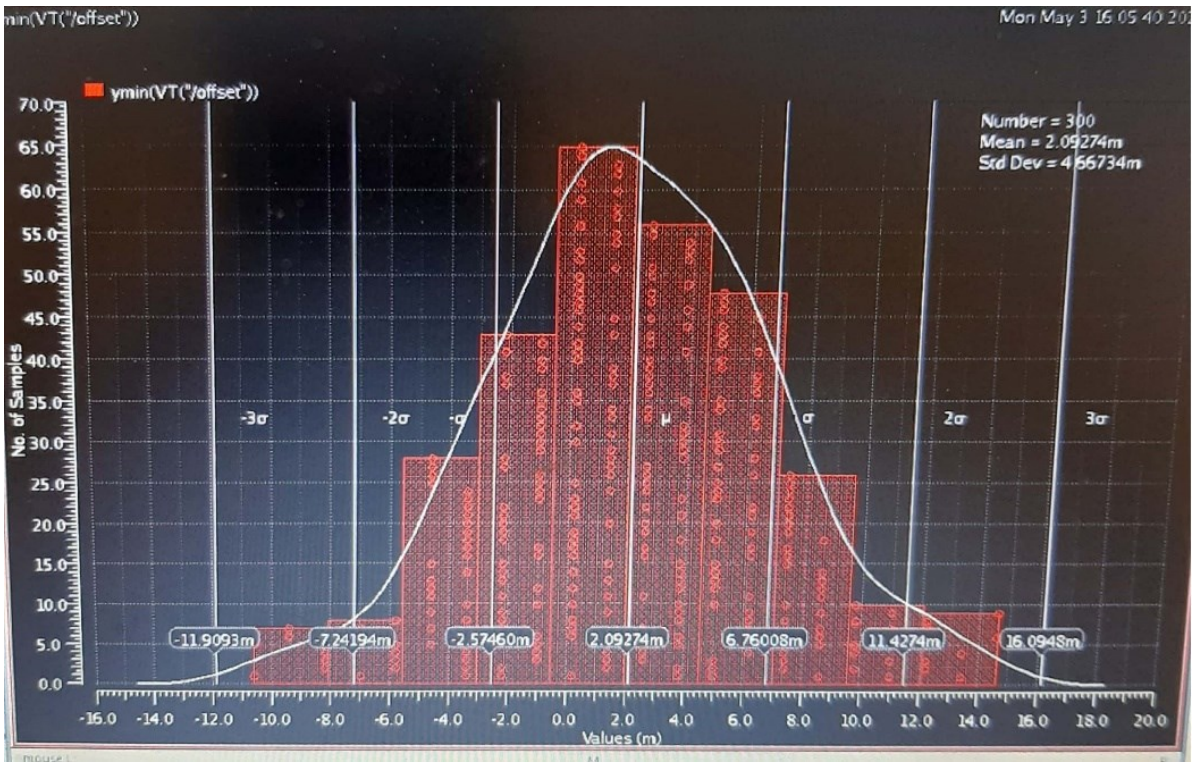


Figure 3. 18. Comparator offset voltage at $V_{DD} = 3\ V$, and T= 27 °C.

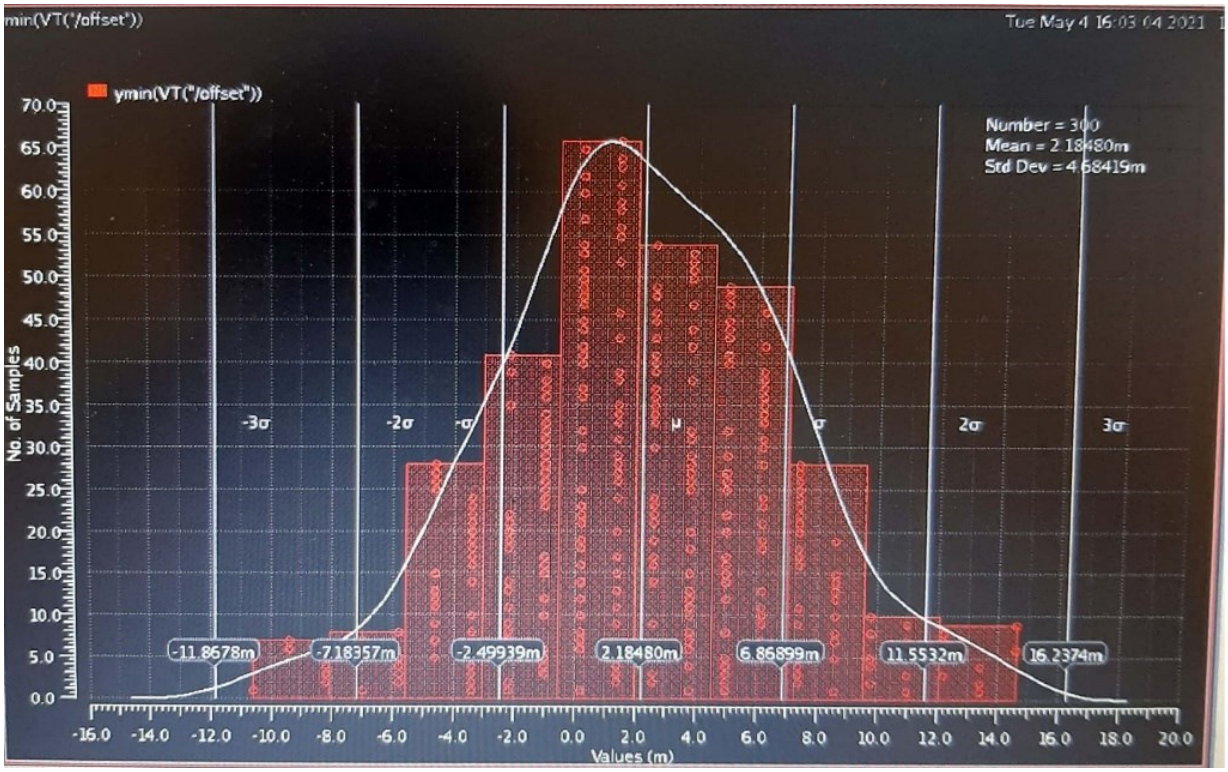


Figure 3. 19. Comparator offset voltage at $V_{DD} = 3\ V$, and T= 50 °C.

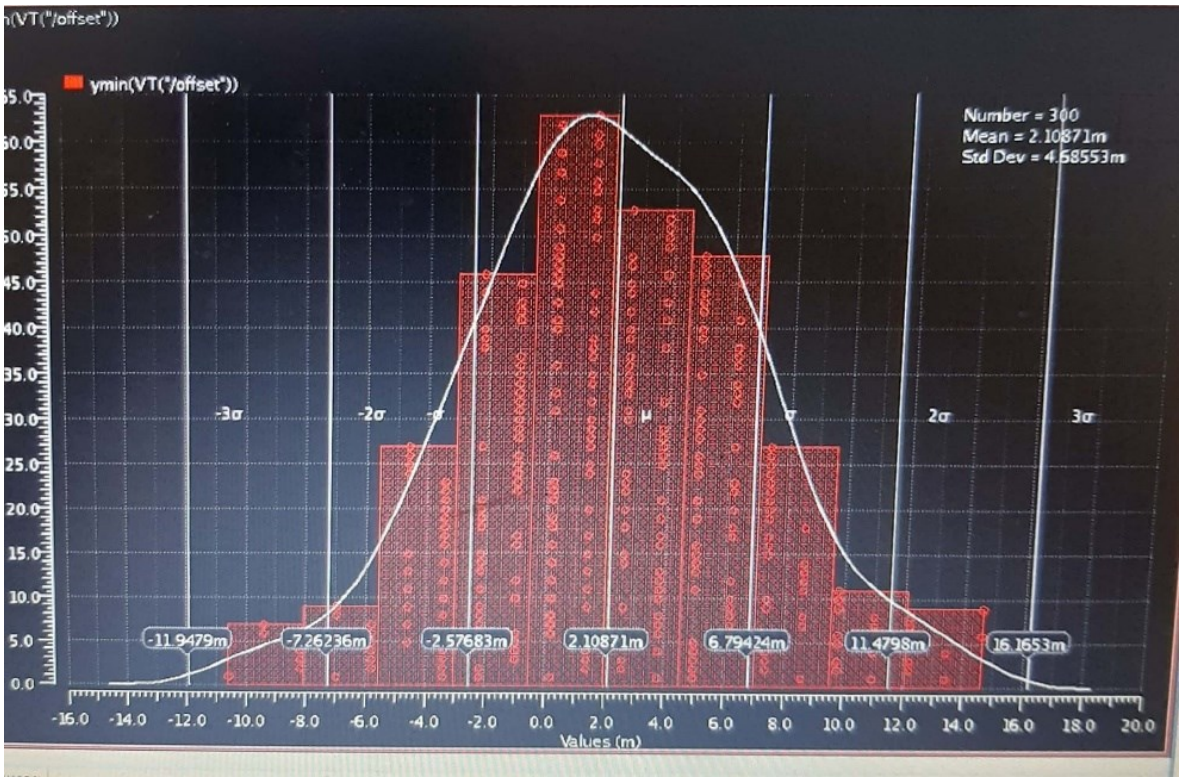


Figure 3. 20. Comparator offset voltage at $V_{DD} = 3.3\ V$, and T= 0 °C.

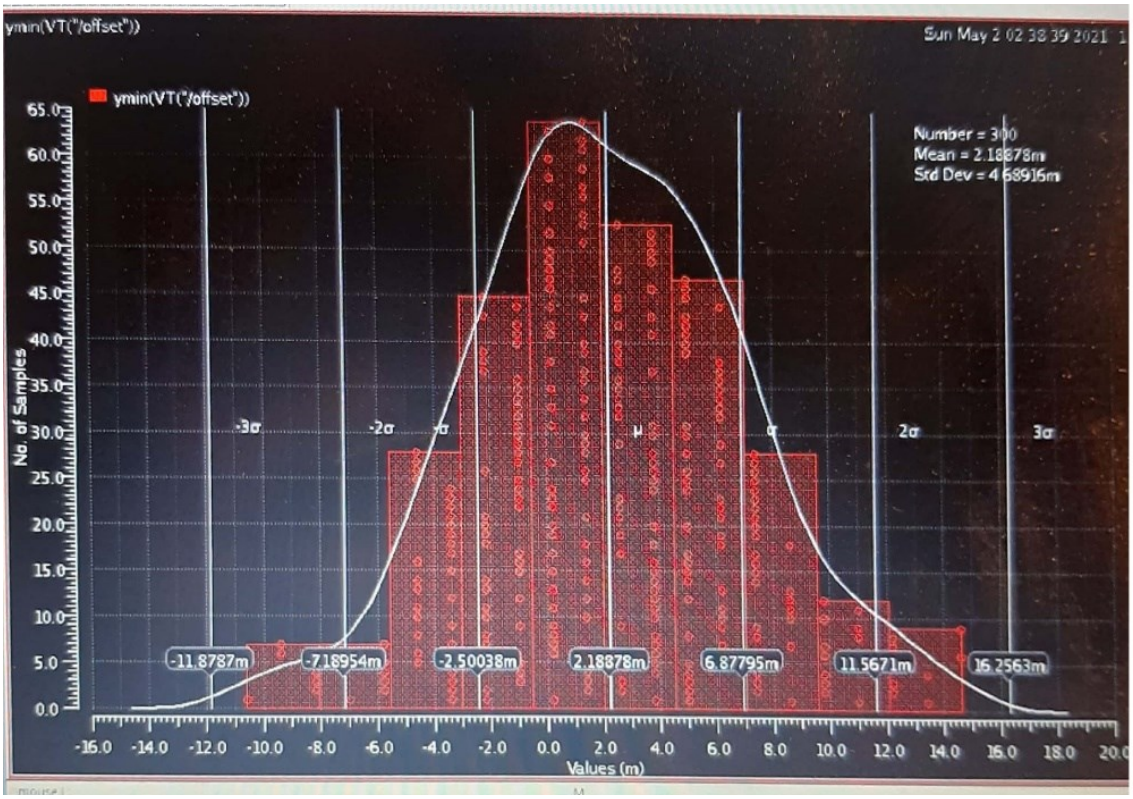


Figure 3. 21. Comparator offset voltage at $V_{DD} = 3.3\ V$, and T= 27 °C.

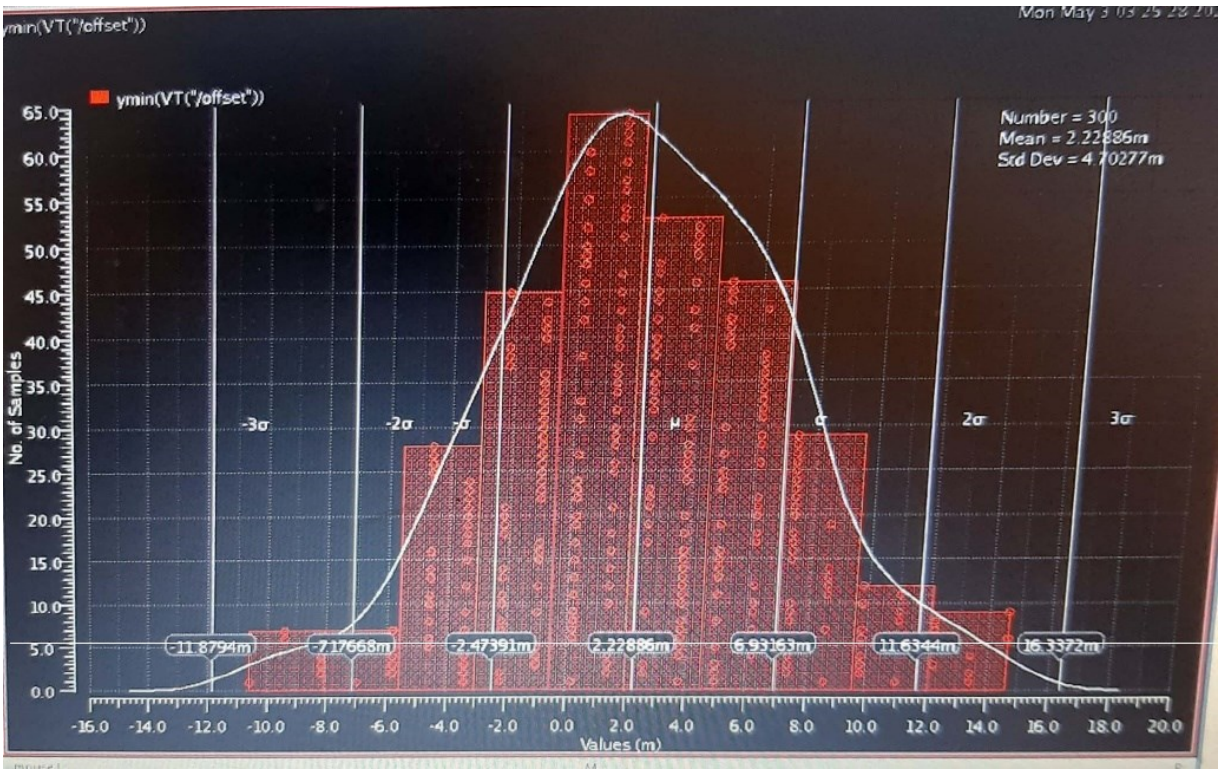


Figure 3. 22. Comparator offset voltage at $V_{DD} = 3.3\ V$, and T= 50 °C.

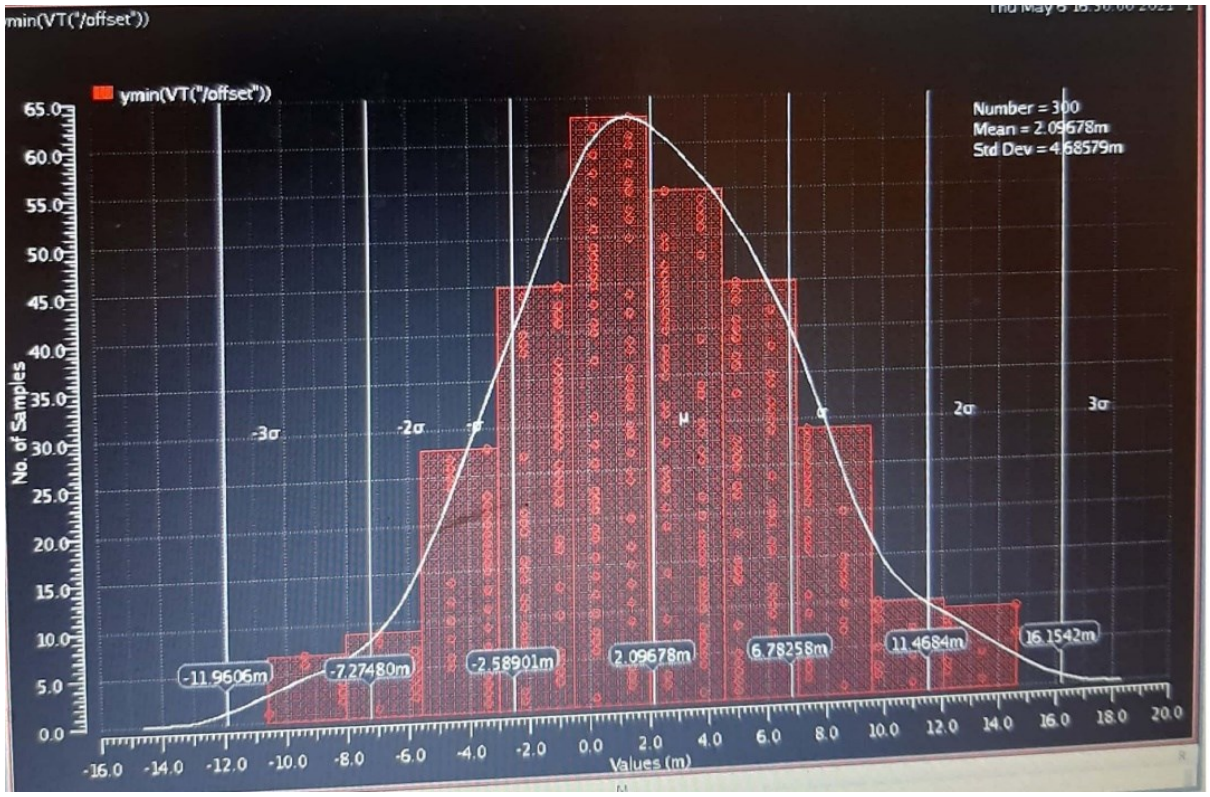


Figure 3. 23. Comparator offset voltage at $V_{DD} = 3.6\ V$, and T= 0 °C.

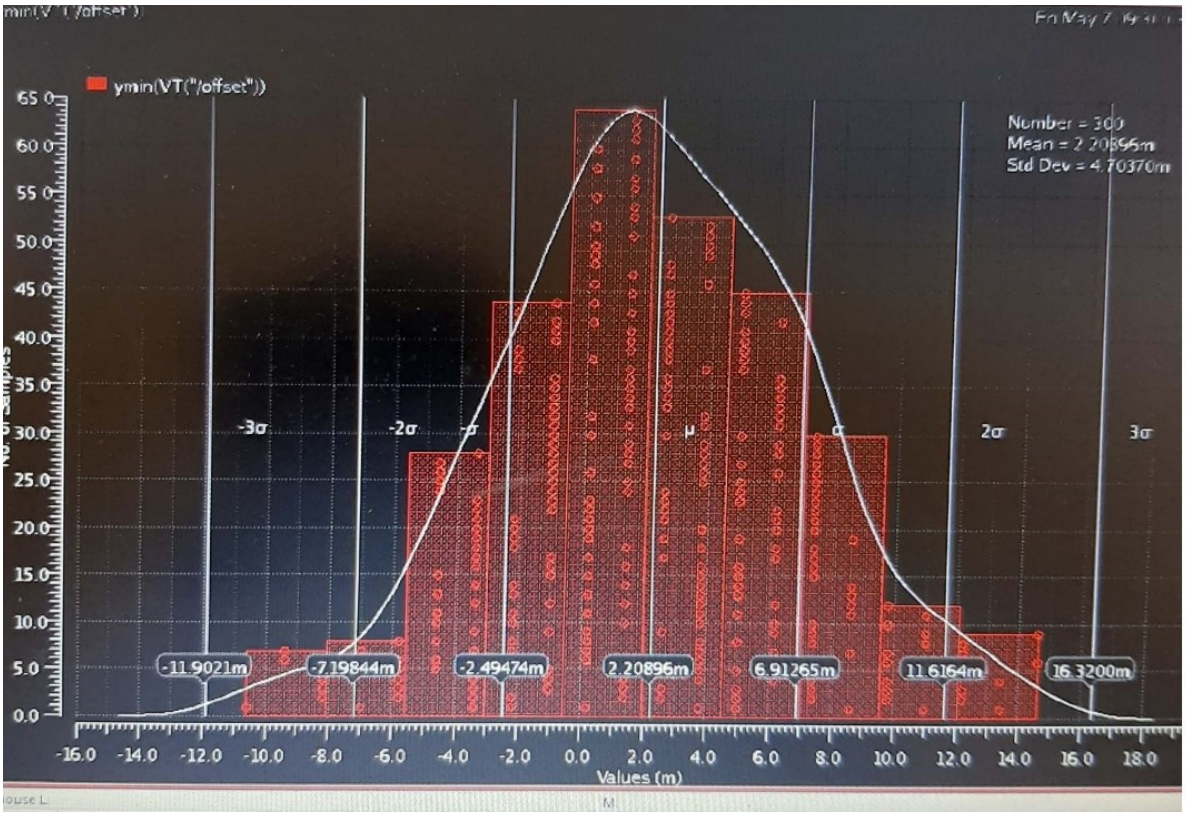


Figure 3. 24. Comparator offset voltage at $V_{DD} = 3.6\ V$, and T= 50 °C.

Table 3. 5. Comparator Offset voltage results with 300-points based Monte Carlo Simulation (Process variations + mismatch)

Sr. No	Temperature (°C)/ VDD (V)	3.0	3.3	3.6
1	0	Offset Data (in mV): Min = -10.6 Max = 14.6 Mean = 2.005 σ = 4.683	Offset Data (in mV): Min = -10.6 Max = 14.6 Mean = 2.109 σ = 4.686	Offset Data (in mV): Min = -10.6 Max = 14.6 Mean = 2.097 σ = 4.686
2	27	Offset Data (in mV): Min = -10.6 Max = 14.6 Mean = 2.093 σ = 4.667	Offset Data (in mV): Min = -10.4 Max = 14.6 Mean = 2.189 σ = 4.689	Offset Data (in mV): Min = -10.5 Max = 14.6 Mean = 1.327 σ = 4.657
3	50	Offset Data (in mV): Min = -10.6 Max = 14.6 Mean = 2.185 σ = 4.684	Offset Data (in mV): Min = -10.6 Max = 14.6 Mean = 2.229 σ = 4.703	Offset Data (in mV): Min = -10.6 Max = 14.6 Mean = 2.209 σ = 4.704

With the help of the simulations, it is verified that the location of the kickback noise of the comparator does not affect its decision. Therefore, it does not need a pre-amplifier. In addition, the comparator does not go metastable, which is verified by long (5000 clock cycles) transient noise-based simulations. It always produces a decision in transient noise simulations, which ensures that the ADC will not lose asynchronous clock (CLK_{int}) for the SAR logic because of the comparator's metastability. Therefore, no metastability

watchdog circuit is needed. Final achieved specifications of the designed comparator are enlisted in Table 3.6. As evidenced from Table 3.6, the power consumption of the comparator is lower with a rising edge only based clock (0.39 µW) than a symmetrical clock (0.5 µW), thus proving efficacy of the rising edge only delay-cell architecture of the ADC from power-efficiency point of view.

Table 3. 6. Comparator's final specifications

Sr. No.	Parameter	Value
1	Input offset	4.683 (< 1 LSB)
3	Power consumption	0.5 µW*; 0.39 µW**
4	Sensitivity	< 1/4 LSB
	Metastability	Does not occur in simulations
5	Kickback noise	Does not affect decision
6	Input-referred electronic noise	(93.5 µV***) < 1/4 LSB

* Assuming a symmetrical clock; ** with real rising edge only clock; *** worst case value (w_s corner value)

3.7.1.5. ADC Simulation Results with Real Comparator, SR-latch, and XOR gate

Verilog-A based comparator is replaced with real comparator in the Verilog-A based ADC and its PSD is plotted (Figure 3.25). For this simulation, the only real component is comparator, SR-latch, and XOR gate, and all other components are Verilog-A based. NAND-based SR-latch and XOR gate have been realized using standard cells. As can be seen from the PSD, the ADC exhibits desired performance (an ENOB of 7.88 bits, and SNDR of 49.2 dB) with the real comparator and SR-latch.

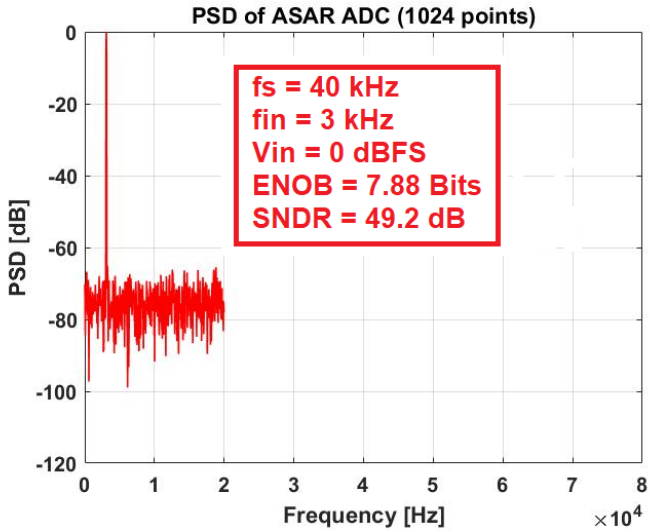


Figure 3. 25. ASAR ADC PSD plot with real comparator and SR-latch; all other components are Verilog-A based.

3.7.1.6. Layout of Comparator, SR-latch, and XOR gate

Figure 3.26 depicts the layout of the comparator circuit. Fingers have been used to reduce parasites. In addition, dummy devices have been added for the input differential pair (M_1 and M_2) to avoid issues because of different boundary conditions. Particular care has been devoted to avoiding any coupling between high switching clock (CLK_{CMP}) and other critical nodes. The layout of SR-latch and XOR gate is shown in Figure 3.27.

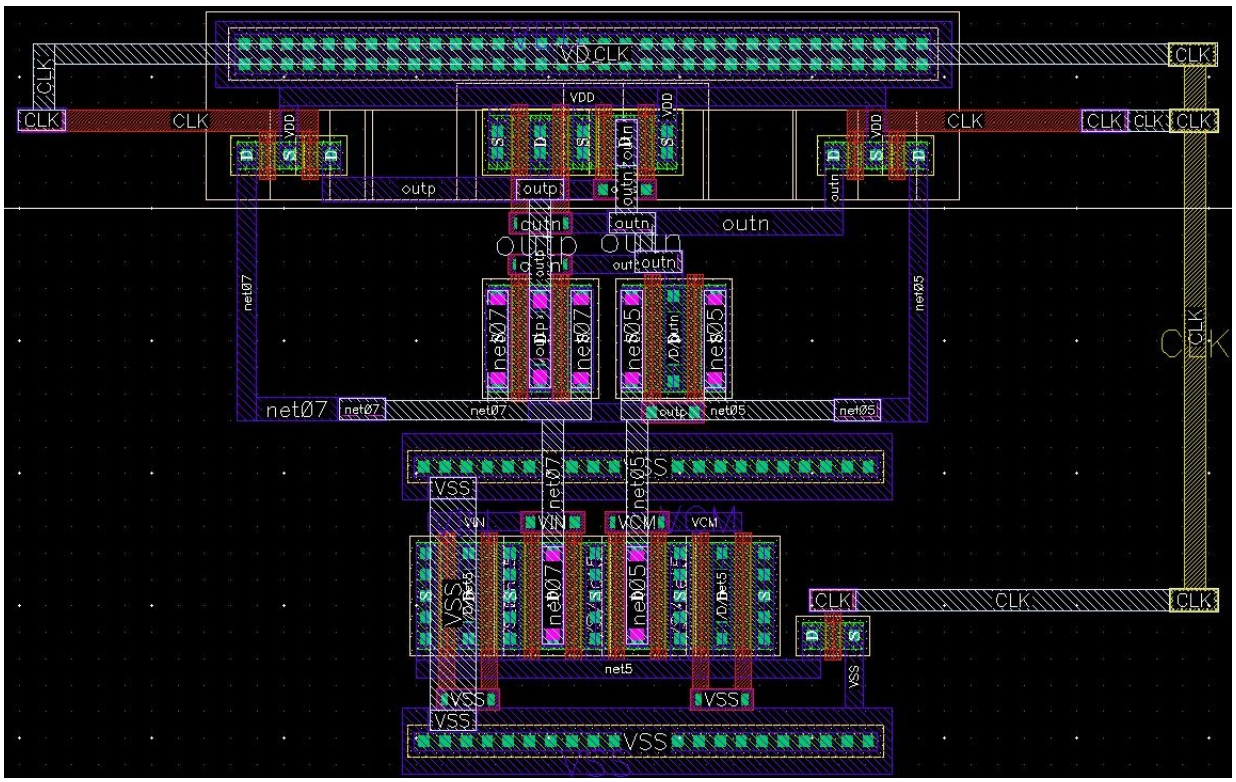


Figure 3. 26. Layout of StrongArm latched comparator.

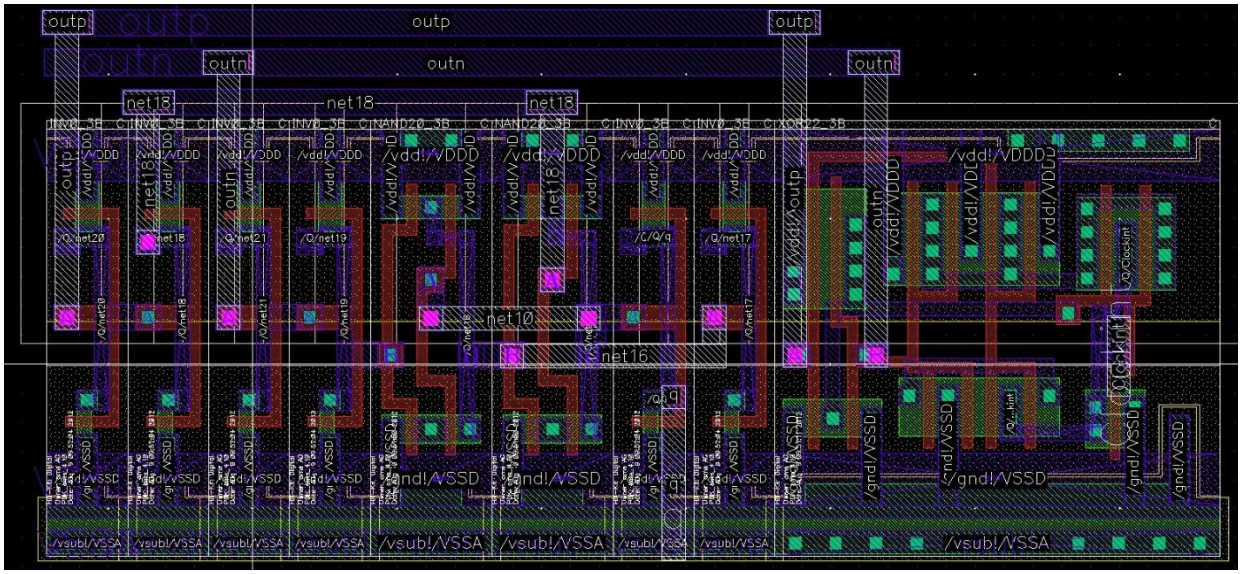


Figure 3. 27. Layout of cells after comparator, i.e., SR-latch and XOR gate.

3.7.2. CDAC Implementation

CDAC, being the active core, is the most critical component of an ASAR ADC from an accuracy point of view. This section describes the step-by-step process of CDAC implementation.

3.7.2.1. Binary-Weighted Vs Bridge/Split Capacitor Topology

The first step is the selection of the CDAC topology for the ADC. For the ASAR ADC, the two most common CDAC topologies include binary-weighted and bridge/segmented capacitor. Figures 3.28 and 3.29 show circuit diagram of both of these topologies. For this design, a fully binary-weighted CDAC topology has been chosen over bridge capacitor because of better linearity of former over latter. The CDAC parasitics capacitors can contribute significantly to the ASAR ADC performance degradation. This is especially applicable for a single-ended ASAR architecture. In comparison with fully binary-weighted CDAC topology, bridge capacitor topology is more susceptible to parasitics capacitances. It is because of the middle capacitor, which is bridged between two split CDAC arrays (LSB and MSB array), as shown in Figure 3.29. To implement this capacitor in the layout is extremely difficult. In addition, matching this bridge capacitor with the unit capacitor is another challenge which needs extra effort during layout design. This results in a mismatch between LSB and MSB capacitor array, leading to non-linearities. To cancel the effect of the CDAC parasitics and mismatches, some SAR ADC designs use CDAC calibration, trimming or mismatch error shaping techniques, which increase area, power, and complexity of the chip. As the target of this design is to avoid using any such calibration method to avoid complexity, the selection of binary-weighted topology becomes logical choice. Another reason for selecting fully binary-weighted CDAC is that the ADC under design is intended to be used as a core of a Noise-Shaping SAR ADC to enhance its SNDR. Selecting a parasitics-robust CDAC topology is, thus, can avoid any potential linearity issues at later stages of the design. Because of the selection of binary-weighted single-ended CDAC solution, a conventional CDAC switching scheme has been opted for the design, as explained in section 3.3.4.

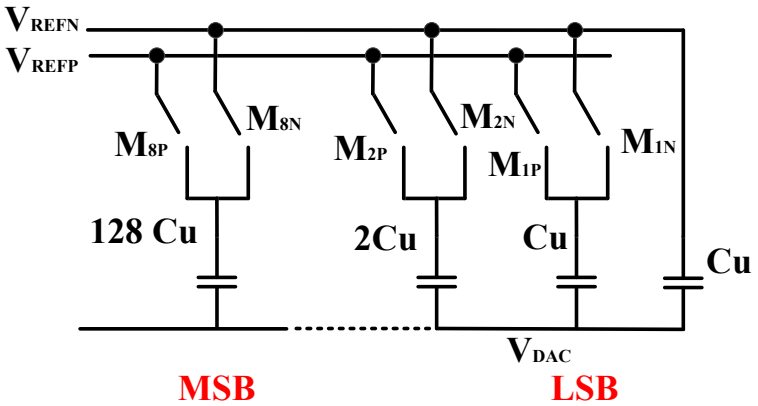


Figure 3. 28. An 8-bt binary-weighted CDAC topology with switches.

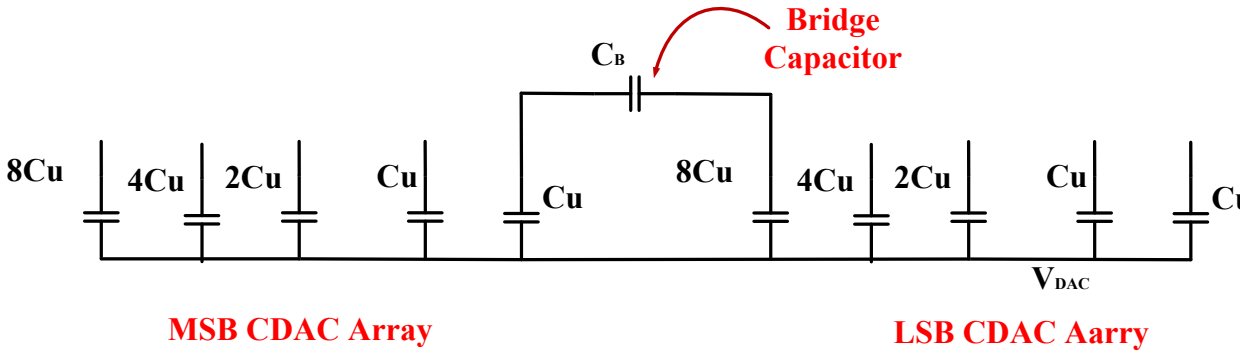


Figure 3. 29. An 8-bit bridge/segmented capacitor CDAC topology without switches.

3.7.2.2. Selection of CDAC Unit Capacitor

The starting point for the CDAC circuit design is determining the reliable value of a unit capacitor (C_U). As CDAC is the primary area-occupying block in ASAR ADC, the value of the unit capacitor should be as

minimum as possible. This is also needed to reduce power and enhance bandwidth. However, the minimum value of the unit capacitor is limited by two factors: the thermal ($^{kT}/_{C}$) noise and matching.

Thermal noise is caused by the switches controlling the CDAC, which form an RC low pass filter with the CADC capacitors. It is well known that the thermal noise in such switched capacitor circuits depends only on the value of the capacitance (C) and is given by:

$$\mathrm{v_{nrms}} = \sqrt{\frac{\mathrm{kT}}{\mathrm{C}}}$$

Where:

k = Boltzmann's constant with a value of $1.38\times10^{-23}\mathrm{J/K}$

T = Temperature in Kelvin

The total thermal noise contribution from the CDAC is given below:

$$\mathrm{v_{nrms}} = \mathrm{v^2_{nsampling}} + \mathrm{v^2_{nDAC}}$$

Where, the sampling noise ($v^2_{nsampling}$) depends on total CDAC capacitance as shown below:

$$\mathrm{v^2_{nsampling}} = \frac{\mathrm{kT}}{\mathrm{C_{DAC}}}$$

The second noise term (v^2_{nDAC}) is the CDAC contribution when the CDAC capacitors are floating, and the relevant capacitance is the parasitic to ground (C_{par}), given below:

$$\mathrm{v^2_{nDAC}} = \frac{\mathrm{kT}}{(1+\frac{\mathrm{C_{par}}}{\mathrm{C_{DAC}}})\mathrm{C_{par}}} = \frac{\mathrm{kT}}{\mathrm{C_{par}}}, \text{if } \mathrm{C_{DAC}} \gg \mathrm{C_{par}}$$

Out of these two noise contributions, the minimum sampling unit capacitance is limited by the thermal noise of the sampling CDAC array. Therefore, the requirement to select the minimum unit capacitance with respect to the thermal noise is:

$$\sqrt{\frac{\mathrm{kT}}{\mathrm{C_{DAC}}}} < 0.5\ \mathrm{V_{LSB}}$$

Matching of the capacitors is another decisive factor behind the unit capacitor selection. The output voltage generated by the CDAC is a result of capacitance ratio. A good capacitance matching is essential to get an accurate output voltage. Any mismatch, induced during fabrication, will lead to non-linearities in the CDAC, producing performance degradation. Therefore, a minimum reliable unit capacitor must satisfy the matching requirements.

For this design, the selection of the unit capacitance has been done keeping in view both the thermal noise and matching requirements. The minimum reliable unit capacitor value has been determined in two ways: first, it has been calculated by a systematic analysis method; second, Monte Carlo simulations have been used to verify the reliability of the selected unit capacitor.

[238] provides a method for determining a reliable unit capacitor value for a binary-weighted CDAC after a systematic analysis keeping in view matching and thermal noise requirements, assuming that a common-centroid layout of the CDAC is ensured. It is important that the calculations have been done keeping in

view the poly-poly capacitor from AMS 0.35 µm CMOS process, which is the technology node used for this ADC design.

According to this method, the minimum reliable unit capacitance for process matching can be calculated by following derived relationship:

$$C_{min,matching} = 0.86[\frac{0.45\% \times 3.5 \times \left[2^{N+2}\left(\sqrt{2^N}-1\right)+(\sqrt{2}-1)\sqrt{2^N}\right]}{(\sqrt{2}-1)2^N}]^2$$

For thermal noise point of view, the minimum reliable unit capacitance value can be determined as follows:

$$C_{min,thermalnoise} = \frac{4kT \times 2^{N+4}}{V_{FS}^2}$$

Both of the above-mentioned formulas have been calculated considering that the CDAC error sources because of both the factors are less than $0.5\ V_{LSB}$. Increasing the unit capacitance reduces the errors caused by both the sources, i.e., matching, and thermal noise. Assuming half of the error budget is assigned to each type, it can be written that:

$$C_{min} = \max\left[C_{min,matching}, C_{min,thermalnoise}\right]$$

Calculations of the unit capacitance for 8-bits CDAC for the ADC results in:

$$C_{min,matching} = 4.5\ \text{fF}$$

$$C_{min,thermalnoise} = 0.08\ \text{fF}$$

Thus, the minimum reliable unit capacitance turns out to be,

$$C_{min} = 4.5\ \text{fF}$$

However, this is the minimum unit capacitance value for a standalone CDAC. For the use of the CDAC in a ASAR ADC, this value should increase 3-4 times to be on a safe side. Therefore, a unit capacitance value of about 16 fF is the minimum reliable value for the CDAC of the ASAR ADC. To make it more reliable, a value of 20 fF has been chosen for this design since increasing the capacitor value improves matching. This results in a total CDAC capacitance of 5.12 pF.

To verify the robustness of selected unit capacitance, Monte Carlo CDAC capacitors mismatch simulations have been used for the following worst-case matching condition for the CDAC:

$$\sqrt{\sigma_{code10000000}^2 + \sigma_{code01111111}^2} < \frac{1}{4}V_{LSB}$$

where,

$\sigma_{code10000000}^2$=Standard deviation CDAC output voltage against code 10000000

$\sigma_{code01111111}^2$=Standard deviation CDAC output voltage against code 01111111

Table 3.7 shows Monte Carlo simulation results for different unit capacitor values. Both analytical as well as simulation results demonstrate that the minimum unit capacitor value has been dictated by the matching requirement for this design. Poly-poly capacitor of AMS 0.35 µm CMOS process has been selected. These capacitors have typical capacitive density of 0.86 fF/μm^2. In addition, they show good matching properties. Moreover, they are low-cost since no additional mask or process step is needed for their fabrication.

Table 3. 7. Summary of CDAC unit capacitance results: Monte Carlo Mismatch simulation results for worst-case CDAC condition and thermal noise calculation

C_u (fF)	$\sqrt{\sigma^2_{1code10000000} + \sigma^2_{1code01111111}}$ (mV)	kT/C noise (nV^2)	Less than ¼ LSB? (1 LSB = 7.8 mV)
30	0.049661	0.530906	Yes
20	0.078372	0.80859	Yes
10	0.096038	1.6172	Yes
5	0.1403	3.2344	Yes

3.7.2.3. CDAC Switches Implementation

For the bottom plate of each capacitor of CDAC array, three switches are needed: One for the input signal (V_{IN}), one for the upper voltage refence (V_{REFP}), and one for the lower voltage refence (V_{REFN}). In addition, one switch is enough to connect the top plate of all the capacitor to the common mode voltage (V_{CM}). Simple NMOS and PMOS switches have been chosen for V_{REFN} and V_{REFP}, respectively. Because of linearity requirements and to accommodate a full-scale input signal for the bottom-plate sampling, CMOS transmission gate switches have been selected for V_{IN} and V_{CM}. Figure 3.30 shows configuration of switches for one capacitor of the CDAC.

The sizing of all the sampling switches has been done keeping in view the settling requirements of the input voltage, i.e., less than 0.5 LSB. As the transmission gate switch with CDAC capacitor forms a lowpass filter, whose cut-off frequency is given below:

$$f_{3dB} \geq \frac{(N+1)\ln 2}{\pi} f_s$$

For a typical sampling-frequency (40 kHz),

$$f_{3dB} = 80 \text{ kHz}$$

For maximum sampling-frequency (167 kHz) supported by the ADC,

$$f_{3dB} = 332 \text{ kHz}$$

The on-resistance of the switch can be calculated by following expression,

$$R_{ON} = \frac{1}{\mu C_{ox} \frac{W}{L}(V_{GS} - V_{TH})}$$

Which leads to switch resistance of less than 2.43 MΩ for typical sampling-frequency case and 0.588 MΩ for the maximum sampling-frequency. To facilitate maximum sampling frequency, switches have been designed according to the maximum sampling-frequency criteria. In addition, the sizing of the switches has been optimized with respect to charge injection and clock feedthrough impacts. To minimize these effects, switches with minimum sufficient sizes have been designed.

Sizing of simple PMOS and NMOS switches have been done keeping in view the sufficient settling time for charging and discharging of the CDAC capacitors. As the input to these switches is coming from the on-chip voltage reference buffers, a careful consideration of the input-dependent offset has been made. To balance the input-dependent offset for all the capacitors of CDAC, the switch sizing has been done in a binary weighted way, i.e., the width of the switch connected with LSB capacitor is selected as 1 µm, while the width for MSB capacitor is chosen as 128 µm. Efficacy of this size selection was verified by the simulation. Table 3.8 shows the CDAC switches sizes.

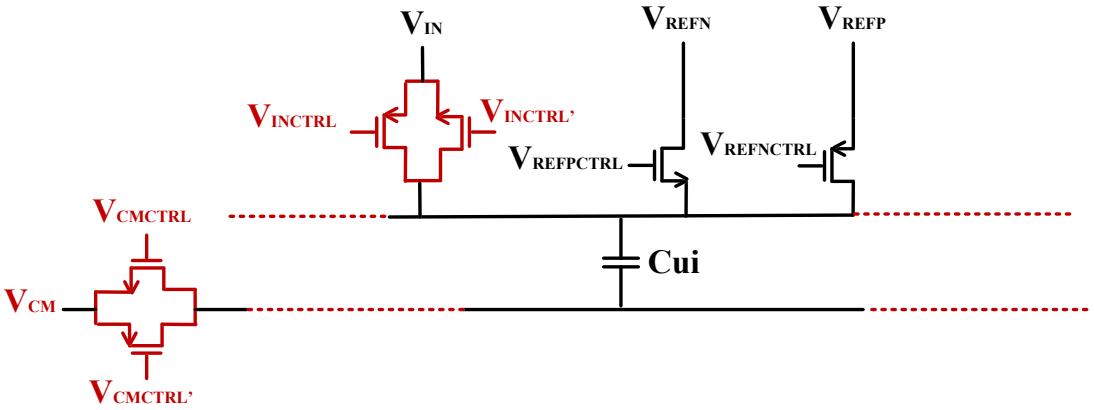


Figure 3. 30. Switches configuration of an i-th capacitor of the CDAC.

Table 3. 8. CDAC switch sizes (L = 0.35 µm for all switches; W = 4 µm for V_{CM} switch)

Switch\Width (µm)	V_{IN}	V_{REFP}	V_{REFN}
Dummy	1	-	1
LSB	1	1	1
MSB-6	1	2	2
MSB-5	2	4	2
MSB-4	2	8	8
MSB-3	4	16	16
MSB-2	4	32	32
MSB-1	8	64	64
MSB	8	128	128

3.7.2.4. ADC Simulation Results with Real CDAC and Switches

In Verilog-A based ADC, the ideal CDAC and switches are replaced with the real CDAC and switches. Besides CDAC and switches, comparator and SR-latch are also real for this simulation. All other components are still Verilog-A based. The aim is to verify the ADC performance with the real CDAC and switches and optimize its performance if needed. Figure 3.31 depicts the PSD of the ADC, which verifies a fully satisfactory performance (ENOB and SNDR) of the ADC with real CDAC and switches.

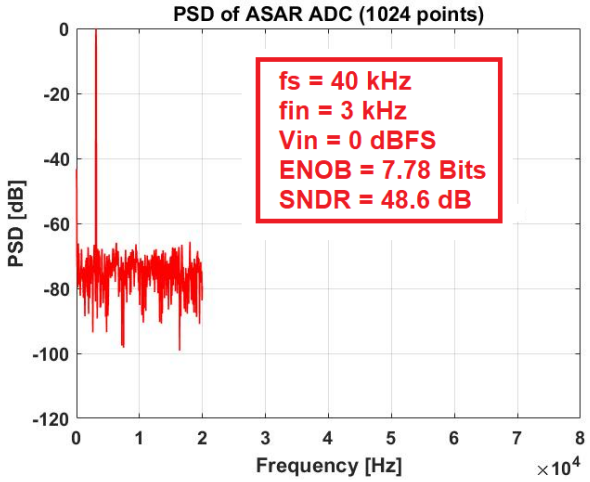


Figure 3. 31. ASAR ADC PSD plot with real comparator, SR-latch, CDAC and switches; all other components are Verilog-A based.

3.7.2.4. Layout of CDAC and Switches

CDAC is the most critical block from layout point of view, since its parasitics can kill the ADC performance. A common-centroid layout, shown in Figure 3.32 (a), has been opted for the CDAC layout design. As the voltage reference switches are also binary-weighted, the unit-cell of a CDAC capacitor also includes one V_{REFP} switch and one V_{REFP} switch. This way, the matching has been ensured for the switches too. Figure 3.32 (b) displays layout of a unit-cell of the CDAC and reference switches. The CDAC node of the unit-cell has been extensively shielded to protect it from undesired effects of parasitics. The critical capacitances of the CDAC node were identified by performing an analysis of the post-layout netlist of the CDAC. After identifying the critical parasitics capacitances, equal values capacitances were back annotated in the CDAC schematic, and simulations were performed to see their impact on the ADC performance. This way, all the critical parasitics were mitigated using shielding. The layout of the complete CDAC with all the switches is shown in Figure 3.33.

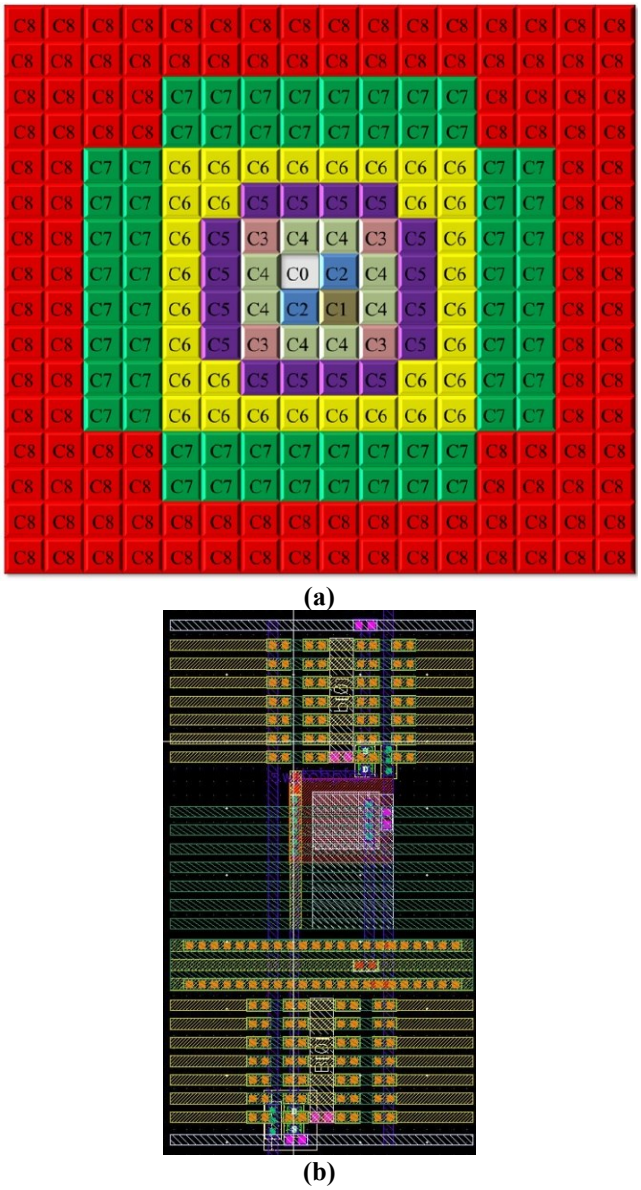


Figure 3. 32. (a) Common-centroid arrangement adopted for the CDAC and voltage references switches layout [239], (b) unit-cell layout of CDAC with voltage references switches; the CDAC node in the unit-cell has been shielded to mitigate critical parasitic capacitances impacts on ADC performance.

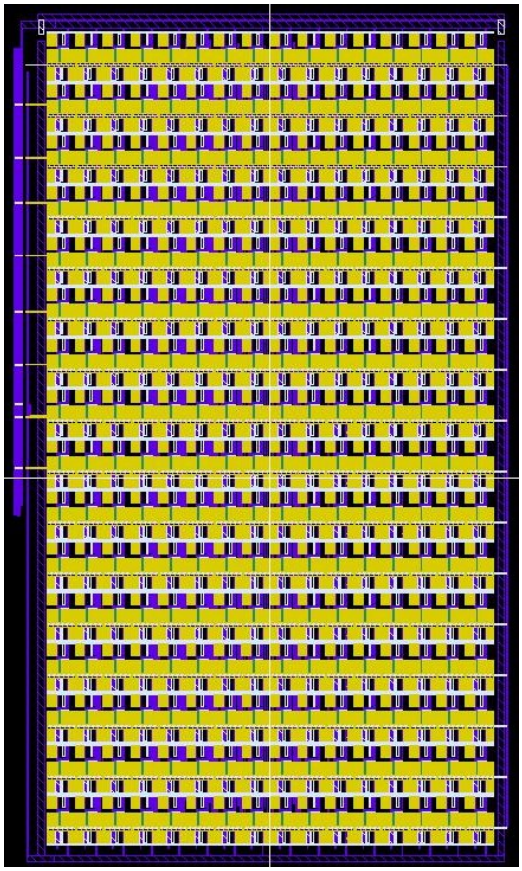


Figure 3. 33. Layout of the CDAC with all the switches.

3.7.3. Implementation of Asynchronous SAR Logic with Auxiliary Components

The SAR logic is used to generate control signals for the CDAC switches to ensure SAR algorithm. Figure 3.34 shows schematic diagram of the used asynchronous SAR logic with auxiliary components. ASAR logic consists of shift-register based architecture. The working of SAR logic can be described with the ADC timing waveforms shown in Figure 3.35. The SAR ADC is triggered by external 'CLKSampling' signal, which has a typical conversion time of 25 µs (40 kHz sampling-rate). During the sampling phase, all the signals of SAR logic are low (logic 0) except the B7/MSB. At the start of the conversion phase, the SAR logic forces the MSB_SET signal to go high to set the MSB bit before the comparator can make its first decision. In addition, it enables the NOR signal to go high, which is delayed by a rising edge only delay-cell to enable CDAC to get settled, thus generating comparator clock signal CLK_{CMP}. At the same time, the CLKSampling signal sets the first DFF of the upper side of the SAR logic so that it can transfer its input to the output at the coming rising edge of the CLK_{int} signal. Once the comparator is done with its first decision, its decision is stored in SR-latch, whose output is connected with the DFFs of the lower side of the SAR logic. In addition, the CLK_{int} goes high, which resets the B7 signal with the help of Q' of the first DFF of the upper side of the SAR logic. With the logic high of the CLK_{int} signal, Q' of the second DFF of the upper side of the SAR logic sets the B6 signal. With the rising edge of the B6 signal, the decision of B7/MSB is updated based on comparator' decision. With the update of B7 and B6, MSB and MSB-1 switches of the CDAC are connected to the relevant reference voltages (V_{REFP} or V_{REFN}) depending on B7 and B6 status. The CDAC starts its settling for the next decision (B6) by the comparator. With the rising edge of the CLK_{int} signal, the NOR signal goes low, followed by the CLK_{CMP} signal because of the rising edge only delay effect, forcing the comparator to enter in latched/reset phase. Lowering of the NOR signal forces the CLK_{int} signal to go low. The NOR signal goes high with the falling edge of the CLK_{int} signal, which is again delayed by the delay-cell to provide CDAC adequate time for settling before comparator can perform

next decision. After the CDAC settling, comparator makes the decision after rising edge of the CLK_{CMP} signal, which is stored in SR-latch. The CLK_{int} goes high with the rising edge of the CLK_{CMP} signal, thus triggering the relevant DFFs in SAR logic to set B5 as well as update B6 based on comparator decision. The same procedure continues until conversion of all 8 bits. The EoC signal forces the conversion to an end and the output data is available at the rising edge of the dataavailable signal.

To implement SAR logic, standard cells based DFFs have been used, which are based on CMOS transmission gate technology. Compared to NAND-based DFFs, the use of transmission gate DFFs saves area of SAR logic. All the auxiliary cells have also been realized using standard cells.

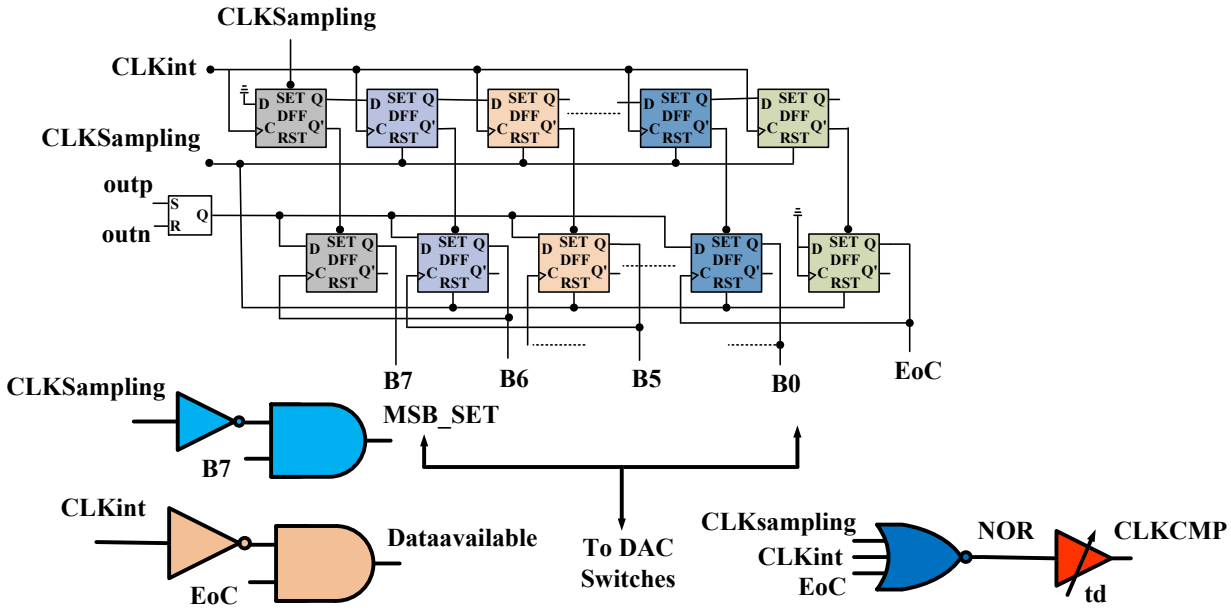


Figure 3. 34. SAR logic with the auxiliary cells and variable delay-cell

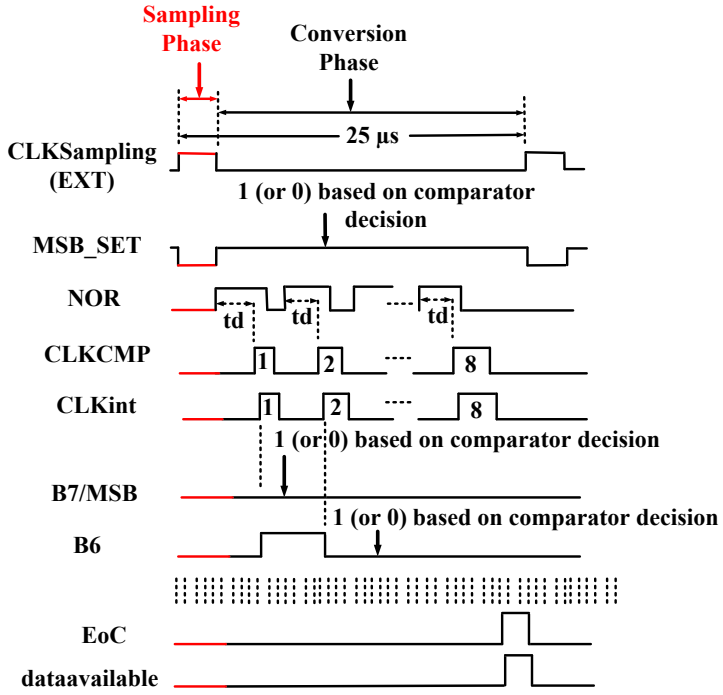


Figure 3. 35. Timing waveforms of ASAR ADC with SAR logic working.

3.7.3.1. ADC Simulation Results with Real SAR Logic and Auxiliary Cells

In Verilog-A based ADC, the ideal SAR logic and auxiliary cells were replaced with the real ones. Besides SAR logic, CDAC, switches, comparator and SR-latch are also real. All other components are still Verilog-A based for this simulation. The aim is to verify the ADC performance with the real SAR logic and optimize its performance if needed. Figure 3.36 shows the PSD of the ADC, which shows a fully satisfactory performance (ENOB and SNDR) of the ADC with real SAR logic and auxiliary cells.

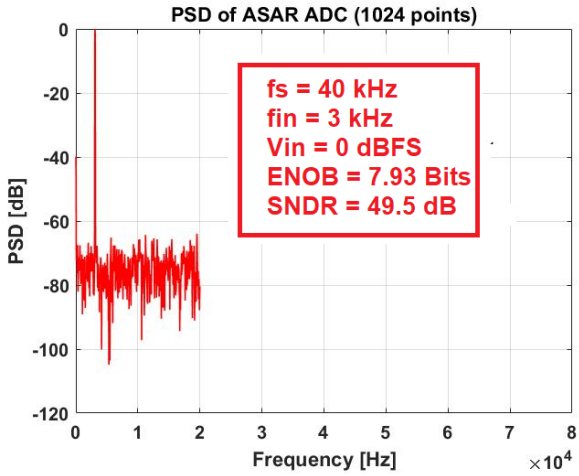


Figure 3. 36. ASAR ADC PSD plot with real SAR logic and auxiliary cells, comparator, SR-latch, CDAC and switches; all other components are Verilog-A based.

3.7.3.2. Layout of SAR Logic and Auxiliary Cells

Figure 3.37 depicts the layout of the SAR logic and auxiliary cells. Care has been taken to place the cells in such a way that the delays to different cells are not changed out of proportionally. This is especially valid for the DFFs of SAR logic which are placed at the end of the row, i.e., the ones which decide the LSB-1 and LSB bits. Delay introduced by the layout parasitics can lead to timing violations and thus performance degradation.

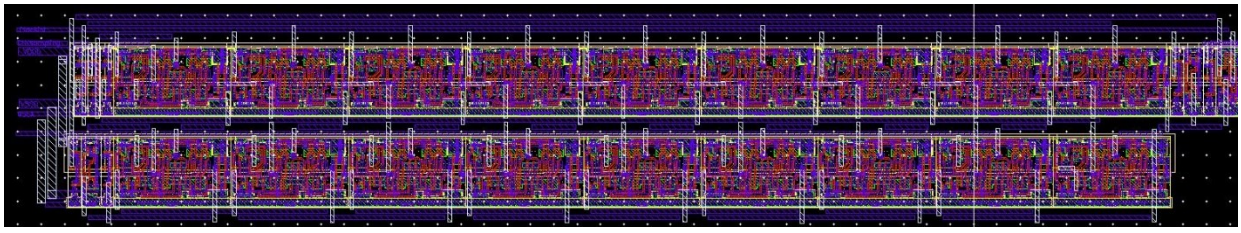


Figure 3. 37. Layout of SAR Logic with auxiliary cells.

3.7.4. Variable Rising Edge Only Delay-Cell Implementation

As described earlier, it is essential to provide CDAC with sufficient time for its settling. If this time is inadequate, the CDAC capacitors will not be fully charged when comparator makes the decision. This leads to an incorrect decision by the comparator, and thus an incorrect conversion of the bit. To ensure sufficient settling time for the CDAC, delay needs to be introduced to the internally generated NOR signal, which could act as an asynchronous clock for comparator. A delay-cell, therefore, is needed to achieve this.

For the proposed ADC architecture, a rising edge only delay-cell is suitable, as described in section 3.4. Figure 3.38 displays circuit diagram of the core of the proposed rising edge only delay-cell. The core components of the delay-cell include a comparator with a NAND-based SR-latch, a current source, a capacitor, a switch, and a digital controlled logic for the switch. The input to the delay-cell is NOR and its output is CLK_{CMP}. The operation of the delay-cell is based on the charging and discharging of the capacitor

using a current source (I) by turning ON and OFF the switch with a digital logic. The amount of delay achieved is given by:

$$t_d = \frac{C}{I}$$

The comparator uses 1.65 V as its threshold voltage. The selection of 1.65 V as its threshold voltage avoids the use of a dedicated pad since 1.65 V is already part of the design being common mode voltage. The comparator switches its output when the input voltage on its negative terminal increases or decreases its threshold voltage as a result of the capacitor charging and discharging. The charging and discharging of the capacitor depend on the ON and OFF state of the switch, which is controlled by the digital control logic. The digital logic ensures capacitor charging during only the rising edge of the input clock signal, up to a time decided by $t_d = \frac{C}{I}$. The same digital logic guarantees a quick capacitor discharge at the falling edge of the input clock signal, resulting in no delay to the falling edge of the input clock ideally. To help achieve rising edge only delay, a NAND based SR-latch has been used, whose S input is connected to the comparator output and R input is connected to NOR signal.

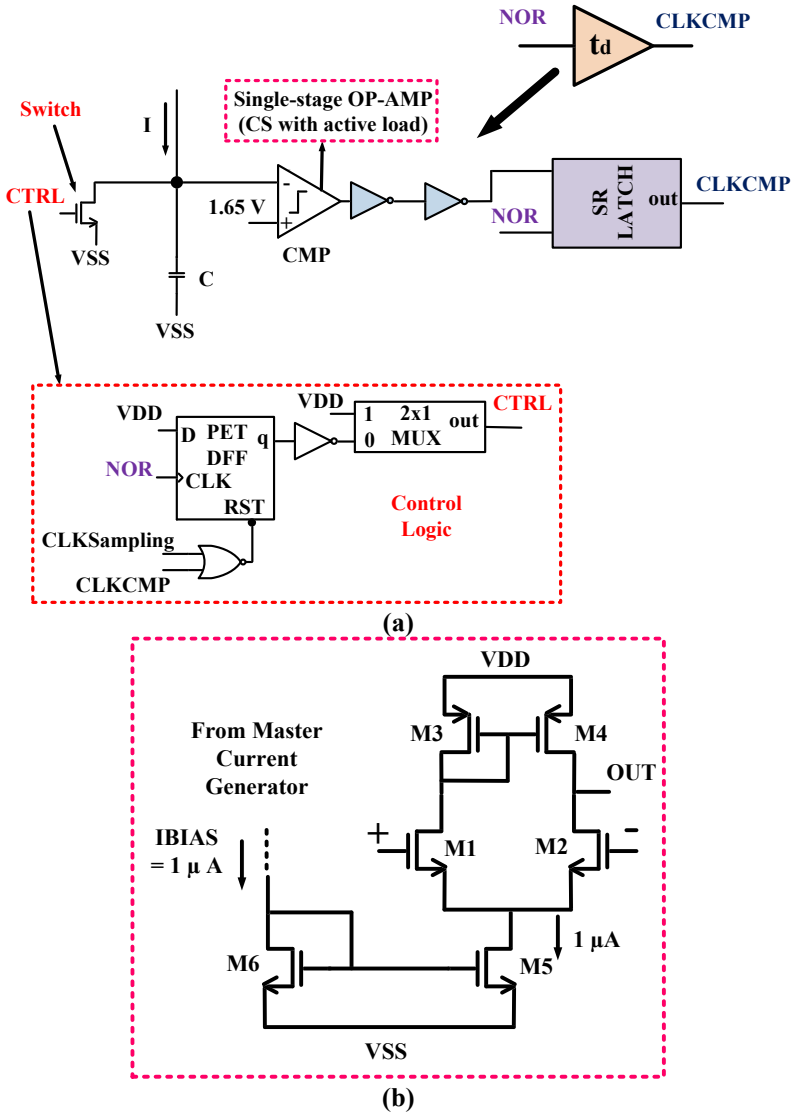


Figure 3. 38. Schematic of (a) the proposed rising edge only variable delay-cell; (b) comparator used in the delay-cell.

3.7.4.1. Operation of the Delay-Cell

The operation of the delay-cell can be described as follows. At the arrival of the rising edge of the input signal NOR, the 'CTRL' signal generated by the control logic turns ON the analog switch. As a result, the current (I) starts capacitor (C) charging and the voltage at the negative terminal of the comparator starts rising from 0 V. The comparator switches its output after making its decision when the voltage on its negative terminal exceeds the threshold voltage (1.65 V). The output of the comparator goes to S input of SR-latch after a couple of inverters. R input of the SR-latch is connected to the input signal NOR. Right after the comparator decision, the 'CTRL' forces the switch to turn off. This starts a quick capacitor discharge and the voltage at the negative terminal of the comparator starts decreasing from the previous value. The comparator changes its state once again when the voltage at its negative terminal drops below 1.65 V. NAND-based SR-latch ensures signal transfer to the output based on its inputs S and R.

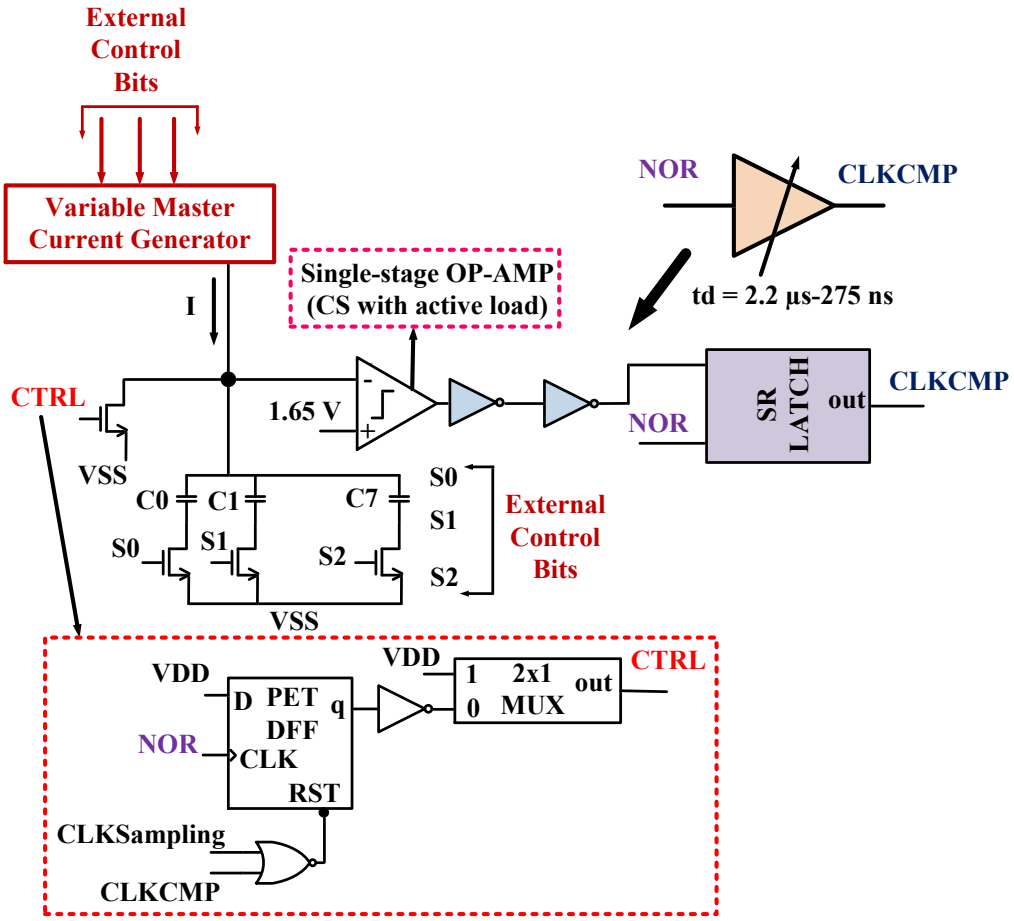


Figure 3. 39. Schematic of the proposed rising edge only delay-cell with variability functionality.

3.7.4.2. Variability in the Delay-Cell

Because of the need of 8 different delay values to facilitate sampling-rate reconfigurability functionality of the ADC as described in section 3.4.1, variability in the delay-cell needs to be introduced. Variability in the delay-cell also makes it robust with respect to PVT variations. As the delay amount depends on $t_d = \frac{C}{I}$, there are three choices to make the delay tunable: first, by tuning the capacitor; second, by tuning the current; and third, by tuning both the capacitor and current. For this design, delay-cell has been made variable by tuning both the capacitance and current. Figure 3.39 shows the complete circuit diagram of the

variable delay-cell. Three capacitors with an external control are added to tune the delay-cell with respect to capacitance. In addition, 8 different current values with an external control have been used to tune the delay-cell. The variability of delay-cell by tuning capacitance as well as current makes it flexible as well as PVT-robust in comparison with a delay-cell tuned only by the capacitance or current. In addition, it makes the delay-cell controllable against layout parasitics. Table 3.9 shows the 8 delay values achieved by the delay-cell.

Table 3. 9. Delay values achieved from the variable delay-cell

Sr. No.	t_d	f_s (kHz)	Comments
1	2.2 µs	40	Maximum delay for typical sampling-rate
2	1.1 µs	71.43	
3	733 ns	100	
4	550 ns	119	
5	440 ns	131.58	
6	367 ns	142.86	
7	314 ns	153.85	
8	275 ns	167	Minimum delay for maximum sampling-rate

3.7.4.3. Simulation Results of the Delay-Cell

Figure 3.40 shows the Monte Carlo results of delay variations of the delay-cell with respect to mismatches for a typical delay value of 1.37 µs. Table 3.10 summarizes the delay value variation with respect to PVT variations based on process and mismatches Monte Carlo simulations. This verifies that the delay value is insensitive to temperature change – a desired characteristic for the application. In addition, the variation of the maximum and minimum delay values with respect to different corners is listed in Table 3.11 and 3.12, respectively. These results verify that the variations in the delay amount is within ± 30 %. To cater for this variation in the delay value is another reason behind making the delay cell variable with an external control.

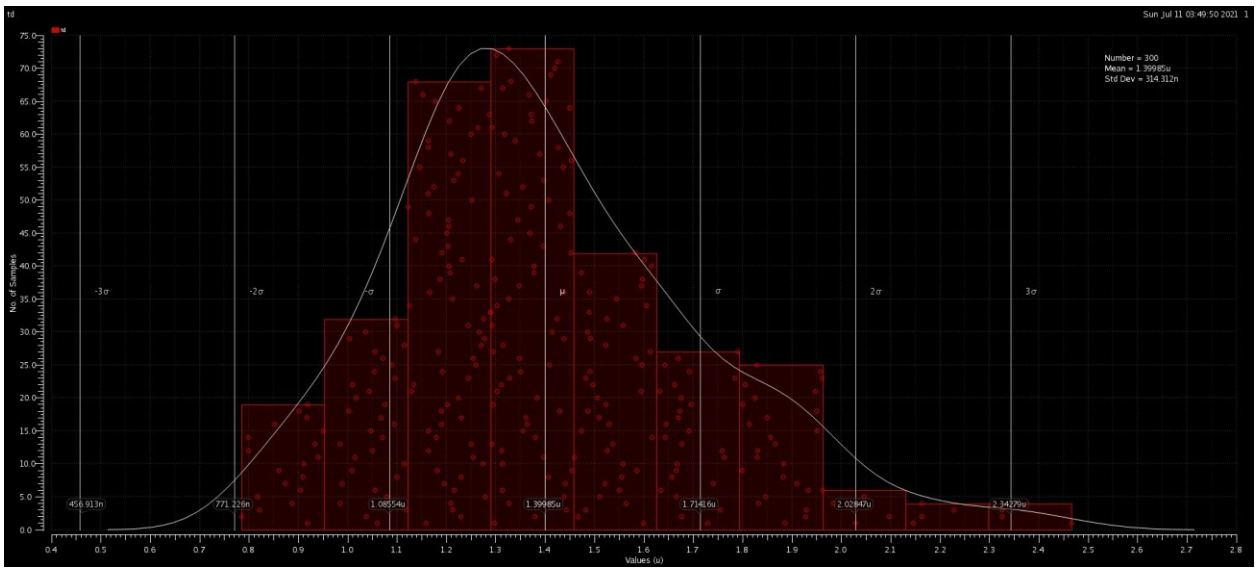


Figure 3. 40. Monte Carlo Simulation results (Process variations and mismatches) of the delay-cell for the typical delay value of 1.37 µs at 27 ℃.

Table 3. 10. Delay-cell variability results with 300-points based Monte Carlo Simulation (Process variations + mismatch) for 1.37 µs rising edge delay cell.

Sr. No	Temperature (°C)/ VDD (V)	3.3	3.0	3.6
1	-20	delay Data: Min =791.5 ns Max = 2.498 µs Mean = 1.413 us σ = 317.9 n	delay Data: Min = 798.9 ns Max = 2.533 µs Mean = 1.428 µs σ = 321.8 ns	delay Data: Min = 785.1 ns Max = 2.467 µs Mean = 1.4 µs σ = 314.3 ns
2	20	delay Data: Min = 795.3 s Max = 2.4 µs Mean = 1.371 µs σ = 320.1 ns	delay Data: Min = 795.2 ns Max = 2.43 µs Mean = 1.397 µs σ = 315.2 ns	delay Data: Min = 782.4 ns Max = 2.372 µs Mean = 1.372 µs σ = 310.4 ns
3	80	delay Data: Min = 791.1 ns Max = 2.284 µs Mean = 1.359 µs σ = 310.5 ns	delay Data: Min = 864 ns Max = 2.311 µs Mean = 1.426 µs σ = 272.4 µs	delay Data: Min = 779.5 ns Max = 2.261 µs Mean = 1.305 µs σ = 290.5 ns

Table 3. 11. Process corner simulation results for maximum delay (at 27 °C)

Corner	t_d (µs)
w_n	2.22
w_p	1.885
w_s	2.414

Table 3. 12. Process corner simulation results for minimum delay (at 27 °C)

Corner	t_d (ns)
w_n	275.3
w_p	250.3
w_s	300.3

3.7.4.4. Simulation Results of ADC with Real Delay-Cell

In Verilog-A based ADC, the ideal delay-cell was replaced with the real one. Besides delay-cell, SAR logic with auxiliary cells, CDAC, switches, comparator and SR-latch are also real. All other components are still Verilog-A based for this simulation. The aim is to verify the ADC performance with the real delay-cell and optimize its performance if needed. Figure 3.41 shows the PSD of the ADC, which shows a fully satisfactory performance (ENOB and SNDR) of the ADC with real delay-cell.

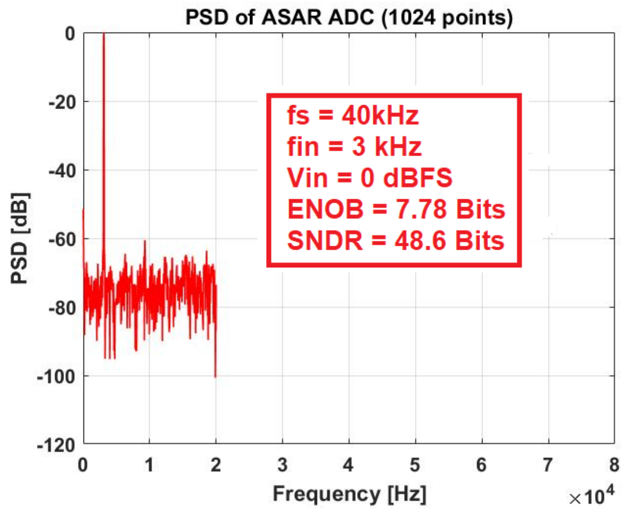


Figure 3. 41. ASAR ADC PSD plot with real delay-cell, SAR logic and auxiliary cells, comparator, SR-latch, CDAC and switches; all other components are Verilog-A based.

3.7.4.5. Layout of Delay-Cell

Figure 3.42 depicts the layout of variable delay-cell. Particular attention has been paid to the parasitics, which could affect the delay amount. Adequate distance has been kept between capacitors and other cells of the delay-cell to avoid any coupling issues as well as reduce variations in the delay value.

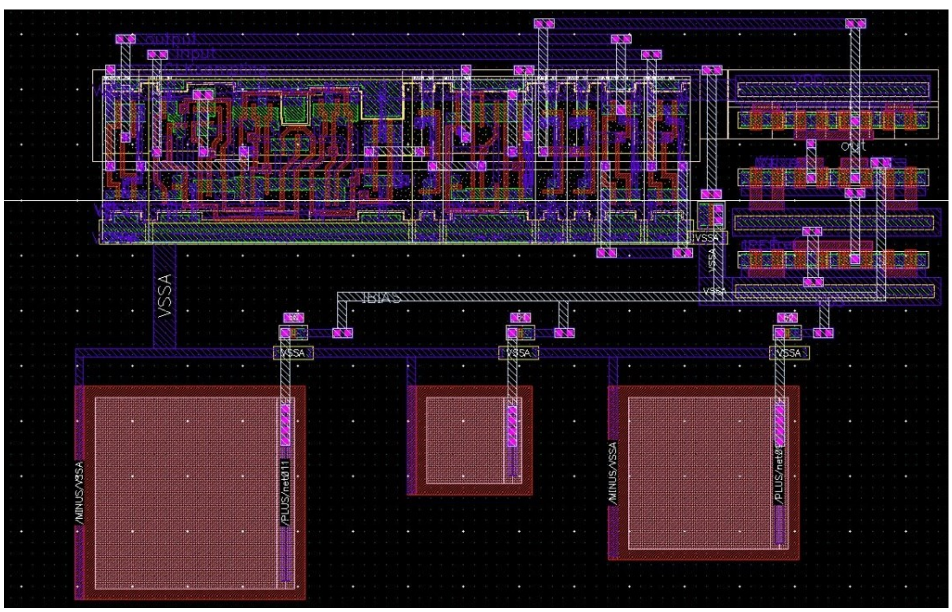


Figure 3. 42. Layout of variable rising edge only delay-cell.

3.7.5. On-Chip Voltage Buffers

There are two implementation choices for voltage buffers for the ADCs. First, design and use of a separate discrete voltage buffer IC to drive the ADC or provide the voltage in an off-chip manner. Second, design of voltage buffer on-chip with the ADC. There are several challenges associated with the first choice. The primary challenge is the effect of parasitics and mutual inductances of the bond-wires, and PCB traces. These exacerbate the CDAC settling. In addition, the voltage buffers can draw large currents via inductances, which can introduce ringing to CDAC capacitor node being charged. This will result in the CDAC node ringing too. Usually, the bond wires parasitic inductance is significant because of the diameter

of the gold wires used for bonding. Just as an example, the bond wire with a diameter of 25. 4 µm and length of 3 mm results in an inductance of 3.24 nH. This can become about 4 nH with the addition of PCB traces inductance. With this inductance, the CDAC of a fully differential 10-bit, 50 MS/s SAR ADC can exhibit significant ringing, which can go higher than the LSB of the ADC, as shown in Figure 3.43 [240]. This degrades ADC performance unacceptably.

There are two methods to mitigate the CDAC settling problems due to inductance parasitics. The first way is to ensure sufficient timing margin for the CDAC settling to diminish the ringing up to desired accuracy level. However, the drawback of this method is the reduced sampling-rate. The second method is to use on-chip decoupling capacitors to cancel ringing. However, the unavoidable need of large value capacitors to restrict the ringing below 1 LSB enhances area, which is impractical for majority of the applications [240].

The use of on-chip voltage buffer is the best way to cater for the ringing effect, which isolates the CDAC capacitors from ringing sources. In addition, the use of on-chip buffer can often reduce area, power, and cost. Therefore, on-chip voltage buffers have been designed for this ADC.

Four voltage buffers are needed for the proposed ASAR ADC, i.e., one for each of V_{IN}, V_{CM}, V_{REFP} and V_{REFN}. For all of these, closed-loop buffer topology has been opted out because of its better robustness and accuracy-based advantages compared to open-loop topology.

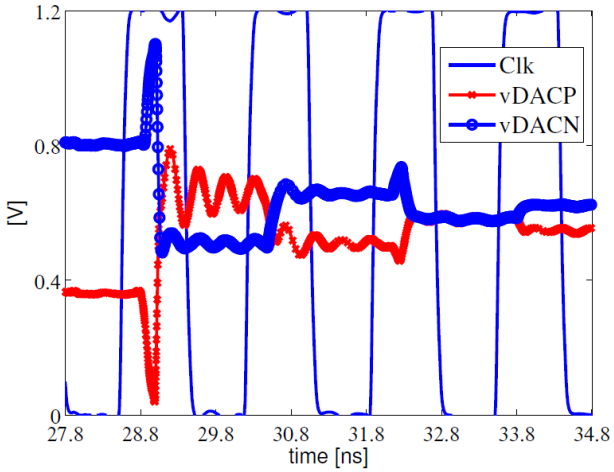


Figure 3. 43. Ringing on the CDAC node of a differential SAR ADC due to a 4 nH parasitic inductance [240].

3.7.5.1. Input Voltage (V_{IN}) and Common Mode Voltage (V_{CM}) Buffers Design

The first step in the design of input and common mode voltage buffers design is to derive their specifications analytically according to the ADC requirements, which can act as a starting point for the buffers design. These parameters can then be optimized with the help of the simulations. The main specification parameters include voltage settling time, slew-rate, unity gain frequency, and DC gain. Requirements for the input and common-mode voltage buffers (V_{IN} and V_{CM}) are the same since both of them are active during the sampling phase, so the following derivation process is valid for both of these voltage buffers. However, the linearity of the input buffer is an essential requirement, which will be considered during the design of the input buffer in the following section.

3.7.5.1.1. Buffer output Voltage Settling Time (t_s)

The approximate sampling period (T_s) of CLKSampling is given below (for calculations purpose):

$$T_s = 2.78\ \mu s$$

To ensure proper settling for the buffer output voltage, its settling time (t_s) has been calculated by:

$$t_s = \frac{T_s}{4} = 0.6\ \mu s$$

Keeping in view the settling nature of the buffer output (Figure 3.44), t_s can be divided into 2 parts: constant slope region (slewing) and linear (almost) settling region. As linear settling takes longer time than the constant slop, a better approximation is to allocate 10 % of the total buffer settling time (t_s) to slewing region and 90 % to linear slope region. This approximation has been taken for calculation purposes. In other words:

(a) Constant slop (slewing) settling time = 10 % (t_s)

(b) Linear settling time = 90 % (t_s)

(a) will give us the slew-rate, and (b) will provide us with the unity-gain frequency of the voltage buffers.

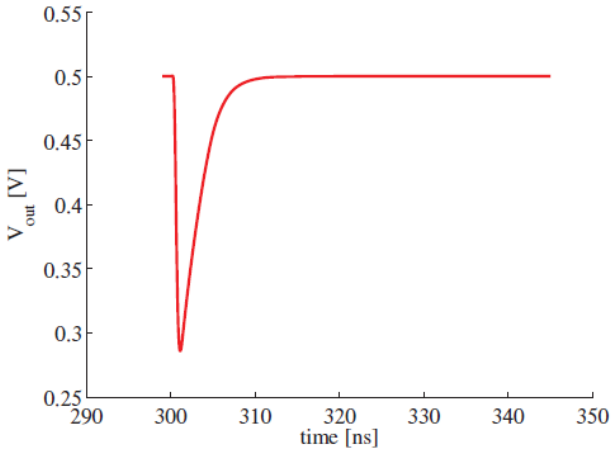


Figure 3. 44. Settling nature of voltage buffers for the SAR ADC, taken from [241].

3.7.5.1.2. Slew Rate

To calculate the slew rate, first we need to calculate the worst-case output settling of the voltage buffers for the CDAC. Figure 3.45 shows the worst-case settling condition for the input and common mode voltage buffers.

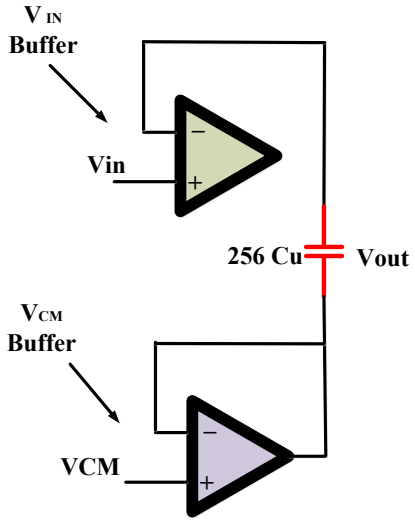


Figure 3. 45. Worst-case settling condition of input and common mode voltage buffers outputs for the CDAC.

Based on charge conservation, the change in output voltage for this worst case can be calculated as follows:

$$\Delta V_{out} = \frac{V_{FS}}{2} = 1\ V$$

So,

$$\text{Slew rate} = \frac{\Delta V_{out}}{t_{slew}} = \frac{1}{(0.1)(0.6u)} = 16.67\ V/\mu s$$

However, the slew rate is not significant for these buffers because of the charge redistribution operation of CDAC. The settling is mainly determined by the unity gain frequency. Based on this observation, we may simply ignore the slew rate or assume a lower value for calculation purposes. Let us assume that:

$$\text{Slew rate (selected)} = 5\ V/\mu s$$

Also,

$$\text{Slew rate(selected)} = \frac{\Delta V_{out}}{t_{slew}} = \frac{I_{out,min}}{C_L}$$

Where $C_L = C_{DAC} = 5.12\ pF$

Thus,

$$I_{out,min} = 15\ \mu A$$

3.7.5.1.3. Unity-Gain Frequency

Step response for a single pole amplifier in a closed loop configuration is given by:

$$V_{out}(t) = V_{step}(1 - e^{-t/\tau})$$

Here,

$$\tau = \frac{1}{(\beta)(2\pi f_{ug})}$$

For unity feedback configuration, β=1.

The settling error is given by:

$$\varepsilon = e^{-t/\tau}$$

Based on above:

$$f_{ug} = \frac{-\ln(\varepsilon)}{2\pi t}$$

For 10-bits settling (to be on safer side):

$$f_{ug} = 2\ MHz$$

This is a reasonably good approximation for the common mode buffer. However, a higher value will be required for the input buffer to enable sampling-rate reconfigurability as well as get required linearity. This fact will be taken care of during input buffer design.

3.7.5.1.4. DC Gain (A_0)

The gain-error factor due to the finite open loop DC gain in closed loop configuration:

$$\text{Gain error factor} = \frac{1}{A_0\beta} = \frac{1}{A_0}$$

Accepting 0.5 % error, we get,

$$A_0 = 200 = 46\ \text{dB}$$

For common mode buffer, this value is a good starting point. However, this is not adequate for the input buffer because of linearity requirements. This will be taken care of while designing the input buffer. Table 3.13 summarizes the derived specification parameters for voltage reference buffers.

Table 3. 13. A Summary of Specifications of input and common mode Voltage Buffers (V_{IN} and V_{CM}) derived analytically

Sr. No.	Parameter	Calculated Value
1.	Sampling phase duration of ADC	2.78 µs
3.	Buffer voltage Settling Time (t_s)	0.6 µs
3.	V_{DD}	3.3 V
4.	DC Gain	46 dB*
5.	C_L=C_{DAC}	5.12 pF
6.	Slew Rate (SR)	~ 5 V/µs
7.	GBW	2 MHz*
8.	I_{REF}	~ 15 µA*
9.	Offset	Temperature independent
10.	Input noise	< ¼ LSB
11.	Linearity	Must for V_{IN} buffer

* Good approximation only for V_{CM} buffer; a higher value is needed for V_{IN} buffer

3.7.5.2. Input Buffer Design

The first step is the selection of a suitable architecture for the input buffer. As the input signal swing is large (1.65 ±1 V), the design of simple closed loop amplifiers (e.g., two stage OP-AMP, etc.) is not possible to design at 3.3 V because of the signal swing limitations. As a result, a non-inverting OP-AMP with a gain of 2 has been chosen as the input buffer. Figure 3.46 shows the schematic diagram of the buffer. A 2 stage CMOS amplifier has been selected as the OP-AMP of the buffer. Circuit diagram of the selected 2 stage CMOS amplifier is shown in Figure 3.47. Table 3.13 shows the target specifications of the input voltage buffer derived analytically.

First step in the buffer design process is to calculate the resistors (R_1 and R_2) values. Because of a gain of 2, both the resistors need to be equal valued, as dictated by the following relationship:

$$A_{\text{noninverting}} = 1 + \frac{R_2}{R_1} = 1 + 1 = 2$$

The noise of the input buffer must be lower than ¼ LSB (1.95 mV) of the ADC. Therefore, the resistor values should be chosen to ensure this requirement. Assuming 100 kΩ resistor values for a GBW of 2 MHz,

$$V_{nR} = 4kTRBW = 3.3nV$$

Also,

$$V_{nRMS} = V_{nR} \times \sqrt{2} = 4.66\ \text{nV} < \frac{1}{4}\text{LSB}$$

The above calculations show that 100 kΩ resistor value is fine from noise requirements point of view. Next step is to calculate a value of the current needed to maintain the required value of noise. It can be written,

$$\frac{4kT}{g_{m1}} \times BW < 500\ \mu V\ (< \frac{1}{4} LSB) \qquad (3.2)$$

Also,

$$\frac{1}{g_{m1}} = 100\ k\Omega$$

This implies,

$$g_{m1} = 10\ \mu A/V$$

From (3.2)

$$\frac{4kT}{g_{m1}} \times BW = 2.345 \times 10^{-18} < \frac{1}{4} LSB$$

This value of g_{m1} satisfies the condition. Now, the required current can be calculated as:

$$g_{m1} = \frac{2I_{D1}}{V_{OV}}$$

which leads to:

$$I_{D1} = 10\ \mu A$$

This value of the current is a good starting point from calculation point of view. This leads to a tail current of 20 µA for the first stage of the OP-AMP (Figure 3.47).

The next step is to calculate transistor dimensions for 2-stage OP-AMP, which have been achieved using the following analysis. Supply voltage is 3.3 V.

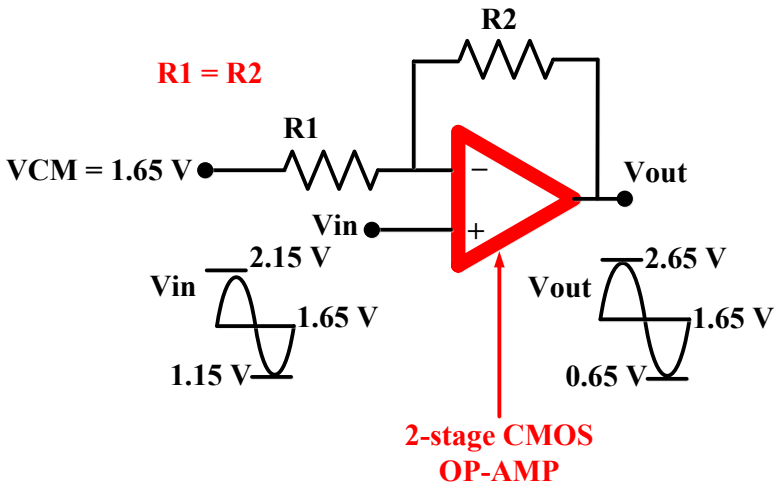


Figure 3. 46. Schematic diagram of a non-inverting OP-AMP with a gain of 2 acting as the input voltage buffer for ADC.

As $I_{BIAS} = I_D = 20\ \mu A$

So, $I_{D1} = 10\ \mu A$

$$g_{m1,2} = \frac{2I_{D1}}{V_{ov}} \tag{3.3}$$

Let, $V_{ov} = 0.1\ V$

$V_{gs} = 0.65\ V$

(3.3) leads to $g_{m1,2} = 200\ \mu S$

To have a margin, let:

$$g_{m1,2} = 250\ \mu S$$

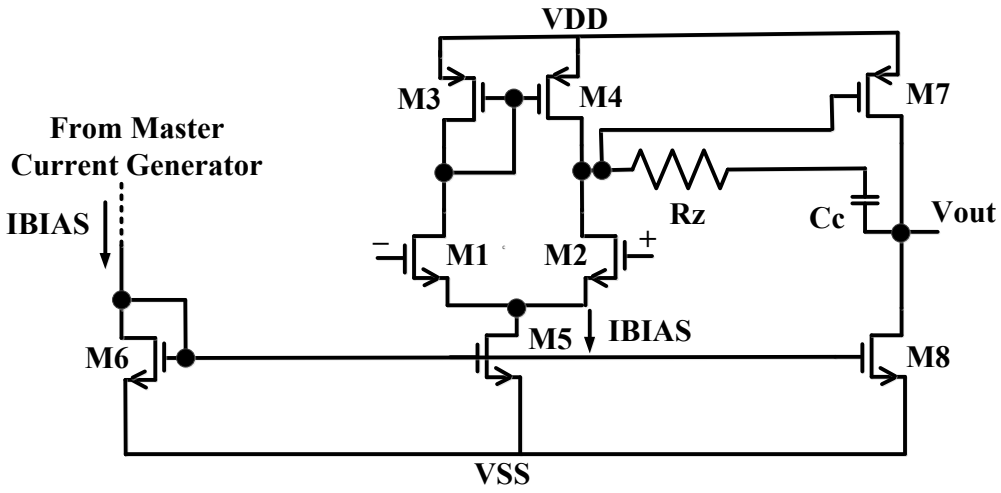


Figure 3. 47. 2-stage OP-AMP schematic for the input buffer.

For M_1 and M_2,

$$\left(W/L\right)_{1,2} = \frac{g_{m1,2}^2}{2I_{D1}u_n C_{ox}} = 17$$

For M_3, and M_4,

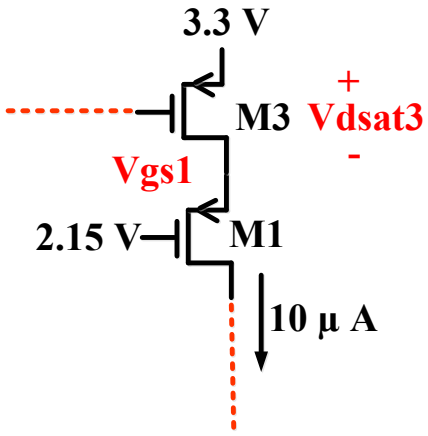


Figure 3. 48. Part of input buffer schematic for calculation of M_3 and M_4 aspect ratios.

From Figure 3.48,

$$V_x > 2.15 - 0.1\ V$$

Let, $$V_x = 3.1\ V$$

Then, $$V_{dsat3} = 3.3 - 3.1 = 0.2\ V$$

$$I_{D3,4} = \frac{1}{2} u_n C_{ox} \left(\frac{W}{L}\right)_1 (V_{dsat3})^2$$

$$\left(\frac{W}{L}\right)_{3,4} = 10$$

For M_5, and M_6,

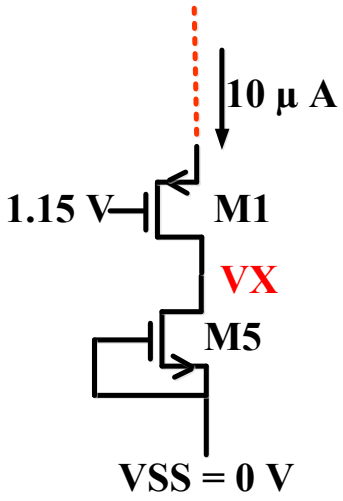


Figure 3. 49. Part of input buffer schematic for calculation of M_5 and M_6 aspect ratios.

From Figure 3.49,

$$1.15\ V > V_{gs1} + V_{dsat5}$$

$$V_{dsat5} < 1.76\ V$$

Let, $$V_{dsat5} = 0.15\ V$$

Then,

$$I_{D5,6} = \frac{1}{2} u_n C_{ox} \left(\frac{W}{L}\right)_1 (V_{dsat5})^2$$

$$\left(\frac{W}{L}\right)_{5,6} = 7$$

To ensure same tail current in both the stages, and thus symmetrical slew-rate:

$$\left(\frac{W}{L}\right)_{1,2} = \left(\frac{W}{L}\right)_7 = 20$$

Also, to ensure same current in both the stages:

$$\left(\frac{W}{L}\right)_{5,6} = \left(\frac{W}{L}\right)_8 = 7$$

For zero nulling resistor,

$$R_z = \frac{1}{g_{m6}} = 16\ k\Omega$$

The circuit was simulated with these initial values. To minimize the offset and input refereed noise, the width of M_1 and M_2 were increased from 17 to 20. Also, a few changes were made to optimize the performance. Table 3.14 shows the final achieved specifications of the designed input buffer circuit, which shows that all the requirements set initially are met. In addition, the input offset voltage of the buffer is temperature insensitive, as verified by the Monto Carlo (mismatch and process variations) simulations results (Figure 3.53-3.55 and Table 3.15). Linearity of the input buffer has been measured in two ways. Static linearity has been assessed by plotting the transfer characteristics (Figure 3.51), which shows a linear response. Dynamic linearity has been verified with the help of the PSD plot of the buffer (Figure 3.52), which confirms an ENOB of about 15 bits.

To enable the turn on and off capability of the buffer, four switches (S_1-S_4) have been added in the circuit. These switches are directly driven by the Enable (CLKSampling) signal. When the CLKSampling signal is high (during the sampling phase only), input buffer is on. It is off when the CLKSampling signal is low, i.e., during the conversion phase. This results in a significant reduction in the average power of the buffer. Figure 3.50 shows the final schematic of the buffer with the switches.

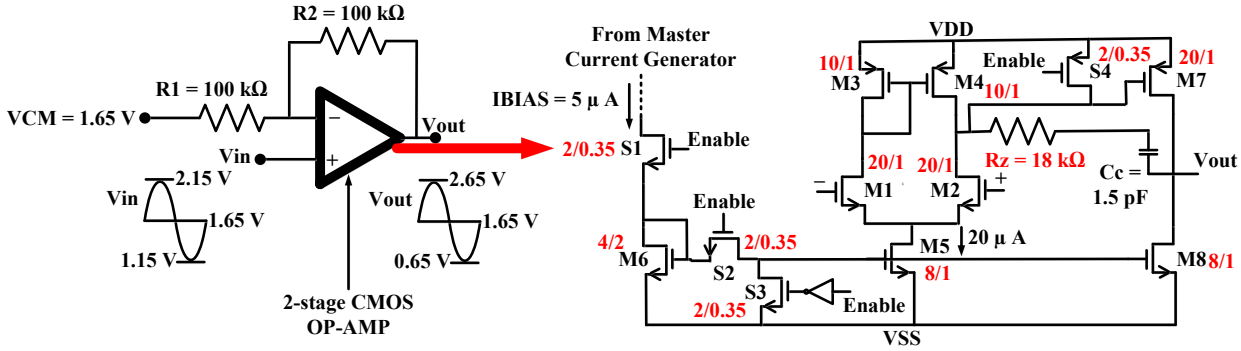


Figure 3. 50. Circuit diagram of the designed input buffer.

Table 3. 14. Specifications and Results of designed V_{IN} Buffer

Sr. No.	Parameter	Value
1.	I_{REF} (µA)	20 (first stage) + 20 (second stage) = 40 *Only for open loop OP-AMP of the buffer*
2.	C_L(pF)	5.12 (C_{DAC})
3.	Loop Gain (dB)	68.422
4.	Phase Margin	62°
5.	Total summarized noise (mV)	1.063 (< ¼ LSB)
6.	GBW (MHz)	6.63
7.	Systematic Offset/Gain error (mV)	6.5 (< 1 LSB)
8.	Settling Time (µs)	0.5
9.	PSRR	-53.49 dB/2.15 mV @ 20 kHz
10.	Linearity*: Method1; Method 2	0.035 %; 15.13 bits and SNR = 92.8 dB @ 20 kHz

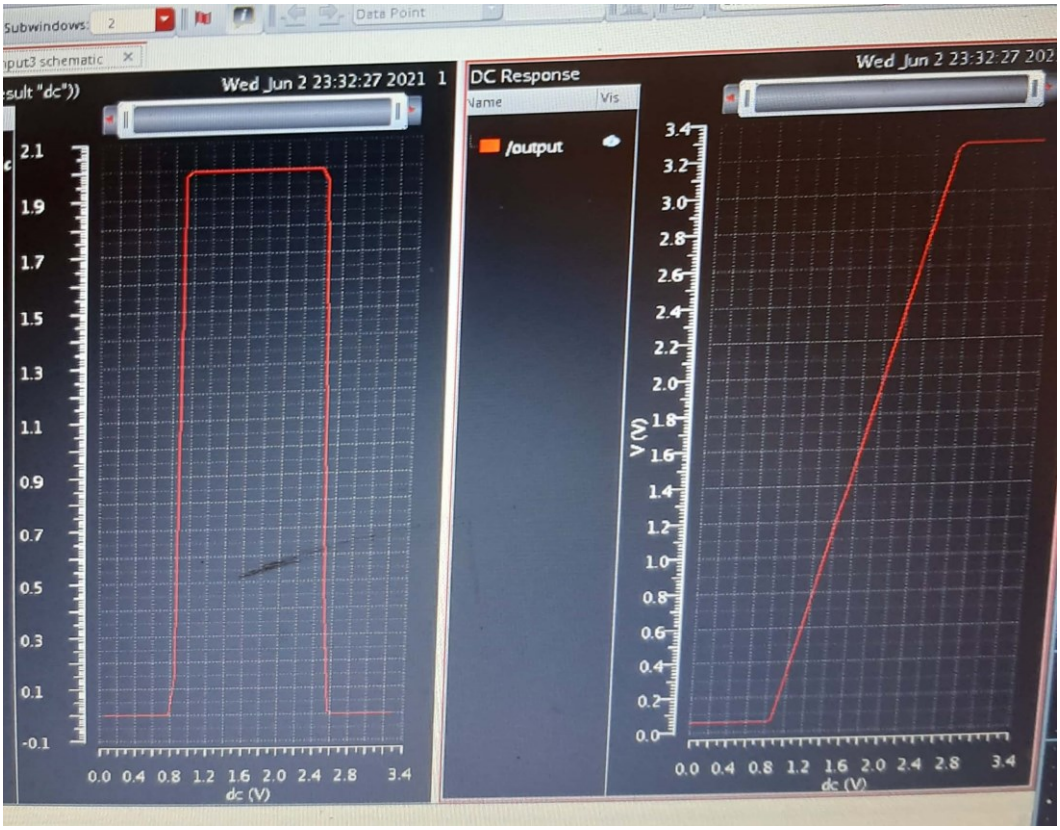


Figure 3. 51. Result of the derivative/static linearity of the input buffer transfer function (input is at x-axis and the output is at y-axis).

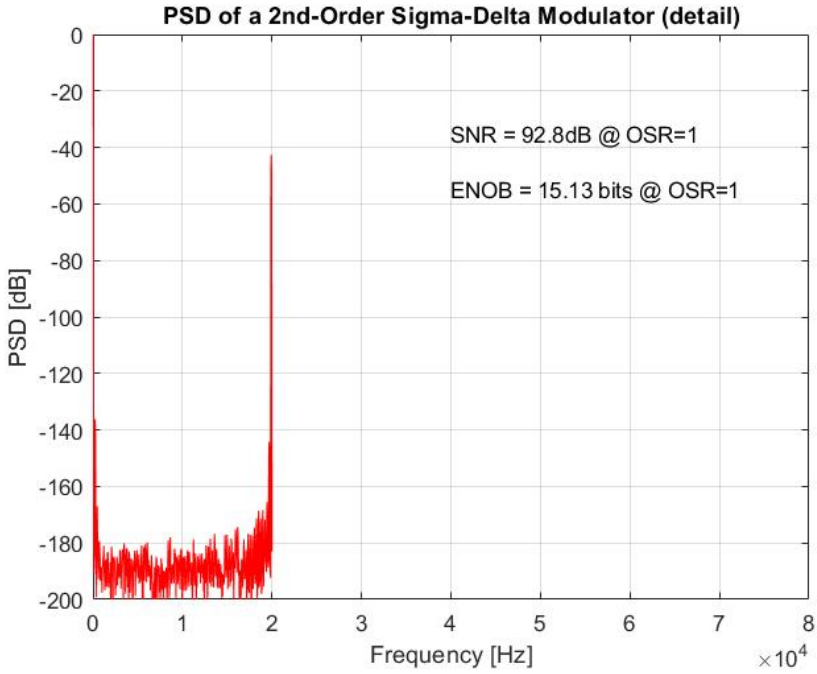
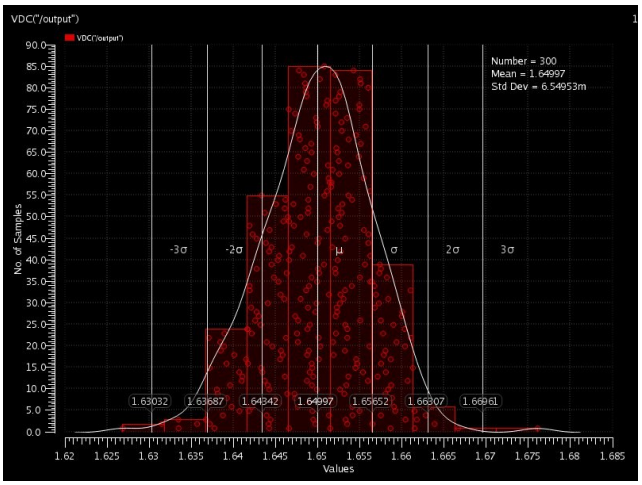
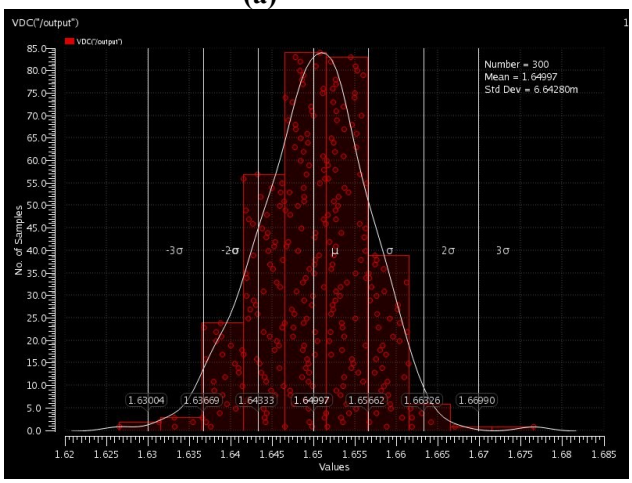


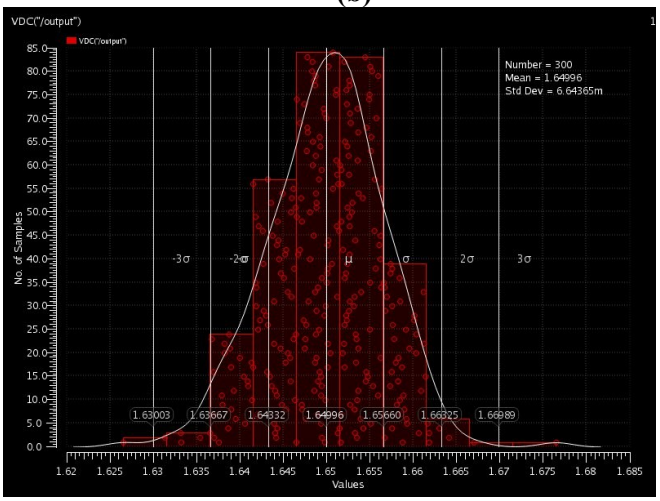
Figure 3. 52. PSD plot of input buffer output at 20 kHz showing dynamic linearity.



(a)

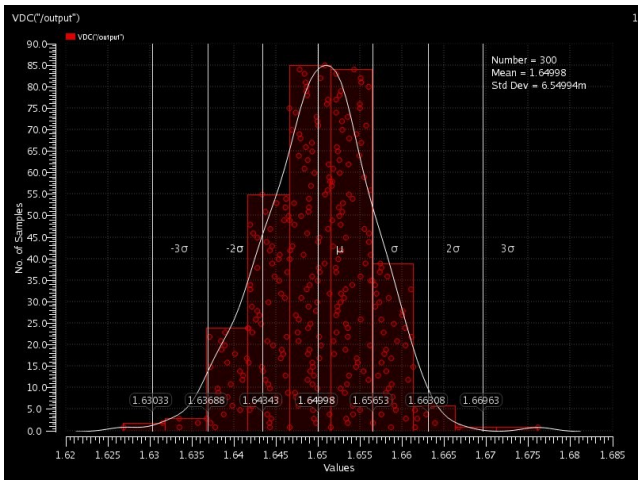


(b)

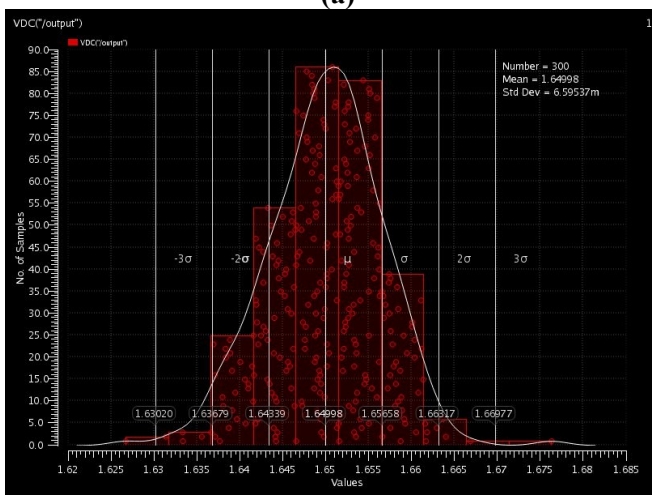


(c)

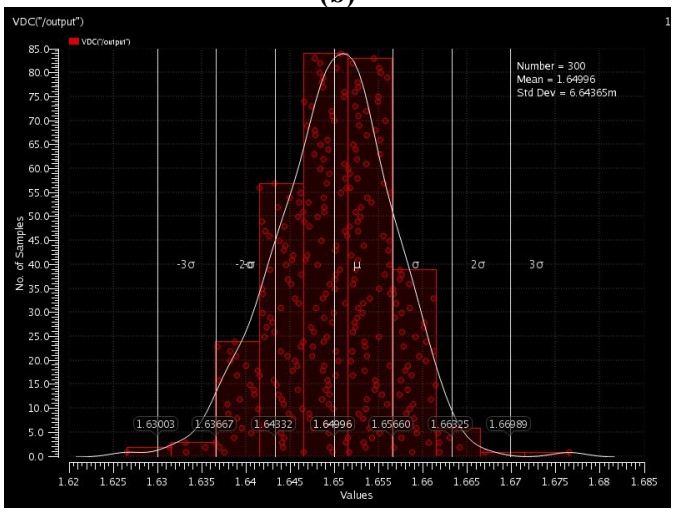
Figure 3. 53. Monte Carlo (mismatch + process variations) simulation result of V_{IN} buffer offset voltage at $V_{DD} = 3.3\ V$ and (a) T= 0 °C, (b) T= 27 °C, and (c) T= 50 ℃.



(a)

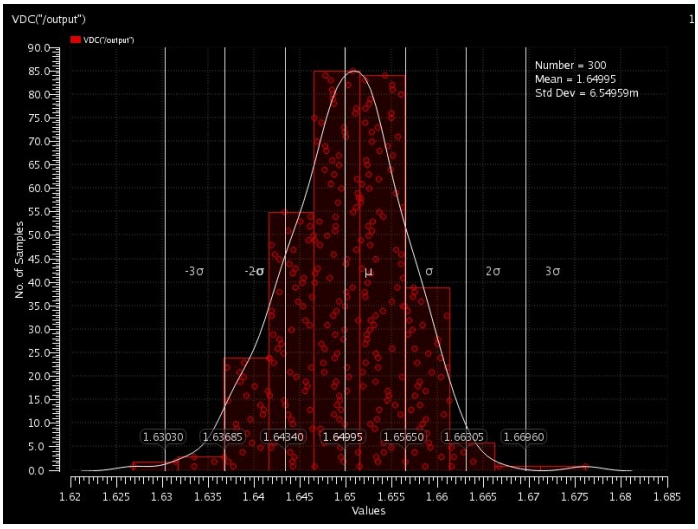


(b)

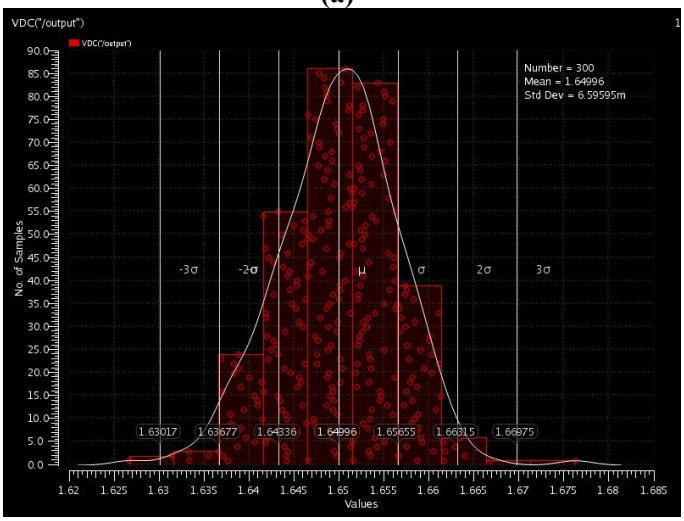


(c)

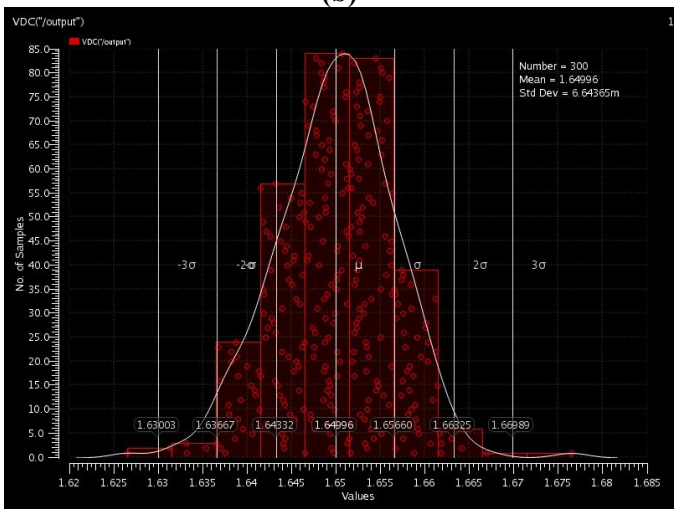
Figure 3. 54. Monte Carlo (mismatch + process variations) simulation result of V_{IN} buffer offset voltage at $V_{DD} = 3.6\,V$ and (a) T= 0 °C, (b) T= 27 °C, and (c) T= 50 °C.



(a)



(b)



(c)

Figure 3. 55. Monte Carlo (mismatch + process variations) simulation result of V_{IN} buffer offset voltage at $V_{DD} = 3.0\ V$ and (a) T= 0 °C, (b) T= 27 °C, and (c) T= 50 °C.

Table 3. 15. Input buffer Offset voltage's standard deviation with 300-points based Monte Carlo Simulation (Process variations + mismatch) calculated with Vin = 1.65 V in buffer configuration

Sr. No	Temperature (°C)/ VDD (V)	3.0	3.3	3.6
1	0	Offset Data (in mV): σ = 6.54	Offset Data (in mV): σ = 6.656	Offset Data (in mV): σ = 6.549
2	27	Offset Data (in mV): σ = 6.595	Offset Data (in mV): σ = 6.701	Offset Data (in mV): σ = 6.595
3	50	Offset Data (in mV): σ = 6.643	Offset Data (in mV): σ = 6.747	Offset Data (in mV): σ = 6.643

3.7.5.2.1. ADC Simulation Results with Real Input Buffer

In Verilog-A based ADC, the ideal input voltage was replaced with the real input buffer. Besides input buffer, delay-cell, SAR logic with auxiliary cells, CDAC, switches, comparator and SR-latch are also real. All other components are still Verilog-A based for this simulation. The aim is to verify the ADC performance with the real delay-cell and optimize its performance if needed. Figure 3.56 shows the PSD of the ADC, which shows a fully satisfactory performance (ENOB and SNDR) of the ADC with real input buffer.

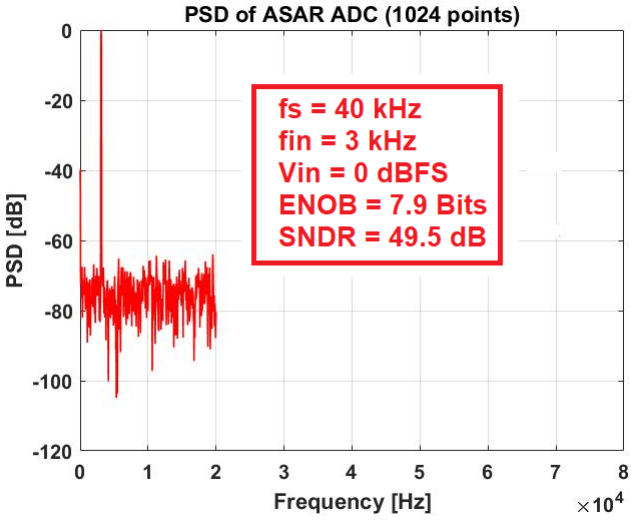


Figure 3. 56. ASAR ADC PSD plot with real input buffer, comparator, SR-latch, CDAC and switches; SAR logic and auxiliary cells. All other components are Verilog-A based.

3.7.5.2.2. Layout of Input Buffer

Figure 3.57 depicts layout of the input buffer. Besides stacked and interdigitated structure to ensure matching, dummy devices have been added to cater for the boundary conditions. To save area, turns have been introduced to the feedback resistors. A square capacitor layout has been preferred for better matching.

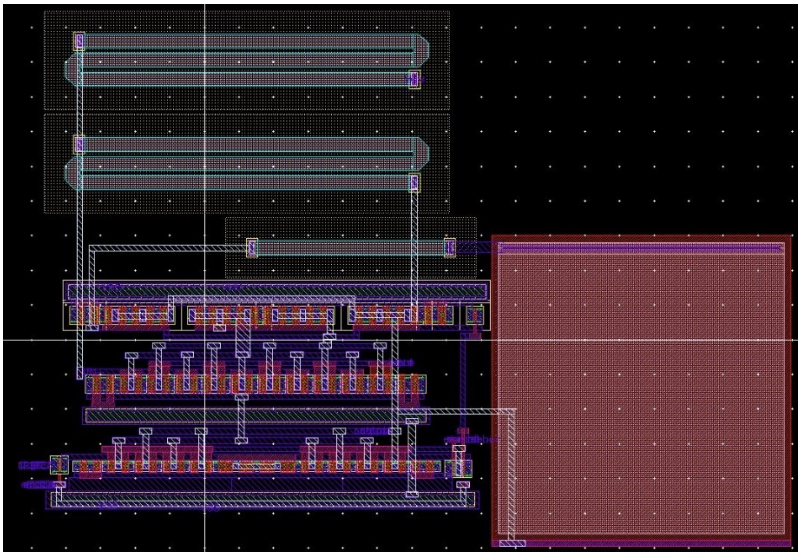


Figure 3. 57. Layout of input buffer.

3.7.5.3. Common Mode (V_{CM}) Voltage Buffer Design

A closed-loop single stage common source with active load topology has been selected for the common mode voltage buffer with NMOS input pair. The circuit diagram of the voltage buffer is given in Figure 3.58. Table 3.13 enlists the target derived specifications of the voltage buffer. Transistor dimensions have been achieved using the following analysis. Supply voltage is 3.3 V.

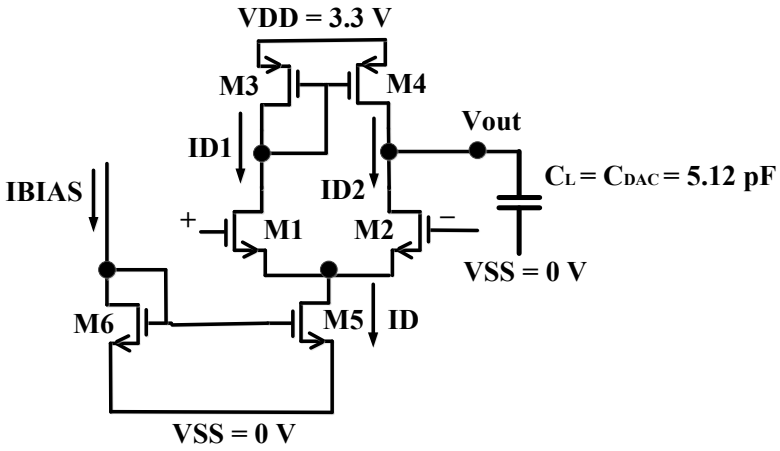


Figure 3. 58. Schematic diagram of common mode voltage buffer.

From the analysis, $I_D = 15\ \mu A$

So, $I_{D1} = 7.5\ \mu A$

$$g_{m1,2} = \frac{2I_{D1}}{V_{ov}} \tag{3.4}$$

Let, $V_{ov} = 0.1\ V$

$V_{gs} = 0.65\ V$

(3.4) leads to $g_{m1,2} = 150\ \mu S$

For M_1 and M_2,

$$(W/L)_{1,2} = \frac{g_{m1,2}^2}{2I_{D1}u_nC_{ox}} = 10$$

For M_5, and M_6,

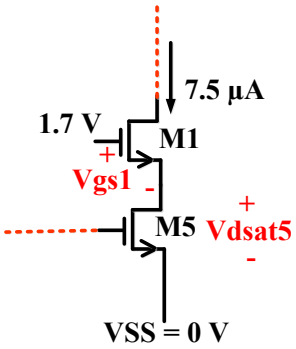


Figure 3. 59. Part of common mode buffer schematic for calculation of M_5 and M_6 aspect ratios.

From Figure 3.59,

$$1.7\ V > V_{gs1} + V_{dsat5}$$

$$V_{dsat5} < 1\ V$$

Let, $$V_{dsat5} = 0.3\ V$$

Then,

$$I_{D5,6} = \frac{1}{2}u_nC_{ox}(\frac{W}{L})_1(V_{dsat5})^2$$

$$(\frac{W}{L})_{5,6} = 2$$

For M_3, and M_4,

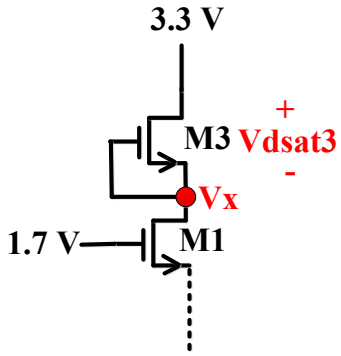


Figure 3. 60. Part of common mode buffer schematic for calculation of M_3 and M_4 aspect ratios.

From Figure 3.60,

$$V_x > 1.7 - 0.1\ V$$

Let, $$V_x = 3\ V$$

Then, $$V_{dsat3} = 3.3 - 3 = 0.3\ V$$

$$I_{D3,4} = \frac{1}{2} u_n C_{ox} \left(\frac{W}{L}\right)_1 (V_{dsat3})^2$$

$$\left(\frac{W}{L}\right)_{3,4} = 4$$

The circuit was simulated with these initial values. To minimize the offset and input refereed noise, the width of M_1 and M_2 were increased from 10 to 14. Table 3.16 summarizes the final specifications of the designed common mode buffer circuit, which shows that all the requirements set initially are met. In addition, the input offset voltage of the buffer is temperature insensitive, as verified by the Monto Carlo (mismatch and process variations) simulations results (Figure 3.64-3.71 and Table 3.17). In addition, PSRR plots of the buffer are also shown in Figure 3.62 and Figure 3.63. The achieved PSRR is adequate for a single ended buffer architecture.

To enable the turn on and off capability of the buffer, three switches (S_1-S_3) have been added in the circuit. These switches are directly driven by the Enable (CLKSampling) signal. When the CLKSampling signal is high (during the sampling phase only), the common mode buffer is on. It is off when the CLKSampling signal is low, i.e., during the conversion phase. This results in a significant reduction in the average power of the buffer. Figure 3.61 shows the final schematic of the buffer with the switches.

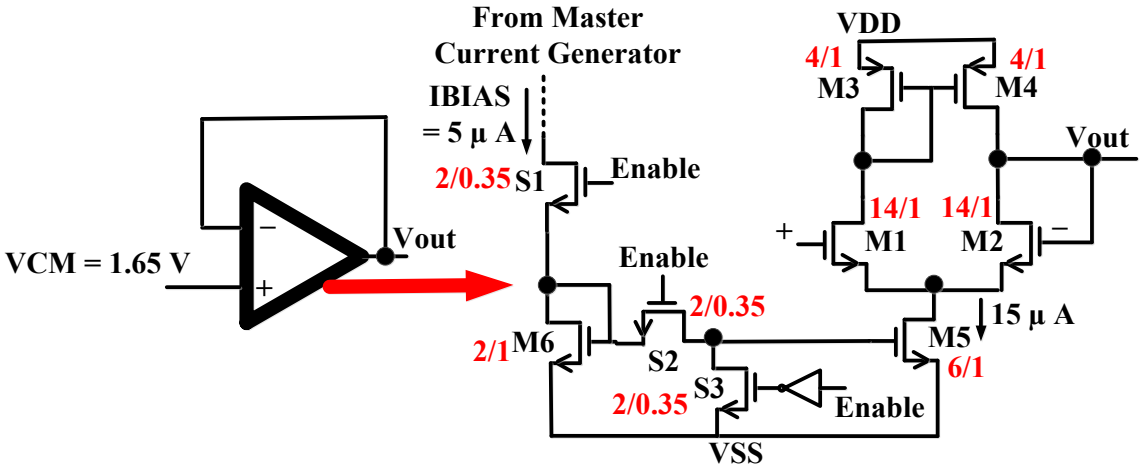


Figure 3. 61. Common mode voltage buffer with transistor dimensions.

Table 3. 16. Specifications and Results of designed V_{CM} Buffer

Sr. No.	Parameter	Value
1.	I_{REF} (µA)	15
2.	C_L(pF)	5.12 (C_{DAC})
3.	Loop Gain (dB)	47
4.	Total summarized noise (µV)	381(< ¼ LSB)
5.	Input-referred noise (mV)	0.8
6.	Bandwidth (MHz)	4
7.	Systematic Offset/Gain error (mV)	3.8 (~ ½ LSB)
8.	Settling Time (µs)	0.25
9.	PSRR	-48.32 dB/3.87 mV

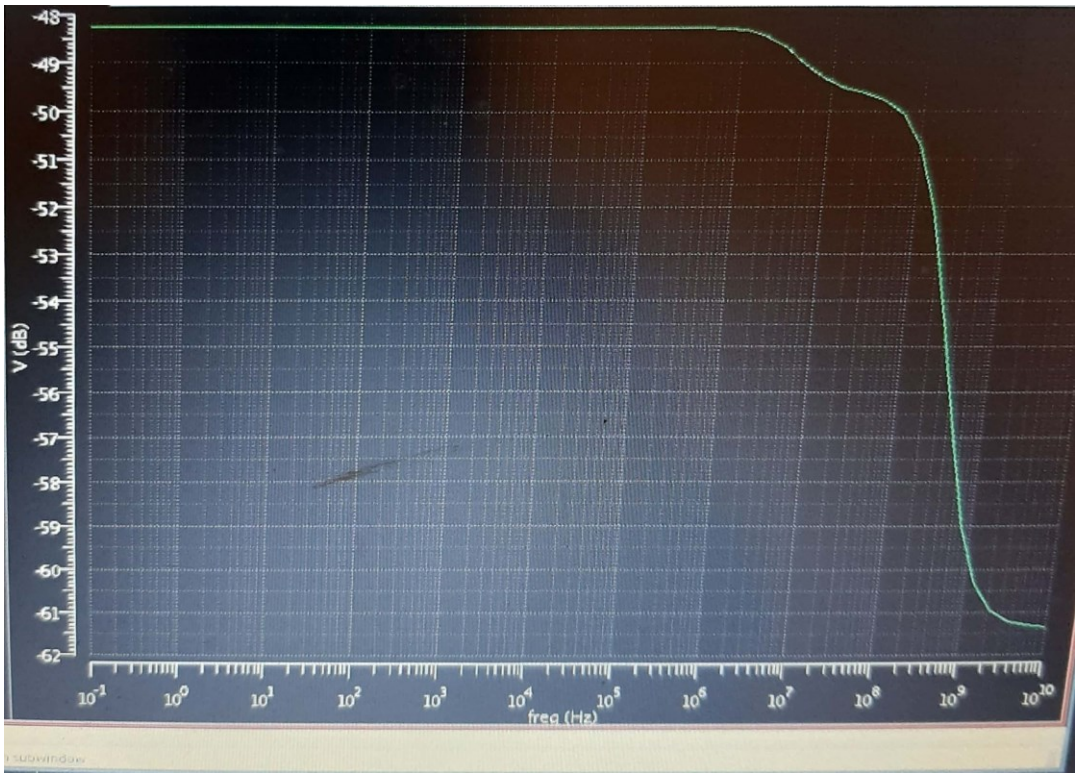


Figure 3. 62. PSRR plot for V_{CM} Buffer (dB).

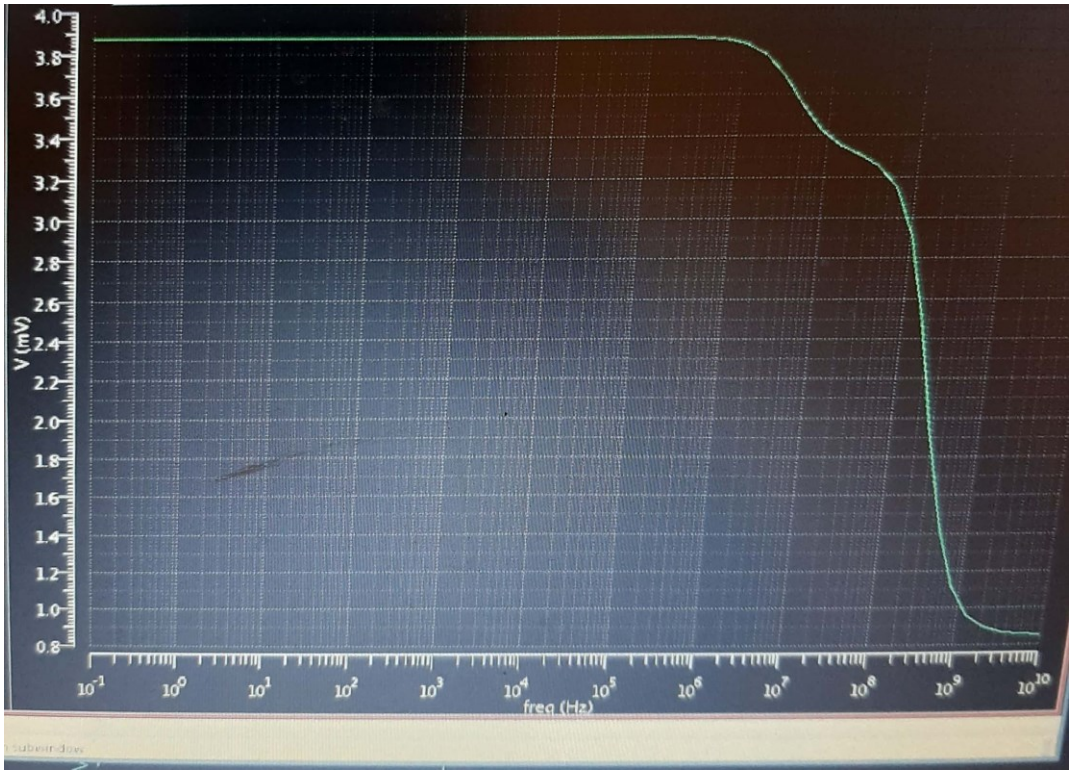


Figure 3. 63. PSRR plot for V_{CM} Buffer (V).

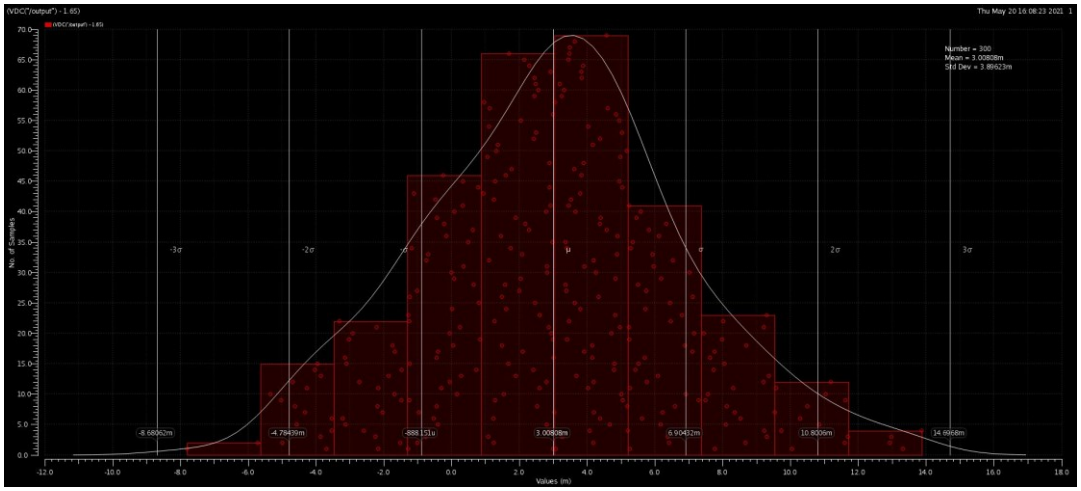


Figure 3. 64. Monte Carlo (mismatch + process variations) simulation result of V_{CM} buffer offset voltage at $V_{DD} = 3.3\ V$ and T= 0 °C.

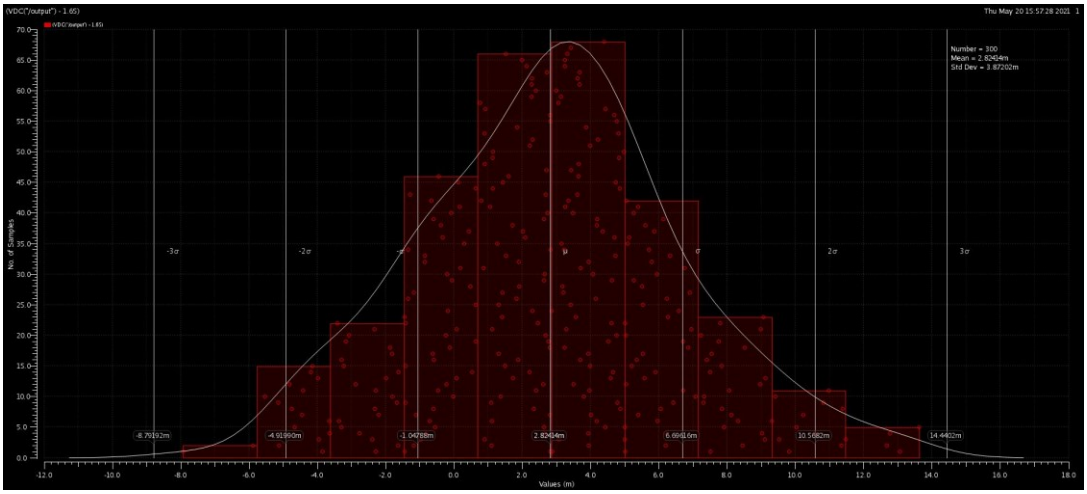


Figure 3. 65. Monte Carlo (mismatch + process variations) simulation result of V_{CM} buffer offset voltage at $V_{DD} = 3.3\ V$ and T= 27 °C.

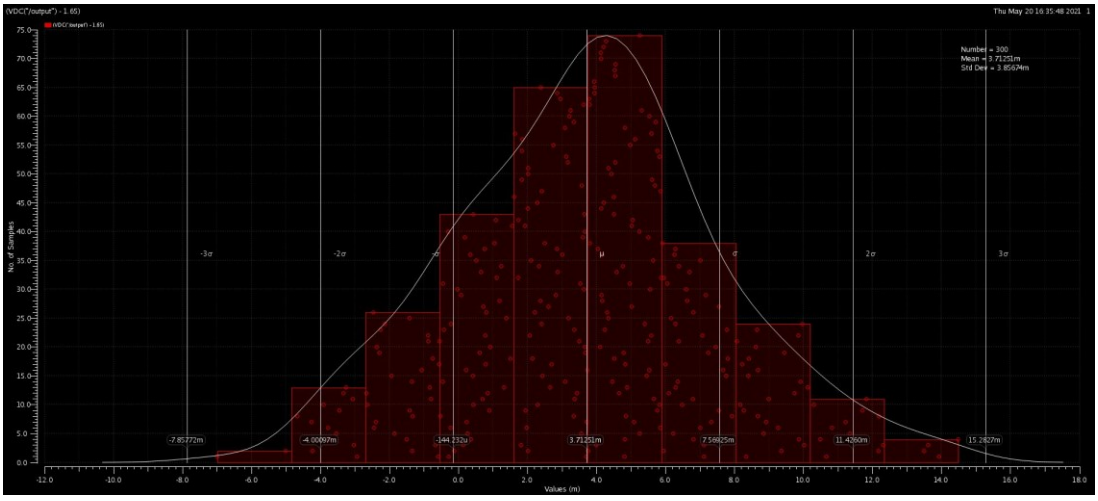


Figure 3. 66. Monte Carlo (mismatch + process variations) simulation result of V_{CM} buffer offset voltage at $V_{DD} = 3.6\ V$ and T= 0 °C.

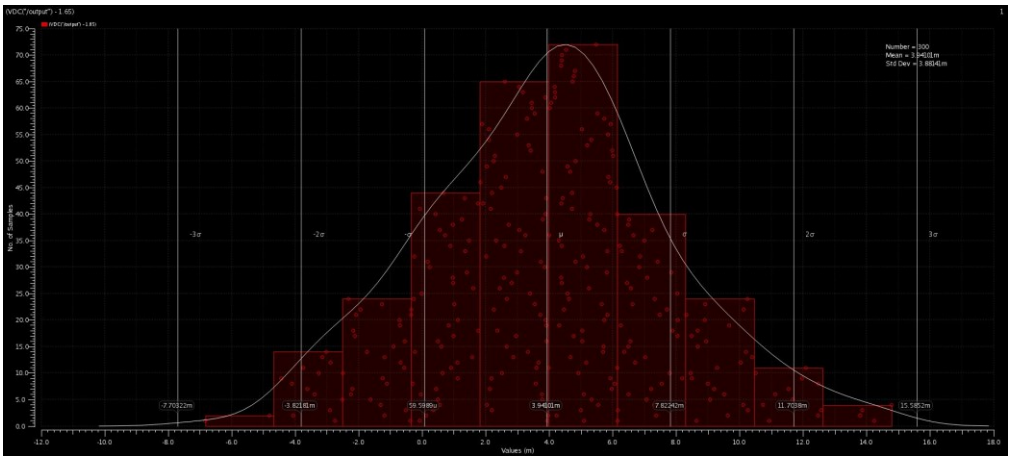


Figure 3. 67. Monte Carlo (mismatch + process variations) simulation result of V_{CM} buffer offset voltage at $V_{DD} =$ 3.6 V and T= 27 °C.

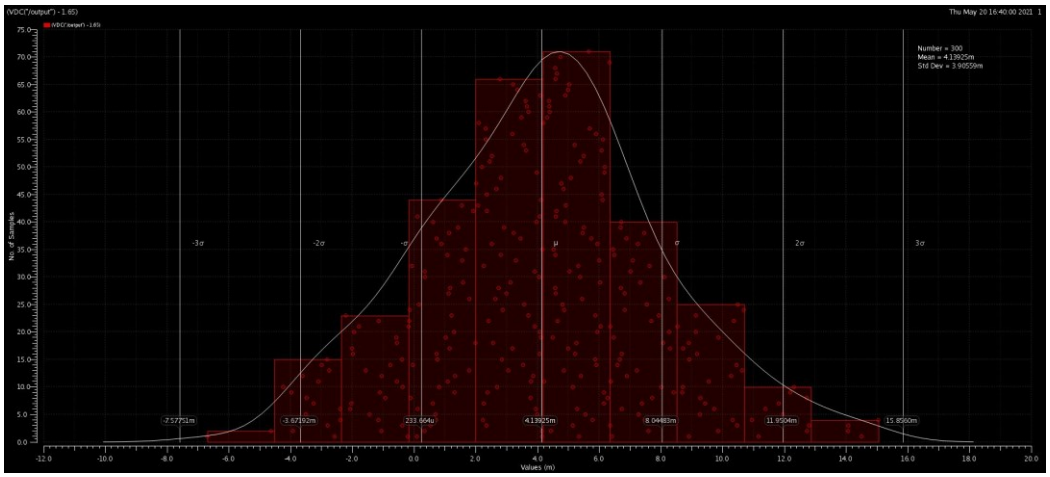


Figure 3. 68. Monte Carlo (mismatch + process variations) simulation result of V_{CM} buffer offset voltage at $V_{DD} =$ 3.6 V and T= 50 °C.

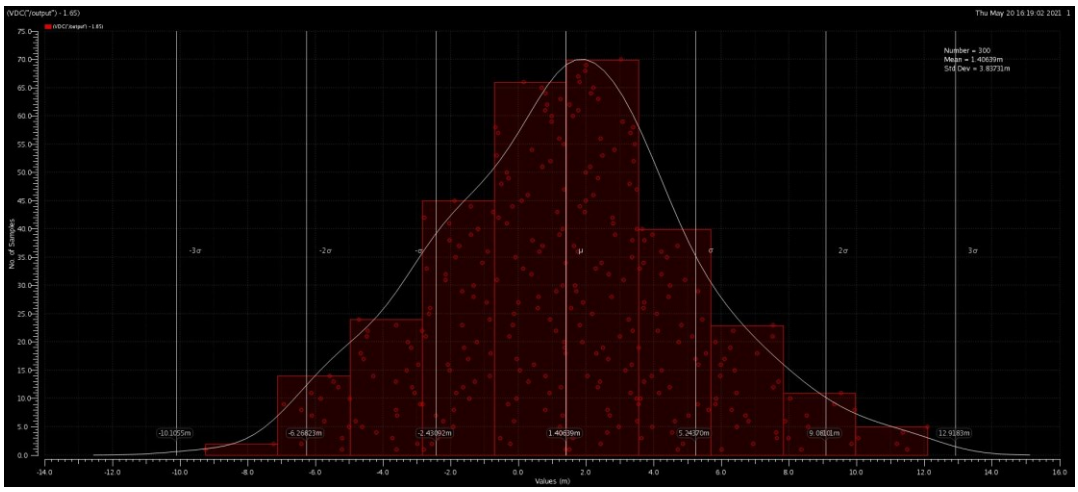


Figure 3. 69. Monte Carlo (mismatch + process variations) simulation result of V_{CM} buffer offset voltage at $V_{DD} =$ 3.0 V and T= 0 °C.

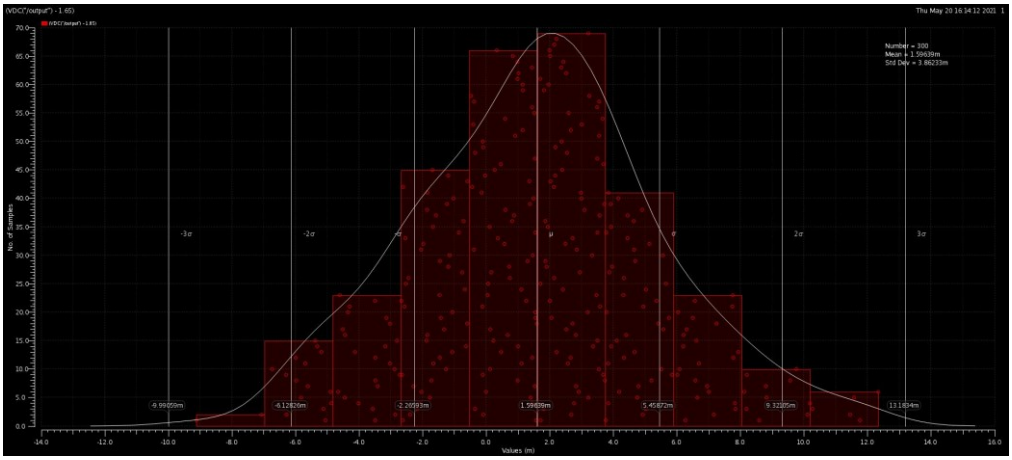


Figure 3. 70. Monte Carlo (mismatch + process variations) simulation result of V_{CM} buffer offset voltage at $V_{DD} = 3.0\ V$ and T= 27 °C.

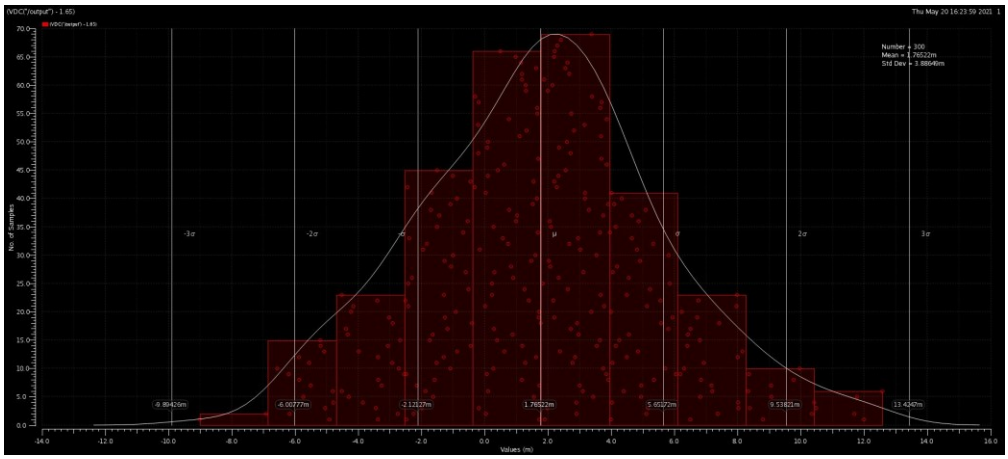


Figure 3. 71. Monte Carlo (mismatch + process variations) simulation result of V_{CM} buffer offset voltage at $V_{DD} = 3.0\ V$ and T= 50 °C.

Table 3. 17. Common mode buffer Offset voltage results with 300-points based Monte Carlo Simulation (Process variations + mismatch)

Sr. No	Temperature (°C)/ VDD (V)	3.0	3.3	3.6
1	0	Offset Data (in mV): Min = -9.251 Max = 12.1 Mean = 1.406 σ = 3.837	Offset Data (in mV): Min = -8.073 Max = 13.35 Mean = 2.614 σ = 3.847	Offset Data (in mV): Min = -6.998 Max = 14.49 Mean = 3.713 σ = 3.857
2	27	Offset Data (in mV): Min = -9.118 Max = 12.34 Mean = 1.596 σ = 3.862	Offset Data (in mV): Min = -7.927 Max = 13.63 Mean = 2.824 σ = 3.872	Offset Data (in mV): Min = -6.834 Max = 14.79 Mean = 3.941 σ = 3.881
3	50	Offset Data (in mV): Min = -9.014 Max = 12.59 Mean = 1.765 σ = 3.886	Offset Data (in mV): Min = -7.802 Max = 13.88 Mean = 3.008 σ = 3.896	Offset Data (in mV): Min = -6.698 Max = 15.06 Mean = 4.139 σ = 3.906

3.7.5.3.1 ADC Simulation Results with Real Common Mode Buffer

In Verilog-A based ADC, the ideal voltage source was replaced with the real common mode buffer. Besides common mode buffer, input buffer, delay-cell, SAR logic with auxiliary cells, CDAC, switches, comparator and SR-latch are also real. All other components are still Verilog-A based for this simulation. The aim is to verify the ADC performance with the real delay-cell and optimize its performance if needed. Figure 3.72 shows the PSD of the ADC, which shows a fully satisfactory performance (ENOB and SNDR) of the ADC with real common mode buffer.

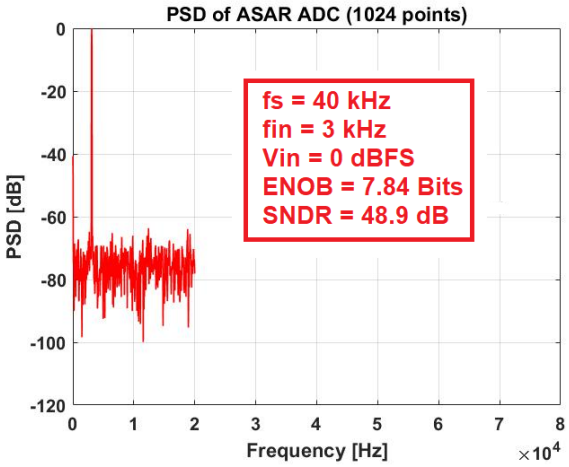


Figure 3. 72. ASAR ADC PSD Plot with real common mode buffer, input buffer, SAR logic and auxiliary cells, comparator, SR-latch, CDAC and switches; all other components are Verilog-A based.

3.7.5.3.2 Layout of Common Mode Buffer

The layout of common mode buffer is displayed in Figure 3.73, which is based on stacked layout design methodology. It consists of three stacks: 2 stacks for the NMOS devices, and one stack for the PMOS devices. Besides interdigitated structure for better matching, dummy devices are part of the design to compensate for the boundary conditions.

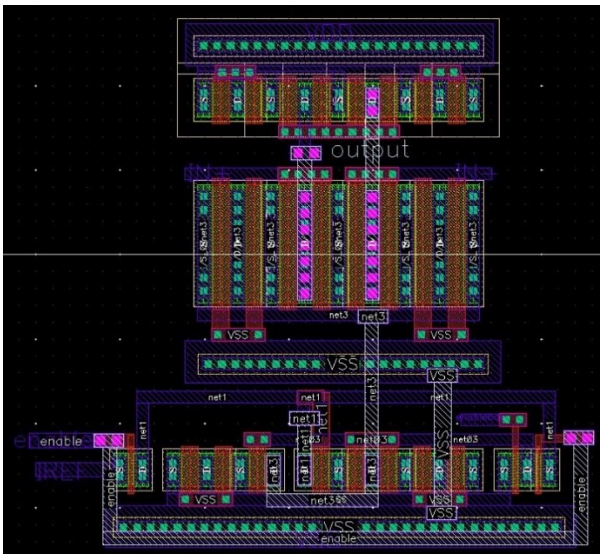


Figure 3. 73. Layout of V_{CM} buffer.

3.7.5.4. Voltage References Buffer Design

The first step in the design of voltage reference buffers design is to derive their specifications using analytical method according to the ADC requirements, which can act as a starting point for the buffers design. These parameters can then be optimized with the help of the simulations. The main specification parameters include voltage settling time, slew-rate, unity gain frequency, and DC gain. As the requirements for the upper and lower voltage buffers (V_{REFP} and V_{REFN}) are the same, so the following derivation process is valid for both of these voltage buffers.

3.7.5.4.1. Buffer output Voltage Settling Time (t_s)

The approximate clock period (T_{clk}) of asynchronous clock (CLK_{int}) is given below (for calculations purpose):

$$\mathrm{T_{clk}} = 2.4\ \mu\mathrm{s}$$

To ensure proper settling for the buffer's output voltage, its settling time ($t_{settling}$) has been calculated by:

$$\mathrm{t_{settling}} = \frac{\mathrm{T_{clk}}}{4} = 0.6\ \mu\mathrm{s}$$

Keeping in my mind the settling nature of the buffer's output (Figure 3.74), $t_{ssettling}$ can be divided into 2 parts: constant slope region (slewing) and linear (almost) settling region. As linear settling takes longer time than the constant slop, a better approximation is to allocate 10 % of the total buffer settling time (t) to slewing region and 90 % to linear slope region. This approximation has been taken for calculation purposes. In other words,

(a) Constant slop (slewing) settling time = 10 % ($t_{settling}$)

(b) Linear settling time = 90 % ($t_{settling}$)

(a) will give us the slew-rate, and (b) will provide us with the unity-gain frequency of the voltage buffer.

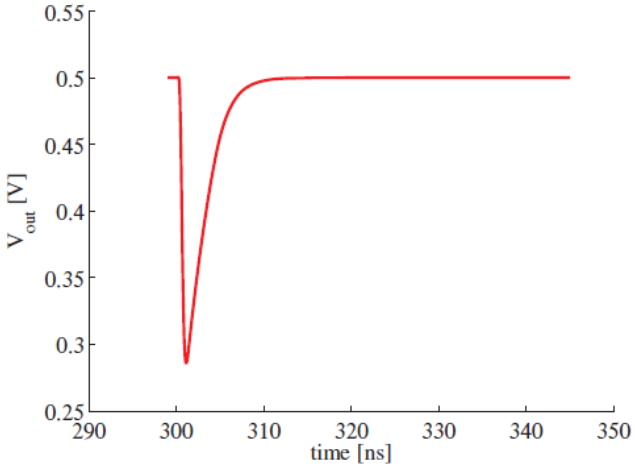


Figure 3. 74. Settling nature of Voltage reference buffer, taken from [241]. Slew rate settling time can be ignored for the reference voltage buffers because of charge redistribution nature of CDAC.

3.7.5.4.2. Slew Rate of Reference Voltage Buffers

To calculate the slew rate, first we need to calculate the worst-case output settling of the reference voltage buffers for the CDAC. Which is depicted in Figure 3.75.

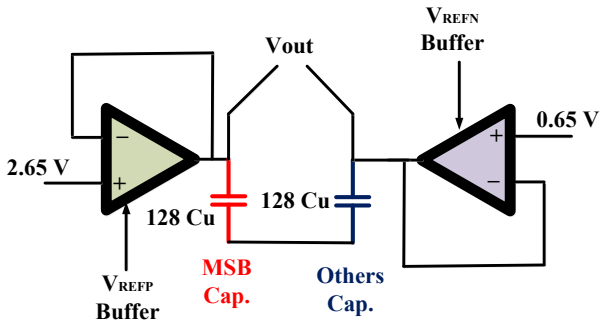


Figure 3. 75. Worst-case settling condition of reference voltage buffers outputs for the CDAC.

Based on charge conservation, the change in output voltage for this worst case can be calculated as follows:

$$\Delta V_{out} = \frac{V_{REFP} - V_{REFN}}{2} = 1\ V$$

So,

$$\text{Slew rate} = \frac{\Delta V_{out}}{t_{slew}} = \frac{1}{(0.1)(0.6u)} = 16.67\ V/\mu s$$

However, slew rate is not important for the voltage reference buffers because of the charge redistribution operation of CDAC. The settling is determined by the unity gain frequency. Based on this observation, we may simply ignore the slew rate or assume a lower value for calculation purposes. Let us assume that:

$$\text{Slew rate (selected)} = 1.56\ V/\mu s$$

Also,

$$\text{Slew rate(selected)} = \frac{\Delta V_{out}}{t_{slew}} = \frac{I_{out,min}}{C_L}$$

Where $C_L = 1/2.\, C_{DAC} = 2.56\ pF$

Thus,

$$I_{out,min} = 4\ \mu A$$

3.7.5.4.3. Unity Gain Frequency of Reference Voltage Buffers

Step response for a single pole amplifier in a closed loop configuration is given by:

$$V_{out}(t) = V_{step}(1 - e^{-t/\tau})$$

Here,

$$\tau = \frac{1}{(\beta)(2\pi f_{ug})}$$

For unity feedback configuration, β=1.

The settling error is given by:

$$\varepsilon = e^{-t/\tau}$$

Based on above,

$$f_{ug} = \frac{-\ln(\varepsilon)}{2\pi t}$$

For 10-bits settling (to be on safer side),

$$f_{ug} = 2 \text{ MHz}$$

3.7.5.4.4. DC Gain (A_0) of Reference Voltage Buffers

The gain-error factor due to finite open loop DC gain in closed loop configuration,

$$\text{Gain error factor} = \frac{1}{A_0\beta} = \frac{1}{A_0}$$

Accepting 0.5 % error, we get,

$$A_0 = 200 = 46 \text{ dB}$$

Table 3.18 summarizes the derived specification parameters for voltage reference buffers.

Table 3. 18. A Summary of Specifications of Reference Voltage Buffers (V_{REFP} and V_{REFN}) derived analytically

Sr. No.	Parameter	Calculated Value
1.	Time period of Asynchronous Clock	2.4 µs
3.	Buffer voltage Settling Time (t_s)	0.6 µs
3.	V_{DD}	3.3 V
4.	DC Gain	46 dB
5.	C_L=1/2. C_{DAC}	2.56 pF
6.	Slew Rate (SR)	1.56 V/µs
7.	GBW	2 MHz
8.	I_{REF}	~ 4 µA
9.	Offset	Temperature independent
10.	Input noise	< ¼ LSB

3.7.5.5. Upper Voltage Reference (V_{REFP}) Buffer Design

A common source with active load (with NMOS input pair) OP-AMP topology has been chosen for V_{REFP} buffer. Figure 3.76 shows the circuit diagram of the OP-AMP. Transistor dimensions have been calculated as follows.

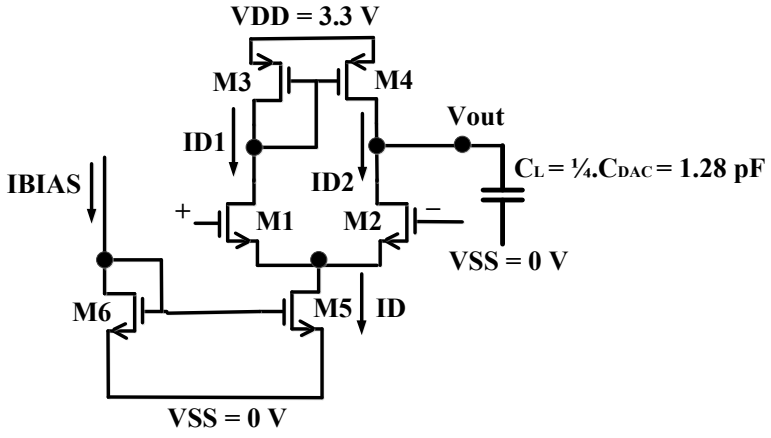


Figure 3. 76. Schematic diagram of open-loop CS differential amplifier selected for V_{REFP} buffer.

Let, $C_L = 1.28\ pF$

For the circuit, following relationship can be written,

$$GBW = \frac{g_{m1,2}}{2\pi C_L}$$

$$GBW = \frac{1}{0.6\mu}$$

Thus,

$$g_{m1,2} = 67\ \mu A/V$$

$$g_{m1,2} = \frac{2I_{D1}}{V_{OV}}$$

Let, $V_{OV} = 0.1\ V$

$$V_{gs1} = 0.8\ V$$

$$I_{D1} = 4\ \mu A$$

For M_1 and M_2,

$$(W/L)_{1,2} = \frac{2I_D}{u_p C_{ox}(V_{OV})^2} = 4.25 = 4$$

For M_5, and M_6,

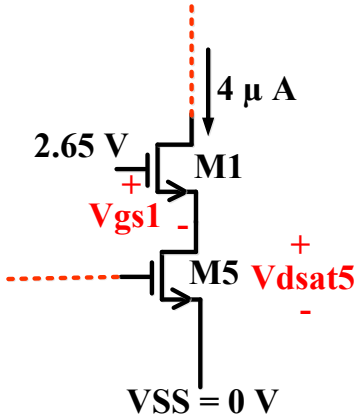


Figure 3. 77. Part of V_{REFP} buffer schematic for calculation of M_5 and M_6 aspect ratios.

From Figure 3.77,

$$2.65\ V > V_{gs1} + V_{dsat5}$$

$$V_{dsat5} < 1.85\ V$$

Let, $V_{dsat5} = 0.15\ V$

Then,

$$I_{D5,6} = \frac{1}{2} u_n C_{ox} (\frac{W}{L})_5 (V_{dsat5})^2$$

$$(\frac{W}{L})_5 = 2$$

Let,

$$(\frac{W}{L})_6 = 2$$

For M_3, and M_4,

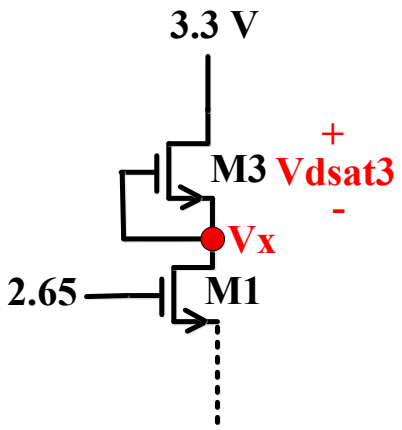


Figure 3. 78. Part of V_{REFP} buffer schematic for calculation of M_3 and M_4 aspect ratios.

From Figure 3.78,

$$V_x > 2.65 - 0.2 \text{ V}$$

$$V_x > 2.45 \text{ V}$$

Let $$V_x = 3.1 \text{ V}$$

Then, $$V_{dsat3} = 3.3 - 3.1 = 0.2 \text{ V}$$

$$I_{D3,4} = \frac{1}{2} u_n C_{ox} (\frac{W}{L})_{3,4} (V_{dsat3})^2$$

$$(\frac{W}{L})_{3,4} = 4$$

With these analytical values, the circuit was simulated for verification. Table 3.19 summarizes the achieved results of the designed buffer, which clearly shows that all the initially set specifications are fulfilled. In addition, Monto Carlo (mismatch and process variations) simulations results (shown in Figure 3.81-3.89, summarized in Table 3.20) validate circuits performance with respect to PVT variations. In addition, the input offset of the buffer is independent of temperature, as desired. PSRR plots (Figure 3.80) display satisfactory response for a single ended architecture.

To enable the turn on and off capability of the buffer, three switches (S_1-S_3) have been added in the circuit. These switches are directly driven by the external Enable signal. When this signal is high, the buffer is on.

It is off when the Enable signal is low. This enables sampling-rate reconfigurability functionality of the ADC, where desired number of these buffers can be turned on externally. Figure 3.79 shows the final schematic of the buffer with the switches.

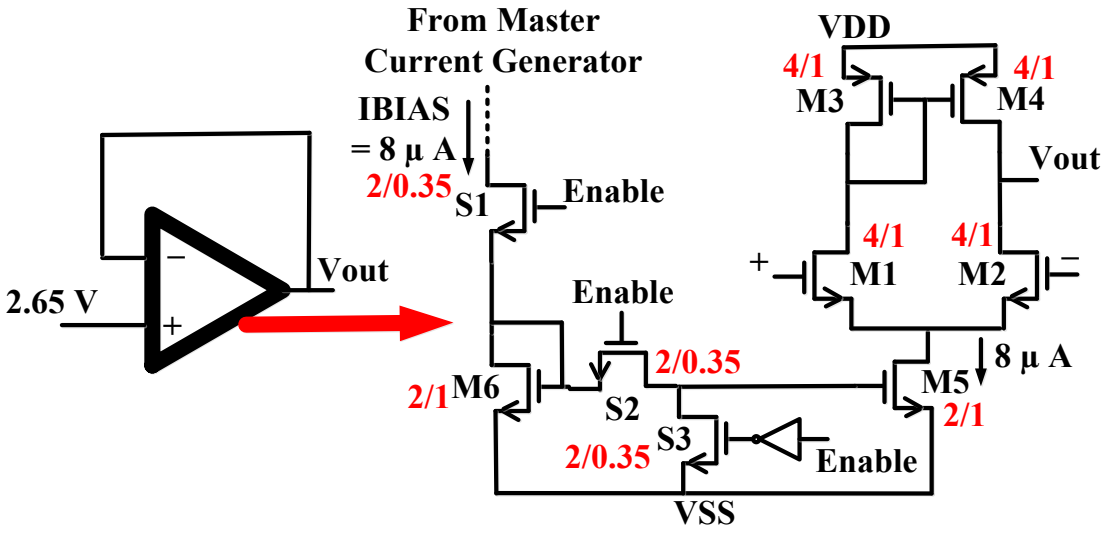
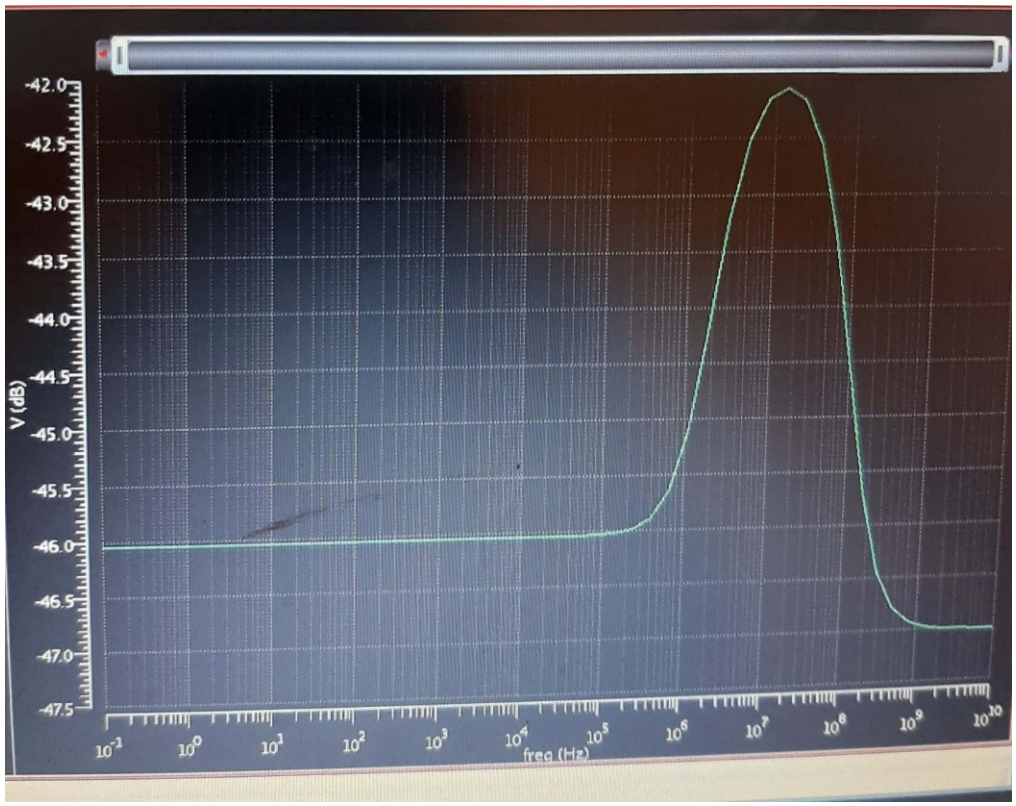


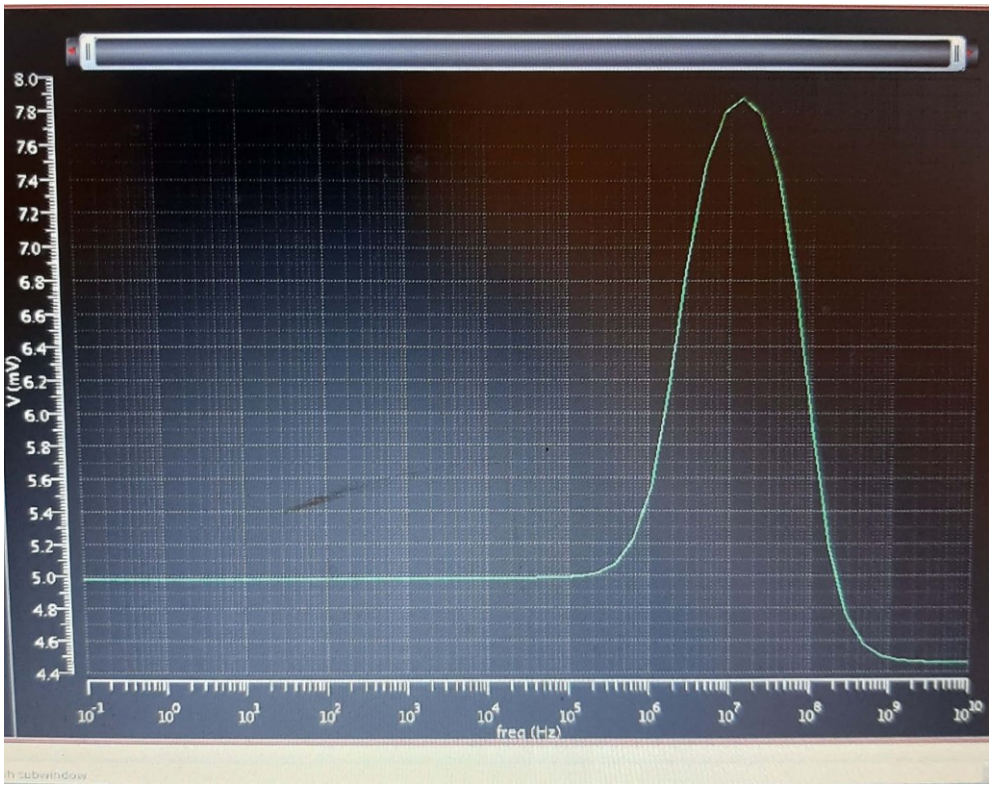
Figure 3. 79. V_{REFP} buffer with schematic diagram of its OP-AMP.

Table 3. 19. Specifications and Results of V_{REFP} Buffer

Sr. No.	Parameter	Value
1.	I_{REF} (µA)	8
2.	C_L(pF)	1.28 ($C_{DAC}/4$)
3.	Loop Gain (dB)	46
4.	Total summarized noise (µV)	600 (< ¼ LSB)
5.	Input-referred noise (mV)	2.1
6.	Bandwidth (MHz)	2.57
7.	Systematic Offset/Gain error (mV)	7.2 (~ 1 LSB) (Given in table)
8.	Settling Time (µs)	0.4
9.	PSRR	-46 dB/4.99 mV



(a)



(b)

Figure 3. 80. PSRR plots of V_{REFP} buffer.

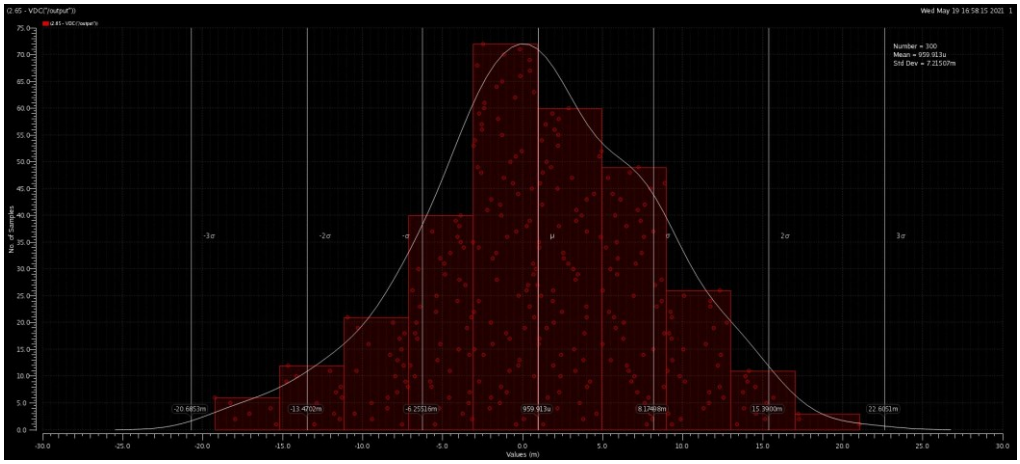


Figure 3. 81. Monte Carlo (mismatch + process variations) simulation result of V_{REFP} buffer offset voltage at $V_{DD} = 3.3\ V$ and T= 0 °C.

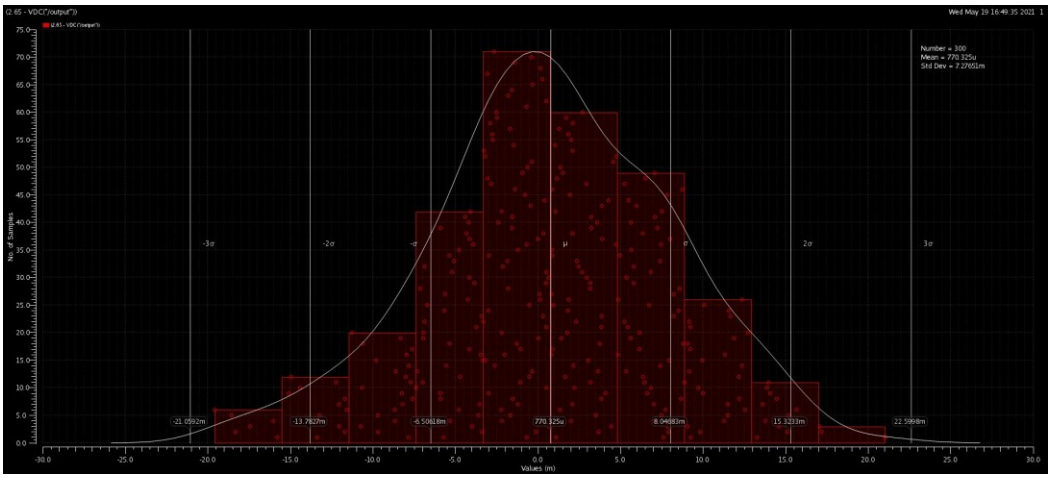


Figure 3. 82. Monte Carlo (mismatch + process variations) simulation result of V_{REFP} buffer offset voltage at $V_{DD} = 3.3\ V$ and T= 27 °C.

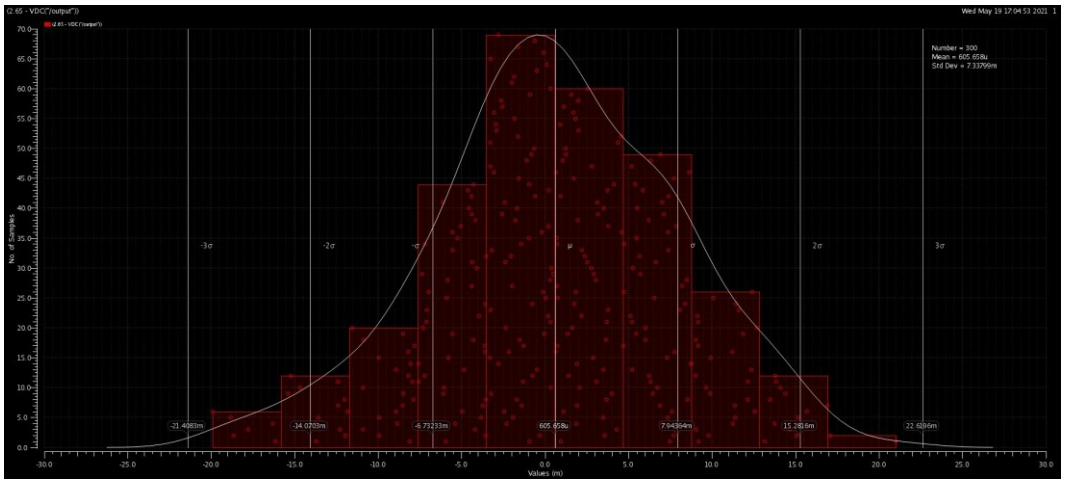


Figure 3. 83. Monte Carlo (mismatch + process variations) simulation result of V_{REFP} buffer offset voltage at $V_{DD} = 3.3\ V$ and T= 50 °C.

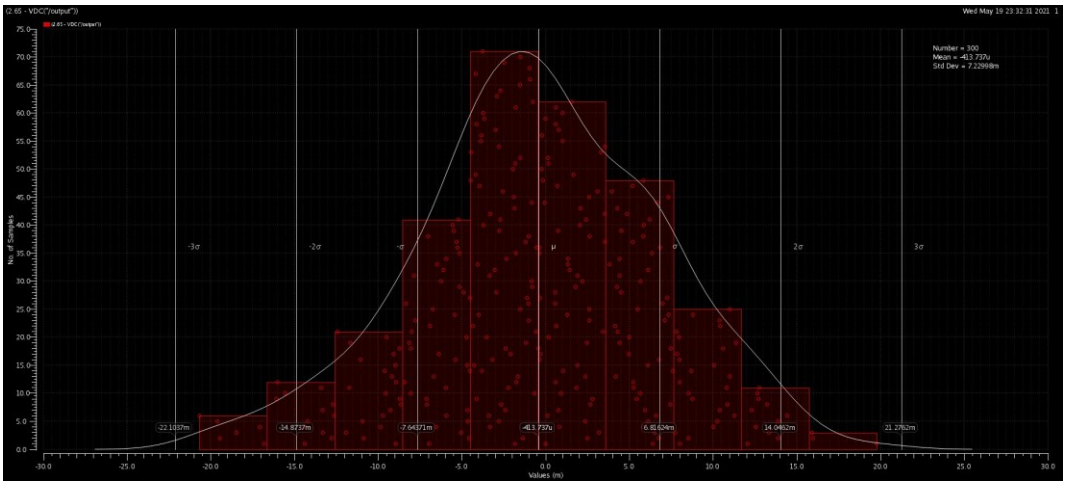


Figure 3. 84. Monte Carlo (mismatch + process variations) simulation result of V_{REFP} buffer offset voltage at $V_{DD} = 3.6\ V$ and T= 0 °C.

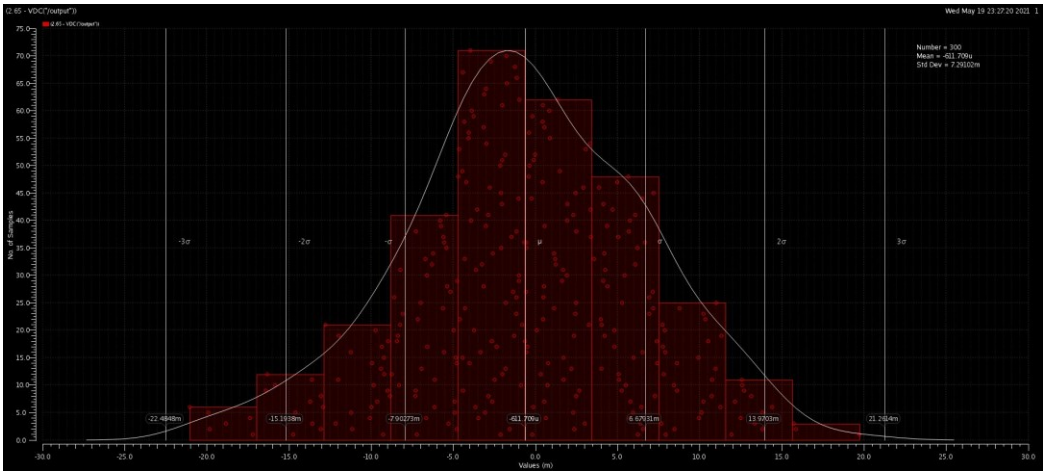


Figure 3. 85. Monte Carlo (mismatch + process variations) simulation result of V_{REFP} buffer offset voltage at $V_{DD} = 3.6\ V$ and T= 27 °C.

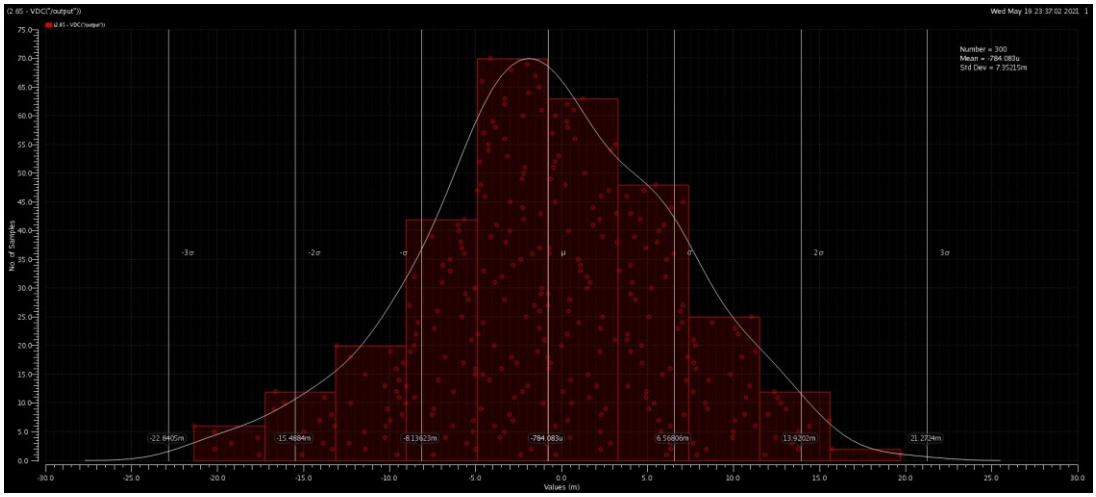


Figure 3. 86. Monte Carlo (mismatch + process variations) simulation result of V_{REFP} buffer offset voltage at $V_{DD} = 3.6\ V$ and T= 50 °C.

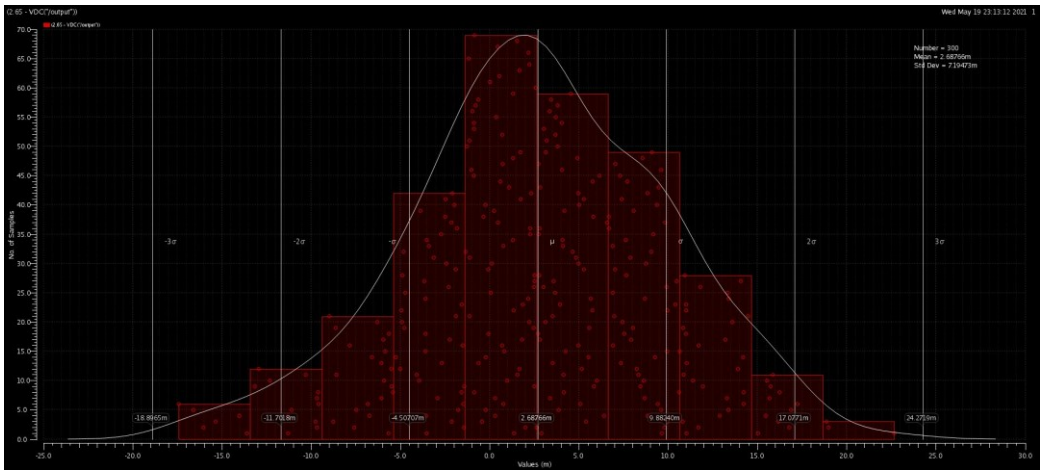


Figure 3. 87. Monte Carlo (mismatch + process variations) simulation result of V_{REFP} buffer offset voltage at $V_{DD} = 3.0\ V$ and T= 0 °C.

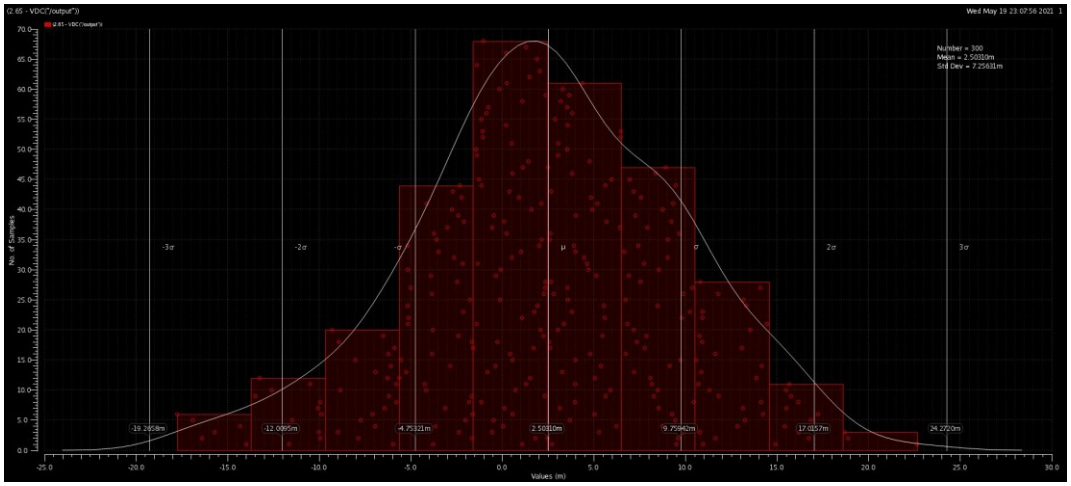


Figure 3. 88. Monte Carlo (mismatch + process variations) simulation result of V_{REFP} buffer offset voltage at $V_{DD} = 3.0\ V$ and T= 27 °C.

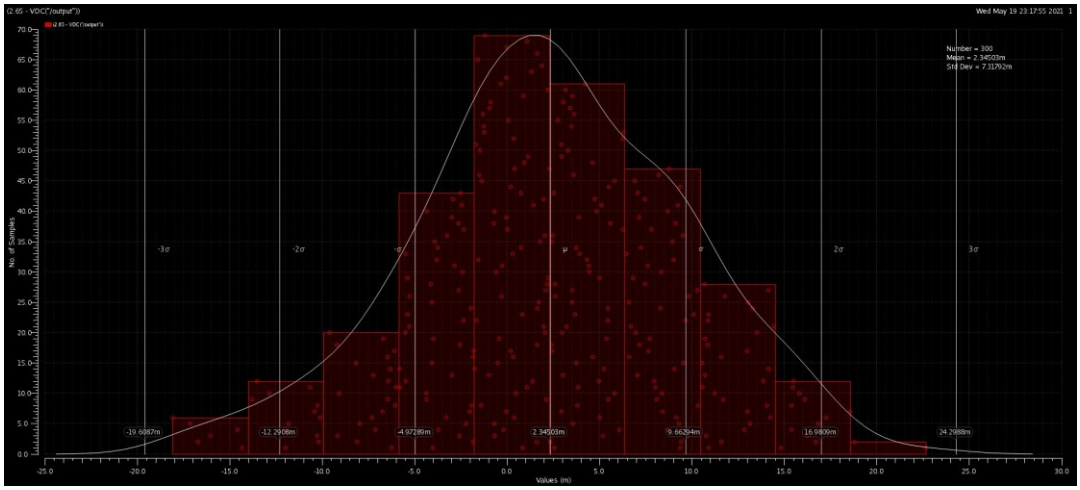


Figure 3. 89. Monte Carlo (mismatch + process variations) simulation result of V_{REFP} buffer offset voltage at $V_{DD} = 3.0\ V$ and T= 50 °C.

Table 3. 20. Offset voltage results of V_{REFP} buffer with 300-points based Monte Carlo Simulation (Process variations + mismatch)

Sr. No	Temperature (°C)/ VDD (V)	3.0	3.3	3.6
1	0	Offset Data (in mV): Min = -17.42 Max = 22.68 Mean = 2.688 σ = 7.195	Offset Data (in mV): Min = -19.23 Max = 21.09 Mean =0.959 σ = 7.215	Offset Data (in mV): Min = -20.67 Max = 19.78 Mean = -0. 414 σ = 7.23
2	27	Offset Data (in mV): Min = -17.76 Max = 22.66 Mean = 2.503 σ = 7.256	Offset Data (in mV): Min = -19.58 Max = 21.06 Mean =0.77 σ = 7.277	Offset Data (in mV): Min = -21.04 Max = 19.75 Mean = -0. 611 σ = 7.291
3	50	Offset Data (in mV): Min = -18.08 Max = 22.66 Mean = 2.345 σ = 7.318	Offset Data (in mV): Min = -19.9 Max = 21.05 Mean =0.605 σ = 7.338	Offset Data (in mV): Min = -21.36 Max = 19.74 Mean = -0. 838 σ = 7.352

3.7.5.5.1. ADC Simulation Results with Real V_{REFP} Buffer

In Verilog-A based ADC, the ideal voltage source was replaced with the real V_{REFP} buffer. Besides V_{REFP} buffer, input buffer, delay-cell, SAR logic with auxiliary cells, CDAC, switches, comparator and SR-latch are also real. All other components are still Verilog-A based for this simulation. The aim is to verify the ADC performance with the real delay-cell and optimize its performance if needed. Figure 3.90 shows the PSD of the ADC, which shows a fully satisfactory performance (ENOB and SNDR) of the ADC with real buffer.

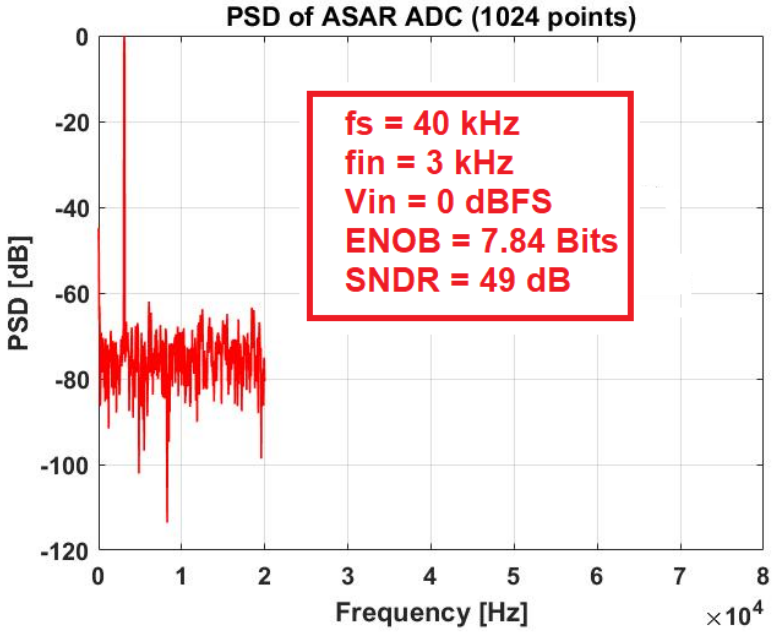


Figure 3. 90. ASAR ADC PSD plot with real V_{REFP} buffer, common mode buffer, input buffer, comparator, SR-latch, CDAC and switches; all other components are Verilog-A based.

3.7.5.5.2. Layout of V_{REFP} Buffer

Stacked transistors-based layout of V_{REFP} buffer is shown in Figure 3.91. It consists of 3 stacks: 2 for NMOS devices, and 1 for PMOS devices. Dummy devices are introduced to compensate for the boundary conditions.

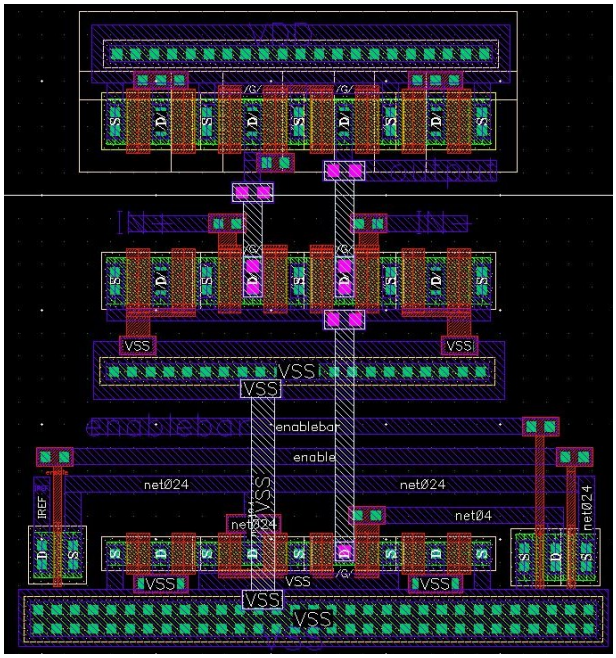


Figure 3. 91. Layout of V_{REFP} buffer.

3.7.5.6. Lower Voltage Reference (V_{REFN}) Buffer Design

Figure 3.92 shows the circuit diagram of the OP-AMP for the V_{REFN} buffer. A common source with active load (with PMOS input pair) OP-AMP topology has been chosen. Transistor dimensions have been calculated as follows.

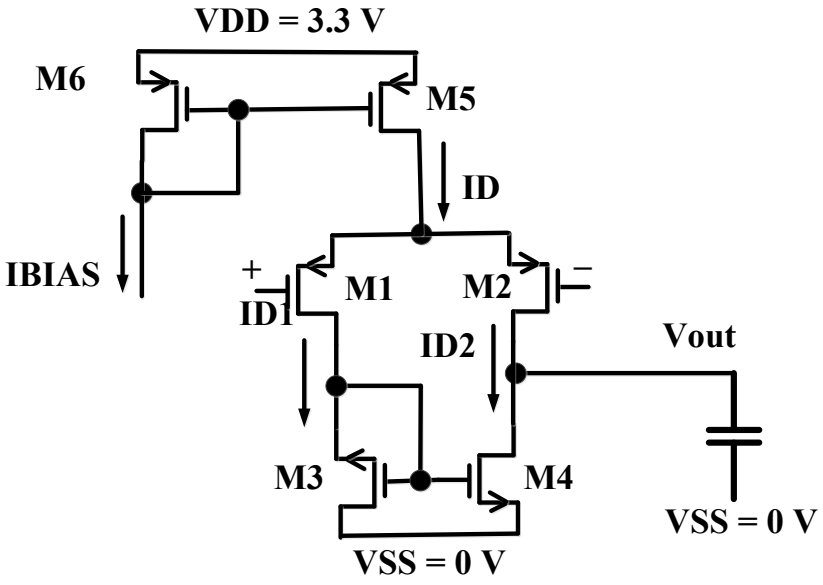


Figure 3. 92. Schematic diagram of open-loop CS differential amplifier selected for V_{REFN} buffer.

Let, $C_L = 1.28\ pF$

For the circuit, following relationship can be written:

$$GBW = \frac{g_{m1,2}}{2\pi C_L}$$

$$GBW = \frac{1}{0.6\mu}$$

Thus,

$$g_{m1,2} = 67\ \mu A/V$$

$$g_{m1,2} = \frac{2I_{D1}}{V_{OV}}$$

Let, $V_{OV} = 0.2\ V$

$$V_{gs1} = 0.9\ V$$

$$I_{D1} = 4\ \mu A$$

For M_1 and M_2,

$$(W/L)_{1,2} = \frac{2I_D}{u_p C_{ox}(V_{OV})^2} = 8$$

For M_5 and M_6,

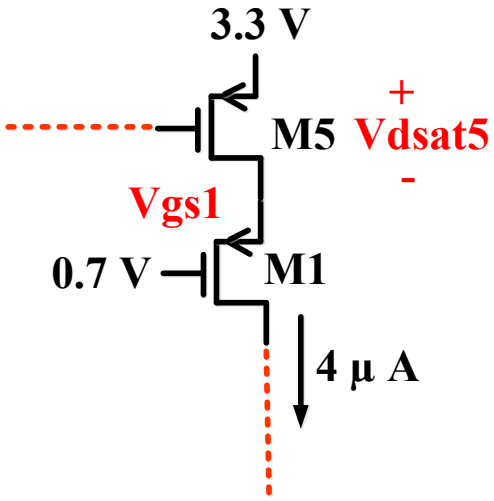


Figure 3. 93. Part of common mode buffer schematic for calculation of M_5 and M_6 aspect ratios.

From Figure 3.93,

$$0.7\ V > |V_{gs1}| + |V_{dsat5}|$$

$$|V_{dsat5}| < 1.6\ V$$

Let, $$|V_{dsat5}| = 0.15\ V$$

Then,

$$I_{D5,6} = \frac{1}{2} u_n C_{ox} (\frac{W}{L})_5 (|V_{dsat5}|)^2$$

$$(\frac{W}{L})_5 = 2$$

Let,

$$(\frac{W}{L})_6 = 2$$

For M_3 and M_4,

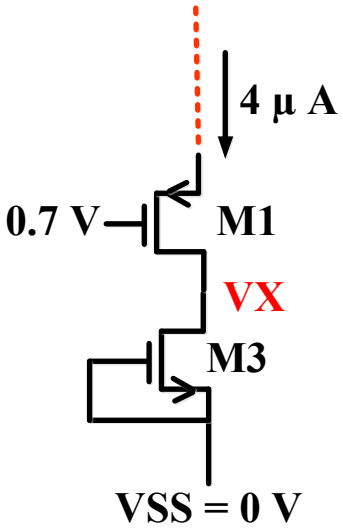


Figure 3. 94. Part of common mode buffer schematic for calculation of M_3 and M_4 aspect ratios.

From Figure 3.94,

$$|V_x| > 0.7 - 0.2\ V$$

Let, $$|V_x| > 0.5\ V$$

Let $$|V_x| = 3.1\ V$$

Then, $$|V_{dsat3}| = 3.3 - 3.1 = 0.2\ V$$

$$I_{D3,4} = \frac{1}{2} u_n C_{ox} (\frac{W}{L})_{3,4} (|V_{dsat3}|)^2$$

$$(\frac{W}{L})_{3,4} = 4$$

With these analytical values, the circuit was simulated for verification. Table 3.21 summarizes the achieved results of the designed buffer, which clearly show that all the initially set specifications are fulfilled. In addition, Monto Carlo (mismatch and process variations) simulations results (shown in Figure 3.98-Figure 3.106, summarized in Table 3.22) validate circuits performance with respect to PVT variations. In addition, the input offset of the buffer is independent of temperature, as desired. PSRR plots (Figure 3.96-3.97) display satisfactory response for a single ended architecture.

To enable the turn on and off capability of the buffer, three switches (S_1-S_3) have been added in the circuit. These switches are directly driven by the external Enable signal. When this signal is high, the buffer is on. It is off when the Enable signal is low. This enables sampling-rate reconfigurability functionality of the ADC, where desired number of these buffers can be turned on externally. Figure 3.95 shows the final schematic of the buffer with the switches.

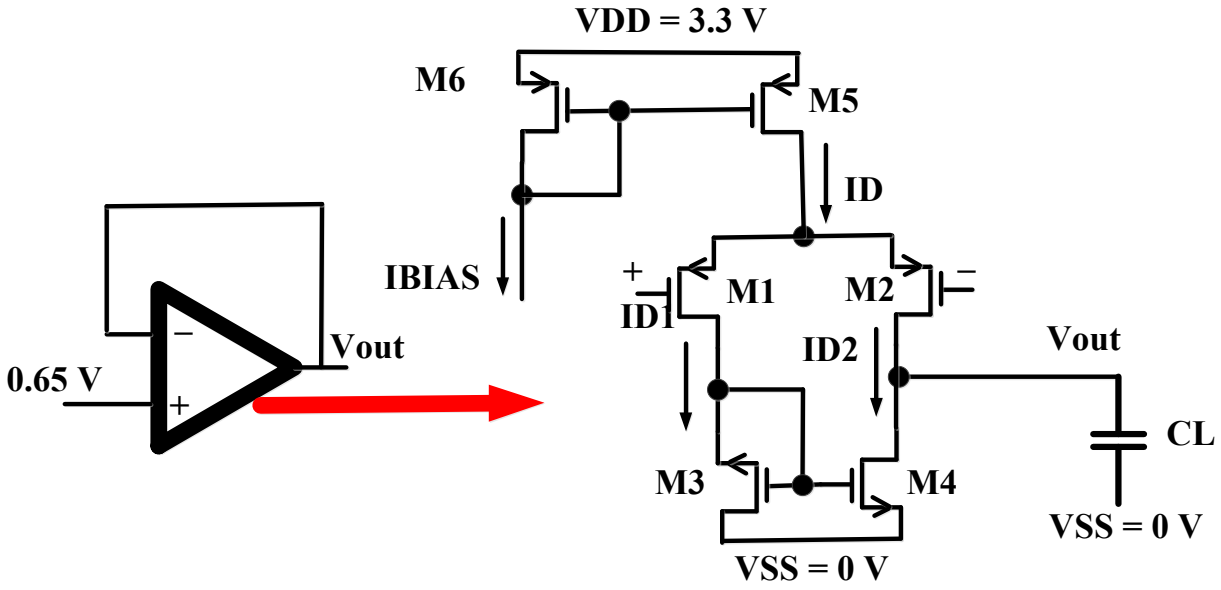


Figure 3. 95. V_{REFN} buffer with schematic diagram of its OP-AMP.

Table 3. 21. Specifications and Results of the designed V_{REFN} Buffer

Sr. No.	Parameter	Value
1.	I_{REF} (µA)	15
2.	C_L(pF)	5.12 (C_{DAC})
3.	Loop Gain (dB)	47
4.	Total summarized noise (µV)	381 (< ¼ LSB)
5.	Input-referred noise (mV)	0.8
6.	Bandwidth (MHz)	4
7.	Systematic Offset/Gain error (mV)	7.18
8.	Settling Time (µs)	0.25
9.	PSRR	-48.32 dB/3.87 mV

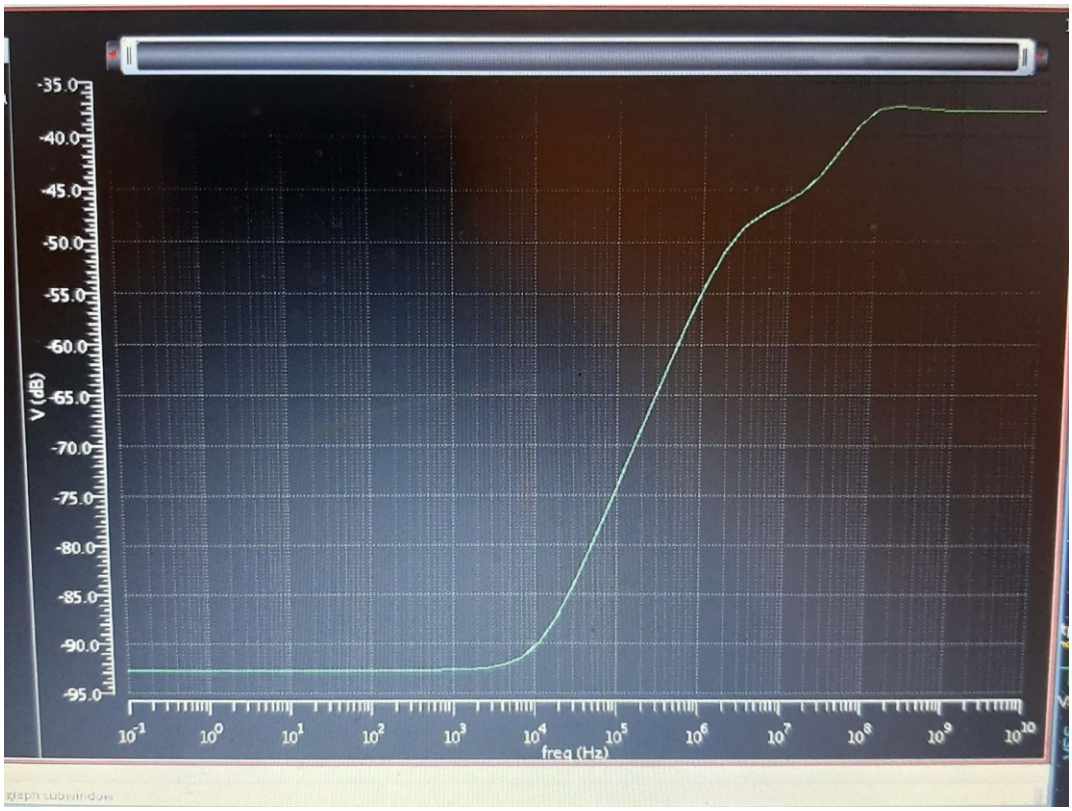


Figure 3. 96. PSRR plot of V_{REFN} buffer (dB).

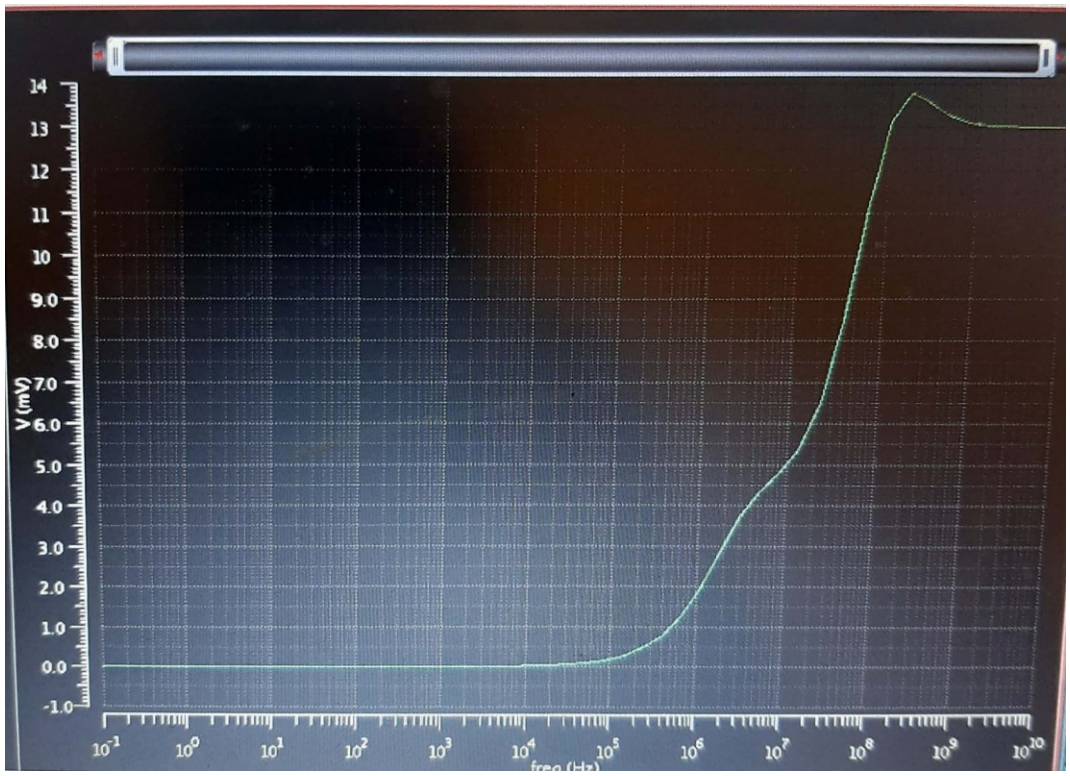


Figure 3. 97. PSRR plot of V_{REFN} buffer (dB).

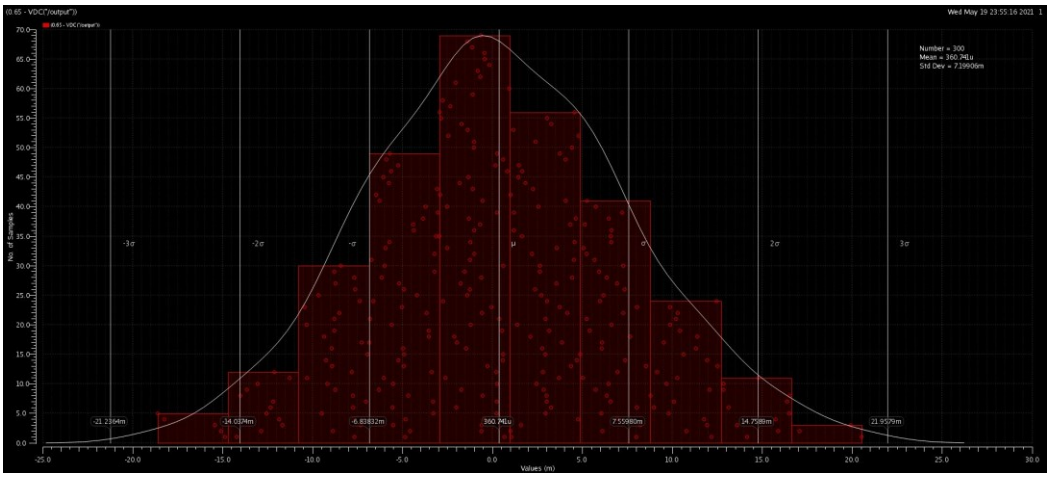


Figure 3. 98. Monte Carlo (mismatch + process variations) simulation result of V_{REFN} buffer offset voltage at $V_{DD} = 3.3\ V$ and T= 0 °C.

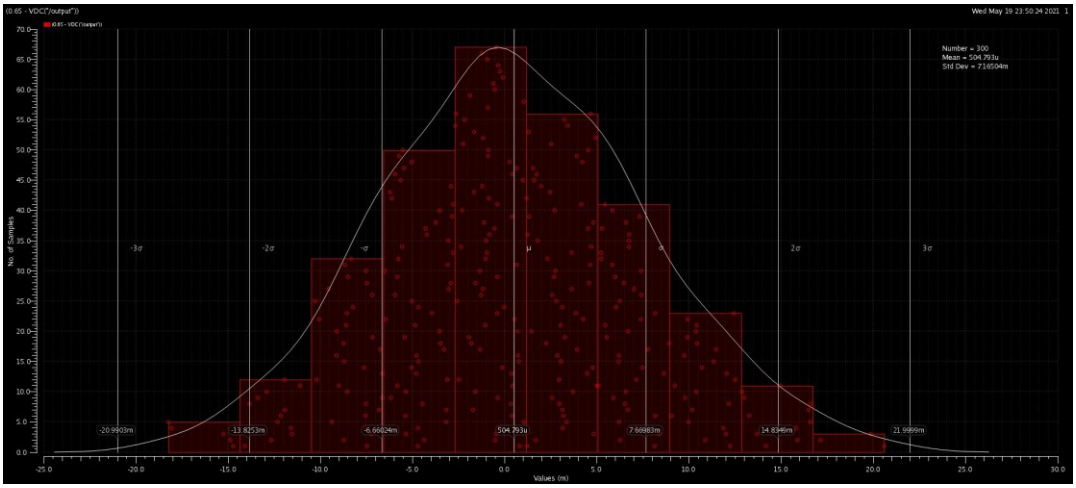


Figure 3. 99. Monte Carlo (mismatch + process variations) simulation result of V_{REFN} buffer offset voltage at $V_{DD} = 3.3\ V$ and T= 27 °C.

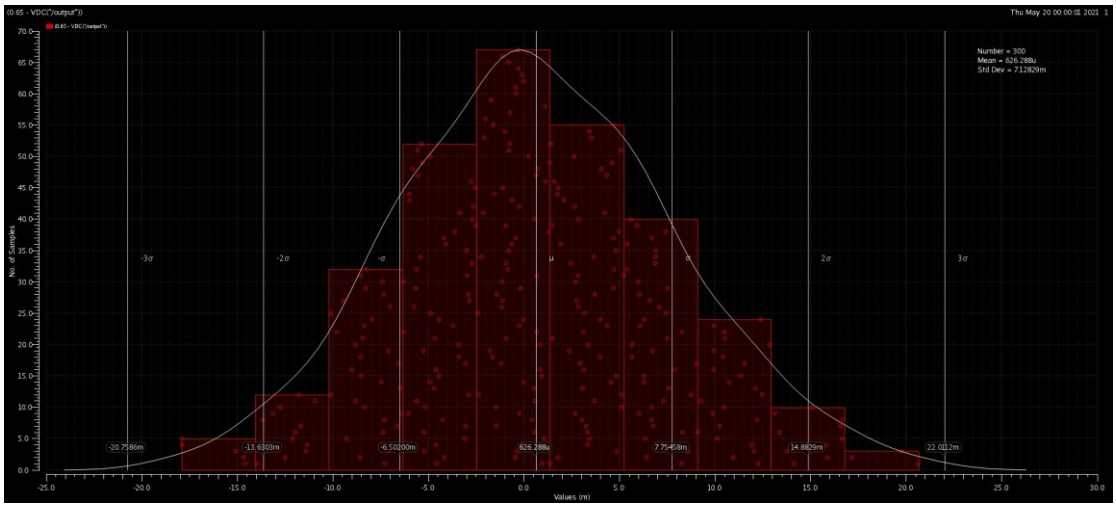


Figure 3. 100. Monte Carlo (mismatch + process variations) simulation result of V_{REFN} buffer offset voltage at $V_{DD} = 3.3\ V$ and T= 50 °C.

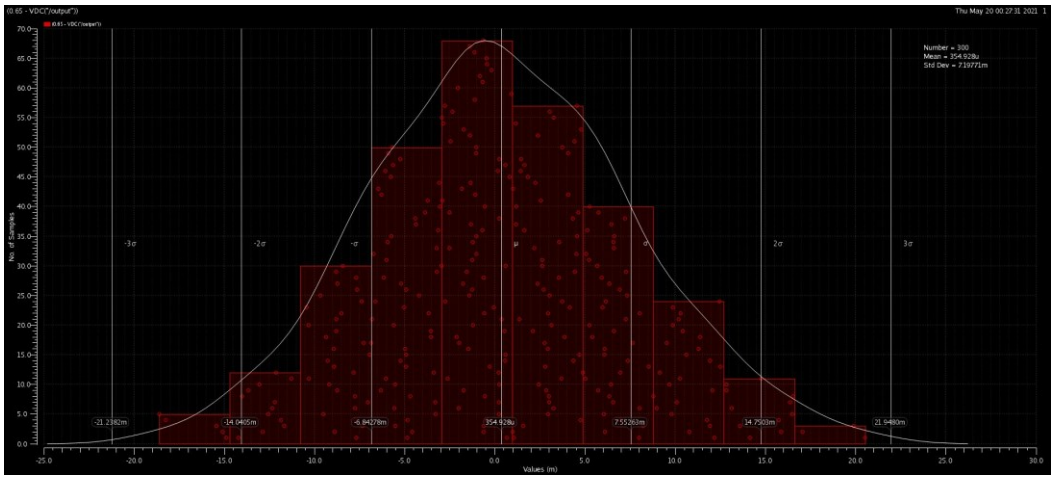


Figure 3. 101. Monte Carlo (mismatch + process variations) simulation result of V_{REFN} buffer offset voltage at $V_{DD} = 3.6\ V$ and T= 0 °C.

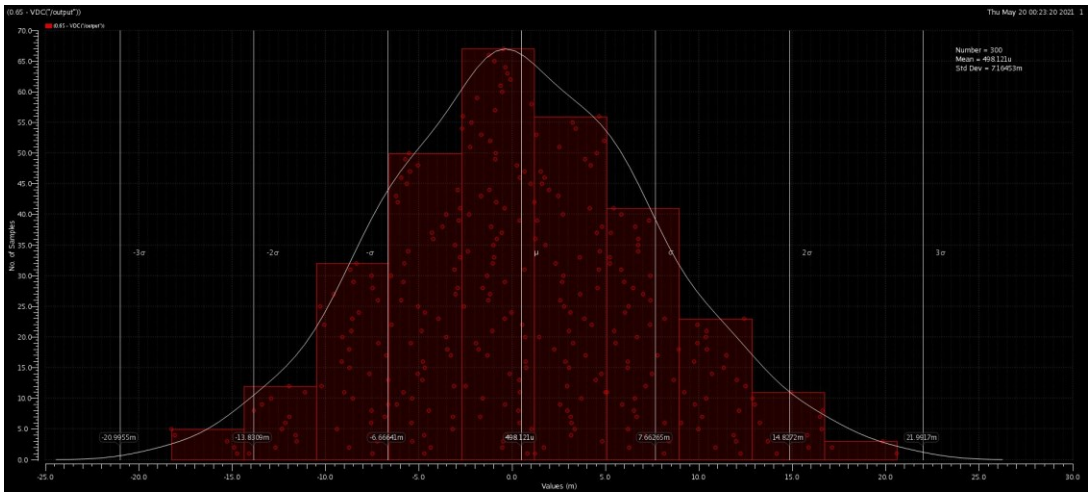


Figure 3. 102. Monte Carlo (mismatch + process variations) simulation result of V_{REFN} buffer offset voltage at $V_{DD} = 3.6\ V$ and T= 27 °C.

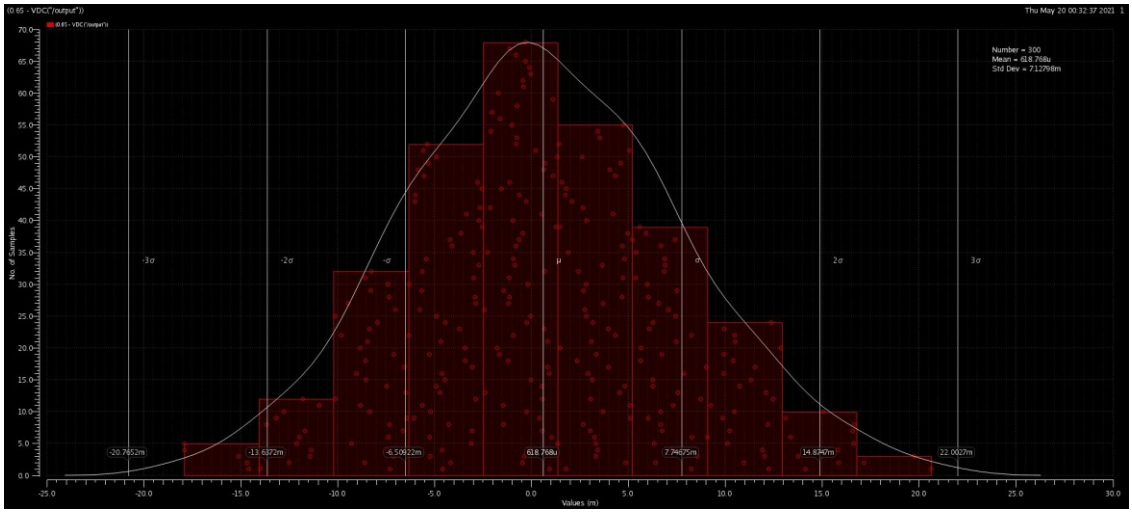


Figure 3. 103. Monte Carlo (mismatch + process variations) simulation result of V_{REFN} buffer offset voltage at $V_{DD} = 3.6\ V$ and T= 50 °C.

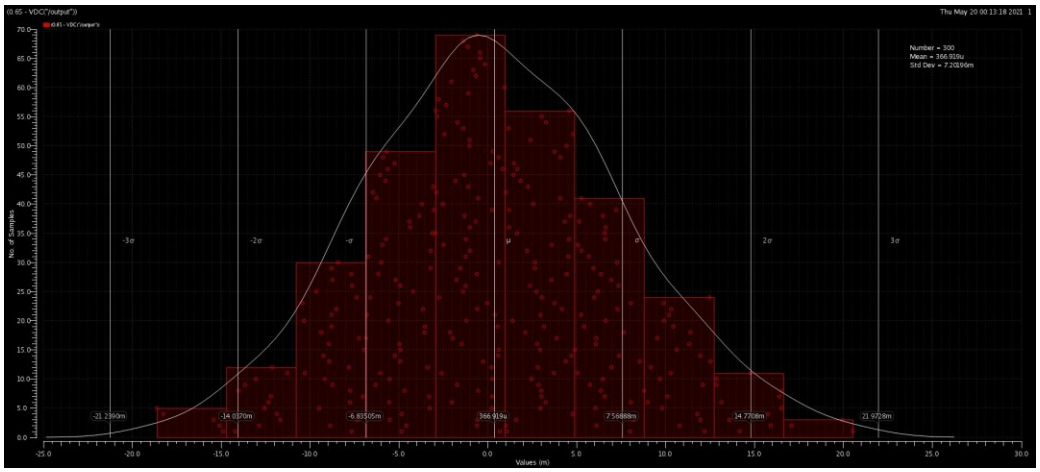


Figure 3. 104. Monte Carlo (mismatch + process variations) simulation result of V_{REFN} buffer offset voltage at $V_{DD} = 3.0\ V$ and T= 0 °C.

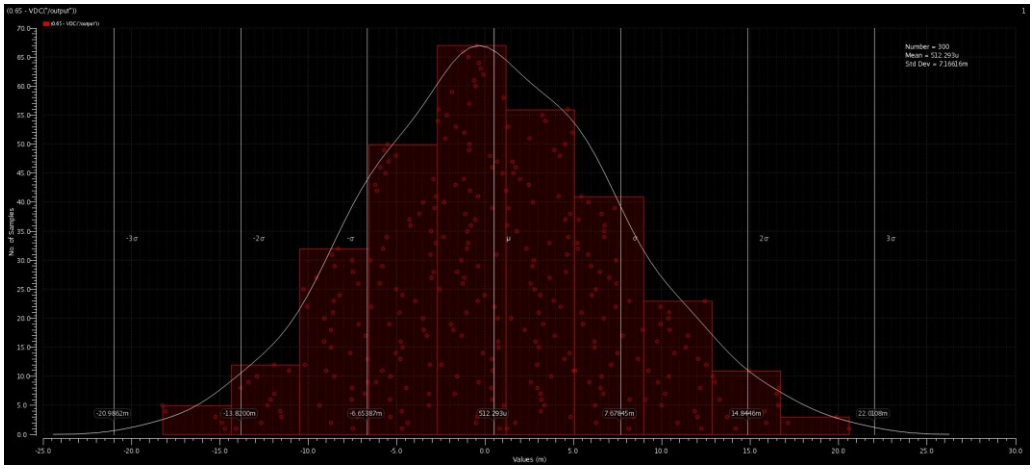


Figure 3. 105. Monte Carlo (mismatch + process variations) simulation result of V_{REFN} buffer offset voltage at $V_{DD} = 3.0\ V$ and T= 27 °C.

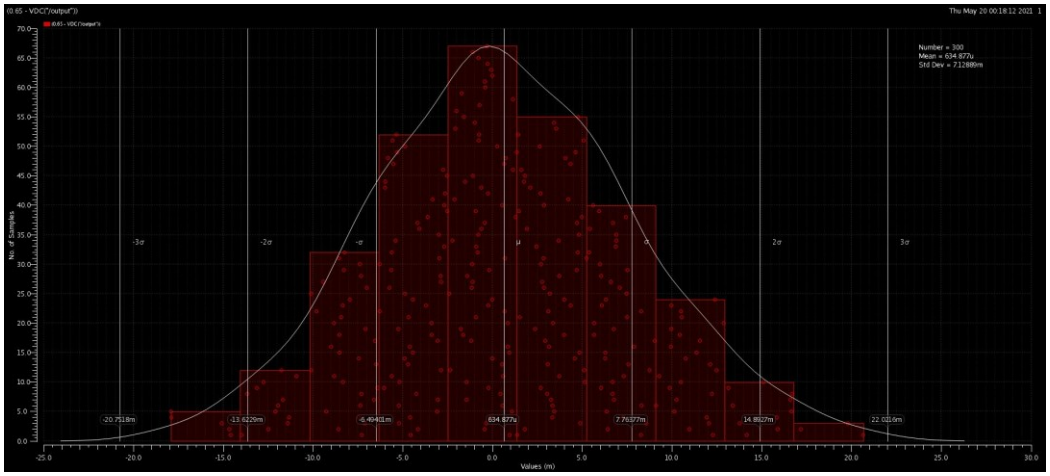


Figure 3. 106. Monte Carlo (mismatch + process variations) simulation result of V_{REFN} buffer offset voltage at $V_{DD} = 3.0\ V$ and T= 50 °C.

Table 3. 22. Offset voltage results with 300-points based Monte Carlo Simulation (Process variations + mismatch) results for V_{REFN} buffer

Sr. No	Temperature (°C)/ VDD (V)	3.0	3.3	3.6
1	0	Offset Data (in mV): Min = -18.62 Max = 20.55 Mean = .365 σ = 7.202	Offset Data (in mV): Min = -18.6 Max = 20.54 Mean = .360 σ = 7.199	Offset Data (in mV): Min = -18.6 Max = 20.54 Mean = .354 σ = 7.198
2	27	Offset Data (in mV): Min = -18.25 Max = 20.62 Mean = .512 σ = 7.166	Offset Data (in mV): Min = -18.25 Max = 20.61 Mean = .504 σ = 7.165	Offset Data (in mV): Min = -18.25 Max = 20.61 Mean = .498 σ = 7.165
3	50	Offset Data (in mV): Min = -17.91 Max = 20.66 Mean = .634 σ = 7.129	Offset Data (in mV): Min = -17.91 Max = 20.66 Mean = .626 σ = 7.128	Offset Data (in mV): Min = -17.91 Max = 20.65 Mean = .618 σ = 7.128

3.7.5.6.1. ADC Simulation Results with Real V_{REFN} Buffer

In Verilog-A based ADC, the ideal voltage source was replaced with the real V_{REFN} buffer. BesidesV_{REFN} buffer, V_{REFP} buffer, input buffer, delay-cell, SAR logic with auxiliary cells, CDAC, switches, comparator and SR-latch are also real. All other components are still Verilog-A based for this simulation. The aim is to verify the ADC performance with the real delay-cell and optimize its performance if needed. Figure 3.107 shows the PSD of the ADC, which shows a fully satisfactory performance (ENOB and SNDR) of the ADC with real V_{REFN} buffer.

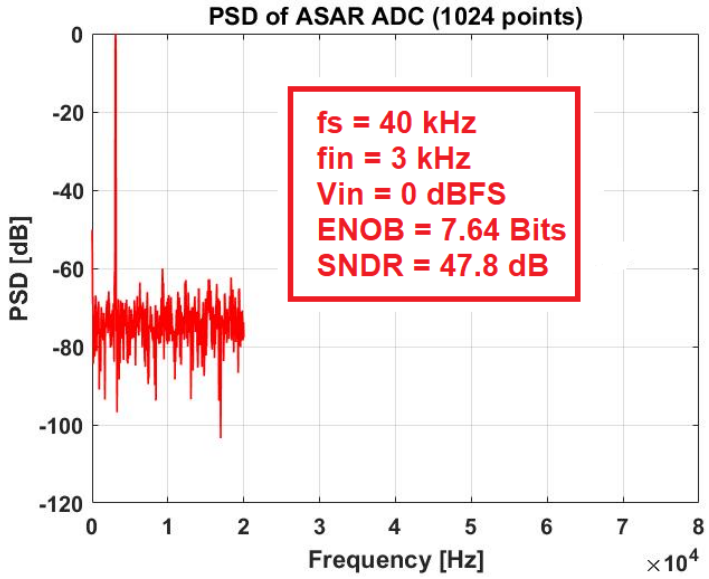


Figure 3. 107. ASAR ADC PSD plot with all real components including V_{REFN} buffer.

3.7.5.6.2. Layout of V_{REFN} Buffer

Following stacked transistor-based approach, layout of V_{REFN} buffer has been designed, which is shown in Figure 3.108. Out of three stacks, two belong to PMOS devices and one belongs to NMOS devices. Dummy devices are added at both sides of each stack to compensate for the boundary conditions.

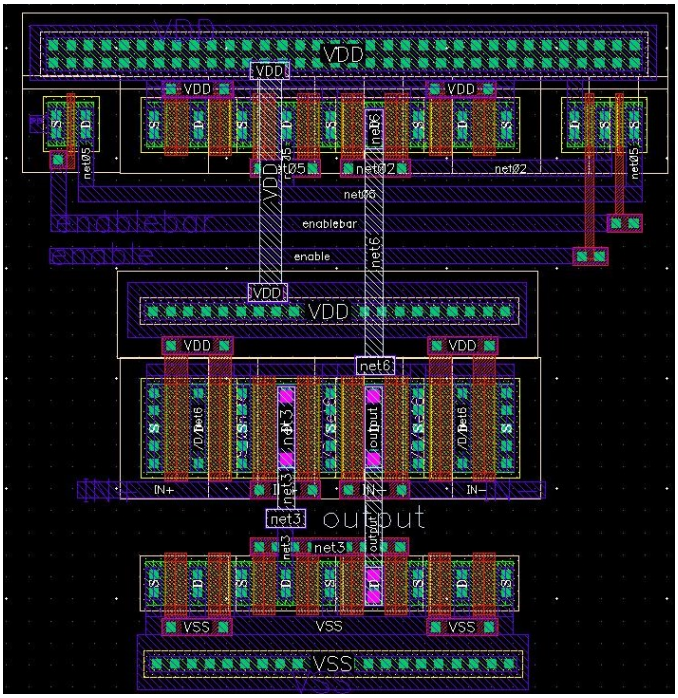


Figure 3. 108. Layout of V_{REFN} buffer.

3.7.5.6.3. Multiple V_{REFP} and V_{REFN} Buffers in parallel for Sampling-Rate Reconfigurability

As discussed in section 3.4, 8 voltage reference buffer slices of each type (V_{REFP} and V_{REFN}) with their control logic has been integrated on-chip to faciliatte sampling-rate reconfigurability of the ADC. Figure 3.109 shows the conceptural representation of 8 voltage referenc buffer slcies in paralell. With the external control, any number of these buffer slices can be turned on. Table 3.23 shows the number of buffers needed/turned on for different sampling-rates supported by the ADC. Besides enabling sampling-rate reconfigirablity, this aproach makes the ADC robust with respect to possible PVT variations. Layout of these buffers wih their control logic is shown in Figure 3.110.

Table 3. 23. No of voltage reference buffer slices needed for different sampling-rates of the ADC

Sr. No.	Sampling-rate (kHz)	No. of buffer slices needs to be ON
1.	40	1
2.	71.43	2
3.	100	3
4.	119	4
5.	131.58	5
6.	142.86	6
7.	153.85	7
8.	167	8

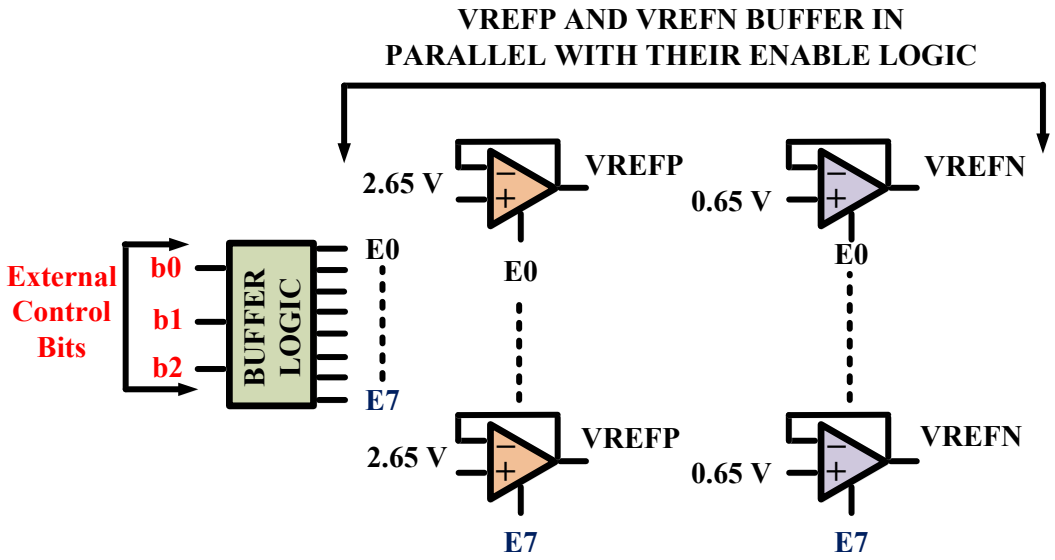


Figure 3. 109. Multiple (8 for this ADC) voltage reference buffer slices integrated in parallel with their external control to get sampling-rate reconfigurability.

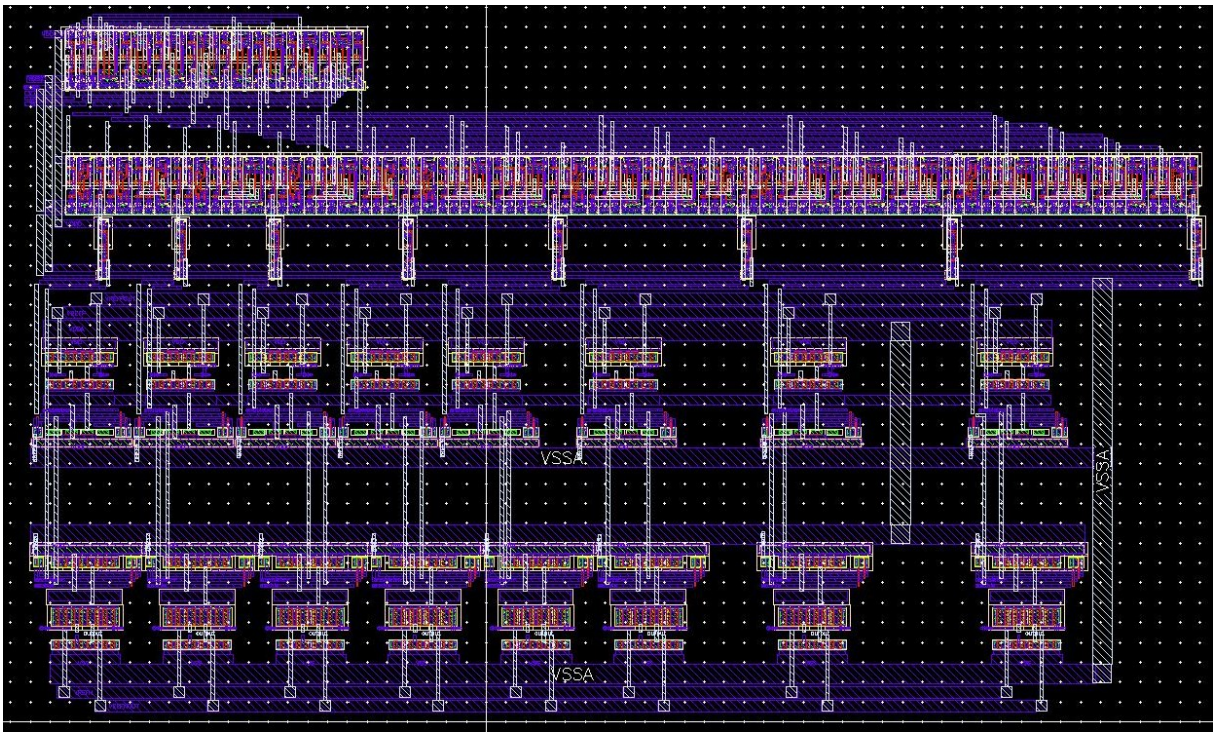


Figure 3. 110. Layout of 8 V_{REFN} and V_{REFP} buffers in parallel with their enable and disable logic.

3.7.5.7. Biasing Current generator Circuit

Biasing current generation for all the buffers as well as the comparator for the delay-cell needs to be designed. Cascode current mirror has been used as a bias current generator because of its high output resistance. Circuit diagram of the master bias circuit is shown in Figure 3.111 with all the currents generated. The input external bias current to the cascode current mirror circuit is chosen as 1 µA since

generating this current externally is convenient. The circuit has power down (PD) switches to facilitate its externa turn on and off functionality as per the need. Table 3.24 indicates the transistor sizes for the bias circuit. The layout of bias circuit is shown in Figure 3.112. To ensure matching, an interdigitated technique with stack approach has been used. Dummy devices have been used to ensure same boundary conditions for the devices.

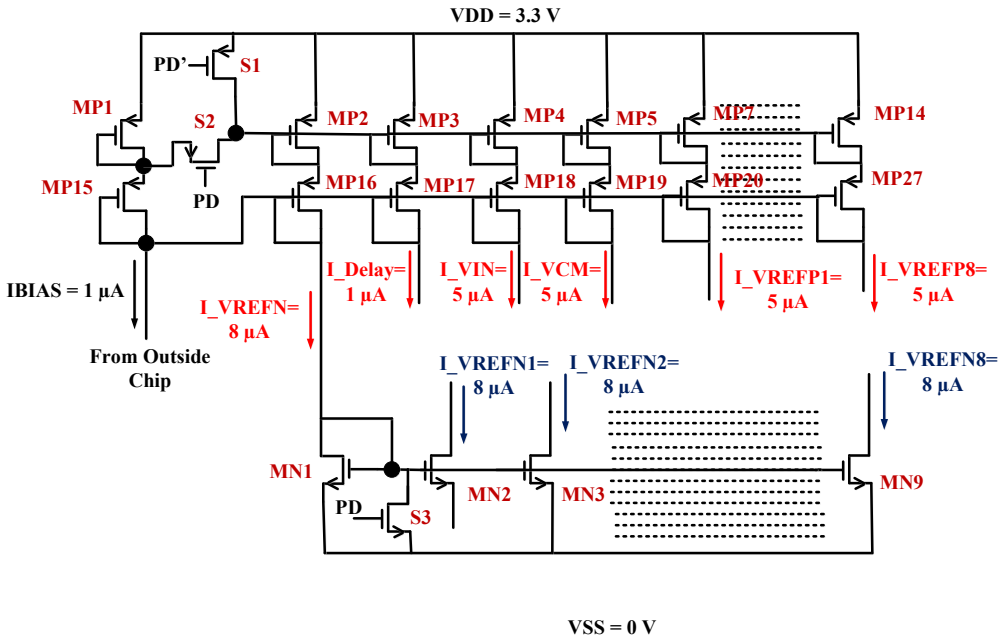


Figure 3. 111. Circuit diagram of master biasing current generator.

Table 3. 24. Transistor sizes for bias current generator circuit

Transistor	W (µm)	L (µm)	No. of Fingers/Gates
MP_1	10	1	2
MP_2	80	1	16
MP_3	10	1	2
MP_4	50	1	10
MP_5	50	1	10
MP_7-MP_{14}	80	1	16
MP_{15}-MP_{27}	10	1	2
MN_1-MN_9	10	2	2
S_1-S_3	2	0.35	1

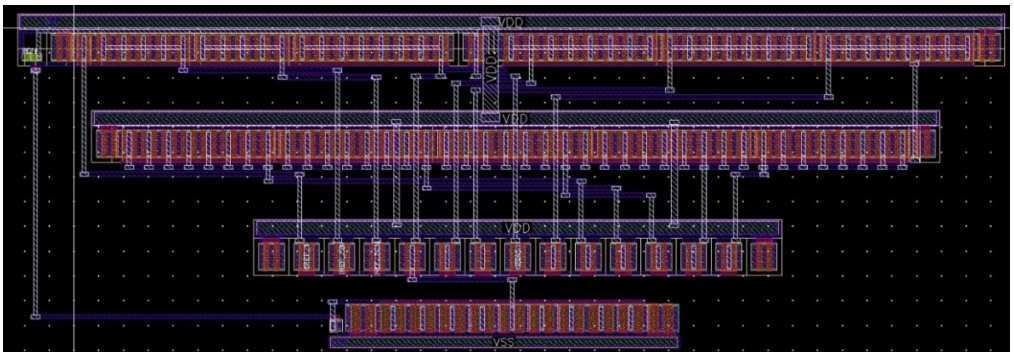


Figure 3. 112. Layout of master biasing current generator.

3.8. Version 2: Fixed Sampling-Rate ADC With the Delay-Cell and Digital Section at 1.2 V

Because of the reasons already mentioned, ADC has been designed at a supply voltage of 3.3 V. The obvious penalty of designing at 3.3 V is high power consumption since the power consumption is directly proportional to the square of the supply voltage. This results in a lower conversion-efficiency. To investigate the potential of the proposed ADC architecture with respect to its power consumption and conversion-efficiency, its delay-cell and digital section have also been implemented at 1.2 V supply. Analog section (CDAC, switches, comparator, and buffers) is not possible to implement using 1.2 V supply voltage because of the high input signal swing requirements. Level-shifters have been utilized to facilitate the design of the digital and analog sections at separate supply voltages. A metastability watchdog circuitry is also part of this version of the ADC for detection and correction of metastability events of the comparator.

Figure 3.113 shows the architecture of the updated ADC. The architecture and working of the ADC is the same except that its delay-cell and digital sections are working at 1.2 V supply. Level-shifters have been used to transform the signals from 1.2 V to 3.3 V and vice versa. For this version of the ADC, a fixed value delay-cell has been used instead of a variable delay-cell. Also, the delay-cell is based on long-channel CMOS inverters. Figure 3.113 clearly differentiates the ADC sections working at two different supply voltages as well as showing the level-shifters. ADC functionality and timing waveform are exactly the same as of 3.3 V version. However, the delays have been appropriately adjusted because of the working of its digital section at 1.2 V.

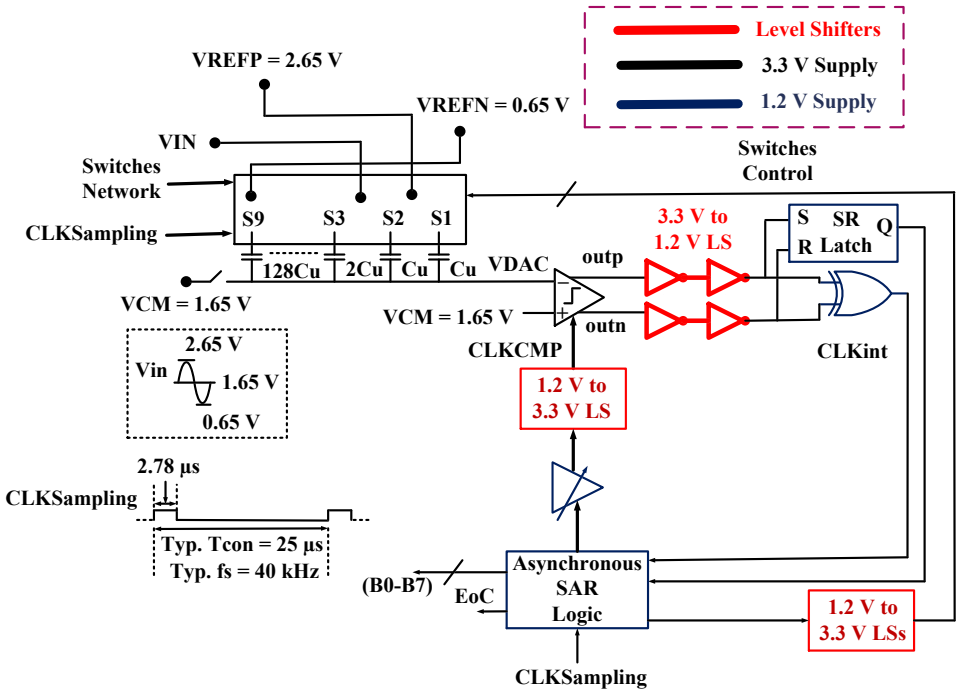


Figure 3. 113. ADC with its delay-cell and digital section working at 1.2 V supply with the help of the level-shifters.

3.8.1. Circuit Level Implementation of Updated Components

All the components of this version of the ADC are the same as of 3.3 V version except the delay-cell and metastability watchdog circuitry. Also, there is an addition of level-shifters to translate signals from 3.3 V to 1.2 V and vice versa. This section, therefore, provides design details of these three components.

3.8.1.1. Delay-Cell

Instead of using a variable delay-cell, a fixed value delay-cell has been designed for this version. The delay-cell has been designed to get minimum delay (275 ns) to enable maximum sampling-rate from the ADC. Figure 3.114 represents the circuit diagram of the delay-cell. The use of 1.2 V supply enables the use of a cascade of long-channel CMOS inverters with capacitors to get the desired delay value. This delay-cell has also been made rising edge only by adding a couple of switches which are driven by the output of the delay-cell. As the output goes high, these witches are turn off, thus disconnecting the capacitors. This introduces much lesser delay to the falling edge of the input signal. To cater for the delay variations caused by the PVT variations, three capacitors with different values have been used to get desired delay if needed. The delay value can be tuned by selecting appropriate capacitor value. External control bits (DC_B0, DC_B1, and DC_B2) allow an easy tuning of the delay-cell. The layout of the delay-cell is shown in Figure 3.115.

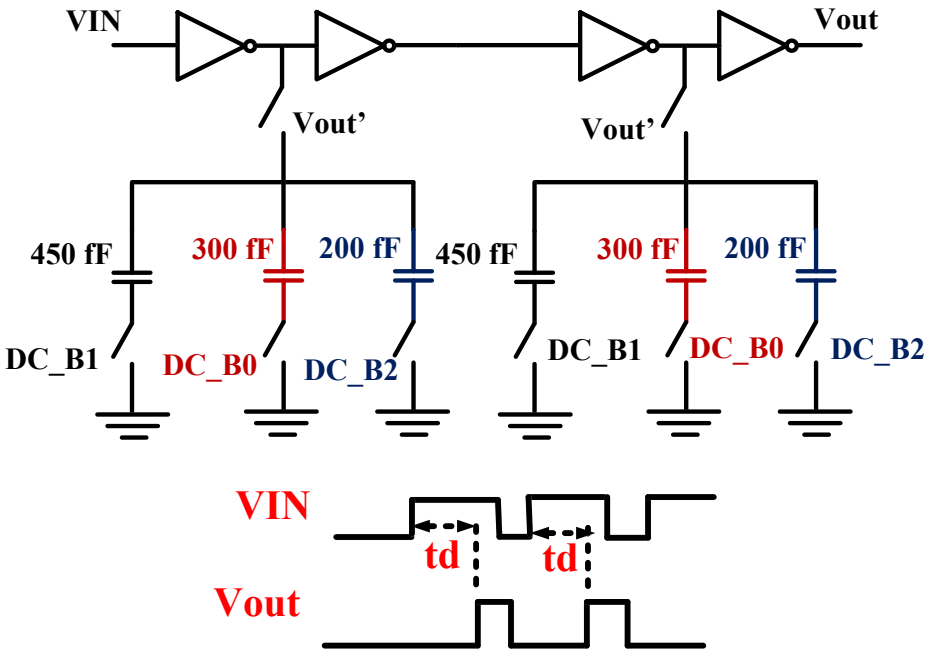


Figure 3. 114. Fixed value delay-cell with its input-output waveforms for Version 2 of the ADC.

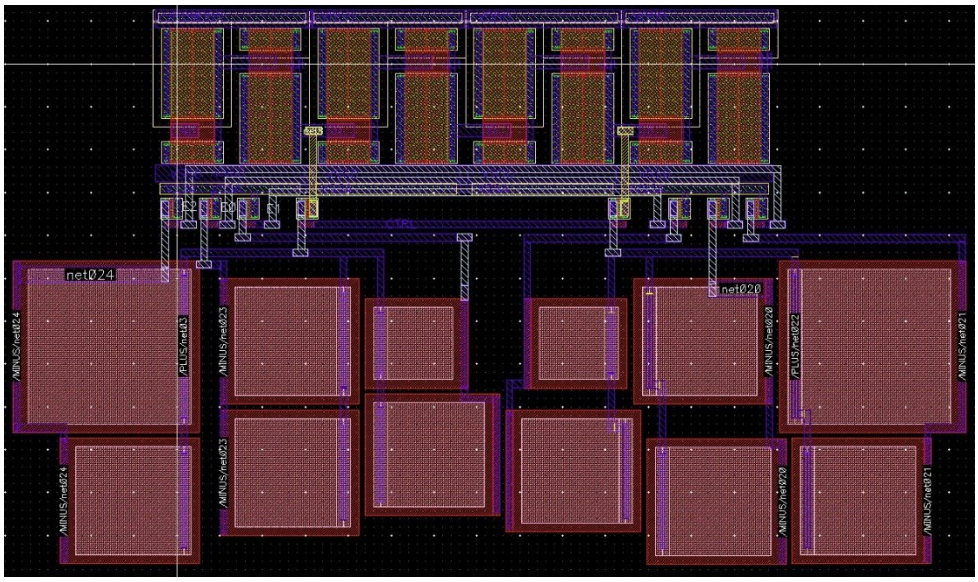


Figure 3. 115. Layout of the delay-cell operating at 1.2 V for Version 2 of the ADC.

3.8.1.2. Level-Shifters

Two types of level-shifters are needed: Lower-to-upper (1.2 V to 3.3 V) and upper-to-lower (3.3 V to 1.2 V). Upper-to-lower level-shifting has been achieved by the use of two simple CMOS inverters, as shown in Figure 3.116. Instead of using traditional lower-to-upper level-shifters (Figure 3.117 (a)), power-efficient level-shifters (Figure 3.117 (b)), have been used to reduce their overall power consumption. The use of two additional transistors (M_{P1} and M_{P2}) above M_{N1} and M_{N2} enables a faster transition at the output as compared to the traditional level-shifters. This reduces the switching power consumption [242]. Table 3.25 provides transistor sizes for the lower-to-upper-level shifter circuit. The layout of lower-to-upper level shifter is presented in Figure 3.118.

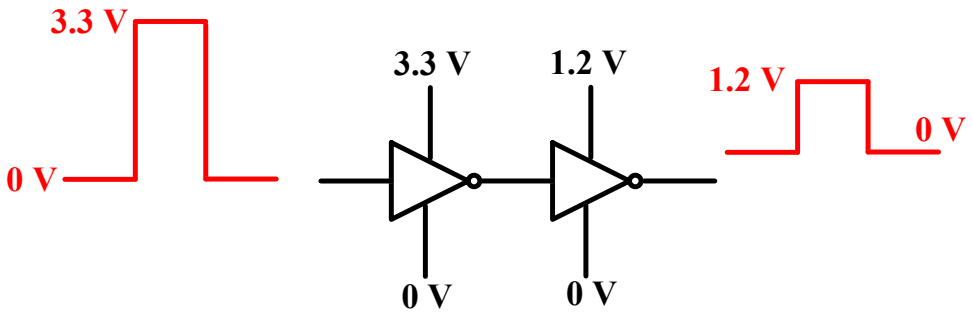
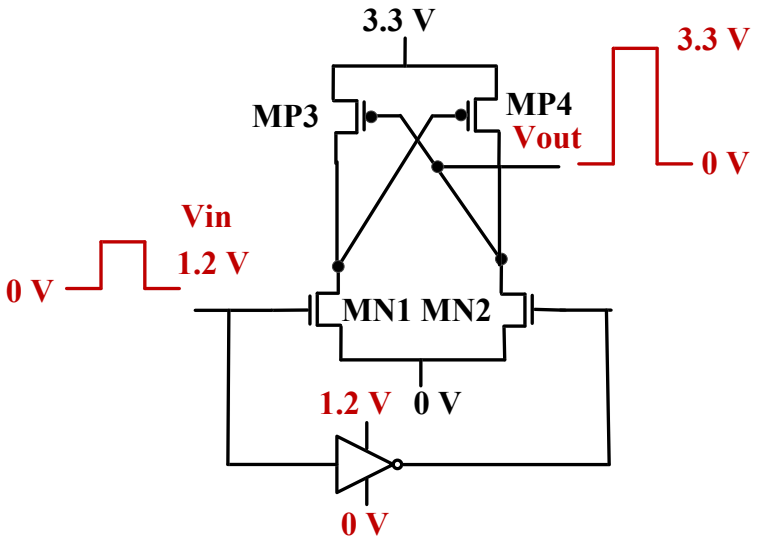


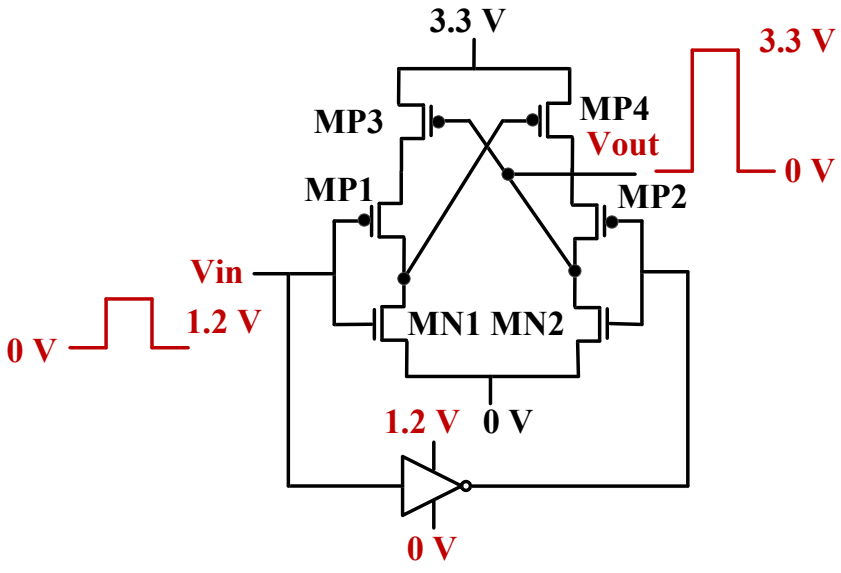
Figure 3. 116. Upper-to-lower level-shifters.

Table 3. 25. Transistor sizes for the lower-to-upper level-shifter circuit (L = 0.35 µm for all devices)

Sr. No.	Transistor	Width (µm)
1.	M_{N1}, M_{N2}	2
2.	M_{P1}, M_{P2}	1
3.	M_{P3}, M_{P4}	2



(a)



(b)

Figure 3. 117. Lower-to-upper level-shifters: (a) traditional, and (b) employed power-efficient [242].

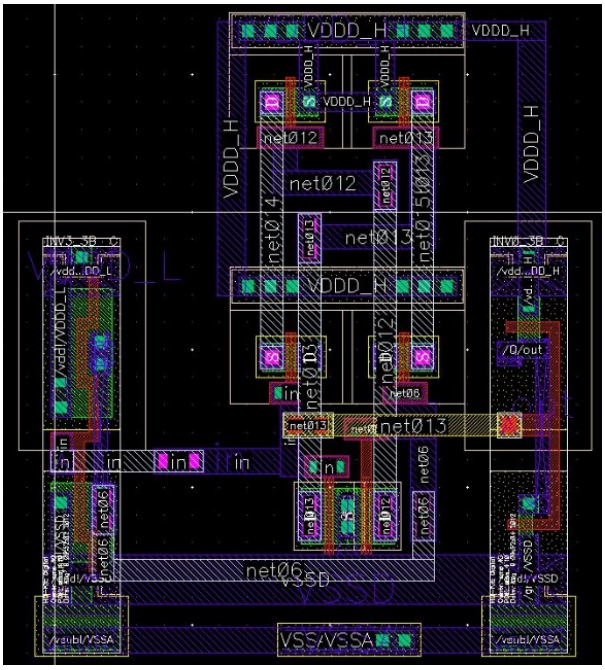


Figure 3. 118. Layout of lower-to-upper-level shifter.

3.8.1.3. Metastability Watchdog Circuitry

Comparator metastability can be a problem for the correct and reliable operation of the ASAR ADC. This is because the clock for the SAR logic (CLK_{int}) is generated internally by XORing the outputs of the comparator. It goes high when comparator makes the decision during regeneration phase. If comparator goes metastable, the rising edge of the CLK_{int} will not arrive within allocated time duration. As a result, the normal operation of the ADC is disturbed, and a wrong conversion result is achieved for that particular sample.

To prevent ADC performance degradation by metastability, a simple metastability watchdog circuitry has been proposed for this version of the ADC. This circuitry detects the metastability event and forces the CLK_{int} to go high right after the metastability detection to resume normal operation of the ADC. Figure 3.119 shows the proposed metastability watchdog circuitry, which consists of simple digital logic and CMOS inverters-based delay-cell. Operation of metastability watchdog circuitry is explained by the timing waveforms of Figure 3.120. The circuit employs a delay-cell and an AND gate to detect metastability event. The amount of delay (T_d) introduced by the delay-cell is the worst-case regeneration time of the comparator. This circuit waits for the rising edge of the CLK_{int} by T_d delay value. If there is no rising edge of the CLK_{int} after T_d, MD signal goes high indicating that comparator has gone metastable. Hence, metastability watchdog circuitry is triggered, and forces the CLK_{int} to go high. This resumes the ADC normal operation. The metastability circuit sends a fixed '0' decision from the comparator to the SAR logic during an event of metastability to avoid a possible scenario of an undefined and random output from the comparator.

A cascade of long-channel CMOS inverters has been used to implement delay-cell for metastability watchdog circuitry. A tunability in the delay-cell has been added to make it robust against PVT variations. In addition, the circuit can be enabled or disabled externally by controlling MD_ext bit. This adds flexibility to the design. During the fabricated chip testing, initially metastability watchdog circuitry can be disabled and ADC function can be verified. Metastability circuitry can only be enabled if needed. This saves the power consumed by the metastability circuitry. The layout of the delay-cell used for metastability watchdog circuitry is shown in Figure 3.121.

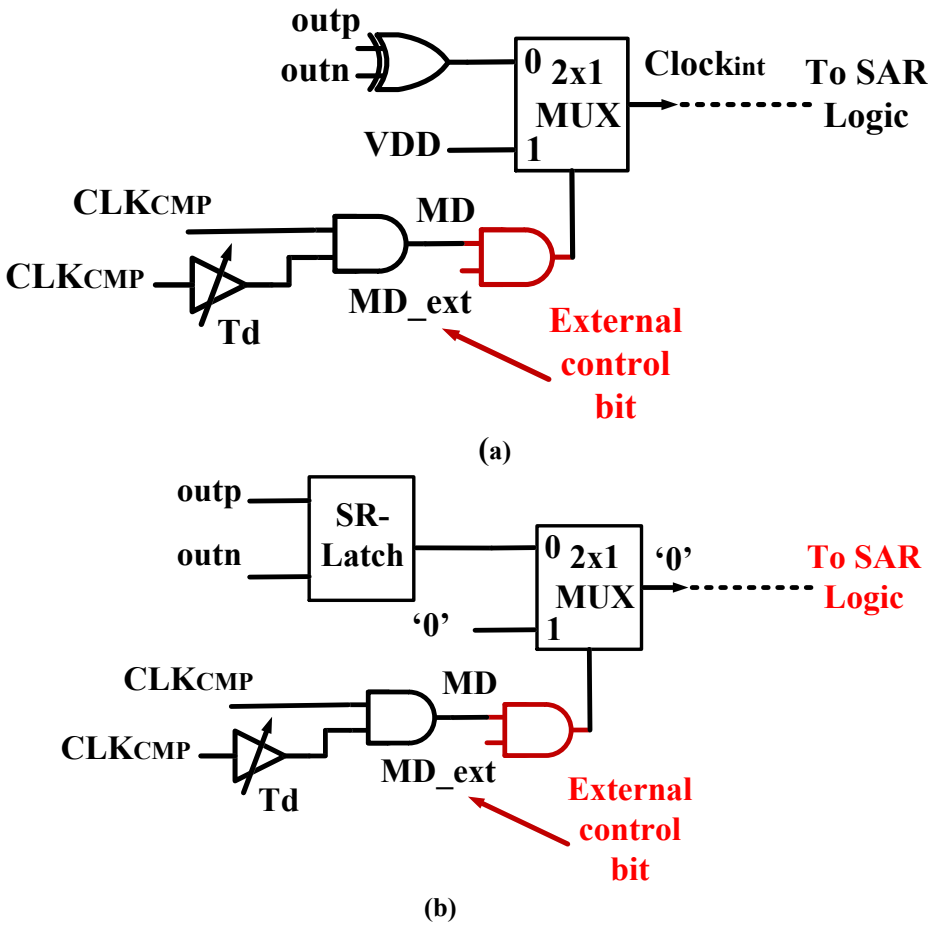


Figure 3. 119. Externally controlled metastability watchdog circuitry for the proposed ADC: (a) circuit ensuring 'CLK_{int}' rising edge generation in case of metastability event; (b) circuit ensuring a fixed logic low '0' decision from the comparator in an event of comparator metastability.

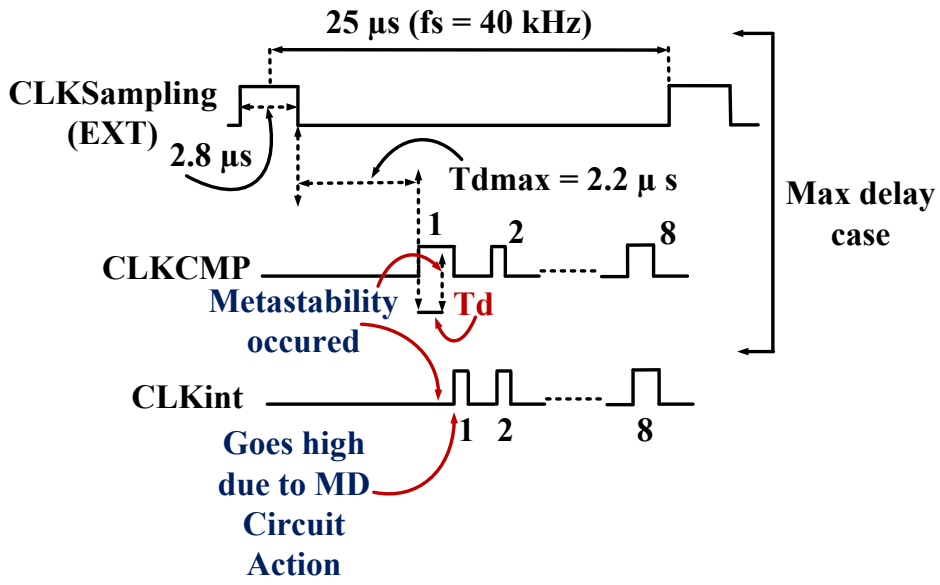


Figure 3. 120. Timing waveforms showing the operation of metastability watchdog circuit for the proposed ADC.

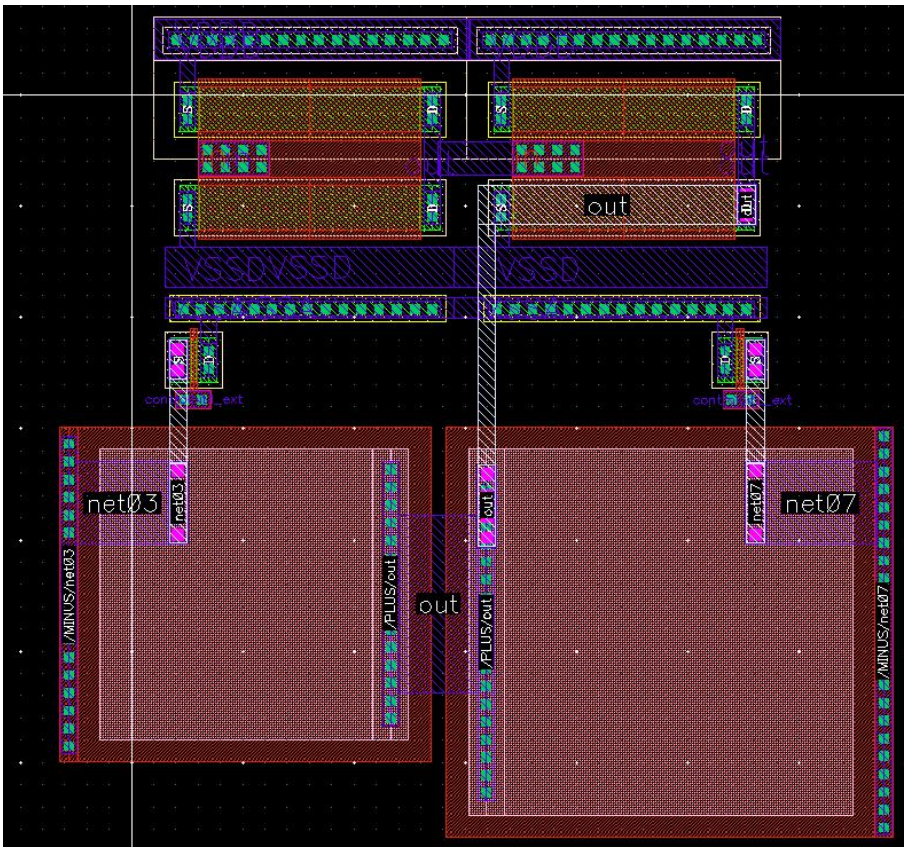


Figure 3. 121. Layout of delay-cell of metastability watchdog circuitry.

3.9. Schematic Level Simulation Results of ADC

After completing the schematic level implementation, the ADC performance is verified using extensive simulations. Figure 3.122 shows the PSD plots of the ADC at its typical f_s in three corners (w_t, w_s, and

w_p) based on transient noise simulations. The ADC secures a minimum ENOB of 7.79 Bits and SNDR of 48.5 dB. To validate its f_s-reconfigurability functionality, Figure 3.123 shows its PSD plots at all supporting sampling-rates. The achieved performance (ENOB and SNDR) is the same at all sampling-rates and hence f_s-reconfigurability functionality is vindicated.

Figure 3.124 shows the ADC PSD plots for version 2 of the ADC, i.e., the one whose delay-cell and digital section are working at 1.2 V. The secured performance (ENOB and SNDR) is the same as for the 3.3 V version. As the delay-cell of this version is fixed, it operates at only one sampling-rate. The efficacy of metastability watchdog circuitry is also evaluated. As comparator never goes metastable in the transient noise simulations, ADC performance is exactly same as with metastability watchdog circuitry activated or deactivated. However, comparator can go metastable in the measurements, therefore the use of the metastability watchdog circuitry is critical for the fabricated chip.

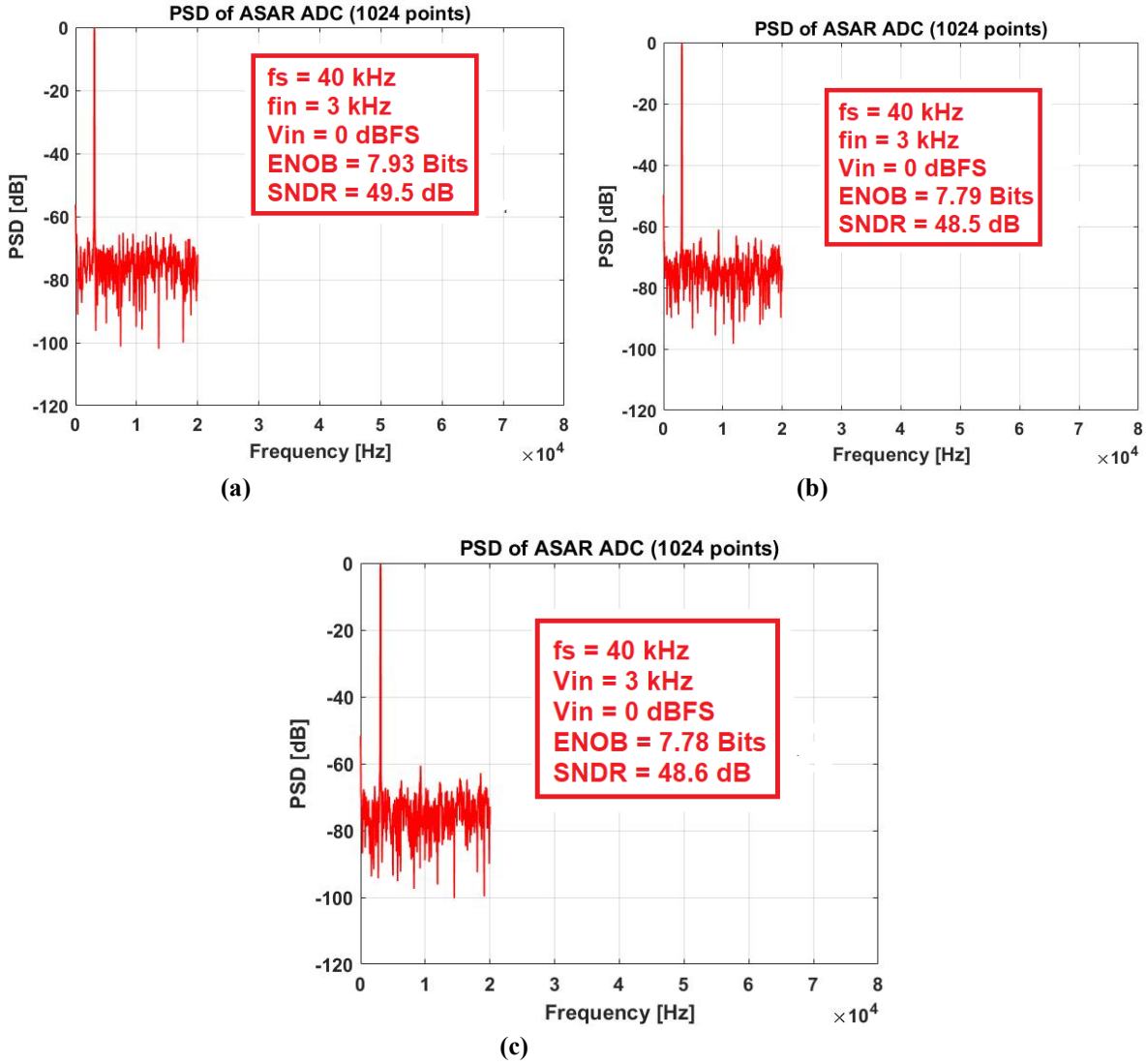


Figure 3. 122. Shematic-level transient noise simulated PSD plots of ADC at its typical sampling-rate in (a) w_t corner, (b) w_p corner, and (c) w_s corner.

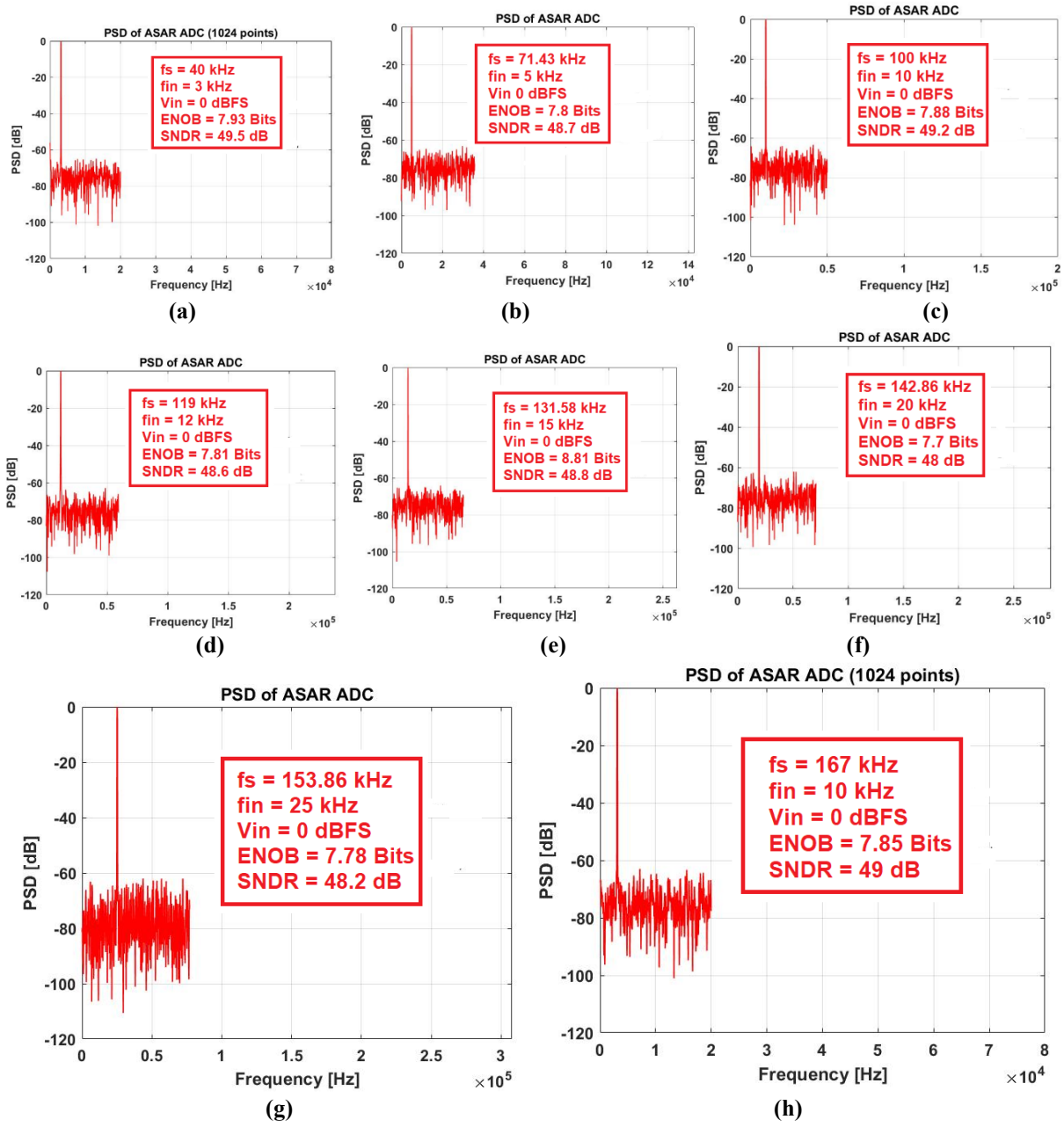


Figure 3. 123. Shematic-level simulated PSD plots of ADC at all its supprted sampling-rates: (a) at $f_s = 40\ kHz$ with one unit voltage buffer of each type on; (b) at $f_s = 71.43\ kHz$ with two unit voltage buffers of each type on; (c) at $f_s = 100\ kHz$ with three unit voltage buffers of each type on; (d) at $f_s = 119\ kHz$ with four unit voltage buffers of each type on; (e) at $f_s = 131.58\ kHz$ with five unit voltage buffers of each type on; (f) at $f_s = 142.86\ kHz$ with six unit voltage buffers of each type on; (g) at $f_s = 153.85\ kHz$ with seven unit voltage buffers of each type on; (h) at $f_s = 167\ kHz$ with all eight unit voltage buffers of each type on. All simulations are based on transient noise.

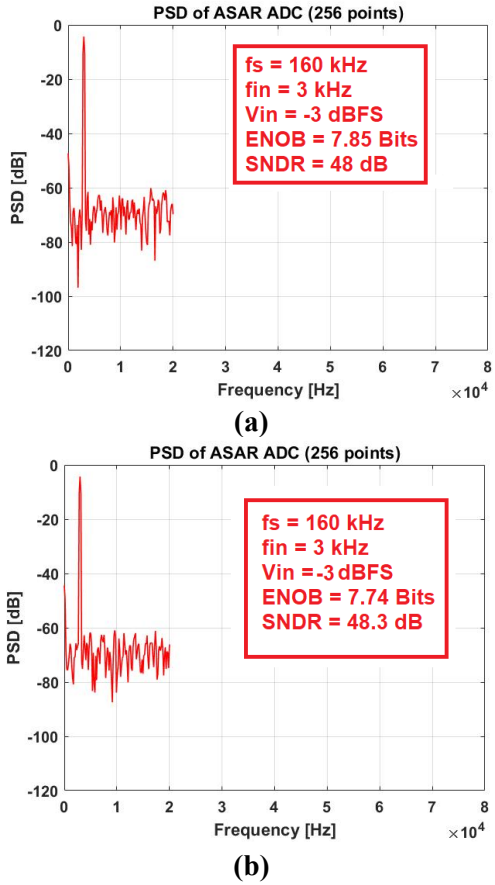
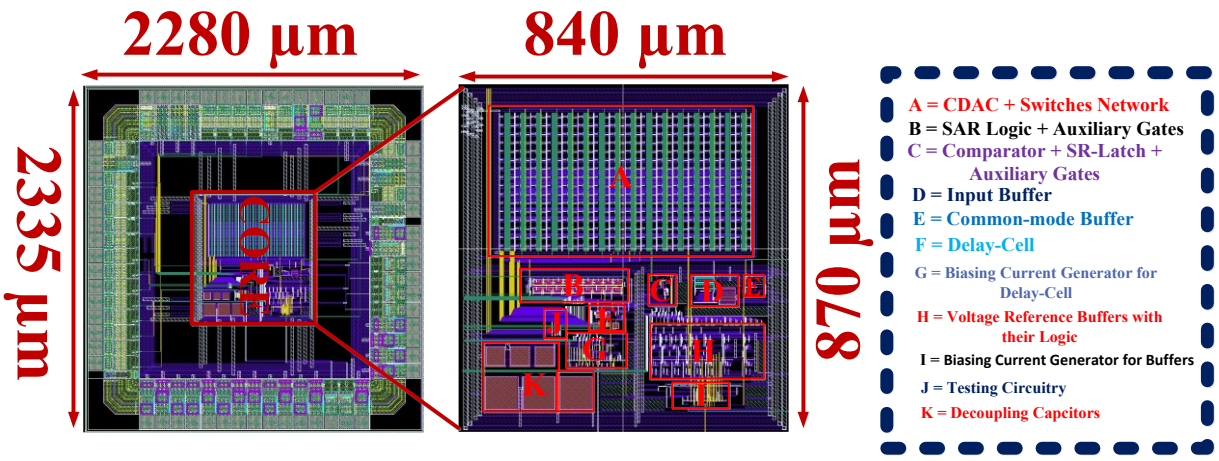


Figure 3. 124. Shematic-level transient noise simulated PSD plot of ADC with delay-cell and digital section working at 1.2 V (a) without mestability watchdog circuitry, and (b) with mestability watchdog circuitry.

3.10. Post-Layout Simulation Results of ADC

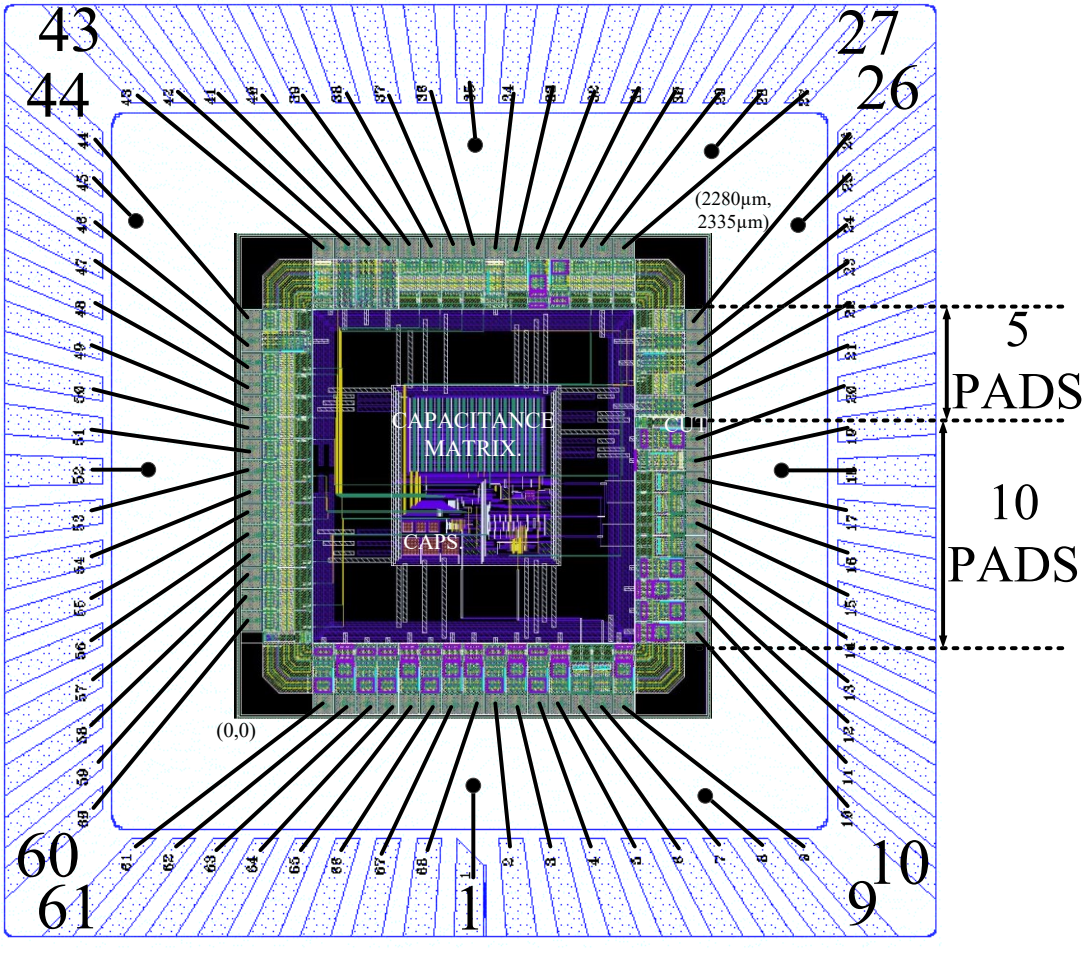
Figure 3.125 shows the final top-level layout of the designed ADC with its core. Designed in a 0.35 µm CMOS process at a supply voltage of 3.3 V, the ADC core occupies 840 µm× 870 µm chip-area. Extensive post-layout simulations have been carried out to verify ADC performance. Initially, the ADC performance is tested with the extracted view of each designed component (e.g. comapartor) to identify possible problem due to parasitics. In case of problem, the layout is updated to get rid of the parasitics responsbile for performance degradation. Once done, core of the ADC is laidout according to the plan shown in Figure 3.125. Special attention has been paid to the floor planning of different cells to avoid issues, such as crossotalk, coupling, etc. An adequate separation is ensured between the analog and digital sections of the ADC. Shiedling has been done for critical nodes, scuh as CDAC node of the CDAC. On-chip decoupling capcitors have been added to filter supply noise. After successful design of the core layout, top-level layout is achieved by designing and integrating the padring. Figure 3.126 depcits bonding diagram of the chip with JLCC68 package.

To showcase post-layout dynamic performance of ADC, Figure 3.127 shows its PSD plots at all covered sampling-rates. As it is evidenced by these plots, ADC performance is fully satisfactory, achieving an ENOB of 7.8-bits and SNDR of 48.5 dB at all the sampling-rates. SNDR vs input signal amplitude plot of the ADC is shown in Figure 3.128 (b), which shows its dynamic range of 48 dB. ADC is also characterised with respect to its static performance. Figure 3.128 (a) shows its DNL and INL, which are well below 0.5 LSB. Figure 3.129 shows the PSD plots of version 2 of the ADC, i.e., whose delay-cell and digtial section are operating at 1.2 V. This version also shows a performance comparable to the 3.3 V version.



(a) **(b)**

Figure 3. 125. Layout photo of the designed chip: (a) top-level; (b) core with detail of placement of each block.



JLCC_68_pin.gif

Figure 3. 126. Bonding diagram of ADC chip with JLCC68 package.

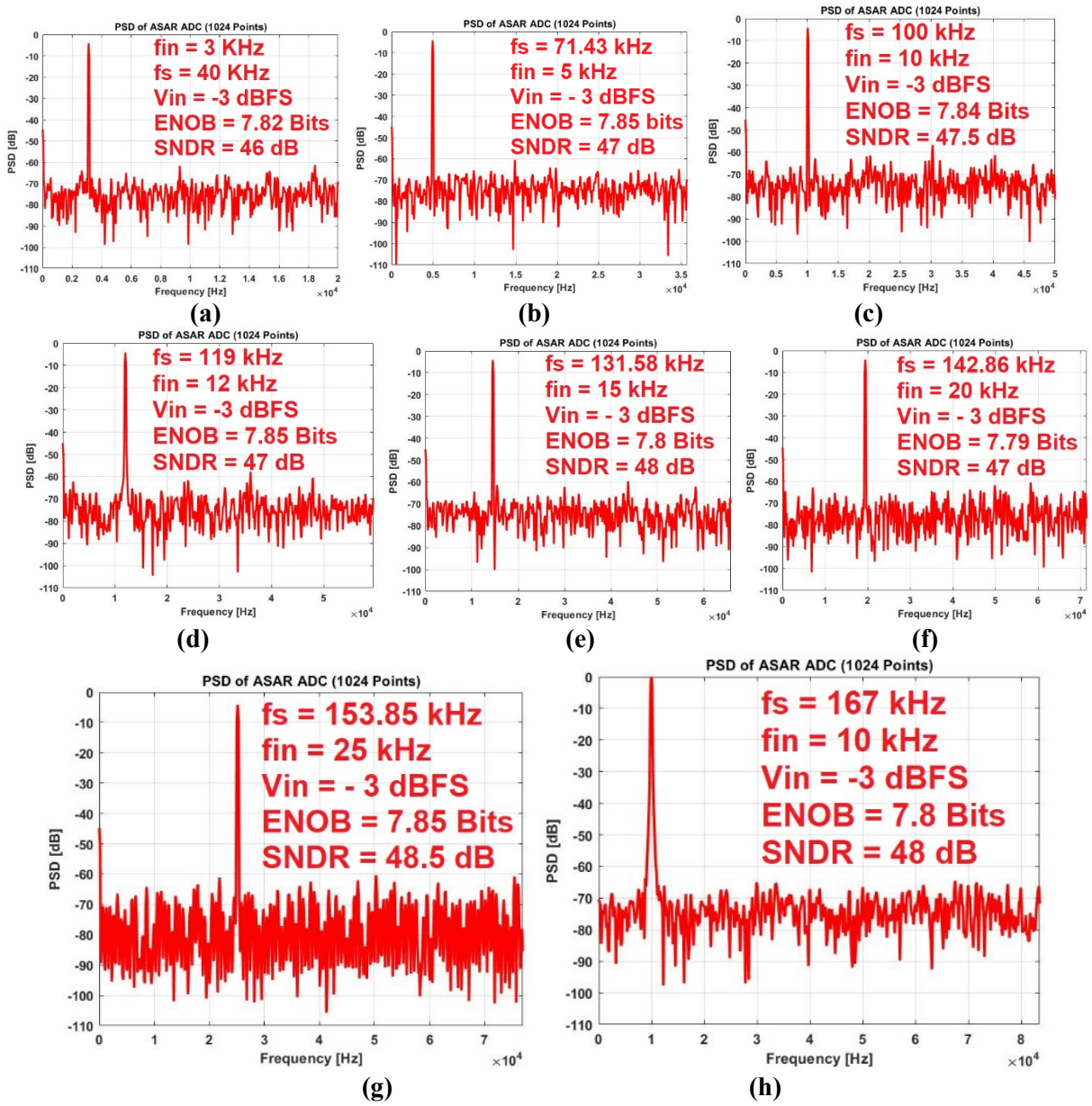


Figure 3. 127. Post-layout simulated PSD of ADC at all its supported sampling-rates: (a) at $f_s = 40\ kHz$ with one unit voltage buffer of each type on; (b) at $f_s = 71.43\ kHz$ with two unit voltage buffers of each type on; (c) at $f_s = 100\ kHz$ with three unit voltage buffers of each type on; (d) at $f_s = 119\ kHz$ with four unit voltage buffers of each type on; (e) at $f_s = 131.58\ kHz$ with five unit voltage buffers of each type on; (f) at $f_s = 142.86\ kHz$ with six unit voltage buffers of each type on; (g) at $f_s = 153.85\ kHz$ with seven unit voltage buffers of each type on; (h) at $f_s = 167\ kHz$ with all eight unit voltage buffers of each type on. All simulations are based on transient noise.

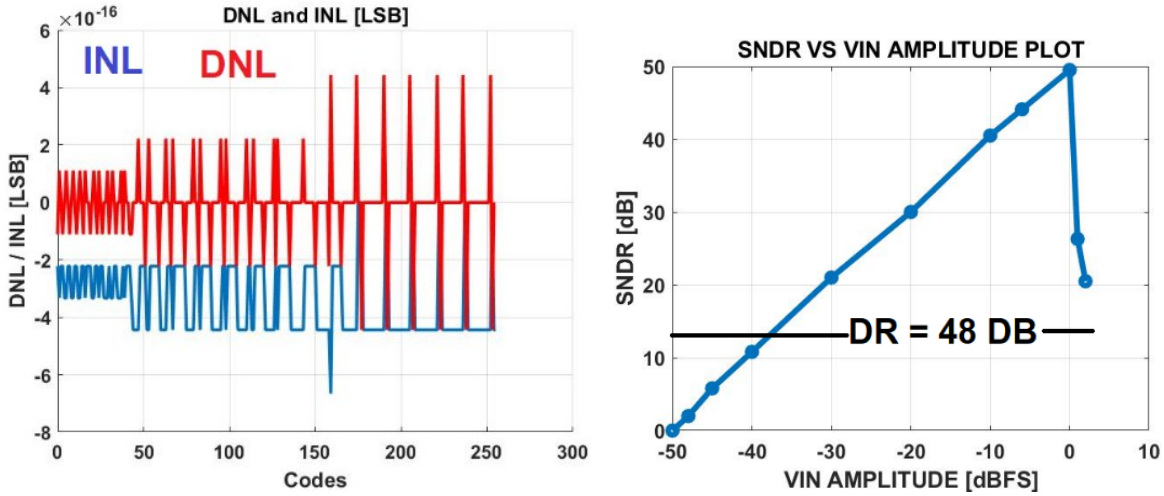
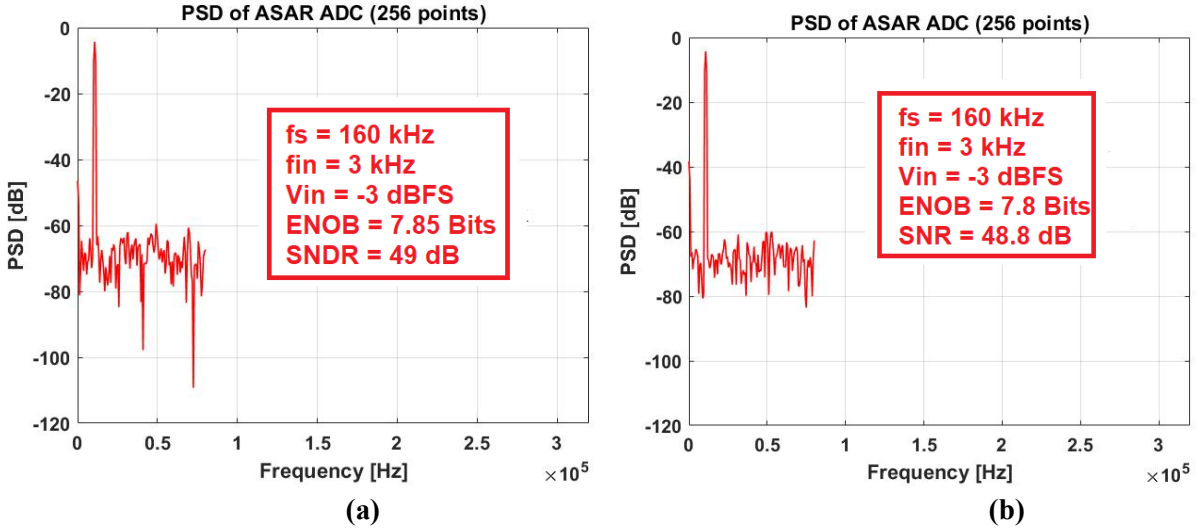


Figure 3. 128. (a) DNL and INL plots of the proposed ADC; (b) SNDR vs. V_{IN} amplitude plot.



(a) **(b)**

Figure 3. 129. Post-layout transient noise simulated PSD plots of ADC version with delay-cell and digital section working at 1.2 V (a) without mestability watchdog circuitry, and (b) with mestability watchdog circuitry.

3.11. Measurement Results

Figure 3.130 shows the fabricated chip micro photograph. A custom PCB board (Figure 3.130 (d)) is designed for testing the ADC chip. The ADC chip is measured using laboratory equipment. Figure 3.130 (e) shows the measurement set-up. Measurement set-up consists of signal generator (APx524 audio analyzer; HEWLETT PACKARD 3245A universal source; Tektronix AFG3252 function generator) for input signal generation, power supply (Keysight E3641A triple output power supply), logic analyzer (Tektronix TLA5202B) to acquire output data, digital multimeter, Oscilloscope (LeCro 204Xi) and clock generator (Tektronix AFG3252 function generator) to provide the CLKSampling signal, besides the PCB.

First, ADC is measured with respect to its dynamic performance. Figure 3.131 depicts ADC PSD plots at all supported sampling-rates. As evidenced by the plots, the measured performance (ENOB and SNDR) of the ADC is equal to its post-layout performance at all the sampling-rates. It is despite the fact that the signal generator used for generating the input signal for the ADC introduces its own noise unlike the ideal generator in the simulations. ADC SNDR vs. input signal amplitude plot is shown in Figure 3.133, which

shows a dynamic range of 48 dB. This is again the same as obtained in post-layout simulation results. Figure 3.132 shows the static parameters (DNL and INL plots) of the ADC. Both of these lie within one LSB. Measured DNL is -0.4/+0.6 LSB, while INL is -0.5/+0.5 LSB. A sharp transition in INL plot can be observed at the middle code (127 and 128). It is because of the worst-case matching at these codes. Good static performance vindicates the effectiveness of the CDAC capacitor matching and the suitability of unit capacitor for the CDAC.

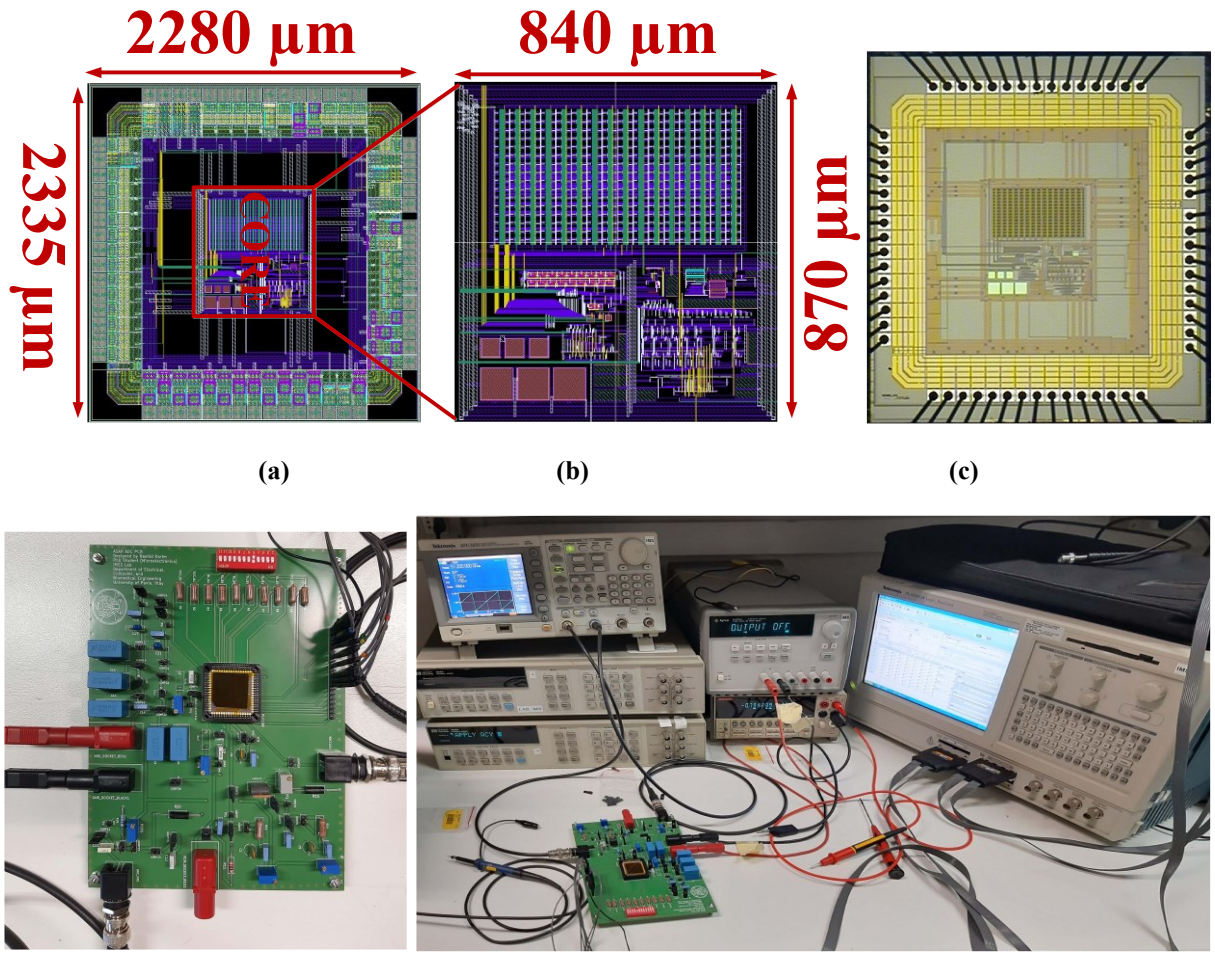
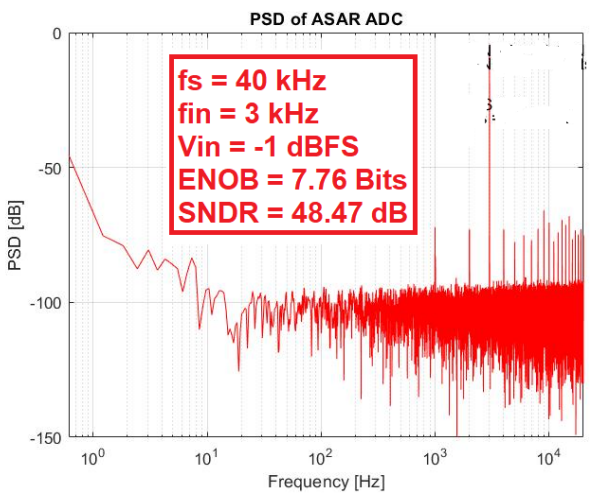
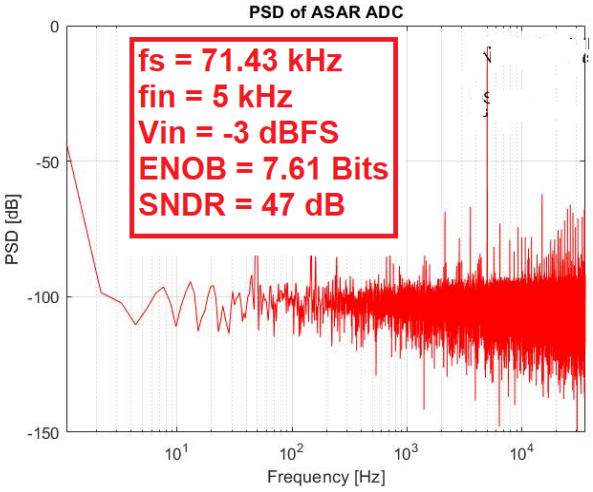


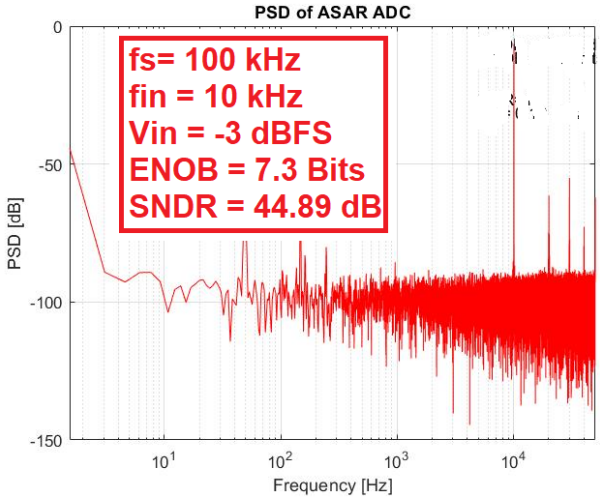
Figure 3. 130. Layout photo of the designed chip: (a) top-level; (b) core; (c) die microphotograph; (d) custom designed PCB test board, and (e) Measurement set up of ADC using custom made PCB.


PSD of ASAR ADC
fs = 40 kHz
fin = 3 kHz
Vin = -1 dBFS
ENOB = 7.76 Bits
SNDR = 48.47 dB
PSD [dB]
Frequency [Hz]

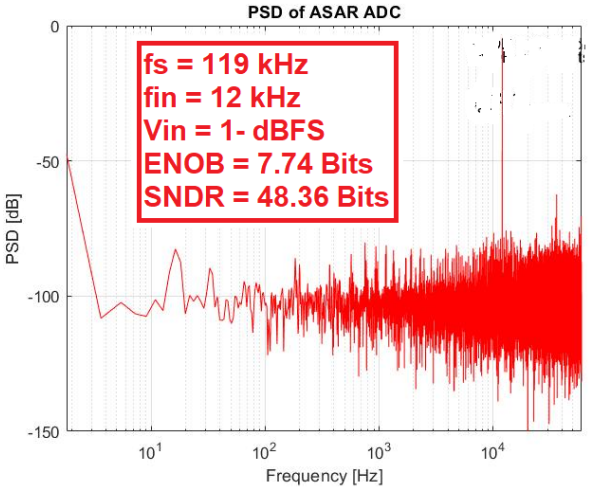
(a)


PSD of ASAR ADC
fs = 71.43 kHz
fin = 5 kHz
Vin = -3 dBFS
ENOB = 7.61 Bits
SNDR = 47 dB
PSD [dB]
Frequency [Hz]

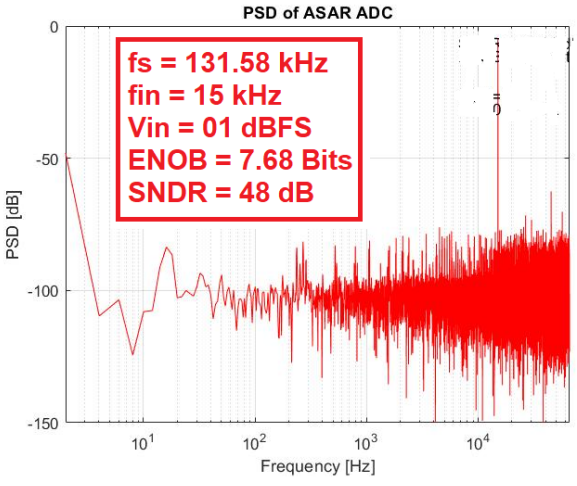
(b)


PSD of ASAR ADC
fs= 100 kHz
fin = 10 kHz
Vin = -3 dBFS
ENOB = 7.3 Bits
SNDR = 44.89 dB
PSD [dB]
Frequency [Hz]

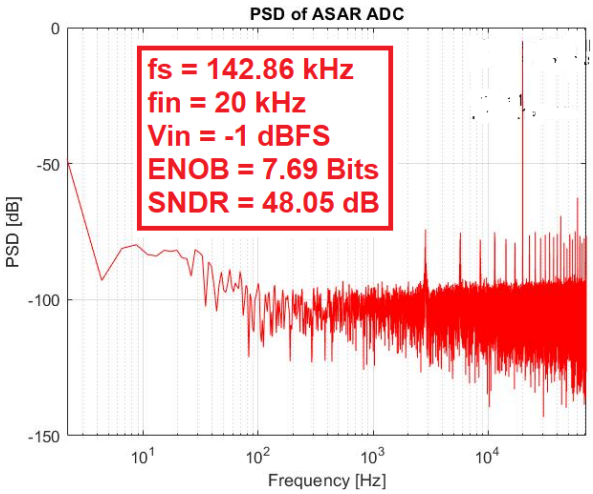
(c)


PSD of ASAR ADC
fs = 119 kHz
fin = 12 kHz
Vin = 1- dBFS
ENOB = 7.74 Bits
SNDR = 48.36 Bits
PSD [dB]
Frequency [Hz]

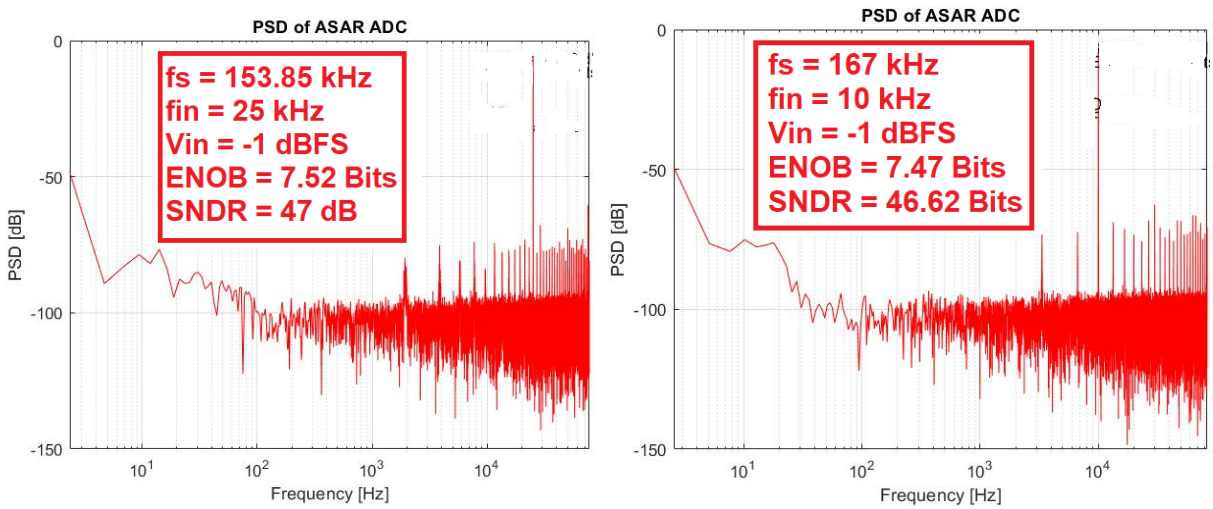
(d)


PSD of ASAR ADC
fs = 131.58 kHz
fin = 15 kHz
Vin = 01 dBFS
ENOB = 7.68 Bits
SNDR = 48 dB
PSD [dB]
Frequency [Hz]

(e)

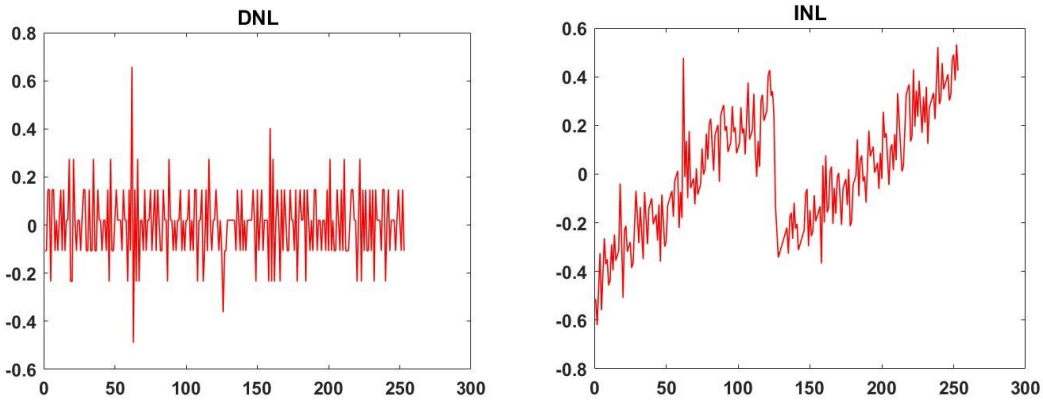

PSD of ASAR ADC
fs = 142.86 kHz
fin = 20 kHz
Vin = -1 dBFS
ENOB = 7.69 Bits
SNDR = 48.05 dB
PSD [dB]
Frequency [Hz]

(f)



(g) **(h)**

Figure 3. 131. Measured PSD of ADC at all its supprted sampling-rates: (a) at $f_s = 40\ kHz$ with one unit voltage buffer of each type on; (b) at $f_s = 71.43\ kHz$ with two unit voltage buffers of each type on; (c) at $f_s = 100\ kHz$ with three unit voltage buffers of each type on; (d) at $f_s = 119\ kHz$ with four unit voltage buffers of each type on; (e) at $f_s = 131.58\ kHz$ with five unit voltage buffers of each type on; (f) at $f_s = 142.86\ kHz$ with six unit voltage buffers of each type on; (g) at $f_s = 153.85\ kHz$ with seven unit voltage buffers of each type on; (h) at $f_s = 167\ kHz$ with all eight unit voltage buffers of each type on.



(a) (b)

Figure 3. 132. Measured (a) DNL plot; (b) INL plot of the proposed ADC.

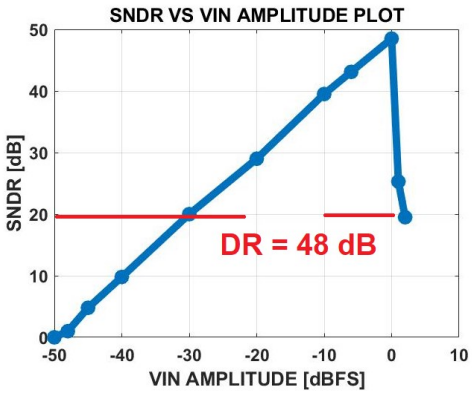


Figure 3. 133. SNDR vs. V_{IN} amplitude plot of ADC in measurements.

3.12. Comparison of ADC with State-of-the-Art

Table 3.26 compares performance of the designed ASAR ADC with other slimier SAR and ASAR ADCs. Performance of the ASAR ADC is better or at least comparable with other ADCs of Table 3.26. For example, the ENOB and DNL/INL of the proposed ADC are better than all other fabricated ADCs of Tabe 3.26. Also, it is sampling-rate reconfigurable unlike all other fixed sampling-rate ADCs. It is worth mentioning that this measured performance of the ADC has been achieved without the use of any complex and sophisticated design technique, such as CDAC trimming and calibration, comparator offset cancellation, etc., unlike other ADCs in comparison. This fact makes this ADC further superior.

As already described, the supply voltage of the fabricated ADC is 3.3 V to accommodate high input signal swing (as high as 2 V). This is also highly beneficial from crosstalk and interference point of view. These benefits come at the cost of high-power consumption or low energy-efficiency. Consequently, the comparison of this high supply voltage-based ADC with recent low supply voltage-based ADC is extremely difficult with respect to power consumption, energy-efficiency, and hence conventional figure-of-merit (FoM_W). It is because the power consumption is directly proportional to the square of the supply voltage. Besides several other ADCs such as proposed in [243][244][245][246], a couple of high supply voltage-based ADCs listed in Table 3.26 corroborate this fact. This pushes the need for a new figure-of-merit for a fair comparison of these two types of ADCs. Therefore, this thesis has proposed a novel figure-of-merit (FoM_{WN}), which is a normalized version of the traditional figure-of-merit (FoM_W). This FoM is listed in Table 3.26. All the ADCs listed in Table 3.26 have been compared with both the FoMs, i.e., FoM_W and FoM_{WN}.

Considering ADC performance keeping in view the FoM_{WN}, the proposed ADC becomes an excellent competitor for the state-of-the-art ADCs proposed in recent literature even with respect to the energy-efficiency. In addition, the other ADCs are void of the additional advantages and functions provided by the proposed ADC. These advantages include f_s-reconfigurablity with constant energy-efficiency at all covered sampling-rates, its scalability and flexibility. The proposed ADC architecture is an auspicious candidate for implementation in ultra-scaled technology nodes (< 65 nm) with low supply voltage and input signal swing. Such implementation would also bring high speed advantage.

Although the power consumption of the standalone ADC seems high, it actually becomes negligible when calculated in multi-channel ASICs environment for space applications. Let us assume that there are 1024 channels of the ASIC and there is one ASAR ADC per channel. Also assume that the event-rate is 10^5 events/sec, which is a quite reasonable approximation since the events in space are sporadic. The typical conversion time for the ASAR ADC is 25 µs with a power consumption of 52.8 µW at 3.3 V. Based on these numbers, the average power consumption of one ASAR ADC comes out to be only 5.28 µW, as per (3.5).

$$\mathrm{P_{integratedwithASIC}} = 10^5 \times 52.8 \times 10^{-6} = 5.28\ \mu\mathrm{W} \tag{3.5}$$

This power calculation considers that the ADC is operating continuously. This is actually not true since the ADC does not consume power, being idle, when there is no event. The probability that there is no event for space applications is significant. Takin into account this fact reduces ADC power significantly. The power consumption becomes even lower (about 0.39 µW based on above assumptions) for the version 2 of the ADC, i.e., whose delay-cell and digital section are operating at 1.2 V. The power consumption of the ADC becomes even insignificant while comparing it with the power consumption of analog front-end section of the ASIC for space applications.

Table 3. 26**.** Comparison of proposed ASAR ADC with other similar SAR and ASAR ADCs

	[247] (Meas.)	[78] (Sim.)	[248] (Meas.)	[249] (Meas.)	[250] (Sim.)	[251] (Meas.)	[252] (Meas.)	**This Work (Meas.)**		
Topology	SAR	ASAR	ASAR	SAR	SAR	SAR	SAR	**ASAR**		
Process (nm)	90	180	180	180	180	130	350	**350**		
V_{DD} **(V)**	1.2/1.8	0.5	0.23	3.3/1.2	1.8	3.3	3.3	**3.3**	**3.3/1.2**	
									w LS	**w/o LS**
f_s **(kHz)**	50000	5	20	830	1231500	830	100	**40-167**	**167**	
f_s**-reconfig.?**	N	N	N	N	N	N	N	**Y**		
Res. (Bits/ENOB (Bits)	10/7.2	10/9.9	10/-	8/7.48	8/7.2	/9.71	/10.4	**8/7.76**		
SNDR (dB)	58.4	-	52	-	45.1	60.218	64.3	**48.47**		
INL (LSB)	-	-	± 1.7	+0.63/-1.34	-4.5/-3	-2.27/+2.02	-0.86/+0.83	**-0.5/+0.5**		
DNL (LSB)	-	-	± 1	+1.65/1.45	-3/-4	-0.82/_1.41	-0.3/+1.3	**-0.4/+0.6**		
P_{avg} **(µW)**	6	1.43	0.0575	209	20400	3200	247.5	**52.8***/ **221.65**#	**39**	**35**
P_{avgN} **(µW)**	4.167	5.72	1.1	145.14	6269.3	293.85	22.73	**4.85***/**20**#	**6.7**	**6.22**
FoM_W **(fJ/c-step)**	816	143.08	8.8	1410	13800	4603.31	1830	**5150***/ **5180**#	**1520**	**1360**
FoM_{WN} **(fJ/c-step)**	566.82	1197.4	537	980	3.47	422.7	168.22	**473.4***/ **476**#	**261.7**	**243**

LS: Level-Shifters; * at typical f_s; # at maximum f_s; $FoM_W = \frac{P_{avg}}{2^{ENOB}.f_s}$; $FoM_{WN} = \frac{P_{avgN}}{2^{ENOB}.f_s}$

Finally, Table 3.27 provides a performance summary of the proposed ADC at all its covered sampling-rates. It can be witnessed that the ADC exhibits the same performance (ENOB, SNDR, INL and DNL) at all covered sampling-rates. In addition, its power consumption is proportional to its sampling-rate, resulting in constant energy-efficiency. In other words, its energy-efficiency is independent of its sampling-rate.

Table 3. 27. ADC performance parameters at all supporting sampling-rates

Parameter/Sampling-rates	f_{s1} **(kHz)**	f_{s2} **(kHz)**	f_{s3} **(kHz)**	f_{s4} **(kHz)**	f_{s5} **(kHz)**	f_{s6} **(kHz)**	f_{s7} **(kHz)**	f_{s8} **(kHz)**
Topology	ASAR	ASAR	ASAR	ASAR	ASAR	ASAR	ASAR	ASAR
Process (nm)	350	350	350	350	350	350	350	350
V_{DD} **(V)**	3.3	3.3	3.3	3.3	3.3	3.3	3.3	3.3
f_s **(kHz)**	40	71.43	100	119	131.58	142.86	153.85	167
ENOB (Bits)	7.76	7.61	7.3	7.74	7.68	7.69	7.52	7.47
SNDR (dB)	48.47	47	45	48.36	48	48.05	47	46.62
INL (LSB)	≤ 1	≤ 1	≤ 1	≤ 1	≤ 1	≤ 1	≤ 1	≤ 1
DNL (LSB)	≤ 1	≤ 1	≤ 1	≤ 1	≤ 1	≤ 1	≤ 1	≤ 1
P_{avg} **(µW)**	52.8	91	128	152	169	186	200	221.65
P_{avgN} **(µW)**	4.85	8.4	11.73	13.94	15.52	17	18.36	20
FoM_W **(fJ/c-step)**	5150	5014	4980	4980	5000	5090	5070	5180
FoM_{WN} **(fJ/c-step)**	473.4	460	456	458	460	465	466	476

Chapter 4

A SINGLE-CHANNEL SAMPLING-RATE RECONFIGURABLE DUAL-MODE NOISE-SHAPING SAR ADC

Chapter Abstract

This chapter is dedicated to the design and measurement of the second ADC chip, which is on single-channel sampling-rate reconfigurable dual-mode NS-SAR ADC. The chapter does so in a top-down approach. The chapter starts with motivation for the design of the ADC in section 4.1. ADC specifications are part of section 4.2. Section 4.3 is focused on the system level details of the ADC. The description of the ADC architecture and operating principle is done in section 4.4. Verilog-A implementation of the ADC is part of section 4.5. Section 4.6 is devoted to schematic level design of the ADC. The details on making the ADC operate in incremental mode is provided in section 4.7. Schematic level simulation results of the ADC are part of section 4.8, followed by the post-layout simulation results in section 4.9. The detailed measurement results of the ADC are summarized in section 4.10. Section 4.11 provides a comparison of the ADC with state-of-the-art. The chapter concludes with a performance summary of the ADC in section 4.12.

4.1. Motivation

The ASAR ADC chip meets all the targeted requirements, mentioned in chapter 1, of multi-channel ASICs for space applications. However, its ENOB (8 bits) and SNDR (48 dB) are at the lower side of the performance metric. As described in chapter 1, the typical requirements of ADCs for multi-channel ASICs for space applications in terms of ENOB and SNDR are 10-12 bits and 66-72 dB, respectively. This pushes the need for improvement of these metrics of the ASAR ADC to make it more attractive for target application. As illustrated in chapter 2 (section 2.5), one of the best and optimized ways to do so is to introduce Noise-Shaping (NS) into the ASAR ADC to realize a noise-shaping SAR ADC. In contrast to the other available choices, the progression of the ASAR ADC into the noise-shaping SAR ADC offers several benefits. First, it is simple since it needs minimum modifications to the standard ASAR ADC. Second, it is a low-profile, cost-effective, and power-efficient solution. Third, it permits tradeoff bandwidth with the ENOB by choosing desired oversampling ratio (OSR). Fourth, it can be tuned with respect to its OSR value to achieve configurable sampling-rate and performance (e.g., ENOB and SNDR). Fifth, it provides flexibility in terms of the order of noise-shaping and OSR value. Finally, noise-shaping SAR operation can judiciously be exploited to achieve both free-running as well as incremental mode operation in a simpler and more efficient manner than the traditional ways.

Motivated by the need to improve the ASAR ADC performance (ENOB and SNDR) and instigated by the benefits of noise-shaping SAR ADC, this chapter presents a single-channel sampling-rate reconfigurable dual-mode noise-shaping SAR ADC. The core of the NS-SAR ADC is 8-bit ASAR ADC presented in chapter 3. The proposed NS-SAR ADC operates in two modes: NS or free-running mode, and incremental mode. The ADC can be made to operate either in NS mode or incremental mode based on an external control. This introduces great flexibility in the ADC and makes it versatile and multi-purpose.

4.2. Dual-Mode NS-SAR ADC: Specifications

Table 4.1 shows the target specifications of the dual-mode NS-SAR ADC. As the core of the NS-SA ADC is the ASAR ADC, all the parameters and specifications are the same as for the ASAR ADC except ENOB, SNDR, bandwidth, and sampling-rate. 2-4 bits enhancement in ENOB and 18-24 dB improvement in SNDR need to be achieved in 8-bit ASAR ADC with the help of the NS. To achieve flexibility, it is decided to make the ADC OSR-tunable, supporting OSR values of 8, 16, and 32. For a typical bandwidth of 20 kHz and sampling-rate of 40 kHz case:

-Bandwidth at an OSR value of $8 = \frac{20}{8} = 2.5$ kHz

-Bandwidth at an OSR value of $16 = \frac{20}{16} = 1.25$ kHz

-Bandwidth at an OSR value of $32 = \frac{20}{32} = 0.625$ kHz

-Sampling $-$ rate at an OSR value of $8 = \frac{40}{8} = 5$ kHz

-Sampling $-$ rate at an OSR value of $16 = \frac{40}{16} = 2.5$ kHz

-Sampling $-$ rateat an OSR value of $32 = \frac{40}{32} = 1.25$ kHz

However, the NS-SAR ADC is also intended to feature sampling-rate reconfigurability owing to the use of the ASAR ADC as its core. Therefore, the NS-SAR ADC will be tunable with respect to its bandwidth, sampling-rate and OSR values. Besides NS or free-running mode, the ADC is expected to exhibit incremental mode operation too for great flexibility. The NS mode enables the use of the ADC for a single channel or sensor, while the incremental mode facilitates its use for multiple channels or sensors, as explained with detail in chapter 1 (section 1.7.7).

Table 4. 1. Targeted specifications of dual-mode NS-SAR ADC

Parameter/Specifications	**Value**
Technology Process (µm)	AMS 0.35
Operating Modes	NS/Free running; Incremental
Resolution (Bits)	10-12
Improvement in ENOB of ASAR ADC (Bits)	2-4
Typical Bandwidth (kHz)	20*
OSR	Tunable (8, 16, and 32 in both modes)
ENOB (Bits)	10-12
Typical $f_s(kHz)$	40*
SNDR (dB)	66-72
Improvement in SNDR of ASAR ADC (dB)?	18-24
P_{cons} (µW)	As low as possible
Input Signal Swing (V)	0.65-2.65 centered at 1.65 V
Supply (V)	3.3/1.2**
Offset error	Must be Temperature-insensitive
Gain Mismatch	Must be Temperature-insensitive
Architecture	Single-ended
Special Techniques for Radiation-hardened operation?	No

* Same as for the ASAR ADC; these are reconfigurable for NS-SAR ADC too as for the case of ASAR ADC

**Two versions of the NS-SAR ADC are intended to be designed: one with a supply voltage of 3.3 V, other with delay-cell and digital section operating at 1.2 V

4.3. Dual-Mode NS-SAR ADC: System Level Considerations

4.3.1. Error-Feedback (EF) vs Cascade of Integrators Feedforward (CIFF) Noise-Shaping Topology

The first key step to introducing NS in the ASAR ADC is to decide the type of NS. As described in chapter 2 (section 2.3.3.1), two types of NS are widely used: EF and CIFF. The EF topology has been preferred because of its advantages over the CIFF topology for this design. The primary goal of the design is to achieve NS functionality without minimum modifications to the standard ASAR ADC to save the area, power, and cost. Comparison of the EF topology with the CIFF reveals that the EF topology is well suited to this criterion. It is because the CIFF topology needs a three-input comparator for realization of loop filter of NS besides other components. This simply means redesign of the comparator for the NS-SAR ADC, leading to extra design efforts, area, power, and cost. In contrast, the EF topology does not need any such comparator. In addition, the CIFF topology needs high gain, i.e., integrators or IIR filter to suppress the quantization noise, which enhances circuit power, area, and complexity. On the other hand, EF topology utilizes a simple Finite Impulse Response (FIR) filter to suppress the quantization noise.

4.3.2. Order of Noise-Shaping

As described in chapter 2 (section 2.7), NS SAR ADCs up to an order of 4 have been proposed in the literature. The choice of NS order depends on application requirement. Following formula provides a relationship between the order of NS and ENOB achieved for NS-SAR ADC operating in NS mode:

$$\mathrm{ENOB} = \mathrm{L} + 0.5 \times \mathrm{OSR} \tag{4.1}$$

where:

L = order of NS loop filter

OSR = Oversampling Ratio

As per (4.1), there is an increase of 1.5 bits in ENOB for every doubling the OSR for 1st-order loop filter. Also, ENOB increases by 2.5 bits for every doubling the OSR for a 2nd-order loop filter. For the ASAR ADC with an 8-bit ENOB, the target enhancement in ENOB and SNDR is 2-4 bits and 18-24 dB, respectively. Assuming a 1st-order loop filter and an OSR of 8,

$$\mathrm{ENOB} = \mathrm{L} + 0.5 \times \mathrm{OSR} = 1 + 4 = 5\ \mathrm{Bits} \tag{4.2}$$

Assuming a 2nd-order loop filter and an OSR of 8,

$$\mathrm{ENOB} = \mathrm{L} + 0.5 \times \mathrm{OSR} = 2 + 4 = 6\ \mathrm{Bits} \tag{4.3}$$

Based on (4.2), 1st-order loop filter provides a theoretical rise of 5 bits in ENOB of 8-bit ASAR ADC. This is one bit more than the required ENOB. This additional bit is good to have initially since circuit imperfections may degrade the increase in the number of bits in later design stage. The use of a 2nd-order loop filter provides an increase of 6 bits to the 8-bits ASAR ADC, which leads to total ENOB of 14 bits from the NS-SAR ADC. Although a 2nd-order NS seems attractive because of the increase of one additional bit over 1st-order NS, its circuit implementation is more complex than 1st-order NS implementation. This complexity results in more chip-area occupation, power consumption, and sources of noise. Based on these factors, 1st-order NS has been chosen for this design.

4.3.3. Selection of OSR Value

The selection of the OSR value for NS-SAR ADC depends on the ENOB of the ASAR ADC and sampling-rate of NS-SAR ADC required by the application. ENOB of ASAR ADC (8 bits) and target ENOB of NS-SAR ADC (10-12 bits) are known for the design. Equation (4.1) shows the relationship between the ENOB

rise and OSR value for different NS orders. With 1st-order NS, the minimum OSR value needed to get target ENOB (10-12 bits) from NS-SAR ADC is 8. OSR is defined as:

$$\mathrm{OSR} = \frac{\mathrm{f_s}}{\mathrm{BW}}$$

where:

$\mathrm{f_s} = \mathrm{sampling} - \mathrm{rate\ as\ per\ the\ nyquisit\ criteria}$

$\mathrm{BW} = \mathrm{Nyquisit\ bandwidth}$

Or,

$$\mathrm{f_s} = \mathrm{OSR(BW)} \tag{4.4}$$

For the case of typical bandwidth of 20 kHz and sampling-rate of 40 kHz for the ASAR ADC, the resulting bandwidth and sampling-rates for NS-SAR ADC with an OSR value of 8 come out to be 2.5 kHz and 5 kHz, respectively. However, the ASAR ADC is sampling-rate reconfigurable with a maximum sampling-rate of 167 kHz. Therefore, it is highly incentivized to make the NS-SAR ADC tunable with respect to OSR value. Therefore, OSR values of 8, 16, and 32 have been chosen for the design to introduce flexibility in the ADC. Table 4.2 shows the resulting sampling-rate and bandwidths for different OSR values for 1st-order NS-SAR ADC.

Table 4. 2. Resulting sampling-rates, bandwidths, and theoretical ENOB of NS-SAR ADC by using OSR values to sampling-rate reconfigurable ASAR ADC

f_{sASAR}/OSR	8			16			32		
	f_{sNS} (kHz)	BW_{NS} (kHz)	ENOB (Bits)	f_{sNS} (kHz)	BW_{NS} (kHz)	ENOB (Bits)	f_{sNS} (kHz)	BW_{NS} (kHz)	ENOB (Bits)
40 kHz	5	2.5	13	2.5	1.25	14.5	1.25	0.625	16
71.43 kHz	8.92	4.46	13	4.46	2.23	14.5	2.23	1.12	16
100 kHz	12.5	6.25	13	6.25	3.125	14.5	3.125	1.56	16
119 kHz	14.875	7.44	13	7.44	3.72	14.5	3.72	1.86	16
131.58 kHz	16.44		13	8.22	4.11	14.5	4.11	2.05	16
142.86 kHz	17.85	8.92	13	8.92	4.46	14.5	4.46	2.23	16
153.85kHz	19.23	9.62	13	9.62	4.80	14.5	4.80	2.40	16
167 kHz	20.875	10.44	13	10.44	5.22	14.5	5.22	2.61	16

4.3.4. The Need for dual-mode Operation

In multi-channel ASIC or multi-sensor applications, the ADC can be utilized in two ways: first, it can be used for the conversion of the signals coming from a single channel or sensor; second, it can be utilized for converting signals arriving from multiple channels or sensors. In the first case, the ADC is not necessarily required to be reset after the conversion of a particular set of signal samples coming from the channel or sensor. In other words, the ADC does not need to have memory-less operation. The ADC operation in this mode is called free running. It is because the signal coming to the ADC is from the same sensor or channel,

so correlation of the signals does not affect ADC accuracy. In the second case, the ADC needs to be reset after conversion of a certain number of samples, i.e., after converting signal coming from a particular sensor or channel and before starting conversion of signal coming from another sensor or channel. Alternatively, the ADC is required to exhibit memory-less operation in order to maintain its accuracy against correlation of signals from different sensors or channels. This operating mode of ADC is called incremental mode. The choice of using the ADC in memory or memory less approach depends on the desired application. However, it is highly preferred to have an ADC capable of functioning in both the modes (memory or memory-less) to achieve great flexibility and versatility in the design. Because of these reasons, dual-mode operation has been introduced to the NS-SAR ADC since the target application of the ADC is multi-channel ASIC.

4.4. Architecture and Working Principle

This section describes the architecture and operation of dual-mode NS-SAR ADC, first in NS or free-running mode, and then in incremental mode. The selection of mode can be done externally depending on the application and need.

4.4.1. Mode 1: Noise-Shaping/ Free-Running Mode

Figures 4.1 and 4.2 show the architecture and timing waveforms, respectively of the NS-SAR ADC in NS/free-running mode. The core of the NS-SAR ADC consists of an 8-bit f_s-reconfigurable ASAR ADC, whose design detail is provided in chapter 3. The first step towards NS implementation is the accurate generation of the residue voltage (V_{res}) at the CADC node. Because of its asynchronous nature, well-controlled period (and thus f_s) of the external 'Sample' signal and variable delay-cell, the ASAR ADC has been enabled to complete all 8 conversions before the arrival of the rising edge of the subsequent 'CLKsampling' signal. This provides sufficient time for one additional CDAC switching based on the comparator final decision, thus generating the residue voltage (V_{res}) at the CADC node. V_{res}, including the quantization error and input-referred-noise of the comparator, is processed by a loop filter $L_{EF}(z)$ and added directly to the input signal in the subsequent sampling phase to get EF-NS functionality. For a 1st-order EF-NS method, the transfer function of the loop filter is z^{-1} [253]. Therefore, to shape the generated V_{res} using 1st-order EF-NS method, it first needs to be sampled and then added to the input signal during the subsequent sampling phase with a multiplication factor of 1. This has been achieved by using an FIR filter, as shown in Figure 4.1.

The operation of the FIR filter and ADC is shown by the timing waveforms of Figure 4.2. Once V_{res} is available after the CDAC switching and settling based on the comparator last decision (after the rising edge of the 'EoC' signal), it is sampled by capacitor C_1 of the FIR filter by applying appropriate clock phases (S and S'). The sampled V_{res} is added to the input signal during the subsequent sampling phase of the ASAR ADC. The duty-cycled OP-AMP of the FIR filter, which acts as a unity-gain buffer to give a gain of 1 in the transfer function, is turned-on just before the arrival of the subsequent sampling phase, as shown by the 'Enable' waveform in Figure 4.2. After the sampling phase, the ASAR ADC starts its conversion phase until the arrival of the 'EoC' signal, as shown in Figure 4.2, where output data is available. After this and before the next sampling phase of the ASAR ADC, V_{res} is generated again; it is first sampled by the FIR filter and then transferred to the coming sampling phase of the ASAR ADC. This process continues for all the successive rising edges of the 'CLKsampling' signal.

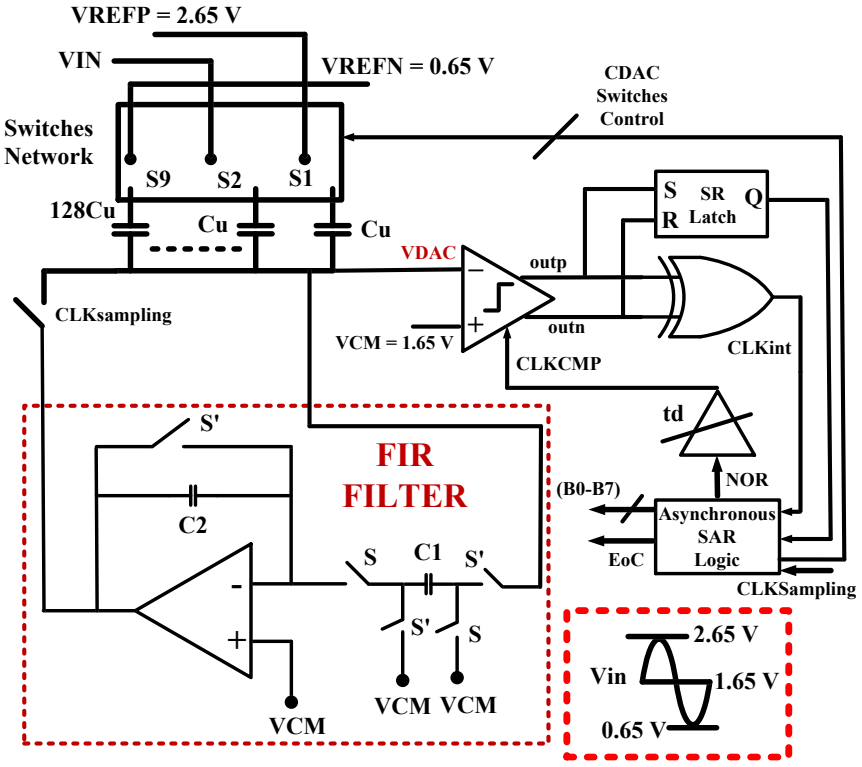


Figure 4. 1. Architecture of dual-mode NS-SAR ADC in NS/free-running mode.

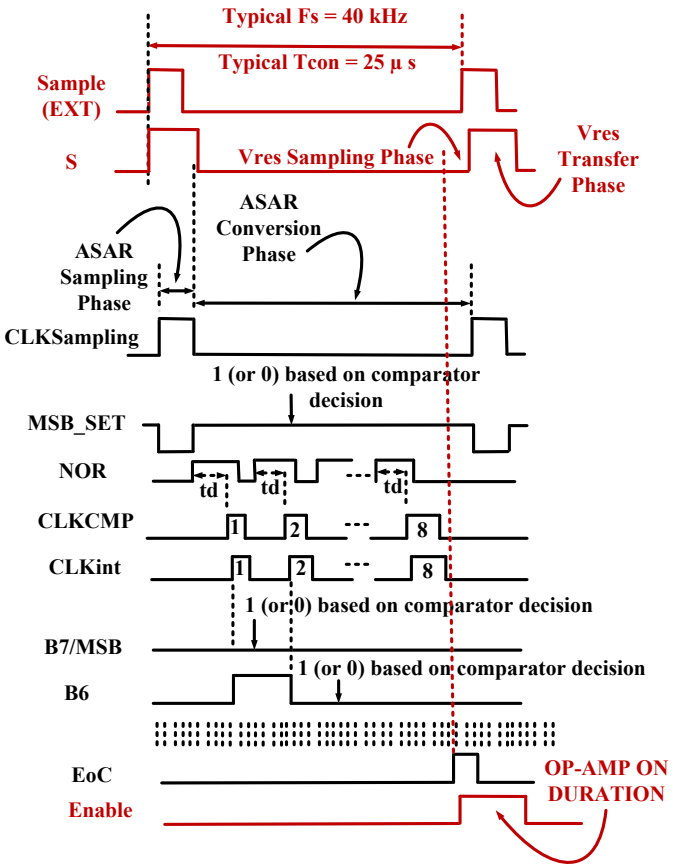


Figure 4. 2. Operation of dual-mode NS-SAR ADC in NS/free-running mode.

4.4.1.1. Sampling-Rate Reconfigurability in Noise-Shaping/ Free-Running Mode

The f_S-reconfigurability of the NS-SAR ADC is inherited from the f_S-reconfigurability of the ASAR ADC, and it is illustrated in Figure 4.3. As described in detail in chapter 3, the f_S-reconfigurability has been achieved by varying the frequency of the external 'Sample' clock which determines the f_s of the ADC by controlling the 'CLKsampling', integrating 8 voltage reference buffers slices in parallel with an external enable and disable functionality, and introducing an externally controlled variable rising edge only delay-cell. The minimum and maximum f_s of the NS-SAR ADC is 40 kHz and 167 kHz, respectively, which results in an equivalent sampling-rate of 5 kHz and 20.875 kHz with an OSR of 8. The f_S-reconfigurability is also achievable with an OSR of 16 and 32, thus changing accordingly the equivalent sampling-rates of the NS-SAR ADC. Like the ASAR ADC, power consumption of the NS-SAR ADC in NS/free running mode is also proportional to its sampling-rate. In other words, it exhibits a constant energy-efficiency at all its covered sampling-rtes.

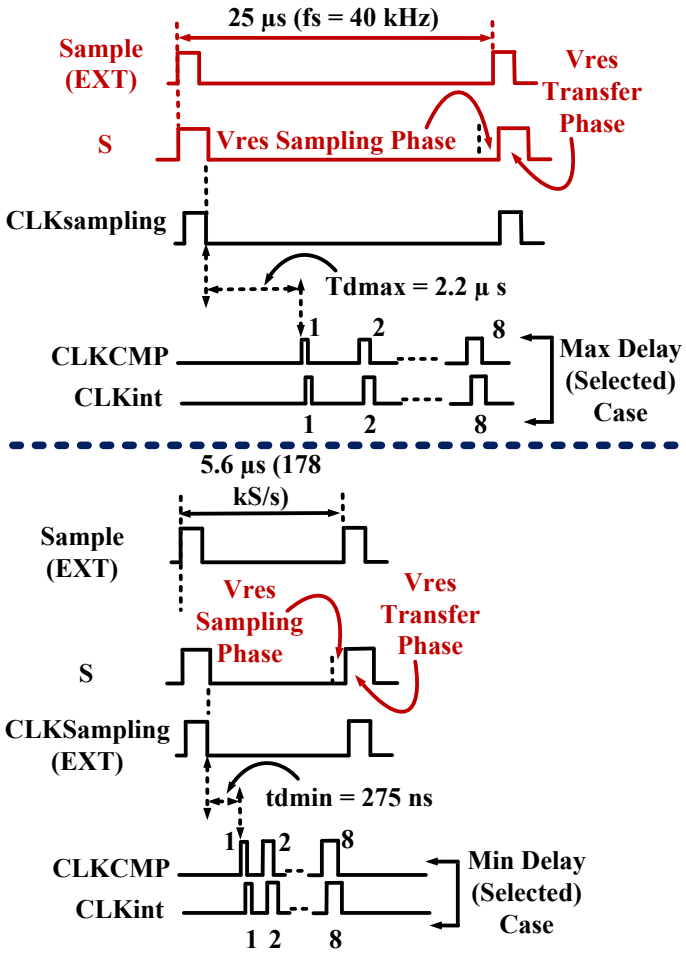


Figure 4. 3. f_S-reconfigurability operation of NS-SAR ADC in NS/free-running mode.

4.4.1.2. Versatility and Flexibility of NS-SAR ADC in Noise-Shaping/ Free-Running Mode

Compounded with sampling-rate reconfigurability, there is another factor which enhances flexibility and versatility of the NS-SAR ADC. Like the ASAR ADC, it is also adaptable with respect to the duty-cycle of 'Sample' signal besides its frequency. For example, varying the logic high duration of the 'Sample' signal has a direct effect on the settling requirements as well as power consumption of the input (V_{IN}) and common mode (V_{CM}) buffers, because these buffers are needed and thus enabled only during the sampling phase. There are scenarios where the duration of the sampling phase can be reduced. The cases where input and

common buffers are implemented off-chip is one such scenario. Because of off-chip buffers, the duration of sampling phase of the ADC can be reduced, which results in an enhanced time for the conversion phase. Another such situation can be the use of ADC for analog front ends of ASICs or sensors accompanied by a sample and hold circuit by itself, such as VEGA ASIC of [11]. Figure 4.4 shows a pictorial representation of the NS-SAR ADC working with reduced sampling phase.

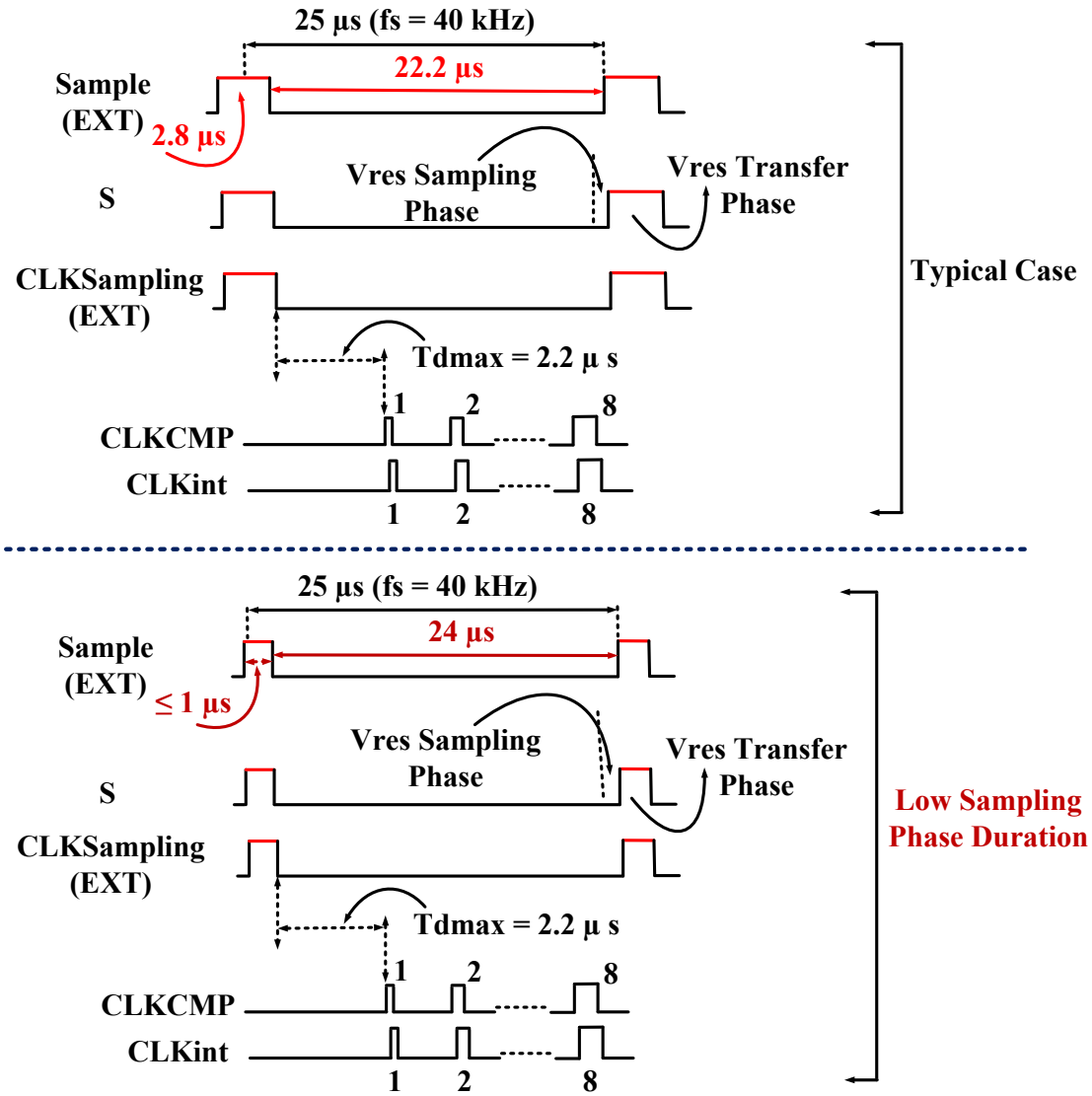


Figure 4. 4. Flexibility of NS-SAR ADC with respect to 'Sample' signal: ADC timing waveforms with reduced sampling phase duration, which can relax the settling time and power consumption of input and common mode buffers.

The fact that the 'Sample' clock is tunable with respect to its frequency can also be useful for sampling-rates lower than typical (40 kHz) assuming an OSR of 8, as is the case for the ASAR ADC. Considering the case of a 4 kHz sampling-rate, as shown in Figure 4.5, the 'Sample' clock can be applied accordingly. In this case, the ADC performs all 8 conversions well before the arrival of the rising edge of the next 'Sample' signal and becomes idle, thus consuming no power. This scenario is particularly attractive if the voltage refence buffers are either implemented off-chip or they are tuned off right after the completion of all 8 conversions by the ADC.

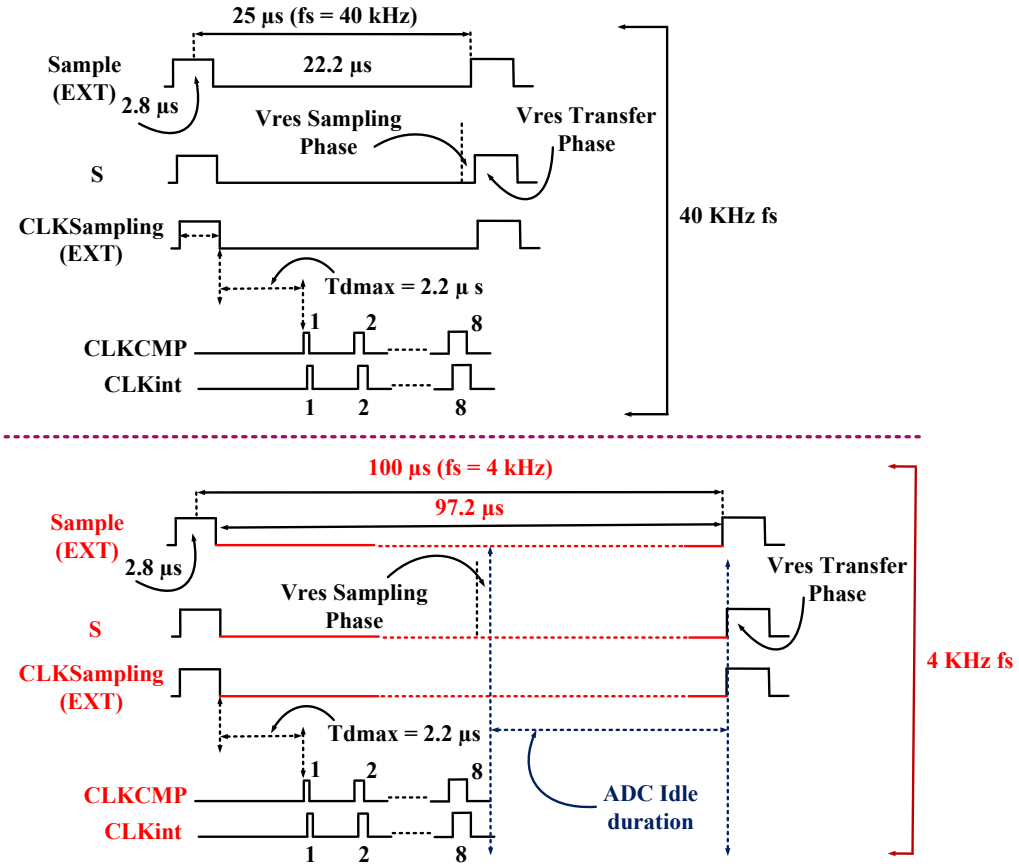


Figure 4. 5. Flexibility of ADC with respect to 'Sample' signal: ADC timing waveforms with a sampling-rate lower (4 kHz) than typical (40 kHz). ADC has the ability to consume no power during its idle duration.

4.4.2. Mode 2: Incremental Mode

Figure 4.6 depicts the architecture of the dual-mode NS-SAR ADC in incremental mode. To introduce a 1st-order incremental mode functionality into the NS-SAR ADC, the reset operation needs to be performed after a certain period, depending on the OSR value. Besides the reset operation, on-chip decimation is also essential. For the 1st-order incremental mode functionality, the decimation is simply a sum-of-sum operation before the reset operation. Both of these functions have been achieved by the use of a dedicated digital logic, as shown in Figure 4.6.

The timing waveforms of Figure 4.7 illustrate the operation of the ADC in incremental mode. The operation in incremental mode is similar to the NS mode except decimation and reset functions. ADC starts its working in free-running mode, i.e., it performs 1st -order NS by first sampling the V_{res} and then transferring it to the next sampling phase. At the rising edge of each EoC signal, sum-of-sum function is performed. At the arrival of the rising edge of the first EoC signal (also for all EOC after the reset operation), the output data is calculated as follows:

$$\text{sum} = 0 + \text{NS\_data}$$

At the arrival of the other EoC signals, the output data is calculated as follows:

$$\text{sum} = \text{sum} + \text{NS\_data}$$

This process continues until the reset function. The reset is performed based on the OSR value. For an OSR value of 8, the reset is performed after each 8 'Sample' clock cycles. During the reset operation, V_{res} is not transferred to the sampling phase. Instead, V_{CM}voltage is connected to the top plates of the CDAC. The

sum-of-sum based output data is ready to be acquired at the rising edge of the EoC_INC signal. After the reset, the ADC starts its operation again and works in exactly the same manner as described above until the next reset operation after 8 'Sample' clocks. This process continues for all other conversions.

Like NS mode, the incremental mode also operates for OSR values of 8, 16, and 32. The decimation and reset operation is adjusted according to the selected OSR values with the help of digital logic. A 2-bits external signal (Mode<1:0 in Figure 4.6) is used to control the ADC mode of operation as well as its OSR value according to the manner shown in Table 4.3. The ENOB, sampling-rate, bandwidth, and power dissipation change according to the selected OSR values in both modes. This adds great flexibility and versatility in the ADC design with respect to these parameters and makes it attractive not only for multi-channel/multi-sensors application, but also for variety of other useful applications.

Table 4. 3. The dual-mode NS-SAR ADC modes of operation and OSR values selection using external control bits

Mode<1:0> value (External control bits)	ADC Operating Mode	OSR
0	NS/Free running	8, 16, 32
1	Incremental	8
2	Incremental	16
3	Incremental	32

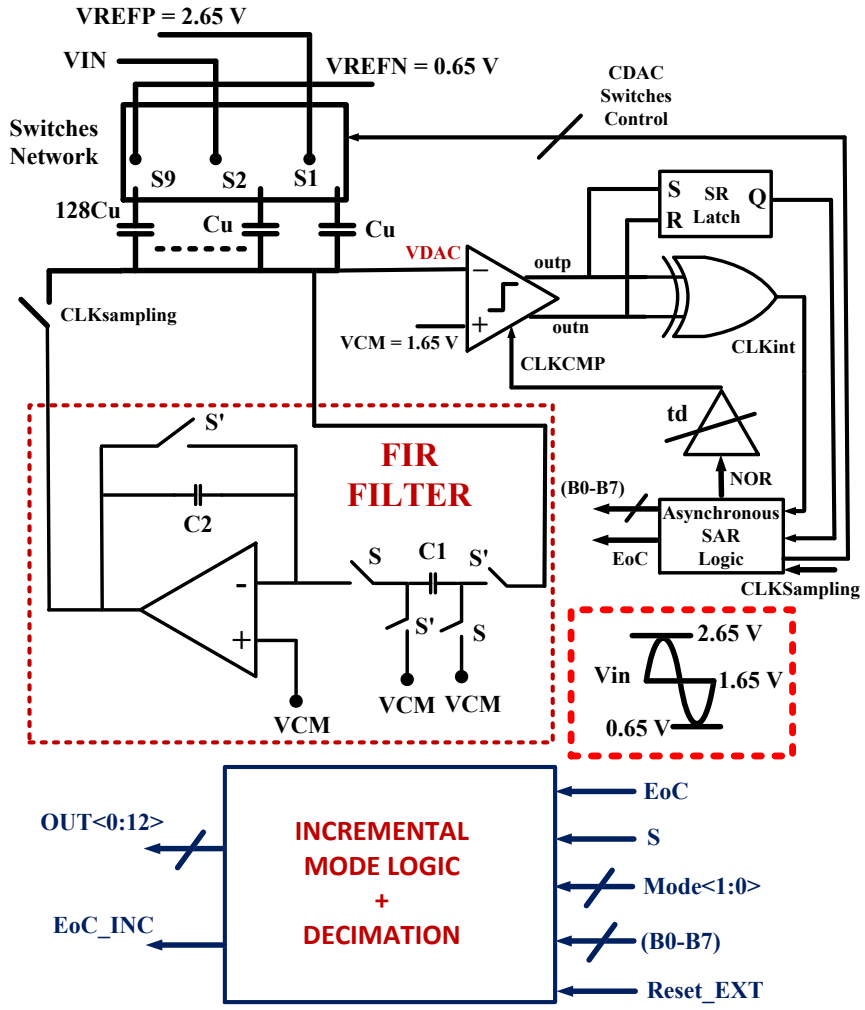


Figure 4. 6. Architecture of the dual-mode NS-SAR ADC with incremental mode included.

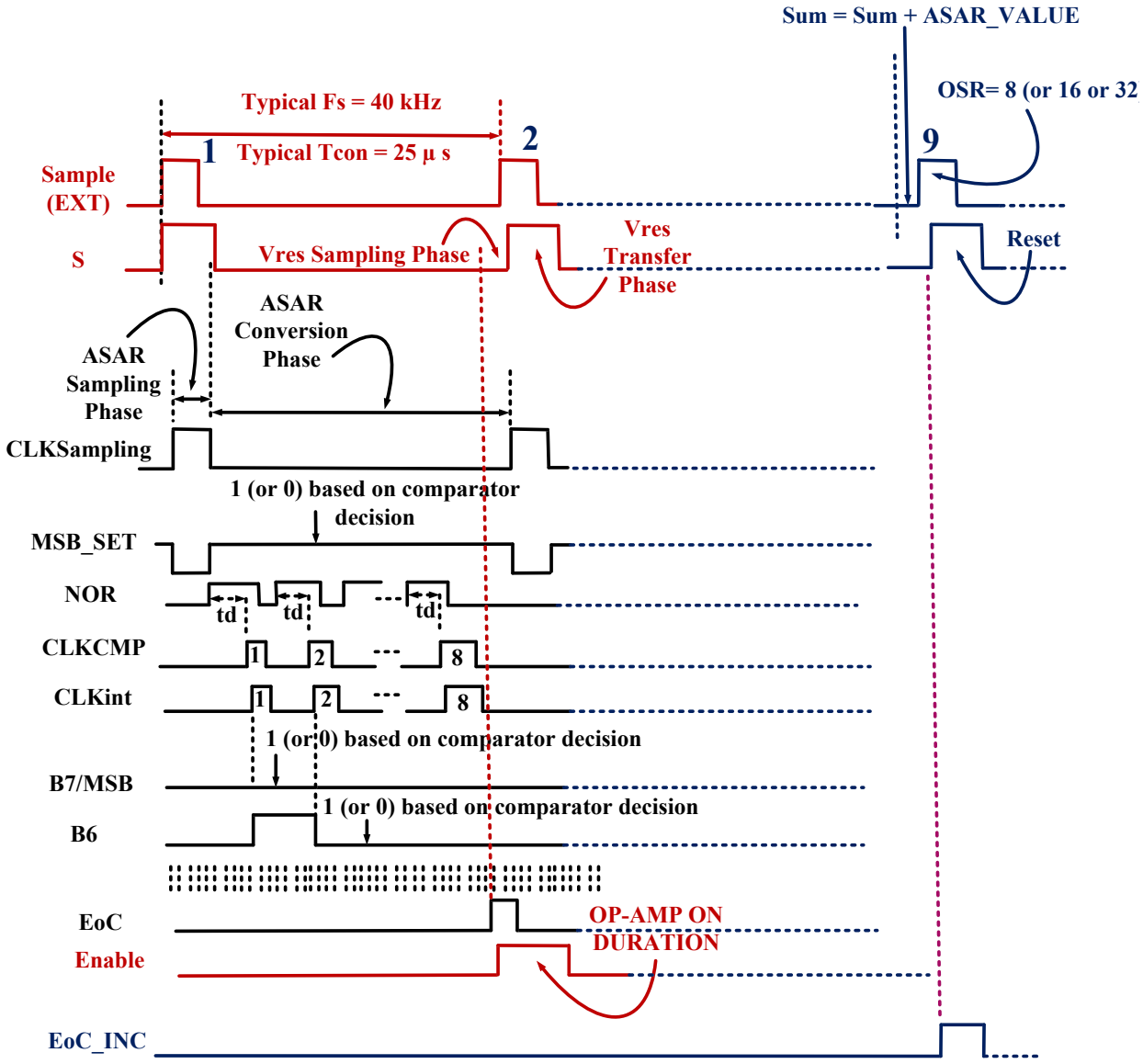


Figure 4. 7. Operation of the dual-mode NS-SAR ADC in incremental mode.

4.4.2.1. Sampling-Rate Reconfigurability and Adaptability in Incremental Mode

NS-SAR ADC in incremental mode also exhibits f_S-reconfigurability functionality, which is primarily inherited by the f_S-reconfigurability feature of the ASAR ADC, being its core. Illustration of f_S-reconfigurability in incremental mode is shown in Figure 4.8. The operating principle is the same as for NS mode except the reset and decimation functionality. Selection of sampling-rates as well as OSR value can be done externally as well as independently. Energy-conversion of the ADC for all the supported sampling-rates is constant. ENOB, SNDR, sampling-rate, bandwidth, and power dissipation vary according to the OSR. These features stupendously enhance the ADC potential, where a variety of parameters can be chosen according to the target application.

Like the ASAR and NS-SAR ADC in NS mode, the dual-mode NS-SAR ADC in incremental mode is also flexible with respect to the duty cycle of its external 'Sample' clock. For example, width of its sampling phase can be reduced or increased as per the target application, which is directly related to the requirements (e.g., settling) of the input and common mode buffers as well as OP-AMP of FIR filter. As the OP-AMP of FIR filter is duty-cycled and its activation duration is controlled by the 'Sample' clock, it does not pose any

restriction to the advantage of ADC from the 'Sample' signal duty-cycle point of view. In addition, the ADC in incremental mode adjusts its operation accordingly for a sampling-rate lower than typical 40 kHz (5 kHz in incremental mode for an OSR of 8), adding further flexibility into its features.

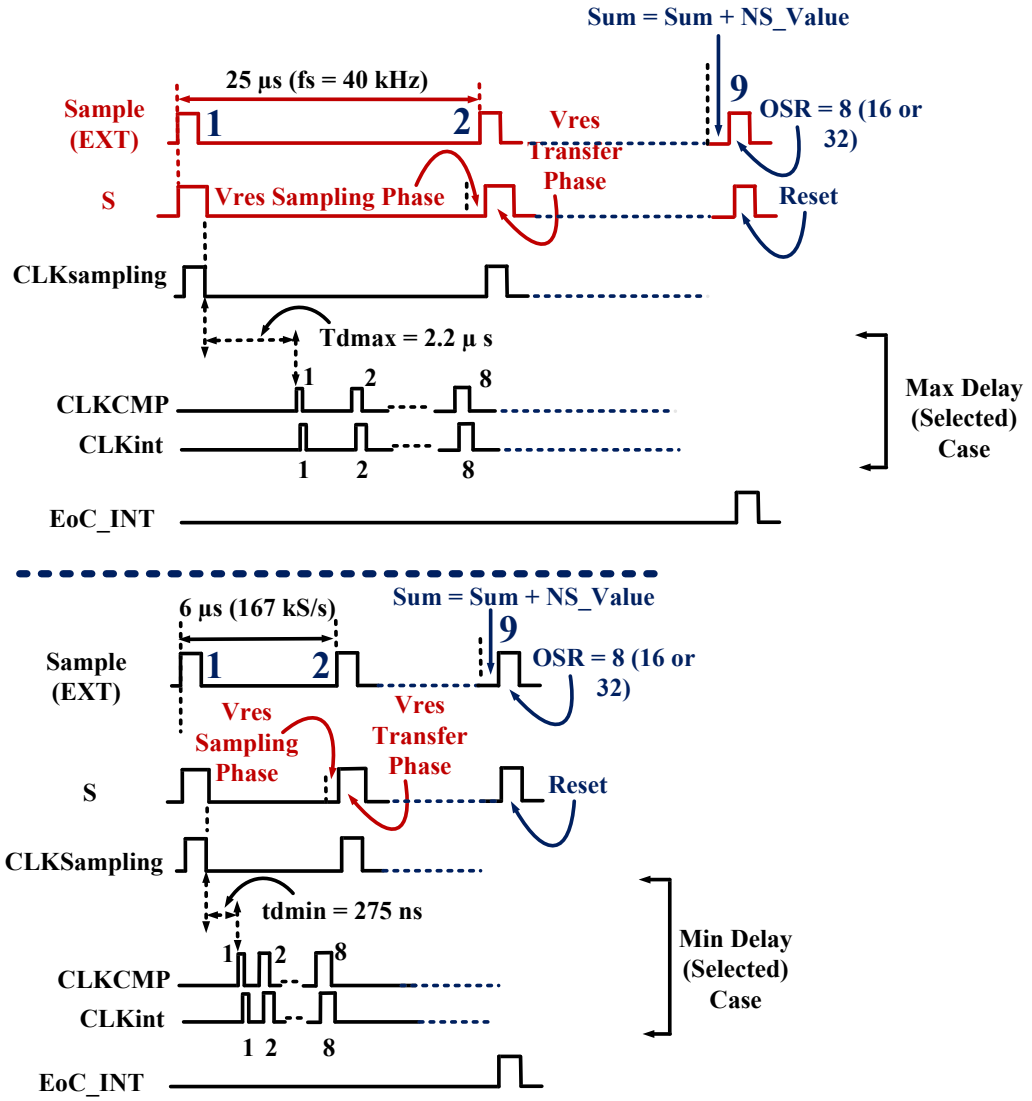


Figure 4. 8. f_s-reconfigurability operation of NS-SAR ADC in incremental mode.

4.5. Verilog-A Implementation

The dual-mode NS-SAR ADC design process started from its Verilog-A based implementation. As the core of the NS-SAR ADC is an 8-bit ASAR ADC whose Verilog-A implementation is part of chapter 3 (section 3.6), this section covers only the detail of the additional aspects, i.e., introduction of 1st-order EF NS with its dual mode operation (NS mode and incremental mode).

4.5.1. Fundamentals of EF NS Topology

As stated earlier, 1st-order EF NS topology has been selected for this design. Based on the discussion in chapter 2 (section 2.3.3.1), there are two ways to implement NS-SAR ADC: Error-Feedback (EF) and Cascaded-Integrators-Feed-Forward (CIFF). In both types of topologies, the first important step is an accurate generation of V_{res}, which is freely available in a SAR ADC. The freely available V_{res}, if applied

to the subsequent sampling phase of the SAR ADC, realizes a long-established ΔΣ modulator with an inherent EF Noise-shaping. This, with a combination of oversampling, provides an enhanced performance (ENOB and SNDR). Besides quantization error, the NS-SAR shapes the comparator noise out of the band of interest. In addition, the $^{kT}/_{C}$ noise of the CDAC is also shaped. The EF NS-SAR (Figure 4.9) is achieved by using a Finite-impulse-response- filter (FIR), which processes the V_{res} before feeding it back to the next sampling phase. With the FIR filter, it is possible to shape the noise only without the signal, as written in (4.5)

$$D_{OUT} = V_{in} + [1 - L_{EF}(z)].(Q_e + n_{cmp}) \tag{4.5}$$

where, $STF = 1$ and $NTF = 1 - L_{EF}(z)$

For a 1st-order EF NS, NTF is given by (4.6),

$$NTF = 1 - z^{-1} \tag{4.6}$$

where,

$$L_{EF}(z) = z^{-1} \tag{4.7}$$

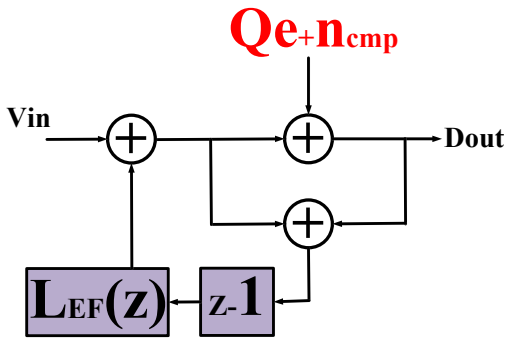


Figure 4. 9. Signal-flow-graph of the EF NS-SAR.

4.5.2. Residue Voltage Generation

The first step in the design process is an accurate generation of the quantization error (Q_e) or residue voltage (V_{res}) from 8-bit ASAR ADC. The quantization error is defined by (4.8):

$$D_{out} = V_{in} + Q_e \tag{4.8}$$

In a traditional ASAR ADC, the residue information generated by the ASAR ADC at the end of the conversion phase is discarded during the next sampling phase, i.e., it is not used or transferred to the next sampling phase. In addition, the last decision of the comparator is not fed back to the DAC array because of the completion of the conversion process after the LSB decision. Therefore, V_{DAC} generated is the difference between sampled input and a 7-bit digital output. In other words, it can be described by (4.9),

$$V_{res} = D_{out7bits} - V_{in} \tag{4.9}$$

To generate the difference between 8 bits digital output data and sampled input, one extra CDAC array switching based on the last decision of the comparator is needed. With this extra CDAC switching, the voltage at the CDAC node is actually V_{res}, given by (4.10),

$$V_{res} = D_{out} - V_{in} \tag{4.10}$$

For the ASAR ADC, the architecture has been designed in such a way that it already makes an extra CDAC switching based on the final decision of the comparator, thus generating V_{res}. As the delay-cell is variable,

its value has been slightly adjusted to create adequate time for V_{res} generation right after the conversion phase and before the arrival of next sampling phase. The pictorial representation of V_{res} generation is shown in Figure 4.10. Figure 4.11 depicts plot of V_{res} generated from the ASAR ADC. It is obvious that V_{res} lies within 1 LSB of the ADC.

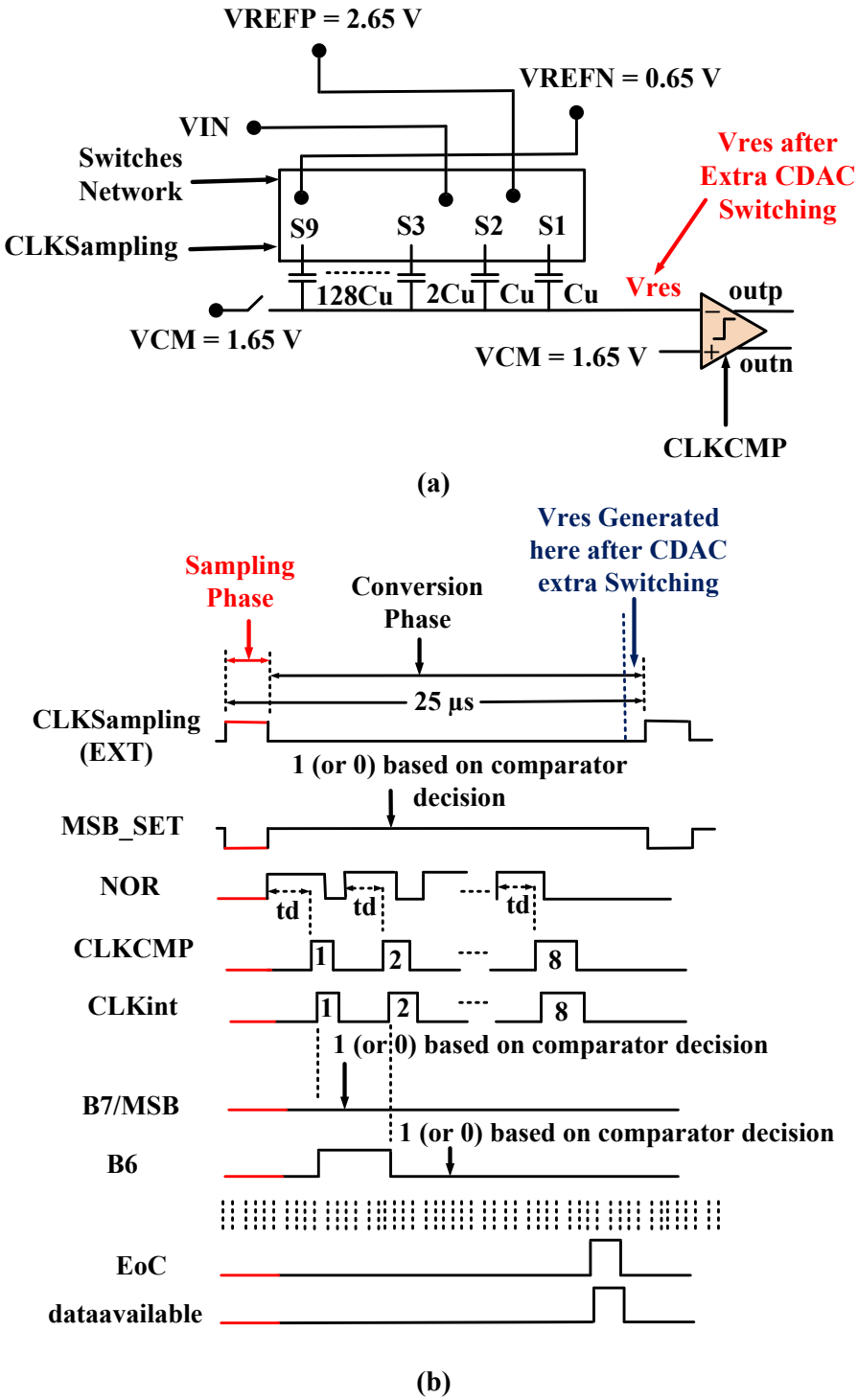


Figure 4. 10. Generation of V_{res} from ASAR ADC: (a) schematic diagram showing extra CDAC switching, and (b) timing waveforms depicting generated V_{res} at the end of the conversion phase based on CDAC extra switching.

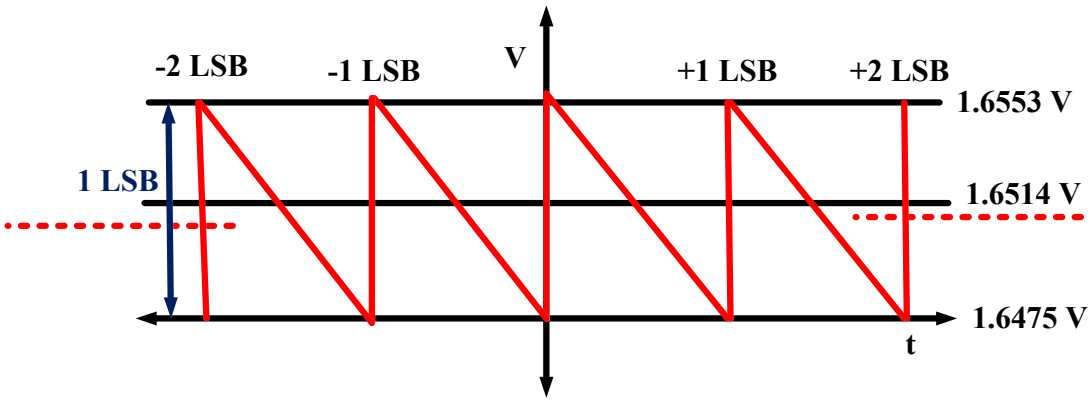


Figure 4. 11. Plot of V_{res} generated from the ASAR ADC.

4.5.3. Loop Filter Implementation to get NS-SAR ADC in NS/Free Running Mode

After an accurate generation of V_{res}, the next step is the realization of loop filter ($L_{EF}(z)$) function of equation (4.7). This has been done by the use of a 1st-order FIR filter shown in Figure 4.12. It consists of switches, capacitors, and an OP-AMP. FIR filter has two operation phases: first, V_{res} sampling and second, V_{res} transfer to the subsequent sampling phase. Working of FIR filter can be described as follows:

Sampling phase starts at the rising edge of the S' signal. During this phase, the input voltage to FIR filter is sampled on capacitor C_1, as shown in Figure 4.13 (a). At the rising edge of the S signal, the sampled voltage at C_1 is transferred to the output of FIR filter because of the unity gain configuration of OP-AMP, as depicted by Figure 4.13 (b). This way, there is a delay of one clock cycle between the sampling of the input and transfer to its output, thus realizing z^{-1} as required by the loop filter. In addition, the values of both the capacitors are equal to ensure unity gain inverting configuration of OP-AMP during the transfer phase, as required by the loop filter characteristics.

For FIR filter, Verilog-A model of OP-AMP has been used. Also, a voltage-controlled voltage source (VCVS) from Cadence AnalogLib has also been used as an ideal OP-AMP. All the switches are modelled in Verilog-A, whose Verilog-A codes can be seen in Appendix 1. Ideal capacitors from AnalogLib have been used. Initially, values of both the capacitors have bene chosen as the unit capacitor value of the CDAC, i.e., 20 fF. This way, the circuit of FIR filter is realized and combined with the Verilog-A based model of the ASAR ADC to build the NS-SAR ADC. This realizes the 1st order EF NS-SAR ADC in NS/free running mode.

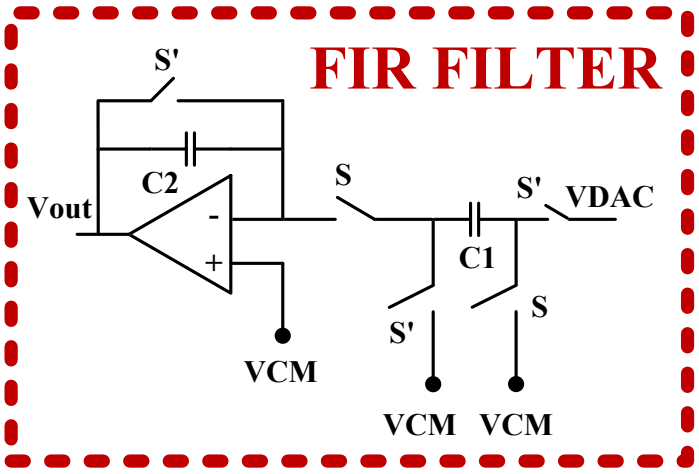


Figure 4. 12. Schematic of FIR filter.

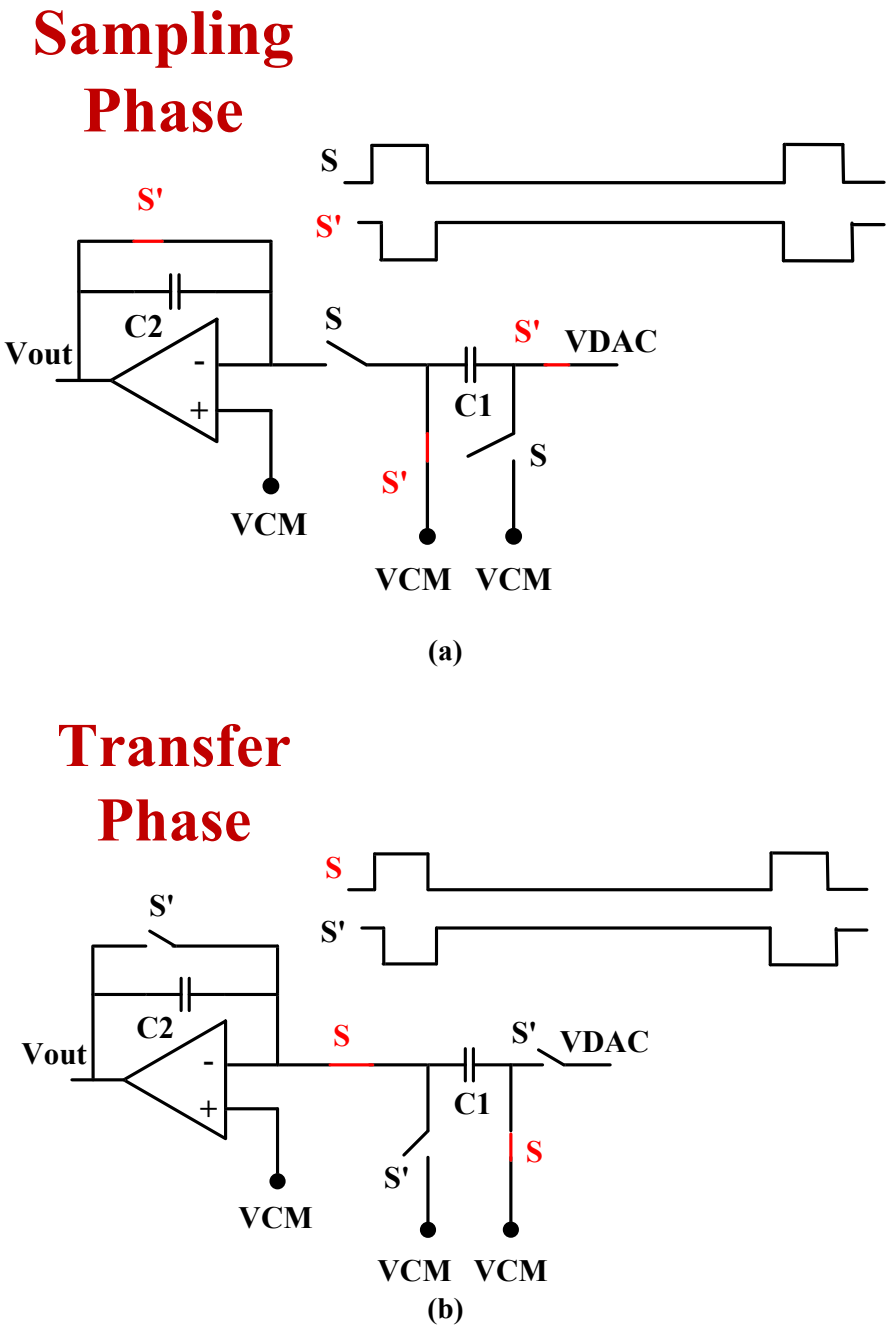


Figure 4. 13. Operation of FIR filter: (a) sampling phase, and (b) transfer phase.

4.5.4. Realization of Incremental Mode to develop Dual-Mode NS-SAR

Incremental mode operation has been realized by resetting the NS-SAR ADC after certain clock periods depending on OSR value and performing 1st-order decimation (sum-of-sum), as described in section 4.4.2. Both of these functions have been achieved with Verilog-A model-based blocks. Verilog-A codes of the relevant blocks are listed in Appendix 2. The block diagram of the dual mode ADC and its operation is the same as described earlier in section 2.3.3.1.

4.5.5. Verilog-A Implementation based Simulation Results

To verify Verilog-A based implementation of the dual-mode NS-SAR ADC, PSD has been plotted in both modes. Figure 4.14 shows the PSD plots in NS/free running mode, while PSD plots in incremental mode are displayed in Figure 4.15. In NS mode, the ADC achieves an ENOB of 11.5 bits at typical sampling-rate at OSR of 8, which is almost 4 bits higher than the ASAR ADC. While the ADC secures an ENOB of 10.72 bits at an OSR of 8 in incremental mode, which is about 3 bits higher than ASAR ADC. In NS/free running mode, an increase of 1.5 bits in ENOB and 9 dB in SNDR can be witnessed for doubling the OSR value with a 20 dB/dec slope for the quantitation noise shaping effect. These validate correct 1st-order NS functionality exhibited by the ADC. In incremental mode, 1 bit rise in ENOB, and 6 dB raise in SNDR per doubling OSR value can be noticed. The degradation in ENOB and SNDR in incremental mode in comparison with NS mode is because of the reset operation.

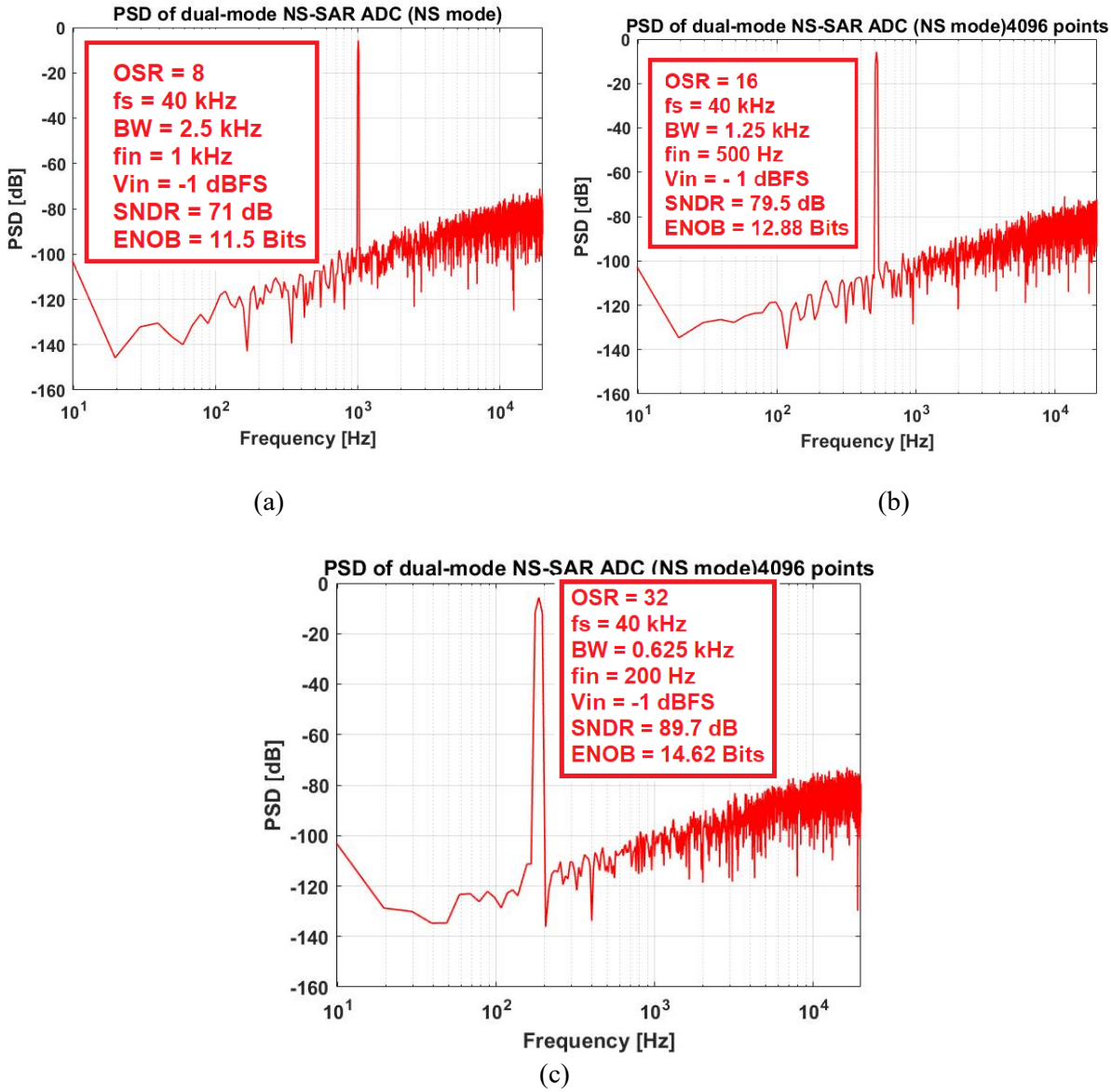


Figure 4. 14. PSD plot of Verilog-A model-based dual mode NS-SAR ADC in NS/free running mode at (a) OSR =8, (b) OSR = 16, and (c) OSR = 32.

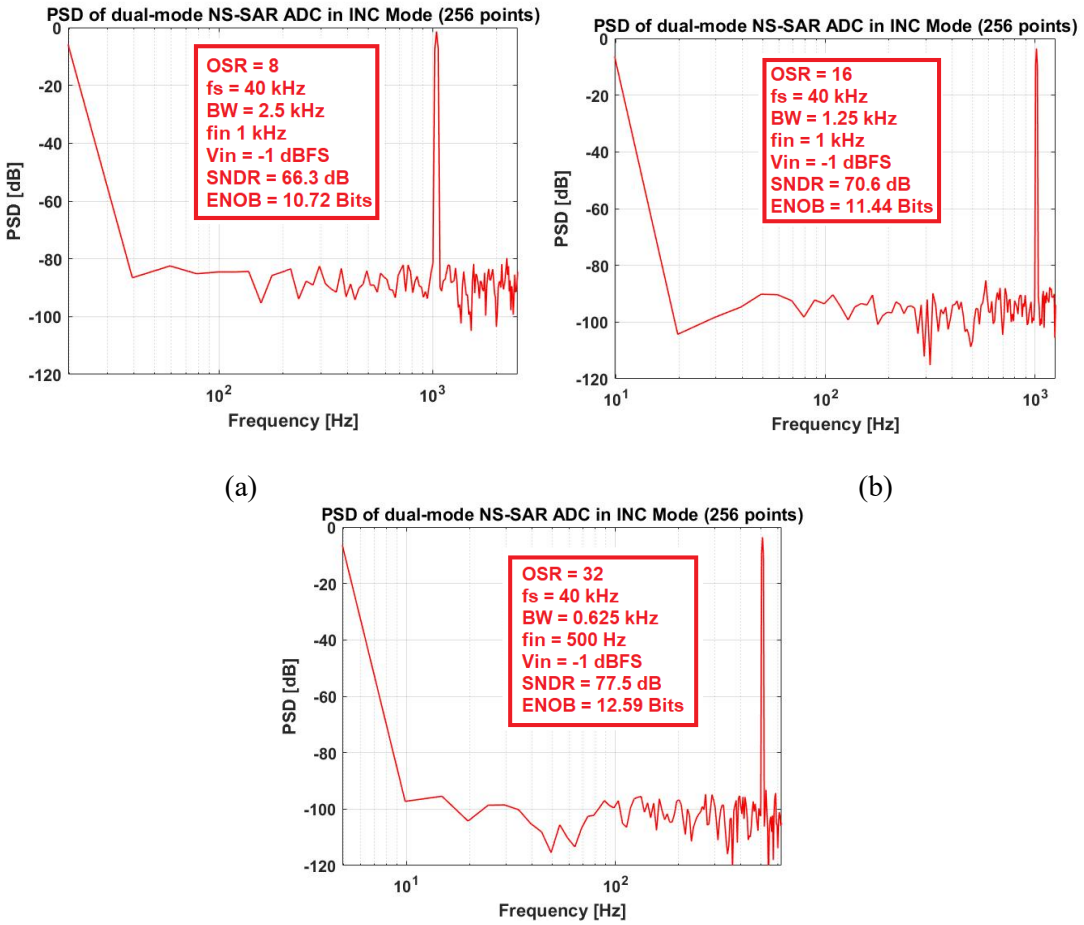


Figure 4. 15. PSD plot of Verilog-A model-based dual mode NS-SAR ADC in incremental mode at (a) OSR =8, (b) OSR = 16, and (c) OSR = 32.

4.6. Circuit Level Implementation and Layout Considerations

After the successful implementation based on Verilog-A modelling, the next step is the schematic level design of the ADC. Schematic level detail of all components of 8-bit ASAR ADC, the core of the dual-mode NS-SAR ADC, is part of chapter 3. Therefore, this section is devoted to the circuit level design detail of the remaining components, i.e., implementation of FIR loop filter, and digital logic for incremental mode operation. Layout considerations of FIR filter is also part of this section.

4.6.1. FIR Loop Filter Implementation

Figure 4.16 shows the circuit diagram of the FIR filter, whose operating principle has already been described in section 4.5.3. It consists of capacitors, switches, and OP-AMP. Design detail of each of these components is provided below.

4.6.1.1. Capacitors Values Selection of FIR Filter

Selection of capacitor values for FIR filter depends on correct implementation of loop filter transfer function, settling time, and $^{kT}/_{C}$ noise requirements. As the transfer function of the loop filter is $-z^{-1}$, equal valued capacitors (C_1 and C_2) are needed to realize unity-gain. As far as the settling is concerned, capacitors with values as minimum as possible are preferred for fast settling. This is to ensure an insignificant increase in the CDAC capacitive load. That in turn is critical for proper settling of all the buffers of the ADC, which have already been designed. A significant increase in CDAC capacitance means

stringent settling requirements for the buffers, which might require redesign of the buffers to meet settling requirements, thus adding substantial complexity in the design. Therefore, selecting the values of these capacitors equal to the unit capacitor value (20 fF) of the CDAC is a good starting point. This value does not affect the settling requirements of any of the buffers. If this value is proved to be not adequate from $^{kT}/_{C}$ noise point of view, it can be enhanced later on. For FIR filter design, poly-poly capacitor has been chosen, which is the same capacitor type selected for the CDAC capacitors.

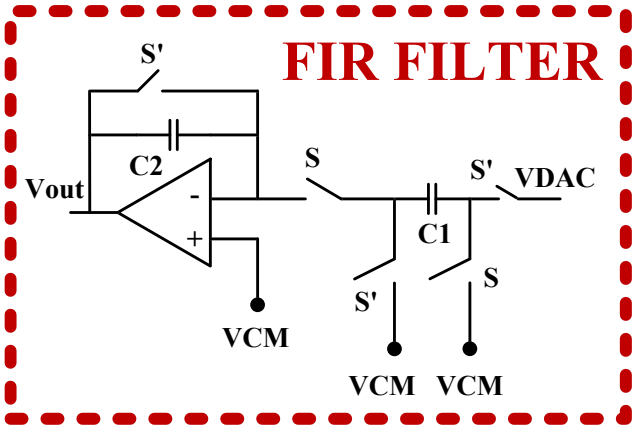
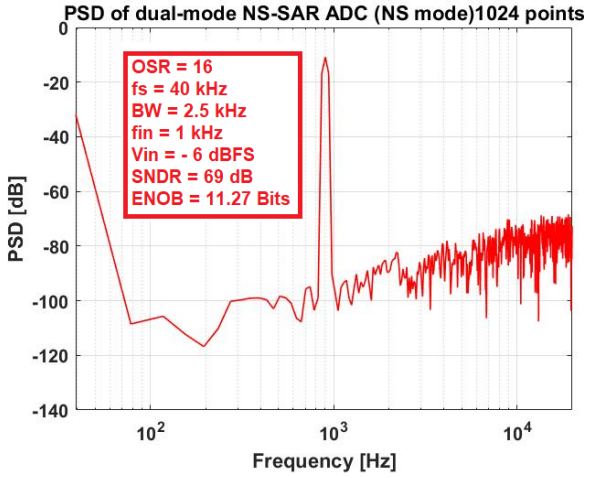
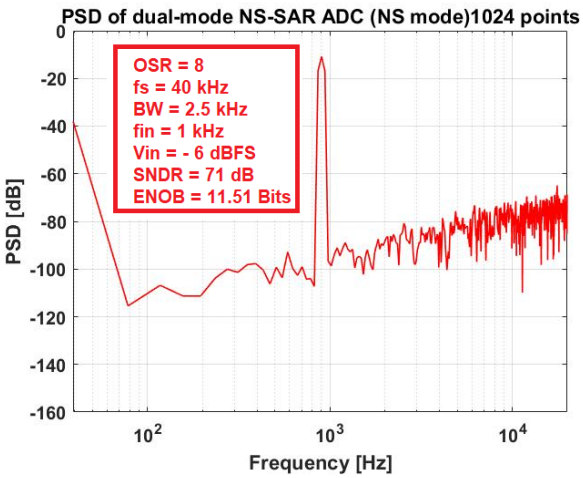


Figure 4. 16. Schematic diagram of FIR filter.

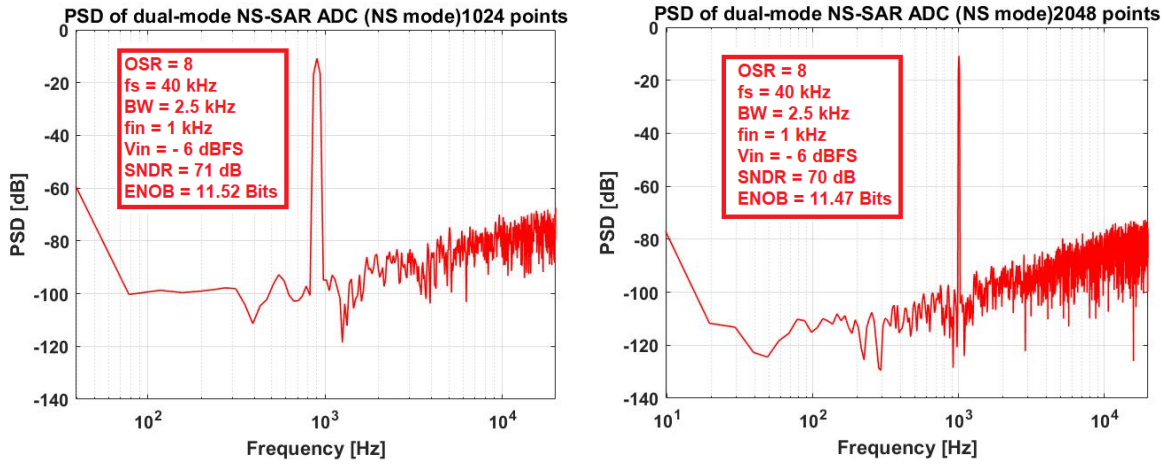
After the initial selection of FIR capacitor values, the next step is to figure out whether this value is satisfactory for $^{kT}/_{C}$ noise. This has been done with the help of the PSD plots of the ADC, where all the components of the NS-SAR ADC are real, except FIR filter whose OP-AMP and switches are ideal. This is to sort out the impact of the $^{kT}/_{C}$ noise of FIR filter capacitors on the ADC performance. Figure 4.17 shows the ADC PSD plots for four different values of capacitors: 20 fF, 40 fF, 60, and 200 fF. These plots reveal that ADC ENOB and SNDR improve by 0.3 bits and 3 dB, respectively when capacitor values are increased from 20 fF to 40 fF. However, no improvement can be noticed for capacitance values of 60 fF or above. Based on these simulation results, 40 fF capacitance value has been chosen for FIR filter capacitors. This value does not affect settling requirements of the buffers. Table 4.4 summarizes ADC performance for different values of FIR filter capacitor.



(a)



(b)



(c) (d)

Figure 4. 17. ADC PSD plots with FIR filter capacitor values of (a) 20 fF, (b) 40 fF, (c) 60 fF, and (d) 200 fF.

Table 4. 4. Summary of ADC performance vs capacitor values of FIR filter

Sr. No.	Capacitor Value (fF)	ENOB (Bits)	SNDR (dB)
1.	20	11.42	69
2.	40	11.51	71
3.	60	11.52	71
4.	200	11.47	70

4.6.1.2. Selection of Switches of FIR Filter

As the range of V_{res} lies within one LSB of the common mode voltage (1.65 V), CMOS transmission gate switches have been chosen for better linearity. To reduce parasitics, minimum size switches ($W = 1\mu m$; $L = 0.35\ \mu m$) have been chosen. In addition, the sizes of all the switches are kept the same. This ensures a constant offset from the input to the output of FIR filter caused by the switches, thus causing no degradation to ADC performance. These sizes of all switches are fine for settling, charge injection, and clock feedthrough. Figure 4.18 shows the PSD of ADC with all real components including switches of FIR filter, except the OP-AMP.

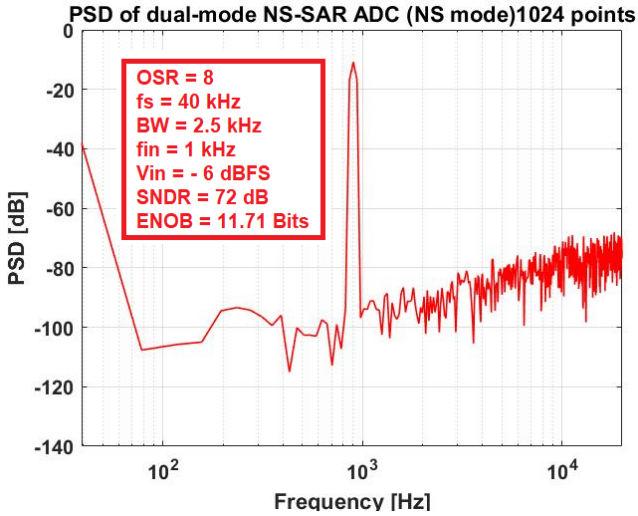


Figure 4. 18. ADC PSD plot with real switches of FIR filter; OP-AMP of FIR filter is ideal for this simulation.

4.6.1.3. OP-AMP Implementation of FIR Filter

The first step in the design of OP-AMP for FIR filter is to derive its specifications. It is evident from the operation of the ADC described in section 4.4.1, OP-AMP needs to be turned on only during V_{res} transfer phase; otherwise, it must be turned off to save power. It is also revealed that V_{res} transfer phase is actually the sampling phase of the ASAR ADC. Therefore, the requirements for OP-AMP of FIR filter should be the same as for the common mode and input buffer of the ASAR ADC since the conditions and requirements (e.g., load, gain-bandwidth, noise, etc.) for both are the same. The only different requirement is the input signal swing, which is lower for the OP-AMP of FIR filter. It is, therefore, judicious to start with the specifications of common mode and input buffer and design the OP-AMP based on these specifications. The OP-AMP designed based on these specifications can be optimized later on. Based on these rationales, Table 4.5 shows the target specifications of FIR filter OP-AMP.

Table 4. 5. A summary of target specifications of OP-AMP of FIR filter

Sr. No.	Parameter	Calculated Value
1.	V_{res} transfer phase duration of ADC	2.78 µs
3.	OP-AMP Settling Time (t_s)	0.6 µs
3.	V_{DD}	3.3 V
4.	DC Gain	~ 60 dB
5.	C_L=C_{DAC}	5.12 pF
6.	Slew Rate (SR)	~ 5 V/µs
7.	GBW	2 MHz
8.	I_{REF}	~ 15 µA
9.	Offset	Temperature independent
10.	Input noise	< ¼ LSB

The next step is the selection of a suitable architecture for the OP-AMP circuit. For simplicity, it is sensible to start with a single stage architecture and see if it can satisfy the OP-AMP requirements and thus provide the needed performance for the ADC. The common mode buffer of the ASAR ADC, described in section 3.7.5.3, looks an attractive choice in this regard since its requirements are similar to the OP-AMP of FIR filter. Figure 4.19 shows the circuit diagram of the common mode buffer and Table 4.6 depicts its achieved specifications, which is to be used as an OP-AMP for FIR filter in the first attempt.

Figure 4.20 shows the PSD plot of NS-SAR ADC with real OP-AMP (common mode buffer) of FIR filter. However, the performance (ENOB of 11. 2 bits and SNDR of 67 dB) is bit degraded from the previous Verilog-A/ideal OP-AMP based ADC performance. It is because the gain (47 dB) of the OP-AMP is not adequate. This pushes the need for architecture with a higher gain. A simple way to enhance the gain is the use of a 2-stage OP-AMP. Open-loop 2-stage amplifier of the input buffer of the ASAR ADC, described in section 3.7.5.2, can be an attractive choice in this regard.

Figure 4.21 depicts the circuit diagram of amplifier of the input buffer, which is to be used as OP-AMP of FIR filter. Table 4.7 lists its specifications. PSD plot of ADC with this OP-AMP is provided in Figure 22. ADC performance (SNDR and ENOB) is fully satisfactory with this OP-AMP circuit. Therefore, this 2-stage OP-AMP has been chosen for FIR filter implementation. To get a duty-cycled operation, switches have been added in the circuit to turn the circuit on only when needed to save its power. OP-AMP is turned on only during V_{res} transfer phase. The complete design process of 2-stage OP-AMP is provided in section 3.7.5.2.

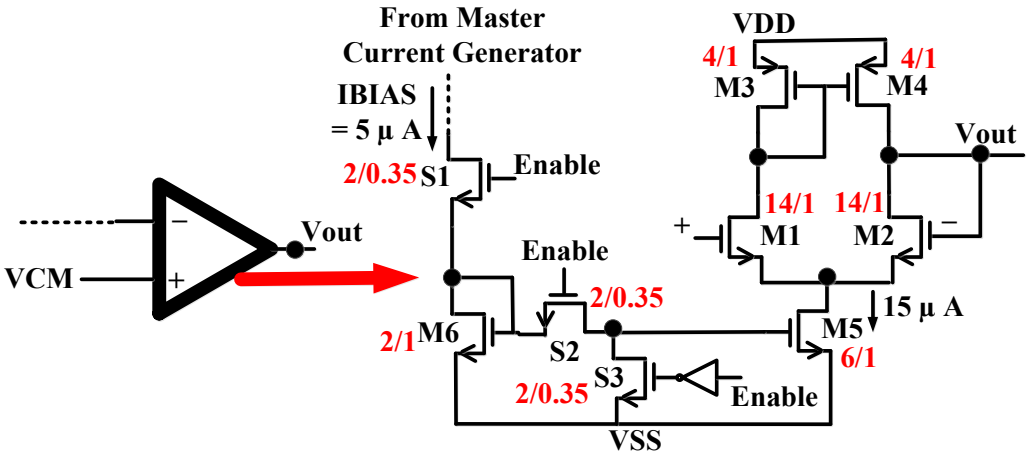


Figure 4. 19. Common mode voltage buffer with transistor dimensions as an OP-AMP of FIR filter.

Table 4. 6. Specifications and Results of designed V_{CM} Buffer to be used as OP-AMP of FIR filter

Sr. No.	Parameter	Value
1.	I_{REF} (µA)	15
2.	C_L(pF)	5.12 (C_{DAC})
3.	Loop Gain (dB)	47
4.	Total summarized noise (µV)	381(< ¼ LSB)
5.	Input-referred noise (mV)	0.8
6.	Bandwidth (MHz)	4
7.	Systematic Offset/Gain error (mV)	3.8 (~ ½ LSB)
8.	Settling Time (µs)	0.25
9.	PSRR	-48.32 dB/3.87 mV

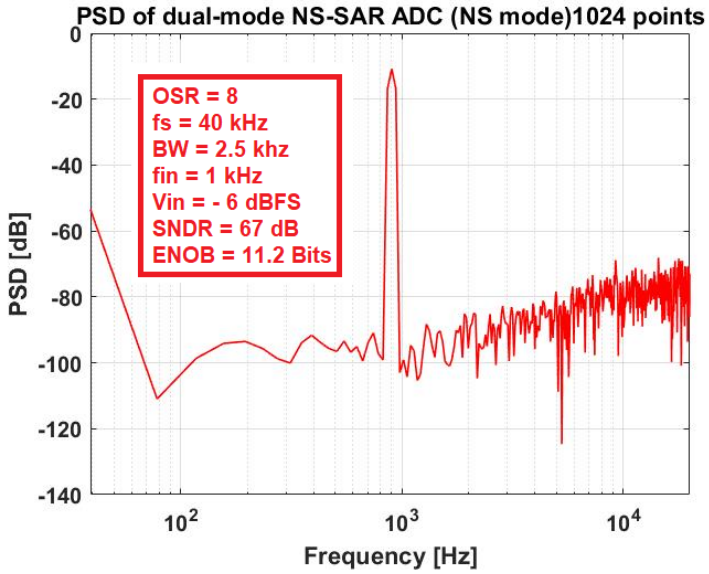


Figure 4. 20. ADC PSD plot with real OP-AMP (common mode buffer) of FIR filter.

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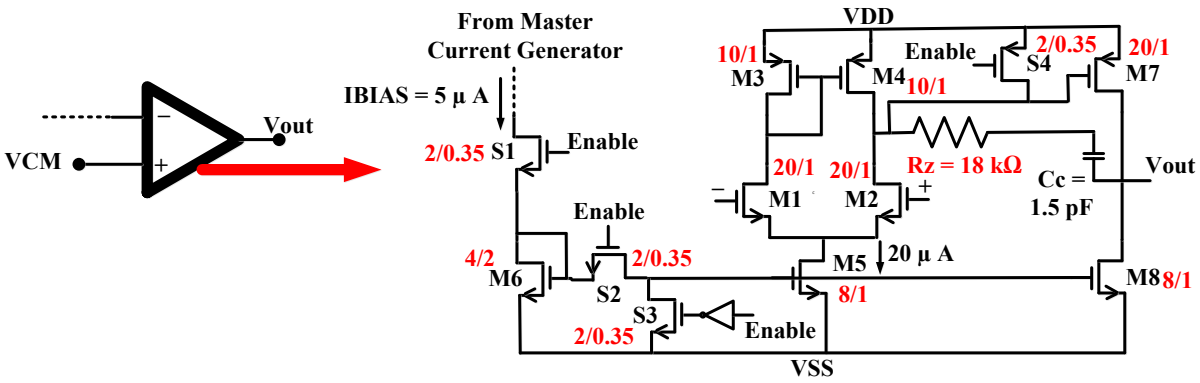


Figure 4. 21. Circuit Diagram of the final OP-AMP of FIR filter.

Table 4. 7. Specifications and Results of designed OP-AMP of FIR filter

Sr. No.	Parameter	Value
1.	I_{REF} (µA)	20 (first stage) + 20 (second stage) = 40 *Only for open loop OP-AMP of the buffer*
2.	C_L(pF)	5.12 (C_{DAC})
3.	Loop Gain (dB)	68.422
4.	Phase Margin	62°
5.	Total summarized noise (mV)	1.063 (< ¼ LSB)
6.	GBW (MHz)	6.63
7.	Systematic Offset/Gain error (mV)	6.5 (< 1 LSB)
8.	Settling Time (µs)	0.5
9.	PSRR	-53.49 dB/2.15 mV @ 20 kHz
10.	Linearity*: Method1; Method 2	0.035 %; 15.13 bits and SNR = 92.8 dB @ 20 kHz

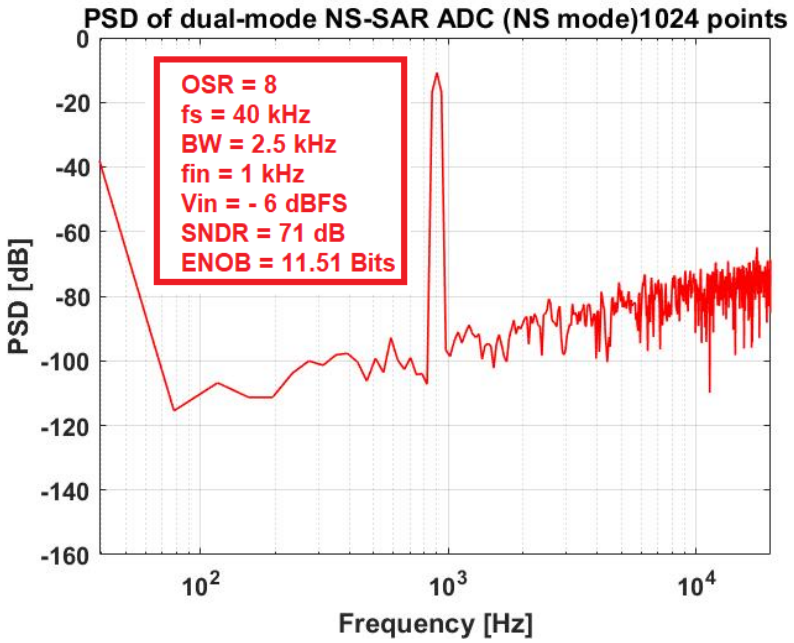


Figure 4. 22. ADC PSD plot with real OP-AMP of FIR filter. All other components are also real.

4.6.1.4. Introducing Autozeroing in FIR Filter to lower OP-AMP offset

A minor change in FIR filter circuit enables freely-available auto-zeroing without modifying its function, which helps offset voltage reduction of OP-AMP. Figure 4.23 shows the modified cirucit diagarm of FIR filter. During V_{res} sampling phase, offset voltage is also sampled at C_1, as shown in Figure 4.24. Offset voltage is substracted during V_{res} transfer phase, as shown in Figure 4.25. The freely-available autozeroing in FIR filter has the potential to reduce the offset voltage of OP-AMP, espcially in the fabrciated chip.

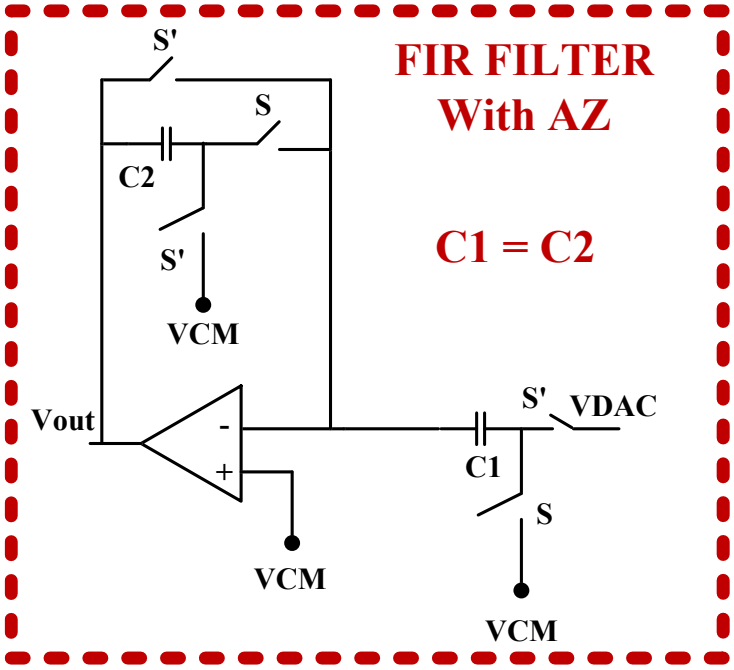


Figure 4. 23. FIR filter with autozeroing to reduce OP-AMP offset.

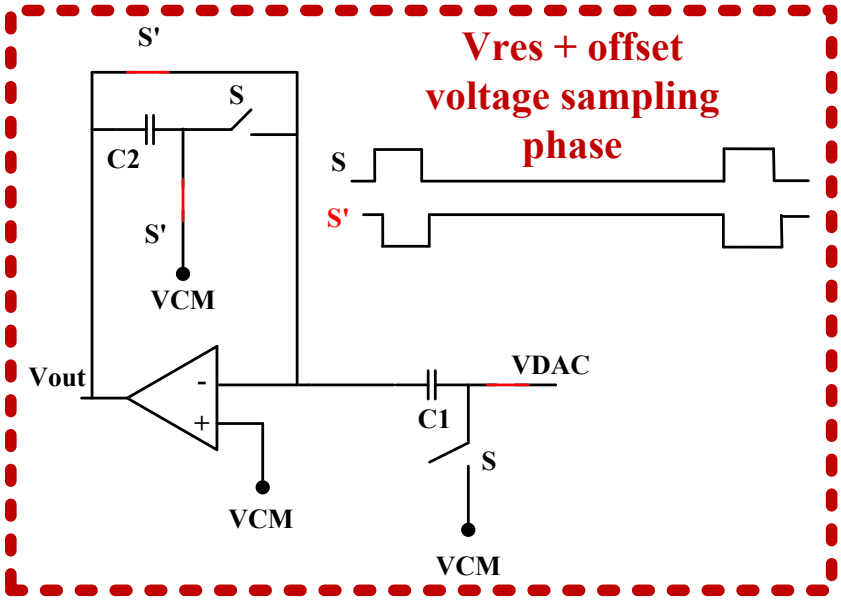


Figure 4. 24. Autozeroing in FIR filter: offset voltage sampling phase.

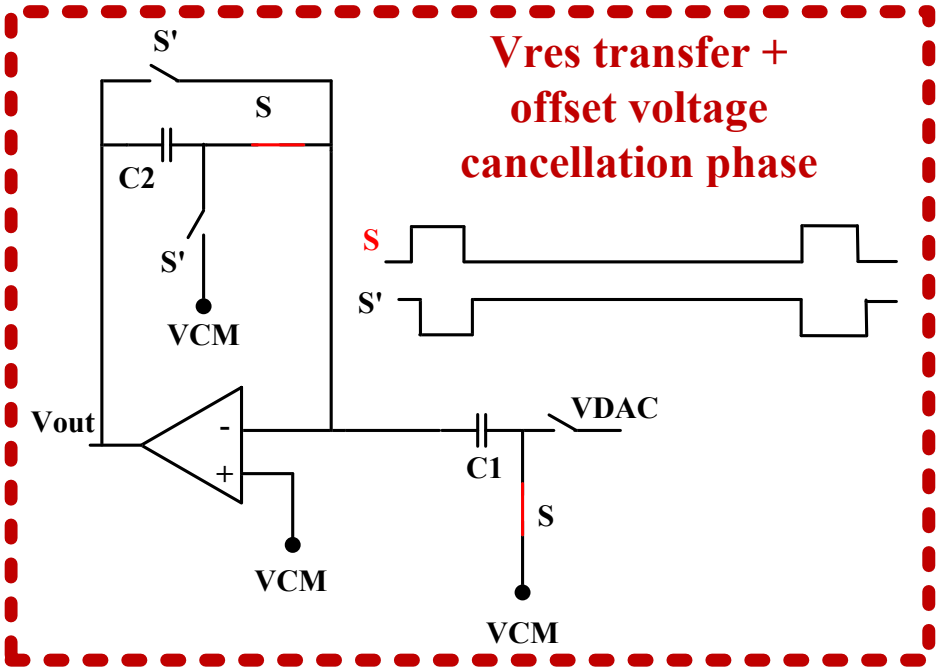


Figure 4. 25. Autozeroing in FIR filter: offset voltage cancellation phase.

4.6.1.5. Layout of FIR Filter

Figure 4.26 depicts the layout of FIR filter. Special attention has been paid to the placement and routing of two capacitors to avoid any performance degradation because of layout parasitics. In addition, 5 switches have been placed in close proximity to each other to ensure same offset because of these. Stacked layout approach has been adopted for the OP-AMP of FIR filter with dummy devices. The input node of FIR filter, which is connected with the CDAC node, has been properly shielded to avoid any coupling and crosstalk effect.

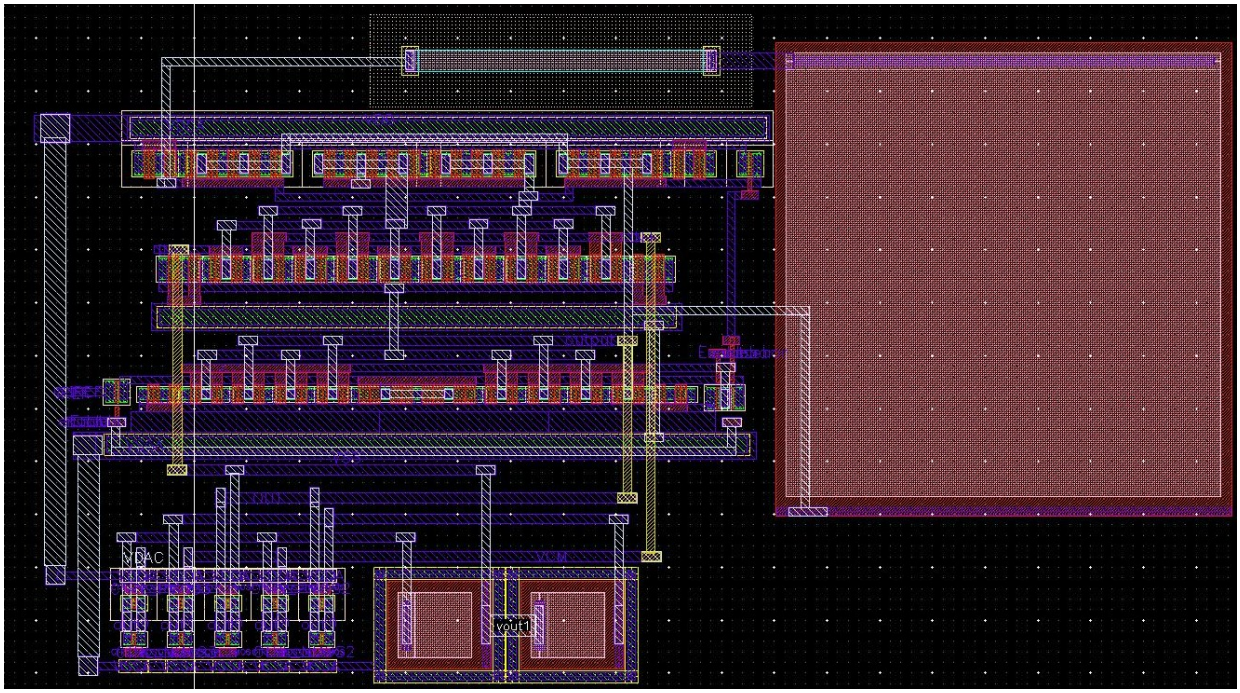


Figure 4. 26. Layout photo of FIR filter.

4.7. Achieving Incremental Mode Operation to Enable Dual-mode NS-SAR Operation

As described earlier, incremental mode operation is highly beneficial for multi-channel and multi-sensor systems to get memoryless operation from the ADC. For the 1st-order NS-SAR, 1st-order incremental functionality is needed. To introduce a 1st-order incremental mode functionality into NS-SAR ADC, reset operation needs to be performed after a certain period, depending on the OSR value. Besides the reset operation, on-chip decimation is also needed. For the 1st-order incremental mode functionality, decimation is simply a sum-of-sum operation before the reset operation. Both of these functions have been achieved by the use of a digital logic and some auxiliary digital cells, as shown in Figure 4.27.

The reset and decimation functionalities have been achieved by digital logic, implemented in Verilog HDL and synthesized. Verilog code of digital logic is provided in Appendix 3. The inputs to this logic are following signals:

- EoC: This is EoC signal generated by the NS-SAR ADC when output data is ready to be acquired. This signal acts as one of the clocks for the synchronous digital logic to generate an end-of-conversion signal (EOC_INC) for incremental mode operation of the ADC.

- S: This is external clock signal which triggers the ADC conversion process and controls its sampling-rate. It also acts as a clock for the digital logic and helps perform reset as well as sum-of-sum functions.

- Mode<1:0>: These are two external control bits dedicated to selecting the mode of ADC as per the desired application. The ADC mode can be selected by controlling these external bits in the way listed in Table 4.8.

Table 4. 8. dual-mode NS-SAR ADC modes of operation and OSR values selection using external control bits

Mode<1:0> value (External control bits)	**ADC Operating Mode**	**OSR**
0	NS/Free running	8, 16, 32
1	Incremental	8
2	Incremental	16
3	Incremental	32

- B0-B7: This is the output data of the NS-SAR ADC. These are needed to perform sum-of-sum function for incremental mode operation.

- Reset_EXT: This is external reset signal for the digital logic. Digital logic is reset at the start by this signal to avoid any strange/unknown behavior/values from the logic.

The outputs to the digital logic are following signals:

- OUT<0:12>: This is output data of the dual-mode NS-SAR ADC. For NS mode, only 8 bits of data is available, while other bits are zero. For incremental mode, output data value depends on OSR value. For an OSR value of maximum 32, 13 bits output data is available after each conversion.

- EoC_INC: This is the output end-of-conversion signal for the incremental mode operation. At the rising edge of this signal, output data is ready to be acquired.

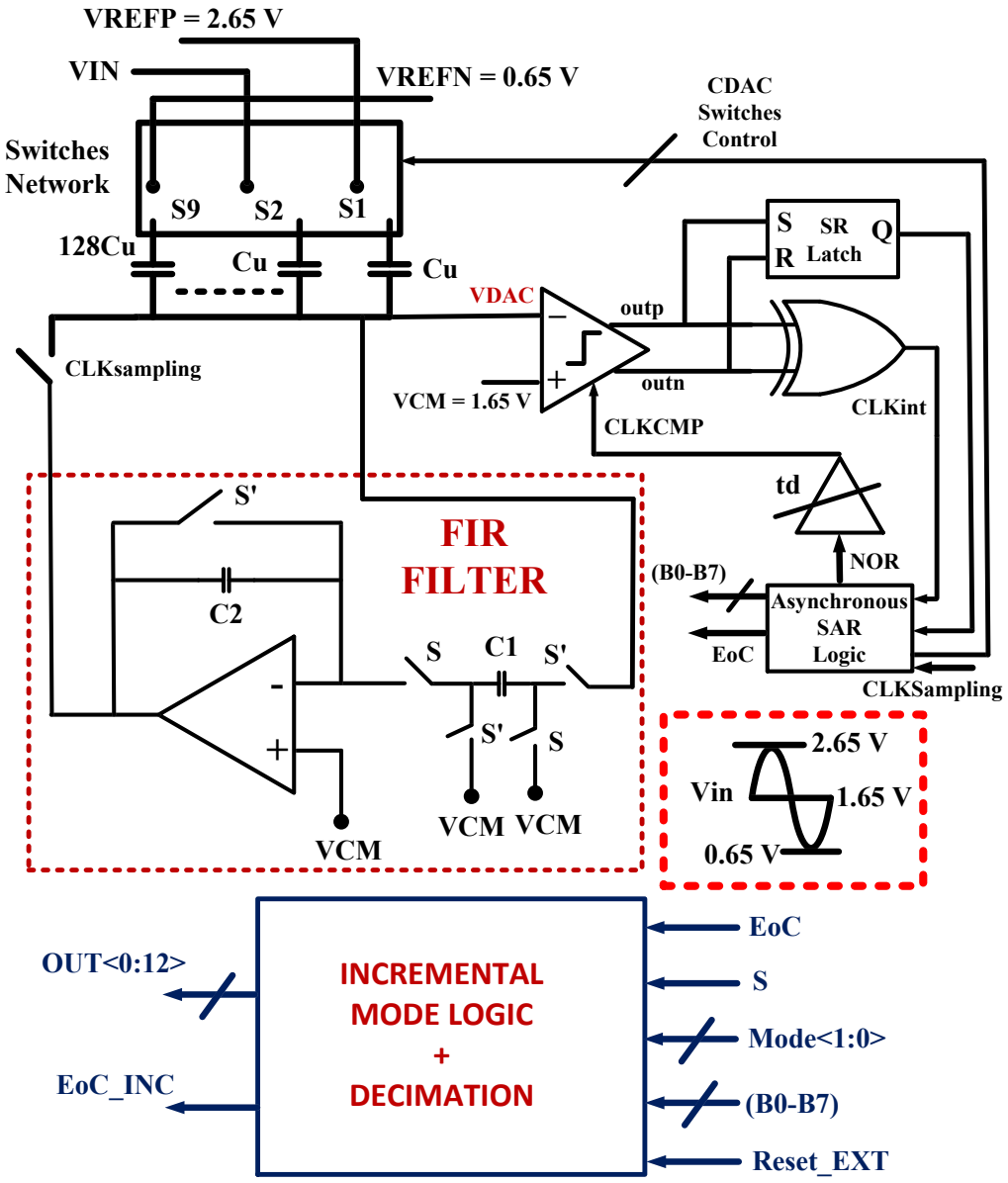


Figure 4. 27. Use of digital logic to introduce incremental mode operation in NS-SAR ADC, thus converting it into dual-mode ADC.

4.8. Schematic Level Simulation Results

After completing the schematic level design, performance of the ADC has been validated by extensive simulations. Figure 4.28 depicts the PSD plots of the ADC in NS/free running mode at an OSR value of 8, 16, and 32 at typical sampling-rate of 40 kHz. At an OSR of 8, the ADC secures an ENOB of 11.51 bits and a peak SNDR of 71 dB. Both of these values are comparable with the results achieved with Verilog-A based implementation. Thanks to the 1st-order NS, 3.5 bits increase in ENOB, and 23 dB rise in SNDR in 8-bit ASAR ADC have been achieved. The minor degradation in achieved ENOB and SNDR is attributed to circuit non-idealities, such as the $^{kT}/_{C}$ noise of FIR filter switches, and the thermal noise of FIR filter OP-AMP. Doubling the OSR value, about 1.5 bits rise in ENOB and 9 dB increase in SNDR can be observed, thus verifying the 1st-order NS operation. All the PSD plots show a correct 20 dB/dec slope because of the 1st-order NS functionality. SNDR vs. the input signal amplitude plot in NS/free running

mode is shown in Figure 4.29, which shows the ADC dynamic range of 73 dB. The dynamic range of 8-bit ASAR ADC has been enhanced by 25 dB because of the 1st-order NS functionality.

Performance of the ADC in incremental mode has also been verified by its PSD plots at supported OSR values for typical sampling-rate of 40 kHz, shown in Figure 4.30. The ADC gets an ENOB of 10.88 bits and peak SNDR of 67.2 dB at an OSR value of 8. About 3 bits enhancement in ENOB and 20 dB in SNDR can be observed in 8-bit ASAR ADC owing to the 1st-order incremental operation. About 1 dB rise in ENOB and 6 dB in SNDR have been secures for doubling the OSR value, which is consistent with the theoretical 1st-order incremental mode operation.

For the sake of simplicity, PSD plots of the dual-mode NS-SAR ADC in both the modes have been plotted for only typical sampling-rate of 40 kHz (5 kHz at an OSR of 8). Otherwise, the dual-mode NS-SAR ADC is sampling-rate reconfigurable (from typical 40 kHz to 167 kHz at OSR value of 8), as described earlier. At all these sampling-rates, the ADC performance remains the same with a proportionate power consumption and constant energy-efficiency. This will be verified by the measured PSD plots of the ADC at all its sampling-rates later in this chapter.

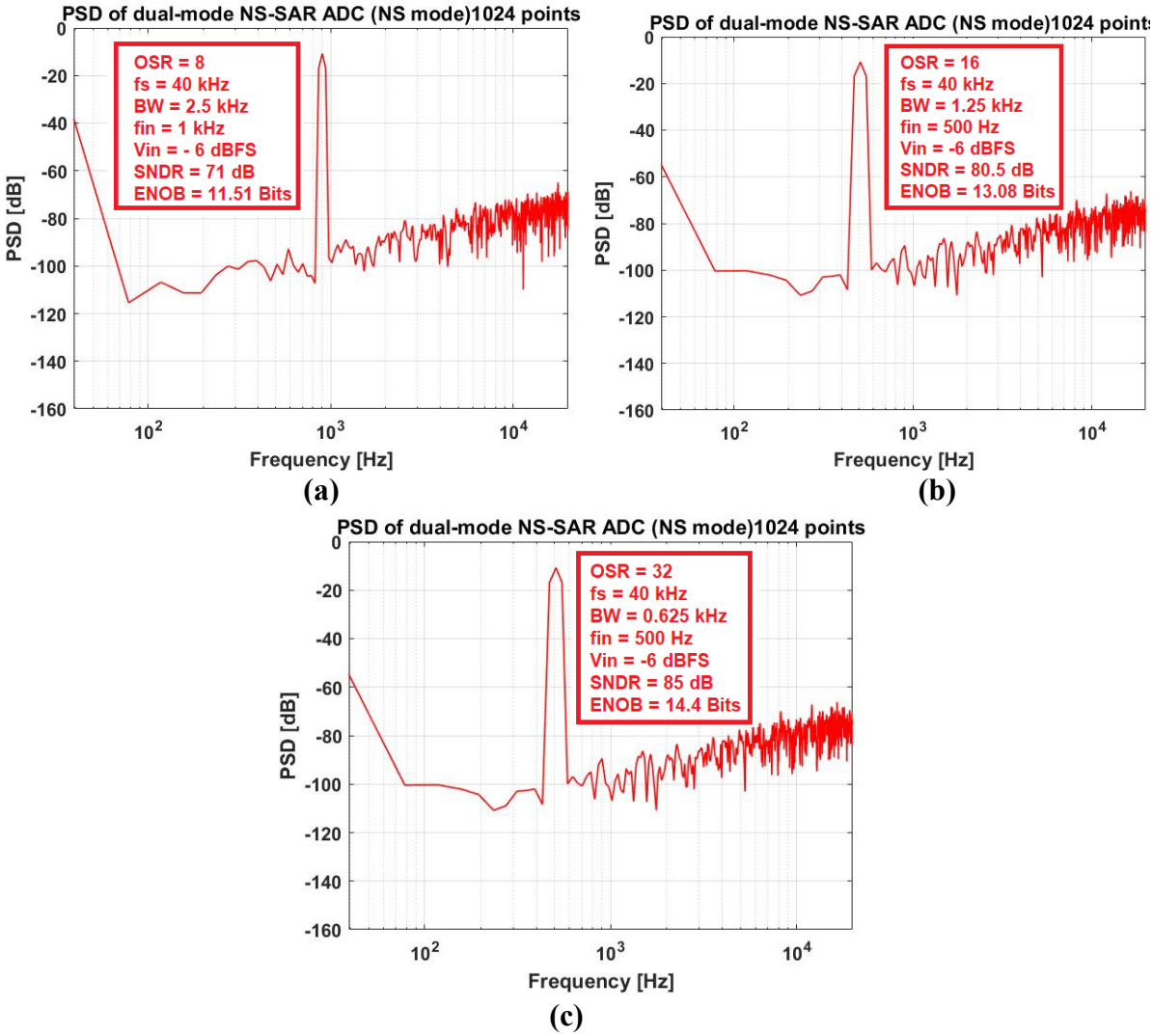


Figure 4. 28. Transient noise simulations-based PSD plot of schematic level dual mode NS-SAR ADC in NS/free running mode at (a) OSR =8, (b) OSR = 16, and (c) OSR = 32.

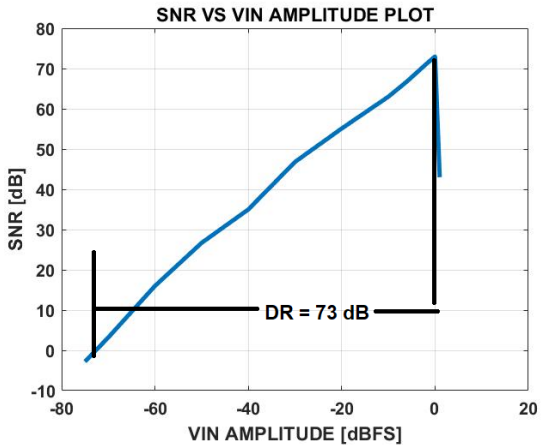


Figure 4. 29. Simulated SNDR vs. input signal amplitude plot of the dual-mode NS-SAR ADC in NS/free running mode, showing a dynamic range of 73 dB.

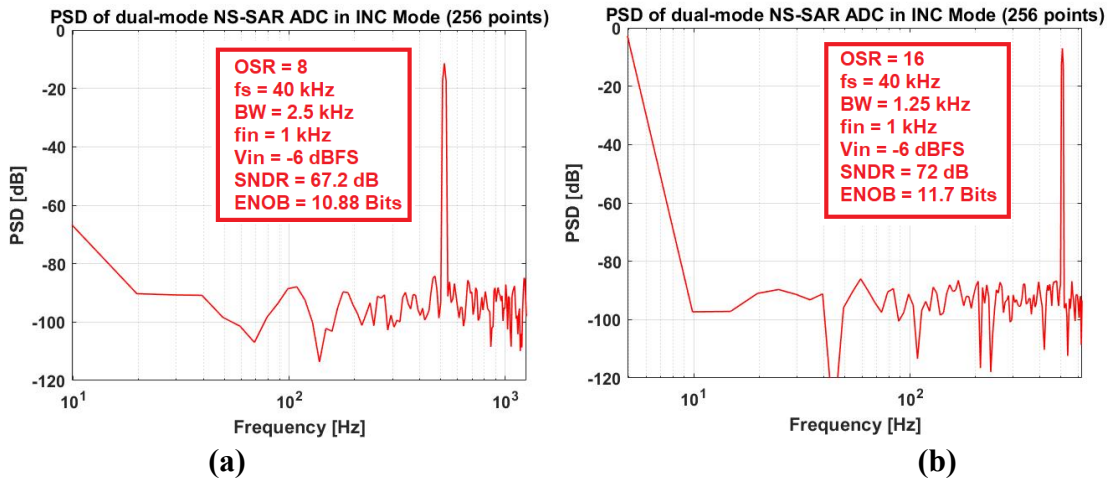


Figure 4. 30. Transient noise simulations-based PSD plot of schematic level dual mode NS-SAR ADC in incremental mode at (a) OSR =8, and (b) OSR = 16.

4.9. Post-layout Simulation Results

Figure 4.31 shows the top-level layout photo of the ADC, designed in a 0.35 µm CMOS process. The chip consists of two different versions/cores of the dual-mode NS-SAR ADC. The first core 'CORE_V1' is the version of the ADC with all its sections working at supply voltage of 3.3 V. 'CORE_V2' is the second version of the ADC whose delay-cell and digital section are operating at a supply voltage of 1.2 V with the help of the level-shifters, while analog section is operating at 3.3 V. Version 1 occupies a chip-area of 845 µm×1120 µm, while version 2 occupies an area of 875 µm×1190 µm. Figure 4.32 shows the bonding diagram of the ADC chip with JLCC84 package. Placement and routing of different cells have been done in such a way to avoid coupling and cross talk issues. An adequate separation has been maintained between the analog and digital sections. Significant care has been taken for routing of the critical nodes/signals, such as high switching internal clock signals.

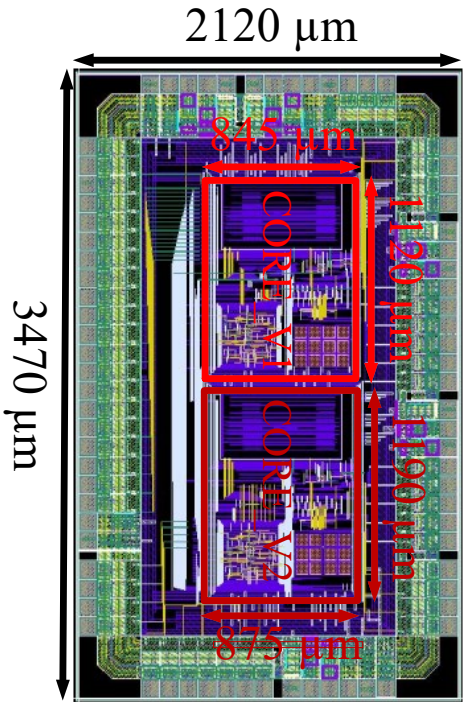


Figure 4. 31. Layout photo of the top-level of the designed ADC chip.

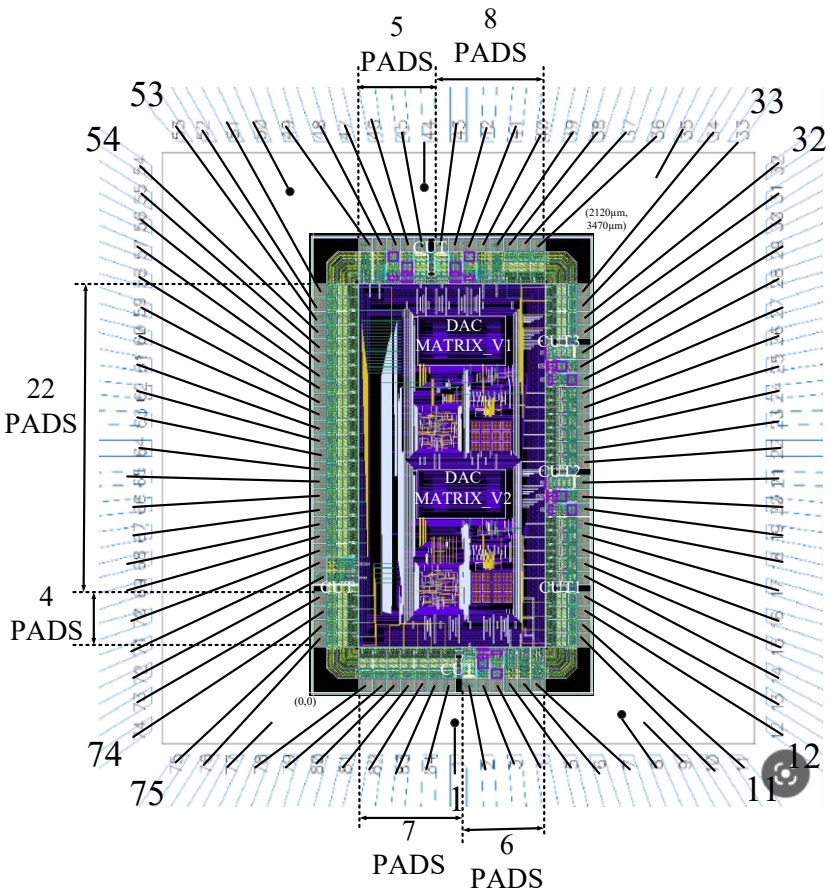


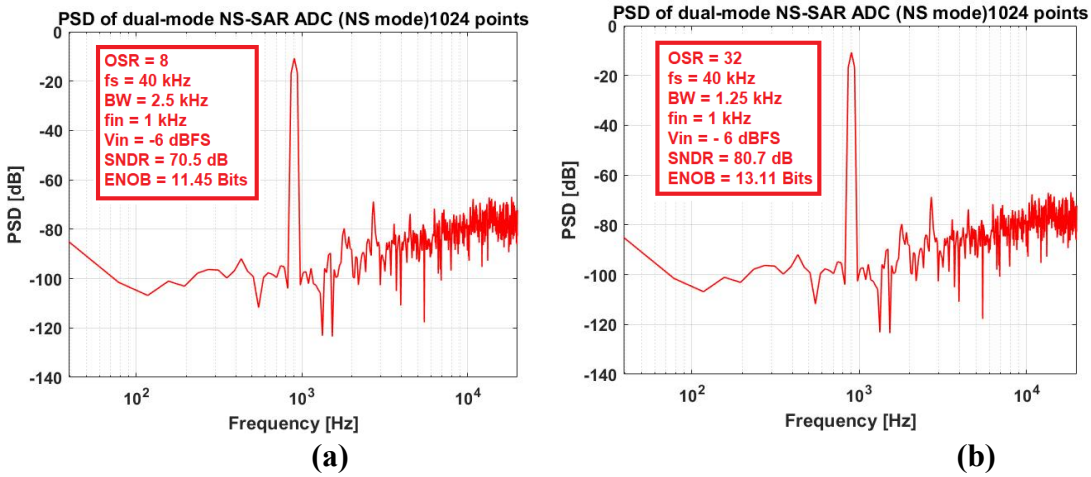
Figure 4. 32. ADC chip bonding diagram with JLCC84 package.

Extensive post-layout simulations have been performed to verify ADC performance in both modes. Figure 4.33 depicts ADC PSD plots in NS/free running mode at OSR value of 8 and 16 at a typical sampling-rate (40 kHz) for version 1 of the ADC. The ADC secures an ENOB of 11.45 bits and a peak SNDR of 70.5 dB at an OSR value of 8. Performance of the ADC is comparable with schematic level simulations. Because of the thermal noise and offset effect, the PSD plot is uniform before the input signal peak.

Incremental mode performance of the ADC is shown by PSD plots in Figure 4.34 at OSR values of 8 and 16 at the typical sampling-rate (40 kHz) for version 1 of the ADC. The ADC performance, in this mode too, is same as in schematic level simulations. The achieved ENOB and SNDR in incremental mode are slightly deteriorated in comparison with NS/free running mode. This is the cost paid because of the reset operation in incremental mode.

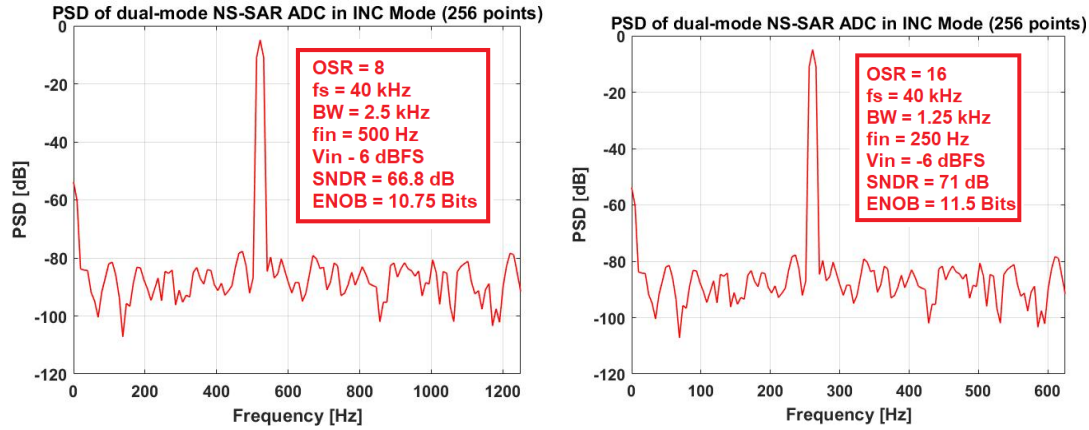
PSD plot of version 2 of the ADC in NS/free running mode is shown in Figure 4.35. As the core of this version is ASAR ADC whose delay cell is of fixed value, it operates at one sampling-rate of 160 kHz. Its performance (ENOB and SNDR) is the same as for version 1 of the ADC.

Figures 4.33-4.35 show ADC PSD plots at only typical sampling-rate (40 kHz) for the sake of simplicity and to save extensive simulations time. However, the performance of the ADC at all its 8 sampling-rates is the same as for typical sampling-rate. This will be further validated by the measured results.



(a) **(b)**

Figure 4. 33. PSD plot of post-layout level simulations of the dual mode NS-SAR ADC in NS/free running mode at (a) OSR =8, and (b) OSR = 16 for version 1 of the ADC.



(a) **(b)**

Figure 4. 34 . PSD plot of post-layout level simulations of the dual mode NS-SAR ADC in incremental mode at (a) OSR =8, and (b) OSR = 16 for version 1 of the ADC.

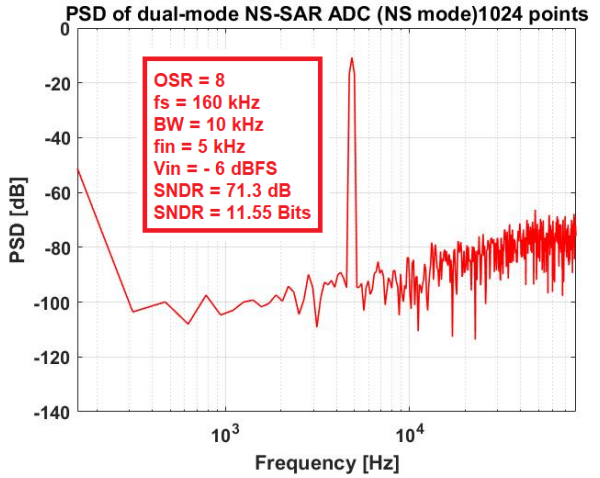


Figure 4. 35. PSD plot of post-layout level simulations of the dual mode NS-SAR ADC in NS/free running mode for version 2 of the ADC at OSR =8.

4.10. Measured Results

Figure 4.36 displays layout photo of the chip top level, chip microphotograph, custom PCB for ADC testing with ADC chip mounted, and measurement set up. The input signal was applied by the signal generator, while 'Sample' clock was provided by a clock generator. All reference and common mode voltages, biasing currents and input digital signals were gnerated on PCB. Measurement set-up consists of signal generator (APx524 audio analyzer; HEWLETT PACKARD 3245A universal source; Tektronix AFG3252 function generator) for input signal generation, power supply (Keysight E3641A triple output power supply), logic analyzer (Tektronix TLA5202B) to acquire output data, digital multimeter, Oscilloscope (LeCro 204Xi) and clock generator (Tektronix AFG3252 function generator) to provide the CLKSampling signal, besides the PCB.

Measurement of both the versions (version 1 with supply voltage of 3.3 V, and version 2 whose delay cell and digital section working at 1.2 V) of the ADC chip has been performed individually. In addition, both the modes (NS and incremental) of each version of the ADC have been tested separatly.

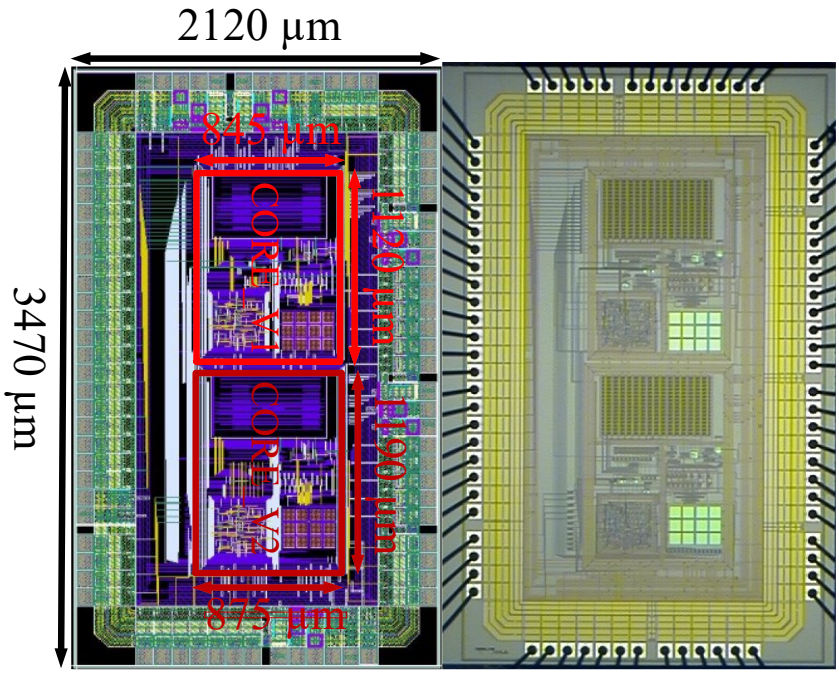
Initially, characterization of version 1 (with all components at 3.3 V) of the ADC was performed in both modes. Figure 4.37-4.39 show the PSD plots of version 1 of the ADC in NS/free running mode at all its supported sampling-rates at OSR value of 8, 16, and 32. As visible from the PSD plots, the ADC exhibits correct 1st-order NS functionality with 20 dB/dec slope. In addition, the ADC exhibits same perofrmance at all 8 sampling-rates, thus corroborating its sampling-rate reconfigurability functinality. Slight deagardtion in measured performance (about 5-6 dB in SNDR) can be seen from PSD plots in comparison with post layout simulation results. It is because of the preence of few in-band harmonics in PSD plots. These are ascribed to the distortion and nosie of the input signal source, reference voltage generation, and other non-idealities of the meausrement set up. SNDR vs input signal amplitude plot in NS/free running mode is shown in Figure 4.40. The measured dynamic range of the ADC is 66 dB at OSR of 8, which is 5-6 dB lower than the simulation based results because of the noise, distortion, and non-idealities of the mesuremet set up. It is also obvious from the PSD plots that ENOB and SNDR rise by about 1.4 bits and 0.8 dB per doubling the OSR value. This agin validates the correct 1st-order NS functinality from the proposed ADC in NS mode.

PSD plots of version 1 of the ADC in incremental mode at all covered sampling-rates at the OSR value of 8 are shown in Figure 4.41. The ADC performance (ENOB and SNDR) is slighlty degaraded in measurement in comparison with the post layout simulation results. The reasons behind this degaradtion is

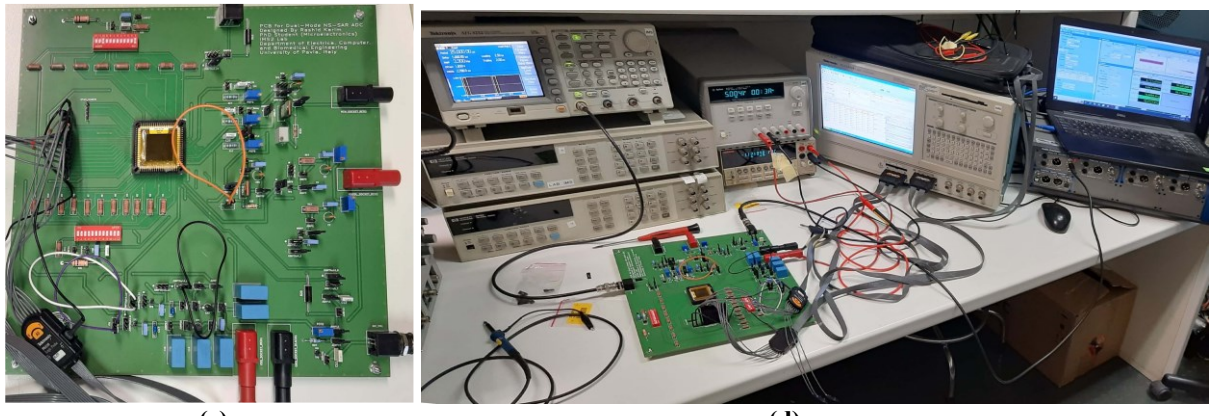
the in-band harmonics in PSD plots due to non-idealities, noise, and distortion of measurement setup and signal source. Like NS mode, the ADC exhibits same perofrmane at all 8 sampling-rates in incremental mode too, validating its sampling-rate reconfigurability function. Due to the reset operation, ADC performance (ENOB and SNDR) is slightly lower than NS mode.

Figure 4.42 shows the PSD plots of version 2 of the ADC in NS/free running mode at OSR of 8, 16, and 32. Its perofrmance (ENOB and SNDR) is same as for version 1 in NS/free running mode. This shows the potential and robustness of the ADC architecture at lower supply voltage. In addition, it corroborates the staemement that the proposed ADC architecture is a highly attractive choice for implementation in ultra scaled technology noces (< 65 nm).

Version 2 of the ADC PSD plots in incremental mode at OSR of 8, 16, and 32 are shown in Figure 4.43. The performance is same as for version 1. For doubling the OSR, there is an increase of about 1 bit in ENOB and 6 dB in SNDR can be noticed, which is well -aligned with the 1st-order incremental operation.

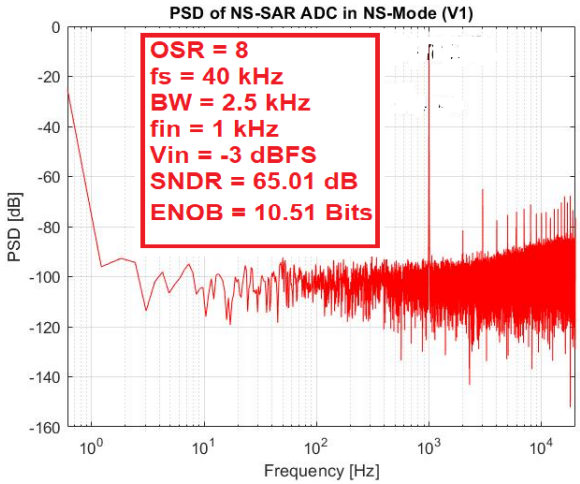


(a) **(b)**

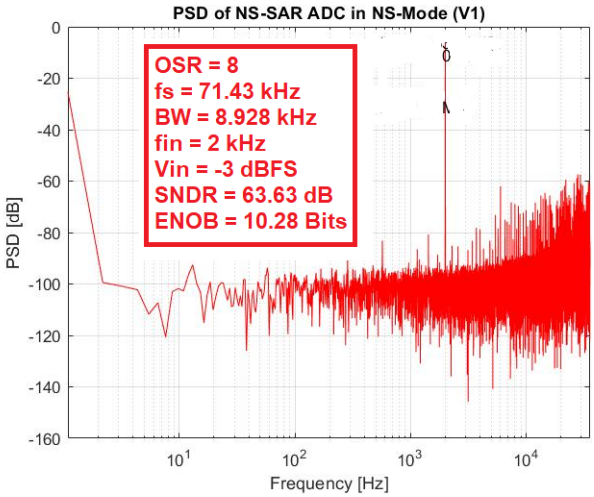


(c) **(d)**

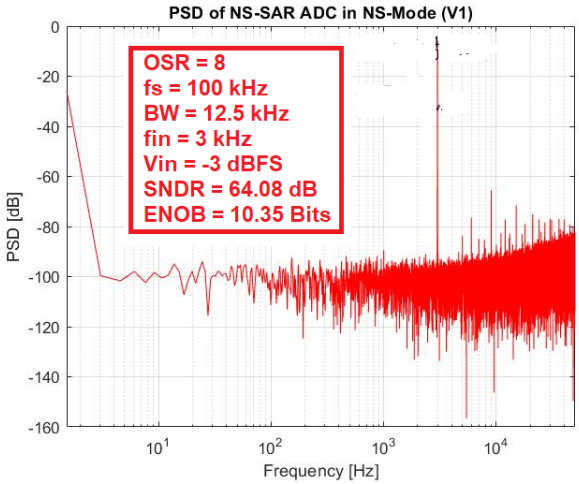
Figure 4. 36. Layout photo of the designed ADC chip: (a) top-level; (b) die microphotograph; (c) custom designed PCB test board, and (d) Measurement set up of the ADC using custom made PCB.


PSD of NS-SAR ADC in NS-Mode (V1)
OSR = 8
fs = 40 kHz
BW = 2.5 kHz
fin = 1 kHz
Vin = -3 dBFS
SNDR = 65.01 dB
ENOB = 10.51 Bits
PSD [dB]
Frequency [Hz]

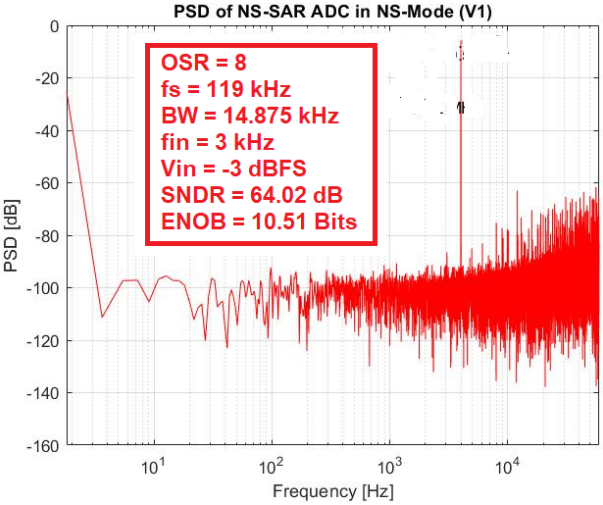
(a)


PSD of NS-SAR ADC in NS-Mode (V1)
OSR = 8
fs = 71.43 kHz
BW = 8.928 kHz
fin = 2 kHz
Vin = -3 dBFS
SNDR = 63.63 dB
ENOB = 10.28 Bits
PSD [dB]
Frequency [Hz]

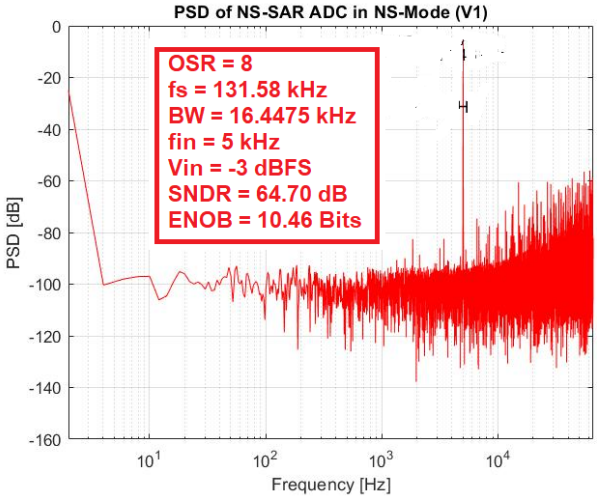
(b)


PSD of NS-SAR ADC in NS-Mode (V1)
OSR = 8
fs = 100 kHz
BW = 12.5 kHz
fin = 3 kHz
Vin = -3 dBFS
SNDR = 64.08 dB
ENOB = 10.35 Bits
PSD [dB]
Frequency [Hz]

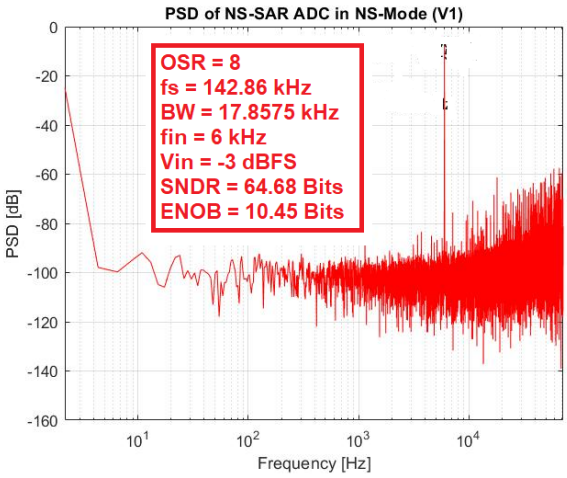
(c)


PSD of NS-SAR ADC in NS-Mode (V1)
OSR = 8
fs = 119 kHz
BW = 14.875 kHz
fin = 3 kHz
Vin = -3 dBFS
SNDR = 64.02 dB
ENOB = 10.51 Bits
PSD [dB]
Frequency [Hz]

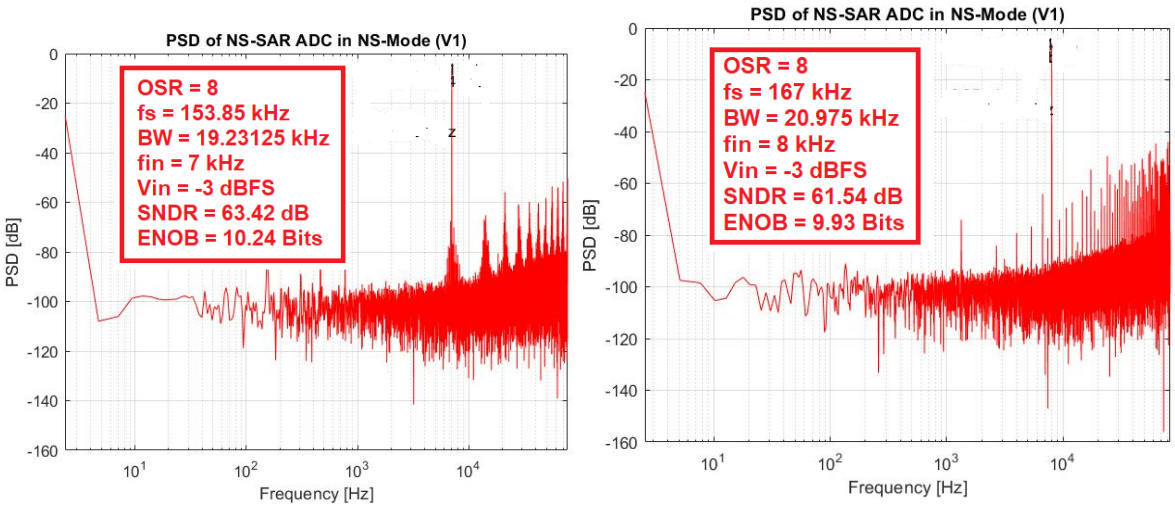
(d)


PSD of NS-SAR ADC in NS-Mode (V1)
OSR = 8
fs = 131.58 kHz
BW = 16.4475 kHz
fin = 5 kHz
Vin = -3 dBFS
SNDR = 64.70 dB
ENOB = 10.46 Bits
PSD [dB]
Frequency [Hz]

(e)

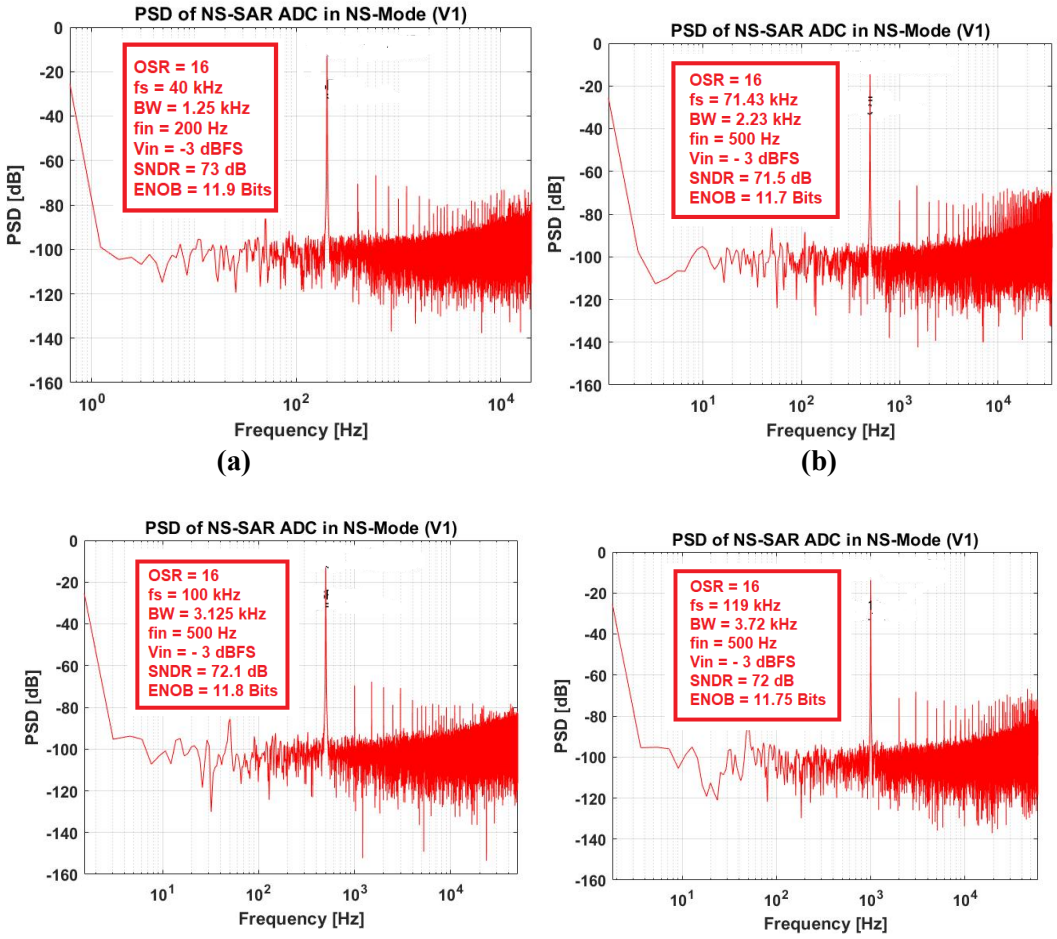

PSD of NS-SAR ADC in NS-Mode (V1)
OSR = 8
fs = 142.86 kHz
BW = 17.8575 kHz
fin = 6 kHz
Vin = -3 dBFS
SNDR = 64.68 Bits
ENOB = 10.45 Bits
PSD [dB]
Frequency [Hz]

(f)



(g) **(h)**

Figure 4. 37. Measured PSD of ADC in NS mode at all its supprted sampling-rates at an OSR = 8: (a) at $f_s = 40\ kHz$ with one unit voltage buffer of each type on; (b) at $f_s = 71.43\ kHz$ with two unit voltage buffers of each type on; (c) at $f_s = 100\ kHz$ with three unit voltage buffers of each type on; (d) at $f_s = 119\ kHz$ with four unit voltage buffers of each type on; (e) at $f_s = 131.58\ kHz$ with five unit voltage buffers of each type on; (f) at $f_s = 142.86\ kHz$ with six unit voltage buffers of each type on; (g) at $f_s = 153.85\ kHz$ with seven unit voltage buffers of each type on; (h) at $f_s = 167\ kHz$ with all eight unit voltage buffers of each type on.



(a) **(b)**

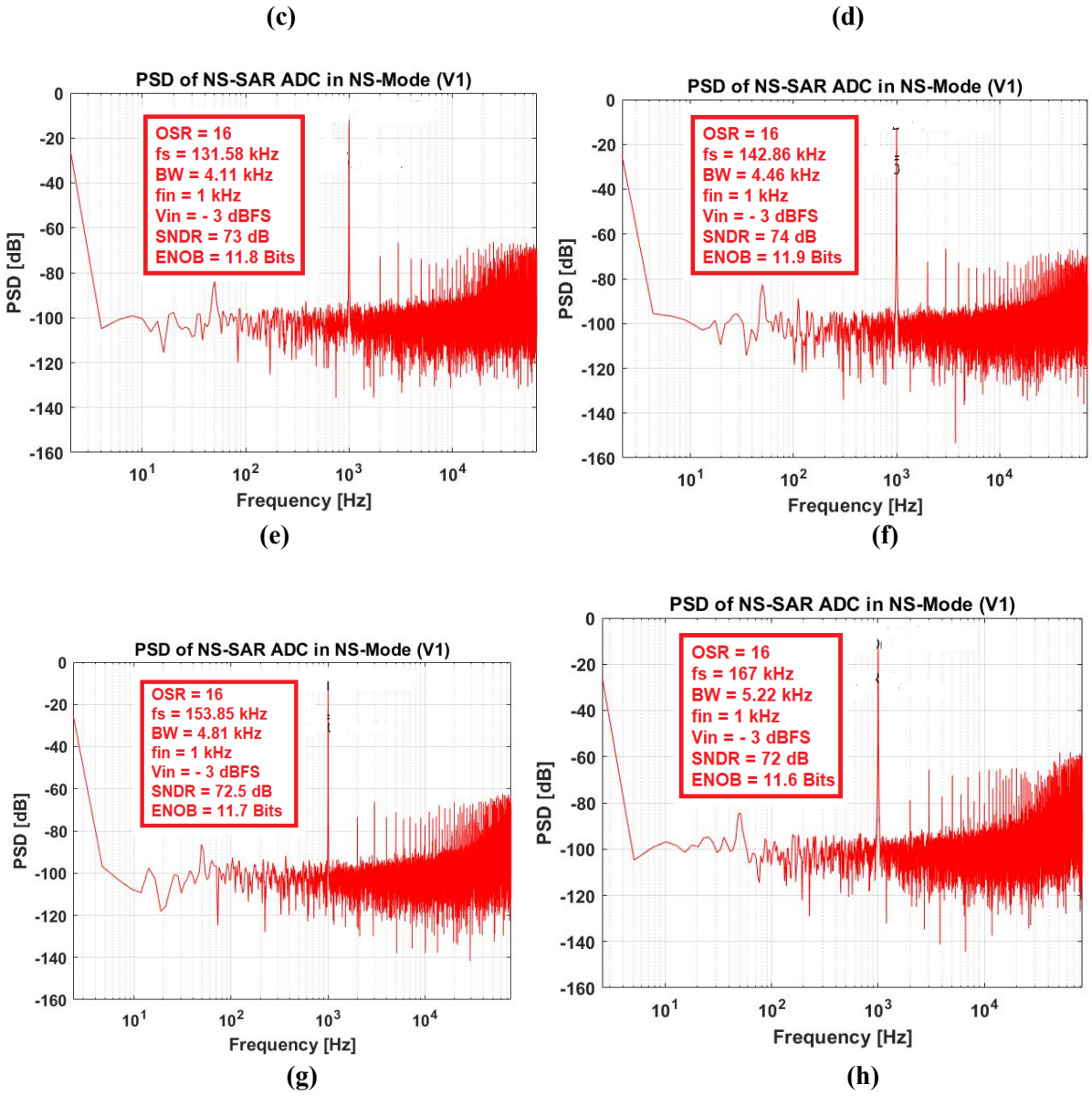
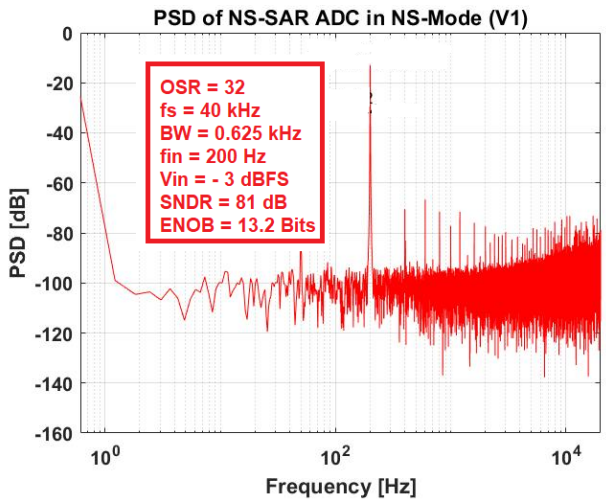
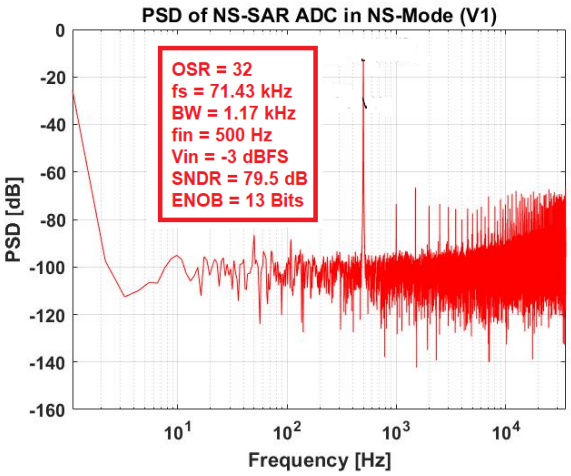


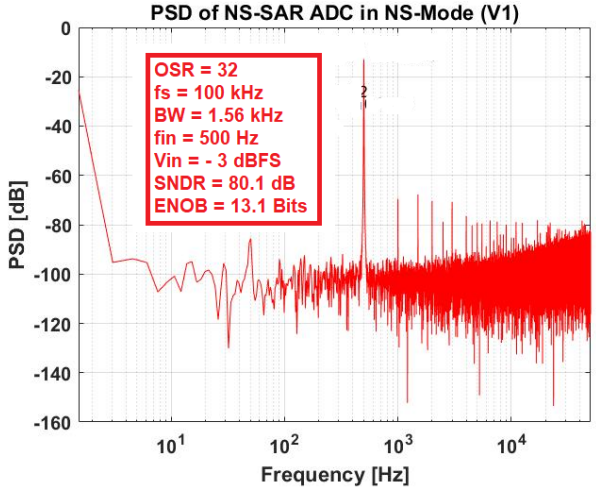
Figure 4. 38. Measured PSD of ADC in NS mode at all its supprted sampling-rates at an OSR = 16: (a) at $f_s = 40\ kHz$ with one unit voltage buffer of each type on; (b) at $f_s = 71.43\ kHz$ with two unit voltage buffers of each type on; (c) at $f_s = 100\ kHz$ with three unit voltage buffers of each type on; (d) at $f_s = 119\ kHz$ with four unit voltage buffers of each type on; (e) at $f_s = 131.58\ kHz$ with five unit voltage buffers of each type on; (f) at $f_s = 142.86\ kHz$ with six unit voltage buffers of each type on; (g) at $f_s = 153.85\ kHz$ with seven unit voltage buffers of each type on; (h) at $f_s = 167\ kHz$ with all eight unit voltage buffers of each type on.


PSD of NS-SAR ADC in NS-Mode (V1)
OSR = 32
fs = 40 kHz
BW = 0.625 kHz
fin = 200 Hz
Vin = - 3 dBFS
SNDR = 81 dB
ENOB = 13.2 Bits
PSD [dB]
Frequency [Hz]

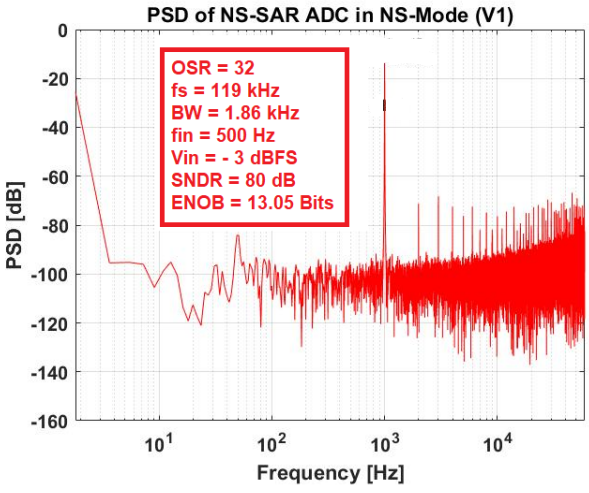
(a)


PSD of NS-SAR ADC in NS-Mode (V1)
OSR = 32
fs = 71.43 kHz
BW = 1.17 kHz
fin = 500 Hz
Vin = -3 dBFS
SNDR = 79.5 dB
ENOB = 13 Bits
PSD [dB]
Frequency [Hz]

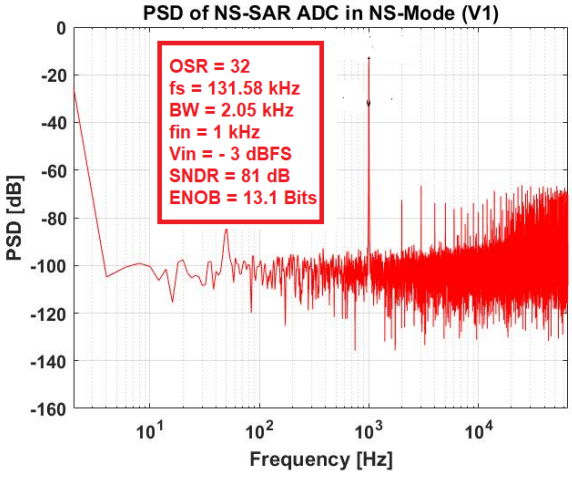
(b)


PSD of NS-SAR ADC in NS-Mode (V1)
OSR = 32
fs = 100 kHz
BW = 1.56 kHz
fin = 500 Hz
Vin = - 3 dBFS
SNDR = 80.1 dB
ENOB = 13.1 Bits
PSD [dB]
Frequency [Hz]

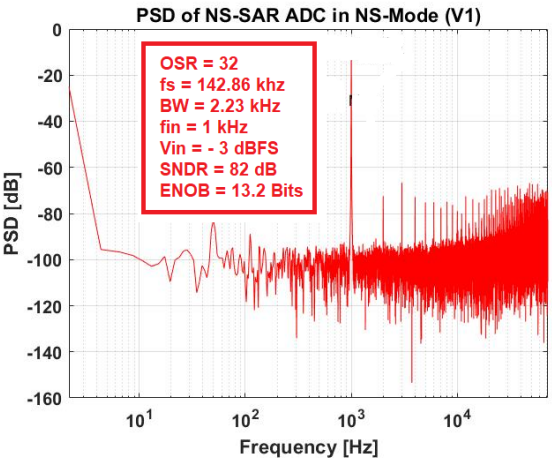
(c)


PSD of NS-SAR ADC in NS-Mode (V1)
OSR = 32
fs = 119 kHz
BW = 1.86 kHz
fin = 500 Hz
Vin = - 3 dBFS
SNDR = 80 dB
ENOB = 13.05 Bits
PSD [dB]
Frequency [Hz]

(d)


PSD of NS-SAR ADC in NS-Mode (V1)
OSR = 32
fs = 131.58 kHz
BW = 2.05 kHz
fin = 1 kHz
Vin = - 3 dBFS
SNDR = 81 dB
ENOB = 13.1 Bits
PSD [dB]
Frequency [Hz]

(e)


PSD of NS-SAR ADC in NS-Mode (V1)
OSR = 32
fs = 142.86 khz
BW = 2.23 kHz
fin = 1 kHz
Vin = - 3 dBFS
SNDR = 82 dB
ENOB = 13.2 Bits
PSD [dB]
Frequency [Hz]

(f)

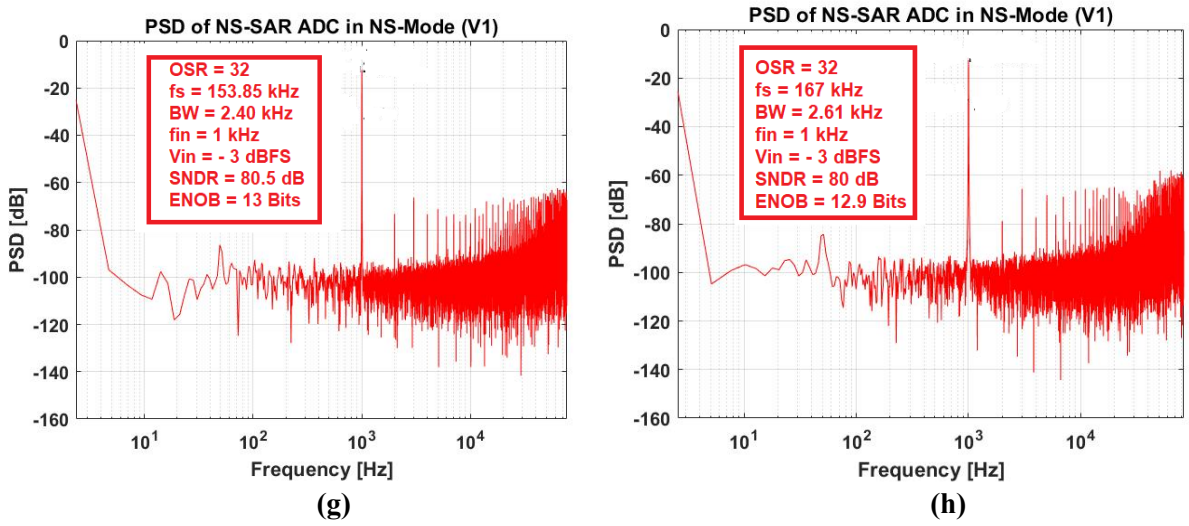


Figure 4. 39. Measured PSD of ADC in NS mode at all its supprted sampling-rates at an OSR = 32: (a) at $f_s = 40\ kHz$ with one unit voltage buffer of each type on; (b) at $f_s = 71.43\ kHz$ with two unit voltage buffers of each type on; (c) at $f_s = 100\ kHz$ with three unit voltage buffers of each type on; (d) at $f_s = 119\ kHz$ with four unit voltage buffers of each type on; (e) at $f_s = 131.58\ kHz$ with five unit voltage buffers of each type on; (f) at $f_s = 142.86\ kHz$ with six unit voltage buffers of each type on; (g) at $f_s = 153.85\ kHz$ with seven unit voltage buffers of each type on; (h) at $f_s = 167\ kHz$ with all eight unit voltage buffers of each type on.

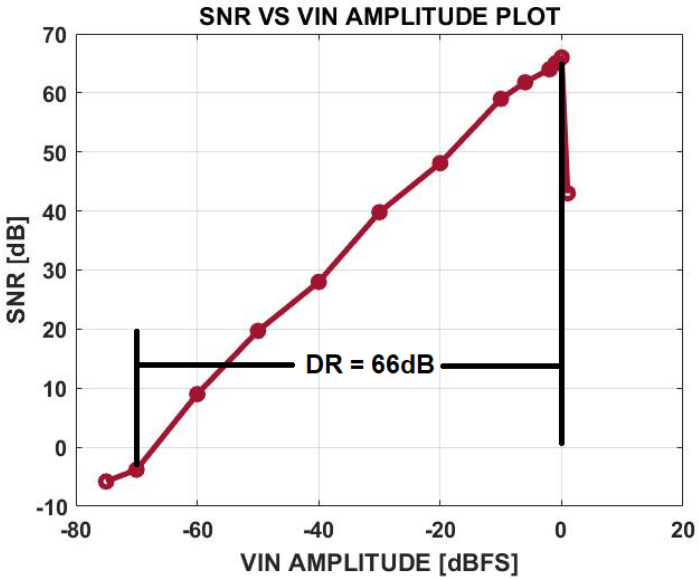
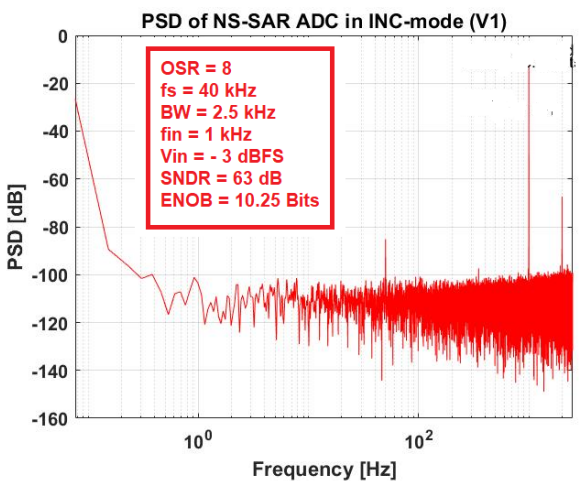
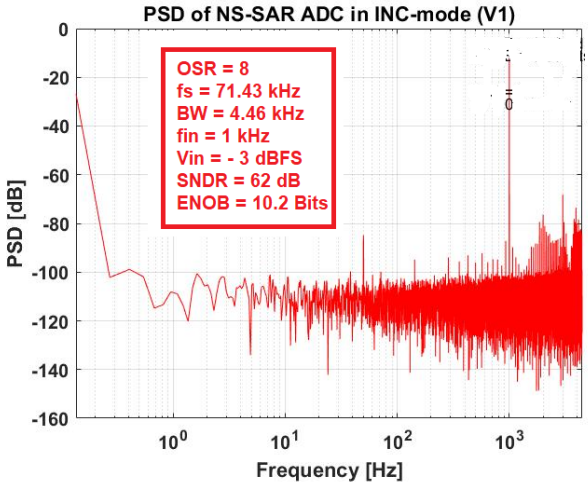


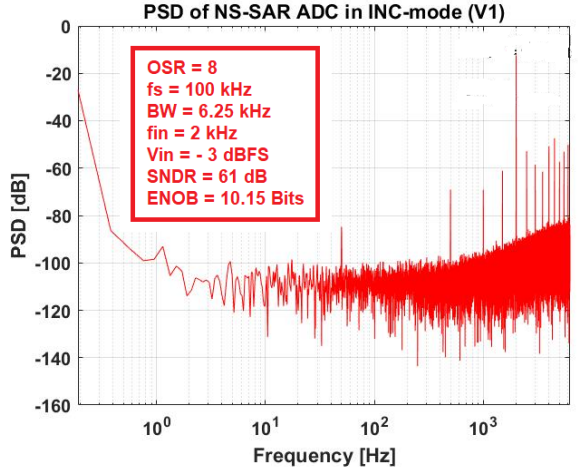
Figure 4. 40. Measured SNDR vs. input signal amplitude plot of the dual-mode NS-SAR ADC in NS/free running mode, showing a dynamic range of 66 dB.


PSD of NS-SAR ADC in INC-mode (V1)
OSR = 8
fs = 40 kHz
BW = 2.5 kHz
fin = 1 kHz
Vin = - 3 dBFS
SNDR = 63 dB
ENOB = 10.25 Bits
PSD [dB]
Frequency [Hz]

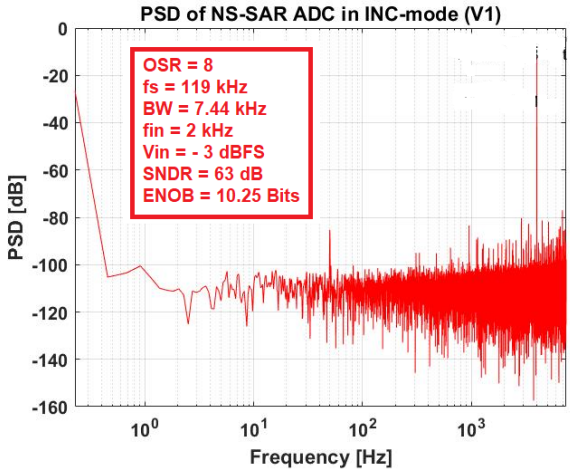
(a)


PSD of NS-SAR ADC in INC-mode (V1)
OSR = 8
fs = 71.43 kHz
BW = 4.46 kHz
fin = 1 kHz
Vin = - 3 dBFS
SNDR = 62 dB
ENOB = 10.2 Bits
PSD [dB]
Frequency [Hz]

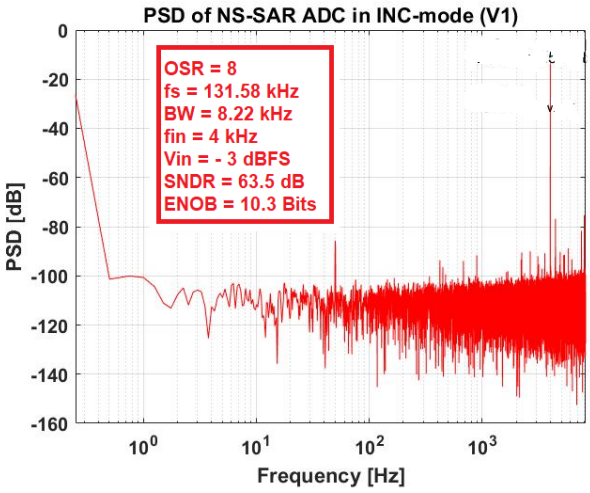
(b)


PSD of NS-SAR ADC in INC-mode (V1)
OSR = 8
fs = 100 kHz
BW = 6.25 kHz
fin = 2 kHz
Vin = - 3 dBFS
SNDR = 61 dB
ENOB = 10.15 Bits
PSD [dB]
Frequency [Hz]

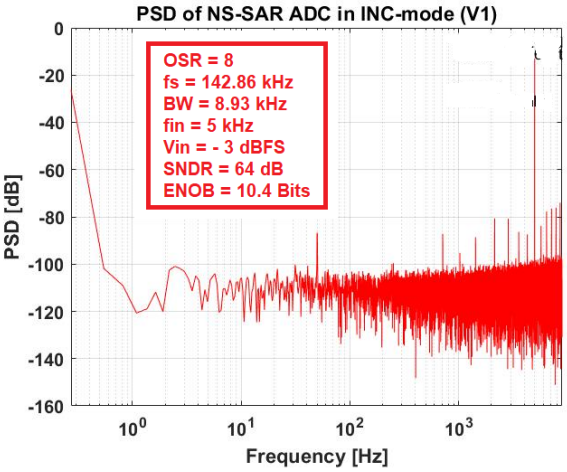
(c)


PSD of NS-SAR ADC in INC-mode (V1)
OSR = 8
fs = 119 kHz
BW = 7.44 kHz
fin = 2 kHz
Vin = - 3 dBFS
SNDR = 63 dB
ENOB = 10.25 Bits
PSD [dB]
Frequency [Hz]

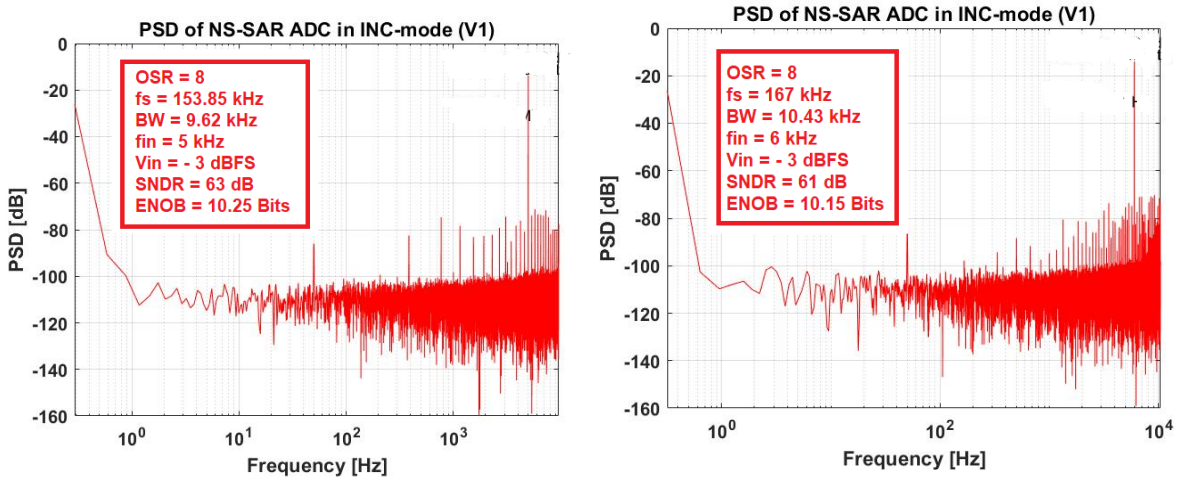
(d)


PSD of NS-SAR ADC in INC-mode (V1)
OSR = 8
fs = 131.58 kHz
BW = 8.22 kHz
fin = 4 kHz
Vin = - 3 dBFS
SNDR = 63.5 dB
ENOB = 10.3 Bits
PSD [dB]
Frequency [Hz]

(e)

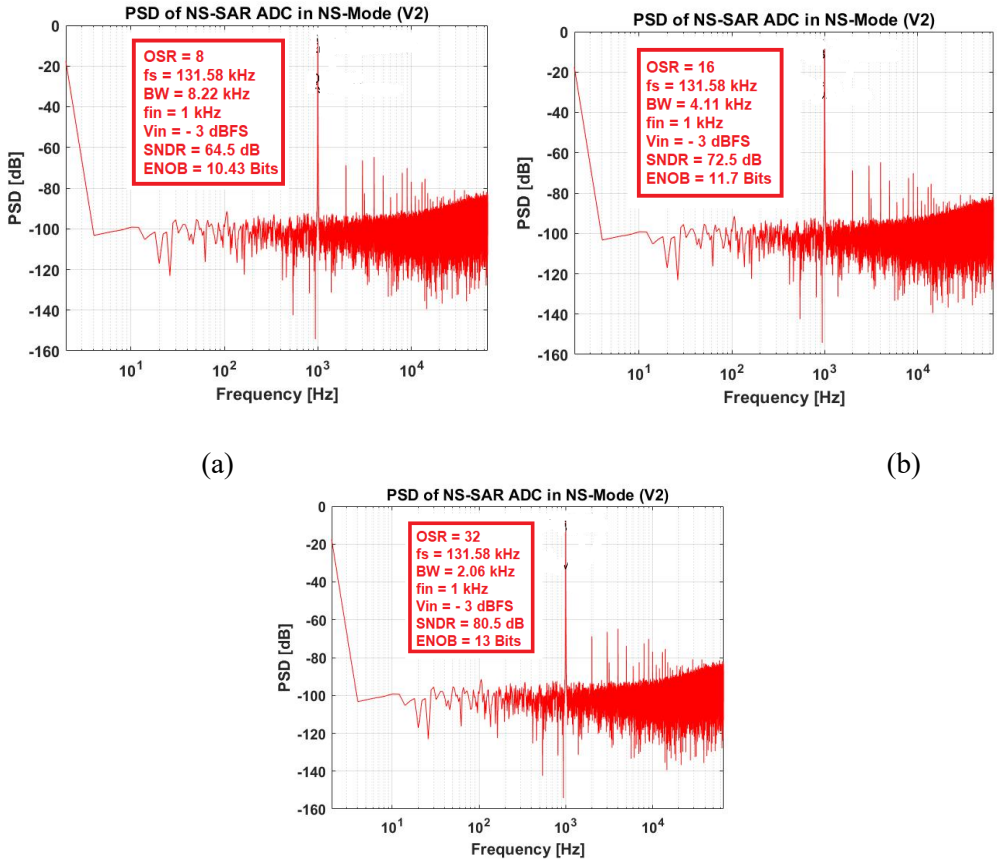

PSD of NS-SAR ADC in INC-mode (V1)
OSR = 8
fs = 142.86 kHz
BW = 8.93 kHz
fin = 5 kHz
Vin = - 3 dBFS
SNDR = 64 dB
ENOB = 10.4 Bits
PSD [dB]
Frequency [Hz]

(f)



(g) **(h)**

Figure 4. 41. Measured PSD plots of the dual-mode NS-SAR ADC in incremental mode at all its supprted sampling-rates at an OSR = 8: (a) at $f_s = 40\ kHz$ with one unit voltage buffer of each type on; (b) at $f_s = 71.43\ kHz$ with two unit voltage buffers of each type on; (c) at $f_s = 100\ kHz$ with three unit voltage buffers of each type on; (d) at $f_s = 119\ kHz$ with four unit voltage buffers of each type on; (e) at $f_s = 131.58\ kHz$ with five unit voltage buffers of each type on; (f) at $f_s = 142.86\ kHz$ with six unit voltage buffers of each type on; (g) at $f_s = 153.85\ kHz$ with seven unit voltage buffers of each type on; (h) at $f_s = 167\ kHz$ with all eight unit voltage buffers of each type on.



(a) (b)

(c)

Figure 4. 42. Measured SNDR of version 2 (delay cell and digital section operating at 1.2 V) of the dual-mode NS-SAR ADC in NS/free running mode at OSR (a) 8, (b) 16, and (c) 32.

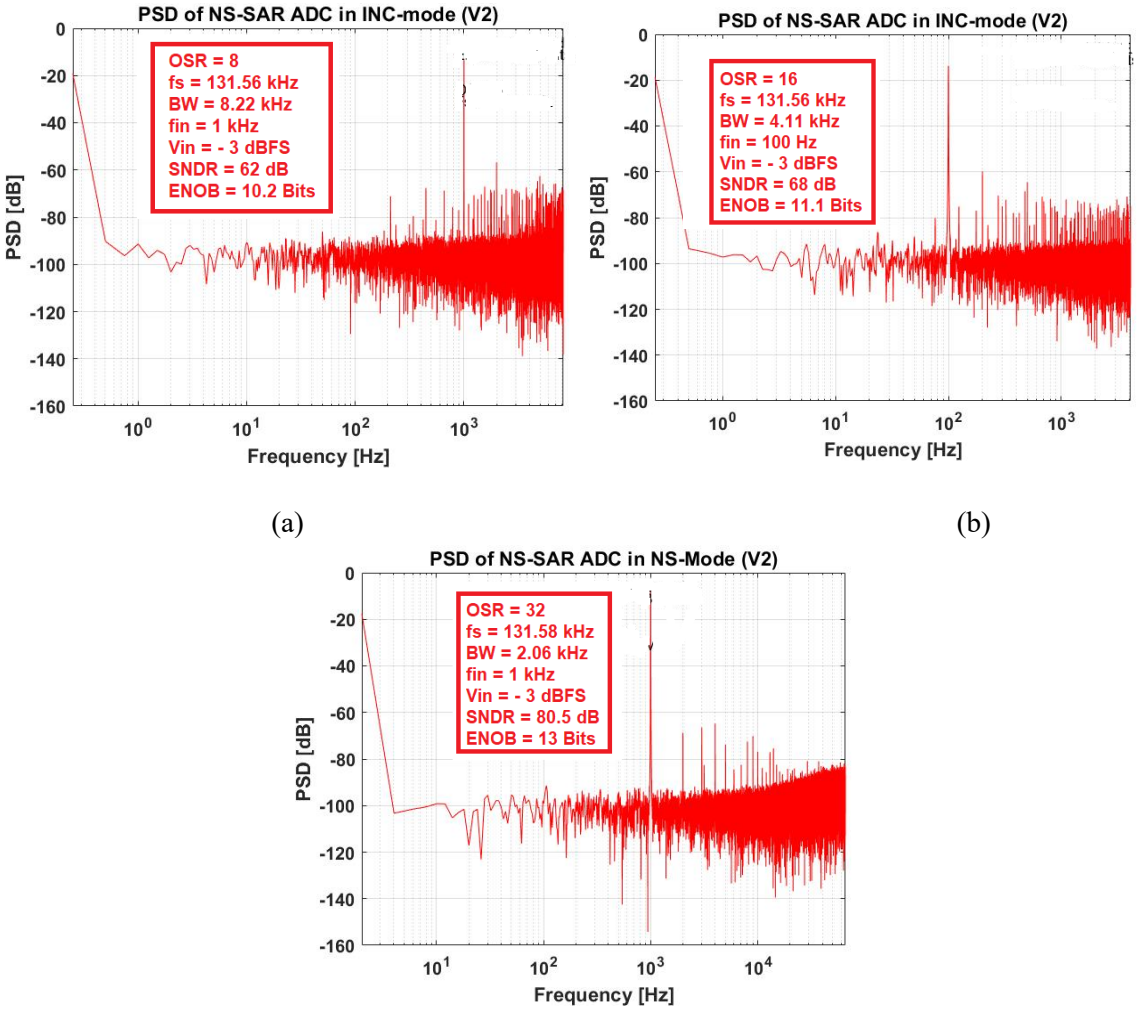


Figure 4. 43. Measured SNDR of version 2 (delay cell and digital section operating at 1.2 V) of the dual-mode NS-SAR ADC in Incremental mode at OSR (a) 8, (b) 16, and (c) 32.

4.11. Comparison With State-of-the-art

Table 4.9 compares performance of the designed NS-SAR ADC (in NS mode) with other slimier NS-SAR and SAR ADCs. Performance of NS-SAR ADC is better or at least comparable with other ADCs of Table 4.9. For example, the ENOB of the proposed ADC is better than all other fabricated ADCs of Table 4.9 working at 3.3 V. Also, it is sampling-rate reconfigurable unlike all other fixed sampling-rate ADCs. It is worth mentioning that this measured performance of the ADC has been achieved without the use of any complex and sophisticated design techniques, such as CDAC trimming, calibration and mismatch error shaping, comparator's offset cancellation, etc., unlike other ADCs in comparison. In comparison with the literature, this is one of those very few fabricated ADCs which have achieved such a high ENOB and SNDR using the 1st order NS without the use of any complex design technique. In addition, this is the first ever NS-SAR ADC which also operates in incremental mode, as per the author's best knowledge. These facts make this ADC further superior.

Table 4.10 provides a comparison of the dual-mode NS-SAR ADC (incremental mode) with the other incremental ΔΣ ADCs. This is the first ever incremental NS-SAR ADC, i.e., the way incremental

functionality has been achieved in the ADC. Therefore, its comparison with state-of-the-art becomes difficult because of the existence of no similar incremental mode NS-SAR ADC. Therefore, traditional incremental ΔΣ ADCs have been chosen for the comparison. As visible from Table 4.10, ADC performance in incremental mode is superior to other incremental ADC solutions, including the energy efficiency. Besides innovative way of achieving incremental mode operation, the ADC has two other unique features. First, it is asynchronous unlike all other traditional incremental ΔΣ ADCs. Second, it is f_s-reconfigurable in contrary to any other such solution. As SNDR and DR requirements of the proposed incremental NS-SAR ADC were dictated by the application, therefore they have been kept lower than traditional incremental ΔΣ ADCs. In addition, the proposed incremental NS-SAR ADC operates with the low OSR value unlike traditional incremental ΔΣ ADCs. The comparison of all the incremental ADCs in Table 4.10 has also been made with respect to conventional as well as normalized figure-of-merits for a fair comparison, as detailed below.

As already described for the ASAR ADC, the supply voltage of the fabricated dual-mode NS-SAR ADC is 3.3 V to accommodate high input signal swing (as high as 2 V). This is also highly beneficial from crosstalk and interference issues point of view. These benefits come at the cost of high-power consumption or low energy-efficiency. Consequently, the comparison of this high supply voltage-based ADC with recent low supply voltage-based ADCs is extremely difficult with respect to power consumption, energy-efficiency, and hence conventional figure-of-merit (FoM_W). It is because the power consumption is directly proportional to the square of the supply voltage. Besides several other ADCs such as proposed in [243] [244-246], a couple of high supply voltage-based ADCs listed in Table 4.9 and Table 4.10 corroborate this fact. This pushes the need for a new figure-of-merit for a fair comparison of these two types of ADCs. Therefore, we have proposed a novel figure-of-merit (FoM_{WN}), which is a normalized version of the traditional figure-of-merit (FoM_W). This FoM is listed in Table 4.9 and 4.10. In addition, we have also proposed normalized version (FoM_{SN}) of other conventional figure-of-merit (FoM_S), which is also listed in Table 4.9 and 4.10. Therefore, comparison of all the ADCs of Table 4.9 and Table 4.10 has been done not only with respect to traditional figure-of-merits (FoM_W and FoM_S), but also with respect to normalized figure-of-merits (FoM_{WN} and FoM_{SN}).

Considering the NS-SAR ADC performance keeping in view the FoM_{WN} and FoM_{SN}, the proposed dual-mode NS-SAR ADC becomes an excellent competitor for the state-of-the-art ADCs proposed in recent literature even with respect to the energy-efficiency. In addition, the other ADCs are void of the additional advantages and functions provided by the proposed ADC. These advantages include f_s-reconfigurablity with constant energy-efficiency at all covered sampling-rates, its scalability and flexibility, and dual-mode operation. The proposed ADC architecture is an auspicious candidate for implementation in ultra-scaled technology nodes (< 65 nm) with low supply voltage and input signal swing. Such implementation would also bring high speed advantage.

Although the power consumption of the standalone NS-SAR ADC seems high, it actually becomes negligible when calculated in multi-channel ASICs environment for space applications. Let us assume that there are 1024 channels of the ASIC and there is one NS-SAR ADC per channel. Also assume that the event-rate is 10^5 events/sec, which is a quite reasonable approximation since the events in space are sporadic. The typical conversion time for the NS-SAR ADC in NS mode is 25 µs with a power consumption of 105 µW at 3.3 V at an OSR value of 8. Based on these numbers, the average power consumption of one NS-SAR ADC comes out to be only 10.50 µW, calculated in 4.11:

$$\mathrm{P_{integratedwithASIC}} = 10^5 \times 105 \times 10^{-6} = 10.5\ \mu\mathrm{W} \tag{4.11}$$

Also, for ADC in incremental mode, this power comes out to be only 7.9 µW, as calculated in (4.12):

$$\mathrm{P_{integratedwithASIC}} = 10^5 \times 79 \times 10^{-6} = 7.9\ \mu\mathrm{W} \tag{4.12}$$

This power calculation considers that the ADC is operating continuously. This is actually not true since the ADC does not consume power, being idle, when there is no event. The probability that there is no event for space applications is significant. Considering this fact reduces ADC power dissipation significantly. The power consumption becomes even lower (about 6.59 µW based on the above assumptions) for the version 2 of the ADC (NS mode), i.e., whose delay-cell and digital section are operating at 1.2 V. Power consumption of version 2 of ADC in incremental mode cones out to be only 4.056 µW. The power consumption of the ADC becomes even insignificant while comparing it with the power consumption of the analog front-end section for multi-channel ASICs for space applications.

Table 4. 9. Dual-mode NS-SAR ADC (NS mode) comparison with state-of-the-art

Parameter/Ref.	**This Work (V1)**	**This Work (V2)**	[149]	[254]	[171]	[158]	[252]	[251]
Architecture	**Dual-mode NS-SAR**	**Dual-mode NS-SAR**	NS-SAR	NS-SAR	NS-SAR	NS-SAR	SAR	SAR
Asynchronous. (Y/N)?	**Y**	**Y**	N	N	N	Y	N	N
Process (nm)	**350**	**350**	180	130	28	40	350	130
Supply (V)	**3.3**	**3.3/1.2**	1.5	1.6	0.6	1.1	3.3	3.3
f_s (kHz)	**$40^{\&}/167^{\#}$**	**132**	128	128	320	12800	100	830
f_s-reconfig?	**Y**	**Y**	N	N	N	N	N	N
OSR	**8**	**8**	32	32	16	64	1	1
ENOB (Bits)	**10.6**	**10.5**	12.80	13.5	11.2	16	10.4	9.71
SNDR (dB)	**66**	**65.5**	78.8	82.6	69	98.3	64.3	60.218
P_{avg} (µW)	**$105^{\&}/231^{\#}$**	**65.9**	74.2	40.8	6.9	1998	247.5	3200
P^{*}_{avgN} (µW)	**$9.68^{\&}/22^{\#}$**	**10**	32.98	15.94	19.17	1651.24	22.73	293.85
FoM^{**}_{SN}; FoM_S (dB)	**$151^{\&}/157^{\#}$; $141^{\&}/157^{\#}$**	**157;157**	156.63; 153.1	163.58;160	156.17;160.61	176.12;175.3	157.72;147.35	151.72;141.35
FoM^{***}_{WN}; FoM_W (fJ/c-step)	**$945^{\&}/511^{\#}$; $10295^{\&}/5603^{\#}$**	**296;1950**	1156.13; 2601.12	343.97;880.43	407.43; 147	125.97;152.43	168.22;1830	422.7;4603.31

& at typical f_s; # at maximum f_s; $P_{avgN} = \frac{P_{avg}}{V_{DD}^2}$; $FoM_W = \frac{P_{avg}}{2^{ENOB}.{}^{f_s}/_{OSR}}$; $FoM_{WN} = \frac{P_{avgN}}{2^{ENOB}.{}^{f_s}/_{OSR}}$; $FoM_W = SNDR + 10\log\left(\frac{{}^{f_s}/_{OSR}}{P_{avg}}\right)$;

$FoM_{WN} = SNDR + 10\log\left(\frac{{}^{f_s}/_{OSR}}{P_{avgN}}\right)$

Table 4. 10. Dual-mode NS-SAR ADC (incremental mode) comparison with state-of-the-art

Parameter/Ref.	**This Work (V1)**	**This Work (V2)**	[255]	[256]	[257]	[258]	[259]	[260]
Architecture	**Incremental NS-SAR**	**Incremental NS-SAR**	Incremental ΔΣ	Incremental ΔΣ	Incremental ΔΣ	Incremental ΔΣ	Incremental ΔΣ	Incremental ΔΣ
Asynchronous. (Y/N)?	**Y**	**Y**	N	N	N	N	N	N
Process (nm)	**350**	**350**	180	180	150	160	180	180
Supply (V)	**3.3**	**3.3/1.2**	1.8	3	1.6	1	3.3	2
f_s (kHz)	**$40^{\&}/167^{\#}$**	**132**	1000	?	320		1520	115000
f_s-reconfig?	**Y**	**Y**	N	N	N	N	N	N
OSR	**8**	**8**	?	?	160	750	1026	5
ENOB (Bits)	**10.25**	**10.2**		19.64	10.3	80	13	11.5
SNDR (dB)	**63**	**62**	86.3	120	64	81.9	80	72
DR (dB)	**64**	**64**	90.1	?	68.2	81.9		73
P_{avg} (µW)	**$79^{\&}/221^{\#}$**	**40.56**	38100	300	96	20	56	48000
P^{*}_{avgN} (µW)	**$7.22^{\&}/20.26^{\#}$**	**8.25**	11760	100	37.5		5.14	
FoM^{**}_{SN}; FoM_S (dB)	**$155^{\&}/155^{\#}$; $155^{\&}/155^{\#}$**	**155;155**	147;161.3	161;161	154;137.18	1480;1480	154;154.7	161;156.8
FoM^{***}_{WN}; FoM_W (fJ/c-step)	**$966^{\&}/670^{\#}$; $10900^{\&}/7310^{\#}$**	**334;1670**	718;1460	128;24460	7437; 18500	;157.157.1	207;2050	180;1020

& at typical f_s; # at maximum f_s; $P_{avgN} = \frac{P_{avg}}{V_{DD}^2}$; $FoM_W = \frac{P_{avg}}{2^{ENOB}.{}^{f_s}/_{OSR}}$; $FoM_{WN} = \frac{P_{avgN}}{2^{ENOB}.{}^{f_s}/_{OSR}}$; $FoM_W = SNDR + 10\log\left(\frac{{}^{f_s}/_{OSR}}{P_{avg}}\right)$;

$$\mathrm{FoM_{WN}} = \mathrm{SNDR} + 10\log\left(\frac{f_s/_{OSR}}{P_{avgN}}\right)$$

4.12. Performance Summary of the dual-mode NS-SAR ADC

Finally, Table 4.11 and 4.13 provide performance summary of the proposed dual-mode NS-SAR ADC (Version1) at all its covered sampling-rates in NS mode and incremental mode, respectively. Performance summary in NS and incremental mode (Version 2) is provided in Table 4.12 and 4.14, respectively. It can be witnessed that the ADC exhibits the same performance (ENOB, and SNDR) at all covered sampling-rates. In addition, its power consumption is proportional to its sampling-rate, resulting in almost constant energy-efficiency. In other words, its energy-efficiency is independent of its sampling-rate. However, it is worth-noticing that ADC energy-efficiency improves with increase in its sampling-rate in both modes. This can be witnessed by observing FoM_S and FoM_{SN} at all sampling-rates. FoM_W and FoM_{WN} remain same at all sampling-rates.

Table 4. 11. ADC (Version 1) performance parameters in NS mode at all supporting sampling-rates at OSR = 8

Parameter/Sampling-rates	**f_{s1} (kHz)**	**f_{s2} (kHz)**	**f_{s3} (kHz)**	**f_{s4} (kHz)**	**f_{s5} (kHz)**	**f_{s6} (kHz)**	**f_{s7} (kHz)**	**f_{s8} (kHz)**
Topology	NS-SAR	NS-SAR	NS-SAR	NS-SAR	NS-SAR	NS-SAR	NS-SAR	NS-SAR
Process (nm)	350	350	350	350	350	350	350	350
V_{DD} (V)	3.3	3.3	3.3	3.3	3.3	3.3	3.3	3.3
f_s (kHz)	40	71.43	100	119	131.58	142.86	153.85	167
OSR	8	8	8	8	8	8	8	8
BW	2.5	4.46	6.25	7.44	8.22	8.92	9.62	10.43
ENOB (Bits)	10.51	10.28	10.35	10.51	10.46	10.45	10.24	9.93
SNDR (dB)	65.01	63.63	64.08	64.02	64.70	68.68	63.42	61.54
P_{avg} (µW)	105	138.5	167.7	192	206	215.82	219	231
P_{avgN} (µW)	9.68	12.7	15.4	17.63	19	19.8	20	22
FoM_W (fJ/c-step)	10295	7500	6549	6291	6096	5887	5770	5603
FoM_{WN} (fJ/c-step)	945	690	601	578	562	540	525	511
FoM_S (dB)	141	142	143	143	157	157	157	157
FoM_{SN} (dB)	151	153	157	157	157	157	157	157

Table 4. 12. ADC (Version 2) performance parameters in NS mode at all supporting sampling-rates at OSR = 8

Parameter/Sampling-rates	**f_s (kHz)**
Topology	NS-SAR
Process (nm)	350
V_{DD} (V)	3.3
f_s (kHz)	132
OSR	8
BW	8.25
ENOB (Bits)	10.5
SNDR (dB)	65.5
P_{avg} (µW)	65.9
P_{avgN} (µW)	10
FoM_W (fJ/c-step)	1950
FoM_{WN} (fJ/c-step)	296
FoM_S (dB)	157
FoM_{SN} (dB)	157

Table 4. 13. ADC (Version 1) performance parameters in incremental mode at all supporting sampling-rates at OSR = 8

Parameter/Sampling-rates	**f_{s1} (kHz)**	**f_{s2} (kHz)**	**f_{s3} (kHz)**	**f_{s4} (kHz)**	**f_{s5} (kHz)**	**f_{s6} (kHz)**	**f_{s7} (kHz)**	**f_{s8} (kHz)**
Topology	Incremental NS-SAR	Incremental NS-SAR	Incremental NS-SAR	Incremental NS-SAR	Incremental NS-SAR	Incremental NS-SAR	Incremental NS-SAR	Incremental NS-SAR
Process (nm)	350	350	350	350	350	350	350	350
V_{DD} (V)	3.3	3.3	3.3	3.3	3.3	3.3	3.3	3.3
f_s (kHz)	40	71.43	100	119	131.58	142.86	153.85	167
OSR	8	8	8	8	8	8	8	8
BW	2.5	4.46	6.25	7.44	8.22	8.92	9.62	10.43
ENOB (Bits)	10.25	10.2	10.15	10.25	10.3	10.4	10.25	10.15
SNDR (dB)	63	62	61	63	63.5	64	63	61
P_{avg} (µW)	79	115	144.87	168.3	184.8	194.7	207.9	221
P_{avgN} (µW)	7.22	10.5	13.3	15.42	16.93	17.84	19	20.26
FoM_W (fJ/c-step)	10900	8920	7950	7800	7734	7521	7458	7310
FoM_{WN} (fJ/c-step)	966	814.6	552.4	715.8	708.5	689	681	670
FoM_S (dB)	155	155	155	155	155	155	155	155
FoM_{SN} (dB)	155	155	155	155	155	155	155	155

Table 4. 14. ADC (Version 2) performance parameters in NS mode at all supporting sampling-rates at OSR = 8

Parameter/Sampling-rates	**f_s (kHz)**
Topology	NS-SAR
Process (nm)	350
V_{DD} (V)	3.3
f_s (kHz)	132
OSR	8
BW	8.25
ENOB (Bits)	10.2
SNDR (dB)	62
P_{avg} (µW)	40.56
P_{avgN} (µW)	8.25
FoM_W (fJ/c-step)	1670
FoM_{WN} (fJ/c-step)	334
FoM_S (dB)	155
FoM_{SN} (dB)	155

Chapter 5

CONCLUSIONS

Chapter Abstract

This chapter starts with the conclusions of thesis work in Section 5.1. Section 5.2 is devoted to the contributions of this thesis work and highlights novelty and distinctiveness of the proposed ADC architectures. The chapter ends with a brief description of some future directions and potential application scenarios for the proposed ADC architectures in Section 5.3.

5.1. Conclusions

This thesis has presented two novel single-channel ADC architectures for multi-channel CMOS ASICs for space applications. The thesis started with a description of background, introduction, significance, requirements, and challenges of multi-channel CMOS ASICs and ADCs for space applications, which are part of chapter 1. Chapter 1 also included a detail of initial target specifications of the ADCs to be proposed. Chapter 2 of the thesis provided a background study and comprehensive literature review of the ADCs. Based on an extensive literature review of the ADCs, suitable ADC architectures (ASAR and NS-SAR ADC) were chosen because of their well-alignment with the target application. A detailed review of the state-of-the-art of the selected ADC architectures was performed to investigate their pros. and cons. and identify research gaps. As per the literature review, no ASAR and NS-SAR ADC have been proposed for space application before this work.

Chapter 3 provided step-by-step design detail and measurement results of the first proposed ADC architecture, i.e., an 8-bit single-channel sampling-rate reconfigurable ASAR ADC, following a top-down methodology. The proposed ASAR ADC needs a single low duty-cycle and low-switching external trigger start-of-conversion 'CLKSampling' clock signal to start the A/D conversion process. The sampling-rate of the ADC is solely dictated by this well-controlled 'CLKSampling' signal. The 'CLKSampling' clock signal can either be provided externally if the ADC is being operated as a standalone device, or by the analog front-end section of the ASIC if the ADC is being operated in an integrated environment. All other control signals required by the ADC, including clock for the comparator and SAR logic, are generated internally. An innovative rising edge only variable delay-cell has been proposed for the ADC, which provides required delay only to the rising edge of the internally generated clock for the StrongArm latched comparator. The comparator's unsymmetrical clock, generated as a result of the rising edge only delay effect of the delay-cell, saves comparator mean power significantly in comparison with the comparator driven by the symmetrical clock. The proposed ADC features sampling-rate reconfigurability with a proportional power consumption, where its sampling-rate range varies from typical 40 kHz to a maximum 167 kHz. The trigger 'CLKSampling' signal is also tunable with respect to its duty-cycle besides time-period. Compounded by sampling-rate reconfigurability functionality, this extra feature makes ADC highly flexible, adaptable, and versatile. To detect and mitigate any metastability events of the comparator, the ADC is equipped with a simple metastability watchdog circuitry.

The ASAR ADC has been designed and fabricated in a 0.35 µm CMOS process and operates at a supply voltage of 3.3 V. In measurements, the ADC shows an ENOB of 7.76-bits and a peak SNDR of 48.47 dB at its typical sampling-rate of 40 kHz. Measured DNL and INL of the ADC lie within one LSB, while its measured DR is 48 dB. The measured performance (ENOB, SNDR, DR, DNL, and INL) of the ADC is the same at all sampling-rates covered by it. To highlight potential of the ADC architecture in terms of conversion-efficiency, a second version of the ADC has also been designed, whose digital section and

delay-cell operate at a supply voltage of 1.2 V. This has been achieved with the help of the level-shifters. The second version of the ADC exhibits the same performance as version 1. For a fair comparison of high voltage-based ADCs with low voltage-based ADCs, a normalized version of the figure-of-merit (FoM_{WN}) has been introduced. Version 1 of the ADC exhibits FoM_{WN} of 476 fJ/c-step at its maximum f_s of 167 kHz. For version 2 of the ADC, FoM_{WN} improves to 261.7 fJ/c-step with the level-shifter's power consumption included. It is further reduced to 243 fJ/c-step excluding power contribution of the level-shifters.

Single-channel, sampling-rate reconfigurable, dual-mode, 1st-order, EF NS-SAR is the second ADC architecture proposed in this thesis, whose step-by-step design process and measurement results were described in chapter 4. The core of the dual-mode NS-SAR ADC is 8-bit ASAR ADC of chapter 3. Dual-mode NS-SAR ADC has two operating modes: NS or free running mode, and incremental mode. This enables the use of the ADC for not only single-channel or single-sensor system, but also multi-channel or multi-sensor system. A 1st-order FIR filter has been utilized to introduce 1st-order EF NS functionality into 8-bit ASAR ADC. To save power, the OP-AMP of FIR filter is duty-cycled, i.e., it is turned on only when needed. A dedicated synthesized digital logic has been employed in the NS-SAR ADC to introduce the reset and decimation functions to achieve incremental mode operation. The operating mode of the dual-mode NS-SAR ADC can be selected externally. The dual-mode NS-SAR ADC also features f_s-reconfigurability functionality, owing to the use of an 8-bit f_s-reconfigurable ASAR ADC as its core. The f_s-reconfigurability range of dual-mode NS-SAR ADC spans from 40 kHz to 167 kHz at an OSR value of 8 and it comes with a proportional power consumption. This results in an equivalent Nyquist bandwidth of 2.5 kHz and 10.43 kHz, respectively. In both operating modes, the dual-mode NS-SAR ADC supports OSR values of 8, 16, and 32, thus changing its $f_s$and bandwidth accordingly. All the supported sampling-rates of the ADC can be operated with these OSR values, thus introducing a great flexibility and versatility in the ADC. Like the ASAR ADC, two versions of the dual-mode NS-SAR ADC have been designed: version 1 and version 2. All the sections of version 1 operate at a supply voltage of 3.3 V, while the digital section and delay-cell of version 2 operate at a supply voltage of 1.2 V.

The dual-mode NS-SAR ADC has been characterized in both modes separately. In NS mode, the version 1 of the ADC secures a measured ENOB of 10.6-bits, a peak SNDR of 66 dB, and dynamic range of 67 dB at typical f_s of 40 kHz with an OSR value of 8. The same performance (ENOB, SNDR, and DR) has been achieved at all other supported sampling-rates. 1.3 bits increase in ENOB and 8 dB in SNDR is achieved with doubling the OSR. The ADC achieves best FoM_{WN} of 511 fJ/c-step at the f_s of 167 kHz with an OSR value of 8. FoM_{WN} for version 2 of the ADC comes out to be only 296 fJ/c-step at its f_s of 132 kHz with an OSR value of 8. FoM_{SN} is 157 dB at all supported sampling-rates for both the versions. There is no degradation in performance (ENOB, SNDR, and DR) at all other supported sampling-rates of version 1 of the ADC. In addition, version 2 of the ADC in NS mode exhibits the same performance (ENOB, SNDR, and DR) as version 1.

In incremental mode, version 1 of the ADC secures a measured ENOB and peak SNDR of 10.25-bits and 63 dB, respectively at an OSR value of 8 at its typical f_s of 40 kHz. Doubling the OSR provides a 0.9-bit increase in ENOB and 6 dB in SNDR. At all other supported sampling-rates, the ADC exhibits the same performance as at typical f_s. Version 1 of the ADC achieves best FoM_{WN} at its maximum f_s of 167 kHz at an OSR of 8, and it is 670 fJ/c-step. Thanks to the use of 1.2 V for digital section and delay-cell, FoM_{WN} improves to 334 fJ/c-step at 132 kHz f_s at an OSR value of 8 for version 2. FoM_{SN} in incremental mode is constant for all covered sampling-rates and its value is 155 dB. Performance (ENOB and NSDR) of both the versions of the ADC in incremental mode is the same.

Section 3.12 and Section 4.12 provide performance summary of the ASAR ADC and the dual-mode NS-SAR ADC, respectively in tabular form.

5.2. Contributions

This section provides a summary of the contributions made during this thesis work. This is done by precisely listing the novelty and uniqueness of the two proposed ADC architectures one-by-one.

Distinctiveness and novelty of the proposed 8-bit ASAR ADC over all other ASAR ADCs proposed in the literature are summarized as follows:

(a) f_s-reconfigurability functionality with a proportional power consumption or almost constant energy-efficiency for all covered sampling-rates.
(b) The potential of further increase in the f_s by reducing the amount of the delay if desired for the application.
(c) The use of a novel variable rising edge only delay-cell.
(d) Generation of asymmetrical internal clock for the dynamic comparator, which reduces its average power consumption in comparison with a symmetrical clock driven dynamic comparator.
(e) Adaptability and flexibility of the ADC with respect to the duration of its sampling and conversion phase by varying the duty-cycle of well-controlled external 'CLKSampling' clock signal.
(f) Suitability of the proposed ADC architecture for ultra-scaled CMOS nodes (< 65 nm) with a high potential of power reduction and speed enhancement.
(g) Potential of resolution enhancement of the proposed ASAR ADC by introducing simple circuitry, such as noise-shaping without adding any significant design complexity.
(h) 1st ever ASAR ADC for multi-channel ASICs for space applications as per the author's best knowledge.
(i) Suitability of the ADC for use either at a fixed conversion speed or variable conversion speeds as per the application requirements.
(j) Open for the use for any radiation hardened technique if needed by the specific application.
(k) Suitable for other emerging earth/ground applications, such as wireless sensor nodes, biomedical implant devices, energy harvesting sensor nodes, neural recoding networks, etc.
(l) Suitable to be used as an ADC slice for time-interleaved ADCs for high-speed applications.

Besides the features (a-l) mentioned for the ASAR ADC, uniqueness and innovation of the proposed dual-mode NS-SAR ADC over all other NS-SAR ADCs proposed in the literature are further summarized as follows:

(m) 1st ever dual-mode NS-SAR ADC, which supports NS/free running mode and incremental mode for any application.
(n) 1st ever ADC which introduces a novel and simpler way of achieving incremental mode functionality in the NS-SAR ADC.
(o) 1st ever dual-mode NS-SAR ADC proposed for multi-channel ASICs for space applications.
(p) 1st ever dual-mode NS-SAR ADC implemented and fabricated in a 0.35 µm CMOS process.
(q) 1st ever dual-mode NS-SAR ADC which is asynchronous.
(r) Potential of further increase in ENOB and SNDR by introducing higher order (> 1st-order) NS without adding a substantial design complexity.
(s) One of those very few manufactured NS-SAR ADCs, which exhibit very good, measured performance (ENOB and SNDR) without the use of any complex design technique, such as mismatch error shaping, any type of CDAC calibration or trimming, etc.
(t) Suitable to be used as a coarse ADC for Zoom ADC architecture for high resolution applications.

5.3. Future Research Directions and Application Avenues

This section suggests some potential directions for the performance enhancement of the proposed ADC solutions. In addition, it highlights some important application areas and avenues where the proposed ADCs can be an attractive choice. It is worth mentioning that the performance enhancement methods mentioned in this section are not adopted during this thesis work, because the target application did not require this. However, these methods are highly auspicious for implementation in these ADC architectures if needed by the target application.

5.3.1. Further optimization of Area and Switching Energy of the CDAC of the ASAR ADC

One key ASAR ADC component, whose area and switching energy can further be reduced, is the CDAC. This is attractive since the CDAC is the primary area occupying block in the ASAR ADC. This can be achieved in two different ways. First, by the use of split capacitor CDAC topology instead of binary-weighted topology. Second, by the use of energy efficient CDAC switching technique. The use of split capacitor CDAC reduces the overall CDAC capacitance from $256.C_u$ of binary weighted CDAC to about $33.C_u$ for an 8-bit CDAC. This results in a significant decrease in area, and power of the CDAC. In addition, it increases the conversion speed of the ADC. However, particular care is needed for the layout design of split capacitor CDAC to ensure linearity.

Regarding the energy efficient CDAC switching scheme, two strategies can be adopted. First way is to use a technique like [89], where the MSB decision is done right in the start of the ADC conversion phase without the need for setting the MSB. This avoids the need for the MSB capacitor in the CADC, thus substantially reducing area, and switching energy. The second way is to adopt the top plate sampling method. In comparison with the bottom plate sampling, the top plate sampling permits the MSB decision right in the start of the conversion phase. This again leads to a significant reduction in the CDAC switching energy. One such scheme has been proposed in [234]. Both of these methods come with their own disadvantages, which need to be addressed judiciously.

5.3.2. Power and area optimization of digital section of the ADCs

For the proposed ADCs, the digital section has been realized using standard cells of the technology. The digital logic based on these standard cells might not be optimized in terms of power consumption. As the ASAR ADC is digital-intensive architecture, the digital section (e.g., SAR logic) power consumption is a significant source of power dissipation in the ADC. The power consumption of the digital section can be reduced if it is realized based on fully custom designed cells. This provides an opportunity to play with the metrics such as area, power, and speed.

5.3.3. Differential implementation

The proposed ADC architectures are also suitable for differential implementation if needed by the application. Differential implementation offers several advantages over single-ended architecture. First, it automatically cancels all common mode noise and interference sources, thus relaxing the design of the CADC layout. Second, it provides 6 dB more dynamic range. Third, it enables the use of energy efficient CDAC scheme. Some of these switching schemes include monotonic switching [87], V_{CM}-based switching [89], and bidirectional switching [233]. All these schemes need differential implementation.

5.3.4. The use of a preamplifier for StrongArm latched comparator

If required by the application, a low-gain preamplifier can be added before StrongArm latched comparator. This is especially useful if the application requires an ENOB more than 8 bit. The use of the preamplifier reduces the input refereed noise and offset voltage of the comparator. Also, it mitigates kickback noise problem.

5.3.5. Enhancement of Sampling-Rate of the ADCs

The proposed ASAR ADC exhibits a maximum sampling-rate of 167 kHz. It is because of the selection of a minimum delay value of 275 ns from the delay-cell (Figure 3.7). However, the ADC is capable of operating with a delay value as less as 30 ns with the utilized binary weighted CDAC. This delay value can further be reduced for other CDAC architectures, such as split capacitor. This simply means a significant increase in the sampling-rate of the ASAR ADC. Assuming a minimum delay of 30 ns, the ASAR ADC's sampling-rate turns out to be about 2-3 times the current maximum sampling-rate (167 kHz), i.e., about 350 kHz at-least. As the core of the dual-mode NS-SAR ADC is the ASAR ADC, the sampling-rates of dual-mode ADC also increase accordingly. For an OSR value of 8, the sampling-rate of the dual-mode NS-SAR ADC turns out to be about 45 kHz for the ASAR ADC sampling-rate of 350 kHz, as listed in Table 5.1. In addition, it becomes even more promising since achieving a delay of 30 ns or lower is easier than 275 ns or longer. This delay value can further be reduced if split capacitor CDAC topology is utilized, thus further increase in ADCs sampling-rates.

Table 5. 1. Relationship between delay value and sampling-rate of the ASAR ADC

Sr. No	Delay Value	f_s (kHz)	Comments
1	2.2 µs	40	1. Maximum Delay
2	1.1 µs	71.43	1. 1/2 of maximum delay (double sampling-rate in comparison with maximum delay case
3	550 ns	119	1. 1/4 of maximum delay (4 times sampling-rate in comparison with maximum delay case
4	275 ns	167	1. 1/8 of maximum delay (8 times sampling-rate in comparison with maximum delay case
5	137 ns	220	1. 1/16 of maximum delay (16 times sampling-rate in comparison with maximum delay case
6	68.5 ns	275	1. 1/32 of maximum delay (32 times sampling-rate in comparison with maximum delay case
7	30 ns	350	1. 1/64 of maximum delay (64 times sampling-rate in comparison with maximum delay case

5.3.6. The use of Open-Loop on-chip Buffers to reduce analog power consumption of the ADC

The ADCs use four closed loop on-chip buffers: input, common mode, and two voltage reference buffers. To reduce power consumption of these buffers, open-loop buffers can be utilized. This is especially attractive for the input buffer since it consumes significant power. Open loop input buffers, such as proposed in [261, 262], for ADC can be a promising choice in this regard. Open loop source follower topology can be an attractive choice for the realization of reference voltage buffers for their power saving.

5.3.7. The SNDR enhancement of the dual-mode NS-SAR ADC by introducing higher order NS

The ENOB and SNDR of the dual-mode NS-SAR ADC can further be enhanced by introducing higher order NS functions if needed by the application. As described in detail in section 2.7, NS-SAR ADCs with an order of 4 have already been proposed in the literature. Therefore, the proposed dual-mode NS-SAR ADC has a potential for high order NS functionality. The use of a 2nd-order NS can be especially attractive since it does not introduce significant design complexity and stability issues. With a 2nd order NS, the ENOB of ADC can be increased by 3-bits per doubling the OSR, which is twice as much as for the 1st-order NS.

5.3.8. The SNDR enhancement of the dual-mode NS-SAR ADC by introducing Mismatch Error Shaping Technique

Linearity errors caused by the CDAC mismatches are one of the biggest sources of performance degradation for the NS-SAR ADC. Achieving SNDR greater than 70 dB from NS-SAR ADC is extremely difficult without the use of some dedicated methods to offset CDAC mismatch and linearity errors. Several such techniques have been presented in literature, such as mismatch error shaping, dynamic element matching, background, and foreground calibration, as detailed in the literature review section for the NS-SAR ADCs in section 2.7. The proposed dual-mode NS-SAR ADC is a viable candidate for these techniques, especially if higher order NS needs to be adopted.

5.3.9. The possibility of making the ADCs radiation-hardened

Because of the radiation-robust characteristics of the use technology process (0.35 µm) as detailed in section 1.8.1.12, no dedicated technique has been adopted to make the ADCs radiation-hardened. However, the ADCs are open to any such technique to make it more robust against radiation effects (total ionizing dose and single events effects). This is especially valid if the proposed ADC architectures are to be implemented in the scaled technology processes, where small-channel devices are more susceptible to the radiation effects.

5.3.10. Implementation in Scaled Technology Nodes to get full advantages

These proposed ADC architectures are impeccably scaling-friendly because of their digital-intensive nature. Implementation in scaled technology nodes offers numerous benefits. First, it reduces the chip area. Second, it saves power. Third, it increases the ADC speed and sampling-rate significantly. Fourth, it enables achieving a better energy-efficiency. The improvement in power and energy efficiency of the ADC architectures have been validated by version 2 of the ADCs, where digital section operates at 1.2 V. A substantial improvement in both these metrics have been witnessed, as shown in Table 3.26 and Table 4.9.

5.3.11. The use of ADCs for multi-channel analog front-ends ASICs providing start-of-conversion signal for the ADC

Both the proposed ADCs need a start-of-conversion ‘Sample’ signal to start conversion process. They provide end-of-conversion (EoC) signal once they are done with the conversion process. The duty cycle and time period of the start-of-conversion (SOC) signal are flexible, as explained earlier during the operation of the ADCs. These observations make the ADC attractive for multi-channel analog front-end ASICs which can generate the start-of-conversion signal for the ADCs and provide this signal to the ADCs when an A/D conversion is needed. The ADCs after performing the conversion, can feed back the EoC signal to the analog front-end, thus informing it of their availability for the next conversion. This is shown pictorially in Figure 5.1. This can greatly be facilitated by the co-design of the analog front-end and ADC of multi-channel ASICs.

5.3.12. The use of the ASAR and dual-mode NS-SAR ADC as a core for the Zoom ADC for higher resolution applications

Zoom ADC is an emerging hybrid architecture to get high dynamic range at relatively lower sampling-rates. The Zoom ADC uses two ADCs: coarse ADC and fine ADC. The details of the working of Zoom ADC are provided in section 2.3.3.2. The coarse ADC in Zoom ADC architecture is almost always a SAR ADC or NS-SAR ADC. Because of its flexible and tunable sampling-rate-based advantages, the proposed ASAR ADC is an attractive choice to serve as a coarse ADC in a Zoom ADC architecture if a high dynamic range is needed by the application. The same is the case for the NS-SAR ADC which is even more promising because of its high SNDR than simple ASAR ADC.

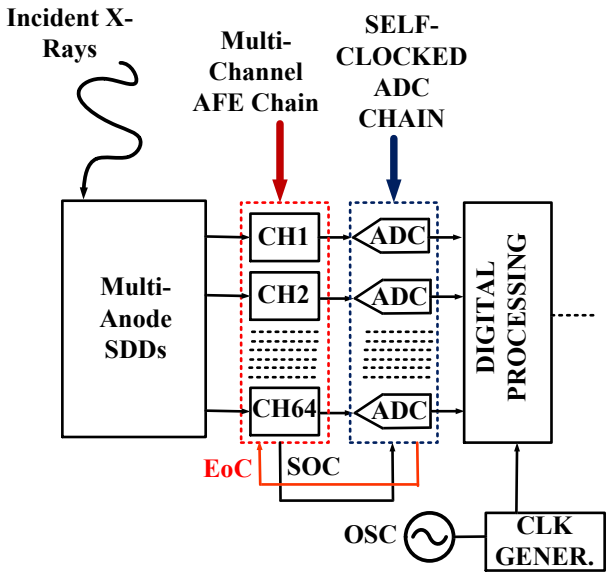


Figure 5. 1. The use of ADC for analog front-end ASICs providing the start-of-conversion (SOC) signal to the ADCs.

5.3.13. The use of the ASAR and dual-mode NS-SAR ADC as a slice of time-interleaved ADC for higher data rate communication applications

Time-interleaved ADCs are popular ADC architecture for high-speed applications, such as wireless transceivers for 5G and 6G communication, as well as wireline transceivers for Serializer and Deserializer (Serdes) applications. For these applications, multiple slices of the ADCs are interleaved to get a high sampling-rate. Typical ENOB needed for one slice of these ADCs is 6-8 bits. Because of robustness and flexibility-based advantages, proposed ASAR ADC is an auspicious choice to act as a slice for time-interleaved ADC. For applications where lesser number of ADC slices are needed because of relatively lower sampling-rate requirement, even dual-mode NS-SAR ADC becomes an attractive option as a slice for time-interleaved ADC.

5.3.14. The use of ADCs for applications other than Space

Besides space applications, the proposed ADCs are highly promising candidates for other emerging applications which need low-to-medium sampling-rates. Some of such applications include biomedical implants devices and wearable sensors, neural signal acquisition, wireless power transfer systems, internet-of-things, and energy harvesting sensor nodes.

APPENDICES

APPENDIX 1: Verilog-A Codes of ASAR ADC

1.1. Verilog-A code of an NMOS switch

```
// VerilogA for Rashid_Veriloga, MOS_Switch1, veriloga
`include "constants.h"
`include "disciplines.h"
module MOS_Switch1 (vp, vn, vcontrolp, vcontroln);
input vcontrolp, vcontroln;
inout vp, vn;
electrical vp, vn, vcontrolp, vcontroln;
parameter real vth=1.65;
parameter real Ron=2;
parameter real Roff=1e15;
parameter real td=0, tr=100p, tf=100p;
real R, Rr;
analog
begin
if(V(vcontrolp,vcontroln)>vth)
R=Ron;
else
R=Roff;
Rr=transition(R, td, tr, tf);
V(vp,vn) <+ I(vp,vn)*Rr;
end
endmodule
```

1.2. Verilog-A code of a PMOS switch

```
// VerilogA for Rashid_Veriloga, MOS_Switch2, veriloga
`include "constants.h"
`include "disciplines.h"
module MOS_Switch2 (vp, vn, vcontrolp, vcontroln);
input vcontrolp, vcontroln;
inout vp, vn;
electrical vp, vn, vcontrolp, vcontroln;
parameter real vth=1.65;
parameter real Ron=2;
parameter real Roff=1e15;
parameter real td=0, tr=100p, tf=100p;
real R, Rr;
analog
begin
if(V(vcontroln,vcontrolp)>vth)
R=Ron;
else
R=Roff;
Rr=transition(R, td, tr, tf);
V(vp,vn) <+ I(vp,vn)*Rr;
end
endmodule
```

1.3. Verilog-A code of comparator

```
// VerilogA for Rashid_Veriloga, Comparator44, veriloga
`include "constants.h"
`include "disciplines.h"
module comparator44 (vin, outp, outn, vdd, vss, vref, clock_comp);
input vin, vref, clock_comp;
inout vdd, vss;
output outp, outn;
parameter clock_vth=1.65, delay=1n, tr=100p, tf=100p;
electrical vin, vref, vdd, outp, outn, vss, clock_comp;
real result, result1;
analog
begin
@(cross(V(clock_comp)-clock_vth,+1))
begin
result=(V(vin)>V(vref))?V(vdd):V(vss);
result1=(V(vin)>V(vref))?V(vss):V(vdd);
end
@(cross(V(clock_comp)-clock_vth,-1))
begin
result=V(vdd);
result1=V(vdd);
end
V(outp) <+ transition(result, delay, tr, tf);
V(outn) <+ transition(result1, delay, tr, tf);
end
endmodule
```

1.4. Verilog-A code of 2-inputs AND gate (NAND operation can be achieved by using inverter)

```
// VerilogA for Rashid_Veriloga, AND2, veriloga
`include "constants.h"
`include "disciplines.h"
module AND2 (in1, in2, out);
input in1, in2;
output out;
electrical in1, in2, out;
parameter vth=1.65;
parameter real td=200p;
parameter real tr=100p, tf=100p;
real result;
analog
begin
@(cross(V(in1)-vth) or cross(V(in2)-vth))
result= ((V(in1) > vth) && (V(in2) > vth) ? 3.3 : 0);
V(out) <+ transition (result, td, tr, tf);
end
endmodule
```

1.5. Verilog-A code of 2-inputs XOR gate

```
// VerilogA for Rashid_Veriloga, XOR2, veriloga
`include "constants.h"
```

```
`include "disciplines.h"
module XOR2 (in1, in2, out);
input in1, in2;
output out;
electrical in1, in2, out;
//parameter real vh=3.3;
//parameter real vl=0;
parameter vth=1.65;
parameter real td=200p;
parameter real tr=100p, tf=100p;
real result;
analog
begin
@(cross(V(in1)-vth) or cross(V(in2)-vth))
result= ((V(in1) > vth) ^ (V(in2) > vth) ? 3.3 : 0);
V(out) <+ transition (result, td, tr, tf);
end
endmodule
```

1.6. Verilog-A code of Inverter

```
// VerilogA for Rashid_Veriloga, NOT, veriloga
`include "constants.h"
`include "disciplines.h"
module NOT (in, out);
input in;
output out;
electrical in, out;
//parameter real vh=3.3;
//parameter real vl=0;
parameter vth=1.65;
parameter real td=500p;
parameter real tr=100p, tf=100p;
real result;
analog
begin
// @(cross(V(in)-vth))
// result= ((V(in) > vth) ? 0 : 3.3);
if (V(in) > vth)
result=0;
else
result=3.3;
V(out) <+ transition (result, td, tr, tf);
end
endmodule
```

1.7. Verilog-A code of one DFF used in SAR logic

```
// VerilogA for Rashid_Veriloga, DFF_reset2, veriloga
`include "constants.h"
`include "disciplines.h"
module DFF_reset22 (d, clock, q, qbar, set, reset);
input d, clock, set, reset;
output q, qbar;
electrical d, clock, q, qbar, set, reset;
```

```
parameter real tdcq=10n; // clock to q delay of DFF
parameter real tr=1p, tf=1p;
parameter real vth=1.65;
parameter integer dir=+1; //for positive edge triggered operation
real result, result1;
analog
begin
if(V(set) > vth) // set logic
begin
result=3.3;
result1=0;
end
if(V(reset) > vth) // reset logic
begin
result=0;
result1=3.3;
end
@(cross(V(clock)-vth,dir)) // Normal DFF operation at positie edge of the clock
begin
if(V(d) > vth)
begin
result=3.3;
result1=0;
end
1
else
begin
result=0;
result1=3.3;
end
end
V(q)<+ transition(result,tdcq,tr,tf);
V(qbar)<+ transition(result1,tdcq,tr,tf);
end
endmodule
```

1.8. Verilog-A code of other DFF used in SAR logic

```
// VerilogA for Rashid_Veriloga, DFF_reset3, veriloga
`include "constants.h"
`include "disciplines.h"
module DFF_reset3 (d, clock, q, qbar, set, reset);
input d, clock, set, reset;
output q, qbar;
electrical d, clock, q, qbar, set, reset;
parameter real tdcq=1n; // clock to q delay of DFF
parameter real tr=100p, tf=100p;
//parameter real vh=3.3; // level high of output
//parameter real vl=0; // level low of output
//parameter real vth=(vh+vl)/2; // threshold level for input
parameter real vth=1.65;
parameter integer dir=+1; //for positive edge triggered operation
real result, result1;
analog
begin
```

```
if(V(set) < vth) // set logic
begin
result=3.3;
result1=0;
end
if(V(reset) > vth) // reset logic
begin
result=0;
result1=3.3;
end
/* @(initial_step) // initializing the outputs
begin
result=0;
result1=3.3;
1
end */
@(cross(V(clock)-vth,dir)) // Normal DFF operation at positie edge of the clock
begin
if(V(d) > vth)
begin
result=3.3;
result1=0;
end
else
begin
result=0;
result1=3.3;
end
end
V(q)<+ transition(result,tdcq,tr,tf);
V(qbar)<+ transition(result1,tdcq,tr,tf);
end
endmodule
```

APPENDIX 2: Verilog-A Codes of dual-mode NS-SAR ADC (Incremental mode)

2.1. Verilog-A code of counter 1 for incremental mode logic

```
// VerilogA for Rashid_Veriloga, counter_inc, veriloga
`include "constants.h"
`include "disciplines.h"
module counter_inc (clock, count);
input clock;
output count;
electrical clock;
electrical count;
parameter vth=1.65;
parameter osr=8;
parameter increment=1;
parameter del=100p, tr=100p, tf=100p;
real result;
analog
begin
@(initial_step)
```

```
begin
result=0;
// result1=0;
end
@(cross(V(clock)-vth,+1))
begin
//while (result==osr)
if (result<osr)
result=result+increment;
else if (result==osr)
result=1;
end
V(count) <+ transition(result, del, tr, tf);
end
endmodule
```

2.2. Verilog-A code of counter 2 for incremental mode logic

```
// VerilogA for Rashid_Veriloga, counter_inc_1, veriloga
`include "constants.h"
`include "disciplines.h"
module counter_inc_1 (in, out);
input in;
output out;
electrical in, out;
parameter osr=8;
real result;
analog
begin
if (V(in)==osr)
result=0;
else
result = 3.3;
V(out) <+ result;
end
endmodule
```

2.3. Verilog-A code of decimator for incremental mode logic

```
// VerilogA for Rashid_Veriloga, decimator_inc, veriloga
`include "constants.h"
`include "disciplines.h"
module decimator_inc(vin, vout, vclk);
input vin,vclk;
output vout;
electrical vin, vout, vclk;
parameter integer OSR=8;
parameter real vth=1.65;
parameter real tdel = 100p;
parameter real trise = 100p;
parameter real tfall = 100p;
integer count;
real sum=0;
real vout_val;
analog begin
@ (cross(V(vclk) - vth, 1.0)) begin
// sum = sum + V(vin);
```

```
// if (count < OSR) begin
sum = sum + V(vin);
count= count + 1;
//end
if (count == OSR) begin
count = 0;
// vout_val = sum;
// sum = 0.0;
sum = V(vin);
// sum = sum + V(vin);
end
vout_val = sum;
end
V(vout) <+ transition(vout_val,tdel,trise,tfall);
end
endmodule
```

2.4. Verilog-A code of digital to decimal conversion for incremental mode logic

```
// VerilogA for Rashid_Veriloga, printer1, veriloga
`include "constants.h"
`include "discipline.h"
module printer1(v0, v1, v2, v3, v4, v5, v6, v7, vectorout);
input v0, v1, v2, v3, v4, v5, v6, v7;
output vectorout;
electrical v0, v1, v2, v3, v4, v5, v6, v7, vectorout;
parameter real threshold=1.65;
integer vector, vv0, vv1, vv2, vv3, vv4, vv5, vv6, vv7;
analog begin
if (V(v0) > threshold)
vv0=1;
else vv0=0;
if (V(v1) > threshold)
vv1=2;
else vv1=0;
if (V(v2) > threshold)
vv2=4;
else vv2=0;
if (V(v3) > threshold)
vv3=8;
else vv3=0;
if (V(v4) > threshold)
vv4=16;
else vv4=0;
if (V(v5) > threshold)
vv5=32;
else vv5=0;
if (V(v6) > threshold)
vv6=64;
else vv6=0;
if (V(v7) > threshold)
vv7=128;
else vv7=0;
vector=vv0+vv1+vv2+vv3+vv4+vv5+vv6+vv7;
V(vectorout) <+ transition (vector,100p,100p,100p);
```

```
end
endmodule
```

APPENDIX 3: Verilog Codes of dual-mode NS-SAR ADC (Incremental mode)

3.1. Verilog code of Synthesized digital logic for dual-mode NS-SAR ADC to get incremental mode operation

```
//Verilog HDL for "DK2021TRY", "verilog_decimator11" "functional"
module verilog_decimator1111 (in, CLK1, CLK2, reset, mode, out, EOC_new, RESET_GLOBAL);
input [7:0] in;
input [1:0] mode;
input CLK1, CLK2;
input RESET_GLOBAL;
output reset;
output EOC_new;
output [12:0] out;
reg [12:0] out;
reg [12:0] sum;
reg [4:0] counter;
reg [4:0] counter1;
reg reset;
reg reset_internal;
reg EOC_new;
reg EOC_new_internal;
//reg [4:0] OSR;
always@(posedge CLK1, posedge RESET_GLOBAL)
begin
if(RESET_GLOBAL)
begin
// reset<=0;
// EOC_new<=0;
sum<=0;
counter<=0;
out<=0;
// counter1<=0;
// reset_internal<=0;
// OSR<=0;
end
else
begin
case (mode)
0:
begin
out<=in;
counter<=0;
// EOC_new<=0;
end
1:
begin
// OSR =7;
1
if(counter==7)
begin
counter<=0;
```

```
sum<=in;
// EOC_new<=1;
end
else
begin
sum<=sum+in;
counter<=counter+1;
// EOC_new<=0;
end
out<=sum;
end
2:
begin
// OSR =15;
if(counter==15)
begin
counter<=0;
sum<=in;
// EOC_new<=1;
end
else
begin
sum<=sum+in;
counter<=counter+1;
// EOC_new<=0;
end
out<=sum;
end
3:
begin
2
// OSR =31;
if(counter==31)
begin
counter<=0;
sum<=in;
// EOC_new<=1;
end
else
begin
sum<=sum+in;
counter<=counter+1;
// EOC_new<=0;
end
out<=sum;
end
//default:
endcase
end
end
always@(posedge CLK2, posedge RESET_GLOBAL)
begin
if(RESET_GLOBAL)
begin
reset<=0;
EOC_new<=0;
```

```
EOC_new_internal<=0;
// sum<=0;
// counter<=0;
counter1<=0;
reset_internal<=0;
// OSR<=0;
end
else
begin
case(mode)
0:
begin
reset<=1'b0;
counter1<=0;
3
EOC_new<=0;
end
1:
begin
// OSR=7;
if(counter1==7)
begin
counter1<=0;
reset_internal<=1'b1;
EOC_new_internal<=1;
end
else
begin
counter1<=counter1+1;
reset_internal<=1'b0;
EOC_new_internal<=0;
end
reset<=reset_internal;
EOC_new<= EOC_new_internal;
end
2:
begin
// OSR=15;
if(counter1==15)
begin
counter1<=0;
reset_internal<=1'b1;
EOC_new_internal<=1;
end
else
begin
counter1<=counter1+1;
reset_internal<=1'b0;
EOC_new_internal<=0;
4
end
reset<=reset_internal;
EOC_new<= EOC_new_internal;
end
3:
begin
```

```
// OSR=31;
if(counter1==31)
begin
counter1<=0;
reset_internal<=1'b1;
EOC_new_internal<=1;
end
else
begin
counter1<=counter1+1;
reset_internal<=1'b0;
EOC_new_internal<=0;
end
reset<=reset_internal;
EOC_new<= EOC_new_internal;
end
//default:
endcase
end
end
endmodule
```

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List of Publications

1. **R. Karim**, M. Grassi, and P. Malcovati, “An Asynchronous Incremental/Noise-Shaping SAR ADC Featuring Sampling-Rate Reconfigurability with Power-Scalability for Space Applications”, submitted in IEEE Journal of Solid State Circuits

2. **R. Karim**, M. Grassi, and P. Malcovati, “An 8 bit-ENOB Sampling-Rate Reconfigurable Asynchronous SAR ADC With Metastability Watchdog Circuit for Activity-Driven Multi-Channel CMOS Readout ASICs for Space Applications,” in International Journal of Electronics and Communications (AEUE), vol 173, 2024, doi: https://doi.org/10.1016/j.aeue.2023.154979

3. **R. Karim** and P. Malcovati, “On-Chip-Antennas: Next Milestone in the Big World of Small Satellites— A Survey of Potentials, Challenges, and Future Directions,” in IEEE Aerospace and Electronic Systems Magazine, vol. 36, no. 1, pp. 46-60, 1 Jan. 2021, doi: 10.1109/MAES.2020.3016751.

4. **R. Karim**, M. Grassi and P. Malcovati, "1st-Order Error-Feedback Sampling-Rate Reconfigurable Noise-Shaping SAR ADC for Multi-Channel CMOS Front-End ASICs for Space Applications," *2023 21st IEEE Interregional NEWCAS Conference (NEWCAS)*, Edinburgh, United Kingdom, 2023, pp. 1-5, doi: 10.1109/NEWCAS57931.2023.10198081.

5. **R. Karim**, M. Grassi and P. Malcovati, “An 8-ENOB Sampling-Rate Reconfigurable Asynchronous SAR ADC for Space Applications,” 2022 International Conference on Microelectronics (ICM), Casablanca, Morocco, 2022, pp. 173-176, doi: 10.1109/ICM56065.2022.10005517.