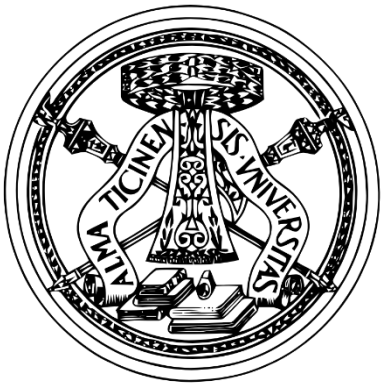

Università degli Studi di Pavia

Dipartimento di Ingegneria Industriale e dell'Informazione,

Ph.D. School in Microelectronics

Ultra-Low Phase Noise DCO Design for Automotive Radar Applications Using Advanced CMOS Technologies

Author:

Ioanna Apostolina

Supervisors:

D. Manstretta, R. Castello

Abstract

In applications where precise frequency synthesis is crucial, such as generating carrier signals for transmission systems, the issue of phase noise takes center stage in defining system performance. The demand for low phase noise frequency synthesizers has significantly increased, especially with the growing need for higher data rates in modern communication systems. Another critical domain where phase noise plays a pivotal role is in radar systems.

Radar systems utilize the Doppler effect to extract essential information about target distance and speed by comparing the frequencies of transmitted and received signals. While radar systems are renowned for their precision, their inherent complexity often results in high costs. Traditionally, they have found extensive use in aviation, particularly for detecting disturbances. However, in recent years, radar systems have made their way into the automotive sector, specifically in advanced driving assistance systems (ADAS). In a digitally controlled oscillator (DCO)-based frequency synthesizer DCO itself, is one of the most critical building blocks in an integrated mm-wave radar transceiver. In truth, when designing a DCO, stringent tradeoffs between various performance parameters must be considered, such as the phase noise (PN), frequency tuning range (TR), start-up robustness, power consumption, and area. The design of DCOs that are capable of simultaneously achieving low PN and a wide TR is a very challenging task, especially at mm-wave frequencies.

This thesis focuses on oscillators, which are the fundamental building blocks of frequency synthesizers in ultra-scaled CMOS technology, addressing this challenge. The primary challenge now is to achieve performance levels comparable to those attainable with bipolar technology.

After providing a brief overview of the fundamental operating principles of a typical radar, we proceed to outline a methodology for identifying the optimal oscillation frequency in analog circuit design. This critical frequency, essential for achieving peak performance, is systematically determined to ensure optimal circuit operation. The subsequent section details the design of a 20GHz quad-core oscillator, leveraging the advantages of a class B oscillator with tail coupling at the second

harmonic through transformers. This strategic design effectively mitigates flicker noise from active devices, addressing a significant limitation in modern CMOS technologies.

Finally, we present measured results following a fourfold multiplication, demonstrating the oscillator's suitability for automotive radar applications in compliance with regulatory requirements.

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List of Acronyms

ADAS Advanced Driver Assistance Systems

BER Bit Error Rate

BiCMOS Bipolar and Complementary Metal-Oxide-Semiconductor

BJT Bipolar Junction Transistor

CMOS Complementary Metal-Oxide-Semiconductor

DCO Digitally Controlled Oscillator

FMCW Frequency Modulated Continuous Wave

FoM Oscillator Figure of Merit

FR2 Frequency Range 2

HBT Heterojunction Bipolar Transistor

IC Integrated Circuit

IF Intermediate Frequency

IoT Internet of Things

ISF Impulse Sensitivity Function

LO Local Oscillator

LoS Line of Sight

LTE Long Term Evolution

LTI Linear Time Invariant

LTV Linear Time Variant

MIMO Multiple Input Multiple Output

MOS Metal-Oxide-Semiconductor

PA Power Amplifier

PLL Phase-Locked Loop

PSD Power Spectral Density

Q Quality factor

RF Radio Frequency

RMS Root Mean Square

SCR Signal-to-Clutter Ratio

SiGe Silicon Germanium

SNR Signal-to-Noise Ratio

TR Tuning Range

V2X Vehicle to everything

VCO Voltage-Controlled Oscillator

Intoduction

Radar systems stand as pivotal tools across applications, spanning from defense and surveillance to weather monitoring and automotive safety. Their significance lies in their ability to precisely detect and track targets amidst various environmental conditions, thereby necessitating a deep understanding of their operational intricacies. This thesis has a particular focus on Digitally Controlled Oscillators used Frequency Modulated Continuous Wave (FMCW) radar systems and the challenges they entail.

Chapter 1 introduces the foundational principles of radar operation. It starts with an overview of basic concepts and then moves on to discuss the Radar Range Equation, which is crucial for understanding radar performance factors. Following that, the chapter explores FMCW radars, detailing how they work and highlighting their unique characteristics.

Chapter 2 moves on to discuss the critical requirements and design considerations in radar systems. It covers topics like selecting the appropriate frequency synthesizer and managing phase noise effectively, which are key factors influencing radar performance. These discussions lay the groundwork for the subsequent chapters, ensuring a comprehensive understanding of radar technology.

Chapter 3 shifts the focus to oscillator noise, a significant challenge for radar precision. This chapter conducts a detailed analysis using impulse sensitivity functions to examine phase noise in both single and multicore oscillator setups. It also explores innovative techniques like harmonic-coupled oscillators and quad-core designs to enhance phase noise performance.

Chapter 4 delves into advanced techniques for frequency multiplication in millimeter-wave applications. It focuses on designing frequency quadruplers and enhancing buffering mechanisms for seamless integration with high-frequency outputs. The empirical validation of these methodologies through test chip implementations and measurement results adds an important practical aspect to the theoretical discussion.

In conclusion, this thesis aims to advance radar technology by focusing on the practical design and optimization of digitally controlled oscillators (DCOs). Addressing

challenges and exploring pragmatic solutions, the research seeks to enhance DCO performance and contribute to the continuous improvement of radar systems.

Chapter 1

1.1 Introduction

In the fast-paced world of automotive radar applications, precision and reliability are non-negotiable. These systems are entrusted with the critical task of safeguarding vehicles by accurately detecting and tracking objects in their vicinity. To achieve this, radar systems rely on precise frequency synthesis, a key factor that significantly impacts their performance. Traditionally, phase-locked loops (PLLs) have been employed as frequency synthesizers due to their ability to filter out much of the low-frequency phase noise originating from the local oscillator, the heart of a PLL-based system. However, with the rise of modern communication systems demanding ever-increasing data rates and the stringent accuracy requirements of next-generation radar technology, operating frequencies in the millimeter-wave range have become indispensable, as depicted in Figure 1.1.

Oscillator phase noise holds immense significance in the context of frequency synthesis for automotive radar applications. While radar technology has undergone significant advancements, with ever-more sophisticated algorithms and hardware, the fundamental element of precise frequency synthesis remains indispensable. Phase noise, often overlooked in casual discussions about radar, can have a profound impact on system performance, affecting critical aspects such as range accuracy, target resolution, and interference rejection.

Pursuing high-performance solutions has often led to the preference for compound technologies like Silicon Germanium (SiGe). In contrast, Complementary Metal-Oxide-Semiconductor (CMOS) technologies offer economic advantages by enabling high integration into modern applications. However, ultra-scaled CMOS technologies present a challenge in the form of significant flicker noise, which can be upconverted into phase noise by the oscillator. This necessitates careful consideration and specialized design approaches to mitigate this issue. This chapter serves as a valuable reference point for delving into radar principles and the operational intricacies of Frequency Modulated Continuous Wave (FMCW) radar, providing critical design considerations and insights into emerging trends in the field.

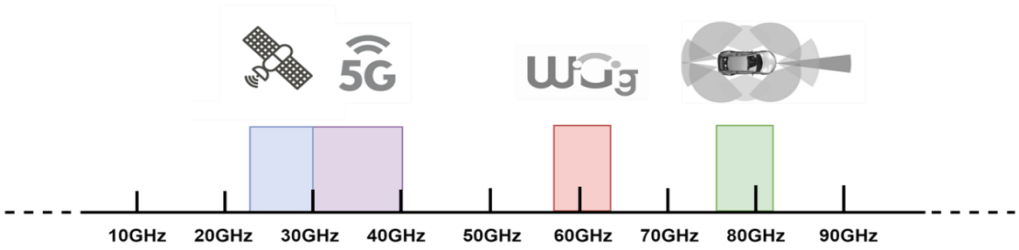


Figure 1.1 Contemporary applications allocation in the frequency spectrum.

1.2 Concept of Radar Operation

Radar is an electromagnetic device primarily used for detection and location of objects (targets). The word radar is an acronym derived from the phrase Radio Detection and Ranging. In general, radar operates by transmitting electromagnetic energy—a pulse-modulated sine wave for example—and detects the returned echo to extract target information such as range, velocity, position, and reflectivity signature. In general, radar operates by transmitting electromagnetic energy—a pulse-modulated sine wave for example—and detects the returned echo to extract target information such as range, velocity, position, and reflectivity signature [1].

Radar technology is typically classified into two primary branches: pulsed radar and continuous wave (CW) radar. Pulsed radar systems operate by sending out finite-duration signals at regular intervals. During the time interval between transmissions, they remain in a listening mode to capture any reflected signals. Distance estimation from a target is then calculated based on the elapsed time between transmission and reception. On the other hand, continuous wave (CW) radars operate by continuously emitting a continuous waveform into the medium while simultaneously listening for any scattered waveforms from potential targets. CW radars can estimate the velocity of the target by comparing the received waveform to the transmitted one, taking advantage of the Doppler effect, which causes an apparent frequency shift in the reflected signal.

However, in the case of CW radars, estimating the distance to a target is challenging unless some form of modulation is added to the transmitted waveform. To overcome this limitation, the transmitted signal can be modulated either in amplitude or frequency, enabling the radar system to estimate the distance to the target.

1.3 The Radar Range Equation

The radar equation represents a fundamental mathematical relationship that considers various factors affecting a radar system. It not only considers the radar system's key parameters but also factors in the characteristics of the target, its surroundings, the propagation path, and the medium through which the radar signal travels. This equation serves several valuable purposes, such as determining the maximum range at which a radar can detect a target, aiding in radar system comprehension, and forming the foundation for radar system analysis and design. It takes into account essential factors such as the transmitter's power P_t, the gains of both the transmitting G_t and receiving G_r antennas, the wavelength of the radar signal λ, the target's radar cross-section σ_{tgt}, and the radar's minimum detectable power threshold $P_{r(min)}$ [2]. The Radar max range is defined as:

$$R_{max} = \sqrt[4]{\frac{P_t G_t \sigma_{tgt} \lambda^2 G_r}{64\pi^3 P_{r(min)}}} \tag{1.3-1}$$

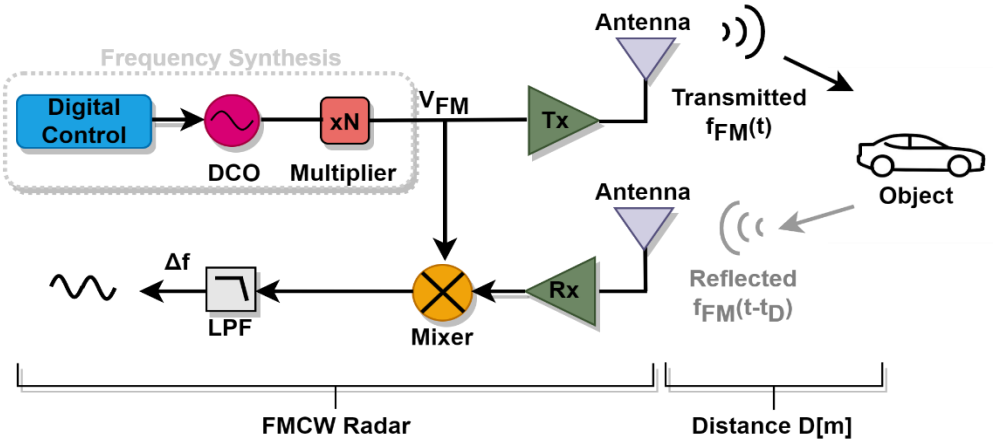


Figure 1.2 Block diagram of a generic FMCW radar system

This simplified radar equation serves as a basic framework for preliminary radar range estimations but falls short in accurately predicting the performance of real-world radar systems. Its limitations stem from its failure to encompass the multitude of losses within

the radar system and the inherent unpredictability of certain parameters. To obtain a more realistic and precise assessment of radar range, a comprehensive analysis must factor in a multitude of variables. These variables include losses within the radar system, such as thermal and signal-processing losses, as well as considerations related to the propagation medium and atmospheric noise.

Frequency-Modulated Continuous Wave (FMCW) radars as seen in Fig. 1.2 represent a specialized subclass of Continuous Wave (CW) radars, characterized by their utilization of frequency modulation to enable precise estimation of target distances [3]. In the context of FMCW radar operation, a sinusoidal wave with frequency modulation is transmitted. This modulation is organized into periodic segments termed "chirps." Each chirp exhibits a consistent structure, commencing with a predetermined base frequency, followed by a linear increase in frequency to a predetermined maximum frequency, and concluding with an abrupt frequency reduction to the initial starting point. At the receiver's end, the reflected signal is combined with the original signal to yield a waveform with a constant frequency. This waveform simplifies subsequent signal processing.

A group of chirps constitutes what is referred to as a "radar frame." Typically, these radar frames consist of 256, 512, or 1024 chirps within a single frame.

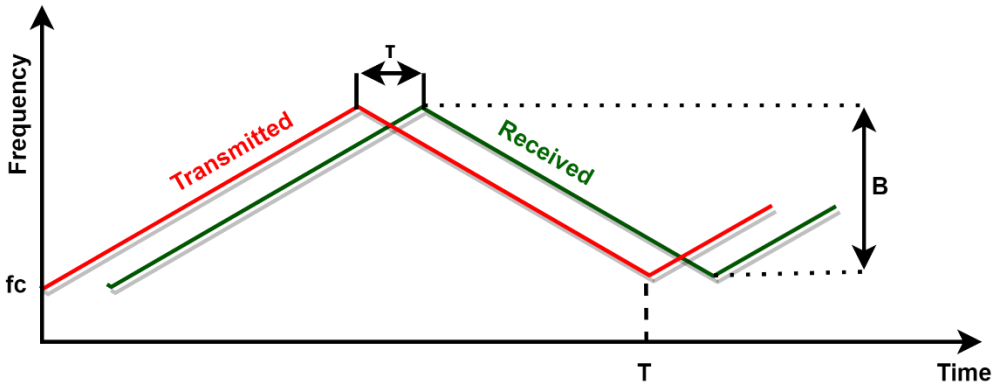


Figure 1.3 Simplified Chirp frequency representation.

1.4 FMCW Radars

Frequency-Modulated Continuous Wave (FMCW) radars represent a specialized subclass of Continuous Wave (CW) radars, characterized by their utilization of frequency modulation to enable precise estimation of target distances. In the context of FMCW radar operation, a sinusoidal wave with frequency modulation is transmitted. This modulation is organized into periodic segments termed "chirps." Each chirp exhibits a consistent structure, commencing with a predetermined base frequency, followed by a linear increase in frequency to a predetermined maximum frequency, and concluding with an abrupt frequency reduction to the initial starting point. At the receiver's end, the reflected signal is combined with the original signal to yield a waveform with a constant frequency as in Fig. 1.3. This waveform simplifies subsequent signal processing. A group of chirps constitutes what is referred to as a radar frame.

1.4.1 Operation of an FMCW Radar

The linear frequency increment within a period T, as described, can be expressed by the function [2]:

$$f(t) = f_0 + St \tag{1.3-1}$$

Here, f_0 represents the carrier frequency, and S denotes the steepness of the linear frequency increase. The steepness, S, is defined as:

$$S = B / T \tag{1.4-2}$$

Where B represents the bandwidth, and T is the duration of the frequency sweep.

Depending on the sign of S, the chirp is classified as either an up-chirp (when $S > 0$) or a down-chirp (when $S < 0$). The transmitted waveform of an FMCW radar is a cosine wave in the following form:

$$X(t) = A\,cos\,(\psi(t))$$

(1.4-3)

Here, $X(t)$ represents the waveform, A is the amplitude, and $\psi(t)$ signifies the phase of the waveform. After integrating the over time, the angle $\psi(t)$ the equation becomes:

$$X_{tx} = A_{tx}\cos\left(2\pi\left(f_c t + \frac{S}{2}t^2\right) + \psi_0\right)$$

(1.4-4)

In this equation, A_{tx} represents the signal amplitude, f_c stands for the carrier frequency, S indicates the steepness of the curve, and ψ_0 denotes the phase at time 0.

In an FMCW (Frequency Modulated Continuous Wave) radar system, the radar signal is transmitted towards the target, and upon interaction with the target, it is scattered back towards the receiver. This interaction, often referred to as reflection, enables the radar system to measure various parameters, including the distance R between the target and the receiver. When considering a scenario where the target is stationary, we can analyze how the time delay between the transmission of the radar signal and its reception is determined. In this context, the time delay corresponds to the time it takes for the radar signal to travel from the transmitter to the target and then return to the receiver. This time delay is a crucial factor in calculating the distance to the target and is determined based on the finite speed of the radar signal's propagation.

$$\tau_{st} = \frac{2R}{C}$$

(1.4-5)

Considering that R is the distance between the target and the antenna, c represents the speed of light, and the factor 2 is required because of the round -trip delay, we can deduce the additional time delay, τ, when the target is moving at a constant radial velocity v away from the receiver. The additional time delay, τ, due to the target's motion can be calculated as follows:

$$\tau_{mv} = \frac{2vt}{c}$$

(1.4-6)

The total delay can be expressed as the sum of two components: one component represents the additional distance the target has traveled from the receiver at time t, denoted as vt, and the other component is related to the speed of light, represented by c. It's important to note that the reference point for time $t = 0$ is when the target was initially at a distance R from the receiver. Therefore, the total delay is a combination of these two factors as:

$$\tau_{tot} = \frac{2(R + vt)}{c}$$

(1.4-7)

So, the received signal will be:

$$X_{rx}(t - \tau) = A_{rx} \cos\big(\psi(t - \tau)\big)$$

(1.4-8)

After applying a low-pass filter on the receiver side in the case of FMCW radar, when mixing the received signal (RX) and the transmitted signal (TX), the equation simplifies to:

$$X_{IF} = \frac{A_{rx}A_{tx}}{2}\big[\cos\big(\psi(t) - \psi(t - \tau)\big)\big]$$

(1.4-9)

When both the radar and the target are stationary, the Doppler frequency becomes zero, resulting in a simplified equation:

$$X_{IF} = \frac{A_{rx}A_{tx}}{2}\left[\cos\left(4\pi\left(\frac{SR}{c}t + \frac{f_c R}{c}\right)\right)\right]$$

(1.4-10)

The final frequency will be determined by:

$$f_{XIF} = \frac{2SR}{C} = S\tau_{st}$$

(1.4-11)

1.4.2 Features of FMCW Radars

FMCW radars have some benefits that make them appropriate for industrial packages. A few of the foremost benefits are referred to underneath [3-4].

Precision Distance Measurement and Resolution

In the realm of FMCW (Frequency Modulated Continuous Wave) radar systems, precise distance measurements are paramount for diverse applications. Central to this accuracy is the fundamental range equation:

$$R = \frac{cf_s N_T}{4N_B}$$

(1.4-12)

Here, R represents the measured range to the target, c is the speed of light, f_s is the sampling frequency, N_T is the number of samples denoting the time delay, and N_B refers to the number of samples indicating the total sweep time. Crucially, this equation hinges on a sweep bandwidth (Δf) precisely half of the sampling frequency. This meticulous compliance ensures that the highest frequency component of the FMCW signal remains within the bounds for accurate sampling, safeguarding the precision of range measurements and enhancing target detection within FMCW radar systems.

By upholding this relationship between sweep bandwidth and sampling frequency, FMCW radar systems stand poised to deliver unwaveringly accurate distance measurements, bolstering applications spanning autonomous vehicles, object detection, and remote sensing. Within the domain of FMCW radar systems, the precision of distance measurements and the capacity to distinguish between multiple targets within the radar's field of view pivot on the concept of range resolution. This fundamental concept is concisely captured by the equation:

$$\Delta \mathrm{d} = \frac{c}{2BT}$$

(1.4-13)

Here, Δd refers to range resolution, c is the speed of light, B is the sweep bandwidth, and T is the sweep duration.

Range resolution Δd refers to the smallest distinguishable difference in distance between two targets along the radar's line of sight. Several critical factors contribute to the determination of this resolution, including the sweep bandwidth B and the sweep duration T. Notably, increasing the sweep bandwidth or prolonging the radar sweep duration serves to refine range resolution. This heightened resolution empowers the radar to effectively differentiate between targets positioned very closely in range, an indispensable capability for applications encompassing object detection, tracking, and maintaining situational awareness in environments harboring multiple objects of interest.

The validity of resolution results in an FMCW radar system depends on various critical factors, including high signal-to-noise ratio (SNR), precise range resolution, and meticulous calibration. Additionally, factors such as antenna characteristics, target properties, interference management, environmental conditions, and effective signal processing all contribute to result validity. These considerations collectively ensure that the radar system provides accurate and reliable resolution measurements, meeting the specific requirements of diverse applications.

Reduced Peak Transmit Power Efficiency in CW Radar Systems

Continuous Wave (CW) radars offer a distinct advantage compared to pulsed radars by allowing for the attainment of the same maximum detection range with a reduced peak transmit power. This advantage arises from the way CW radars evenly distribute power across the entire sweep, as opposed to concentrating it in narrow pulses. This approach simplifies the design of the radar transmitter, enhancing its compatibility with solid-state transmitters and alleviating concerns about the linearity of power amplifier stages within the transmitter.

Reduced Clutter Interference

Area clutter, such as ground and sea clutter, typically fills the entire antenna beam, whereas other targets like humans occupy only a fraction of the beam. A finer resolution leads to a proportional decrease in clutter power with the narrowing of the beamwidth. This concept can be leveraged to enhance the signal-to-clutter ratio (SCR), which serves as the ultimate performance metric for ground- and sea-based radars. Millimeter-wave (MMW) radars, owing to their high transmit frequency, particularly benefit from this principle.

Reduced IF/Baseband Bandwidth

FMCW radars exhibit a lower Intermediate Frequency (IF) bandwidth when compared to pulsed radar systems. This distinction can be understood by considering that in pulsed radars, range resolution is determined by the pulse width, which remains relatively constant whether at Radio Frequency (RF) or baseband. Conversely, in FMCW radars, range resolution hinges on the swept bandwidth, while range itself is determined by the frequency difference between the transmitted and received signals. Depending on the transmitted power and the desired maximum range, it is possible to apply low pass filtering to the IF signal to restrict its bandwidth.

Smaller Component Dimensions

Incorporating insights from both Microwave Engineering and Optics, MMW (Millimeter-Wave) circuits and components operate in the frequency range that falls between the microwave and far-infrared bands. In Microwave Engineering, it is well-established that the physical dimensions of circuits scale down relative to the wavelength of electromagnetic signals. Notably, MMW signals boast frequencies approximately ten times higher than microwave signals, resulting in MMW circuits being roughly ten times smaller than their microwave counterparts.

Range Harmonics Under Saturation

In FMCW radar systems, the possibility of mixer diodes or the IF/baseband chain saturating due to a substantial return power from a target leads to the production of harmonics of the beat frequency. This effect is unique to FMCW radar systems, lacking

an equivalent counterpart in pulsed radars. Consequently, it can result in false target indications. While an equivalent pulsed radar can also experience saturation from the same target, baseband pulse saturation does not induce harmonics.

Transmit/Receive Isolation

In continuous wave (CW) and FMCW radar systems, the transmitter remains active continuously, necessitating special measures to minimize leakage power coupling, especially when the transmitter and receiver are co-located, as in monostatic radars. Leakage power can propagate through various paths, including direct transmission from the transmit antenna to the receive antenna and reflections from metal structures. To maintain performance, it is crucial to ensure that the total leakage power remains below the thermal noise figure of the radar, which should ideally be low.

Pulsed Radar Blind Spots

In contrast, pulsed radar systems turn off the transmitter once the pulse is transmitted. Consequently, there is no leakage power to contend with. However, pulsed radar systems generate much higher peak power in their transmitted pulses compared to FMCW systems. As a result, the receiver must be temporarily deactivated during transmission, creating a mandatory blind spot around the radar. In well-calibrated FMCW systems, such a blind spot is typically not present, offering a significant advantage over pulsed radars.

1.5 Conclusion

In the context of designing ultra-low phase noise oscillators, Chapter 1 introduces the critical role of precise frequency synthesis in automotive radar applications. The emphasis on phase-locked loops (PLLs) as synthesizers is particularly relevant, given their capability to mitigate low-frequency phase noise.

The exploration of oscillator phase noise's impact on radar performance helps in addressing these challenges in the subsequent chapters. The chapter acts as an introduction, guiding the reader through radar principles, classification, and the unique features of Frequency Modulated Continuous Wave (FMCW) radar systems.

By establishing the importance of range resolution and providing insights into the benefits of FMCW radars, the chapter bridges the gap between radar fundamentals and the overarching theme of designing ultra-low phase noise oscillators. It sets a foundation for the analysis and exploration that will follow in the subsequent sections of the thesis.

Chapter 2

2.1 Introduction

In this chapter, we explore how to connect Frequency-Modulated Continuous Wave (FMCW) radars with frequency synthesizers, highlighting the crucial role of phase noise in achieving optimal radar performance. The accuracy of FMCW radar systems relies on carefully managing microwave frequency signals, especially paying attention to phase noise in oscillators. Before we proceed, we make sure to understand key radar system requirements, such as operating frequency, bandwidth, and modulation scheme. We then discuss how to wisely choose frequency synthesizers, considering aspects like frequency range, precision, stability, and modulation capabilities.

To handle phase noise in radar systems, we adopt a two-pronged approach involving low-noise oscillators and external Phase-Locked Loops (PLLs). We take a closer look at the Analog Phase-Locked Loop (PLL) Type II, explaining its intricate control system designed for precise frequency and phase control. The chapter concludes by introducing Digital Phase-Locked Loops (DPLLs) and highlighting their components. We explore the design and implementation of a Digital Controlled Oscillator (DCO) within a Digital PLL framework. This digital approach enhances flexibility and allows seamless integration with modern signal processing and communication technologies. The main aim of Chapter 2 is to provide a solid foundation for understanding the basic concepts for frequency synthesizers, with a specific focus on effective phase noise management.

2.2 Radar Requirements

The accuracy of a Frequency-Modulated Continuous Wave (FMCW) radar system relies heavily on the precise generation and control of microwave frequency signals. One key factor that significantly impacts radar performance is the phase noise present in oscillators. Given their essential role in FMCW radar systems, frequency synthesizers require careful attention to phase noise to guarantee optimal radar functionality. This chapter delves into the detailed process of connecting FMCW radars

with frequency synthesizers, placing special emphasis on the critical role played by phase noise.

The precision and accuracy of a Frequency-Modulated Continuous Wave (FMCW) radar system hinge on the precise generation and control of microwave frequency signals. Among the critical factors influencing radar performance, phase noise in oscillators takes center stage. Frequency synthesizers, as fundamental components of FMCW radar systems, necessitate thorough consideration of phase noise to ensure optimal radar functionality. This chapter delves into the intricate process of connecting FMCW radars and frequency synthesizers, with a particular emphasis on the pivotal role of phase noise.

Before delving into the intricate details of connecting radars and frequency synthesizers, it is crucial to establish a comprehensive understanding of the fundamental requirements of the radar system. These requirements encompass three key dimensions. Firstly, the radar's operating frequency, typically situated within the microwave spectrum, is foundational, determining the radar's effectiveness in transmitting and receiving signals [2]. Secondly, defining the necessary bandwidth tailored to the specific radar application is a critical parameter influencing signal processing and data acquisition strategies, necessitating careful analysis [3]. Thirdly, a profound understanding of the chosen Frequency-Modulated Continuous Wave (FMCW) modulation scheme, including its intricate frequency sweep characteristics, is of pivotal importance. This forms the basis for unlocking the radar's full range of capabilities [4]. Together, these requisites provide a solid foundation for comprehending radar systems and their seamless integration with frequency synthesizers, establishing an essential framework for the successful execution of radar operations.

2.3 Optimal Frequency Synthesizer Choice in Radar Systems

The cautious selection of an appropriate frequency synthesizer is of paramount importance in aligning the radar system with its stringent operational requirements. This detailed process entails a comprehensive evaluation of several critical factors. First and foremost, the frequency range is a foundational consideration, requiring the synthesizer to comprehensively span the desired frequency spectrum. This encompasses not only the radar's prescribed operating frequency, which is non-negotiable, but also

any essential modulation bandwidth requirements calculated to accommodate the radar's exacting precision objectives. Precision and stability stand as fundamental pillars in the selection process, underscoring the imperative to opt for synthesizers recognized for their exceptional precision and stability. It is essential to acknowledge that even minor deviations in phase noise can pose significant challenges to radar performance [5]. Finally, the synthesizer's modulation capabilities become the focus of attention, demanding not only the adept execution of the complex FMCW modulation scheme but also a commitment to mitigating phase noise. This dual objective is paramount to safeguarding the radar's precision-critical measurements and overall functionality.

2.4 Phase Noise Management in Radar Systems

In the domain of automotive radar applications, the significance of addressing phase noise emerges as a paramount concern owing to its multifaceted implications on system performance and safety. Phase noise, an inherent characteristic stemming from electronic instabilities within Phase-Locked Loop (PLL) circuits, imposes substantial challenges on radar functionality, particularly in terms of range, Doppler, and angular resolution. Notably, the presence of phase noise can lead to a reduction in range resolution, blurring the distinction between closely spaced objects and impeding the accurate identification of vehicles, pedestrians, or obstacles. Furthermore, the degradation of Doppler resolution exacerbates the difficulty in precisely detecting and tracking the velocities of moving objects, crucial for discerning various types of motion encountered on roadways. Moreover, in the realm of angular resolution, phase noise-induced distortions in phase information introduce errors in angle estimation, compromising the system's ability to determine azimuth and elevation angles of detected objects with requisite accuracy. This confluence of factors underscores the critical role of mitigating phase noise in automotive radar systems, given the stringent imperatives for precision, reliability, and safety inherent to vehicular environments. In light of the dynamic and unpredictable nature of automotive settings, where the repercussions of errors can be profound, concerted efforts aimed at minimizing phase noise are indispensable for safeguarding optimal performance and ensuring the well-being of vehicle occupants and other road users.

Frequency synthesizers are often implemented as phase-locked loops (PLLs) due to their effective management of phase noise performance. Phase-Locked Loops (PLLs),

crucial in numerous communication and signal processing applications, exist in two primary forms: Analog PLLs and Digital PLLs.

The Analog Phase-Locked Loop (PLL) Type II functions as a sophisticated control system designed for precise frequency and phase control. At its essence, the phase detector, often realized as a charge pump, intricately compares the phase difference between the reference input signal and the feedback signal from the Voltage-Controlled Oscillator (VCO). This pivotal charge pump component translates the phase error into a current, dynamically adjusting the control voltage applied to the VCO. Following the charge pump, the importance of the loop filter becomes apparent. Serving as a critical intermediary, the loop filter actively filters out high-frequency noise. Its nuanced parameters, including bandwidth and damping characteristics, exert substantial influence over the overall performance of the PLL.

The Voltage-Controlled Oscillator (VCO) assumes a central role by generating the output signal, its frequency intricately controlled by the feedback from the loop. This closed-loop system relies on the VCO's frequency, directly proportional to the control voltage. In certain configurations, a Frequency Divider (Divider) is introduced to selectively divide the VCO output frequency. This strategic division yields a lower-frequency feedback signal, instrumental for precise comparison with the reference signal in the phase detector.

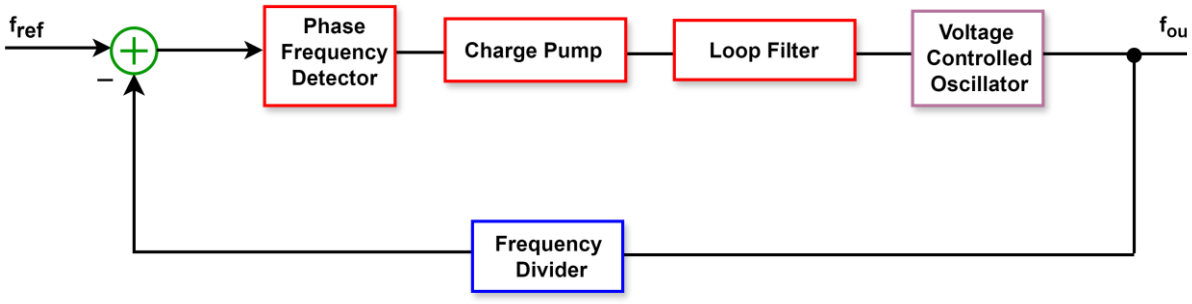


Figure 2.1 Block Diagram of an analog type II PLL

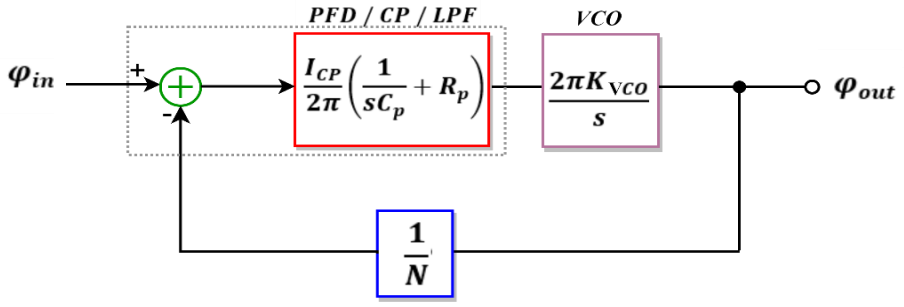


Figure 2.2 Linearized Model of an analog type II PLL

Ultimately, the output of the PLL is derived either directly from the VCO or, alternatively, from a divided version of the VCO frequency. Noteworthy for its employment of a charge pump, the Analog Type II PLL stands out for its enhanced noise performance compared to its Type I counterparts. The control of the loop's bandwidth and damping ratio through the loop filter permits tailored dynamic behavior, making it a versatile choice for applications where precision and noise performance are paramount. The specific values and configurations of these components are meticulously determined based on the nuanced requirements of the desired application and performance objectives. Fig. 2.1 illustrates the APLL, and in the subsequent analysis, a well-established linearized model is employed to enhance our understanding of its dynamic characteristics.

In Fig.2.2, a linearized model of the PLL can be derived, depicting the contribution to G_{LOOP} function from every part of the PLL system architecture. The equations expressing the characteristics of the PLL are as follows:

$$G_{LOOP}(s) = \frac{I_{CP}}{2\pi}\left(\frac{1}{sC_p}+R_p\right)\frac{2\pi K_{VCO}}{s}\frac{1}{N} \tag{2.4-1}$$

$$\frac{\varphi_{out}(s)}{\varphi_{in}(s)} = \frac{\frac{I_{CP}}{2\pi}\left(\frac{1+sC_pR_p}{sC_p}\right)\frac{2\pi K_{VCO}}{s}}{1+G_{LOOP}(s)} = N\frac{2\zeta\omega_n s+{\omega_n}^2}{s^2+2\zeta\omega_n s+{\omega_n}^2}$$

(2.4-2)

$$\text{Where } \omega_n = \sqrt{\frac{I_{CP}K_{VCO}}{C_p\,N}}$$

(2.4-3)

and

$$\zeta = \frac{R_p}{2}\sqrt{\frac{I_{CP}K_{VCO}C_p}{N}}$$

(2.4-4)

The closed-loop transfer function presented in equation 2.4-2 is characterized by one zero and two poles, showcasing a discernible low-pass response. This implies that gradual input phase fluctuations are transmitted to the output, while rapid phase changes are effectively filtered out. Additionally, as expressed in equation 2.4-4, it is evident that the damping ratio (ζ) increases proportionally with the parameter C_p. Equations 2.4-3 and 2.4-4 exhibit a notable feature wherein the terms I_{CP} and K_{VCO} are coupled solely as a product. This observation suggests that if these parameters undergo changes in opposite directions, the system response remains invariant.

Digital Phase-Locked Loops (DPLLs) represent a crucial class of digital control systems employed for achieving synchronization between a reference signal and a digital output signal. This section provides an in-depth exploration of the primary components constituting a DPLL, explaining their functions and interactions within the digital domain. The Digital Phase-Locked Loop (DPLL) featuring a Time-to-Digital Converter (TDC), Digital Loop Filter, Digital Controlled Oscillator (DCO), and Divider represents a sophisticated architecture tailored for precise frequency and phase synchronization in digital systems [6].

At the core of the system is the Time-to-Digital Converter (TDC), a crucial component for measuring time intervals. The TDC quantizes the phase difference between the reference and feedback signals, providing a digital representation of the phase error. Processing the digital output from the TDC, the Digital Loop Filter operates in discrete time. It refines the error signal, shaping the loop dynamics, and eliminating undesirable frequency components. The digital nature of the loop filter enables precise control over the system's response.

The Digital Controlled Oscillator (DCO) takes the refined signal from the loop filter to generate the controlled output signal. Unlike traditional analog Voltage-Controlled Oscillators (VCOs), the DCO operates in the digital domain, offering precise frequency tuning and rapid adaptability to varying conditions. For applications requiring frequency scaling, a divider may be integrated into the system. This component scales down the frequency of the output signal, and the divided signal is fed back into the loop for continuous phase comparison. This DPLL architecture incorporates a feedback network to ensure the constant iteration of the phase comparison process. The output signal, controlled by the DCO and potentially the divider, continuously returns to the TDC and Digital Loop Filter, maintaining synchronization.

In summary, the integration of a TDC, Digital Loop Filter, DCO, and Divider in a Digital PLL presents a comprehensive approach to precision frequency and phase control in digital systems. This configuration, characterized by its digital-centric components, holds relevance in applications demanding high adaptability, programmability, and accuracy and is depicted in Fig 2.3.

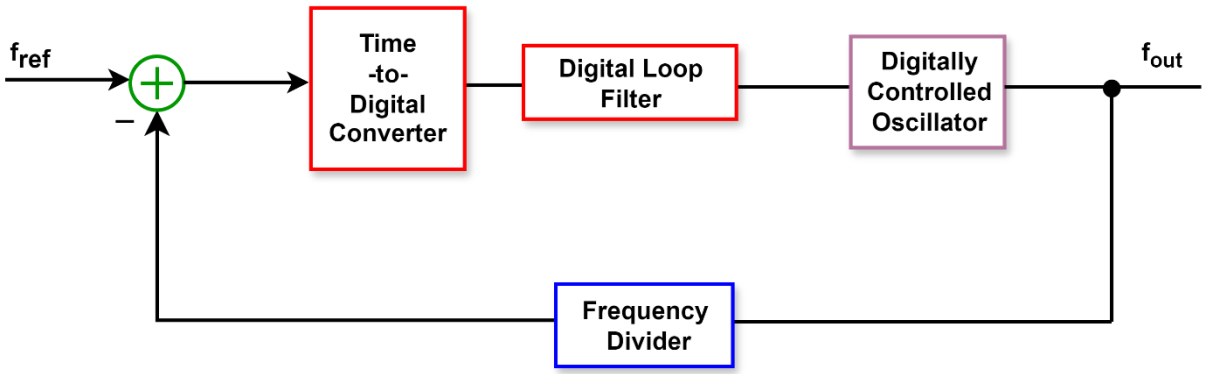


Figure 2.3 Block Diagram of a Digital PLL.

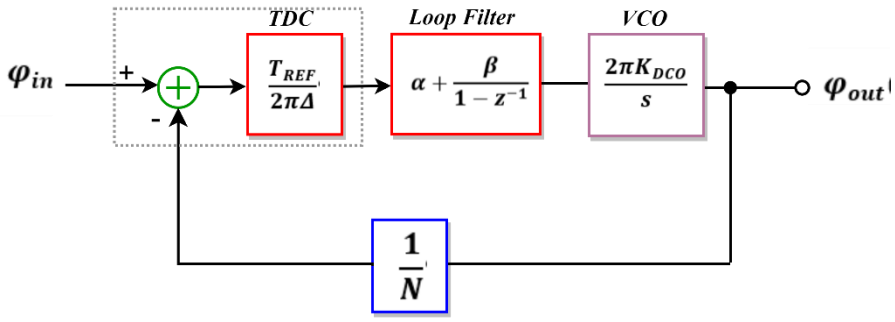


Figure 2.4 Linearized Model of a Digital PLL.

In a Digital PLL (DPLL), the construction of the transfer function must be properly stated. An extensive and complex link between the analog and digital PLLs is established. We will compare the forward transfer functions of the analog and digital PLL loops, and subsequently determine the closed-loop parameters for the digital PLL [6].

$$\frac{I_{CP}}{2\pi}\left(\frac{1}{sC_p}+R_p\right)\frac{2\pi K_{VCO}}{s}=\frac{T_{REF}}{2\pi\Delta}\left(\frac{\beta}{sT_{REF}}+\alpha\right)\frac{2\pi K_{DCO}}{s} \tag{2.4-5}$$

The parameters α and β in the digital loop are to be calculated, forming a crucial part of the loop design process in Fig 2.4. These digital parameters are intricately linked to their analog counterparts and will be determined based on established relationships derived from analog loop parameters. The calculated values of α and β will play a pivotal role in shaping the behavior and performance of the digital filter, ensuring a tailored and effective design in alignment with the characteristics of the analog loop. The intermediary calculations and observations fall beyond the scope of this study and are omitted.

$$a = I_{CP}R_P\frac{\Delta}{T_{REF}}\frac{K_{VCO}}{K_{DCO}} \tag{2.4-6}$$

$$\beta = \frac{I_{CP}\Delta}{C_P}\frac{K_{VCO}}{K_{DCO}}$$

(2.4-7)

Furthermore, closed loop parameters can be calculated as:

$$\omega_n = \sqrt{\frac{\beta K_{DCO}}{2\pi\Delta N}}$$

(2.4-8)

$$\zeta = \frac{\alpha T_{REF}}{2\pi}\sqrt{\frac{K_{DCO}}{2\pi\beta\Delta N}}$$

(2.4-9)

Fig. 2.5 provides a visual representation that clarifies the impact of the loop on Digital Controlled Oscillator (DCO) noise. It is evident that beyond the limits set by the loop bandwidth, precisely determined by the features of the digital loop filter, the intrinsic noise profile of the DCO remains unchanged. This observation suggests that the loop predominantly governs and alleviates the DCO noise within its designated bandwidth, emphasizing the crucial role of the loop filter in shaping the system's noise characteristics [56].

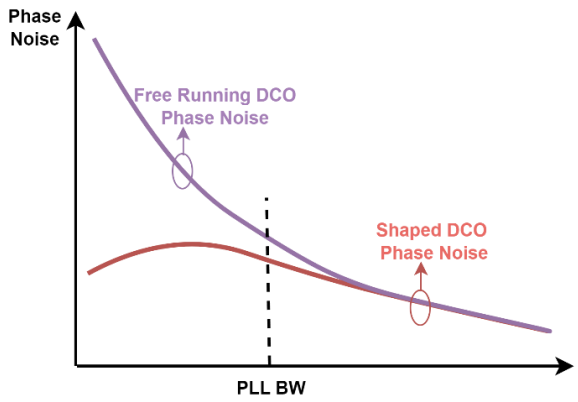


Fig 2.5 Shaped VCO phase noise in a PLL.

This work centers on the design and implementation of a Digital Controlled Oscillator (DCO) within the framework of a Digital PLL. The DCO, a pivotal circuit in the generation of controlled output frequencies, provides programmable precision. This digital-centric approach not only enhances flexibility but also facilitates seamless integration with digital systems, aligning with the evolving demands of modern signal processing and communication technologies.

2.5 Conclusion

The critical factor in the intricate integration of frequency synthesizers and Frequency Modulated Continuous Wave (FMCW) radars lies in the careful management of phase noise. A resilient radar system, capable of precise target identification and tracking across diverse applications, is forged by addressing these challenges through deliberate oscillator selection and design, all while strictly adhering to radar system specifications.

Chapter 3

3.1 Introduction

The central challenge in FMCW radar systems is the need to achieve highly precise and controlled frequency sweeps to accurately measure the characteristics of targets. Phase noise poses a significant threat to this precision by introducing unwanted variations in the radar signal, potentially leading to errors in range, velocity, and direction measurements. Thus, the mitigation of phase noise assumes critical importance for the effective functioning of FMCW radar systems. The choice between LC oscillators and ring oscillators is influenced by various factors. While ring oscillators offer compactness and power efficiency, it is worth noting that LC oscillators are often preferred due to their ability to provide highly stable, low-phase noise signals, which are crucial for precise range and velocity measurements. [8-9].

The fundamental question we must address is whether it is more advantageous to implement a single oscillator operating at a lower frequency or to adopt a frequency multiplication approach, which involves a single oscillator operating at a lower frequency and then subsequently multiplying its output to attain the desired local oscillator (LO) frequency as seen in Fig. 3.1. This inquiry is rooted in the precise study of phase noise, power consumption, and practical considerations, particularly in the realm of millimeter-wave (mm-wave) and high-frequency applications, where precision and efficiency are paramount. Our pursuit of understanding involves the rigorous examination of the inherent trade-offs and performance implications associated with these two approaches.

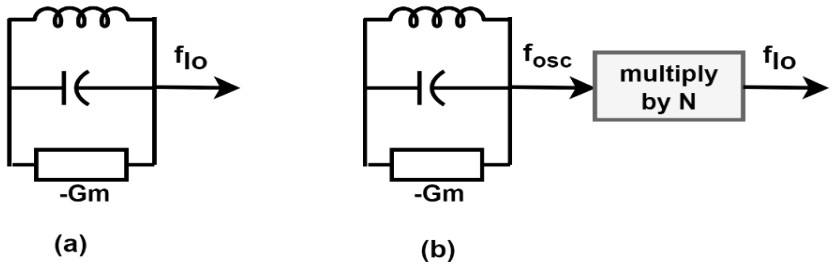


Figure 3.1 Synthesis of frequency f_{LO} by using (a) fundamental LC oscillator (b) multiple core oscillator.

Despite the technology favoring a frequency below 10GHz, regulatory constraints for the next generation of automotive radar mandate a band allocation between 76 to 81 GHz. This allocation, divided into 76-77 GHz for long-range radar and 77-81 GHz for short and medium range, poses challenges for designing an oscillator operating below, necessitating frequency multiplication by a factor of at least 8 times. However, the design difficulties, high power dissipation and the area occupation make the implementation complex.

Considering these challenges and to strike a balance between design complexity and phase noise performance, a center frequency of 20 GHz has been chosen for the DCO. This decision reduces the required frequency multiplication to a factor of 4, offering a compromise that addresses concerns related to design intricacies, power consumption, and potential interference with nearby circuits. This choice reflects a pragmatic approach to achieving balance between oscillator performance and practical implementation considerations.

In this chapter, the design of a quad core class-B oscillator will be presented giving emphasis to the design challenges occurred and the novelty regarding the coarse bank array implementation, quad core layout and minimization of the undesired effects of the state-of-the-art implementations that now are resolved by this new topology. Before explaining the quad-core design, a thorough analysis of a single-core oscillator is conducted. This foundational step allows for a detailed examination of core components and their interactions. The insights gained from this analysis serve as a basis for refining and optimizing the quad-core design.

3.2 Noise in Oscillators

In the context of mmWave frequencies, Digitally Controlled Oscillators (DCOs) operating beyond 20 GHz encounter significant degradation in phase noise, primarily attributed to suboptimal integrated capacitor quality factors in the mmWave spectrum [10]. While the inductive quality factor improves with frequency, it saturates around 20-30 GHz, as illustrated in Fig 3.2. Simulations verify this phenomenon, revealing an abrupt reduction in the oscillator's Figure of Merit (FoM) beyond a specific threshold, particularly noticeable when utilizing a single-turn inductor due to detrimental trace coupling, as shown in Fig. 3.3.

Moreover, Fig. 3.2 indicates that the capacitive quality factor diminishes with rising frequency, becoming the primary source of losses at mmWave frequencies. Consequently, the overall quality factor of the LC Tank exhibits a noticeable decline above 20 GHz, leading to degraded phase noise performance. For mmWave frequency synthesizers, a practical solution involves employing a 20 GHz oscillator followed by a multiplier. Coupling multiple identical oscillators has been shown as a viable strategy for achieving low phase noise (PN) with high FoM in CMOS [11], [12]. Ideally, the total PN for N coupled oscillators is 10*log10(N) times lower than for a single core, leaving the FoM unchanged [13].

The careful design of the coupling network is crucial to avoid performance degradation and significantly diminish sensitivity to parasitic elements, thereby broadening the DCO's tuning range. Furthermore, this design allows the avoidance of one or more power-intensive pre-scaler stages within the Phase-Locked Loop (PLL) chain, compensating for the additional power consumption imposed by the frequency multiplier. Additionally, deploying a subharmonic oscillator has the advantageous effect of reducing the multiplication factor required by the PLL, resulting in less amplification of in-band noise, and further enhancing the overall system performance.

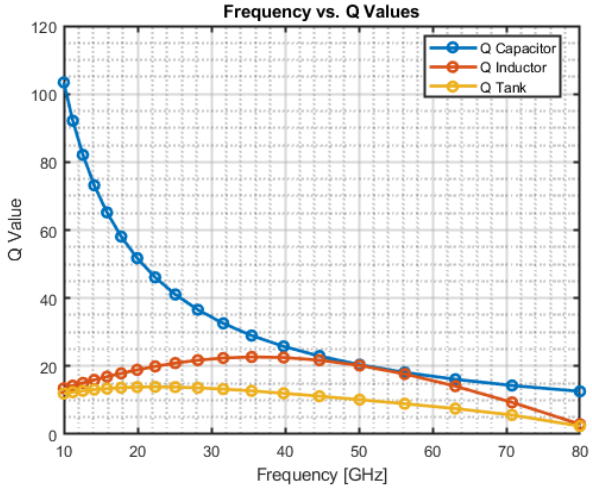


Figure 3.2. Simulated Quality Factor Analysis of Integrated Inductors, Switched Capacitor Elements, and Equivalent Tank in 28nm CMOS Technology.

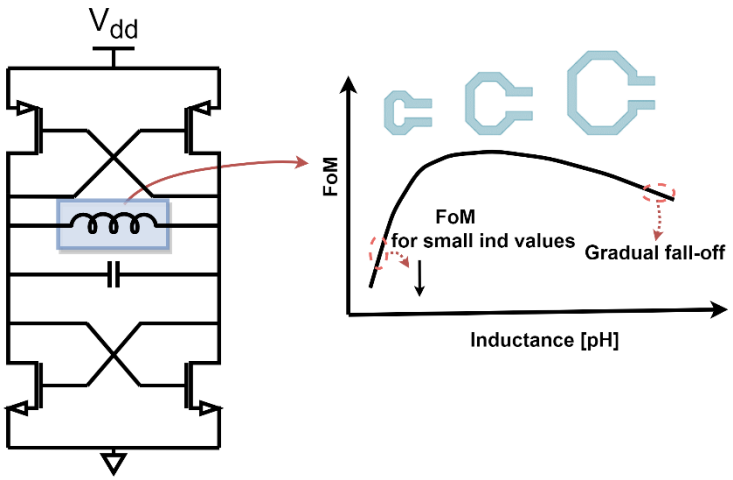


Figure 3.3. FoM drop-off of the Integrated Inductor.

As is widely known, the PN at a frequency offset Δω may be stated using Leeson's equation as follows:

$$\mathcal{L}(\Delta\omega) = 10 \cdot log_{10}\left[\frac{k_B T F}{2P_{rf}}\left(\frac{\omega_o}{Q_T \Delta\omega}\right)^2\right]. \tag{3.2-1}$$

where k_B is the Boltzmann's constant, T is the absolute temperature, F is the noise factor, that accounts for the noise contributions from active devices and bias circuitry, and P_{rf} is the resonator dissipated power. In single-tank oscillator, P_{rf} can be written as $\frac{1}{2}\frac{A_0^2 Q_T}{\omega_o L}$, where A_o is the amplitude of oscillation, L is the tank inductance and Q_T is the tank quality factor. For a given A_o, phase noise improves by reducing the inductance and maximizing Q_T. While Leeson's initial analysis provided a simplified derivation, equation 3.2-1 has subsequently been formally validated. It has been observed that when the noise of the biased circuit is ignored and the appropriate assumption is made, the parameter F depends only on the noise coefficient of the active components and nothing else associated with the topology chosen of the oscillator. In contrast, the conversion of flicker noise measured by the parameter K to noise level is affected by second order effects, which depends on the selected topology [16].

The evaluation of an oscillator's performance typically involves the use of a Figure of Merit (FoM) that standardizes phase noise concerning both frequency and power consumption, denoted as P_{DC}.[17]

$$FoM = \mathcal{L}(\Delta f) - 10log_{10}\left[\frac{1}{P_{DC}}\left(\frac{f_{osc}}{\Delta f}\right)^2\right] = -174\frac{dBc}{Hz} - 10log_{10}\left(\frac{2{Q_T}^2\eta_P}{F}\right)$$

(3.2-2)

Where P_{DC} represents the LO power consumption normalized to 1mW, and η_P stands for the efficiency of the DC to RF power conversion. In the case of a well-designed oscillator, power efficiency remains uncorrelated with the oscillator frequency.

In the context of Controlled Oscillator, the tuning range (TR) emerges as a fundamental parameter. Notably, recent advancements in this field have given rise to a refined metric that concurrently considers power consumption, tuning range, and noise characteristics. Given the often-observed correlation between tuning range and tank quality factor in VCOs, this equation emerges as a more equitable metric for the comparative assessment of VCO performance. This metric provides a more comprehensive and rigorous framework for the evaluation of VCO design [18]:

$$FoM_T = FoM - 20log_{10}\left[\frac{TR}{10}\right]$$

(3.2-3)

3.3 Impulse Sensitivity Function based Phase Noise Analysis for Single and Multiple Core Implementation

Before starting to describe the implementations examined it is important to understand the comparison in terms of noise for single and multiple core implementation. The primary aim of this study is to empirically demonstrate that our proposed harmonic coupling technique can achieve a significant reduction in phase noise, quantified as a $10logN$ improvement when compared to a single core, all the while maintaining an equivalent high Figure of Merit (FoM). Importantly, this technique is employed with the explicit goal of sidestepping the degradation

mechanisms that are commonly associated with other coupling methods [19] and [11]. The results of this research underscore the effectiveness and practical significance of our harmonic coupling technique for improving the performance of the studied system.

To justify this principle, our initial step involves a thorough examination of the Impulse Sensitivity Function (ISF) pertaining to the thermal noise sources within a standalone oscillator. Subsequently, we shall juxtapose these findings with the scenario involving four interconnected oscillators. The ISF serves as an invaluable analytical instrument for the assessment of phase noise in oscillators, as it facilitates the quantification of the oscillator's susceptibility to diverse noise sources. From the ISF, it is possible to formulate a formal expression for the phase noise in a single oscillator operating within the thermal noise region as follows:

$$L_{single}\{\Delta\omega\} = 10\ log\ \left[\frac{kT}{P_{sig}}\left(\Gamma_{Tank,rms}^2 + (G_{Tailtank}/G_{tank})\Gamma_{TailTank,rms}^2 + \alpha\Gamma_{MOS,rms}^2\right)\left(\frac{\omega_0}{Q\Delta\omega}\right)^2\right] \tag{3.3-1}$$

where $\Gamma_{Tank,rms}$, $\Gamma_{TailTank,rms}$ and $\Gamma_{MOS,rms}$ are the RMS values of the ISF of the main tank, tail tanks and cross-coupled MOS devices respectively and P_{sig} is the dissipated power of the resonator. The $G_{Tailtank}/G_{tank}$ is the ratio of the conductance related to the tail tank and main tank. The Impulse Sensitivity Function (ISF) analysis was conducted for the main tank, tail tank, and MOS cross-coupled transistors, denoted as (Γ_{Tank}, $\Gamma_{TailTank}$ and Γ_{MOS}), utilizing a simulation methodology as outlined in the reference [20]. This method entailed the execution of periodic transfer function simulations. The comparison of ISF plots for a single oscillator and a quad-core oscillator, wherein the latter exhibited four times the ISF, serves as a visual representation of the substantial performance enhancement achieved through oscillator coupling. The study findings posit that the coupling of identical oscillators offers a straightforward and effective means of improving the phase noise characteristics of CMOS oscillators while maintaining critical parameters such as power consumption and frequency range. The results obtained from this investigation are meticulously

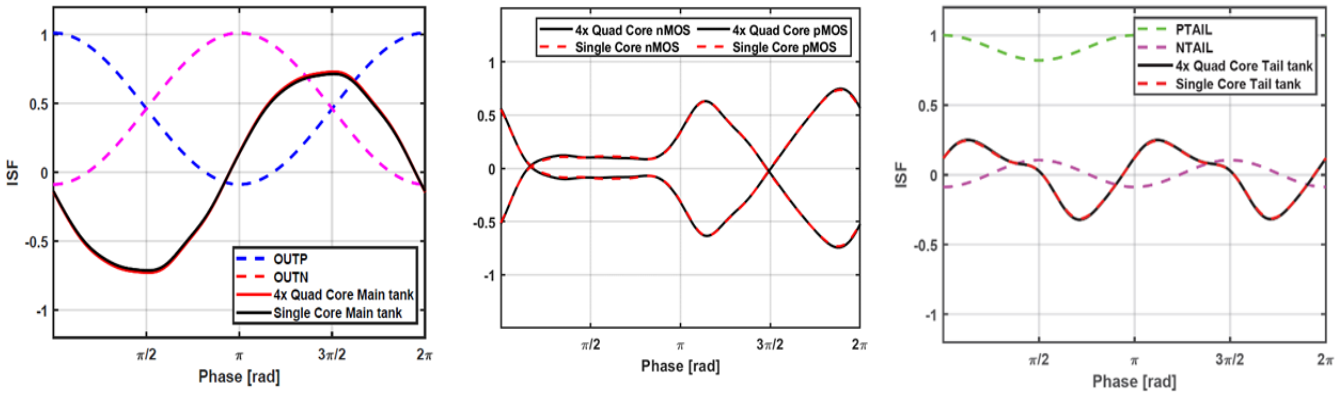


Figure 3.4 Simulated ISFs of (a) active devices, (b) Main tank, and (c) Tail tanks for single and quad core implementation.

detailed in Fig. 3.4. In the context of oscillator coupling, the determination of overall phase noise for a configuration involving N = 4 cores is performed using:

$$L_N\{\Delta\omega\} = 10\,log\left[\frac{NkT}{P_{sig}}\left(\Gamma^2_{Tank,rms} + (G_{TailTank}/G_{tank})\Gamma^2_{TailTank,rms} + \alpha\Gamma^2_{MOS,rms}\right)\left(\frac{\omega_0}{Q\Delta\omega}\right)^2\right] \tag{3.3-2}$$

With the introduction of the proposed coupling technique, it is observed that the total Integrated Phase Noise (ISF) of the system is improved by a factor of four in comparison to the ISF of a solitary core oscillator, with marginal discrepancies. This reduction is achieved without introducing supplementary circuit elements into the system, preserving the absence of additional noise sources, and ensuring no degradation in the quality factor and tuning of the resonator. Consequently, it can be conclusively affirmed that, in accordance with the intended goal, the phase noise of the oscillator comprising four cores is enhanced by 10 * log (4) = 6 dB, as contrasted with that of a solitary core oscillator. In a more general context, employing the proposed technique, one can couple N cores, resulting in a collective phase noise, which can be expressed formally as follows:

$$L_{N-Array}\{\Delta\omega\} = L_{single}\{\Delta\omega\} - 10logN \tag{3.3-3}$$

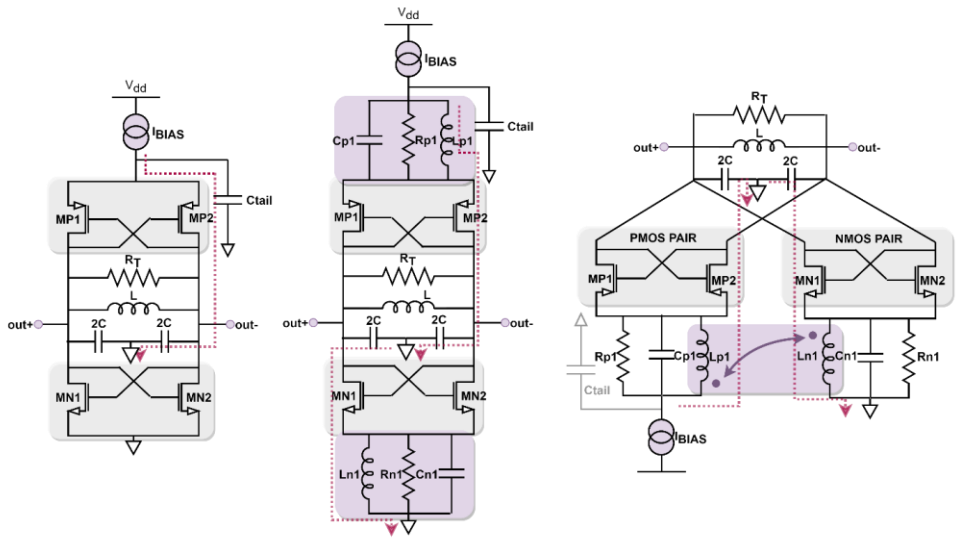


Figure 3.5. Class-B DCO core schematic. (a) without tail tanks (b) with tail tanks (c) with tail tanks and transformer coupling.

This formula provides an estimate of the improvement in phase noise when N cores are coupled together using this technique.

3.4 Single Core Design

This chapter presents the comprehensive schematic of the 20GHz single-core DCO as illustrated in Figure 3.5. Voltage-biased topologies [21-23] are instrumental in eliminating a source of phase noise, such as the current generator, and enhancing power efficiency. However, they also introduce challenges, notably an increased frequency of pushing. A large voltage swing, relative to the supply voltage, is desirable to achieve high power efficiency and reduce phase sensitivity to device noise [26]. Yet, the trade-off emerges as active devices, driven by large signals, may enter the triode region, potentially degrading phase noise. This dilemma can be mitigated by adopting a low supply voltage, preventing active devices from entering triode even as the signal swing approaches or exceeds the supply rails. Alternative solutions include class-D oscillators [24], where transistors operate in deep triode for good phase noise owing to low R_{ON} and rapid switching, and clip-and-restore [23], compensating for loading effects through step-up transformers to boost gate voltage and reduce phase sensitivity to

device noise. The design of high-quality factor components for the main tank poses significant challenges.

Considering these aspects, the chosen topology for each individual core of the oscillator is a complementary push-pull structure featuring magnetic coupling between the PN. For a single core oscillator, the decision to employ a Class B complementary structure, as opposed to an NMOS-only design, stems from a thoughtful consideration of various factors. While an NMOS-only configuration can yield enhanced phase noise performance due to a larger achievable swing, approaching twice the value of voltage supply at maximum power efficiency, the adoption of a complementary structure is motivated by the imperative to pass long-term reliability checks [25]. The introduction of magnetic coupling at the tails introduces a significant advantage: the capacity for source nodes to swing below ground for an overall enhancement in noise performance. This addition results in improved voltage efficiency and higher impedance in series with the tail inductors, ultimately leading to an enhancement in noise performance.

The oscillator's topology plays a crucial role in transforming circuit noise sources into phase noise by influencing the impulse sensitivity function (ISF) [11]. The introduction of a magnetically coupled tail filter has notable effects, and the use of two resonators is necessitated by the absence of a perfectly differential LC main tank. For a more direct and intuitive comparison, Fig. 3.6 serves as a valuable reference in such a scenario, the noise from active devices may find a low-impedance path, significantly impacting phase noise performance by potentially pushing the transistors into the triode region. One might question whether the use of a transformer could alter the Impulse Sensitivity Function (ISF), consequently affecting the conversion of noise to phase noise from the main noise sources. According to the ISF theory, when a noise impulse charge is applied, it exclusively influences the voltage across the capacitor, without any observable effect on the current flowing through the inductor [26]. From the simulation results in Fig.3.6 it is evident that the single core topology advantage with coupling is minor but when it comes to four core implementations as we show before the advantage is not minor anymore.

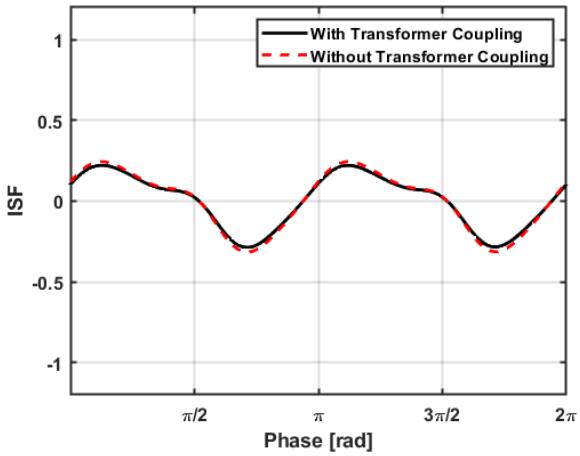


Figure 3.6 Simulated ISF with and without magnetic coupling.

3.5 Multicore DCO Implementation

The challenge of coupling numerous oscillators stems from the complex layout implementation and the consequential power consumption considerations in the final design. Overcoming the performance disparity compared to commercial DCOs, which exploit expensive technologies with higher supply voltages and enhanced quality factors of passive components, requires a substantial reduction exceeding $3dB$ in single-core oscillator phase noise. To attain this goal, the strategy involves the coupling of resonators with a specified number of cores which targets in the phase noise performance improvement. The phase noise improvement as the numbers of cores increases is depicted in Fig. 3.7.

3.6 State of the art Implementations

To achieve higher integration and lower system cost, the implementation of oscillators in advanced CMOS technologies is highly desirable. Coupling multiple identical oscillators has proven to be a viable strategy for achieving low phase noise (PN) with a high Figure of Merit (FoM) [27], [28] in CMOS. Ideally, the total PN for N coupled oscillators is $10{\cdot}\log_{10}(N)$ times lower than for a single core, while leaving the

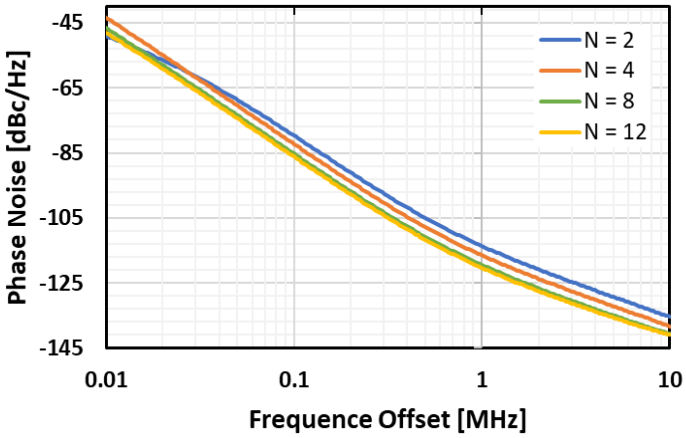


Figure 3.7 Simulated Phase Noise Performance for multiple N cores oscillators.

FoM unchanged [29]. However, the design of the coupling network must be accurate to avoid performance degradation.

Direct coupling of differential LC tanks can introduce additional parasitics, increase losses, and create asymmetries, ultimately degrading PN. Furthermore, in scenarios where multiple inductors are closely packed, undesired magnetic coupling can increase, leading to the emergence of spurious oscillation modes [30]. In resistively coupled multi-core oscillators, a small coupling resistance is required to ensure strong coupling and minimize the PN penalty caused by mismatches between the resonant tanks. However, this can lead to a degradation of the tuning range due to parasitic capacitors. Alternatively, distributed resonators can serve as coupling elements, but this typically results in excessive chip area occupation [31].

3.7 Harmonic Coupled Oscillators: Key Concept

Within the scope of this thesis, we present a novel approach to oscillator design by introducing a four-core digitally controlled oscillator (DCO) that leverages harmonic coupling. To grasp the underlying concept, it is essential to first explore the dual-core analysis technique, as it provides valuable insights crucial for optimizing the design of the quad-core DCO. This investigation into harmonic coupling and dual-core analysis

establishes a foundation for comprehending the intricacies of our proposed four-core DCO, shedding light on its potential enhancements and applications.

In figure 3.8, the concept of two coupled oscillators is visually articulated through the utilization of a noninverting transformer. The resonance between coupled inductors and the parasitic capacitance at common source nodes, particularly centered around the second harmonic, is evident. Under conditions of minor oscillation amplitudes, the coupled tail nodes establish a virtual ground. However, as oscillation amplitudes increase, these nodes exhibit movement, indicating a transition to strong coupling, as elucidated in the plot on the right of Fig. 3.8. This configuration concurrently achieves robust coupling and effective filtering.

The benefits of harmonic coupling become apparent in the improved phase noise observed, with the added advantage of retaining the merits of a single-core topology without introducing extra parasitic elements. Achieving symmetrical coupling necessitates a delicate approach due to inherent disparities between the primary and secondary sides of the transformer. Specifically, coupling the NMOS tail of one oscillator with the PMOS tail inductance of the nearest oscillator is crucial to avoid systematic mismatches that could otherwise lead to phase noise degradation. The simulation results depicted in the figure below reveal a notable correlation: the closer the resonance of the coupled transformers to the second harmonic, the more pronounced the improvement in phase noise performance. In comparison with the initial configurations, this enhancement reaches a substantial 3 dB.

Furthermore, Fig. 3.9 emphasizes the versatility of this technique, demonstrating its applicability with inverting transformers to facilitate quadrature output generation. Even when initially forced by a switch at the schematic level to synchronize and run in phase as the oscillation strengthens, there is a transition to running in quadrature, resulting in an improvement of 10log(N) as anticipated. The adaptability underscores the potential of the proposed approach in diverse oscillator configurations.

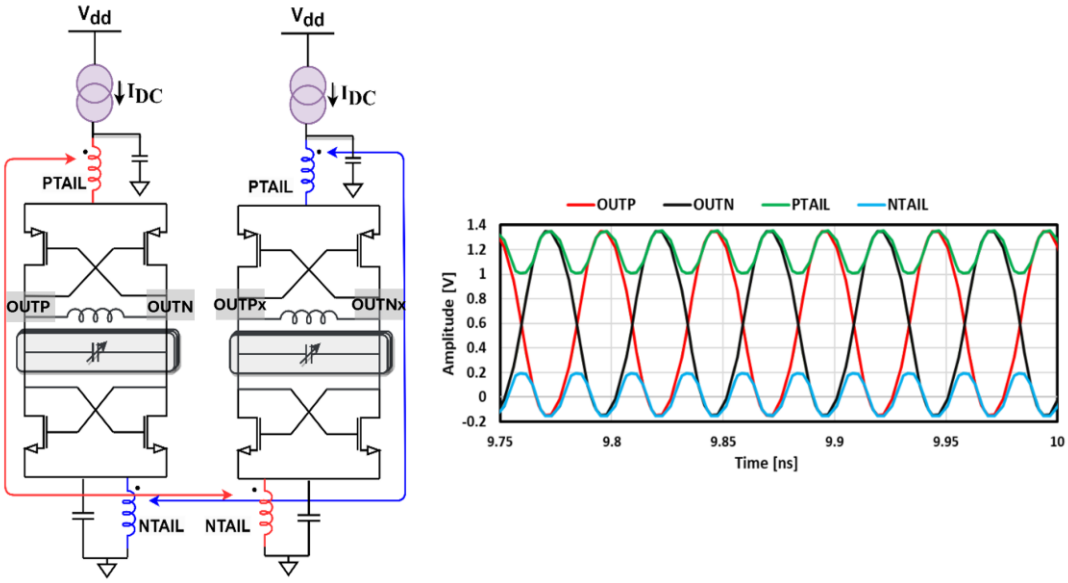


Figure 3.8 In Phase Magnetically Coupled Oscillators and Output Waveforms.

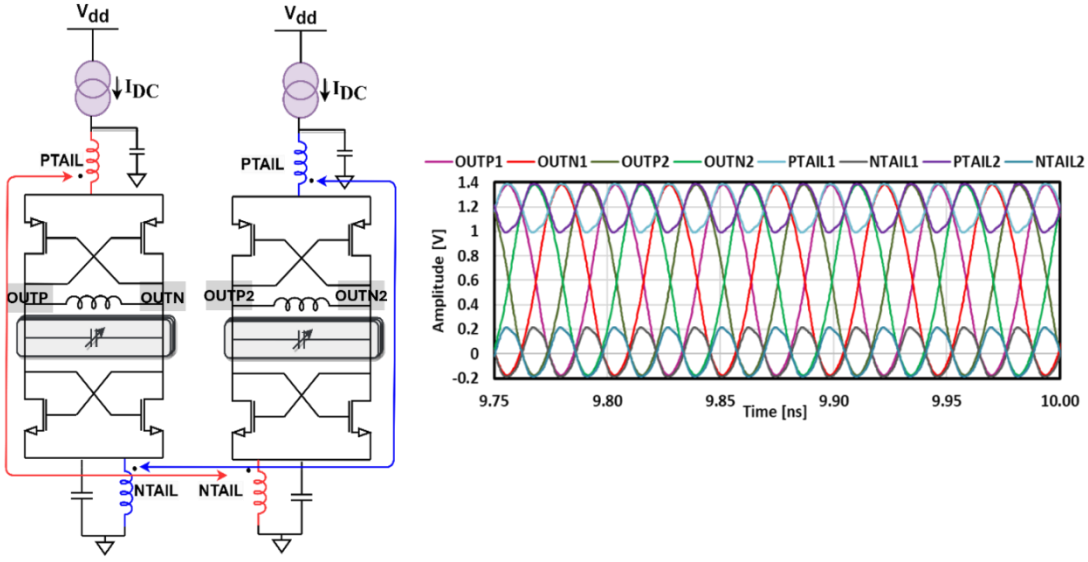


Figure 3.9 Out of Phase Magnetically Coupled Oscillators and Output Waveforms.

An additional significant drawback associated with the NMOS topology is its susceptibility to high flicker noise corner, primarily stemming from the uncontrolled second harmonic current return path of the decoupling capacitors as it is depicted in Fig. 3.10. In conventional NMOS oscillators, the physical separation between the supply and ground introduces parasitic inductance, posing a challenge in terms of control and potentially altering the common mode resonant frequency [35].

However, in magnetically coupled oscillators, the physical connection facilitated by placing the decoupling capacitors in-between the transformers ensure the shortest return path for the common-mode current. This arrangement contributes to the mitigation of parasitic effects, addressing concerns related to flicker noise and enhancing the overall performance and stability of the oscillator system. The figures below depict how the transformer plays a crucial role in creating a concise pathway for closing the loop from the voltage supply to the ground. A comparative analysis with the NMOS topology is presented, offering insights into the distinctive features. Furthermore, a 3D layout representation of the utilized transformers is provided in Fig. 3.11 to enhance visual clarity of Cfilter.

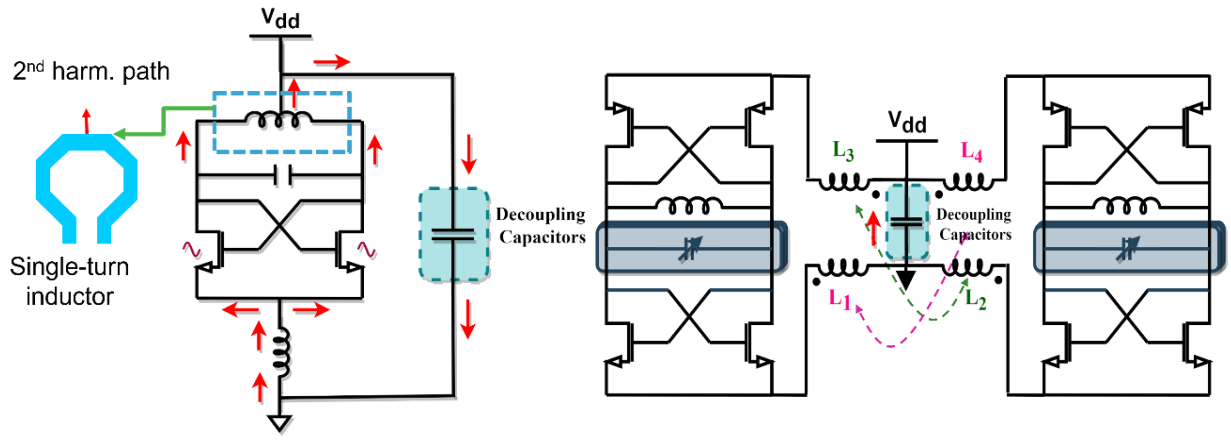


Figure 3.10 Common mode return path issue in NMOS oscillators vs resolved in transformer coupled oscillators.

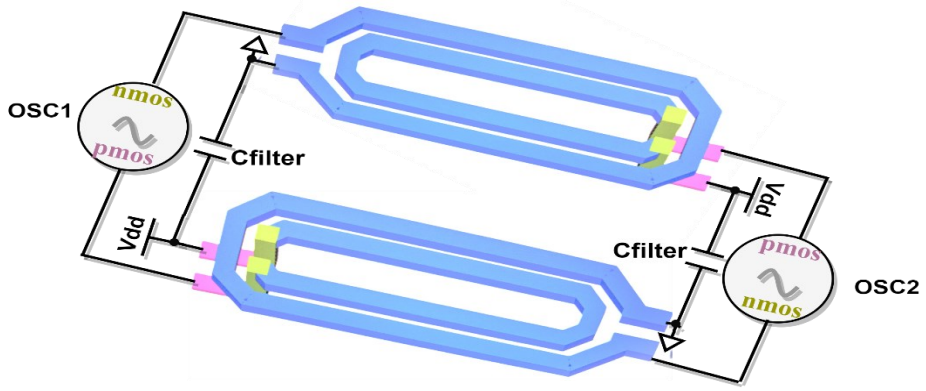


Figure 3.11 Common mode return path issue in transformer coupled oscillators. With 3D Capacitor layout Representation

In magnetically coupled oscillators, the strategic placement of decoupling capacitors between the transformers serves to establish a direct physical connection, ensuring the shortest return path for the common-mode current. This deliberate arrangement plays a crucial role in mitigating parasitic effects, particularly addressing concerns associated with flicker noise. By optimizing the electrical pathways, this approach enhances the overall performance and stability of the oscillator system.

3.8 Quad Core Implementation

In pursuit of advancing oscillator topology, this chapter focuses on a novel N = 4 core configuration, seeking a substantial 6dB decline in phase noise a goal signified by 10log (4). This innovative configuration holds the promise of significantly improving the performance of oscillators, particularly in the critical aspect of phase noise reduction. In the final implementation of the quad-core DCO, each core adopts a complementary class-B P-N configuration featuring second harmonic tail resonators, as illustrated in Fig. 3.12. In the stand-alone P-N oscillator, the tail resonators typically employ coupled inductors to optimize space utilization and preserve all the advantages referred to in the previous section. These inductors resonate with the parasitic capacitance at the common-source nodes of NMOS and PMOS core transistors around the second harmonic of the oscillation frequency. In this work, tail transformers play a crucial role in simultaneously achieving filtering and strong coupling among the four cores. At small oscillation amplitudes, the coupled tail nodes establish a virtual ground, and as amplitudes increase, the nodes' movement signifies the onset of coupling.

To ensure symmetrical coupling, the NMOS tail inductance of one oscillator is coupled with the PMOS tail inductance of the nearest oscillator, as depicted in Fig. 3.12. This strategic coupling strategy avoids systematic mismatches that could arise from coupling NMOS tails to NMOS tails and PMOS tails to PMOS tails.

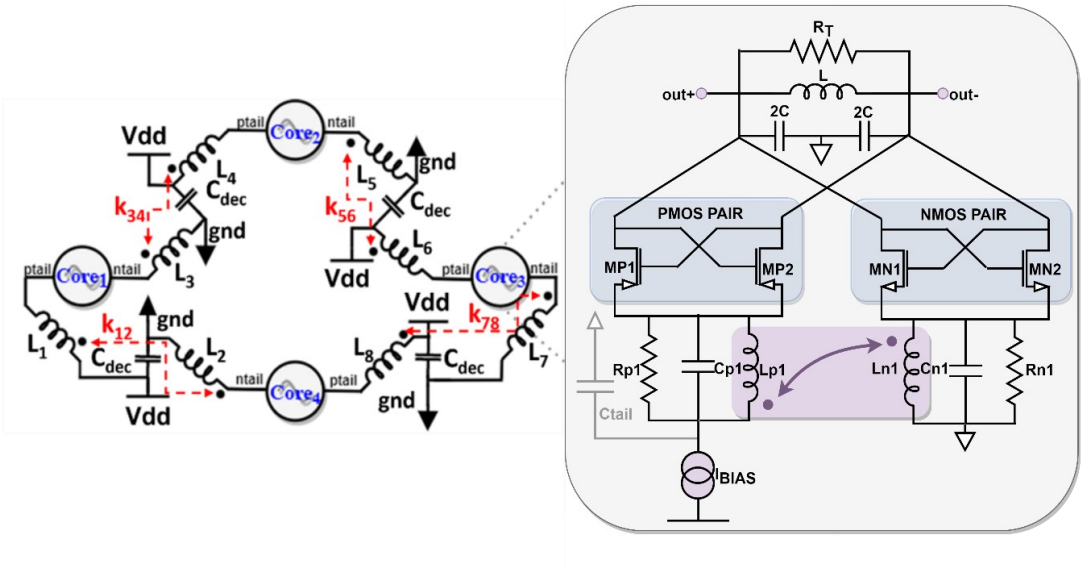


Figure 3.12 Final Implementation of quad core oscillator.

The previous section demonstrated the harmonic coupling of two oscillators through an inverting tail transformer to generate quadrature outputs. By coupling the tail nodes at the second harmonic in anti-phase, the NMOS oscillators' outputs are forced to be in quadrature. In the p-n oscillator, where NMOS and PMOS tails exhibit opposite polarity, coupling adjacent NMOS and PMOS tail nodes with inverting transformers results in in-phase oscillations across the four cores. This coupling approach helps to circumvent undesired parasitic elements and retains the benefits of the single-core oscillator topology without introducing additional undesired elements.

Harmonic coupling facilitates effective coupling between adjacent cores, enabling high-power efficiency by pushing core transistors into deep triode without loading the tank. The high series impedance formed around the second harmonic by the tail resonators ensures efficient power transfer. Additionally, the design choice of a P-N oscillator achieves the same peak Figure of Merit (FoM) as an N-only design with the same tank, with half the voltage swing. This approach mitigates reliability concerns associated with large voltage swings and provides a more optimal compromise between

FoM and phase noise. In the Fig. 3.12, large decoupling capacitors ($Cdec$) are strategically incorporated to close the loop for common-mode currents. The physical proximity of the transformer terminals to which $Cdec$ is connected minimizes undesired parasitic inductances, resulting in a 6 dB lower phase noise compared to a single oscillator configuration.

To minimize the residual phase noise contribution coming from the current source, PMOS devices with long channel length were preferred for the current generator. A long channel makes the effects of channel modulation and flicker noise minimum. The current generator provides the current for all the oscillators of the quad-core DCO.

3.8.1 Tank Scaling and Choice of Tank Components

Main Tank Scaling

The frequency of operation of the oscillator, denoted as f_{osc} as outlined with the following equation:

$$f_{osc} = \frac{1}{2\pi\sqrt{LC}}\sqrt{\frac{\delta^2 - 1}{\delta^2}} \tag{3.8.1-2}$$

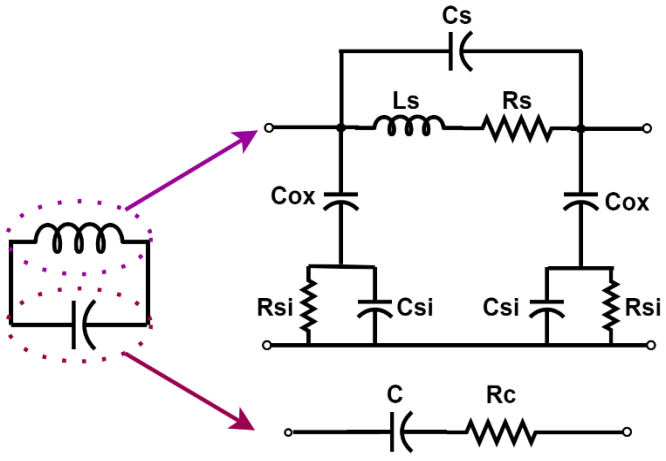


Figure 3.13 LC Scalable Tank Model.

Where the parameter $\delta = \frac{f_{srf}}{f_{osc}}$ is the ratio between the self-resonance frequency of the inductor and the oscillation frequency that is directly inversely proportional to the value of the total parasitic capacitance of the inductor. Given a specific frequency f_{osc}, it is important to note that the selection of inductance L and capacitance C is not singular. Consequently, should be comprehensively analysed the trade-offs associated with the tank component choices. According to the 9-element model described in [36] the capacitive coupling scales linearly with the inductance value. The component that is considered is presented in Fig. 3.13 and exhibits a dual-branch structure, comprising an inductive branch, designated as L-RL, and a capacitive branch formed by $Cox, Csub$, and $Rsub$. The inductive branch primarily addresses the desired inductive behavior of the component while also accounting for losses associated with the traces. On the other hand, the capacitive branch serves to model the capacitive coupling between the inductor and the substrate, as well as the losses related to this capacitive interaction. This dual-branch configuration is crucial for a comprehensive analysis of the component's behaviour. The capacitor is simply modelled by an $C - Rc$ branch that considers the losses of the capacitor. The total parasitic capacitance of the inductor can be estimated as:

$$C_{par} = \frac{C_{ox} C_{sub}}{C_{ox} + C_{sub}} \propto K'_{tot}\, L$$

(3.8.1-3)

According to equations above the values of and L and C are chosen as:

$$L = \frac{1}{2\pi\delta\sqrt{K'_{tot}}}$$

(3.8.1-4)

and

$$C = K'_{tot}\, L(\delta^2 - 1)$$

(3.8.1-5)

The above equations provide further insight by illustrating that when we scale up the oscillation frequency by a factor of M, it necessitates a corresponding reduction of M in both the tank's inductance and capacitance. This proportional adjustment is essential to maintain the desired frequency performance.

The minimum achievable phase noise is primarily governed by the smallest feasible inductor, characterized by the highest Quality (Q) factor achievable in the manufacturing process. Electromagnetic (EM) simulations are conducted to scale down the inductor diameter while ensuring the preservation of Q by preventing destructive cancellation of magnetic flux around the octagonal shape. The tank exhibits a quality factor Q≈15, predominantly influenced by the inductor, and presents an approximate equivalent differential parallel resistance of 440 Ω (with R ≈220 Ω in the block diagram in Fig. 3.14). The width of the main core devices is approximately 30um with the channel minimum length of 30nm used.

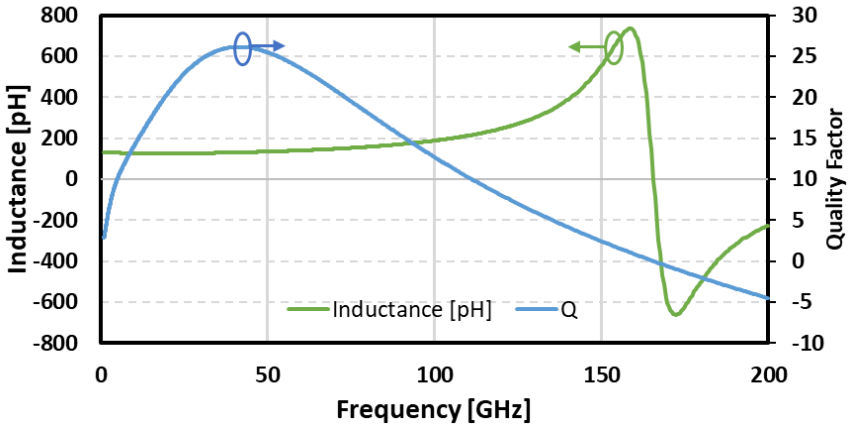


Figure 3.14 Inductance and Quality Factor of the chosen Inductor vs Frequency.

Tail Tank Scaling

In the realm of DCO design, the conventional approach entails the utilization of a tail LC network resonating at the second harmonic, thereby introducing a high series impedance. The implementation of two uncoupled networks in the oscillator tails results in a dual configuration of independent second-order filter networks. This investigation scrutinizes the optimization prospects arising from the incorporation of common mode coupling (k) and the fine-tuning of tail inductance values as seen in Fig. 3.15. The introduction of an enhancement factor serves as a quantitative metric to systematically assess the circumstances conducive to the augmentation of performance through common mode coupling, relative to the independent second-order network paradigm. Give as reference [37].

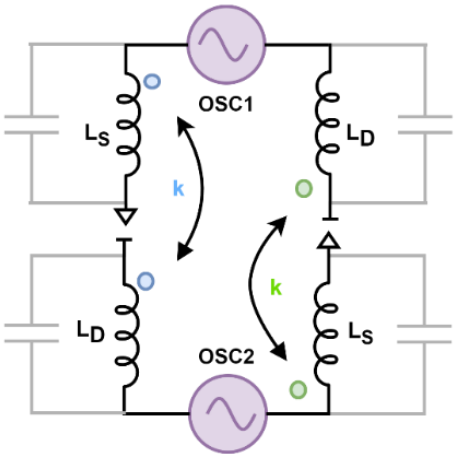


Figure 3.15 Schematic Diagram of the tail tank coupling between two oscillators.

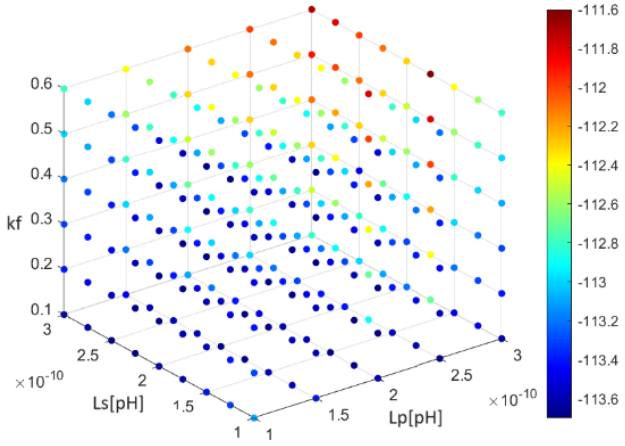


Figure 3.16 Phase Noise performance vs inductors Lp, Ls and coupling coefficient kf.

After careful consideration of the simulation results between two coupled oscillators as presented in Fig. 3.16, we conclude in an enhancement factor described below. The enhancement factor E is defined as:

$$\mathrm{E} = \frac{(1 - k_f)Z_D}{Z_D + Z_S - \sqrt{2}k_f\sqrt{Z_D Z_S}} \tag{3.8.1-6}$$

In the context of our study, the parameters Z_D and Z_S denote the inductances corresponding to of L_S and L_D, respectively. By examining the derivative of the enhancement factor, it becomes apparent that this factor achieves its maximum value when the inductance values are equal. To assess the circumstances under which incorporating common-mode coupling, denoted by kds, comm, and adjusting the value of the tail inductance LS, can yield the maximum advantage compared to the independent second-order network, an enhancement factor E is formulated. This enhancement factor G serves as a metric for quantifying the improvement achieved by introducing common-mode coupling and adjusting the tail inductance LS, facilitating a comparative analysis between the coupled and independent filter configurations. Fig. 3.17 presented herein serves as a visual means for the validation of the reported results. Equation 3.8.1 5 serves as a foundational tool for determining the key parameters for the implementation of our circuit, as elaborated in subsequent sections.

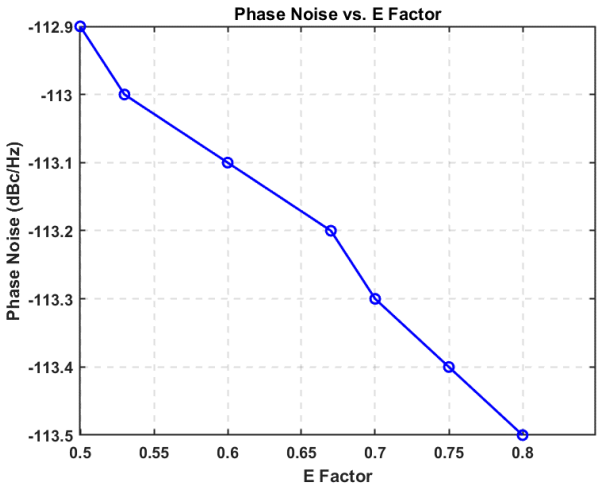


Figure 3.17 Phase Noise Performance vs Factor.

3.8.2 Design of Capacitor Arrays

In the pursuit of achieving swift and precise frequency ramps crucial for Frequency Modulated Continuous Wave (FMCW) applications, a fundamental requirement is a wide bandwidth with fine resolution for the digital control of the oscillator's frequency. The monotonicity of the Digitally Controlled Oscillator (DCO) characteristic is paramount, enabling the application of digital calibration techniques to enhance linearity. However, challenges arise when utilizing small inductors to mitigate phase noise, as the resulting large footprint of the capacitor array in the tuning bank introduces significant systematic errors in the frequency steps generated by the coarse tuning bank [32].

This substantial area occupation can lead to non-monotonic behavior, even when segmented arrays are employed. Such non-monotonicity imposes limitations on the achievable frequency resolution through digital tuning, thereby compromising linearity. Moreover, the increased size of the capacitor array contributes to elevated power dissipation within the Phase-Locked Loop (PLL). This intricate interplay of factors underscores the trade-offs and challenges associated with designing DCOs for FMCW applications, necessitating meticulous consideration of tuning bank configurations to strike a delicate balance between phase noise reduction, linearity enhancement, and power efficiency [33].

The incorporation of multiple independently addressed capacitor banks introduces a potential risk of compromising the monotonicity in the characteristic of the Digitally Controlled Oscillator (DCO). This concern arises from inherent mismatches among the unit cells within the expansive coarse array. Even when efforts are made to minimize random mismatches, as confirmed through Monte Carlo simulations, the presence of systematic errors may still emerge due to parasitic effects introduced by the array interconnects. This challenge is particularly pronounced in the context of our design's large coarse array.

To achieve precise linear control of the Digitally Controlled Oscillator (DCO), a comprehensive tuning strategy employs three capacitor banks: a PVT bank, a medium bank, and a coarse bank. Each bank is under the control of a dedicated digital component. In the initial tapeout, the design incorporates the PVT, medium, and coarse banks, as depicted in Fig. 3.18. Following this, in the following test chips, fine-tuning is introduced, playing a pivotal role in further enhancing control precision, as illustrated in the same figure. This careful design ensures close matching between the coarse and medium banks, promoting excellent linearity in the tuning process.

Specifically, the medium bank is equipped with 4-unit cells, providing a resolution of 10 MHz, while the coarse bank features 32-unit cells with a resolution of 40 MHz. In the second design iteration, a fine-tuning bank is introduced with a higher resolution of 500 kHz, offering enhanced control granularity. This addition addresses the need for finer frequency adjustments and contributes to the overall tuning precision. To counteract frequency variations arising from Process, Voltage, and Temperature (PVT) variations, a dedicated PVT bank with 16-unit cells is

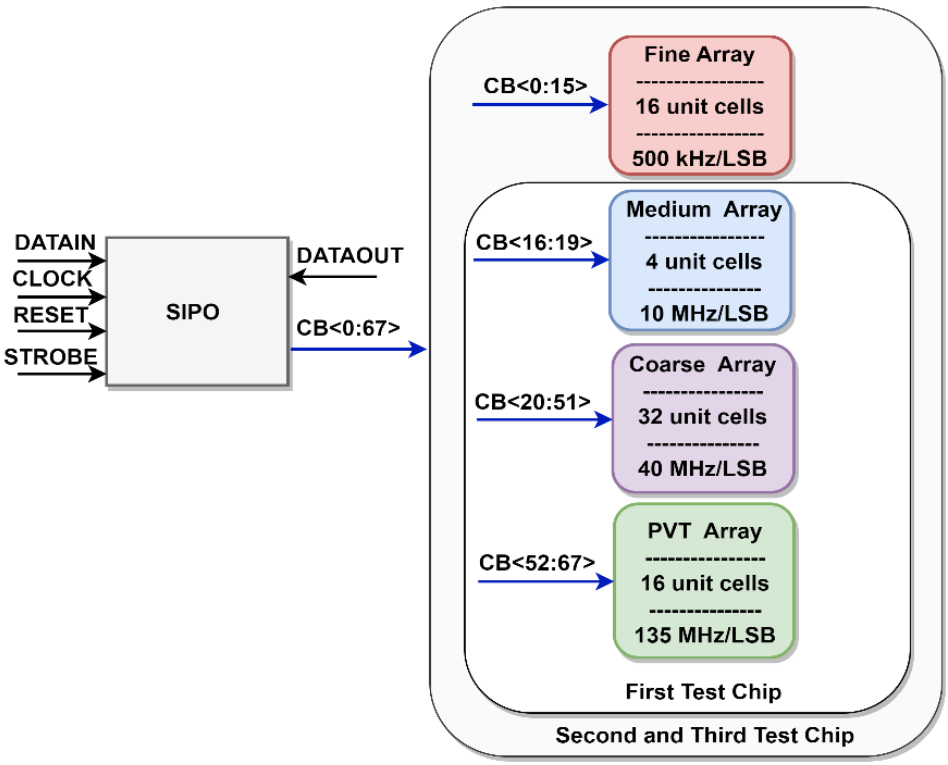


Figure 3.18 The Serial-in, parallel-out shift registers and capacitor arrays block diagram.

incorporated by a serial in parallel out shift register. Each unit cell, across all banks, is individually addressed using digital control bits, facilitating precise control over the tuning process. This comprehensive tuning approach, encompassing multiple banks with varying resolutions, showcases a thoughtful and versatile design strategy tailored to optimize the DCO's linearity and performance characteristics.

Design of Medium Array

In the medium unit cell, a switchable capacitor structure is implemented, following a conventional design. Each coarse unit cell comprises four identical medium bank unit cells, each independently addressable as it can be seen in Fig. 3.19. The architecture ensures that each coarse unit cell comprises four, contributes to effective matching and performance consistency. The average effective capacitance of the total array is equal to 2.21fF as it can be seen from monte carlo simulation results in Fig. 3.20. The width of the transistor M_{sw} has been chosen as a compromise between the quality factor of the capacitor cell, and the tuning range. The larger is the switch, the

higher is the quality factor, but the lower is the on/off capacitance ratio of the switched capacitor unit-cell.

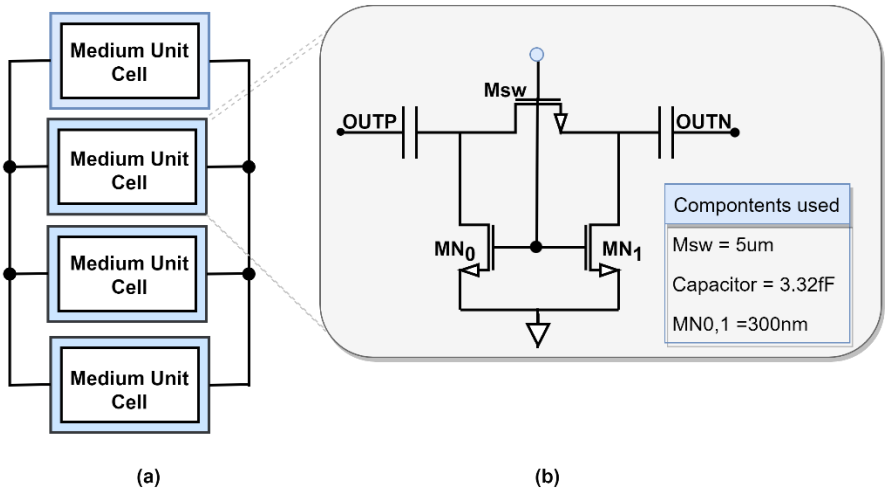


Figure 3.19 (a) Medium Array (b) Medium Unit Cell.

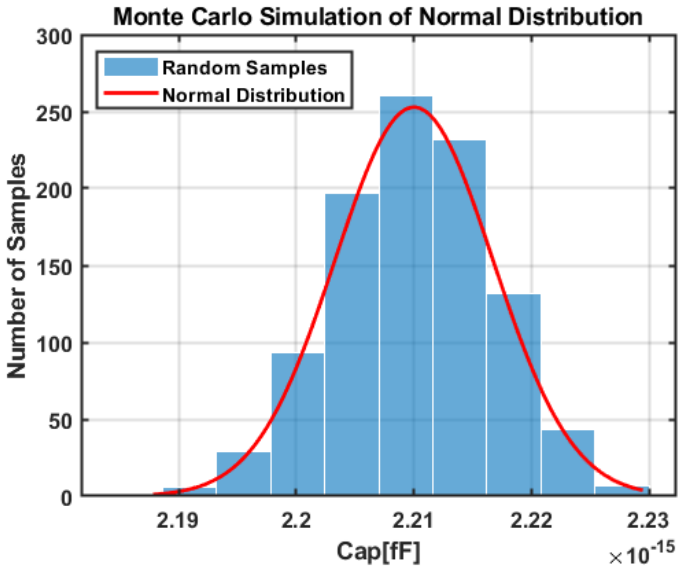


Figure 3.20 Con-Coff for medium bank array.

Design of Coarse Array

Emphasis is placed on the design strategy of each coarse unit cell, which encompasses four medium bank unit cells as shown in Fig. 3.21. This deliberate arrangement aims for careful matching and yields a notable frequency step of 40 MHz. The collective impact of these cells results in an array comprising a total of 32 units, establishing a foundation for the subsequent discussions on the array's functionality and characteristics. The coarse array and inductor are of comparable size, which makes it challenging to maintain an acceptable phase noise performance.

To comprehensively assess the impact of parasitics, electromagnetic simulations utilizing EMX were employed to construct a model that incorporates the effects introduced by the top.

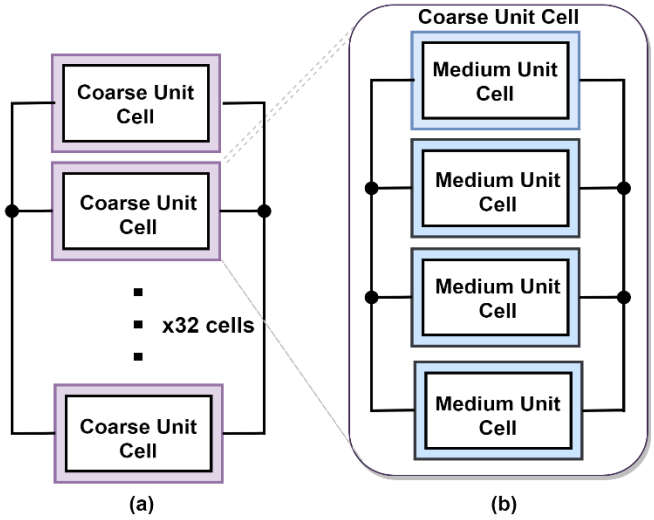


Figure 3.21 (a) Coarse Array (b) Coarse Unit Cell.

Notably, series inductors within these parasitics exert disparate influences on the effective capacitance of each cell within the array. In an initial design step, control bits were systematically arranged in the large coarse array, following the initial order depicted in Fig. 3.22 with a red arrow. However, the outcome revealed a frequency step with a maximum error exceeding ±1 MHz, a deviation deemed unacceptable in terms of linearity.

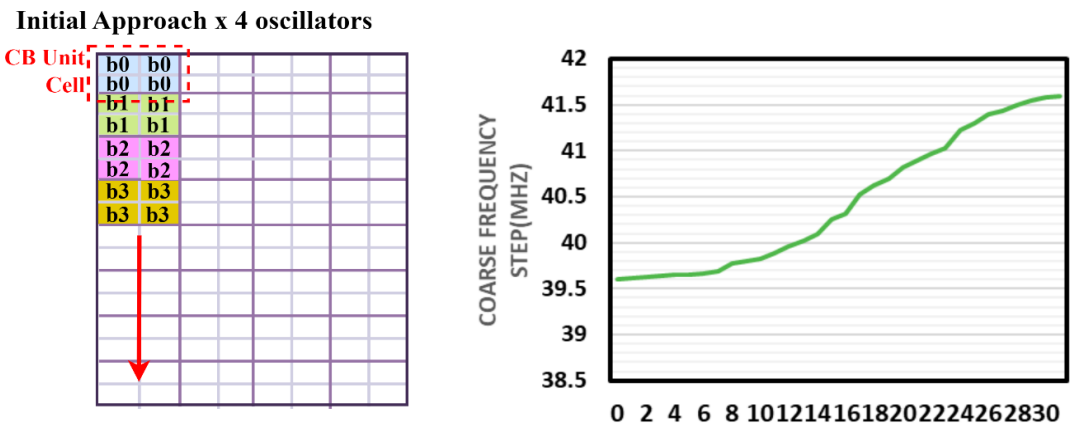
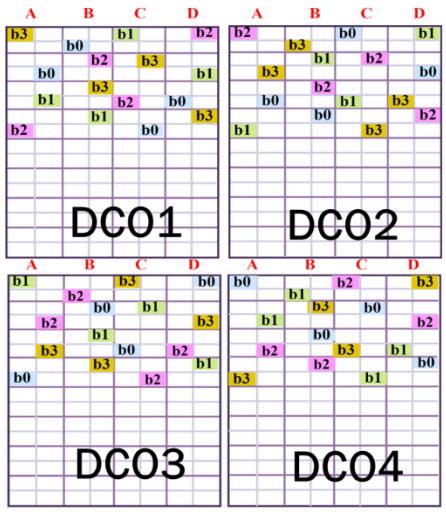


Figure 3.22 Initial Layout Approach for the Coarse Array.



	DCO1	DCO2	DCO3	DCO4
b0	A2+B1+C4+D3	A3+B4+C1+D2	A4+B2+C3+D1	A1+B3+C2+D4
b1	A3+B4+C1+D2	A4+B2+C3+D1	A1+B3+C2+D4	A2+B1+C4+D3
b2	A4+B2+C3+D1	A1+B3+C2+D4	A2+B1+C4+D3	A3+B4+C1+D2
b3	A1+B3+C2+D4	A2+B1+C4+D3	A3+B4+C1+D2	A4+B2+C3+D1

Figure 3.23 Bit Mixing Technique for Coarse Array.

To address the frequency step error in the coarse array and mitigate the impact of varying effective capacitance at different positions, an averaging (bit mixing) technique was introduced, as depicted in Fig. 3.23 Each coarse unit cell includes four independently addressable medium bank unit cells, employing four different bit lines for each coarse bank unit (CB) and utilizing four. different combinations for each DCO. By mixing the bit positions in a unique rotational order for each oscillator, the residual error was minimized to a few hundred kHz—a result validated by measurement outcomes. Consequently, effectively mitigates frequency step discrepancies, ensuring improved linearity in the DCO characteristic.

Design of PVT Array

Notably, the PVT bank is designed independently, further emphasizing its role in mitigating the impact of environmental variations on the oscillator's frequency. Across all unit cells, a conventional switched capacitor structure is implemented, aligning with established design principles in oscillator control. The configuration of the PVT cell is delineated in the accompanying Fig. 3.24. To enhance the quality factor, a differential RF MOS switch is employed. Two small grounded NMOS transistors are included in both capacitor unit cells to bias the floating nodes in the ON-state. Additionally, pull-up devices are incorporated for the PVT unit cells to augment the OFF-state quality factor. This configuration results in a substantial OFF-state quality factor, as expressed in the subsequent equation:

$$\frac{1}{Q_{total,OFF}} = \frac{C_{par}}{C_{par}+C_{mom}} \times \frac{1}{Q_{mom}} + \frac{C_{mom}}{C_{par}+C_{mom}} \times \frac{1}{Q_{par}} \quad (3.8.2\text{-}1)$$

Where the quality factor of the customized capacitor C_{mom} is $Q_{mom} = (r_{mom} \times C_{mom\times}\omega)^{-1}$, and the quality factor of resistor of MOS devices and $Q_{par} = r_{on,MOS} \times C_{par} \times \omega$ the quality factor of the parasitic capacitor, $C_{par} = C_{db,sw} + C_{p,MOM} + C_{db,bias}$. The design choices made in the implementation of the proposed circuit are carefully aligned with the goal of optimizing performance. Notably, the integration of MOS devices is a pivotal aspect of the design, leveraging components that offer high resistivity within their paths. This deliberate selection contributes to an increase in the parallel quality factor Q_{par}, a crucial parameter in enhancing circuit efficiency.

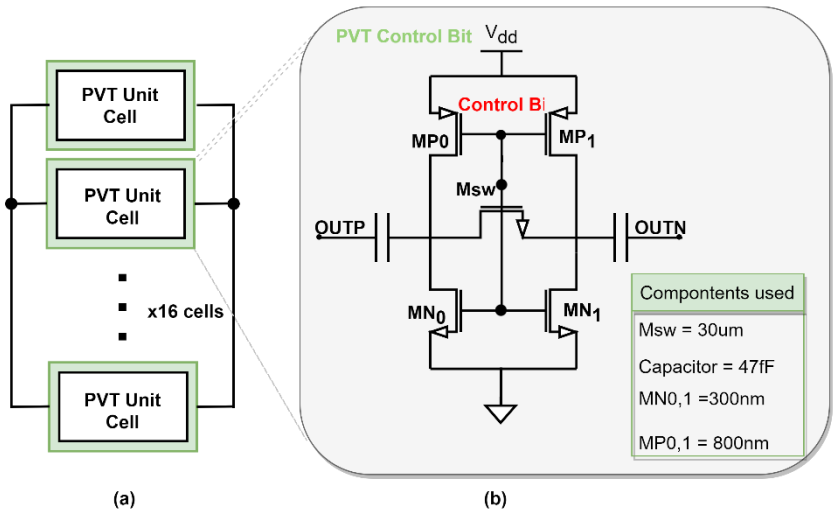


Figure 3.24 (a) PVT Array (b) PVT Unit Cell.

Design of Fine Array

In the second and third test chip implementation, the design is augmented with the addition of the fine-tuning array. The configuration involves connecting the gates of MN0 and MN1 to VDD, creating a continuously conducting path. The common source of these two transistors is linked to the inverted control signal. In the on-state, the NMOS pair operates as a low-ohmic path to the ground. Given that the gate and source voltages of MN0 and MN1 are both approximately at VDD, these transistors are biased in the sub-threshold region, resulting in highly resistive paths from the drain/source of the switch transistor Msw to VDD [34].

The design carefully incorporates the modeling of custom-made small capacitors. The effective capacitance of each unit cell is standardized at 34 aF, corresponding to a frequency step of 625 kHz. Ideally, the total frequency range covered by the 16 fine unit cells of the array is 10 MHz. This careful implementation ensures the accurate functioning of the fine-tuning array, contributing to the overall precision and performance of the design.

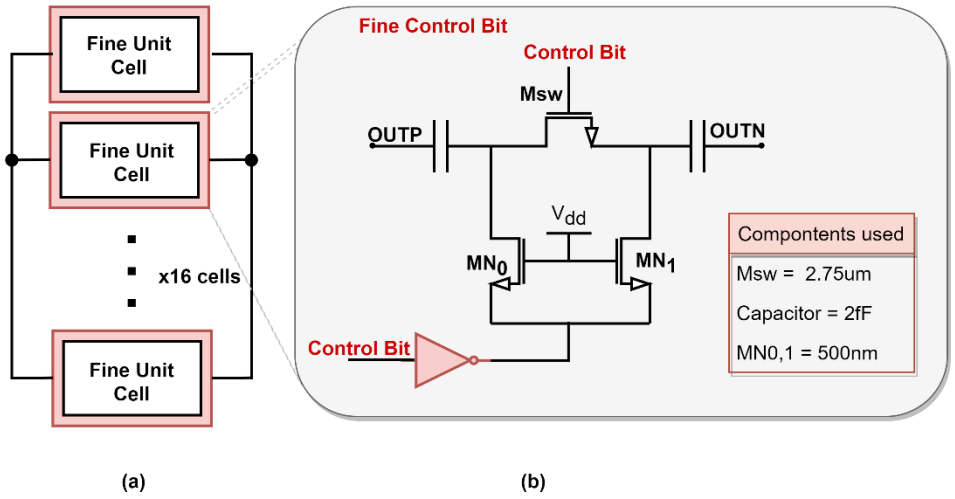


Figure 3.25 (a) Fine-Array (b) Fine-Unit Cell.

3.8.3 Layout Considerations

Careful layout considerations for transformers and main core tank inductors aim to minimize parasitic magnetic couplings within the quad-core DCO structure. The current generator is placed in the center of the chip and as a result current matching across the multi-core oscillator array is optimized. Simulations indicate that mismatches in transistors and bias currents have a negligible impact compared to mismatches in the tank components. Symmetry is a key aspect of the arrangement, not only in terms of signal pathways but also in terms of ground return paths. On-chip capacitors are strategically employed for power supply decoupling, enhancing the overall stability and performance of the quad-core DCO in the final implementation.

3.9 Phase Noise Robustness in Quad-Core Oscillator

In practical implementations, mismatches between the oscillators' resonators result in each oscillator having a slightly different self-resonance frequency. As highlighted in prior publications [19], [27], this frequency mismatch can lead to phase noise degradation. Fig. 3.26 illustrates the impact of frequency mismatch on phase noise penalty in a quad-core system. The obtained results lead to the conclusion that the impact of frequency mismatch on the phase noise penalty is significant only when it exceeds one coarse step. This observation suggests that the quad-core oscillators

operate effectively when coupled, demonstrating robustness in the presence of systematic layout mismatches. In real-world scenarios, variations between the array resonators result in each oscillator having a slightly different self-resonance frequency.

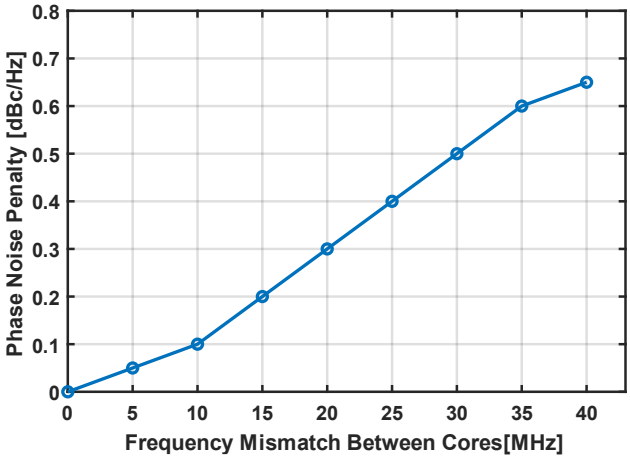


Figure 3.26 Phase Noise Penalty for a quad-core in presence of frequency mismatch.

3.10 Test Scheme and Measurement Results for the First Test Chip

The fabrication of the first prototype circuit was successfully completed, followed by a series of comprehensive measurement procedures. To fully grasp the subsequent analysis, it is essential to have a firm grasp of the overall schematic layout, as illustrated in Figure 3.27. In the preliminary stages of our investigation, we encountered a notable challenge regarding the precise measurement of Phase-Noise within the designated frequency offsets, spanning from 100 kHz to 1MHz. To address this challenge, a method of injecting-locking into DCO was devised, relying on a weak inductive coupling mechanism between the oscillator inductor and an external coil. This external coil, energized by a signal generator, emits a pure harmonic signal precisely aligned with the average oscillation frequency of interest. Strategic positioning of the external coil above the chip surface, at a carefully determined distance from the oscillator inductor, ensures optimal coupling. To maintain measurement accuracy, adjustment of the signal generator's power is undertaken to attain a locking range spanning a few kilohertz. This precise adjustment serves to mitigate potential inaccuracies in Phase-Noise measurements.

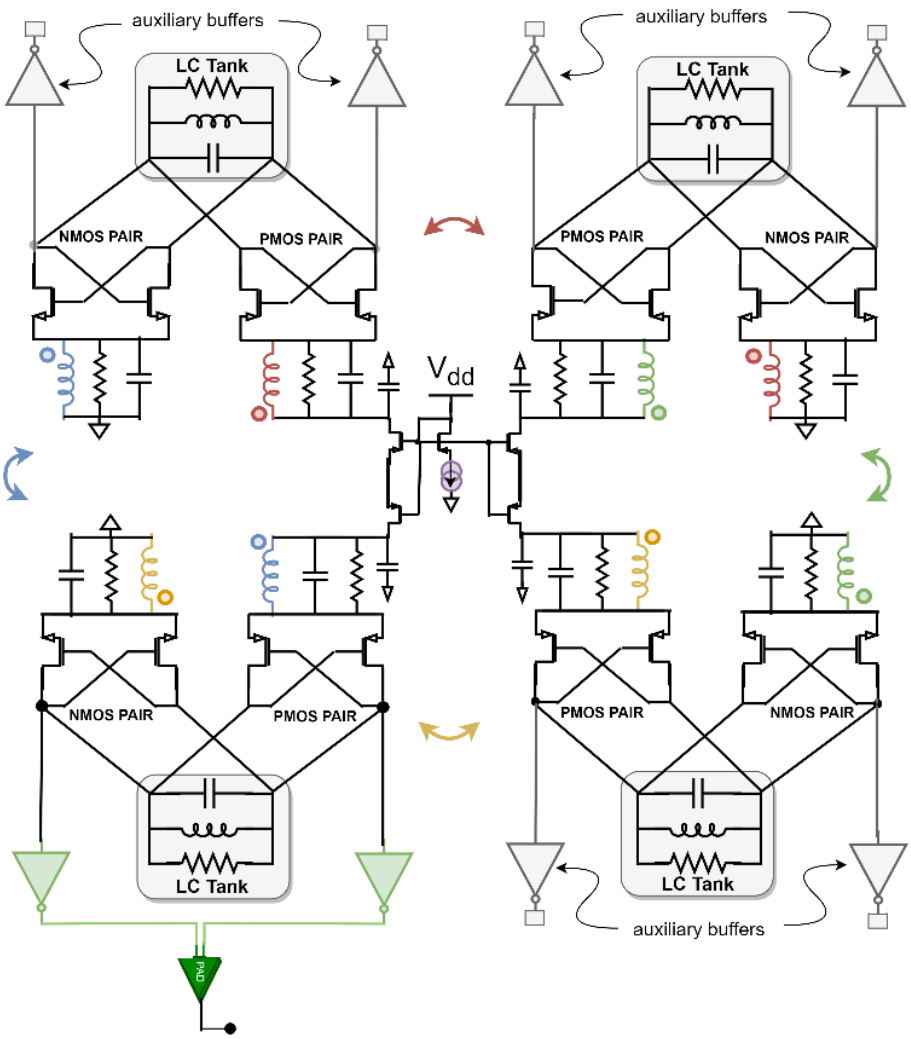


Figure 3.27 Overall Schematic of Quad Core DCO.

The chip operates with a supply voltage of 1.2 V and is biased at a current of 18.4 mA. The Voltage-Controlled Oscillator (VCO) outputs are carefully buffered through the output chain, ultimately reaching a differential GSGSG pad frame for precise differential probing. Power-supply, bias currents, bias voltages, and both digital and analog frequency control are facilitated using bonding wires. A Microphotograph of the chip is presented in Fig. 3.28.

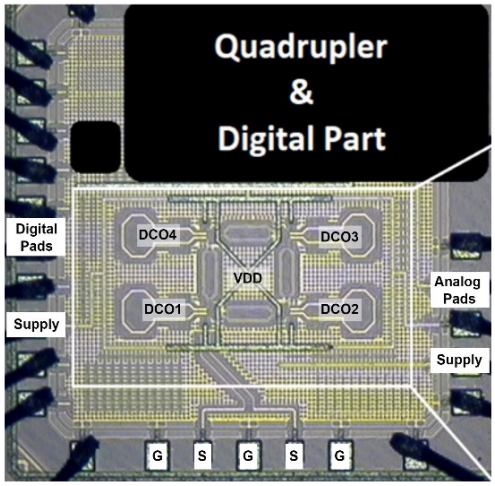


Figure 3.28 Test Chip Microphotograph.

The output signal of the DCO is systematically measured utilizing a GSGSG probe, which is intricately connected to a spectrum analyzer. Power supply, analog bias signals, and digital controls are seamlessly delivered through bonding wires, facilitated by an analog DC-Board and a digital interface programmable via PC, as illustrated in Fig. 3.29. The measurement setup is visually depicted in the corresponding figure. To ensure the integrity of the measurements, a thoughtful arrangement of on-board capacitors, spanning from 1 μF to 33 pF, has been strategically positioned near the chip. This placement aims to effectively filter out extraneous noise originating from the bias circuitry and instrumentation. The oscillator, in its operational state, consumes an estimated 22.1 mW of power derived from a 1.2 V supply. Certainly, here's a revised version that reflects a positive outcome: During the initial tape-out, an underestimation of parasitics resulted in a frequency drop, primarily due to the extended interconnects of the coarse array acting as an unintended inductor. Notably, this issue was successfully addressed and rectified during the final test chip.

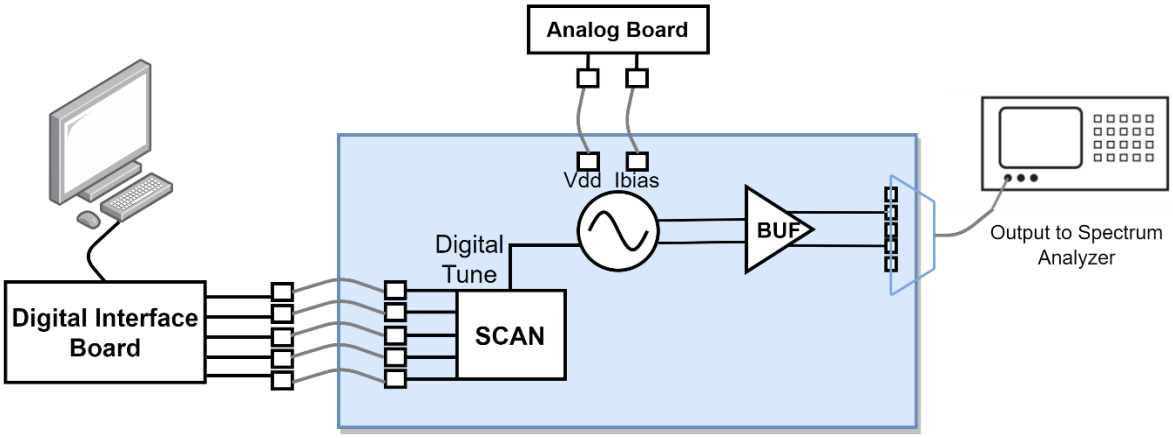


Figure 3.29 Measurement setup for the stand-alone Quad-Core DCO.

Despite potential power reflections, the output wave directed to the spectrum analyzer retains sufficient energy (with a carrier power of -5 dBm) to yield accurate measurements of the Phase Noise. Notably, the phase noise performance is observed to be optimal, reaching a low of -117.3 dBc/Hz at a 1 MHz offset from the central frequency of 15.35 GHz. Conversely, the worst-case scenario demonstrates a phase noise performance of -114.2 dBc/Hz at a 1 MHz offset from the carrier frequency.

The implemented oscillator spans a tuning range from 14.5 to 17.9 GHz with a medium resolution of 10 MHz. In the final test chip implementation, a fine resolution of 500 kHz is introduced. Fig. 3.30 depicts the oscillation frequency measured as a function of sequentially switching on an extra control bit over the coarse bank array. When a single control bit of the coarse bank array is enabled, the figure also illustrates the frequency step error from the ideal 40 MHz. The maximum residual error is ±240 kHz within a total range of 1.28 GHz covered by the coarse bank. This indicates that the resolution of digital frequency tuning, at four times the oscillation frequency, could be pushed down to less than 1 MHz without encountering non-monotonicity issues.

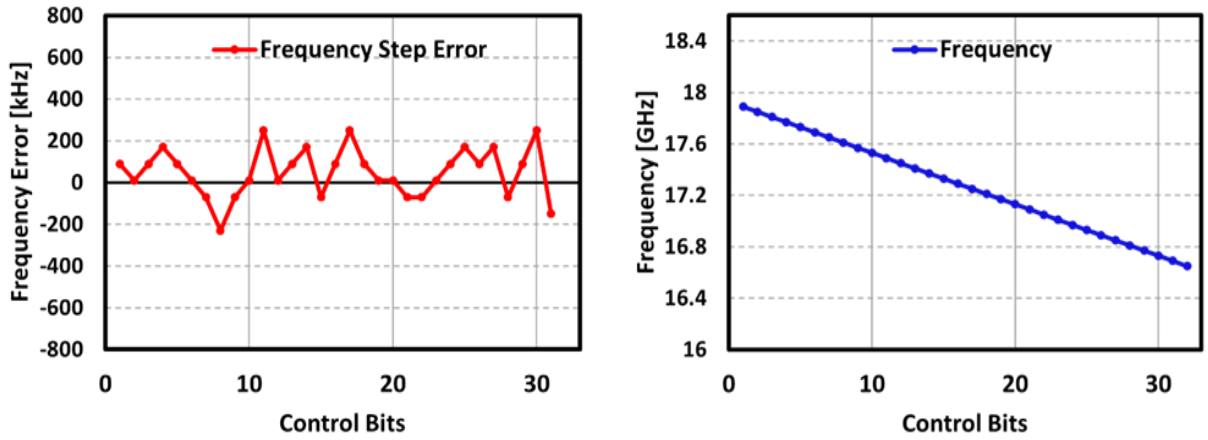


Figure 3.30 Measured Frequency Step per Control Bit and (b) Frequency Step Error for each 40 MHz Coarse Step.

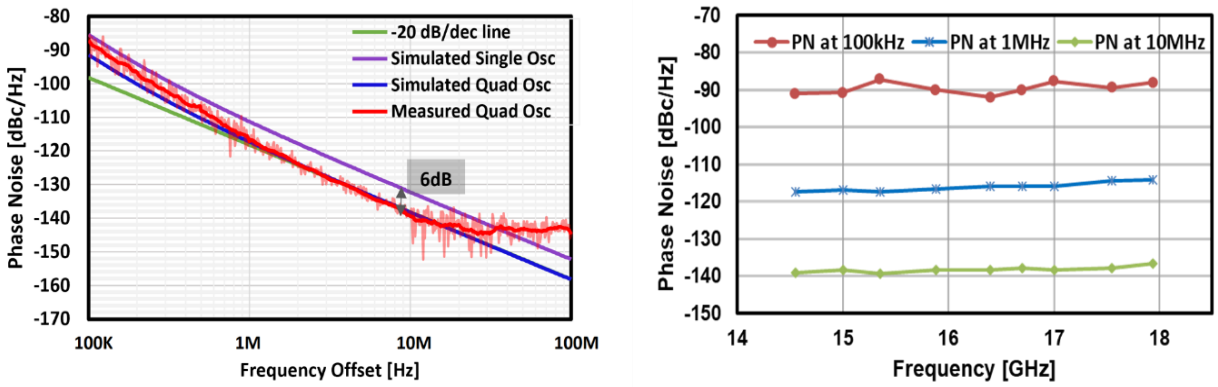


Figure 3.31 (a) Measured Best Phase Noise Performance (b) Phase Noise over a range of Frequency Offsets.

The phase noise performance of the proposed four-core class-B DCO, with a total current Itotal = 18.4 mA, is depicted in Fig 3.31. Notably, at a 1 MHz offset from the carrier frequency of = 15.35 GHz, the observed phase noise is exceptionally low at -117.3 dBc/Hz. Within the $1/f^2$ noise region, the measurements align closely with the simulations within the accuracy limits of the phase noise analyzer. The corner frequency $1/f^3$ is measured at approximately 660 kHz. Fig 3.31 further illustrates the phase noise measurements across a range of offset frequencies. It is noteworthy that the increase in phase noise becomes more pronounced at higher frequencies. This phenomenon is likely attributed to a mistuning of the common-mode resonances in the tails induced by parasitic elements.

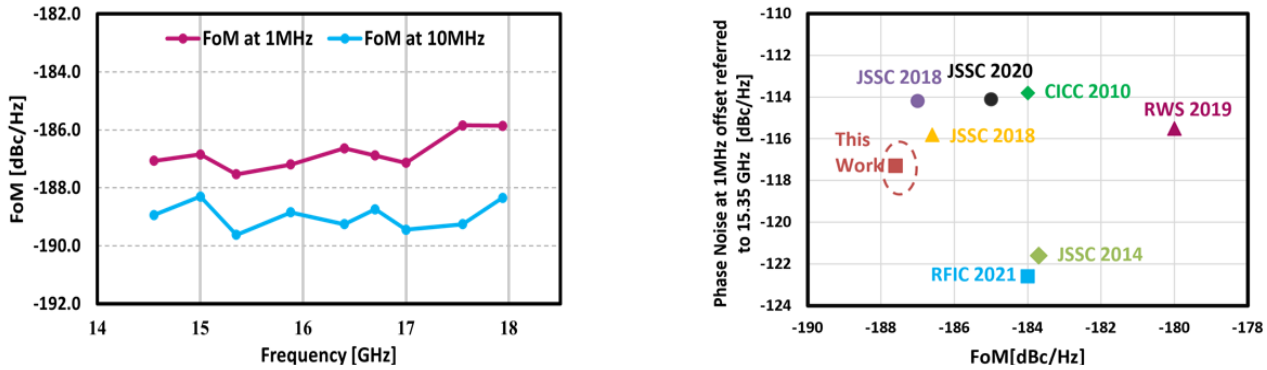


Figure 3.32 (a)FoM at 1MHz and 10MHz Offset from the carrier frequency (b) Comparison of the structure with the state-of-the-art.

The corresponding Fig 3.32 depicts the Figure of Merit (FoM) across the tuning range, specifically at 1 MHz and 10 MHz offsets. The FoM values range between -187.6 and -185.8 dBc/Hz at 1 MHz offset and between -189.6 and -188.2 dBc/Hz at 10 MHz offset.The second graph in Figure highlights that the overall performance of the DCO is highly commendable, excelling in both phase noise performance and efficiency when compared to the state of the art in the field. Figure 3.33 presents a thorough comparison of phase noise performance between post-layout simulations and experimental results. Post-layout simulations employed both nominal and worst-case flicker noise models from the TSMC 28nm technology library. Phase noise performance was evaluated across various offset frequencies, namely 100 kHz, 1 MHz, and 10 MHz from the carrier frequency.

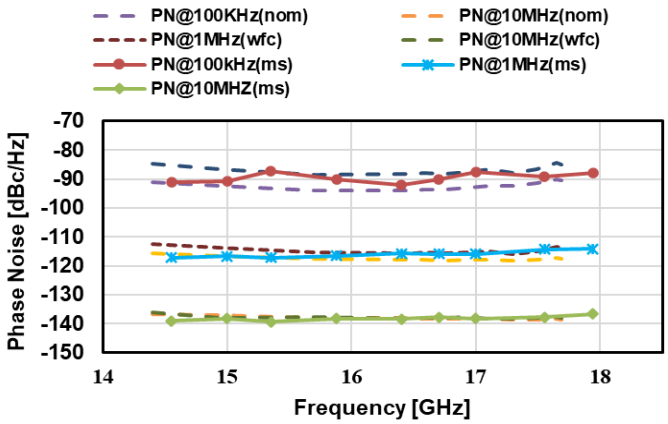


Figure 3.33 Phase Noise Performance at different Offsets for nominal and worst flicker models and Measurements.

The table below provides a comprehensive summary and comparison of the quadcore overall performance against state-of-the-art counterparts. To facilitate a fair assessment of phase noise, the normalized phase noise performance is introduced at a 1 MHz offset from the carrier for each implementation. The proposed DCO demonstrates outstanding phase noise characteristics along with a highly competitive Figure of Merit (FoM) and compact footprint when compared to other implementations.

	Test Chip 1	[47]	[31]	[30]	[12]	[48]	[49]	[50]
Number of Cores	**4**	8	4	4	4	2	1	1
Center Frequency [GHz]	**16.25**	12.4	54.2	26.45	46.75	12.8	19.5	18.7
Technology	**28 nm CMOS**	28 nm CMOS	65nm CMOS	40nm CMOS	65nm CMOS	65nm CMOS	28 nm CMOS	28 nm CMOS
TR [%]	**20.3**	27	9	26	16.5	31.3	12	11.6
V_{dd} [V]	**1.2**	1.1	1.2	0.95	0.9	1.2	0.9	1.8
P_{DC} [mW]	**22.1**	173	144	16	21.5	22.5	20.7	90
PN at 1MHz Offset [dBc/Hz]	**-117.3**	-126	-111	-110	-106.1	-115.5	-112	-113.8
PN at 1MHz offset referred to 15.35 GHz [dBc/Hz]	**-117.3**	-122.6	-121.6	-114.2	-115.8	-113.8	-114.1	-115.5
FoM [dB]	**-187.6**	-184	-183.7	-187	-186.6	-184	-185	-180
Core Area [mm^2]	**0.16**	3.8	1.7	0.1	0.039	0.23	0.07	0.038

Table 3-1 Table Overall First Test Chip Performance and Comparison with the State-of-the-art.

3.11 Test Scheme and Measurement Results for the Second Test Chip

The testing methodology employed for this tape-out remained consistent with the approach adopted during the initial tape-out, with minor modifications to the PCB design. As predicted, the frequency range achieved matched expectations. Under nominal conditions, the covered frequency spectrum spans from 16.77 to 20.77 GHz. The phase noise performance of the oscillator exhibited a slight deviation from the simulated values. As illustrated in the accompanying plot, the optimal phase noise performance was observed at 18.73 GHz, recording -114.72 dBc/Hz. This value closely approximates the worst-case simulated scenario.

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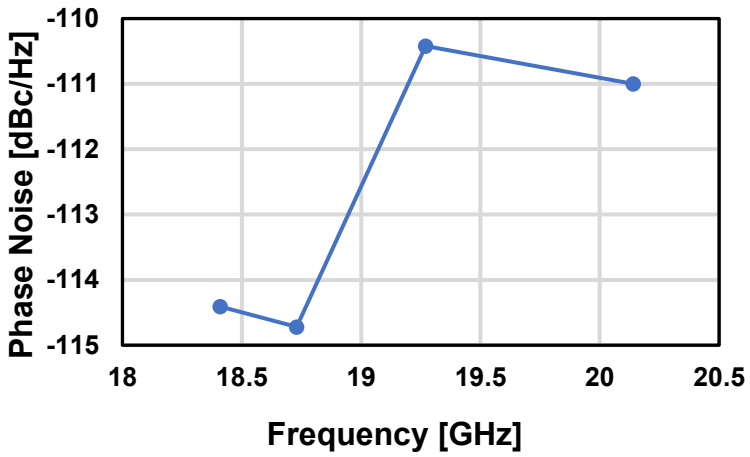

Figure 3.34 Phase Noise Performance at 1MHz offset.

3.12 Test Scheme and Measurement Results for the Third Test Chip

The oscillator testing methodology employed for this tape-out maintained consistency with the methods employed in previous iterations. The oscillator's linear frequency tuning range is accomplished through the implementation of three capacitor banks. These include a coarse bank comprising 32 elements with a nominal step of 40 MHz, a medium bank incorporating 4 elements with a nominal step of 10 MHz, and a fine bank consisting of 16 elements with a nominal step of 540 kHz. The measured frequency steps for each element within these three arrays are presented in Figure 3.35, depicted as a function of the control bits associated with the oscillator output. It is crucial to emphasize that the reported values in the plots represent the actual frequency steps. It is noteworthy to mention that, for this measurement, the oscillator output (before the frequency quadrupler) was utilized.

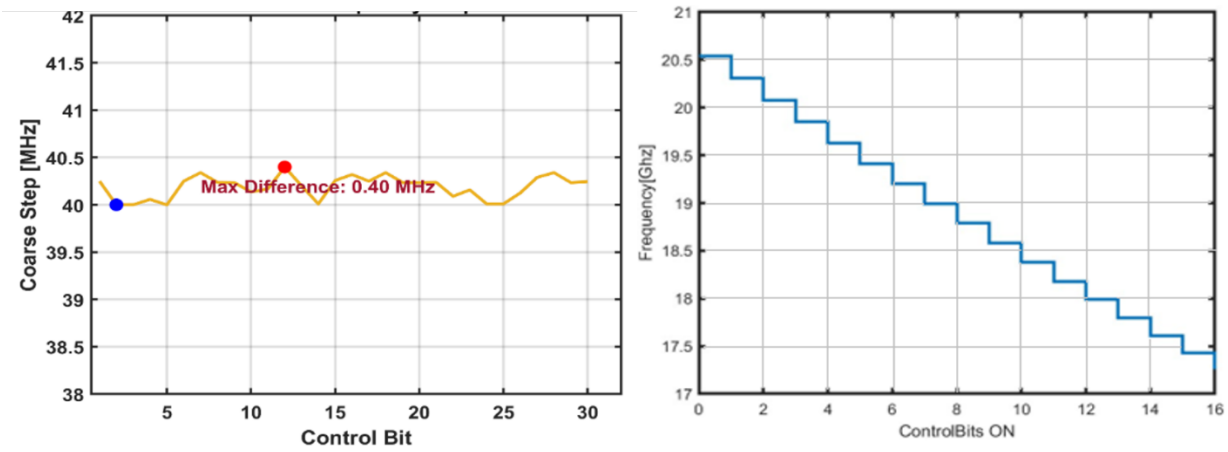

Figure 3.35 Coarse array oscillator frequency (a) step variation (b) step.

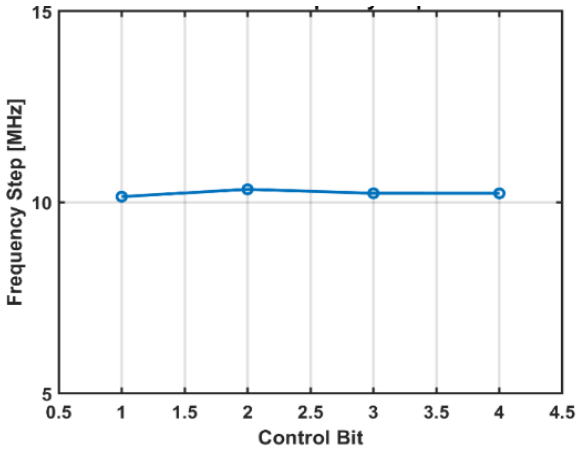

Figure 3.36 Medium array oscillator frequency step.

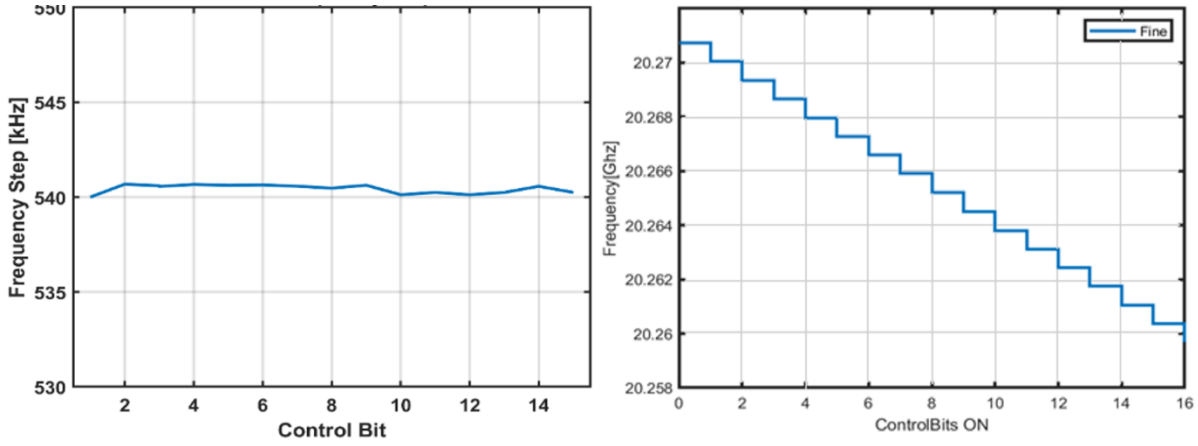

Figure 3.37 Fine array oscillator frequency (a) step variation (b) step.

The measured frequency step error for the coarse array is found to be less than 400 kHz, representing the ultimate precision limit of the proposed solution. The medium frequency step closely aligns with the nominal value. However, the fine frequency step is measured at 540 kHz, slightly less than the nominal 625 kHz. This results in an integral error when the entire fine array is switched off and one medium bank element is turned on, amounting to 540 kHz x 16 – 10 MHz = 1.36 MHz at the oscillator output and 5.4 MHz at the multiplier output as we will spot in the next chapter. This is in proximity to the target maximum nonlinearity error of 5 MHz. Furthermore, resizing the capacitors in the fine-tuning array has the potential to significantly reduce this frequency error.

The plot in Fig. 3.38 illustrates the relationship between the output frequency (fout) at a 20 GHz output DCO frequency and the code relationship. Various cases were simulated by selectively switching one control bit of the coarse array, the two bits of the medium band, and different combinations of the fine bank unit cells. Notably, the 2 Least Significant Bits (LSBs) of the fine array were excluded to streamline simulations. In this context, the minimum and maximum values for each array are defined as follows: for the fine array, it ranges from 0000 to 11xx; for the medium array, it ranges from 00 to 11; and for the coarse array, it ranges from 0000 to 0001. The frequency step at the multiplier output will be four times the one plotted in the following figures.

The steps observed in Fig 3.38 deviate slightly from the nominal value of 2.5 MHz. The extreme cases are highlighted in red, with a maximum deviation from nominal of +180 kHz and -156 kHz. The first critical case, labeled as #13, involves all bits in the fine and medium banks (m1 m0) (f3 f2 f1 f0) changing from 1 to 0, while the Least Significant Bit (LSB) of the coarse array goes from 0 to 1, transitioning from (11) (11xx) to (00) (00xx), activating one control bit in the coarse array. The second worst-case scenario is #17, where all fine bank control bits are turned off, and one bit from the medium array is turned on, transitioning from (01) (11xx) to (10) (00xx).

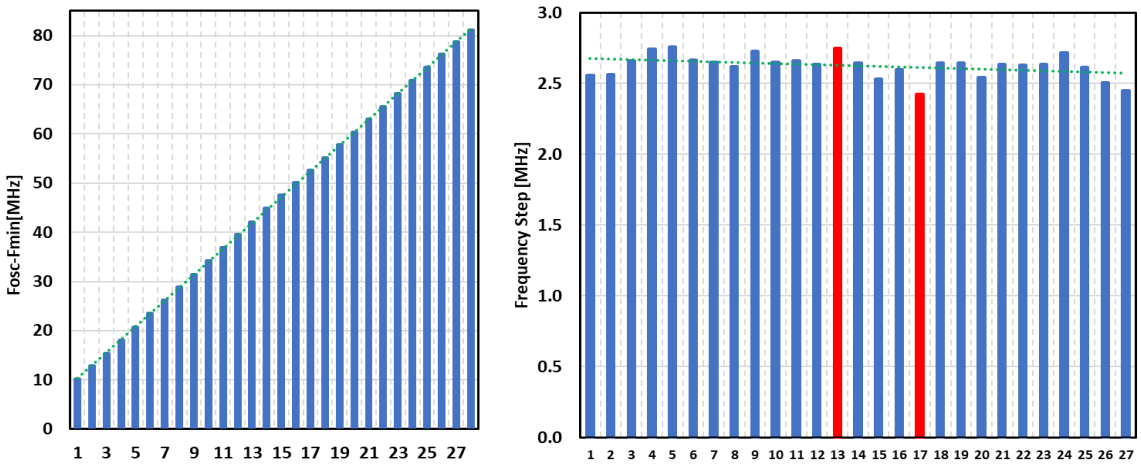

Figure 3.38 (a) Fout (b) Nominal Step.

The measured oscillator phase noise at a 1 MHz offset from the carrier exhibits variation, ranging from -113.5 dBc/Hz near 18 GHz to -115.5 dBc/Hz at both 17.3 GHz and 20.25 GHz in Fig 3.39-. Similarly, at a 10 MHz offset from the carrier, the measured oscillator phase noise ranges from -133 dBc/Hz in the proximity of 17.5 GHz to -137.9 dBc/Hz at 20.25 GHz as seen in Fig 3.40. Fig 3.41 gives a comparison with the simultations at 1MHz offset from the carrier so we can observe that there is a degradation of 2 dB.

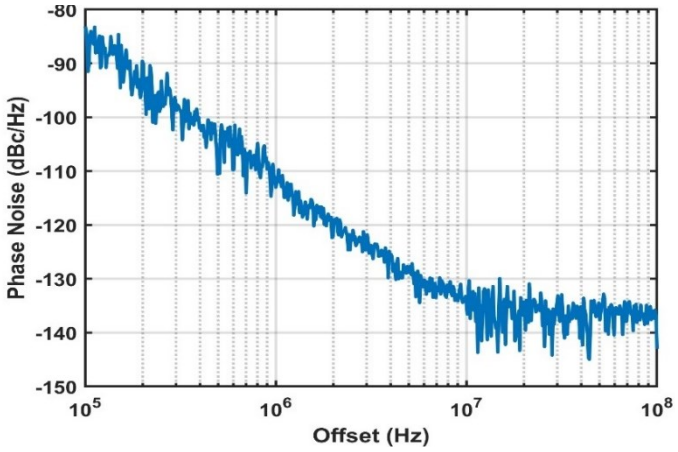

Figure 3.39 Oscillator phase noise performance at 18.5GHz.

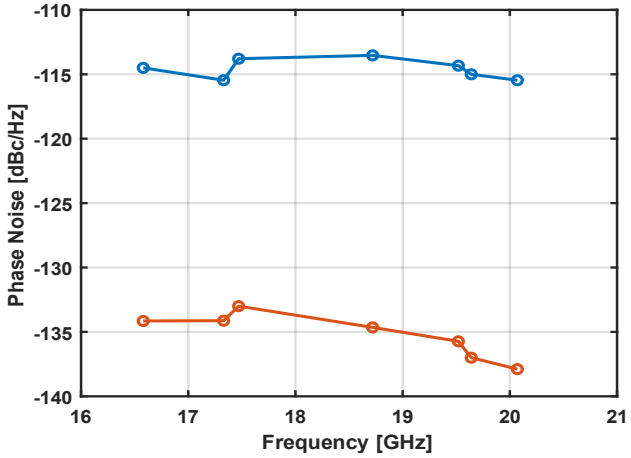

Figure 3.40 Oscillator phase noise measurements as a function of the oscillator frequency.

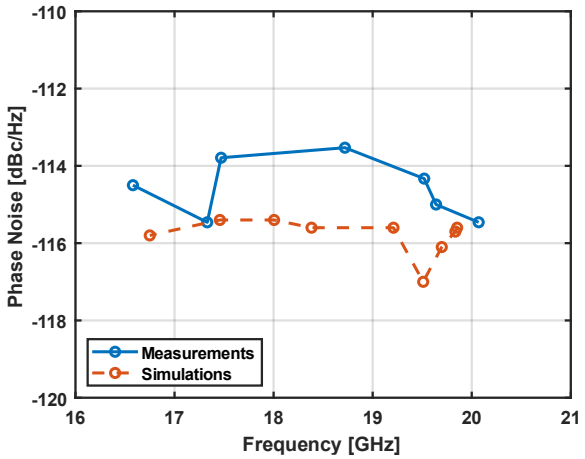

Figure 3.41 Comparison of Measured and Simulated of Phase Noise at 1MHz Offset.

In the evaluation of our final implementation of the quad-core oscillator, a comprehensive comparison against state-of-the-art counterparts in table 3-2 reveals an exceptional level of performance and comparability. Our quad-core oscillator demonstrates prowess in key aspects such as phase noise, frequency stability, and overall signal quality, placing it on par with or even surpassing established benchmarks in the field.

3.12 Conclusion

In summary, this chapter has outlined the development of a harmonic coupled oscillator with excellent phase noise performance and tuning range. Through systematic analysis and optimization, including single-core, multicore, and quad-core implementations, the oscillator design has been efficiently refined. Key aspects such as tank scaling, component selection, and layout design were carefully considered to enhance performance and reliability. The test schemes and measurement results presented across three test chips demonstrate the effectiveness of the design approach. Overall, the harmonic coupled oscillator represents a significant achievement in RF circuit design, offering advanced phase noise characteristics and broad tunability.

	Test Chip 3	[49]	[19]	[51]	[11]
Technology	28 nm CMOS	28 nm CMOS	65nm CMOS	65nm CMOS	40nm CMOS
Supply Voltage [V]	1.2	0.9	0.75	1.1	0.95
Center Frequency [GHz]	18.6	19.5	19	27.3	26.4
TR [%]	18	12	16	15.3	26
Pdc [mW]	24	14.4	16.4	3.4	16
Phase Noise at 1MHz[dBc/Hz]	-115.5	-108.5	-115	-104	-110
FoM at 1MHz [dBc/Hz]	-187.2	-183	-188.4	-187.6	-187

Table 3-2 Overall Third Test Chip Oscillator's Performance and Comparison with the State-of-the-art.

Chapter 4

4.1 Introduction

As described in Chapter 1, the targeted frequency range for the forthcoming high-performance automotive radar system lies between 76 GHz and 81 GHz. Chapter 4 delves into the design of a quad-core class B oscillator primarily intended for operation close to 20 GHz. To fulfill the application requirements, a critical aspect involves achieving frequency multiplication by a factor of 4. This chapter introduces a novel method for extracting the 4th harmonic from the quad-core class B oscillator, utilizing a redesigned buffer implementation. It's important to acknowledge that the multiplier circuit employed in this design is the result of a collaborative effort, with the actual multiplier having been designed by my colleague Paolo Ricco.

4.2 Frequency Multiplication Circuits in Millimeter-Wave Applications

In the domain of millimeter-wave (mm-wave) circuits, [38] presents a comprehensive overview of multiplier circuit architectures, neatly categorized into three distinct groups. The first category encompasses mixer-based architectures, thoroughly documented in references [39] and [40]. These circuits harness the efficiency of mixers to achieve multiplication in the mm-wave spectrum. The second category comprises strategies centered on device nonlinearities, with references [41] and [42] offering insights into this specific avenue. By exploiting the inherent nonlinearities of devices, these circuits offer a unique approach to achieving high-frequency multiplication. The third category delves into injection-lock-based methodologies, as elaborated in [43] and [44]. These approaches draw upon the principles of injection-locking to enable efficient multiplication in the demanding mm-wave domain. Collectively, these categorized multiplier circuits contribute to a refined understanding of the diverse methodologies employed in advancing mm-wave technologies.

The quest for high-frequency multiplication encounters challenges such as excessive power dissipation, reduced power efficiency, and limited bandwidth within frequency multiplier circuits. Notably, these limitations can result in scenarios where the power consumption of the frequency multiplier exceeds that of the oscillator it is intended to augment. In the context of our project, we introduce a novel approach—a proposed E-band frequency quadrupler that utilizes the cascaded integration of push-push frequency doublers. This innovative design aims to address these limitations and make a significant contribution to the advancement of frequency multiplier technologies.

4.3 Frequency Quadrupler Design

A single-supply (1 V) design utilizes a transformer-based matching network with multiple secondary windings to achieve a significant differential mode and minimal common-mode inductance, leveraging mutual couplings. This design strategy enables the use of a larger common-mode capacitor for the harmonic reflector, effectively suppressing the parasitic resonance of the push-push doubler output impedance at high frequencies. Additionally, the differential mode inductance is precisely controlled to the desired value [45].

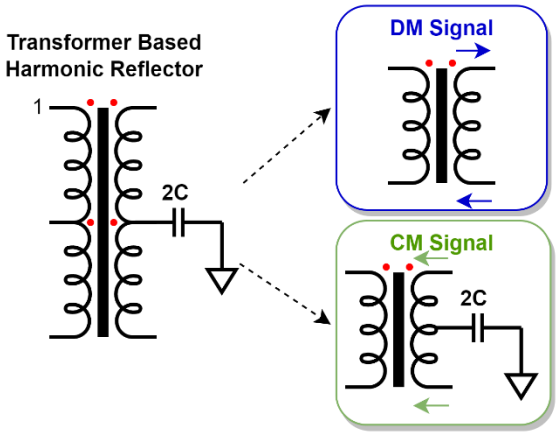

Figure 4.1 Proposed transformer-based harmonic reflector (a) and equivalent circuit for (b) differential-mode and (c) common-mode signals.

The quadrupler input connects through a transmission line to the input pads. An intentional offset between the primary and secondary transformer windings is incorporated to regulate their coupling factor and extend the overall bandwidth available for our automotive application as seen in Fig. 4.1.

In terms of specific transformer details, the first transformer features a differential secondary inductance of 663 pH and a common-mode inductance of 60 pH. Meanwhile, the second transformer has a differential secondary inductance of 360 pH and a common-mode inductance of 28 pH. Both transformers utilize a step-up configuration to amplify the effective voltage swing driving the gates of the push-push doublers. It's noteworthy that the first doubler is designed to approach the saturation level of the succeeding doubler. While this choice may slightly reduce peak power efficiency, it ensures a consistent quadrupler output power across a broader bandwidth.

The output matching network employs a transformer with single-turn inductors, and notably, no additional power amplification is introduced to achieve the desired 0 dBm output power through the targeted bandwith. This strategic combination of transformer-based techniques and design choices results in a robust and efficient frequency quadrupler architecture that could multiply the frequency of the outout of the oscillator as to operate in automotive application without any significant concern. The overall schematic representation of the quadrupler block diagram and schematic representation are presented in Fig. 4.2 and Fig. 4.3.

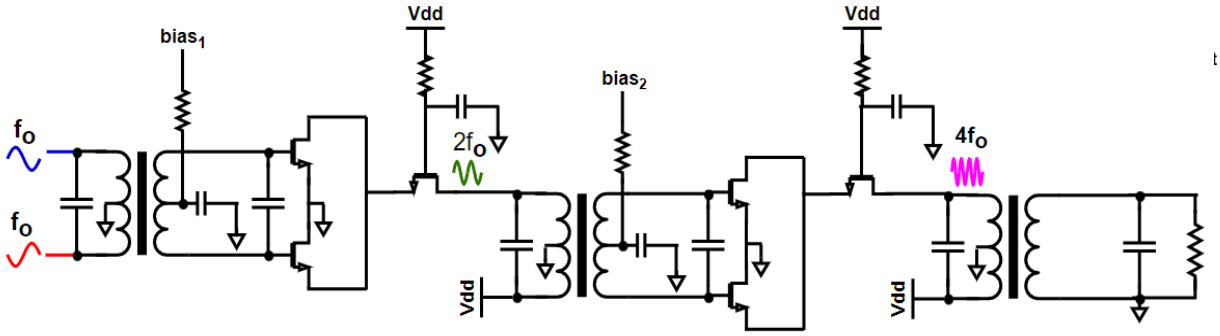

Figure 4.2 Block Diagram of Quadrupler.

Figure 4.3 Complete Schematic Representation of the Quadrupler.

4.4 Enhanced Buffering for Seamless Integration with 80GHz Output

The cascode buffer serves as a critical interface between the Digitally Controlled Oscillator (DCO) and the multiplier, ensuring their separation and minimizing signal interference. Its primary purpose is to provide a robust and stable signal to the multiplier, driving it towards saturation to maximize its efficiency. The adopted topology effectively utilizes a cascode common-source amplifier architecture, as illustrated in the accompanying schematic.

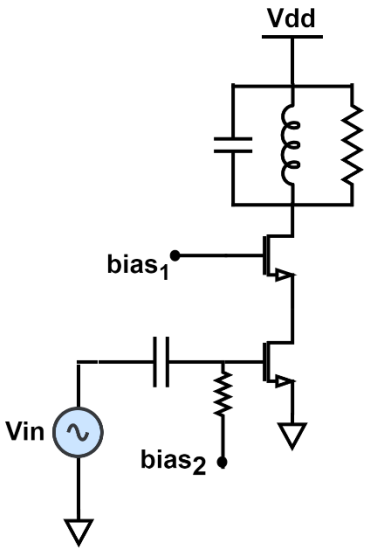

Figure 4.4 Single-ended cascode buffer.

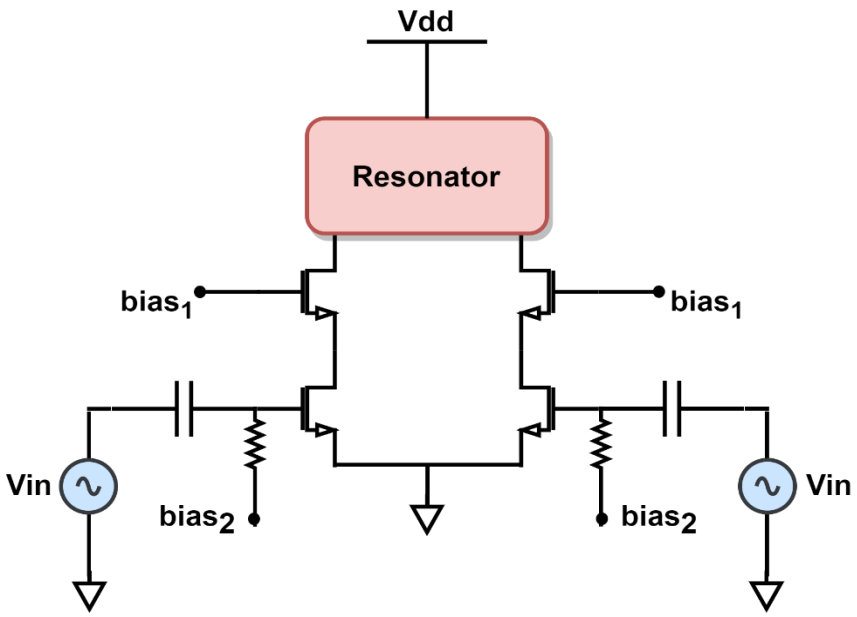

Figure 4.5 Differential cascode buffer.

In the single-ended implementation, C1 serves as a DC blocking capacitor for signal coupling, while Rb acts as a sizable base resistor. The circuit integrates both a common-source amplifier and a common-gate stage. Owing to the large input signal voltage, various harmonic components arise at the output. To address this issue, a resonant load element is incorporated to selectively extract the desired harmonic. Recognizing that the oscillator output is a differential signal, an equivalent design approach is adopted for the differential configuration.

The buffer circuit is meticulously designed with the following parameters, as depicted in Fig. 4.5. A nominal supply voltage (VDD) of 1.2 V is employed, while the bias voltages (bias1 and bias2) are precisely set at 1.2 V and 0.6 V, respectively. The circuit is tailored to operate with a controlled drain current (IDC) of 10 mA, yielding a measured power dissipation (PDC) of 12 mW. Transistors M1, M2, M3, and M4 are carefully selected with dimensions of 1 μm x 18 fingers each to ensure efficient signal amplification. A DC blocking capacitor (C1) is incorporated to suppress interference, and biasing is accomplished using a precision 10 kΩ resistor (Rb). The input signal (Vin) exhibits a peak-to-peak amplitude of 400 mV at a frequency of 20 GHz.

This comprehensive configuration establishes proper biasing conditions and operational parameters for the buffer circuit, enabling it to effectively fulfill its intended purpose within the specified electrical environment. For the input voltage level Vin, a peak value of 400 mV is chosen to represent the worst-case scenario at the oscillator output. The transistor sizes are carefully selected based on the necessary current required to achieve the desired voltage drop across the output resistor. The buffer circuit is subsequently fine-tuned to achieve optimal matching with the input of the quadrupler, ensuring seamless integration and enhanced performance of the overall circuit configuration, as illustrated in Fig. 4.6.

In the depicted Fig 4.6, the core oscillator's output from the quad core is prominently featured. These outputs are strategically interfaced with the input of the buffer, where amplification is employed to propel the signal towards the multiplier. To ensure uniformity and prevent any potential mismatch, the remaining three cores are seamlessly linked to auxiliary buffers.

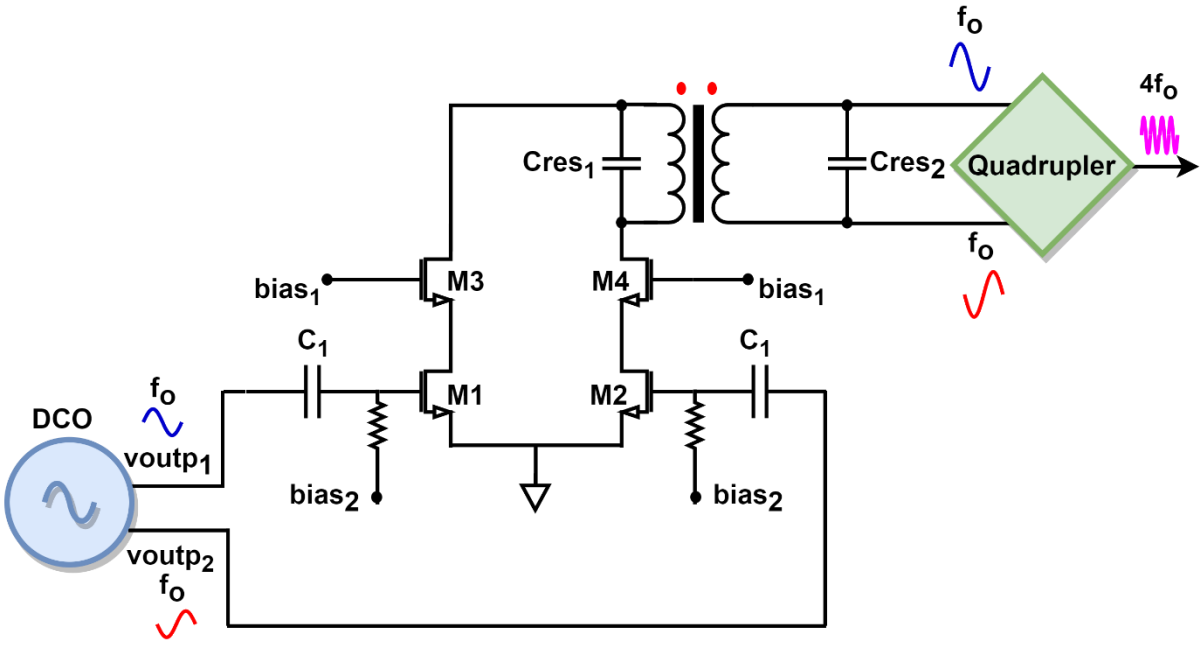

Figure 4.6 Cascode Buffer Final Representation.

4.5 Test Chip and Measurements

In this section, we present a comprehensive overview of our measurement results, accompanied by a microphotograph of the chip, captured using a high-resolution microscope. The photograph reveals a compact overall area of 1 mm x 1 mm, accommodating six distinct functional blocks. The centrally located Digitally Controlled Oscillator (DCO) serves as the heart of the circuit. Each DCO output is carefully connected to a dedicated buffer amplifier, ensuring signal integrity. One output is designated for standalone oscillator testing, while another is linked to the quadrupler, enabling the evaluation of the entire frequency multiplication chain. The chip's bottom and top sides are equipped with pads that serve dual purposes: biasing the transistors and providing power supply connections. The schematic representation of the overall implementation and the microchip photograph are provided below for detailed reference.

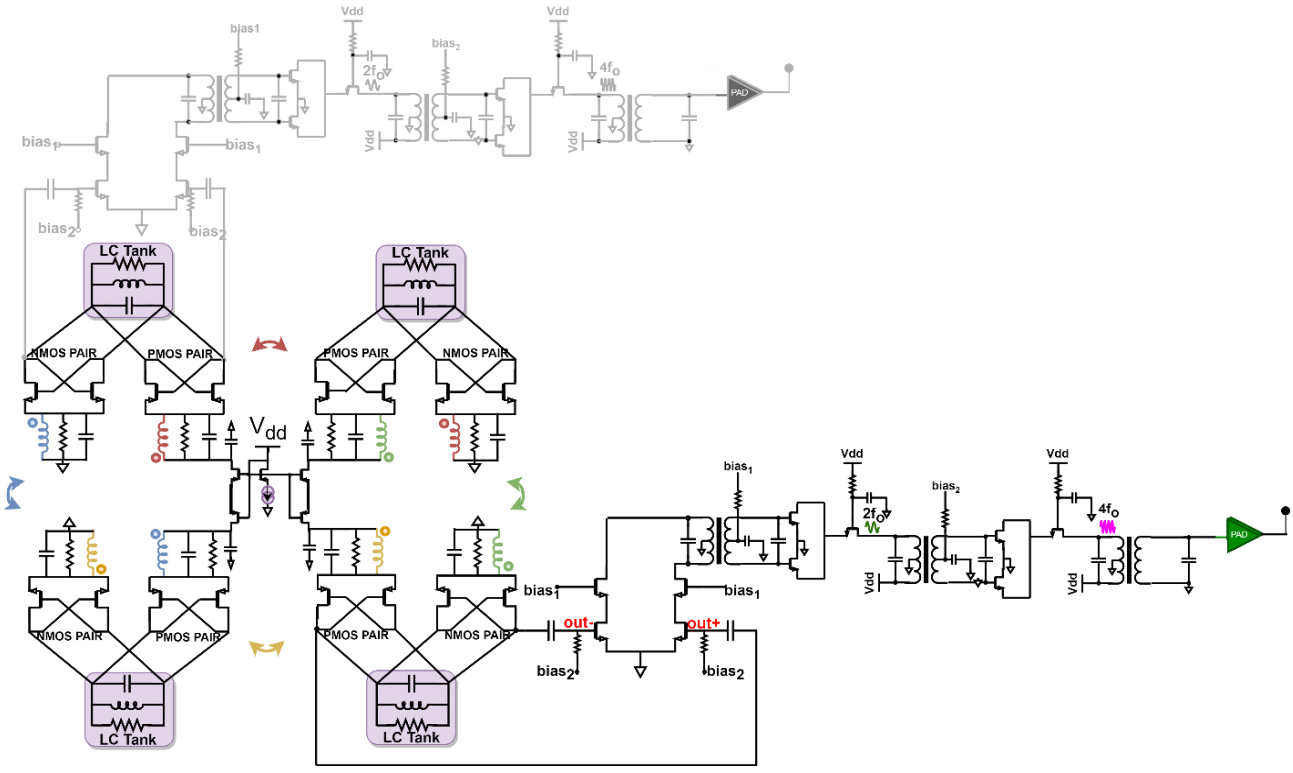

Figure 4.7 Final Schematic Implementation.

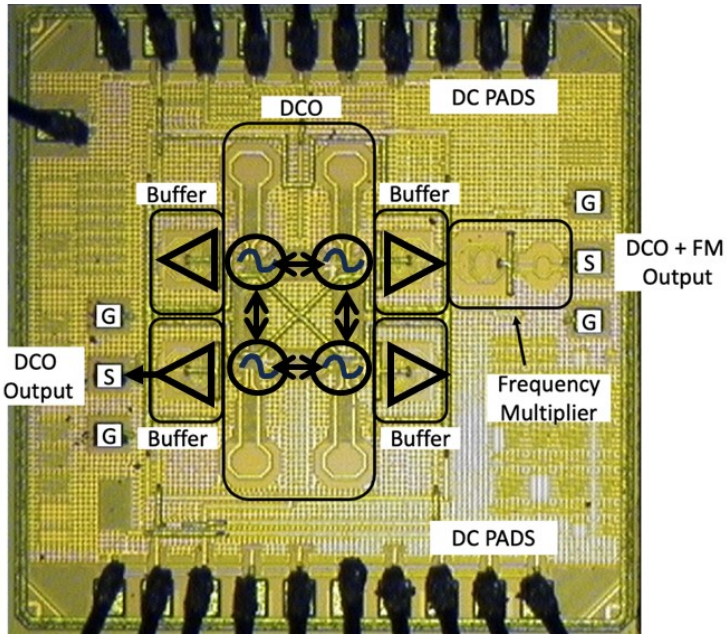

Figure 4.8 Final Chip Microphotograph.

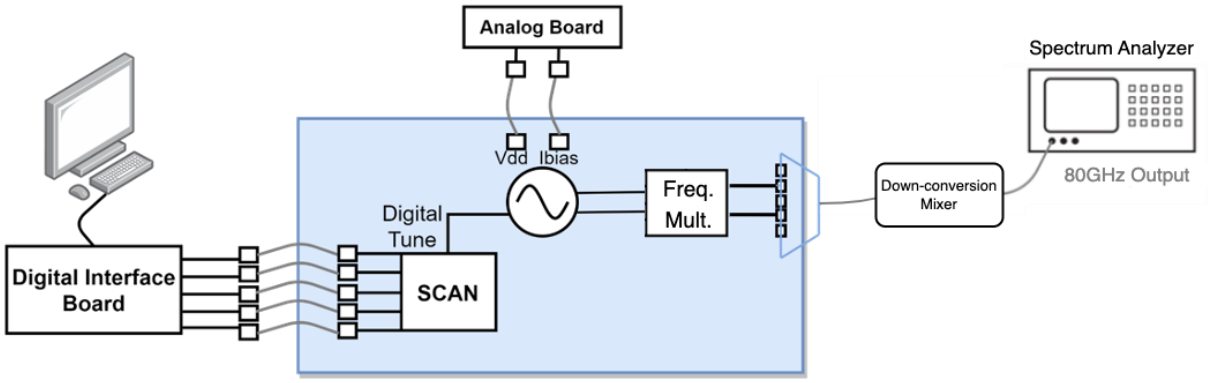

Figure 4.9 Measurement setup for DCO and Frequency Quadrupler.

To provide clarity on our methodology for phase noise measurements at the multiplier output, we present an illustrative depiction of the measurement setup. The experimental setup comprises several integral components: a digital interface facilitating bit programming and oscillator frequency adjustment, DC and RF boards responsible for supplying necessary bias and power to the chip, and a down-conversion

mixer tasked with lowering the output signal frequency for compatibility with Spectrum Analyzer measurements. The Spectrum Analyzer, the final component, is instrumental in visualizing the spectrum and phase noise of the output signal.

For frequency measurements, a harmonic down-conversion mixer was employed, while a fundamental mixer with a maximum frequency of 75 GHz was utilized for phase noise measurements. Notably, the oscillator's output, prior to the frequency quadrupler, is directly accessible through an on-chip buffer, which, in turn, drives the RF probes. Remarkably, this setup obviates the need for off-chip mixers or buffers when analyzing the spectrum as seen in Fig 4.9.

The oscillator's tuning range is presented in the accompanying plot, with the x-axis representing the oscillator frequency and the y-axis representing the corresponding frequency at the quadrupler's output. The desired frequency range of 76-81 GHz is comprehensively covered, achieving an overall tuning range of approximately 16 GHz. This substantial margin beyond the required 5 GHz range indicates the potential for performance improvement by reducing the overall PVT tuning capacitance bank, which would increase the minimum frequency and minimize losses at higher frequencies.

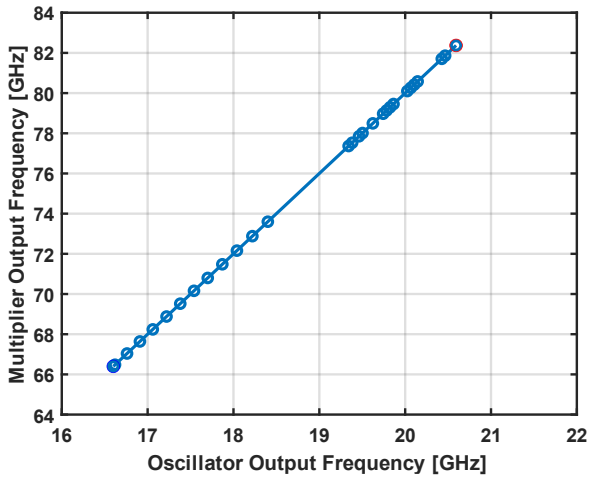

Figure 4.10 Oscillator tuning range.

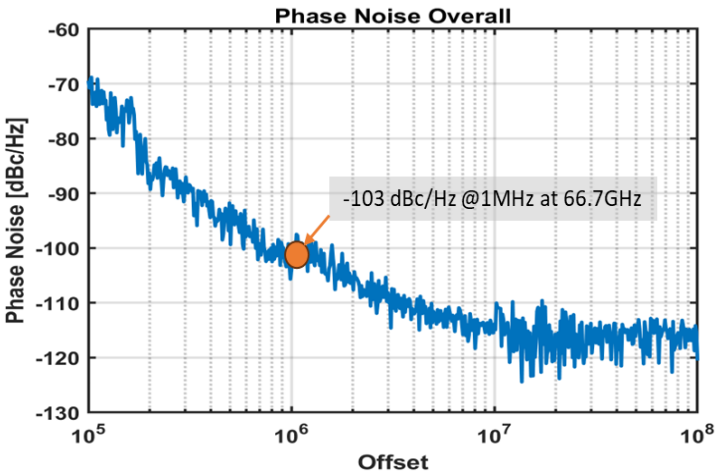

Figure 4.11 Phase Noise at the output of the multiplier.

Furthermore, Fig. 4.11 illustrates the phase noise performance at the quadrupler's output, assuming a 16.7 GHz oscillator carrier frequency (corresponding to 66.7 GHz at the quadrupler's output). This figure provides a comprehensive overview of the phase noise characteristics under these conditions.

Due to limitations imposed by the mixer in our measurement setup, we were only able to evaluate the phase noise at the multiplier output within the 67-75 GHz frequency range. The observed phase noise at a 1 MHz offset from the carrier exhibits a slight variation, ranging from -103.6 dBc/Hz at 67 GHz to -102.15 dBc/Hz at 75 GHz. As seen in Fig. 4.12, based on the oscillator's phase noise measurements, a consistent phase noise range is expected at higher frequencies. Figure 4.13 clearly compares our simulations to the actual results, revealing a minimal and insignificant discrepancy. This close correspondence between simulated and observed data confirms the accuracy and reliability of our modeling and simulation procedures. This consistency further reinforces the validity of our findings, demonstrating the robustness and effectiveness of our implemented approach.

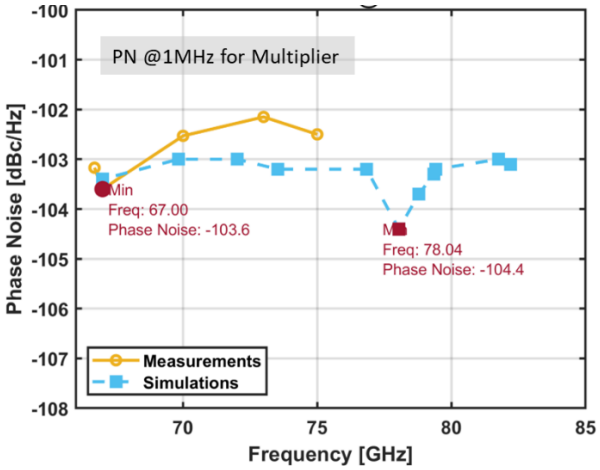

Figure 4.12 Phase noise measurements at the multiplier output as a function of the output frequency.

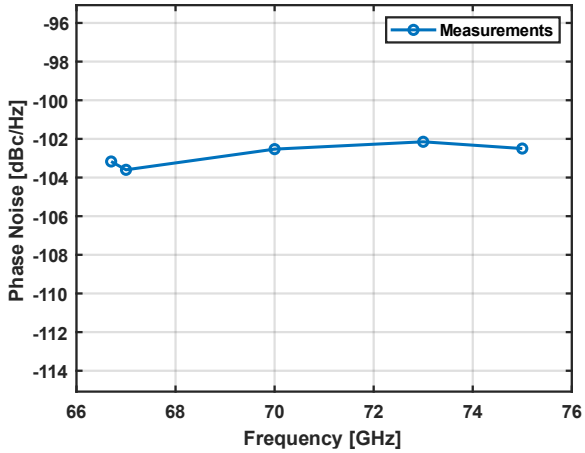

Figure 4.13 Measured Phase Noise at the multiplier output as a function of the output frequency.

The output power at the quadrupler's output was comprehensively evaluated across the frequency range of 70-82 GHz. The accompanying figure presents a detailed comparison between the measured output power and simulated values. A notable observation is the relatively constant simulated output power over the entire frequency spectrum. In contrast, the measured output exhibits a slight downward shift in peak power. This discrepancy is likely due to variations in the input signal swing at the multiplier's input. Nevertheless, it is noteworthy that the measured output power remains within a 2 dB range of the targeted 0 dBm throughout the designated bandwidth (76-81 GHz), as evident in Fig. 4.14.

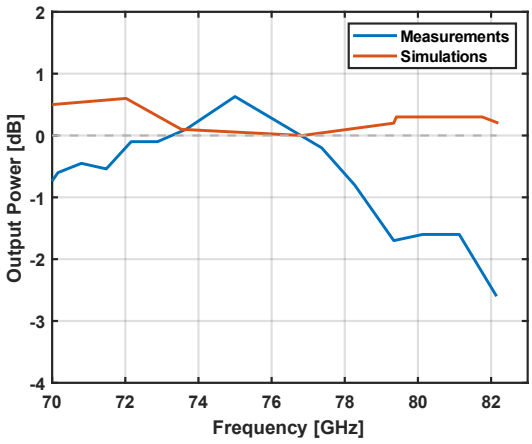

Figure 4.14 Measured vs Simulated Output Power at the multiplier output as a function of the output frequency.

To comprehensively evaluate the performance and advancements achieved in the proposed circuit, a comparative analysis is presented against state-of-the-art designs. The following table serves as a concise summary, providing a systematic breakdown of key metrics across various parameters. This assessment aims to highlight the distinctive features, improvements, and innovations incorporated in our design compared to existing benchmarks in the field. When evaluating noise performance at frequencies more than 1 MHz away, the noise observed is primarily attributed to the proposed circuit, not the locking source. If it were sourced from the locking source, the noise levels would be significantly lower. Therefore, to ensure a fair and accurate comparison, we focus on a standard 3 MHz offset in the noise performance comparison with the best-known designs.

	This Work	[49]	[52]	[53]	[54]	[55]
Technology	CMOS 28nm	CMOS 28nm	CMOS 28nm	CMOS 28nm	CMOS 40nm	CMOS 55nm
Center Frequency [GHz]	76	78	66.88	60	57.8	77.3
TR [%]	16	12	15.6	16	25.4	3.25
Pdc [mW]	58	36	22	37	22	15.1
PN@3MHz	-109.4	-111	-106.7	-99.7	-109.4	-102
Pout[dBm]	0	-4	1	-23	0	-1.12
FoM [dBc/Hz]	-184	-183.6	-179	-171	-182	-166

Table 4-1 Table Performance Summary and Comparison with the State-of-the-art.

As we present the table summarizing the final performance metrics across the three tapeouts, it's important to emphasize the iterative design and optimization processes that have contributed to these results. The following table provides a comprehensive overview, highlighting the notable advancements and outcomes achieved through multiple rounds of refinement and adjustment. This demonstrates the continuous improvement and evolution of the circuit design throughout its development stages.

	DCO Test Chip 1	DCO Test Chip 2	DCO Test Chip 3 with MULTIPLIER	Target
Frequency Range [GHz]	N/A	N/A	70 -82	76-81
Frequency Range DCO [GHz]	14.5-17.9	16.82 – 20.8	16.6 – 20.6	19-20.25
Power Dissipation [mW]	22.1	24	58	<80
Output Power [dBm]	N/A	N/A	0 /-2	0
PN @ 1MHz [dBc/Hz]	N/A	N/A	-103.6/-102.5	-103
PN @ 1MHz (DCO) [dBc/Hz]	-114.3/-117.3	-110/-114.4	-115.5 /-113.5	-115
Frequency Step (DCO) [kHz]	10^4	625	540	500
Linearity Error [kHz]	+/- 240 @ 16GHz	N/A	<1.2x10 @80GHz	$5x10^3$@80GHz

Table 4-2 Table Overall Performance Summary.

4.5 Conclusion

In conclusion, this section has provided a comprehensive examination of the frequency quadrupler, including the experimental setup, phase noise measurements, and output power characteristics. Despite limitations in fully characterizing the phase noise at higher frequencies, the results demonstrate consistent performance across the measured range. The analysis of the output power indicates a subtle downward shift in peak power, attributed to input signal variations. Nonetheless, the measured power remains within a 2 dB range of the targeted value. Furthermore, the chip's

microphotograph reveals a compact design with well-defined functional blocks. The cascode buffer was optimized to achieve seamless integration with the quadrupler, as evident in the detailed parameters presented in the dedicated table. Overall, this phase of the study provides valuable insights into the behavior and performance of the frequency quadrupler and its associated components.

Conclusions

FMCW radars play a crucial role in various fields due to their ability to provide accurate range, velocity, and direction measurements. These radars are particularly important in automotive safety systems, surveillance, and environmental monitoring applications. Their continuous wave modulation enables precise distance measurements, making them indispensable in scenarios where accurate object detection and tracking are paramount. Furthermore, the development of CMOS/BiCMOS integrated transceivers for mmWave applications offers the potential to significantly reduce equipment costs and physical footprint.

This dissertation delved into LO generation requirements for E-Band radar applications. It outlined phase-noise specifications for the frequency synthesizer and explored strategies to reduce phase noise, particularly focusing on inductor shrinking. A detailed examination of the multi-core approach was conducted, analyzing different coupling techniques and their impact on system performance, considering mismatches and design trade-offs. Test-chips were fabricated, featuring a 20 GHz 4-core class-B DCO in 28nm CMOS technology. Measurement results revealed impressive phase noise performance of -115.5 dBc/Hz at 1MHz offset, with a power consumption of 24mW and a tuning range of 18%. Additionally, the addition of the multiplier demonstrated 0dB power at the output and state-of-the-art phase noise performance across the band of interes, making the DCO design compatible with the latest generation of FMCW radar applications.

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