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DEPARTMENT OF ELECTRICAL, COMPUTER AND BIOMEDICAL ENGINEERING

PH.D. THESIS IN MICROELECTRONICS
XXXVI CYCLE

Low-Noise Amplifiers and Phase Shifters
in SiGe BiCMOS for D-Band RX Front-Ends

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"I think it's very important to have a feedback loop, where you're constantly thinking about what you've done and how you could be doing it better."

Elon Musk

Abstract

The ever-increasing demand for faster data transfer-rate and higher device density in mobile applications is posing severe requirements to the network infrastructure for 5G and beyond networks. Concurrently, radar imaging is a trending topic, mainly driven by assisted/autonomous driving and gesture recognition applications. Both wireless communication and remote sensing are going towards millimeter-waves and sub-THz bands, where unlicensed portions of the electromagnetic spectrum are largely available and wide bandwidth is easily accessible.

Within this framework, BiCMOS is a promising technology, offering both high-speed high-power HBTs and CMOS nodes, enabling the possibility to realize complex systems on chip capable of going directly from the digital domain to the air and vice-versa. Nonetheless, today's available nodes still suffer from a maximum oscillation frequency which is only twice or three times the operating frequency; this mandates a careful selection of circuits configurations and, possibly, the investigation of unconventional design solutions to get the most out of the technology.

Phased-arrays have the benefit of increasing the total radiated power through beamforming and over-the-air-power combining, thus going beyond the power capability of a single-transistor transmitter, which is very limited compared to the one achieved in III-V technologies. On the receiver side, in-

stead, they combine multiple channels giving a signal-to-noise ratio increase, thus enhancing the system sensitivity. For this reason, arrays with thousands of antennas are likely to become popular in the next future, and a high integration is required to make these systems affordable and reliable. Moreover, phased-arrays also open to the possibility of beam-steering, increasing the flexibility of point-to-point radio links.

This thesis focuses on D-band (110 - 175 GHz) building blocks for a receiver front-end. A description of transmission-line-based broadband matching networks is proposed to gain some insights about their working principle and it is applied to the design of high-frequency wideband amplifiers. A test chip demonstrates a LNA with 50% fractional bandwidth in D-band and state-of-the-art noise figure. A discussion on gain boosting based on reactive feedback applied to common-emitter devices follows, and a low-noise amplifier demonstrates $23.8\,\mathrm{dB}$ power gain, $130 - 165$ GHz bandwidth and $5\,\mathrm{dB}$ noise figure at $150\,\mathrm{GHz}$, a record value which is found in literature only in works that operate with more advanced technology nodes. Phase shifters, needed to perform a coherent summation of the signals at different antenna elements, are investigated in their passive implementation both for fine and coarse phase shift control. Stand-alone structures are realized together with an on-chip TRL calibration kit to validate the concepts. Finally, a front-end module comprising a LNA and a passive phase shifter is described. Phase shifting elements are interleaved with gain-boosted active stages to maximize the receiver's dynamic range. Experimental results show an average gain of $20\,\mathrm{dB}$ and a phase resolution of $7°$ over the full $0 - 360°$ phase shifting range. The average noise figure is $7\,\mathrm{dB}$, the best to the authors' knowledge in similar works to date. With an $\mathrm{OP_{1dB}}$ of $-2\,\mathrm{dBm}$ and a DC power consumption of $80\,\mathrm{mW}$ from a 2V supply, measurement results prove advances in perfor-

mance with respect to previous works, especially in terms of power efficiency, particularly critical in large arrays.

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Introduction

Figure 1: Network infrastructure with D-band backhaul links.

T HE ever-increasing demand for faster transfer rate in mobile applications and ubiquitous connectivity are posing severe requirements to the mobile network infrastructure. To address this challenge, millimeter-wave (mmWave) and sub-THz bands are progressively gaining interest in the recent years, enabling high data-rate wireless communications, competitive with fiber solutions, and are ideal for the creation of flexible and high-capacity point-to-point backhaul links aimed at connecting the cells at the edges of the network to the network core and for the interconnection of adjacent cells.

The main regulatory entities of both US and Europe have deeply analyzed the potential of the bands within $115 \sim 275$ GHz, especially for short-reach point-to-point radio backhaul links [1][2][3] and D-band, ranging from 110 GHz to 170 GHz, covers a promising spectrum portion, thanks to the favorable oxygen attenuation and the wide bandwidth available, but the lack of standardization and the uncertainty about business opportunities in the field is still leaving this matter to a research level, with the first working demonstrators being presented just in the past few years [4][5][6]. Nonetheless, significant spectrum portions have been already reserved in D-band for point-to-point short-reach radio links in 5G and beyond [7].

Also human vital sign monitoring via radar sensing and imaging are pushing the evolution towards mmWave, driven by the advantage on resolution provided by the short wavelength and the wide bandwidth, allowing to achieve high accuracy in distance measurements, in the order of micrometers [8][9]. Gesture recognition with radar sensors is another trending topic, and a high range resolution (the ability to distinguish between adjacent targets) is required to detect even the most delicate movements of fingers and hands [10].

For all such kind of applications, BiCMOS technology gives an optimal compromise between cost and performance, joining high-speed and high-power HBTs with CMOS nodes, thus empowering the integration of systems on chip (SoC) in the Sub-THz band. Nonetheless, in most of the current technologies, transistors are pushed to operate close to their frequency limit (f_{max}). Fig. 2 reports in red the SiGe BiCMOS technologies available versus f_t and f_{max}, which are only twice and three times the operating frequency in D-band [7]. This implies limited performance and a high effort in the design. In fact, the low available gain mandates careful selection of the active stage

configurations and, possibly, investigation of unconventional design solutions to get the most out of the technology. The main challenge is the ability
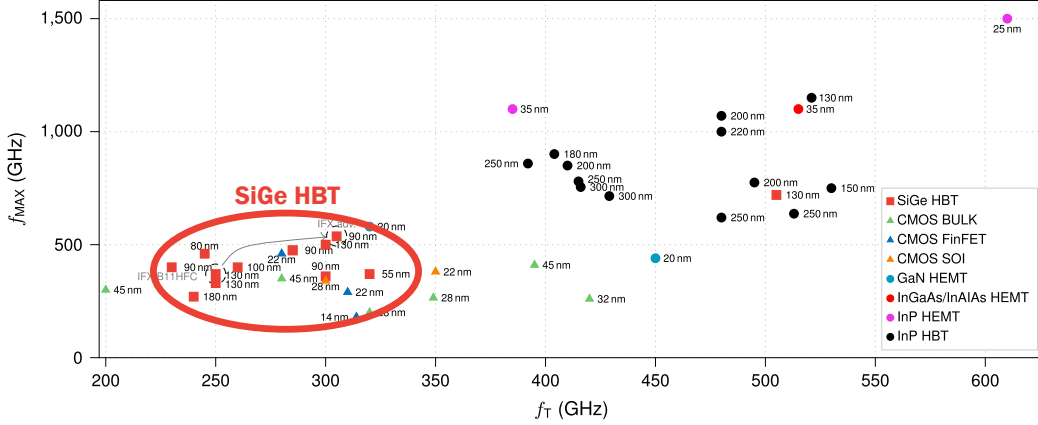
Figure 2: f_t and f_{max} of most of today's available technology nodes

to provide enough amplification over the required bandwidth. In fact, for D-band circuits to operate in real-world applications, gain-bandwidth products in the order of several hundreds of GHz are essential [11][12].

To cope with the high path loss, transceivers exploit phased-array architectures, where multiple radiating elements rise the equivalent antenna gain through beam forming. In active beam forming systems [13][14][15], the radiating elements are connected to multiple Power Amplifiers (PA) or low-noise amplifiers (LNA) at the TX and RX side, respectively, followed by a programmable phase shifter. In this way, the system performance is enhanced by a higher radiated power and a better sensitivity. Moreover, active phased-arrays benefit from the flexibility given by the programmable beam-steering capability [16]. In this scenario, each antenna element of a phased-array needs to be operated with a specific phase shift, in order to perform a coherent summation of the different signals coming from or delivered to each antenna element.

This work is organized as follows: chapter 1 faces the issue of broadband amplification focusing on the implementation of ultra-wideband matching networks for the realization of high-frequency broadband amplifiers. Follows chapter 2 that analyzes the limitation of available power gain in high-frequency cascode amplifiers and introduces reactive feedback around the common-emitter device to increase the power gain. Chapter 3 focuses on passive structures to realize digital fine and coarse phase shifters. Finally, chapter 4 makes use of the previously illustrated components and describes the design of a receiver front-end with a two-stage LNA with reactive feedback and passive phase shifters interleaved with gain-boosted active stages for D-band phased arrays.

Chapter 1

Broadband Amplifiers
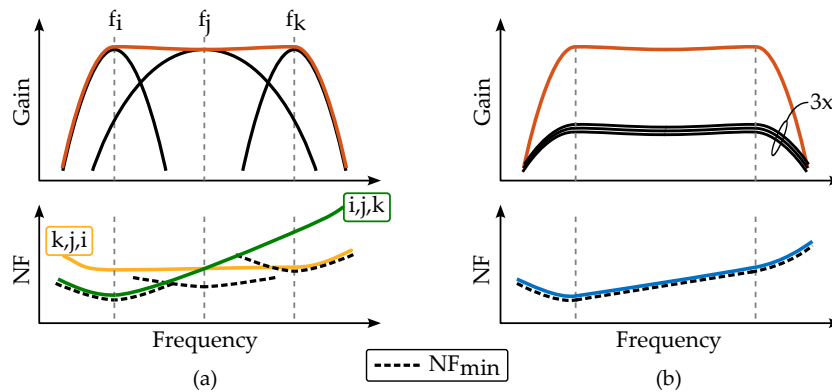
Figure 1.1: Qualitative gain response (upper) and NF (lower) for a three-stage amplifier with stagger-tuning (a) and inherently broadband design (b).

A MPLIFIERS are key building blocks in phased-array systems, but the high operating frequency, close to the technology limits (f_t / f_{max}), complicates the design and penalizes the performance. Distributed amplifiers [17] have been deeply explored for high-frequency wideband amplification since the vacuum-tube era, but lead to large area, poor power efficiency and high noise figure [18], making them hardly attractive

for low power and compact applications, such as phased-arrays, where the spacing between antenna elements must be equal to half wavelength ($\approx$ 1mm in D-band).

A common way to extend the amplifiers bandwidth is the stagger-tuning technique where multiple tuned stages are cascaded with center frequencies purposefully misaligned such that the overall response appears broader [12][19][20][21]. When a high fractional bandwidth is needed, several staggered stages are required but, notably, the stage ordering is arbitrary, i.e. the stage tuned at the lowest frequency does not need to be necessarily the first stage in the chain. In [21], a three-stage amplifier is designed, and the authors place the middle frequency first, observing that this gives a flat NF profile. In fact, an impact of stage ordering on the overall amplifier performance, such as linearity and noise figure [22], exists. Fig. 1.1a depicts qualitatively this issue. The stages are characterized by center frequencies $f_{i,j,k}$. While the overall gain is independent on the stage ordering, the green and yellow curves report the overall noise figure for two different cases: lowest frequency first (i,j,k), and highest frequency first (k,j,i). Indeed, by departing from the center frequency of the first stage, the gain drops until it may be no more sufficient to suppress the noise of the subsequent stages. This determines a signal-to-noise ratio degradation in the portions of the bandwidth far from the center frequency of the first stage.

In this work, the amplifiers are inherently broadband stages, as depicted in Fig. 1.1b, such that the noise figure is minimized across all the band. The active cores are cascode stages loaded by high-order matching networks realized with transmission lines.

A three-stage LNA is designed and a test chip fabricated in SiGe BiCMOS to validate the concept. Experimental results demonstrate 23 dB gain from

105 GHz to 175 GHz with 30 mA current consumption from a 2V supply. The corresponding fractional bandwidth is more than 50%, to the authors' knowledge the highest reported in literature for a 3-stage amplifier. Only [23] outperforms with a remarkably higher value of 77%, but the design comprises five active stages and benefits from a technology node with a substantially higher f_t/f_{max}. The measured noise figure (NF), between 5 dB and 6.5 dB, was demonstrated so far only by narrow-band designs.

1.1 Ultra-wideband Matching Networks
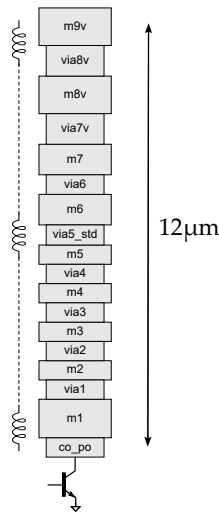
Figure 1.2: Section (not in scale) of the stackup and parasitic inductance.

Cascode structures are commonly employed in multi-stage amplifiers. At high frequency, the cascode shows a relatively low input impedance but high output impedance, requiring impedance match to rise the gain of cascaded stages. While providing impedance scaling, the interstage network has also to feed the supply and the bias voltage to the AC-coupled stages. Moreover, in the sub-THz region, even the shortest interconnection between a transis-
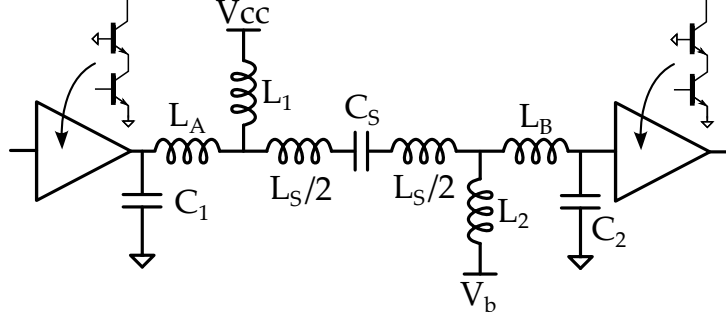
Figure 1.3: Topology of the matching network employed

tor terminal and the topmost low-loss metal layer introduces a non-negligible reactance. The issue is sketched in Fig. 1.2, that shows the inductive path between the transistor's collector and the 9th layer of the BEOL stack. The parasitic inductance should be properly absorbed by the interstage network, and the topology chosen for this work is drawn in Fig. 1.3. L_A and L_B embed the connection to the collector of the driving stage and to the base of the following stage. Capacitors $C_{1,2}$ model the output/input parasitic capacitance of the HBTs. $L_{1,2}$ provide two convenient paths to the supply (V_{CC}) and biasing (V_b) voltage. Capacitor C_S grants the necessary AC coupling and the two $L_S/2$ segments incorporate its connections.

A rigorous study of the network in Fig. 1.3, in order to exploit all the available design degrees of freedom, is cumbersome. Insights on components sizing and how they affect the frequency response are analyzed here following an intuitive approach to identify the network singularities and drive the design.

1.1.1 Region Around $L_S C_S$ Resonance

From Fig. 1.3, the two inductors $L_S/2$ can be concentrated into a single component, L_S, as shown in Fig. 1.4a. For frequencies around $\omega_s = 1/\sqrt{L_s C_s}$, the

series tank constituted by L_S and C_S resonates, giving ideally an AC short-circuit and leading to the simplified network of Fig. 1.4b, where $L_C = L_1 // L_2$. Since the T-structure of L_A, L_B, L_C can be described by two magnetically-
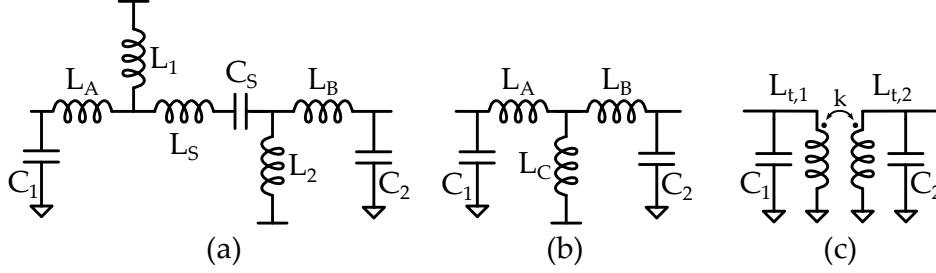
Figure 1.4: Matching network rearranged (a), its simplification around ω_S (b), and equivalent circuit with a doubly-tuned transformer (c).

coupled inductors, the network is analytically equivalent to a doubly-tuned transformer with primary and secondary inductance $L_{t,1}$ and $L_{t,2}$, respectively, and magnetic coupling k, as in Fig. 1.4c. The relations between the parameters of the networks in Fig. 1.4b and Fig.1.4c are:

$$L_{t,1} = L_A + L_C \qquad L_{t,2} = L_B + L_C$$
$$k = \frac{L_C}{\sqrt{(L_A + L_C)(L_B + L_C)}} \tag{1.1}$$

Transformers are well known for their capability of providing broadband impedance match, and this equivalence is exploited to describe the behavior of the network of Fig. 1.3. In [24], a deep study on doubly-tuned transformers was carried out. Considering Z_{in}, the impedance synthesized at the primary side, two pairs of complex-conjugate poles appear. Under the simplifying assumption that $L_{t,1}C_1 = L_{t,2}C_2 = 1/\omega_0{}^2$, their frequencies are given by:

$$\omega_{p1,2} = \frac{\omega_0}{\sqrt{1 \pm |k|}} \tag{1.2}$$

In addition, a pair of in-band complex zeroes appear. By properly setting the impedance transformation at these three frequencies, it is possible to achieve a broadband behavior.

When a step-up impedance match is required (which is the case of practical interest), given a bandwidth requirement, the capacitance C_1 limits the maximum amount of impedance transformation, i.e. a higher gain can be realized only on a reduced bandwidth [24]. In the case of $C_1 = 40\,\text{fF}$, Fig. 1.5 shows Z_{in} of the doubly-tuned transformer with $50\,\Omega$ load and a 1:2 impedance transformation ratio ($C_2 = 80\,\text{fF}$ and $L_{\text{t,1}} = 30\text{pH}$, $L_{\text{t,2}} = 15\text{pH}$, $k = 0.28$, implemented with $L_A = 24\,\text{pH}$, $L_B = 9\,\text{pH}$, $L_C = 6\,\text{pH}$).
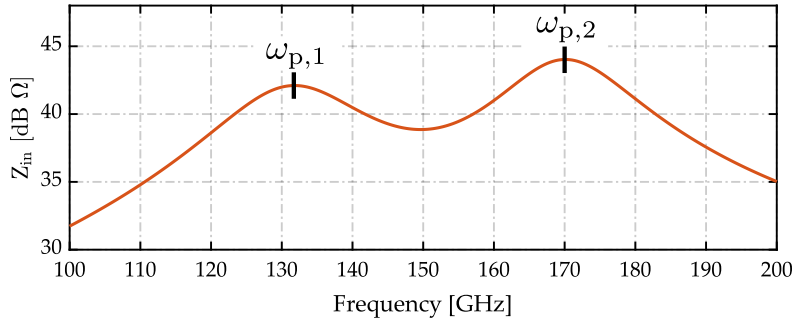
Figure 1.5: Z_{in} synthesized by the doubly-tuned transformer

1.1.2   Region Far From $L_S C_S$ Resonance

The presence of capacitor C_S and inductor L_S introduces additional singularities to the network. Regarding the zeroes on the input impedance, they can be identified by circuit inspection, noticing that a frequency exists at which the components L_1, L_S, C_S, L_2, L_B and C_2 present a capacitive impedance with reactance equal and opposite in sign to the one of L_A, thus determining a series resonance. For this reason, C_1 plays no role in these additional zeroes. The analytical expression of such singularities appears cumbersome and

hardly intuitive, but it can be simplified assuming the resonance between C_2 and L_B falls at frequency sufficiently high, a condition met in practice. With this assumption, L_B is floating and the following approximated expression is found:

$$\omega_{z,s} = \sqrt{\frac{1}{C_S \left[L_2 + L_S + (L_A \mathbin{//} L_1) \right]}} = \sqrt{\frac{1}{C_S L_{eq,z}}} \qquad (1.3)$$

The term within square brackets at the denominator of (3) is an equivalent inductance, $L_{eq,z}$. Interestingly, (1.3) can be compared with (1.2). Replacing (1.1), (1.2) can be rewritten as:

$$\omega_{p1,2} = \sqrt{\frac{1}{C_1 \left[(L_A + L_C) \left(1 \pm \frac{L_C}{\sqrt{(L_A+L_C)(L_B+L_C)}} \right) \right]}} \qquad (1.4)$$

Again, the inductive term at the denominator of (1.4) may be called $L_{eq,p1}$ and $L_{eq,p2}$ with the plus and minus sign, respectively, giving:

$$\omega_{p1,2} = \sqrt{\frac{1}{C_1 L_{eq,p1,2}}} \qquad (1.5)$$

It is evident that the additional zeroes introduced by C_S, with proper components sizing, may fall below $\omega_{p,1}$ or above $\omega_{p,2}$, thus determining bandwidth extension. For this to happen:

$$C_S > C_1 \frac{L_{eq,p1}}{L_{eq,z}} \quad \text{or} \quad C_S < C_1 \frac{L_{eq,p2}}{L_{eq,z}} \qquad (1.6)$$

Fig. 1.6 reports the frequency response of Z_{in} (red curve) when L_S and C_S resonate at 177 GHz, while the additional zeroes fall below $\omega_{p,1}$. The value of $C_S = 50$ fF is set considering practical implementation issues of such a floating MOM capacitor; going towards higher values would introduce non-negligible parasitic capacitance to ground, impairing the desired performance. L_S is set, according to (1.5), to 16 pH.

A further degree of freedom not yet considered exists: only the value of $L_1 \mathbin{//} L_2$ has been set equal to L_C, and their ratio can be expressed as
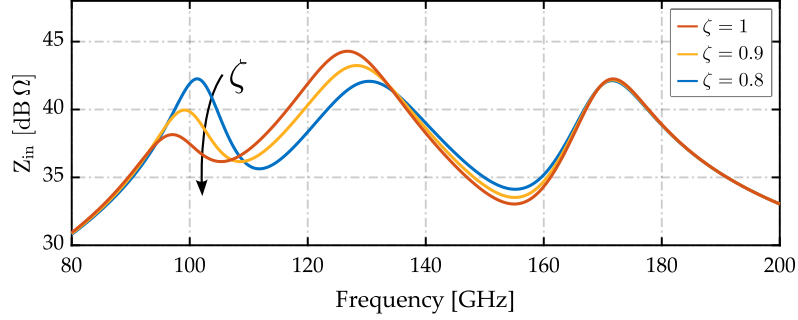
Figure 1.6: Z_{in} synthesized by the network of Fig. 1.3. The impact of reducing values of ζ is reported.

$\zeta = L_2/L_1$. Interestingly, ζ controls the impedance transformation ratio in the bandwidth-extended region, with a negligible impact on the position of the singularities. To gain insight, Fig. 1.6 reports Z_{in} at different ζ values. While the frequencies of the singularities (hence the overall bandwidth) are marginally affected, it is possible to equalize the synthesized input impedance at the poles frequencies ($\zeta=0.8$ gives the same Z_{in} at the three peaks).
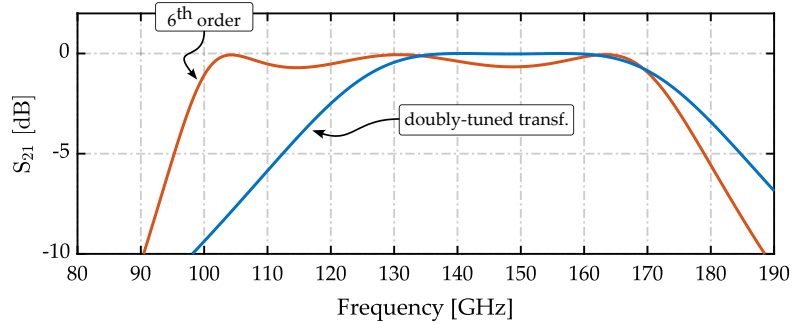
Figure 1.7: S_{21} of a doubly-tuned transformer (blue) and of the network of Fig. 1.3 with a 1:2 impedance transformation (50 Ω load).

The performance of the sixth-order matching network is finally compared (in terms of S_{21}) to the doubly-tuned transformer that gives the input impedance plotted in Fig. 1.5. The simulated S_{21} are plotted in Fig. 1.7.

Despite an increased in-band ripple ($< 1\,\mathrm{dB}$), a remarkable 30% extension of the -3 dB bandwidth is evident.

1.2 Circuit Design

The schematic of the realized three-stage LNA is reported in Fig. 1.8. The number of stages is selected so to obtain a power gain greater than 20 dB, a reasonable value to ensure that the noise introduced by the following blocks within a receiver front-end is well suppressed. All the transistors have an emitter area of $10\,\mathrm{x}\,0.2\,\mu\mathrm{m}^2$ and are biased with 10 mA. $\mathrm{MN_{3,4,5}}$ are sixth-order matching networks analyzed in the previous section, where the inductors are implemented with coplanar transmission lines in the topmost 9th metal layer. The lengths are tuned after lines meandering, in order to improve the area efficiency. $\mathrm{MN_3}$ and $\mathrm{MN_4}$ are basically identical while $\mathrm{MN_5}$ embeds the GSG output pad parasitic capacitance to step-up the off-chip $50\,\Omega$ termination. $\mathrm{MN_1}$ is a single-resonance matching network that transforms the $50\,\Omega$ source impedance into the optimal noise termination for $\mathrm{Q_1}$. The same task is performed by $\mathrm{MN_2}$ that transforms the collector impedance of $\mathrm{Q_1}$ into the one that minimizes the noise figure of $\mathrm{Q_2}$. Capacitors labeled as $\mathrm{C_\infty}$, realized with a stack of MIM and MOM components, provide an AC ground path. Low-Q multi-turn coils isolate the supply to cut uncontrolled return signal paths.

1.3 Experimental results

The amplifier (chip photo in Fig. 1.9) is realized in the SiGe BiCMOS 55 nm technology provided by STMicroelectronics. The core area (without GSG
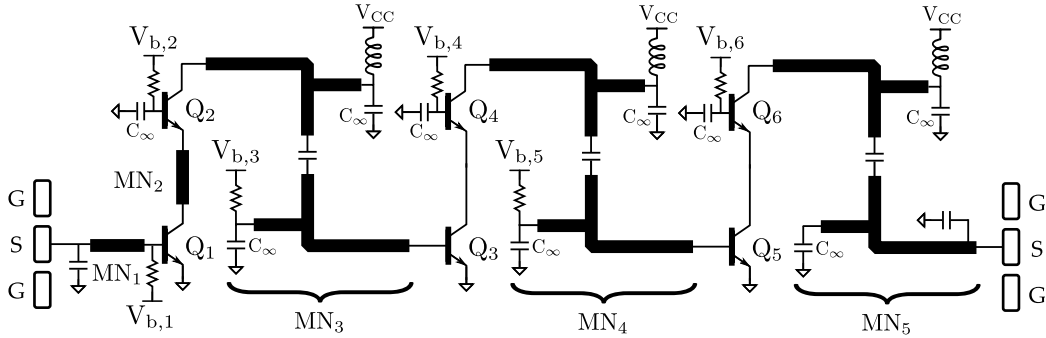
Figure 1.8: Schematic of the realized ultra-wideband LNA
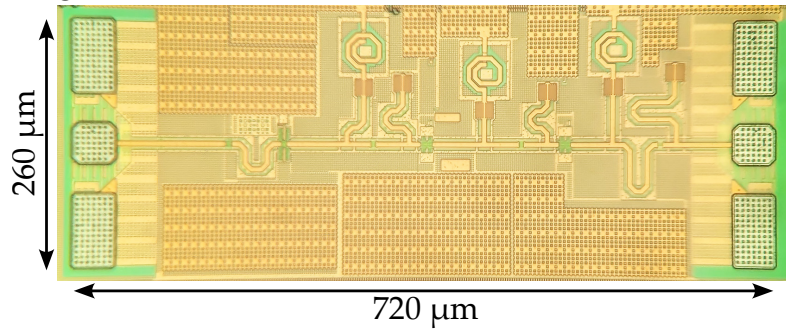
Figure 1.9: Photo of the realized test-chip

pads) is $560\,\mu$m x $195\,\mu$m. The chip is mounted on a custom PCB that provides the necessary voltage supplies and on-wafer probing is realized through Infinity Waveguide GSG probes. They are connected to the VDI WR6.5-VNAX frequency multipliers that perform frequency extension for the Agilent E8361C VNA. A Farran WGNS-06 noise source is employed for noise figure characterization, together with a VDI WR6.5SAX-M harmonic mixer (provided with the high sensitivity option for enhanced displayed average noise level (DANL)) and a PXA N9030A spectrum analyzer by Agilent. Additional IF amplification is used to increase the accuracy of the results. Power measurements are performed with an ELVA-1 DPM-06 D-band power meter in combination with an Agilent E8257D signal generator and the VDI WR6.5-VNAX. A summary of the three different measurement setups is schematized

in fig. 1.10, while Fig. 1.11 reports a detail of setup for the acquisition of the S-Parameters. The chip can be recognized on the screen, captured by the camera mounted on the microscope of the probe station. The mea-
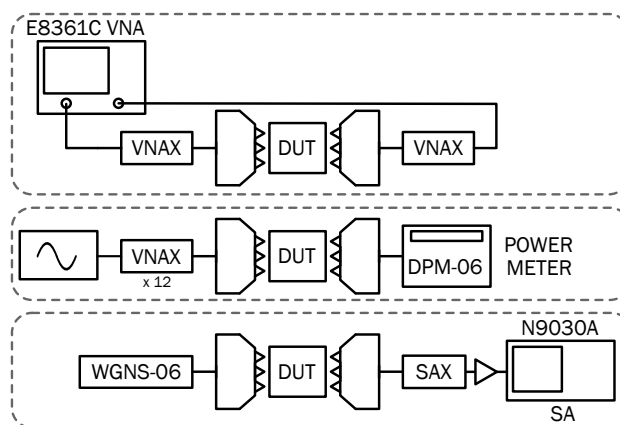
Figure 1.10: Block diagrams of the measurement setups
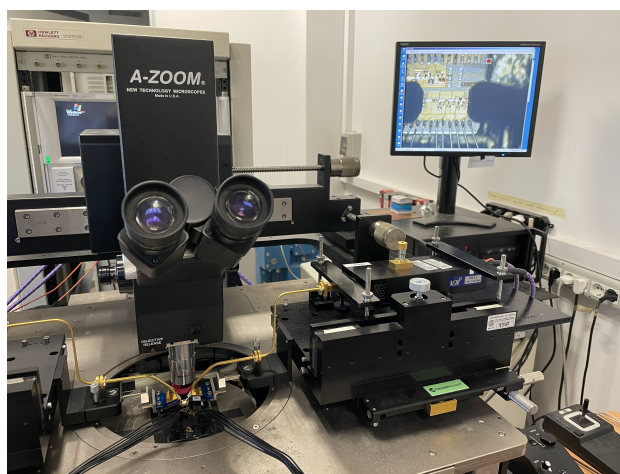
Figure 1.11: Detail of the setup for the acquisition of S-Parameters

surement setup allowed S-parameters and noise figure acquisition only in the 105‑175 GHz and 120‑170 GHz bands, respectively. Fig. 1.12 plots the measured results and proves a good agreement with simulations. The lower -3 dB

point is below 105 GHz, not detected by measurements due to the setup lim-
itation. The -3 dB bandwidth, centered around 140 GHz, is (slightly) larger
than 105 - 175 GHz which corresponds to a more than 50% fractional band-
width. The NF ranges from 5 dB to 6.5 dB within the measured band. The
P_{1dB} of the amplifier, reported in Fig. 1.13 is fairly constant and greater
than 0.7 dBm (output-referred) across the bandwidth, with a peak 1.4 dBm
at 150 GHz.   A summary of the results is reported in Table 4.1. Compared to
prior works, the LNA demonstrates a remarkably high bandwidth, the high-
est among 3-stage amplifiers, with NF across the full bandwidth aligned to
the best performance demonstrated only by narrow-band designs. Only [23]
shows a wider fractional bandwidth which however needs more than twice
the power consumption with a 5-stage design in a technology with higher
f_t/f_{max}, and with a 3-to-6 dB worse NF. The figure of merit proposed in [25]
is used to normalize the gain and bandwidth to the number of stages (n):

$$FoM_{[25]} = \sqrt[n]{G_T} \left(\frac{f_0}{f_{max}} \right)^2 \frac{BW}{f_0} \qquad (1.7)$$

The presented amplifier shows the highest FoM, similar to [21], but with a
3 dB lower NF.

1.4 Summary

The drawbacks of stagger tuning, in contrast to inherently broadband designs have been discussed, and a sixth-order transmission-line-based matching network has been proposed and analyzed for ultra-wideband amplifiers. The network can be approximated as a doubly-tuned transformer where the bandwidth is further extended leveraging the singularities introduced by the AC-coupling capacitor. The concept has been applied to the design of a wideband three-stage LNA and measurements compare favorably against previous works in terms of gain-bandwidth FoM and noise figure.

	This Work	[21]	[26]	[23]	[27]	[20]	[12]	[22]
SiGe BiCMOS Tech.	55 nm	55 nm	55 nm	130 nm	55 nm	130 nm	130 nm	130 nm
f_t/f_{max}	320 / 370	320 / 370	320 / 370	470 / 560	320 / 370	300 / 500	250 / 370	300 / 500
n. of stages	3	3	2	5	3	7	3	4
G_T [dB]	23	28.6	22.8	35	28	15.5	32.8	32.6
f_0 [GHz]	140	140	148	201.5	148	180	140	140
3 dB BW [GHz]	70	64.3	33.5	155	41	80	23.2	52
NF [dB]	5 - 6.5	8.8 - 10.5*	5 - 6.5	8.4 - 12	5.2 - 6.6	6.1 - 8.5	7.8 - 9.5*	4.8 - 6.1
IP_{1dB} / OP_{1dB} [dBm]	-21.3 / 0.7	-29.7 / -2.1	-21.8 / 0	-32 / 2	-25 / 2	-16.7 / -2.2	-28.6 / 3.2	-37.6 / -6
P_{DC} [mW]	60	36	40	152	60	46	39.6	28
Core Area [mm^2]	0.109	0.11	0.122	0.092	0.107	0.48	0.075	0.6
Frac. BW [%]	50	45.9	22.6	76.9	27.7	44.4	16.6	37.1
FoM[25]	**0.204**	0.201	0.173	0.151	0.135	0.085	0.076	0.07

* simulated value

Table 1.1: Comparison with the state-of-the-art.
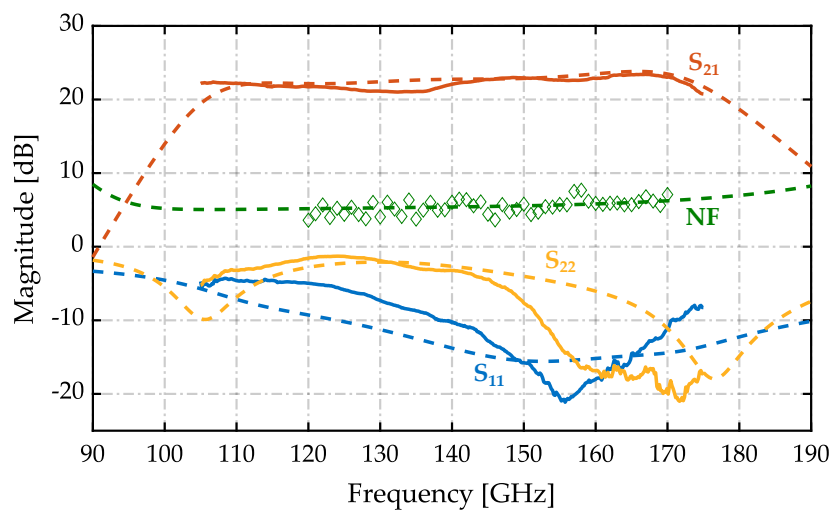
Figure 1.12: Measured S-Parameters and noise figure compared to simulations (dashed lines).
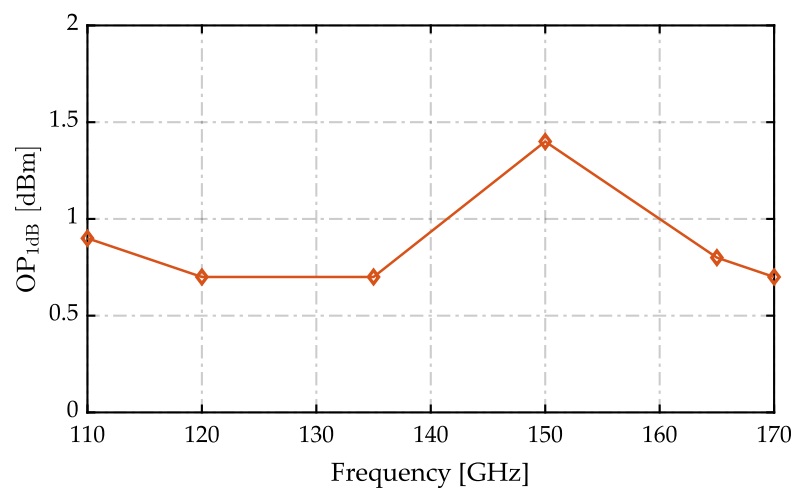
Figure 1.13: Measured output-referred 1dB compression point.

Chapter 2

Gain Boosting

S EVERAL D-band LNAs in Bipolar or BiCMOS have been demonstrated [28][29][30], proving the technology viability. Nonetheless, in current technologies, transistors are pushed to operate close to their frequency limit (f_{max}). The common-emitter (CE) gives the best noise performance and simplifies impedance matching, but its maximum available gain (MAG) is limited to few dBs only in D-band. Approaches aimed at improving power gain have been investigated, but end up with a cumbersome design approach and lead to a narrow-band response [31][32]. Most commonly, D-band amplifiers leverage straightforward cascode structures to rise the gain, stacking a common-base (CB) onto the CE [33][34]. In [35][36], interstage matching between CE and CB is also introduced to improve both gain and noise performance of the stack. Solutions to boost the gain for CB transistors, such as inductive base degeneration, have been deeply studied, with the drawback of further increasing the already high output impedance [37] and complicating matching networks implementation. Recognizing that the gain of a conventional cascode is limited by the CE, this chapter investigates the use of local feedback to enhance the CE gain by shifting the device

into a conditionally-stable operating region. Then, provided the impedance levels and matching networks are carefully selected, when the CE is combined with a CB, the resulting cascode structure displays superior gain with unconditional stability. The concept is exploited in the design of a two-stage D-band LNA which shows 22.8 dB gain with 33.5 GHz bandwidth around 148 GHz, NF down to 5 dB and 0 dBm output compression point with 40 mW power consumption. Measurements compare favorably against previously reported silicon amplifiers in D-band.

2.1 Inductive feedback on the CE

As the operating frequency increases, the available power gain of a transistor drops, being unity at f_{max}. Moreover, beyond a certain corner frequency, which depends on the transistor configuration (e.g. CE or CB), the losses by parasitic elements make the device unconditionally stable. In this case, a useful figure of merit to evaluate gain capability is the maximum available gain (MAG):

$$\text{MAG} = \frac{|S_{21}|}{|S_{12}|} \left(K - \sqrt{K^2 - 1} \right) \tag{2.1}$$

with S_{21}, S_{12} the forward and reverse scattering parameters of the device and $K > 1$ the stability factor. In the unconditionally stable region, MAG defines an upper bound to power gain, achieved with simultaneous input/output conjugate match. On the other hand, under a certain frequency, K falls below unity and stability is constrained by a careful selection of input/output terminations. Within this regime, an alternative figure of merit is the maximum stable gain (MSG), which is (2.1) with $K = 1$:

$$\text{MSG} = \frac{|S_{21}|}{|S_{12}|} \tag{2.2}$$

It is worth noticing that the maximum available power gain for a conditionally stable device is unbounded, and MSG only defines the gain that could be achieved once the stage is resistively loaded and kept at the boundary of unconditional stability (K = 1) [38].
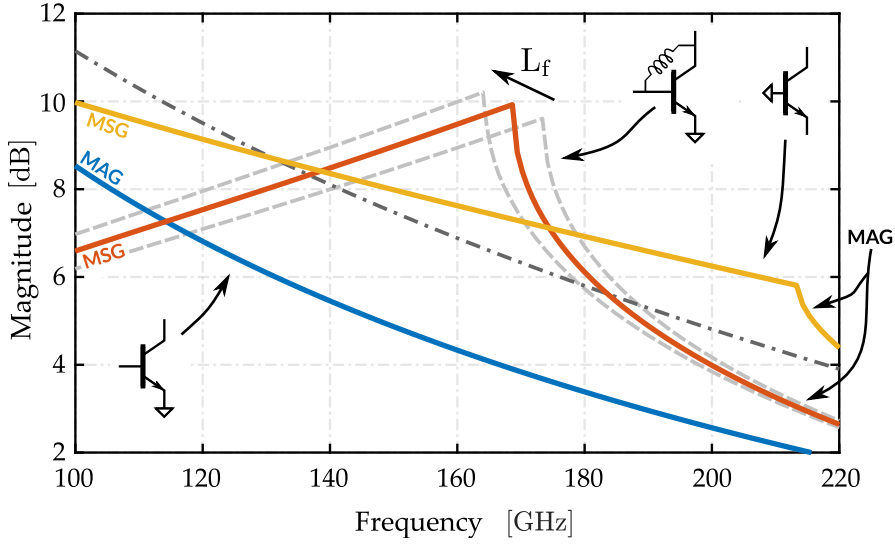
Figure 2.1: Maximum power gain of CE, CB, CEf with L_f around 50 pH.

Fig. 2.1 shows the MAG/MSG curves for different transistor configurations in D-band. The CB stage is conditionally stable with the corner frequency (K = 1) beyond 200 GHz. On the other hand, the CE is more sensitive to device parasitic losses which make it unconditionally stable above 80 GHz and limit the power gain to only ~ 4 dB at 160 GHz. When the CE and CB are combined in a cascode structure, no more than MAG can be extracted from the CE, thus the CB provides most of the gain. A possibility to boost the CE gain consists in pushing its stability corner to higher frequency, such that the device is operated into a conditionally stable region. The solution proposed in this work is based on the introduction of a feedback inductor, L_f, from the collector to the base. The MAG/MSG curves for the CE with

L_f (referred to as CEf) are plotted in Fig. 2.1. The positive feedback introduced by L_f and the parasitic capacitors of the device (base-to-emitter and collector-to-ground, C_{BE}, C_C) shifts the stability corner upwards, to a frequency set by L_f. Looking at Fig. 2.1, this solution provides an evident benefit to the achievable power gain, but mandates a careful design flow not to compromise the stability of the overall amplifier. Finally, it is important to highlight the conceptual difference of this technique from device unilateralization (i.e. neutralization of the feedforward base-to-collector capacitance, C_{BC}). Unilateralization, easily implemented in differential stages with explicit cross-coupled capacitors, brings the advantage of unconditional stability but with limited gain enhancement. To gain insight, the MAG for a neutralized CE at 160 GHz, shown with a dash-dot line in Fig. 2.1, is remarkably lower than the MSG of the CE with L_f.

2.2 Circuit design
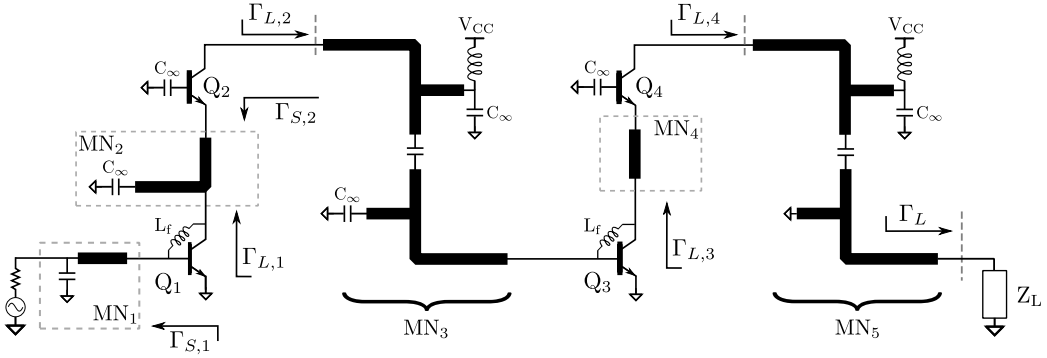
Figure 2.2: Schematic of the proposed LNA.

The schematic of the two-stage cascode LNA is shown in Fig. 2.2. All the multi-emitter HBTs have the same drawn emitter area, $A_e = 2 \times 5 \times 0.2 \, \mu\text{m}^2$, and are biased at $5 \, \text{mA}/\mu\text{m}^2$ current density. Shielded coplanar Tlines,

optimized in the 9 metal layers ($Z_0 = 60\,\Omega$ and quality factor $Q_{TL} = 30$ at 160 GHz), are used in matching networks. AC shorts for bias and supply decoupling (labeled C_∞) are realized with a stack of MIM ad MOM capacitors to ensure the best compromise between low impedance over the band of interest and self-resonance. The -3 dB bandwidth is primarily limited by matching the high impedance at the collectors of CB devices, which show the highest nodal Q. Matching networks MN_3 and MN_5, at the collectors of the CB transistors, realize a broadband impedance transformation, as discussed in the previous chapter. Two complex-conjugate pole pairs match the impedance at two resonance frequencies, set nominally to 140 GHz and 160 GHz, yielding a flat wideband response. The remaining matching networks (MN_1, at the input, and MN_2, MN_4, between CE and CB) are characterized by a low nodal Q and do not limit the bandwidth; hence, simpler single resonance networks are implemented. The feedback inductance in CE transistors is set
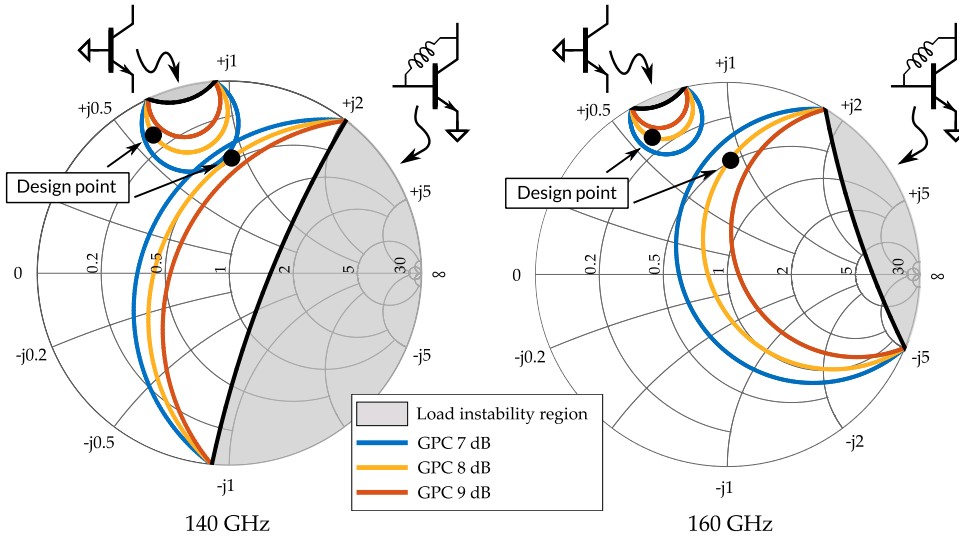
Figure 2.3: G_P and load stability circles of the CB and CEf at 140 GHz, 160 GHz.

to 50 pH and shifts the stability corner frequency to 170 GHz. Fig. 2.3 shows the operating power gain (G_P) and load stability circles for the CEf and CB devices at 140 GHz and 160 GHz. The load impedances are carefully selected such that, once accounting for the matching networks losses, the amplifier is unconditionally stable. The black dots in Fig. 2.3 represent the selected load reflection coefficients, $\Gamma_{L,3}$, $\Gamma_{L,4}$ (or, equivalently, the load impedances $Z_{L,3} = 26 + j57$, $Z_{L,4} = 6 + j31$) for the second stage transistors, Q_3, Q_4. The points lie on the $G_P = 8$ dB circles at both 140 GHz and 160 GHz. The loss (~ 2 dB) introduced by MN_5 from the output pad (nominally terminated to $Z_L = 50\,\Omega$) to the collector of Q_4 compresses the variation of $\Gamma_{L,4}$ against variations of Z_L and ensures stability of the CB device. The network MN_4,
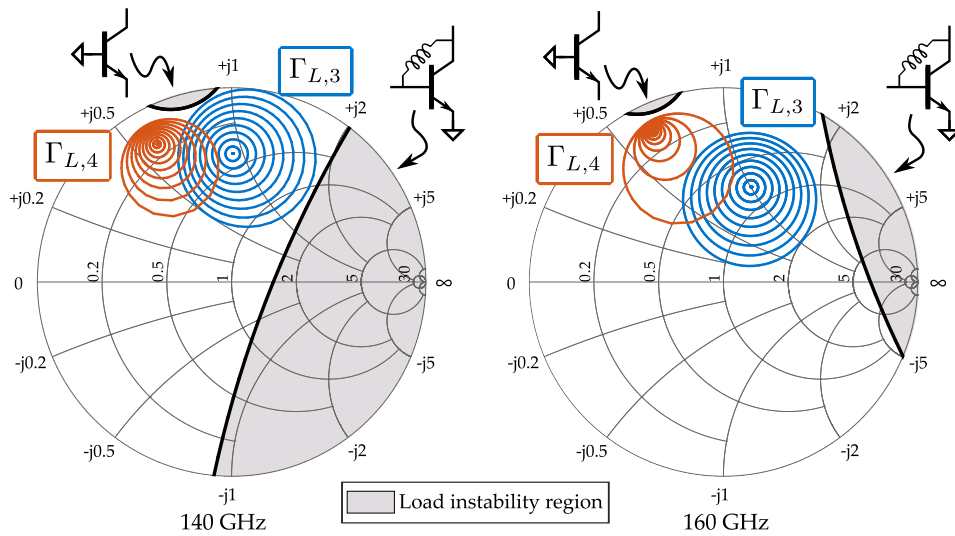
Figure 2.4: CB and CE load stability circles and possible variation of $\Gamma_{L,3}$ and $\Gamma_{L,4}$ at 140 GHz and 160 GHz.

implemented with a simple series Tline, transforms the impedance at the emitter of Q_4 to the target load for the CEf, $Z_{L,3}$. The latter is selected sufficiently far from the CEf potentially-unstable region to still preserve the

stability against variation of the off-chip load impedance Z_L. To gain insight, Fig. 2.4 shows the load reflection coefficient for Q_3 and Q_4, obtained by sweeping Z_L across the whole Smith chart (thus considering any possible passive termination at the GSG output pad). $\Gamma_{L,3}$ and $\Gamma_{L,4}$ remain always out of the CB and CEf load potentially-unstable regions (the gray areas in Fig. 2.4), confirming the unconditional stability of the implemented cascode structure. The nominal load impedance of Q_2 (the CB device in the first stage) is the same as for Q_4. Thus, the multi-resonance network MN_3 is designed such that the impedance at the base of Q_3 is matched to the load of Q_2, $Z_{L,2} = Z_{L,4} = 6 + j31$ at 140 GHz and 160 GHz. Similarly to what done in the design of the LNA of chapter 1, networks MN_1 and MN_2 are designed to optimize the noise performance. The amplifier noise factor, dominated by Q_1 and Q_2, is given by:

$$F \approx F_1 + \frac{F_2 - 1}{G_{A,1}} \qquad (2.3)$$

where F_1, F_2 are the noise factors of Q_1, Q_2, and $G_{A,1}$ is the available power gain of Q_1. The noise factor of Q_1 and Q_2 is minimized by well-defined source terminations, while a trade-off may exist between F_1 and $G_{A,1}$. Fig. 2.5 shows the noise circles and constant G_A curves for Q_1, in CEf configuration, at 150 GHz. The center of the circles defines the source impedance $Z_{OPT,F1}$ that gives $F_1 = F_{1,min}$. With $Z_{OPT,F1}$, $G_{A,1} \approx 10$ dB. Thus, the input matching network MN_1 transforms the 50 Ω off-chip nominal source impedance into $Z_{OPT,F1}$. Once MN_1 is set, the impedance at the collector of Q_1 is defined and matching network MN_2 is designed such that the input termination of Q_2, the CB device, is $Z_{OPT,F2}$ leading to $F_2 = F_{2,min}$. Since Q_1 is a conditionally stable device, once MN_1 and MN_2 are fixed, its stability conditions must be verified. To this aim, Fig. 2.6 reports load stability circles of Q_1 and the values of $\Gamma_{L,1}$ for any passive load impedance Z_L. It is clearly seen that, with
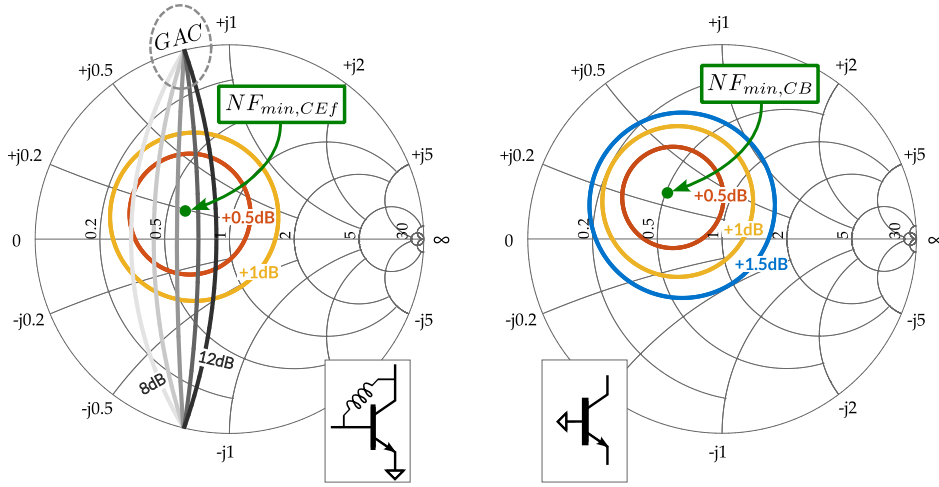
Figure 2.5: G_A and noise circles of CEf, noise circles of CB. $f = 150\,\mathrm{GHz}$.

respect to Fig. 2.4, the increased isolation from the output provided by the second stage makes stabilization easier, and the matching networks designed to minimize the noise factor do not compromise the amplifier unconditional stability.

2.3   Experimental Results

The amplifier (chip photo in Fig. 4.5) is realized in STMicroelectronics' SiGe BiCMOS 55 nm technology. The occupied area is $742\times256\,\mu\mathrm{m}^2$, including GSG pads. RF signals are conveyed through Infinity Waveguide GSG probes to VDI WR6.5-VNAX extension modules for the Agilent E8361C VNA. Fig. 2.8 compares small signal measurements and simulations, showing good agreement. Farran WGNS-06 noise source, FBC-06 frequency extender and Keysight N8975A analyzer constitute the noise figure (NF) measurement equipment. The minimum measured NF is 5 dB and rises by 1.5 dB

	This work	[33]	[39]	[35]	[30]	[40]	[29]	[37]	[36]	[28]	[34]
SiGe BiCMOS Tech.	55 nm	55 nm	120 nm	130 nm	55 nm	130 nm	90 nm	130 nm[1]	130 nm	130 nm	130 nm
f_t/f_{max}	320/370	320/370	200/265	250/370	320/370	250/370	300/350	300/500	300/500	300/500	300/500
# of stages	2	2	4	3	2	3	4	2	2	4	4
# of actives	4	4	8	6	4	6	7	4	6	8	6
G_T [dB]	22.8	20.1	26	32.8	20.6	23	30	27.5	26	32.6	25.3
f_0 [GHz]	148	150	130	140	144	157	136	126	150	140	134
-3 dB BW [GHz]	33.5	24.5	13	23.2	65.8	55	28	16	60	52	44
P_{DC} [mW]	40	27	57	39.6	24	25/60	45	12	70	28	30
NF [dB]	5-6.5	-	-	7.8-9.5*	8.1-10.2*	6-7.9	6.2-8	5.5-6.5	-	4.8-6.1	5.9-7
P_{OP1dB} [dBm]	0	-	-	3.2	-1.9*	-	-	-6.5	2	-6	-
FoM_{ITRS}	**19.65**	-	-	16.88	8.15	-	-	10.59	-	7.14	-
FoM	**0.59**	0.52	0.51	0.5	0.5	0.44	0.41	0.31	0.24	0.2	0.19

* simulated value

Table 2.1: Comparison with the state-of-the-art.
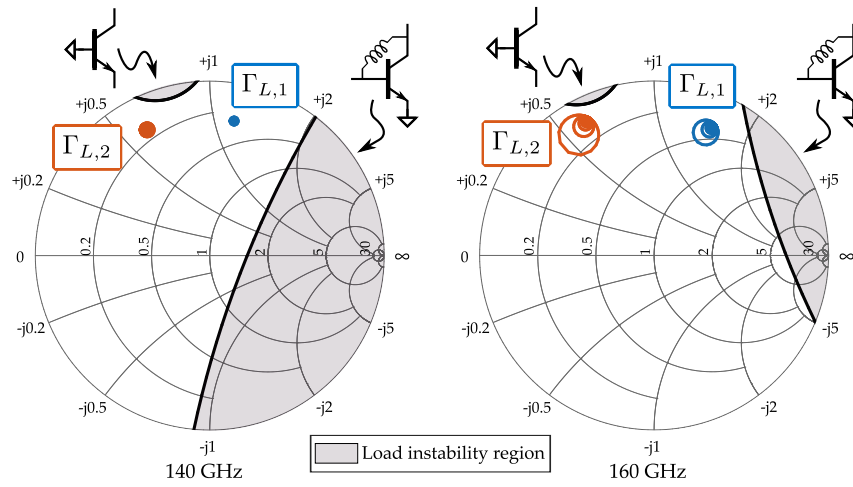
Figure 2.6: CB and CE load stability circles and possible variation of $\Gamma_{L,1}$ and $\Gamma_{L,2}$ at 140 GHz and 160 GHz.

within the bandwidth. Notably, the measured NF is slightly lower (~ 1 dB) than simulations. The gain at 148 GHz is 22.8 dB and the -3 dB bandwidth extends from 131 GHz to 165 GHz. The K factor, reported in Fig. 2.9, con-
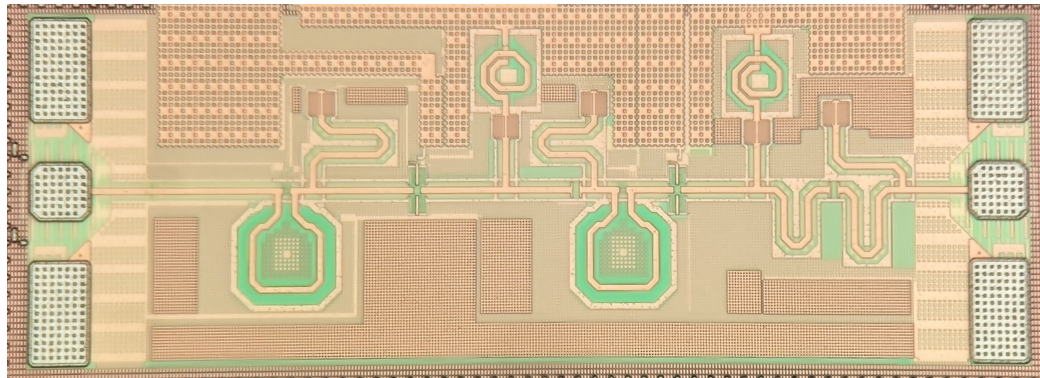
Figure 2.7: Chip microphotograph.

firms unconditional stability. The output power at 1 dB gain compression, OP_{1dB}, measured with ELVA-1 DPM-06 power meter is greater than 0 dBm, as reported in Fig. 2.10. Experimental results are summarized in Table

2.1 together with state-of-the-art D-band amplifiers in bipolar or BiCMOS technology. The performance of the presented amplifier is compared against previous works with two figures of merit;

$$FoM = \sqrt[n]{G_T} \left(\frac{f_0}{f_{max}} \right)^2 \tag{2.4}$$

normalizes gain, G_T, at the center frequency f_0 to the number of devices n and the cut-off frequency f_{max} [32]. This FoM is a useful benchmark for the amount of gain extracted from devices operated close to their frequency limit. The overall LNA performance, like noise figure (NF), linearity (IIP_3[1]), and
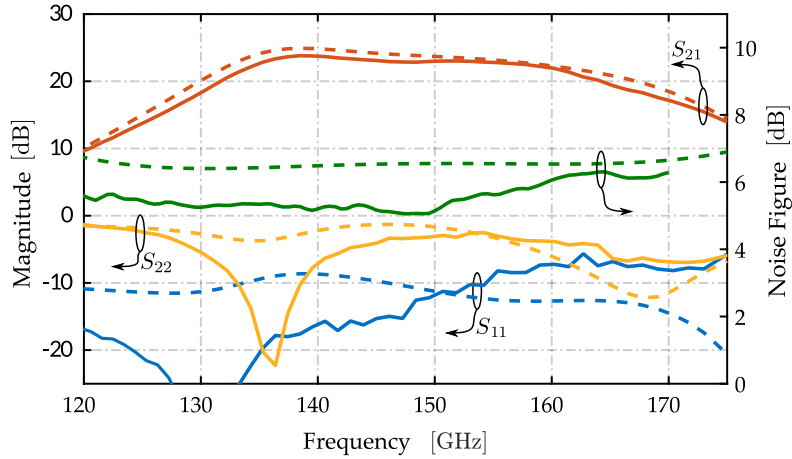
Figure 2.8: Small signal measurements (solid) vs. simulations (dashed).

power consumption, are included into the FoM_{ITRS} [41], given by

$$FoM_{ITRS} = \frac{G_T \cdot IIP_3 \cdot f_0}{(NF - 1) \cdot P_{DC}} \tag{2.5}$$

All the quantities in the figures of merit are expressed in linear scale. The good achieved FoM and FoM_{ITRS}, beyond what demonstrated by previous works, support the proposed local inductive feedback in CE transistors as an effective solution to improve D-band amplifiers performance.

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[1]Where unreported, IIP$_3$ was estimated as P$_{IP1dB}$ + 9.6 dB
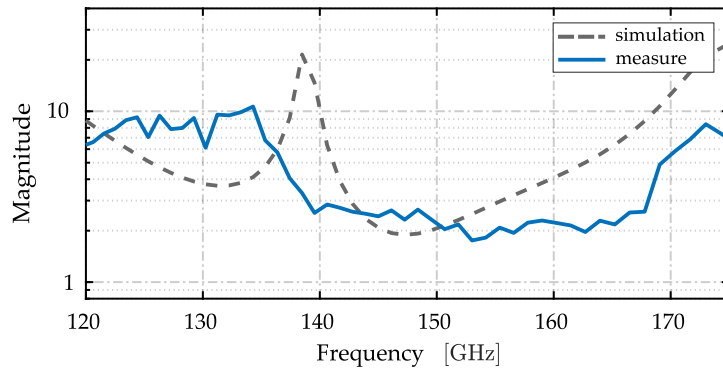
Figure 2.9: Measured stability factor K.
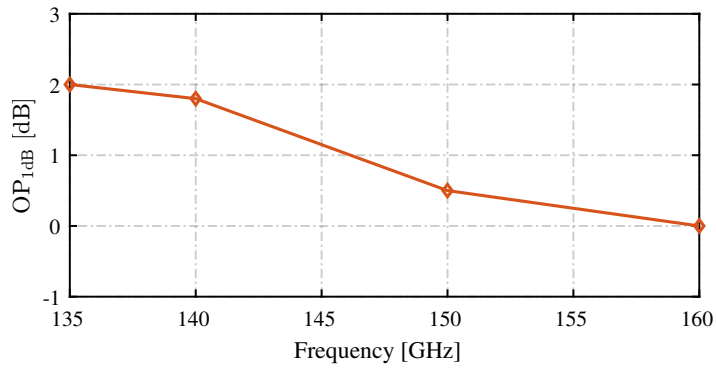
Figure 2.10: Measured output-referred 1dB compression point.

2.4   Summary

Inductive feedback applied to a common-emitter device has been investigated as a solution to trade gain for stability. The technique forces the transistor to operate in a conditionally stable region with gain above the device maximum available gain. The concept has been applied to a D-band LNA and a design procedure has been described such that the overall amplifier features unconditional stability with high gain and minimum noise figure. The measured results, combined in figures of merit typically used as benchmark for high-frequency LNA, confirm the effectiveness of the proposed solution to push the state-of-the-art performance.

Chapter 3

Passive Phase Shifters

P HASE shifters (PS) can be realized in both active and passive form. Active PSs are based on the vector interpolation principle. In D-band, they are typically characterized by high resolution but limited power gain (or even loss) [42] or limited linearity, even at moderately high power consumption [43]. This work investigates passive D-band PSs leveraging the availability of good MOS switches and a 9-level metal stack, with two thick top layers, in the SiGe BiCMOS 55nm process. Different passive networks providing a programmable phase shift are presented in this section. To cover the four-quadrants (0°-360°) with good enough resolution, phase shifters (PS) with fine and coarse control are developed. The former feature a digitally-controlled phase shift in small steps but the maximum range is limited to keep low insertion loss. The latter provide a 1-bit phase control with a large step (nominally 0°/90° and 0°/180°). By cascading the fine- and coarse-control networks, the four quadrants are covered maintaining fine resolution and limited insertion loss.

A test chip is realized with an embedded on-chip TRL calibration kit, essential for the correct de-embedding of probes and interconnections, allowing
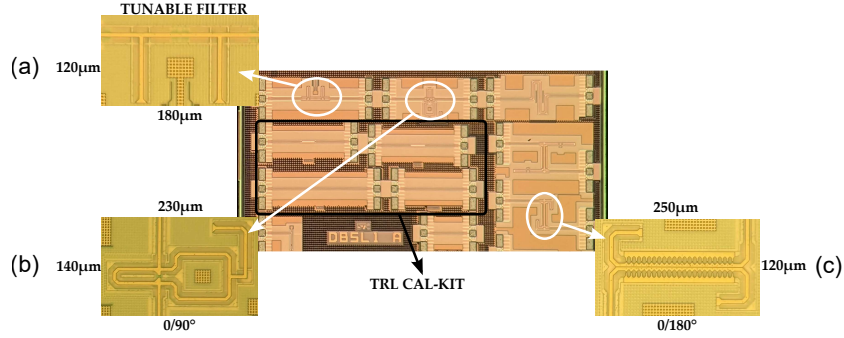
Figure 3.1: Chip photo of the realized passive phase shifters.

to characterize the S-Parameters of the passive structures alone. The chip photo is represented in Fig. 3.1. Even though the structures to be measured and the calibration standards appear close to each other, the short wavelenght at the operating frequencies allows to have a compact organization of the various blocks without degrading the accuracy of measurements due to crosstalk between adjacent cells.

3.1 Tunable Band-Pass Filter for Fine-Control Phase Shift

The fine-control PS network is based on a 4th order band-pass filters with a tunable center frequency. Such kind of frequency response may be achieved with magnetically-coupled resonators, shown in Fig. 3.2a. A detailed analysis of this network with design guidelines is available in [24]. If the components (R, L, C, k) are sized such that the two pairs of complex conjugate poles provide a flat in-band response, the phase of the transfer function is fairly linear across frequency, with a variation of π radians within the -3 dB bandwidth, $BW_{-3dB} = f_H - f_L$ (Fig. 3.2b). Therefore, $d\varphi/df \approx \pi/BW_{-3dB}$. If the filter center frequency, f_0, is shifted by Δf_0 by varying the network capacitors
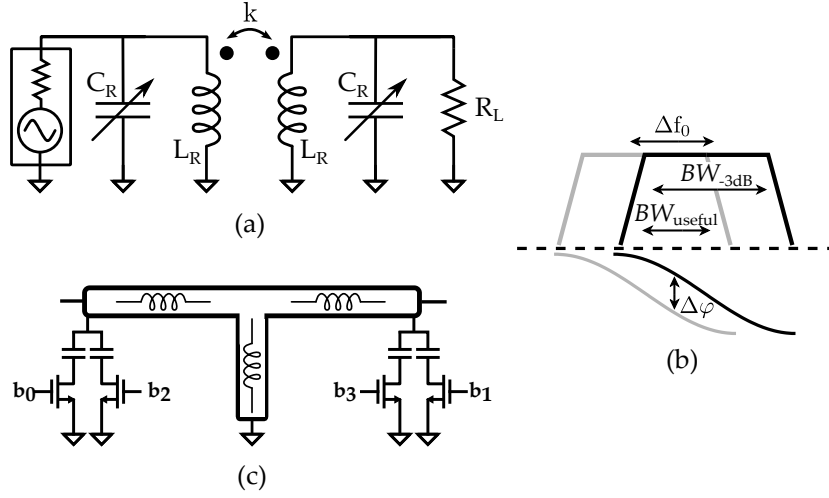
Figure 3.2: Coupled-resonator band-pass filter (a) and transfer function (amplitude / phase) variation by tuning the center frequency (b). Schematic of the implemented network (c).

(gray plot in Fig. 3.2b), the signal experiences a phase shift variation equal to:

$$\Delta\varphi \approx \frac{\pi}{BW_{-3dB}} \cdot \Delta f_0 \tag{3.1}$$

However, to avoid attenuation when the network transfer function is translated, the useful bandwidth (BW_{useful}) is lower than BW_{-3dB}. Looking at Fig. 3.2b, $BW_{useful} = BW_{-3dB} - \Delta f_0$ and, making use of (3.1):

$$BW_{useful} = BW_{-3dB}\left(1 - \frac{\Delta\varphi}{\pi}\right) \tag{3.2}$$

From (3.2), given a target BW_{useful}, the wider is the desired maximum phase variation, the largest must be BW_{-3dB}. On the other hand, $BW_{-3dB} \propto 1/(RC)$, thus an upper bound on BW_{-3dB} (and hence $\Delta\varphi$) is finally set by the smallest variable capacitors that can be reliably implemented to achieve the required tunability of f_0. In order to extend the attainable phase shift, multiple identical networks can be cascaded. This leads to higher out-of-band

roll-off with a marginal bandwidth reduction. The implemented schematic is shown in Fig. 3.2c. The coupled inductors of Fig. 3.2a are replaced by their equivalent T-network, realized with short Tlines that provide lower loss compared to magnetically-coupled coils. The Tlines are shielded microstrips with the signal routed in the topmost metal layer and display a quality factor $Q = 35$ at $165\,\mathrm{GHz}$. The network center frequency is digitally tuned by a bank of four switched MOM capacitors. The switches are nMOS with $W/L = 40\,\mathrm{um}\,/\,55\,\mathrm{nm}$, implemented in triple well to improve the substrate isolation and reduce losses [44]. Each MOM-switch combination features $C_{\mathrm{MAX}} = 16\,\mathrm{fF}$ with $C_{\mathrm{MAX}}\,/\,C_{\mathrm{min}} = 1.5$ and minimum quality factor $Q_{\mathrm{min}} = 10.5$. The band-pass cells are sized for a center frequency of $150\,\mathrm{GHz}$ and $90\,\%$ fractional bandwidth. The capacitors bank shifts the center frequency by $\pm 10\%$ thus, using (3.2), each cell introduces roughly $35°$. Fig. 3.3a describes S_{21} magnitude and phase of the cascade of two elementary cells; their layout is visible in Fig. 3.1a. The total insertion loss ranges between 3 and $7\,\mathrm{dB}$. Fig. 3.3b reports the phase shift normalized to the first phase step, showing a total variation of $62°$ and $84°$ at $110\,\mathrm{GHz}$ and $170\,\mathrm{GHz}$, respectively, and an average phase step of $7°$. The input and output return loss (not shown) are below $-15\,\mathrm{dB}$ over the $130\,\text{-}\,170\,\mathrm{GHz}$ frequency range. The core size of a unitary cell of the tunable filter is $90\,\mu\mathrm{m}$ x $85\,\mu\mathrm{m}$.

3.2   0° / 180° Phase shifters

The well-known reflective-type phase shifter approach is selected to implement a passive network that provides a phase shift of nominally 0° or 180° PS. The schematic is reported in Fig. 3.4a and consists of a quadrature hybrid whose I and Q ports are terminated onto variable impedances. The input
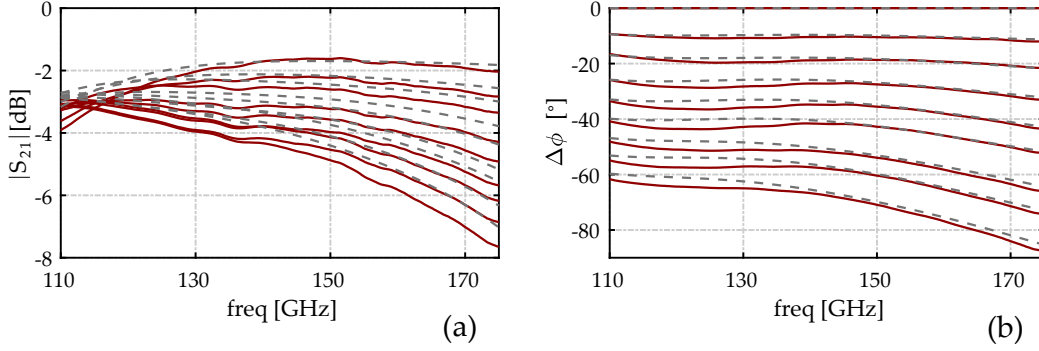
Figure 3.3: S_{21} magnitude (a) and phase response (b) of the tunable filter at different states. Measures (solid) vs. simulations (dashed).

signal S_{in} splits evenly and appears halved at the I/Q ports. If an identical impedance Z_L with non-zero reflection coefficient (Γ_L) loads the I/Q ports, the signals are reflected and get summed up at ISO port, giving the output signal S_{out}. Neglecting the hybrid losses, the following relation holds:

$$\left|\frac{S_{out}}{S_{in}}\right| = |\Gamma_L|^2 \quad \angle\frac{S_{out}}{S_{in}} = -90° + \angle\Gamma_L \quad (3.3)$$

The I/Q ports are terminated by the nMOS switches $M_{1,2}$, yielding ideally $\Gamma_L = \pm 1$ in the off and on state, respectively. Using (3.3), S_{in} is transferred to the ISO port with the same magnitude but $\pm 90°$ phase, corresponding to a 180° relative phase variation. The finite channel resistance and the parasitic capacitance of the nMOS switches introduce signal loss and deviation from the ideal 180° phase. The transistors are sized with $W/L = 50\,\mu m\,/\,55\,nm$ to achieve $r_{on} = 7\Omega$. In the off-state, the parasitic capacitance at the drain terminal is resonated out by the parallel inductors $L_{p1,2} = 40\,pH$, implemented with meandered transmission-line stubs, to rise the equivalent impedance. The simulated S_{21} of the network with V_{ctrl}=0 and V_{ctrl}=1.2V is reported in Fig. 3.5. The relative phase variation is within $\pm 30°$ between 140 GHz and 170 GHz. The insertion loss between 3.5 and 4.4 dB. The input/output
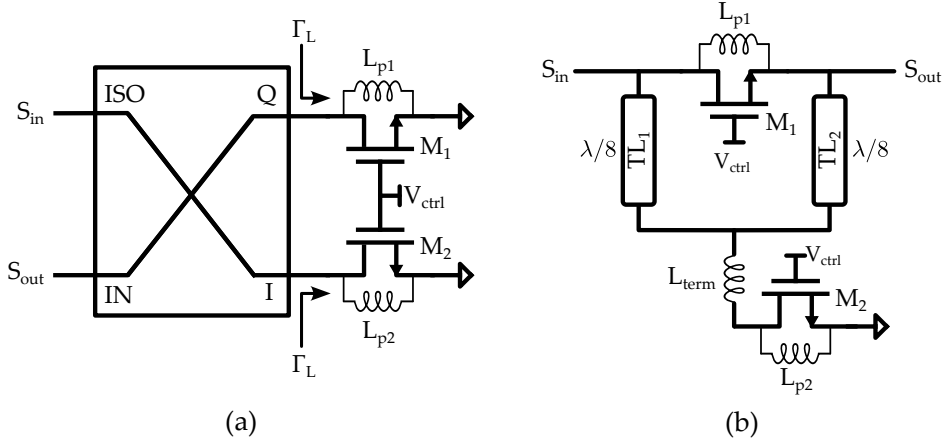
Figure 3.4: Schematic of the 0/180° Hybrid-coupler-based PS (a) and of the 0/90° switched-Tline-based PS (b)

return loss (not shown), remains below -16 dB over the full bandwidth. The hybrid coupler determines the occupied silicon area. It is realized with 230 μm-long coupled lines with a total size of 250μm x 120μm.

3.3 0° / 90° Phase shifters

The hybrid coupler could be used also to implement a 0° / 90° phase shifter by selecting either the I or the Q output but with an intrinsic insertion loss (IL) of 3 dB [45] because half of the signal power is wasted. To avoid this loss, the proposed 0° / 90° PS leverages a bypassed λ/4-long transmission line. The schematic is reported in Fig. 3.4b. The inductors $L_{p1,2} = 60$ pH, in parallel to the nMOS switches $M_{1,2}$, resonate the transistors parasitic capacitors in order to rise the off-state impedance and improve isolation. In this condition, L_{term} is floating and the signal flows through TL_1 and TL_2, experiencing a 90° phase shift due to the $\lambda / 4$ total length. When $M_{1,2}$ are on, instead, the transmission lines are bypassed by M_1 and the

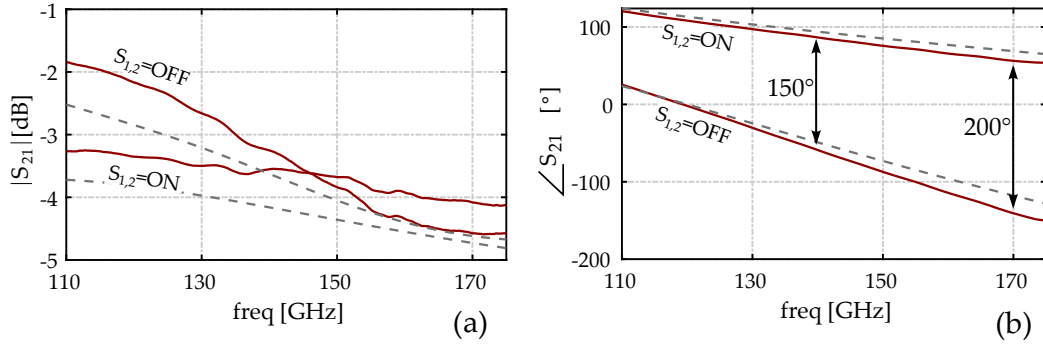Figure 3.5: S$_{21}$ magnitude (a) and phase (b) of the 0°-180° PS in the two states. Measures (solid) vs. simulations (dashed)
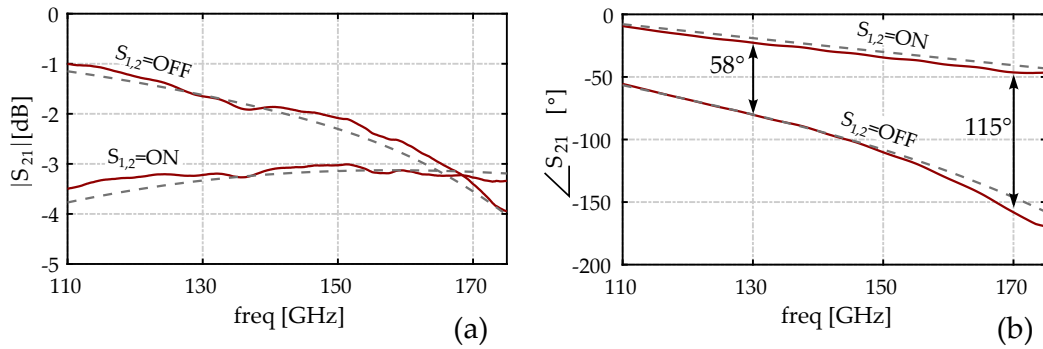
Figure 3.6: S$_{21}$ magnitude (a) and phase (b) of the switched-transmission-lines-based PS in the two states. Measures (solid) vs. simulations (dashed)

signal experiences ideally no phase shift. To limit the insertion loss and improve the return loss, the other end of $TL_{1,2}$ is terminated by $L_{term} = 25\,pH$ which is connected to ground through M_2. In fact, in the on-state, $TL_{1,2}$ shunt the input/output ports and are equivalent to a $\lambda/8$ Tline with half the characteristic impedance, $Z_0/2$. L_{terms} realizes an impedance equal to $+jZ_0/2$, such that a high impedance (ideally an open circuit) appears at the top end of $TL_{1,2}$, thus not affecting the signal transmission. The size of the nMOS switches is set to $W/L = 35\,\mu m/55\,nm$ as a compromise between insertion loss and phase error, caused by the channel resistance and device parasitic capacitors, respectively. Inductors $L_{p1,2}$ and L_{term} are realized with Tlines. Fig. 3.6 reports the simulated performance of the $0°/90°$ with the switches in the on and off state. The relative phase shift is $58°$ at $130\,GHz$ and $115°$ at $170\,GHz$ with the insertion loss within 2 - 4 dB. The input/output return loss (not shown) is below -15 dB over the same bandwidth. The core size of the circuit is $230\mu m$ x $140\mu m$.

Chapter 4

Receiver Front-End

The D-band RX front-end, shown in fig. 4.1 comprises a two-stage LNA followed by a phase shifter, realized by combining the building blocks presented in the previous chapters. Passive phase shifting elements are interleaved with gain-boosted cascode stages to maximize the receiver dynamic range.

4.1 Low-Noise Amplifier

Fig. 4.2 shows the schematic of the implemented LNA. The cascode structure presented in chapter 2 is used in the second stage (Q_3 - Q_4) with $Z_{L,CB}$ the impedance synthesized by the matching network MN_5 as load impedance
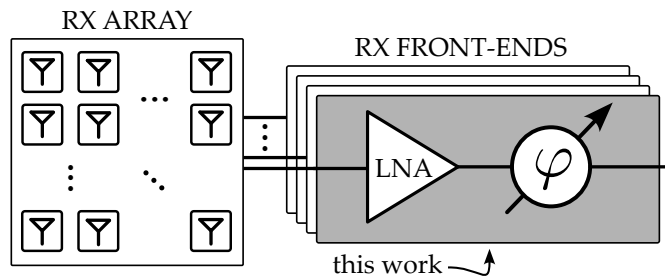

Figure 4.1: Block diagram of a phased-array receiver front-end.
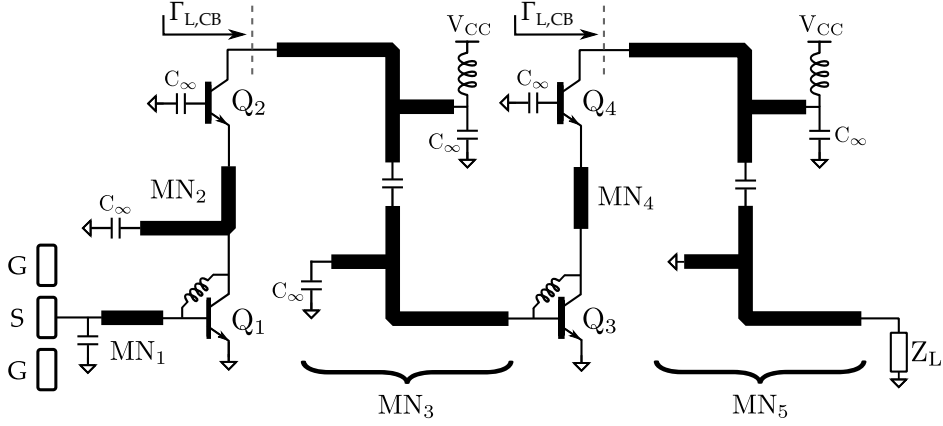
Figure 4.2: Schematic of the gain-boosted two-stage LNA.

for Q_4. With the target of wideband operation, the design starts by considering the G_P circles of Q_3 - Q_4 at 130 GHz and 170 GHz, shown in Fig. 4.3. To have a fairly flat gain over frequency, MN_5 is required to scale up the impedance presented by the cascaded block (Z_L in Fig. 4.2, nominally 50 Ω) to the impedance $Z_{L,CB}$ at the intersection of the G_P circles at the two frequencies. MN_5 is a fourth-order network with two parallel resonance frequencies, enabling broadband impedance transformation. At RF and lower frequency, such kind of response is commonly achieved with a doubly-tuned transformer, realized by magnetically coupling spiral inductors [46]. On the other hand, their accurate modeling is difficult in D-band and parasitic elements limit self-resonance frequency and quality factor. Tlines are more attractive due to lower loss and a simpler scalable model which limits the iterations with a time-consuming electromagnetic simulator to reach the desired performance. The network MN_5 is realized with a combination of two T-shaped Tline-based sections, separated by a series capacitor that provides the required AC coupling. The network is similar to the one exposed in chapter 1, but it just mimics the response of a doubly-tuned transformer and is

Figure 4.3: Power gain circles of the gain-boosted cascode and load impedance synthesized by a fourth-order broadband matching network over the D-band.
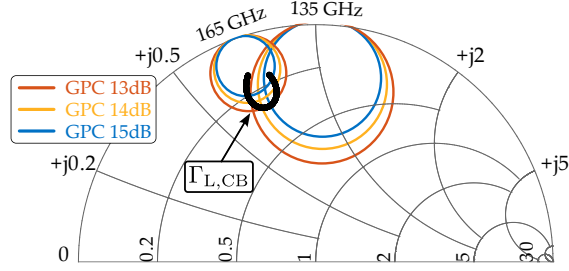
sized following the design flow described in [27]. The Tlines are realized in the topmost 9th metal layer and show a quality factor $Q_{\text{TL}} = 35$ at $165\,\text{GHz}$. The simulated $Z_{\text{L,CB}}$ at the input of MN_5, from $100\,\text{GHz}$ to $200\,\text{GHz}$, is plotted with the black solid line on the Smith chart in Fig. 4.3.

Looking again at the schematic of the LNA, the interstage network MN_3 has the same structure of MN_5 and transforms the relatively low impedance at the base of Q_3 to $Z_{\text{L,CB}}$ seen at the collector of Q_2. The first stage of the LNA (Q_1 - Q_2) is still a cascode structure, but the matching networks MN_1 and MN_2 are sized for optimal noise performance, rather than for maximum power gain. MN_1 transforms the off-chip source termination (nominally $50\,\Omega$) into the optimal impedance that minimizes the noise figure of Q_1. MN_2 transforms the impedance at the collector of Q_1 into the optimal impedance for noise of Q_2. This design choice minimizes simultaneously the noise figure of the first two transistors, which account for most of the signal-to-noise ratio degradation within the LNA, with an acceptable penalty in the power gain.

Capacitors labeled C_∞ in the schematic of Fig. 4.2 provide AC ground paths and are realized with a stack of MIM and MOM components. The

supply voltage V_{CC} is fed through low-Q multi-turn coils to cut uncontrolled signal return paths. From post-layout simulations, with $20\,mA$ DC current from a 2V supply, the LNA provides $22\,dB$ gain with $5 \sim 6.5\,dB$ NF and $0\,dBm$ OP_{1dB}.

4.2 $0° \sim 360°$ Phase Shifter

The $0° \sim 360°$ programmable phase shifter is realized by properly combining the passive networks described in Ch. 3. While the tunable band-pass filters allow a fine phase control resolution, the insertion loss would be prohibitively large if many cells are cascaded to cover the required $360°$ relative phase change. The phase shifter is thus implemented by cascading the $0° / 180°$ and $0° / 90°$ networks with the minimum number of band-pass filters required to cover the $360°$ range, with some margin, across the band of interest. Considering the results of Ch. 3, with five tunable band-pass filters (in addition to the $0° / 180°$ and $0° / 90°$ networks) the overall chain covers $0° \text{-} 375°$ at $130\,GHz$ and $0° \text{-} 515°$ at $170\,GHz$.

An effortless implementation of the phase shifter in the front-end is by straightly cascading all the passive networks after the LNA, as depicted in Fig. 4.4a, and compensate the loss with a post amplifier. The maximum insertion loss of each network, as described in Ch. 3, is reported in the block diagram. Summing all the contributions, the total IL, of $24\,dB$ in the worst case, would have a detrimental impact on the front-end noise. In fact, considering the simulated LNA performance, $NF \approx 6\,dB$ and $22\,dB$ gain, the NF after the passive phase shifter would rise to $7.5\,dB$ with an overall signal attenuation of $2\,dB$. Assuming, optimistically, $6\,dB$ NF also for the post-amplifier, the overall NF would rise above $10.5\,dB$. The noise penalty can

be avoided shifting the additional amplifier before the passive phase shifter chain, as shown in Fig. 4.4b. However, in this case the linearity is dramatically impaired. In fact, assuming $0\,\mathrm{dBm}$ output-referred 1dB compression point ($\mathrm{OP_{1dB}}$) for the cascaded amplifiers, the $24\,\mathrm{dB}$ insertion loss added at the output would limit the OP1dB of the front-end to $-24\,\mathrm{dBm}$ only.

The above discussion highlighted the well-known noise and linearity trade-off, which can be mitigated in this case by interleaving lossy blocks and gain stages in order to keep the highest dynamic range along the chain. To this purpose, the architecture in Fig.4.4c is finally implemented. All the required passive networks are split in two sections, of nearly equal insertion loss, and each one is followed by a single-stage amplifier, balancing the NF and linearity degradation. Each gain stage, with schematic shown in the bottom part of Fig. 4.4, is the same cascode presented in Ch. 2 and implemented in the second-stage of the LNA. The dual-resonance matching network $\mathrm{MN_3}$ scales up the characteristic impedance of the passive networks to the load required at the collector of Q_2 to have a flat and wideband gain profile. The impedance at the base of Q_1 is already close to $50\,\Omega$, and a simpler network ($\mathrm{MN_1}$) is used at the input. With a bias current of $10\,\mathrm{mA}$ from 2V supply, each gain stage displays $\mathrm{G_P} = 13\,\mathrm{dB}$, $\mathrm{NF} = 6.5\,\mathrm{dB}$ and $\mathrm{OP_{1dB}} = 1\mathrm{dBm}$. The noise and compression performances estimated along the chain, in the worst-case, are reported in the block diagram of Fig. 4.4c. The dynamic range degradation of the phase shifter is marginal, being the NF and $\mathrm{OP_{1dB}}$ of the RX front end only slightly worse than those at the output of the LNA. The test-chip includes also a serial register to load the digital configurations required to program the desired phase shifts. The insertion loss variation of the passive networks is compensated by adjusting the bias current of the gain stages, around the nominal value, with an off chip D-to-A converter.
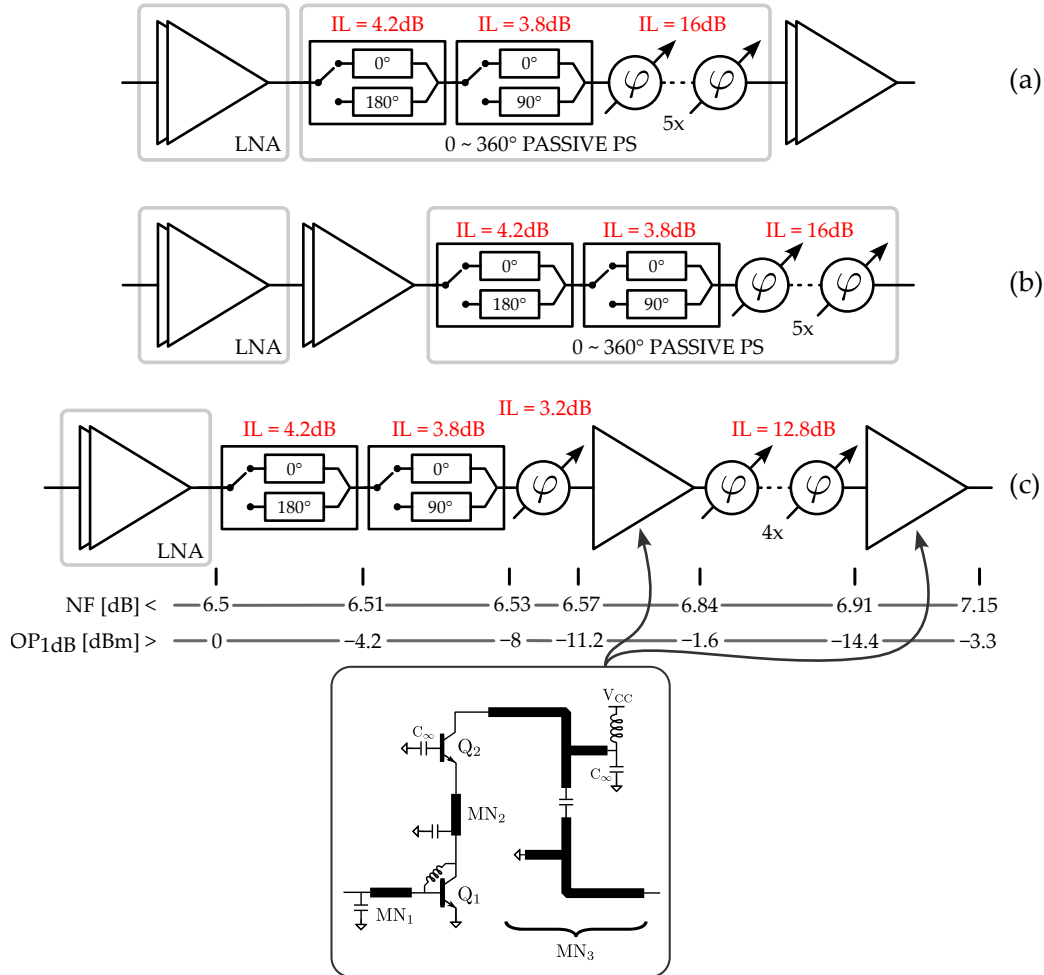
Figure 4.4: Different combinations in the cascade of a LNA, a passive PS and amplifiers (a, b). Proposed solution with lossy blocks interleaved with amplifiers (c). The corresponding worst-case NF and OP_{1dB} at the output of each block is reported. Amplifiers are based on cascode stages with gain boosted by reactive feedback on the common-emitter.
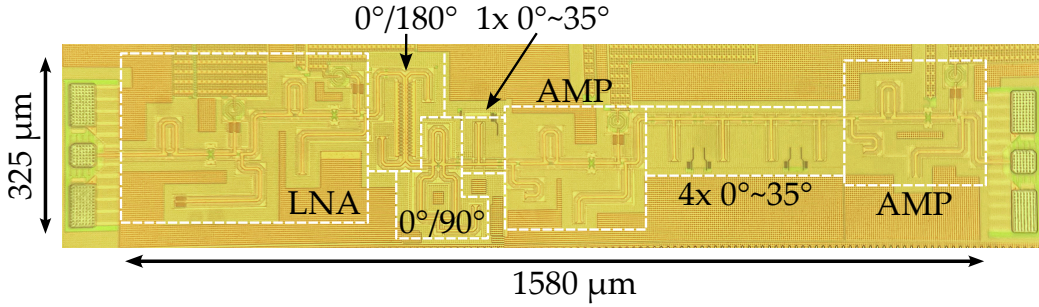
Figure 4.5: Chip photograph of the realized D-band RX front-end.

4.3 Experimental Results

The RX front-end is realized in STMicroelectronics' SiGe BiCMOS 55 nm technology. Fig. 4.5 presents the chip photo, with a core area of 1580 μm x 325 μm. The chip is glued on a PCB which provides the supply, biasing and digital signals through bond-wires, clearly visible in Fig. 4.6. The test setup includes also a custom PCB (shown in Fig. 4.7) equipped with a microcontroller, used to program the on-chip serial register, and 5-bit current DACs that set the bias currents of the integrated amplifiers.

The small-signal measurements are captured with an Agilent E8361C VNA equipped with VDI WR6.5-VNAX frequency extension modules which are connected to Infinity Waveguide GSG probes. S-parameter curves are acquired by an automated routine for all the phase-shift program codes. To compensate for gain variation at different settings of the passive cells, the bias currents of the amplifiers are swept up to 40 % below the nominal value, as a mean to perform variable gain control, except for the last stage, which is kept at the optimal current not to degrade excessively the compression performance. Fig. 4.8 plots all the acquired S_{11} (magnitude) and S_{21} (magnitude and phase) curves in gray. Measurements are then processed and, with
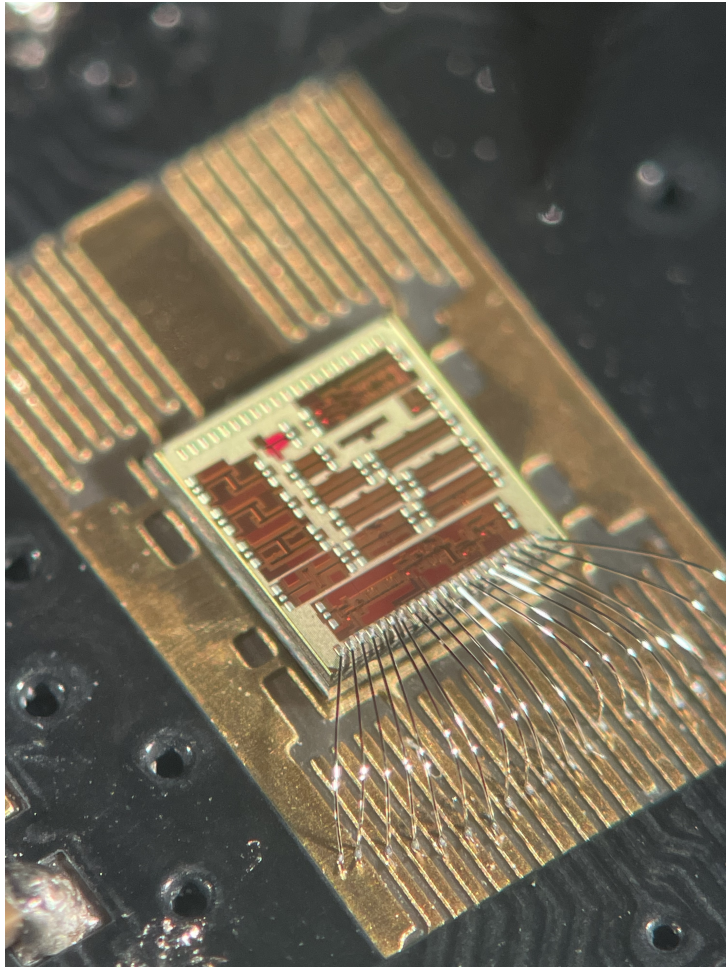
Figure 4.6: Photo of the test-chip mounted onto a PCB and connected through bond wires.
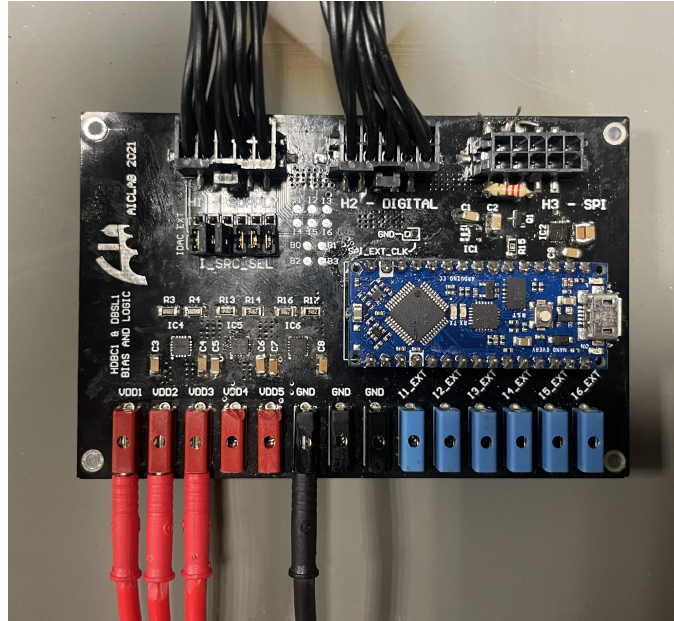
Figure 4.7: DC board used to provide supply, biasing and digital controls to the test-chip.

an offline calibration procedure, a subset of coefficients is selected to have a constant-gain $0° \sim 360°$ phase shift at three frequencies, $137\,\text{GHz}$, $151\,\text{GHz}$ and $165\,\text{GHz}$. The corresponding S_{11} and S_{21} curves are highlighted in red, yellow and blue in Fig. 4.8, demonstrating an average gain of $20\,\text{dB}$ (dashed black line) and a $3\,\text{dB}$ bandwidth from 130 to $170\,\text{GHz}$.

Fig. 4.9a shows the polar characteristic of the RX front-end using the coefficients calibrated at the three frequencies. The average phase step is $7°$. Fig. 4.9b,c report the point-to-point effective phase step, with an error lower than $\pm 7°$, and the gain deviation from the ideal circle which remains within $\pm 2\,\text{dB}$. The calculated RMS gain and phase errors [43] across frequency in the three sub-bands are plotted in Fig. 4.10 and are on average $1\,\text{dB}$ and $10.9°$, respectively. Lower errors can be achieved calibrating the coefficient at more than three frequencies.
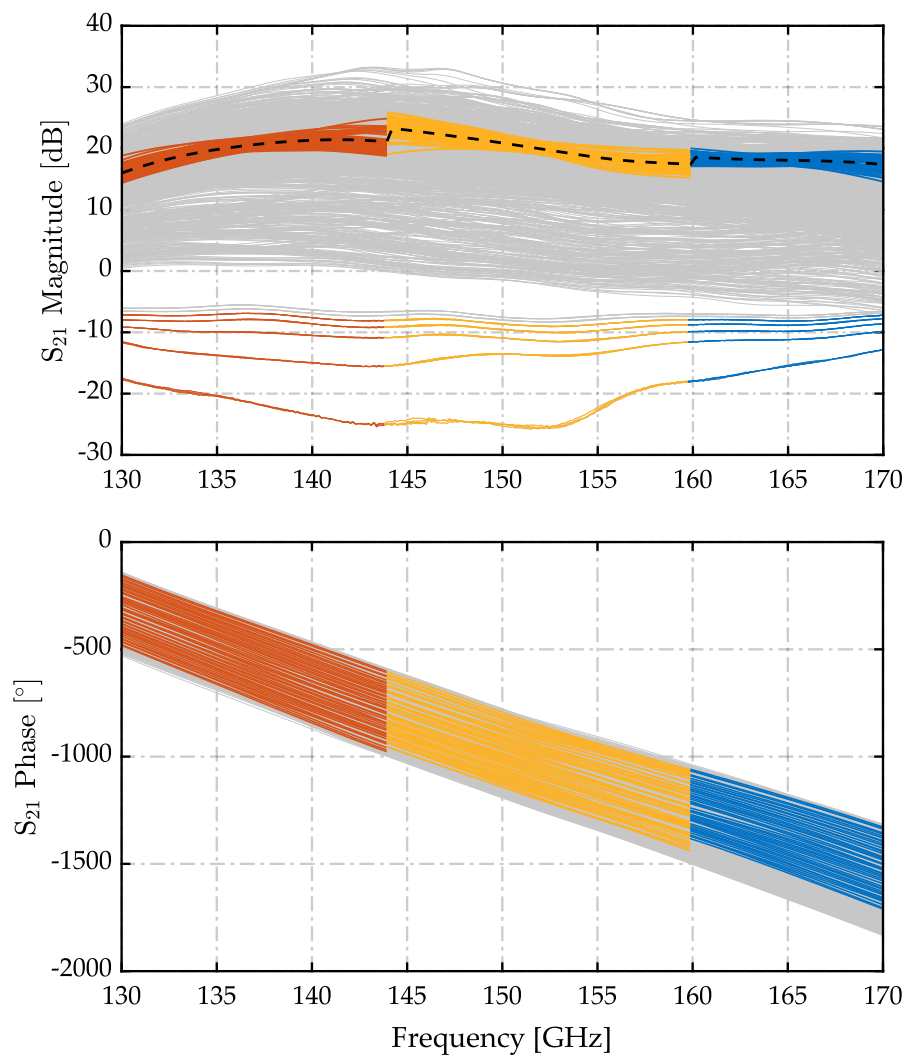
Figure 4.8: S_{21} magnitude and phase. Highlighted are the curves acquired at the selected calibration settings.
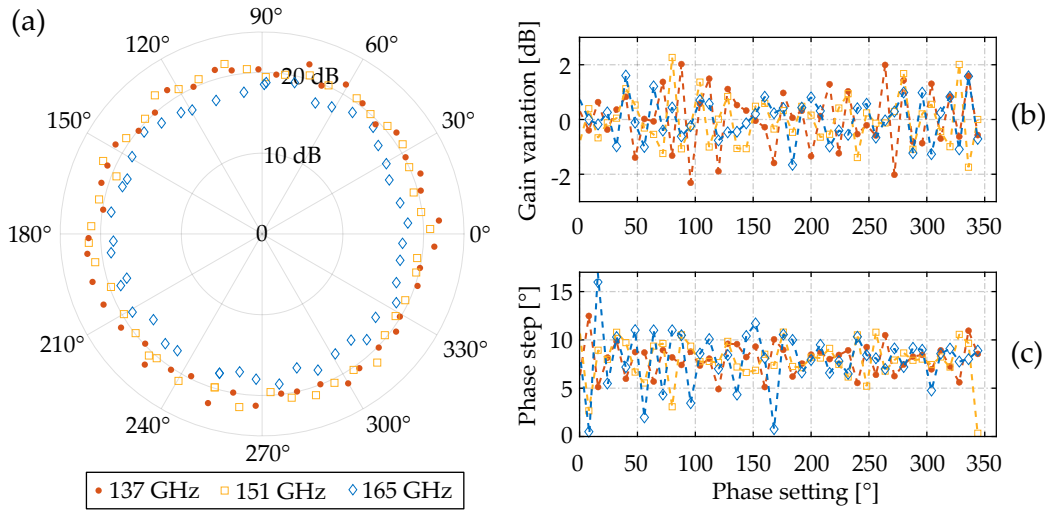
Figure 4.9: S_{21} on polar plot at the frequencies and settings used for offline calibration (a). Punctual gain variation (b) and phase steps (c) versus phase setting.
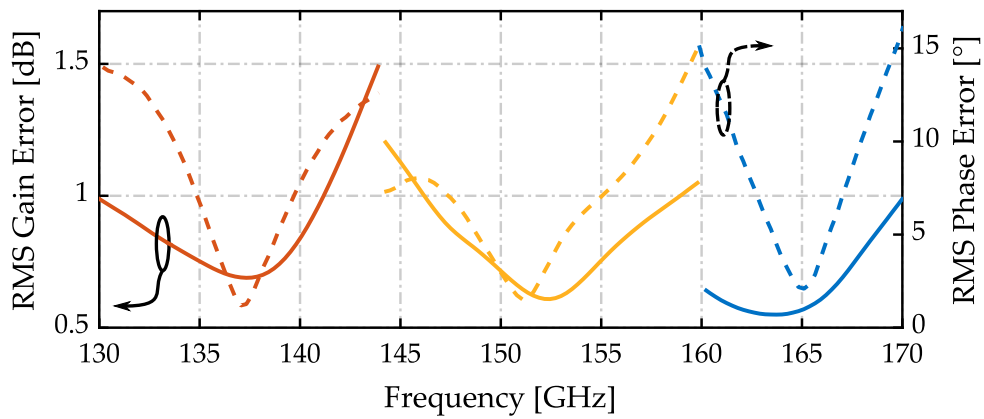

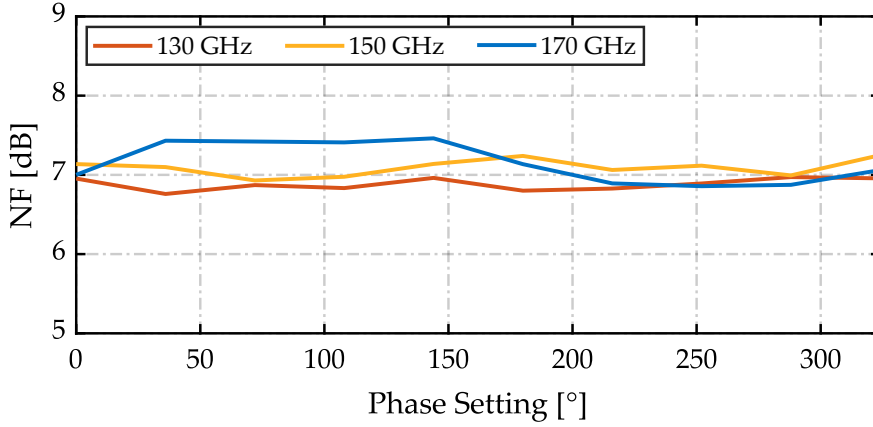Figure 4.10: RMS gain (solid) and phase (dashed) errors.

Figure 4.11: Measured NF at three frequencies versus phase settings (36°
average steps).

The noise figure measurements are carried out with a Farran WGNS-06
D-band waveguide noise source, a VDI WR6.5SAX-M frequency extender
and a PXA N9030A spectrum analyzer by Agilent. The setup was calibrated
at three frequencies (130, 150 and 170 GHz), and measurements performed
programming a 0° - 360° phase shift in 10 steps (i.e. with average phase steps
of 36°) at the three frequencies . The results are plotted in Fig. 4.11. The NF
ranges from 6.8 dB to 7.5 dB across frequency and at different phase shifts.
Gain compression measurements are performed with an ELVA-1 DPM-06 D-
band power meter in combination with an Agilent E8257D signal generator
and the VDI WR6.5-VNAX. The measured OP_{1dB} at 130, 150 and 170 GHz,
still spanning the 0° - 360° phase shift in 10 steps, is reported in Fig 4.12
and, at 130 GHz and 150 GHz, it is from -2 dBm to -1 dBm. OP_{1dB} drops to
-3.5 dBm at 170 GHz, for phase shift settings above 150°.

The experimental results are finally summarized in table 4.1 and com-
pared against previously presented RX front-ends designed for similar appli-
cations. With center operation frequency, bandwidth and gain aligned with
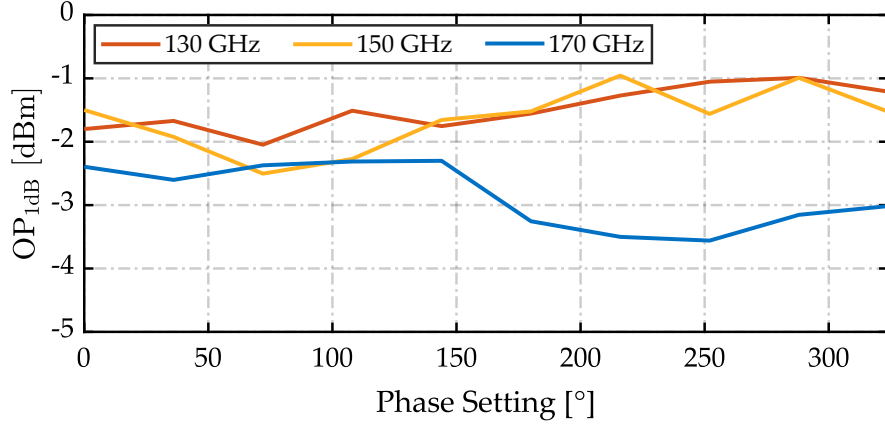state of the art, the presented front-end shows the lowest NF. The achieved

Figure 4.12: Measured OP_{1dB} at three-frequencies versus phase setting (36°
average steps).

Table 4.1: Comparison with the state-of-the-art

	This work	[47] RFIC2020	[15] LMWC 2018	[13] TMTT 2015	[14] SiRF 2017	[48] SSC-L 2021
SiGe Tech.	55 nm BiCMOS	130 nm	130 nm	120 nm	130 nm	130 nm
f_t/f_{max}	320 / 370	300 / 500	200 / 220	– / 270	250 / 340	300 / 500
f_0 / BW [GHz]	150 / 40	150 / 40	115 / 20*	92 / 8	125 / 14	140 / 60
BW [%]	26.7	27	17	9	11	42.8
Gain [dB]	20	22	13	30	12[§]	7.3
Ph. res. [°]	7	2	22.5	11	-	20[‡]
IP_{1dB} [dBm]	-22.5 / -21	-22	-17*	-37	-20.7	-30
OP_{1dB} [dBm]	-3.5 / -2	-1	-5*	-8	-9.7	-23.7
NF [dBm]	6.8 / 7.4	10	11*	8[†]	8[#]	9[†]
$P_{DC,MAX}$	80	165	53	80	125	436
Area [mm^2]	0.59	0.92	0.82	0.4	0.1	1.02
FoM [x 100]	**27.8 / 43.3**	10.1	7.4	4.3	2.5	0.02

* simulated   [†] T/R switches de-embedded   [§] baluns de-embedded   [#] LNA only   [‡] estimated from time-delay meas.

OP_{1dB} is remarkably higher than other works at comparable power consumption, except [47], which is demonstrating a slightly better compression performance but with twice the power consumption and 2.5 dB worst NF in a technology with higher f_t / f_{max}. For performance benchmarking, the figure of merit (FoM) introduced by ITRS for amplifiers is used [41], where the input power at 1dB gain compression, IP_{1dB}, is adopted instead of IIP3:

$$FoM = \frac{G_T \cdot IP_{1dB} \cdot f_0}{(F-1) \cdot P_{DC}} \qquad (4.1)$$

G_T is the power gain, f_0 the center frequency, F the noise factor, P_{DC} the power consumption, and all the quantities are expressed in linear scale. The FoM of the presented front-end is 3 times higher than previous works. Being the operation frequency similar to other works, the FoM advantage comes from the higher dynamic range normalized to power dissipation, i.e. the lower NF and higher gain compression point enabled by the use of programmable passive networks to implement the phase shifter. Notably, despite the intensive use of passive networks in this work, the layout footprint is very compact, being the occupied silicon area comparable or lower than the majority of other works.

Conclusions

This work presented a D-band receiver Front-End for phased-arrays. Its building blocks have been analyzed and their performance optimized to get the most out of the today's available technology.

An initial discussion on high-frequency amplifiers focused on the drawbacks of stagger tuning, in contrast to inherently broadband designs, and a sixth-order transmission-line-based matching network has been proposed for the realization of ultra-wideband amplifiers. The network can be approximated as a doubly-tuned transformer where the bandwidth is further extended leveraging the singularities introduced by the AC-coupling capacitor.

The gain limitation of common-emitters in high-frequency cascodes has been pointed out, and inductive feedback has been applied to a common-emitter device to trade gain for stability. The technique forces the transistor to operate in a conditionally stable region with gain above the device maximum available gain, thus enabling power gain boosting.

Several fine and coarse passive phase shifting blocks have been described. By cascading fine- and coarse-step PSs, a large programmable phase shift range can be covered maintaining the fine resolution in the phase control.

The concepts discussed above have been validated singularly on different test-chips and have finally been applied to the design of a receiver front-end.

The typical configuration comprising a LNA and a PS has been analyzed, focusing on the trade-off existing between noise figure and linearity. A two stage gain-boosted LNA with reactive feedback has been employed. Passive PS blocks and gain-boosted active cores have been interleaved to obtain a phase shifter with enhanced dynamic range. The combination of the LNA and the PS has demonstrated state-of-the-art noise figure and the highest power efficiency reported to date in similar works, proving the validity of the technique.

Acknowledgment

List of Own Publications

1. **G. De Filippi**, L. Piotto, A. Bilato and A. Mazzanti, "A SiGe BiCMOS D-Band LNA with Gain Boosted by Local Feedback in Common-Emitter Transistors," *2023 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), San Diego, CA, USA, 2023.*

2. **G. De Filippi**, L. Piotto, A. Bilato and A. Mazzanti, "A D-Band Low-Noise-Amplifier in SiGe BiCMOS with Broadband Multi-Resonance Matching Networks," *2023 18th European Microwave Integrated Circuits Conference (EuMIC), Berlin, Germany, 2023.*

3. **G. De Filippi**, L. Piotto, M. M. Pirbazari and A. Mazzanti, "D-Band RX Front-End with a 0°-360° Phase Shifter Based on Programmable Passive Networks in SiGe-BiCMOS" - ***submitted*** *to RWW Mini Special Issue of IEEE Transactions on Microwave Theory and Techniques, 2024.*

4. **G. De Filippi**, L. Piotto and A. Mazzanti, "A D-Band LNA Exploiting Ultra-Wideband Sixth-Order Matching Networks in SiGe BiCMOS," - *conference paper -* ***to be submitted***.

5. L. Piotto, **G. De Filippi**, D. D. Maistro, S. Erba and A. Mazzanti, "A K-band Gilbert-Cell Frequency Doubler with Self-Adjusted 25% LO Duty-Cycle in SiGe BiCMOS Technology," *ESSCIRC 2022- IEEE 48th European Solid State Circuits Conference (ESSCIRC), Milan, Italy, 2022.*

6. L. Piotto, **G. D. Filippi**, G. Brozzetti, D. D. Maistro, S. Erba and A. Mazzanti, "A 14–32 GHz SiGe-BiCMOS Gilbert-Cell Frequency Doubler With Self-Adjusted Reduced Duty-Cycle Performance Enhancement," *in IEEE Journal of Solid-State Circuits, 2023.*

7. L. Piotto, **G. D. Filippi**, A. Bilato and A. Mazzanti, "A 20mW 130-175GHz Phase Shifter with Meandered $\lambda/2$ TLINEs in BiCMOS 55nm," *ESSCIRC 2023 - IEEE 49th European Solid State Circuits Conference (ESSCIRC), Lisbon, Portugal, 2023.*

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