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Design and Stability Analysis of a Three-Phase Triple-Stage Solid-State Transformer

a dissertation submitted for
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Contents

Abstract

The electrical distribution system is experiencing a profound evolution process triggered by the increasing integration of Renewable Energy Sources (RES) and Distributed Generation (DG), alongside the widespread use of Electric Vehicles (EVs), the related charging stations, and the growing adoption of Energy Storage Systems (ESSs). The behavior of such loads and sources, interfaced with the grid via an increasing number of power electronics converters and often intermittent in nature, together with a bidirectional power flow requirement, poses new challenges for the reliable and safe operation of the distribution system. In this context, the concept of Internet of Energy (IoE), or Energy Internet (EI), has emerged and is nowadays widely discussed in the literature as a new paradigm shift to address the growing demand for modernization of the current distribution network. The goal in the IoE scenario is reshaping the current distribution grid into an intelligent and flexible active network, both through a radical informatization process that involves the renewal of the grid communication infrastructure and the addition of distributed monitoring points and via the implementation of advanced energy management and control functionalities to enable the safe, robust, effective, and efficient integration of intermittent sources and loads.

At the core of this future smart grid scenario, the Solid-State Transformer (SST) is envisioned as the best candidate due to its flexibility and advanced control features. This is because the SST is a power electronic-based transformer capable of providing advanced services and grid-supporting features, besides galvanic isolation and voltage adaptation, through its control system, and therefore is intended for replacing conventional Line Frequency Transformers (LFTs) at strategic nodes of the grid. Moreover, the core isolation stage of the SST operates at high frequencies and, therefore, it enables volume and weight reduction of the whole system compared to traditional and bulky LFTs.

In the IoE scenario, the most suitable SST configuration is the triple-stage one, which consists of three conversion stages. Due to the large number of stages, the SST control is intrinsically complex. It has been shown in the literature how the coupling among controllers makes the design of the overall control system challenging and, additionally, multistage cascaded converters are significantly prone to instability due to interaction between converters. Moreover, even if the SST is stable as a standalone system, it may become unstable when connected to the grid because of dynamic interactions with other grid-connected converters, leading to the so-called harmonic instability phenomenon.

In this context, this thesis aims to explore the SST stability issue from both the DC-link and grid-connection perspectives. To do so, in the first part of this work, the SST suitable topologies and their conversion stages are reviewed. Once the SST architecture is selected, the main ratings and parameters are designed according to the presented IoE application requirements. An average model of the converter, that enables faster simulations and physical insights into the SST dynamics, is then derived. Through it, the small-signal model of the SST can be obtained. Based on that, the SST control system is presented and designed and the related impedance model is derived. The latter is selected as assessment tool to evaluate the DC-link and grid-connection stability of the SST under investigation. The results obtained provide support during the design phase of the SST and its control strategy, with the aim to achieve a stable grid-connected operating system.

Abbreviations

AC Alternate Current.

AFE Active Front-End.

B2B-PM Back-to-Back Power Module.

CC Current Controller.

CHB Cascaded H-Bridge.

CVC Cluster Voltage Controller.

DAB Dual Active Bridge.

DC Direct Current.

DG Distributed Generator.

DSCC Double-Star Chopper-Cell.

EI Energy Internet.

ER Energy Router.

ESS Energy Storage System.

ET Electronic Transformer.

EV Electric Vehicle.

FACTS Flexible AC Transmission System.

FB Full Bridge.

GVC Global Voltage Controller.

HFT High-Frequency Transformer.

HV High Voltage.

IoE Internet of Energy.

IPOP Input-Parallel Output-Parallel.

IPOS Input-Parallel Output-Series.

ISOP Input-Series Output-Parallel.

ISOS Input-Series Output-Series.

LFT Line Frequency Transformer.

LV Low Voltage.

LVC Local Voltage Controller.

LVRT Low Voltage Ride-Through.

MAB Multiple Active Bridge.

MMC Modular Multilevel Converter.

MMCC Modular Multilevel Cascaded Converter.

MP-SST Multi-Port Solid-State Transformer.

MV Medium Voltage.

NPC Neutral Point Clamped.

OLTC On Load Tap Changer.

PCC Point of Common Coupling.

PEBB Power Electronic Bulding Block.

PET Power Electronic Transformer.

PETT Power Electronics Traction Transformer.

PFC Power Factor Correction.

PI Proportional Integral.

PLL Phase-Locked Loop.

PQ Power Quality.

PS Phase Shift.

PV Photovoltaic.

PWM Pulse-Width Modulation.

QAB Quadruple Active Bridge.

RES Renewable Energy Sources.

RMS Root Mean Square.

SRC Series Resonant Converter.

SSBC Single-Star Bridge-Cell.

SST Solid-State Transformer.

ST Smart Transformer.

STATCOM Static Synchronous Compensator.

TAB Triple Active Bridge.

THD Total Harmonic Distortion.

VSC Voltage Source Converter.

VSI Voltage Source Inverter.

WBG Wide BandGap.

ZCS Zero-Current Switching.

ZVS Zero-Voltage Switching.

Chapter 1

Introduction

In recent years, the public awareness regarding environmental issues and global resource limitations has increased as a result of global warming and climate change. This led to a strong focus on promoting renewable energy sources and enhancing energy efficiency in political agendas, exemplified by initiatives like the now passed *Europe 2020* strategy [1] which is currently driven forward by new climate targets defined within 2030 and also 2050 [2]. To this extent, besides the goals defined within the year 2020, i.e. the reduction of greenhouse gas by 20% compared to the levels of 1990 by means of 20% increase in energy efficiency and in integration of Renewable Energy Sources (RES) on the total gross energy consumption, current binding targets endorsed by the European Council are the net domestic reduction of greenhouse gas emissions by at least 55% within 2030 (compared to 1990 levels) and the European Union climate neutrality by 2050. The latter means achieving net zero greenhouse gas emissions for European countries as a whole, mainly by cutting emissions, investing in green technologies and protecting the natural environment [3].

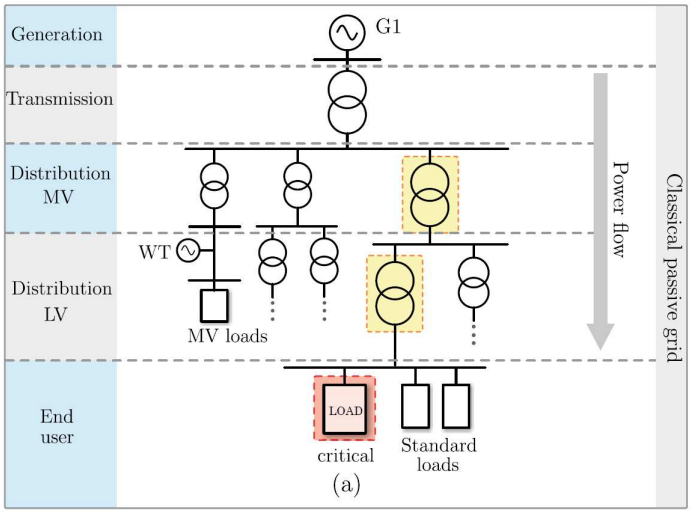
The increasing share of RES helps reduce the fossil fuel utilization which are responsible of polluting gases emissions, supporting the so-called energy transition towards a cleaner sources. Therefore, RES play a vital role in reducing the emissions of greenhouse gases. However, their integration in the utility grid is not straightforward. In traditional grid, the power is generated in large central plants and it is distributed through transmission and distribution networks, in which the voltage level usually decreases when moving from sources towards loads. Typically, these are directly connected to the distribution

grid, i.e. at Medium Voltage (MV) level, in case of high power demand or to the Low Voltage (LV) distribution grid when residential loads. Hence, the traditional distribution network has been established as a passive network in which the power flow is unidirectional, i.e. from the large power plants to the end users. On the other hand, except for hydro power plants, other major RES like wind and solar cannot be easily centralized. Furthermore, their availability depend on weather conditions, thus it shows fluctuating and intermittent behavior. Those aspects pose new challenges for the penetration of RES in the current distribution grid. This has led to the concept of distributed generation where renewable sources are connected to distribution grids at remote locations.

In the last years, with the evolution of power electronics, the integration process of such Distributed Generator (DG) have been greatly developed. Therefore, nowadays a large number of RES are connected to the grid at different voltage levels (either LV or MV) and at various and remote locations. Usually, they are placed near the loads so as to reduce transmission line congestion and thus losses. However, the extensive deployment of DGs can negatively impact grid reliability and power quality. Factors like voltage fluctuations, especially evident during abrupt changes in DGs output caused by weather shifts, and the lack of synchronization between DGs output power and load profiles (particularly noticeable with wind energy systems), can contribute to the distribution network congestion if not properly managed, etc. To mitigate those negative effects, Energy Storage Systems (ESSs) are increasingly being incorporated into the grid to store excess energy produced by DGs and thus improve the grid power quality. For instance, battery storage systems can charge during off-peak hours when electricity costs are low and discharge during peak demand periods, smoothing out load profiles and alleviating distribution line congestion. Furthermore, even more recently the rise of Electric Vehicles (EVs) technology has necessitated the installation of charging stations into the distribution grid to meet the EV demand. However, while EV integration shares similarities with storage systems features in terms of grid reliability, the rapid charging times requested from EVs can strain the distribution network, leading to increased peak demand and potential congestion.

The increasing adoption of these systems along with the widespread penetration of RES has reshaped the infrastructure of the electric distribution network, resulting in a more complex system that largely relies on power electronics devices. Furthermore,

the legacy concept of passive network should be revised to meet with current grid requirements, in which the power flow is no longer exclusively unidirectional, but it can be bidirectional. Consequently, the network has transitioned into an active network as Fig. 1.1b shows, posing new challenges related to power quality, reliability, and voltage regulation.



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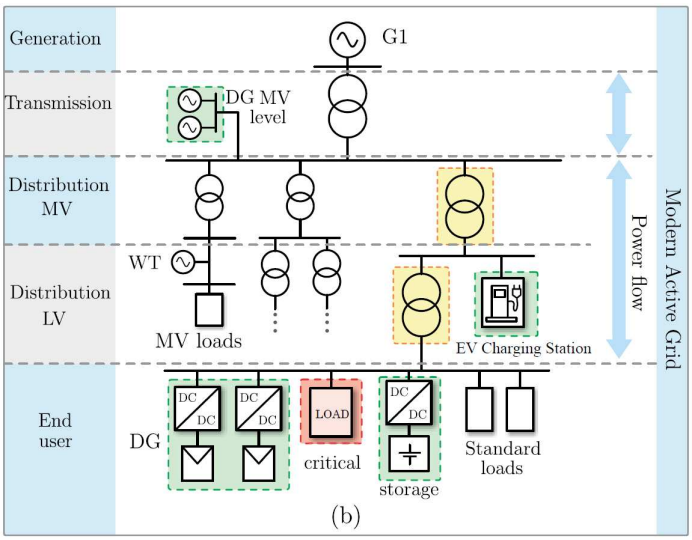


(b)

Figure 1.1: The evolution of electric distribution network driven by modernization: (a) legacy passive network in which the power flow is unidirectional, i.e. from sources to loads and (b) modern active distribution network dominated by bidirectional power flows and power electronics-based system [4].

In order to address the aforementioned challenges, power electronics is becoming more vital to enhance the distribution grid with controllability and flexibility features, making it a *Smart Distribution Grid*. Besides power converters that interface RES with the grid, devices such a Flexible AC Transmission System (FACTS), Static Synchronous Compensator (STATCOM), etc. are nowadays widely adopted (in recent times also in combination with ESS) to improve the power quality and the voltage regulation of the grid. In this context, a crucial component of the traditional distribution network is the Line Frequency Transformer (LFT), which is responsible of galvanic isolation and voltage scaling between different networks. Despite its high efficiency (which for oil-filled MVA transformers is typically well above 99% for most of the load range [5]) and relatively long lifetime (around 30 years [5]), traditional LFTs lack of control and hence they are not suitable to be deployed in the active network scenario described by Fig. 1.1b. Usually, the most standard solution to provide a form of voltage regulation for LFT is the implementation of On Load Tap Changers (OLTCs). However, they offer limited regulation range and poor dynamic performances and also this solution cannot provide any sort of regulation on the power flows, etc.

Therefore, being the transformer a key element of the network, its upgrade would help to support and promote the network modernization process that is ongoing in recent times. It is in light of this that the concept of Solid-State Transformer (SST) began to spread and to be discussed as a promising solution in replacing the conventional LFT since the early 2000s [6–14]. Also known in literature as Electronic Transformer (ET) or Power Electronic Transformer (PET), the SST technology originates as the advancement of a traditional LFT through the implementation of power electronics devices. The idea behind the SST is to achieve voltage conversion and galvanic isolation between two AC lines through a High-Frequency Transformer (HFT), while the low-frequency input and output ports are coupled to the HFT via one or more cascaded power electronic converter stages. Compared to conventional line-frequency transformers, an HFT can achieve reduced volume, weight, and cost, thus allowing for a fully modular, scalable, and compact conversion system. In addition, the presence of controlled power electronics allows the implementation of advanced and flexible control features and grid services, such as bidirectional power flow, reactive power support, voltage regulation, harmonic compensation,

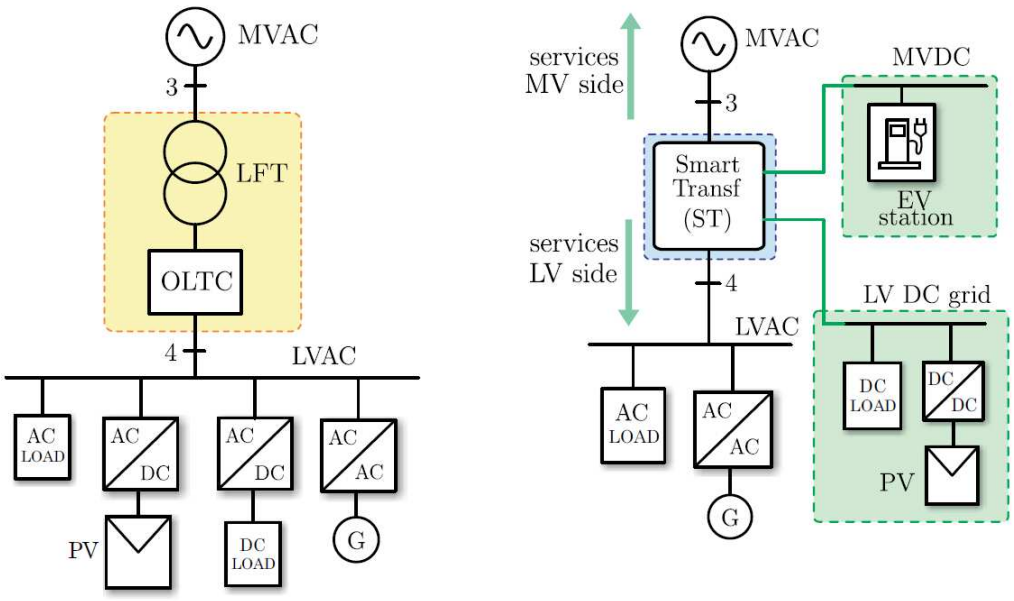
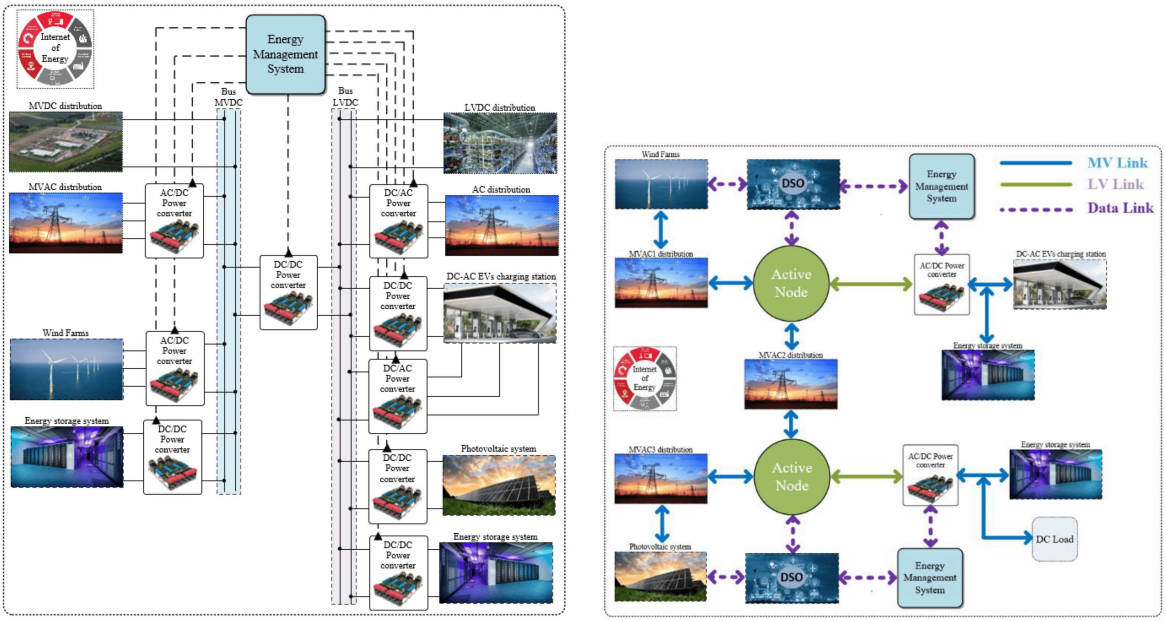


Figure 1.2: Modernization trend of the distribution grid based on the Solid State Transformer deployment:(a) traditional distribution grid based on the LFT, (b) modern distribution grid based on the SST [4].

power factor correction, etc. [15]. Thus, in addition to voltage scaling and galvanic isolation, a SST can provide volume, weight and costs reduction along with controllability functionalities of voltage and current. This features allows the SST technology to be promising and beneficial in a wide range of applications, such as traction, smart distribution grid, AC/DC micro- or nanogrids and in emerging fields like data centers and fast charging stations [5, 16–20]. Fig. 1.2 shows the modernization process of the current distribution grid by means of SST technology.

Recently, the latest evolution of the *Smart Distribution Grid* scenario brought to the so-called concept of Internet of Energy (IoE), or Energy Internet (EI), which is now being actively discussed in the literature as the last paradigm shift for the evolution of the current distribution system [12, 21–23]. The goal in the IoE scenario is reshaping the concept of *Smart Distribution Grid* into an intelligent and flexible active network, both through a radical informatization process that involves the renewal of the grid communication infrastructure and the addition of distributed monitoring points and via the



(a) (b)

Figure 1.3: The Energy Router Multi-Port Solid-State Transformer in the Internet of Energy scenario: (a) DC distribution, (b) AC distribution [15].

implementation of advanced energy management and control functionalities to enable the safe, robust, effective, and efficient integration of intermittent sources and loads. In this context, the implementation of intelligence together with the communication and control functionalities make the SST to act in the IoE scenario much like an Energy Router (ER). As an Energy Router (ER), the SST allows plug-and-play access to the network, proper integration of RESs, and the deployment of smart power dispatching and management features [12, 24, 25]. For such a purpose, the ER-SST works effectively as an active node of the distribution grid. To fully exploit its role within the modern grid, it should provide multiple ports for the integration of various local sources and loads. This is because connecting multiple loads and sources to these types of SST configurations, a large number of additional converters are required to properly interface with the available AC and/or DC buses provided by the SST, drastically affecting the overall system efficiency and reliability. For this purpose, to meet the demand of such IoE scenario, Multi-Port Solid-State Transformer (MP-SST) represents the evolution of the SST technology, that fits optimally in the IoE framework [21]. It represents an advancement in the SST technology and enables the integration of RESs, DGs and ESS through suitably isolated ports within

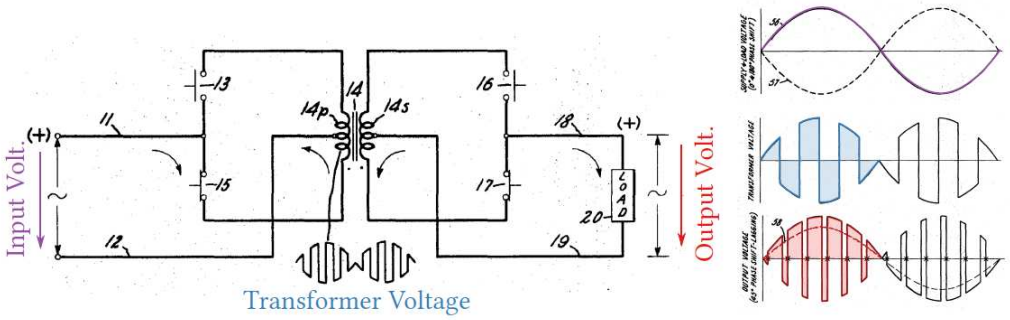
one single adjustable, modular and compact configuration, thus minimizing the number of components involved in the power conversion and increasing both the power density and reliability of the whole system [15, 18, 23, 25].

In the next, the SST main applications, topologies and future developments will be comprehensively presented and discussed.

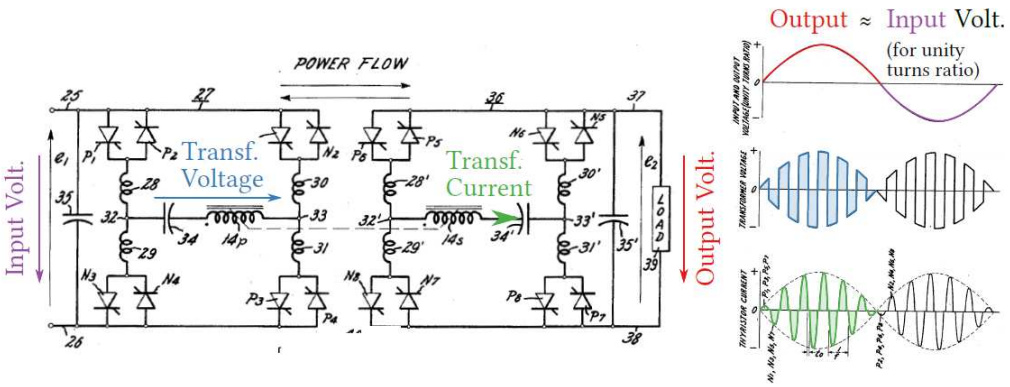
1.1 The Early Developments of the Power Electronic Transformer

The early concept of SST was firstly introduced by E. McMurray in 1968 with the US patent "converter circuits having a high frequency link" [26]. The main goal of the proposed topology was to introduce a power supply converter that was able to adjust the output voltage while also reducing the volume and weight of the converter stage. This was achieved by mean of a non-isolated topology incorporating a HFT as Fig. 1.4a shows. Later, in order to facilitate the commutation of at the time available semiconductors, i.e. thyristors, a resonant variant of that topology was proposed in [27] as Fig. 1.4b shows. The benefits of volume and weight reduction, more that the capability of the voltage regulation, led years later to the first ever significant application that took advantage of this concept, a Power Electronics Traction Transformer (PETT) for railways application [14, 28]. This is because many railways networks based on AC transmission work at very low frequency, for instance $16^2/_3$ Hz in Switzerland [5, 28], in order to reduce the inductive behavior of the AC network that is less dominant at low frequencies. McMurray's topology found then application in reducing the size of the traditional LFT that was installed on locomotives. This is achieved since the magnetic components volume and weight decrease as the working frequency is increased [29]. This resulted in a lighter and smaller on board traction transformer, which shows also higher power density and efficiency hence being more competitive [14, 19, 28].

While the main advantages brought by the early SST prototypes where mostly at hardware level (i.e. size and weight reduction), at the same time researchers began working also on software level, i.e. on specific control architectures, to assess the feasibility of such system for distribution/utility grid applications. Among many projects, the UNIFLEX-



(a)



(b)

Figure 1.4: (a) Non-resonant AC-AC power converter with a HF link as proposed in 1968 by McMurray [26]; and (b) resonant variant mploying the half-cycle discontinuous conduction mode, from a patent filed by McMurray in 1968 [27]. Colors in converter waveforms are added by the author of [30].

PM at first and later the FREEDM were two large ones that have investigated this possibility [13, 31].

The "*Advanced Power Converters for Universal and Flexible Power Management in Future Electricity Networks*" project, namely UNIFLEX-PM, was a research project supported by the European Community under the 6th Framework Programme aimed to research and experimentally verify new innovative power conversion architectures for universal application in the future European electricity network. It successfully demonstrated the possibility of a SST-based interconnected transmission network. On the other hand, the "*Future Renewable Electric Energy Delivery and Management System*", namely FREEDM, analyzed the features of plug-and-play of distributed renewable energy and in-

tegration of distributed energy storage devices in the future electric power distribution system by means of a SST. It was in this time that the EI concept was envisioned for the future distribution network and matched with the SST technology [12, 15]. These advances in SST technology drew the attention of both academic and industrial communities, leading the Massachusetts Institute of Technology (MIT) to cite it as one of the most emerging technologies in 2010 [16].

In more recent times, the development of more advanced control and communication features demanded by the distribution grid modernization, resulted in a further evolution of SST concept, that is the Smart Transformer (ST) [32]. The efficiency, reliability and advanced communication and functionalities are at the heart of the "*The Highly Efficient And Reliable Smart Transformer, a new Heart for the Electric Distribution System*" project, namely HEART, founded by the European Research Council under the 7th Framework Programme.

These relevant and interesting SST projects, along with the prototypes that has been built, will be discuss in details in the following paragraphs.

1.2 Key Features of Solid-State Transformers

Over the past two decades, solid-state transformer technology has undergone significant advancements, leading to the analysis and development of numerous topologies, systems, and applications. The development of SST technology as core component of future smart distribution grids has been the focus of several ongoing projects, in which the SST can facilitate the integration of energy storage systems or renewable energy sources like Photovoltaic (PV), wind etc. into the grid, or it can control the power routing and make local microgrid energy management easier.

Beside its role in smart distribution grids, SST has gather attention for its potential applications in environments characterized by severe volume and weight restrictions. For instance, traction applications have emerged as a prominent field of application for SSTs thanks to the benefits brought by the HFTs over the traditional bulky LFTs. As said in the previous paragraph, in traction applications the employment of a SST enables volume and weight reduction improving both power density and efficiency, which are key

requirements for different traction manufacturers [5, 14].

Based on the potential SST application fields, researchers have identified several key characteristics that modern SST systems must provide in order to fulfill the applications requirements. These common characteristics can be summarized as:

- Connection to MV: modern SSTs must interface with MV levels, whether AC or DC. This is a direct consequence of the high power demand requested by current SSTs applications such as traction or smart distribution grids. For this purpose, SSTs must provide at least one MV connection port;

- Galvanic isolation and potential separation by means of HFT: as already pointed out in this section, by increasing the operating frequency of a transformer (and, in general, of any magnetic component) it is possible to reduce its volume and weight without increasing the current density and/or the peak core magnetic flux (and thus worsen the efficiency). Therefore, at the same power rating, an HFT is less bulky and more efficient than the LFT one [5, 29]. This can be seen by considering the product of the transformer core area A_{core} with the winding window area A_{wdg} as follows [29]:

$$A_{\text{core}}A_{\text{wdg}} = \frac{\sqrt{2}}{\pi}\frac{P}{kJ_{\text{rms}}\hat{B}_{\text{max}}f} \quad \rightarrow \quad V \propto (A_{\text{core}}A_{\text{wdg}})^{\frac{3}{4}} \propto \frac{1}{f^{3/4}}; \tag{1.1}$$

  where V is the transformer volume, k is the windings factor, J_{rms} is the Root Mean Square (RMS) value of the windings current density, $\hat{B}_{\text{max}}$ is the peak value of the core magnet flux and f is the working frequency. As can be noted from eq. (1.1), the transformer total volume decreases with the increase of the working frequency f. As aforementioned, this key characteristic is particularly significant in applications characterized by space and weight constraints, such as traction systems. Recent advancements in traction technology, including distributed propulsion and high-speed trains, have further valued the significance of medium-frequency isolation in SST design.

- Controllability: unlike conventional transformers, SSTs offer controllability functionalities, enabling regulation of both input and output current and voltage waveforms, power flows and enabling advanced and ancillary services like power factor

correction, reactive power compensation, frequency regulation, harmonics and disturbances rejection, etc. These set of advanced control features are of particular interest nowadays and find especially application in the smart distribution grid field, allowing the proper integration of RESs and ESSs systems.

In light of these key characteristics, contemporary SSTs represent a paradigm shift in power distribution system technology, playing a crucial role in shaping the future of energy distribution and consumption.

1.3 Modern Solid-State Transformers Architectures

Several SST architectures are proposed and discussed in the literature as best candidates to replace the traditional LFT. However, the selection of the ST architecture is directly impacted by system level requirement such as efficiency, redundancy, reliability and so on. For instance, in case of distribution system applications, the main issue is the combined effect due to the high penetration of RESs and DGs, such as solar and wind power [4,33]. Thus, in order to maintain power system stability and integrity, the SST should:

- Improve the distribution network power quality even in presence of unbalanced, non-linear or perturbed loads, by ensuring symmetrical and balanced phase currents and unity power factor;
- Avoid the propagation of faults and disturbances such as voltage sags, harmonics, etc. towards the main power system by keeping them localized;
- Allows the direct connection to future MVDC power transmission and the integration of low voltage DC grid, ESSs, and RESs.

Fig. 1.5 provides an overview of the common SSTs architectures based on the classification presented in [8] and [34].

1.3.1 Single-Stage Topologies

The simplest configuration of a SST is represented by its single-stage topology, which uses transformer isolation in conjunction with direct power conversion to step down HV

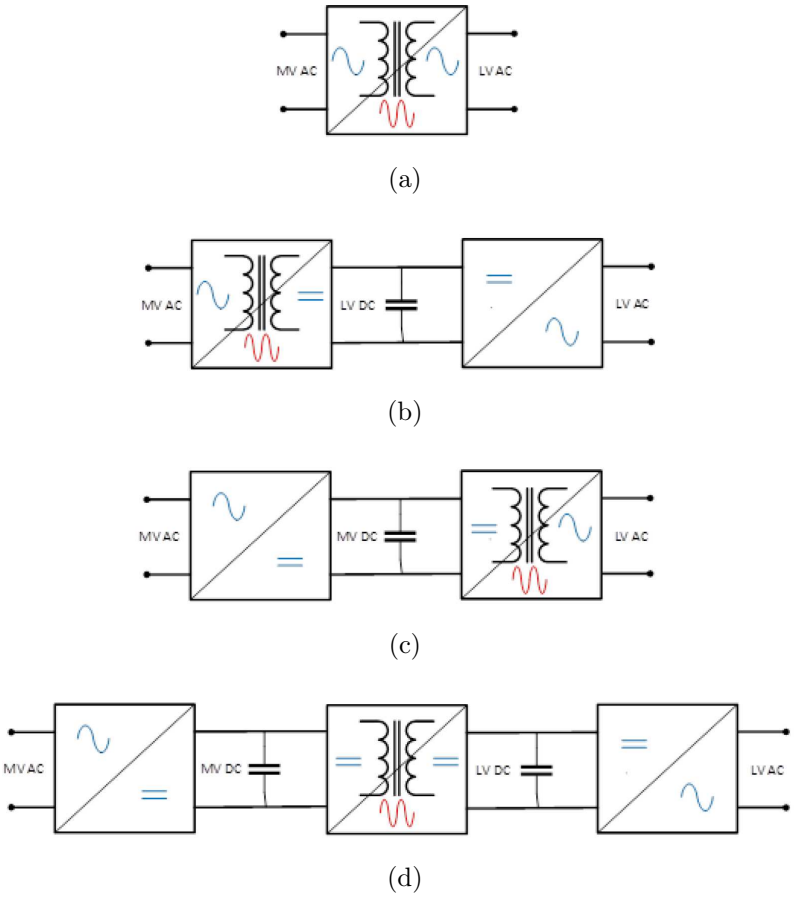


Figure 1.5: Solid-state transformer architectures classification: (a) Single-Stage SST topology; (b) and (c) Double-Stage SST topology with respectively MV and LV DC-links; (d) Triple-Stage SST topology [15].

to LV. With no conduction or switching losses, this topology—which functions with direct DC-DC or AC-AC power conversion stages—offers improved efficiency and dependability over the three-stage SST topology. Electrolytic capacitors are not required because of its high switching frequency operation. The direction and amount of power transfer in this topology are controlled by the phase shift angle between the secondary and primary bridges, allowing for bi-directional power flow with four-quadrant switches to improve control strategy and manage harmonic content.

A small phase shift between the input and output voltages happens during steady-state operation because of the characteristics of the load and output filter. In addition, the output voltage maintains a constant ratio independent of the direction of the transformer current and the polarity of the input voltage by following the sinusoidal waveform of

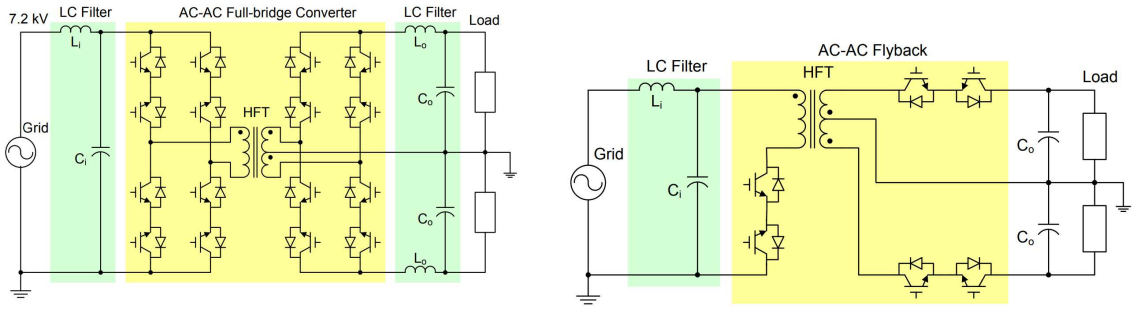
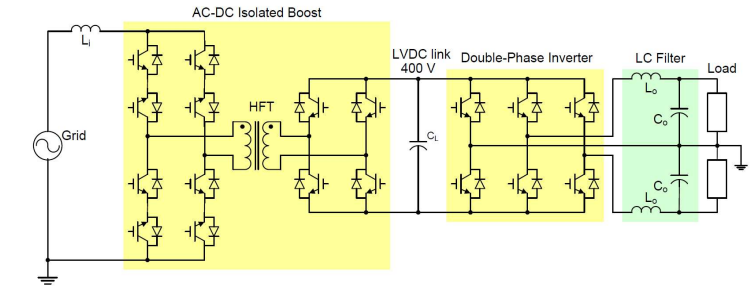


Figure 1.6: Single-Stage SST topologies: (a) AC-AC full-bridge converter (b) AC-AC Flyback converter [34].

the input voltage. A straightforward control mechanism to convert power into a high-frequency square wave with a 50% duty cycle and rectify it to a sinusoidal waveform on the LV side is shown by the AC-AC full-bridge converter shown in Fig. 1.6a. In the meantime, Fig. 1.6b shows the flyback converter, which has few switches but is not equipped with power factor correction in the DC-link and experiences voltage stress on the switches. Because SSTs are designed to operate optimally at MV levels, 7.2 kV AC, for example, multiple LV converters are connected in series to distribute power and voltage in modular multilevel configurations. However, power and voltage balancing becomes difficult in these systems due to their intricate configuration. Consequently, in order to reduce system complexity and control schemes, a two-level approach is adopted within the single-stage design.

1.3.2 Double-Stage Topologies

The main difference between a two-stage SST and a single-stage SST is the presence of a DC-link, which can be placed on the LV or HV side. On the LV side of the AC-DC converter, an uncontrolled rectifier can be used to change the bidirectional power flow to unidirectional power flow. However, a lot of switching devices and a sophisticated switching methodology are required for this topology. The two-stage SST has benefits like reactive power compensation even though it increases system complexity. It is difficult to maintain Zero-Voltage Switching (ZVS) over such a broad input range, which makes the two-stage SST with an LVDC link inappropriate for HV operation. While renewable



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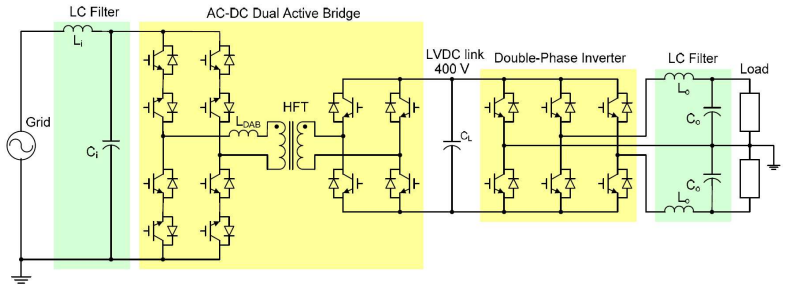


(b)

Figure 1.7: Double-Stage SST topologies: (a) AC-DC isolated boost converter (b) AC-DC DAB converter [34].

applications in LV are limited by the lack of an LVDC link, this problem can be addressed by converting HVDC to LVDC rather than LVAC. As an alternative, these issues can be resolved with the three-stage SST topology. Recently, a novel three-phase, four-wire output, AC-AC high-frequency matrix type SST was proposed [35]. In this design, the utility source voltage is converted into 50% duty square wave pulses using Pulse-Width Modulation (PWM). These pulses are then transmitted via a single-phase high-frequency transformer. Numerous advantages come with this configuration: galvanic isolation, high power density, controllable input power factor, flexible voltage transfer ratio, bidirectional power flow, and high power density. Additionally, by utilizing modified three-dimensional spaced vector PWM, the topology can lower harmonic distortion in both input and output currents under unbalanced load conditions.

1.3.3 Triple-Stage Topologies

The advanced features of the triple-stage SST topology have made it more and more popular in research. This SST offers optimized performance in both distribution and

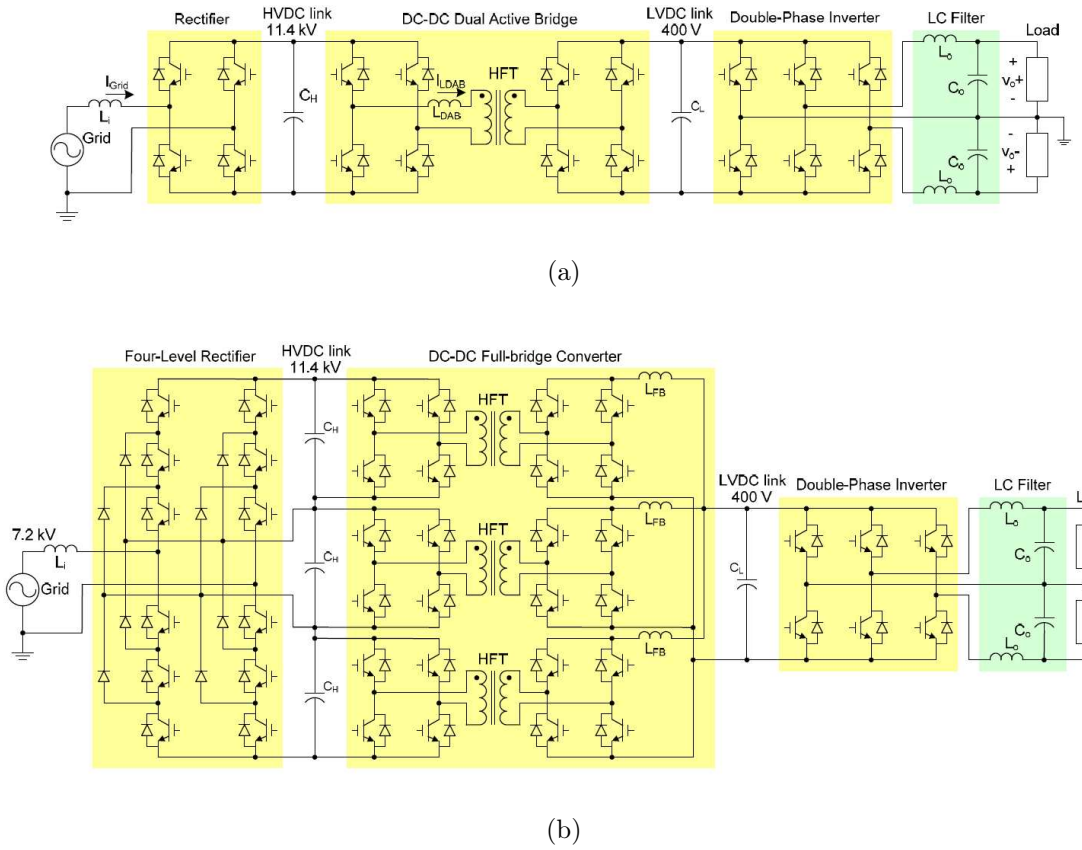


Figure 1.8: Three-Stage SST topologies: (a) AC-DC isolated boost converter (b) AC-DC DAB converter [34].

transmission grids, in addition to its small size and light weight. These topologies include two DC links, which can accommodate devices in the MV and LV domains and effectively address Power Quality (PQ) issues. In particular, the three-stage topology works better in terms of power factor control, protection, voltage regulation, and current limitation than the single-stage and two-stage configurations. The integration of energy storage systems and renewable energy sources has been made easier by the emergence of numerous SST initiatives. Fig. 1.8 shows two different implementations of a three-stage SST. A minimum of two power converters, such as an MV frequency converter and an LV converter, make up the architecture of the three-stage SST. Three-stage SSTs, with their bidirectional power flow that allows power to be transferred from LV to HV, were mainly developed for smart grid applications before. Subsequent subsections provide more detail on each stage's distinct attributes.

Based on the power conversion stages classification, Table 1.1 summarizes the main

capabilities and features supported by each SST topology presented before [18, 34]. *

Table 1.1: Functional and regulation capabilities supported by the standard SST architectures defined in Fig. 1.5.

Functionality	Single-Stage	Double-Stage	Triple-Stage
Bidirectional power flow	✓	✓	✓
Input current limiting	✗	✓	✓
Output current limiting	✗	✓	✓
Input current Regulation	✗	✓✓	✓✓✓
HVDC link regulation	N/A	N/A	✓✓
LVDC link regulation	N/A	✓✓	✓✓✓
Input voltage sag ride through	✓	✓✓	✓✓✓
Output voltage regulation	✓	✓✓	✓✓
LVDC undervoltage protection	N/A	✓	✓
LVDC overvoltage protection	N/A	✓	✓
HVDC undervoltage protection	N/A	N/A	✓
HVDC overvoltage protection	N/A	N/A	✓
Modularity implementation	Simple	Hard	Simple
Reactive power support	✗	✓	✓
Power factor correction	✗	✓	✓
Frequency regulation	✗	✓	✓

*Table legends: ✓ = yes or poor; ✓✓ = good; ✓✓✓ = very good; ✗ = No; N/A = Not applicable.

1.3.4 Additional Topology Classification

Another classification that can be made for SST-based systems is based on the modularity. Based on that, SSTs can be classified in modular, non-modular or semi-modular [4]. When interfacing a distribution grid, a MV level need to be handled by the system. In this case, a common approach is to employ a modular solution by connecting several basic converters - i.e. for example H-Bridges (FBs) - rated for lower voltage or currents. This brings several advantages, like reduced voltage and current stresses on devices, scalability, redundancy, the possibility to use standard, tested and well-estabilished components already available on the market and the implementation of fault-tolerant strategies [4].

Therefore, when a modular structure is adopted, an additional common classification based on the SSTs module connection is shown in Fig. 1.9 [16]. In this regard, defined a

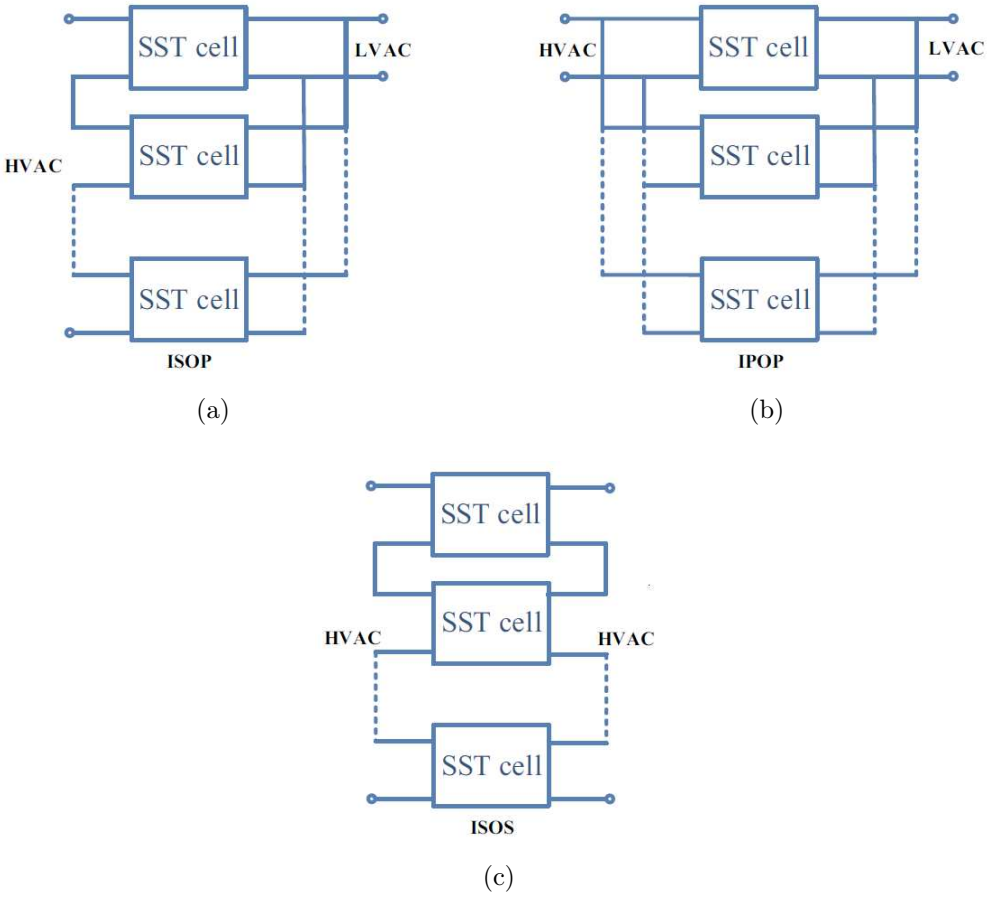


Figure 1.9: Solid-state transformer architectures classification based on the basic cells connection: (a) ISOP connection; (b) IPOP connection; (c) ISOS connection [16].

base Power Electronic Bulding Block (PEBB) of the converter, which is the key element that is replicated many times to build the full topology, it can be connected either in series on in parallel with other PEBBs to cope respectively with voltage and current system requirements as Fig. 1.9. This gives rise to three different possible connections, namely Input-Series Output-Parallel (ISOP) connection required to handle MV levels at the input and high currents at the output (load side), Input-Parallel Output-Parallel (IPOP) connection required to handle a LV high power system and Input-Series Output-Series (ISOS) connection needed to interface two HV systems. Note that the Input-Parallel Output-Series (IPOS) is not mentioned here because it is equivalent to ISOP connection and, also, is not common nor practical at all to interface a MV load to a LV grid.

1.4 Challenges and Future Trends

As outlined in this Paragraph, SSTs are power electronics-based advanced transformers aimed to replace conventional bulky LFTs. Their primary benefits are that they decouple the MV from the LV grid, offer galvanic isolation while also being scalable, modular, controllable, and facilitating the effective integration of MV and LV AC and DC systems [5, 15, 19]. However, they are more expensive due to their advanced capabilities and also more complex, requiring more maintenance than conventional transformers.

However, in 1000 kVA class SSTs are considerably more expensive and less efficient than typical LFTs used in distribution grids, leading to higher operating costs. While SSTs offer full-range control of input and output voltages and currents, they are not well suited for typical AC-AC grid applications due to efficiency challenges and compatibility issues with existing LV AC grid protection infrastructure. However, they may find use in niche applications where weight and space constraints are critical or where MVDC-LVDC conversion is needed. In this context, the concept of hybrid transformers, which combine power electronics devices and thus controllability features with traditional highly-efficient and robust LFT, is highlighted as possible feasible solution until SSTs efficiency become competitive with LFTs one (e.g. by means of Wide BandGap WBG devices) [5].

Development cycles for SST technology in traction applications span several decades, with prospects for accelerated cycles due to increased experience and advanced design

tools. In contrast, development cycles for grid applications are expected to be slower due to the less established nature of power electronics in this context and the longevity of existing infrastructure. Future research should focus on quantifying the system-level benefits of SSTs in distribution grids and investigating active protection concepts for both AC and DC grids. Despite current challenges, if efficiency and cost challenges can be addressed, as already discussed in Section 1 SSTs could play a significant role in smart grids as Multi-Port Energy Hubs and as key components in hybrid grids integrating AC and DC technologies (i.e. MP-SSTs). However, fundamental questions remain regarding the conceptual shift towards intelligent energy hubs and the balance of control tasks in future grids. Increased collaboration between power electronics and power systems engineers is essential to address the interdisciplinary challenges in designing future power grids.

Based on the above, the concepts of hybrid transformers and MP-SSTs are worthy of being discussed in more detail.

1.4.1 Hybrid Transformers

As evidenced by the successful deployment of voltage regulation distribution transformers, there's often a need for some level of controllability, although not necessarily the complete control over voltages and currents achievable with SSTs. Consequently, hybrid transformers—which combine a powerful and highly efficient LFTs with a power electronic converter that can provide the required controllability without processing the bulk power—might be a compelling solution. Hybrid transformers are LFTs that have active filters and/or integrated series voltage compensators. There are several hybrid transformer configurations available, including shunt or series connections between the power electronics converter and the LV winding of the LFT. Fig. 1.10 shows the four standard configurations reported in the existing literature. Flexibility is provided by these configurations, some of which even permit active power exchange with the grid. For many uses, such as power factor correction or harmonic filtering, this makes it possible to inject arbitrary voltages. In contrast to SSTs, where the power electronic stage processes a significant portion of the power, hybrid transformers have the power electronics stage handling only a small fraction, minimizing overall losses. Furthermore, they keep compatibility with the current LV

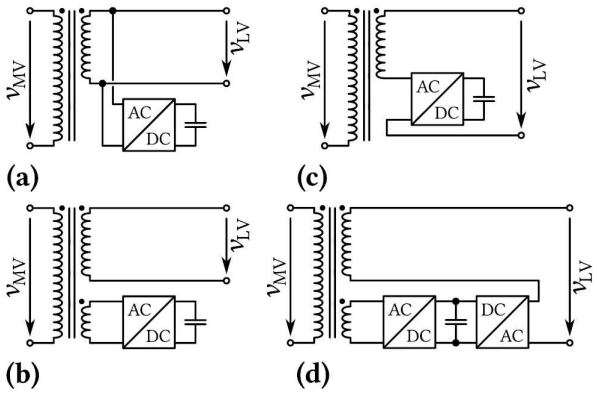


Figure 1.10: (a)-(d) Main series/shunt configurations of hybrid transformers [5, 36].

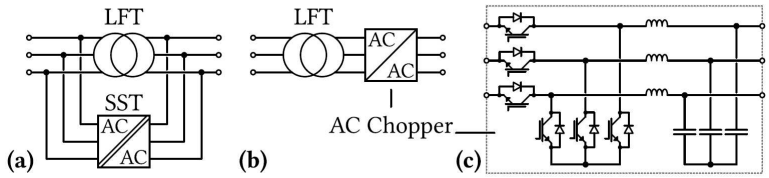


Figure 1.11: (a) Parallel configuration of an LFT and an SST [37]; (b) series configuration of an LFT and an AC chopper and (c) realization option of an AC chopper [38].

grid protection strategies. Product development for high-efficiency reactive power support and voltage control has already been accelerated by hybrid transformers.

An alternative method involves directly connecting an SST in parallel to an already-existing LFT. Fig. 1.11 shows these configurations. This approach improves controllability and power transfer capacity without adding more short-circuit power to the system. Alternately, voltage control and current limitation could be provided as needed by an AC chopper and LFT configured in series.

1.4.2 The MultiPort (MP) evolution of the SSTs

Early versions of SSTs proposed in the literature have been developed based on a two-port architecture [16, 18]. However, in order to connect multiple loads and sources to these types of SST configurations, a large number of additional converters are required to properly interface with the available AC and/or DC buses provided by the SST, drastically affecting the overall system efficiency and reliability. On the contrary, the concept of MP-SST fits optimally in the IoE framework [21]. It represents an advancement in

the SST technology and enables the integration of RES, DGs and ESSs through suitably isolated ports within one single adjustable, modular and compact configuration, thus minimizing the number of components involved in the power conversion and increasing both the power density and reliability of the whole system [18, 23, 39]. As an extended version of the common two-ports SST, the MP-SST shares the same basic core structure. According to the definition of SST, all of them share the same concept of isolated AC-AC high-frequency conversion. In recent years, MP-SSTs have been introduced in different industrial applications, including railway electric traction, EV chargers and vehicle-to-grid technology, distributed generation, and DC power distribution, among others. Much research and many innovative works have been presented in the literature concerning these topologies. As an extension of the standard two-port SST, the MP-SST also provides isolation between its input and output sides, namely the MV side and the LV side. However, isolation may not be guaranteed between all LV side ports, depending on the chosen MP-SST topology. In the literature, most of the proposed MP-SSTs belong to either the three- or four-port topologies. SSTs with more than four ports are intrinsically quite complex systems that have only been introduced recently; thus, laboratory prototypes are still hard to find. Based on the level of isolation between their ports, MP-SSTs can be broadly grouped into two main categories, namely partially or fully isolated. In partially isolated topologies, the number of connected sources is larger than the number of available transformer windings. As a consequence, multiple sources are connected to a single transformer winding on the LV side sharing a common ground and, therefore, the related ports are not galvanically isolated one from each other but only from the MV side [39]. Partially isolated solutions can provide higher efficiency with fewer components, although providing a connection to the same transformer winding to sources and loads with different voltage levels is not obvious in practice [39]. In this case, the integration of multiple sources with the LV bus is frequently achieved through additional non-isolated DC-DC converters. When the voltage ratings of these DC-DC converters are not consistent with the LV bus voltage or galvanic isolation is required, this solution is not feasible [22, 40]. In fully isolated MP-SSTs, each source is connected to the system through a dedicated winding of the HFT. Each converter port is then galvanically isolated from the others both on the LV and LV sides and the appropriate voltage level required by each port can

be obtained by properly adjusting the transformer turn ratio. In this section, most of the MP-SST topologies discussed in the literature so far have been analyzed and, then, classified according to their isolation capabilities and the configuration of their various conversion stages. For the clarity of reading, this section is structured as follows. First, partially isolated MP-SSTs are discussed, followed by fully isolated architectures. As stated in the introduction, non-isolated topologies can also be found in the literature and will be discussed together with other special configurations.

Partially Isolated MP-SSTs topologies

One of the most common partially isolated MP-SST configurations reported in the literature is a three-port SST that integrates the additional ports on the LVDC links. The concept of the three-port SST arises in the framework of multiple DC sources connected to the grid, such as in the case of PV and energy storage integration. This topology enables an LVDC link for the integration of such sources. The LVDC link can be derived either by the LV port of the DC-DC stage of the SST or by a dedicated winding of the HFT, resulting in a partially isolated or a fully isolated SST, respectively. In the literature, the partially isolated topology, generally based on the DAB converter, is the most commonly used three-port SST configuration. However, its application is unfeasible when the voltage ratings of the non-isolated converters connected to the same LV bus are highly different or when isolation is required between each LV port [22, 41, 42]. The popular FREEDM Gen-1 silicon-based SST is an example of this type of configuration [12, 24, 42]. The FREEDM Gen-1 SST, a project supported by the ERC Program of the National Science Foundation, consists of a 20 kVA single-phase three-port SST prototype designed to operate with a 7.2 kV primary voltage providing a 120/240 V AC port for utility applications and a 400 V DC port for RES and DG integration. The converter topology is reported in Fig. 1.12. The MP-SST configuration adopted for the FREEDM converter is commonly referred to as ISOP. It relies on a CHB converter as the input rectifier stage and on a DAB converter as the isolated DC-DC stage. The output LV ports are derived from the LVDC bus; thus, they are isolated from the MV input side but not from each other. A three-phase version of this configuration was presented in [43] alongside with some considerations of the control system and experimental results. The

CHB converter represents a good candidate for the multi-level AC-DC stage of the SST, due to its modularity and simplicity. It can provide LVDC, LVAC, and MVAC ports, but no MVDC port can be derived due to the lack of a common DC bus. For this reason, CHB-based MP-SSTs are not suitable for hybrid AC/DC distribution systems [44, 45]. On the contrary, MMC-based MP-SSTs inherently enable a four-port converter structure providing both MVAC and MVDC ports for the hybrid distribution system integration, in addition to the LVAC and LVDC ports typically required in utility applications. Despite its flexibility, the MMC-based MP-SST is usually a partially isolated topology due to the natural configuration of the MMC converter, which provides a direct non-isolated connection between the MVAC port and the MVDC bus. Fig. 1.13 shows a partially isolated four-port MMC-based SST able to provide low- and medium-voltage connections in both DC and AC. As can be observed in the figure, the MV ports are isolated from the LV ones, but not each other. In [46], some simple three-port MMC-based SST topologies providing an isolated LVDC port are discussed. In [45], an in-depth comparison between CHB- and MMC-based MP-SST configurations is carried out highlighting the benefits and drawbacks of both topologies. It has been shown that the advantage of the MVDC port enabled by the MMC converter is achieved at the price of a larger number of components and higher device ratings. In fact, to support the same voltage level of a CHB-based MP-SST, the MMC-based solution requires four times the number of cells in comparison

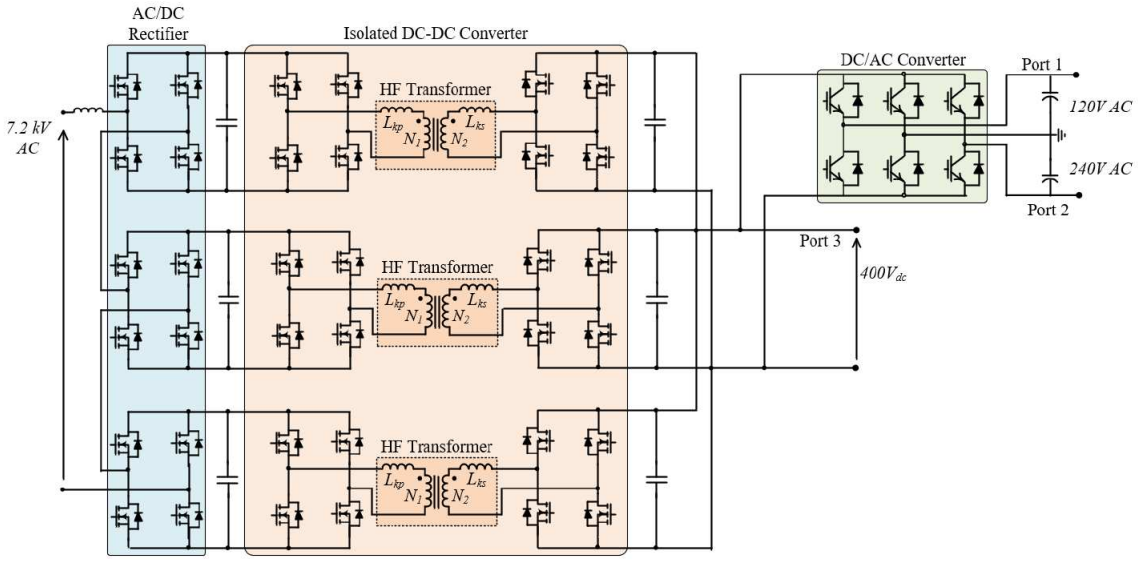


Figure 1.12: FREEDM Gen-1 SST topology [15].

to the CHB-based one. If the common MMC configuration is used, i.e., half-bridge cells, then the number of devices required by the MMC is two times the CHB. Furthermore, the MMC flexibility that allows the coupling of multiple ports leads to a considerably different amount of power that the cells and the power devices must handle compared to the CHB-based solution. This results in a higher rating of the converter devices. The authors of [44] have discussed three basic MMC-based MP-SST configurations providing four-port connection capability. Such topologies are partially isolated, as MV ports and LV ports are not isolated each other, but galvanic isolation is provided only between MV and LV sides. The isolated DC-DC stage is provided by a DAB converter. The MMC-based MP-SST configurations differ from each other only in the interconnection of the basic building blocks. In particular, the topologies investigated in [44] include an ISOS and an ISOP cell-to-cell connected MMCs. In a further configuration, the building blocks still employ an ISOP connection, but one of the MMCs is replaced with a different topology (e.g., a two-level or a neutral-point-clamped inverter). The authors of [47, 48] have illustrated the MV prototype of an MMC-based four-port SSTs. Acting as an ER, the proposed 10-kVAC 750-VDC converter takes advantage of MMC flexibility to interface

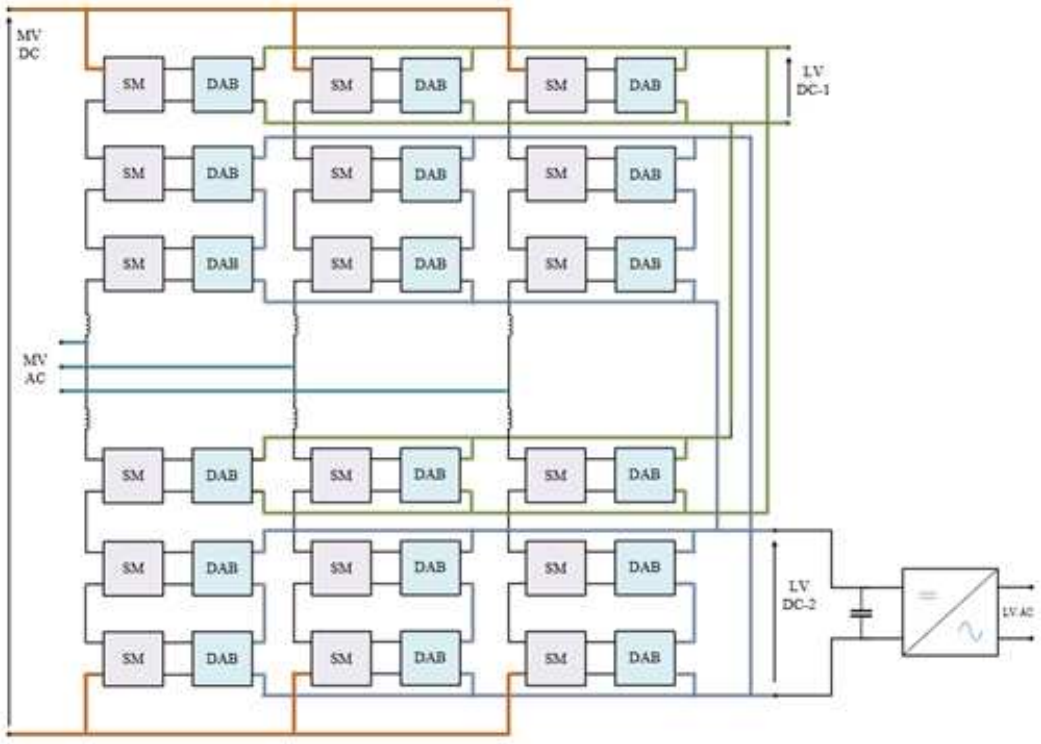


Figure 1.13: Four-port MMC-based MP-SST [15].

MV and LV grids. The discussed topology achieves galvanic isolation through HFTs and the DC-DC modules are ISOP-connected. In [49], an MMC-based MP-SST using an LC resonant circuit and HFT in replacement of the DAB converter has been proposed. A resonant tank is connected in parallel with each arm of the MMC, across which a medium frequency voltage is generated through a mixed-frequency modulation technique. The resonant tanks, together with the HFT, impose the isolation barrier among the MV and LV ports. The proposed configuration achieves the power flow between MV and LV side with only three conversion stages (instead of four as in standard DAB-based solutions), thus reducing the converter size and improving the system efficiency. As an optimization of such a topology, in [49], the number of HFTs is reduced to only two by employing a shared configuration of the resonant tanks. Furthermore, the degrees of freedom and flexibility of the MMC allow for a further reduction of the number of conversion stages between the MV and LV ports as reported in [50, 51], where only two power conversion stages are employed. The main drawbacks of these topologies are the absence of a MVDC port for hybrid AC/DC distribution systems and the requirement of H-bridge-based MMC cells to generate the high-frequency voltage waveform for the transformer windings. Finally, in [52] the authors have proposed an MMC-based MP-SST in which the galvanic isolation between MV and LV ports is achieved through a Quadruple Active Bridge (QAB) converter, a four-port isolated DC-DC converter featuring a multi-winding HFT. Further details about the QAB converter will be given in the next section, where a case study is discussed directly involving this topology. The QAB converter couples together three submodules of the MMC (one per phase) with the LVDC link. Such a solution, along with its dedicated control strategy, is able to achieve a better distribution of the power flow among the three phases of the MP-SST.

Fully Isolated MP-SSTs topologies

As in the case of partially isolated architectures, also for fully isolated MP-SSTs, the most common configurations are the three- and four-port SSTs. Fully isolated versions of the three-port SST can be found in the literature based on essentially two different approaches, either by means of a three-port isolated DC-DC converter based on the Triple Active Bridge (TAB) topology, which is an extended version of the DAB converter with

a three-winding transformer, or by employing other isolated DC-DC topologies together with a series or parallel connection of the MP-SST building blocks that ensures the mutual isolation of any of the ports. In the first case, the MP-SST relies on the TAB converter as the core isolating stage [53]. A proper control system should be provided when multi-winding DC-DC converters are employed. First, since the power delivered by one bridge depends on the phase-shifts of the other two bridges, the power flow of the converter should be decoupled in order to obtain a power equation for each port independently from the others. Furthermore, as explained in [14], when the converter ports operate at voltage levels that are highly different, large circulating currents will flow in the TAB converter, leading to important conduction losses and, in some cases, even to the loss of the soft-switching features. Thus, a control system based on both phase-shift and duty-cycle variations should be adopted for this converter to optimize dynamics and efficiency. In case the isolation is achieved through a dedicated converter building blocks interconnection, one suitable MP-SST configuration that ensures isolation between all ports consists of an ISOS connection of the circuit building blocks and the DAB converter as the core isolation component. As an example of this configuration, one of the major converter designs known in literature is the UNIFLEX SST project, supported and promoted by the European Community under the 6th Framework Programme [13]. The UNIFLEX topology is depicted in Fig. 1.14. It consists of a three-port 300-kVA SST designed for the future electricity network with the purpose to interface two 3.3-kV AC grids with a 415-V AC grid. This configuration provides a fully modular and scalable converter. The control system of the DC-DC stage is less sophisticated compared to the TAB-based topology as it consists of the DAB converter and, thus, the power cross-coupling consideration is avoided. However, in this system, the power flow among the output ports, referred to in [54] as Port 2 and Port 3, is not direct, since those two ports can only exchange power between them through coupling with Port 1. Two different configurations of an isolated SST topology based on the CHB and DAB converters are proposed to achieve a lower number of conversion stages between the ports. The proposed solutions provide better efficiency and the downsizing of the LV feeders, compared to the commonly adopted topology reported in [14]. Regardless of the partially or fully isolation class, it is important to report that the QAB converter has also been tested as a possible feasible basic cell for a three-port SST.

This is because a generic n-winding isolated DC-DC converter can be connected to less than n different ports. In this case, any port is coupled with the others through more than one winding, since the QAB converter provides a flexible connection and can be connected either in a symmetrical or in an asymmetrical way, providing different solutions to the voltage and power level for the isolating stage of the converter. Beside three-port SSTs, the majority of MP-SSTs are basically four-port SST converters. This topology has been introduced mainly through the development of the aforementioned QAB converter, an isolated DC-DC converter developed as an extension of the DAB converter and belonging to the Multi Active Bridge (MAB) topologies [40], in which multi-winding HFT are used. As depicted in Fig. 1.15, it is made of four active bridges; thus, it provides a connection to four isolated sources. The major benefit brought by the QAB converter in a multi-port architecture is the reduced number of transformer cores and modules, and thus, less encumbrance compared to a DAB-based MP-SST, while still preserving the same advantages. Furthermore, it provides modularity, scalability, high power density, and also additional degrees of freedom in the converter connection ports [40]. Thus, the standard fully isolated four-port SST topology, which can be found in the literature, relies on the QAB converter. The very first QAB-based four-port SST was developed in [40], for ESS and DG integration. The paper highlights the benefits of a QAB-based MP-

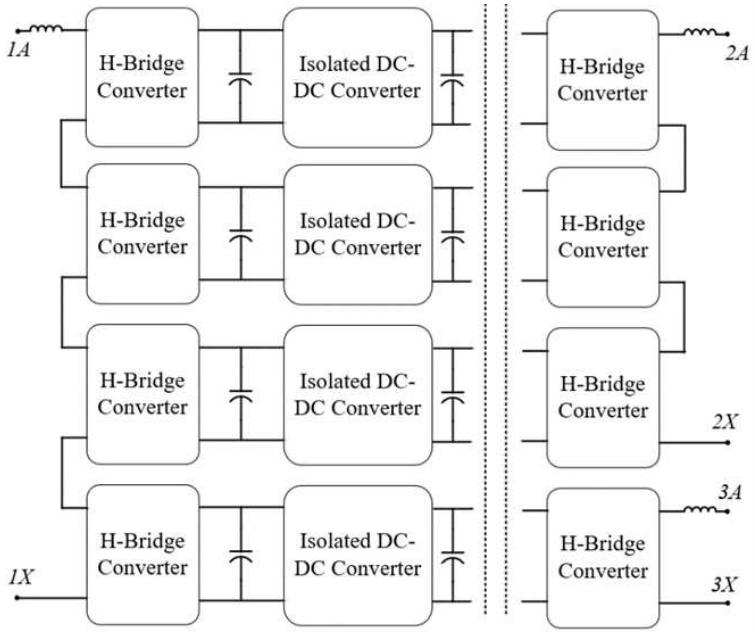


Figure 1.14: Single-phase representation of the UNIFLEX-PM SST topology [15].

SST structure, providing an average model used to properly design the converter control system. In fact, as also reported in [55] and mentioned above for the TAB converter, the power delivered by one port depends on the phase angle of the other three ports. This cross-coupling characteristic needs to be taken into account when designing the control system of the QAB converter. A linearization around a nominal operating point is needed to decouple the power equation for each port. Through this procedure, it is possible to obtain a better dynamic performance of the converter. The experimental results reported in both [40,55] provide a validation of the theory. The authors of [23] pointed out that in a QAB system there are some operating modes characterized by high phase-shift values that produce large reactive currents. It was mentioned that even under light-load conditions the phase-shift control of the converter produces high circulating currents. Thus, the authors propose a new control strategy, designed as a combination of phase-shift and duty-cycle control to ensure both the power balance among the ports and the desired output voltage. In general, considering an IoE scenario with intermittent DERs, DG, and storage, [56] suggests a Multi-Input-Multi-Output (MIMO) control scheme to meet all the operating modes discussed in the article. It is worth pointing out that the major issues with QAB-based SSTs are the complexity of the control system and the manufacturing of the multi-winding transformer. In particular, the latter has been discussed in several

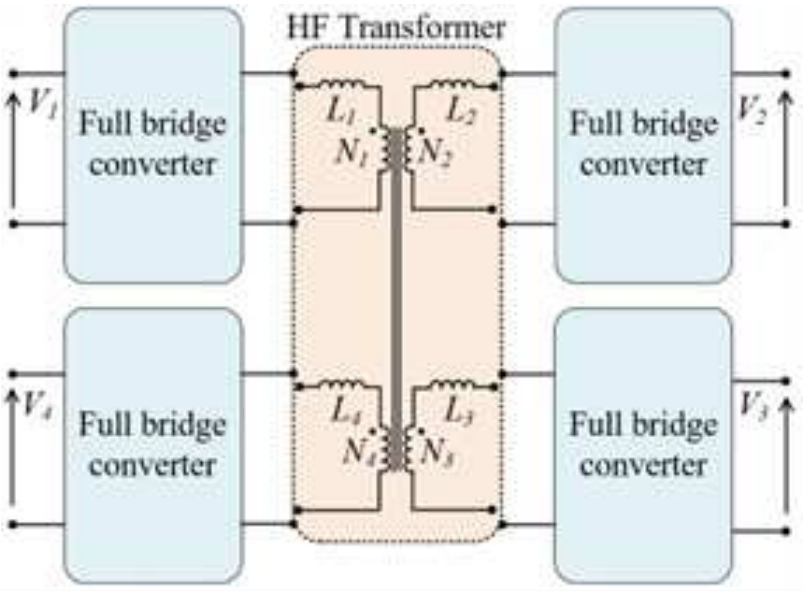


Figure 1.15: Quadruple-Active-Bridge converter topology [15].

papers. In [57]], the operating principle of a SiC-based QAB converter for fast charging station application has been discussed, together with the design procedure of the HFT and the selection criteria of the power devices. The authors of [58]] discussed the HFT design for a QAB-based SST for microgrids, considering one port of the converter as having a MV rating. Through Finite Element Analysis, the HFT have shown 99.7 efficiency; some preliminary laboratory results are also given. To avoid the use of a multi-winding HFT, the authors of [47] proposed a megawatt-level high-frequency bus-based four-port SST, which relies on the so-called Modular-MAB (M-MAB). The proposed topology presents mutual isolation, mutual independence among different ports and a modular structure. Despite its benefits, the topology has as a drawback that the control strategy is complex due to the high-frequency bus, which may easily propagate a disturbance occurring at one of the ports to the others. MMC-based, fully isolated SST architectures have also been proposed in the literature. As discussed in the previous subsection, the MMC structure is inherently a partially isolated topology; however, in some cases, the MVDC port is used as a grid or load interface and the MVAC one is not directly accessible since it is employed as a coupling interface with other converters. This is for example the case of isolated multi-port DC-DC converters acting as DC hub. Nowadays, the High Voltage Direct Current (HVDC) technology is becoming more popular. As for traditional AC lines, even for DC distribution systems, there is a need for an intelligent and flexible multi-port DC-DC converter that interconnects and manages DC sources and loads acting as a DC energy router. The MMC converter fits optimally as a DC-AC interface that provides an AC-link, through which an HFT is connected to achieve isolation between all the DC ports, as pointed out in [59]]. In this paper, the authors have presented a review of different topologies suitable for DC hub converter applications. The MMC-based one has been identified as the most promising and a three-port MMC-based DC hub is considered as a case study. In [60]], two parallel-connected MMC have been proposed to build a three-port DC hub; this solution, known as bifurcate MMC, avoids the use of a multi-winding transformer. The authors of [61]] investigated the MMC-based MP DC-DC converter as a truly modular HV DC-DC converter, built with multiple submodules that can be controlled individually through decentralized controllers, thus allowing the easy reconfiguration of the power converter circuit for different DC applications. Finally,

in [62]] a fully isolated four-MV-port SST based on MMC and MAB converters was proposed for the HVAC distribution architecture. Such a solution acts as an ER in a HVAC distribution system scenario and provides isolation between all the AC ports. It is worth noticing that a MVDC port could be derived from each AC interface; however, in this case, the topology becomes a partially isolated one, since there is no isolation between the DC and the respective AC ports.

Other topologies

As discussed previously, the most common MP-SST configurations are three- or four-port based, while generic n-port topologies, with n greater than four, are uncommon due to complexity in design and control. A n-port SST based on the MAB architecture comprises n full bridges coupled together through a n-winding HFT. It enables the isolated interconnection of multiple sources and loads at different voltage levels through the adjustment of the HFT turn ratios, achieving a high-power density conversion in a single system [40]. The limitation on the number of ports of a MP-SST is usually dictated, as for the QAB converter, by the complexity of the control system and by the HFT magnetic core design [40, 47]. Beside the ideal design based on a n-winding HFT, the n-port SST can be built through the proper interconnection of the isolated DC-DC converter outputs, regardless of the partially or fully isolation approach, as stated for the other MP-SST topologies. To the authors' best knowledge, in the literature, only [21] presented n-port SST, which is a nine-port ER in a LV smart grid scenario. In the article, the authors highlighted two converter variants and provided the circuit parameter design and the adopted control strategy, which is based on an energy management system. Experimental results on the two Multiple Energy Router prototypes validated the analysis. Beyond that, in [63]], further direct AC-AC MMC-based topologies that fit quite well as ERs are discussed. In particular, the Hexagonal MMC and the Ring-Star MMC provide connection to a multiple number of ports and phases realizing a modular active node converter. However, these topologies are direct AC-AC converters, and therefore, they do not provide any kind of galvanic isolation between ports; thus, the basic concept beyond the SST decays. Still, those topologies are quite interesting and deserves further investigation as ER concept.

1.5 Aims and Contributions of the Thesis

Considering what discussed in the previous sections, the aim of this thesis is to contribute to the detailed modeling, control and stability analysis of SST technology for smart distribution grid applications. Moreover, the starting point of the work was the UNIFLEX-PM converter topology. Thus, based on the current SSTs state of the art, the main contributions of this thesis aim to fill the research gaps related to the control aspects and the stability issues of such complex topology. Specifically, the key contribution of this thesis are summarized as follows:

- **SST topologies:** the thesis first presents a comprehensive literature review of the current SST topologies presented in the literature and the existing prototypes. Current trends and future developments, such as hybrid transformers or MP-SSTs, are highlighted.

- **Three-phase triple-stage SST:** after a brief introduction on the SST topology object of this work, a mathematical *averaged* model of the converter is derivated both for speeding up the simulations and, especially, for design the control system of the whole converter.

- **SST control architectures:** considering the smart distribution grid scenario of [13], the control functionalities and capabilities required are underlined. Then, common control architectures and features of SST systems are discussed. In this context, to ensure the proper operation of the SST, a cluster and local voltage balancing algorithms are developed in this work.

- **SST stability analysis:** the main research gap covered by this thesis is the stability analysis of three-phase triple-stage SST topology considered here. An overview of stability techniques and tools is presented. Then, based on the impedance model methodology, both DC-link and the grid connection stability issues of the SST are evaluated and discussed. The outcome of this analysis reveals that the the direction of the power flow and the low voltage operating modes can compromise the system stability. Furthermore, it is shown that the effect of the dc-dc converter on the grid

connection stability enhance the low-frequency SST stability margin. Based on that analysis, a stability-oriented design of the control system can be performed.

- **SST prototype:** lastly, the aim of this work was to build a down-scaled laboratory prototype of the converter. The SST demonstrator ratings are defined and the passive components selection is presented in this work. Out of that, the base PEBB board is designed and the PCB layout is developed by means of the software Altium Designer, along with the gate driver boards. Finally, the experimental results show the proper operation of PEBB. The connection of several modules allows to build the final prototype.

1.6 Outline of the Thesis

According to the goals and contributions mentioned, this thesis is structured as follow:

- In Chapter 2, the UNIFLEX-PM converter, which constitutes the starting point of this thesis, is reviewed with respect to the current available topologies. The MV AC-DC stage is discussed and a comparison between two well-known topologies, i.e. the MMC and CHB converters, is presented. Design rules are also highlighted. As for the AC-DC stage, also the DC-DC isolation stage, i.e. the DAB converter originally implemented on the UNIFLEX-PM, is introduced and its choice is motivated. These results allow to confirm the UNIFLEX-PM topology as suitable SST architecture for the future IoE scenario;

- Chapter 3 presents the modeling of the whole SST system. The CHB average and small-signal models are presented, both for the natural reference frame and for the synchronous reference frame. As for the CHB, the DAB small-signal model is also provided. Thereafter, the SST control architecture is presented. Special focus is posed on the CHB DC-link balancing control system, which for a three-phase topology consists of a three-layer regulation system. Finally, simulation results verify the validity of the proposed SST model;

- In Chapter 4, the stability assessment of the SST is finally presented, from both DC-bus and grid-connection point of view. In the first case, through the dq small-signal

SST model, the DC-bus impedance model of the SST is derived. Then, DC-link stability is assessed via Middlebrook's stability criterion. In the second case, the SST *dq* impedance seen at its AC terminals is derived. The, the input impedance matrix properties are discussed in terms of their passivity. Furthermore, a simplified expression for the *d*-axis impedance is derived.

- In Chapter 5, the design of the modular SST structure under investigation is presented. In particular, the topology which consists of two H-Bridges interfaced via a DC-link is chosen as basic building block. The component selection is discussed and both power and gate driver PCB boards are designed. Ultimately, open-loop test verified the proper operation of the B2B-PM under both no-load and light-load conditions.

- Finally, this thesis concludes with Chapter 6, where the main contributions and findings of the thesis are summarized.

1.7 List of Publications

The work developed in this thesis, and also additional research projects, resulted in the following publications:

Journal Papers

[J1] Granata, S., Di Benedetto, M., Terlizzi, C., Leuzzi, R., Bifaretti, S., Zanchetta, P. (2022). "Power Electronics Converters for the Internet of Energy: A Review". *Energies*, 15(7), 2604;

Conference Papers

[C1] Granata, S., Leuzzi, R., Tresca, G., Bassi, E., Benzi, F. and Zanchetta, P., 2022, October. "Stability Assessment Study for a Triple-Stage Three-Phase Solid-State Transformer". In *2022 IEEE Energy Conversion Congress and Exposition (ECCE)* (pp. 1-8). IEEE;

[C2] Granata, S., Tresca, G., Benzi, F. and Zanchetta, P., 2023, October. "Impact of the DC-DC Stage on Grid-Connection Stability in Solid-State Transformer". In *2023 IEEE Energy Conversion Congress and Exposition (ECCE)* (pp. 2668-2675). IEEE;

[C3] Volpini, A., Granata, S., Postiglione, G. and Zanchetta, P., 2023, October. "Negative Voltage Sequence Control for an Electric Arc Furnace Power Supply based on a Multilevel AC-AC Converter". In *2023 IEEE Energy Conversion Congress and Exposition (ECCE)* (pp. 2817-2824). IEEE;

[C4] Tresca, G., Granata, S., Postiglione, G., Finotti, C. and Zanchetta, P., 2023, May. "Balancing voltage algorithm for a medium voltage Cascaded H-Bridge STATCOM in zero-current mode". In *2023 11th International Conference on Power Electronics and ECCE Asia* (ICPE 2023-ECCE Asia) (pp. 3340-3345). IEEE;

[C5] Tresca, G., Formentini, A., Granata, S., Leuzzi, R. and Zanchetta, P., 2022, October. "Direct AC charging of EV Reconfigurable Cascaded Multilevel Converter". In *2022 IEEE Energy Conversion Congress and Exposition (ECCE)* (pp. 1-8). IEEE;

[C6] Tresca, G., Formentini, A., Granata, S., Magrini, C. and Zanchetta, P., 2023, October. "Kalman filter estimation method for battery cell parameters in Reconfigurable Cascaded Multilevel Converter". In *2023 IEEE Energy Conversion Congress and Exposition (ECCE)* (pp. 3648-3653). IEEE.

Submitted Papers

[S1] Granata, S., Finotti, C., Postiglione G. and Zanchetta. "132-MVAr 35-kV STATCOM Equipped With a Novel Power Oscillation Damping Control Strategy". In *IEEE Journal of Emerging and Selected Topics in Power Electronics* (under review process).

Chapter 2

Topology Selection and System Design: The UNIFLEX-PM Case Study

In the electric distribution system, the SST plays a crucial role in connecting different grids, whether they are MV or LV, providing galvanic isolation through a HFT. The variety of voltage and power levels involved in the SST architecture design presents significant challenges. Additionally, the selection of the optimal power converter topology and system specifications adds complexity to achieving an optimal design. Typically, the design process involves customizing the power converter to meet specific grid specifications, which limits its applicability to a particular country. For instance, an SST designed for use in Europe may not be suitable for installation in the USA due to differing requirements. This variation in applications necessitates different designs, further complicating the task. To address the need for multiple designs required by different SST applications, a modular approach can be adopted to allow for power and voltage scalability. Modules are designed once and then combined according to grid specifications to create the complete SST structure, providing flexibility and scalability. Some key design parameters for SSTs, from both system and converter levels depending on the specific application, can be the number of submodules, semiconductors selection, redundancy capability, modularity level, etc as shown in Fig. 2.1. Some of these are interconnected, such as the number of modules and semiconductor voltage rating. Therefore, a careful trade-off between these parameters must be considered during the SST design process. The proper selection of these parameters determines the functionality, efficiency, cost, reliability, and flexibility

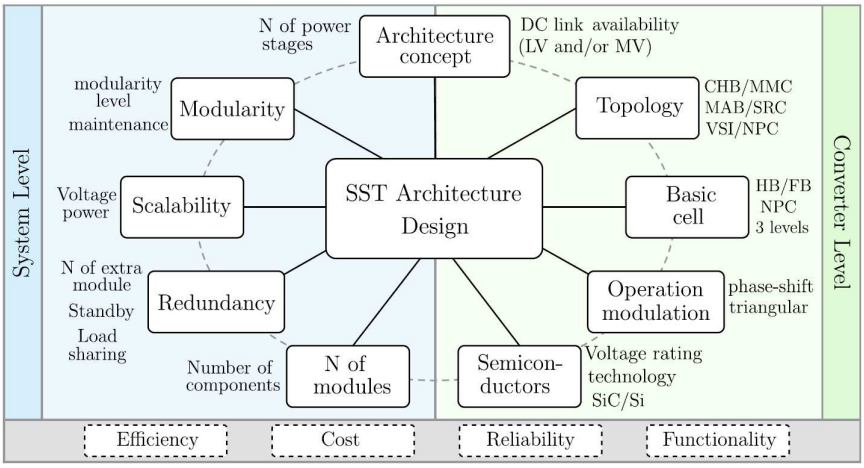


Figure 2.1: Overview of the main SST design parameters and requirements, from both converter and system level [4].

of the SST.

Moreover, in the early stages of its design process, the SST conceptualization is crucial since it shapes and constrains later stages of the process. The availability of the DC link for both MV and LV interfaces is an important aspect that defines the SST architecture in terms of number of conversion stages (single-, double- or triple-stage). In this regard, the modular triple-stage architecture provides enough adaptability to support one, two, or no connections to DC links based on the power converters topologies and PEBB connection (ISOP, IPOP or ISOS configuration) [4,15]. The inherent flexibility of the triple-stage SST topology is the reason why this architecture is the most widespread among the possible solutions highlighted in Section 1.3. In this context, the availability of the LV DC-link (i.e. LVDC link) is the most adopted solution when the SST serves as an interface between the distribution network and a local grid, enabling a microgrid scenario [4]. More recently, the rise in MV DC loads such as EV fast charging stations drove to a growing interest in the MV DC link (i.e. MVDC link) availability [4].

As mentioned earlier, the work developed in this thesis is a prosecution of the previous analysis carried out under the 6$^{\text{th}}$ Framework Programme supported by the European Community, which led to the conception, construction and test of the UNIFLEX-PM converter [13]. Therefore, the starting-point topology considered in this work is a triple-stage three-phase SST, as it is the UNIFLEX-PM. To work as an active node of the grid, i.e. an intelligent ER, the UNIFLEX-PM converter was meant to interface two MV

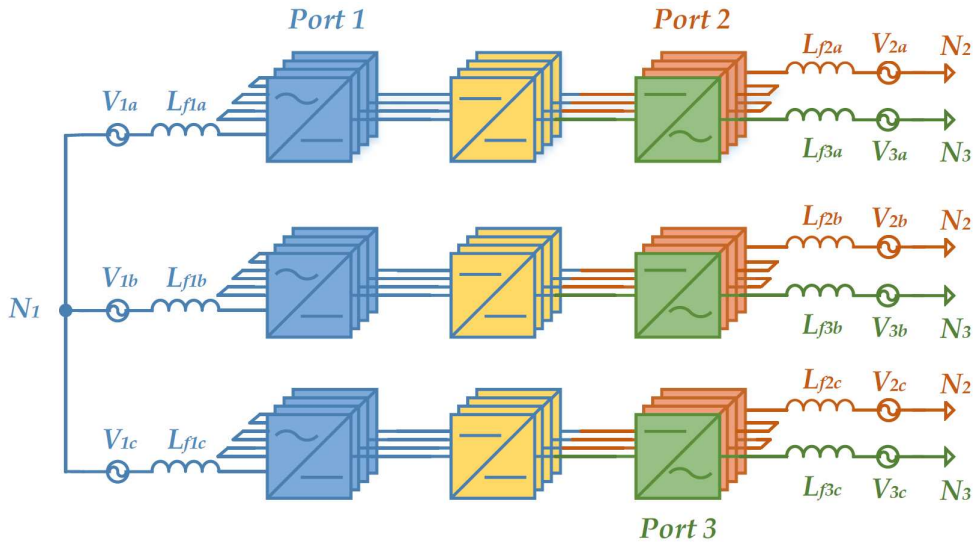
distribution grids and a LV utility grid, eventually providing the availability of LVDC links for future integration of DC loads. These assumptions led to the choice of an ISOS connection of the UNIFLEX-PM PEBBs, resulting in a multilevel structure at the external interfaces of the converter, providing MVAC connection capability. At the inner core of the converter, each isolated single-phase DC-DC converter was responsible for linking the upstream and downstream DC links, creating galvanic isolation between them. Depending on these considerations and requirements, the UNIFLEX-PM configuration was a triple-stage three-phase SST configuration based on the CHB and DAB topologies [13, 15].

This chapter introduces the SST topology under investigation. i.e. the UNIFLEX-PM converter, presenting, motivating and discussing the selection of the power conversion topologies suitable for each conversion stage of the converter. Moreover, the design of the SST ratings and passive components is shown, with the purpose of rounding off the SST topology design prior to present the control system design. Note that, from now on in this thesis, the term SST will be used referring to only *Smart Grid* applications, thus assuming and taking for granted a grid-connected system at distribution (i.e. MV) level.

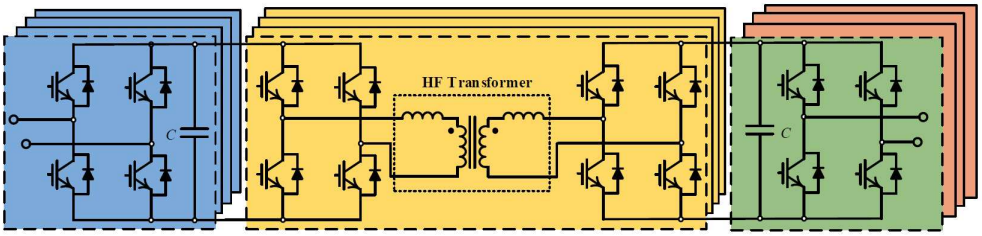
2.1 The UNIFLEX-PM Project

2.1.1 System Description

As introduced in Section 1.2, as one of the first approaches, the three-port UNIFLEX-PM system aims to provide a universal, flexible and modular power electronic interface that can link various sources and loads, such as MV distribution networks, RES, DGs and ESSs, without the need for bulky line frequency transformers [13, 64]. To directly handle the MV connection, the system comprises two AC-DC conversion stages based on the series connection of multiple HBs, realizing the well-known multilevel multicellular CHB topology. Furthermore, to guarantee galvanic isolation between the AC terminals while also reducing the system size, an isolated DC-DC converter based on HFT is implemented, i.e. the DAB converter. Fig. 2.2a shows the three-port UNIFLEX-PM concept, in which Port 1 (in blue) and Port 2 (in orange) are connected to MVAC buses, while Port 3 interfaces a LVAC utility grid. As said before, the floating DC buses provide a possible LVDC connection for future integration of DC loads. The converter is based on a per-phase



(a)



(b)

Figure 2.2: UNIFLEX-PM converter structure: (a) per-phase representation; (b) conceptual schematic of a single AC-DC-AC PEBB [15].

modular cascaded architecture, using four identical modules per phase. The single module, i.e. the basic PEBB whose conceptual schematic is shown in Fig. 2.2b, is composed of an isolated bidirectional AC-DC-AC multi-stage converter. Using the modular PEBB approach, many possible future implementations are possible [4, 30]. As aforementioned, in the case of the UNIFLEX-PM structure considered in Fig. 2.2a, PEBBs are connected in ISOS configuration, realizing a triple-stage three-phase ISOS SST architecture.

With reference to Fig. 2.2, a nine-level CHB converter has been used to interface the MV line on Port 1, while Port 2 interfaces the other MV network through a seven-level CHB converter. A single HB per phase is used for LV connection of Port 3. On the DC side, each HB on Port 1 is connected via DAB converter to another HB on Port 2 or Port 3, realizing an HF isolation barrier among the three ports. Figure 2.3 shows an

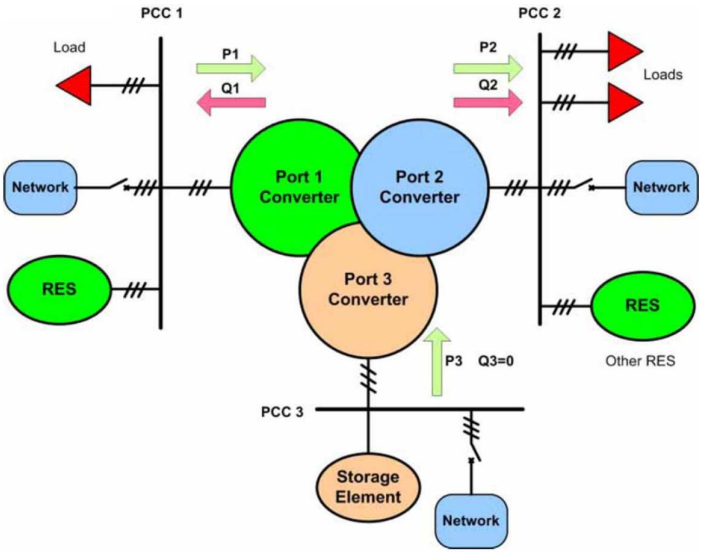


Figure 2.3: Example of UNIFLEX-PM concept connecting three electricity systems together [13].

application example of a three-port UNIFLEX-PM system [13].

2.1.2 Basic Functionalities

Depending on the control system implemented for each port, the UNIFLEX-PM can perform several tasks. With standard control structures (e.g. synchronous reference frame control, etc.), the following basic functionalities can be implemented for such system [64]:

- Voltage ratio adjustment: the voltage at each port can be controlled independently;
- Frequency regulation: each port can operate at different frequencies, allowing the interconnection of asynchronous distribution systems;
- Phase control: the voltage phase angle can be controlled for each port;
- Voltage asymmetry cancellation: one or more converter ports can operate with unbalanced grid conditions while maintaining a balanced operation for the remaining ones;
- Asymmetric load cancellation: even if one or more ports are operating with unbalanced loads (unbalanced currents), the others can still operate in a balanced condition;

- Active and reactive power regulation: the active and reactive powers at each port can be regulate independently and simultaneously, allowing grid features like power balancing and voltage support;
- Power factor correction: being capable of controlling independently both active and reactive power at each port, the power factor can be thus adjusted as required;
- Harmonic cancellation: a complete decoupling of ports in terms of harmonics can be obtained, for both voltages and currents;
- Low Voltage Ride-Through (LVRT) capability: the UNIFLEX-PM system can still operate under low-voltage conditions (e.g. during transients, load disconnections, etc.), providing voltage support capabilities.

2.1.3 Limitations and Unresolved Issues

The UNIFLEX-PM converter is expected to control the power flow between the three ports at any power factor. However, in [65], a detailed analysis has pointed out some constraints on the power flow capability. In particular, managing the power flow at Port 1 would be more challenging compared to Port 2 and 3 as Port 1 is simultaneously

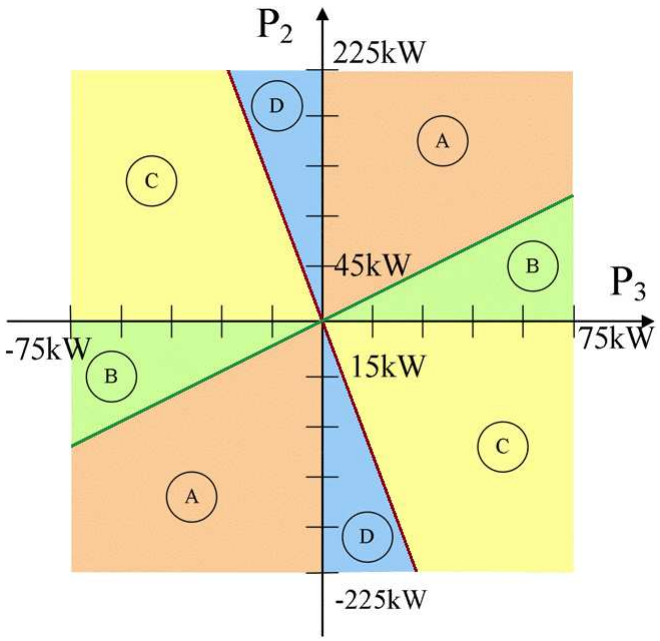


Figure 2.4: Active power operating zones and limitation on Port 2 and 3 [65].

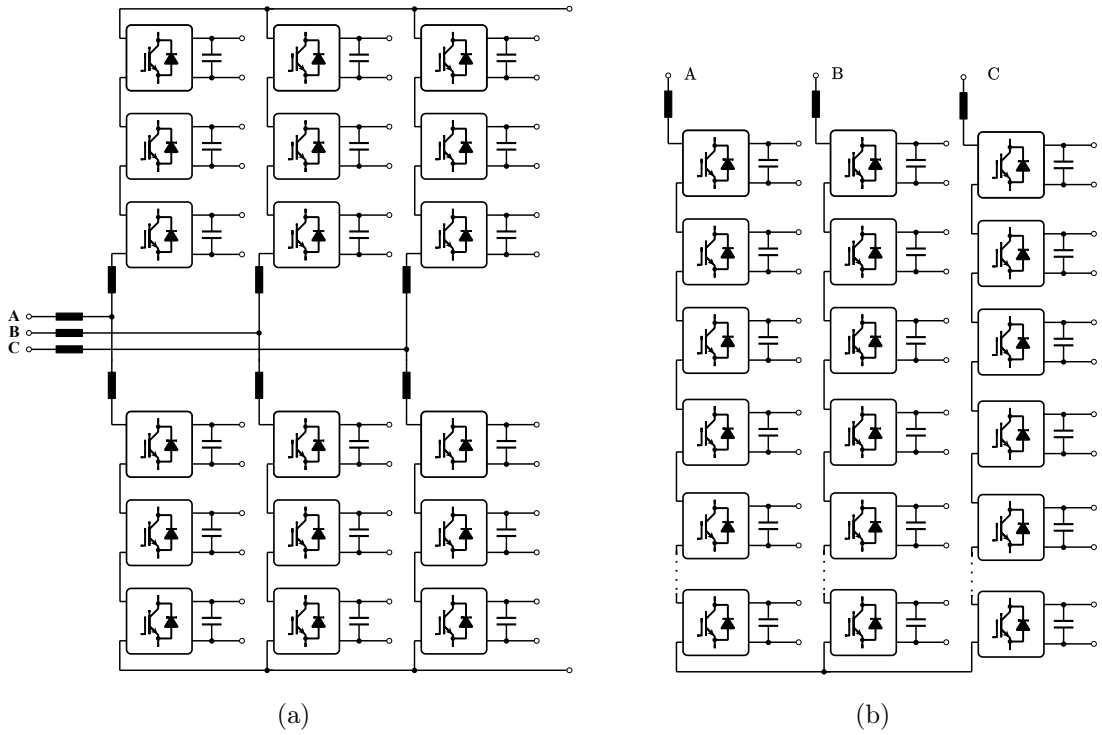
exchanging power with Port 2 and 3. This comes from voltage restrictions at Port 1 [65]. As can be seen in Fig. 2.4, the operating areas are divided into four zones according to the active power on Port 2 and 3. The red and green lines represent the active power limits on Port 2 and Port 3, beyond which a unity power factor operation cannot be reached. In operating areas A and D, no reactive power on Port 1 is required, while in areas B and C, a certain amount of reactive power is needed to ensure the power balance. This means that would be impossible to achieve unity power factor at Port 1 in some operating modes. In addition, from the performance perspective, the UNIFLEX-PM topology is not optimized in terms of efficiency when exchanging power between Port 2 and 3. This is because, with such topology, the power flow between Port 2 and 3 is never direct but it always transits through Port 1. Therefore, as the number of conversion stages involved is greater, exchanging power between Port 2 and 3 is less efficient than doing it between Port 1 and 2 and Port 1 and 3.

Further key aspects that deserve a more in-depth analysis were already mentioned in Chapter 1 and represent the motivation of this thesis, i.e. the development of a synchronous reference frame control for the converter, eventually expandable to the three-port configuration, and especially the modeling and stability analysis of the closed-loop converter dynamics and interactions amongst different conversion stages (e.g. the DAB and CHB converters) and with the grid.

In the next Sections, the topology selection for each conversion stage of the UNIFLEX-based SST will be discussed in detail, along with the system parameters design (i.e. DC bus capacitance, filter inductance, etc.). Finally, based on the topologies review, the selected SST architecture object of this research work is presented.

2.2 AC-DC Rectifier Stage: Power Converter Topologies Suitable for MV Connection

The AC-DC stage interfaces the SST to the MV distribution grid, being responsible for managing the active and reactive power drawn from the network and controlling the voltage at its DC side (i.e. at the input terminals of the DC-DC stage). Therefore, through a dedicated control system, the MV AC-DC stage works as an Active Front-End (AFE)



(a) (b)

Figure 2.5: Modular multicellular power converters topologies suitable for the MV AC-DC stage implementation: (a) Modular Multilevel Converter [72] (MMC) and (b) Cascaded H-Bridge (CHB) Converter [73].

rectifier [4, 15, 16, 30, 31]. Also, through the control, it is capable of providing ancillary services (e.g. reactive power generation) supporting the grid operation. When dealing with the MV level, multilevel topologies are the most logical and advantageous choice for implementing such MV stage as the system is then fully modular, scalable, and reliable [66–71]. When adopting the modular approach at MV levels, the options are limited to two power converter topologies: the Modular Multilevel Converter (MMC) [72] and the Cascaded H-Bridge (CHB) converter [73]. Figures 2.5a and 2.5b present the MMC and CHB topologies. They share advanced features such as reduced filter size due to the low Total Harmonic Distortion (THD) of the voltage waveform produced, reduced switching frequency (and thus reduced switching losses) still maintaining the voltage harmonic content low, reduced submodule blocking voltage allowing the installation of well-established semiconductor devices, modularity, and scalability in both voltage and power. This enables their application in various locations with different grid specifications without major changes in the design of the basic module. These converters belong to the same family of

converters referred to as Modular Multilevel Cascaded Converter (MMCC) [74]. In the case of the MMC of Fig. 2.5a, submodules are usually realized either with Full Bridge (FB) or FB topologies (the first is the most commonly adopted solution). Moreover, the MMC topology represented in Fig. 2.5a is also, and even more appropriately, known as Double-Star Chopper-Cell (DSCC) because the upper arms are connected in star, as well as the lower arms, resulting in two stars connection [74]. On the other hand, the CHB converter of Fig. 2.5b is also known as Single-Star Bridge-Cell (SSBC) due to its unique start connection of the phases [74]. Despite the interesting terminology proposed by Akagi [74], in this work these topologies are referred to as MMC and CHB, respectively, due to the widespread acceptance of this nomenclature. In the next, both converters are briefly described and analyzed, motivating the selection of one or the other (the CHB in the case of the UNIFLEX-based SST) for SST applications.

2.2.1 Modular Multilevel Converter (MMC)

The MMC converter, firstly proposed by Lesnicar and Marquardt in 2003 [72], was designed to address HV applications. Despite the limited number of operative MMC converters in use in industry, it has already become a well-established solution for innovative and promising HV DC (i.e. HVDC) transmission systems [75]. The topology consists of a series connection of cells to form a converter arm, with two arms connected to the AC grid through two inductors (the so-called arm inductors) as shown in Fig. 2.5a [72,76]. As previously mentioned, although there are various possible topologies for the basic module, the Half-Bridge topology is the most commonly used due to its minimal component count and reduced conduction losses on the current path compared to other options. An important advantage of the MMC topology is the availability of the MVDC link, which contributes to the MMC suitability for HVDC applications and also for certain applications in SST (e.g. SST-based fast charging stations, as mentioned at the beginning of this Chapter). However, the complex control system and the considerable amount of required capacitance are notable drawbacks. In addition to controlling the three-phase input currents and the total MVDC voltage like a typical AFE converter, the MMC also needs to regulate the individual voltage of its submodules and the circulating current which flows internally in the converter, which rises because of the AC current divided between both arms of one

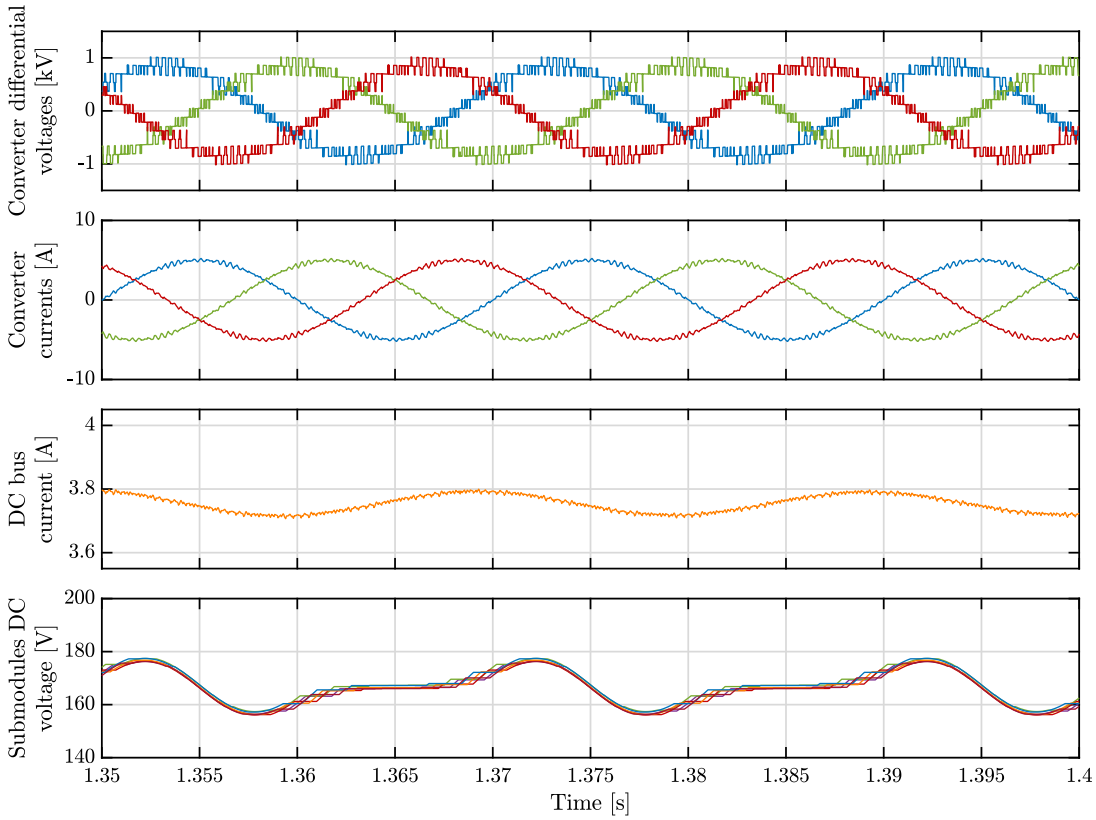


Figure 2.6: Typical Half-Bridge-Cell MMC (i.e. DSCC) waveforms. The submodule DC voltage shows the characteristic ripple at both the fundamental (50 Hz) and double-line frequency (100 Hz) that occurs when half-bridge submodules are used.

phase. This necessitates multiple voltage and current loops, significantly increasing the complexity of the control system design and implementation. Moreover, each submodule of the converter requires a large amount of energy storage but has low energy density, resulting in a substantial capacitance requirement. While the MMC is highly effective in HV applications, its feasibility for MV levels remains uncertain, requiring further research in this area.

For multilevel grid-connected converters, the main design parameters are the number of submodules N (per arm in case of MMC, while in the case of a CHB it refers to the entire branch as will be shown later on), the submodule DC-link voltage V_{dc} and capacitance C_{dc}, the semiconductor blocking voltage V_b, the rated modulation index m_r, etc. For the MMC (i.e. DSCC) converter of Fig. 2.5a, the voltage of the common DC-link V_{dc}^{tot} is calculated by knowing the AC phase voltage that the converter must interface during the

normal operation and the rated modulation index m_r as [76, 77]:

$$V_{dc_{(MMC)}}^{tot} = \frac{\sqrt{2}V_{ac}}{\sqrt{3}m_r} \tag{2.1}$$

where V_{ac} is the line-to-line RMS value of the grid voltage at the Point of Common Coupling (PCC) where the converter is connected. The DC-link voltage of each submodule is chosen considering the semiconductor blocking voltage V_b scaled down of the utilization factor k_u [78]:

$$V_{dc} = k_u V_b \tag{2.2}$$

Usually, is a good practice to operate the semiconductors around 50% of their blocking voltage (i.e. $k_u = 0.5$) so as to be able to withstand possible overvoltage conditions happening during switching transients or faults [78]. Once V_{dc} is defined, the number of submodules (per arm) N can be calculated as:

$$N_{(MMC)} = \frac{V_{dc}^{tot}}{V_{dc}} = \frac{\sqrt{2}V_{ac}}{\sqrt{3}m_r k_u V_b} \tag{2.3}$$

Then, it is possible to calculate the required capacitance of each submodule C_{dc} based on the power fluctuation that affects them. This phenomenon is due to the power exchange from the AC to the DC side or vice versa and it show up as voltage ripple across the DC capacitor at the fundamental (f) and double-line frequency ($2f$) in case of half-bridge submodules (see Fig. 2.6). Therefore, at rated conditions, knowing the converter apparent power S, the grid angular frequency ω and defined a maximum permissible percentaage peak-to-peak DC voltage fluctuation (around the steady-state rated value V_{dc}) $\Delta V_{dc\%}$, the submodule minimum capacitance C_{dc} can be calculated as [77, 79]:

$$C_{dc_{(MMC)}} = \frac{S}{3mN\omega\Delta V_{dc\%}V_{dc}^2}\left(1 - \left(\frac{m\cos\phi}{2}\right)^2\right)^{\frac{3}{2}} \tag{2.4}$$

2.2.2 Cascaded H-Bridge Converter

The CHB converter is probably the most popular and well-established multilevel converter topology used in MV high-power industrial applications. The first traceable patent about this topology was published back in 1975 by R. H. Baker and L. H. Bannister [73], in which the series connection of multiple isolated DC sources was employed to synthesize a staircase AC voltage waveform. As said, this topology consists of several submodules

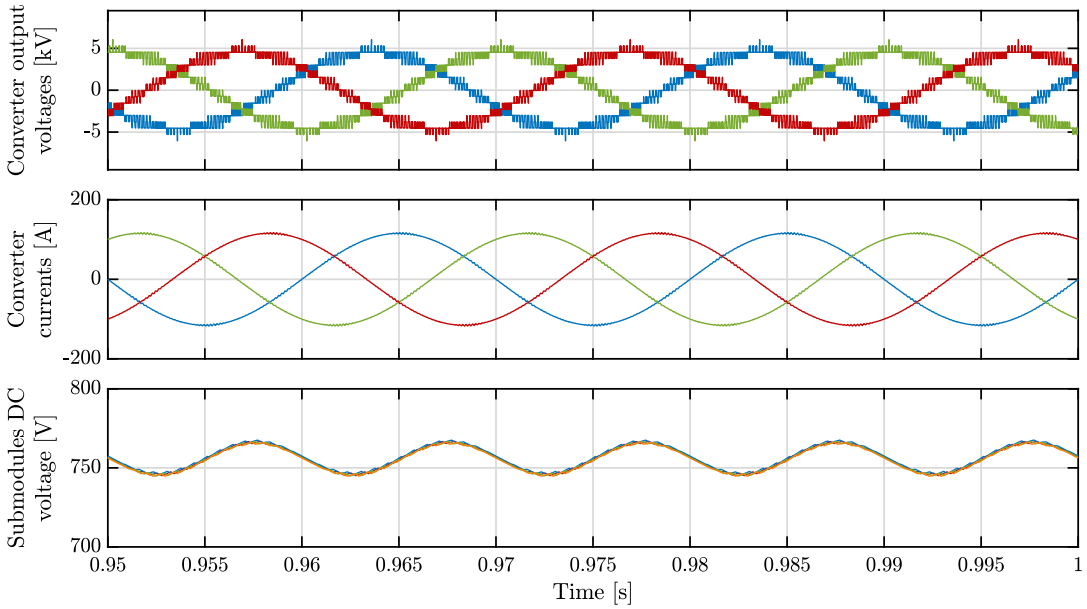


Figure 2.7: Typical CHB (i.e. SSBC) waveforms. Note that, in this case, the submodules DC voltage shows only a ripple at twice the line frequency (i.e. 100 Hz) because of FB cells.

connected in series to create one phase branch, with the three-phase branches connected in a star configuration, as shown in Fig. 2.5b. As for the MMC, in practice, the number of submodules N connected in series is determined either by the AC operating voltage of the converter and manufacturing costs [4, 66]. This topology is well-established and widely utilized especially in MV drives and power quality applications [66–71, 80]. Although other topologies can be used, the H-bridge is the most commonly adopted basic cell [66–71]. At the basis of its popularity among MV converters, there is the simple submodule topology implementation (i.e. FB), modulation, and control. Indeed, even though there are various modulation strategies for the converter, the simple and well-known Phase Shift (PS)-PWM modulation offers several advantages in terms of losses distribution in the semiconductors and reduction in AC filter size [4, 66]. Note that the modulation techniques suitable for multilevel converters will be briefly discussed in the next Section. Furthermore, the operation and control scheme are straightforward when this modulation strategy is employed, unlike the MMC converter which requires an additional control loop to manage the internal circulating current. The main drawbacks of the CHB include the absence of a medium voltage direct current (MVDC) link for connecting MV loads and

sources and the requirement of isolated sources connected to each module. However, in modular SST applications, the need for isolated sources is not a disadvantage, as in most triple-stage architectures the CHB converter is connected to the DC-DC stage, which is composed of several isolated DC-DC converters [4].

The design procedure of this converter is similar to the one made for the MMC. Therefore, the total MVDC link can be defined based on the per-phase AC voltage that the CHB must interface as [4, 81]:

$$V_{dc_{(CHB)}}^{tot} = \frac{\sqrt{2}V_{ac}}{\sqrt{3}m_r} \tag{2.5}$$

Note that, in the case of the CHB, it doesn't make sense to define a total DC-link voltage V_{dc}^{tot} as this converter doesn't feature a MVDC link connection. Thus, this quantity just refers to the sum of submodule capacitor voltages $V_{dc} = k_u V_b$ (see eq. (2.2)) for one phase. Then, the number of required submodules per phase is defined as [4, 81]:

$$N_{(CHB)} = \frac{V_{dc}^{tot}}{V_{dc}} = \frac{\sqrt{2}V_{ac}}{\sqrt{3}m_r k_u V_b} \tag{2.6}$$

From the electrical point of view, the three-phase CHB converter operation can be assimilated to the one of a triple single-phase system. This is due to the lack of a common DC-link. Therefore, the instantaneous power that flows in each converter phase is of a single-phase nature, i.e. a pulsating at twice the line frequency [4, 80, 81]:

$$p(t) = v(t)i(t) = \hat{V}\sin(\omega t)\,\hat{I}\sin(\omega t) = \frac{\hat{V}\hat{I}}{2}(1 - cos(2\omega t) \tag{2.7}$$

Therefore each CHB submodule must process an oscillating instantaneous power, which causes a second harmonic voltage ripple across each cell capacitor (see Fig. 2.5b). This requires a much larger capacitance compared to a three-phase system with a common DC-link (e.g. a common three-phase three-leg inverter). Hence, for the CHB converter, the most common way to design the submodule DC-link capacitance C_{dc} is through the 2nd harmonic capacitor current equation [82]:

$$C_{dc_{(CHB)}} = \frac{m\hat{I}}{2}\frac{1}{2\omega\Delta V_{dc\%}V_{dc}} = \frac{m\hat{I}}{2}\frac{1}{2\omega\hat{V}_{dc,2\omega}} \tag{2.8}$$

where $\hat{V}_{dc,2\omega}$ is the maximum permissible peak value of the 2nd harmonic component of the capacitor voltage, which can be defined (as done previously for the MMC) by knowing

V_{dc} and setting $\Delta V_{dc\%}$. Similar to the MMC design procedure (i.e. equation (2.4)), there is also another approach to determine the submodule capacitance for a CHB converter, which is based on the maximum energy stored in the capacitor [4, 81, 83]:

$$C_{dc_{(CHB,e)}} = \frac{S}{f_{sw}\left(V_{dc}\Delta V_{dc\%} - \frac{\Delta V_{dc\%}^2}{2}\right)} \tag{2.9}$$

where f_{sw} is the switching frequency of each submodule. Note that, both key equations (2.4) and (2.8) used for the design of the MMC and CHB DC-link submodule capacitance refer to the minimum capacitance required to maintain the 2nd harmonic voltage ripple within the limits (i.e. $\Delta V_{dc\%}$) during normal (rated) operation. Moreover, eq. (2.4), (2.8) and (2.9) allows the user to design the DC-link capacitance with respect to only the low-frequency ripple stresses. To assess also the high-frequency ripple related to switching harmonics, other considerations must be done, which can be found in [82].

2.2.3 Modulation Techniques

The last 20 years have seen extensive research into modulation techniques for multilevel converters. Figure 2.8 provides an overview of the traditional modulation methods for AC/DC multilevel converters based on the switching frequency [84]. The primary distinction among the three modulation families lies in the switching frequency: PWM-based methods are categorized as high-switching frequency approaches, while the fundamental switching frequency techniques usually perform one or two commutations of power semiconductors over one fundamental cycle of the output voltage, meaning that they have the lowest switching frequency. Mixed switching frequency modulation method falls between

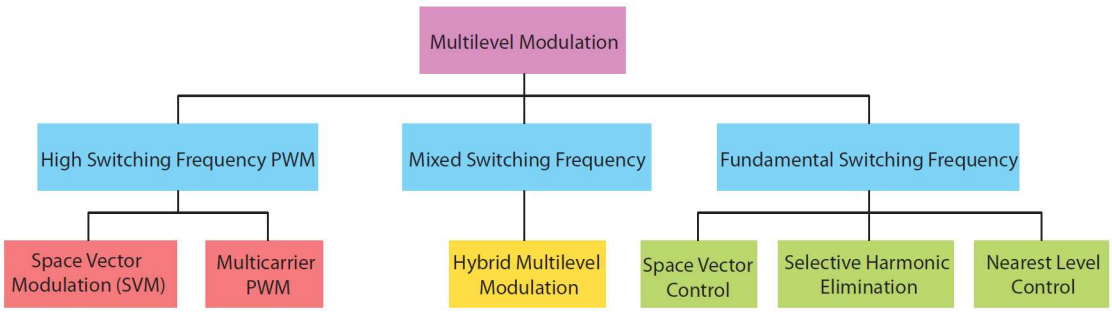


Figure 2.8: Classification of multilevel converter modulation techniques [77, 84].

the aforementioned methods in terms of switching frequency. In most cases, multilevel converters are utilized as inverters/rectifiers to generate a low-frequency, high-resolution AC waveform at 50/60 Hz from a DC voltage. To minimize commutation losses in high-power converters, the switching frequency should be kept as low as possible. Conversely, higher switching frequencies are needed to achieve high voltage resolution and dynamic range. For industrial applications of multilevel converters, in particular, the most utilized modulation strategies are PWM-related. In this context, a very popular modulation technique already introduced in the previous section is the classic carrier-based sinusoidal PWM that implements the phase-shifting technique (i.e. PS-PWM) to remove or reduce specific groups of harmonics in the synthesized output AC voltage waveform [84]. For the scope of this work, it is only necessary to specify that the PS-PWM technique is adopted for the operation of the multilevel stage of the SST topology selected, whereas the detailed analysis of multilevel modulation techniques is omitted. A detailed description of these methods can be found in [84] and [77].

2.2.4 Comparison and Discussion

The MMC and CHB converters share several characteristics, such as modularity, the potential for fault-tolerance implementation, low voltage THD, multilevel operation, low switching frequency and dv/dt, and filter size. Table 2.1 reports the main equations used in this work to design both converters. The additional advantage of the MMC is the availability of the MVDC link for connecting MV loads and sources. On the other hand, the highly complex control system, bulky filter on the DC side, and high overall cost are the main MMC disadvantages when compared to the CHB converter. As a result, so far it has only been used in HV applications and not yet widely adopted for MV applications. A detailed and comprehensive assessment of the MMC and CHB topologies for MV applications has been reported in [4]. In this work, both converters wee designed based on different grid requirements (voltage and power levels), and the results were compared in terms of power device requirements. The design of both converters was made according to the equations reported in Section 2.2.1 for the MMC and in Section 2.2.2 for the CHB, thus according to [66, 77, 79, 81]. An utilization factor of the semiconductor voltage of $k_u = 0.65$ was taken into account, meaning that the maximum voltage over

Table 2.1: Main design equations of the MMC and CHB converters.

Design Quantity	MMC	CHB
MVDC link, V_{dc}^{tot}	$\frac{\sqrt{2}V_{ac}}{\sqrt{3}m_r}$	$\frac{\sqrt{2}V_{ac}}{\sqrt{3}m_r}$
N° of submodules, N	$\frac{\sqrt{2}V_{ac}}{\sqrt{3}m_r k_u V_b}$	$\frac{\sqrt{2}V_{ac}}{\sqrt{3}m_r k_u V_b}$
Capacitance, C_{dc}	$\frac{S}{3mN\omega\Delta V_{dc\%}V_{dc}^2}\left(1-\left(\frac{m\cos\phi}{2}\right)^2\right)^{\frac{3}{2}}$	$\frac{m\hat{I}}{2}\frac{1}{2\omega\hat{V}_{dc,2\omega}}$

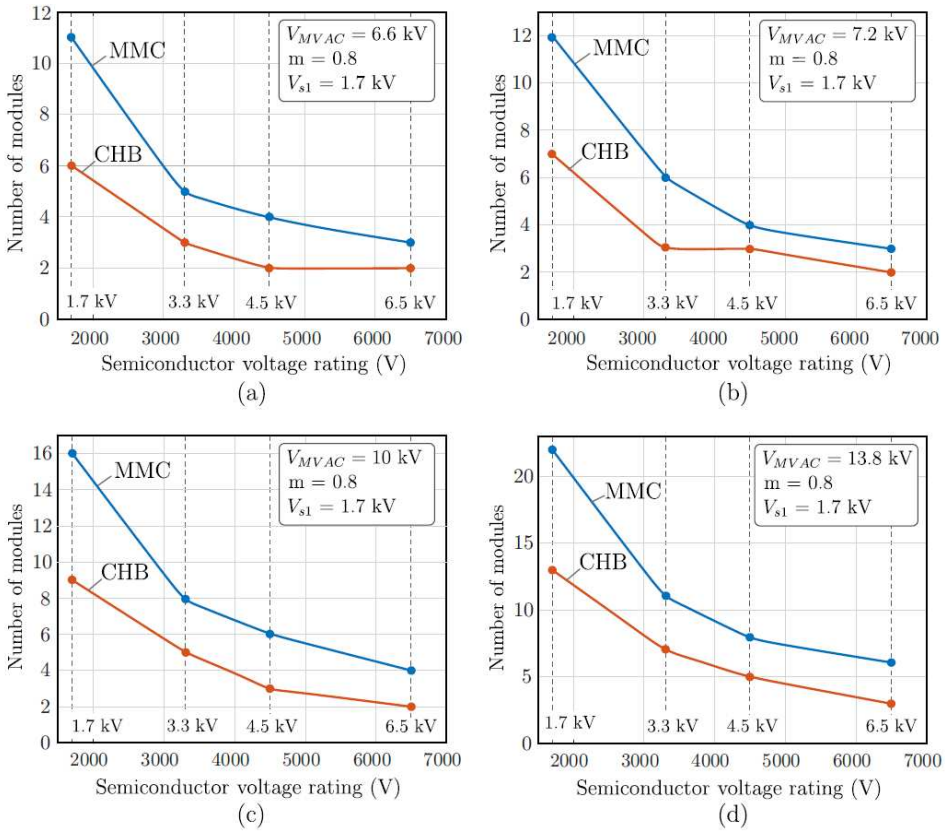


Figure 2.9: Comparison between the MMC and CHB converters. Required number of modules in function of the selected semiconductor blocking voltage for different grid voltages: (a) 6.6 kV, (b) 7.2 kV, (c) 10 kV, (d) 13.8 kV. [4].

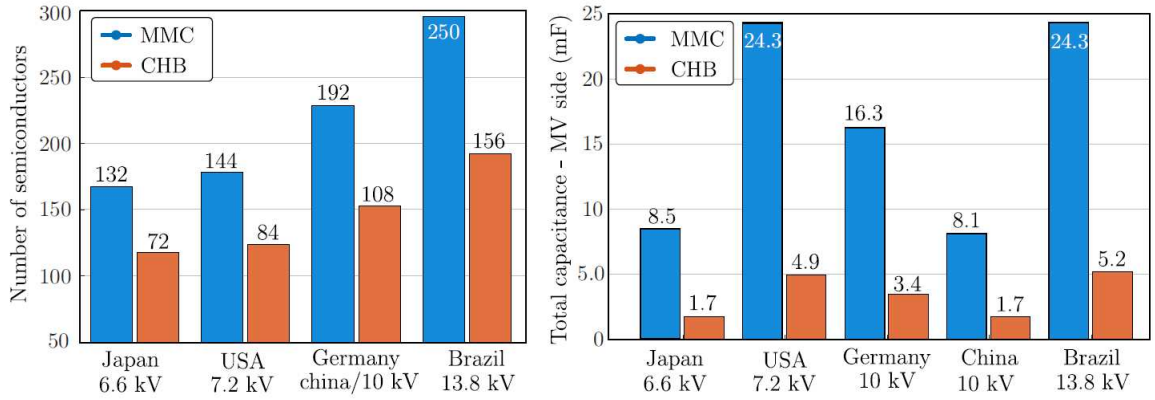


Figure 2.10: Comparison between the MMC and CHB converters. (a) Number of semiconductors according to the grid voltage application (considering a semiconductor blocking voltage of 1.7 kV), (b) required capacitance according to the grid voltage [4].

the semiconductor is 65% of its voltage rating. The results are presented in Fig. 2.9 and Fig. 2.10. Fig. 2.9 shows the number of modules required by each topology based on the voltage rating of the chosen semiconductor, for various grid voltage cases. It can be observed that the CHB converter requires fewer modules compared to the MMC, resulting in a lower number of components. Moreover, the total number of semiconductors required by each converter is shown in Fig. 2.10 (a) when semiconductors rated for 1.7 kV are used. Furthermore, the total required DC link capacitance (per phase) for both converters is plotted in Fig. 2.10 (b), for different grid requirements. These results indicate that the total capacitance of the MVDC link can be reduced by approximately 80% when the CHB converter is adopted instead of the MMC. To explore the full analysis, refer to [4]. Overall, the CHB offers more advantages than the MMC in terms of the number of modules and semiconductors required, necessary capacitance, as well as modulation and control implementation simplicity. Moreover, as the availability of a MVDC link is not a requirement in the UNIFLEX-based SST analyzed in this work, the CHB is definitely a better option. For these reasons, the PS-PWM modulated CHB converter is selected as MV AC-DC stage of the SST considered in this work.

2.3 DC-DC Isolation Stage

2.3.1 Topologies Discussion and Requirements

The DC-DC stage is the fundamental component of the SST architecture, as it connects both sides of the SST (either they are both MV in case of ER-SST applications or MV and LV in case of utility smart grid SSTs) and provides galvanic isolation at high or medium frequency thus maintaining a compact footprint. This stage is particularly challenging to implement due to its strict requirements [4, 30, 32]. The high voltage and current levels involved in power conversion make the DC-DC stage responsible for most of the system losses, so it requires careful attention during the design phase. For instance, the MV side of the SST works with high voltages and low currents, therefore high blocking voltage capability is required for the semiconductors, magnetics and other passive components installed on the DC-DC converter. On the other hand, in case of LV AC/DC-link availability, this stage operates with low voltages and high currents, hence high current capability is required [4, 30, 32]. The main bottleneck of such systems is the design of the high/medium frequency transformer. To increase system efficiency and power density, thus decreasing the size and weight, high switching frequencies are required, which are nowadays made available and extremely high due to the advancement in Wide BandGap (WBG) semiconductors technology. However, higher switching frequency results in higher switching losses. Therefore, in practice higher efficiencies are achieved by implementing ZVS and/or Zero-Current Switching (ZCS) modulation schemes, as these converter topologies are intrinsically prone to allow that in certain operating conditions [30]. Moreover, also the DC-DC converter design is often done specifically for enhance the soft switching operation of the converter.

Hence, as the DC-DC stage is a key component of a SST, it is important to highlight its main requirements, which can be summarized as follows [4]:

- High voltage capability in the MV side: able to handle voltage levels of approximately 10 kV to 25 kV;
- High current in the LV side, if available: expected current levels in the range of 100 A to 2000 A;

- High voltage isolation: the medium or high frequency transformer used must provide isolation in the range of 10 kV to 15 kV, regardless of the solution adopted for this stage;

- Decoupling between both sides of the converter: the ability to provide total decoupling between two MVAC grids of between the MVAC grid and a LVAC grid so that the these stages can operate independently from each other. This means the MV AC-DC stage can operate and provide the required ancillary services to the MV grid without disturbing or being disturbed by the MV/LV DC-AC stage operation. To achieve such decoupling, both DC links must be maintained constant with minimal voltage oscillation (i.e., 5% in case of LVDC link [32]), and the DC-DC must ensure voltage regulation;

- Power flow control: the DC-DC converter must be able to control the power flow between its input and output terminas and manage the connection of loads on both sides;

- Bidirectionality: bidirectional power flow capability is required for the DC-DC stage for almost any scenario unless the reverse power is not allowed in the specific distribution grid system under evaluation. Despite this, bidirectionality is considered a requirement in this thesis.

- DC breaker function: Overload and short-circuit protection (acting as a DC breaker) for the possible load/source/microgrid connected to the LVDC link [16-19, 22].

- High efficiency: the SST is intended not only to replace the LFT of the distribution system but also to solve problems resulting from grid modernization. However, high efficiency is expected for the SST to compete with the traditional LFT [5]. In this context, the DC-DC isolation converter plays a crucial role since it is recognised that its efficiency is usually slightly less than that of the other stages [4].

The DC-DC isolation stage of the SST can be implemented using various suitable topologies, which can be classified according to their operation principle as shown in Fig. 2.11 [4]. There are three different families of isolated DC-DC converters suitable for the SST application: Active Bridge, Resonant Converters, and Full-Bridge DC-DC converter

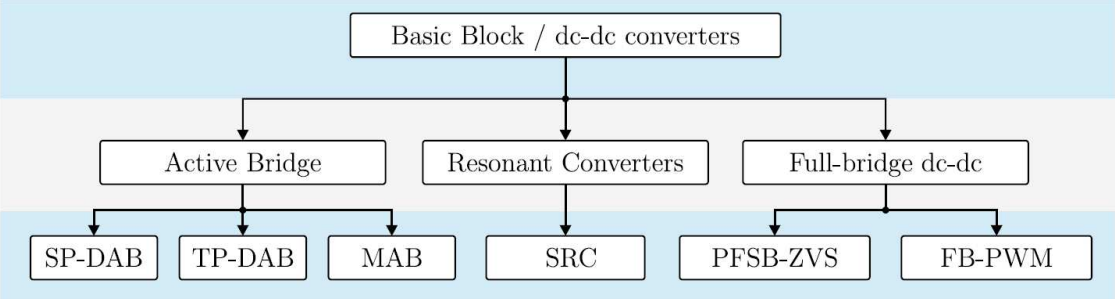


Figure 2.11: Classification of the most suitable DC-DC converters to be used as the basic module of the DC-DC stage. The topologies can be classified in three types: active bridge converters type, resonant converter and full-bridge conventional converters [4].

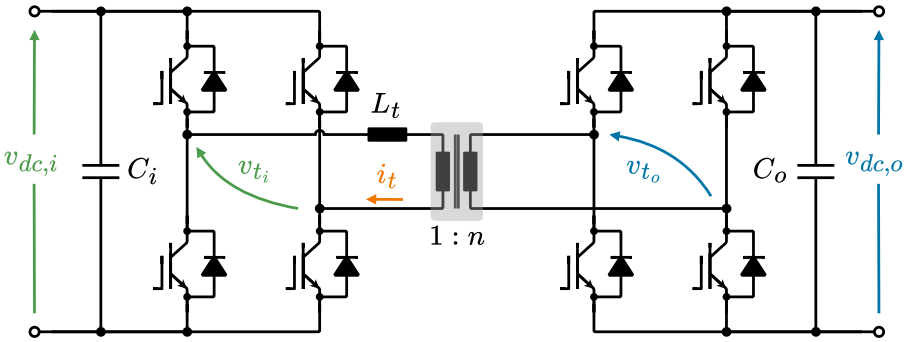


Figure 2.12: Dual Active Bridge (DAB) topology.

families. The DAB converter, which belongs to the Active Bridge family, and the Series Resonant Converter (SRC), belonging to the Resonant Converters family, are the two main realization options typically considered. The DAB converter was proposed in [85] and patented in 1989 [86] by DeDoncker. In its standard form, shown in Fig. 2.12, the DAB converter consists of two H-Bridges connected to the input and output terminals of an isolation transformer which features a leakage inductance L_t. By actively controlling these two bridges (hence the name of the converter topology), the transformer current and thus the power flow can be properly controlled. The main advantages of this converter are the possibility to implement a simple technique (i.e. square wave PS modulation) still guaranteeing good system performances and the simple control system required [4]. Furthermore, ZVS can be achieved within a certain operating range and converter design [4, 30, 85]. Also, the DAB converter is available in two variants, as shown in Fig. 2.11: the single-phase (SP) and three-phase (TP) one. However, even if the TP-DAB topology

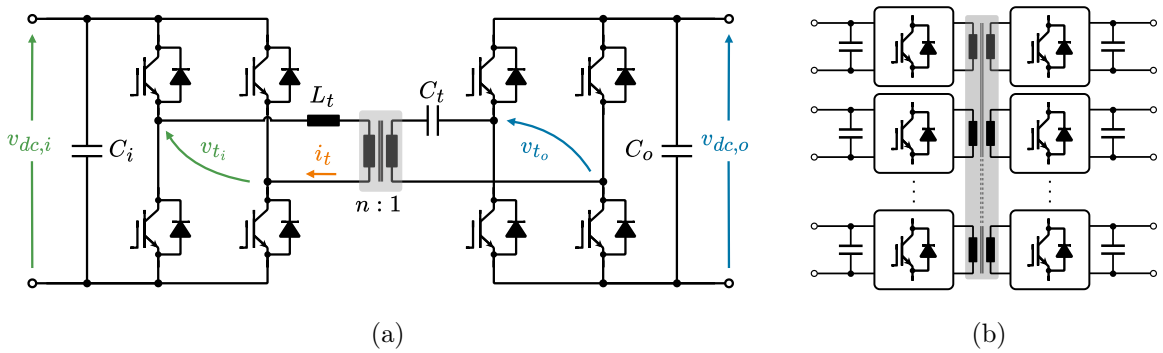


Figure 2.13: SRC and MAB topologies.

shows some good benefits (as, for example, reduced current stresses on the DC-link [4], and therefore reduced voltage ripple and required total capacitance), the most common and employed topology is the SP-DAB [4]. Fig. 2.13b shows another variant topology derived from the DAB is the Multiple Active Bridge (MAB) (or Multi Active Bridge), which is obtained by connecting multiple active bridges to a multiwing transformer [4, 40, 87, 88]. From this family, the most known topologies are the Triple Active Bridge (TAB) [89, 90] and the Quadruple Active Bridge (QAB) converters [4, 40, 88] in which, respectively, three and four active bridges are interconnected through a multiwinding transformer. This structure preserves the same advantages of the DAB but also offers the possibility to connect more sources/loads with different voltage and power levels to the same converter, enhancing the power density and compactness [4]. However, the optimized design of the multiwinding transformer, which is the key element of the MAB converter, and the implementation of a controller that allows decoupling the operation of each active bridge are the main drawback of this topologies [15]. Moreover, a multiwing transformer failure interrupts the operation of all connected H-bridges. By adding a capacitor in series with the leakage inductance L_t, a resonant tank is formed and the basic circuit topology of the SCR is obtained and shown in Fig. 2.13a. This converter is well-known and it has been very used in a large range of voltage and power applications [4]. Because of the resonant tank, when a square wave voltage excitation is applied to the transformer, a piece-wise sinusoidal current is obtained [4, 30]. Therefore, the main difference in the operation of the SRC compared to the DAB is the sinusoidal current shape. Another feature of the SRC is that the input and output ports are intrinsically tightly coupled.

Therefore, it doesn't require a closed-loop control [30]. Therefore, in contrast with the DAB, the SRC doesn't need complex modulation strategies and control schemes, and it can inherently achieve ZVS/ZCS for many operating points [30]. However, when a control on the power flow or the output voltage is required, the lack of controllability might be more a drawback instead of a benefit [30]. Finally, also the phase-shifted full bridge (FB) converter deserves a mention as a possible viable option to implement the isolation DC-DC stage in SST applications. It was recently proposed for multicellular Power Factor Correction (PFC) rectifier for telecom applications [91]. However, being the topology typically only unidirectional and requiring an output inductor that would carry high currents in case of LVDC-link availability, this topology is generally not suitable for high-power SST applications [30]. A more detailed analysis and comparison of all these DC-DC topologies can be found in [4].

For the purpose of this work, and in light of the benefits and drawbacks briefly highlighted above, the DAB topology is confirmed (with reference to the UNIFLEX-based SST) as DC-DC isolation stage topology for the SST architecture investigated in this work. This is due, at first instance, to the simplicity of the modulation and control of the DAB. Furthermore, it is shown in [4] that the DAB offers the highest efficiency, along with the SRC and FB, among the topology proposed in a power range of few to tens of kW. Also, the SRC and FB present drawbacks in terms of, respectively, controllability and bidirectionality compared to the DAB. Therefore, the DAB is the best choice among these three topologies. Moreover, the SP-DAB is preferred over the TP-DAB because the performances of both converters are quite similar but the DAB requires fewer semiconductor components. From the comprehensive literature review carried out in [4], the MAB converter could be directly discharged because of its poor performance, in terms of efficiency, compared to other DC-DC topologies. However, its potential as core DC-DC isolation crosslink has been evaluated in [4, 88, 92]. It resulted that, besides the economic advantage enabled by the MAB converter, the efficiency of the MAB-based SST was similar to the one brought by the DAB-based SST. Therefore, despite the DAB converter has been confirmed as the DC-DC stage in this work due to its simplicity, this topology deserves more attention for future investigations.

In the following, the operation principle of the DAB is briefly presented along with the

selection principle of the leakage inductance L_t, transformer turns ration n, rated phase shift angle φ and output capacitance C_o.

2.3.2 Dual Active Bridge Operation and Design

The DAB topology is shown in Fig. 2.12. Has already mentioned, it consists of two active bridges interfaced via a HFT that features a leakage inductance, namely L_t. The basic operation principle of the DAB converter consists of controlling the phase displacement between the AC voltage generated by both active bridges in order to regulate the power flow across the HFT. This comes from power system theory, where the active power transferred among two electrical grids interfaced via an inductor is controlled by changing the phase shift between the grid voltages, while the reactive power is controlled by changing the amplitude of the voltages [93]. Therefore, based on the aforementioned operation principle, the resulting DAB equivalent model is shown in Fig. 2.14 [94]. To do so, depending on the modulation scheme adopted, the current and voltage waveforms at the HFT might be different, resulting in different operations. Among many strategies proposed [94–96],

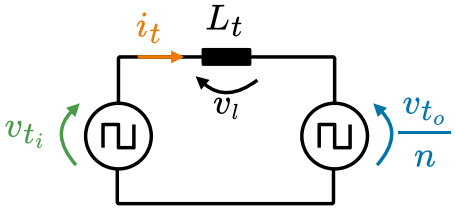


Figure 2.14: Equivalent circuit model of the DAB.

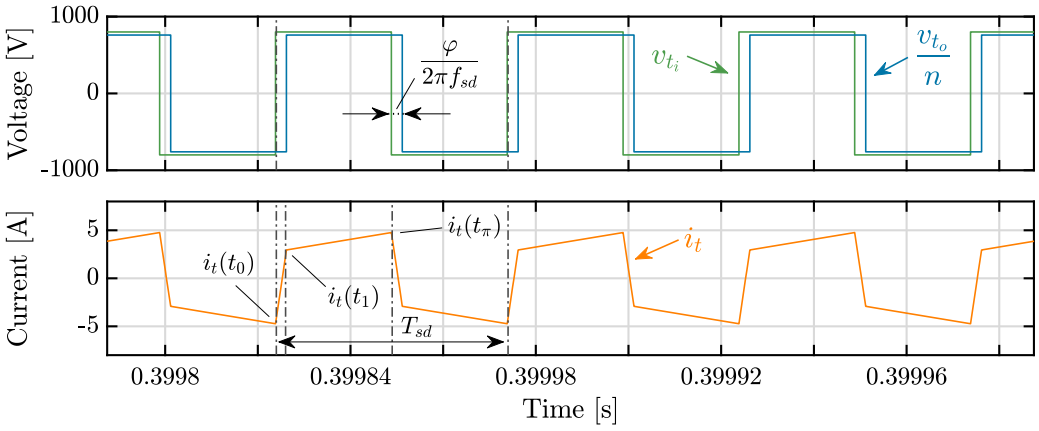


Figure 2.15: Typical DAB voltage and current waveforms at the HFT.

the phase-shift modulation (PSM) is the most adopted one because of its simplicity and performance. In this scheme, the active bridges both generates square voltage waveforms, i.e. with 50% duty cycle, at constant switching frequency f_{sd} and phase-shifted of a given angle φ. Fig. 2.15 shows the main DAB voltage and current waveforms when the PSM is employed. If the input/output voltages of the converter can be maintained closed to their nominal values, the PSM features ZVS during the turn-on of the semiconductors, low RMS current, symmetrical share of the losses among the semiconductor switches, high power transfer capability and simplicity of implementation [4]. For this reasons, and also because the investigation of advanced DAB modulation technique is not the aim of this work, the PSM is selected as modulation strategy for the DAB converter.

To design the converter passive elements, i.e. the leakage inductance L_t and the output capacitance C_o, the transferred average power (P_{dab}) equation of the converter must be derived when using the PSM. With reference to the equivalent circuit of Fig. 2.14, P_{dab} can be defined as [4, 85, 94]:

$$P_{dab} = \frac{1}{T_{sd}} \int_{t_0}^{t_0+T_{sd}} p_{dab}(t)\, dt = \frac{1}{T_{sd}} \int_{t_0}^{t_0+T_{sd}} v_{t_i}(t) i_t(t)\, dt = \frac{2V_{dc,i}}{T_{sd}} \int_{t_0}^{t_0+T_{sd}/2} i_t(t)\, dt \quad (2.10)$$

where $T_{sd} = 1/f_{sd}$ is the DAB switching period while $V_{dc,i}$ is the amplitude of the input voltage supplied to the DAB converter, with reference to Fig. 2.12. The inductor current i_t is defined as:

$$i_t(t) = i_t(t_0) + \frac{1}{L_t} \int_{t_0}^{t_0+T_{sd}} v_l(t)\, dt = i_t(t_0) + \frac{1}{L_t} \int_{t_0}^{t_0+T_{sd}} \left(v_{t_i} - \frac{v_{t_o}}{n} \right) dt \quad (2.11)$$

With reference to the waveforms of Fig. 2.15, it can be noted that i_t shows a piece-wise shape, which can be defined as [4, 85, 94]:

$$i_t(t) = \begin{cases} i_t(t_0) + \dfrac{v_{t_i} - \frac{v_{t_o}}{n}}{L_t} t, & t_0 < t < t_1 \\ i_t(t_1) + \dfrac{v_{t_i} - \frac{v_{t_o}}{n}}{L_t} (t - t_1), & t_1 < t < t_0 + \frac{T_{sd}}{2} \end{cases} \quad (2.12)$$

where:

$$i_t(t_0) = -\frac{\left(V_{dc,i} - \dfrac{V_{dc,o}}{n} \right) \pi - 2nV_{dc,o}\varphi}{4n\pi f_{sd} L_t} \quad (2.13)$$

$$i_t(t_1) = \frac{\left(\dfrac{V_{dc,o}}{n} - V_{dc,i} \right) \pi - 2V_{dc,i}\varphi}{4\pi f_{sd} L_t} \quad (2.14)$$

where $V_{dc,o}$ is the amplitude of output voltage. Note that $i_t(t_0) = -i_t(t_\pi)$ only during the steady-state. Replacing eq. (2.12) in (2.10) and rearranging it, the transferred average power of the DAB is obtained as [4, 85, 94]:

$$P_{dab} = \frac{V_{dc,i}V_{dc,o}}{2nf_{sd}L_t}\varphi\left(1 - \frac{|\varphi|}{\pi}\right) \tag{2.15}$$

Introducing the phase-shift ratio d as $d = \varphi/\pi$, eq. (2.15) can be rewritten as [97, 98]:

$$P_{dab} = \frac{V_{dc,i}V_{dc,o}}{2nf_{sd}L_t}d\left(1 - |d|\right) \tag{2.16}$$

Fig. 2.16a shows the transferred active power P_{dab} as a function of the phase shift angle φ. As can be noted, the maximum positive and negative transferred power is obtained when $\varphi = \pm\pi/2$. Equation (2.15) is used in this work to design, at rated conditions, the leakage inductance L_t as:

$$L_t = \frac{V_{dc,i}^{nom}V_{dc,o}^{nom}}{2nf_{sd}P_{dab}^{nom}}\varphi^{nom}\left(1 - \frac{|\varphi^{nom}|}{\pi}\right) \tag{2.17}$$

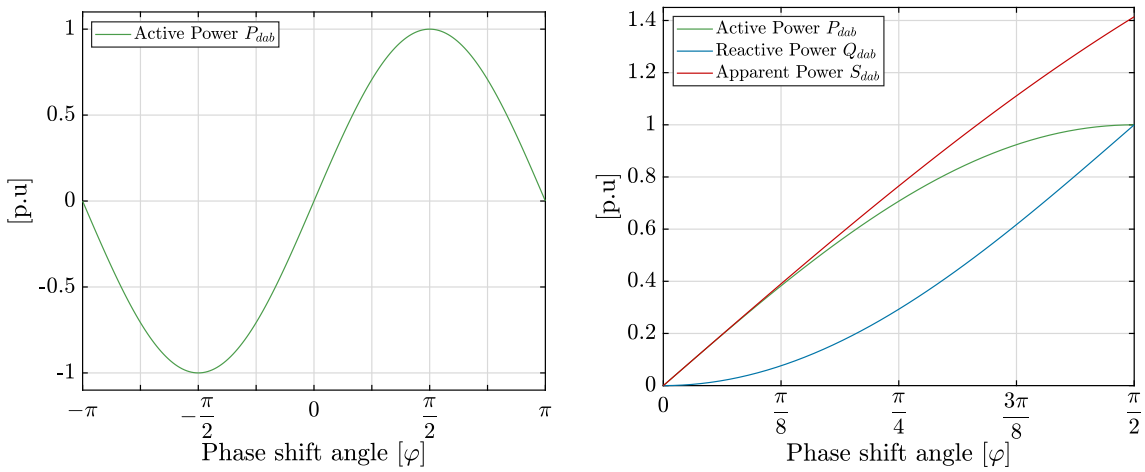
where the superscript "nom" is used to indicate the nominal value of the parameters. To do so, once the rated power P_{dab}^{nom}, the input and output voltages $V_{dc,i}^{nom}$ and $V_{dc,o}^{nom}$ and the semiconductor switching frequency f_{sd} are defined (depending on the system and requirements), the leakage inductance L_t is calculated after choosing the transformer turns ratio n and the rated phase shift angle φ^{nom}. In the first instance, the HFT turns ratio n is typically chosen accordingly to the required output voltage compared to the input one. Typically, the value of n can also be object of an optimization procedure of the converter design, especially when advanced modulation technique are implemented, with the aim to expand the ZVS region [94]. However, this is not the focus of this work. Therefore, in this thesis n is chosen as:

$$n = \frac{V_{dc,i}^{nom}}{V_{dc,o}^{nom}} \tag{2.18}$$

Either way, the value of n is limited by the maximum input and output voltages as [94]:

$$n < \frac{V_{dc,i}^{max}}{V_{dc,o}^{max}} \tag{2.19}$$

where the superscript "max" is used to indicate the maximum value of the parameters. The value of φ^{nom} must be design in the rage of $-\pi/2 < \varphi^{nom} < +\pi/2$, according to Fig. 2.16a. However, the selection procedure of φ^{nom} deserves more attention because,



(a) (b)

Figure 2.16: (a) Active power of the DAB in function of the phase shift angle φ and (b) comparison of the active, reactive and apparent power increments as a function of of φ in the range of $0 \leq \varphi \geq \pi/2$.

when φ increases or decreases with respect to $\varphi = 0$, a reactive power flow originates at the HF link of the converter. This is quite simple to prove with a simplified time domain analysis of the converter, in which only the fundamental components of the transformer voltage and current are considered (i.e. at $\omega_{sd} = 2\pi f_{sd}$). The accuracy of this analysis was presented in [4]. In this context, the transformer voltages are defined as:

$$v_{t_i} = \frac{4V_{dc,i}}{\pi} \sin(\omega_{sd} t) \tag{2.20}$$

$$v_{t_o} = \frac{4V_{dc,o}}{\pi n} \sin(\omega_{sd} t + \varphi) \tag{2.21}$$

Therefore, the active, reactive and apparent powers can be calculated as follow:

$$P_{dab}^{fund} = \frac{4V_{dc,i}V_{dc,o}}{\pi^3 n f_{sd} L_t} \sin(\varphi) \tag{2.22}$$

$$Q_{dab}^{fund} = \frac{4V_{dc,i}V_{dc,o}}{\pi^3 n f_{sd} L_t} (1 - \cos(\varphi)) \tag{2.23}$$

$$S_{dab}^{fund} = \sqrt{P_{dab}^{fund^2} + Q_{dab}^{fund^2}} \tag{2.24}$$

As fig. 2.16b shows, for growing φ the active power increases sinusoidally while the reactive power increases exponentially. This means that, for small values of φ (i.e. typically in the range of $0 < \varphi < \pi/4$) a small increment of φ determines a significant increment of active

power P_{dab}^{fund} while just a light increases in the reactive power Q_{dab}^{fund}. Instead, for larger values of φ (i.e. in the range of $\pi/4 < \varphi < \pi/2$), even a small increment in φ may cause a relevant increment in the reactive power, while the active power just slightly increases. In light of that, the reactive power circulation must be minimized as much as possible since its circulation increments the HFT current and therefore the losses, reducing the converter efficiency [4]. Moreover, ideally zero reactive power would be required as the DAB is interconnecting two DC systems whose exchange only active power. Therefore, the rated phase shift angle φ^{nom} should be selected in the range of $0 < \varphi < \pi/4$.

Finally, the output capacitance C_o is also designed. Considering the SST topology investigated in this work, i.e. the UNIFLEX-based SST, each DAB is linking an H-Bridge submodule of the AC-DC rectifier multilevel stage with either a H-Bridge of the Port 2 DC-AC inverter stage (which is also a multilevel CHB topology, as Fig. 2.2a shows) or with a single H-Bridge belonging to the Port 3 inverter. Therefore, the output capacitor of each DAB converter is shared with either a submodule of a CHB inverter or with a single H-Bridge inverter. This is due to the ISOS configuration of the UNIFLEX-based SST. Hence, in both cases the output capacitance C_o of the DAB converter can be designed by using eq. (2.8) introduced in Section 2.2.2.

2.4 DC-AC Inverter Stage

The last stage of conversion of the triple-stage SST under investigation is the DC-AC inverter stage (i.e. the Voltage Source Inverter (VSI)). The UNIFLEX-based SST features a CHB-based multilevel VSI that realizes the Port 2 of the converter and a single H-Bridge inverter per-phase that realizes the Port 3 connection. However, Port 3 per-phase topology is not limited to one single H-Bridge but, depending on the voltage or current levels required for that connection, it can feature more submodules connected in series or even in parallel, thus realizing either again a CHB converter or different topology/architecture. The challenges of this stage relate to the its voltage level. For MV level, these are the same presented in Section 2.2 for the AC-DC rectifier stage, as it usually interface a MV distribution grid. For LV level, the high current involved and the EMI filter design are mein challenges of this conversion stage [4]. Moreover, for LV three-phase connection

usually a fourth wire (namely the neutral wire) is required based on the Terra-Terra (TT) configuration, forming the four wire system. These affect the topology selection for this stage. Among them, the standard two level VSI, the three-level Neutral Point Clamped (NPC) and the T-type topologies are commonly adopted [4]. An evaluation of the possible converter topologies suitable for implementing a LV DC-AC inverter stage can be found in [4].

The AC-DC inverter stage of the UNIFLEX-based SST is realized whit the already presented and quited discussed CHB topology. Furthermore, the DC-AC inverter stage plays a secondary role in the analysis carried out in this work. Therefore its detailed topological description will be omitted here.

2.5 Final SST Configuration and Considerations

Before presenting and discussing the final SST architecture investigated in this work and summarizing the key points covered in this Chapter, to round off the converter design procedure also the grid filter (i.e. the input AC inductance) design must be covered.

2.5.1 Grid Filter Design

Grid filter covers a twofold role in grid-connected Voltage Source Converters (VSCs). It first allows the VSC to exchange active and reactive power with the grid as happens among different network nodes in the legacy grid. Therefore it must present a dominant inductive behavior to replicate the well-known interactions among synchronous generators in transmission lines, where the power flow is regulated by controlling the phase and magnitude of the PCC voltages [93, 99]. On the other hand, the voltage generated by VSCs contains, beside the fundamental component, a wide range of harmonics due to the switching nature of the waveform. These harmonics may trigger an undesired harmonic current flow into the grid, which can disturb the normal operation of loads and equipment and increase the system losses. Therefore, to prevent such unwanted phenomena, these current harmonics must be properly filtered out, guaranteeing sinusoidal currents waveform with low distortion (i.e. low THD) [99]. Among many possible passive filter implementations, the L, LC and LCL filters are the most common ones. Their topological

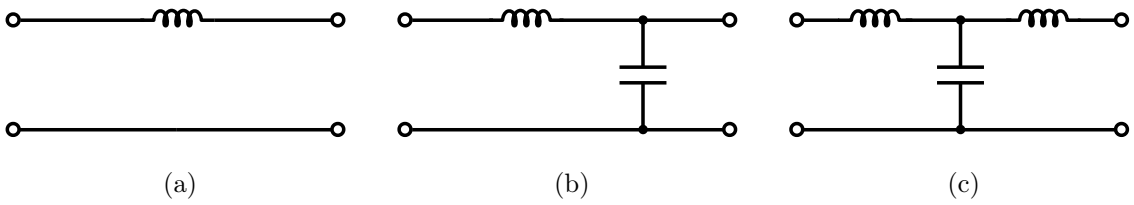


Figure 2.17: Single-phase representation of common grid filter topologies: (a) L filter; (b) LC filter; (c) LCL filter.

implementation is shown in Fig. 2.17. The L filter is simplest solution to comply with both requirements specified above. However, if the switching frequency of the VSC is too low (as usually happens for high power converters, to limit switching losses), the required inductance may be quite large and therefore the inductor realization can be expensive and bulky. On the other hand, for higher switching frequencies even a small inductance may be enough, as its reactance increases with the frequency. However, still the encumbrance of the inductor may be a problem as usually this system must be well compact. It is in this frame that high-order filters like LC or LCL come in to play to help the designer. With this solution, the size and cost of inductors and capacitors can be reduced. Nevertheless, the main disadvantage of those filters, in which more than one reactive element is used, is the resonance problem. Indeed, when prior selecting the proper filter, a trade-off between the filter size and the switching frequency should be done. Then, to chose the filter parameters, typically a good criterion is to achieve a balance among the topology and the size of the reactive elements and the power losses [99]. In this work, for simplicity an L filter is selected, as the network is interfaced with the chosen SST through a multilevel topology (i.e. the CHB converter), which normally shows a good equivalent switching frequency $f_{sw,eq} = 2N_{(CHB)}f_{sw}$ even if the rated power is high [66].

To design the L filter, many strategies were proposed in the literature: among them, the maximum current ripple criterion [81, 100–102], the power transfer [81] and power losses principles [17] and other iterative algorithms [102] are common design procedure. In this thesis, the filter inductor L_f is design based on the worst case current ripple [101]. The peak ripple current is defined as the difference between the peak volt-second and the average volt-second applied to the filter inductor over the switching period. Considering the CHB converter shown in Fig. 2.5b with each submodule DC-link voltage equal to the

nominal value V_{dc} as defined in eq. (2.2). The maximum ripple occurs when the duty cycle is set to be 50%. In this case the average volt-second equals zero. On the other hand, the peak volt-seconds applied to the inductor is equal to:

$$V_{L_f}\,\Delta t = \frac{V_{dc}}{2}\,T_{sw,eq}\,\frac{1}{2} = \frac{V_{dc}}{2}\,\frac{1}{2N_{(CHB)}f_{sw}}\,\frac{1}{2} = \frac{V_{dc}}{8N_{(CHB)}f_{sw}} \tag{2.25}$$

and its lasts for half of the equivalent switching period of the converter $T_{sw,eq} = 1/f_{sw,eq}$. Assuming that the fundamental voltage is constant during one switching period, from (2.25) the minimum inductance value can be calculated as [101]:

$$L_{f,min} = \frac{V_{L_f}\,\Delta t}{\Delta i_{L_f,max}} = \frac{V_{dc}}{8N_{(CHB)}f_{sw}}\,\frac{1}{\sqrt{2}I_{L_f}\Delta i_{L_f\%}} \tag{2.26}$$

where $\Delta i_{L_f,max}$ is the maximum allowable peak ripple current, defined as the peak inductor current $\hat{I}_{L_f} = \sqrt{2}I_{L_f}$ times the allowable percentage current ripple $i_{L_f\%}$.

2.5.2 Final SST Configuration and Summary

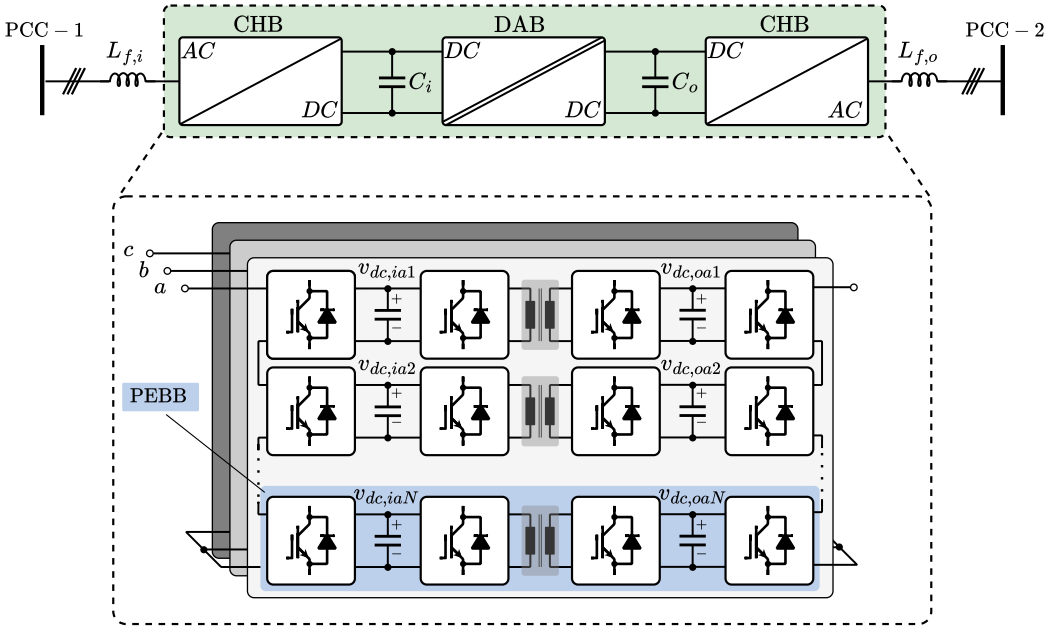
The aim of the research work developed in this thesis is to further investigate the UNIFLEX-PM converter, addressing many key points there were left open at the time of the project, i.e. the modeling, control and stability analysis of the system (see Section 1.6). Considering the advancement in SST technology of the last two decades, before explore these aspects the UNIFLEX-PM topology had to be revised based on the current state-of-the-art. On this basis, the topology review and discussion carried out in this Chapter allowed to confirm the UNIFLEX-based SST as selected topology for future investigation, within the context of Intelligent Energy Router for future smart distribution networks.

Finally, the key points covered in this Chapter whose define the SST topology and application investigated in this work can be summarized as follow:

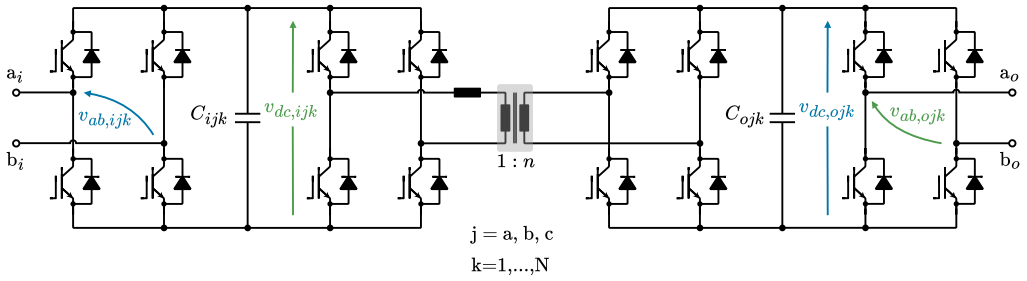
- The final topology under investigation is a Three-Phase Triple-Stage ISOS SST. It is based on the Cascaded H-Bridge and Dual Active Bridge topologies and it features two MV-level ports. The SST topology and its configuration are shown in Fig. 2.18a, whereas the fundamental PEBB is presented in Fig. 2.18b;

- The application scenario considered in this work provides that the SST works as Intelligent Energy Router linking two distribution network through the MV-level

ports, as Fig. 2.18a shows. Further extension of the select SST topology, which is planned for future works, involves the implementation and analysis of a third port to interface a LV utility grid. In this context, different SST configuration or topologies might be considered to solve the power routing issue for the UNIFLEX-PM topology highlighted in Section 2.1 and to bring an easy-to-scale SST topology. To this end, in the context of utility distribution grid applications, through the HEART project many researches explored and analyzed the deployment and suitable topologies to properly integrate extra LV ports in a SST system [4, 32];



(a)



(b)

Figure 2.18: (a) Selected SST architecture and its applications: Three-Phase Triple-Stage ISOS topology featuring two MV-level ports and interconnecting two distribution grids; (b) basic PEBB for the selected SST topology.

- MV AC-DC Rectifier Stage: to implement this conversion stage the CHB topology has been selected because of its advantages in terms of number of submodules, semiconductor requirements, necessary capacitance and modulation and control complexity compared to the MMC solution, which becomes a more attractive solution when a MVDC-link is requested. For this work, the PS-PWM has been selected to drive the CHB converter;

- DC-DC Isolation Stage: the single-phase DAB converter has been selected as core isolation stage due to its simplicity in both modulation and control and for its good performances in terms of efficiency. The square-wave PS modulation is chosen;

- MV DC-AC Inverter Stage: being the port 2 of the converter interfacing a MV distrubtion grid, as for the MV rectifier stage, the CHB topology and the PS-PWM modulation are adopted;

Chapter 3

Solid-State Transformer Modeling and Control System Design

In this Chapter, the control system for the SST topology investigated (see Fig. 2.18a) is designed and its operation is validated through time-domain simulations. Differently from the original control scheme proposed for the UNIFLEX-PM converter, i.e. a Dead-Beat controller [13], the control strategy proposed in this work is developed in the rotating dq reference frame and, moreover, it is able to work properly also during unbalanced load conditions that may lead to unbalanced DC-link voltages among different submodules (i.e. the local DC-link voltages) or phases (i.e. the clustered DC-link voltages). The control system is tuned by means of the open-loop transfer functions of the system. To obtain these transfer functions, the system to be controlled must be properly modeled. For this purpose, the first step of the SST modeling process is the development of the switching model, through which the average model of the converter is derived. The average model of the converter allows to capture the fundamental behavior of the system, thus synthesize its low-frequency behavior and removing high-frequency noise due to switching harmonics [103]. Then, the average model is perturbed and linearized around an steady-state equilibrium point, obtaining the small-signal model of the converter. Through it, the relevant open-loop transfer function can be derived and therefore the control system can be finally tuned in order to ensure a stable closed-loop operation of the SST. The controller design process is outlined in Fig. 3.1.

In this Chapter, the average model of the rectifier, isolation and inverter stages of

the SST are derived. Based on these representations, the relative small-signal models are derived. Then, the plants useful for tune the control system are identified. Therefore, the overall SST control structure is presented and the tuning procedure is described. Finally, time-domain simulation results of the SST average model verify the effectiveness of both modeling and tuning procedures.

3.1 AC-DC Active Front-End Rectifier and DC-AC Inverter Modeling

In this Section, the modeling process for the SST rectifier and inverter stages is presented. Since they share the same converter topology, i.e. the multilevel CHB converter, their model development is gathered in the next.

3.1.1 CHB Switching and Average Model

Considering only the AC-DC AFE rectifier stage of the SST, which consists of the multilevel CHB topology, its circuit schematic and submodule representation are given in Fig. 3.2. From now on, the subscript i will be used to identify the input-side quantities of the SST, i.e. Port 1 of the converter, while subscript o will be used to identify the output-side quantities, i.e. Port 2 of the SST. Also, the subscript j identifies the phase variables (i.e. j = a, b, c) while k identifies the submodule index (i.e. k = 1, ..., N where

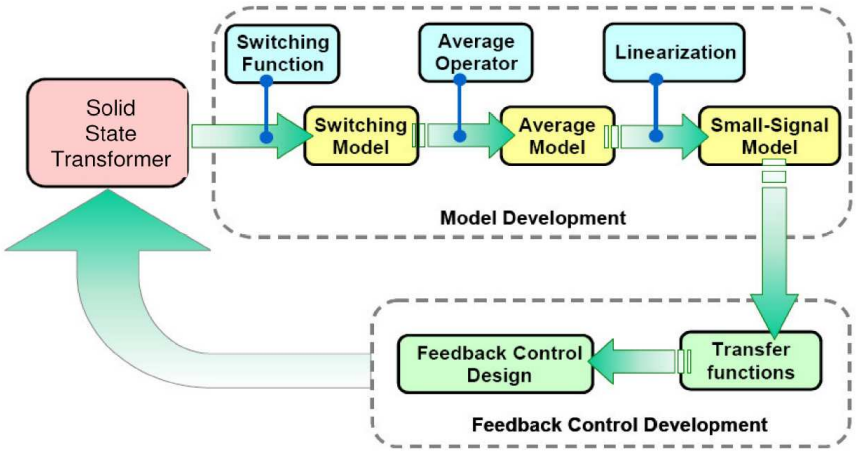


Figure 3.1: Controller design process [81].

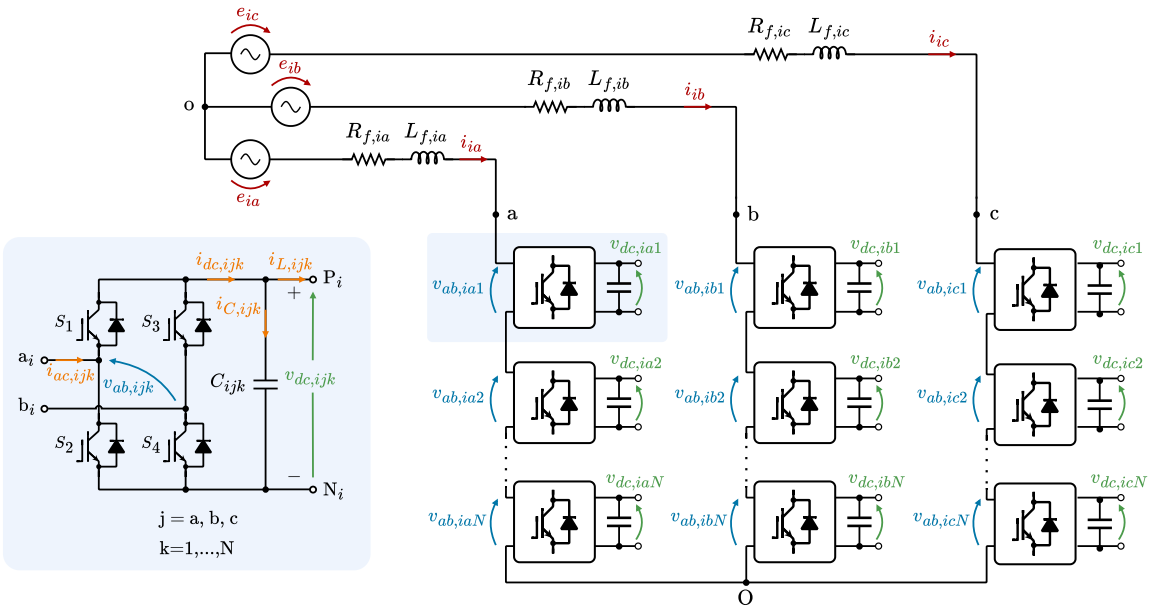


Figure 3.2: Grid-connected three-phase CHB converter and circuit representation of the k-*th* H-Bridge connected to the j-*th* phase.

Table 3.1: Switching states table of the k-*th* H-Bridge connected to the j-*th* phase of a CHB converter.

S_1	S_2	S_3	S_4	$v_{ab,ijk}$	$i_{dc,ijk}$
1	0	0	1	$v_{dc,ijk}$	$i_{ac,ijk}$
1	0	1	0	0	0
0	1	0	1	0	0
0	1	1	0	$-v_{dc,ijk}$	$-i_{ac,ijk}$

N is the number of submodules per phase). To analyze the operation of the converter, which is composed of several H-Bridges connected in series, the switching function of the single submodule is developed here. Considering the PS-PWM modulation technique as stated in Chapter 2, three possible output voltage states can be defined, considering that the devices connected to the same leg (S_1 and S_2, for example) must be switched ON and OFF complementarily to avoid short circuits. Table 3.1 summarize the switching combination of an H-Bridge, where "0" stands for OFF state wile "1" stands for ON state.

Therefore, the switches S_1 and S_3 can be used as switching variables to represent the switching status of, respectively, the leg A and B of the H-Bridge converter of Fig. 3.2.

Hence, the instantaneous switching model is given by [81, 104, 105]:

$$v_{aN,ijk} = S_1 v_{dc,ijk} \tag{3.1}$$

$$v_{bN,ijk} = S_3 v_{dc,ijk} \tag{3.2}$$

where $v_{dc,ijk}$ is the DC-link voltage of submodule j,k. Therefore, from eq. (3.1) and (3.2), the relationship between the DC- and AC-side voltage is derived as:

$$v_{ab,ijk} = v_{aN,ijk} - v_{aN,ijk} = (S_1 - S_3)\, v_{dc,ijk} \tag{3.3}$$

Similarly, for the DC and AC currents it holds:

$$i_{dc,ijk} = (S_1 - S_3)\, i_{ac,ijk} \tag{3.4}$$

Defining the switching function of the j,k-*th* submodule at the input side i as:

$$S_{ijk} = (S_1 - S_3) \tag{3.5}$$

where $S \in \{-1, 0, 1\}$, eq. (3.3) and (3.4) can be rewritten as:

$$v_{ab,ijk} = S_{ijk}\, v_{dc,ijk} \tag{3.6}$$

$$i_{dc,ijk} = S_{ijk}\, i_{ac,ijk} \tag{3.7}$$

Equations (3.6) and (3.7) describes the switching model of the H-Bridge submodule j,k. Based on that, the switching model of the total output voltage generated by each phase of the CHB converter can be derived as:

$$v_{jO} = \sum_{k=1}^{N} v_{ab,ijk} = \sum_{k=1}^{N} S_{ijk}\, v_{dc,ijk} \tag{3.8}$$

Assuming equal and constant DC-link voltages among submodules and phases (i.e. $v_{dc,ijk}(t) = v_{dc,i}(t) = v_{dc,i}, \quad \forall j,k$), the instantaneous switching model of the three-phase output voltages generated by the CHB can be derived as:

$$\begin{cases} v_{aO}(t) = \sum_{k=1}^{N} v_{ab,iak}(t) = \sum_{k=1}^{N} S_{iak}(t)\, v_{dc,iak}(t) = v_{dc,i} \sum_{k=1}^{N} S_{iak}(t) \\ v_{bO}(t) = \sum_{k=1}^{N} v_{ab,ibk}(t) = \sum_{k=1}^{N} S_{ibk}(t)\, v_{dc,ibk}(t) = v_{dc,i} \sum_{k=1}^{N} S_{ibk}(t) \\ v_{cO}(t) = \sum_{k=1}^{N} v_{ab,ick}(t) = \sum_{k=1}^{N} S_{ick}(t)\, v_{dc,ick}(t) = v_{dc,i} \sum_{k=1}^{N} S_{ick}(t) \end{cases} \tag{3.9}$$

To develop the average model of the CHB converter, the switching function of each submodule is averaged over one switching period T_{sw} as [103–105]:

$$\bar{v}_{ab,ijk} = \frac{1}{T_{sw}} \int_{t}^{t+T_{sw}} S_{ijk}(\tau)\, v_{dc,ijk}(\tau)\, d\tau \tag{3.10}$$

$$\bar{i}_{dc,ijk} = \frac{1}{T_{sw}} \int_{t}^{t+T_{sw}} S_{ijk}(\tau)\, i_{ac,ijk}(\tau)\, d\tau \tag{3.11}$$

where the accent mark $\bar{x}$ indicates the averaged value of the variable x of the switching period, while the variable τ is introduced to discern the time variable indicated as t. Assuming the DC voltages and output AC currents to be constant in one switching cycle [104], equations (3.10) and (3.11) can be averaged as follows:

$$\begin{aligned}\bar{v}_{ab,ijk} &= \frac{1}{T_{sw}} v_{dc,ijk} \int_{t}^{t+T_{sw}} S_{ijk}(\tau)\, d\tau = v_{dc,ijk} \frac{1}{T_{sw}} \int_{t}^{t+T_{sw}} \left(S_{1,ijk}(\tau) - S_{3,ijk}(\tau)\right)\, d\tau = \\ &= v_{dc,ijk}\left(d_{1,ijk} - d_{3,ijk}\right)\end{aligned} \tag{3.12}$$

$$\begin{aligned}\bar{i}_{dc,ijk} &= \frac{1}{T_{sw}} i_{ac,ijk} \int_{t}^{t+T_{sw}} S_{ijk}(\tau)\, d\tau = i_{ac,ijk} \frac{1}{T_{sw}} \int_{t}^{t+T_{sw}} \left(S_{1,ijk}(\tau) - S_{3,ijk}(\tau)\right)\, d\tau = \\ &= i_{ac,ijk}\left(d_{1,ijk} - d_{3,ijk}\right)\end{aligned} \tag{3.13}$$

where $d_{1,ijk}$ and $d_{3,ijk}$ are the duty cycle of, respectively, the leg A and B of the submodule j,k. In a single-phase H-Bridge converter, the relation between the duty cycle of each leg and the modulation index is:

$$m_{ijk} = d_{1,ijk} - d_{3,ijk} \tag{3.14}$$

Therefore, substituting (3.14) in (3.12) and (3.13), the average model of a single H-Bridge submodule is obtained as:

$$\bar{v}_{ab,ijk} = m_{ijk} \cdot v_{dc,ijk} \tag{3.15}$$

$$\bar{i}_{dc,ijk} = m_{ijk} \cdot i_{ac,ijk} \tag{3.16}$$

which holds if the DC voltage $v_{dc,ijk}$ and the AC output current $i_{ac,ijk}$ are constant over one switching cycle, assumption that can be considered reasonably correct in PWM-drive converters, where the switching frequency must be quite higher compared to the

fundamental frequency. From (3.8) and (3.15), the average multilevel output voltage of the j-*th* phase of the CHB becomes then:

$$\bar{v}_{jO} = \sum_{k=1}^{N} \bar{v}_{ab,ijk} = \sum_{k=1}^{N} m_{ijk} \cdot v_{dc,ijk} \tag{3.17}$$

while, with reference to the nomenclature given in Fig. 3.2, the average DC current of the j-*th* phase of the CHB can be expressed as:

$$\bar{i}_{dc,ijk} = m_{ijk} \cdot i_{ij} \tag{3.18}$$

Equations (3.17) and (3.18) represent the average model of the j-*th* phase of the CHB converter given in Fig. 3.2.

From the circuit analysis of the network given in Fig. 3.2, supposing that $R_{f,ia} = R_{f,ib} = R_{f,ic} = R_{f,i}$, $L_{f,ia} = L_{f,ib} = L_{f,ic} = L_{f,i}$, $C_{ijk} = C_i$, $\forall j = a,b,c,\ \forall k = 1,...,N$ and considering the equations (3.17) and (3.18), a general average model in the natural reference frame (i.e. in *abc* coordinates) of a grid-connected CHB featuring N submodules is given by:

$$\begin{cases} \vec{e}_{i,abc} - R_{f,i}\,\vec{i}_{i,abc} - L_{f,i}\,\dfrac{d\vec{i}_{i,abc}}{dt} - \vec{v}_{i,CHB} + \vec{v}_{i,oO} = 0 & \text{(3.19a)} \\ C_i \dfrac{dv_{dc,ijk}}{dt} - m_{ijk}\,i_{ij} + i_{L,ijk} = 0, \quad \forall j = a,b,c,\ \forall k = 1,...,N & \text{(3.19b)} \end{cases}$$

where:

$$\vec{e}_{i,abc} = \begin{bmatrix} e_{ia} \\ e_{ib} \\ e_{ic} \end{bmatrix},\ \vec{i}_{i,abc} = \begin{bmatrix} i_{ia} \\ i_{ib} \\ i_{ic} \end{bmatrix},\quad \vec{v}_{i,CHB} = \begin{bmatrix} \bar{v}_{aO} \\ \bar{v}_{bO} \\ \bar{v}_{cO} \end{bmatrix} = \begin{bmatrix} \sum_{k=1}^{N} m_{iak} \cdot v_{dc,iak} \\ \sum_{k=1}^{N} m_{ibk} \cdot v_{dc,ibk} \\ \sum_{k=1}^{N} m_{ick} \cdot v_{dc,ick} \end{bmatrix},\ \vec{v}_{i,oO} = \begin{bmatrix} v_{ioO} \\ v_{ioO} \\ v_{ioO} \end{bmatrix} \tag{3.20}$$

where, with reference to Fig. 3.2, $i_{L,ijk}$ is the current absorbed by the DC load connected to the DC-bus j,k, which for the SST under consideration will be the current absorbed by the DAB connected to the j,k-*th* submodule. Instead, v_{ioO} is the voltage between the neutral points of the converter and the grid. For the balanced three-phase operation of the converter, it can be assumed to be $v_{ioO} = 0$. A reasonable simplification of the CHB average model given in (3.19) can be done by considering equal DC-link voltages, i.e.:

$$v_{dc,ijk} = v_{dc,i}, \quad \forall j = a,b,c,\ \forall k = 1,...,N \tag{3.21}$$

Considering also equal DC loads among the three phases for each string of submodules (which means in symmetric three-phase load for each string), i.e.:

$$i_{L,iak} = i_{L,ibk} = i_{L,ick} = i_{L,ik}, \quad \forall k = 1, ..., N \tag{3.22}$$

Substituting eq. (3.21) and (3.22) in (3.19) leads to:

$$\begin{cases} \vec{e}_{i,abc} - R_{f,i}\,\vec{i}_{i,abc} - L_{f,i}\,\dfrac{d\vec{i}_{i,abc}}{dt} - v_{dc,i}\,\vec{M}_{i,abc} = 0 & \text{(3.23a)} \\ 3C_i\dfrac{dv_{dc,i}}{dt} - \vec{m}^T_{i,abc}\,\vec{i}_{i,abc,k} + 3i_{L,ik} = 0, \quad \forall k = 1, ..., N & \text{(3.23b)} \end{cases}$$

where:

$$\vec{M}_{i,abc} = \begin{bmatrix} \sum_{k=1}^{N} m_{iak} \\ \sum_{k=1}^{N} m_{ibk} \\ \sum_{k=1}^{N} m_{ick} \end{bmatrix}, \; \vec{m}_{i,abc,k} = \begin{bmatrix} m_{iak} \\ m_{ibk} \\ m_{ick} \end{bmatrix}, \; \forall k = 1, ..., N \tag{3.24}$$

Both the CHB average model descriptions, i.e. eq. (3.19) and (3.23), holds also for the MV DC-AC inverters stage, in which the subscript i becomes o being the inverter on the output side of the SST.

3.1.2 CHB Average Model Validation

The CHB *abc*-frame average model developed in the previous Section is validated through time-domain simulations in MATLAB/Simulink and PLECS. To do so, the grid-connected CHB converter circuit given in Fig. 3.2 is implemented and then simulated. The CHB converter is operated in AFE rectifier mode thourgh a dedicated control system, which will be introduced in next Sections. Two different case-studies were considered to verify the effectiveness of the average models, i.e. a balanced DC-load scenario in which equals resistors are connected to the available 3xN DC-links and an unbalanced case where resistors of different values are connected. To deal with both balanced and unbalanced operation, the average model implemented in simulation is the general one represented in eq. (3.19). Table 3.2 reports the simulation parameters. In case of unbalanced operation, resistance of the loads connected to the DC-links varies from the rated valued given in 3.2 by a few percent. Fig. 3.3 shows the simulation results in case of balanced DC loads. The phase-to-ground converter voltages, the grid currents and the phase A DC-link voltages are plotted, for both the switching and average models. As can be observed, the averaged

Table 3.2: Simulation parameters for the validation of the CHB average model.

Quantity	Symbol	Value
Grid RMS voltage	E_i	1.9 kV
Grid frequency	f_g	50 Hz
Grid filter resistance	$R_{f,i}$	0.5 Ω
Grid filter inductance	$L_{f,i}$	7 mH
N° of submodules	N	4
DC-link capacitance	C_i	8 mF
DC-link rated voltage	$V_{dc,i}$	756 V
DC-link rated load	$R_{dc,i}$	14.84 Ω

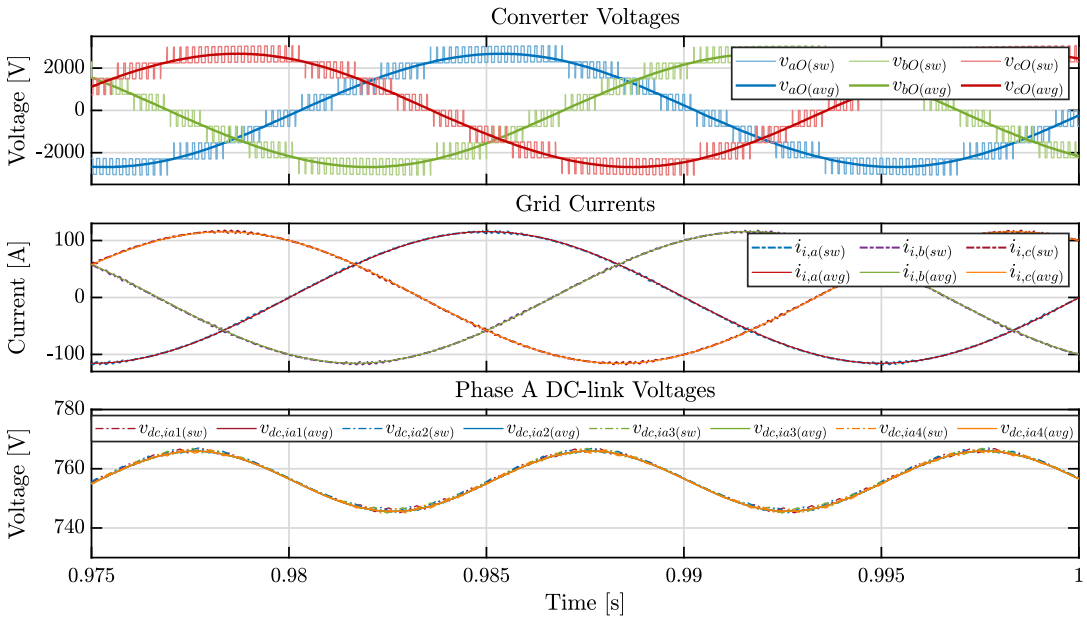


Figure 3.3: Comparison between the switching and the average model simulation results of a grid-connected CHB converter working as AFE rectifier during balanced operation.

waveform contains only low-frequency spectrum (i.e. the fundamental component and low-frequency harmonics). Basically, the average operator results in a low-pass filter action whose cut-off frequency is half of the converter switching frequency [103, 106]. Fig.

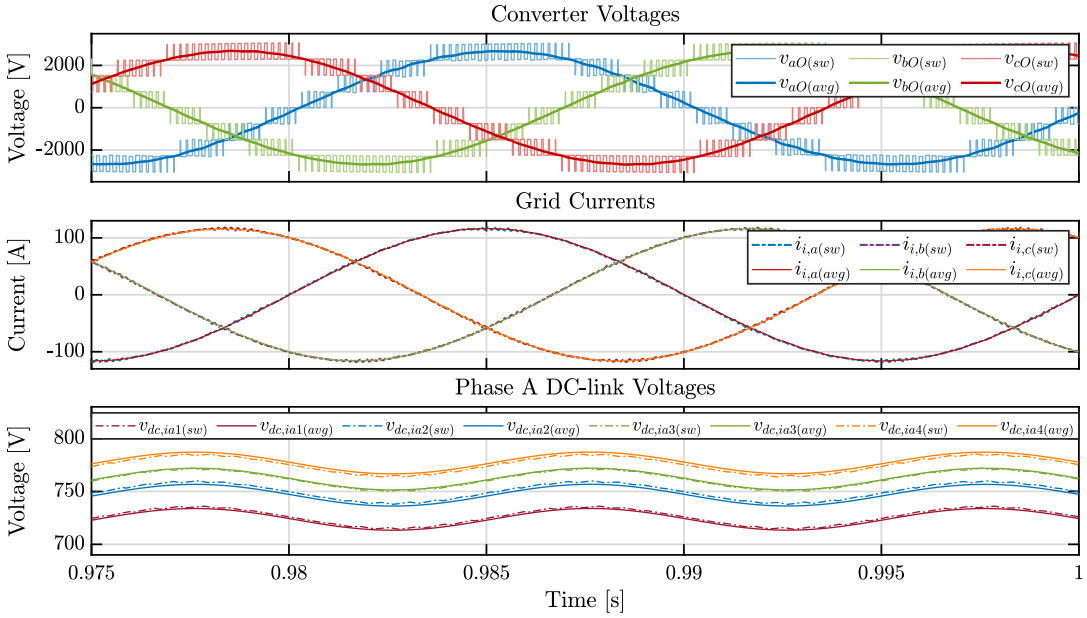


Figure 3.4: Comparison between the switching and the average model simulation results of a grid-connected CHB converter working as AFE rectifier during unbalanced operation.

3.4 demonstrates how the general CHB average model developed in this chapter is effective and accurate also for unbalanced operation of the converter. As can be observed from the figure, in case of unbalanced DC loads, the DC-link voltages drifts from the rated valued $V_{dc,i}$ defined in Table 3.2. The new steady-state average DC-link voltage is defined based on the operating point defined by each DC load. As it is clear from the image, the average model can correctly predict each DC-link voltage based on the corresponding DC load.

3.1.3 CHB Average and Small-Signal Model in *dq0* Reference Frame

Being the SST control system developed in the rotating *dq* reference frame, the average model represented by eq. (3.23) need to be transformed in the synchronous reference frame. In this work, the amplitude-invariant Park's transformation matrix is used to generate the rotating reference frame, i.e.:

$$\boldsymbol{T} = \frac{2}{3}\begin{bmatrix} \cos(\omega t) & \cos\left(\omega t - \frac{2\pi}{3}\right) & \cos\left(\omega t + \frac{2\pi}{3}\right) \\ -\sin(\omega t) & -\sin\left(\omega t - \frac{2\pi}{3}\right) & -\sin\left(\omega t + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{3.25}$$

where ω is the angular frequency at which the dq-frame rotates (i.e. normally at the grid angular frequency ω_g) and the bold-face letters indicates, from now on, matrices. Multiplying both sides of the equations (3.23a) and (3.23b) by Park's transformation matrix the following is obtained:

$$\begin{cases} \dfrac{d}{dt}\begin{bmatrix} i_{i,d} \\ i_{i,q} \\ i_{i,0} \end{bmatrix} = \dfrac{1}{L_{f,i}}\begin{bmatrix} e_{i,d} \\ e_{i,q} \\ e_{i,0} \end{bmatrix} - \dfrac{v_{dc,i}}{L_{f,i}}\begin{bmatrix} M_{i,d} \\ M_{i,q} \\ M_{i,0} \end{bmatrix} - \begin{bmatrix} \dfrac{R_{f,i}}{L_{f,i}} & -\omega_g & 0 \\ \omega_g & \dfrac{R_{f,i}}{L_{f,i}} & 0 \\ 0 & 0 & R_{f,i} \end{bmatrix}\begin{bmatrix} i_{i,d} \\ i_{i,q} \\ i_{i,0} \end{bmatrix} & (3.26a) \\ \dfrac{d}{dt}v_{dc,i} = \dfrac{1}{2C_i}\begin{bmatrix} m_{i,dk} & m_{i,qk} & m_{i,0k} \end{bmatrix}\begin{bmatrix} i_{i,d} \\ i_{i,q} \\ 2i_{i,0} \end{bmatrix} - \dfrac{i_{L,ik}}{C_i}, \quad \forall k = 1, ..., N & (3.26b) \end{cases}$$

Assuming the balanced and symmetric operation of both the grid and CHB converter, the *0*-components in (3.26) can be neglected and, moreover, the dq modulation signal applied to each CHB submodule string can be considered identical $\forall k$, i.e.:

$$m_{i,dk} = m_{i,d}, \;\; m_{i,qk} = m_{i,q}, \quad \forall k = 1, ..., N \tag{3.27}$$

$$\Rightarrow M_{i,d} = \sum_{k=1}^{N} m_{i,dk} = N m_{i,d}, \;\; M_{i,q} = \sum_{k=1}^{N} m_{i,qk} = N m_{i,q} \tag{3.28}$$

Therefore, under the assumptions made here, a final general dq average model of a grid-connected CHB converter in the compact form is given by:

$$\begin{cases} \dfrac{d}{dt}\vec{i}_{i,dq} = \dfrac{1}{L_{f,i}}\vec{e}_{i,dq} - \dfrac{1}{L_{f,i}} N v_{dc,i}\vec{m}_{i,dq} - \begin{bmatrix} \dfrac{R_{f,i}}{L_{f,i}} & -\omega_g \\ \omega_g & \dfrac{R_{f,i}}{L_{f,i}} \end{bmatrix}\vec{i}_{i,dq} & (3.29a) \\ \dfrac{d}{dt}v_{dc,i} = \dfrac{1}{2C_i}\vec{m}_{i,dq}^{T}\vec{i}_{i,dq} - \dfrac{i_{L,ik}}{C_i}, \quad \forall k = 1, ..., N & (3.29b) \end{cases}$$

where, for simplicity, the DC load current can be expressed through a generic resistor that models the power absorbed by the k-*th* DC load:

$$i_{L,ik} = v_{dc,i}/R_{dc,ik}, \quad \forall k = 1, ..., N \tag{3.30}$$

Note that the system (3.29) is non-linear due to the cross-product between the modulation indexes and DC-link voltage in (3.29a) and grid currents in (3.29b), since both terms are

time-dependet functions. To design the control system based on the frequency domain representation of the converter, the small-signal transfer functions need to be derived. The *dq* small-signal model the grid-connected CHB is derived by perturbing and linearizing the large-signal *dq* average model given in (3.29) around a steady-state (quiescent) operating point [103, 106]. A steady-state operating point can be defined solving the system (3.29) considering the time derivative null (i.e. $d/dt = 0$). To do this, owing to a perfect synchronization with the grid using the amplitude-invariant Park's transformation matrix given in (3.25), and assuming that the grid is balanced and symmetric, i.e.:

$$\begin{cases} e_{ia} = \sqrt{2}E_i \cos(\omega t) \\ e_{ib} = \sqrt{2}E_i \cos\left(\omega t - \dfrac{2\pi}{3}\right) \\ e_{ic} = \sqrt{2}E_i \cos\left(\omega t + \dfrac{2\pi}{3}\right) \end{cases} \tag{3.31}$$

the following holds [107]:

$$e_{i,d}(t) = E_{i,d}, \;\; e_{i,q}(t) = E_{i,q} = 0 \tag{3.32}$$

where

$$E_{i,d} = \sqrt{2}E_i \tag{3.33}$$

the capital letters in (3.32) indicates the steady-state values. Considering for simplicity the AFE rectifier operating mode of the CHB, i.e. unity power factor, the steady-state q-component of the grid current will also be null, i.e.:

$$I_{i,q} = 0 \tag{3.34}$$

Based on the assumptions made in (3.32) and (3.34), the steady-state values of $i_{i,d}(t)$, $m_{i,d}(t)$ and $m_{i,q}(t)$ can be calculated solving (3.29) in quiescent conditions, resulting

in [108]:

$$\begin{cases} I_{i,d} = \dfrac{E_{i,d} - \sqrt{E_{i,d}^2 - \dfrac{8NR_{f,i}V_{dc,i}^2}{R_{dc,i}}}}{2R_{f,i}} & \text{(3.35a)} \\ M_{i,d} = \dfrac{4R_{f,i}V_{dc,i}}{R_{dc,i}\left(E_{i,d} - \sqrt{E_{i,d}^2 - \dfrac{8NR_{f,i}V_{dc,i}^2}{R_{dc,i}}}\right)} & \text{(3.35b)} \\ M_{i,q} = -\dfrac{\omega_g L_{f,i}\left(E_{i,d} - \sqrt{E_{i,d}^2 - \dfrac{8NR_{f,i}V_{dc,i}^2}{R_{dc,i}}}\right)}{2NR_{f,i}V_{dc,i}} & \text{(3.35c)} \end{cases}$$

where, when solving the system (3.29), the DC load currents defined in (3.30) are assumed all equal (i.e. $R_{dc,ik} = R_{dc,i}, \quad \forall k = 1, ..., N$). Once the steady-state operating point is defined, the small-signal perturbations (from this point on denoted with a "$\sim$" symbol over the variables) around this equilibrium point are defined as:

$$e_{i,d} = E_{i,d} + \tilde{e}_{i,d} \tag{3.36}$$

$$e_{i,q} = E_{i,q} + \tilde{e}_{i,q} = \tilde{e}_{i,q} \tag{3.37}$$

$$i_{i,d} = I_{i,d} + \tilde{i}_{i,d} \tag{3.38}$$

$$i_{i,q} = I_{i,q} + \tilde{i}_{i,q} = \tilde{i}_{i,q} \tag{3.39}$$

$$m_{i,d} = M_{i,d} + \tilde{m}_{i,d} \tag{3.40}$$

$$m_{i,q} = M_{i,q} + \tilde{m}_{i,q} \tag{3.41}$$

$$v_{dc,i} = V_{dc,i} + \tilde{v}_{dc,i} \tag{3.42}$$

The average model (3.29) is then perturbed and linearized as described in [103] by plugging (3.36)–(3.42) into (3.29) and neglecting the second-order terms. Therefore, the CHB dq small-signal model under AFE rectifier operation is finally obtain:

$$\begin{cases} \dfrac{d}{dt}\vec{\tilde{i}}_{i,dq} = \dfrac{1}{L_{f,i}}\vec{\tilde{e}}_{i,dq} - \dfrac{1}{L_{f,i}}NV_{dc,i}\vec{\tilde{m}}_{i,dq} - \dfrac{1}{L_{f,i}}N\begin{bmatrix} M_{i,d} \\ M_{i,q} \end{bmatrix}\tilde{v}_{dc,i} - \begin{bmatrix} \dfrac{R_{f,i}}{L_{f,i}} & -\omega_g \\ \omega_g & \dfrac{R_{f,i}}{L_{f,i}} \end{bmatrix}\vec{\tilde{i}}_{i,dq} & \text{(3.43a)} \\ \dfrac{d}{dt}\tilde{v}_{dc,i} = \dfrac{1}{2C_i}\begin{bmatrix} I_{i,d} & I_{i,q} \end{bmatrix}\vec{\tilde{m}}_{i,dq} + \dfrac{1}{2C_i}\begin{bmatrix} M_{i,d} & M_{i,q} \end{bmatrix}\vec{\tilde{i}}_{i,dq} - \dfrac{\tilde{v}_{dc,i}}{R_{dc,i}C_i} & \text{(3.43b)} \end{cases}$$

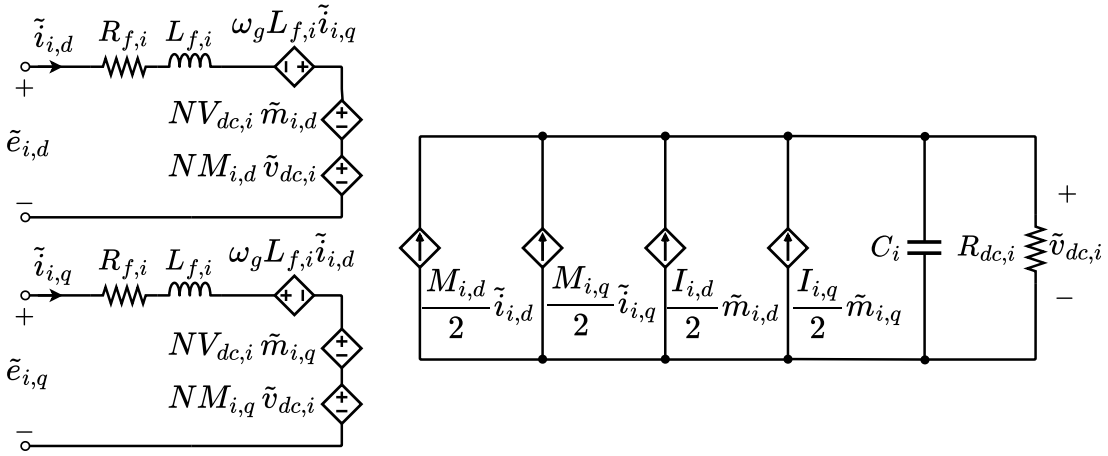


Figure 3.5: Circuit representation of the grid-connected three-phase CHB converter *dq* small-signal model developed in (3.44).

an its expanded form is:

$$\begin{cases} L_{f,i}\dfrac{d\tilde{i}_{i,d}}{dt} = \tilde{e}_{i,d} - R_{f,i}\cdot\tilde{i}_{i,d} + \omega_g L_{f,i}\cdot\tilde{i}_{i,q} - NV_{dc,i}\cdot\tilde{m}_{i,d} - NM_{i,d}\cdot\tilde{v}_{dc,i} & \text{(3.44a)} \\ L_{f,i}\dfrac{d\tilde{i}_{i,q}}{dt} = \tilde{e}_{i,q} - R_{f,i}\cdot\tilde{i}_{i,q} - \omega_g L_{f,i}\cdot\tilde{i}_{i,d} - NV_{dc,i}\cdot\tilde{m}_{i,q} - NM_{i,q}\cdot\tilde{v}_{dc,i} & \text{(3.44b)} \\ C_i\dfrac{d\tilde{v}_{dc,i}}{dt} = \dfrac{1}{2}\left(M_d\tilde{i}_{i,d} + M_q\tilde{i}_{i,q}\right) + \dfrac{1}{2}\left(I_d\tilde{m}_{i,d} + I_q\tilde{m}_{i,q}\right) - \dfrac{\tilde{v}_{dc,i}}{R_{dc,i}} & \text{(3.44c)} \end{cases}$$

Based on (3.44), the circuit representation of the CHB *dq* small-signal model is shown in Fig. 3.5. The CHB AFE rectifier *dq* small-signal model represented in (3.44) holds also for the CHB inverter, for which the variables are marked with the subscript *o* instead of *i*.

3.2 DC-DC Isolation Stage Modeling

The development of a closed-loop control strategy for the DC-DC isolation stage of the SST investigated in this thesis, i.e. the DAB converter, is made, also in this case, by means of the small-signal average model of the converter. To this extent, there are various approaches to modeling the DAB converter. A common classification categorizes them as reduced-,full-order models and discrete-time models [97, 109]. In this work, except for the discrete-time one, both reduced- and full-order models are evaluated. The main

distinction among them is the modeling of HFT dynamics. This is because the reduced-order models completely neglect the dynamics of the HFT current i_t, while full-order models preserve it. In the next, a generalized full-order and a simplified reduced-order average models are explored and compared in time-domain simulations. After choosing the best one, the small-signal model of the DAB converter is finally derived.

3.2.1 Generalized Average Model of DAB Converter

The well known state-space averaging and circuit averaging techniques presented in [103] are not suitable for modeling the HF dynamics of the DAB converter. This is because these methods assume negligible voltage and current changes (small ripple assumption) during one switching period, but in case of the DAB the HFT current changes significantly during a full commutation period. This is true also for other DC-DC converter topologies (such as SRC) that transfer energy through AC waveforms. Indeed, small-signal models based on state-space equations are widely used for PWM DC-DC converters because the switching ripples on inductor currents and capacitor voltages are (or, at least, expected to be) small. To deal with such problem, a more general approach which is called Generalized State-Space Averaging method (GSSA) is proposed in [97] and [110]. This method approximates state variables by a Fourier series expansion with time-dependent coefficients (while, in the standard state-space averaging method the basic assumption of negligible voltage and current changes during one switching period implies that the DC component of a Fourier expansion is the predominant term over the full harmonic content). This averaging method is based on the representation of a signal $x(\tau)$ on the interval $\tau \in [t-T, t]$ by the Fourier series [97, 109]:

$$x(\tau) = \sum_{-\infty}^{\infty} \langle x \rangle_k(t) e^{jk\omega_{sd}\tau} \tag{3.45}$$

where $\omega_{sd} = 2\pi f_{sd}$ in which f_{sd} is the DAB switching frequency and the complex number $\langle x \rangle_k(t)$ is the time-dependent k-*th* Fourier coefficient. The model accuracy depends on how many Fourier coefficients are considered during the series computation of the signal. The conventional state-space, as said previously, is a special case of the generalized state-space in which only the DC components are considered, i.e. only the coefficient $k = 0$ are calculated. To include the fundamental AC components of the DAB HFT current i_t,

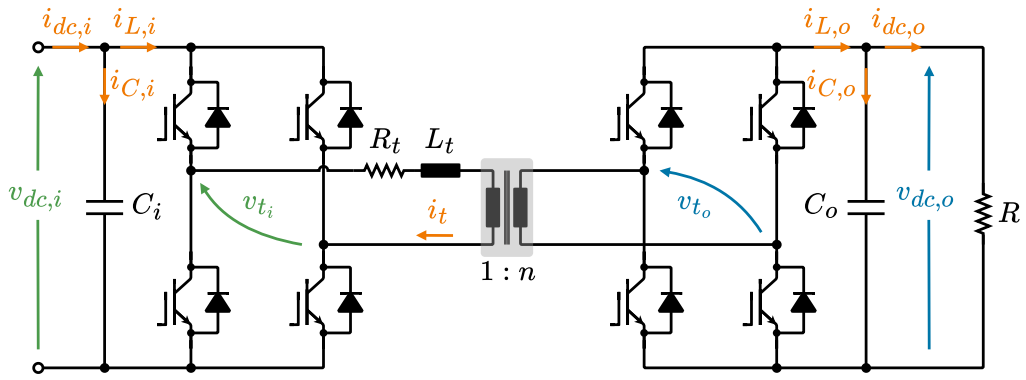


Figure 3.6: Dual Active Bridge (DAB) schematic circuit.

the Fourier expression (3.45) must be extended so as to at least include the coefficients $k = \pm 1$. Including more complex coefficient will result in higher model accuracy but at the cost of higher complexity. Therefore, a trade-off between the model accuracy and complexity is usually done.

Considering the DAB circuit schematic represented in Fig. 3.6 and assuming, for simplicity, that the transformer turns ratio is $n = 1$ and the employed modulation technique is the PS square wave modulation, the following state equations can be written:

$$\begin{cases} \dfrac{d}{dt} i_t(\tau) = -\dfrac{R_t}{L_t} i_t(\tau) + \dfrac{s_1(\tau)}{L_t} v_{dc,i}(\tau) - \dfrac{s_2(\tau)}{L_t} v_{dc,o}(\tau) & \text{(3.46a)} \\ \dfrac{d}{dt} v_{dc,o}(\tau) = -\dfrac{1}{RC_o} v_{dc,o}(\tau) + \dfrac{s_2(\tau)}{L_t} i_t(\tau) & \text{(3.46b)} \end{cases}$$

Being the modeling procedure intricate, it will be omitted here. The full explanation can be found in [97]. The final generalized state-space average model of the DAB converter, considering $k = \{0, \pm 1\}$, is given by [97]:

$$\frac{d}{dt} \begin{bmatrix} v_{dc,o(0)} \\ i_{t(1R)} \\ i_{t(1I)} \end{bmatrix} = \begin{bmatrix} -\dfrac{1}{RC_o} & -\dfrac{4\sin(d\pi)}{\pi C_o} & -\dfrac{4\cos(d\pi)}{\pi C_o} \\ -\dfrac{2\sin(d\pi)}{\pi L_t} & -\dfrac{R_t}{L_t} & \omega_{sd} \\ -\dfrac{2\cos(d\pi)}{\pi L_t} & -\omega_{sd} & -\dfrac{R_t}{L_t} \end{bmatrix} \cdot \begin{bmatrix} v_{dc,o(0)} \\ i_{t(1R)} \\ i_{t(1I)} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ -\dfrac{2}{\pi L_t} \end{bmatrix} \cdot v_{dc,i} \tag{3.47}$$

where the subscripts 0 and 1 denotes, respectively, the DC and fundamental component, whereas the subscripts R and I mean the real and imaginary parts of the complex coefficient and d is the phase shift ratio as introduced in Section 2.3.

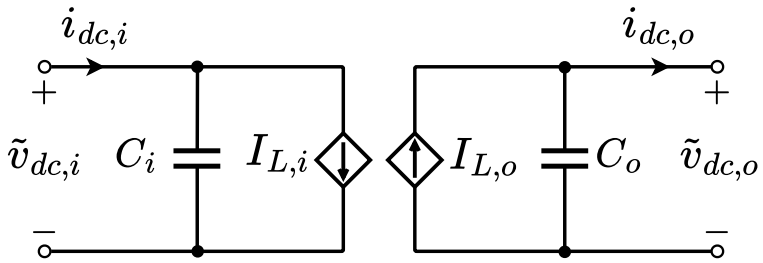


Figure 3.7: DAB large-signal reduced-order average model [109, 111].

3.2.2 Simplified First Order Average Model of DAB Converter

The reduced-order average model of the DAB, also named simplified average model, is based on the average power equation of the converter, already introduced in Section 2.3.2 as (2.16) and here reported again with reference to Fig. 3.6:

$$P_{dab} = \frac{V_{dc,i} V_{dc,o}}{2 n f_{sd} L_t} d\,(1 - |d|) \tag{3.48}$$

Equation (3.48) simply ignores the HFT dynamics (being calculated as average equation over one switching cycle T_{sd}) and it can be used to describe the characteristics of the average input and output DAB quantities [109]. Indeed, from (3.48) and considering $P_{dab} = P_{dab,in} = V_{dc,i} \cdot I_{L,i}$, the DAB average input current (over one switching cycle $T_{sd} = 1/f_{sd}$) when the PS modulation technique is employed is:

$$I_{L,i} = \frac{V_{dc,o}}{2 n f_{sd} L_t} d\,(1 - |d|) \tag{3.49}$$

while, supposing a loss-less conversion, the average output current is calculated from (3.48) considering $P_{dab} = P_{dab,out} = V_{dc,o} \cdot I_{L,o}$ as:

$$I_{L,o} = \frac{V_{dc,i}}{2 n f_{sd} L_t} d\,(1 - |d|) \tag{3.50}$$

The DAB large-signal reduced-order average model represented by equation (3.49) and (3.50) is represented in Fig. 3.7.

3.2.3 DAB Average Model Validation and Discussion

Both the full-order GSSA and the reduced-order average model presented before are validate and compared in terms of accuracy through time-domain simulation in MATLAB/Simulink and PLECS. The DAB converter parameters used for the simulations are

Table 3.3: DAB simulation parameters used for the average models comparison.

Quantity	Symbol	Value
Input DC voltage	$V_{dc,i}$	756 V
HFT turns ration	n	1
Load resistance	R	14.84 Ω
Input capacitance	C_i	8 mF
Output capacitance	C_o	8 mF
Leakage inductance	L_t	44.5 μH
Leakage resistance	R_t	0.4 mΩ
Rated Power	P_{dab}^{nom}	48 kW
Rated phase shift angle	φ^{nom}	$\pi/10$ rad
Switching frequency	f_{sd}	12 kHz

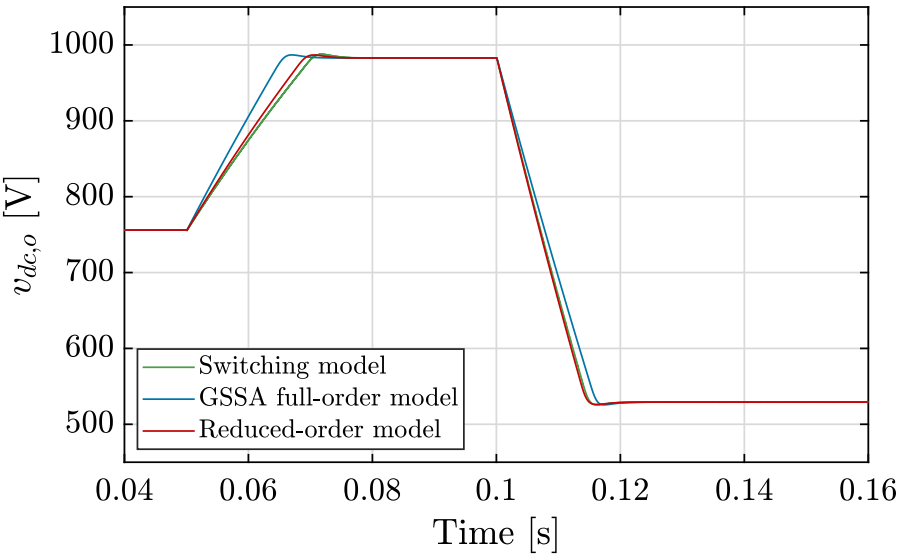


Figure 3.8: Time-response comparison of the full-order and reduced-order DAB models.

listed in Table 3.3. Fig. 3.8 shows the simulation results for the switching model, full-order and reduced-order average models in presence of a step-variation of the phase shift angle φ, which cause a step-variation in the output voltage $v_{dc,o}$. As can be observed,

both average models correctly predict the output voltage variation, but the reduced-order seems to be more accurate. Moreover, as pointed out in [109], even if this is not the case, the GSSA model sometimes may result in steady-state error if high order components of the HFT current are ignored. Being the reduced-order model complexity pretty low while still being pretty accurate, in this work it is chosen as modeling approach for the DAB converter. Furthermore, as it will be shown later in the next section, by using the reduced-order it is very simple and straightforward to derive analytically the control-to-output and input-to-output transfer function of the DAB converter as functions of the system parameters, thus highlighting how they affect the converter dynamics. In case of the GSSA model, instead, the analytical expression of transfer functions may be difficult to derive because of high complexity of the model, therefore usually these transfer function are expressed numerically.

3.2.4 Small-Signal Model of DAB Converter

As already described in Section 3.1.3, the small-signal model of the DAB converter is derived by perturbing and linearizing the average model. For the full-order GSSA model, perturbation are introduced in the input and control state-space variables as:

$$v_{dc,i}(t) = V_{dc,i}(t) + \tilde{v}_{dc,i}(t) \tag{3.51}$$

$$v_{dc,o(0)}(t) = V_{dc,o(0)}(t) + \tilde{v}_{dc,o(0)}(t) \tag{3.52}$$

$$i_{t(1R)}(t) = I_{t(1R)}(t) + \tilde{i}_{t(1R)}(t) \tag{3.53}$$

$$i_{t(1I)}(t) = I_{t(1I)}(t) + \tilde{i}_{t(1I)}(t) \tag{3.54}$$

$$d(t) = D + \tilde{d} \tag{3.55}$$

Perturbing and linearizing the system (3.47) through (3.51)–(3.55), the following full-order small-signal model for the DAB converter is obtained:

$$\begin{cases} \dfrac{d}{dt}\vec{x} = \mathbf{A}\vec{x} + \mathbf{B}\vec{u} & \text{(3.56a)} \\ \vec{y} = \mathbf{C}\vec{x} & \text{(3.56b)} \end{cases}$$

$$\Rightarrow \frac{d}{dt}\begin{bmatrix}\tilde{v}_{dc,o(0)}\\ \tilde{i}_{t(1R)}\\ \tilde{i}_{t(1I)}\end{bmatrix} = + \begin{bmatrix} -\frac{1}{RC_o} & -\frac{4\sin(D\pi)}{\pi C_o} & -\frac{4\cos(D\pi)}{\pi C_o}\\ -\frac{2\sin(D\pi)}{\pi L_t} & -\frac{R_t}{L_t} & \omega_{sd}\\ -\frac{2\cos(D\pi)}{\pi L_t} & -\omega_{sd} & -\frac{R_t}{L_t}\end{bmatrix}\cdot\begin{bmatrix}\tilde{v}_{dc,o(0)}\\ \tilde{i}_{t(1R)}\\ \tilde{i}_{t(1I)}\end{bmatrix} + $$
$$+ \begin{bmatrix}\frac{4}{C_o}(I_{t(1I)}\sin(D\pi) - I_{t(1R)}\cos(D\pi)) & 0\\ 2\frac{V_{dc,o(0)}}{L_t}\cos(D\pi) & 0\\ -2\frac{V_{dc,o(0)}}{L_t}\sin(D\pi) & -\frac{2}{\pi L_t}\end{bmatrix}\cdot\begin{bmatrix}\tilde{d}\\ \tilde{v}_{dc,i}\end{bmatrix} \tag{3.57}$$

$$\Rightarrow \begin{bmatrix}\tilde{y}_1\\ \tilde{y}_2\\ \tilde{y}_3\end{bmatrix} = \begin{bmatrix}1 & 0 & 0\\ 0 & 1 & 0\\ 0 & 0 & 1\end{bmatrix}\cdot\begin{bmatrix}\tilde{v}_{dc,o(0)}\\ \tilde{i}_{t(1R)}\\ \tilde{i}_{t(1I)}\end{bmatrix} \tag{3.58}$$

The control-to-output and input-to-output transfer functions can be then dervied solving the following equation:

$$\mathbf{G}(s) = \mathbf{C}(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B} \tag{3.59}$$

where s is the Laplace operator and $\mathbf{I}$ is the identity matrix.

For the derivation of the reduced-order small-signal DAB model, perturbations (3.51), (3.52) and (3.55) are introduced into DAB average current equations (3.49) and (3.50), along with these other two:

$$i_{L,i}(t) = I_{L,i}(t) + \tilde{i}_{L,i}(t) \tag{3.60}$$

$$i_{L,o}(t) = I_{L,o(0)}(t) + \tilde{i}_{L,o}(t) \tag{3.61}$$

The resulting reduced-order small-signal model is given by:

$$\begin{cases}\tilde{i}_{L,i} = G_d^{i_i}\tilde{d} + G_{v_o}^{i_i}\tilde{v}_{dc,o} = \dfrac{V_{dc,o}(1-2D)}{2nf_{sd}L_t}\tilde{d} + \dfrac{D(1-2D)}{2nf_{sd}L_t}\tilde{v}_{dc,o} & \text{(3.62a)}\\ \tilde{i}_{L,o} = G_d^{i_o}\tilde{d} + G_{v_i}^{i_o}\tilde{v}_{dc,o} = \dfrac{V_{dc,i}(1-2D)}{2nf_{sd}L_t}\tilde{d} + \dfrac{D(1-2D)}{2nf_{sd}L_t}\tilde{v}_{dc,i} & \text{(3.62b)}\end{cases}$$

where G_u^y denotes the general transfer function from the input variable u to the output variable y. Fig. 3.9 shows the circuit representation of the reduced-order small-signal model developed in (3.62). Transfer functions $G_d^{i_i}$ and $G_d^{i_o}$ are the control-to-output-current transfer functions, while $G_{v_o}^{i_i}$ and $G_{v_i}^{i_o}$ represent the input-to-output transfer functions. As can be seen, these transfer functions show simple expression and they depend

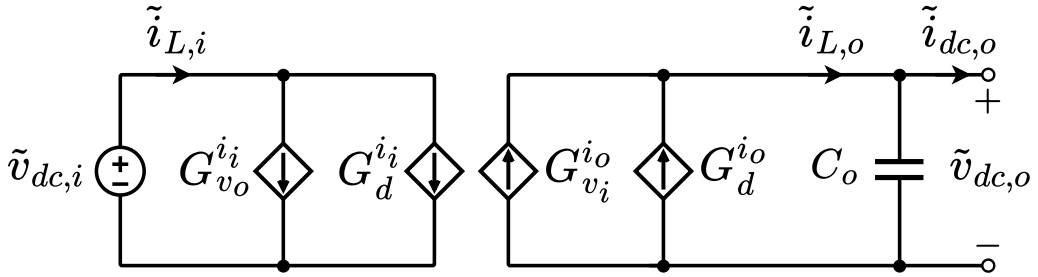


Figure 3.9: DAB reduced-order small-signal model circuit representation.

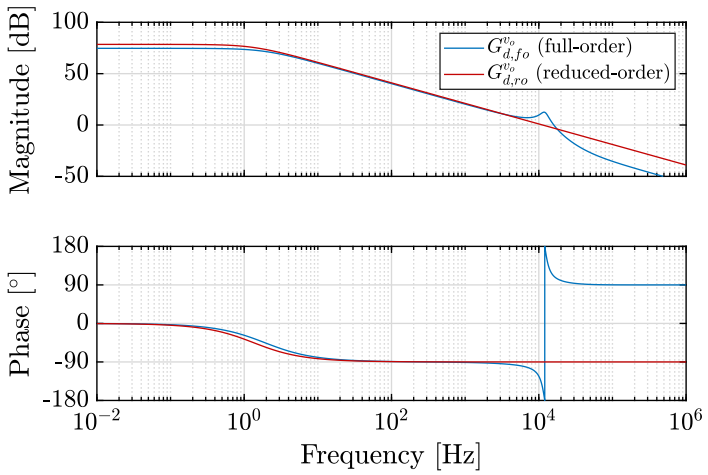


Figure 3.10: Bode diagram of the control-to-output voltage transfer function based on full- and reduced-order models.

on the system parameters $V_{dc,i}$, $V_{dc,o}$, D, f_{sd}, n and L_t. Therefore, is straightforward to evaluate how these parameters influence the dynamic behavior of the DAB converter. Very often, the output voltage $v_{dc,o}$ of the DAB is the variable under control [111]. From the circuit analysis of the network depicted in Fig. 3.9, and supposing a resistive load $R_{dc,o}$ is connected to the output terminals, the control-to-output-voltage transfer function $G_d^{v_o}$ can be easily derived as:

$$G_d^{v_o} = G_d^{i_o} \cdot Z_{rcDAB} = \frac{V_{dc,i}\,(1-2D)}{2nf_{sd}L_t} \frac{R_{dc,o}}{1+sC_oR_{dc,o}} \tag{3.63}$$

Considering the parameters given in Table 3.3, (3.63) results in:

$$G_{d,ro}^{v_o} = \frac{8404}{0.1187s+1} \tag{3.64}$$

While, in case of full-order small-signal model, instead, the transfer function $G_d^{v_o}$ is derived solving numerically equation (3.59) through MATLAB for the dynamic system represented

by equation (3.57) and (3.58). With the parameters given in Table 3.3, the following is obtained:

$$G_{d,fo}^{v_o} = \frac{-9.6 \cdot 10^3 s^2 - 1.7 \cdot 10^8 s + 3.7 \cdot 10^{14}}{s^3 + 1.8 \cdot 10^4 s^2 + 5.8 \cdot 10^9 s + 6.9 \cdot 10^{10}} \tag{3.65}$$

As additional comparison between this two modeling approaches, Fig. 3.10 shows the bode diagram of the control-to-output-voltage transfer function derived in (3.64) through the reduced-order model and in (3.65) via full-order model. As can be noted, they are quite similar, except for the high-frequency resonance between L_t and C_o which is, as expected, only predicted by the full-order model. It is also evident the low-frequency gain mismatch between $G_{d,ro}^{v_o}$ and $G_{d,fo}^{v_o}$, which may bring to steady-state errors because the third and higher order components of i_t are ignored [109]. Considering that the HFT current dynamics are not the focus of this work, and given the simplicity and effectiveness of the reduced-order small-signal model, the latter is chosen as modeling tool of DAB converter for the control design and stability assessments presented in this work.

3.3 SST Control System Design

The SST is intended to provide advanced control functionalities to comply with grid and load requirements, providing a flexible and smart system. Among many control features required, active/reactive power flow control, reactive power compensation, power factor correction, voltage and frequency regulation and power quality improvements are some of them [13, 32, 42, 43, 81]. To accomplish this, the proposed SST control diagram is shown

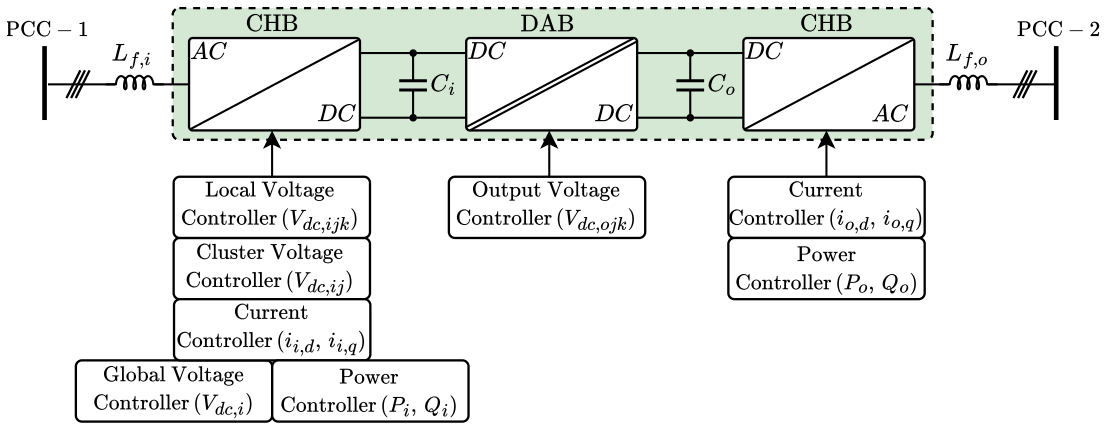


Figure 3.11: SST control diagram

in Fig. 3.11. It shows the required functionalities for each stage of the SST. Based on that, the presented SST control system has two main tasks: it is responsible for the power routing of the converter along with the regulation of both input and output DC-link voltages. For this purpose, the inverter stage regulates the converter power flow through a current controller in the dq synchronous reference frame, while the AFE rectifier manages the voltage balancing of its DC-links, i.e. the input-side DC-link voltages in this work denoted with the label $v_{dc,ijk}$. Each DC-DC isolation stage, i.e. DAB converter, controls the DC-link voltage at its secondary side, namely the output-side DC-link voltages $v_{dc,ojk}$. The synchronization with the grid (in both sides of the SST) is achieved through a Phase-Locked Loop (PLL). While the DAB and Inverter control loops are quite basilar, one major challenge of this configuration is the AFE rectifier control system, that is in charge of the DC-link voltage control and balancing. Imbalance arises from the uneven distribution of the power between modules and between phases due to unbalanced loads, unbalanced operation and modulation and different loss distribution among the devices. For this reason, a three-layer hierarchical control structure is usually needed and in this work adopted for the AFE rectifier, to achieve the voltage balancing of its submodules [42, 112]. It structure is the following:

- Global Voltage Controller (GVC): the outer voltage loop, which provides a setpoint of total active power needed to balance the global AFE DC voltage;
- Cluster Voltage Controller (CVC): required to redistribute the active power defined by the GVC in a weighted way among the three phases, coherently with the per-phase average DC voltage unbalance. This is done, for the star-connected CHB considered in this work, through and injection of a zero-sequence voltage as described in [112];
- Local Voltage Controller (LVC): the inner loop that rebalances the active power drawn by each submodules within the same phase [43, 89, 113];

In the following, the overall control system adopted for each stage of the SST is presented, described and the tuning procedure is reported. The emphasis is more on the AFE rectifier control system, being it the most challenging stage to control in the proposed SST and, also, the one that is more prone to instability issue due to its complex control structure.

3.3.1 AFE Control System

The AFE rectifier control system is shown in Fig. 3.12. As aforementioned, its consists of GVC, CVC, LVC besides the decoupled Current Controller (CC) and the PLL which ensure the correct synchronization with the grid. The target of the AFE rectifier is to enable the active power flow driven by the inverter stage and to control its DC-link voltages. Additionally, it can provide reactive power to the PCC-1. Based on the DC-link voltage deviation from the defined value $V^*_{dc,i}$, the GVC generates the set-point for d-axis current $i^*_{i,d}$. The q-axis current set-point $i^*_{i,q}$ is, instead, generated based on the eventual reactive power requested from the grid. The dq-axis current setpoints $i^*_{i,d}$ and $i^*_{i,d}$ are then compared with the actual values and the resulting errors are sent to the decoupled CCs, whose generate the dq-axis voltage setpoints for the CHB converter. The textitdq-axis modulation indexes $m_{i,d}$ and $m_{i,q}$ are therefore generated. Through the amplitude invariant Park's transformation matrix given in (3.25), the control system is synchronized with the grid by means of the PLL angle θ_g, and the resulting abc-frame modulating waveforms $m_{i,a}$, $m_{i,b}$ and $m_{i,c}$ are finally generated. In case of balanced operation of the DC-link voltages, these modulation indexes are directly supplied to each phase submodule (i.e. $m_{i,jk} = m_{i,j}, \ \forall j,k$). When an unbalanced rises, either among

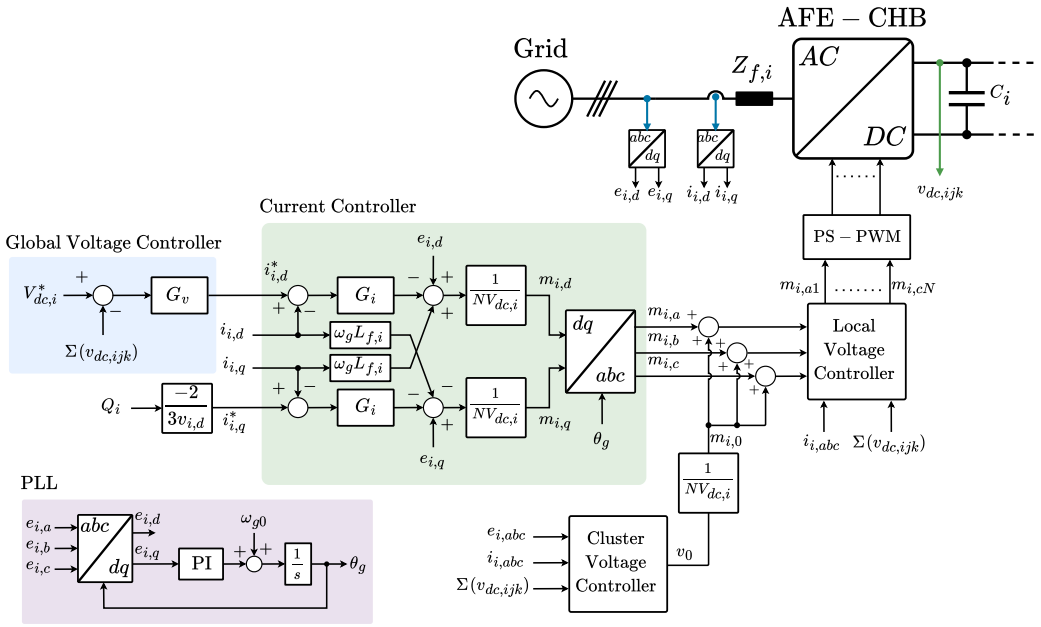


Figure 3.12: Control system strategy of the CHB-based AFE rectifier.

the three-phases or between the submodules of one phase, these modulation signals are changed according to the CVC and LVC. The CVC takes over when the per-phase average DC voltage (i.e. $V_{dc,ij}$) drifts from each other, generating a zero-sequence voltage according to the unbalance amount [112]. This voltage is summed to the voltage set-points for defined for each phase by the GVC and CC. On the other hand, the LVC becomes active when an unbalance among the submodules of one phase occurs. Based on a closed-loop control action, it locally modifies the per-phase modulation index $m_{i,j}$ thus generating individual modulating signals that are applied finally applied to the respective submodules [43, 89, 113]. In the next, the design of the AFE controllers is presented and discussed.

Current Controller (CC)

The current controller is the first to be designed if good decoupling of cascaded controllers is desired. This is because the CC is the inner, and therefore the faster, controller of the SST. It consists of two Proportional Integral (PI) controllers, each one controlling one axis (either d or q) current errors. At the PI output, the decoupling between the dq axis is done and the grid voltage is feedforwarded to enhance the dynamic performances of the system. The PI gains are chosen so as to guarantee a fast current response while providing enough phase margin to keep the system stable [103]. The loop bandwidth is limited by the switching frequency of the CHB converter [114], which in this case is set to be 1.5 kHz. Table 3.4 reports the rated parameters of the SST system. Usually, choosing the CC bandwidth to be one-tenth of the switching frequency is a good compromise between system performances and stability [114]. The CC plant can be calculated by solving the CHB dq average model presented in (3.44) through (3.59). In this case, the equivalent DC load resistance is calculated as the ratio between the square of the DC-link rated voltage $V_{dc,i}$ adn the DAB average power, i.e.:

$$R_{dc,i} = \frac{V_{dc,i}^2}{P_{dab}^{nom}} = \frac{(756)^2}{48 \cdot 10^3} \approx 11.9\,\Omega \tag{3.66}$$

A simpler approach to derive the CC plant transfer function, which avoids to solve system (3.44), is to assume that DC-link voltage variation can be neglected. This means that $V_{dc,i}(t) = V_{dc,i}$. Therefore, the DC-link equation of (3.44) can be neglected, and the CC

Table 3.4: System nominal parameters of the investigated SST architecture.

CHB parameters		
Quantity	Symbol	Value
Grid RMS voltage	E_i, E_o	1.9 kV
Grid frequency	f_g	50 Hz
Grid filter resistance	$R_{f,i}, R_{f,o}$	0.5 Ω
Grid filter inductance	$L_{f,i}, L_{f,o}$	1 mH
N° of CHB submodules	N_i, N_o	4
CHB submodules switching frequency	$f_{sw,i}, f_{sw,o}$	1.5 kHz
Submodule capacitance	C_i, C_o	8 mF
DC-link rated voltage	$V_{dc,i}, V_{dc,o}$	756 V
DAB parameters		
Quantity	Symbol	Value
DAB leakage inductance	L_t	44.5 μH
HFT turns ratio	n	1
DAB rated phase shift ratio	D	0.1
Rated Power	P_{dab}^{nom}	48 kW
DAB switching frequency	f_{sd}	12 kHz

plant for both dq axis is simply the grid filter admittance, i.e.:

$$G_{i_{id}}^{v_{id}} = G_{i_{iq}}^{v_{iq}} = \frac{1}{R_{f,i} + sL_{f,i}} \tag{3.67}$$

The current PI controller is expressed as:

$$G_i(s) = K_{Pi} + \frac{K_{Ii}}{s} \tag{3.68}$$

The current PI controller is tuned considering a bandwidth of 250 Hz and a phase margin of at least 75°. Based on the plant (3.67) and through MATLAB PID tuner app, the

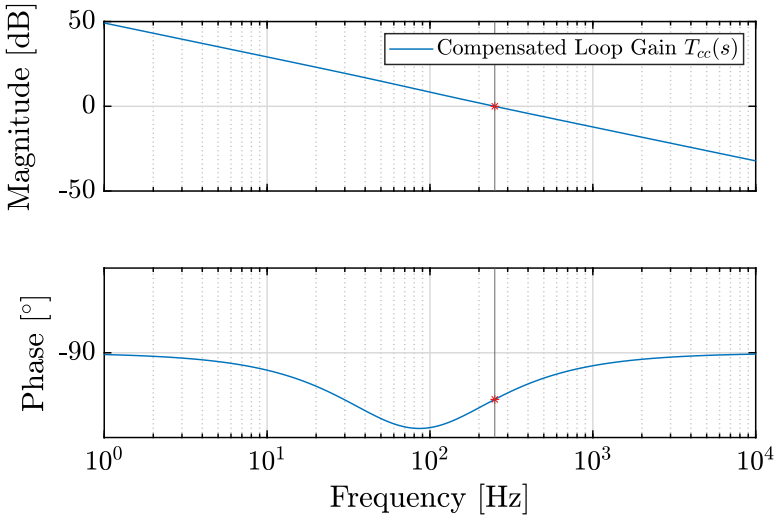


Figure 3.13: Bode diagram of the compensated current loop gain $T_{cc}(s)$.

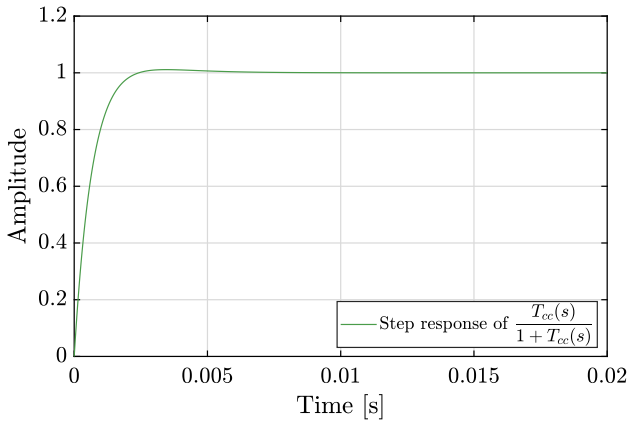


Figure 3.14: Step response of the current control loop.

resulting current PI controller is:

$$G_i(s) = K_{Pi} + \frac{K_{Ii}}{s} = 1.54 + \frac{900}{s} \tag{3.69}$$

Fig. 3.13 presents the bode diagram of the compensated loop gain $T_{cc}(s) = G_i(s) \cdot G_{iid}^{vid}(s)$, clearly showing the crossover frequency and phase margin required. Finally, fig. 3.14 shows the step response of the presented current controller.

Global Voltage Controller (GVC)

The global voltage controller is responsible of the overall DC-link voltage balance. When the input-side DC-link voltages diverge from the set-point $V_{dc,i}$, the CHB must absorb or release active power depending on the unbalance. Therefore, the GVC generates a

d-axis current request. If the DC-link voltages are lower than the defined setpoint, the CHB is controlled to absorb active power from the grid, whilst to release active power thus decreasing the capacitor voltages. There are mainly two approaches to design the GVC: one is based on the average capacitor stored energy, while the other is based on the current balance at each DC-link node. In the first method, the variable under control is the square of the capacitor voltage $v_{dc,i}^2$. This is because the capacitor stored energy is directly proportional to its terminal voltage $v_{dc,i}^2$. The main advantage of this approach is that the system under control becomes completely linear [113]. Based on the procedure presented in [115], the GVC plant is:

$$G_{i_{id}}^{v_{dci}^2} = \frac{\tilde{v}_{dc,i}^2}{\tilde{i}_{i,d}} = \frac{2NR_{dc,i}E_{i,d}}{6 + s3C_iR_{dc,i}} \tag{3.70}$$

The second approach is based on current balance at the DC-link node of each submodule [105]. Considering the third equation of the CHB dq small-signal developed in (3.44), and neglecting for simplicity q-axis terms since they are not involved in net active power balance of the converter, the following equation is obtained:

$$C_i\frac{d\tilde{v}_{dc,i}}{dt} = \frac{1}{2}M_d\tilde{i}_{i,d} + \frac{1}{2}I_d\tilde{m}_{i,d} - \frac{\tilde{v}_{dc,i}}{R_{dc,i}} \tag{3.71}$$

By transforming it into Laplace domain, it leads to:

$$sC_iv_{dc,i} = \frac{1}{2}M_d\tilde{i}_{i,d} + \frac{1}{2}I_d\tilde{m}_{i,d} - \frac{\tilde{v}_{dc,i}}{R_{dc,i}} \tag{3.72}$$

Solving the first equation of (3.44) for $\tilde{m}_{i,d}$ in the Laplace domain yields to:

$$\tilde{m}_{i,d} = \frac{1}{NV_{dc,i}}\left(\tilde{e}_{i,d} - (R_{f,i} + sL_{f,i})\tilde{i}_{i,d} + \omega_gL_{f,i}\cdot\tilde{i}_{i,q} - NM_{i,d}\cdot\tilde{v}_{dc,i}\right) \tag{3.73}$$

Substituting (3.73) into (3.72), neglecting $i_{i,q}$ (owing to perfect decoupled control) and solving for $v_{dc,i}$, the following plant is obtained [105]:

$$G_{i_{id}}^{v_{dci}} = \frac{NV_{dc,i}M_dR_{dc,i} - I_dR_{dc,i}\left(R_{f,i} + sL_{f,i}\right)}{N\left(2V_{dc,i} + I_dM_dR_{dc,i} + s2C_iV_{dc,i}R_{dc,i}\right)} \tag{3.74}$$

The second approach is chosen in this work since simulation results shown better system dynamics. The GVC PI is finally designed based on the plant $G_{i_{id}}^{v_{dci}}$, considering ten-times lower bandwidth with respect to the CC one, to ensure proper decoupling among these

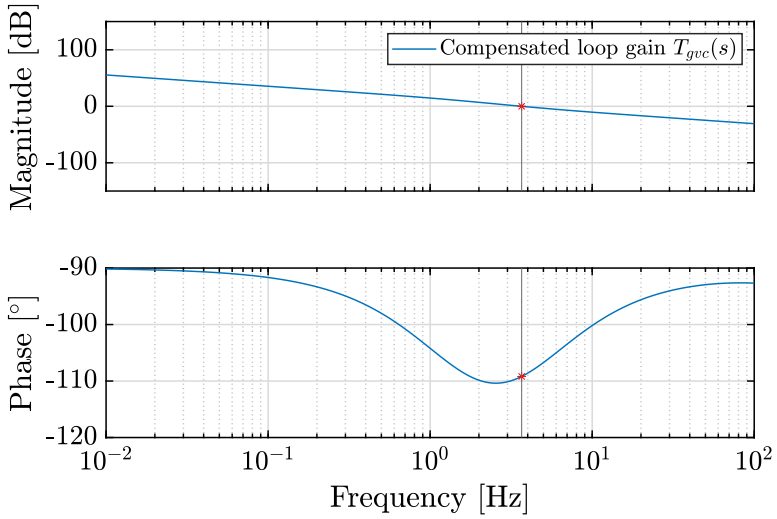


Figure 3.15: Bode diagram of the compensated global voltage loop gain $T_{gvc}(s)$.

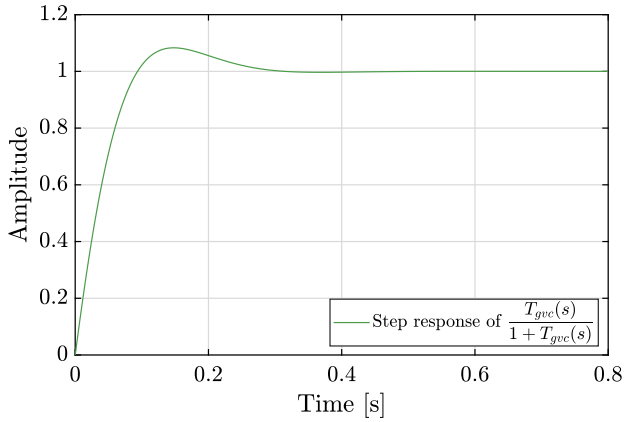


Figure 3.16: Step response of the global voltage control loop.

controllers, and a minimum phase margin of 75°. Through MATLAB PID tuner app, this leads to:

$$G_v(s) = K_{Vi} + \frac{K_{Vi}}{s} = 0.02184 + \frac{0.7384}{s} \tag{3.75}$$

Fig. 3.15 presents the bode diagram of the compensated loop gain $T_{gvc}(s) = G_v(s) \cdot G_{i_{id}}^{v_{dci}}(s)$, clearly showing the crossover frequency and phase margin required. Finally, fig. 3.16 shows the step response of the presented global voltage controller.

Power Feedforward To enhance the dynamic performance of the system and increase its stability boundary, suitable feedforwards can be added to the control system of the SST. In this case, a power feedforward based on the active power requested from the inverter stage (i.e. P_o) is added at the AFE control. The power feedfoward is first transformed

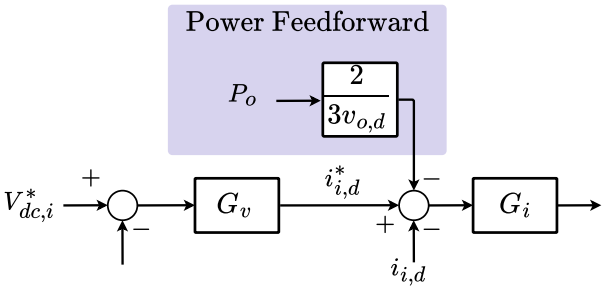


Figure 3.17: Inverter power feedfoward added at the AFE rectrifier i-axis current reference.

into a current feedforward and then is added to the GVC current setpoint, as Fig. 3.17 shows. It is demonstrated in the literature how such feedforward loop can help reduced the AFE DC-link voltages sensitivity to load variations [116, 117].

Cluster Voltage Controller (CVC)

Among the three layers of the DC voltage balancing control used for the AFE rectifier, the cluster voltage controller is certainly the most complicated and crucial one since it has to deal not only with uneven submodules operation but also with unbalances and abnormal conditions of the power grid [112]. In the literature there are several approaches to deal with the cluster voltage balance in a star-connected CHB converter. Typically, the can be categorized in negative-sequence current or voltage injection and zero-sequence voltage injection [112]. Both of them works pretty well in redistributing the active power among three clusters, and in particular the regulation capability of negative-sequence current-based approaches is very effective. However, the negative-sequence current and voltage generated to balanced the clusters will be unavoidably injected in the power grid, which is not preferred and allowed to preserve the grid power quality. Therefore, the second approach based on the zero-sequence voltage generation is usually preferred [112] and adopted in this work. Moreover, the three-phase CHB topology, i.e. star-connected or delta-connected, determines a primary distinction among cluster balancing methods. If in the case of a star-connected CHB a zero-sequence voltage injection is preferred, then in case of delta-connected CHB a zero-sequence current injection should be considered. This

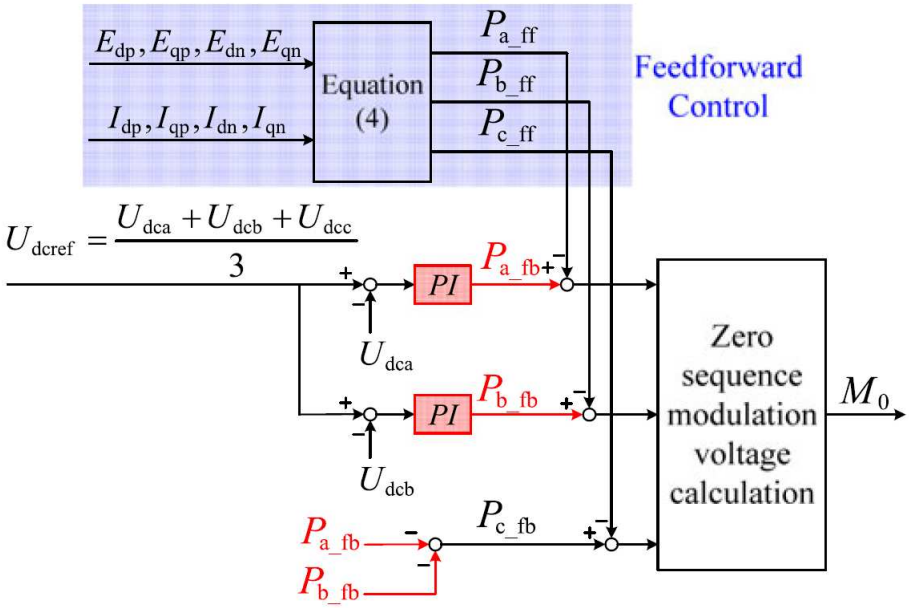


Figure 3.18: Control block diagram of the Cluster Voltage Controller (CVC) of the CHB-based AFE rectifier adopted in this work [112].

is because the zero-sequence current path is enclosed inside the converter due to the delta connection of its phases, and therefore (as for the star-connected CHB) the power grid is not perturbed when the cluster controller is working. The CVC implemented in this work is designed based on the detailed description given in [112]. The CVC control block diagram is represented in Fig. 3.18. The unbalances in phase a and b active power, i.e. P_{a_fb} and P_{b_fb}, are obtained by means of two PI regulators whose error is the difference between the average cluster voltage $\bar{V}_{dc,ij}$ and the actual one $V_{dc,ij}$. On the other hand, the uneven active power in phase C is calculated as the difference $P_{c\_fb} = -P_{a\_fb} - P_{b\_fb}$ so as the net unbalance power that has to be compensated generated among three phases is null. This is required to do not interfere and contrast the active power reference generated by the outer GVC. As fig. 3.18 shows, a feedforward control is also introduced to improved the CVC dynamic performance. The zero-sequence voltage (and therefore the associated zero-sequence modulation signal) is generated according to the uneven active powers P_{a_fb}, P_{b_fb} and P_{b_fb} which must be balanced. The full description of the proposed CVC can be found in [112]. The CVC plant is therefore [112]:

$$G_{v_0}^{v_{dcij}} = \frac{N}{sC_i\bar{V}_{dc,ij}} \tag{3.76}$$

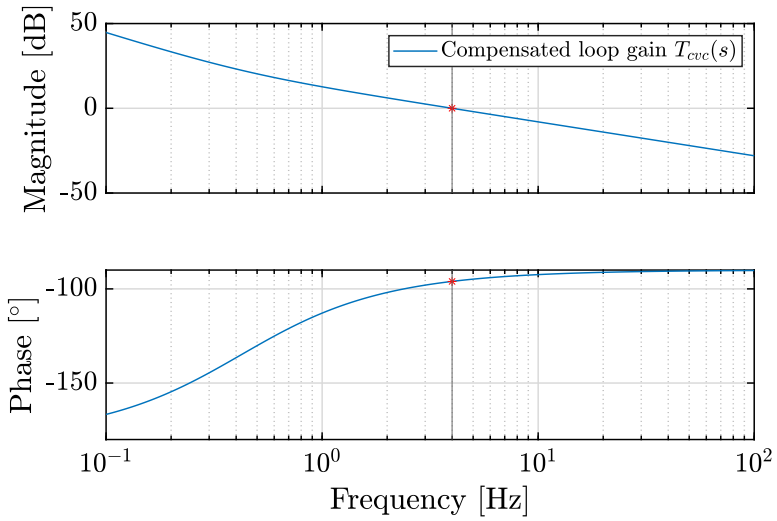


Figure 3.19: Bode diagram of the compensated cluster voltage loop gain $T_{cvc}(s)$.

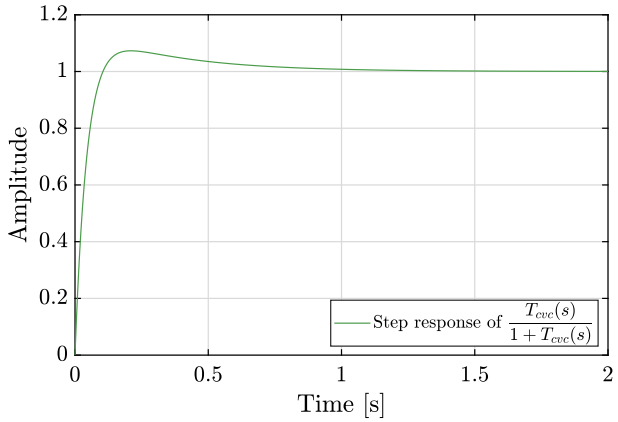


Figure 3.20: Step response of the cluster voltage control loop.

As for the CC and GVC, the CVC PI controller G_{cvc} is designed considering ten-times lower bandwidth with respect to the CC one, to ensure proper decoupling among these controllers, and a minimum phase margin of 75°. Through MATLAB PID tuner app, this leads to:

$$G_{cvc}(s) = K_{cvc} + \frac{K_{cvc}}{s} = 150.96 + \frac{400}{s} \tag{3.77}$$

Fig. 3.19 presents the bode diagram of the compensated loop gain $T_{cvc}(s) = G_{cvc}(s) \cdot G_{v_0}^{v_{dcij}}(s)$, clearly showing the crossover frequency and phase margin required. Finally, fig. 3.20 shows the step response of the presented cluster voltage controller.

Local Voltage Controller (LVC)

The goal of the local voltage controller is to ensure the balance operation among the submodules of one CHB phase. To do so, various individual balancing methods have been proposed in the literature. Depending on whether the local balance is achieved through the modulation process or by means of a closed-loop control strategy, these methods can be classified into two main categories [118,119]: modulation-based or control-based approaches. The first category achieve the individual submodule balancing through advanced modulation techniques, as sorting modulation, multidimensional space vector modulation, etc. [119]. The second category relies on closed-loop controllers to guarantee balanced DC-link voltages, as for example PI-based control [119]. In this work, the second approach is selected as it presents faster dynamics. However, note that PI-based methods may require a significant number of closed-loop controllers. The block diagram of the LVC implemented in this work is shown in Fig. 3.21 and it is based on [113]. In this approach, N-1 submodule voltages (i.e. $v_{dc,ij1}, ..., v_{dc,ij(N.1)}$) are compared to the average DC-voltage of the same phase (i.e. $\bar{V}_{dc,ijk}$). Based on the errors, PI controllers generates output signals that, when multiplied for the normalized current waveform of that phase (i.e. $i_{i,j}$), give rise to small DC voltage variations $\Delta v_{dc,ijk}$. For the N-th submodule, the small voltage change is derived as negative sum of the others, i.e. $\Delta v_{dc,ijN} = -\Delta v_{dc,ij1} - ... - \Delta v_{dc,ij(N-1)}$. This is required, as explained in [113], to not interfere with the outer voltage controllers, i.e. CVC and GVC, thus decoupling the three-layer hierarchical DC voltage control structure implemented in this work. The small voltage variations are then divided by the available global DC link voltage to generate small variation in the modulation indexes. Finally,

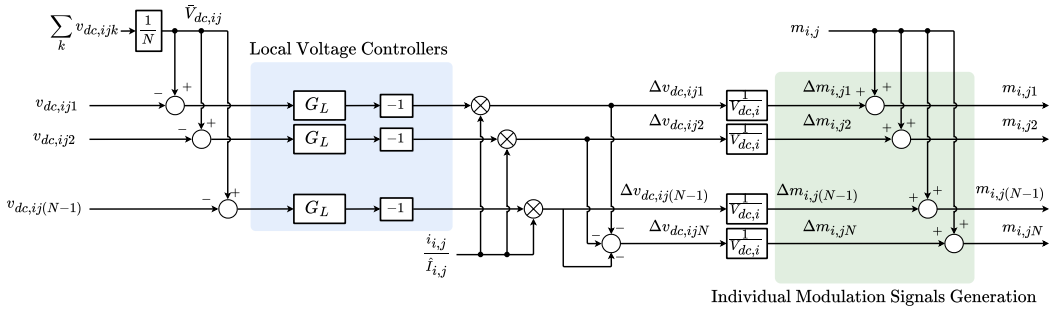


Figure 3.21: Local Voltage Control (LVC) strategy of the CHB-based AFE rectifier.

individual modulation signals are obtained as sum of the overall modulation signal defined for the j-th phase, i.e. $m_{i,j}$, and of the small variation of the modulation indexes $\Delta m_{i,j}$. The LVC plant is derived considering the DC-link node equation in the natural reference frame, i.e.:

$$C_i \frac{d}{dt} v_{dc,ijk} = m_{dc,ijk} \cdot i_{i,j} - i_{L,ijk}, \;\; \forall j = a,b,c, \;\; \forall k = 1, ..., N \tag{3.78}$$

Introducing small perturbation on the modulation index $m_{dc,ijk}$ in (**??**), i.e. $\tilde{m}_{dc,ijk}$, the following is obtained:

$$C_i \frac{d}{dt} v_{dc,ijk} = (m_{dc,ijk} + \tilde{m}_{dc,ijk}) \cdot i_{i,j} - i_{L,ijk}, \;\; \forall j = a,b,c, \;\; \forall k = 1, ..., N \tag{3.79}$$

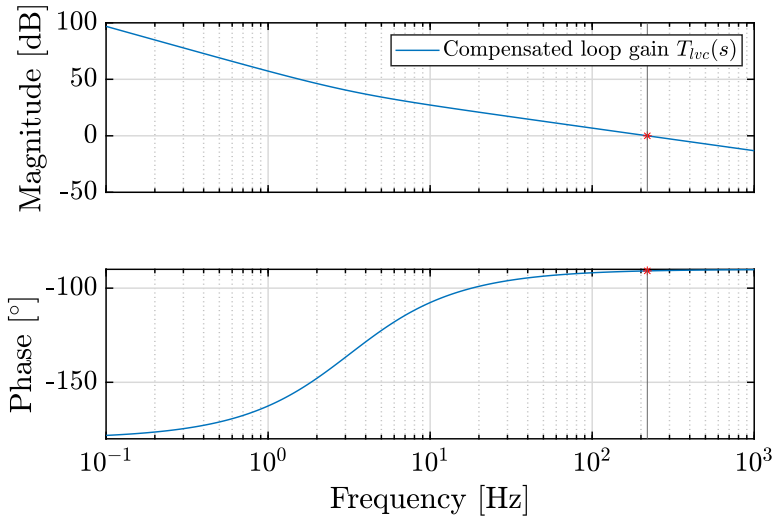


Figure 3.22: Bode diagram of the compensated local voltage loop gain $T_{lvc}(s)$.

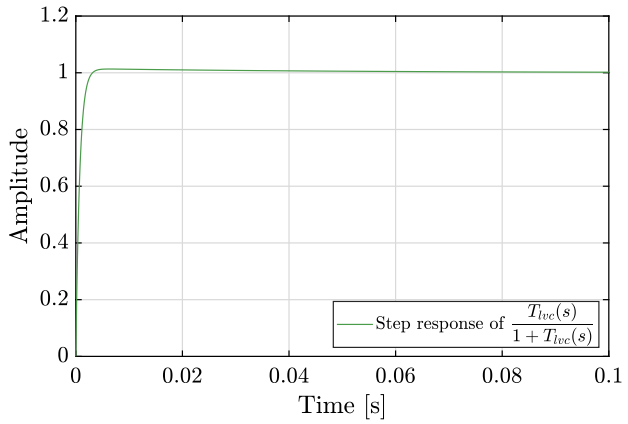


Figure 3.23: Step response of the local voltage control loop.

Perturbing and linearizing eq. (3.79) and solving it in Laplace domain, the LVC plant is obtained as:

$$G_{\Delta m_{ijk}}^{v_{dcijk}} = \frac{\tilde{v}_{dc,ijk}}{\tilde{m}_{dc,ijk}} = \frac{\hat{I}_{i,j}}{sC_i} \tag{3.80}$$

Based on (3.80), the LVC is tuned considering a bandwidth lower than the switching frequency of the CHB (since the modulation signals are updated every T_{sw} and a faster update ration is pointless). Note that there is no need to guarantee a LVC bandwidth ten-times lower that the one of CC because, following the procedure reported here, the LVC is completely decoupled. Through MATLAB PID tuner app, the following is obtained:

$$G_{lvc}(s) = K_{lvc} + \frac{K_{lvc}}{s} = 0.5 + \frac{10}{s} \tag{3.81}$$

Fig. 3.22 presents the bode diagram of the compensated loop gain $T_{lvc}(s) = G_{lvc}(s) \cdot G_{\Delta m_{ijk}}^{v_{dcijk}}(s)$, clearly showing the crossover frequency and phase margin required. Finally, fig. 3.23 shows the step response of the presented cluster voltage controller.

3.3.2 DAB Control System

In the standard control mode operated for the SST under investigation, the DAB converter regulates its output voltage $v_{dc,ojk}$. Fig. 3.11 shows its control strategy. For general purpose of the converter, an output current control has also been implemented. This is useful when the inverter stage of the SST topology is replaced with an active load such as a battery or PV [111]. For the DC-DC converter voltage control, as highlighted in Section 3.2.4, the plant is the control-to-output-voltage transfer function $G_d^{v_o}$ derived through the reduced-order small signal model (3.62), here reported for clarity of the text:

$$G_d^{v_o} = G_d^{i_o} \cdot Z_{rcDAB} = \frac{V_{dc,i}\,(1-2D)}{2nf_{sd}L_t} \frac{R_{dc,o}}{1+sC_oR_{dc,o}} \tag{3.82}$$

While, in case of output load current control, the plant is derived as:

$$G_d^{i_{dc,o}} = G_d^{i_o} \cdot \frac{Z_C}{Z_C+Z_R} = \frac{V_{dc,i}\,(1-2D)}{2nf_{sd}L_t} \frac{\frac{1}{sC_o}}{\frac{1}{sC_o}+R_{dc,o}} = \frac{V_{dc,i}\,(1-2D)}{2nf_{sd}L_t} \frac{1}{1+sC_oR_{dc,o}} \tag{3.83}$$

For both voltage and current controllers, i.e. G_{vDAB} and G_{iDAB}, the bandwidth requested is set to be in the range of 200-300 Hz. As for the AFE controllers, the phase margin

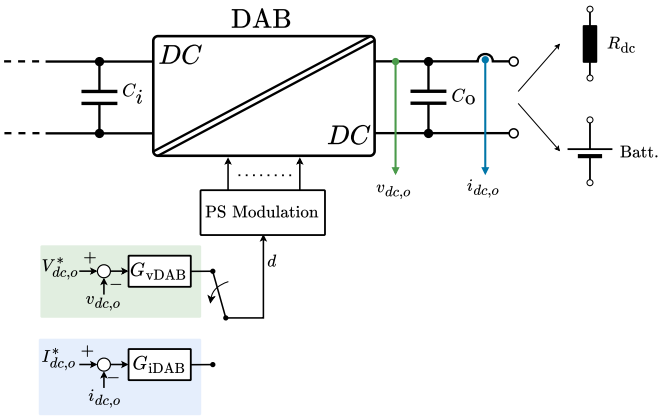


Figure 3.24: Control strategy of the DAB converter.

must be greater on at least equal to 75°. This leads to:

$$G_{vDAB}(s) = K_{Pdab,v} + \frac{K_{Idab,v}}{s} = 0.02 + \frac{8.12}{s} \tag{3.84}$$

$$G_{iDAB}(s) = K_{Pdab,i} + \frac{K_{Idab,i}}{s} = 0.24 + \frac{96.53}{s} \tag{3.85}$$

Fig. 3.25 presents the bode diagram of the compensated loop gain $T_{vDAB}(s) = G_{vDAB}(s) \cdot G_d^{v_o}(s)$, clearly showing the crossover frequency and phase margin required. Fig. 3.26 shows the step response of the presented cluster voltage controller. Fig. 3.27 presents the bode diagram of the compensated loop gain $T_{iDAB}(s) = G_{iDAB}(s) \cdot G_d^{i_o}(s)$, clearly showing the crossover frequency and phase margin required. Fig. 3.28 shows the step response of the presented cluster voltage controller.

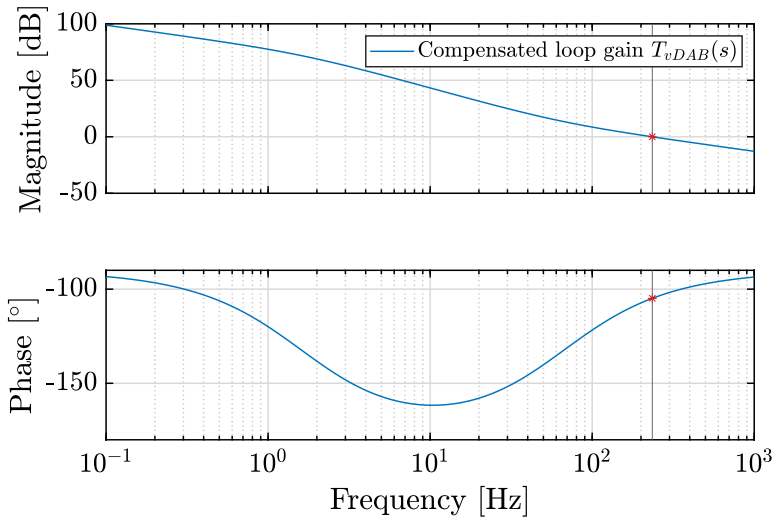


Figure 3.25: Bode diagram of the compensated DAB voltage loop gain $T_{vDAB}(s)$.

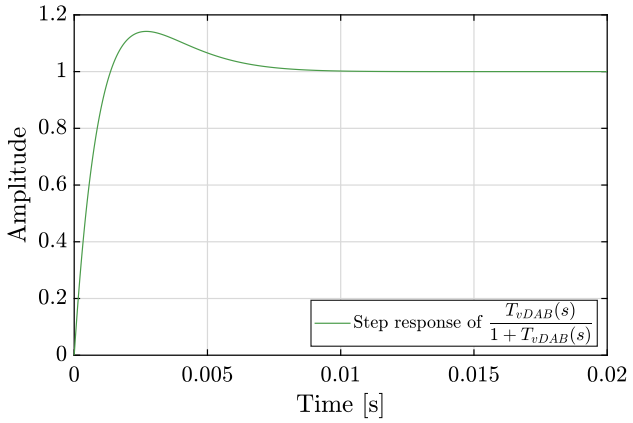


Figure 3.26: Step response of the DAB voltage control loop.

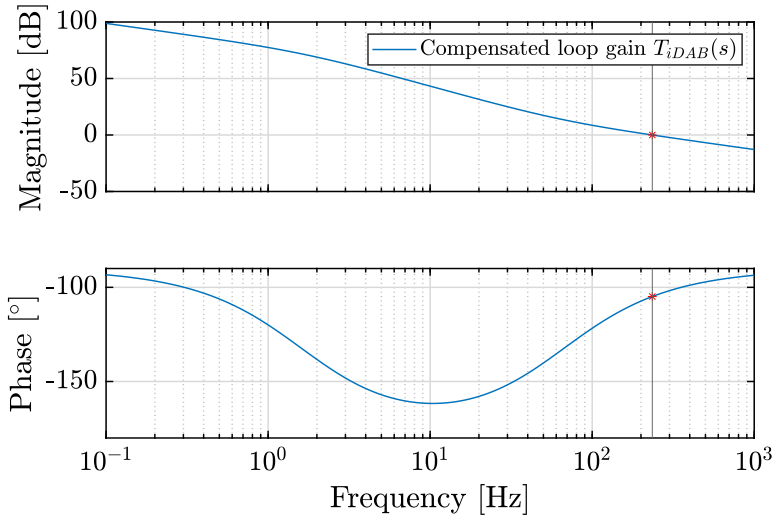


Figure 3.27: Bode diagram of the compensated DAB current loop gain $T_{vDAB}(s)$.

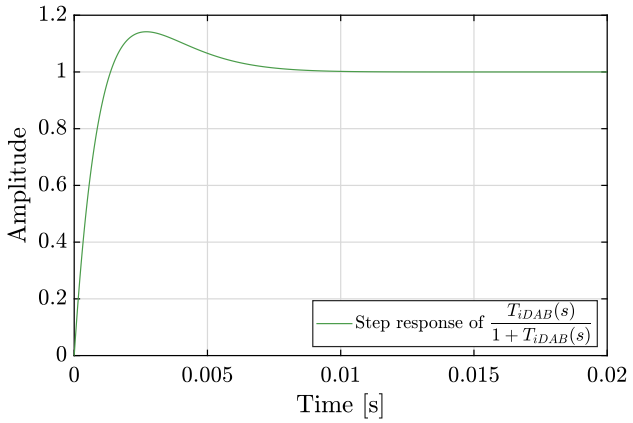


Figure 3.28: Step response of the DAB current control loop.

3.3.3 Inverter Control System

Fig. 3.29 shows the control block diagram for the Inverter stage of the SST. It basically consists of only a current controller, being its DC-link voltages regulated by the DAB converters. The design procedure for the CC of the Inverter stage is the same explained for the AFE rectifier, therefore it will be omitted here.

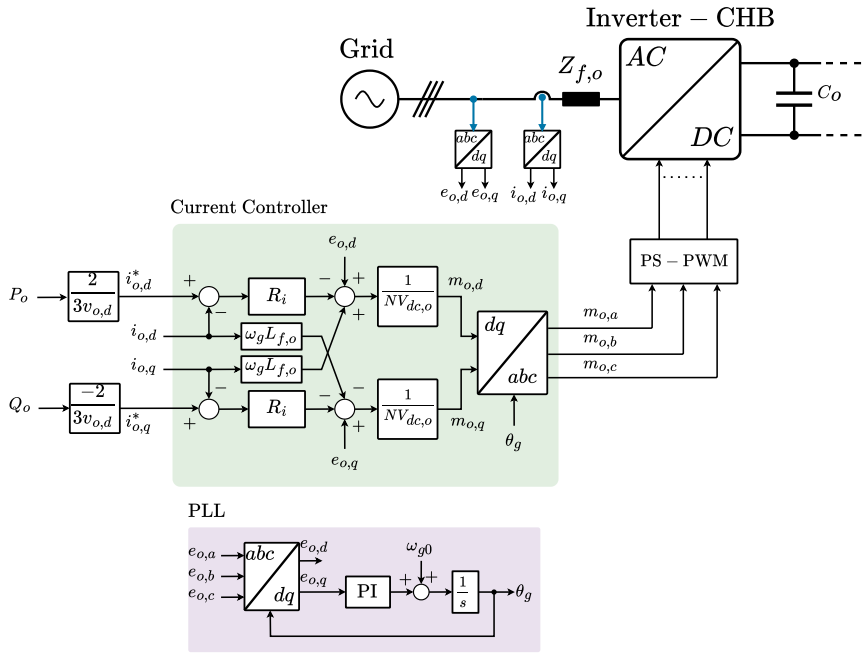


Figure 3.29: Control system strategy of the CHB-based Inverter.

3.4 Simulation Results

The developed SST average model was tested in time-domain simulations in MATLAB/Simulink to verify the correctness of the modeling procedure and the proper operation of both the SST and the control system. The simulation parameters are defined according to Table 3.4. The following test scenarios are evaluated:

1. Steady-state operation: the SST absorbs P_i=127 kW from Port 1 and therefore P_o=-127 kW. No reactive power on both ports is exchanged (see Fig. 3.30);

2. Load step: after having reached the steady-state, at t=1.2s P_i is increased of about 40 % (see Fig. 3.31);

3. Reactive power exchange with Port 1: after having reached the steady-state, at t=1.2s Q_i is set to be 50 kVAr (see Fig. 3.32);

4. Reactive power exchange with Port 2: after having reached the steady-state, at t=1.2s Q_o is set to be 50 kVAr (see Fig. 3.33);

5. DC-link voltage increase: after having reached the steady-state, at t=1.2s $V^*_{dc,i}$ is set increased of 5 % with respect to the nominal value (see Fig. 3.34);

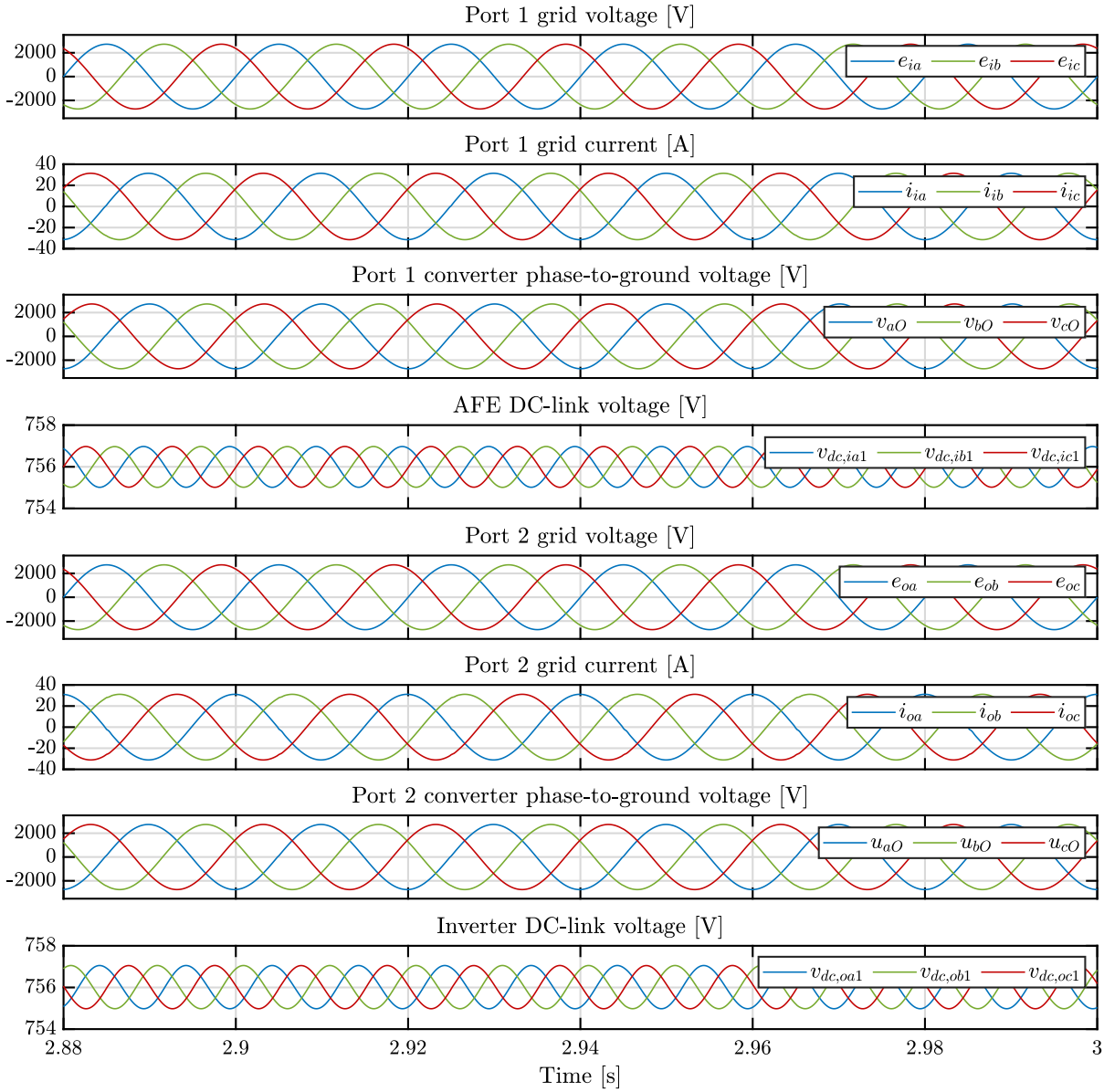


Figure 3.30: Steady-state operation simulation results.

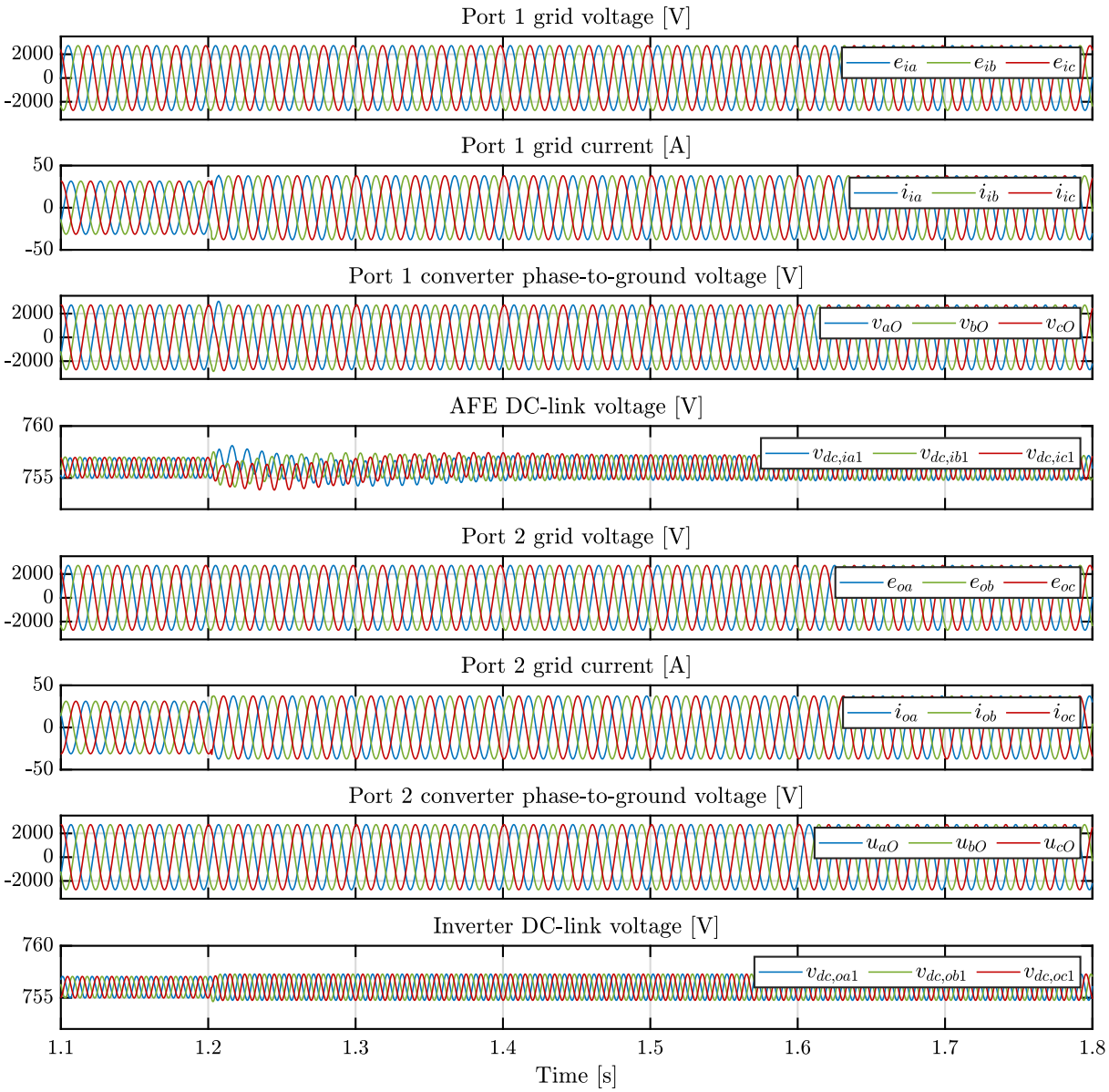


Figure 3.31: Load step simulation results.

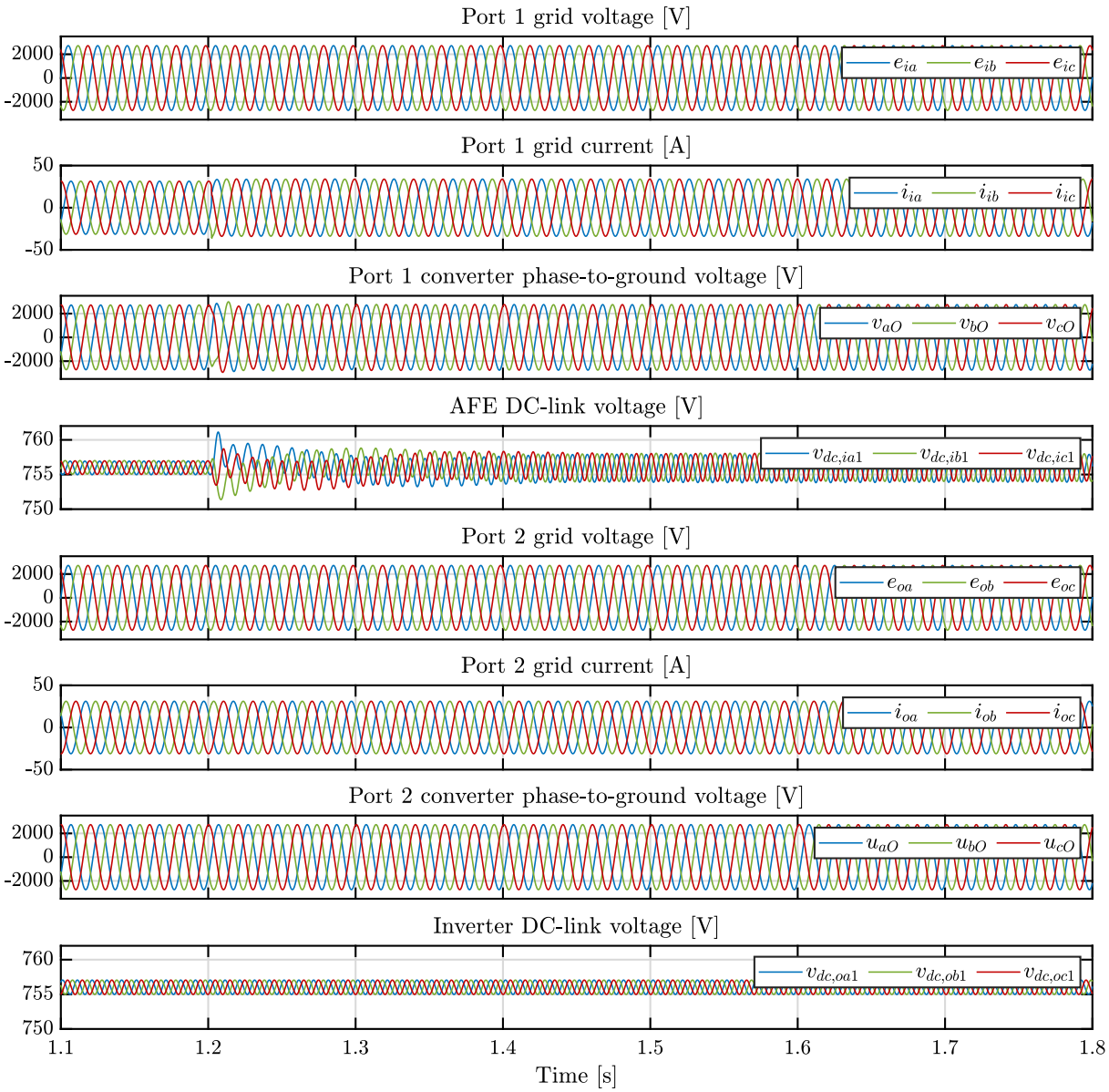


Figure 3.32: Reactive power exchange with Port 1 simulation results.

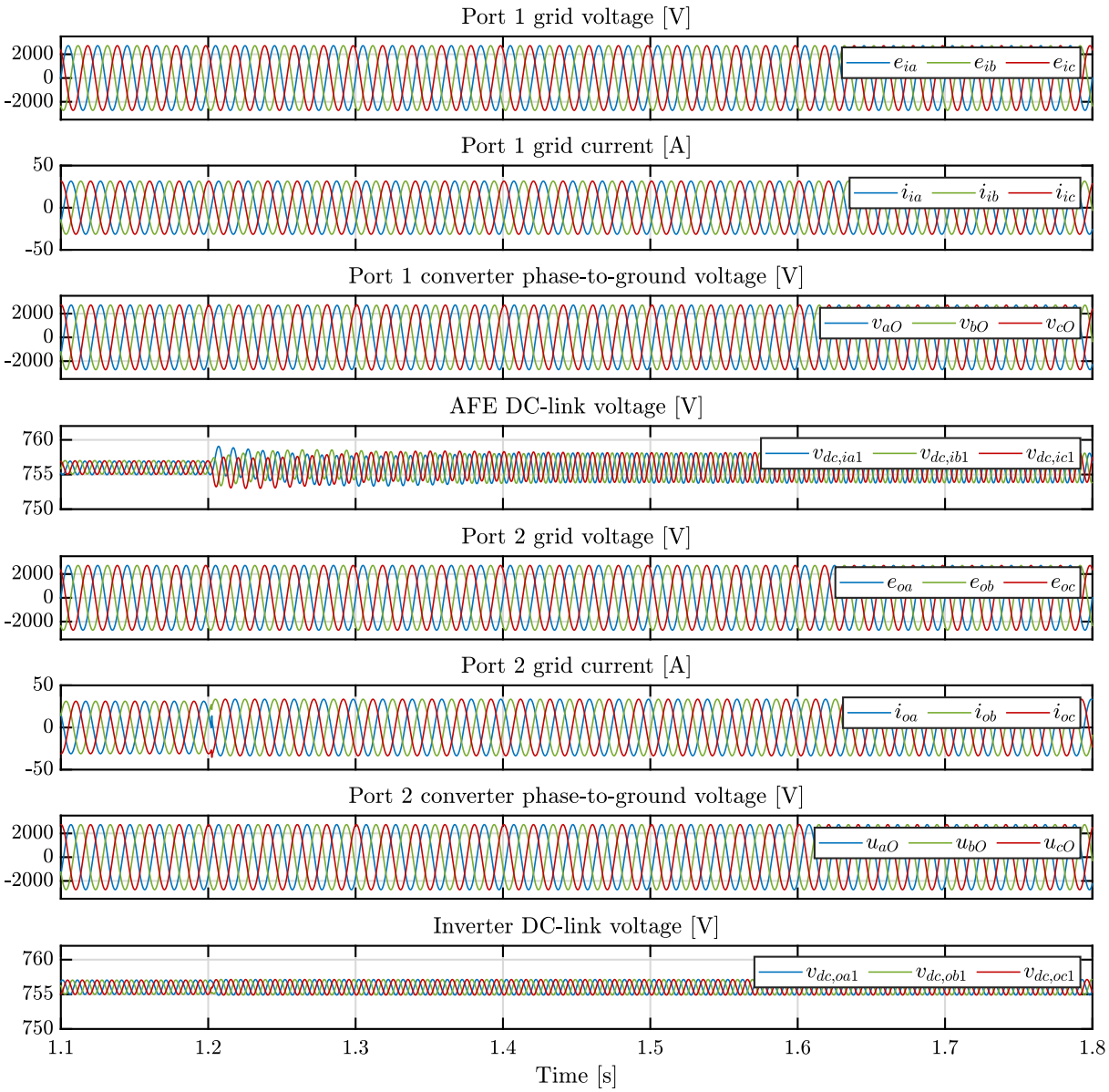


Figure 3.33: Reactive power exchange with Port 2 simulation results.

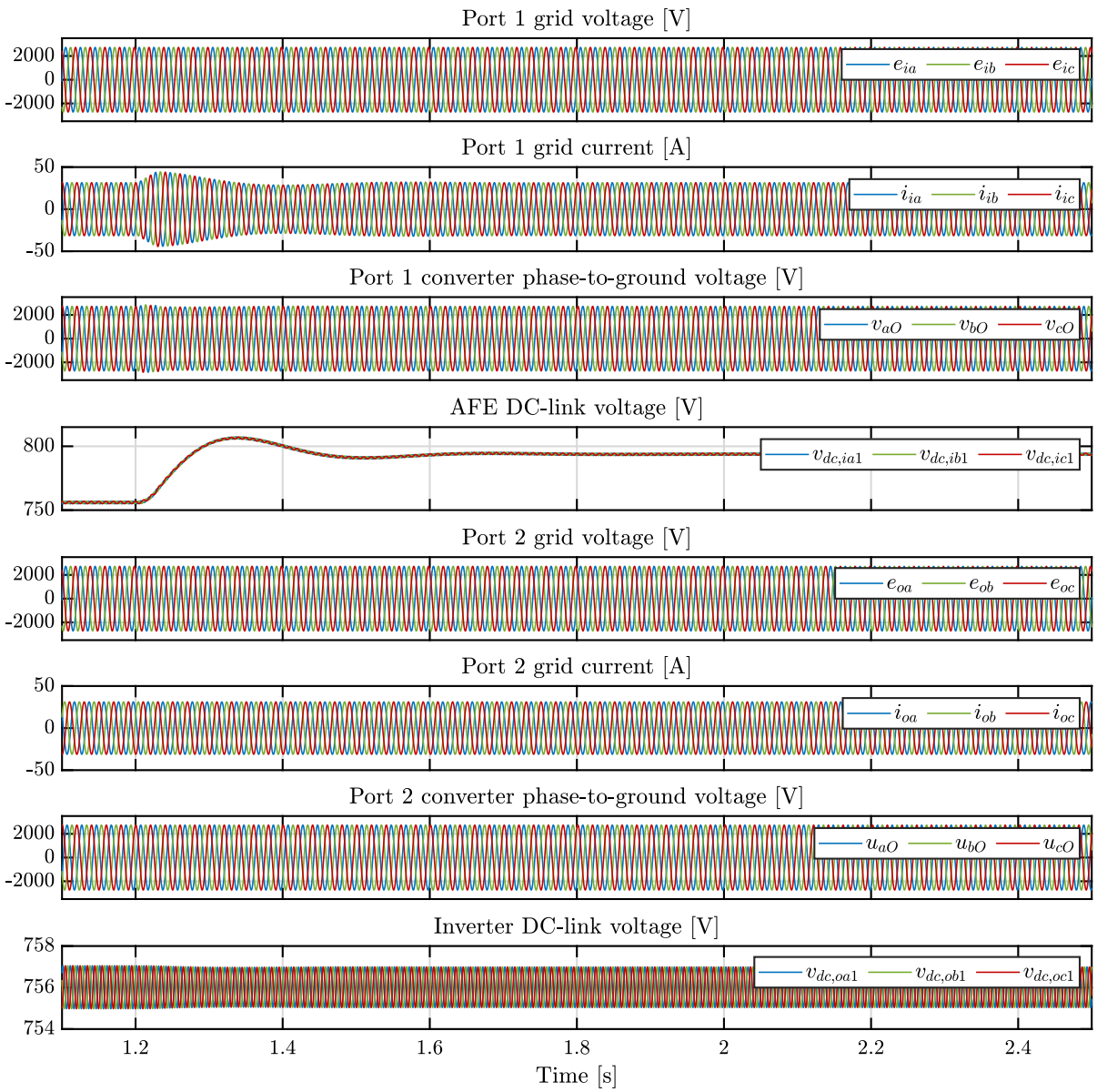


Figure 3.34: DC-link voltage increase simulation results.

Chapter 4

Stability Analysis of Three-Phase Triple-Stage Solid-State Transformer

4.1 Stability Analysis Background and Motivation

Nowadays, power electronics converters play a crucial role in a variety of applications ranging from RES/ESSs integration to transportation and smart grid facilities. Because of the today's need of efficient, smart and reliable electric systems, their deployment is continuously growing. However, power converters show non-linear behavior due to their switching dynamics. Therefore, during their operation they inherently produce harmonics and, moreover, they could interact with each others and/or with other equipments generating disturbances and unwanted interactions. Furthermore, power electronics converters are usually operated under closed-loop control mode. This adds an additional element of complexity to the overall system operation because the closed-loop control typically reshapes the converter dynamic behavior. To deal with such disturbances, the need for robust stability analysis becomes ever more pressing. Stability analysis is a fundamental tool in the design, optimization, and operation of power electronic converters and control systems, providing critical insights into their dynamic behavior and response to various operating conditions, disturbances, and uncertainties. By comprehensively evaluating stability, engineers can mitigate the risk of undesirable phenomena such as oscillations, instability, and system failures, thereby enhancing performance, reliability, and life-time of power electronic devices.

Instabilities may involve both AC and DC systems. In the first case, usually instabilities arise from interaction among the converter control or switching dynamics and the grid ones [120, 121]. Also, undesired interactions may also arise between different converters. On the other hand, in DC networks instabilities often results from the () behavior that causes a negative incremental input impedance at the DC converter terminals [122–125]. This is due to the constant-power control often used in such systems.

The SST is a complex power electronics-based system featuring structured control architecture. Moreover, it has to deal with both AC and DC quantities, being it a grid-connected system (in some case even interconnecting multiple grids) and providing DC-buses for the integration of various DC sources and loads. Therefore, in order to guarantee the proper operation of the SST, stability analysis is fundamental for such system. Among many approaches that can be used to assess power electronics stability issues, when dealing with linearized models such as small-signal models there are mainly two methodologies: the state-space analysis and the impedance-based analysis [121]. The first typically results in high-order system when the control system is integrated into the open-loop converter model. Furthermore, converter and control parameters need to be known in order to develop the state-space model. On the other hand, impedance-based modelling captures the converter dynamic behavior as transfer functions [121, 122]. The converter operation can be characterized by an impedance seen at its output or input terminals. Therefore, when interconnected with other converters or with the grid, stability can be evaluated by means of an equivalent circuit through circuit analysis tools. The impedance-based analysis is nowadays widely preferred over the state-space one because it offer the great advantage of allowing the black-box modeling of the converter [121].

For the reasons highlighted above, in this work the impedance-based analysis is chosen as approach to assess the SST stability. Furthermore, in this thesis both DC and AC stability issues has been investigated. The aim of the analysis proposed in this work is to provide a valuable design SST tool from both the control and system level perspective. In the next two Sections, both DC and AC stability assessments are presented.

4.2 Impedance-based DC-Link Stability Analysis

In DC distribution systems, potential stability degradation may occur when switching converters are connected to a common bus. There are two possible explanations for this phenomenon. The first interpretation is that the stability degradation is due the interactions among the feedback loops of the interconnected converter. The second interpretation considers the issue to be caused by the CPL effect. In general, converters tend to act as CPLs at their input terminals when subject to tight feedback regulation within their control loop bandwidth. CPLs have a negative incremental input impedance, which is the cause of the subsystem interaction problem and origin of the undesired destabilizing effects. Although each subsystem is designed to be stable independently, a system consisting of multiple power-electronics-based subsystems may experience a decline in stability due to subsystem interactions caused by CPLs. The subsystem interaction may substantially alter the control bandwidth from the standalone case and may compromise control stability both at the converter and system level. Therefore, because of its complex control structure, which has been presented in Section 3.3, the SST is a conversion system highly prone to instability and to performance degradation if not well designed. However, the SST stability issue has been barely ever addressed in the existing literature. In [126] a stability analysis has been performed for a system composed of a rectifier connected to a DAB converter, but the control changes depending on the power flow direction. Acharya et al. [127] performed a stability analysis on medium-voltage (MV) SST, which, however, is not a multilevel configuration with multiple building blocks. In [128], Ye et al. investigated the stability of a SST considering a single control for the DAB regardless of the power flow direction, but the analysis is only focused on the dc bus. In [129] a comprehensive analysis regarding the stability and control is carried out considering bidirectional power flow in the case of a single-phase SST. However, as shown in Section 3.3.1, three-phase converters require a different voltage balancing control scheme.

In case of multi-stage cascaded system such as a SST, the direct link between two cascaded systems is the output impedance of the upstream converter and the input impedance of the downstream converter. Thus, the behavior of the cascaded system can be influenced by those two impedances. The effect of the multilayer control system and of its

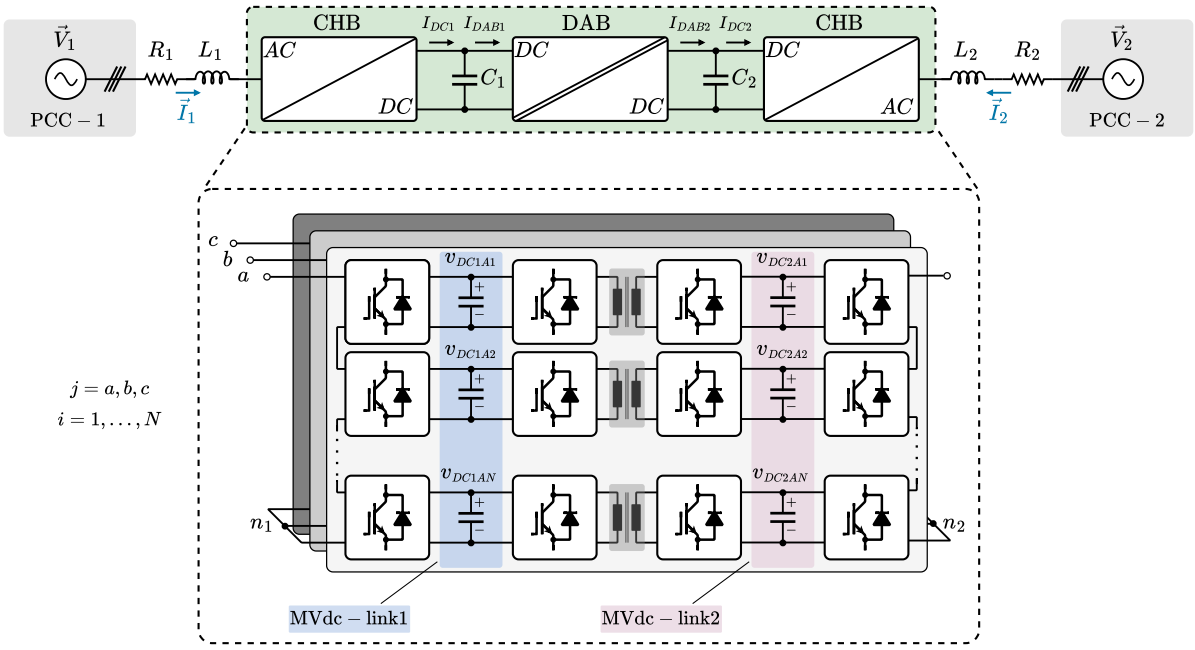


Figure 4.1: Triple-stage three-phase ISOS-connected SST topology connected between two electrical grids.

bandwidth can alter the impedance shape at the dc-link interfaces. To ensure the system is stable, one approach can be the Middlebrook's stability criterion, which is based on the converter impedance-model. Cascaded converters need to satisfy the Middlebrook's criterion to avoid unwanted interaction between subsystems [130].

To fill the discussed literature gap, in this Section the DC-bus stability of the SST is presented, providing a comprehensive stability analysis of the triple-stage three-phase modular SST topology previously introduced in this thesis, whose circuit diagram is shown in Fig. 4.1. As stated above, the analysis is based on the converter impedance-model which will be derived through the small-signal models presented in Sections 3.1 and 3.2. The Middlebrook's criterion is then used to guarantee a stable system.

For the rest of the work presented in this Section, the nomenclature used in equations follows the one exhibited in Fig. 4.1. Also, in this section the subscript i denotes the submodule number, i.e. $i = 1, ..., N$ while the subscript j, as for Chapter 3 refers to the phase, i.e. $j = a, b, c$.

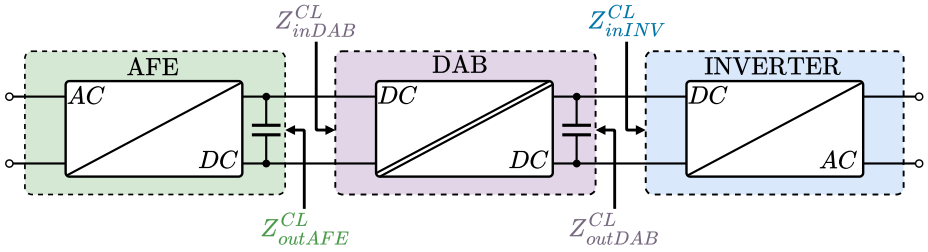


Figure 4.2: SST input and output transfer functions diagram.

4.2.1 Problem Statement and Methodology

As mentioned before, in this thesis the converter DC-link stability assessment is performed through the Middlebrook stability criterion [130]. For two cascaded systems, the sufficient condition expressed by (4.1) should be met for every operating point to ensure the stability [130]:

$$||Z_{out}(s)|| \ll ||Z_{in}(s)|| \tag{4.1}$$

which means that the input impedance of the downstream converter needs to be higher than the output impedance of the upstream stage. By evaluating the converter closed-loop impedances at both PEBB interfaces, i.e. at input DC-link which interfaces each AFE submodules (i.e. MVdc-link1 with reference to Fig. 4.1) with the DAB converter and at output DC-link interface that connects each DAB converters with the Inverter submodules (i.e. MVdc-link2), the stability of the SST can be analyzed. Fig. (4.2) shows the closed-loop impedance transfer functions $Z^{CL}_{outAFE}, Z^{CL}_{inDAB}, Z^{CL}_{outDAB}$ and Z^{CL}_{inINV}, which are respectively the closed-loop AFE output impedance, DAB closed-loop input and output impedances and the closed-loop Inverter input impedance, that need to be derived in order to assess the stability issue of the SST converter considered in this work. Note that the effect of the hierarchical voltage control loop on the individual MVdc-link1 voltages is therefore taken into account by performing the analysis on the single SST PEBB.

In the next section, the analytical expression of the SST impedance transfer functions is presented through the derivation of the small signal model for each conversion stage based on the converter average model developed in 3.1 and 3.2.

4.2.2 SST DC-bus Impedance Model Derivation

Active Front-End Rectifier Impedance Model

For the AFE rectifier, the DC-bus impedance model is derived starting from the CHB-based AFE *dq* small-signal model given in (3.44) and represented by the equivalent circuit shown in 3.5. Thus, recalling (3.44) and referring to the nomenclature of Fig. 4.1:

$$\frac{d}{dt}\begin{bmatrix}\tilde{i}_{1d}\\ \tilde{i}_{1q}\\ \tilde{v}_{DC1}\end{bmatrix}=\begin{bmatrix}-\frac{R_1}{L_1} & \omega & -\frac{NM_{1d}}{L_1}\\ -\omega & -\frac{R_1}{L_1} & -\frac{NM_{1q}}{L_1}\\ \frac{M_{1d}}{2C_1} & \frac{M_{1q}}{2C_1} & 0\end{bmatrix}\begin{bmatrix}\tilde{i}_{1d}\\ \tilde{i}_{1q}\\ \tilde{v}_{DC1}\end{bmatrix}+\begin{bmatrix}\frac{1}{L_1} & 0 & -\frac{NV_{DC1}}{L_1} & 0 & 0\\ 0 & \frac{1}{L_1} & 0 & -\frac{NV_{DC1}}{L_1} & 0\\ 0 & 0 & \frac{I_{1d}}{2C_1} & \frac{I_{1q}}{2C_1} & -\frac{1}{C_1}\end{bmatrix}\begin{bmatrix}\tilde{v}_{1d}\\ \tilde{v}_{1q}\\ \widetilde{m}_{1d}\\ \widetilde{m}_{1q}\\ \tilde{i}_{DAB1}\end{bmatrix} \tag{4.2}$$

By sorting out (4.2) to develop the state-space equations, the AFE rectifier model is then transformed into Laplace domain and, through eq. (3.59), the following solution is obtained:

$$\begin{bmatrix}\tilde{i}_{1d}\\ \tilde{i}_{1q}\\ \tilde{v}_{DC1}\end{bmatrix}=\begin{bmatrix}G_{v_{1d}}^{i_{1d}} & G_{v_{1q}}^{i_{1d}} & G_{m_{1d}}^{i_{1d}} & G_{m_{1q}}^{i_{1d}} & G_{i_{DAB1}}^{i_{1d}}\\ G_{v_{1d}}^{i_{1q}} & G_{v_{1q}}^{i_{1q}} & G_{m_{1d}}^{i_{1q}} & G_{m_{1q}}^{i_{1q}} & G_{i_{1qAB1}}^{i_{1q}}\\ G_{v_{1d}}^{v_{DC1}} & G_{v_{1q}}^{v_{DC1}} & G_{m_{1d}}^{v_{DC1}} & G_{m_{1q}}^{v_{DC1}} & G_{i_{DAB1}}^{v_{DC1}}\end{bmatrix}\begin{bmatrix}\tilde{v}_{1d}\\ \tilde{v}_{1q}\\ \widetilde{m}_{1d}\\ \widetilde{m}_{1q}\\ \tilde{i}_{DAB1}\end{bmatrix} \tag{4.3}$$

where G_u^y denotes the transfer function from the input variable u to the output variable y. Eq. (4.3) dynamic behavior of the AFE converter. Note that $-\mathrm{G}_{\mathrm{i_{DAB1}}}^{\mathrm{vDC1}}$ represents the AFE converter open-loop transfer function $\mathrm{Z}_{\mathrm{outAFE}}^{\mathrm{OL}}$, which is defined as:

$$Z_{outAFE}^{OL}= -\frac{\widetilde{v}_{DC1}}{\widetilde{i}_{DAB1}}\bigg|_{\widetilde{v}_{1d}=\widetilde{v}_{1q}=\widetilde{m}_{1d}=\widetilde{m}_{1q}=0} \tag{4.4}$$

To derive the AFE closed-loop output impedance, it is necessary to include the effect of the control actions on system dynamics. The AFE control system was previously introduced and designed in Section 3.3.1, along with the DAB and Inverter control schemes. Based on that, Fig. 4.3 shows an overview on the SST control system considered for the DC-bus stability analysis presented in this Section, whose new nomenclature is defined according to Fig. 4.1. Considering first the LVC, the corresponding control block diagram is derived based on Fig. 3.21 and it is depicted in Fig. 4.4. Taking into consideration the DC-side equation of the i-*th* HB inside the j-*th* converter phase given in (3.78) and

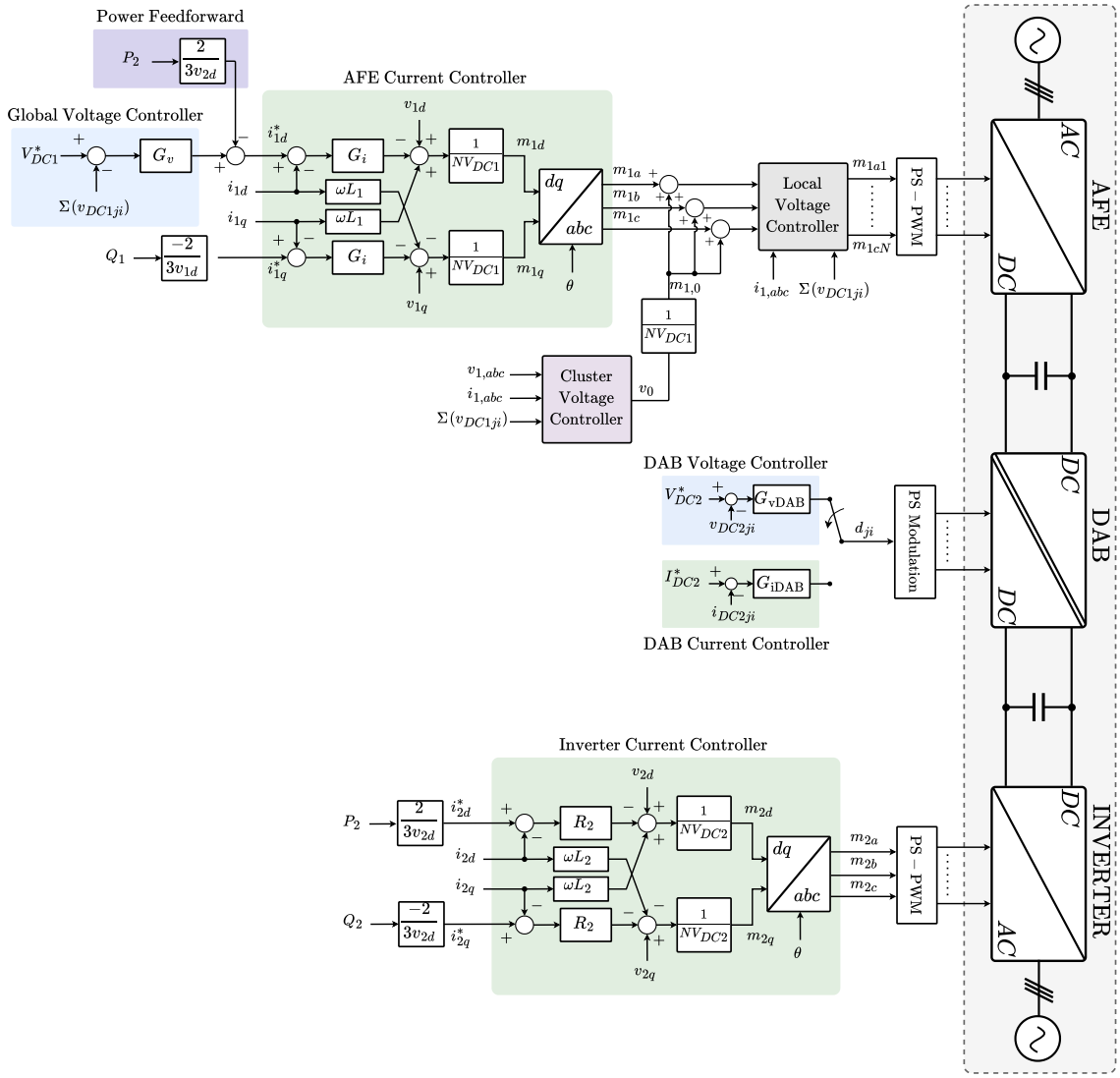


Figure 4.3: Overall SST control system considered for the DC-bus stability analysis carried out in this Section.

supposing to introduce a small variation of the modulation index, (3.78) can be rewritten as:

$$sC_1\tilde{v}_{DC1ji} = (M_{1ji} + \Delta M_{1ji})\,\tilde{i}_{1j} + I_{1j}\tilde{m}_{1ji} + I_{1j}\tilde{\Delta m}_{1ji} - \tilde{i}_{DAB1ji},\ \ \forall j = a,b,c,\ \forall k = 1,...,N \tag{4.5}$$

At this point, considering the sum of the N dc voltage inside the j-*th* phase and assuming that $v_{DC1j1} = \ldots = v_{DC1jN} = v_{DC1ji}$, the following is obtained:

$$\sum_i \tilde{v}_{DC1ji} = N\tilde{v}_{DC1ji} = \left(N\frac{M_{1ji}}{sC_1} + \frac{N\Delta M_{1ji}}{sC_1}\right)\tilde{i}_{1j} + \frac{NI_{1j}}{sC_1}\widetilde{m}_{1ji} + \frac{NI_{1j}}{sC_1}\widetilde{\Delta m}_{1ji} - \frac{N}{sC_1}\tilde{i}_{DAB1ji} \tag{4.6}$$

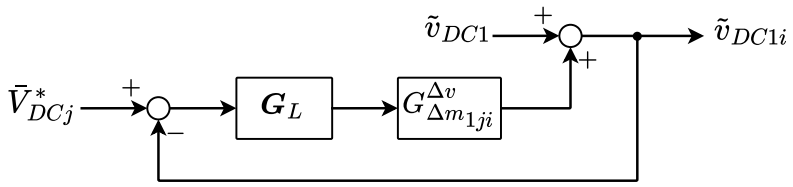


Figure 4.4: Local Voltage Control block diagram.

The term $N\Delta M_{1ji}$ is the sum of the steady-state variations of the modulation indexes of the N HB submodules inside the j-*th* converter phase, which is always null according to the LVC scheme outlined in this Section, which has been designed in order to obtain the decoupling among voltage controllers as explained in [113]. Therefore (4.6) becomes:

$$N\tilde{v}_{DC1ji} = \underbrace{\left(N\frac{M_{1ji}}{sC_1}\right)\tilde{i}_{1j} + \frac{NI_{1j}}{sC_1}\widetilde{m}_{1ji}}_{\text{GVC } (dq \text{ control})} + \underbrace{\frac{NI_{1j}}{sC_1}\tilde{\Delta m}_{1ji}}_{\text{LVC}} \underbrace{-\frac{N}{sC_1}\tilde{i}_{DAB1ji}}_{\text{DC-Load}} \tag{4.7}$$

The first two terms of (4.7) correspond to the GVC effect on the dc link voltages through the *dq* control loop, while the third term of the equation represents the LVC effect and the last one the load effect. Thus, according to the diagram given in Fig. 4.4, the LVC plant is given by:

$$G^{\Delta v}_{\Delta m_{1ji}} = \frac{I_{1j}}{sC_1} \tag{4.8}$$

Then, according to the AFE dq small-signal model circuit representation given in Fig. 3.5 and according to Fig. 4.4, the transfer function between the average dc-link voltage $\widetilde{v}_{DC1}$ and the i-th HB submodule local voltage $\widetilde{v}_{DC1i}$, namely $G^{v_{DC1i}}_{v_{DC1}}$, can be expressed as:

$$G^{v_{DC1i}}_{v_{DC1}} = \left.\frac{\widetilde{v}_{DC1i}}{\widetilde{v}_{DC1}}\right|_{V^*_{DC1i}=0} = \frac{1}{1 + G_L G^{\Delta v}_{\Delta m_{1ji}}} \tag{4.9}$$

where G_L is the local voltage PI controller.

The CVC controller scheme was presented in Fig. 3.18. However, the CVC operates only during transients, providing practically null contribution at steady-state. Therefore, because the DC-bus stability analysis of the SST is performed at steady-state conditions, the effect of the CVC on the system stability can be neglected.

Based on these assumptions, the AFE control block diagram is derived according to both the inherent plant description given in (4.3) and control system represented in Fig. 4.3 and it is shown in Fig. 4.5. In the figure, boldface capital letters are used to denote

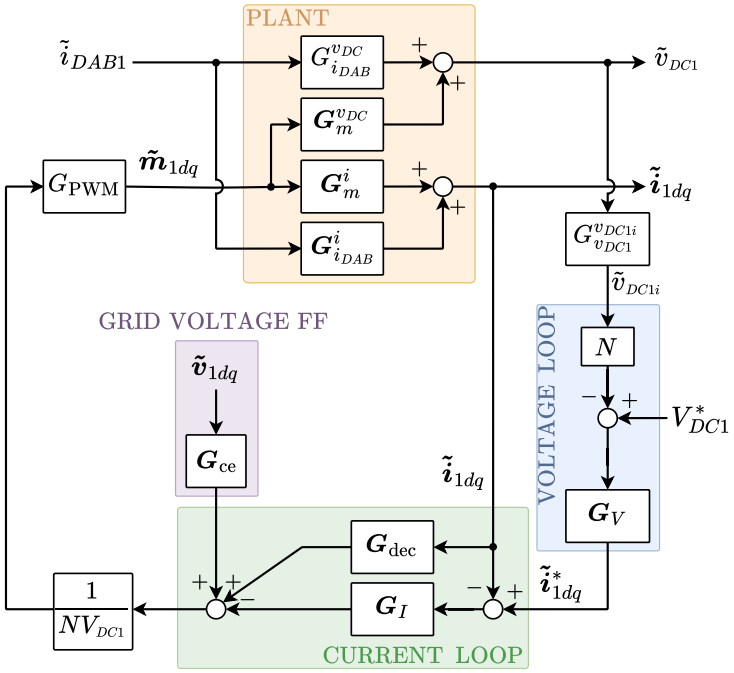


Figure 4.5: The CHB-based AFE rectifier control block diagram.

transfer function matrices while boldface lowercase ones to denote vectors. Except for the terms already specified in the text, the plant transfer functions $G_{i_{DAB}}^{v_{DC}}$, $\boldsymbol{G}_m^{v_{DC}}$, $\boldsymbol{G}_m^i$ and $\boldsymbol{G}_{i_{DAB}}^i$ are defined based on (4.3) as:

$$G_{i_{DAB}}^{v_{DC}} = G_{i_{DAB1}}^{v_{DC1}} \tag{4.10}$$

$$\boldsymbol{G}_m^{v_{DC}} = \begin{bmatrix} G_{m_{1d}}^{v_{DC1}} & G_{m_{1q}}^{v_{DC1}} \end{bmatrix} \tag{4.11}$$

$$\boldsymbol{G}_m^i = \begin{bmatrix} G_{m_{1d}}^{i_{1d}} & G_{m_{1q}}^{i_{1d}} \\ G_{m_{1d}}^{i_{1q}} & G_{m_{1q}}^{i_{1q}} \end{bmatrix} \tag{4.12}$$

$$\boldsymbol{G}_{i_{DAB}}^i = \begin{bmatrix} G_{i_{DAB1}}^{i_{1d}} \\ G_{i_{DAB1}}^{i_{1q}} \end{bmatrix} \tag{4.13}$$

the remaining transfer functions are defined as:

$$\boldsymbol{G}_V = \begin{bmatrix} K_{Pv} + \dfrac{K_{Iv}}{s} \\ 0 \end{bmatrix} \tag{4.14}$$

$$\boldsymbol{G}_I = \begin{bmatrix} K_{Pi} + \dfrac{K_{Ii}}{s} & 0 \\ 0 & K_{Pi} + \dfrac{K_{Ii}}{s} \end{bmatrix} \tag{4.15}$$

$$\boldsymbol{G}_{\text{dec}} = \begin{bmatrix} 0 & \omega L_1 \\ -\omega L_1 & 0 \end{bmatrix} \tag{4.16}$$

$$\boldsymbol{G}_{\text{ce}} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \tag{4.17}$$

$$\boldsymbol{G}_{PWM} = \begin{bmatrix} e^{-sT_{\text{d}}} & 0 \\ 0 & e^{-sT_{\text{d}}} \end{bmatrix} \tag{4.18}$$

where [131]:

$$T_{\text{d}} = 1.5T_{\text{sw}} = \frac{3}{2f_{\text{sw}}} \tag{4.19}$$

in which f_{sw} is the switching frequency of the AFE.

Based on the AFE control block diagra, and neglecting for simplicity the cross coupling matrix $\boldsymbol{G}_{dec}$, the AFE output impedance under current closed-loop can be derived as:

$$Z_{\text{outAFE}}^{CL(G_i)} = -\left.\frac{\tilde{v}_{DC1i}}{\tilde{\tilde{i}}_{DAB1}}\right|_{I_{Id}^*=I_{1q}^*=0} = -G_{v_{DC1}}^{v_{DC1i}}\left(G_{i_{DAB1}}^{v_{DC1}} + G_{m_{1d}}^{v_{DC1}}K_dG_{i_{DAB1}}^{i_{1d}} + G_{m_{1q}}^{v_{DC1}}K_qG_{i_{DAB1}}^{i_{1q}}\right) \tag{4.20}$$

where:

$$K_d = \frac{G_{PWM}G_I}{NV_{DC1} - G_{PWM}G_IG_{m_{1d}}^{i_{1d}}} \tag{4.21}$$

$$K_q = \frac{G_{PWM}G_I}{NV_{DC1} - G_{PWM}G_IG_{m_{1q}}^{i_{1q}}} \tag{4.22}$$

Finally, the AFE output impedance under voltage and current closed-loop control is given as:

$$Z_{outAFE}^{CL} = -\left.\frac{\widetilde{v}_{DC1i}}{\widetilde{i}_{DAB1}}\right|_{V_{DC1}^*=I_{1q}^*=0} = \frac{Z_{outAFE}^{CL(Gi)}}{1 - NK_dG_{v_{DC1}}^{v_{DC1i}}G_VG_{m_{1d}}^{v_{DC1}}} \tag{4.23}$$

Dual Active Bridge Impedance Model

For the DAB converter, the impedance model is derived starting from the reduced-order small-signal model presented in (3.62) and represented by the equivalent circuit shown in 4.6, that reports the variable nomenclature used in this Section. Note that $\tilde{i}_{DC2}$ represents the small-signal perturbation on the Inverter DC-side current request. Based on the DAB control block diagram given in Fig. 4.7, defined considering only the voltage-control

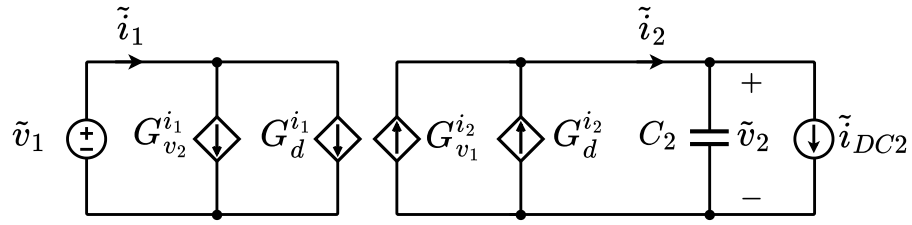


Figure 4.6: Dual Active Bridge small signal model.

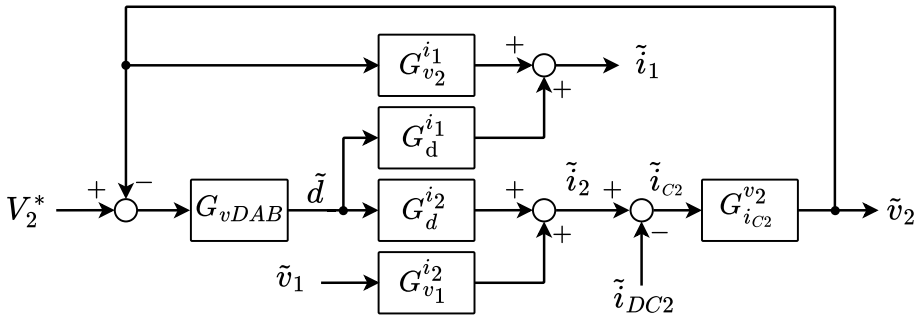


Figure 4.7: Voltage control block diagram model of the DAB.

mode of the DAB (cfr. 4.3 for the whole control strucutre), the closed-loop DAB input impedance is:

$$Z_{inDAB}^{CL} = \left.\frac{\widetilde{v}_1}{\widetilde{i}_1}\right|_{V_2^*} = \frac{1 + G_{i_{c2}}^{v_2} G_d^{i_2} G_{vDAB}}{\left(G_{v_2}^{i_1} - G_d^{i_1} G_{vDAB}\right) G_{i_{c2}}^{v_2} G_{v_1}^{i_2}} \tag{4.24}$$

where $\widetilde{i}_{DC2}$ is the dc current absorbed by the Inverter according to Fig. 1, $\widetilde{G}_{vDAB}$ is the DAB voltage controller and $G_{i_{c2}}^{v_2}$ is defined as:

$$G_{i_{c2}}^{v_2} = \frac{1}{sC_2} \tag{4.25}$$

Then, according to Fig. 4.7, the closed-loop DAB output impedance is given by:

$$Z_{outDAB}^{CL} = -\left.\frac{\widetilde{v}_2}{\widetilde{i}_{DC2}}\right|_{V_2^*=\tilde{v}_1=0} = \frac{G_{i_{c2}}^{v_2}}{1 + G_{i_{c2}}^{v_2} G_d^{i_2} G_{vDAB}} \tag{4.26}$$

Inverter Impedance Model

In this work, the Inverter stage is connected with the Grid 2 and it exchanges active and reactive power with it. As outline in Section 3.3, the Inverter control loop consists of a simple current control in the *dq* reference frame. Thus, the Inverter stage drives the power across the SST and therefore it is responsible for the SST power routing. The

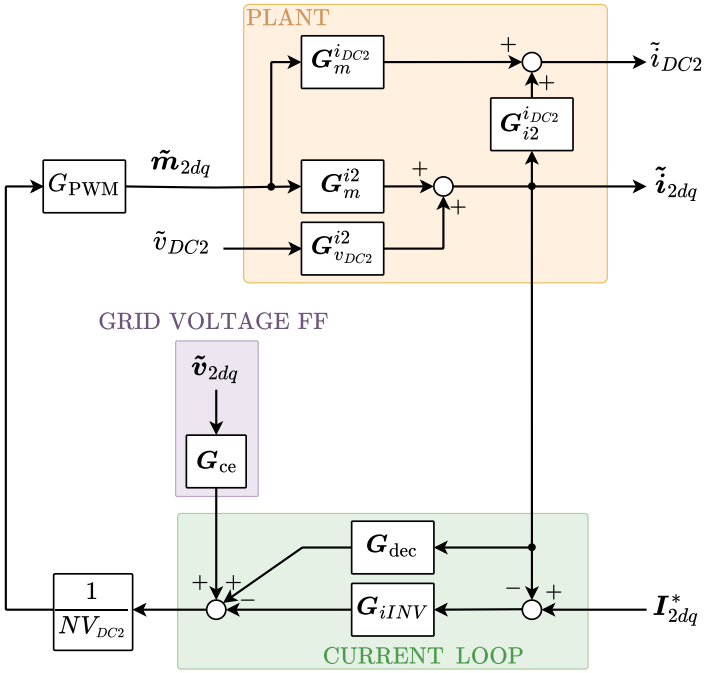


Figure 4.8: Inverter control block diagram.

Inverter small signal model is exactly the same presented for the AFE rectifier except for dc-link voltages being now input variables and no more state variables, as the voltage at MVdc-link2 is controlled by the DAB converters. For this reason, the small-signal plant derivation is omitted here as the procedure is the same given for the AFE stage. As for the AFE, the inverter control block diagram is derived based on both plant and control system and it is depicted in Fig. 4.8. The transfer functions $\boldsymbol{G}_{ce}$ and $\boldsymbol{G}_{PWM}$ are the same introduced for the AFE control diagram, while $\boldsymbol{G}_{dec}$ and $\boldsymbol{G}_{iINV}$ are:

$$\boldsymbol{G}_{\mathrm{dec}} = \begin{bmatrix} 0 & \omega L_2 \\ -\omega L_2 & 0 \end{bmatrix} \tag{4.27}$$

$$\boldsymbol{G}_{iINV} = \begin{bmatrix} K_{PiINV} + \dfrac{K_{IiINV}}{s} & 0 \\ 0 & K_{PiINV} + \dfrac{K_{IiINV}}{s} \end{bmatrix} \tag{4.28}$$

The plant transfer functions $\boldsymbol{G}_m^{i_{DC2}}$, $\boldsymbol{G}_m^{i_2}$, $\boldsymbol{G}_{v_{DC2}}^{i_2}$ and $\boldsymbol{G}_{i2}^{i_{DC2}}$ can be derived following the same procedure presented for the AFE converter.

The input impedance Z_{inINV}^{CL} is thus derived from the Inverter control block diagram

depicted in Fig. 9 and it is given as:

$$Z_{inINV}^{CL} = \left.\frac{\tilde{v}_{DC2i}}{\tilde{i}_{DC2}}\right|_{I_{2d}^*=I_{2q}^*=0} = \\ = \left(\frac{NV_{DC2}G_{v_{DC2}}^{i_{2d}}G_{i_{2d}}^{i_{DC2}} + G_{PWM}G_{iINV}G_{v_{DC2}}^{i_{2d}}G_{m_{2d}}^{i_{DC2}}}{NV_{DC2} - G_{PWM}G_{iINV}G_{m_{2d}}^{i_{2d}}} + \frac{NV_{DC2}G_{v_{DC2}}^{i_{2q}}G_{i_{2q}}^{i_{DC2}} + G_{PWM}G_{iINV}G_{v_{DC2}}^{i_{2q}}G_{m_{2q}}^{i_{DC2}}}{NV_{DC2} - G_{PWM}G_{iINV}G_{m_{2q}}^{i_{2q}}}\right)^{-1} \tag{4.29}$$

where $G_{i_{2d}}^{i_{DC2}}$, $G_{m_{2d}}^{i_{DC2}}$, $G_{i_{2q}}^{i_{DC2}}$ and $G_{m_{2q}}^{i_{DC2}}$ are DC-side Inverter transfer functions derived through its small-signal model given as:

$$G_{i_{2d}}^{i_{DC2}} = -\frac{M_{2d}}{2} \tag{4.30}$$

$$G_{m_{2d}}^{i_{DC2}} = -\frac{I_{2d}}{2} \tag{4.31}$$

$$G_{i_{2q}}^{i_{DC2}} = -\frac{M_{2q}}{2} \tag{4.32}$$

$$G_{m_{2q}}^{i_{DC2}} = -\frac{I_{2q}}{2} \tag{4.33}$$

4.2.3 DC-bus Impedance Model Validation

Table 4.1 shows the model parameters and the rated steady state values together with controller gains used to validate the transfer function equations (4.23), (4.24), (4.26) and (4.29) which were derived analytically in the previous subsections. The SST analyzed in this work has been simulated in MATLAB/Simulink with the parameters given in Table 4.1. The AFE closed-loop output impedance, the DAB closed-loop input and output impedances and the closed-loop Inverter input impedance were mapped through the controlled injection of perturbation sinusoidal signals at given frequencies covering the range 0.01 Hz - 5 kHz. The comparison between the impedances derived analytically and the ones obtained from the frequency response is reported in Fig. 10. Considering the AFE and DAB output impedances, represented in Fig. 4.9a and Fig. 4.9c, the low impedance value at low frequencies depends on the high gain of the voltage controller (GVC in case of the AFE rectifier) in the same region, while the frequency value at which the impedance slope changes correspond to the voltage control bandwidth. Above that frequency, the dc-link capacitor affects the impedance magnitude, which falls at a rate of -20 dB/decade. Regarding the DAB and Inverter Input impedances, shown in Fig. 4.9b and Fig. 4.9d, the low frequency impedance gains is influenced by the feedback effect and by the component

Table 4.1: SST system parameters used for the DC-bus stability analysis of the SST.

Symbol	Value	Symbol	Value
V_1, V_2 (RMS)	1.9 kV	M_{1q}, M_{2q}	0
f	50 Hz	n	1
L_2, L_2	2 mH	f_{sD}	12 kHz
R_1, R_2	0.5 Ω	L_t	45 μH
I_{1d}, I_{2d}	118,-118 A	D	0.1
I_{1d}, I_{2d}	0 A	$K_{Pv}, K_{Iv}\,(G_V)$	0.022, 0.738
C_1, C_2	8 mF	$K_{Pi}, K_{Ii}\,(G_I)$	6.3, 9057
V_{DC1}, V_{DC2}	756 V	$K_{PiINV}, K_{IiINV}\,(G_{iINV})$	6.3, 9057
M_{1d}, M_{2d}	0.88	$K_{Pdab,v}, K_{Idav,v}\,(G_{vDAB})$	0.02, 8.126

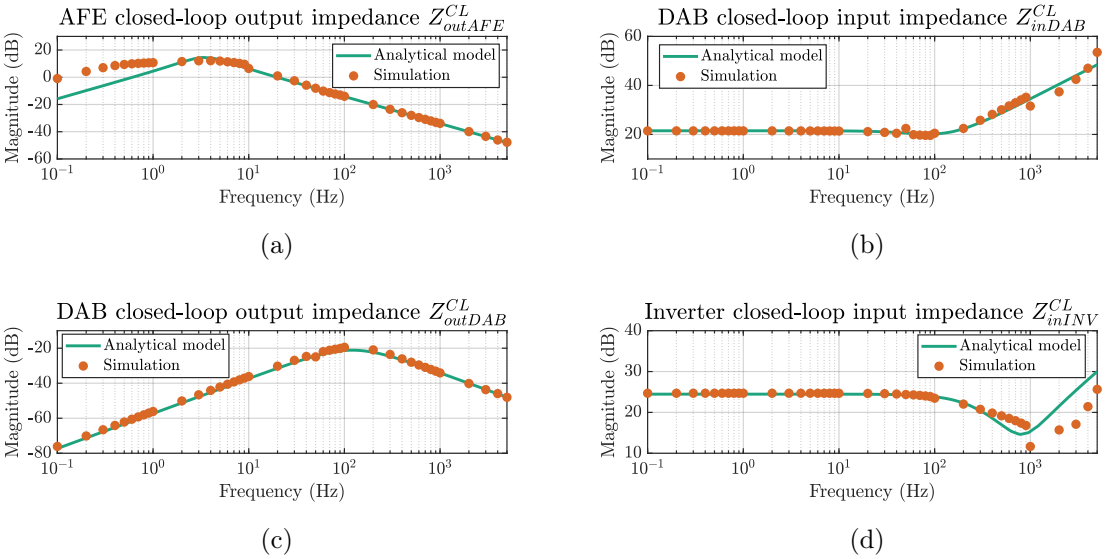


Figure 4.9: Validation of the analytical impedance model derived in this Section through time-domain simulations. (a) AFE output impedance, (b) DAB input impedance, (c) DAB output impedance, (d) Inverter input impedance.

values and rated conditions at which the DAB and Inverter are designed. The change in the impedance slope occurs instead at the frequency corresponding to the bandwidth of the voltage controller for the DAB impedance and of the dq current controller for the Inverter impedance. The high frequency slope of the impedances depends on the influence of the dc-link capacitor C2 for the DAB impedance whereas on the Grid 2 line filter for the Inverter impedance transfer function. SST system parameters used for the DC-bus stability analysis of the SST.

4.2.4 DC-bus Stability Assessment

In this section, the stability issue of the proposed SST converter is discussed. The aim is to point out how the controllers and the operating conditions affect the SST stability. As can be noted from the converter transfer functions and thus from the small signal models derived previously, the system stability is influenced by the parameters selection, the steady state values defined by the operating conditions and by the controllers tuning. Assuming that the parameters selection has been done to achieve a desired converter design and performances, the stability analysis discussed here takes into account only the effect of the voltage controllers and of the relevant operating modes. The rated values and parameters of the converter, which was simulated in Simulink, are given in Table

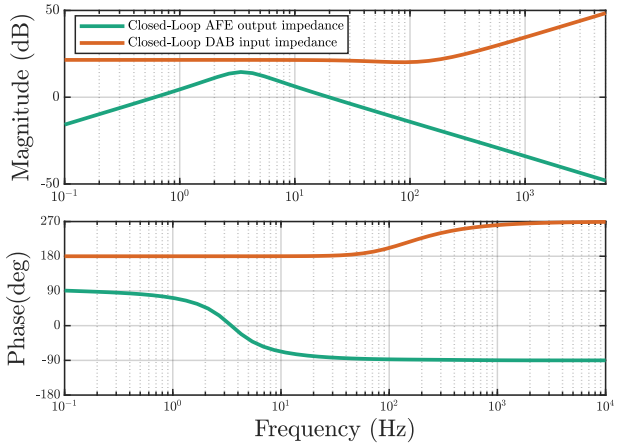
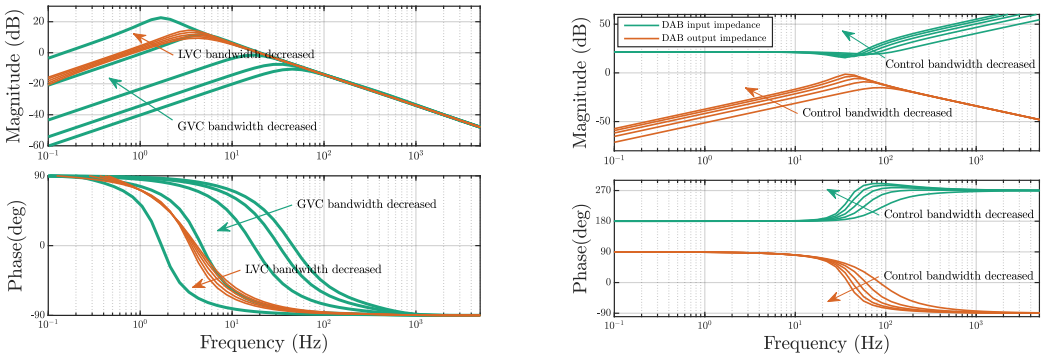


Figure 4.10: AFE output impedance and DAB input impedance under the stable rated scenario given in Table 4.1.

Table 4.2: Case studies for the DC-bus stability assessment of the SST under investigation.

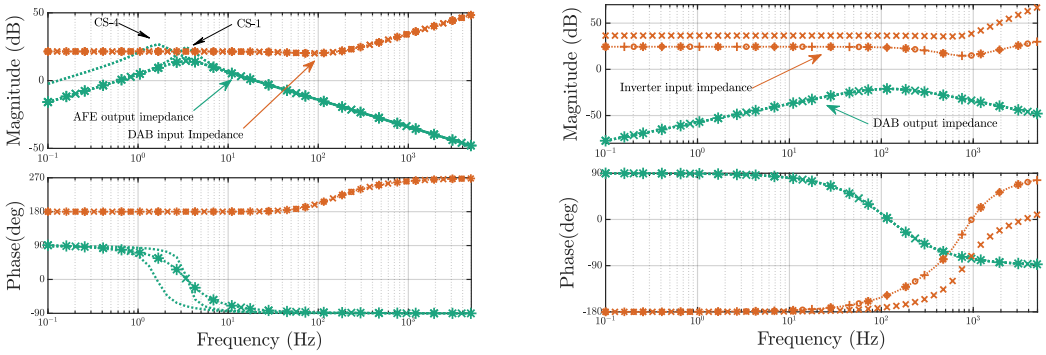
Case Study	Parameters of interest	Value
CS-1	I_{1d}, I_{2d}	-118,+118 A
CS-2	I_{1q}	+118 A
CS-3	I_{1q}	-118 A
CS-4	M_{1d}, M_{2d}	0.2

4.1. For these values, the SST is stable as shown in Fig. 4.10, since the Middlebrook criterion is satisfied for both MVdc-link interfaces. Fig. 4.11a shows how the change in GVC and LVC bandwidth for the AFE influence the impedances shape. The same comparison for the DAB converter is made in Fig. 4.11b as the voltage control bandwidth changes. When the voltage controls bandwidth decreases, the PI controllers proportional gain decreases and the system become more unstable due to slow response of the control to a perturbation, which may cause the system quantities to diverge. This appears as an increase in magnitude for the AFE and DAB output impedances. Regarding the impact of the operating modes on the converter stability, the direction of the power flow, the exchange of reactive power and the low voltage mode are relevant case studies, which may cause instability in the SST converter investigated. This is because, as can be seen from the small signal models discussed in Section III, the steady state variables, which may influence the converter impedances and hence the system stability, are mainly the direct and quadrature steady state component of the grid currents I_{1d}, I_{2d}, I_{1q} and I_{2q} and the direct steady state component of the modulation index M_{1d} and M_{2d}. Thus, based on the rated values given in Table 4.1, four case studies to be analyzed are defined in Table 4.2. For each case study, it is indicated a new value for the parameters of interest, while the other parameters remain those expressed in Table 4.1. Fig. 4.12a and Fig. 4.12b show the new impedances shape for the case studies given in Table 4.2. As can be noted in Fig. 4.12a, the DAB input impedance is not sensitive to a change in operation mode for the SST, while in the case of the AFE, the output impedance rises in case studies CS-1 and CS-4 whereas the case studies CS-2 and CS-3 do not affect in any sense the AFE output



(a) (b)

Figure 4.11: (a) influence of the GVC and LVC loops on the AFE output impedance; (b) variation of the DAB impedances depending on the DAB control bandwidth changes.

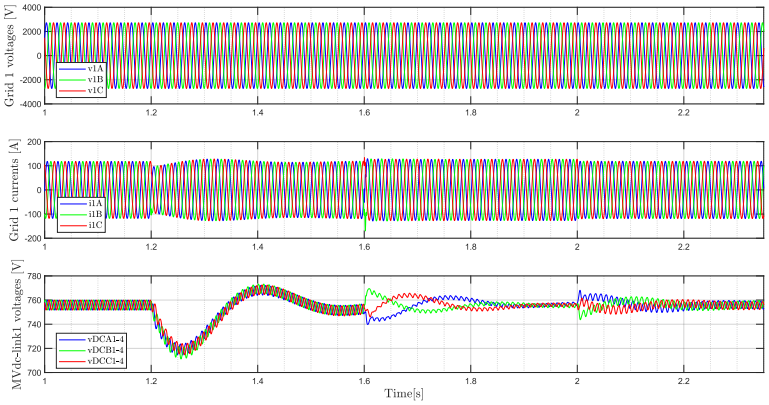


(a) (b)

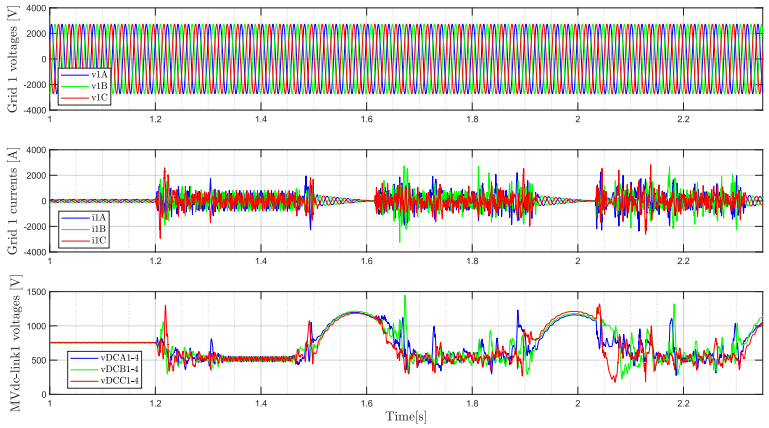
Figure 4.12: Variation of the SST impedance under different operating scenarios given in Table II. Different line styles identify the four different operating scenarios. (a) AFE output and DAB input impedances, (b) DAB output and Inverter input impedances.

impedance. Thus, the direction of the power flow and the voltage rating at which the SST operates may cause instability in the system. Meanwhile, as Fig. 4.12b shows, the DAB output impedance and the Inverter input impedance are not affected by the operation mode expect for the case study CS-4, in which the lower steady state direct component of the modulation index causes an increase in the Inverter input impedance magnitude, which however increases the system stability at the MVdc-link2 interface. To validate this analysis, the SST model was simulated with the parameters given in Table 4.1 as

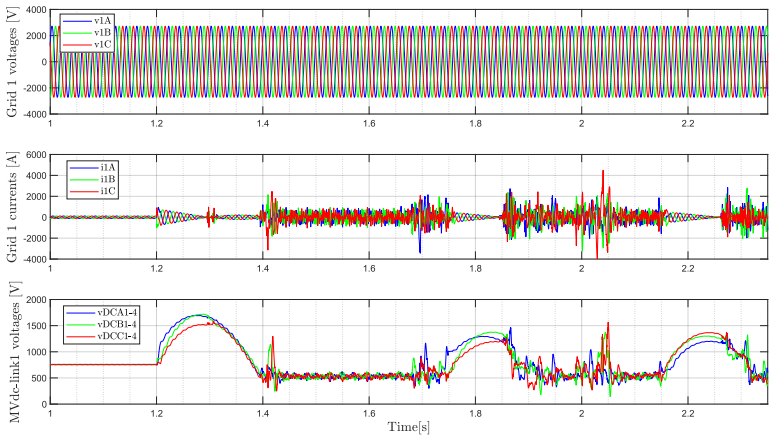
the case of stable system, and with the parameters given in Table 4.2 for the unstable scenarios CS-1 and CS-4. Fig. 4.13a shows the stable operation of the converter at the Port 1. At t = 1.2 s the active power absorbed by the SST from Grid 1 is reduced from about 470 kW to 370 kW, while at t = 1.6 s and t = 2 s the reactive power is set to be -185 kVAr and +140 kVAr respectively. As the figure shows, the system is stable and the voltage balancing loop works well. Fig. 4.13b and Fig. 4.13c demonstrate how the system becomes unstable under the scenario CS-1 when the power flow is reversed and in case of the scenario CS-4 when the converter operates at low modulation index. In this case, the voltage control fails to track the reference values and the dc-link voltages highly oscillate.



(a)



(b)



(c)

Figure 4.13: Simulation results of (a) stable operating scenario, (b) unstable CS-1 scenario and (c) unstable CS-4 scenario.

4.2.5 Discussion

In this Section, the dc-LINK stability issue of a Triple-stage three-phase ISOS connected SST based on the CHB and DAB topologies has been assessed using the Middlebrook's criterion. A small signal model of the converter and its control system has been presented, through which the relevant impedance transfer functions for the stability analysis have been derived and verified in simulation. The stability has then been discussed and it was pointed out that the direction of the power flow and the voltage rating at which the SST works may be sources of instability. These results have finally been validated through simulation. The presented analysis represents a good design tool for the discussed SST topology and its control system. The impedance models presented here can be used, combined with the optimal design of the converter, to define the rated conditions of operation for this SST topology and thus defining the passive elements values, together with the control system tuning

4.3 Impedance-based Grid-Connection Stability Analysis

As a result of the extensive and increasing integration of power electronic-based systems, the stability of modern power grids faces significant challenges. The multi-timescale nature of modern power electronic converter control systems can lead to dynamic interactions with the grid, resulting in local instabilities in the power system, i.e. voltage and current oscillations, harmonic and sub-harmonic instability and interactions and resonances phenomena over a wide frequency range. [120, 123, 132]. These phenomena originate as small-signal oscillations due to the existence of a negative (or poor) damping in the power system, provoking the so-called harmonic instability [120]. Depending on the specific control loop, the oscillations may happen on a very broad frequency range [120, 123, 133]. It has been widely reported in literature how the constant-power load (CPL) control of rectifiers introduces a negative incremental resistance region on the converter d-axis input impedance Z_{dd} within the dc-link voltage control bandwidth [123, 134]. Therefore the faster the dc-link controller the wider is the negative conductance region of Z_{dd}. Low frequency instabilities can also be introduced on the q-axis input impedance Z_{qq} by phase-locked loop (PLL) in case of inverter mode [123, 135, 136]. In this case the negative resistance region extends within PLL bandwidth. Either of these instabilities are low frequency phenomena narrowed nearby the sub- and near-synchronous frequency range [120, 123, 134, 135]. With regard to the high frequency range, the time delay introduced by digital controllers and the frequency-coupling introduced by the modulator may be sources of instabilities [120, 123, 133]. Therefore, the stability assessment of grid-connected voltage-source converter (VSC) is becoming more and more essential to identify and analyze the converter-grid interactions in modern power systems. One effective way to assess the interconnection stability of a VSC is by means of the passivity properties of its input impedance [123, 133, 137]. This is because oscillations due to critical resonances at a certain frequency cannot be established if the converter has nonnegative input conductance at that frequency, i.e. the input impedance is passive, because the power is dissipated. Thus, knowing the converter input impedance properties is a useful tool that can be used to properly design the VSC control systems to prevent instability [123, 133, 137].

Although the grid-connection issue of single-stage ac-dc converter topologies has already been widely discussed in the literature, really poor attention has been posed to cascaded topologies such as ac-dc-dc isolated systems, that are nowadays widely used in many applications as for example in Solid-State Transformer (SST) applications [138].

To the author's best knowledge, in literature only [139] and [140] have recently derived the impedance model of a cascaded two-stage topology and addressed the stability issue from the grid-interaction point of view. The work presented in [139] analyzes the impact of a non-isolated cascaded dc-dc converter on a front-end power factor correction (PFC) converter's dq impedance. However, the impedance properties under different operating modes has not been assessed. Authors in [140] proposed a two-stage DAB-based interfacing a BESS with the grid, in which an input impedance model is also derived. However, the paper only deals with the converter working principle and the stability issue is just pointed out and not discussed at all.

The aim of the analysis carried out in this Section is to fill the aforementioned literature gap by deriving the dq input impedance expressions for a SST topology based on the aforementioned isolated bidirectional ac-dc-dc building block, and then by showing the effect of the dc-dc stage on the SST input impedance. For this purpose, first the SST dq impedance model is derived - based on the dq-frame small signal model - considering the dc-dc converter impact. Then, the impedance model is verified by means of time-domain simulations. Finally, SST dq input impedance is analyzed and the effect of the cascaded topology on its shapes is highlighted and discussed (in comparison to single stage topology), with particular emphasis on the low frequency passivity properties of the d-axis Z_{dd}.

4.3.1 System Description and Impedance Model Derivation

For the grid-connection stability assessment of the SST, the simplified topology shown in Fig. 4.14 is considered, in which the Inverter stage is represented either as a pure resistive load or an active one, depending on the power flow. This is done to make the analysis more genera and to simplify the equations used in this Section. The input side connection of the circuit shown in Fig. 4.14 is of the input-series (IS) type, while the output side of the circuit is intentionally left unconnected to keep the impedance analysis as general

as possible, i.e. the SST output side can be connected either in output-series (OS) or in output-parallel (OP) type, and the load connected can be a purely passive one, an active one such as a battery or a BESS or it can be either another converter. This is because, as will be shown later in this section, the dc-dc converter small-signal model will be derived assuming the output side of the DAB connected to a purely resistive load in the case of a direct power flow (DPF) (from the AFE to the load) or to a dc voltage source in the case of reverse power flow (RPF) (from the source to the AFE). Thus, no matter what the load connected downstream of the DAB, it can be assumed to be a resistive load or an active source according to the power flow. Fig. 4.15 shows the control diagram of the grid-connected SST system [141]. Note that, for the analysis carried out in this section, the nomenclature used in equations follows the one shown in Fig. 4.15. As explained in Section 3.3, the AFE control is implemented in the synchronous dq-frame and the synchronization with the grid is achieved through a PLL. The AFE control is responsible of the grid power flow control together with the regulation of its dc-link voltages ($v_{\mathrm{dc,i}}$). Instead, the dc-dc converter regulates the output dc-link voltage $v_{\mathrm{dc,o}}$ in the case of DPF or the output current $i_{\mathrm{dc,o}}$ in the case of RPF [141, 142].

In this Section, the closed-loop input impedance $\boldsymbol{Z}_{\mathrm{inCL}}$ expression of the cascaded topology of Fig. 4.14 is determined by firstly deriving the AFE rectifier impedance model. In this case, it is supposed that the load connected at the dc-side of the converter is a generic resistor. For this purpose, the real dq-frame is employed to derive a

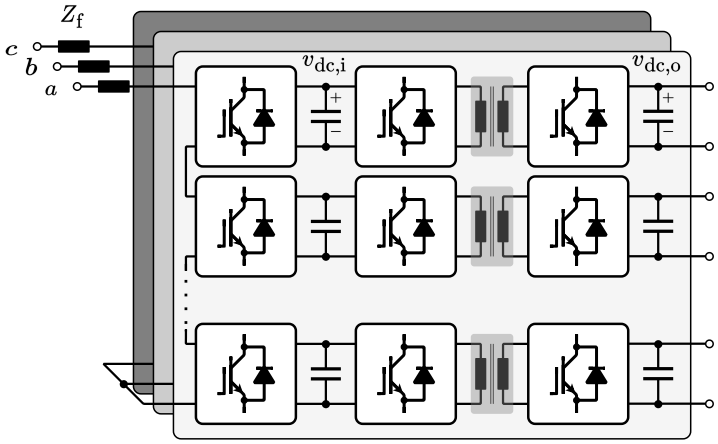


Figure 4.14: Simplified CHB- and DAB-based SST architecture considered for the grid-connection stability analysis.

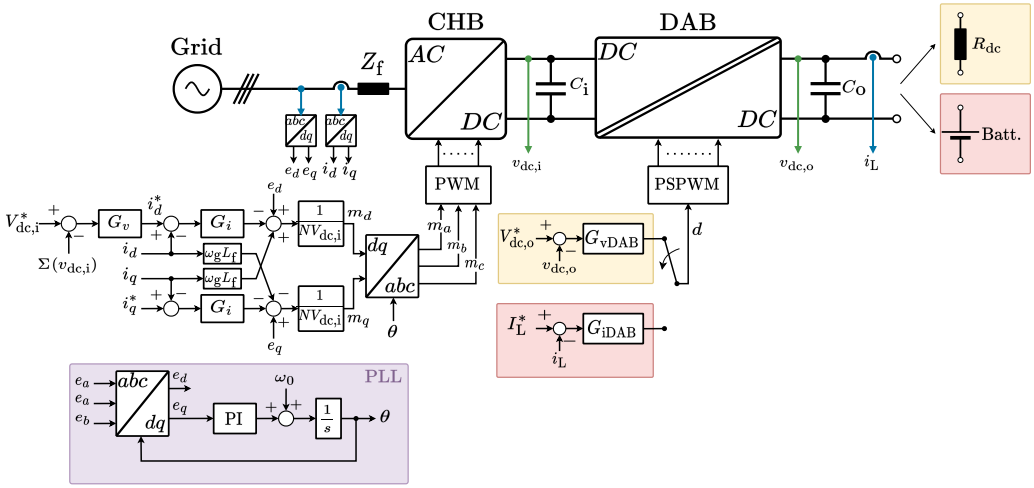


Figure 4.15: Simplified grid-connected control block diagram considered for the grid-connection stability analysis of the SST.

linear time-invariant (LTI) multi-input multi-output (MIMO) system [143, 144]. Then, when considering the dynamics of the cascaded topology, the generic resistor will be replaced with the input impedance of the DAB, that is also derived in this Section. In the following, boldface capital letters are used to denote transfer function matrices while boldface lowercase ones to denote vectors.

Active Front-End Rectifier Modeling

The impedance model of the grid-connected multilevel AFE rectifier represented in Fig. 4.14 is derived based on the dq-frame average model of the converter, already presented in Section 3.3.1, and here reporter for clarity of the text:

$$\begin{cases} L_\mathrm{f}\frac{di_d}{dt} = e_d - R_\mathrm{f} i_d + \omega_\mathrm{g} L_\mathrm{f} i_q - N m_d v_{\mathrm{dc,i}} \\ L_\mathrm{f}\frac{di_q}{dt} = e_q - R_\mathrm{f} i_q - \omega_\mathrm{g} L_\mathrm{f} i_d - N m_q v_{\mathrm{dc,i}} \\ C_\mathrm{i}\frac{dv_{\mathrm{dc,i}}}{dt} = \frac{1}{2}\left(m_d i_d + m_q i_q\right) - \frac{v_{\mathrm{dc,i}}}{R_{\mathrm{dc,i}}} \end{cases} \tag{4.34}$$

where R_f, L_f and C_i are the line filter resistance and inductance and the AFE submodule capacitance, N is the number of submodules per phase, ω_g is the grid angular frequency, $v_{\mathrm{dc,i}}$ is the submodule dc voltage, $i_{d,q}$, $e_{d,q}$ and $m_{d,q}$ are respectively the line currents, the grid voltages and the AFE modulation indexes in the dq-frame, while $R_{\mathrm{dc,i}}$ is the generic load resistor connected to the dc side of each submodule. Note that the model in

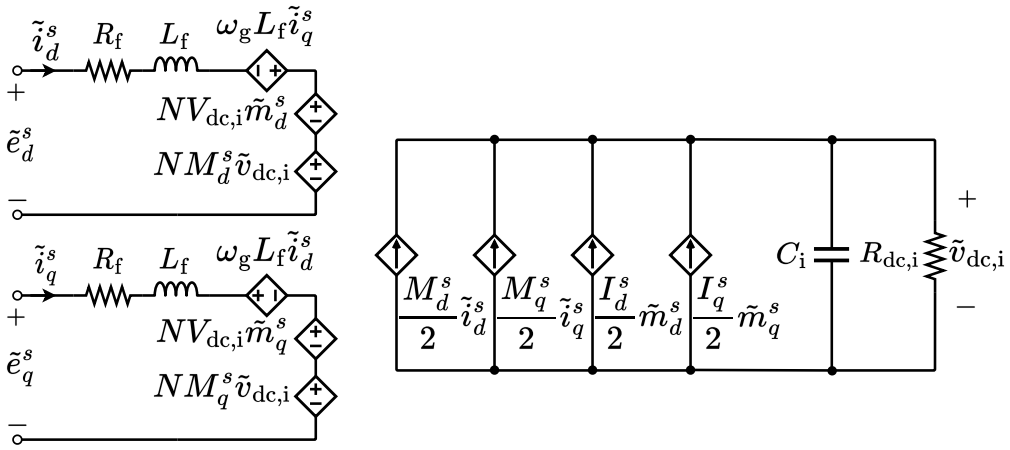


Figure 4.16: AFE dq small-signal model circuit representation [141, 146].

(4.34) has been derived assuming that the dc voltage of the CHB cells are all equal and considering the amplitude-invariant Park transformation matrix [141, 145].

By perturbing the model in (4.34) and linearizing around the steady-state operating points (neglecting the second order terms), the AFE dq small-signal model is obtained as [141]:

$$\begin{cases} L_\mathrm{f} \frac{d\tilde{i}_d}{dt} = \tilde{e}_d - R_\mathrm{f} \tilde{i}_d + \omega_\mathrm{g} L_\mathrm{f} \tilde{i}_q - NV_{\mathrm{dc,i}} \tilde{m}_d - NM_d \tilde{v}_{\mathrm{dc,i}} \\ L_\mathrm{f} \frac{d\tilde{i}_q}{dt} = \tilde{e}_q - R_\mathrm{f} \tilde{i}_q - \omega_\mathrm{g} L_\mathrm{f} \tilde{i}_d - NV_{\mathrm{dc,i}} \tilde{m}_q - NM_q \tilde{v}_{\mathrm{dc,i}} \\ C_\mathrm{i} \frac{d\tilde{v}_{\mathrm{dc,i}}}{dt} = \frac{1}{2} \left(M_d \tilde{i}_d + M_q \tilde{i}_q \right) + \frac{1}{2} \left(I_d \tilde{m}_d + I_q \tilde{m}_q \right) - \frac{\tilde{v}_{\mathrm{dc,i}}}{R_{\mathrm{dc,i}}} \end{cases} \tag{4.35}$$

where the variable capital letters identifies the steady-state values. The steady state values of i_d, m_d and m_q in (4.35) are derived solving (4.34) and considering I_q and E_q equal to zero (meaning null reactive power exchange and perfect steady-state grid synchronization), leading to:

$$\begin{cases} I_d = \dfrac{E_d - \sqrt{E_d^2 - \frac{8NR_\mathrm{f}V_{\mathrm{dc,i}}^2}{R_{\mathrm{dc,i}}}}}{2R_\mathrm{f}} \\ M_d = \dfrac{4R_\mathrm{f}V_{\mathrm{dc,i}}}{R_{\mathrm{dc,i}} \left(E_d - \sqrt{E_d^2 - \frac{8NR_\mathrm{f}V_{\mathrm{dc,i}}^2}{R_{\mathrm{dc,i}}}} \right)} \\ M_q = -\dfrac{\omega_\mathrm{g} L_\mathrm{f} \left(E_d - \sqrt{E_d^2 - \frac{8NR_\mathrm{f}V_{\mathrm{dc,i}}^2}{R_{\mathrm{dc,i}}}} \right)}{2NR_\mathrm{f}V_{\mathrm{dc,i}}} \end{cases} \tag{4.36}$$

where E_d equals the amplitude of the grid voltage e.

Based on (4.35), the AFE small-signal model is represented in Fig. 4.16. The su-

perscript s it is used to denote the system frame, i.e. the grid dq frame. It must be distinguished from the control dq frame that is defined by the PLL angle θ [123, 136]. In steady-state, owing to a perfect grid synchronization, these two frames coincide.

Fig. 4.17 shows the grid-connected AFE control block diagram based on the control system reported in Fig. 4.15. The yellow box identifies the open-loop small signal model of the AFE, where where $\tilde{\boldsymbol{i}}^s_{dq} = [\tilde{i}^s_d \ \tilde{i}^s_q]^T$, $\tilde{\boldsymbol{e}}^s_{dq} = [\tilde{e}^s_d \ \tilde{e}^s_q]^T$ and $\tilde{\boldsymbol{m}}^s_{dq} = [\tilde{m}^s_d \ \tilde{m}^s_q]^T$. Based on that, it is possible to define the following open-loop transfer functions:

$$\boldsymbol{Z}_{\text{inOL}} = \boldsymbol{Z}_{\text{rl}} + N\frac{Z_{\text{rc}}}{2}\begin{bmatrix} M_d^{s2} & M_d^s M_q^s \\ M_d^s M_q^s & M_q^{s2} \end{bmatrix} \tag{4.37}$$

$$\boldsymbol{G}_m^i = -N\boldsymbol{Z}_{\text{inOL}}^{-1}\left(\frac{Z_{\text{rc}}}{2}\begin{bmatrix} M_d^s \\ M_q^s \end{bmatrix}\begin{bmatrix} I_d^s & I_q^s \end{bmatrix} + \begin{bmatrix} V_{\text{dc,i}} & 0 \\ 0 & V_{\text{dc,i}} \end{bmatrix}\right) \tag{4.38}$$

$$\boldsymbol{G}_e^{v_{\text{dc}}} = \frac{\frac{Z_{\text{rc}}}{2}\begin{bmatrix} M_d^s & M_q^s \end{bmatrix}\boldsymbol{Z}_{\text{rl}}^{-1}}{1 + N\left(\frac{Z_{\text{rc}}}{2}\begin{bmatrix} M_d^s & M_q^s \end{bmatrix}\boldsymbol{Z}_{\text{rl}}^{-1}\begin{bmatrix} M_d^s \\ M_q^s \end{bmatrix}\right)} \tag{4.39}$$

$$\boldsymbol{G}_m^{v_{\text{dc}}} = \frac{\frac{Z_{\text{rc}}}{2}\left(\begin{bmatrix} I_d^s & I_q^s \end{bmatrix} - NV_{\text{dc,i}}\begin{bmatrix} M_d^s & M_q^s \end{bmatrix}\boldsymbol{Z}_{\text{rl}}^{-1}\right)}{1 + N\left(\frac{Z_{\text{rc}}}{2}\begin{bmatrix} M_d^s & M_q^s \end{bmatrix}\boldsymbol{Z}_{\text{rl}}^{-1}\begin{bmatrix} M_d^s \\ M_q^s \end{bmatrix}\right)} \tag{4.40}$$

where $I^s_{d,q} = I_{d,q}$, $M^s_{d,q} = M_{d,q}$ as defined previously in this Section, and:

$$\boldsymbol{Z}_{\text{rl}} = \begin{bmatrix} R_{\text{f}} + sL_{\text{f}} & -\omega_{\text{g}}L_{\text{f}} \\ \omega_{\text{g}}L_{\text{f}} & R_{\text{f}} + sL_{\text{f}} \end{bmatrix} \tag{4.41}$$

$$Z_{\text{rc}} = \frac{R_{\text{dc,i}}}{1 + sC_{\text{i}}R_{\text{dc,i}}} \tag{4.42}$$

Equations (4.37)-(4.40) describe the system plant. Also, note that (4.37) is the open-loop input impedance matrix of the multilevel AFE. To derive the closed-loop input impedance matrix $\boldsymbol{Z}_{\text{inCL}}$ under both current and voltage controllers, it is necessary to introduce a set of transfer functions that model the PLL effect on the closed-loop converter dynamics. These transfer functions are the ones located inside the purple box of Fig. 4.17. They account for the PLL effect on the feedback current vector $\tilde{\boldsymbol{i}}^c_{dq}$, the PCC voltage feedforward (FF) vector $\tilde{\boldsymbol{e}}^c_{dq}$ and on the system modulation index vector $\tilde{\boldsymbol{m}}^s_{dq}$ [123, 136].

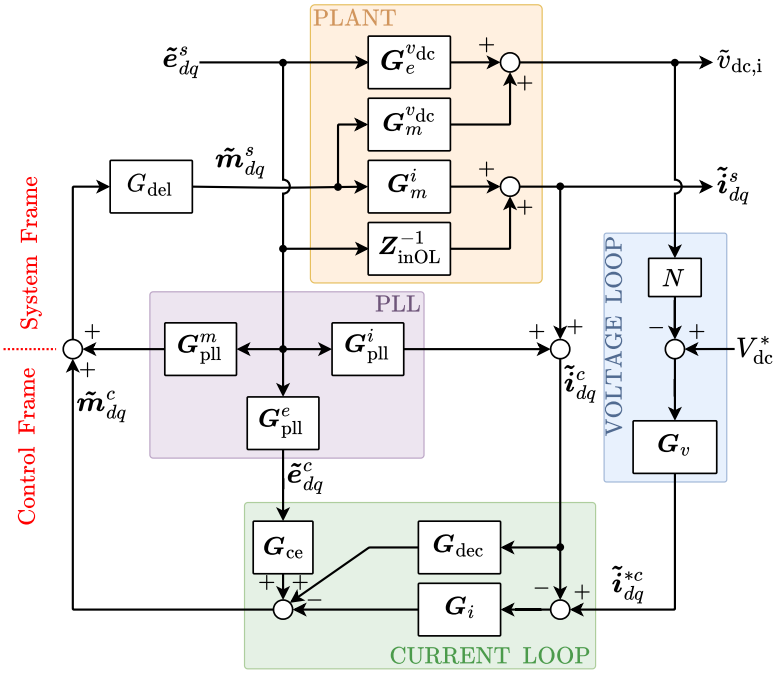


Figure 4.17: AFE control block diagram [141, 146].

Those are defined as [123, 136]:

$$\boldsymbol{G}^e_{\text{pll}} = \begin{bmatrix} 1 & E^s_q G_{\text{pll}} \\ 0 & 1 - E^s_d G_{\text{pll}} \end{bmatrix} \tag{4.43}$$

$$\boldsymbol{G}^i_{\text{pll}} = \begin{bmatrix} 0 & I^s_q G_{\text{pll}} \\ 0 & -I^s_d G_{\text{pll}} \end{bmatrix} \tag{4.44}$$

$$\boldsymbol{G}^m_{\text{pll}} = \begin{bmatrix} 0 & -M^c_q G_{\text{pll}} \\ 0 & M^c_d G_{\text{pll}} \end{bmatrix} \tag{4.45}$$

where:

$$\boldsymbol{G}_{\text{pll}} = \frac{T_{\text{pll}}}{s + E^s_d T_{\text{pll}}} \tag{4.46}$$

$$T_{\text{pll}} = K_{\text{Ppll}} + \frac{K_{\text{Ipll}}}{s} \tag{4.47}$$

in which K_{Ppll} and K_{Ipll} are respectively the proportional and integral gains of the PLL PI controller.

The remaining transfer functions that need to be introduced before deriving the input impedance analytical expression are the voltage controller $\boldsymbol{G}_v$, the dq-frame current controller $\boldsymbol{G}_i$, and the current decoupling, the modulation effect on the PCC voltage

FF and digital control system delay matrices $\boldsymbol{G}_{\text{dec}}$, $\boldsymbol{G}_{\text{ce}}$ and $\boldsymbol{G}_{\text{del}}$. These are defined as follow [134, 146]:

$$\boldsymbol{G}_v = \begin{bmatrix} K_{\text{Pv}} + \frac{K_{\text{Iv}}}{s} \\ 0 \end{bmatrix} \tag{4.48}$$

$$\boldsymbol{G}_i = \frac{1}{NV_{\text{dc,i}}} \begin{bmatrix} K_{\text{Pi}} + \frac{K_{\text{Ii}}}{s} & 0 \\ 0 & K_{\text{Pi}} + \frac{K_{\text{Ii}}}{s} \end{bmatrix} \tag{4.49}$$

$$\boldsymbol{G}_{\text{dec}} = \frac{1}{NV_{\text{dc,i}}} \begin{bmatrix} 0 & \omega_{\text{g}} L_{\text{f}} \\ -\omega_{\text{g}} L_{\text{f}} & 0 \end{bmatrix} \tag{4.50}$$

$$\boldsymbol{G}_{\text{ce}} = \frac{1}{NV_{\text{dc,i}}} \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \tag{4.51}$$

$$\boldsymbol{G}_{\text{del}} = \begin{bmatrix} e^{-sT_{\text{d}}} & 0 \\ 0 & e^{-sT_{\text{d}}} \end{bmatrix} \tag{4.52}$$

where [131]:

$$T_{\text{d}} = 1.5T_{\text{sw}} = \frac{3}{2f_{\text{sw}}} \tag{4.53}$$

in which f_{sw} is the switching frequency of the AFE.

It is now possible to define the closed-loop input impedance of the grid-connected AFE by solving the control block diagram of Fig. 4.17. By firstly considering only the closed-loop current control, the AFE dq input impedance $\boldsymbol{Z}_{\text{inCL,i}}$ is derived as (4.54):

$$\begin{aligned} \boldsymbol{Z}_{\text{inCL},i} = \tilde{\boldsymbol{v}}^s_{dq}(\tilde{\boldsymbol{i}}^s_{dq})^{-1} = \big[{\boldsymbol{Z}_{\text{inOL}}}^{-1} + \boldsymbol{G}^i_m \boldsymbol{G}_{\text{del}} \big(\boldsymbol{G}_{\text{ce}} \boldsymbol{G}^e_{\text{pll}} + (\boldsymbol{G}_{\text{dec}} + \boldsymbol{G}_i)\boldsymbol{G}^i_{\text{pll}} + \boldsymbol{G}^m_{\text{pll}}\big)\big]^{-1} \\ \big(\boldsymbol{I}_2 - \boldsymbol{G}^i_m \boldsymbol{G}_{\text{del}} (\boldsymbol{G}_{\text{dec}} + \boldsymbol{G}_i)\big) \end{aligned} \tag{4.54}$$

Finally, considering also the closed-loop voltage control, the AFE closed-loop input impedance matrix $\boldsymbol{Z}_{\text{inCL}}$ is obtained in (4.55):

$$\begin{aligned} \boldsymbol{Z}_{\text{inCL}} = \tilde{\boldsymbol{v}}^s_{dq}(\tilde{\boldsymbol{i}}^s_{dq})^{-1} = \big[\boldsymbol{Z}^{-1}_{\text{inOL}} + \boldsymbol{G}^i_m \left(\boldsymbol{I}_2 - \boldsymbol{G}_{\text{del}} (\boldsymbol{G}_i \boldsymbol{G}_v N \boldsymbol{G}^{v_{\text{dc}}}_m)\right)^{-1} \boldsymbol{G}_{\text{del}} \big(\boldsymbol{G}_{\text{ce}} \boldsymbol{G}^e_{\text{pll}} + \\ (\boldsymbol{G}_{\text{dec}} + \boldsymbol{G}_i)\boldsymbol{G}^i_{\text{pll}} + \boldsymbol{G}_i \boldsymbol{G}_v N \boldsymbol{G}^{v_{\text{dc}}}_m + {\boldsymbol{G}^m_{\text{pll}}}^{-1} \cdot \\ \cdot \big[\boldsymbol{I}_2 - \boldsymbol{G}^i_m \left(\boldsymbol{I}_2 - \boldsymbol{G}_{\text{del}} (\boldsymbol{G}_i \boldsymbol{G}_v N \boldsymbol{G}^{v_{\text{dc}}}_m)\right)^{-1} \boldsymbol{G}_{\text{del}} \left(\boldsymbol{G}_{\text{dec}} + \boldsymbol{G}_i\right)\big] \end{aligned} \tag{4.55}$$

Dual Active Bridge Modeling

A simple reduced order small-signal model for the DAB can be derived from the power equation of the converter [141,142]. Adopting the single phase-shift modulation technique, the average active power transferred through the DAB leakage inductor L_{t} during one switching cycle T_{sd} is given by:

$$P = \frac{V_{\mathrm{dc,i}} V_{\mathrm{dc,o}}}{2 n f_{\mathrm{sd}} L_{\mathrm{t}}} d\,(1 - |d|) \tag{4.56}$$

where n, f_{sd} and d are respectively the high-frequency transformer (HFT) turn ratio, DAB switching frequency and the rated phase-shift ratio. By perturbing and linearizing (4.56), the small signal model of the DAB is derived as follow:

$$\begin{cases} \tilde{i}_{\mathrm{dc,i}} = G_d^{i_{\mathrm{i}}} \tilde{d} + G_{v_{\mathrm{o}}}^{i_{\mathrm{i}}} \tilde{v}_{\mathrm{dc,o}} = \frac{V_{\mathrm{dc,o}}(1-2D)}{2 n f_{\mathrm{sd}} L_{\mathrm{t}}} \tilde{d} + \frac{D(1-2D)}{2 n f_{\mathrm{sd}} L_{\mathrm{t}}} \tilde{v}_{\mathrm{dc,o}} \\ \tilde{i}_{\mathrm{dc,o}} = G_d^{i_{\mathrm{o}}} \tilde{d} + G_{v_{\mathrm{i}}}^{i_{\mathrm{o}}} \tilde{v}_{\mathrm{dc,o}} = \frac{V_{\mathrm{dc,i}}(1-2D)}{2 n f_{\mathrm{sd}} L_{\mathrm{t}}} \tilde{d} + \frac{D(1-2D)}{2 n f_{\mathrm{sd}} L_{\mathrm{t}}} \tilde{v}_{\mathrm{dc,i}} \end{cases} \tag{4.57}$$

where D is the steady-state rated phase-shift ratio. Based on (4.57), Fig. 4.18 shows the circuit representation of the DAB small-signal, where i_{L} is the current to the output load connected to the DAB. Based on the control scheme given in Fig. 4.15, two different control block diagrams can be developed for the DAB, depending on the power flow direction. Fig. 4.19 shows the DAB control block diagram in the case of DPF, where a passive load is connected to the output side of the DAB. Instead, Fig. 4.20 shows the control block diagram in the case of RPF scenario, in which an active load is connected. In the previous, G_{vDAB}, G_{iDAB} and Z_{rcDAB} are respectively the DAB voltage controller, DAB currrent controller and DAB output impedance defines as:

$$G_{\mathrm{vDAB}} = K_{\mathrm{Pdab,v}} + \frac{K_{\mathrm{Idab,v}}}{s} \tag{4.58}$$

$$G_{\mathrm{iDAB}} = K_{\mathrm{Pdab,i}} + \frac{K_{\mathrm{Idab,i}}}{s} \tag{4.59}$$

$$Z_{\mathrm{rcDAB}} = \frac{R_{\mathrm{dc,o}}}{1 + s C_{\mathrm{o}} R_{\mathrm{dc,o}}} \tag{4.60}$$

while $R_{\mathrm{dc,o}}$ is the output load. Note that, in both cases, $R_{\mathrm{dc,o}}$ models the power absorbed/generated by the passive/active load (and thus $R_{\mathrm{dc,o}}$ is positive in the former case while it is negative in the latter).

Thus, from Fig. 4.19 and 4.20, the DAB closed loop input impedance $Z_{\mathrm{inCL,DAB}}$, defined as the ratio between $\tilde{v}_{\mathrm{dc,i}}$ and $\tilde{i}_{\mathrm{dc,i}}$, can be derived under the two different control

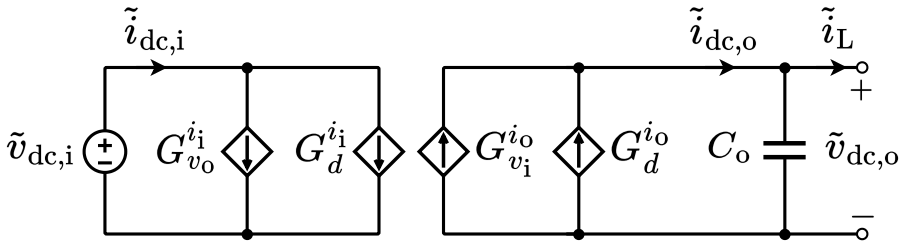


Figure 4.18: Dual active bridge small-signal model [141, 142].

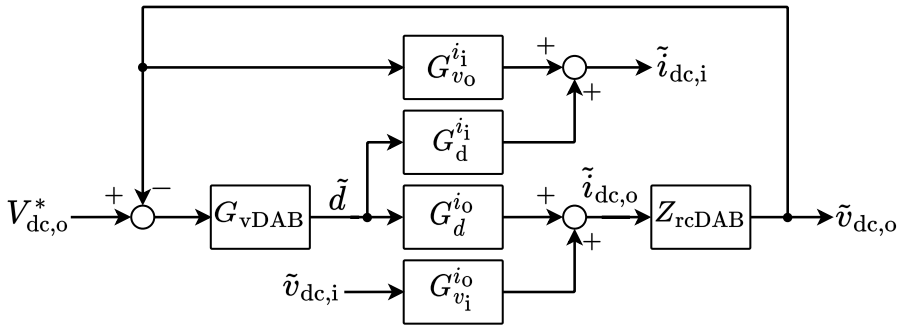


Figure 4.19: Dual active bridge control block diagram in the case of DPF [142].

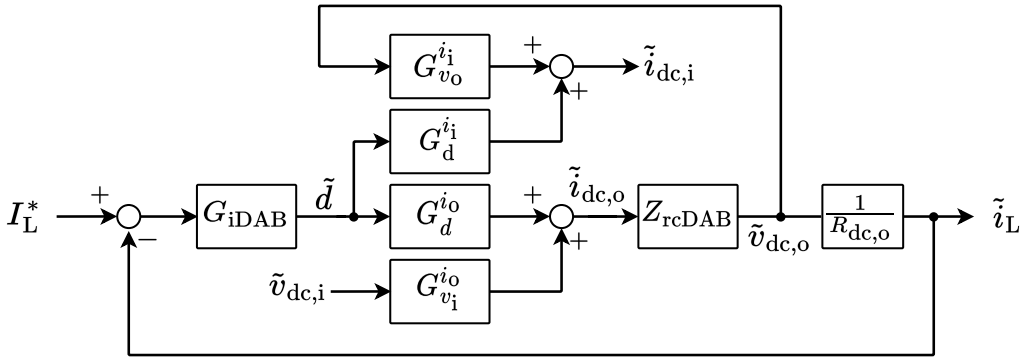


Figure 4.20: Dual active bridge control block diagram in the case of RPF [142].

modes as (4.61) and (4.62):

$$Z_{\mathrm{inCL,DAB}}\Big|_{\mathrm{DPF}} = \frac{1+Z_{\mathrm{rcDAB}}G_{d}^{i_{\mathrm{o}}}G_{\mathrm{vDAB}}}{\left(G_{v_{\mathrm{o}}}^{i_{\mathrm{i}}}-G_{d}^{i_{\mathrm{i}}}G_{\mathrm{vDAB}}\right)Z_{\mathrm{rcDAB}}G_{v_{\mathrm{i}}}^{i_{\mathrm{o}}}} \tag{4.61}$$

$$Z_{\mathrm{inCL,DAB}}\Big|_{\mathrm{RPF}} = \frac{R_{\mathrm{dc,o}}+Z_{\mathrm{rcDAB}}G_{d}^{i_{\mathrm{o}}}G_{\mathrm{iDAB}}}{\left(G_{v_{\mathrm{o}}}^{i_{\mathrm{i}}}R_{\mathrm{dc,o}}-G_{d}^{i_{\mathrm{i}}}G_{\mathrm{iDAB}}\right)Z_{\mathrm{rcDAB}}G_{v_{\mathrm{i}}}^{i_{\mathrm{o}}}} \tag{4.62}$$

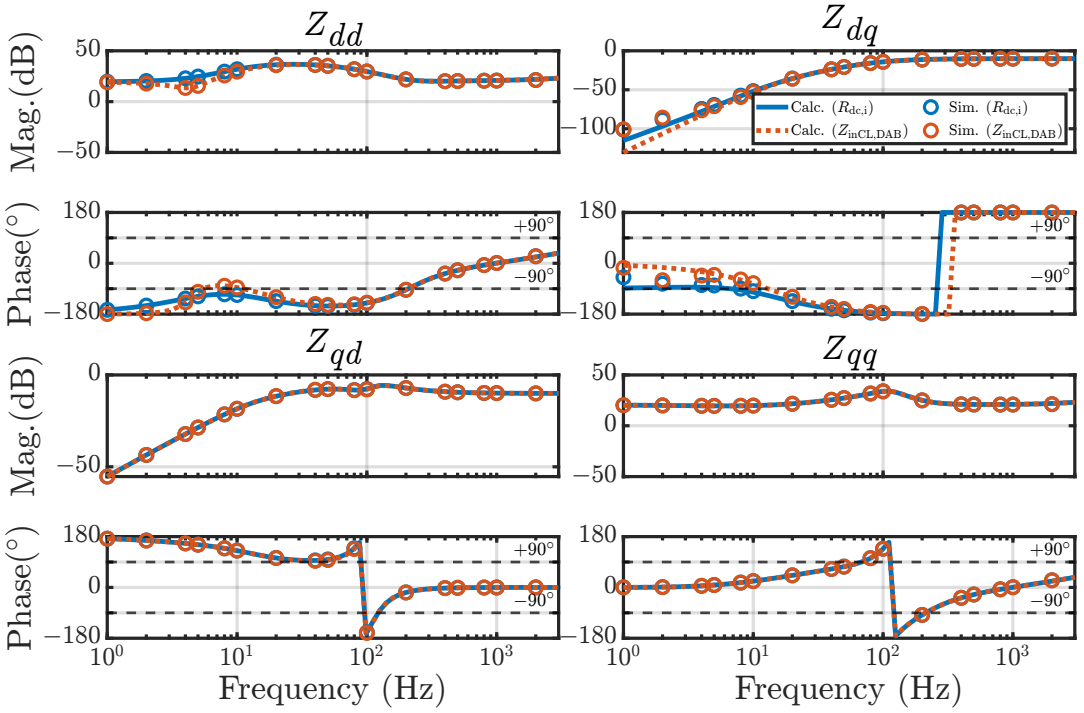


Figure 4.21: Comparison between the calculated and the simulated dq impedances in the case of pure resistive load and DAB load.

4.3.2 Impedance Model Validation

Before analyzing the properties of the input dq impedance matrix of the cascaded topology investigated in this Section, the impedance model derived in the previous section is validated by means of time-domain simulations in MATLAB/Simulink. The input impedance matrix of the cascaded topology is obtained, as stated previously, by replacing load resistor expression $R_{\mathrm{dc,i}}$ in (4.55) with the DAB input impedance given in (4.61) or in (4.62), depending on the power flow. Extracting the DAB closed-loop input impedance $Z_{\mathrm{inCL,DAB}}$ is relatively simple since it is a dc circuit, thus it is only required to inject a perturbation signal (which can be a current or either a voltage perturbation) over the frequency range of interest, and measure the frequency response of the converter at the input interface. Whilst, extracting the AFE closed-loop input impedance $\boldsymbol{Z}_{\mathrm{inCL}}$ is not trivial since it is required to solve a system of four unknown variables. It is thus necessary to inject two sets of linear-independent perturbation signals and to sweep such injection over the frequency range of interest. To do so, the procedure explained in [147, 148] is employed. Being the impedance model derived in Section II based on the average model

of the converter, which is accurate till half of the switching frequency f_{sw} [137, 146], the impedance model is validated in the frequency range of 1 Hz - 2 kHz since the multilevel AFE swithing frequency is 4 kHz. Therefore, based on the circuit parameters given in Table 4.3, the comparison between the impedances derived analytically and the ones measured in simulation is reported in Fig. 4.21 for both configurations (AFE with resistive load and AFE connected to a DAB). As can be noted, the simulation results show good agreement with the analytical ones, thus the impedance model derived in this work is finally validated.

4.3.3 Input Impedance Properties Analysis

In this section, the effect of the cascaded topology on the input impedance matrix is revealed and analyzed.

Note that, being the DAB a dc-load for the grid-connected SST and as can also be deduced from the equations given in Section II, the effect of the dc-dc converter on the AFE input impedance matrix is only visible on the d-axis impedance Z_{dd}, as it depends on M_d^s (see eq. (4.37)) while is much less visible on Z_{dq}, Z_{dq} and Z_{qq} because M_q^s is generally small. In particular, the effect on Z_{dq} is negligible unless there it is a reactive power exchange in the converter. Fig. 4.21, that refers to the AFE mode (DPF) confirm this point. Thus, as said in the introduction, particular attention will be paid on the passivity properties of d-axis input impedance Z_{dd}. Before doing that, it is necessary to recall some basic assumptions made in this work. First, it is supposed that the two converter stages that build the ac-dc-dc topology (i.e. the AFE and the DAB) are, together with their own control system, individually stable. To do so, the AFE control system has been design following the guidelines provided by [123, 133]. Thus, the voltage controller bandwidth, along width the PLL loop bandwidth, where design at least 10 times smaller than the current control loop, so as to guarantee stable operation in both AFE and inverter modes [123, 133]. Therefore, in the case under consideration the current controller bandwidth is $\omega_{\text{cc}} = 2\pi 250$ rad/s, the voltage controller bandwidth $\omega_{\text{vc}} = 2\pi 10$ rad/s while the PPL bandwidth is chosen to be is $\omega_{\text{pll}} = 2\pi 25$ rad/s. This brought to the controller gains provided in Table 4.3. Secondly, the DAB controller bandwidth (both the voltage and the current one) is designed to be larger than the AFE current control in

Table 4.3: SST system parameters used for the grid-connection stability analysis.

E_d^s, E_q^s	M_d^s, M_q^s	I_d^s, I_q^s	R_{f}, L_{f}, C_{i}, $R_{\mathrm{dc,i}}$, N
[V]	[adm]	[A]	[mΩ,mH,mF,Ω,adm]
340, 0	0.66, -0.02	32.68, 0	500, 1, 5, 11.13, 4
$V_{\mathrm{dc,i,o}}$	f_{g}	f_{sw}, f_{sd}	C_{o}, $R_{\mathrm{dc,o}}$, n, L_{t}
[V]	[Hz]	[kHz]	[mF, Ω, adm, μ H]
122	50	4, 12	5, 11.13, 1, 41.74
K_{Pv}, K_{Iv}	K_{Pi}, K_{Ii}	K_{Ppll}, K_{Ipll}	$K_{\mathrm{Pdab,v,i}}$, $K_{\mathrm{Idab,v,i}}$
0.067, 3.37	1.15, 1490	0.46, 10.11	0.3, 2.8, 228.7, 2574

order to decouple the conversion stages timescale dynamics. In fact, as Fig. 4.22a shows, in the frequency range of the DAB control system (and thus within the AFE control system bandwidth), the closed-loop DAB input impedance $Z_{\mathrm{inCL,DAB}}$ can be modeled as a negative resistor in case of DPF or as a positive one in case of RPF [139, 142] (that reminds the typical behaviour of a CPL [123]). Therefore, as Fig. 4.22b shows, in case of DAB connection the dc-side impedance Z_{rc} can be assumed to be the parallel impedance of C_{i} with a negative resistance $-R_{dc,i}$ or with a positive one depending on the power flow. This assumption will be made to simplify the passivity analysis carried out in this Section.

Impact on Active Front-End Mode

Fig. 4.21 shows the effect of the dc-dc converter on the AFE input impedance matrix, in comparison to a more common pure resistive load R_{dc}. Such impact is visible at low frequencies, i.e. around the voltage control loop bandwidth ω_{vc}. As stated at the beginning of this Section, the impact is more evident in the d-axis Z_{dd}, while the impact on Z_{dq} is negligible because its magnitude is really low (no reactive power exchange). In the low frequency range the connection of a dc-dc converter slightly lowers the magnitude of Z_{dd} compared to the case in which only a resistor is connected [139]. This can worse the

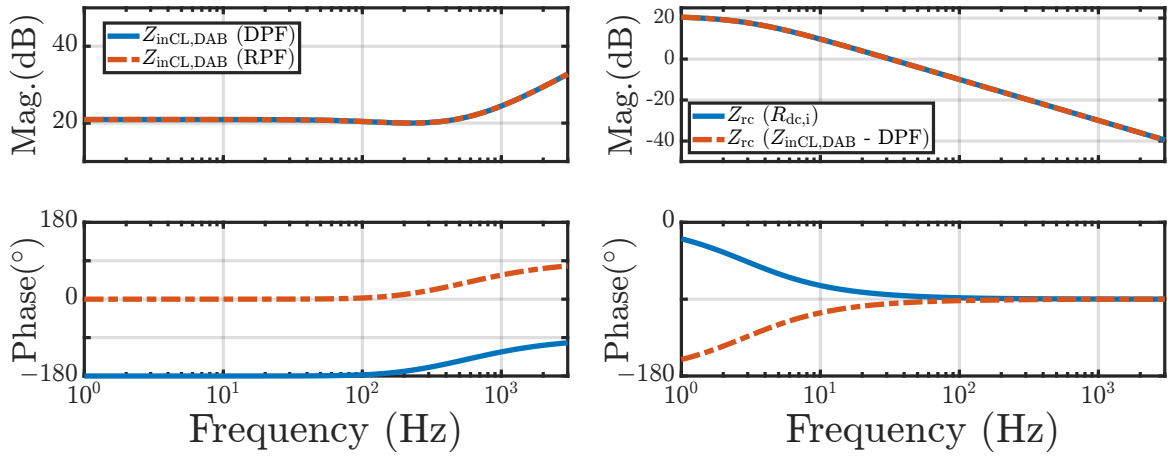


Figure 4.22: (a) $Z_{\text{inCL,DAB}}$ in case of both DPF and RPF. (b) influence of a pure resistive load $R_{\text{dc,i}}$ or $Z_{\text{inCL,DAB}}$ (DPF) on Z_{rc}.

grid-connection stability of the system. However, differently from what shown in [139], it seems that, for the system parameters given in Table 4.3, the d-axis low-frequency passivity is enhanced in the case of a DAB-connected AFE compared to the resistive-load one. Thus, it might be of interest to deeply analyze the passivity properties of Z_{dd} within the voltage controller bandwidth. To do so, we first derive a simplify expression for Z_{dd} that holds for the low-frequency range. To this end, contrary to the parameters of Table 4.3, a lower bandwidth for the voltage controller (i.e. $\omega_{\text{vc}} = 2\pi 5$ rad/s) is selected to highlight more the passivity properties of Z_{dd} in the case of DAB as dc-load. This yields to $K_{\text{Pv}} = 0.029$ and $K_{\text{Iv}} = 1.440$. In the AFE mode, for a amplitude-invariant Park transformation matrix, in steady-state it holds [134, 139]:

$$\frac{3}{2} v_d^s i_d^s = 3N v_{dc,i} i_{dc,i} \tag{4.63}$$

By perturbing and linearizing (4.63), supposing for simplicity that $R_{\text{f}} = 0\ \Omega$, the following is derived:

$$I_d^s \tilde{v}_d^s + V_d^s \tilde{i}_d^s = 2NV_{\text{dc,i}} \tilde{i}_{\text{dc,i}} + 2NI_{\text{dc,i}} \tilde{v}_{\text{dc,i}} \tag{4.64}$$

At low frequency, only the voltage controller affects the d-axis impedance shape, since the current controller is supposed to be much faster and thus the d-axis current closely follows the current reference provided by the voltage controller. Also, PLL has no effect

on Z_{dd} [123, 134]. Therefore, based on the AFE control block diagram of 4.17:

$$\tilde{i}_d = -NG_v\tilde{v}_{\mathrm{dc,i}} \tag{4.65}$$

$$\tilde{v}_{\mathrm{dc,i}} = Z_{\mathrm{rc}}\tilde{i}_{\mathrm{dc,i}} \tag{4.66}$$

where Z_{rc} is assumed to be $+R_{\mathrm{dc,i}}$ in case of pure resistive load or $-R_{\mathrm{dc,i}}$ in case of DAB. Combining eq. (4.64) with (4.65) and (4.66), and neglecting the impact of the digital control delay (which is impactless at low frequencies), it is possible to derive the simplify expression of Z_{dd} that holds in the low frequency range as:

$$Z_{dd}\Big|_{\omega\leq\omega_{vc}} = -\frac{2V_{dc,i} + Z_{\mathrm{rc}}\left(2I_{\mathrm{dc,i}} + G_vV_d\right)}{G_vI_dZ_{\mathrm{rc}}} \tag{4.67}$$

Fig. 4.23 shows the comparison between the approximated expression of Z_{dd} given in (4.67) and the original one derived in Section II, that holds withing ω_{vc} range.

At this point, it is interesting to note that for small integral-gain K_{Iv} of G_v (i.e. $K_{\mathrm{Iv}} \approx 0$ which is a common good design approximation, that usually leads to the choice $K_{\mathrm{Pv}} = \omega_{vc}C_{\mathrm{i}}$, [123]) and for $\omega \to 0$, (4.67) becomes:

$$\lim_{\omega\to 0} Z_{dd}(j\omega)\Big|_{Z_{\mathrm{rc}}=-R_{dc,i}} = -\frac{V_d^s}{I_d^s} \tag{4.68}$$

$$\lim_{\omega\to 0} Z_{dd}(j\omega)\Big|_{Z_{\mathrm{rc}}=+R_{dc,i}} = -\frac{4V_{dc,i} + K_{\mathrm{Pv}}R_{dc,i}V_d^s}{I_d^sK_{\mathrm{Pv}}R_{dc,i}} \tag{4.69}$$

in which $I_{dc,i} = V_{dc,i}/|R_{dc,i}|$ since the active power is absorbed in both cases (AFE mode).

Eq. (4.68) shows that, in the case of a controlled dc-dc converter connected to the dc-side of the AFE (thus with negative $R_{dc,i}$), even with null voltage controller integral-gain K_{Iv} the d-axis impedance shows the characteristic negative incremental behavior typical of the AFE rectifiers [134]. That means, even with null voltage controller integral-gain K_{Iv}, the cascaded ac-dc-dc topology still absorb the reference active power imposed by the controller (but most likely $v_{dc,i}$ will deviate from its reference value). This is because of the DAB voltage controller that force the dc-load of the AFE to be a CPL within the regulation limit of G_{vDAB}. The same doesn't hold for the pure resistive load $R_{dc,i}$, as eq. (4.69) demonstrates. In this case, since $v_{dc,i}$ will deviate from its reference value, is obviously and straightforward that the active power absorbed by the AFE will also deviate from the reference value. For the systems parameters defined in Table 4.3 and for

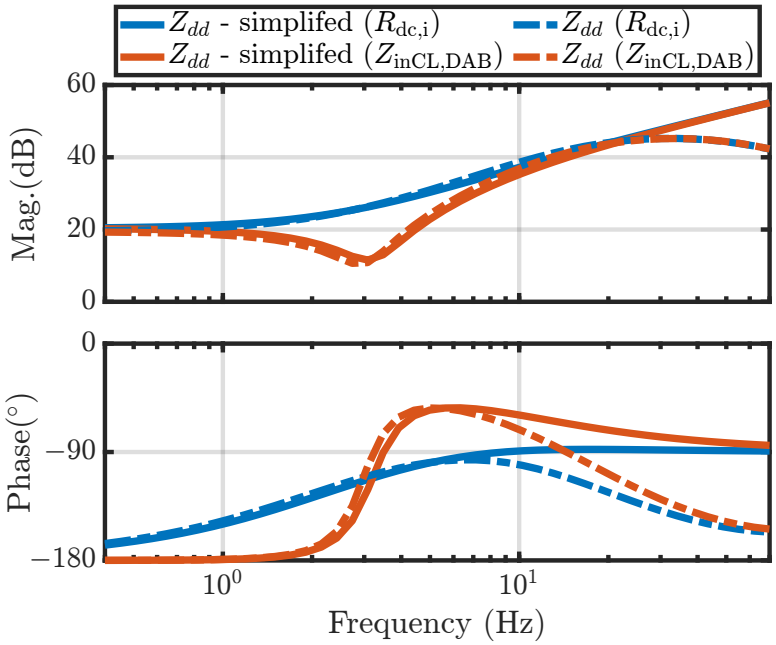


Figure 4.23: Comparison between the simplified expression of Z_{dd} and the accurate one given in (4.55).

$K_{\mathrm{Pv}} = 0.029$, Fig. 4.24 shows the effectiveness of (4.68) and (4.69). As can be observed, the low-frequency magnitude of Z_{dd} in case of DAB is equal to the absolute value of the ratio of V_d^s and I_d^s (≈ 10.38), while a different value is found (≈ 57.42) for the resistive load case according to (4.69). However, for both cases $\mathrm{Re}(Z_{dd})$ is negative at low frequencies since the CPL behavior is obviously preserved.

Recalling the aim to analyze the passivity properties of Z_{dd}, Fig. 4.23 show a larger passivity border (i.e. $\mathrm{Re}(Z_{dd}) \geq 0$) in the case of DAB connected to the AFE in contrast to the case of a pure resistive load, whose passivity range seems to barely get passive at some value of the frequency. Thus, it might be of interest to derive an expression for $\mathrm{Re}(Z_{dd})$. Starting from (4.67), the real part of $\mathrm{Re}(Z_{dd})$ can be derived as in (4.70):

$$\begin{aligned}&\mathrm{Re}\{Z_{dd}(j\omega)\}\Big|_{\omega\leq\omega_{vc}} = \\ &= \frac{\left(2C_{\mathrm{i}}K_{\mathrm{Iv}}R_{\mathrm{dc,i}}V_{\mathrm{dc,i}} - 2I_{\mathrm{dc,i}}K_{\mathrm{Pv}}R_{\mathrm{dc,i}} - K_{\mathrm{Pv}}^2R_{\mathrm{dc,i}}V_d^s - 2K_{\mathrm{Pv}}V_{\mathrm{dc,i}}\right)\omega^2 - K_{\mathrm{Iv}}^2R_{\mathrm{dc,i}}V_d^s}{I_d^sR_{\mathrm{dc,i}}K_{\mathrm{Iv}}^2 + I_d^sR_{\mathrm{dc,i}}K_{\mathrm{Pv}}^2\omega^2}\end{aligned} \tag{4.70}$$

At this point, setting $\mathrm{Re}(Z_{dd}) = 0$ in (4.70) and solving the second order equation for ω by considering (for both the DAB and the pure resistance case) the only root that lies in the domain of (4.67), it is possible to derive the upper limit value ω_{c} of the non-positive

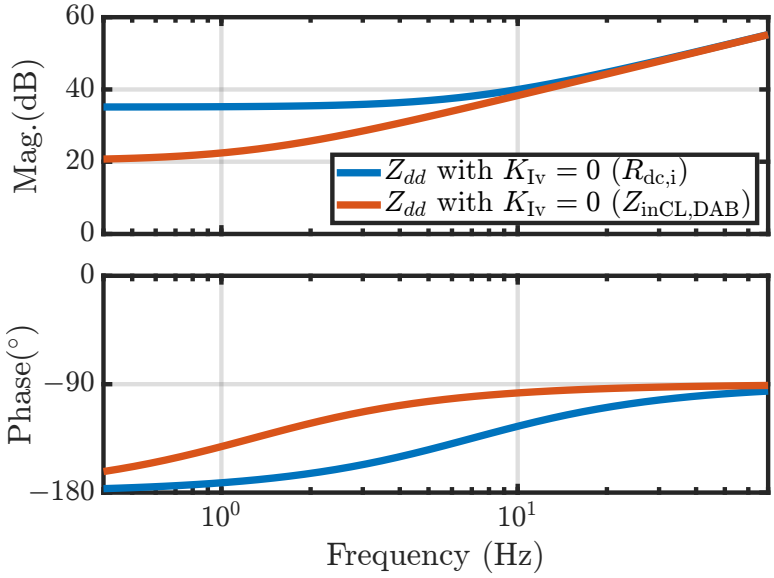


Figure 4.24: Comparison between Z_{dd} in case of both pure resistive load and DAB with voltage controller integral gain $K_{\mathrm{Iv}} = 0$.

resistance region, i.e. the angular frequency at which $\mathrm{Re}(Z_{dd})$ becomes positive, that is:

$$\omega_{\mathrm{c}}\Big|_{Z_{\mathrm{rc}}=Z_{\mathrm{rc,dab}}} = \omega_{\mathrm{c,dab}} = \frac{K_{\mathrm{Iv}}\sqrt{-Z_{\mathrm{rc,dab}}V_d^s K_{\mathrm{dab}}}}{K_{\mathrm{dab}}} \tag{4.71}$$

$$\omega_{\mathrm{c}}\Big|_{Z_{\mathrm{rc}}=Z_{\mathrm{rc,R_{dc}}}} = \omega_{\mathrm{c,R_{dc}}} = -\frac{K_{\mathrm{Iv}}\sqrt{-Z_{\mathrm{rc,R_{dc}}}V_d^s K_{\mathrm{R_{dc}}}}}{K_{\mathrm{R_{dc}}}} \tag{4.72}$$

where:

$$\begin{aligned} K_{\mathrm{dab}} =& 2K_{\mathrm{Pv}}V_{\mathrm{dc,i}} + 2I_{\mathrm{dc,i}}K_{\mathrm{Pv}}Z_{\mathrm{rc,dab}} + \\ & K_{\mathrm{Pv}}^2 Z_{\mathrm{rc,dab}}V_d^s - 2CK_{\mathrm{Iv}}Z_{\mathrm{rc,dab}}V_{\mathrm{dc,i}} \end{aligned} \tag{4.73}$$

$$\begin{aligned} K_{\mathrm{R_{dc}}} =& 2K_{\mathrm{Pv}}V_{\mathrm{dc,i}} + 2I_{\mathrm{dc,i}}K_{\mathrm{Pv}}Z_{\mathrm{rc,R_{dc}}} + \\ & K_{\mathrm{Pv}}^2 Z_{\mathrm{rc,R_{dc}}}V_d^s - 2CK_{\mathrm{Iv}}Z_{\mathrm{rc,R_{dc}}}V_{\mathrm{dc,i}} \end{aligned} \tag{4.74}$$

where, for clarity of reading, $Z_{\mathrm{rc,dab}} = -|R_{\mathrm{dc,i}}|$ and $Z_{\mathrm{rc,R_{dc}}} = R_{\mathrm{dc,i}}$, $\forall R_{\mathrm{dc,i}} > 0$. Equations (4.71) and (4.72) show the angular frequency at which $\mathrm{Re(Z_{dd})}$ starts to be positive for both cases under analysis. Recalling that, for AFE mode, $Z_{\mathrm{rc,dab}} = -Z_{\mathrm{rc,R_{dc}}}$, it is possible to define the ratio of (4.71) over (4.72) as:

$$\omega_{\mathrm{r}} = \sqrt{\frac{R_{\mathrm{dc,i}}V_d^s K_{\mathrm{Pv}}^2 + 4V_{\mathrm{dc,i}}K_{\mathrm{Pv}} - 2C_{\mathrm{i}}K_{\mathrm{Iv}}R_{\mathrm{dc,i}}V_{\mathrm{dc,i}}}{R_{\mathrm{dc,i}}(V_d^s K_{\mathrm{Pv}}^2 - 2C_{\mathrm{i}}K_{\mathrm{Iv}}V_{\mathrm{dc,i}})}} \tag{4.75}$$

which, for the parameters listed in Table 4.3 and for $K_{\mathrm{Pv}} = 0.029$ and $K_{\mathrm{Iv}} = 1.440$ is lower than 1 ($\omega_{\mathrm{r}} \approx 0.39$ in agreement with Fig. 4.23) meaning that the DAB-based

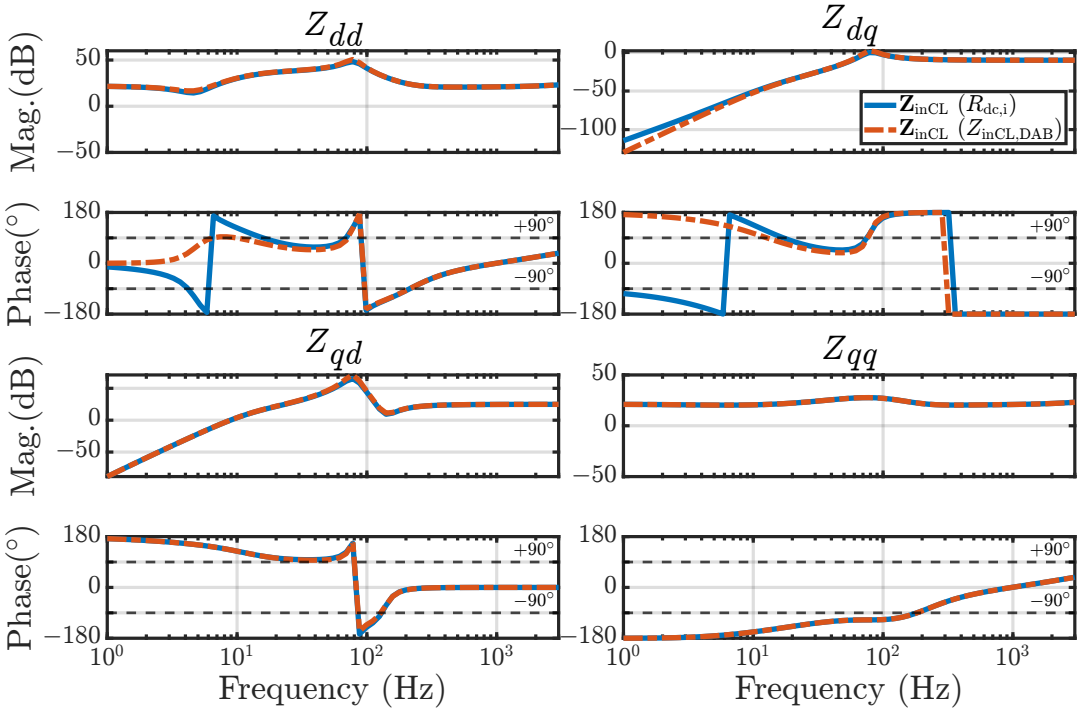


Figure 4.25: SST input dq impedances during the inverter mode, based on parameters given in Table 4.3.

cascaded topology shows a larger passivity boundary (or a smaller non-passive area) in the low-frequency region compared to the pure resistive case.

Equations (4.71) and (4.72) can be used to predict the low-frequency passivity region boundary in both DAB and pure resistor cases. What is more, (4.71) and (4.72) can be used together with (4.67) and (4.70) to perform a passivity-oriented design of both the cascaded and not cascaded multilevel AFE investigated in this thesis. Not least, it can be shown that the same analysis holds also for the inverter mode of the ac-dc-dc topology considered here, but the low-frequency region of Z_{dd} should be already passive enough (even for higher ω_{cv}) since the inverter mode is less susceptible to an increase in ω_{cv} [123].

Impact on Inverter Mode

Fig. 4.25 shows the effect of the cascaded topology compared to the pure resistor one in case of RPF (and thus in inverter mode). As explained in the previous Subsection, even in this case the dc-dc stage seems to enhance the passivity boundary of the d-axis impedance Z_{dd}, which in case of pure resistive load is poor due to the low voltage

controller bandwidth ω_{vc}, that enhance passivity when increased in this operation mode [133]. The same analysis carried out previously can be repeated also for the inverter mode, as already mentioned. Either way, it can a priori be concluded that cascaded ac-dc-dc topology investigated in this work already enhance the passivity region of the d-axis input impedance Z_{dd} without increasing the voltage controller bandwidth ω_{vc}.

Impact on Reactive Mode and Synchronization Loop

As stated before in this Section, the effect of the cascaded topology on the AFE input impedance matrix Z_{inCL} is only visible on Z_{dq} when I_q^s is not null anymore. Instead, Z_{qd} is unaltered if the grid voltage is symmetric and balanced (i.e. $V_q^s = 0$).

With regard to the effect of the ac-dc-dc topology on the synchronization loop, it is well known that the PLL mainly effects the q-axis impedance Z_{qq} [123, 135], where the dc-dc converter has no impact since usually $M_q^s \approx 0$. The only noticeable impact will be, again, on Z_{dq} if there is a reactive power exchange while, still, Z_{qd} will be unaltered if the grid voltage is healthy.

4.3.4 Discussion

In this Section, the dq-frame input impedance expressions of the CHB- and DAB-based ac-dc-dc building block of a SST topology has been derived through the small-small signal analysis. The dq impedance model derived has been validated by means of time-domain simulation in MATLAB/Simulink. Then, the effect of the dc-dc stage on the input impedance matrix has been assessed and analyzed in comparison to a pure resistive load connected to the dc-link. In particular, the analysis aimed to discuss the input impedance matrix properties in terms of its passivity, thus helping the designer to achieve a stable grid-connected system. For this purpose, the d-axis input impedance Z_{dd} has been mainly addressed during the DPF scenario (AFE mode) as it is the more sensitive matrix element to a load connected to the dc-side of the CHB. A simplified expression for Z_{dd} and for its real part - that holds for low frequencies - has been derived in Section 4.3.3. Furthermore, an expression for the upper limit of the negative resistance region of Z_{dd} is proposed, and it is demonstrated that the dc-dc load can increase the passivity region boundary. Equations (4.67), (4.70), (4.71) and (4.72) can be used to perform a

passivity-oriented design of the SST topology investigated in this thesis. Moreover, the impedance model derived in this work (and thus the analysis done) is valid for a generic ac-dc-dc topology. Finally, a mention regarding the effect of the dc-dc stage during also the inverter and reactive modes, along with the impact on the synchronization loop (i.e. the PLL), has been given. These aspects are left open to future work.

4.4 Summary of Results and Final Discussion

In this chapter, the stability assessment of the SST is presented, from both DC-bus and grid-connection perspectives. In the first case it was pointed out that that the direction of the power flow and the voltage rating at which the SST works may be sources of instability. The first issued is due to the non-symmetric control structure of the SST. In the second case, in particular the analysis aimed to discuss the input impedance matrix properties in terms of its passivity, thus helping the designer to achieve a stable grid-connected system. Through the derivation of a simplified expression for the d-axis impedance, it is demonstrated that the DC-DC load can increase the passivity region boundary. Also, a mention regarding the effect of the DC-DC stage on the inverter and reactive operation modes of the MV AFE, along with the impact on the synchronization loop (i.e. the PLL), is presented. These aspects are left open to future work

Chapter 5

Solid-State Transformer Hardware Prototype Design, Construction and Test

In this final Chapter, the design and open-loop test of the SST prototype is presented. The three-phase triple-stage SST investigated in this thesis is a highly modular structure, therefore the whole converter structure is obtain by the connection of several power modules. The goal behind the SST prototype development is to keep a modular approach even during the design phase. Therefore, after having identify the best power unit configuration in terms of modularity, scalability and flexibility, the design of the SST is carried out on the single power module.

In the following Sections, then component selections and design considerations for the SST power module, which consists of the power and gate driver board, are presented. The, the PCBs development is introduced and the final assembled power unit is shown. Finally, open-loop tests of the power module conclude this work.

5.1 Power Module Component Selection and Design

Fig. 5.1 shows the three-phase triple-stage SST topology considered in this work and already presented in Section 2.5.2. As can be observed from the figure, the best power module topology that provides the highest maximum degrees of modularity, flexibility

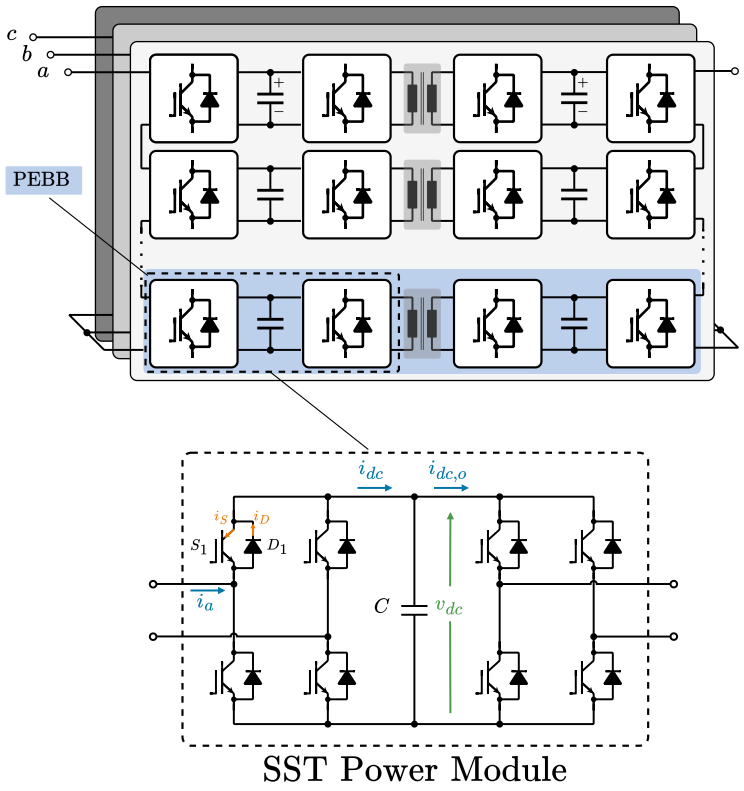


Figure 5.1: Three-phase triple-stage SST under investigation and chosen modular Back-To-Back H-Bridge Power Module (B2B-PM) topology.

and scalability consists of the back-to-back configuration of two H-Bridges, which corresponds to half of a SST PEBB. Therefore, the key power unit selected for the prototype development of the presented SST architecture is the Back-To-Back H-Bridge Power Module, i.e. B2B-PM. In the next, the power unit ratings, component selection and design considerations are presented.

5.1.1 Power Module Ratings

The SST power stage developed here is for laboratory purposes, therefore it is a three-phase down-scaled prototype. The power rating selected is $S_{sst} = 15$ kVA and the nominal grid line-to-line voltage considered for the design is $V_g = 400$ V. Therefore, the RMS phase current is given by:

$$I_{sst} = \frac{S_{sst}}{\sqrt{3}V_g} \approx 22\,\text{A} \tag{5.1}$$

The AFE and Inverter stages consists of the CHB topology. Considering a rated modulation index if $m_{sst} = 0.7$ to ensure enough margin of operation (without third harmonic injection), the total DC-link voltage required is calculated based on (2.5):

$$V_{dc,sst}^{tot} = \frac{\sqrt{2}V_g}{\sqrt{3}m_{sst}} \approx 465\,\text{V} \tag{5.2}$$

The number of submodules is calculated according to (2.6). Therefore, the semiconductor block voltage V_b must be selected, along with the utilization factor which is chosen to be $k_u = 0.5$ here. Semiconductors can be either selected as discrete components or power modules. The first choice allows a more customizable and flexible power stage design. However the circuit design and routing must be carried out carefully to avoid unwanted parasitic disturbances that may rise because of the circuit layout. The second option, instead, offers less degree of freedom in terms of power circuit realization, but the advantage lies in the simplified power layout being power modules inherently optimized by the supplier. Since the focus of this work is not on converter design optimization, the semiconductor choice falls on IGBT power modules. Being the converter stage a down-scaled prototype, the total required DC-link voltage is quite low, therefore low-blocking voltage devices could be selected. Nevertheless, actual IGBT power modules available on the market are usually rated for a minimum of $V_b = 600$ V [149]. Hence, even considering $k_u = 0.5$, just one power module would be almost sufficient. However, to maintain the advantages of a SST topology based on multilevel converters, the number of submodules is independently chosen to be $N = 4$. Therefore, the rated apparent power S_{sst} is spread among four per-phase PEBBs. Hence the power rating for each submodule is:

$$S_{sm} = \frac{S_{sst}}{3N} = 1.25\,\text{kVA} \tag{5.3}$$

and the the rated DC-link voltage of each submodule is given by:

$$V_{dc,sst} = \frac{V_{dc,sst}^{tot}}{4} \approx 116\,\text{V} \tag{5.4}$$

Eq. (5.4) concludes the definition of the SST down-scaled prototype main ratings.

5.1.2 Semiconductor Comparison and Selection

Based on the B2B-PM ratings presented in the previous Section, the minimum blocking voltage required for the semiconductors is:

$$V_{b,min} = \frac{V_{dc,sst}}{k_u} = 232\,\mathrm{V} \tag{5.5}$$

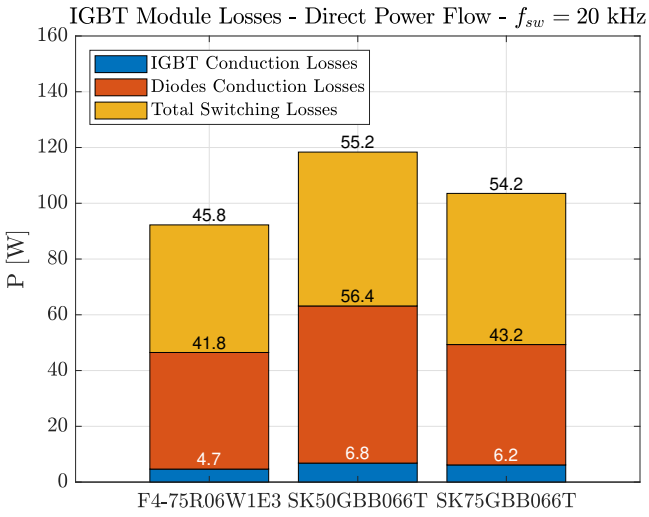
Based on (5.5), the commonly available on the market blocking voltage of $V_b = 600$ V is selected. Three different IGBT power modules are then compared in terms of total losses and the best one is selected. Neglecting the driving losses, whose are related to the gate driver circuit, the total semiconductor losses consists of static (or conduction) and switching losses [78]. The conduction losses take into account the ON-state losses and the OFF-state losses, i.e. the blocking losses. Whilst, the switching losses consists of turn-on and turn-off losses. The power losses computation is carried out here based on the comprehensive application note [78]. The IGBT power modules under evaluation are, respectively, *Semikron Danfoss* SEMITOP 3 - SK50GBB066T [150], SEMITOP 3 - SK75GBB066T [151] and *Infineon* EasyPACK F4-75R06W1E3 [152]. Based on [78], the IGBT (S) and diode (D) conduction losses for a sinusoidal PWM-driven Half-Bridge are computed as:

$$P_{cond,S} = \left(\frac{1}{2\pi} + \frac{m\cos\varphi}{8}\right) V_{CE0}(T_j)\hat{I}_S + \left(\frac{1}{8} + \frac{m\cos\varphi}{3\pi}\right) r_{CE}(T_j)\hat{I}_S^2 = V_{CE0}(T_j)\bar{I}_S + r_{CE}(T_j)I_S^2 \tag{5.6}$$

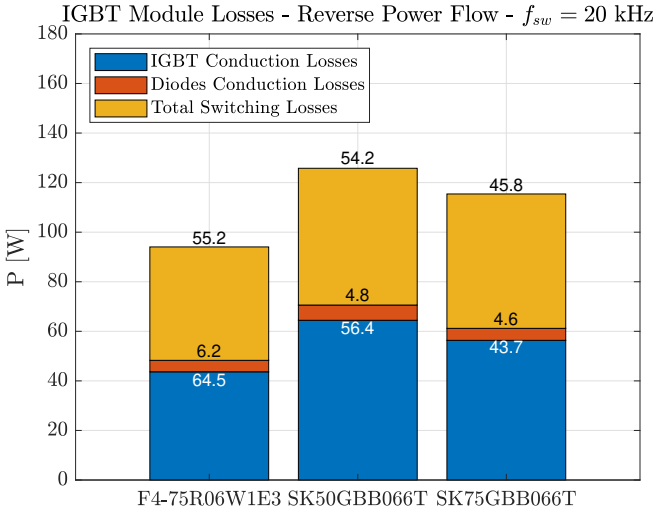
$$P_{cond,S} = \left(\frac{1}{2\pi} - \frac{m\cos\varphi}{8}\right) V_{F0}(T_j)\hat{I}_D + \left(\frac{1}{8} - \frac{m\cos\varphi}{3\pi}\right) r_F(T_j)\hat{I}_D^2 = V_{F0}(T_j)\bar{I}_D + r_F(T_j)I_D^2 \tag{5.7}$$

where m is the modulation index, $\cos\varphi$ is the power factor, $V_{CE0}(T_j)$ is the IGBT temperature-dependent threshold voltage of the on-state characteristic, $V_{F0}(T_j)$ is diode temperature-dependent threshold voltage of the on-state characteristic, $r_{CE}(T_j)$ is the IGBT temperature-dependent bulk resistance of the on-state characteristic, $r_F(T_j)$ is the diode temperature-dependent bulk resistance of the on-state characteristic while $\hat{I}_S$, $\hat{I}_D$, $\bar{I}_S$, $\bar{I}_D$ and I_S, I_D are the peak, average and RMS values of the IGBT and diode current respectively, as show in the schematic of Fig. 5.1. On the other hand, the switching losses are computed as [78]:

$$P_{sw,S} = f_{sw}(E_{on+off})\frac{\sqrt{2}}{\pi}\frac{\hat{I}_S}{I_{ref}}\left(\frac{V_{dc}}{V_{ref}}\right)^{K_v}(1 + TC_{Esw}(T_j - T_{ref})) \tag{5.8}$$



(a)



(b)

Figure 5.2: Comparison between the IGBT module Direct Power Flow (DPF) total losses (a) and (b) Reverse Power Flow (RPF) total losses.

$$P_{sw,D} = f_{sw}(E_{rr})\frac{\sqrt{2}}{\pi}\frac{\hat{I}_D}{I_{ref}}\left(\frac{V_{dc}}{V_{ref}}\right)^{K_v}(1 + TC_{Err}(T_j - T_{ref})) \tag{5.9}$$

where f_{sw} is the switching frequency, E_{on+off} is the sum off the IGBT turn-on and turn-off energy losses, E_{rr} is the diode reverse recovery energy loss, TC_{Esw} is the IGBT temperature coefficient of the switching losses, TC_{Err} is the diode temperature coefficient of the switching losses, T_j is the actual junction temperature, K_v is an exponent for the voltage dependency of switching losses and I_{ref} , V_{ref} , T_{ref} are the reference values of the switch-

ing loss measurements taken from the datasheet. Considering the worst case scenario, i.e. $m = 1$, $\cos\varphi = \pm 1$, $\hat{I}_{S,D} = \sqrt{2} \cdot 25$ A, $f_{sw} = 20$ kHz and $V_{dc} = 200$ V, power modules total losses, for both direct (i.e. $\cos\varphi = 1$) and reverse (i.e. $\cos\varphi = -1$) power flows, are represented in Fig. 5.2a and 5.2b. As can be noted, among these three IGBT modules, the *Infineon* EasyPACK F4-75R06W1E3 shows the best performances and therefore is finally selected.

5.1.3 Submodule Capacitance Design

Submodules DC-link capacitance is designed according to equation (2.8), based on the maximum allowable voltage ripple. The rated and the worst case scenarios have been considered for comparison. In the rated scenario, the submodule DC-link voltage, modulation index and grid currents are set to be the rated ones, i.e. $V_{dc,sst} = 116$ V, $m = 0.7$ and $I_{sst} = 22$ A. On the other hand, the worst case scenario is defined by the maximum current $I_{sst}^{max} = 25$ A and by the maximum modulation index $m = 1$. Fig. 5.3 shows the comparison of the DC-link minimum capacitance required in both cases versus the maximum allowable voltage ripple $\Delta v_{dc\%}$. Considering the worst case scenario, and setting $\Delta v_{dc\%} = 5\%$, the minimum required capacitance is $C_{sm}^{min} = 4.64$ mF. Hence, the chosen

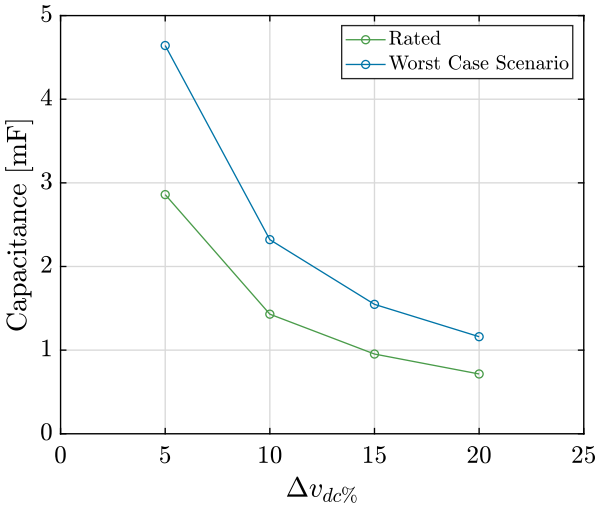


Figure 5.3: Required submodule capacitance versus maximum allowable voltage ripple for both rated and worst case scenarios according to (2.8).

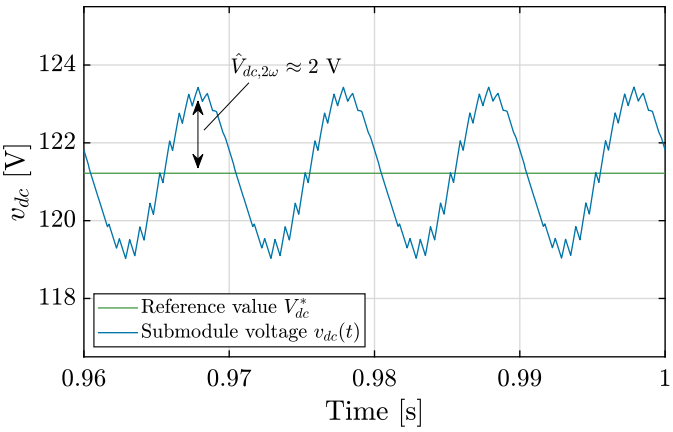


Figure 5.4: Simulated submodule voltage ripple.

capacitance:

$$C_{sm}^{min} = 5\,\text{mF}. \tag{5.10}$$

For instance, Fig. 5.4 shows the effectiveness of eq. (2.8), where for $m = 0.7$, $\hat{I}_{sst} = 18$ A and $C_{sm}^{min} = 5$ mF a peak voltage ripple of 2 V is obtained:

$$\hat{V}_{dc,2\omega} = \frac{m\hat{I}_{sst}}{2\omega C_{sm}} = \frac{0.7 \cdot 18}{2(2\pi 50)0.005} \approx 1.99\,\text{V} \tag{5.11}$$

Once the DC-link capacitance is defined, the capacitor bank is realized by the series or parallel connection of multiple capacitors, to cope with not only the total capacitance required, but also with the voltage and current requirements for the DC-bus. For instance, series connection of capacitors allows to spread the total DC-link voltage among them, while their parallel connection allows to spread the total DC-link ripple current. Moreover, the number of required capacitors and their series or parallel connection should be object of an optimization procedure to maximize the DC bank performance, efficiency and therefore its reliability and life-time [153]. The DC-link current ripple can be estimated in the worst condition as [154]:

$$\hat{I}_{dc,2\omega} = \frac{m\hat{I}_{sst}^{max}}{2} \approx 17.63\,\text{A} \tag{5.12}$$

Finally, considering the required capacitance given by (5.10), the rated DC voltage $V_{dc,sst} = 116$ V and DC ripple current to withstand given by (5.12), the selected capacitor bank is composed of seven *TDK/EPCOS* B43547A9687M000 each one providing 680 μF. Moreover, two additional film capacitors of 50 μF each, i.e. *TDK/EPCOS* B32776G4506K000, are connected in parallel with the DC-link bank, as suggest in [153]. This is because film

capacitors offer a fast dynamic response to high-frequency current requests, due to their inherent behavior. Finally, the total DC-link capacitance is 4.86 mF.

5.1.4 Heatsink Design

A single heatsink is considered for the B2B-PM, for being cost/effective while also guarantee a mechanical support to the whole power module structure, as whill be shown in next Section. Therefore, the heatsink must be capable of dissipating the thermal power produced by bot power modules of the B2B-PM. The maximum power to be dissipated, calculated in worst case scenario, is the one computed through equations (5.6), (5.7), (5.8), (5.9) and plotted in Fig. 5.2 for the *Infineon* IGBT module. That is:

$$P_{B2B-PM}^{max} \approx 94\,\mathrm{W} \tag{5.13}$$

The heatsink is then designed in order to maintain a maximum semiconductor junction temperature of $T_j = 125°\mathrm{C}$, considering an ambient temperature of $T_a = 50°\mathrm{C}$, as explain in [4].

5.2 PCBs Design and Final Assembly

Once the system ratings are known, the B2B-PM PCB designed is carried out through the software Altium Designer, for both the power and gate driver boards.

For the main power board, a two-layers PCB is selected. This is done to maximize the electrical isolation among the top and bottom layers. The PCB dimensions are chosen as to be able to fit all components needed while also guaranteeing the proper isolation between them and between power and signal circuits, while still realizing a compact layout. IGBT power modules are placed in the bottom side of the PCB and they are directly attached to the heatsink, that serves as mechanical support for the whole board. Three power connectors are displaced on the board: two of them represents the AC input and output terminals, while the third one provides a direct connection to the DC-bus, enabling the connection of possible external DC loads. Besides the main power module circuit represented in Fig. 5.1, an auxiliary signal circuitry is arranged on the PCB. This additional circuit is composed of a +15 V rail that serves as power supply for the PCB

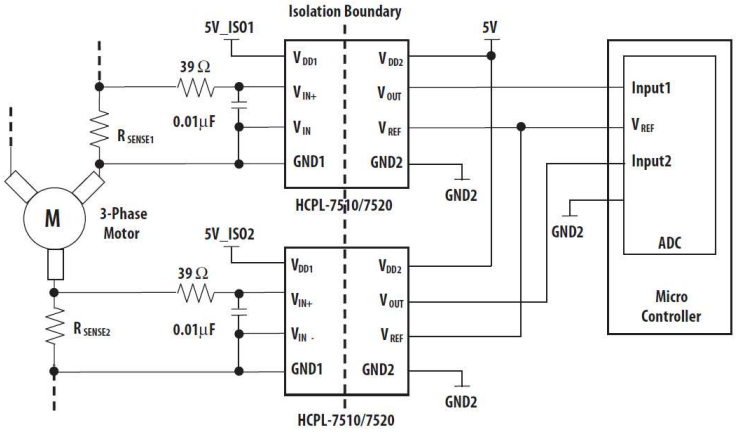


Figure 5.5: Three-phase current sensing circuit with HCPL-7510 [155].

utilities and of two isolated linear optocouplers used to measure the DC-link voltage and the DC-link current. This Integrated Circuits (ICs) are both HCPL-7510 produced by *Avago Technologies*. Their common configuration circuit as current sensing ICs (in the example for three-phase inverter-fed induction motors) is represented in Fig. 5.5 [155]. Because of their good bandwidth, in this work the HCPL-7510 is also used as voltage sensing ICs. The auxiliary +15 V rail is also employed as auxiliary power supplies for the gate drive circuits. The gate driver boards are placed directly on top of IGBTs top-layer footprint. These is done to reduce the current path between the gate drivers ICs and the IGBT power module, so as to avoid unwanted parasitic effects that may deteriorate the switching operation. Furthermore, in the whole layout crucial traces and planes are placed - when possible - so as to reduce as much capacitive and inductive parasitic effects.

Figure 5.6 and 5.7 show the top and bottom layers design for the power board, while Fig. 5.8 shows its 3-D view. Whilst, Fig. 5.9 and 5.12 show the top and bottom layers design for the gate driver board and Fig. 5.10 and 5.11 depict two inner layers. Fig. 5.13 shows the gate driver board 3-D view. Finally, Fig. 5.14a and 5.14b show both B2B-PM power stage and gate driver board once assembled and ready for validation tests.

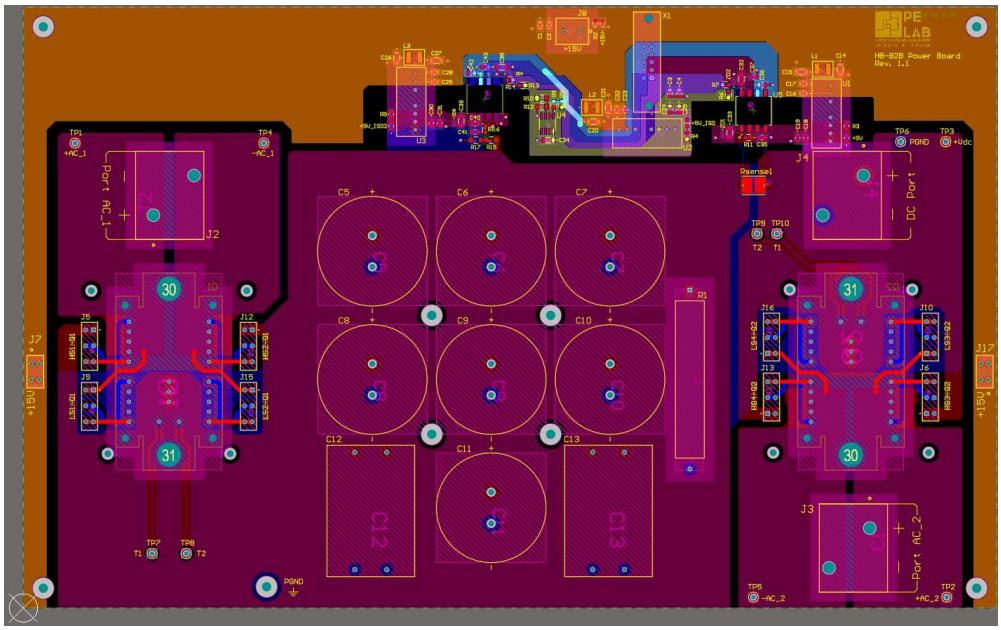


Figure 5.6: Top layer view of the power board.

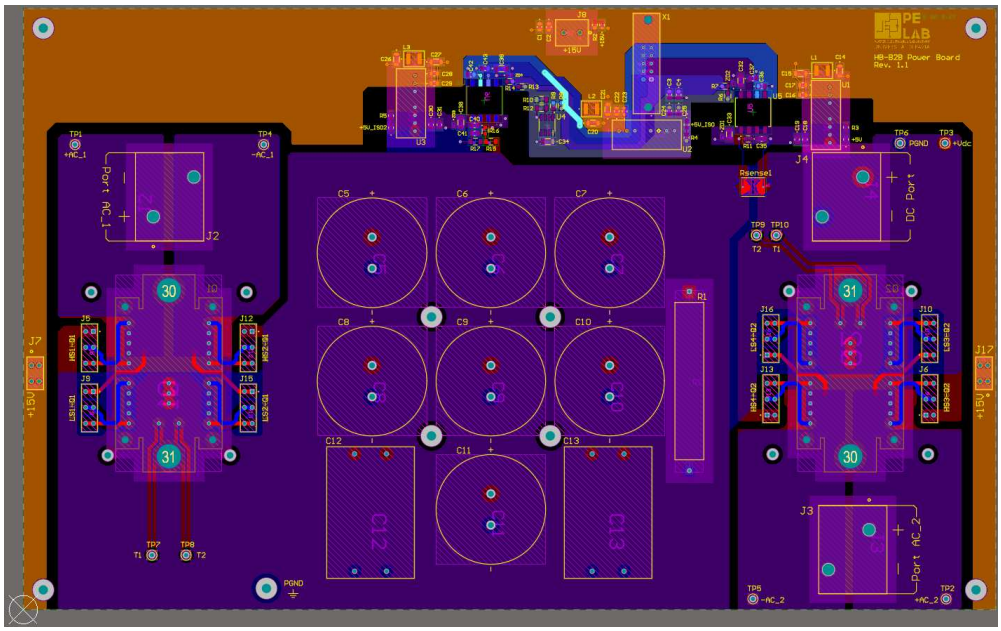


Figure 5.7: Bot layer view of the power board.

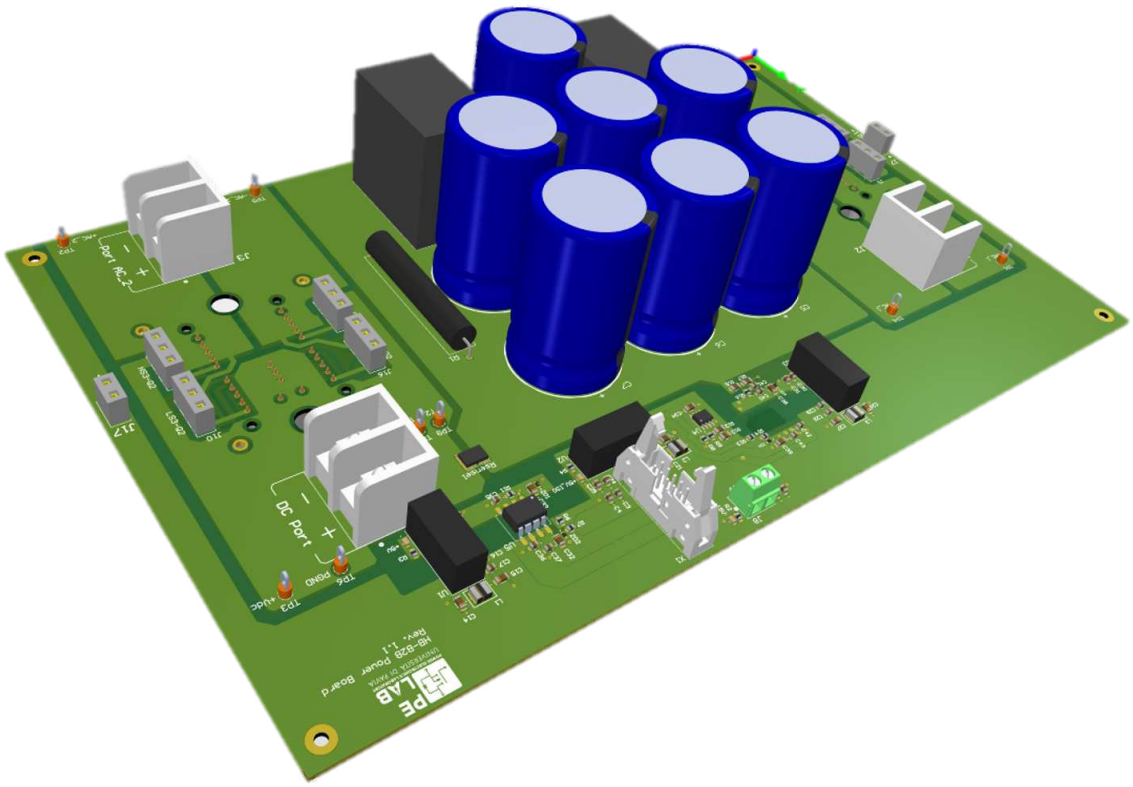


Figure 5.8: 3-D view of the B2B-PM main power board.

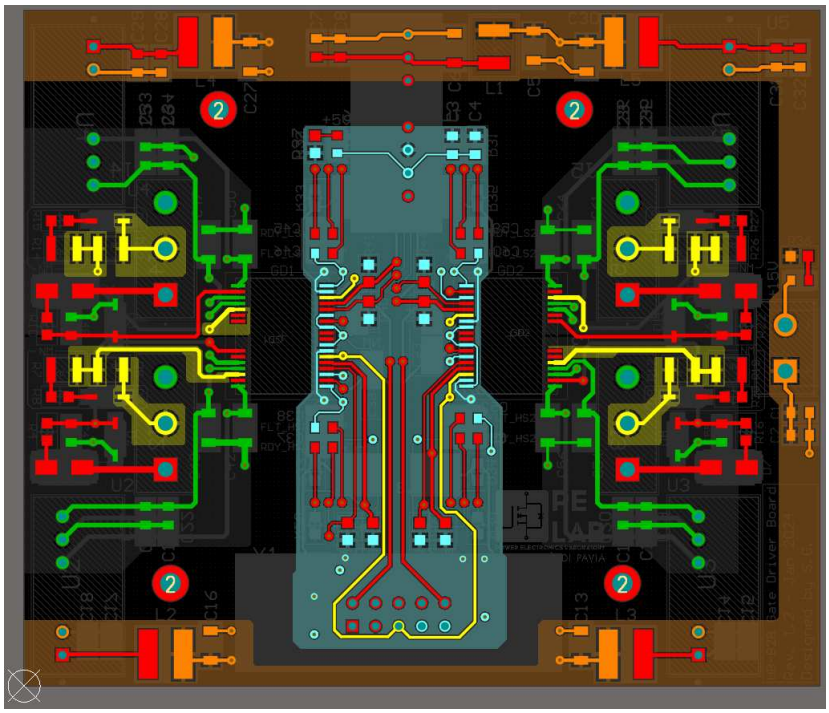


Figure 5.9: Top layer view of the gate driver board.

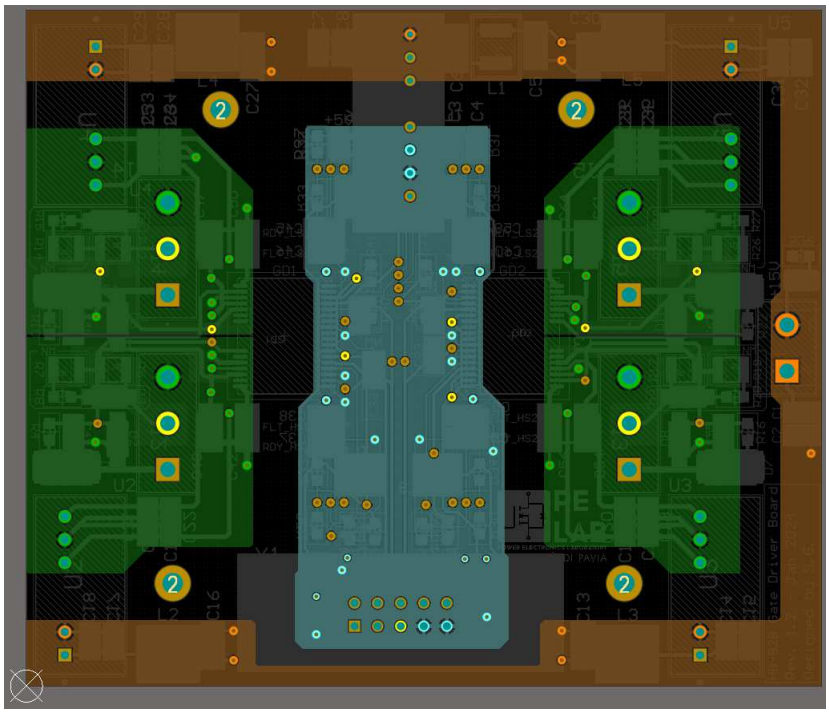


Figure 5.10: Top inner layer view of the gate driver board.

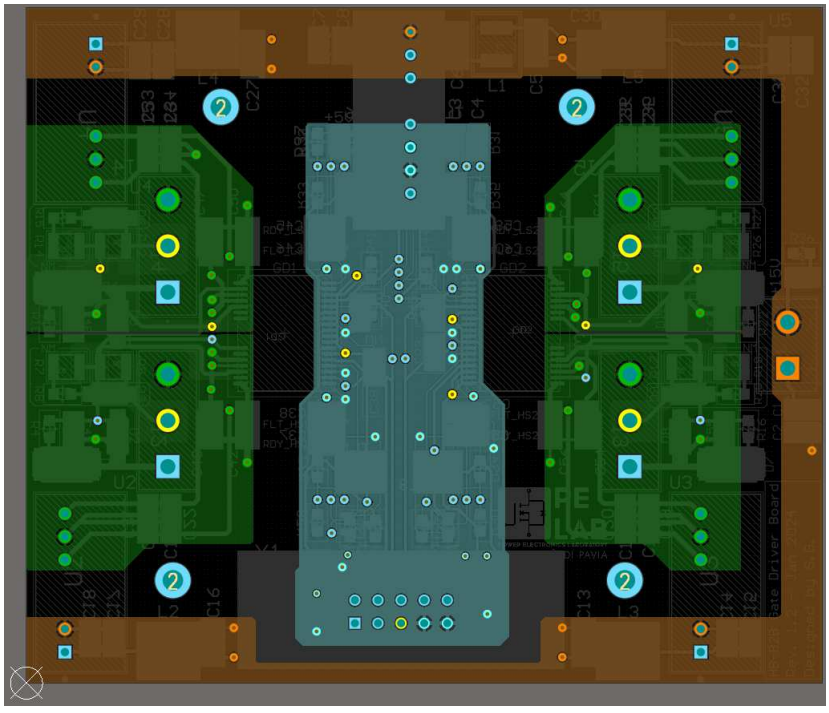


Figure 5.11: Bot inner layer view of the gate driver board.

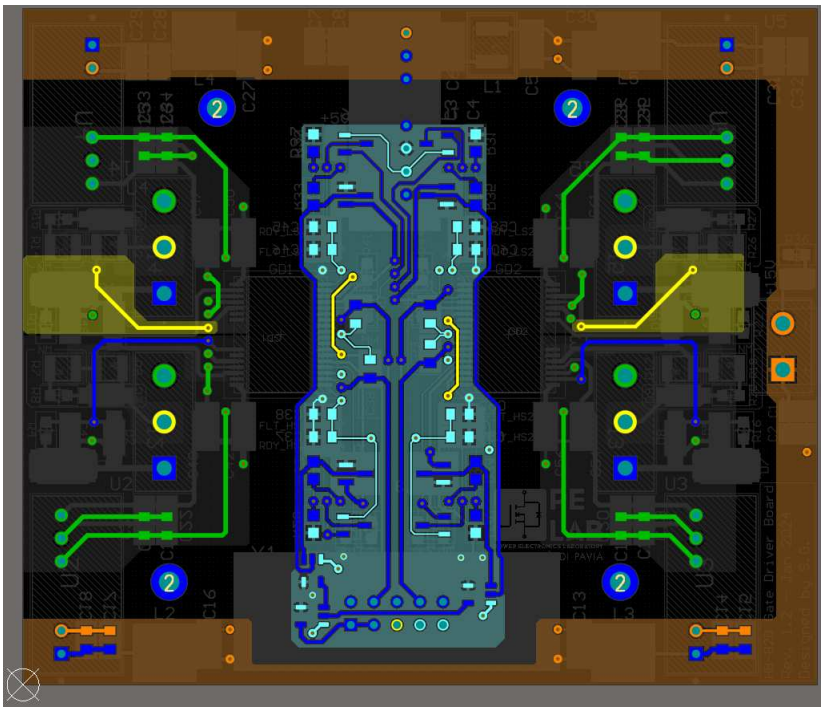


Figure 5.12: Bot layer view of the gate driver board.

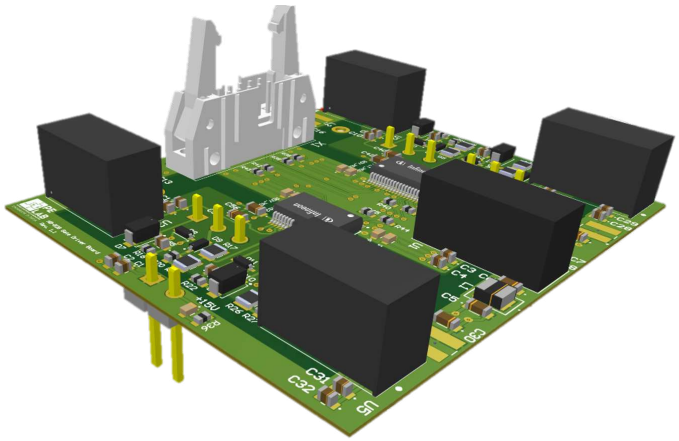
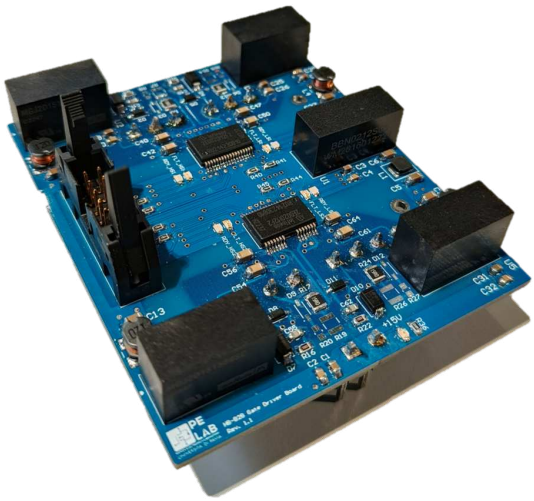


Figure 5.13: 3-D view of the gate driver board.

(a)



(b)

Figure 5.14: (a) HBH-PM and (b) gate driver boards finally assembled.

5.3 Open-Loop Power Module Test

Ultimately, open-loop loop tests are carried out to verify the proper operation of both power and gate driver boards. For this purpose, the following tests were planned:

1. No-load test: low-voltage no-load test, to verify the switching behavior under zero-current mode;

2. Light-load test: medium-voltage light-load test, to verify the effective operation of the B2B-PM board and gate driver boards when near to the rated conditions;

Both tests were carried out in open-loop. This is because the control system is still under development at the time this thesis is written. Therefore, open-loop generated modulating signals were manually provided to a modulator, whose generates the pulse patterns for the IGBTs. The control/modulator board used for the tests is PED-Board V3. That is a board designed by the University of Roma 3 and the Italian company Elettronica Dedicata. The board features a National Instruments (NI) System on Module sbRIO-9651 that provides a reconfigurable FPGA, Xilinx Zynq-7000, and an embedded real-time processor. The PED-Board conditions the NI chip ports and provides 30 PWM channels

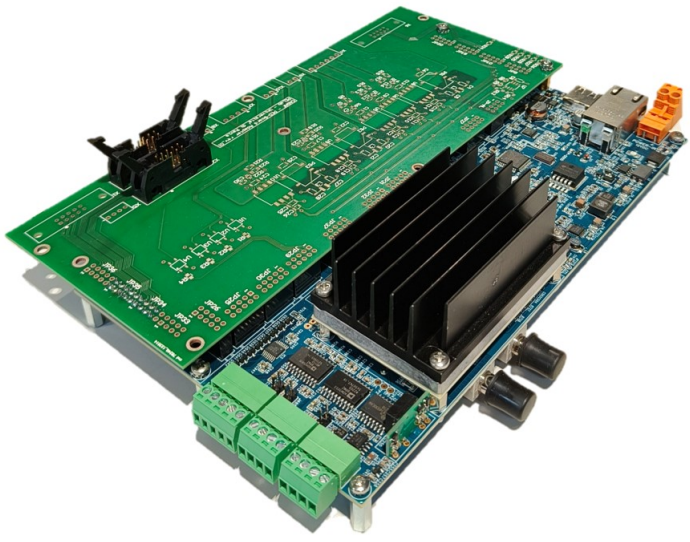


Figure 5.15: PED-Board V3 control board.

that can operate at either 0-5 V or 0-15 V, 16 ADC channels with 14-bit resolution, and 8 ADC channels with 10-bit resolution. Additionally, there are 46 digital input/output ports at 3.3V which can be conditioned to increase the number of PWM signals of the controller. Finally, the board also has 4 DAC channels and the communication protocols RS-485 and CAN-bus installed. The controller and modulator can be programmed via an Ethernet port using the software LabVIEW, which is a programming language that uses a graphical interface to create programs developed by National Instruments (NI).

5.3.1 No-load low-voltage open-loop test

First, the B2B-PM board is tested under no-load conditions. This is done to verify the switching behavior when no current is flowing in semiconductor circuits. The test setup is shown in Fig. 5.16, in which the B2B-PM board is tested without the heatsink to preliminary validate the power circuitry. Fig. 5.17 shows the switching transient of both legs of one H-Bridge installed on the B2B-PM that verifies the effective application of the

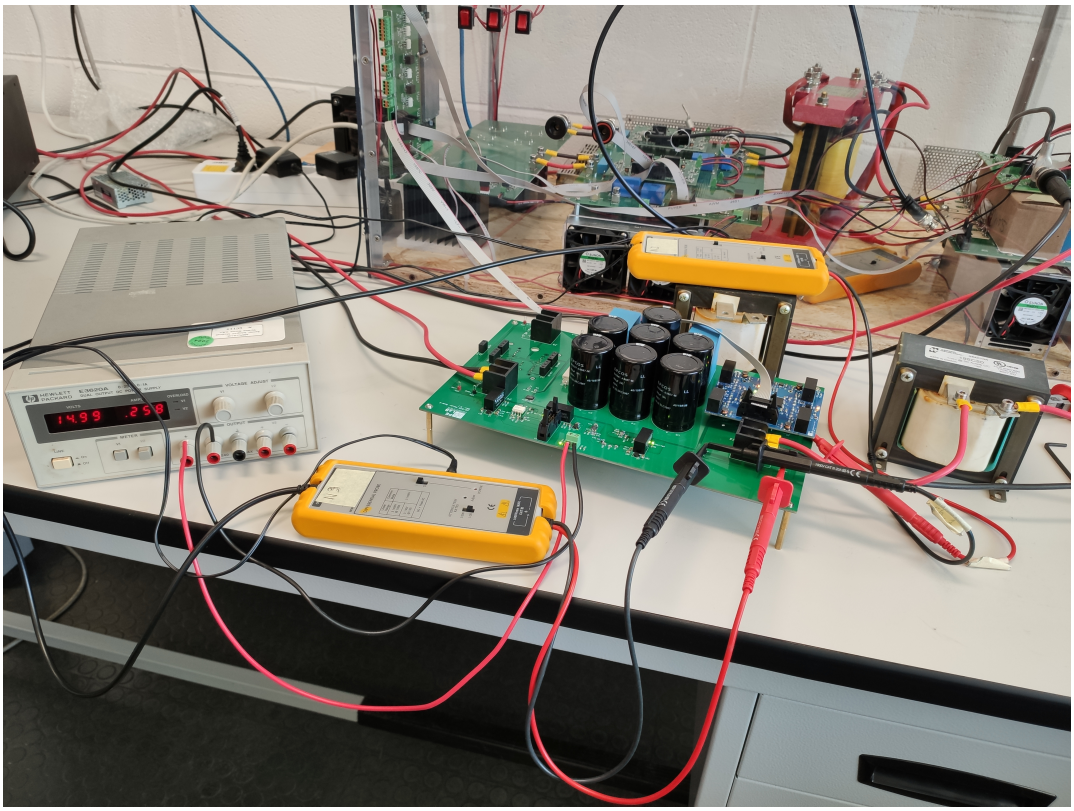
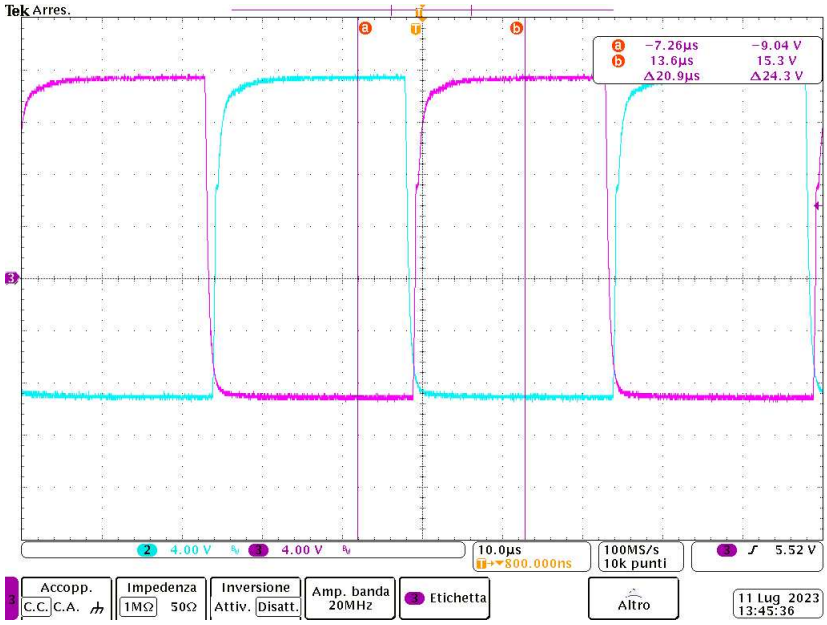
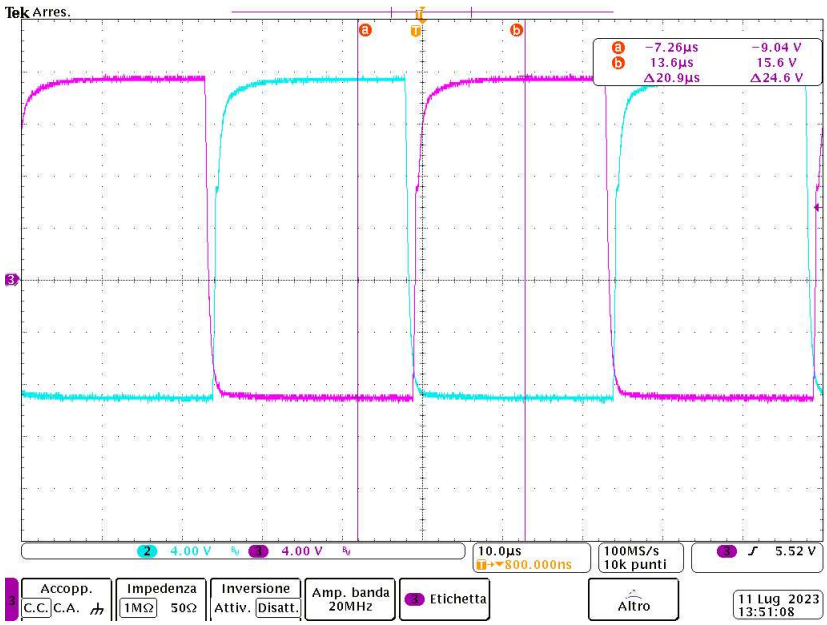


Figure 5.16: No-load low-voltage open-loop test setup.



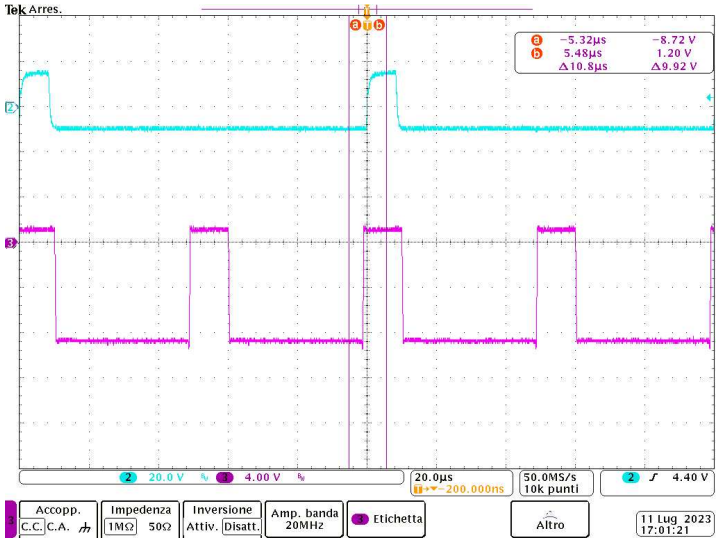
(a)



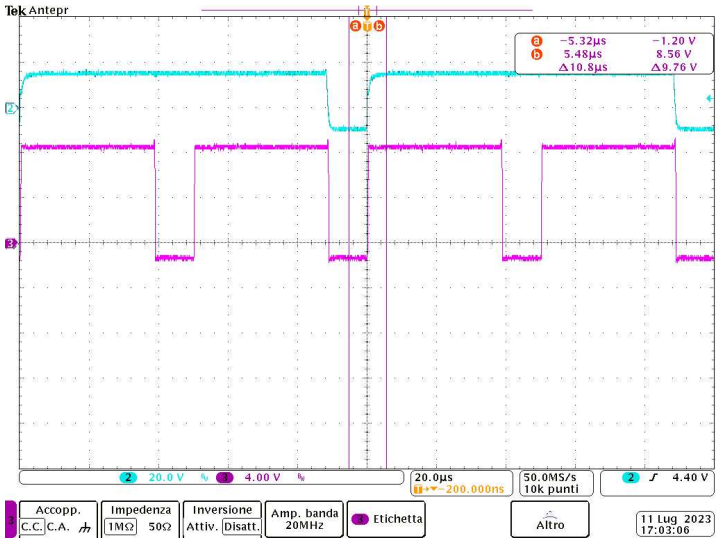
(b)

Figure 5.17: Gate drivers gate-emitter voltage under no-load condition: (a) top and bottom side switch of Leg A; (b) top and bottom side switch of Leg B

dead-time, to avoid short-circuits. Fig. shows the experimental results when the DC-link is supplied with a constant DC source that provides 10 V and one H-Bridge is switched on and off, according to a predefined duty cycle, to generate an AC waveform under no load. Fig. 5.18a refers to a positive duty cycle equal to $d = 0.8$, while in Fig. 5.18b the



(a)



(b)

Figure 5.18: (a) Output AC voltage waveform (cyan) of one H-Bridge and collector-emitter voltage (pink) of the top-side switch connected to the positive AC terminal in case of $d = 0.8$; (b) Output AC voltage waveform (cyan) of one H-Bridge and collector-emitter voltage (pink) of the bot-side switch connected to the negative AC terminal in case of $d = -0.8$;

duty cycle is set to be $d = -0.8$. As can be observed, in the first case the output AC waveforms is positive in average over one switching period, while in the second case it is negative as expected.

5.3.2 Light-load open-loop test

For this test, the B2B-PM board was supplied through the DC-link terminal with a constant DC voltage of 100 V. During the test, a resistive-inductive load was connected to the AC output terminals of one H-Bridge at a time. The load resistance was set to 12.3 Ω, while the inductance was 1 mH. Through the Ped-Board, the H-Bridge under test was switched in order to supply the load with an increasing AC pulsed voltage, till reaching the saturation of the modulating signal. Fig. 5.19 shows the test setup.

Fig. 5.20 shows the experimental results of the test when the modulation index is set to be $m = 0.9$, close to the saturation threshold. As can be observed from the red waveforms, the H-Bridge effectively creates a pulsed AC waveforms, and the resulting AC current is almost purely sinusoidal due to the inherent inductive nature of the load. The blue waveform shows the constant DC-link voltage provided by an external power supply. Moreover, Fig. 5.21a and 5.21b show the detailed switching transient of the high-side inverter IGBT when $m = 0.9$. As can be noted, even with current flowing in

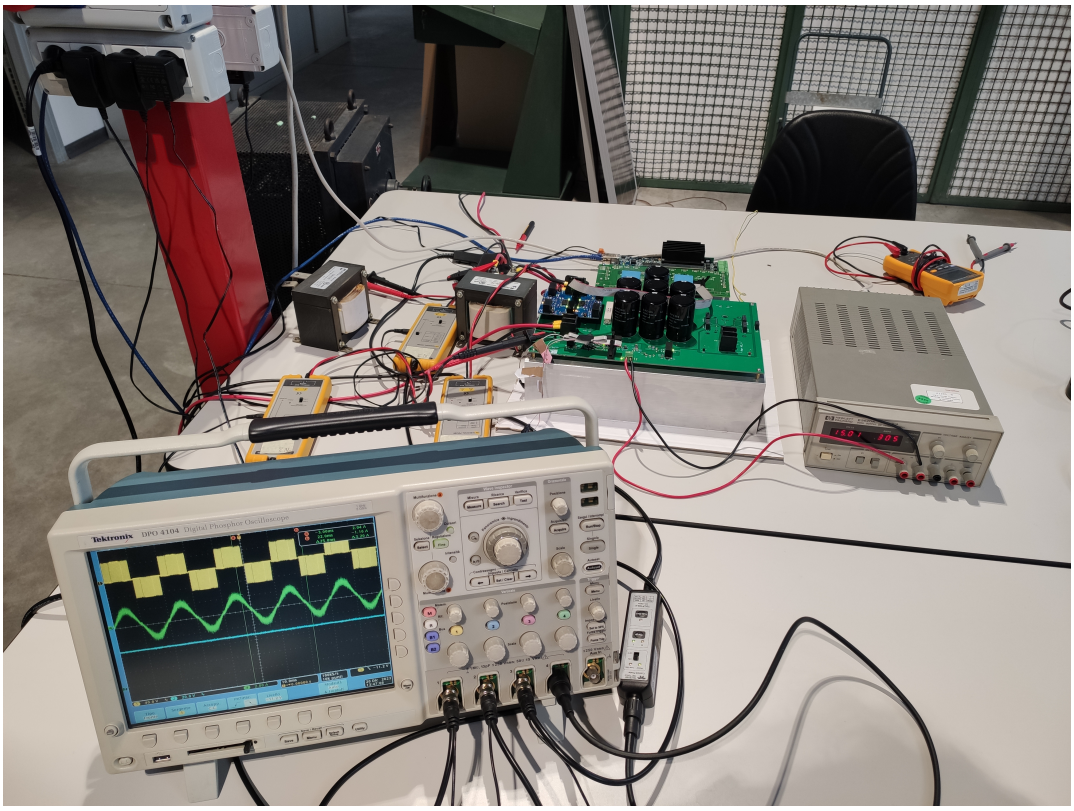


Figure 5.19: Light-load open-loop test setup.

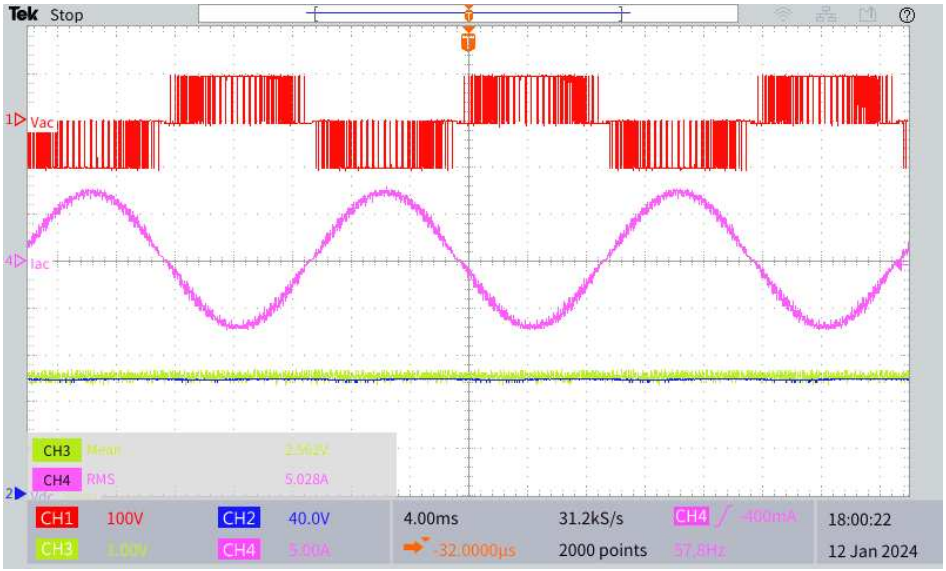
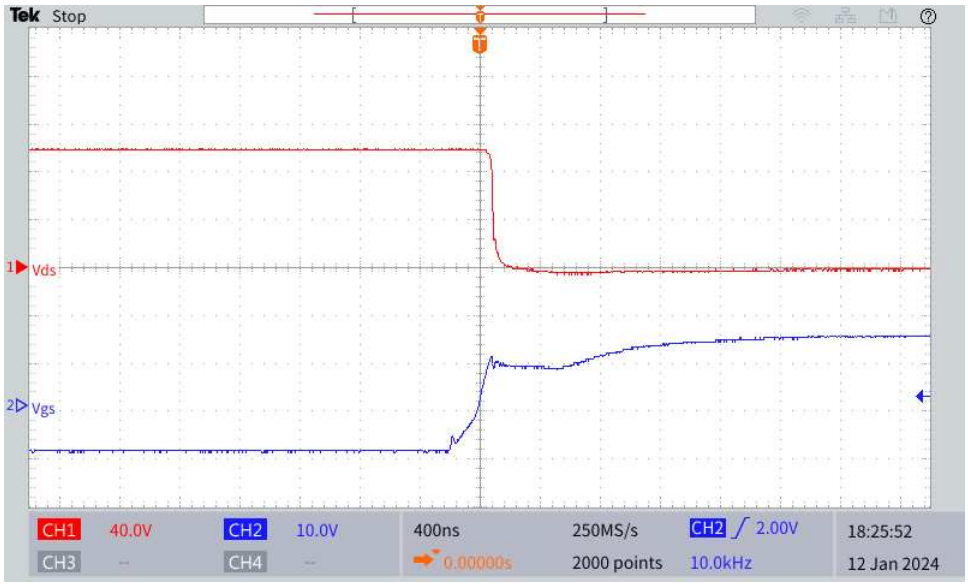
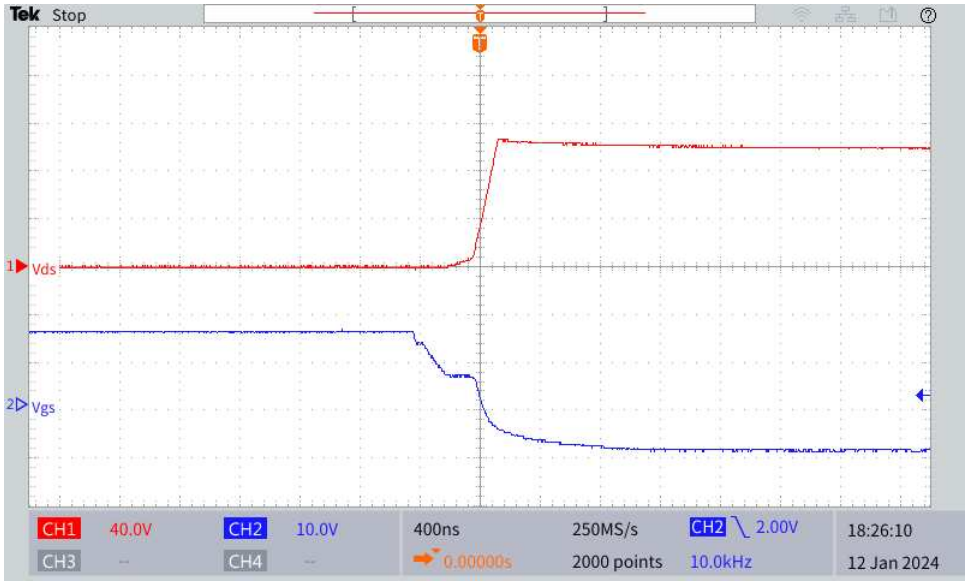


Figure 5.20: Light-load open-loop test setup.

semiconductors, the switching transient of the H-Bridge is good.



(a)



(b)

Figure 5.21: Collector-emitter (red) and gate-emitter (blue) voltages of the high-side inverter IGBT during light-load switching transient condition: (a) turn-on; (b) turn-off.

Chapter 6

Conclusion

The integration of Renewable Energy Sources (RES) and Distributed Generation (DG) and the widespread use of Electric Vehicles (EVs) and Energy Storage Systems (ESSs) have triggered a profound evolution process in the electrical distribution system. This requires a reliable and safe operation of the distribution system, which poses new challenges because of the intermittent nature of such loads and sources, interfaced with the grid via an increasing number of power electronics converters, along with a bidirectional power flow requirement. To address these challenges, the concept of Internet of Energy (IoE) or Energy Internet (EI) has emerged, which aims to reshape the current distribution grid into an intelligent and flexible active network. This involves a radical informatization process that involves the renewal of the grid communication infrastructure and the deployment of distributed monitoring points, as well as the implementation of advanced energy management and control functionalities to enable the safe, robust, effective, and efficient integration of intermittent sources and loads.

The Solid-State Transformer (SST) is envisioned as the best candidate for the future smart grid scenario due to its flexibility and advanced control features. The SST is a power electronic-based transformer that can provide advanced services and grid-supporting features, besides galvanic isolation and voltage adaptation, through its control system, and therefore is intended for replacing conventional Line Frequency Transformers (LFTs) at strategic nodes of the grid. The core isolation stage of the SST operates at high frequencies, enabling volume and weight reduction of the whole system compared to traditional and bulky LFTs.

In the IoE scenario, the most suitable SST configuration is the triple-stage one, consisting of three conversion stages. However, the SST control is intrinsically complex due to the large number of stages. The design of the overall control system is challenging because of the coupling among controllers. Additionally, multistage cascaded converters are significantly prone to instability due to interaction between converters. Furthermore, even if the SST is stable as a standalone system, it may become unstable when connected to the grid because of dynamic interactions with other grid-connected converters, leading the harmonic instability phenomenon.

6.1 Results and Conclusions

In light of the above, this thesis aimed to explore the SST stability issue from both the DC-bus and grid-connection perspectives, providing insights on the SST dynamics and offering a valuable design tool from both the control and system level aspects. The key points covered in this work are the following:

- The work developed in this thesis starts by reviewing the modern SST topologies and architectures, in order to clarify the current state-of-the-art of the SST technology. The main advantages and disadvantages of the most common SST structures, i.e. the single-stage, double-stage and triple-stage topologies, are also highlighted. The SST topology at the basis of this thesis is introduced, namely the UNIFLEX-PM. Moreover, existing applications and future trends are presented. In this context, with the current grid paradigm that tends to shift towards the so-called IoE scenario, suitable topologies for such applications are discussed as future ERs;

- In Chapter 2, the UNIFLEX-PM converter which constitutes the starting point of this thesis is reviewed with respect to the current available topologies. The MV AC-DC stage is discussed and a comparison between two well-known topologies, i.e. the MMC and CHB converters, is presented. Design rules are also highlighted. As for the AC-DC stage, also the DC-DC isolation stage, i.e. the DAB converter originally implemented on the UNIFLEX-PM, is introduced and its choice is motivated. These results allowed to confirm the UNIFLEX-PM topology as suitable SST architecture for the future IoE scenario;

- Chapter 3 presents the modeling of the whole SST system. This is required to developed the control system and, later, to assess the stability issue of the converter. Moreover, the SST average model allows to perform faster simulations. In this context, the CHB average and small-signal models are presented, both for the natural reference frame and for the synchronous reference frame. As for the CHB, the DAB small-signal model is also provided. Thereafter, the SST control architecture is presented. Special focus is posed on the CHB DC-link balancing control system, which for a three-phase topology consists of a three-layer regulation system. In particular, the cluster balancing loop is often omitted in the literature as the balance operation of the converter or of the grid is almost always assumed. Finally, simulation results verify the validity of the proposed SST model;

- In Chapter 4, the stability assessment of the SST is finally presented, from both DC-bus and grid-connection points of view. In the first case it was pointed out that that the direction of the power flow and the voltage rating at which the SST works may be sources of instability. The first issued is due to the non-symmetric control structure of the SST. In the second case, in particular the analysis aimed to discuss the input impedance matrix properties in terms of its passivity, thus helping the designer to achieve a stable grid-connected system. Through the derivation of a simplified expression for the d-axis impedance, it is demonstrated that the DC-DC load can increase the passivity region boundary. Also, a mention regarding the effect of the DC-DC stage on the inverter and reactive operation modes of the MV AFE, along with the impact on the synchronization loop (i.e. the PLL), is presented. These aspects are left open to future work.

- Finally, Chapter 5 concludes this work. The design of the modular SST structure under investigation is presented. In particular, a B2B-PM which consists of two H-Bridges interfaced via a DC-link is chosen as basic building block. The component selection is discussed and both power and gate driver PCB boards are designed. Ultimately, open-loop test verified the proper operation of the B2B-PM under both no-load and light-load conditions.

Based on that, from the author's perspective future research work challenges for the

selected UNIFLEX-based SST topology concerns the implementation of the third port, thus shifting towards a multi-port SST topology. From the topological review, more recent SST topologies based on multi-port DC-DC converters might be considered to solve the intrinsic problem of the UNIFLEX-PM converter, highlighted in Chapter 2. From the stability point of view, modeling the interactions among different ports and, especially, among different controllers is challenging and is still almost an open topic today. Furthermore, advanced SST control approaches such as the grid-forming control should be considered and analyzed from the stability perspective.

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