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Design of a High Efficiency Inverting Buck-Boost Converter for OLED Displays

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Abstract

This thesis addresses the design of high-efficiency inverting DC–DC converters for AMOLED display applications in mobile devices. AMOLED panels require negative bias voltages whose magnitude varies with operating conditions and luminance, imposing stringent constraints on efficiency, silicon area, and passive component count in power management integrated circuits.

The work presents a comprehensive analysis of different converter topologies, including inductive, switched-capacitor, and hybrid solutions. Their operating principles, advantages, and limitations are discussed with particular attention to efficiency, scalability, and integration feasibility. Hybrid architectures combining inductors and flying capacitors are shown to offer an effective trade-off between performance and implementation complexity.

A switched-capacitor inverting buck–boost converter is identified as a particularly suitable solution for the target application. Analytical models are developed to describe its steady-state operation, power losses, and design constraints, enabling an in-depth understanding of the key trade-offs among switching frequency, passive component sizing, efficiency, and silicon area.

An optimization methodology for power switch sizing under area constraints is proposed, allowing efficient operation across a wide load range in advanced CMOS technologies. In addition, a dedicated control strategy is introduced to address capacitor voltage balancing in multi-level architectures, ensuring stable operation without additional sensing circuitry. Simulation results validate the effectiveness of the proposed design and control approaches.

Overall, this thesis provides a systematic design framework for inverting DC–DC converters in low-power integrated applications, offering methodologies and insights that can be extended to a broad class of power management systems beyond AMOLED displays.

Chapter 1

Introduction

In recent years, Organic Light Emitting Diode (OLED) displays have progressively replaced traditional Liquid Crystal Displays (LCDs) in a wide variety of electronic devices, including smartphones, wearable electronics, tablets, automotive dashboards, and consumer televisions. This widespread diffusion is mainly driven by the superior characteristics of OLED technology in terms of contrast ratio, response time, color gamut, power efficiency, and mechanical flexibility. Furthermore, since OLEDs are self-emissive devices, no backlight is required, enabling the realization of ultra-thin, flexible, foldable, and even transparent displays.

OLED displays can be classified into two main categories: Passive Matrix OLED (PMOLED) and Active Matrix OLED (AMOLED). In PMOLED displays, the pixel matrix is driven by orthogonal row and column electrodes, while each pixel can be modeled as a diode connected between the supply lines. A simplified view of the PMOLED panel and of the corresponding pixel equivalent circuit is shown in Fig. 1.1.

Due to the absence of local storage elements, only one row can be actively driven at a time in PMOLED panels. This limitation severely restricts the achievable resolution, maximum display size, brightness, and lifetime.

In contrast, AMOLED displays employ a Thin Film Transistor (TFT) active matrix with a storage capacitor integrated into each pixel. This architecture allows every pixel to preserve its state even when it is not directly addressed, enabling higher brightness levels at lower driving voltages, improved uniformity, and longer lifetime. A simplified representation of an AMOLED panel and the corresponding pixel equivalent circuit is reported in Fig. 1.2.

For these reasons, AMOLED technology currently represents the dominant solution for medium- and high-resolution portable electronic devices.

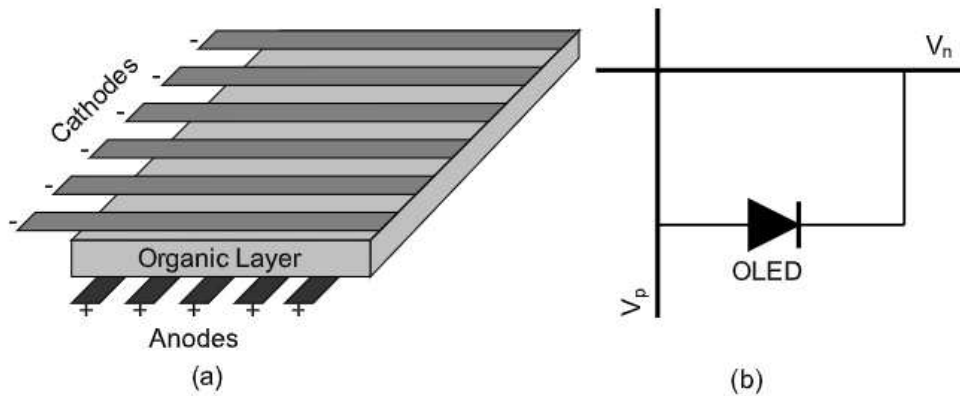


Figure 1.1: Simplified schematic of a PMOLED display: (a) matrix architecture with row and column electrodes, (b) equivalent electrical pixel model.

1.1 Power Supply Requirements of AMOLED Displays

AMOLED panels require multiple regulated supply voltages to properly bias the pixel circuits, data drivers, and gate drivers. In particular, alongside the positive supply voltage, a negative voltage rail is required for the correct operation of the pixel driving transistors and the analog front-end circuitry. Since mobile devices are powered by a single lithium-based battery whose voltage typically ranges from approximately 2.0 V to 5.5 V, dedicated DC–DC conversion stages are mandatory to generate the required negative voltage levels, commonly ranging from -3 V down to -10 V.

The design of such converters is particularly challenging due to:

- the high output current required by modern high-resolution AMOLED panels;
- stringent efficiency constraints to maximize battery lifetime;
- strict limits on external component size and count (low Bill of Materials, BOM);
- tight constraints on output voltage ripple and electromagnetic interference (EMI).

The inverting buck–boost converter represents the most straightforward solution for generating a negative voltage from a positive input supply. However, when operated at high output current and large conversion ratios, conventional inverting buck–boost converters suffer from severe drawbacks, including high inductor current stress, large current ripple, high conduction and switching

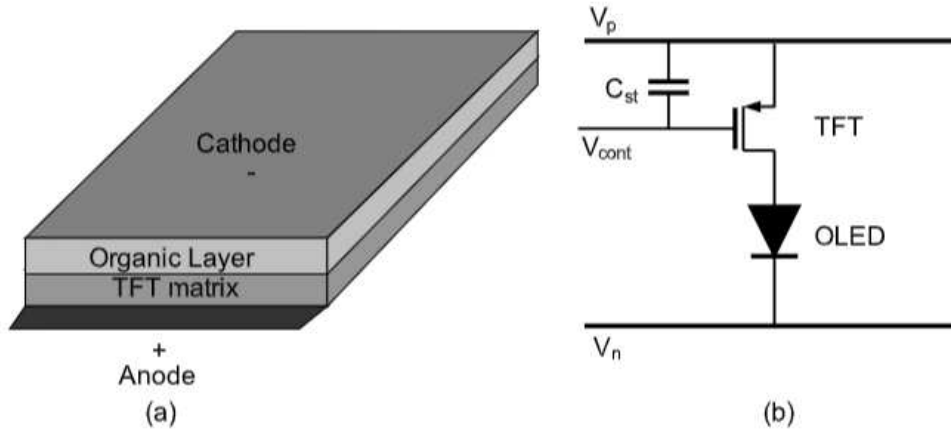


Figure 1.2: Simplified schematic of an AMOLED display: (a) active-matrix architecture, (b) equivalent electrical pixel model with driving TFT and storage capacitor.

losses, and limited achievable efficiency. These limitations motivate the exploration of advanced conversion architectures.

1.2 Motivation for Multi-Level and Switched-Capacitor Architectures

Multi-level power converters were originally developed for medium- and high-voltage power electronics applications. More recently, thanks to the continuous advances in semiconductor devices and the widespread availability of high-performance multilayer ceramic capacitors (MLCCs), multi-level and switched-capacitor architectures have become highly attractive also for low-voltage, high-current consumer applications, such as AMOLED display power management systems.

Compared to conventional single-stage converters, these techniques allow:

- reduction of voltage stress across power switches;
- reduction of inductor current ripple;
- improved power conversion efficiency;
- smaller passive components.

Among the various multi-level solutions, three-level architectures represent an excellent compromise between complexity, performance, and component count, especially in space-constrained applications. Nevertheless, despite

the growing interest in these techniques, the application of multi-level and switched-capacitor concepts to inverting buck–boost converters for AMOLED display drivers remains only partially explored in the literature, and a comprehensive comparison among classical, multiphase, switched-capacitor, and three-level inverting solutions is still lacking.

1.3 Objectives and Original Contributions

The main objective of this Ph.D. work is the design, analysis, and experimental validation of a high-efficiency inverting DC–DC converter optimized for AMOLED display drivers, operating under the following specifications:

- input voltage range: 2.0 V–5.5 V;
- output voltage range: -3 V – -10 V ;
- maximum output current: up to 1 A;
- output voltage ripple: below 50 mV;
- target efficiency: significantly higher than 90%;
- strong optimization of external component size and BOM.

Starting from the limitations of the conventional inverting buck–boost converter, this thesis systematically investigates several enhanced topologies, including:

- multiphase inverting converters;
- switched-capacitor assisted converters;
- multi-level inverting converters.

This analysis leads to the proposal of a novel switched-capacitor three-level inverting buck–boost architecture, specifically conceived to simultaneously reduce:

- average inductor current;
- inductor current ripple;
- switch voltage stress;
- overall power losses.

In addition to the power stage, particular attention is devoted to the design of the flying capacitor voltage control loop, which is a key element for the correct and stable operation of the proposed three-level topology.

The main original contributions of this thesis can be summarized as follows:

1. A comprehensive theoretical comparison of classical, multiphase, switched-capacitor, and three-level inverting buck–boost converters under AMOLED-relevant operating conditions.
2. The proposal of a new switched-capacitor three-level inverting buck–boost topology capable of achieving high conversion ratios with reduced

inductor stress.

3. The development of a dedicated flying capacitor voltage balancing and control loop, specifically tailored to the proposed architecture.
4. The definition of a power switch sizing and optimization strategy aimed at maximizing efficiency under strict silicon area constraints.
5. The complete design flow including simulations, layout, and experimental validation on silicon.
6. A detailed comparison with the state of the art, demonstrating the advantages of the proposed solution in terms of efficiency, current stress, voltage ripple, and component count.

1.4 Thesis Organization

The rest of this thesis is structured as follows:

- Chapter 1 introduces the fundamental theory of DC–DC converters and reviews inductor-based switching converters, with particular focus on inverting buck–boost architectures.
- Chapter 2 presents the systematic theoretical analysis of the investigated topologies and introduces the proposed switched-capacitor three-level inverting buck–boost converter.
- Chapter 3 describes the power switch modeling, sizing strategy, and the complete circuit implementation.
- Chapter 4 focuses on the design and stability analysis of the flying capacitor voltage control loop, including small-signal modeling and simulation-based validation.
- Chapter 5 reports the post-layout simulations and the experimental measurement results obtained from the fabricated prototype.
- Chapter 6 summarizes the main achievements of the work, discusses its limitations, and outlines possible future research developments.

Chapter 2

DC-DC Converters

In a mobile device the battery supplies a variable voltage that is dependent on the charge level. A DC-DC converter is a circuit that provides a stable voltage from the one supplied by the battery, while also being able to increase it, reduce it or invert its sign. Parameters employed in order to characterize converters are range of conversion, output voltage stability (ripple), noise and efficiency defined as:

$$\eta = \frac{P_{out}}{P_{in}} \quad (2.1)$$

where P_{out} is the converter output power and P_{in} the converter input power. Converters can be classified in three families based on the components used [1]:

- Linear Regulators are circuits only able to provide a voltage lower than the supply. They have the advantages of requiring a small area, while having no need for external components, and providing a low noise output; however they feature a low efficiency. This type of converters is not taken into consideration in this thesis because of the high efficiency requirement of this particular project.
- Switched Capacitor converters are based on the switching of a charged capacitor to provide a higher or lower voltage than the supply. They need a larger area with respect to linear regulators but have higher efficiency.
- Inductive-based Switching Converters make use of the inductor's inability to change instantaneously its current to regulate the voltage at the output. By correctly steering the current with switches, it is possible to provide an output voltage increased, reduced and also inverted with respect to the input voltage. They can reach a very high efficiency, however the required inductance value usually does not allow employing integrated inductors, therefore a bulky external component is required.

Another distinction can be made based on the performed conversion:

- Boost, which provides voltages higher than the supply.
- Buck, which provides voltages lower than the supply.
- Buck-Boost, that can perform both previous operations.
- Inverting Buck-Boost, that can also change the sign of the supply voltage.

2.1 Switching Converters

The analysis of an inductor-based switching converter can be rather difficult considering the circuit is time dependent, however some approximations can be made in order to simplify the calculations. The output voltage of a converter is ideally constant but, as it is impossible to build the perfect low-pass filter, in practice a ripple remains. This output voltage ripple is very small in a well-designed converter, so it is reasonable to assume it is much smaller than the DC component and neglect it. This approximation, known as the small ripple approximation, greatly simplifies the analysis and will be employed throughout the rest of this thesis.

The analysis process is aimed at finding the conversion ratio :

$$M = \frac{V_{out}}{V_{in}} \quad (2.2)$$

which depends on the duty cycle of the switch. The operation of the converter is periodic: this means that eventually a point in time is reached when the net change of the currents and voltages of the circuit is zero over a complete switching period, and the converter operates in steady state. From this assumption two important principle can be found [2]:

- Inductor volt-second balance: the integral over the period of the voltage over an inductor is equal to zero.
- Capacitor charge balance: the integral over the period of the current flowing through a capacitor is zero.

Relying on the illustrated principles, every switching DC-DC converter can be analysed employing the following process:

1. Calculate inductor voltages and capacitor currents for each phase;
2. Apply the two principles previously mentioned;
3. Resolve the system of equations to find the conversion ratio.

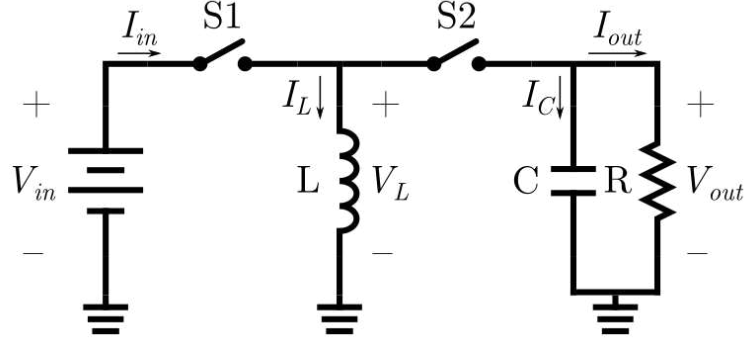


Figure 2.1: Inverting buck-boost circuit.

2.1.1 Inverting Buck-Boost Converter

The circuit shown in Fig. 2.1 is the standard inductor-based inverting buck-boost converter which provide a negative output as required by the target application. As described previously, the analysis is started by calculating the inductor voltage and capacitor current for each phase. For the first phase switch $S1$ is closed and switch $S2$ is open, vice versa in the second phase as shown in Fig. 2.2 where $D' = (1 - D)$. The results are:

$$V_L = \begin{cases} V_{in} & \text{in Phase 1} \\ V_{out} & \text{in Phase 2} \end{cases} \quad I_C = \begin{cases} -I_{out} & \text{in Phase 1} \\ -I_{out} - I_L & \text{in Phase 2} \end{cases} \quad (2.3)$$

Now applying the volt-second balance and the capacitor charge balance principles, the following equations are derived:

$$\begin{aligned} \int_0^{T_s} V_L dt &= V_{in} * DT_s + V_{out} * (1 - D) T_s = 0 \\ \int_0^{T_s} I_C dt &= -I_{out} * DT_s + (-I_{out} - I_L) * (1 - D) T_s = 0 \end{aligned} \quad (2.4)$$

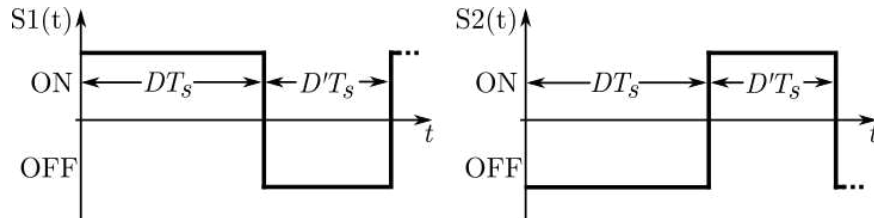


Figure 2.2: Inverting buck-boost switching phases.

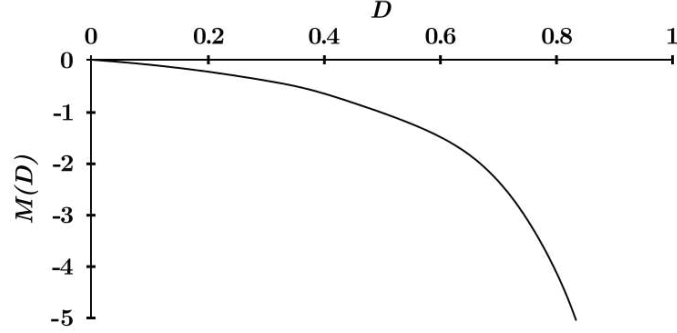


Figure 2.3: Conversion ratio $M(D)$ of the standard inverting buck-boost.

The last step is to resolve for the conversion ratio $M(D) = \frac{V_{out}}{V_{in}}$ and for the inductor current:

$$\begin{aligned}
 V_{in} * DT_s + V_{out} * (1 - D) T_s &= 0 \quad \Rightarrow \\
 V_{out} * (1 - D) \cancel{T_s} &= -V_{in} * D \cancel{T_s} \quad \Rightarrow \\
 V_{out} &= -V_{in} * \frac{D}{(1 - D)} \quad \Rightarrow \quad M(D) = -\frac{D}{(1 - D)}
 \end{aligned} \tag{2.5}$$

$$\begin{aligned}
 -I_{out} * DT_s + (-I_{out} - I_L) * (1 - D) T_s &= 0 \quad \Rightarrow \\
 -I_{out} * D \cancel{T_s} &= -(-I_{out} - I_L) * (1 - D) \cancel{T_s} \quad \Rightarrow \\
 I_{out} * D + I_{out} * (1 - D) &= -I_L * (1 - D) \quad \Rightarrow \\
 I_L &= -I_{out} * \frac{1}{(1 - D)}
 \end{aligned} \tag{2.6}$$

It can be seen from (2.5) that in fact the conversion ratio is negative, which means that the output voltage will be opposite to the input voltage: by varying $0 < D < 1$ we get $0 < M(D) < -\infty$ as shown in Fig. 2.3.

From (2.6) it can be noticed that the inductor current will always be equal or greater in modulus than the output current and this will be a limit for this type of architecture.

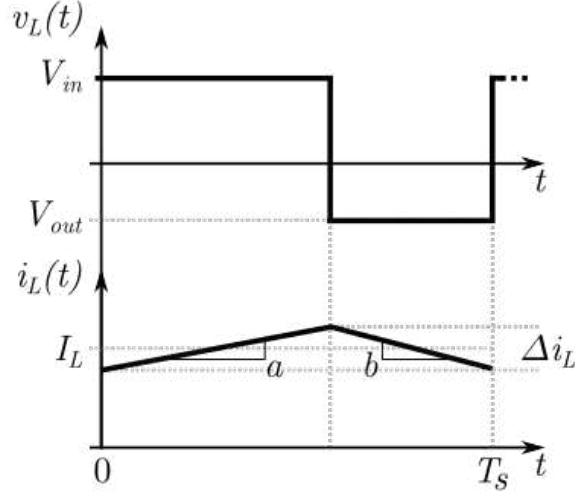


Figure 2.4: Inductor waveform of the inverting buck-boost.

Fig. 2.4 shows the inductor voltage and current waveform in more detail. Since the inductor voltage is constant in each phase, the current waveform is formed by a series of ramps with a slope given by:

$$a : \frac{V_{in}}{L}, \quad b : \frac{V_{out}}{L} \quad (2.7)$$

The ripple amplitude is then computed by multiplying the slope by the corresponding phase duration:

$$\Delta i = \frac{V_{in}}{L} DT_s \quad (2.8)$$

The voltage ripple at the output can be computed in a similar way. Considering the inductor current constant and equal to its average it can be said that the voltage waveform on the capacitor will be composed by ramps as shown in Fig. 2.5. As for the inductor the slope in each phase is:

$$a : -\frac{I_{out}}{C} = -\frac{V_{out}}{CR} > 0, \quad b : \frac{-I_{out} - I_L}{C} < 0 \quad (2.9)$$

In the first phase the slope is positive, since the output voltage is negative (supposing a positive input voltage), in the second phase the slope is negative because $-I_{out} > 0$ and $|I_L| > |I_{out}|$.

The output voltage ripple is:

$$\Delta v = \frac{V_{out}}{CR} DT_s \quad (2.10)$$

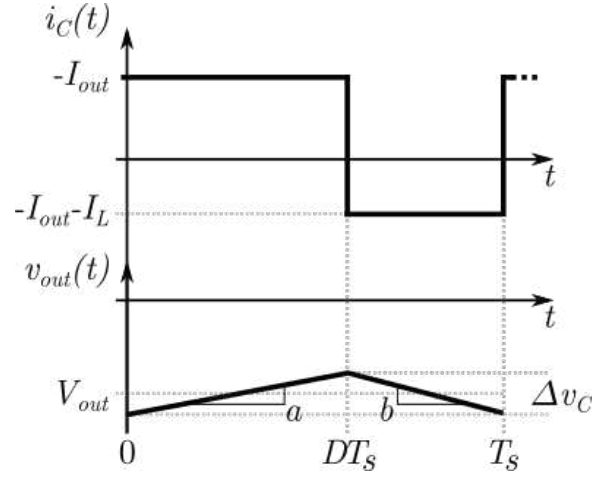


Figure 2.5: Output capacitor waveform of the inverting buck-boost.

In order to have an idea on which voltage rating the switches in the circuit require, it is useful to look at the voltage seen by each switch when closed:

Switch	Phase 1	Phase 2
$S1$	-	$V_{in} - V_{out}$
$S2$	$V_{in} - V_{out}$	-

Table 2.1: Switch supported voltage for the standard inverting buck-boost.

2.2 Switched Capacitor Doubler

An example of switched capacitor converters mentioned at the beginning of Chapter 2 is the switched capacitor doubler. The standard switched capacitor doubler circuit is shown in Fig. 2.6, where C_{out} represents an ideal load. Switch $S1$ and $S3$ have the same control signal, which is opposite to the one of switch $S2$ and $S4$ which work together. In this way when $S1$ and $S3$ are closed the capacitor C is charged to V_{in} , then when $S2$ and $S4$ are closed the bottom plate of capacitor C is connected to V_{in} bringing the top plate and the output to $2V_{in}$. If we consider a duty cycle of 50% as long as the switching frequency is high enough the voltage output is maintained constant.

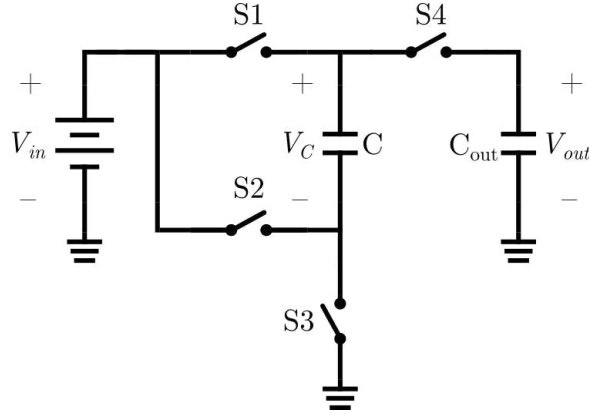


Figure 2.6: Standard switched capacitor doubler circuit.

2.3 Parasitics and Non-Idealities

Until now all components have been considered as ideal but in reality inductors and capacitors suffer from parasitics.

Real inductors have a maximum current that they can support and a parasitic resistance that accounts for dissipation. Moreover, when an alternating current flows in an inductor, a parasitic effect takes place, determining core losses that increase dissipation. This effect depends on the parameters of the component, on the frequency and the amplitude of the current ripple. A good design therefore should limit the ripple on the inductor as a primary target.

A real capacitor has a maximum voltage that it can support and a parasitic resistance that accounts for dissipation. Real capacitors are also affected by de-rating, which degrades their capacitance values when the average voltage applied to the capacitor increases.

Switches are implemented with transistors and diodes that have a non-zero on resistance when closed and a limited voltage rating when open. In general if we consider two transistors with the same size, the one with the higher voltage rating typically features the worst performance in terms of on resistance. For these reasons, it is useful to find a way to limit the number of on transistors in series and try to design the converter in order to employ switches with lower voltage ratings.

These problems can be addressed by employing appropriate topologies, such as multiphase or multilevel solutions, which will be discussed in the next chapter.

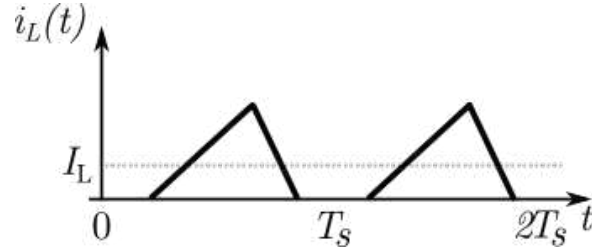


Figure 2.7: DCM inductor current

2.4 Continuous Conduction Mode

All the analyses were performed considering the converter in CCM (continuous conduction mode) which means that the current continuously flows through the inductor. In CCM it is assumed that the current flowing through the circuit is unidirectional; this however is not verified especially in case of light load, when the inductor current ripple is higher than the average inductor current. In such cases, operation in DCM (discontinuous conduction mode) [3] as shown in Fig. 2.7, is considered instead. The analysis process for DCM operation is substantially the same as for CCM: the two principles of inductor volt-second balance and capacitor charge balance still hold, but extra care is required when applying the small ripple approximation, especially on the inductor current as its ripple can no more be considered negligible. In DCM the behaviour of the converter changes significantly: the output voltage becomes load-dependent. For this reason in some converters, when in light load, the control system no longer employs PWM in order to avoid problems. Even if DCM seems a more complex operation mode, some converters are designed specifically to work only in DCM in order to take advantage of the change in the conversion ratio. For this preliminary analysis the behaviour in DCM of the converter will not be considered.

Chapter 3

Proposed Inverting Buck-Boost Converter

In this chapter, the project specifics and the reasoning why a new architecture is needed for this particular case will be presented, first highlighting the limits of the common solutions and then fully analysing the new proposed circuit in order to finally present a comparison.

The specifics are:

- Input Range: $2.0 \sim 5.5V$
- Output Range: $-3 \sim -10V$
- Maximum Load current: $1A$
- Efficiency $\gg 90\%$
- Optimized for efficiency and BOM
- Low output voltage ripple ($< 50mV$)

Another constraint is presented by the maximum size of the external components which cannot be higher than 1 mm and need to fit a precise size. The allowed footprints are: 0402/0603/0805 for the capacitors and 2016/2025 for the inductors.

Since the inductor is the most critical component, a research on inductors available on the market was performed to find a coil that fits all the requirements. A Samsung device has been selected for its high inductance of $1 \mu H$, the very low parasitic resistance of $25 m\Omega$, the high saturation current of 5 A and a footprint size adequate for the project. Its core losses can be computed with:

$$Core Losses = c_1 * (f_i)^{c_2} * (c_3 * \Delta i)^{c_4} \quad (3.1)$$

where $c_1 = 1,261 * 10^{-6}$, $c_2 = 1,207$, $c_3 = 0.0326$, $c_4 = 2.353$ for the chosen inductor, f_i is the inductor current ripple frequency and Δi is the ripple am-

plitude.

For all the following cases a switching frequency of $f_s = 1 \text{ MHz}$ ($T_s = 1 \text{ } \mu\text{s}$) has been considered. As a starting point the standard inverting buck-boost was taken into consideration. This topology has been already analysed in the previous chapter, as a reminder:

$$M(D) = -\frac{D}{(1-D)}, \quad I_L = -I_{out} * \frac{1}{(1-D)}, \quad \Delta i = \frac{V_{in}}{L} D T_s \quad (3.2)$$

Considering a few of the different conversion ratios cases that are required by the application, the results shown in Tab. 3.1 are derived relying on (3.2).

$V_{in}[V]$	$V_{out}[V]$	$I_{out}[I]$	<i>Duty Cycle</i>	$I_L[A]$	$\Delta i[A]$
3.3	-5	0.1	0.602	0.25	2.00
3.3	-10	0.1	0.751	0.40	2.50
5.5	-10	0.1	0.645	0.28	4.00
2.0	-10	0.1	0.833	0.60	1.70
3.3	-5	0.5	0.602	1.25	2.00
3.3	-10	0.5	0.751	2.00	2.50
5.5	-10	0.5	0.645	1.40	4.00
2.0	-10	0.5	0.833	3.00	1.70
3.3	-5	1	0.602	2.50	2.00
3.3	-10	1	0.751	4.00	2.50
5.5	-10	1	0.645	2.80	4.00
2.0	-10	1	0.833	6.00	1.70

Table 3.1: Ideal performance of the standard inverting buck-boost.

It is evident that the average inductor current and the inductor current ripple are extremely high for the standard inverting buck-boost and exceed the current saturation limit of the chosen inductor, for this reason another solution is required.

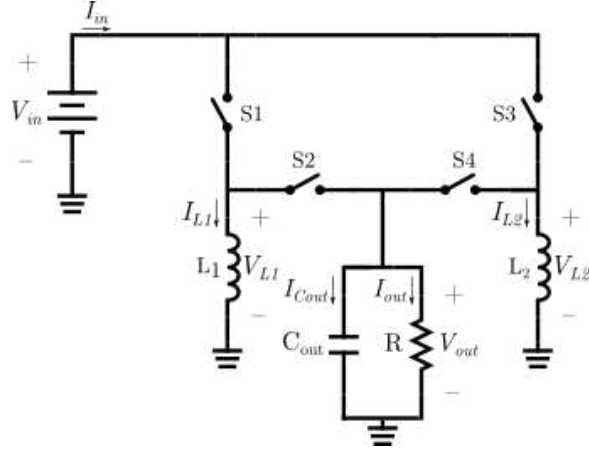


Figure 3.1: Two phase inverting buck-boost circuit.

3.1 Two Phase Inverting Buck-Boost

As shown previously, one of the limits of the standard inverting buck-boost is the high inductor current. Employing a two phase topology allows reducing the current flowing in the overall circuit and especially in the inductor. Fig. 3.1 shows the two phase inverting buck-boost converter scheme.

From the switching sequence, illustrated in Fig. 3.2 and Fig. 3.3, four phases can be identified and it can be also noted that the behaviour of the circuit changes for $D > 0.5$ from the case when $D < 0.5$. This means that the analysis needs to be performed in both cases to fully understand the behaviour of this circuit.

The analysis process starts by computing the inductors voltages and the output capacitor current for each phase, for both $D < 0.5$ and $D > 0.5$.

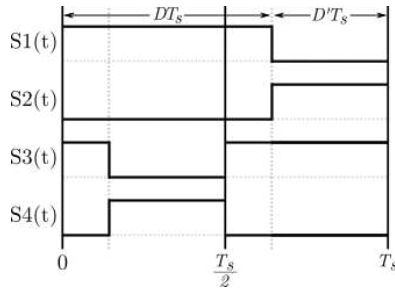


Figure 3.2: Two phase inverting buck-boost switching scheme for $D > 0.5$.

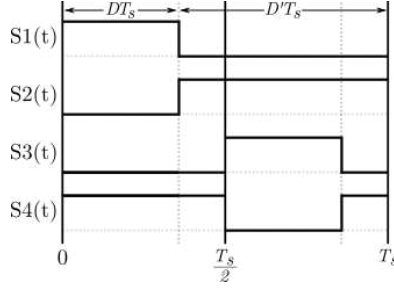


Figure 3.3: Two phase inverting buck-boost switching scheme for $D < 0.5$

For $D > 0.5$:

$$V_{L1} = \begin{cases} V_{in} & \text{in Phase 1} \\ V_{in} & \text{in Phase 2} \\ V_{in} & \text{in Phase 3} \\ V_{out} & \text{in Phase 4} \end{cases} \quad V_{L2} = \begin{cases} V_{in} & \text{in Phase 1} \\ V_{out} & \text{in Phase 2} \\ V_{in} & \text{in Phase 3} \\ V_{in} & \text{in Phase 4} \end{cases} \quad (3.3)$$

$$I_{Cout} = \begin{cases} -I_{out} & \text{in Phase 1} \\ -I_{out} - I_{L2} & \text{in Phase 2} \\ -I_{out} & \text{in Phase 3} \\ -I_{out} - I_{L1} & \text{in Phase 4} \end{cases} \quad (3.4)$$

Now applying the volt-second balance and the capacitor charge balance principles, the following equations are derived:

$$\begin{aligned} \int_0^{T_s} V_{L1} dt &= V_{in} * \left(\frac{T_s}{2} - D'T_s \right) + V_{in} * D'T_s + \\ &\quad + V_{in} * \left(\frac{T_s}{2} - D'T_s \right) + V_{out} * D'T_s = 0 \\ \Rightarrow V_{out} &= -\frac{D}{1-D} V_{in} \\ \int_0^{T_s} V_{L2} dt &= V_{in} * \left(\frac{T_s}{2} - D'T_s \right) + V_{out} * D'T_s + \\ &\quad + V_{in} * \left(\frac{T_s}{2} - D'T_s \right) + V_{in} * D'T_s = 0 \\ \Rightarrow V_{out} &= -\frac{D}{1-D} V_{in} \end{aligned} \quad (3.5)$$

$$\begin{aligned}
\int_0^{T_s} I_{C_{out}} dt &= (-I_{out}) * \left(\frac{T_s}{2} - D'T_s \right) + (-I_{out} - I_{L2}) * D'T_s + \\
&\quad + (-I_{out}) * \left(\frac{T_s}{2} - D'T_s \right) + (-I_{out} - I_{L1}) * D'T_s = 0 \quad (3.6) \\
\Rightarrow \quad (I_{L1} - I_{L2}) &= -\frac{1}{1-D} I_{out}
\end{aligned}$$

Considering $I_{L1} = I_{L2} = I_L$:

$$I_L = -\frac{1}{2(1-D)} I_{out} \quad (3.7)$$

For $D < 0.5$:

$$V_{L1} = \begin{cases} V_{in} & \text{in Phase 1} \\ V_{out} & \text{in Phase 2} \\ V_{out} & \text{in Phase 3} \\ V_{out} & \text{in Phase 4} \end{cases} \quad V_{L2} = \begin{cases} V_{out} & \text{in Phase 1} \\ V_{out} & \text{in Phase 2} \\ V_{in} & \text{in Phase 3} \\ V_{out} & \text{in Phase 4} \end{cases} \quad (3.8)$$

$$I_{C_{out}} = \begin{cases} -I_{out} - I_{L2} & \text{in Phase 1} \\ -I_{out} - I_{L1} - I_{L2} & \text{in Phase 2} \\ -I_{out} - I_{L1} & \text{in Phase 3} \\ -I_{out} - I_{L1} - I_{L2} & \text{in Phase 4} \end{cases} \quad (3.9)$$

Now applying the volt-second balance and the capacitor charge balance principles, the following equations are derived:

$$\begin{aligned}
\int_0^{T_s} V_{L1} dt &= V_{in} * D'T_s + V_{out} * \left(\frac{T_s}{2} - D'T_s \right) + \\
&\quad + V_{out} * D'T_s + V_{out} * \left(\frac{T_s}{2} - D'T_s \right) = 0 \\
\Rightarrow \quad V_{out} &= -\frac{D}{1-D} V_{in} \\
\int_0^{T_s} V_{L2} dt &= V_{out} * D'T_s + V_{out} * \left(\frac{T_s}{2} - D'T_s \right) + \\
&\quad + V_{in} * D'T_s + V_{out} * \left(\frac{T_s}{2} - D'T_s \right) = 0 \\
\Rightarrow \quad V_{out} &= -\frac{D}{1-D} V_{in}
\end{aligned} \quad (3.10)$$

$$\begin{aligned}
\int_0^{T_s} I_{C_{out}} dt &= (-I_{out} - I_{L2}) * D'T_s + (-I_{out} - I_{L1} - I_{L2}) * (\frac{T_s}{2} - D'T_s) + \\
&\quad + (-I_{out} - I_{L1}) * D'T_s + (-I_{out} - I_{L1} - I_{L2}) * (\frac{T_s}{2} - D'T_s) = 0 \\
\Rightarrow (I_{L1} - I_{L2}) &= -\frac{1}{1-D} I_{out}
\end{aligned} \tag{3.11}$$

Considering $I_{L1} = I_{L2} = I_L$:

$$I_L = -\frac{1}{2(1-D)} I_{out} \tag{3.12}$$

Evaluating (3.6) for $D = 0.5$:

$$I_L = -\frac{1}{2(1-D)} I_{out} = -\frac{1}{2(1-0.5)} I_{out} = I_{out} \tag{3.13}$$

This means that for $D < 0.5 \Rightarrow |I_L| < |I_{out}|$ and for $D > 0.5 \Rightarrow |I_L| > |I_{out}|$, however I_L is always half with respect to the standard inverting buck-boost case.

The assumption of considering $I_{L1} = I_{L2}$ is valid in theory but in practice the system needs a control for the current balance between the inductors.

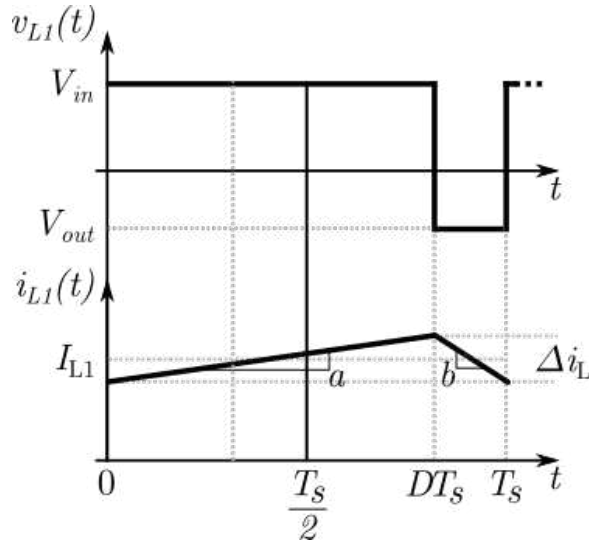


Figure 3.4: Two phase inverting buck-boost inductor current ripple.

As for the standard inverting buck-boost, the inductor current ripple can be easily computed starting from the inductor voltages. Since the inductor voltage is constant in all phases, the inductor current waveform in a period in steady state, as illustrated in Fig. 3.4, is formed by two ramps with a slope given by:

$$a : \frac{V_{in}}{L1}, \quad b : \frac{V_{out}}{L1} \quad (3.14)$$

Which result in a current ripple given by:

$$\Delta i = \frac{V_{in}}{L} DT_s \quad (3.15)$$

These result are valid for both inductors in the circuit.

In a similar way the voltage ripple on the output capacitor can be computed considering first $D > 0.5$ and $I_{L1} = I_{L2} = I_L$ as shown in Fig. 3.5. The derived slopes are:

$$a : -\frac{I_{out}}{C} = -\frac{V_{out}}{CR} > 0, \quad b : \frac{-I_{out} - I_L}{C} < 0 \quad (3.16)$$

In the first phase the slope is positive since the output voltage is negative (supposing a positive input voltage), in the second phase the slope is negative because $-I_{out} > 0$ and $|I_L| > |I_{out}|$, again for $D > 0.5$, as shown in Fig. 3.5

The output voltage ripple is:

$$\Delta v = \frac{V_{out}}{CR} (D - \frac{1}{2}) T_s \quad (3.17)$$

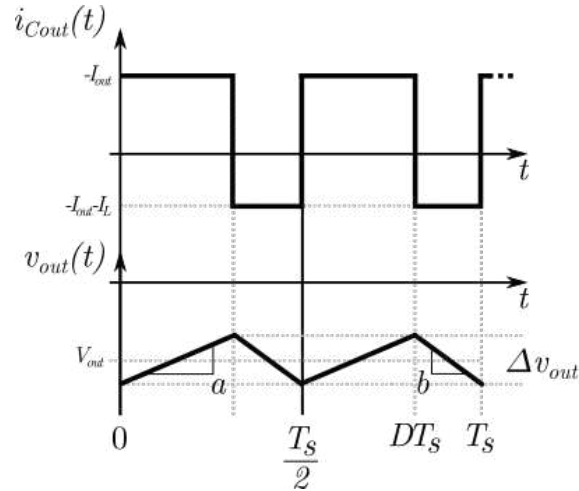


Figure 3.5: Output capacitor waveform of the two phase inverting buck-boost for $D > 0.5$.

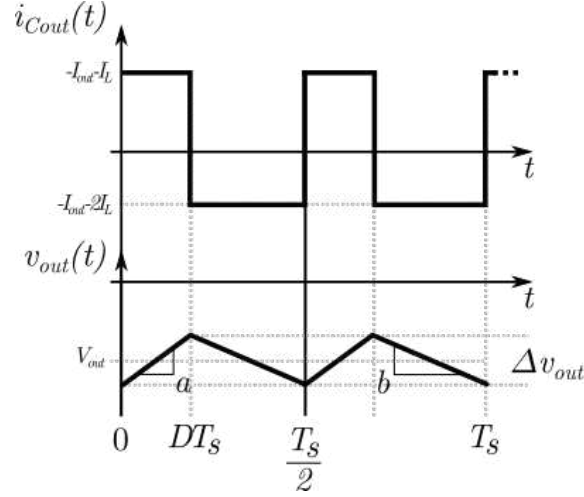


Figure 3.6: Output capacitor waveform of the two phase inverting buck-boost for $D < 0.5$.

Analogously for $D < 0.5$ and $I_{L1} = I_{L2} = I_L$, as shown in Fig. 3.6, the slopes are:

$$a : \frac{-I_{out} - I_L}{C} > 0, \quad b : \frac{-I_{out} - 2I_L}{C} < 0 \quad (3.18)$$

In the first phase the slope is positive since the output voltage is negative (supposing a positive input voltage) and $|I_L| < |I_{out}|$, in the second phase the slope is negative because $-I_{out} > 0$ and $2|I_L| > |I_{out}|$, as shown in Fig. 3.6.

The output voltage ripple is:

$$\Delta v = \frac{-I_{out} - I_L}{C} DT_s \quad (3.19)$$

As shown in Fig. 3.5 and in Fig. 3.6, the output voltage ripple has a frequency doubled with respect to the switching frequency f_s . This is another advantage of this topology: since there are two inductors, while one is delivering to the output the other is magnetising and vice versa; in this way the output voltage ripple is greatly reduced.

In order to have an idea of which voltage rating the switches in the circuit require, it is useful to look at the voltage seen by each switch when closed, as reported in Tab. 3.2 and Tab. 3.3.

Switch	Phase 1	Phase 2	Phase 3	Phase 4
$S1$	-	-	-	$V_{in} - V_{out}$
$S2$	$V_{in} - V_{out}$	$V_{in} - V_{out}$	$V_{in} - V_{out}$	-
$S3$	-	$V_{in} - V_{out}$	-	-
$S4$	$V_{out} - V_{in}$	-	$V_{out} - V_{in}$	$V_{out} - V_{in}$

Table 3.2: Switch supported voltage for the two phase inverting buck-boost for $D > 0.5$.

Switch	Phase 1	Phase 2	Phase 3	Phase 4
$S1$	-	$V_{in} - V_{out}$	$V_{in} - V_{out}$	$V_{in} - V_{out}$
$S2$	$V_{in} - V_{out}$	$V_{in} - V_{out}$	-	$V_{in} - V_{out}$
$S3$	$V_{out} - V_{in}$	-	-	-
$S4$	$V_{in} - V_{out}$	$V_{in} - V_{out}$	-	$V_{in} - V_{out}$

Table 3.3: Switch supported voltage for the two phase inverting buck-boost for $D < 0.5$.

As a recap, these are the results for the two phase inverting buck-boost:

$$M(D) = -\frac{D}{(1-D)}, \quad I_L = -I_{out} * \frac{1}{2(1-D)}, \quad \Delta i = \frac{V_{in}}{L} DT_s \quad (3.20)$$

Considering a few of the different conversion ratios cases that are required by the application, the results illustrated in Tab. 3.4 are derived relying on (3.20). Although this solution allows reducing the inductor average current and the output ripple, two inductor are needed and they are bulky and expensive components. Moreover, the use of two circuits requires employing a more complex the control loop.

3.2 Switched Capacitor Inverting Buck-Boost

Another way to reduce the inductor current can be found by analysing (3.2), focusing on the conversion ratio and the inductor current expression. It can be noticed that the inductor current is inversely proportional to $(1-D)$. If the input voltage is increased in some way, the same conversion ratio could be achieved with a lower duty cycle, thus lowering the average inductor current. The easiest way to do this is interposing a capacitive doubler before the standard inverting buck-boost as shown in Fig. 3.7.

On a further inspection of the circuit it can be noticed that the capacitor

$V_{in}[V]$	$V_{out}[V]$	$I_{out}[I]$	<i>Duty Cycle</i>	$I_L[A]$	$\Delta i[A]$
3.3	-5	0.1	0.602	0.12	2.00
3.3	-10	0.1	0.751	0.20	2.50
5.5	-10	0.1	0.645	0.14	4.00
2.0	-10	0.1	0.833	0.30	1.70
3.3	-5	0.5	0.602	0.63	2.00
3.3	-10	0.5	0.751	1.00	2.50
5.5	-10	0.5	0.645	0.70	4.00
2.0	-10	0.5	0.833	1.50	1.70
3.3	-5	1	0.602	1.75	2.00
3.3	-10	1	0.751	2.00	2.50
5.5	-10	1	0.645	1.40	4.00
2.0	-10	1	0.833	3.00	1.70

Table 3.4: Ideal performance of the two phase inverting buck-boost.

between switch $S5$ and switch $S6$ can be omitted and only one switch is indeed necessary. Fig. 3.8 shows the final circuit. As for the previous two circuits, a full analysis is performed starting with calculating the inductor voltage and capacitor current. From the switching sequence, illustrated in Fig. 3.9, two phases can be identified:

$$V_L = \begin{cases} 2V_{in} & \text{in Phase 1} \\ V_{out} & \text{in Phase 2} \end{cases} \quad (3.21)$$

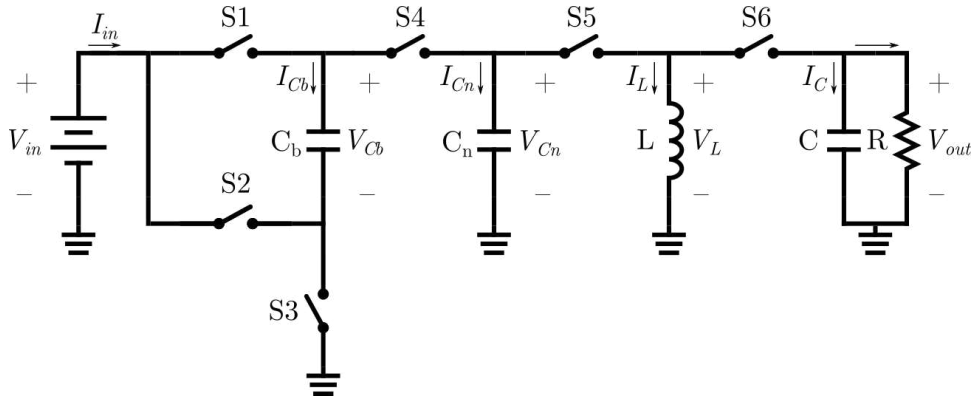


Figure 3.7: Switched capacitor inverting buck-boost scheme.

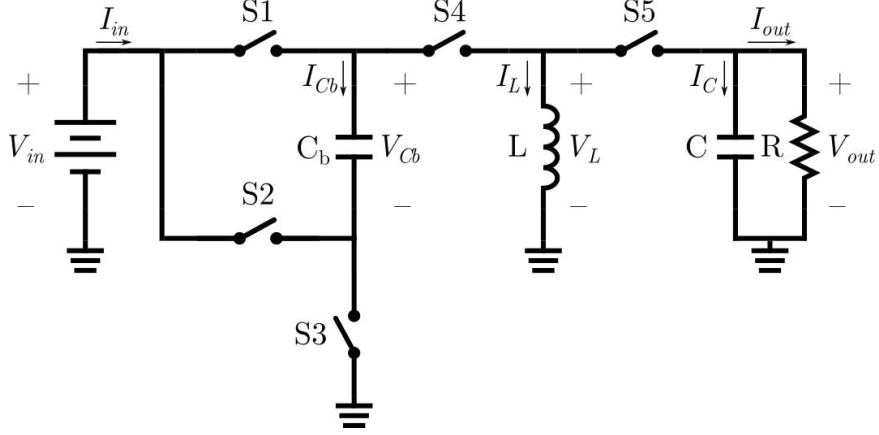


Figure 3.8: *Optimized* switched capacitor inverting buck-boost scheme.

$$I_{Cout} = \begin{cases} -I_{out} & \text{in Phase 1} \\ -I_{out} - I_L & \text{in Phase 2} \end{cases} \quad (3.22)$$

Now applying the volt-second balance and the capacitor charge balance principles, the following equation are derived:

$$\begin{aligned} \int_0^{T_s} V_L dt &= 2V_{in} * DT_s + V_{out} * D'T_s = 0 \\ \Rightarrow V_{out} &= -\frac{2D}{1-D} V_{in} \end{aligned} \quad (3.23)$$

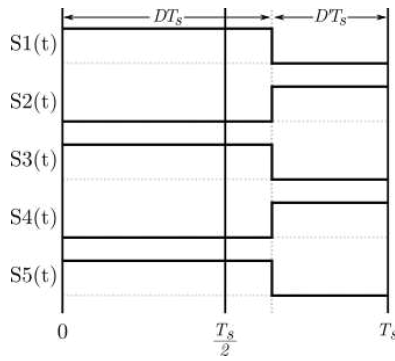


Figure 3.9: Switched capacitor inverting buck-boost switching sequence.

$$\int_0^{T_s} I_{C_{out}} dt = (-I_{out}) * D'T_s + (-I_{out} - I_L) * D'T_s = 0 \quad (3.24)$$

$$\Rightarrow I_L = -\frac{1}{1-D} I_{out}$$

The conversion ratio for the switch capacitor inverting buck-boost is in fact double with respect to the standard inverting buck-boost, if the same duty cycle D is considered.

The equation that links the inductor current with the output current is unchanged, but thanks to the factor 2 in (3.23), the system will need a lower duty cycle to perform the same conversion; therefore also the average inductor current will be lower. This advantage comes with the cost of an extra external component, but, unlike the two phase inverting buck-boost, the external component is a capacitor, usually cheaper and smaller than an inductor, and it does not need any particular balance control. The capacitor for the input doubler just needs to feature the right capacitance value, not too big otherwise it will not charge correctly, and not too small or its voltage ripple will be too large.

Also in this case, the inductor current ripple and the output voltage ripple can be computed. Fig. 3.10 shows the voltage and current waveforms for the inductor, where:

$$a : \frac{2V_{in}}{L}, \quad b : \frac{V_{out}}{L} \quad (3.25)$$

Which result in a current ripple given by:

$$\Delta i = \frac{2V_{in}}{L} DT_s \quad (3.26)$$

As it can be seen, for the switched capacitor inverting buck-boost, the current ripple is actually higher with respect to the standard inverting buck-boost

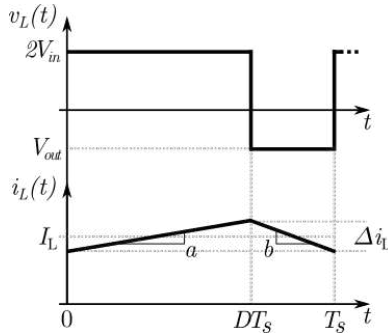


Figure 3.10: Switched capacitor inverting buck-boost inductor current ripple.

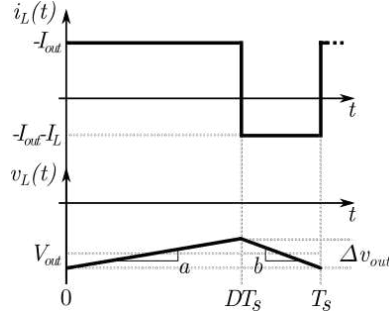


Figure 3.11: Switched capacitor inverting buck-boost output voltage ripple.

even if the duty cycle is reduced. This results in higher dissipation due to core losses in the inductor determining the main disadvantage of this circuit.

For the output ripple, illustrated in Fig. 3.11, the results are:

$$a : -\frac{I_{out}}{C} = -\frac{V_{out}}{CR} > 0, \quad b : \frac{-I_{out} - I_L}{C} < 0 \quad (3.27)$$

In the first phase the slope is positive since the output voltage is negative (supposing a positive input voltage), in the second phase the slope is negative because $-I_{out} > 0$ and $|I_L| > |I_{out}|$. The output voltage ripple is:

$$\Delta v = \frac{V_{out}}{CR} DT_s \quad (3.28)$$

Therefore the output ripple is reduced with respect to the standard inverting buck-boost case because the required duty cycle is reduced.

In order to have an idea of which voltage rating the switches in the circuit require, is useful to look at the voltage seen by each switch when closed, as illustrated in Tab. 3.5

Switch	Phase 1	Phase 2
$S1$	-	$-V_{in}$
$S2$	V_{in}	-
$S3$	-	V_{in}
$S4$	$V_{in} - V_{out}$	-
$S5$	-	$2V_{in} - V_{out}$

Table 3.5: Switch supported voltage for the switched capacitor inverting buck-boost.

$V_{in}[V]$	$V_{out}[V]$	$I_{out}[I]$	<i>Duty Cycle</i>	$I_L[A]$	$\Delta i[A]$
3.3	-5	0.1	0.431	0.18	2.85
3.3	-10	0.1	0.602	0.25	3.98
5.5	-10	0.1	0.476	0.19	4.75
2.0	-10	0.1	0.714	0.34	2.85
3.3	-5	0.5	0.431	0.88	2.85
3.3	-10	0.5	0.602	1.25	3.98
5.5	-10	0.5	0.476	0.95	4.75
2.0	-10	0.5	0.714	1.75	2.85
3.3	-5	1	0.431	1.75	2.85
3.3	-10	1	0.602	2.50	3.98
5.5	-10	1	0.476	1.90	4.75
2.0	-10	1	0.714	3.50	2.85

Table 3.6: Ideal performance of the switched capacitor inverting buck-boost.

As a recap, these are the result for the two phase inverting buck-boost:

$$M(D) = -\frac{2D}{(1-D)}, \quad I_L = -I_{out} * \frac{1}{(1-D)}, \quad \Delta i = \frac{2V_{in}}{L}DT_s \quad (3.29)$$

Considering a few of the different conversion ratios cases that are required by the application , the results reported in Tab. 3.6 are derived relying on (3.29) . This solution allows reducing the average inductor current but the increase in inductor current ripple is so significant that the total inductor current exceeds the saturation current of the chosen inductor. For this reason the solution presented in the next section aim at reducing both the inductor current ripple and the inductor average current.

3.3 Switched Capacitor Three Level Inverting Buck-Boost

Fig. 3.12 shows the new proposed circuit named “switched capacitor three level inverting buck-boost”. The basic idea of this topology is to combine a capacitive doubler at the input, as for the switched capacitor inverting buck-boost, with a three level inverting buck-boost stage.

From the switching sequence illustrated in Fig. 3.13 and Fig. 3.14, four phases can be identified and can be also seen that the switching order changes if the duty cycle is grater or lower than 0.5. Also in this case the analysis needs to

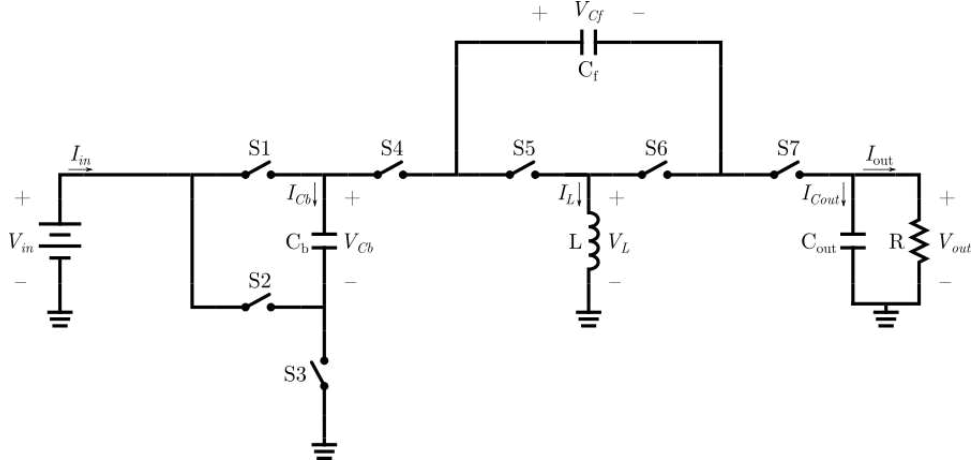


Figure 3.12: Switched capacitor three level inverting buck-boost scheme.

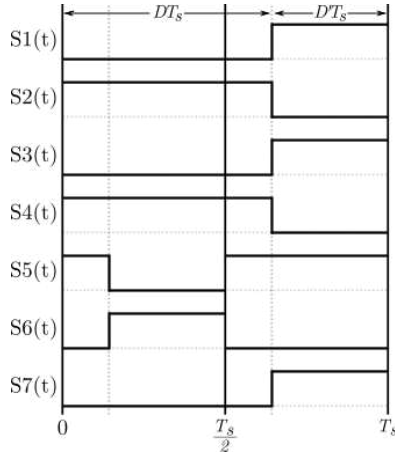


Figure 3.13: Switched capacitor three level inverting buck-boost switching phases for $D > 0.5$.

be performed for both duty cycle cases in order to fully understand the circuit behaviour.

The analysis process starts by computing the inductor voltage and the output capacitor current for each phase, for both $D < 0.5$ and $D > 0.5$.

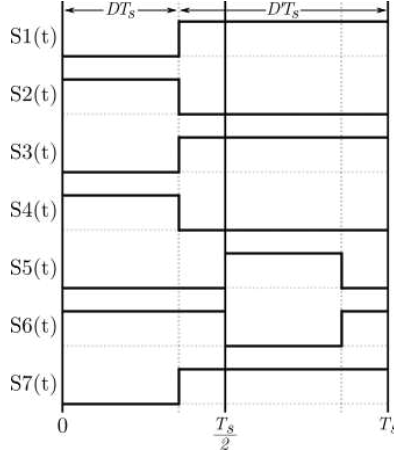


Figure 3.14: Switched capacitor three level inverting buck-boost switching phases for $D < 0.5$.

For $D > 0.5$:

$$V_L = \begin{cases} V_{in} + V_{Cb} = 2V_{in} & \text{in Phase 1} \\ V_{in} + V_{Cb} - V_{Cf} = 2V_{in} - V_{Cf} & \text{in Phase 2} \\ V_{in} + V_{Cb} = 2V_{in} & \text{in Phase 3} \\ V_{out} + V_{Cf} & \text{in Phase 4} \end{cases} \quad (3.30)$$

$$I_{Cout} = \begin{cases} -I_{out} & \text{in Phase 1} \\ -I_{out} & \text{in Phase 2} \\ -I_{out} & \text{in Phase 3} \\ -I_{out} - I_L & \text{in Phase 4} \end{cases} \quad (3.31)$$

Now applying the volt-second balance and the capacitor charge balance principles, the following equations are derived:

$$\begin{aligned} \int_0^{T_s} V_L dt &= 2V_{in} * \left(\frac{T_s}{2} - D'T_s \right) + (2V_{in} - V_{Cf}) * D'T_s + \\ &+ 2V_{in} * \left(\frac{T_s}{2} - D'T_s \right) + (V_{out} + V_{Cf}) * D'T_s = 0 \quad (3.32) \\ \Rightarrow V_{out} &= -\frac{2D}{1-D} V_{in} \quad \text{and} \quad V_{Cf} = \frac{2V_{in} - V_{out}}{2} \end{aligned}$$

$$\begin{aligned}
\int_0^{T_s} I_{C_{out}} dt &= (-I_{out}) * \left(\frac{T_s}{2} - D'T_s \right) + (-I_{out}) * D'T_s + \\
&\quad + (-I_{out}) * \left(\frac{T_s}{2} - D'T_s \right) + (-I_{out} - I_L) * D'T_s = 0 \quad (3.33) \\
\Rightarrow I_L &= -\frac{1}{1-D} I_{out}
\end{aligned}$$

For $D < 0.5$:

$$V_L = \begin{cases} V_{in} + V_{Cb} - V_{Cf} = 2V_{in} - V_{Cf} & \text{in Phase 1} \\ V_{out} & \text{in Phase 2} \\ V_{in} + V_{Cb} + V_{Cf} = 2V_{in} + V_{Cf} & \text{in Phase 3} \\ V_{out} & \text{in Phase 4} \end{cases} \quad (3.34)$$

$$I_{C_{out}} = \begin{cases} -I_{out} & \text{in Phase 1} \\ -I_{out} - I_L & \text{in Phase 2} \\ -I_{out} - I_L & \text{in Phase 3} \\ -I_{out} - I_L & \text{in Phase 4} \end{cases} \quad (3.35)$$

Now applying the volt-second balance and the capacitor charge balance principles, the following equations are derived:

$$\begin{aligned}
\int_0^{T_s} V_L dt &= (2V_{in} - V_{Cf}) * DT_s + V_{out} * \left(\frac{T_s}{2} - DT_s \right) + \\
&\quad + (V_{out} + V_{Cf}) * DT_s + V_{out} * \left(\frac{T_s}{2} - DT_s \right) = 0 \quad (3.36) \\
\Rightarrow V_{out} &= -\frac{2D}{1-D} V_{in} \quad \text{and} \quad V_{Cf} = \frac{2V_{in} - V_{out}}{2}
\end{aligned}$$

$$\begin{aligned}
\int_0^{T_s} I_{C_{out}} dt &= (-I_{out}) * DT_s + (-I_{out} - I_L) * \left(\frac{T_s}{2} - DT_s \right) + \\
&\quad + (-I_{out} - I_L) * DT_s + (-I_{out} - I_L) * \left(\frac{T_s}{2} - DT_s \right) = 0 \\
\Rightarrow I_L &= -\frac{1}{1-D} I_{out} \quad (3.37)
\end{aligned}$$

The results make clear that this topology is in fact an inverting buck-boost with conversion ratio:

$$M(D) = \frac{2D}{1-D} \quad (3.38)$$

Fig. 3.15 shows the conversion ratio for $0 < D < 1$ and comparing it with the standard inverting buck-boost: considering the same D , the new proposed

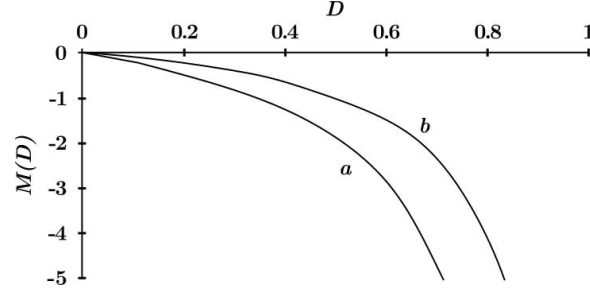


Figure 3.15: Conversion ratio of a) newly proposed solution and b) standard inverting buck-boost.

solution allows achieving a larger conversion ratio in modulus.

From (3.37) it can be seen that the inductor current will always be equal or greater in modulus than the output current, as for the standard inverting buck-boost case. The conversion ratio, however, is doubled with respect to the standard buck-boost case, as for the switched capacitor buck-boost, thanks to the input switched capacitor doubler. This allows reaching the desired output voltages with a lower duty cycle D , lowering also the inductor average current. Focusing on the inductor current waveform illustrated in Fig. 3.16, it is important to point out that the current ripple has a frequency which is double with respect to the switching frequency f_s and a much lower amplitude. The slope of the two ramps for $D > 0.5$ are:

$$a : \frac{2V_{in} + V_{out}}{2L}, \quad b : \frac{2V_{in}}{L} \quad (3.39)$$

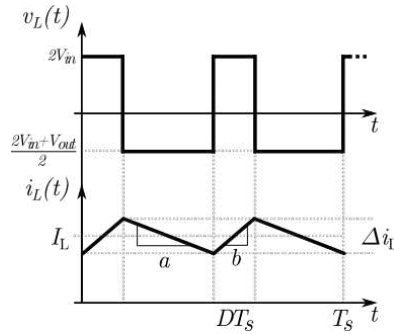


Figure 3.16: Switched capacitor three level inverting buck-boost inductor current and voltage waveform for $D > 0.5$.

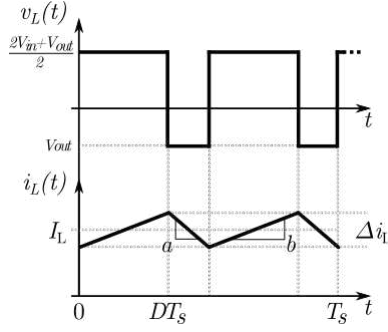


Figure 3.17: Switched capacitor three level inverting buck-boost inductor current and voltage waveform for $D < 0.5$.

Which result in a current ripple given by:

$$\Delta i = \frac{2V_{in}}{L} \left(D - \frac{1}{2} \right) T_s \quad (3.40)$$

For $D < 0.5$ as shown in Fig. 3.17:

$$a : \frac{V_{out}}{L}, \quad b : \frac{2V_{in} + V_{out}}{2L} \quad (3.41)$$

Which result in a current ripple given by:

$$\Delta i = \frac{V_{out}}{L} \left(\frac{1}{2} - D \right) T_s \quad (3.42)$$

This increase in frequency of the ripple can be initially seen as a negative effect since core losses of real inductors are proportional to frequency, however they are also proportional to the square of the amplitude and by considering both effects the total core losses are heavily reduced. This is one of the advantages of the three level, or more in general multi level, structures [4].

As for the other topologies, the output voltage ripple, shown in Fig. 3.18 can be computed :

$$a : -\frac{I_{out}}{C} = -\frac{V_{out}}{CR} > 0, \quad b : \frac{-I_{out} - I_L}{C} < 0 \quad (3.43)$$

In the first phase the slope is positive since the output voltage is negative (supposing a positive input voltage), in the second phase the slope is negative because $-I_{out} > 0$ and $|I_L| > |I_{out}|$. The output voltage ripple for $D > 0.5$ is:

$$\Delta v = \frac{V_{out}}{CR} DT_s \quad (3.44)$$

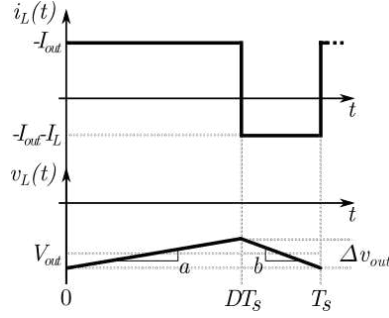


Figure 3.18: Switched capacitor three level inverting buck-boost output voltage ripple.

Another advantage can be found by looking at the voltages that each switch need to support when open. Considering the voltage across each switch in modulus, the result illustrated in Tab. 3.7 and Tab. 3.8 are derived: the required voltage ratings for the switches are lower with respect to the ones of the other considered solutions and, therefore, switches with better figure of merit can be employed.

Switch	Phase 1	Phase 2	Phase 3	Phase 4
$S1$	$-V_{in}$	$-V_{in}$	$-V_{in}$	-
$S2$	-	-	-	V_{in}
$S3$	V_{in}	V_{in}	V_{in}	-
$S4$	-	-	-	$-\frac{V_{out}}{2}$
$S5$	-	$V_{in} - \frac{V_{out}}{2}$	-	-
$S6$	$V_{in} - \frac{V_{out}}{2}$	-	$V_{in} - \frac{V_{out}}{2}$	$V_{in} - \frac{V_{out}}{2}$
$S7$	$V_{in} - \frac{V_{out}}{2}$	$V_{in} - \frac{V_{out}}{2}$	$V_{in} - \frac{V_{out}}{2}$	-

Table 3.7: Switch supported voltage for the switched capacitor three level inverting buck-boost for $D > 0.5$.

As a recap, these are the result for the two phase inverting buck-boost:

$$\begin{aligned}
 M(D) &= -\frac{2D}{(1-D)}, \quad I_L = -I_{out} * \frac{1}{(1-D)}, \\
 \Delta i &= \frac{2V_{in}}{L} \left(D - \frac{1}{2}\right) T_s \text{ for } D > 0.5, \quad \Delta i = \frac{V_{out}}{L} \left(\frac{1}{2} - D\right) T_s \text{ for } D < 0.5
 \end{aligned}
 \tag{3.45}$$

Switch	Phase 1	Phase 2	Phase 3	Phase 4
$S1$	$-V_{in}$	-	-	-
$S2$	-	V_{in}	V_{in}	V_{in}
$S3$	V_{in}	-	-	-
$S4$	-	$-\frac{V_{out}}{2}$	$-\frac{V_{out}}{2}$	$-\frac{V_{out}}{2}$
$S5$	$V_{in} - \frac{V_{out}}{2}$	$V_{in} - \frac{V_{out}}{2}$	-	$V_{in} - \frac{V_{out}}{2}$
$S6$	-	-	$V_{in} - \frac{V_{out}}{2}$	-
$S7$	$V_{in} - \frac{V_{out}}{2}$	-	-	-

Table 3.8: Switch supported voltage for the switched capacitor three level inverting buck-boost for $D < 0.5$.

Considering a few of the different conversion ratios cases that are required by the application and relying on (3.45), the results illustrated in Tab. 3.9 are derived.

$V_{in}[V]$	$V_{out}[V]$	$I_{out}[I]$	Duty Cycle	$I_L[A]$	$\Delta i[A]$
3.3	-5	0.1	0.431	0.18	0.35
3.3	-10	0.1	0.602	0.25	0.67
5.5	-10	0.1	0.476	0.19	0.25
2.0	-10	0.1	0.714	0.34	0.85
3.3	-5	0.5	0.431	0.88	0.35
3.3	-10	0.5	0.602	1.25	0.67
5.5	-10	0.5	0.476	0.95	0.25
2.0	-10	0.5	0.714	1.75	0.85
3.3	-5	1	0.431	1.75	0.35
3.3	-10	1	0.602	2.50	0.67
5.5	-10	1	0.476	1.90	0.25
2.0	-10	1	0.714	3.50	0.85

Table 3.9: Ideal performance of the switched capacitor three level inverting buck-boost.

The results show the significant improvement in the inductor current ripple that allows reducing the dissipation due to core losses and the maximum inductor current which in this way remains below the saturation current limit of the chosen inductor.

Throughout this analysis the voltage across the three level capacitor C_f has

been considered constant and equal to $V_{Cf} = \frac{2V_{in}-V_{out}}{2}$. This assumption is valid in theory but in real circuits parasitic effects and non-idealities, especially in the switching timing, tend to unbalance the capacitor voltage which will drift to a lower or higher value than the expected one [5,6]. Since the capacitor voltage controls directly the inductor voltage, the unbalance in V_{Cf} changes the slope of the inductor current ripple to the point where the improvements provided by the multi level structure are vanished. For this reason a proper control for the balancing of the three level capacitor voltage is needed.

Chapter 4

Power Switches Sizing Optimization

In recent years, several DC–DC converter topologies employing a significant number of power switches have emerged, such as KY topologies, single-inductor multiple-output (SIMO) and single-inductor bipolar-output (SIBO) architectures, and hybrid switched-capacitor (SC) converters, including in particular multi-level structures. KY converters [7] allow boosting the input voltage while maintaining a fast load transient response, similar to that of a buck converter with synchronous rectification, and featuring non-pulsating output current. This not only decreases the current stress on the output capacitor but also reduces the output voltage ripple. SIMO [8] and SIBO [9,10] architectures allow achieving multiple regulated output voltages from a single input while employing a single inductor, thus saving significantly in area and cost, as the inductor is typically the bulkiest and most expensive component in switching DC–DC regulators. Hybrid SC converters, which include merged two-stage converters [11], resonant SC regulators [12], hybrid Dickson converters [13] and multi-level architectures [14,15], show great promise in achieving high power efficiency as well as increased power density. In particular, multi-level structures allow employing power switches with reduced voltage rating, and thus improved figure-of-merit, as well as reducing the inductor current ripple by increasing the effective switching frequency. These features clearly allow targeting very high power efficiency.

The benefits of these topologies, however, come at the expense of an increased number of power switches. Power switch size is a parameter of paramount importance for achieving high efficiency, but the presence of a large number of switches significantly complicates the size optimization process. To

address this issue, this chapter presents a power switch size optimization strategy aimed at maximizing the DC–DC converter power efficiency under a total switch area constraint. The method relies on a compact model of conduction and switching losses and is applied to the case of a 3-level inverting buck–boost regulator.

The remainder of this chapter is organized as follows. Section 4.1 introduces the proposed power switch size optimization strategy. Section 4.2 illustrates its application to a 3-level inverting buck–boost converter and compares the analytical results with Cadence Virtuoso simulations under different combinations of input voltage, output voltage, load current and total switch area. Finally, Section 4.3 summarises the main conclusions.

4.1 Proposed Power Switch Size Optimization Strategy

The proposed power switch size optimization strategy is based on the modelling of power switches with a size-dependent equivalent on-resistance. Each switch features a modular structure, consisting of multiple equal power transistors, acting as unit elements, placed in parallel. The resistance variation with respect to area is derived by means of Cadence Virtuoso simulations: the number of unit power transistors in parallel, defined as power switch multiplicity, is varied and the power switch equivalent on-resistance values are derived through Ohm’s law as the ratio between the transistor drain-to-source voltage, V_{DS} , fixed in the Cadence test-bench by a voltage generator equal to a few tens of mV, and the transistor drain-to-source current, I_{DS} , derived from simulation. The simulation results are then fitted in order to express the switch on-resistance as a function of its multiplicity and, therefore, area.

Considering only the power switch equivalent on-resistance would account exclusively for the converter conduction losses. In order to consider switching losses as well, the gate-to-source ($C_{gs,u}$), gate-to-drain ($C_{gd,u}$) and drain-to-source ($C_{ds,u}$) capacitances of the unit power transistor are also derived through Cadence simulations. The C_{gs} , C_{gd} and C_{ds} of a power switch with multiplicity n are then modelled as n times the corresponding capacitance of the unit power transistor. The test-bench employed for the capacitance estimation is illustrated in Fig. 4.1(a), considering the case of an NMOS power transistor. In order to estimate $C_{ds,u}$, an AC voltage signal equal to 1 V is applied to the transistor drain, while maintaining the NMOS on by applying a sufficiently high DC gate-to-source voltage. The V_{DS} is set equal to the one employed for the on-resistance simulations. The transistor I_{DS} AC current is

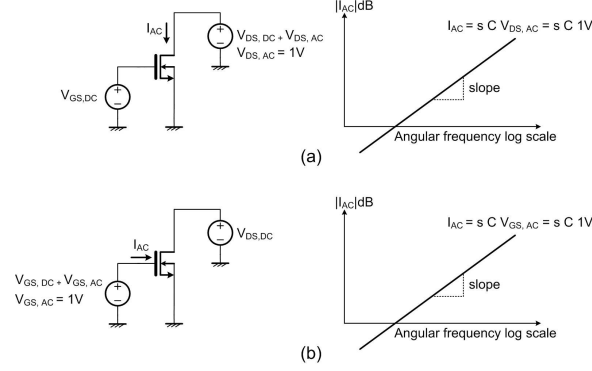


Figure 4.1: (a) Test-bench for the estimation of $C_{ds,u}$, (b) test-bench for the estimation of $C_{gs,u} + C_{gd,u}$.

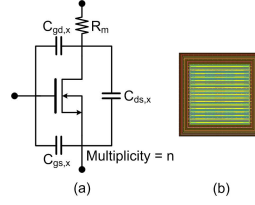


Figure 4.2: (a) Schematic model of the power switch and (b) layout view of a unit-multiplicity NMOS transistor.

then plotted: it exhibits a differentiator-like behaviour, from which the capacitance value can be derived from the intercepting point between the Bode plot of the magnitude of the current and the 0 dB axis. The same procedure, as illustrated in Fig. 4.1(b), is employed to derive $C_{gs,u} + C_{gd,u}$ by applying the AC voltage signal to the gate and measuring the current supplied by the generator. The derived capacitance is then split equally between $C_{gs,u}$ and $C_{gd,u}$, each therefore equal to half of the total capacitance value obtained through simulations.

Core losses are not included in the model, as they are not dependent on the power switch sizes. Furthermore, some architectures, such as multi-level structures, greatly reduce core losses to the point that they can usually be neglected in most cases.

The complete model of an NMOS power switch featuring multiplicity n is illustrated in Fig. 4.2(a). In order to account for parasitics due to layout, a fixed series resistance R_m is added, as well as extra capacitances $C_{gs,x}$, $C_{gd,x}$ and $C_{ds,x}$, each equal to 30% of the simulated switch capacitances $C_{gs} = n \cdot C_{gs,u}$,

Table 4.1: EXAMPLE OF UNIT-MULTIPLICITY POWER SWITCHES

Maximum Voltage Rating [V]	Finger Length [nm]	Finger Width [μm]	Number of Fingers	Total Area [mm ²]
7	700	60	40	0.0059
15	900	60	34	0.007
18	1000	60	26	0.007
21	1300	60	22	0.007
26	1300	60	20	0.0083

$C_{gd} = n \cdot C_{gd,u}$ and $C_{ds} = n \cdot C_{ds,u}$; 30% represents a typical value of parasitics due to interconnections. The unit power transistor size is chosen to feature a nearly squared shape, in order to optimise the layout, as shown in Fig. 4.2(b). Table 4.1 reports the characteristics of various unit-multiplicity isolated NMOS power switches in a tsmc 180-nm BCD technology.

Relying on the proposed power switch model and applying the inductor volt-second balance principle, the capacitor charge balance principle and the small-ripple approximation, expressions for the output voltage, output current and inductor current can be obtained, thus allowing the derivation of the power efficiency as a function of switch multiplicity and, therefore, of the total switch area. By imposing a constraint on the available area, it is then possible, by employing a computation tool (e.g. Wolfram Mathematica), to find the multiplicity values of the different power switches which maximise the efficiency.

4.2 3-Level Inverting Buck–Boost Converter Circuit Example

The power switch size optimization strategy described in Section 4.1 is now applied to the case of a 3-level inverting buck–boost converter, whose schematic and switch control phases are shown in Fig. 4.3. Neglecting parasitics, the conversion ratio CR is given by $CR = \frac{D}{1-D}$, where D is the switches duty cycle, as illustrated in Fig. 4.3. The converter features different switching sequences depending on whether D is greater or smaller than 0.5; the model is derived considering $D > 0.5$, however considering $D < 0.5$ would yield the same results.

In order for the converter to operate correctly, the voltage across the flying capacitor C_F , V_{CF} , needs to be balanced. This can be ensured by a ded-

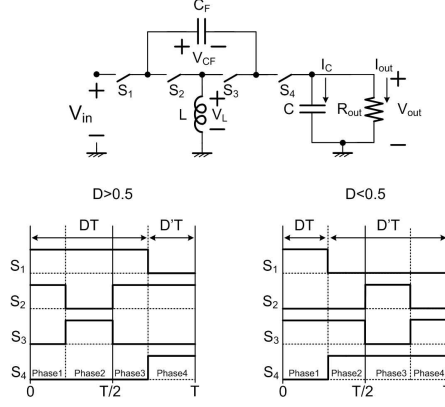


Figure 4.3: 3-level inverting buck-boost schematic view and switch control phases.

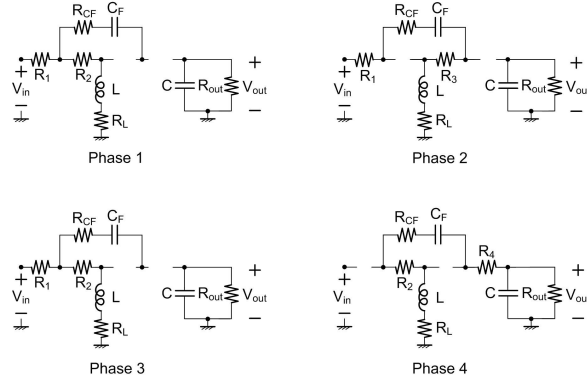


Figure 4.4: 3-level inverting buck-boost equivalent circuit for $D > 0.5$ in the different phases.

icated control loop in the converter [14]. The model is derived under the assumption that such voltage balancing is correctly implemented; in this way $V_{CF} = \frac{V_{in} - V_{out}}{2}$. The switch voltage rating therefore results equal to V_{CF} for all switches. Isolated NMOS power transistors from the tsmc 180-nm BCD technology, such as those reported in Table 4.1, are employed for the switches. 15-V rating switches are chosen in order to allow regulating the output voltage to -10 V in the case of a 5.5-V input voltage, which is assumed as worst-case example.

The 15-V rating switch on-resistance expression is derived by varying the switch multiplicity and then fitting the results with a polynomial function. The

i -th switch on-resistance R_i , with i ranging from 1 to 4, is therefore equal to $R_s(n) + R_m$, where n is the multiplicity, R_s is the function expressing the switch on-resistance as a function of multiplicity and R_m is the resistance added to account for layout parasitics. Extra parasitic capacitances $C_{gs,x} = 0.3 \cdot n \cdot C_{gs,u}$, $C_{gd,x} = 0.3 \cdot n \cdot C_{gd,u}$ and $C_{ds,x} = 0.3 \cdot n \cdot C_{ds,u}$ are included in the power transistor model after deriving the parasitic capacitances for the unit-multiplicity power switch through Cadence simulations, as illustrated in Section 4.1. Furthermore, series resistances R_L and R_{CF} are added to the converter model to account for the inductor and flying capacitor parasitics. The equivalent circuit model for the considered 3-level inverting buck-boost converter in the different phases for $D > 0.5$ is illustrated in Fig. 4.4.

Applying the charge balance principle to capacitor C :

$$\text{Phase 1 / Phase 2 / Phase 3: } -I_C = -I_{out} \quad (4.1)$$

$$\text{Phase 4: } -I_C = -I_{out} - I_L \quad (4.2)$$

Considering the capacitor current $I_C = 0$ over one switching period T , it follows that $I_L = -\frac{I_{out}}{1-D}$, where $I_{out} = \frac{V_{out}}{R_{out}}$ is the load current.

Applying the inductor volt-second balance principle and the small-ripple approximation:

$$\text{Phase 1 / Phase 3: } -V_{in} + R_1 I_L + R_2 I_L + V_L + R_L I_L = 0 \quad (4.3)$$

$$\text{Phase 2: } -V_{in} + R_1 I_L + R_{CF} I_L + V_{CF} + R_3 I_L + V_L + R_L I_L = 0 \quad (4.4)$$

$$\text{Phase 4: } -V_{out} + R_4 I_L - V_{CF} + I_L R_{CF} + R_2 I_L + V_L + R_L I_L = 0 \quad (4.5)$$

Considering $V_L = 0$ over one switching period T and the derived expression of I_L , the following expression for the output voltage is obtained:

$$V_{out} = -\frac{DV_{in}}{1 - D + \frac{DR_1 + DR_2 + R_L}{(1-D)R_{out}} + \frac{R_3 + DR_4 + 2R_{CF}}{R_{out}}} \quad (4.6)$$

where V_{in} is the input voltage, V_{out} the average output voltage, V_L the average inductor voltage, I_L the average inductor current and V_{CF} the flying capacitor average voltage.

The power efficiency is calculated as

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out} I_{out}}{V_{in} I_{in} + P_{sw}} \quad (4.7)$$

where $I_{in} = DI_L$ is the average input current and $P_{sw} = fV_{in}^2(C_{gs,1} + C_{gs,2} + C_{gs,3} + C_{gs,4})$ are the switching losses. Here f is the switching frequency and $C_{gs,i}$ the total gate-to-source capacitance of the i -th switch.

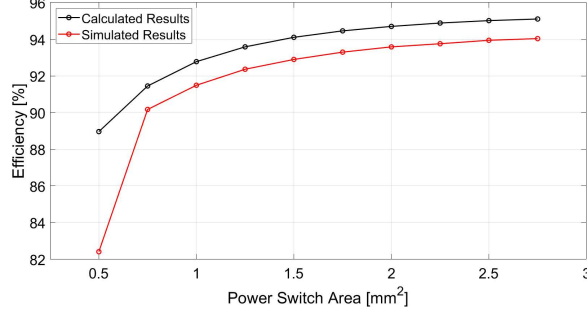


Figure 4.5: Efficiency as a function of total power switch area. The efficiency was derived considering $V_{in} = 3.7$ V, $V_{out} = -6$ V and $I_{load} = 0.5$ A, i.e. the optimisation point used to size the power switches.

By substituting the derived expressions of V_{out} , I_{out} , I_{in} and I_L into (4.7), the efficiency can be expressed as a function of the power switch multiplicities, once the input voltage, output voltage and load current are fixed. The duty cycle is assumed equal to the value that would ensure the desired conversion ratio in the ideal case. In this way, by imposing a constraint on the total switch area and selecting the desired optimisation point (identified by the input voltage/output voltage/load current combination of interest), it is possible to compute the set of switch multiplicity values which maximises the power efficiency. The area constraint is given by $A_{MAX} = (n_1 + n_2 + n_3 + n_4)A_u$, where n_i is the multiplicity of the i -th switch and A_u the area of the unit-multiplicity power transistor. The set of multiplicity values is calculated using Wolfram Mathematica as computation tool.

The considered 3-level converter was simulated in Cadence Virtuoso in order to evaluate the accuracy of the proposed model, by comparing the simulated results with the efficiency values calculated with the model. The flying capacitance was substituted in Cadence with a fixed voltage generator equal to $\frac{V_{in}-V_{out}}{2}$, in order to test the circuit in open loop, without the voltage balancing loop. As an example, the selected switching frequency is 1 MHz, while L is equal to 1 μ H, C to 9 μ F, R_m to 3.5 m Ω , R_L to 25 m Ω and R_{CF} to 3 m Ω . Core losses were not considered in either the model or the simulations.

The efficiency values for different area constraints and the same optimisation point, evaluated at the optimisation point, are illustrated in Fig. 4.5, while Table 4.2 reports the various switch multiplicity values and efficiency results, evaluated and simulated at the optimisation point, considering the same area constraint but different optimisation points. Fig. 4.6 and Fig. 4.7 show

the efficiency curves obtained by varying the load current I_{load} for different combinations of input and output voltage. The optimisation point selected for deriving the results of Fig. 4.6 and Fig. 4.7 is the same (i.e. $V_{\text{in}} = 3.7$ V, $V_{\text{out}} = -6$ V and $I_{\text{load}} = 0.5$ A), while different area constraints were considered.

The accuracy of the model was evaluated by means of the regression index, defined as

$$\text{Regression Index} = 1 - \frac{\sigma_{\text{err}}^2}{\sigma_{\text{var}}^2} \quad (4.8)$$

where σ_{err}^2 is the variance of the error between simulated and calculated efficiency values and σ_{var}^2 is the variance of the observed variable, i.e. the simulated efficiency values. Table 4.3 reports the calculated regression index values, derived from the efficiency curves obtained considering a fixed optimisation point ($V_{\text{in}} = 3.7$ V, $V_{\text{out}} = -6$ V and $I_{\text{load}} = 0.5$ A) and varying the load current for different input/output voltage combinations. The regression index considering $0.2 \text{ A} \leq I_{\text{load}} \leq 1 \text{ A}$ exceeds 0.99 in all cases, thus confirming the goodness of the model. Smaller regression index values are found in some cases when including the range $0.1 \text{ A} \leq I_{\text{load}} \leq 0.2 \text{ A}$. This is due to the fact that the model is not as accurate for light load conditions as it is for medium and high load. For low load current values, indeed, the small-ripple approximation loses validity and switching losses become more dominant. Moreover, the switch capacitance estimation is approximate, as capacitances are derived considering the power transistor in fixed bias conditions, while during normal converter operation it switches from on to off and vice versa, thus varying its capacitance values. Finally, the model assumes continuous conduction mode (CCM) operation for the converter, whereas at light load usually discontinuous conduction mode (DCM) is employed. Nevertheless, the model proves to be very effective for medium and high load conditions in CCM, which are the most relevant operating conditions for the DC–DC converter designs considered in this thesis.

4.3 Conclusions

This chapter has presented a power switch size optimisation procedure aimed at maximising the power efficiency of DC–DC converters under a total switch area constraint. The method can be applied to any type of switching DC–DC regulator and is particularly useful in the case of multi-switch structures such as multi-level converters. The effectiveness of the optimisation strategy has been verified by applying it to a 3-level inverting buck–boost converter.

Table 4.2: EFFICIENCY AND SWITCH MULTIPLICITY FOR VARIOUS OPTIMIZATION POINTS

Power Switches Optimised for $I_{load} = 0.5A$, Area=1mm ²	S1	S2	S3	S4	Simulated Efficiency $I_{load}=0.5A$	Calculated Efficiency $I_{load}=0.5A$
$V_{in}=3.7$ V, $V_{out}=-6$ V	40	39	32	31	92.78%	91.51%
$V_{in}=3.7$ V, $V_{out}=-10$ V	44	43	28	27	91.89%	90.57%
$V_{in}=3.7$ V, $V_{out}=-3$ V	34	34	37	37	92.69%	91.38%

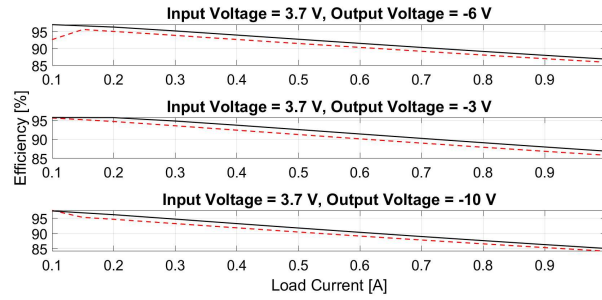


Figure 4.6: Comparison of simulated (red dotted line) and calculated (black solid line) efficiency as a function of load current, considering a 3.7-V input voltage and different output voltages. The power switch size optimisation was performed for $V_{in} = 3.7$ V, $V_{out} = -6$ V and $I_{load} = 0.5$ A, with a 1-mm² maximum area.

Very good matching has been found between simulated and modelled results at medium and high load currents. The proposed model could be further improved by refining the estimation of the power switch capacitances, in order to achieve better matching at light load conditions, where switching losses and deviations from the small-ripple approximation become more significant. The same strategy has been used to optimize the power switches size of the switch capacitor multi-level inverting buck-boost presented in this theses.

Table 4.3: MODEL EVALUATION THROUGH REGRESSION INDEX ESTIMATION

Power Switches Optimised for $I_{load}=0.5\text{A}$, Area= 1mm^2 $V_{in}=3.7\text{ V}$, $V_{out}=-6\text{ V}$	Regression Index $[0.1\text{A} \leq I_{load} \leq 1\text{A}]$	Regression Index $[0.2\text{A} \leq I_{load} \leq 1\text{A}]$
$V_{in}=3.7\text{ V}$, $V_{out}=-6\text{ V}$	0.882759	0.990892
$V_{in}=3.7\text{ V}$, $V_{out}=-3\text{ V}$	0.988853	0.997955
$V_{in}=3.7\text{ V}$, $V_{out}=-10\text{ V}$	0.986823	0.996241
$V_{in}=2.5\text{ V}$, $V_{out}=-6\text{ V}$	0.993413	0.994240
$V_{in}=2.5\text{ V}$, $V_{out}=-3\text{ V}$	0.988622	0.992381
$V_{in}=2.5\text{ V}$, $V_{out}=-10\text{ V}$	0.994875	0.998247
$V_{in}=5.5\text{ V}$, $V_{out}=-6\text{ V}$	0.972462	0.993940
$V_{in}=5.5\text{ V}$, $V_{out}=-3\text{ V}$	0.622442	0.990040
$V_{in}=5.5\text{ V}$, $V_{out}=-10\text{ V}$	0.762600	0.990892

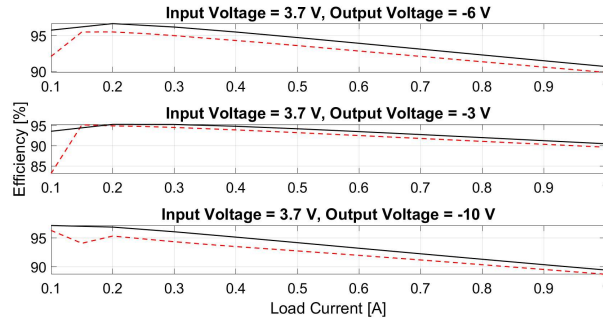


Figure 4.7: Comparison of simulated (red dotted line) and calculated (black solid line) efficiency as a function of load current, considering a 3.7-V input voltage and different output voltages. The power switch size optimisation was performed for $V_{in} = 3.7\text{ V}$, $V_{out} = -6\text{ V}$ and $I_{load} = 0.5\text{ A}$, with a 2-mm^2 maximum area.

Chapter 5

Flying Capacitor Voltage Balancing Control

The schematic architectures of a 3-level buck, a 3-level boost and a 3-level inverting buck–boost switching-mode DC–DC converter are illustrated in Fig. 5.1(a), (b) and (c), respectively.

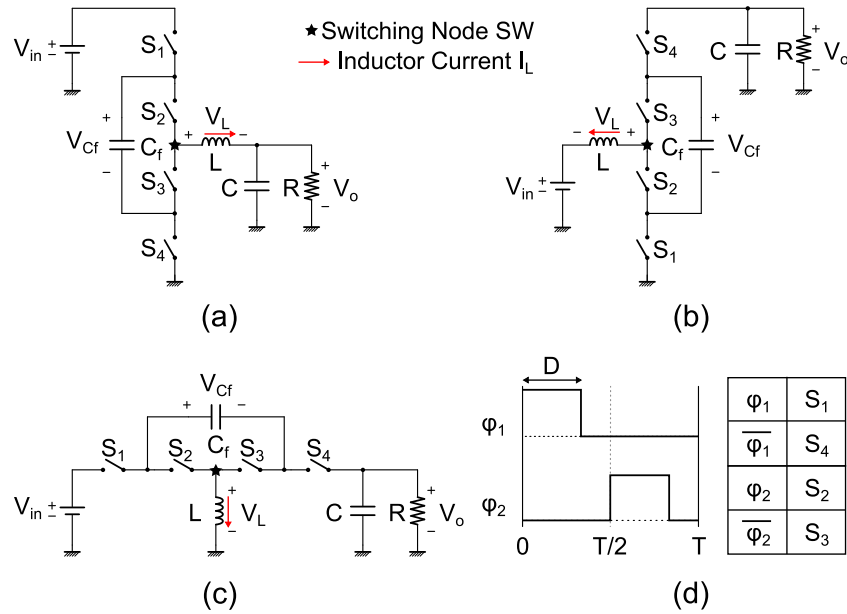


Figure 5.1: Schematic representation of (a) a 3-level buck, (b) a 3-level boost, (c) a 3-level inverting buck–boost and (d) their control signals.

The 3-level architecture is obtained by interposing a flying capacitor in the path of the inductor, which doubles the frequency seen by the inductor with respect to the switching frequency of the converter, thus lowering the inductor peak current by reducing its ripple [16, 17]. As the volume of the inductor component is highly dependent on its saturation current and maximum sustainable current level, lowering the inductor peak current allows choosing devices featuring a significantly reduced volume [17–19], thus addressing the drive towards miniaturisation required in many applications. Moreover, the use of power transistors with reduced voltage rating and, therefore, better figure-of-merit (FoM), is enabled by the 3-level structure [16, 17, 19]: this, together with the core losses reduction determined by the lowering of the inductor current, translates into an improvement in efficiency.

The actual power stage implemented and characterised in this thesis is a hybrid switched-capacitor 3-level inverting buck–boost converter [17]. However, the flying capacitor dynamics and the corresponding balancing condition are qualitatively identical to those of a conventional inductor-based 3-level inverting buck–boost converter. In order to simplify the analytical derivations and obtain compact expressions for the control design, all calculations in this chapter are carried out on the inductor-based 3-level inverting buck–boost topology of Fig. 5.1(c). This modelling choice only changes the numerical value of the balanced flying capacitor voltage, i.e. the reference value $V_{CF,\text{ref}}$, but does not alter the structure of the flying capacitor dynamics nor the form of the proposed balancing loop. The resulting control strategy can therefore be directly applied to the actual hybrid switched-capacitor realisation by appropriately setting the flying capacitor voltage reference.

The correct 3-level structure operation and the consequent advantages are obtained only provided that the voltage across the flying capacitor is balanced, i.e. maintained equal to its nominal value during all the operating phases. The expressions of the desired flying capacitor voltage for different 3-level DC–DC converter topologies are reported in Table 5.1. In practical implementations, however, the flying capacitor voltage can deviate from the nominal value as a result of discharge effects and timing errors caused by parasitics and mismatch [20], thus causing increased inductor current ripple and drain-to-source voltage stress across the switches, which can result in breakdown and reliability issues for the inductor and the power transistors. In order to avoid these issues and correctly maintain the desired balancing of the flying capacitor voltage, appropriate balancing techniques must be employed.

Natural balancing can be achieved by employing phase-shifted PWM [21, 22]: in this way switch pairs S_1 – S_4 and S_2 – S_3 are controlled by two PWM

Table 5.1: FLYING CAPACITOR VOLTAGE EXPRESSIONS FOR DIFFERENT 3-LEVEL SWITCHING-MODE CONVERTER TOPOLOGIES

3-Level Topology	Flying Capacitor Voltage
Buck	$\frac{V_{in}}{2}$
Boost	$\frac{V_o}{2}$
Inverting buck–boost	$\frac{V_{in} - V_o}{2}$

signals, ϕ_1 and ϕ_2 , with the same frequency and duty cycle D but with ϕ_2 delayed by half a period with respect to ϕ_1 , as illustrated in Fig. 5.1(d). Natural balancing, however, may exhibit poor voltage balancing dynamics depending on several factors, such as the duty cycle or the inductor and load resistor values [22]. To improve the natural balancing strength, a passive *RLC* circuit (balancing booster) can be employed [23]; this solution, however, requires external components, increasing the system volume and cost.

In order to ensure the balancing of the flying capacitor voltage in 3-level (and more generally multi-level) converters, several active voltage balancing methods have been proposed, implemented either through repeated switching states [24] or duty cycle compensation [25–28]. Active balancing techniques can be divided into two major groups: those relying on the sensing of the inductor current [18, 25, 27, 29] and those based on the direct sensing of the capacitor voltage [20, 26, 28, 30]. The sensing of the inductor current is not trivial and impacts the output loop compensation, increasing its complexity. Moreover, the direct sensing of the flying capacitor voltage is straightforward only for a 3-level buck topology. In the case of 3-level boost and inverting buck–boost converters, where the voltage across the flying capacitor depends on a wide range of values (and may exceed the input voltage), a differential amplifier able to withstand a wide common-mode voltage range is required. Furthermore, the sensed flying capacitor voltage should be compared with a reference implementing the desired voltage value: since in boost and inverting buck–boost converters the correct flying capacitor voltage depends on the converter output voltage (and also on the input voltage in the case of the inverting buck–boost), which can vary, the reference realisation is not trivial.

An additional possibility for implementing the required balancing on the flying capacitor voltage relies on the sensing of the switching node. This method, however, has mainly been applied to cases where the switching node voltage levels depend solely on the input voltage (e.g. buck topology) and the proposed circuit implementations require a voltage reference for comparing

the sensed switching node voltage with [31, 32]. Hence this strategy faces similar issues as the capacitor-voltage-sensing-based solution and has not been thoroughly investigated, with the analysis largely limited to buck implementations.

This chapter focuses on the possibility of implementing the flying capacitor voltage balancing based on switching node voltage sensing, proposing a detailed circuit implementation that is applicable to different 3-level switching-mode DC–DC converter topologies, including in particular the 3-level inverting buck–boost. In the literature, voltage balancing techniques are generally developed for and applied to 3-level buck converter topologies [18, 20, 25–28], with a few exceptions concerning boost converters [29, 30]. The implementation presented here, instead, constitutes a generalised flying capacitor voltage balancing method.

The proposed approach exploits the sampling of the voltage at the switching node, which is directly correlated with the inductor voltage, to implement a voltage balancing strategy that performs an adjustment of the control signals duty cycle by deriving the error voltage across the flying capacitor through the detection of the inductor voltage. In particular, the proposed circuit implementation allows directly deriving the flying capacitor error voltage by sampling the switching node at proper time instants through a switched-capacitor difference amplifier, thus avoiding the need for a high-requirement differential amplifier and additional reference voltages depending on the converter input and/or output voltages, while also leaving the output loop compensation unchanged.

The versatility of the proposed strategy was verified by means of SIMPLIS simulations considering a 3-level buck, a 3-level boost and a 3-level inverting buck–boost architecture. Moreover, the same strategy was applied to a hybrid switched-capacitor 3-level inverting buck–boost converter fabricated in a 180-nm BCD process [17] and experimentally validated; the corresponding measurement results are presented in a later chapter. The case of an inverting buck–boost converter is particularly significant, as, contrary to the buck and the boost, it features a desired flying capacitor voltage that depends on both the input and the output voltage of the converter. Furthermore, although 3-level inverting buck–boost architectures are rarely found in the literature, they constitute an ideal solution for implementing the negative voltage in AMOLED display driving applications [33]. In recent years, the general trend in power converter circuits for the portable device industry has been to increase the maximum deliverable power and maintain high efficiency over a wide load range, while minimising the volume: a 3-level topology well addresses these

challenges as it allows selecting small-size inductors, thanks to the reduced inductor current ripple, while also employing power switches with improved FoM.

The remainder of this chapter is organised as follows. Section 5.1 introduces the proposed voltage balancing strategy and its circuit implementation, providing a detailed analysis for the selected example case of a 3-level inverting buck–boost converter. Section 5.2 reports SIMPLIS simulation results obtained by applying the proposed voltage balancing method to different 3-level converter cases.

5.1 Proposed Voltage Balancing Strategy

To illustrate the proposed flying capacitor voltage balancing strategy, a 3-level inverting buck–boost converter is considered as reference case. The 3-level inverting buck–boost topology and its control signals are illustrated in Fig. 5.1(c) and Fig. 5.1(d), respectively.

5.1.1 Desired steady-state operation under balanced conditions

For understanding the need for voltage balancing, the desired steady-state operation is first derived. Continuous conduction mode is considered. With the illustrated control scheme, the circuit can assume four configurations, as illustrated in Fig. 5.2(a). Not all the switch configurations are used in the same period; indeed, depending on whether the duty cycle is larger or smaller than 0.5, two modes of operation can be identified: buck mode ($D < 0.5$) and boost mode ($D > 0.5$). When $D = 0.5$ the output voltage is equal to the input, thus representing a limit case of both buck and boost mode and both sets of equations describing those modes are valid. The configuration sequences for $D > 0.5$, $D = 0.5$ and $D < 0.5$ are shown in Fig. 5.2(b).

The analysis for deriving the steady-state operation is performed considering $D > 0.5$, however the same procedure can be applied for the other cases obtaining analogous results. Knowing the switching sequence, the defining parameters of the converter can be derived using the standard method [34]. First, the voltage across the inductor and the current flowing through capacitor C

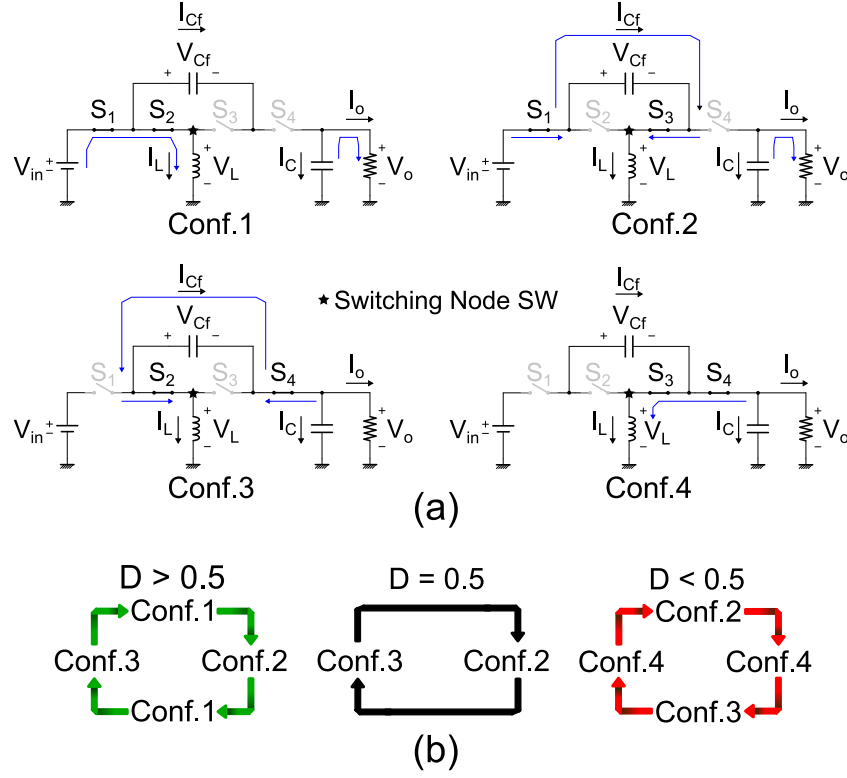


Figure 5.2: (a) Possible operating configurations and (b) configuration sequences for a 3-level inverting buck-boost converter.

are derived for each of the four phases, as shown in (5.1).

$$V_L = \begin{cases} V_{in} & \text{in P1} \\ V_{in} - V_{Cf} & \text{in P2} \\ V_{in} & \text{in P3} \\ V_o + V_{Cf} & \text{in P4} \end{cases} \quad I_C = \begin{cases} -I_o & \text{in P1} \\ -I_o & \text{in P2} \\ -I_o & \text{in P3} \\ -I_o - I_L & \text{in P4} \end{cases} \quad (5.1)$$

Then, applying the volt-second balance and the capacitor charge balance principles, the following equations are derived:

$$\begin{aligned} \int_0^{T_s} V_L dt &= V_{in} \left(\frac{T_s}{2} - D'T_s \right) + (V_{in} - V_{Cf}) D'T_s \\ &\quad + V_{in} \left(\frac{T_s}{2} - D'T_s \right) + (V_o + V_{Cf}) D'T_s = 0 \\ \Rightarrow V_o &= -\frac{D}{1-D} V_{in} \end{aligned} \quad (5.2)$$

$$V_{in} - V_{Cf} = V_o + V_{Cf} \Rightarrow V_{Cf} = \frac{V_{in} - V_o}{2} \quad (5.3)$$

$$\begin{aligned} \int_0^{T_s} I_C dt &= (-I_o) \left(\frac{T_s}{2} - D'T_s \right) + (-I_o)D'T_s \\ &+ (-I_o) \left(\frac{T_s}{2} - D'T_s \right) + (-I_o - I_L)D'T_s = 0 \end{aligned} \quad (5.4)$$

$$\Rightarrow I_L = -\frac{1}{1-D} I_o$$

It can be noticed that the conversion ratio is the same as for the conventional inverting buck–boost converter. According to the desired steady-state behaviour, the average voltage across the flying capacitor, V_{Cf} , is kept constant and properly balanced, so that the inductor voltage in phases P2 and P4 (or P1 and P3 for $D < 0.5$) is equal, as reported in (5.3). Assuming that the flying capacitor is correctly charged to $(V_{in} - V_o)/2$, (5.4) shows how the average inductor current depends on the duty cycle and the output load.

Starting from the inductor voltage, a qualitative representation of the inductor current can be derived through integration, as shown in the graph in Fig. 5.3. As expected, the frequency of the inductor current ripple is doubled with respect to the switching frequency: this results in a reduction of the ripple amplitude, which in turn reduces the overall inductor peak current and core losses, since the ripple amplitude has a larger impact on core losses than the switching frequency. The amplitude of the ripple can be computed as shown in (5.5).

$$\Delta i_L = \frac{V_{in}}{L} \left(D - \frac{1}{2} \right) T_s \quad (5.5)$$

5.1.2 Proposed voltage balancing strategy: principle of operation

The desired steady-state operation is obtained provided that the flying capacitor is correctly charged and that the two PWM control signals share the same duty cycle. Without proper monitoring and correction circuits, however, parasitics discharge the capacitor and affect timing, so that a flying capacitor voltage imbalance may originate. In order to understand the impact of an imbalance in V_{Cf} , it is useful to plot the current of the flying capacitor, I_{Cf} , both when V_{Cf} is equal to its desired value (i.e. $(V_{in} - V_o)/2$) and when it is off by a small amount.

Figure 5.4 shows the two PWM control signals, the inductor voltage, the inductor current and the flying capacitor current. Focusing on the first period of the graph, between 0 and T_1 , when V_{Cf} is correctly balanced, it can be seen

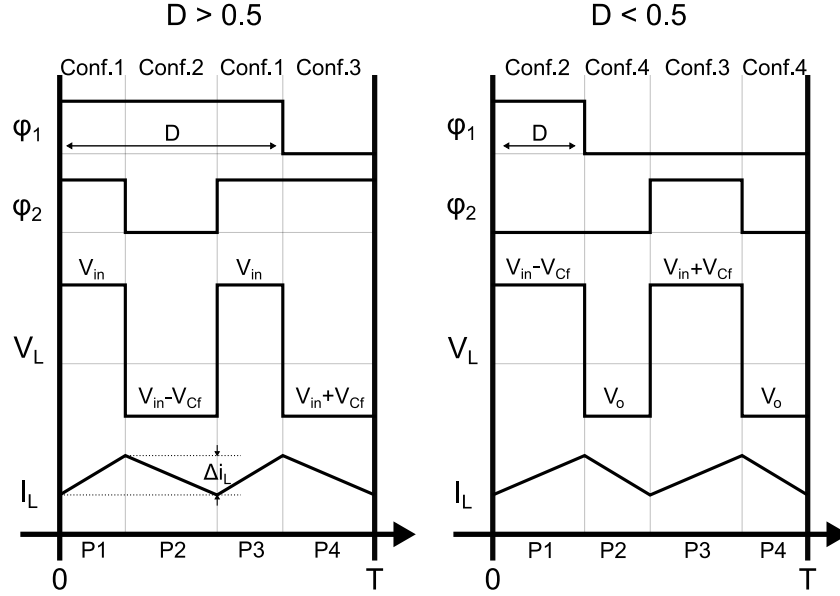


Figure 5.3: Qualitative graph of the control signals, the inductor voltage and the inductor current for $D > 0.5$ and $D < 0.5$.

that the inductor current features the expected frequency (twice the switching frequency of the converter) and the inductor voltage is a perfect square wave at the same frequency, as (5.3) holds. It is important to notice that the net current flowing through the flying capacitor during the considered period is equal to zero, since areas q_2 and q_4 are equal. This is consistent with the steady-state assumption: if the average current flowing through C_f were different from zero, the capacitor voltage would drift.

Now suppose that the voltage across the flying capacitor is

$$V_{Cf,e} = V_{Cf} + \delta V_{Cf} = \frac{V_{in} - V_o}{2} + \delta V_{Cf} \quad (5.6)$$

where δV_{Cf} is a small error caused by non-idealities. The second period, from T_1 to T_2 , illustrated in Fig. 5.4, shows what happens in the case of a flying capacitor overcharge, i.e. considering $\delta V_{Cf} > 0$. In this case V_L is no longer a perfect square wave, as $V_{in} - V_{Cf,e} \neq V_o + V_{Cf,e}$, resulting in a net non-zero current flowing through C_f , as can be seen from the difference between q_6 and q_8 . Consequently, the inductor current frequency is no longer doubled with respect to the switching frequency, and the advantages of the multilevel architecture are lost. The effect on the illustrated curves is qualitative and exaggerated for the sake of clarity.

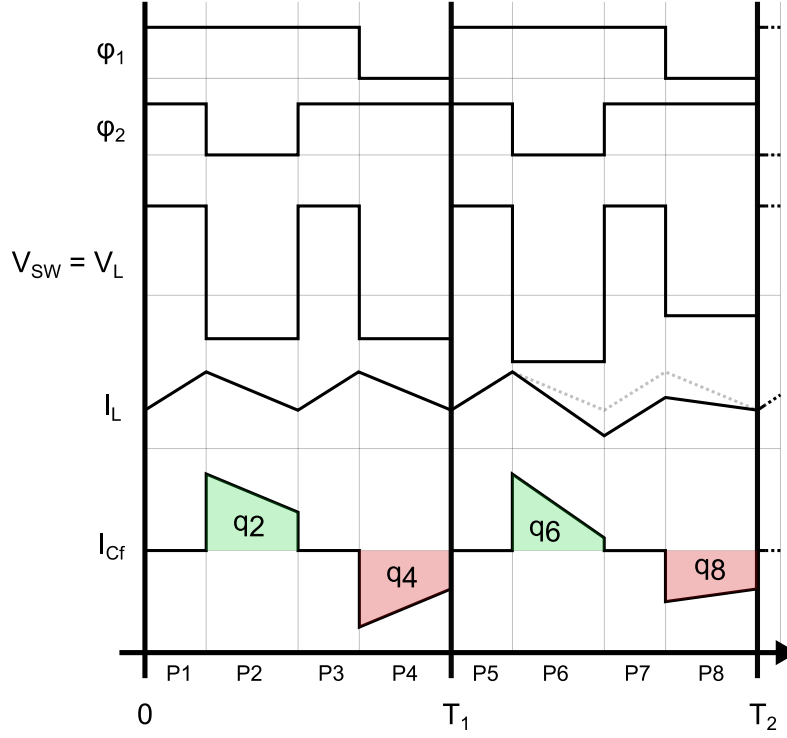


Figure 5.4: Qualitative graph of the control signals, the inductor voltage, the inductor current and the flying capacitor current in both balanced and unbalanced state for $D > 0.5$.

It is therefore necessary to control the flying capacitor voltage in order to ensure balancing. The flying capacitor voltage balancing method requires two main steps: first detecting the imbalance and then applying a correction to remove the error. Directly sensing the flying capacitor voltage is not easy to implement since the voltage across it varies over a wide range, depending on both the converter input and output voltage: a differential amplifier supporting a wide common-mode voltage and a variable voltage reference would be required. Moreover, sensing of the imbalance through detection of the inductor current would require an additional shunt resistance and may increase the complexity of the output voltage control loop compensation.

To overcome these issues, a different way to extract the error is adopted, resulting in a general method for implementing the voltage balancing. As shown in Fig. 5.4, the inductor voltage directly depends on the flying capacitor voltage in two of the four switching phases: this can be exploited to sense the

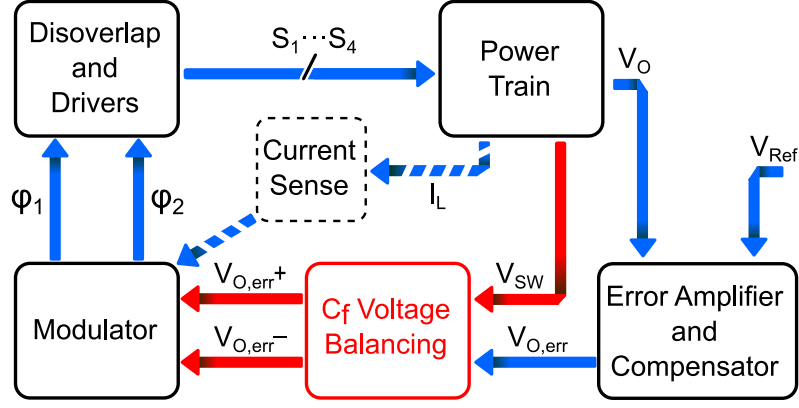


Figure 5.5: Block diagram of the complete control loop system, including the V_{Cf} voltage balancing block.

error δV_{Cf} by sampling and processing the inductor voltage. As illustrated by (5.7), the inductor voltage is sampled during phase P2 and phase P4 and the difference between the two sampled voltages is used as the error signal of interest.

$$\begin{aligned}
 V_{Cf,err} &= V_{L,P2} - V_{L,P4} = (V_{in} - V_{Cf,e}) - (V_o + V_{Cf,e}) \\
 &= V_{in} - V_{Cf} - \delta V_{Cf} - V_o - V_{Cf} - \delta V_{Cf} \\
 &= V_{in} - V_o - 2V_{Cf} - 2\delta V_{Cf}
 \end{aligned} \tag{5.7}$$

By substituting the expected value for V_{Cf} from (5.3), (5.8) is obtained:

$$V_{Cf,err} = V_{in} - V_o - 2\left(\frac{V_{in} - V_o}{2}\right) - 2\delta V_{Cf} = -2\delta V_{Cf} \tag{5.8}$$

Hence, the result of the sampling and subtraction operation returns the error on the flying capacitor voltage multiplied by -2 . All the information needed to monitor the flying capacitor voltage is therefore contained in the amplitude and sign of $V_{Cf,err}$. This way of sampling the error can be implemented with an amplifier and some switched-capacitor logic, requiring significantly less complexity than extracting it directly by sensing the flying capacitor voltage.

The imbalance sensing strategy has been illustrated for the case of an inverting buck–boost converter, however the same reasoning applies to other switching-mode DC–DC converter cases. For the inverting buck–boost, the inductor voltage and the voltage at the switching node SW coincide, as the other terminal of the inductor is connected to ground. For buck and boost topologies, the voltage at the switching node, V_{SW} , is directly correlated with the inductor voltage: $V_{SW} = V_L + V_o$ and $V_{SW} = V_L + V_{in}$ for the buck and

the boost, respectively. Since V_{in} and V_o are substantially constant during the converter steady-state operation, sensing V_{SW} still allows an indirect measurement of V_L .

Once the imbalance has been detected, the error signal is employed to perform the required correction. As previously explained, the 3-level DC–DC converter is controlled through two PWM signals with the same duty cycle, one shifted by half a period with respect to the other, and the output voltage regulation is achieved by changing the duty cycle of both signals in the same way. However, the two duty cycles can also be used to implement the flying capacitor voltage correction by moving them in opposite directions.

Figure 5.5 shows the block diagram of the complete output voltage control loop, including the additional voltage balancing loop. Conventional output voltage control loops consist of an error amplifier and compensation circuit, a modulator and drivers for generating the control signals and driving the power switches. In a current-mode control scheme, an additional current sensing block is required and its output signal is used by the modulator in the power switch control signals generation.

In the proposed architecture, the C_f voltage balancing block is added after the error amplifier and compensator block. In a standard switching-mode DC–DC converter the output of the compensator, $V_{o,err}$, drives a single comparator to generate the PWM signal necessary to control the system. The C_f voltage balancing block instead, starting from $V_{o,err}$, generates two different error voltage signals, $V_{o,err+}$ and $V_{o,err-}$, which are then used by the modulator to generate control signals ϕ_1 and ϕ_2 with different duty cycles, D_1 and D_2 , one larger and one smaller than the nominal duty cycle D .

The voltage $V_{C_f,err}$ extracted from the sampling of V_{SW} is added to $V_{o,err}$ in one case and subtracted from $V_{o,err}$ in the other, creating a difference between the two duty cycles. The effect on ϕ_1 and ϕ_2 , and their duty cycles, is shown in Fig. 5.6, which illustrates the system behaviour. For description purposes the change in the two duty cycles is strongly accentuated. Starting from a condition where the flying capacitor is overcharged, in order to reduce V_{C_f} the duty cycle of signal ϕ_1 needs to be reduced and the one of signal ϕ_2 needs to be increased. The effect of this change can be seen by looking at areas q_6 and q_8 in Fig. 5.6: with respect to the previous period, the charge removed from the capacitor is greater and this results in a discharge of the flying capacitor. The dotted line shows the ideal values for V_L and I_L . The speed of the correction depends on the amount of change applied to the two control signals: excessive correction can make the system unstable, while too little correction would lead to an excessively long response time.

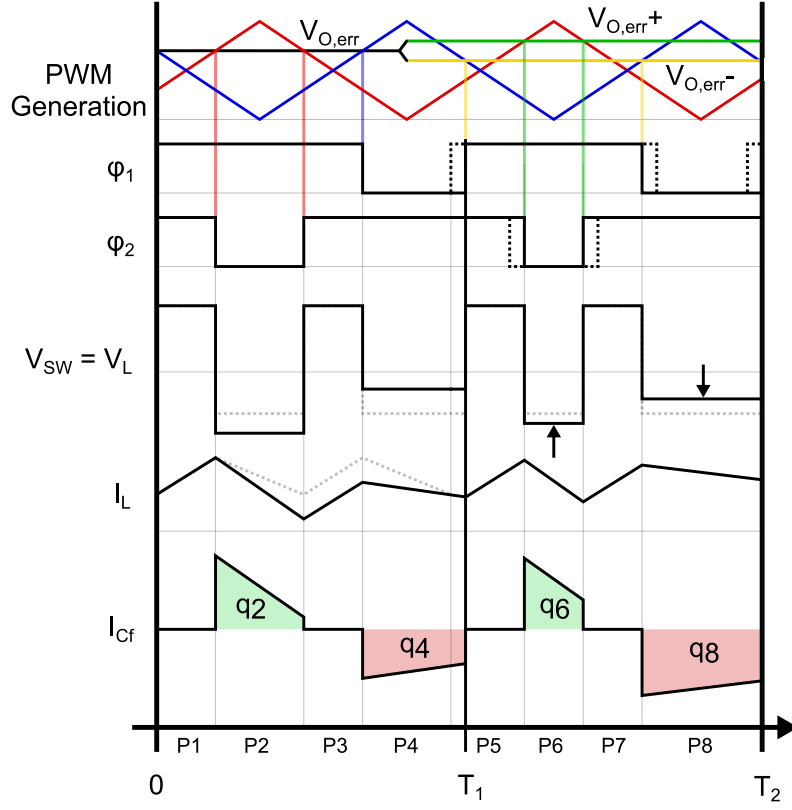


Figure 5.6: Qualitative graph of the PWM generation, control signals, inductor voltage, inductor current and flying capacitor current without and with correction for $D > 0.5$.

A triangular wave is employed for the PWM generation in the modulator to avoid the instability problem detailed in [35]. Indeed, as shown in Fig. 5.7(a), when employing a sawtooth wave, the total charge difference is $\Delta Q_{Cf} = Q_1 - Q_2 + Q_3$, where Q_1 and Q_3 depend on the average inductor current while Q_2 does not: hence there exists a limit current for which ΔQ_{Cf} changes sign and the control loop becomes unstable. Employing a triangular wave to generate the PWM signal eliminates this problem since Q_2 does not exist, as shown in Fig. 5.7(b).

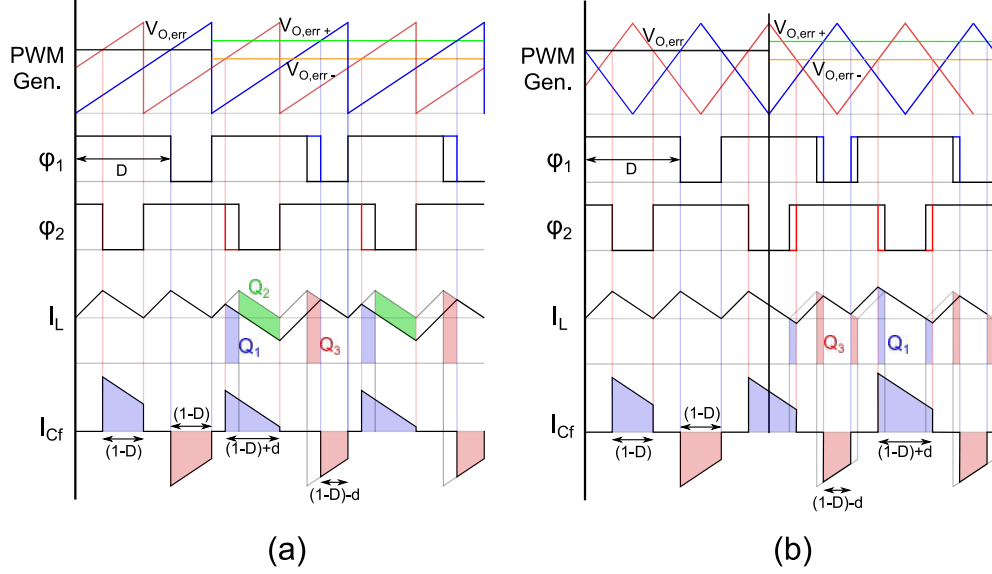


Figure 5.7: Qualitative graph of the PWM generation, control signals, inductor current and flying capacitor current when employing (a) sawtooth waves or (b) triangular waves for PWM generation.

5.1.3 Proposed voltage balancing strategy: circuit implementation

The circuit implementation of the proposed voltage balancing architecture in the case of a 3-level inverting buck–boost with a standard voltage-mode output control loop featuring a type-III compensator [36] is illustrated schematically in Fig. 5.8(a). The detailed implementation corresponds to the one employed for the fabricated hybrid 3-level switched-capacitor inverting buck–boost converter whose measurement results are reported in a later chapter.

The voltage V_{SW} , equal to V_L , is sampled and $V_{C_f,err}$ is extracted in a single operation by means of a switched-capacitor difference amplifier. Resistors R_A and R_B form a divider in order to attenuate the inductor voltage and protect the low-voltage components that implement the following circuit. Signals ϕ_A and ϕ_B are generated in order to close the respective switches in the phases when the flying capacitor is in series with the inductor. The transfer function of the sampling circuit is therefore:

$$V_{C_f,err} = \frac{R_B}{R_A + R_B} \frac{C_A}{C_B} (V_{L,P4} - V_{L,P2}) + V_{CM} \quad (5.9)$$

The ratio between capacitors C_A and C_B allows controlling how much the duty

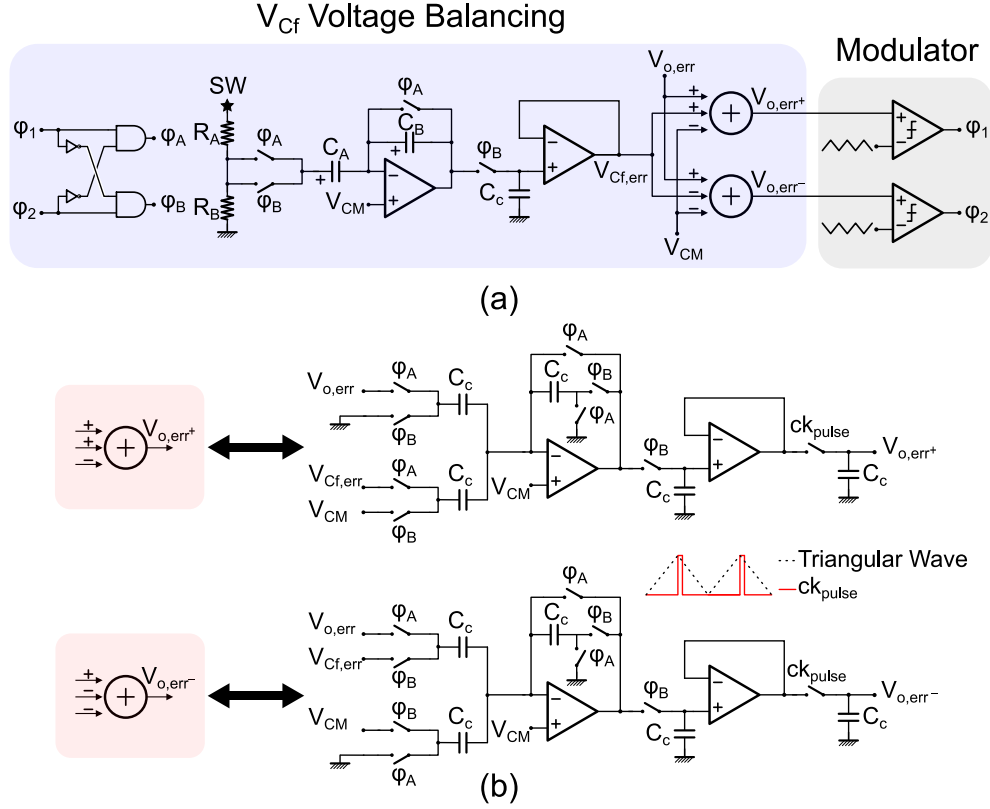


Figure 5.8: Schematic representation of the proposed circuit implementation (a) for the flying capacitor voltage balancing block and (b) for the adder blocks.

cycle is changed with respect to the one set by the output loop compensation. The voltage $V_{Cf,err}$ is added to one side and subtracted from the other in the modulator, thus effectively generating two control signals, ϕ_1 and ϕ_2 , with different duty cycles, D_1 and D_2 .

The adder blocks are implemented by means of a switched-capacitor amplifier, a buffer and a sample-and-hold circuit controlled by the ck_{pulse} signal, as illustrated in Fig. 5.8(b). The buffer and the sample-and-hold circuit controlled by ck_{pulse} are required to ensure that the $V_{o,err+}/V_{o,err-}$ signals supplied to the modulators are correct, i.e. are generated after every transition of V_{SW} has been completed. For this reason, the sampling signal ck_{pulse} is generated in correspondence with the triangular wave maximum/minimum peaks, as they are the farthest from the switching transitions. The signals controlling the switched-capacitor amplifiers, ϕ_A and ϕ_B , are generated from ϕ_1 and ϕ_2

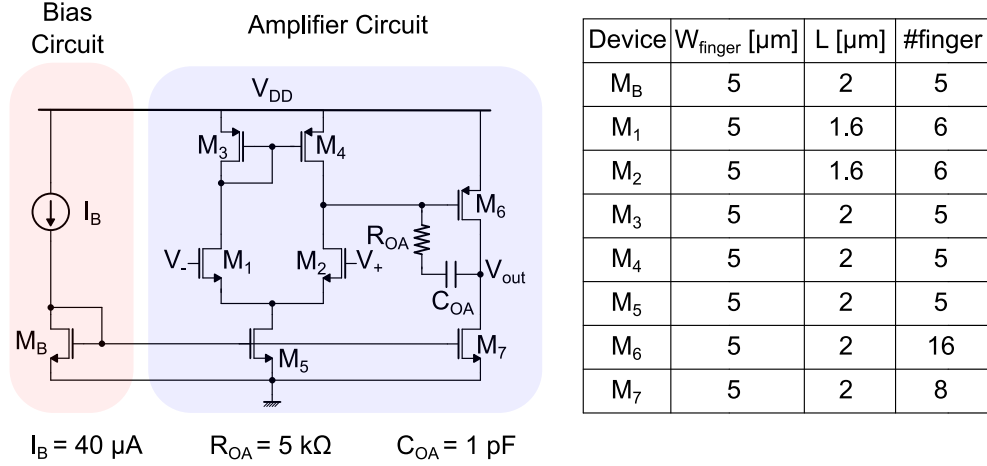


Figure 5.9: Schematic representation of the employed amplifier topology, component values and transistor sizes (finger width W_{finger} , length L and number of fingers $\#finger$).

through appropriate digital logic: in this way ϕ_A and ϕ_B correspond to phases P2 and P4 when $D > 0.5$ or to P1 and P3 when $D < 0.5$, as shown in Fig. 5.3. V_{CM} is the common-mode voltage, set to half of the control loop voltage supply, equal to V_{in} . In addition to the switched-capacitor amplifiers, analogue buffers are required for decoupling.

A conventional two-stage topology, illustrated in Fig. 5.9, is employed for the operational amplifier design. The same operational amplifier schematic is used for all the required amplifier blocks. The switches are realised through complementary MOS devices. Low-voltage transistors are employed for implementing the V_{Cf} voltage balancing block, as the loop supply voltage goes from ground to V_{in} , whose maximum value is assumed to be 5 V.

5.1.4 Generalisation of the proposed solution

The same balancing circuit, presented here for the case of a 3-level inverting buck–boost with a standard voltage-mode output control loop, can be employed also in the case of 3-level buck and 3-level boost converters. The logic circuit providing sampling signals ϕ_A and ϕ_B so that the switching node voltage is always sampled during the phases when the flying capacitor is in series with the inductor is still valid when considering buck and boost topologies. The converter configurations during the sampling phases for the buck and boost cases are illustrated in Fig. 5.10.

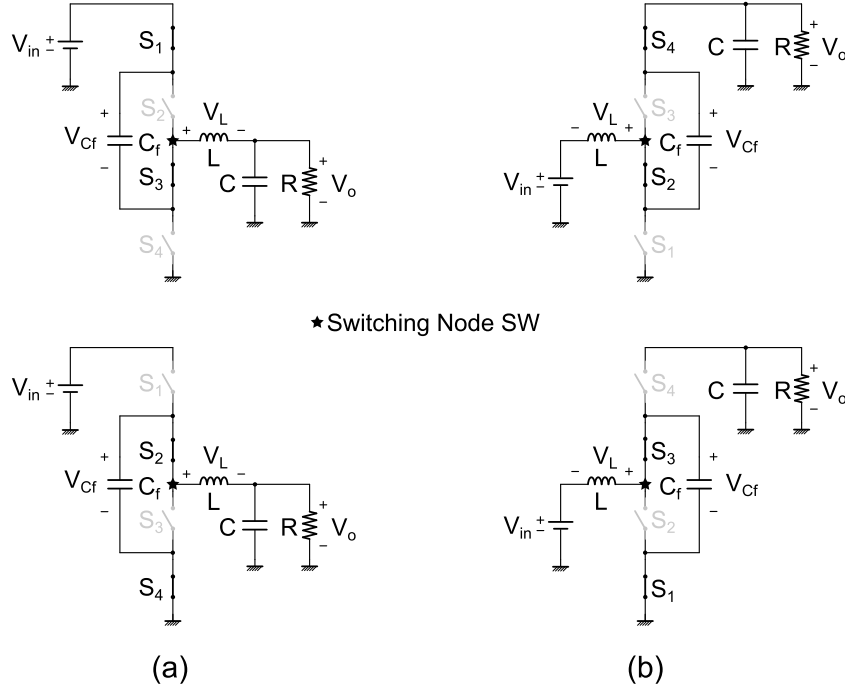


Figure 5.10: Schematic representation of the converter configurations during the sampling phases for the (a) buck and (b) boost topologies.

Considering the buck topology, the sensed switching voltage $V_{SW} = V_L + V_o$ is equal to $V_{in} - V_{Cf}$ and V_{Cf} in the two sampling phases respectively. By sensing the difference between V_{SW} in the two phases, the error voltage is obtained analogously to the inverting buck–boost case:

$$\begin{aligned} V_{Cf,err} &= V_{in} - V_{Cf} - V_{Cf} = V_{in} - 2V_{Cf} \\ &= V_{in} - 2(V_{Cf,ideal} + \delta V_{Cf}) = -2\delta V_{Cf} \end{aligned} \quad (5.10)$$

as the desired flying capacitor voltage in the case of the buck converter is $V_{in}/2$, as reported in Table 5.1.

Considering the boost topology, the sensed switching node voltage $V_{SW} = V_L + V_{in}$ is equal to $V_o - V_{Cf}$ and V_{Cf} in the two sampling phases respectively. In this case the difference between the sensed V_{SW} values yields:

$$\begin{aligned} V_{Cf,err} &= V_o - V_{Cf} - V_{Cf} = V_o - 2V_{Cf} \\ &= V_o - 2(V_{Cf,ideal} + \delta V_{Cf}) = -2\delta V_{Cf} \end{aligned} \quad (5.11)$$

as the desired flying capacitor voltage in the case of the boost converter is $V_o/2$.

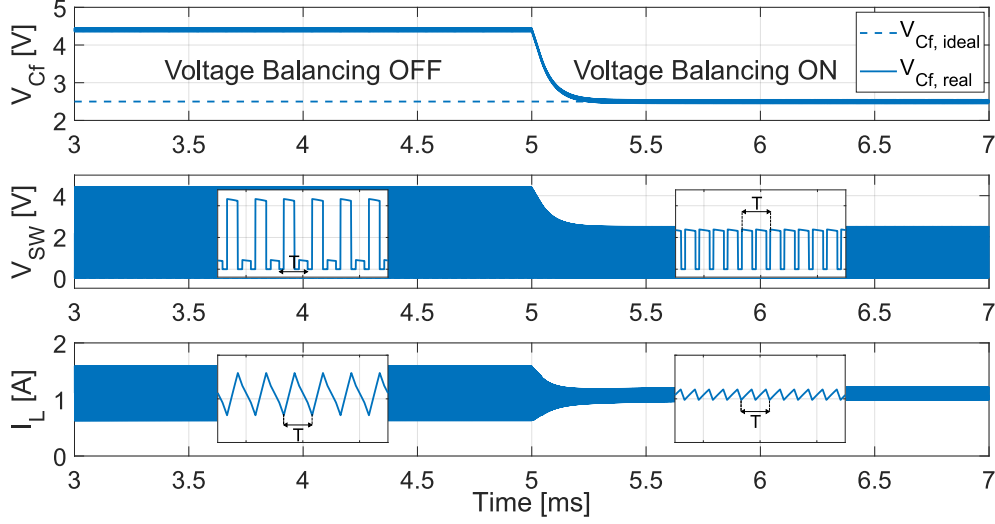


Figure 5.11: Simulated waveforms with and without voltage balancing loop for $V_{in} = 5$ V and $V_o = 1.8$ V ($D < 0.5$).

It is therefore evident that the same active balancing circuit implementation proposed in Section 5.1.3 and illustrated in detail for the case of an inverting buck–boost converter can be employed for buck and boost topologies as well. Furthermore, the proposed circuit could be employed also for the case of a current-mode output control loop, provided that the modulators are modified accordingly in order to properly handle the signal coming from the current sense block.

5.2 Simulation Results

To verify the functionality of the flying capacitor voltage balancing system proposed in Section 5.1, 3-level buck, 3-level boost and 3-level inverting buck–boost converters with a voltage-mode output control loop were designed and evaluated by means of SIMPLIS simulations. The power stage of each converter topology was implemented using ideal switch blocks featuring 35-m Ω on-resistance values. The loop circuit, including both the voltage-mode output loop and the voltage balancing block, as schematically represented in Fig. 5.5 and Fig. 5.8, was implemented using ideal components, ideal switches and type-III compensation. The same compensator block was employed for all topologies. A 4.7- μ F flying capacitance with 3-m Ω ESR, a 10- μ F output capacitance with 5-m Ω ESR and a 1- μ H inductance with 25-m Ω ESR were con-

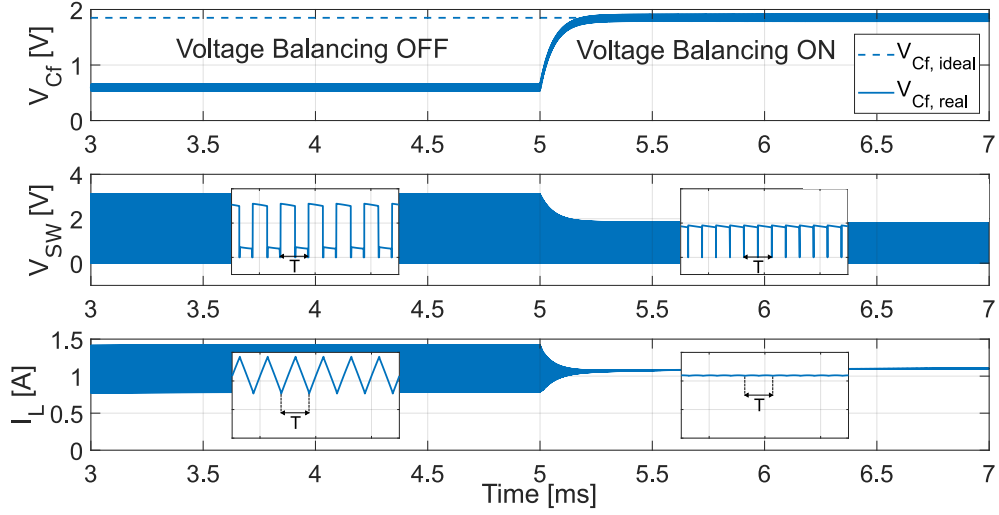


Figure 5.12: Simulated waveforms with and without voltage balancing loop for $V_{in} = 3.7$ V and $V_o = 1.8$ V ($D \simeq 0.5$).

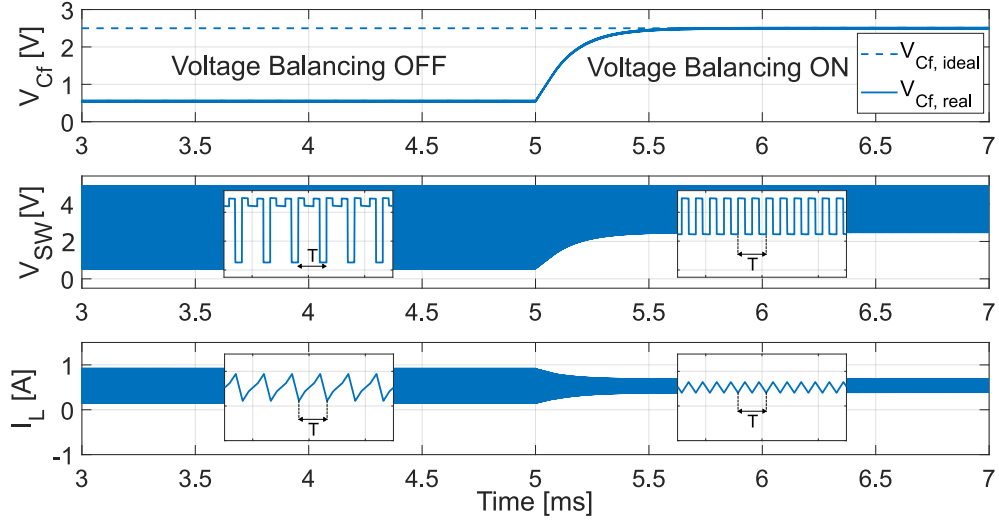


Figure 5.13: Simulated waveforms with and without voltage balancing loop for $V_{in} = 5$ V and $V_o = 3.7$ V ($D > 0.5$).

sidered; these specifications are coherent with what is available on the market for SMD components.

Different combinations of input voltage and output voltage were selected, in

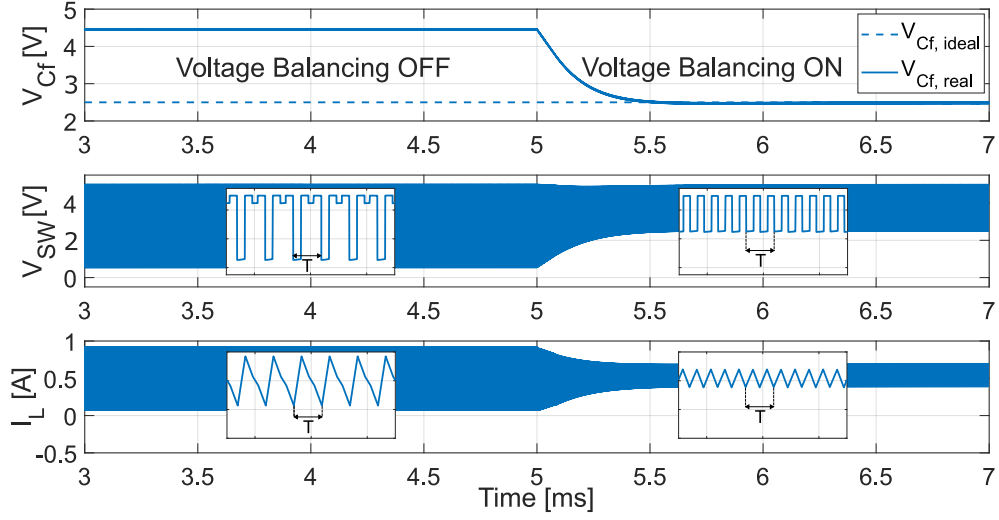


Figure 5.14: Simulated waveforms with and without voltage balancing loop for $V_{in} = 3.7$ V and $V_o = 5$ V ($D < 0.5$).

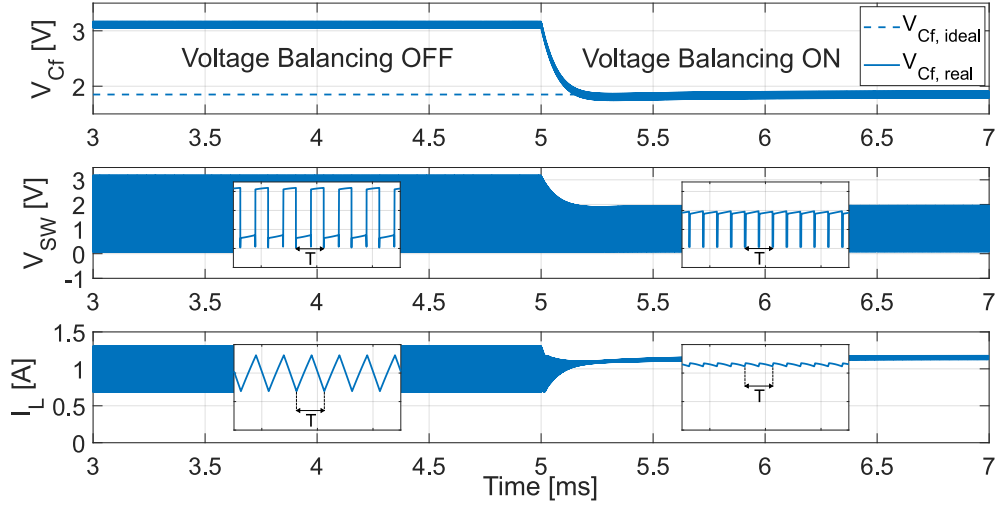


Figure 5.15: Simulated waveforms with and without voltage balancing loop for $V_{in} = 1.8$ V and $V_o = 3.7$ V ($D \simeq 0.5$).

order to cover the cases $D > 0.5$, $D < 0.5$ and $D \simeq 0.5$. The load current values were chosen in order to ensure 2-W output power. The switching frequency, equal to $1/T$, was set to 1 MHz.

For each combination of converter topology and input and output volt-

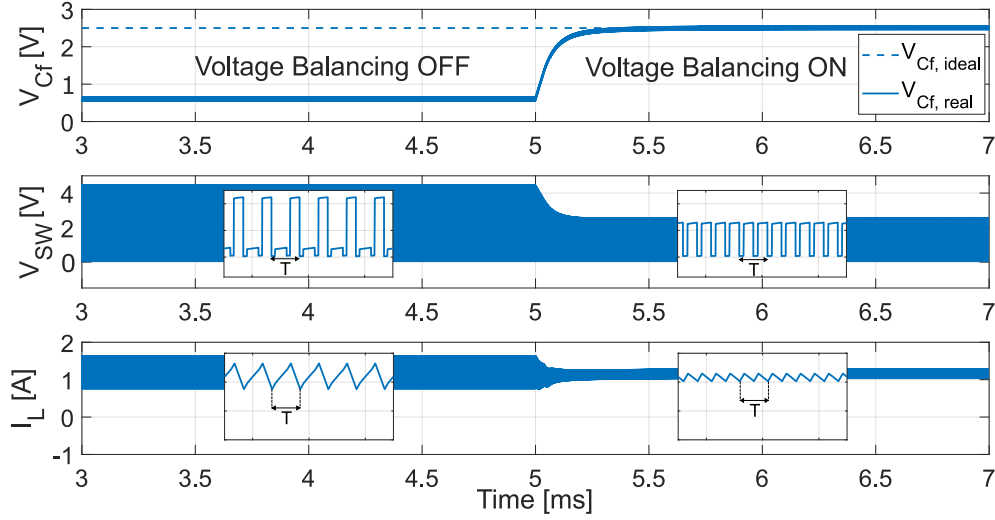


Figure 5.16: Simulated waveforms with and without voltage balancing loop for $V_{in} = 1.8$ V and $V_o = 5$ V ($D > 0.5$).

age, a transient simulation was performed in the SIMPLIS environment. The balancing loop was initially disconnected and the flying capacitor voltage was maintained fixed at a value different (higher or lower) than the correct one, i.e. $V_{Cf,ideal}$, until $t = 5$ ms, when the voltage balancing loop was activated. In order to maintain the flying capacitor voltage at the initial value, different from the balanced one, ideal switches and voltage generators were employed, fixing the flying capacitor voltage. At $t = 5$ ms the ideal switches and voltage generators were disconnected and the flying capacitor voltage was left free to evolve according to the voltage balancing loop action. This setup can only be investigated in simulation, since for a fabricated solution it is not possible to force an unbalanced condition, as this would determine drain-to-source voltages of the power switches which might exceed their rating, selected under the assumption that the flying capacitor voltage balancing is always maintained.

The simulation results for the 3-level buck, 3-level boost and 3-level inverting buck-boost converters are illustrated in Fig. 5.11–5.13, Fig. 5.14–5.16 and Fig. 5.17–5.19, respectively, covering the cases $D < 0.5$, $D \simeq 0.5$ and $D > 0.5$.

Each graph shows the voltage across the flying capacitor (V_{Cf}), the switching node voltage (V_{SW}) and the inductor current (I_L) in both an unbalanced and a balanced state. It can be seen how V_{SW} , and consequently the inductor voltage, carries the information about the imbalance and how, as expected, the inductor current ripple doubles in frequency after the voltage balancing is

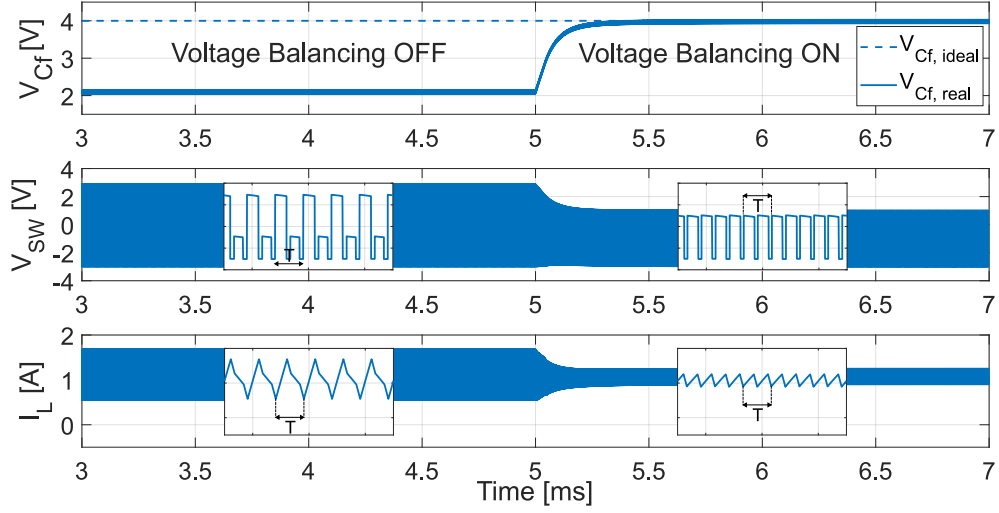


Figure 5.17: Simulated waveforms with and without voltage balancing loop for $V_{in} = 5$ V and $V_o = -3$ V ($D < 0.5$).

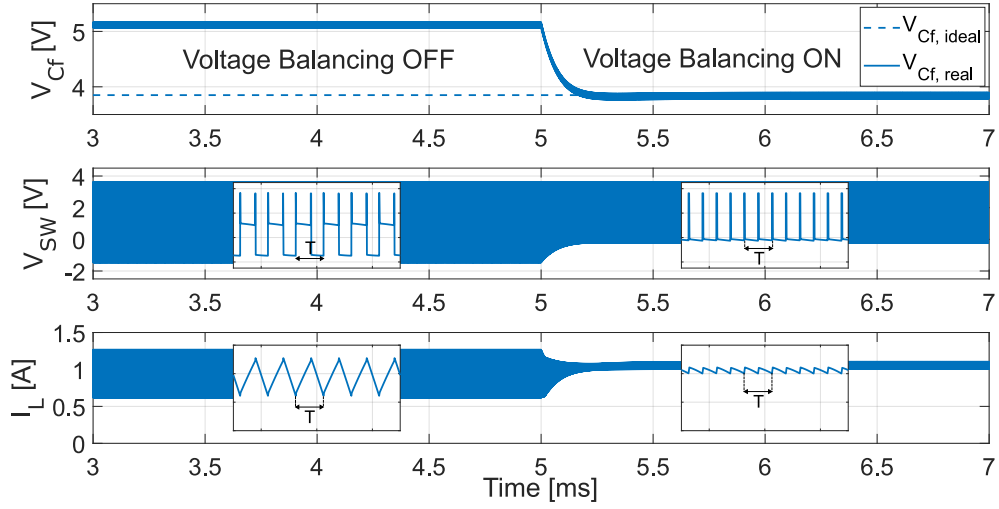


Figure 5.18: Simulated waveforms with and without voltage balancing loop for $V_{in} = 3.7$ V and $V_o = -4$ V ($D \simeq 0.5$).

activated, while also reducing in amplitude. These simulation results confirm the effectiveness and versatility of the proposed flying capacitor voltage balancing strategy. From the simulated waveforms it is also possible to derive an indication of the proposed voltage balancing circuit response time, which is of

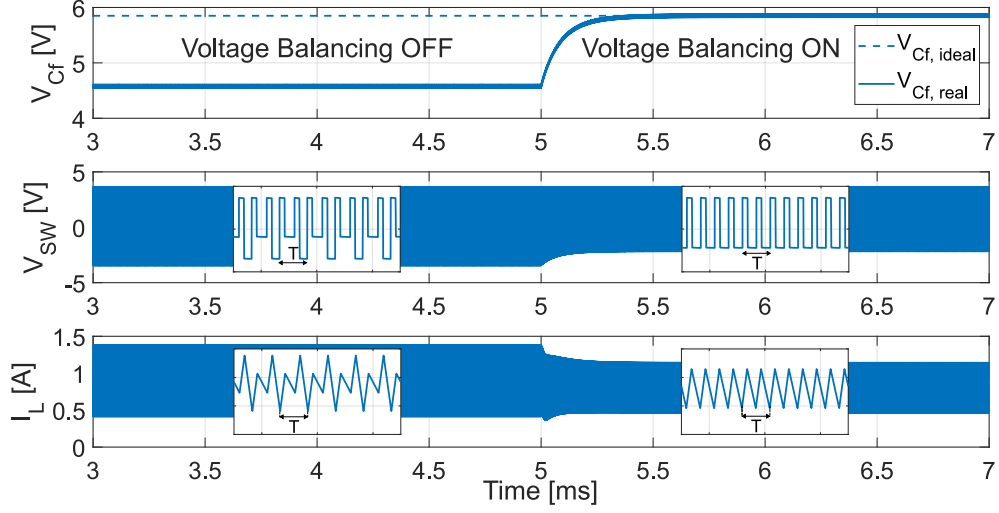


Figure 5.19: Simulated waveforms with and without voltage balancing loop for $V_{in} = 3.7$ V and $V_o = -8$ V ($D > 0.5$).

the order of a few hundreds of microseconds.

In the fabricated circuit it is not possible to force an unbalanced condition, as this would determine drain-to-source voltages of the power switches that might exceed their rating. For this reason, the response time for correcting an imbalance cannot be experimentally verified on silicon and is assessed here through simulation.

Chapter 6

SCMLIBB Simulation and Measurements Results

The simulation results for the proposed solution will be presented in this chapter. All simulations have been performed in Cadence Virtuoso and the technology adopted is the TSMC 180n gen2.

For the switches implementation, power transistors from the said technology have been used. A list of the devices with their respective ratings and FOM (figure of merit) can be seen in Tab. 6.1. The FOM is given by the on resistance multiplied by the occupied area. All the considered transistors are isolated DMOS.

Device	Rating	FOM($m\Omega * mm^2$)
ndl6_g5a_de_iso	$\sim 7V$	~ 4.5
ndl6_g5a_sa_iso	$\sim 7V$	~ 3
ndl6_g5a_iso	$\sim 10V$	~ 8
ndl12_g5a_iso	$\sim 18V$	~ 9.5
ndl12_g5a_iso_hp	$\sim 15V$	~ 7
ndl16_g5a_iso	$\sim 21V$	~ 12
ndl20_g5a_iso	$\sim 26V$	~ 15

Table 6.1: Performance of the two phase inverting buck-boost.

To take into account parasitics given by the metallization, in the simulation schematics for each power switch a $3.5 m\Omega$ series resistance and extra 30% capacitance between gate and drain, gate and source and drain and source, have been added, as illustrated in Fig. 6.1 (b).

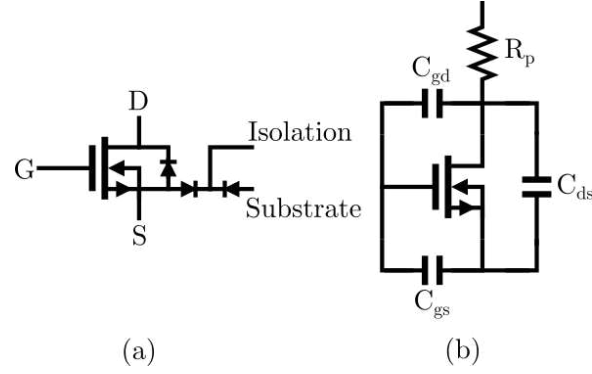


Figure 6.1: a) DMOS structure b) transistor extra capacitances and series resistance.

In the realization of the Cadence model for the solutions proposed in the previous chapter, it is important to consider the orientation of the transistors implementing the power switches. In DMOS, for which a model is illustrated in Fig.6.1 (a), the body is internally connected with the source, thus creating a parasitic diode between source and drain with the anode toward the drain. Due to this, during the circuit implementation particular attention must be paid to positioning the transistor in a way that avoids the turning on of this parasitic diode during standard operation.

Knowing this, before starting the modelling it is useful to consider for each topology the voltage seen by each switch in all operating phases: if this voltage changes sign between phases, in order to avoid the turning on of the parasitic diode, the switch will be modelled with two transistors in back-to-back configuration. The tables in Chapter 3 illustrating the supported voltage by each switch were created by taking as convention the voltage across the switch positive if the left side is higher, in this way by substituting V_{in} and V_{out} for the worst case which is $5.5V \Rightarrow -10V$, the result will show both the ideal ratings and if the switch needs a back-to-back configuration. For all the considered cases the simulations were performed considering all transistors with minimum length, two fingers, each with a width of $450 \mu m$, in the same ISO well and variable multiplicity, changed in order to optimize the switch size. This approach has been verified to give results similar or worse in terms of efficiency, than the case where the fingers width and number in the same ISO were changed. Therefore, for a preliminar analysis this method has been considered adequate to compare the different topologies.

The simulations have been performed considering ideal voltage pulse genera-

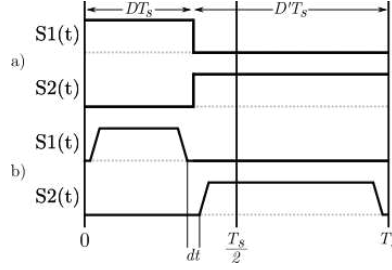


Figure 6.2: a) Ideal case switching signal b) Simulated case switching signal.

tors as drivers for the switches, with $V_{gs,on} = 5V$, $V_{gs,off} = 0V$ and a rise and fall time equal to 2 ns . In the theoretical analysis in Chapter 3, switches were considered ideal with an instant turn on and turn off time: this is, however, not true for real transistors. For this reason, to avoid cross conduction, i.e. the undesired turn on of two or more transistor simultaneously, a dead time of 7 ns has been placed at each switching point as shown in Fig. 6.2.

6.1 Two Phase Inverting Buck-Boost Model and Simulations

Starting with the two phase inverting buck-boost, from Tab. 6.2 that shows the result for the conversion case $5.5V \Rightarrow -10V$, it can be seen that no switch requires a back-to-back and all support at maximum $15.5V$. The chosen device for all switches is the *nd12_g5a_iso* which has a voltage rating of $\sim 18V$.

Switch	Phase 1	Phase 2	Phase 3	Phase 4
$S1$	-	15.5	15.5	15.5
$S2$	15.5	15.5	-	15.5
$S3$	-15.5	-	-	-
$S4$	15.5	15.5	-	15.5

Table 6.2: Switch supported voltage for the two phase inverting buck-boost for $5.5V \Rightarrow -10V$.

The graph in Fig. 6.3 illustrates the inductors current in steady state for the conversion case $V_{in} = 3.3\text{ V}$, $V_{out} = -5\text{ V}$, $I_{out} = 0.5\text{ A}$, $D = 0.601$ with the switches multiplicity $mult = 150$ and a switching frequency $f_s = 1\text{ MHz}$. It can be easily seen than the assumptions made in the previous chapter are valid and approximate well the behaviour of the circuit. The same has been done

for the conversion case $V_{in} = 3.3\text{ V}$, $V_{out} = -10\text{ V}$, $I_{out} = 0.5\text{ A}$, $D = 0.751$ using the same setup. The results are shown in Fig. 6.4.

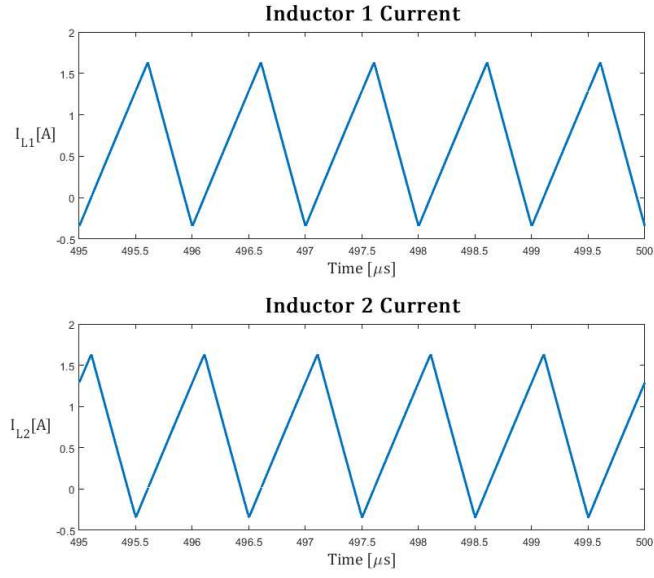


Figure 6.3: Inductor 1 current for the conversion case $3.3V \Rightarrow -5V$.

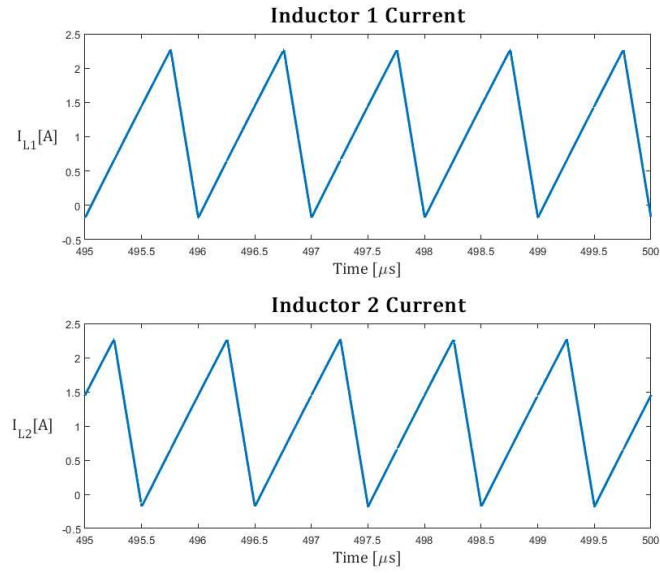


Figure 6.4: Inductor 1 current for the conversion case $3.3V \Rightarrow -10V$.

An important parameter for this project is the output voltage ripple, which needs to be lower than 50 mV . To have an estimation on the size of the required output capacitor, (3.17) or (3.19) can be used considering the worst case ($V_{in} = 2\text{ V}$, $V_{out} = -10\text{ V}$, $D = 0.833$): in order to obtain $\Delta v = 50\text{ mV}$, $C_{out} = 6.66\text{ }\mu\text{F}$ is required. The chosen capacitor, however, needs to have a larger nominal capacitance value in order to account for de-rating. A research on the market resulted in no capacitor respecting the required footprint and the size limit featuring a sufficient capacitance, therefore the solution is to put two equal capacitors in parallel. The chosen capacitor has a nominal capacitance of $22\text{ }\mu\text{F}$ and a rating of 16 V . Considering derating at $V_{out} = -10 \Rightarrow C_{out} = 3.48\text{ }\mu\text{F}$: hence, two capacitors in parallel are sufficient. Fig. 6.5 and Fig. 6.6 show the simulation results for the output voltage for different conversion cases.

The efficiency can be derived from the simulation, which takes into account the losses due to the on resistance of the transistors, the switching losses and the conduction losses due to inductor and capacitor parasitics. The core losses of the inductors were computed using (3.1), and taken into account. Tab. 6.3 shows the efficiency η , the duty cycle D , the average inductor current I_L , the inductor current ripple Δi , the output voltage ripple Δv , the load current I_{out} , the input voltage V_{in} and the output voltage V_{out} for the two phase inverting buck-boost.

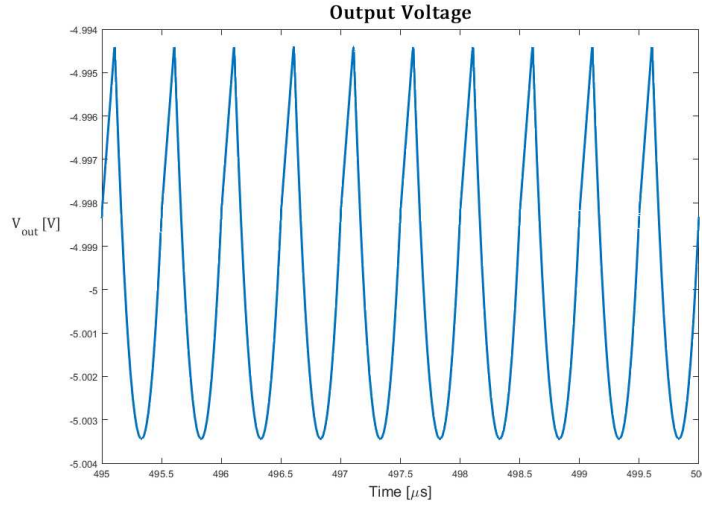


Figure 6.5: Output voltage for the conversion case $3.3\text{ V} \Rightarrow -5\text{ V}$.

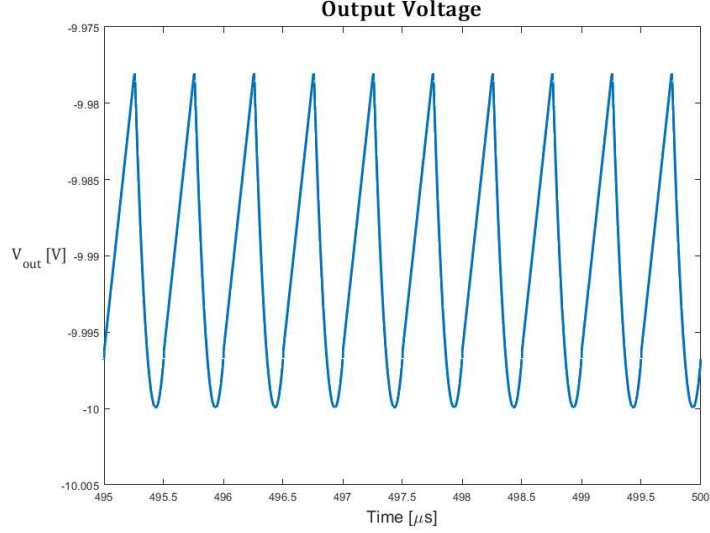


Figure 6.6: Output voltage for the conversion case $3.3V \Rightarrow -10V$.

$V_{in}[V]$	$V_{out}[V]$	$I_{out}[I]$	D	$I_L[A]$	$\Delta i[A]$	$\Delta v[mV]$	η
3.3	-5	0.1	0.601	0.137	2.023	9.6	74.2%
3.3	-10	0.1	0.751	0.219	2.420	13.1	78.5%
3.3	-5	0.5	0.601	0.646	1.974	11.52	91.5%
3.3	-10	0.5	0.751	1.05	2.446	22.6	90.8%
3.3	-5	1	0.601	1.3	1.952	12.9	92.3%
3.3	-10	1	0.751	2.125	2.420	40	91.8%

Table 6.3: Simulation results for the two phase inverting buck-boost.

6.2 Switched Capacitor Inverting Buck-Boost Model and Simulations

Tab. 6.4 shows the result of the switch analysis for the conversion case $5.5V \Rightarrow -10V$. It can be seen that no switch requires a back-to-back and the input charge pump switches support $5.5V$ at maximum, while the inverting buck-boost stage switches support $21V$ at maximum. The chosen device are the *ndl6-g5a-iso* with a voltage rating of $\sim 7V$ for switches $S1, S2, S3$, the *ndl12-g5a-iso* with a voltage rating of $\sim 18V$ for switch $S4$ and the *ndl20-g5a-iso* with a voltage rating of $\sim 26V$ for switch $S5$. From Tab. 3.6 it can be seen that the total inductor current, which is the sum of inductor

Switch	Phase 1	Phase 2
$S1$	-	5.5
$S2$	5.5	—
$S3$	—	5.5
$S4$	15.5	—
$S5$	—	21

Table 6.4: Switch supported voltage for the switched capacitor inverting buck-boost for $5.5V \Rightarrow -10V$.

average current and half of the current ripple, in many case exceed $5A$, i. e. the current saturation limit of the chosen inductor. In order to avoid that, it has been decided to double the switching frequency $f_s = 2\text{ MHz}$ to reduce the inductor current ripple.

The switches multiplicity are 200 for $S1, S2$, 150 for $S4$ and 100 for $S3, S5$. The graph in Fig. 6.7 illustrates the inductor current in steady state for the conversion case $V_{in} = 3.3\text{ V}, V_{out} = -5\text{ V}, I_{out} = 0.5\text{ A}, D = 0.432$. It can be easily seen than the assumptions made in the previous chapter are valid and approximate well the behaviour of the circuit. The same simulation has been

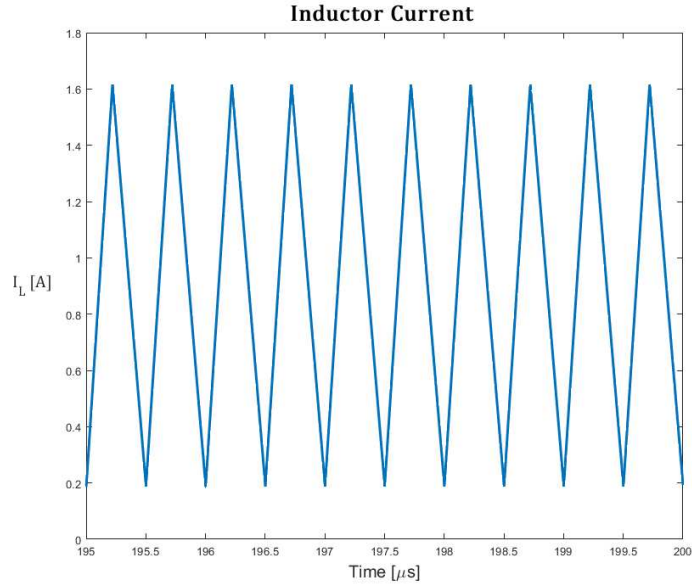


Figure 6.7: Inductor current for the conversion case $3.3V \Rightarrow -5V$.

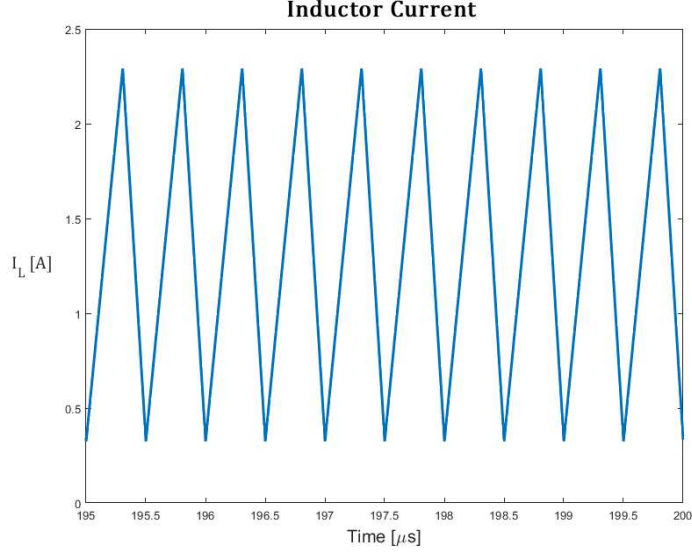


Figure 6.8: Inductor current for the conversion case $3.3V \Rightarrow -10V$.

performed for the conversion case $V_{in} = 3.3\text{ V}$, $V_{out} = -10\text{ V}$, $I_{out} = 0.5\text{ A}$, $D = 0.605$ using the same setup. The results are shown in Fig. 6.8.

For the output capacitors, the ones chosen in the previous section for the two phase satisfy the output voltage requirement also in this case because of the increase in the switching frequency. Fig. 6.9 and Fig. 6.10 shows the simulation results for the output voltage for the typical conversion cases.

The efficiency can be derived from the simulation, which takes into account the losses due to the on resistance of the transistors, the switching losses and the conduction losses due to inductor and capacitor parasitics.

$V_{in}[V]$	$V_{out}[V]$	$I_{out}[A]$	D	$I_L[A]$	$\Delta i[A]$	$\Delta v[mV]$	η
3.3	-5	0.1	0.432	0.185	1.479	10.75	76.3%
3.3	-10	0.1	0.605	0.217	2.029	23.35	82.2%
3.3	-5	0.5	0.432	0.903	1.427	10.75	88.8%
3.3	-10	0.5	0.605	1.311	1.956	23.35	90.2%
3.3	-5	1	0.432	1.807	1.417	18.26	89.8%
3.3	-10	1	0.605	2.671	1.937	47.62	89.8%

Table 6.5: Simulation result for the switched capacitor inverting buck-boost.

The core losses of the inductor were computed using (3.1), and taken into ac-

count. Tab. 6.5 shows the efficiency η , the duty cycle D , the average inductor current I_L , the inductor current ripple Δi , the output voltage ripple Δv , the load current I_{out} , the input voltage V_{in} and the output voltage V_{out} for the

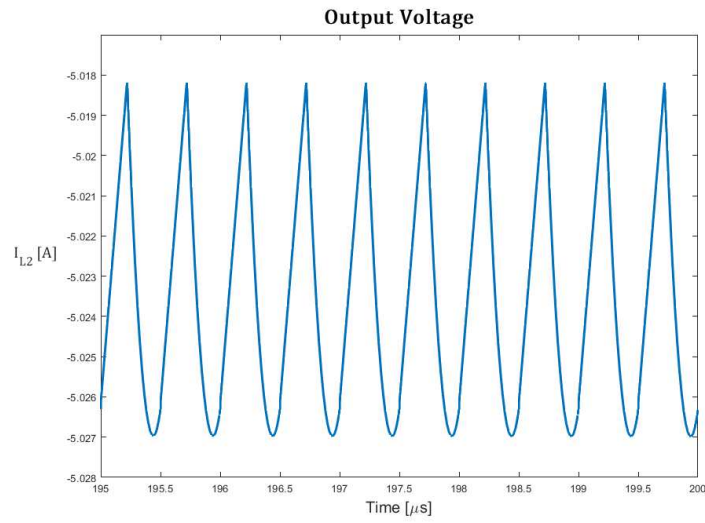


Figure 6.9: Output voltage for the conversion case $3.3V \Rightarrow -5V$.

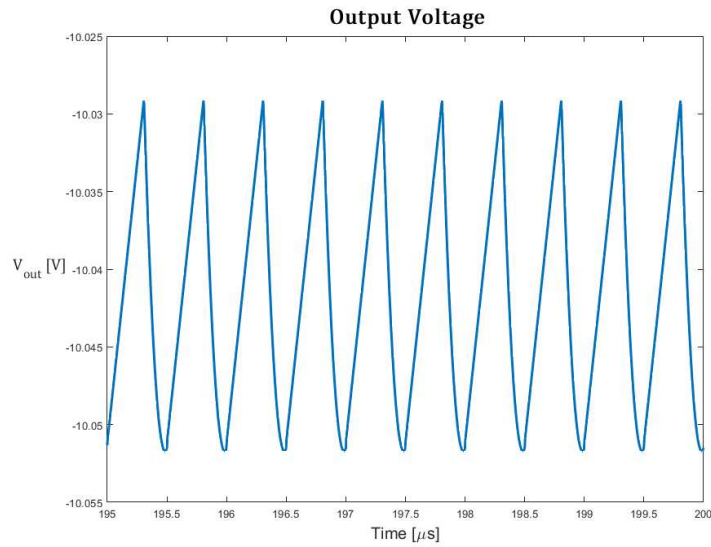


Figure 6.10: Output voltage for the conversion case $3.3V \Rightarrow -10V$.

switched capacitor inverting buck-boost.

6.3 Switched Capacitor Three Level Inverting Buck-Boost Model and Simulations

Tab. 6.6 shows the result of the switch rating analysis for the worst conversion case, i.e. $5.5V \Rightarrow -10V$. It can be seen that no switches require a back-to-back and the input charge pump switches support $5.5V$ at maximum, while the inverting stage switches support $11.5V$ at maximum. The chosen device are the *ndl6_g5a_iso* with a voltage rating of $\sim 7V$ for switches $S1, S2, S3, S4$, the *ndl12_g5a_iso_hp* with a voltage rating of $\sim 15V$ for switch $S5, S6, S7$.

From Tab. 3.9 it can be seen that the inductor current ripple is greatly reduced, which avoids exceeding the inductor saturation limit, thus increasing efficiency and reducing the core losses.

The switches multiplicity are 200 for $S1, S2, S3, S4$ and 150 for $S5, S6, S7$.

The graphs in Fig. 6.11 illustrate the inductor current and voltage in steady

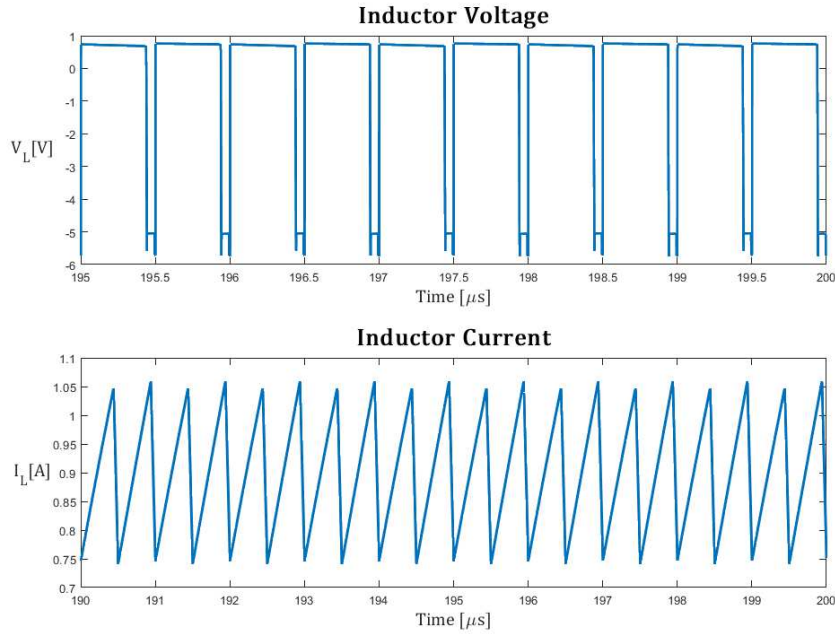


Figure 6.11: Simulated inductor current for the switched capacitor three level buck-boost in the conversion case $3.3V \Rightarrow -5V$.

Switch	Phase 1	Phase 2	Phase 3	Phase 4
$S1$	-5.5	-	-	-
$S2$	-	5.5	5.5	5.5
$S3$	5.5	-	-	-
$S4$	-	5	5	5
$S5$	11.5	11.5	-	11.5
$S6$	-	-	11.5	-
$S7$	11.5	-	-	-

Table 6.6: Switch supported voltage for the switched capacitor three level inverting buck-boost for $5.5V \Rightarrow -10V$.

state for the conversion case $V_{in} = 3.3 V, V_{out} = -5 V, I_{out} = 0.5 A, D = 0.435$. The switching frequency is $f_s = 1 MHz$. It can be easily seen than the assumptions made in the previous chapter are valid and approximate well the behaviour of the circuit. The same simulation has been performed for the conversion case $V_{in} = 3.3 V, V_{out} = -10 V, I_{out} = 0.5 A, D = 0.607$. Results are shown in the graphs in Fig. 6.12.

The multilevel topology, as said in the previous Chapter, has the disadvan-

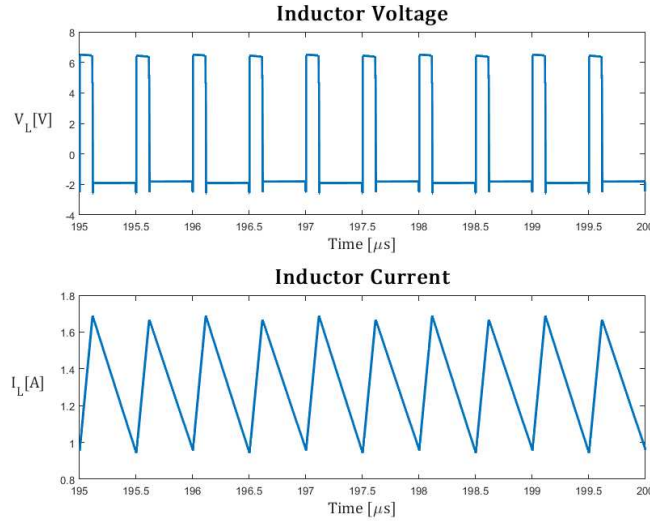


Figure 6.12: Simulated inductor current for the switched capacitor three level buck-boost in the conversion case $3.3V \Rightarrow -10V$.

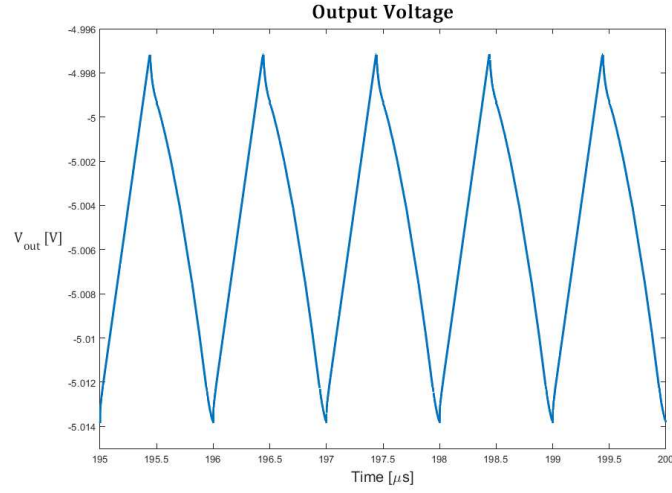


Figure 6.13: Output voltage for the conversion case $3.3V \Rightarrow -5V$.

tage that the flying capacitor voltage need to be balance. In this stage of the modelling this system has not been implemented yet. In order to perform the simulation without adding control loops, the flying capacitor has been substituted with an ideal voltage controlled voltage generator, that maintains the

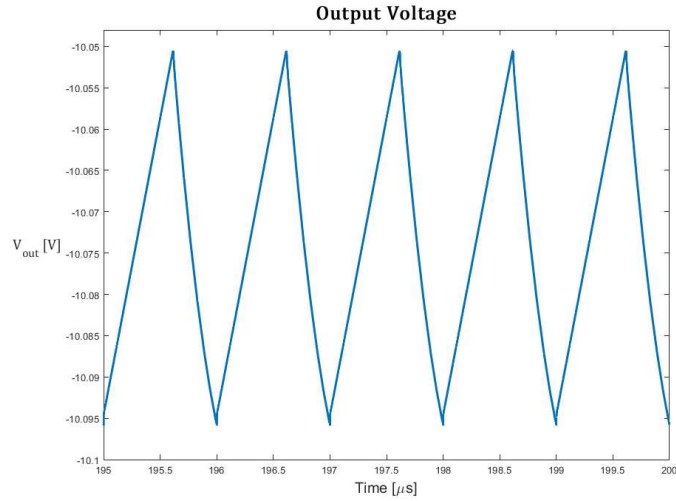


Figure 6.14: Output voltage for the conversion case $3.3V \Rightarrow -10V$.

capacitor voltage to the expected value reported in (3.36).

For the output capacitors the ones chosen in the previous section satisfy the output voltage ripple requirements, except for the case $V_{in} = 3.3\text{ V}$, $V_{out} = -5\text{ V}$, $I_{out} = 1\text{ A}$ when the converter would need four of the chosen capacitors in order to fulfil the requirement on the output voltage ripple. Since this conversion case is rarely employed, increasing the switching frequency for this specific case to 2 MHz has been preferred, to avoid the necessity of extra external output capacitors, paying instead a penalty on the efficiency. Fig. 6.13 and Fig. 6.14 shows the simulation results for the output voltage for the typical conversion ratios.

The efficiency can be derived from the simulation, which takes into account the losses due to the on resistance of the transistors, the switching losses and the conduction losses due to inductor and capacitor parasitics. The core losses of the inductor were computed using (3.1), and taken into account. Tab. 6.7 shows the efficiency η , the duty cycle D , the average inductor current I_L , the inductor current ripple Δi , the output voltage ripple Δv , the load current I_{out} , the input voltage V_{in} and the output voltage V_{out} for the two phase inverting buck-boost.

$V_{in}[V]$	$V_{out}[V]$	$I_{out}[I]$	D	$I_L[A]$	$\Delta i[A]$	$\Delta v[mV]$	η	$f_s[MHz]$
3.3	-5	0.1	0.435	0.187	0.281	5.0	79.4%	1
3.3	-10	0.1	0.607	0.267	0.765	12.0	87.5%	1
3.3	-5	0.5	0.435	0.901	0.314	17.81	91.8%	1
3.3	-10	0.5	0.607	1.306	0.734	46.35	92.4%	1
3.3	-5	1	0.435	1.823	0.294	36.10	90.5%	1
3.3	-10	1	0.607	2.663	0.390	49.65	87.0%	2

Table 6.7: Simulation result for the switched capacitor three level inverting buck-boost.

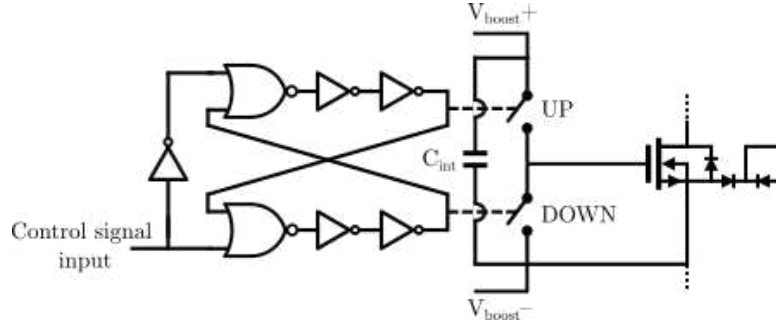


Figure 6.15: Driver circuit.

6.3.1 Standard Bootstrap Driving Scheme

In order to refine the model, the ideal driver was substituted by the circuit illustrated in Fig. 6.15. The disoverlap circuit avoids the turning on of both the up and down path at the same time. This driver requires a bootstrap capacitor, which is at first charged at V_{in} , and then connected with one terminal to the source of the switch that is driven and with the other to the driver up branch. In this way the capacitor provides the driver with a voltage higher than the source enough to turn on the switch. A small integrated capacitance is placed inside the driver to provide supply to the driving logic while the bootstrap capacitor is detached for refresh.

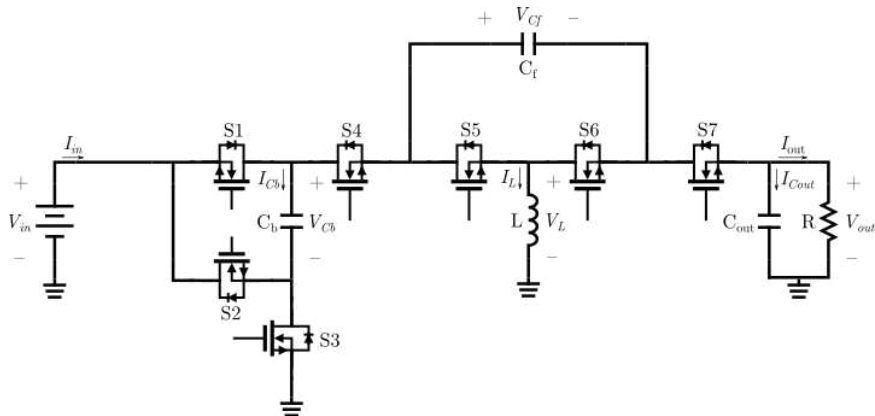


Figure 6.16: Switched capacitor three level inverting buck-boost circuit.

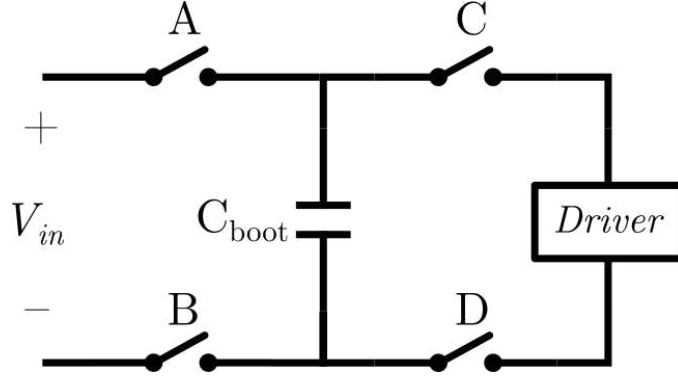


Figure 6.17: Driver bootstrap circuit.

Through simulations the capacitance seen at the gate of a power transistor was estimated roughly equal to 800 pF . Therefore, the bootstrap capacitor required is too large to be integrated, thus an external component must be employed.

As a baseline solution, a driving scheme where each power switch has its own bootstrap capacitor was taken into consideration. On a further inspection of the circuit, illustrated in Fig. 6.16, switch $S2$ and $S3$ do not need an external capacitor: capacitor C_b can be used as a bootstrap for the driver of $S2$ and V_{in} can be used as supply for the driver of $S3$. The other five switches need an external capacitor with a size $\sim 10\text{ nF}$, one with 50 nF has been chosen in order to take into account the de-rating.

Fig. 6.17 shows the complete driver circuit, where switches A and B allow restoring the bootstrap capacitor and switches C and D connect the capacitor to the driver. A parasitic inductor of 5 nH was consider for the bootstrap capacitor. It is important to include the parasitic inductor because it determines ringing which can cause spikes exceeding the voltage supported by the power switch gate, thus breaking the device. Moreover the ringing also affects the required rating of the transistor employed for the switching of the bootstrap capacitor. Fig. 6.18 shows the complete driver section.

A preliminary analysis has been performed in order to estimate the bootstrap switch ratings, orientation and if any need a back to back configuration, considering cases with both $D > 0.5$ and $D < 0.5$. Tab. 6.8 shows the result. This analysis does not take into account the dead time interval, added to avoid cross conduction, the parasitic inductor effect and the startup. A simulation has been performed to check if the transistor ratings and configuration were adequate also including the ringing due to the parasitic inductor and statup:

Ideal Ratings and Implementation													
	<i>S1A</i>	<i>S1B</i>	<i>S1C</i>	<i>S1D</i>	<i>S4A</i>	<i>S4B</i>	<i>S4C</i>	<i>S4D</i>	<i>S5A</i>	<i>S5B</i>	<i>S5C</i>	<i>S5D</i>	
Back-to-Back	No	No	No	No	No	No	Yes	Yes	Yes	Yes	Yes	Yes	
Ratings	5.5	5.5	5.5	5.5	11	11	4	4	6.6	6.6	10	10	
			<i>S6A</i>	<i>S6B</i>	<i>S6C</i>	<i>S6D</i>	<i>S7A</i>	<i>S7B</i>	<i>S7C</i>	<i>S7D</i>			
Back-to-Back			Yes	Yes	No	No	No	No	No	No			
Ratings			10	10	10	10	10	10	10	10			
Simulated Ratings and Implementation													
	<i>S1A</i>	<i>S1B</i>	<i>S1C</i>	<i>S1D</i>	<i>S4A</i>	<i>S4B</i>	<i>S4C</i>	<i>S4D</i>	<i>S5A</i>	<i>S5B</i>	<i>S5C</i>	<i>S5D</i>	
Back to-Back	No	No	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
Device	6 <i>sa</i>	6 <i>sa</i>	6 <i>sa</i>	6 <i>sa</i>	12 <i>hp</i>	12 <i>hp</i>	12 <i>hp</i>	12 <i>hp</i>	12 <i>hp</i>	12 <i>hp</i>	12 <i>hp</i>	12 <i>hp</i>	
			<i>S6A</i>	<i>S6B</i>	<i>S6C</i>	<i>S6D</i>	<i>S7A</i>	<i>S7B</i>	<i>S7C</i>	<i>S7D</i>			
Back-to-Back			Yes	Yes	No	No	No	No	No	No			
Device			12 <i>hp</i>	12 <i>hp</i>	12 <i>hp</i>	12 <i>hp</i>	12 <i>hp</i>	12 <i>hp</i>	12 <i>hp</i>	12 <i>hp</i>			

Table 6.8: Simulation result for the driver switches type and implementation for the standard bootstrap solution.

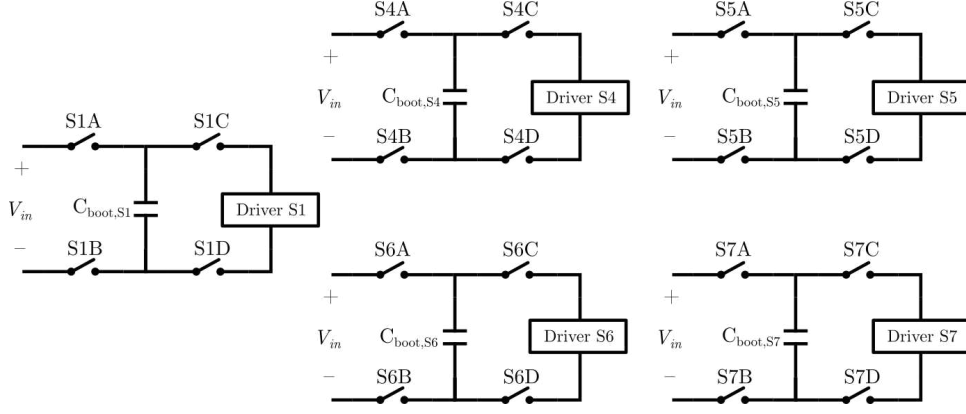


Figure 6.18: Standard driver bootstrap circuit.

the produced changes can be seen in Tab. 6.8 which illustrates the final device choice, where *6sa* stands for *ndl6_g5a_sa_iso* and *12hp* for *ndl12_g5a_iso_hp*. The next step was to size the driver switch transistors in order to achieve the desired rise time for the power switch. Also in this case, as for the power switches, the transistors feature minimum length, two $450 \mu m$ fingers in the same ISO well and variable multiplicity, changed in order to optimize the switch size. The target rise time for the V_{gs} of the power transistor is lower than the $5 ns$ in order to reduce losses due to the inactive time between two consecutive phases. The two switches that provide the refresh of the bootstrap capacitor are not critical since they do not play a role in the turning on of the power switch, thus their multiplicity has been set to 2. The switches that define the rise time are the ones that connect the bootstrap capacitor to the driver and the up side switch of the driver itself. The up and down switch of the driver are implemented in the model employing ideal switches with $R_{on} = 1 \Omega$; therefore, the maximum on resistance of the bootstrap switches must be $\sim 1 \Omega$ in order to meet the requirement of turn on time lower than $5 ns$.

The multiplicity of each bootstrap switch transistor has been chosen relying on Cadence simulations to verify that a turn on time lower $5 ns$ was achieved. Tab. 6.9 shows the driver switches final size.

To conclude, this considered bootstrap solution requires five external capacitors and the total area, considering as unit a transistor with multiplicity 1, is 116.

Final Size and Implementation								
	$S1A$	$S1B$	$S1C$	$S1D$				
Multiplicity	2	2	2	2				
Device	6sa	6sa	6sa	6sa				

	$S4A$	$S4B$	$S4C$	$S4D$	$S5A$	$S5B$	$S5C$	$S5D$
Multiplicity	2	2	12	12	2	2	6	6
Device	12hp	12hp	12hp	12hp	12hp	12hp	12hp	12hp

	$S6A$	$S6B$	$S6C$	$S6D$	$S7A$	$S7B$	$S7C$	$S7D$
Multiplicity	2	2	2	2	2	2	2	2
Device	12hp	12hp	12hp	12hp	12hp	12hp	12hp	12hp

Table 6.9: Final size and implementation for the standard bootstrap solution.

6.3.2 Multiplexer Bootstrap Driving Scheme

Since one of the project requirements is minimizing the BOM, the standard solution with an external capacitor per switch is clearly not attractive. On a further inspection on the switching scheme for the switched capacitor three level buck-boost, illustrated in Fig. 3.13 and in Fig. 3.14, it can be seen that the switches $S4$ and $S5$ never turn on at the same time and the same happens for switches $S6$ and $S7$: their control signals, in fact, are shifted by half a period, which is fixed and not dependent on the duty cycle.

A standard driver can only pull the gate to a high voltage in order to turn the switch on or short it to the source to turn the switch off. If instead a driver which can also leave its output at a high impedance state is employed, once the gate capacitance is charged and the power switch is on, the bootstrap cap can be detached from the driver and used for another switch. Fig. 6.19 shows the complete driver section, while Fig. 6.20 illustrates an example of the control signal required for the up and down switch of the driver.

For the analysis and simulation of this system, the results obtained in the

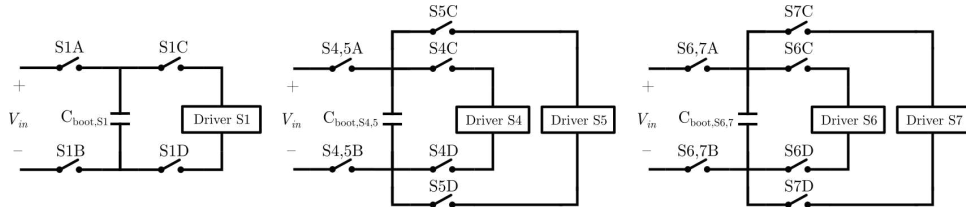


Figure 6.19: Driver multiplexer circuit.

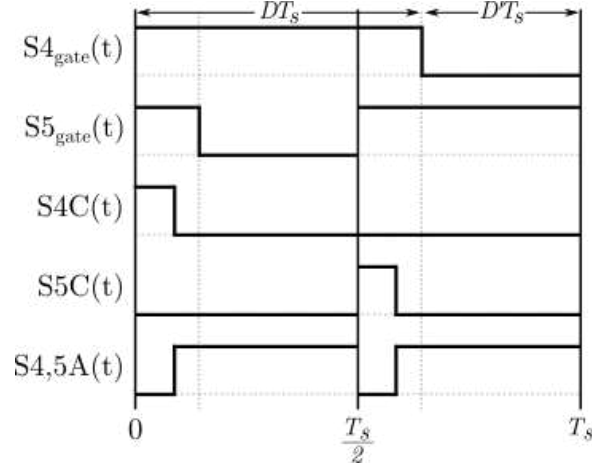


Figure 6.20: Example of the switching scheme for the multiplexer driver.

previous section regarding the gate capacitance and the switch sizing process are still valid. What needs to be recalculated are the ratings of the driver switches and if they need to be implemented with a back-to-back configuration. Tab. 6.11 shows the theoretical analysis results and the simulated results, which differ since in the simulation also ringing and startup were taken into account.

Final size and Implementation						
	<i>S1A</i>	<i>S1B</i>	<i>S1C</i>	<i>S1D</i>		
Multiplicity	2	2	2	2		
Device	6sa	6sa	6sa	6sa		

	<i>S4, 5A</i>	<i>S4, 5B</i>	<i>S4C</i>	<i>S4D</i>	<i>S5C</i>	<i>S5D</i>
Multiplicity	2	2	12	12	6	6
Device	12hp	12hp	12hp	12hp	12hp	12hp

	<i>S6, 7A</i>	<i>S6, 7B</i>	<i>S6C</i>	<i>S6D</i>	<i>S7C</i>	<i>S7D</i>
Multiplicity	2	2	2	2	2	2
Device	12hp	12hp	12hp	12hp	12hp	12hp

Table 6.10: Final size and implementation of the driver switches for the multiplexer bootstrap driving solution.

As said above, the switch sizing process in order to achieve a rise time of the power switch V_{gs} below 5 ns is still valid, thus, since the switches have

Ideal Ratings and Implementation											
	S1A	S1B	S1C	S1D	S4, 5A	S4, 5B	S4C	S4D	S5C	S5D	
Back-to-Back	No	No	No	No	No	No	Yes	Yes	No	No	
Ratings	5.5	5.5	5.5	5.5	11	11	6.6	6.6	10.5	10.5	
	S6, 7A			S6, 7B		S6C	S6D	S7C	S7D		
Back-to-Back	Yes			Yes		No	No	No	No		
Ratings	10			10		10	10	10	10		
Simulated Ratings and Implementation											
	S1A	S1B	S1C	S1D	S4, 5A	S4, 5B	S4C	S4D	S5C	S5D	
Back-to-Back	No	No	No	No	Yes	Yes	Yes	Yes	Yes	Yes	
Device	6sa	6sa	6sa	6sa	12hp	12hp	12hp	12hp	12hp	12hp	
	S6, 7A			S6, 7B		S6C	S6D	S7C	S7D		
Back-to-Back	Yes			Yes		Yes	Yes	Yes	Yes		
Device	12hp			12hp		12hp	12hp	12hp	12hp	12hp	

Table 6.11: Simulation results for the driver switches type and implementation for the multiplexer bootstrap driving solution.

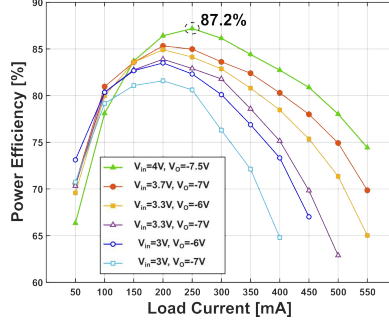


Figure 6.21: (a) Chip microphotograph and (b) layout of the V_{Cf} voltage balancing block.

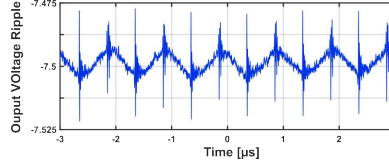


Figure 6.22: (a) Chip microphotograph and (b) layout of the V_{Cf} voltage balancing block.

the same ratings in both solutions, the multiplicity found for the standard driving scheme can be used also for the driver multiplexer. Tab. 6.10 shows the final size for the driver switches. The total area, still considering as unit the transistor with multiplicity of 1, is 104. The multiplexer bootstrap driving scheme features a lower area and fewer of external capacitors with respect to the standard bootstrap driving scheme, thus it will be the one adopted for the considered project.

6.4 Experimental Results

The proposed SC 3L IBB converter was fabricated in a 180nm BCD process and experimentally characterized considering a 1MHz switching frequency, a 1μH inductor, a 4.7μF flying capacitor and a 10μF output capacitor. The SC 3L IBB converter operation was tested for various operating points: the measured efficiency as a function of the load current is reported in Fig. 6.21, along with A peak efficiency value equal to 87.2% is achieved. The measured output voltage ripple is also illustrated in Fig. 6.22.

A comparison with the state-of-the-art is presented in Tab. 6.12

Table 6.12: Comparison with state-of-the-art inverting DC–DC converters

	[1] JSSC 2015	[2] Electr. Letters 2018	[3] JSSC 2021	[7] Commercial 2015	This Work
Process	0.35 μm BCD	0.18 μm BCD	0.35 μm BCD	—	0.18 μm BCD
Area [mm^2]	2.94	1.81	3.68	—	5.98
Input Voltage [V]	2.9 $\sim$ 4	1.8	2.7 $\sim$ 4.5	2.7 $\sim$ 5.5	2.5 $\sim$ 4
Output Voltage [V]	-3.8 $\sim$ -5.9	-4	-4.7	-2 $\sim$ -15	-4 $\sim$ -7.5
Inductor [μH]	10	4.7	10	4.7	1
Output Capacitor [μF]	4.7	4.7	10 + 1	22	44
Switching Frequency [MHz]	1	0.5	1	1.4	1
Maximum Output Current [mA]	300	20	360	400	550
Maximum Output Power [W]	1.8	0.08	3.5	3	4.125
Power Density [W/mm^2]	0.612	0.044	0.951	—	0.690
Peak Efficiency [%]	90.5 @ 50mA	89.0 @ 20mA	89.3 @ 100mA	82.0 @ 250mA	87.2 @ 250mA
Load Regulation [mV/mA]	0.74	—	0.06	0.7	0.5
Output Ripple [mV]	< 57	—	< 30	—	< 50

The voltage balancing block was implemented according to the architecture detailed in Section II and illustrated schematically in Fig. 5.5 and Fig. 5.8. The resistive divider was set to 1/10, by selecting R_A and R_B equal to 10 k Ω and 100 k Ω , respectively; whereas the ratio between capacitors C_A and C_B was set to 1 considering the trade-off between speed (the larger the ratio, the faster the response), area occupation (the larger the ratio, the larger the occupied area by the capacitors) and stability. Capacitances C_A , C_B and C_c were implemented through MOM (metal-oxide-metal) capacitors, as they exhibit better matching with respect to MIM (metal-insulator-metal), and they were all set equal to 1 pF. The total current consumption of the V_{Cf} voltage balancing block is 660 μA , which is negligible with respect to the targeted load current values that are in the range of hundreds of milliamperes. The current consumption of the voltage balancing block could be lowered by careful optimization of the operational amplifier design: this was not performed in the fabricated implementation as the achieved current consumption is acceptable for the targeted application, especially considering the load current levels. In this test-chip realization, in order to ensure extensive testability, the triangular waves and the ck_{pulse} signal were provided externally by means of synchronized function generators; they can however be easily generated on-chip. The switching frequency was set to 1 MHz.

A microphotograph of the fabricated test-chip is illustrated in Fig. 6.23(a), while Fig. 6.23(b) shows the layout of the proposed V_{Cf} voltage balancing block, featuring a 680 $\mu\text{m} \times 420 \mu\text{m}$ area, which could be reduced through layout optimization. The overall converter topology, which combines a voltage-doubler switched-capacitor structure and a 3-level inverting buck-boost architecture, and its performance are detailed in [17]: they are not reported here as this paper focuses specifically on the flying capacitor voltage balancing im-

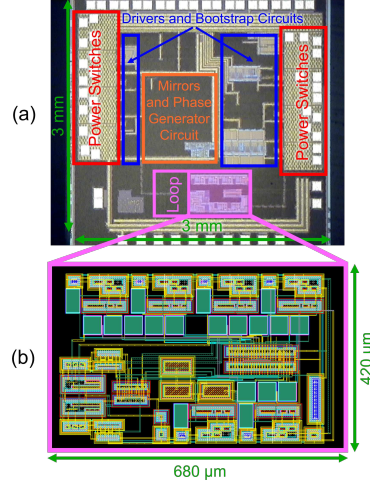


Figure 6.23: (a) Chip microphotograph and (b) layout of the V_{Cf} voltage balancing block.

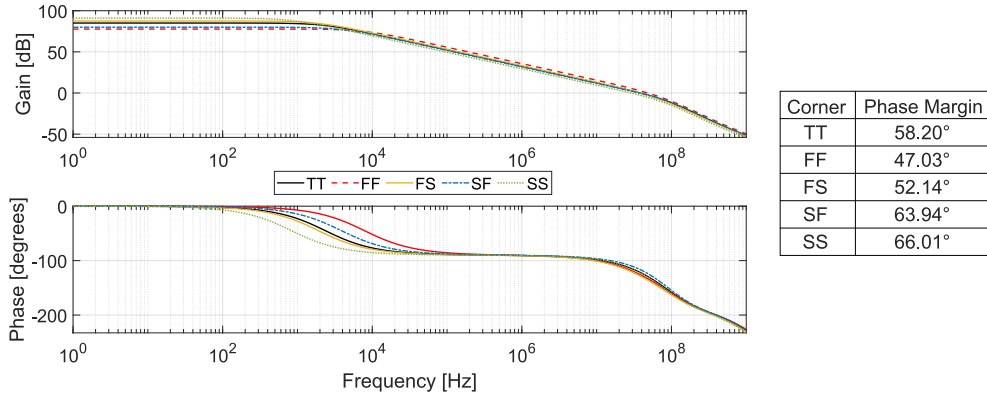


Figure 6.24: Simulated Bode diagrams of the implemented amplifier for different process corners (TT-typical, FF-fast/fast, FS-fast/slow, SF-slow/fast, SS-slow-slow) supposing a 5-V supply voltage .

plementation. A $1\text{-}\mu\text{H}$ inductor, a $4.7\text{-}\mu\text{F}$ flying capacitor and a $10\text{-}\mu\text{F}$ output capacitor, with ESR values matching the ones considered in the simulations reported in Section III, were employed as external components.

As explained in Section II, the same two-stage architecture, reported in Fig. 5.9, was employed for implementing all the required amplifier circuits. As it is not possible to characterize experimentally the amplifier performance as a

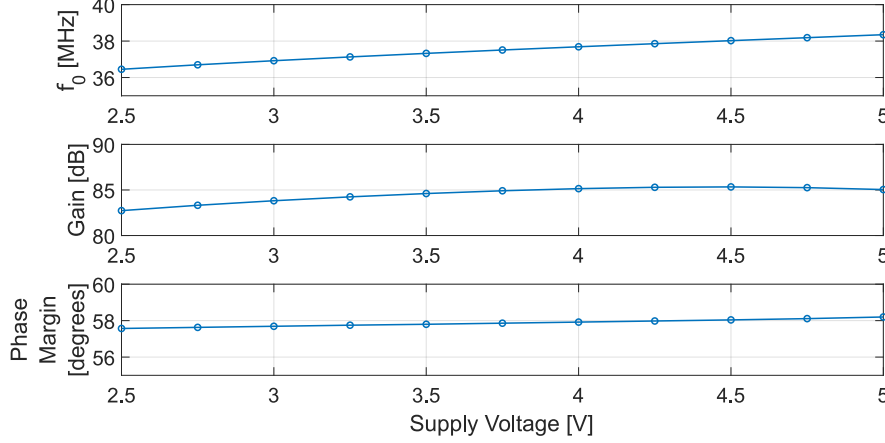


Figure 6.25: Simulated characteristics of the implemented amplifier as a function of the supply voltage, supposing typical conditions.

stand-alone block, extensive simulations were performed in the Cadence Virtuoso environment. In particular, the simulated Bode plots of the implemented amplifier circuit, obtained for different process corners and a 5-V supply voltage, are illustrated in Fig. 6.24, considering the circuit scheme and devices sizing illustrated in Fig. 5.9. As the supply voltage of the voltage balancing circuit, and therefore of the amplifiers, is the DC-DC converter voltage V_{in} , the functionality of the employed amplifier was verified for different supply voltage values, as shown by the simulation results in typical conditions reported in Fig. 6.25, which illustrates the gain-bandwidth product f_0 , the amplifier gain and its phase margin. In this way the amplifier requirements, including stability and robustness, were verified.

The functionality of the overall proposed voltage balancing architecture was verified experimentally considering different input and output voltage combinations. Measurement results of the inductor voltage, equal to the switching node voltage, and inductor current for $D > 0.5$, $D < 0.5$ and $D \simeq 0.5$ are reported in Fig. 6.26, Fig. 6.27 and Fig. 6.28, respectively, thus providing experimental verification of the proposed voltage balancing method. The spikes in the measurement results are due to parasitics determined by the measurement setup and by the bonding wires of the packaged test chip. In order to reduce the spikes, for instance, the parasitic inductance of the package can be reduced by employing ball grids instead of bonding wires. It can be seen from the reported measured waveforms that the achieved voltage balancing

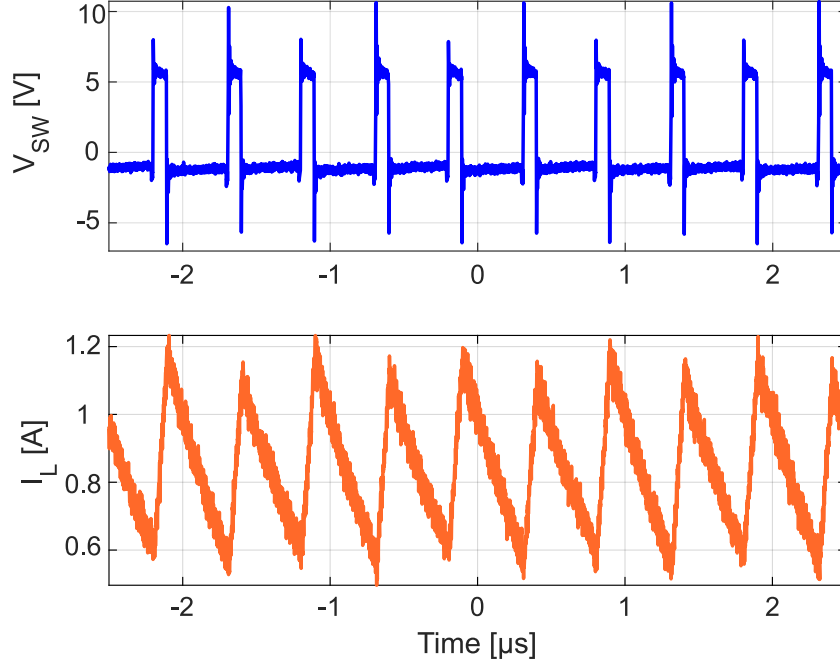


Figure 6.26: Measured waveforms with voltage balancing loop for $V_{in} = 3.3V$ and $V_o = -7.5V$ ($D > 0.5$).

is not perfect (i.e. the switching node voltage and the inductor current do not display perfect periodicity according to twice the switching frequency): this is determined by non-idealities (e.g. parasitics), which are not included in the SIMPLIS models employed in the simulations. The achieved balancing operation, however, is more than sufficient for maintaining under control the inductor current and the drain-to-source voltages of the power switches, thus allowing achieving the advantages of 3-level converters.

Table ?? summarizes the comparison between the proposed active voltage balancing strategy and other state-of-the-art balancing methods, including natural balancing [21,22], RLC balancing booster [23], direct inductor current sensing [18,25,27,29] and direct flying capacitor voltage sensing [20,26,28,30]. Natural balancing can be applied to any kind of converter, without affecting the output loop compensation; however it suffers from poor robustness as it exhibits very limited balancing dynamics and can be severely affected by parasitics. The employment of a RLC balancing booster can improve the robustness of natural balancing, but does not provide the good voltage balancing dynamics ensured by active balancing solutions such as inductor current or

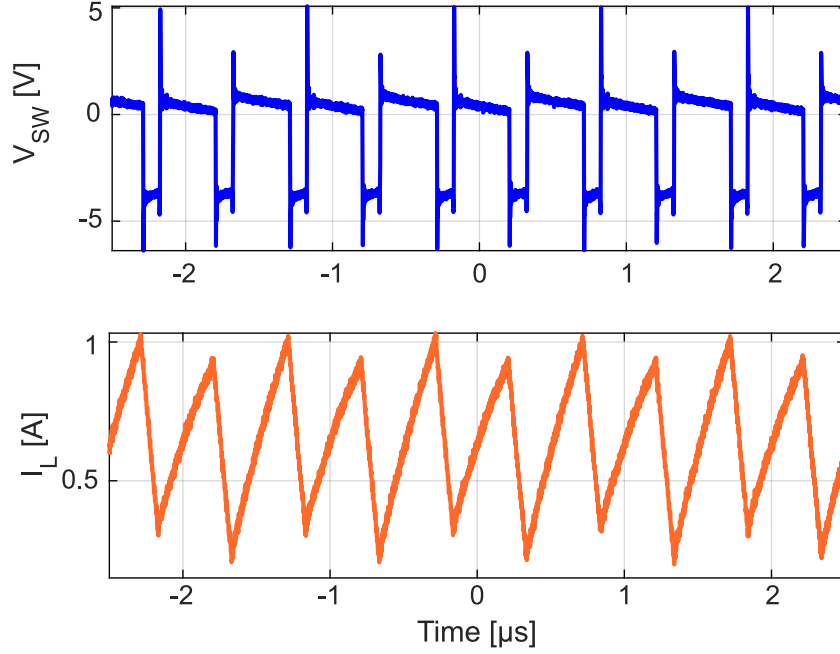


Figure 6.27: Measured waveforms with voltage balancing loop for $V_{in} = 2.7V$ and $V_o = -4V$ ($D < 0.5$).

capacitor voltage sensing. Since the flying capacitor voltage depends solely on the input voltage in the buck converter case, capacitor voltage sensing cannot be applied simply to other converter topologies, as implementing the reference voltage would not be straightforward. Voltage balancing methods based on inductor current sensing are more versatile (they can be applied to any type of converter in principle), however, since they directly impact the output voltage loop compensation, they pose limits on the implementation of the converter regulation circuit. The proposed method, instead, is robust against parasitics and exhibits good dynamics without the need for additional external components, while being highly versatile. Indeed it is easily applicable to every type of switching-mode DC-DC converter, as it solves the issue that typical active voltage balancing techniques (i.e. the ones based on direct inductor current or capacitor voltage sensing) suffer from: by monitoring the switching node there is no more need for differential amplifiers supporting a wide common mode range or for voltage references (which are not trivial to implement especially in the inverting-buck boost case). Moreover the proposed method does not impact the output voltage loop compensation: hence, it can be applied to

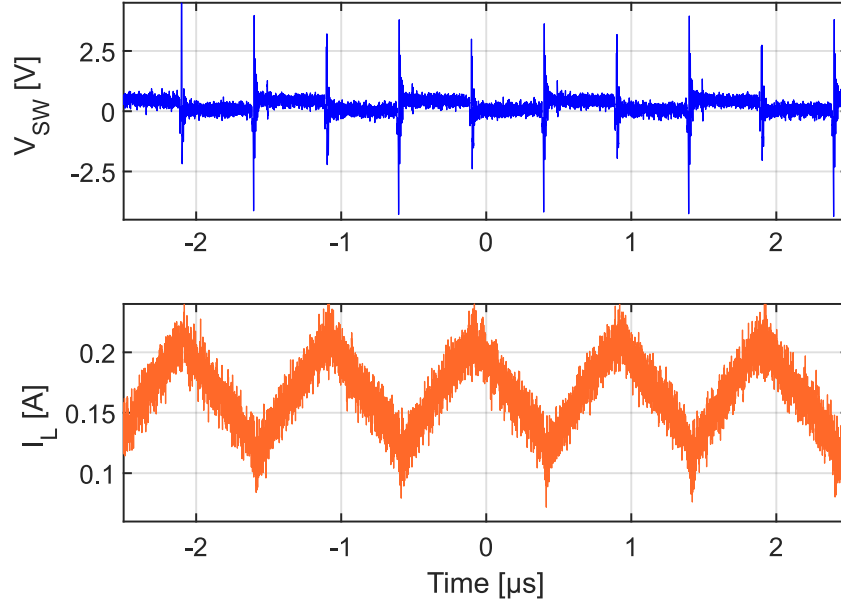


Figure 6.28: Measured waveforms with voltage balancing loop for $V_{in} = 3.3$ and $V_o = -6$ ($D \simeq 0.5$).

Table 6.13: COMPARISON TABLE BETWEEN THE PROPOSED STRATEGY AND THE STATE-OF-THE-ART

	Proposed Strategy	Natural Balancing	RLC Balancing Booster	Inductor Current Sensing	Capacitor Voltage Sensing
Robustness	++	--	+-	++	++
Versatility	++	++	++	+-	--
Additional External Components	NO	NO	YES	NO	NO
Impact on Output Loop Compensation	++	++	++	--	++

any control mode implementing duty cycle modulation. Finally in addition to being applicable to any type of 3-level switching-mode DC-DC converters, the proposed solution can be used independently from the targeted output power levels.

Conclusions

This thesis has investigated high-efficiency DC–DC conversion solutions for AMOLED display applications in mobile devices, a context characterized by stringent constraints on efficiency, silicon area, passive component count, and output voltage range. As AMOLED panels require negative bias voltages whose magnitude depends on luminance and operating conditions, the design of compact and efficient inverting converters represents a critical challenge for modern power management integrated circuits.

A systematic comparison of different converter topologies has been carried out, including inductive, switched-capacitor, and hybrid solutions. This analysis highlighted how purely inductive converters, while flexible, tend to suffer from reduced efficiency and increased area at low output power levels, whereas switched-capacitor architectures excel in compactness but are limited in terms of load regulation and scalability. Hybrid solutions combining inductors and flying capacitors emerged as an effective trade-off, enabling high efficiency over a wide operating range while keeping the number and size of passive components under control.

Among the investigated architectures, the switched-capacitor inverting buck–boost converter demonstrated particularly favorable performance for the target application. Its ability to operate efficiently at low input voltages, together with a reduced passive component count, makes it well suited for integration in mobile systems. Detailed analytical models were developed to describe its steady-state behavior, losses, and operating limits, providing valuable insight into the key design trade-offs between efficiency, switching frequency, passive sizing, and silicon area.

An optimization methodology for power switch sizing was then introduced, allowing the designer to identify optimal transistor dimensions under area constraints while maintaining high efficiency across the load range of interest. This approach proved essential to achieving competitive performance in deeply scaled technologies, where parasitic effects and switching losses play a dominant role.

The thesis further addressed one of the main challenges of multi-level and flying-capacitor converters, namely capacitor voltage balancing. A dedicated control strategy was proposed and analyzed, ensuring robust voltage regulation without the need for additional sensing circuitry or excessive control complexity. Simulation results confirmed that the proposed control scheme effectively maintains capacitor voltage balance under different operating conditions and load variations.

Finally, a comprehensive comparison among the considered topologies was presented, highlighting the advantages of the selected solution in terms of efficiency, area occupation, and passive component requirements. The results demonstrate that the chosen architecture represents a strong candidate for next-generation AMOLED power supplies, combining high performance with practical implementability.

Overall, this work provides a structured design framework for inverting DC–DC converters in low-power applications, from topology selection and analytical modeling to optimization and control. The methodologies and insights developed throughout the thesis can be readily extended to other power management scenarios where efficiency, compactness, and integration are of primary importance.

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