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Imaging Probe for Charged Particle Detection Based on SPAD Sensors

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Introduction

Single Photon Avalanche Diodes, or SPADs, are semiconductor devices that are capable of detecting individual photons. They operate on the principle of avalanche multiplication, where a small amount of light generates a large output signal by triggering a cascade of charge carriers. They are commonly found in array architectures integrated within the same substrate.
SPADs have numerous applications in various fields, including photon counting, fluorescence spectroscopy, quantum optics, and LIDAR sensing offering high sensitivity and time resolution. However, in SPADs an avalanche current can be triggered even when no photons are present, due to random generation of carriers in the depleted region of the detector. This phenomenon, known as dark count rate (DCR), can limit their sensitivity and photon detection efficiency (PDE).
Characterizing SPADs is important because it allows researchers and engineers to understand their behavior in different conditions, which can then be used by the designers to improve and optimize their performance, thus making them more effective in various applications.
The research work presented in this thesis was conducted as part of the APIX2/ASAP project funded by the Italian Institute for Nuclear Physics (INFN). The project aimed to develop a new type of position-sensitive sensor for charged particle detection based on vertically integrated SPAD arrays, with the goal of reducing noise. Among the chips developed, the APIX2LF consists of arrays of SPADs produced using a 150 nm standard CMOS process, with each SPAD having its front-end electronics. Both single- and dual-layer chips can be characterized separately. It is important to note that prolonged exposure to different sources of radiation can lead to device damage, potentially reducing their lifespan and sensitivity, and therefore appropriate investigation and modeling should be carried out to ensure their reliable operation in harsh environments.
This dissertation describes the development of a portable detection probe using the APIX2LF chip and a microcontroller as the interface between the sensor and the computer. Custom firmware for the microcontroller and frameworks on the computer side were developed to perform characterization and radioac-

tive source measurements in different environmental conditions. To understand the behavior of the DCR under different conditions, characterizations were carried out using six APIX2LF chips at different bias voltages and temperatures. A prototype board was designed, and tests with a beta-emitting source were performed with one dual-layer APIX2LF chip.
The first chapter provides a description of the SPAD device, including its operating principle, structure, and key performance parameters. It specifically focuses on the APIX2LF chip, discussing its features and characteristics in detail. The last part of the chapter describes the previous setup used within the research group for the first measurements performed on the APIX2LF chip.
The second chapter outlines the design of the portable detection probe, with a particular focus on the components used. A microcontroller was employed to act as the interface between the sensor and the computer. The firmware developed for characterization is also discussed in detail, as well as two different data acquisition frameworks developed for the PC.
Chapter 3 presents the results of the characterization performed on four single-layer and two dual-layer APIX2LF chips. The breakdown voltage was determined for each chip at various temperatures, and the effect of bias voltage and temperature was studied. Specific measurements were conducted to evaluate the crosstalk impact and extract information about Random Telegraph Signal (RTS), which may occur in SPAD DCR.
Finally, Chapter 4 covers the measurements of the imaging probe, which uses a custom miniaturized carrier designed to house a dual-layer APIX2LF chip. The chapter includes the characterization, in terms of breakdown voltage and DCR, of the specific chip used in the probe. Additionally, the functionality of the chip as a charged particle detector was tested using a beta-emitting source.

Chapter 1

Single photon avalanche diodes: Geiger-mode operation and charged particle detection applications

The single photon avalanche diode (SPAD) is a detector with very high sensitivity, high efficiency, and extremely fast response. It is based on a reversed biased p-n junction and can detect light from near ultraviolet to near-infrared. SPADs operate at a reverse bias voltage (V_{Bias}) above the breakdown voltage (V_{BD}) called Geiger mode, which is why they are also known as G-APD, or GM-APD (Geiger-mode avalanche photodiode). The Geiger mode operation guarantees the avalanche diode a high gain, making possible single photon detection hence the name of the device.
The excellent features made the SPAD the basic element of devices such as the Silicon Photomultiplier (SiPM) which has become an attractive alternative to photo-multiplier tubes (PMTs) replacing them in many applications, on account of the intrinsic advantages of being more compact, and insensitive to magnetic fields.
SPADs are found integrated into a common substrate in array architectures with hundreds, even thousands of elements, referred to as pixels. The progress of silicon technology has enabled the development of arrays of Geiger-mode p-n junctions based on full custom or standard CMOS processes. Two types of SPAD structures can be distinguished based on the interconnection between SPADs inside the array: analog-SiPM, where the SPADs are connected in parallel, and digital SiPM, where each SPAD is read out and digitized by its own electronic channel before the signals are combined to provide information about the number of hit cells. Arrays of SPAD with digital readout can also

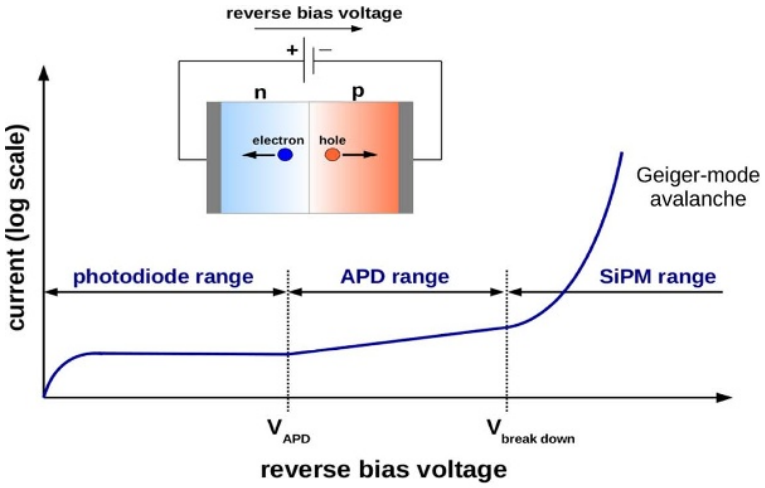
be used as position sensitive detectors.
The first section of this chapter reviews the physical principle of SPAD detection and its main electrical parameters and provides a brief overview of the figures of merit. The second part focuses on the chip developed as part of the APIX2/ASAP project giving a detailed insight into the SPAD array characteristics.

1.1 The SPAD

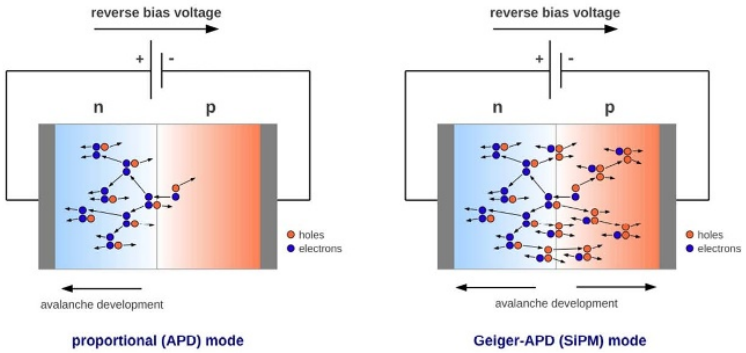
As already mentioned, the SPAD is the elementary micro-cell of an array architecture integrated into a common substrate that forms a photodetector or a radiation detector. This section includes a description of the physical mechanism that leads to photodetection, of the technology used for array fabrication, of the quenching techniques and front-end circuits, and, finally, of SPAD figures of merit.

1.1.1 Geiger-mode operation

The SPAD consists of a p-n junction (a diode) specifically designed to be biased in the reverse mode above the breakdown voltage [1], [2]. This photodetector operates in three different regions depending on the applied voltage. Referring to Figure 1.1a, when the voltage is lower than V_{APD}, the diode works in the photodiode region: an impinging photon can create one electron-hole pair which is separated by the applied field and a current proportional to the light intensity can be measured.
Under the effect of the electric field at the junction, an electron (or a hole) can reach sufficiently high energy to generate new electron-hole pairs by colliding with lattice atoms. Hence, when the applied reverse voltage is increased, in the APD regime, the electric field becomes so high that the electrons can create secondary e-h pairs through impact ionization (Figure 1.1b). In this regime, the gain ranges from tens to hundreds and the measured current is proportional to the number of detected photons or of generated primary e-h pairs. Because holes have a larger effective mass, in this regime, only electrons can generate secondary e-h pairs, and therefore the avalanche is self-quenched. If the applied reverse voltage is further increased to the extent of exceeding the breakdown voltage, also holes become capable to generate secondary e-h pairs (Figure 1.1b). In such operating conditions, the electric field in the depleted region gets larger than $\sim 3 \times 10^5\ V/cm$ and the diode reaches the Geiger-mode condition, where a single injected carrier can trigger a self-sustaining avalanche process resulting in exponential growth of the current. The avalanche can be quenched employing a quenching circuit, which is used to lower the bias voltage below the breakdown voltage. During this process, which may take a



(a)



(b)

Figure 1.1. (a) Operation regimes in a reverse biased solid state p-n junction. (b) In the APD only electrons can sustain the avalanche, whereas in Geiger mode both electrons and holes can generate secondary e-h pairs through impact ionization [3], [4].

relatively long time (tens of nanoseconds), the detector is not sensitive to any other particles. The bias voltage must return above the breakdown voltage to be able to detect another photon.
Due to reverse biasing, the generated electrons always flow in the direction of the n-doped region. The chances that an electron or a hole passing the p-n junction generates enough secondary e-h pairs to trigger a self-sustainable avalanche define the avalanche-triggering probability. This parameter depends

on the SPAD structure, the electric field, and the type of carrier because electrons have a higher triggering probability than holes. Therefore, the avalanche triggered by electrons is preferred to increase the photon detection efficiency (PDE) [3].
Two types of SPAD structures can be distinguished, described in the following [5].

- A p+/n-junction, built in a lightly doped n-type epitaxial layer grown on an n+ type silicon substrate. Such a structure is optimized for blue light detection because photons are absorbed closer to the surface of the SPAD which will traverse the junction towards the n-doped region connected to the positive pole of the bias voltage.

- An n+/p-junction, built in a lightly doped p-type epitaxial layer grown on a p+ type silicon substrate. Such a structure is optimized for red light detection, because photons will generate e-h pairs deeper in the SPAD, away from the surface. Electrons are collected quickly crossing less material, lowering the chance of avalanche triggering. On the other side, the holes crossing the SPAD in the opposite direction, have a smaller avalanche-triggering probability. This leads to a lower overall PDE as compared to photon detection in the blue spectral range.

1.1.2 Equivalent circuit

Figure 1.2a shows the electrical circuit model introduced by Haitz to simulate the behavior of micro-plasma instabilities in silicon [6]. The micro-cell is represented by the SPAD connected in series with the quenching resistance R_Q. The fabrication of R_Q in the same substrate as the diode can determine a parasitic capacitance in parallel, represented by C_Q. The diode is modeled by its diode junction capacitance C_D and its series resistance R_D. In general $R_Q \gg R_D$. There are three fundamental operation modes in a SPAD: quiescent mode, discharge phase, and recovery phase (Figure 1.2b).
In quiescent mode, the diode is reversely biased to $V_{Bias} = V_{BD} + V_{OV}$, where V_{OV} is the overvoltage, i.e., the excess voltage beyond V_{BD}. A voltage source V_{BD} simulates the breakdown voltage. The switch S is open unless a photon is absorbed and, if leakage currents are neglected, the diode remains in this condition. When a photon is absorbed or if a dark event occurs, the switch closes, and a very short current spike is generated through the SPAD. The diode capacitance C_D is discharged from V_{Bias} to V_{BD} through R_D with a time constant $R_D \times (C_D + C_Q)$ (neglecting the influence of R_Q which is usually highly resistive). During this phase, the avalanche multiplication is ongoing inside the diode. Once triggered, the avalanche process is self-sustained, implying that a steady current could flow indefinitely in the device if no quenching is

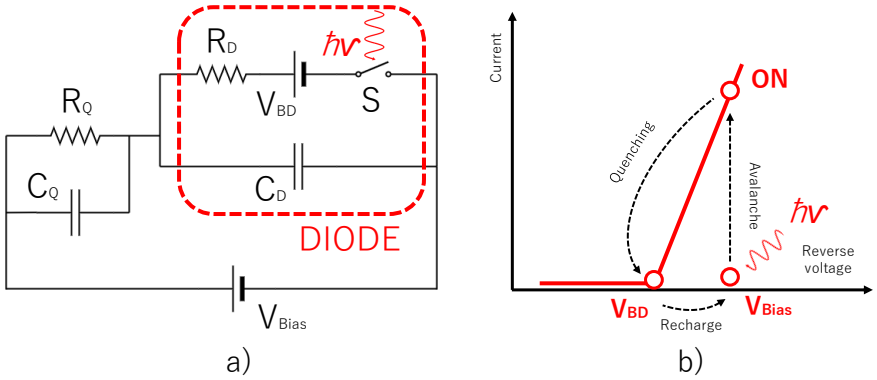


Figure 1.2. (a) Equivalent electrical circuit of the SPAD with integrated quenching resistor based on Haitz model of a GM-APD [6]. (b) SPAD operating modes.

added. With the quenching resistance R_Q, the avalanche process is quenched and the switch S opens again. The SPAD enters in the recovery phase: C_D recharges back to V_{Bias} through R_Q with a time constant $R_Q \times (C_D + C_Q)$. The SPAD returns in the quiescent mode, ready for new detection.
The avalanche can be sensed using a comparator, or even a simple inverter. Considering the limitations in terms of dead time, brought about by the requirement of a quenching circuit, single photon counting can be performed, by exploiting the fast response of a following readout circuit. Induced latch-up events limit the choice of voltages applied to the circuit [7]. Due to a bias voltage exceeding the maximum levels supported by the gate oxide, permanent damage can be caused to the subsequent logic gates. This issue can be avoided using clamping diodes or AC coupling.

1.1.3 Quenching circuits

During the avalanche phase, the generation of e-h pairs leads to a quickly rising current flowing through the diode. To avoid permanent damage to the avalanche device and to improve its time resolution, a quenching circuit is required. Thanks to the quenching circuit, the avalanche is suppressed and the SPAD is restored to its quiescent state so that it is able to detect other particles. The time that is needed to quench the avalanche is called quenching time, whereas the time it takes to bring the SPAD back to the OFF state is called reset time (Figure 1.2b). These times are critical from the time resolution point of view: the rising time of the current is in the range of ps while quenching and reset times are in the range of ns. They also affect SPAD power dissipation and dark count rate. The proper value of R_Q is crucial to let the

internal diode current I_D decrease below a level where even statistical fluctuations may quench the avalanche. However, an excessively high R_Q may lead to a very long dead time, during which the detector is not available to detect photons leading to a reduction in the detector sensitivity [5]. Therefore, it is essential to optimize the quenching circuit. There are two main categories of quenching circuits: passive quenching circuits (PQCs) and active quenching circuits (AQCs). Based on the application, the choice is made as a tradeoff between area occupation, cost, and performance.

Passive Quenching Circuit

The Passive Quenching Circuit represents the simplest way to quench the SPAD. It consists of a high-value resistor R_Q, or a triode-biased transistor, in series to the photodiode. The output of the SPAD is read through a comparator, one or a couple of inverters acting as a digital buffer powered between 0 and V_{DD}. When the reverse voltage applied to the diode is a positive voltage on the cathode and a negative voltage to the anode (with respect to ground) a PMOS can be used to quench the avalanche (Figure 1.3a). On the other hand, when a positive voltage is applied to the cathode, an NMOS can be used to perform the quenching operation (Figure 1.3b). Both solutions have been discussed in the literature [8] [9], [10], [11], [12], as they feature different characteristics. In both configurations, several parasitic capacitances that must be charged and discharged are involved thus deteriorating in different ways the timing performance of the detector, increasing the power consumption and the afterpulsing probability, i.e., a pulse generated by a carrier released after

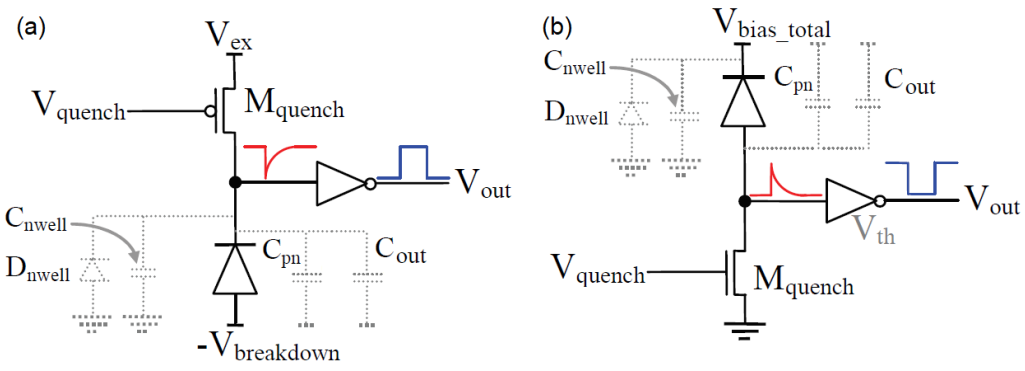


Figure 1.3. Two passive quenching circuits, providing a correct bias to SPADs, with different approaches: (a) PMOS approach, (b) NMOS approach.

a certain time after being trapped inside a silicon defect (see section 1.1.5). Because the output node in (b) has less capacitance than in (a), and the mobility of an NMOS channel transistor is higher than a PMOS, solution (b) is to be preferred. This solution may also be advantageous in terms of area and, since the n-well region can be shared by multiple elements, may result in an easier array arrangement and improved fill factor (see section 1.1.5).

Active Quenching Circuit

A more effective solution for quenching is the Active Quenching Circuit which was introduced to overcome the disadvantages of the PQC in terms of dead time. In this case, it is possible to control and change the voltage across the detector once an avalanche is detected by the readout circuit through active feedback networks. By controlling the bias voltage, it is possible to let the sensor operate below the breakdown voltage for a defined time (hold-off time) minimizing afterpulsing phenomena. The quenching is less sensitive to the statistical fluctuations of the output signal due to the avalanche multiplication process. The reset phase is also performed by active devices that provide a fast reset time improving the maximum counting rate. An example of AQC is shown in Figure 1.4, where the feedback network consists of MOS transistors acting as fast switches. When an event occurs triggering an avalanche, the current flows through the network. The quenching operation is started by the NMOS transistor which acts in the same way as in the PQC. As soon as the feedback network is turned on, the control logic senses the current and starts the active quenching turning on the PMOS transistor. Once the PMOS is on, the anode of the SPAD is at the V_{DD} level, lowering the biasing voltage of the diode below its breakdown voltage. The excess voltage applied to the SPAD must not go beyond the V_{DD} range, otherwise, it wouldn't be possible to quench the diode. The SPAD is kept off for a programmed time interval and then restored to its ready-for-detection condition. This way, the afterpulsing phenomenon is drastically reduced. The bias voltage is eventually brought back to its starting value by the feedback NMOS transistor during a short reset process. Active quenching circuits offer fast and fixed quenching times, reduced reset times, and the chance of keeping the SPAD voltage below the breakdown voltage for a programmable period. This results in greater complexity and larger area occupation, which reduces the overall fill factor in the case of an array architecture.

In summary, PQC offers a simpler and more compact area solution with benefits also in terms of costs. On the other hand, AQC is the solution to be preferred when the timing resolution is the main requirement.

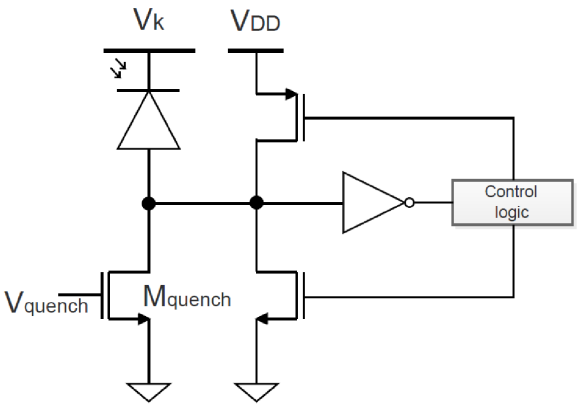


Figure 1.4. Basic schematic of an AQC implemented by using quenching NMOS transistor and fast feedback switches.

1.1.4 SPADs in CMOS technology

Although SPAD devices were initially fabricated using dedicated processes, it was immediately clear that they could benefit from CMOS fabrication process maturity to improve some of their performance and features. CMOS technology in particular enables the fabrication of readout and quenching circuits in the same substrate as the sensor, thus reducing capacitance between them, and allowing on-chip signal processing and analog-to-digital conversion. Moreover, it provides a higher yield and a reduced cost compared to dedicated processes. There are three main categories of manufacturing processes [7]:

- *CMOS compatible processes* - fully custom processes optimized to produce the best possible single detector element. These processes are not suitable for array fabrication and are not compatible with very large-scale integration. Their typical features are low implant doping concentrations, minimum lattice damage through annealing and slow diffusion steps, DCR and crosstalk improvements thanks to dedicated gettering phases.

- *High voltage CMOS processes* - developed thanks to the rising request of integrated circuits for control electronics (actuators, sensors, etc.), which have several common requirements with SPADs, such as lowly doped diffusions, limitation of contaminants, high-quality material. A high voltage feature is possible due to the availability of a relatively low doping deep n-well. The scale of integration is limited, but dense array arrangement and integration of both circuit and sensing element in the same chip are possible.

- *Standard CMOS processes* - the best choice if very large scale of integration, low cost, high yield, and dense array structures are required. However, there are a lot of design rule restrictions, and low PDE (due to the small active area and non-optimized optical stack). Additionally, in advanced CMOS technologies, the breakdown voltage tends to be smaller due to increased doping levels that lead to a strong increase of the DCR caused by tunneling processes.

In terms of fabrication details, SPADs in CMOS technology can be subdivided according to the formation of the guard ring, the overall shape of the detector, the active area diameter, or the diode junction itself.

1.1.5 Definition of SPAD figures of merit

This section contains a brief overview of the main performance parameters of SPADs, valid both for stand-alone and CMOS-integrated SPAD devices.

Photon detection efficiency (PDE)
This parameter specifies the probability that a photon arriving on the sensor surface is detected, producing an output pulse. It can be defined as the ratio between the number of detected photons over the number of incoming ones. Since the penetration depth is wavelength dependent, the PDE also depends on the wavelength of the impinging light.

Afterpulsing probability
Some silicon defects can act as a trap for charge carriers created during the avalanche. These trapped carriers are kept for some time but their subsequent release can trigger a new avalanche. The afterpulsing probability depends mainly on the defect density. Detection pulses, generated by afterpulsing phenomena, can be prevented from reaching the output of the readout chain by controlling the time between quenching and recharging of the SPAD.

SPAD dead time
The time between the avalanche triggering and the reset phase is called dead time and it depends mostly on the quenching circuit. During this time interval, the SPAD cannot detect other photons, thus resulting in a limitation on the maximum photon rate that can be detected. However, a large dead time is desirable to minimize afterpulsing effects. Therefore, a tradeoff is needed.

Dark Count Rate (DCR)
Even in complete darkness, several mechanisms can trigger avalanche events produced by non-photon-generated carriers. It is not possible to distinguish between a dark pulse and a real detected photon or particle, so DCR must

be minimized. Multiple causes may produce dark counts: thermally excited charge carriers, diffusion of carriers from the neutral region into the high-field region, carrier generation at defects (contamination, lattice dislocations), and band-to-band tunneling in regions of very high electric fields. Various parameters affect the overall DCR: excess voltage, temperature, active area, technology, and fabrication process. Possible DCR mitigation methods include processing in a contamination-free environment, high annealing temperature, doping concentration not excessively high, and low defect wafer material.

Timing Jitter
Statistical fluctuations define the time interval between the photon arrival and the produced output pulse. In addition to timing jitter originating from the detection electronics, also the specific position in the multiplication region where the avalanche starts to develop affects the dynamics and timing behavior of the avalanche process [13]. Another contribution comes from the diffusion time of charge carriers created outside the multiplication region.

Homogeneity of DCR distribution of SPADs in an array
All SPADs cells in an array should preferably have very similar parameters. But there is always a fraction of SPADs that have significantly higher DCRs than the others due to local defects. Once these pixels are identified, they can be disabled with benefits in terms of the global DCR.

Crosstalk
The avalanche triggered in one SPAD can lead to charge carriers that reach the multiplication region of a neighboring SPAD and there they trigger an avalanche, resulting in electrical crosstalk. In the case of optical crosstalk, high-energy charge carriers during the avalanche can generate secondary photons that can be detected by neighboring cells.

Fill Factor (FF)
Each microcell in a SPAD array contains some area that is not optically sensitive due to minimum distance rules required by the process, guard rings, or electronics included in the pixel. The FF is defined as the ratio of the optically active area and the total pixel area.

1.2 SPADs in charged particle detection applications

SPADs are good candidates for use in photon detection applications such as optical ranging, positron emission tomography, fluorescence lifetime imaging,

and Raman spectroscopy [14],[15],[16],[17], but also in the field of charged particles tracking [18] thanks to the high internal gain and timing resolution, and the potential for dense integration. Although charged particles do not behave like photons, which are absorbed inside the active area of the SPAD, their effect is similar, as they can generate one or more electron-hole pairs which may produce an avalanche. The development of position-sensitive detectors for charged particle tracking systems is quite challenging and finds wide interest in applications involving High Energy Physics (HEP) experiments as well as in Nuclear Medicine applications. The specific requirements, such as position accuracy, granularity, power consumption, radiation hardness, low material budget, or integration ease, may vary based on the kind of application where they are employed.

1.2.1 The APIX2/ASAP project

Part of this thesis concerns the characterization of SPAD arrays fabricated in 150 nm CMOS standard technology that can be employed as charged particle position-sensitive detectors. This section will describe the project APiX2/ASAP, funded by Istituto Nazionale di Fisica Nucleare (INFN) that also involves the University of Pavia, University of Trento, Trento Institute for Fundamental Physics and Applications (TIFPA), University of Siena and the University of Padova. The main goal of the project was the development of a new generation of layered avalanche detectors for charged particles, pursuing improved efficiency, reduced noise, and low material budget. Three test chips were developed within the project, called APIXFAB0 [18] [19], APIX prototype-I [20], [21], and APiX2LF [22]. APIXFAB0, a single-layer device, was fabricated in a 180 nm CMOS technology with HV option, whose purpose was to study the technology features for the development of SPAD devices. The APIX prototype-I chip was fabricated in 150 nm CMOS standard technology and was also used for the production of the first-ever dual-layer SPAD arrays.
The APIX2LF chip goal is to evaluate the technology features and to prove the feasibility of a moderately large dual-layer sensor with a coincidence-based approach. The APiX2LF position-sensitive detector is based on the vertical connection of two layers of 150 nm CMOS SPAD arrays. The sensing elements are paired face to face building up a basic cell that can produce a coincidence signal when a charged particle strikes two overlapping pixels at the same time. The two layers are fabricated separately on different chips and afterward vertically interconnected through micro bump bonding techniques that guarantee a yield of 100% at a pitch of 50 µm [21]. Each chip is 150 µm thick. Standard CMOS technology was chosen because it represents one of the best solutions when arrays with a high pixel density must be fabricated. It also offers bene-

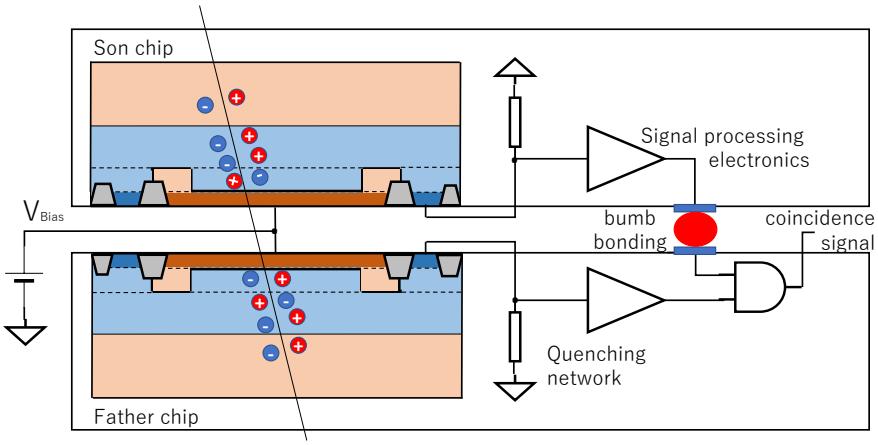


Figure 1.5. Cross-section of two overlapped SPADs, forming a single cell of the APiX2LF detector, crossed by a charged particle.

fits in terms of overall cost reduction while obtaining a high yield, increasing chip robustness, and reducing system complexity.
Every single SPAD has its own readout electronics and quenching circuit. The coincidence signal of two overlapping SPADs, which represent the single detector cell, is produced by an AND gate, that is located only in the bottom chip, as shown in Figure 1.5. Except for the AND gates, the two layers are the same, one being the mirrored version of the other to obtain matching between the corresponding SPAD in the two layers. The bottom chip is called the *FATHER* chip, while the top one, bonded onto the FATHER, is called the *SON* chip (Figure 1.5). Both FATHER and SON chips can be characterized separately since individual versions were fabricated and packaged as standalone structures.

1.2.2 Advantages of a dual layer SPAD structure

The advantages of a dual-layer SPAD structure are mainly related to the device's noise performance. Given that it is not possible to distinguish a source-generated signal from a spurious one, it is possible to leverage the timing difference between them to discard dark count events. The concept behind the dual-layer sensor is exactly this: since it is very unlikely to have two dark count events taking place simultaneously in two overlapped pixels, the effect of DCR on the detection is strongly reduced compared to a single-layer detector. The DCR of the dual layer pixel can be expressed as [21]:

$$DCR_C = 2\Delta t \times DCR_T \times DCR_B, \tag{1.1}$$

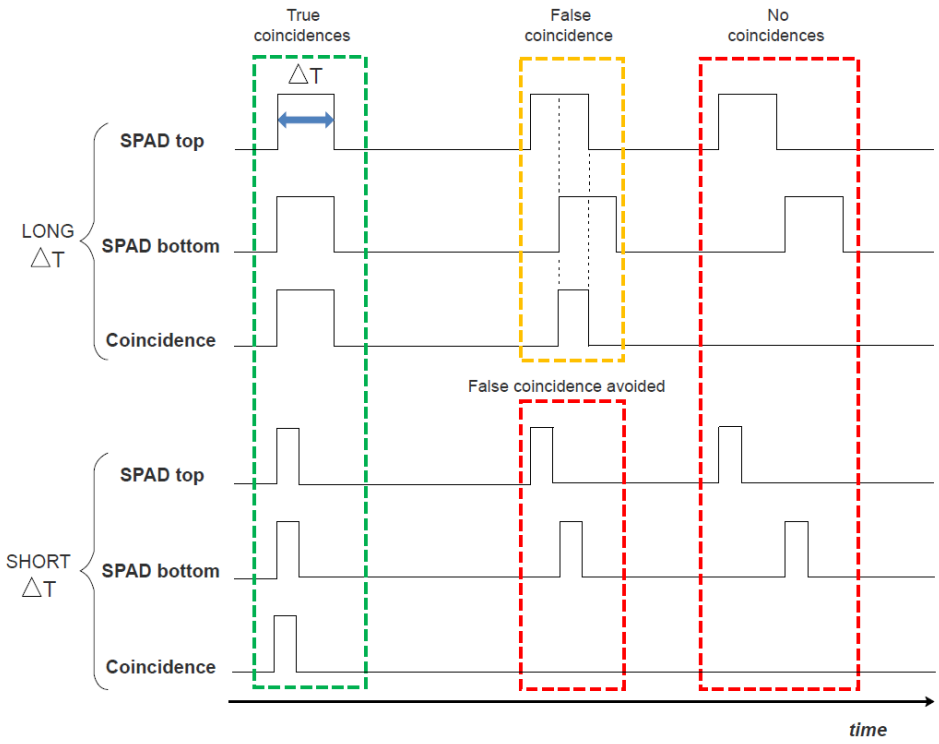


Figure 1.6. Coincidence detection for different Δt duration [19].

where Δt represents the coincidence time window, DCR_T the dark count rate of the top SPAD and DCR_B the dark count rate of the bottom SPAD. If DCR_T and DCR_B are in the order of 1 kHz and Δt in the order of 1 ns, which are reasonable values for SPADs fabricated in a 150 nm CMOS standard technology, from (1.1) the consequent DCR reduction is more than 5 orders of magnitude. The time diagrams of Figure 1.6 show that when a particle passes at the same time through the two aligned detectors, a true event is sensed by the electronics, regardless of the coincidence window duration Δt. The probability of having random coincidence signals due to concurrent dark count events in two overlapping SPADs is decreased by reducing Δt. If the coincidence time window is large, dark pulses coming from the two pixels may overlap for a small fraction of time, producing a false coincidence signal. Therefore, small values of Δt are highly desirable to minimize DCR, but the lower limit is set by the time jitter of the detector response (tens of ps) and by the signal coming from the SON chip, whose rise and fall times may be degraded by the parasitic capacitance associated with the bump connection.

1.3 APIX2LF chip

The APIX2LF bottom (FATHER) and top (SON) chips were fabricated in a standard 150 nm CMOS technology [19]. The dice dimensions are 6 mm x 5 mm for the FATHER chip and 5.4 mm x 5 mm for the SON chip. Compared to the previously developed chip (APIXFAB0, manufactured in 180 nm CMOS technology) [18], the APIX2LF chip features SPAD arrays with a larger area, a different number of cells and a larger variety of readout circuits, including passive and active quenching networks and integrated 10 bit counters. The APIX2LF is designed so that two single-layer chips can be vertically connected employing bump bonding techniques, to obtain a dual-tier structure. The obtained position-sensitive detector provides an output signal that is the result of the logic AND operation performed on the two signals coming from the SPADs in the top and bottom layers. Since simultaneous dark pulses are highly unlikely, the reduction of the dark count rate is significant if compared to the single-layer instance. After the bump bonding is completed, the power supply, the reference voltages, and all the input signals are applied to the FATHER chip, which delivers them to the SON chip through the bump bonding contacts. The output signals are also made available only on the FATHER pins to be read out.
Considering that the layout of the FATHER and SON chips are practically the same, the internal structure of the SPAD arrays is equivalent. Although the following description will refer to the FATHER chip, the same description applies also to the SON chip.

1.3.1 Chip architecture

The APIX2LF detector contains four arrays of SPADs with different areas and signal storage circuits. To get as broad a picture as possible of SPAD performances, several different structures, aiming at different tasks, were developed within the four arrays. Figure 1.7 shows the arrays contained in a single-layer SON chip. The arrays and their characteristics are listed below:

- array 1: 48 (rows) × 48 (columns) pixels, with a pitch of 75 µm, 1-bit memory architecture, fill factor 66% (SPAD active area of $70 \times 52\ \mu m^2$);
- array 2: 48 × 12 pixels, with a pitch of 75 µm, a 10-bit ripple counter architecture, fill factor 44% (SPAD active area of $47 \times 57\ \mu m^2$);
- array 3: 24 × 72 pixels, with a pitch of 50 µm, a 1-bit memory architecture, fill factor 39% (SPAD active area of $44 \times 24\ \mu m^2$);
- array 4: 15 × 11 pixels, with a pitch of 75 µm, used for test purposes: 42 pixels are provided with active quenching circuits, 75 pixels have been

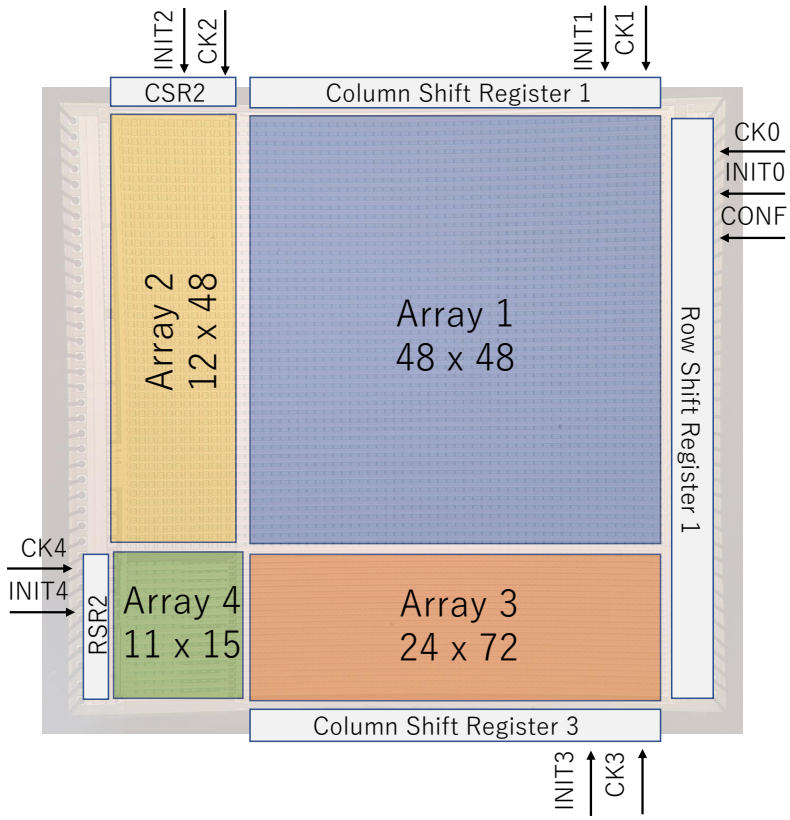


Figure 1.7. Array partition and corresponding shift registers around the sensing arrays.

fabricated with an active area dimension equal to the one used for the SPADs of array 3, 24 pixels have been manufactured following different process splitting, 24 pixels are read out by a front-end electronics with optimized timing.

The SPAD cathode voltages (the diode polarization is of the type shown in Figure 1.3 (b)) are provided independently to each sub-array to measure only one array minimizing electrical crosstalk between different arrays. Every array biasing comes from different lines through different pins of a specially designed printed circuit board (PCB) (see section 1.4). The most severe requirement during the design was the optimization of the fill factor [19].
Each SPAD is built as a p+/n-well junction, with an active volume less than $2\,\mu m$ thick, isolated by a deep n-well from the substrate (Figure 1.8). The chip die can be thinned down to a few microns without deteriorating the sensor functionality [20]. A lowly doped ring surrounding the active area blocks the n-well at the border of the junction to avoid premature edge breakdown acting

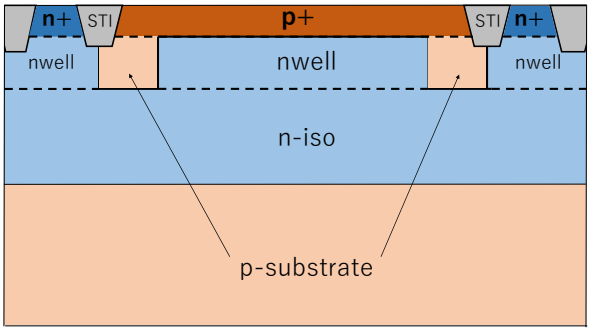


Figure 1.8. Cross section of the sensor used in the chip.

as a guard ring [23].
To characterize a specific SPAD of the arrays, the corresponding cell has to be selected and enabled. This operation is achieved by some shift registers, distributed around the arrays as shown in Figure 1.7. Shift registers are divided into Row Shift Register (RSR) and Column Shift Register (CSR), addressing each SPAD row and column. The corresponding RSR and CSR relevant to each array can be deduced from Figure 1.7. Because some of the arrays have the same pitch, a few shift registers are shared between compatible arrays, while others are specific just for a particular array.
A cell is selected when the shift registers outputs corresponding to the relevant row and column are set to logic 0 while all the other outputs are set to 1. Each shift register has two input signals coming from the input pads: the INIT (initialize) and the CK (clock) signals (INITx and CKx, with x= 0, 1, 2, 3, 4). The INIT signal resets the shift registers, setting the output of the first flip-flop to 0 (the selection signal is active low), and all the other flip-flop output nodes to 1. After the INIT 0 to 1 transition, the first row or column of the array is selected. A CK signal pulse is necessary to proceed to the next row or column, moving the selecting '0'. To select the cell in the row r and column c, one must deliver $r-1$ clock pulses to the row shift register and $c-1$ clock pulses to the column shift register.
Of all the row shift registers, only RSR1 implements an additional feature that allows a parallel selection and enabling of the cells of arrays 1 and 3. This is achieved by acting on the CONF initialization signal. When CONF is set to 1 and the rising edge of the INIT signal arrives, one flip-flop every eight FFs of the row shift register is set to zero (Figure 1.9). Once the pixel has been selected, an enable signal (EN) must be sent, so that when the SPAD is hit, it can produce a current and the electronics can detect it. This enabling operation is completed by the circuit shown in Figure 1.10 that consists of some logic gates, and a negative edge-triggered Set-Reset latch.
The ENRB signal (active low), coming from the input pads, acts on the reset

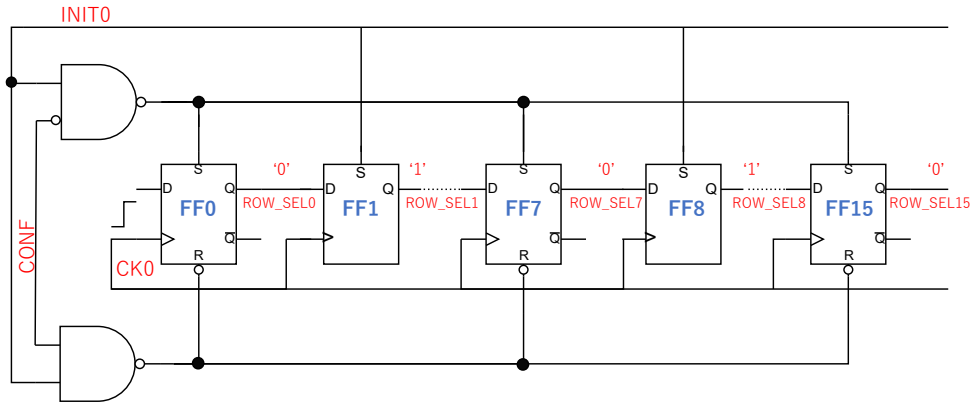


Figure 1.9. Flip-flops of the Row Shift Register 1 with the CONF signal.

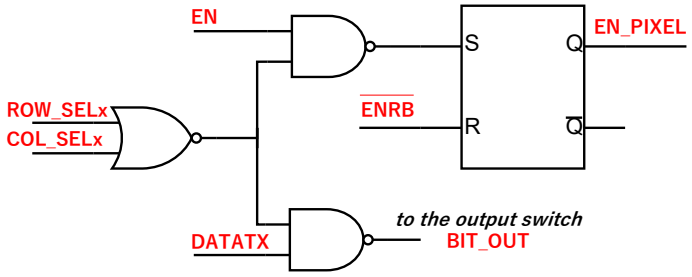


Figure 1.10. Pixel selection and enable circuit.

of the latch to disable the cell. It is a global signal thus once it is activated all the cells are disabled causing all the SPADs to switch off.
Considering that the characterization measurements that will be discussed in this thesis are relevant to array 1 and array 3, in the following subsection, a detailed description of only these two arrays will be provided. For an extensive description of the other matrices, see [19], [24].

1.3.2 Array of SPADs with single bit memory

Arrays 1 and 3 both share the same cell architecture referred to as fast architecture because it has been designed to allow parallel pixel readout up to 100 MHz. Figure 1.11 shows the block diagram of the 1-bit fast readout circuit for arrays 1 and 3 of a FATHER chip, with details at the transistor level. All the transistors are core devices ($V_{DD} = 1.8\,V$), except for the NMOS transistor that performs the quenching operation (passive quenching), and the one used to adapt, or clamp, the level of the anode voltage to the range of the digital buffer, that have thicker oxide ($V_{DD} = 3.3\,V$). The circuit at the top of Figure 1.11 processes the SPAD output pulse, while the circuit at the bottom of the

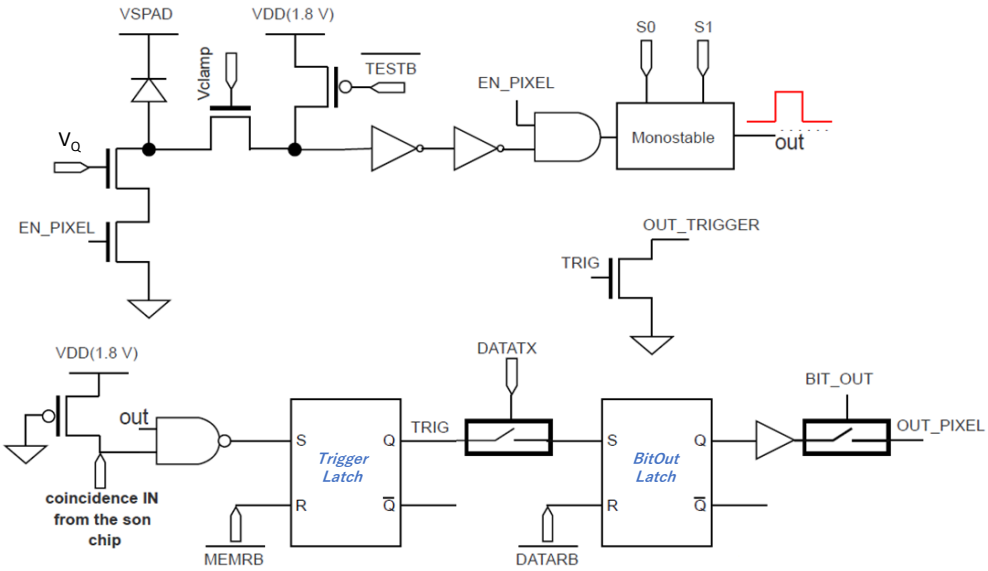


Figure 1.11. Block diagram of the 1-bit fast readout, used in arrays 1 and 3 of the FATHER chip.

figure produces the coincidence signal of the two layers that will be stored inside two dedicated latches. The EN signal drives an NMOS transistor in series with the quenching current source, which prevents the current from flowing if it is disabled by the network of Figure 1.10. To test the functionality of the readout electronics only, a pull-up PMOS transistor driven by the TESTB signal (active low, set by the user) was added. This signal emulates a SPAD firing event by raising the input node of the buffer that delivers the signal to the monostable circuit. The buffer consists of custom-designed inverters with a threshold voltage slightly larger than $V_{DD}/2$. The monostable acts on the input pulse duration: changing two input bits, S0 and S1 (set by the user), four different pulse duration can be chosen as shown in Table 1.1. The duration Δt of the output pulse affects the overall DCR of the dual-layer chip as per (1.1).
A NAND gate, present in the FATHER chip only, produces the coincidence

S0	S1	Pulse duration $[ps]$
0	0	trasparent mode
1	0	400
0	1	750
1	1	2000

Table 1.1. Selectable pulse duration depending on S0 and S1 bits.

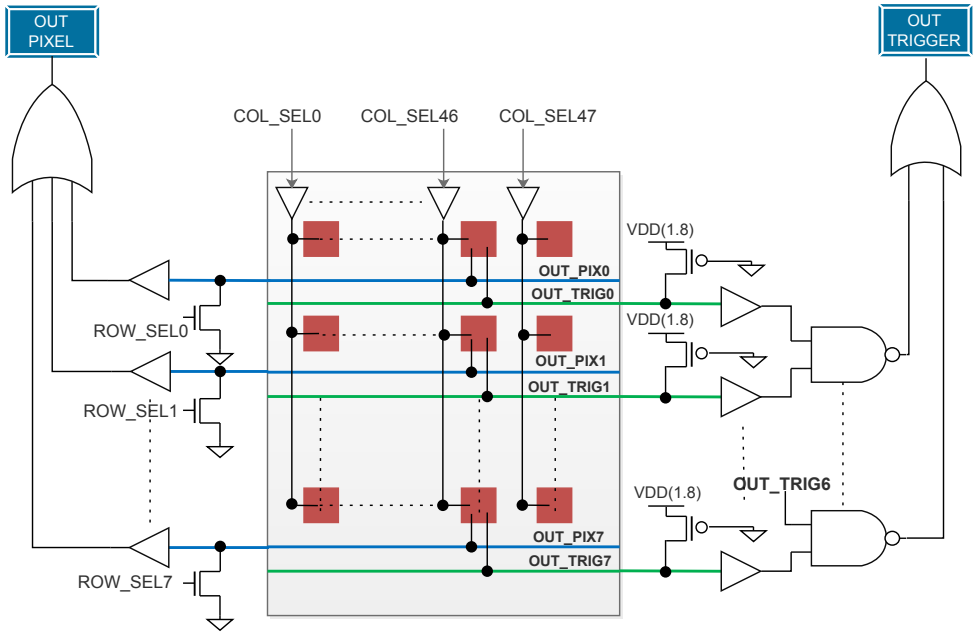


Figure 1.12. Single block of 8 rows, processing the signals coming from different cells.

detection between the signal coming from the monostable of the SON and FATHER chips. A weak pull-up was added to the connecting point with the SON chip, so that FATHER chips could also be characterized as an individual layer when no connection exists with the SON chip. The single bit produced as the coincidence signal is stored inside two cascading Set-Reset latches. The first latch asynchronously stores the bit providing the TRIG (trigger) signal. Data is transferred to the output of the second latch (OUT_PIXEL signal) if the DATATX signal is active, closing the switch between the two latches. Since latches cannot update their signal unless a reset signal is provided, the data stored inside these two latches should be cleared using the MEMRB and DATARB signals (active low) to observe a new detection event.
Figure 1.12 shows the block diagram of the bus connecting OUT_PIXEL and TRIG to the output pads. All the SPADs belonging to the same row share two buses: OUT_PIXx and OUT_TRIGx, physically connected to the two outputs of the cell, TRIG, and OUT_PIXEL. The OUT_PIXx bus is kept at a low logic level through a weak NMOS transistor. The OUT_TRIGx bus is kept at a high logic level through a weak PMOS transistor. So, a stronger pull-down, controlled by pixel signal TRIG, is necessary to drive the OUT_TRIG node at a low logic value. The array is divided into blocks and each readout block includes eight rows, connected to the corresponding output pad through a logic

OR gate. Therefore, the diagram shown in Figure 1.12 is repeated 9 times to cover all 72 rows of the two arrays. Arrays 1 and 3 have 18 output pads: nine pads for the output signal of the cells (OUT[0;8], [0;5] for array 1 and [6;8] for array 3) and nine pads for the trigger signal (TRIG[0;8], [0;5] for array 1 and [6;8] for array 3).

1.3.3 Bonding diagram

The dual-layer structure proposed by the APIX2 project [21] is made up of two chips, FATHER and SON, vertically interconnected through bump bonding techniques. For characterization purposes, some characterization measurements have been performed both on FATHER and SON chips separately. All the chips were bonded in a CPGA144 (Ceramic Pin Grid Array) package, with removable taped lids. Figure 1.13 shows the pin diagram of the FATHER and SON chips. Appendix A provides the complete pin list.

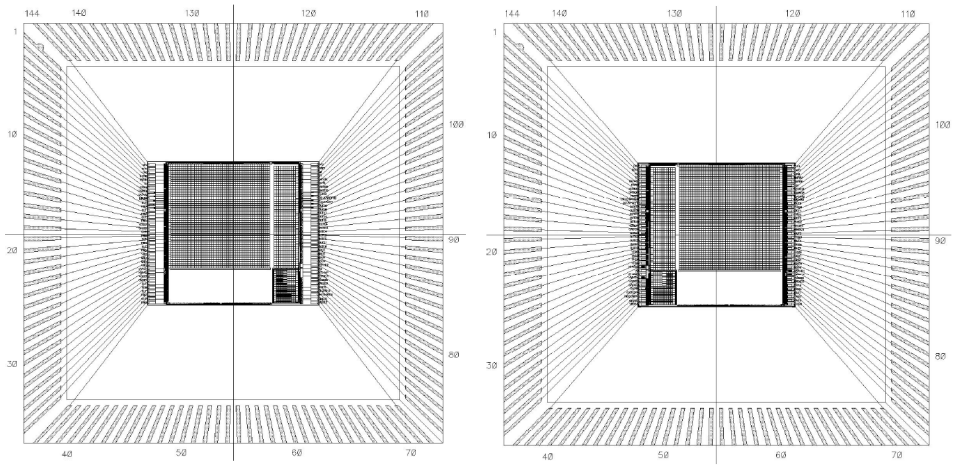


Figure 1.13. Bond diagram of the FATHER (left) and SON (right) chips in a CPGA144 package.

1.3.4 Chip operation and typical signal time diagrams

The SPAD is especially suitable for photon counting at weak light levels because for higher levels it is not possible to establish if one or more photons triggered the avalanche. The SPAD works basically like a switch, it is either ON or OFF, respectively if a particle has passed through or not.
The measurement of the signal from a SPAD is performed by defining a time interval, or a frame, when the SPAD is enabled and ready for detection. This

frame will provide as a result a 1 if an avalanche is triggered inside the junction, or a 0 otherwise. By iterating the same measurement with the defined frame, all the results can be summed up to obtain a total accumulated time that will produce the corresponding rate in Hz. For the APIX2LF chip, a time frame of 10 μs was chosen after an evaluation of the dark count rate range [24]. The accuracy of the small window duration is very important for a reliable count rate measurement.
Since the arrays of the chip are different from each other as far as the readout electronics and the SPAD features are concerned, the control signals needed for their characterization are also different. Some procedures work for all the arrays, while others are typical of some arrays. In the following, typical time signal diagrams related to the 1-bit readout architecture are discussed.

1.3.4.1 TRIGx reading procedure

Figure 1.14 shows the timing diagram of the signals used for the characterization of array 1. First, the parallel reading gets activated by setting the CONF signal to 1 so that a faster readout can be performed. The SPAD is then selected using the INIT and CK signals and the SPAD is then enabled using the EN signal. The small window begins after a reset is completed on both the latches that store data. When the MEMRB signal is released, being the SPAD still enabled, a dark pulse may occur, represented in Figure 1.14 by the red 0-1 transitions in the TRIGx signals. The end of the small window is marked by the activation of the ENRB signal which disables all the array pixels. The results of the measurement are now available to be read. When the measurement is performed one pixel at a time, TRIG, and OUT_PIXEL signals are equivalent. For a simpler reading procedure, the TRIGx pads can be read with x = $1, 2, 3, 4, 5$.
The same is true for array 3, except for the column selection signals that are INIT3 and CK3 (instead of INIT1 and CK1) and the output pads that in this case are TRIGx, with x = $6, 7, 8$.

1.3.4.2 OUTx reading procedure

When the OUTx signals are to be read, the reading procedure involves the use of the DATATX signal which drives the switch that connects the output of latch SR1 with the input of SR2, as shown in the diagram of Figure 1.15. Because the input of SR2 is a floating node if the switch is open, particular attention must be paid to the reset phase. First, SR1 gets reset (MEMRB), followed by DATATX set to 1 which closes the switch, and last, SR2 gets reset (DATARB). If the DATATX signal were not involved during the reset phase, there would be no low-impedance path toward the ground to discharge the S

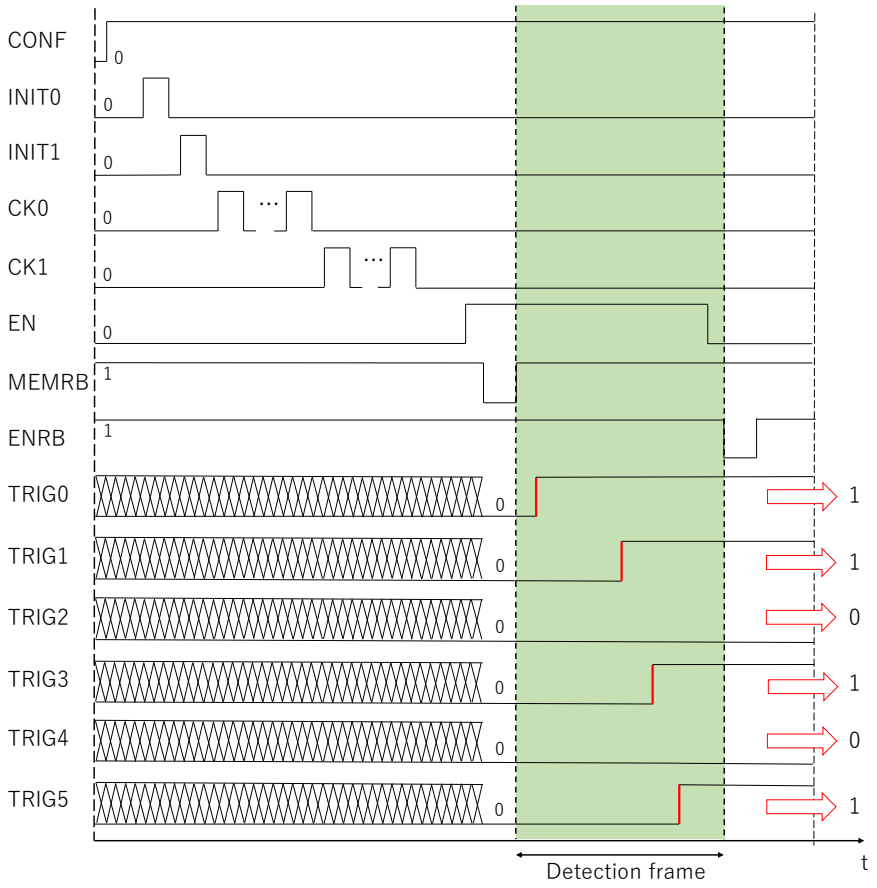


Figure 1.14. Signal time diagram describing the parallel readout approach of the array with 1-bit fast readout circuits (signal identifiers are specific for array 1).

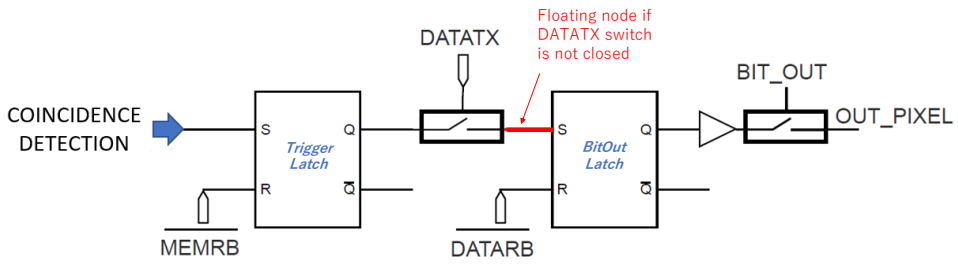


Figure 1.15. Detail of the memory block used in arrays with 1-bit fast readout electronics.

input node of SR2 (in red in the block diagram). If this is the case, when the DATARB signal is applied, the SR2 may find itself in a condition where both the input nodes are set to 1, and, accordingly, the reset operation cannot be performed. When the reset of the latches has finished, the measurement proceeds as already described for the TRIGx reading.

1.4 Characterization boards

Two custom boards, a *mother*, and a *daughter* board were designed to house the sensor and provide power supply, biasing voltages, and input/output signals [19]. The dual board approach offers more flexibility because several chips can be tested on a single mother board.
The daughter board (Figure 1.16) is a small 2-layer PCB designed for housing the CPGA144 package where the chip is bonded. It includes SMD bypass capacitors for power supply and reference voltage stabilization. Every chip package is soldered on its daughter board.
Figure 1.17 shows the layout of the top layer of the mother board. This 4-layer board needs a power supply of $+5/-5V$ and includes:

- 4 headers (black), arranged in a square shape, serving as the socket housing the daughter board.
- 7 voltage level transceivers (purple), used to adjust the voltage range of the signals coming from the microcontroller ($0 - 3.3\ V$) to the one supported by the chip under measurement ($0 - 1.8\ V$) and vice versa.
- 60 pins (orange), arranged in 3 header blocks, that are used to communicate with the microcontroller through a hard-wired connection.

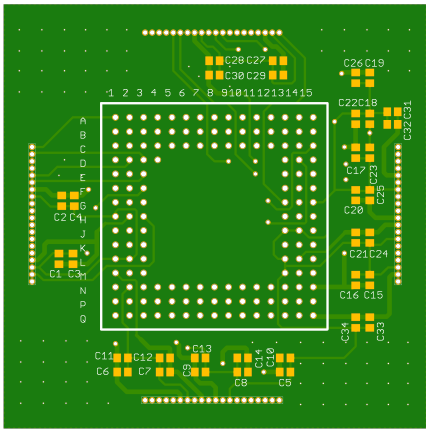


Figure 1.16. Layout of the daughter board.

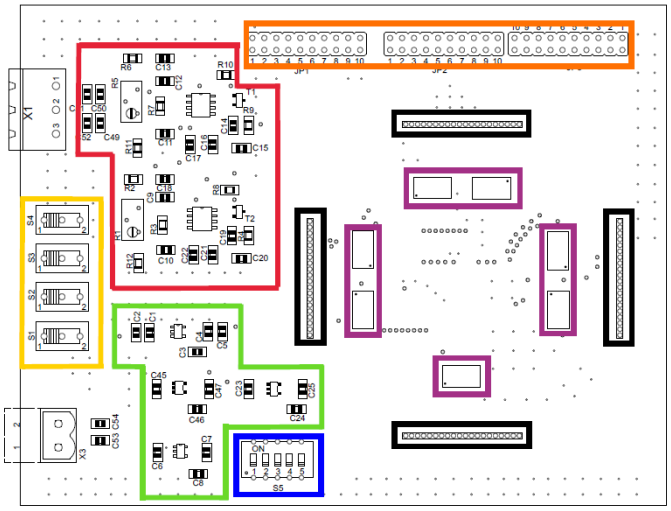


Figure 1.17. Top layout of the mother board.

- 4 regulators (green), that produce the 1.8 V supply voltage for the I/O electronics of the chip, the 1.8 V voltage employed as the supply voltage for the readout electronics surrounding the SPADs in the array structures, the 3.3 V voltage used in the active quenching circuits of the test array and the 3.3 V supply voltage of the level shifters.

- a block of 5 switches (blue), that control the power supply of the four arrays readout circuit (1.8 V) and the power supply for transistors with thicker oxide (3.3 V).

- 4 switches (yellow), one for each of the arrays, connecting SPADs cathode to the bias voltage. The SPADs of the array that will be tested are connected to a bias above their breakdown voltage, while the other SPADS are biased at 5 V. Both voltages are provided by the power supply unit.

- 2 circuits (red) for the generation of V_{CLAMP} and V_Q, the voltage references applied to the gate of the transistors performing the clamping and the quenching operation (Figure 1.11), respectively. Figure 1.18 shows the schematics of these two circuits. The desired voltage is obtained by tuning the trimmer inside the voltage divider. The output voltage (V_{out}), through the virtual short circuit at the OPAMP input terminals, gets stabilized by the feedback provided by the n-p-n bipolar transistor. This approach guarantees the generation of a voltage reference that satisfies the requirements of stability and tunability typical of the application.

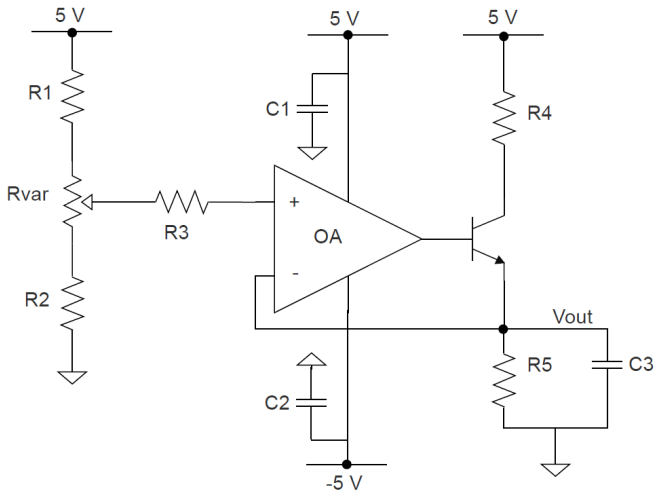


Figure 1.18. Scheme of the circuits used to generate the V_{CLAMP} and V_Q voltage references.

1.4.1 Benchtop setup

Characterization measurements of FATHER, SON, and dual-layer APIX2LF chips were carried out and results are available in [24], [22].
The measurement system used for those results consisted of a microcontroller, a Bluetooth module, three custom boards, a power supply unit, and a computer. The latter is used to run the main program that drives the measurement through the several steps needed for a thorough characterization. A *Matlab* script managed communication with the microcontroller through a Bluetooth connection, and with a power supply unit using a GPIB interface. The measurement system was considered automated because it could perform a complete measurement of DCR at different bias voltages, i.e., different excess voltages, without any external intervention.
The microcontroller used in this setup is an STM32F051 produced by *STMicroelectronics* and mounted on the STM Discovery board. The system clock, generated inside the microcontroller and through an internal PLL, is 48 MHz, which is the maximum oscillation frequency obtainable without any external quartz mounted on the board. The connection between the microcontroller and the Bluetooth module, produced by *STMicroelectronics*, is bidirectional and is based on the USART protocol. The USART link requires a cabled connection implemented on a custom-designed board. Measurements results were sent to the Personal Computer pixel by pixel.
This setup has limited capability of signal processing and acts only as a bridge between the computer and the device under test. All data processing was carried out in the *MATLAB* environment.

Limitations in the operating clock of the STM32F051 microcontroller resulted in some drawbacks in the characterization measurements, especially for dual-layer chips, which took a long time to complete. Furthermore, the setup was unwieldy and difficult to transport to other laboratories to perform necessary measurements in different environments. To fulfill the project objectives of developing a portable detection probe, a more compact solution with an efficient interface with the sensor was required. To address these challenges, a more powerful microcontroller was selected for the setup, enabling also a more compact and portable benchtop measurement setup. In the upcoming chapter, the new microcontroller, which serves as the interface between the chip and the PC for this thesis work, will be introduced.

Chapter 2

Particle Imaging Probe and firmware design

The ASAP collaboration, funded by INFN, has developed a new generation of layered SPAD detectors for charged particles aimed at reducing noise while maintaining a low material budget. This thesis work focuses on the design of a compact probe based on one of these new chips, the APIX2LF sensor, for mapping the activity of laboratory sources and potential use in medical applications such as radio-guided surgery (RGS).
In RGS, the probe effectiveness relies on its ease of handling, lightweight design, and balanced construction. Battery-powered operation ensures portability and maneuverability by removing the need for cables. Real-time feedback, conveyed through visual or audio signals, plays a vital role in providing precise guidance during the procedure.
Several portable solutions have been proposed for particle localization in RGS. In breast tumor localization with gamma rays, a solution described in [25] uses an aluminum-enclosed probe with a scintillation crystal, a SiPM, and a rechargeable battery. The output is displayed on a computer via a cable connection. The Pocket Gamma Camera (PGC), introduced in [26], is a compact and lightweight intraoperative gamma camera for preoperative lymphoscintigraphy. It incorporates a collimator, scintillator, SiPM, and has an embedded system for data processing. Data can be transmitted to a computer through a USB interface. The MAGICS gamma camera, presented in [27], is designed for tumor localization in RGS. It includes a collimator, a scintillator, an array of SiPMs, and a readout system with preamplifiers, shapers, track-and-hold blocks, and an ADC. Data is saved and transferred via USB, with optional wireless transmission. For RGS with beta particles, a probe described in [28] incorporates a shielded scintillator tip, optical fibers, and a PMT. The readout electronics are housed in a compact box that wirelessly connects to a count

rate monitor.
To meet the requirements of portability and wireless data transfer, the probe of the APIX2LF was designed to be battery-powered and interfaced wirelessly with a PC. A different microcontroller was selected to optimize performance and minimize board area to act as the interface between the sensor and the computer and new firmware was developed for it. Data can be sent to the computer by multiple protocols (USB, Wi-Fi, or Bluetooth), depending on the measurement requirements and conditions. Although the initial focus was on the APIX2LF chip, the design, components, and firmware of the probe can be adapted for other SPAD sensors since the underlying principles and methodologies employed in the design of the system can be extended to accommodate other SPAD sensors with similar characteristics.
Research into detector technology is crucial for achieving the necessary expertise for broader commercial and practical use in various applications. As such, chip characterization is essential for understanding the behavior of the new sensors in different conditions and for achieving optimal performance. Therefore, the design of the detection probe and the characterization of the chips are interconnected activities for obtaining comprehensive research results.
The first part of this chapter describes the design of the imaging probe and the selection of the components. A prototype version of the probe was developed and tested, and a miniaturized version is currently being developed. Characterization measurements were performed with both the prototype and benchtop boards using the new microcontroller. The second part of the chapter discusses the setup used to test the probe prototype and characterize the APIX2LF chip, including the programs used to manage the measurement setup and all firmware developed for the microcontroller.

2.1 Probe Design

Given the potential of SPADs as charged particle detectors, it was proposed to use the APIX2LF chip as the core sensor of a portable detection probe [29], [30], [31].
As already mentioned in Section 1.4, for characterization purposes the SPAD based chip was bonded in a CPGA144 package (Figure 2.1, left). The development of a smaller housing case for the APIX2LF sensor was necessary for the miniaturized probe, and a two-stack printed circuit board was designed for this purpose at the University of Padova. As shown in Figure 2.1 (right), the APIX2LF sensor is bonded on the top printed circuit board, while a commercial SiPM (Advansid ASD-NUV4S-P) with a BC-408 scintillator is mounted on the second printed board of the stack, located below the SPAD sensor. To optimize the area, only array 1 and array 3 were connected and made available

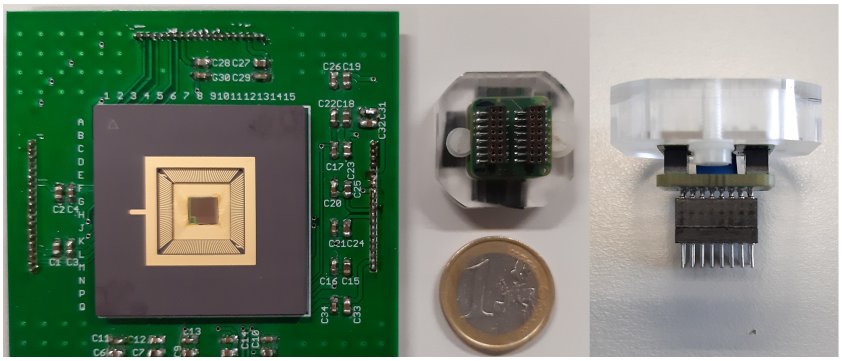


Figure 2.1. APIX2LF housing boards.

for measurements on the APIX2LF carrier.
The probe was designed to be an all-in-one solution, with the microcontroller and all the reference circuits located on the same board, based on the existing characterization boards described in Section 1.4. To ensure flexibility in its use, the probe was designed to be powered either by cable or battery. The following section provides a detailed description of the components selected for the detection probe.
A prototype version of the probe was designed and produced to test and verify the proper functioning of all the new components added in comparison to the previous characterization boards. Once the prototype was validated, the design of the portable probe was finalized with the necessary area optimization. The multi-layer boards were designed using the EAGLE program by Autodesk.

Microcontroller
The microcontroller market nowadays offers excellent solutions in terms of power management, signal processing, and data transfer. The evolution of the Internet of Things (IoT) has enabled the development of system-on-chips (SoC) with integrated wireless solutions.
The ESP32 is a popular choice for IoT applications due to its low power consumption and wireless capabilities. It is also commonly used in embedded systems, robotics, and automation. The dual-core processor and high-speed signal processing make it suitable for applications that require real-time data processing, such as sensor networks and control systems. Additionally, the integrated Wi-Fi and Bluetooth capabilities make it easy to connect to other devices and networks, making it an ideal choice for wireless data transfer applications. Overall, the ESP32 offers a powerful and cost-effective solution for a wide range of applications [32].
The microcontroller works on a 3.3 V power supply. It includes 320 KB RAM, 32 programmable GPIOs, 12-bit SAR ADC, 8-bit DAC, I^2S, I^2C, UART and

Ethernet MAC interfaces, SPI, SDIO, and PWM. Espressif offers a wide choice of frameworks and environments that can be used for ESP32 programming, but in the context of this project, the official ESP framework was used [33]. It is based on C libraries and the operating system is FreeRTOS® with built-in hardware acceleration. For building a full application on ESP32, CMake and Ninja are needed.
The ESP-IDF essentially contains API (Application Programming Interface) such as software libraries and source codes for ESP32 and Python scripts to operate the toolchain needed for compiling the ESP32 code. A lot of documentation is also available for programming the microcontroller by writing directly on its registers. All the protocols, including TCP/IP and Bluetooth suite are fully specified and described in libraries.
There are two CPU cores that can be individually controlled and assigned to different tasks (such as data processing and wireless communications) to optimize the performance of the device. The CPU clock frequency is adjustable between three possible operating frequencies: 80, 160, and 240 MHz. The chip also contains a low-power co-processor that can be used to save power for certain tasks that do not require computing power.
The sleep current of the ESP32 chip is less than 5 µA, making it suitable for battery powered applications. The module supports a data rate up to 150 Mbps [34]. The ESP32 can be found commercially mounted on developing boards offering all the needed components for powering, programming, and debugging, or it can be found also as a module with an integrated antenna for wireless communications. For the preliminary testing and characterization measurements, the WiFi Kit 32 development board from Heltec was used. It includes the ESP32-D0WDQ6 chip, GPIO connectors, 2.4 GHz PCB antenna, a micro-USB interface and a USB to serial port chip for program downloading, debugging, and information printing. The ESP32 WROVER (PCB) [34] was instead used for the probe design. The core of this module is the ESP32-D0WDQ6 chip, and includes the PCB antenna for Wi-Fi and Bluetooth, 4 MB SPI flash memory and 8 MB SPI Pseudo static RAM.
Depending on the kind of measurement or application, the clock frequency used for the microcontroller is 160 MHz when the probe was battery powered and 240 MHz for characterization measurements. Data transfer and signal interface with the sensor and data processing are managed each by a different core of the microcontroller.

Power Supply
The detection probe is intended for continuous use, so a rechargeable battery was assumed to be the best solution. From the perspective of the microcontroller working with a 3.3 V power supply, a higher voltage was required to be used. Besides, the battery should be as small as possible but with a sufficient

energy charge to ensure operation for several hours.
Since their appearance on the market, lithium-ion batteries (Li-Ion) have been the most popular choice in consumer electronics having the best energy density and a very slow discharge when not in use. In particular, Lithium-ion polymer batteries (LiPo) are light in weight, with shape flexibility while also offering slightly higher energy density than Li-ion at a slightly higher cost [35]. The nominal voltage of a LiPo battery varies between 3.6 and 3.7 V, while the charging voltage is 4.2 V. There are specific IC battery charge controllers available in the market for different power supply voltages.
The battery chosen for powering the probe is the RS PRO LiPo rechargeable battery, with a charge capacity of 2.6 Ah that can run between -20 and 60 °C [36]. With the power dissipated by the probe, after full charge, the battery is expected to be able to guarantee up to 10 hours of lifetime.
Since the USB standard has become a spread possibility, the alternative power supply for the board and battery recharge was chosen to be 5 V. The circuit shown in Figure 2.2 adds the possibility of battery power detection and to switch automatically between USB or battery power. The probe also has a battery management system (Figure 2.3) consisting of charge and discharge management, and overcharge protection based on Microchip device MCP73831.

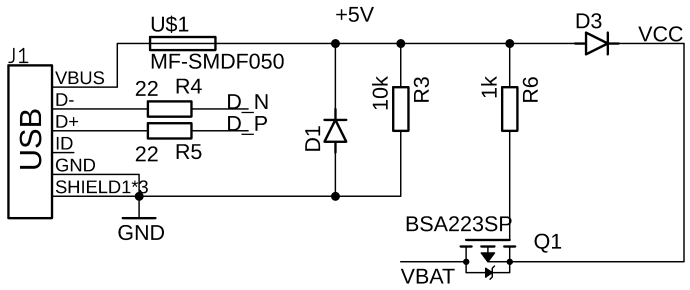


Figure 2.2. Electrical circuit for choosing between battery or USB power supply.

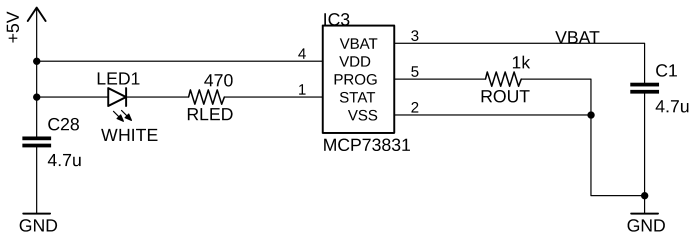


Figure 2.3. Electrical circuit for LiPo battery recharge.

ASD-NUV4S-P readout electronics

The Advansid ASD-NUV4S-P SiPM was added in the stacked carrier to provide a triggering signal when measurements with an active source are performed. It is an analog SiPM, i.e., all SPADs of the array, based on the p-on-n silicon technology for near-ultraviolet light detection, are connected in parallel. The detection spectrum extends from 350 to 900 nm, with the peak efficiency at 420 nm. To achieve a more efficient detection a BC-408 scintillator, with peak emission spectra around 430 nm, covered by a mylar foil was placed on the top of the SiPM.

The ASD-NUV4S-P has 9340 cells, with a pitch of 40 µm, and a fill factor of 60 %. The total effective area is $4 \times 4\ mm^2$. The breakdown voltage ranges between 24 and 28 V and it can operate within a range of 2 up to 6 V of overvoltage.

From characterization measurements performed on the SiPM, the breakdown voltage was found to be 25.5 V. As a compromise between DCR and PDE, the SiPM was biased with 2 V of overvoltage.

A SiPM is basically a current source, but electronic instrumentation normally works by processing voltage signals, therefore it is necessary to convert the current into a voltage. Two main front-end configurations can be distinguished among others [37]:

- active current-to-voltage conversion, based on a transimpedance amplifier
- passive current-to-voltage conversion, where the diode is connected to a resistance and whose voltage drop gets subsequently amplified

In the passive configuration there are two more resistors that contribute to noise, but the active version is slower than the passive one [37].

To minimize noise contribution, a transimpedance two stage inverting amplifier (Figure 2.4) was used to read the current coming from the analog SiPM. The first stage is a common source stage consisting of an NPN 9 GHz wideband transistor, T_1, with a resistive load represented by resistor R_3 and a feedback resistor $R_F = 2.4\ k\Omega$ while C_1 is a decoupling capacitor. The output voltage of this stage is fed to an emitter follower stage consisting of a PNP 5 GHz wideband transistor, T_2, with R_O as load. The first stage assures an adequate gain while the second one presents a low output resistance, thus guaranteeing a sufficiently wide bandwidth.

The output of the transimpedance amplifier is connected to a comparator whose output signal is used as a trigger for reading the APIX2LF chip. When the output voltage is below a certain threshold voltage, meaning that a particle has been detected by the SiPM, the microcontroller starts reading the SPADs of the APIX2LF array.

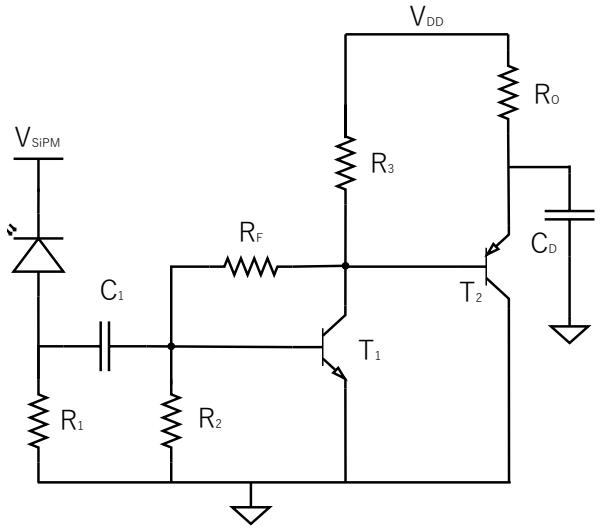


Figure 2.4. Schematic circuit diagram of the transimpedance amplifier connected to the SiPM.

SPAD biasing

During the characterization measurements, the bias voltage for the SPADs was provided by a power supply. However, since the probe needed to be portable and wireless, it was necessary to obtain the SPAD bias voltage from the battery-supplied voltage. One way to generate a higher voltage starting from a lower voltage source is by using a DC-DC boost converter. Among the many commercially available IC, the choice was made based on the voltage source already present on the board and the required bias voltages for the SPADs. The minimum voltage supplied is represented by the LiPo battery with 3.7 V. The SPADs of the APIX2LF are biased between 19 V and 21 V, while the SiPM works with a bias voltage between 27 V and 28 V.

The chosen DC-DC boost converter is a TPS6104 produced by Texas Instruments [38]. From a single-cell Li-Ion battery, this device can generate output voltages up to 28 V operating with a switching frequency of up to 1 MHz in a small package. The TPS61041 has a 250 mA switch current limit, offering a low output voltage ripple. Figure 2.5 shows the schematic circuit diagram. Using a trimmer ($R_2 = 200\ k\Omega$), the output voltage of the DC-DC boost converter can be regulated to obtain the desired value for the APIX2LF and the Advansid SiPM.

Particular attention must be paid to the layout design when using switching power supplies with high peak currents and switching frequencies. In order to minimize ground shifts and noise, wide traces were used for signal connections, and a ground plane was implemented.

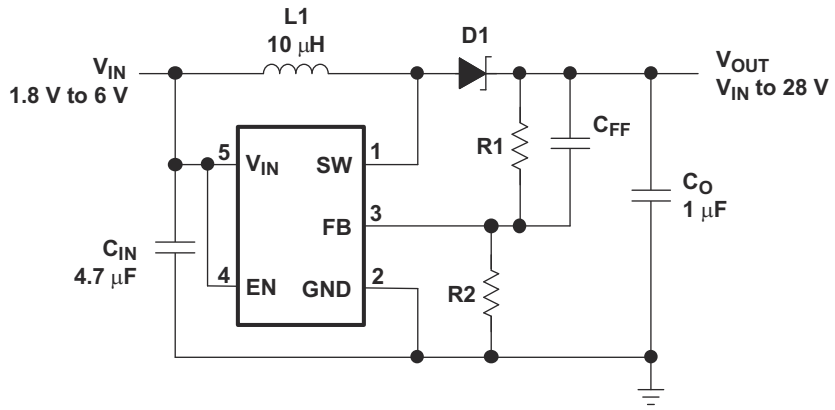


Figure 2.5. Schematic circuit diagram of the DC-DC Boost converter TPS61041 [38].

Supplementary components

Referring to Figure 1.11, the voltage references applied to the gate of the transistors performing the clamping operation (V_{CLAMP}) and the quenching operation (V_Q) are obtained by tunable circuits as described in Section 1.4. Tunability is necessary for initial characterization measurements to investigate DCR dependence on the quenching voltage: measurements performed in [24] show that the DCR increases as the quenching voltage increases because the quenching current rises, causing a greater charge flowing through the device. As a result, the power consumption increases, leading to an augmented temperature which is responsible for a DCR growth. Moreover, when the charge flowing through the device increases, deep levels are more likely to trap a carrier, leading to an afterpulsing phenomenon. The quenching voltage used for further characterization was set to 900 mV because of a lower level of dark count rate and consumed power [24].

Regarding the clamping voltage, no tunability is needed for characterization purposes since it is set by the supply voltage of the APIX2LF chip, i.e., 1.8 V. To minimize the area of the printed circuit board, IC precision low power voltage references were utilized to generate the V_{CLAMP} and V_Q voltages. Specifically, the ISL60002CIH318Z-TK and the ISL21080DIH309Z-TK by Renesas Electronics were chosen for this purpose.

As already specified, the APIX2LF operates with $V_{DD} = 1.8\ V$ while the microcontroller works with 3.3 V so bus transceivers are needed. For area reduction, the probe employs two 16-bit bus transceivers (SN74AVCA164245 by Texas Instruments) instead of the seven 8-bit bus transceivers used for the main board (Figure 1.17).

The ESP32 has a dedicated UART interface with pins labeled as TX and RX.

These pins receive binary data used to flash the device memory with a new application for execution. Using a USB-to-UART bridge, a serial connection can be established between the computer and the ESP32 microcontroller. A terminal emulator can display data received from the ESP32 as characters on the screen. When using serial communications, an essential parameter to consider is the baud rate, which determines the rate at which information is transferred. By default, the ESP32 assumes a baud rate of 115200 bit/s, which is the maximum rate for flashing the microcontroller. Additionally, there are control signals such as RTS, CTS, DTR, DCD, and RI, as specified by the RS-485 standard.
The CP2102 chip produced by Silicon Labs is used as a USB-to-UART bridge for flashing and communication between the ESP32 and the computer (Figure 2.6). It includes an internal clock, a 3.3 V voltage regulator and a programmable ROM and supports rates up to 921600 bit/s. By toggling RTS and DTR signals (Figure 2.7) the microcontroller gets reset.

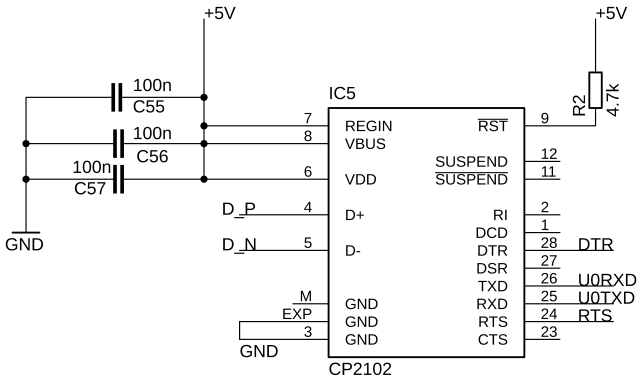


Figure 2.6. Schematic circuit diagram for USB to UART bridge.

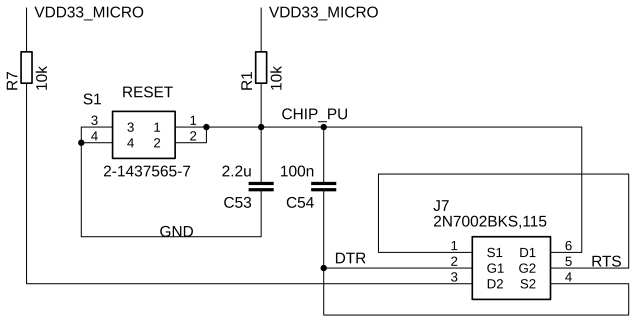


Figure 2.7. Schematic circuit diagram for microcontroller reset via USB connection.

Probe Layout
Several test measurements were performed with the probe prototype and with the benchtop boards to validate the components. Measurements confirmed that all the components added or changed did not affect the behavior of the chip. After the validation process was considered satisfying, a 6-layer miniaturized probe was designed using EAGLE program for printed circuit board (PCB) design.
The layout of the miniaturized probe is shown in Figure 2.8 with the corresponding dimensions. Among the available models, the ESP32 WROVER module was used as the core microcontroller, since it includes the PCB antenna for Wi-Fi or Bluetooth data transfer.

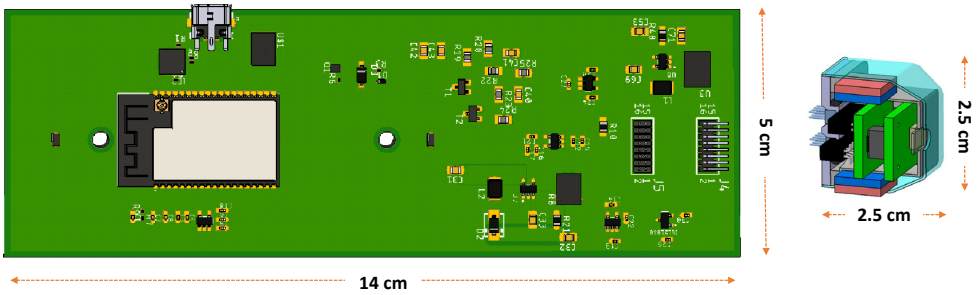


Figure 2.8. Probe board prototype (left) and chip housing board (right).

2.2 Firmware Design

The APIX2LF has been proposed as a new kind of SPAD-based sensor for charged particle detection. Its benefits in terms of noise reduction have been discussed theoretically and proved experimentally [19], [21], [20], [23], [24], [22]. Anyway, to fully characterize a technology, more measurements are needed in order to have more reliable statistics on their behavior such as breakdown voltage uniformity within a chip and among different chips, dark count rate dependence on excess voltage and temperature, crosstalk, and Random Telegraph Signal (RTS) phenomena. For this reason, additional functions have been implemented within the firmware to perform full array characterization. In this section, a more detailed description of the firmware used for measurements and data transfer is discussed. The ESP32 microcontroller was programmed using the official Espressif IoT Development Framework (IDF v4.3) based on C and FreeRTOS. The software used for the design of the firmware was Eclipse IDE (2020-06) with the ESP-IDF plugin.
To achieve flexibility, three firmware versions were developed for data transfer via USB, Bluetooth, and Wi-Fi, depending on the type of measurement and

environment where it is being executed. Bluetooth offers a better performance in terms of power consumption, so it is the best choice when the most pressing requirement is power. On the other hand, Bluetooth has a limited bandwidth and covers smaller distances as compared to the Wi-Fi protocol. The USB data transmission is to be preferred as it can be more reliable when long and iterated measurements are performed.

2.2.1 APIX2LF related functions

In the following sections, the different functions implemented in the firmware for performing various types of measurements will be presented and discussed. The general flowcharts relevant to the five different measurement procedures are shown in Figures 2.9, 2.10 and 2.11. They are referred to as

- "1-by-1", i.e., SPADs are enabled and read one by one while all the others are disabled, (Figure 2.9, left)
- "AllON", i.e., count rate is measured in each SPAD while all the SPADs are simultaneously enabled, (Figure 2.9, right)
- Random Telegraph Signal (RTS) noise investigation (Figure 2.10, left)
- Crosstalk investigation (Figure 2.10, right)
- SiPM triggered measurement (Figure 2.11)

All of the five flowcharts share the first three blocks, while slightly differing in the remaining part. The common blocks concern the configuration of the pins of the microcontroller and the initialization of the chip under test.
Through defined macros, a non-expert user can choose the desired kind of measurement to be performed, which array is to be measured, or even if a specific part of the array is to be characterized.
In the beginning, the general-purpose pins must be configured correctly to function as input or output pins of the microcontroller. Once pin configuration is complete, the system is ready for communication with the sensor. Global initialization is necessary for all input signals of the APIX2LF, to ensure that they have a defined value. During the array initialization phase, several operations are performed, including setting the monostable duration, enabling or disabling parallel reading, and sending a clock signal to all column and row shift registers. The purpose of sending the clock signal is to ensure that all registers have a defined output value.

```
GPIO_config();
Array_PREInitialization();
Array_Initialization();
```

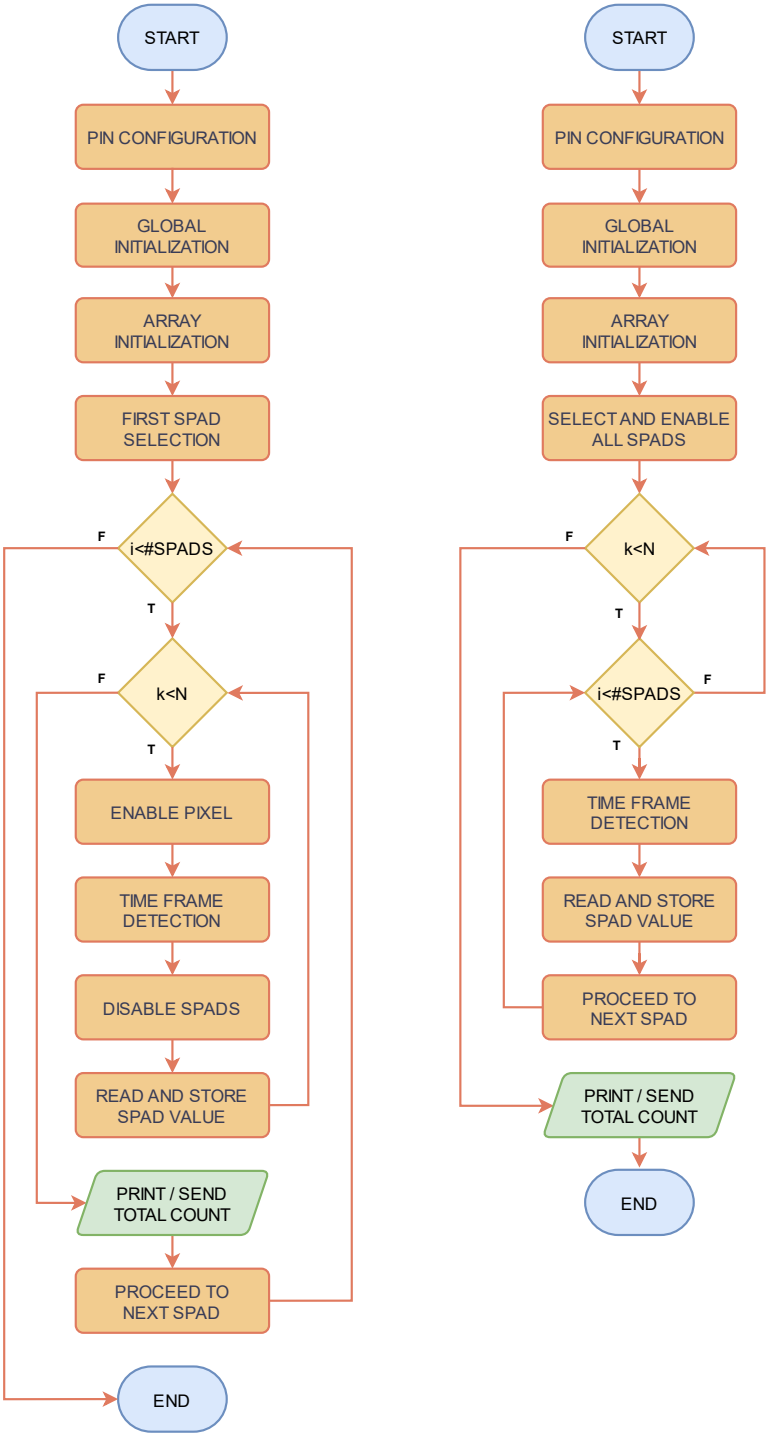


Figure 2.9. Flowchart of "1-by-1" (left) and "AllON" measurement (right).

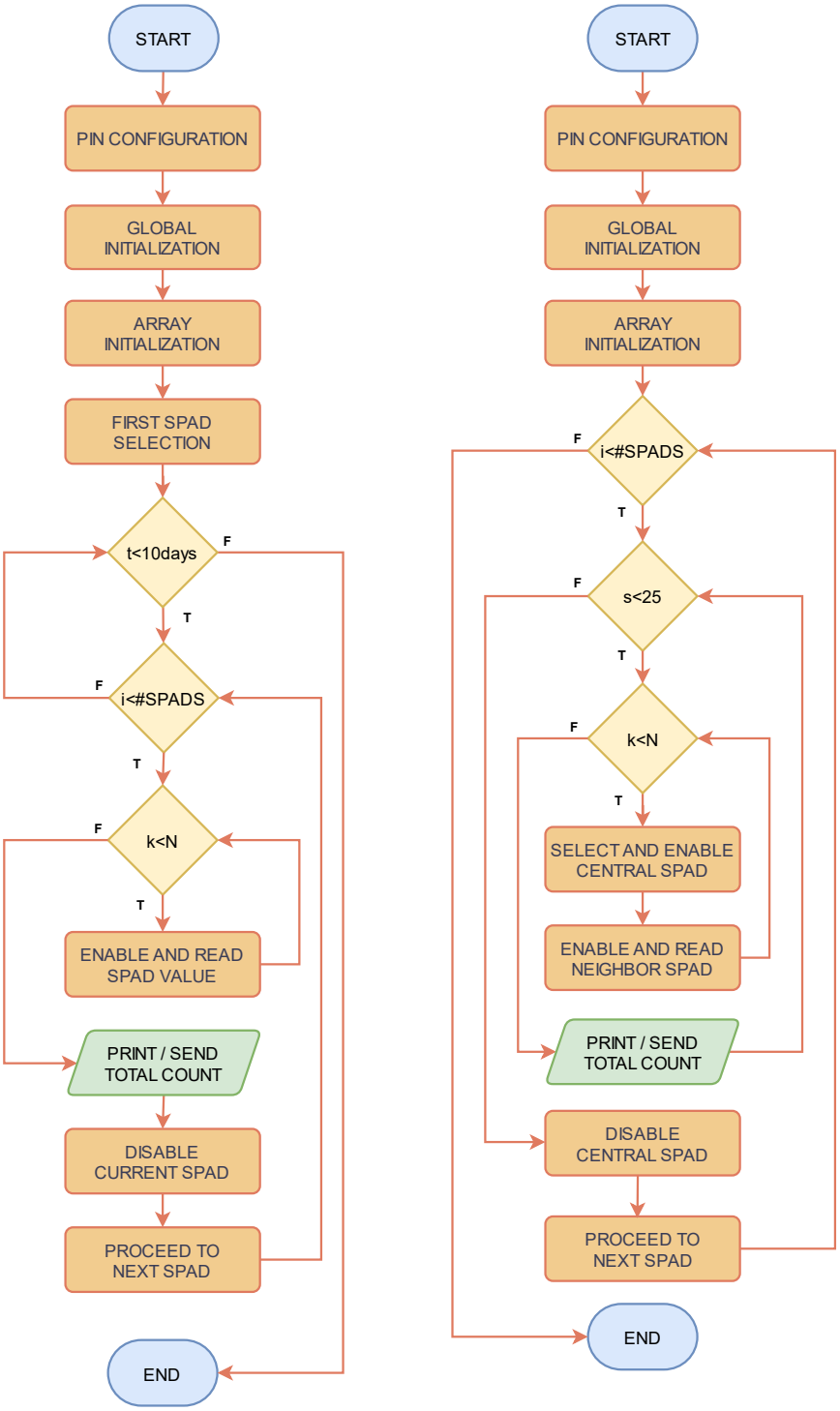


Figure 2.10. Flowchart of RTS (left) and Crosstalk measurement (right).

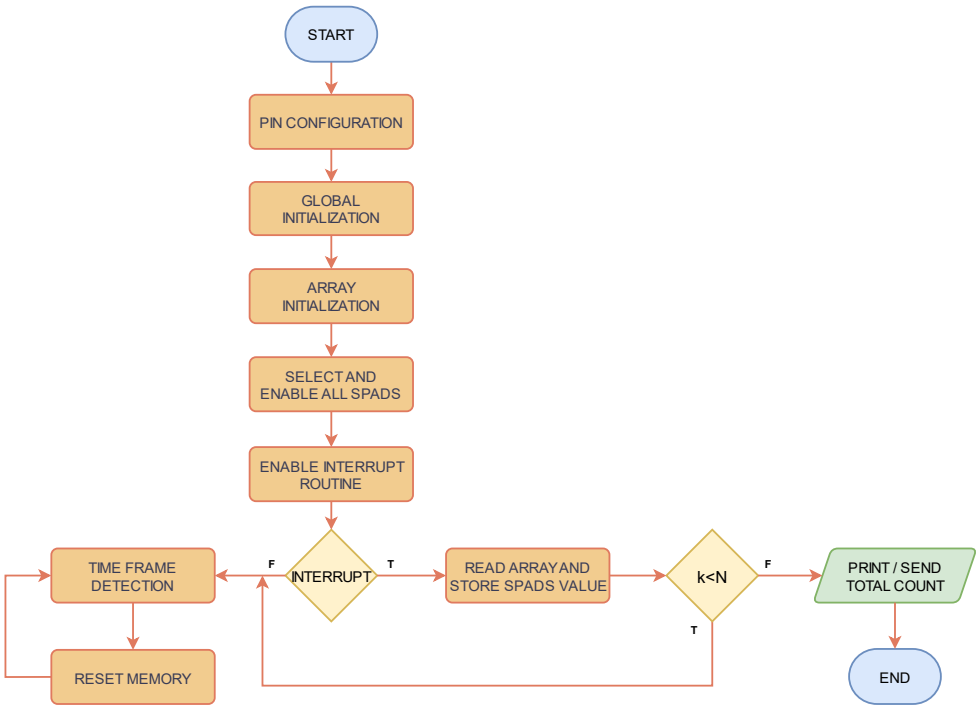


Figure 2.11. Flowchart of SiPM triggered measurement.

2.2.1.1 "1-by-1" measurement

As suggested by its name, in the "1-by-1" firmware characterizes each pixel separately from the others. When the parallel reading is disabled, only one SPAD is enabled and read while the other SPADs are disabled. When the parallel reading is enabled, 9 SPADs are enabled and read while the remaining SPADs are disabled. As described in Section 1.3.1, the first pixel of array 1 is selected when the row and column shift registers are initialized. This firmware is designed to be flexible, allowing users to select a sub-array of SPADs by specifying the starting and ending rows and columns because the reading proceeds row by row.
The function *SelectPixelArray_1* addresses the first desired pixel by specifying its row and column. As explained in section 1.3.4, once the targeted SPAD has been selected (by suitably setting the ROW_SELx and CO_SELx signals of Figure 1.10), the SPAD is enabled by acting on the EN signal. Pixel enabling, time frame detection, output pad reading and data storing is performed by the *ReadArray1_Values* function. The detection time frame is defined by two signals: the MEMRB signal, i.e., the reset signal of the Trigger Latch in Figure 1.11, and the ENRB signal, i.e., the reset signal of the Latch in Figure 1.10. Figure 1.14 illustrates the starting and ending boundaries of the de-

tection frame with dashed lines: the release of the MEMRB signal initiates the detection frame, while the activation of the ENRB signal terminates it. This operation is repeated a defined number of frames, NR_ITERATIONS, (for example 100000) with a duration of 10 µs each, which, sum up to obtain a specific total integration time, TIT, (in this case, 1 s). Each logical value reading is added to a variable that stores the overall count.
Once the total integration time has elapsed, the SPAD is disabled, and the total count value is sent to the PC. This operation is performed by the function *printTotalCountA1*. The reading then proceeds to the next pixel, completing the columns before advancing to the next rows, until the last desired SPAD is read. This function can read either the TRIGx or OUTx pads.

```
SelectPixelArray_1(row_begin, col_begin);
for (i=row_begin; i<row_end; i++)   {
    for(j=col_begin;j<=col_end; j++)    {
        while(k<NR_ITERATIONS){
            ReadArray1_Values(i);
            k++;              }
        printTotalCountA1(CONF,i,j);
        k=0;
        proceedColoumnA1();             }
    proceedRowA1(col_begin);        }
```

2.2.1.2 "AllON" measurement

In the "AllON" measurement, all the pixels of array 1, array 3, or both arrays, are kept enabled during the measurement. The reading operation is slightly different in this case as compared to the "1-by-1" measurement. Here, the initialization of all the input signals is followed by enabling all the SPADs of the array using the *Array_1and3 _EnableAllPixels* function.
Once all SPADs have been enabled, the *timeFrame* function is used to provide a detection frame defined in this case by the MEMRB signal only. Referring to Figure 1.15, when the DATATX is enabled, the signal coming from the SPAD passes to the *BitOut* latch. Before the detection frame starts, the two latches get reset by MEMRB and DATARB signals. They are then released simultaneously initiating the detection frame. After 10 µs, the *Trigger* latch is reset marking the end of the detection frame.
To perform the readout of all SPADs of the array, the *RealAllArrayXEachEvent* function reads the logic value in each *BitOut* latch and adds it to the correspondent element of an array variable with the same dimension as the SPADs array. This operation is repeated for a defined number of frames, NR_ITERATIONS, to obtain a specific total integration time, for example, 1 s for 100000 frames. Once all iterations have been completed, the *printEntireArray* function sends

data to the PC.

```
Array_1and3_EnableAllPixels();
while(k<NR_ITERATIONS)  {
    timeFrame();
    ReadAllArrayXEachEvent();
    k++;                }
printEntireArray();
```

2.2.1.3 Crosstalk measurement

Crosstalk phenomenon contributes to DCR and, as explained in Section 1.1.5, it is caused either by charge carriers or by secondary generated photons that provoke avalanche triggering in the neighboring pixels. It is performed while the parallel reading is disabled. The crosstalk measurement was conceived as a detailed investigation of this phenomenon. As in [39], the focus is on a single SPAD, called Device Under Test (DUT), which is kept enabled all the time, and observe its effect on adjacent SPADs up to a specific number of rows and columns far from it which are enabled one at a time.
The crosstalk measurement was performed on sub-arrays of 5×5 SPADS. The value of $SCREAM\_BOX$ refers to the size of the sub-array, where $SCREAM\_BOX = 2$ means that each sub-array consists of 25 SPADs arranged in a 5×5 grid. The DUT is identified by its row and column, respectively, *screamer_row* and *screamer_col*.
The *EnableScreamerA1* function addresses and enables the DUT. After that, each SPAD belonging to the 5×5 array with the DUT at the center gets enabled and measured while all the other SPADs are kept disabled in the same way as for the "1-by-1" measurement. Once the total integration time has elapsed, data is sent to the PC.
The *SelectPixelArray_1*, *ReadArray1_Values* and *printTotalCountA1* are the same functions described for the "1-by-1" measurement in Section 2.2.1.1.
This 5×5 grid reading is iterated for all the pixels of the arrays, except for the SPADs belonging to the corner, i.e., the first and last two rows and columns.

```
for (i=screamer_row-SCREAM_BOX; i<=screamer_row+SCREAM_BOX; i++){
    for(j=screamer_col-SCREAM_BOX;j<=screamer_col+SCREAM_BOX; j++){
        while(k<NR_ITERATIONS){
            EnableScreamerA1(screamer_row,screamer_col);
            SelectPixelArray_1(i,j);
            ReadArray1_Values(i);
            k++;            }
        printTotalCountA1(0,i,j);
        k=0;    }   }
```

2.2.1.4 RTS measurement

The presence of defects degrades the performance of a SPAD by inducing Random Telegraph Signals. It consists of the discrete switching between two or many different DCR levels with random switching times. In order to mitigate RTS effects it is important to identify them and determine the dependence on the environmental parameters [40].
The core of the RTS measurement is the same as the "1-by-1" measurement, described in Section 2.2.1.1, but the reading process repeats endlessly until the user stops it. Every single SPAD of arrays 1 and 3 is read roughly every minute, which can be considered a reasonable time given that the RTS phenomena have a long time constant, with an overall measurement duration of 10 days. This kind of measurement was accomplished to have a general overview of the number of SPADs that exhibit the RTS behavior inside a defined array. Knowing which pixels have RTS, it is possible to further investigate the characteristics of the RTS phenomenon such as the number of defects that causes it, the characteristic time, and the amplitude distribution. A feature was added to the function so that only a few selected SPADs could be measured with a shorter reading time, for example, every second.

2.2.1.5 SiPM triggered measurement

As shown in Figure 2.1 the small carrier developed for the probe consists of two stacked printed circuit boards. The APIX2LF chip is bonded on the upper PCB while the bottom PCB accommodates the Advansid ASD-NUV4S-P SiPM.
A function was developed for measurements with a radioactive source using the SiPM signal as a trigger for reading the APIX2LF array. As described in section 2.1, the SiPM signal is amplified by a transimpedance amplifier and connected to a comparator, whose output is used as an interrupt signal for the microcontroller to read the SPAD array. Similar to the "AllON" measurement, all pixels are enabled at the start and remain enabled throughout and the detection frame is defined as the period when the reset signal of the *Trigger* Latch (MEMRB, active low) is kept disabled.
When no particle is detected by the SiPM, the APIX2LF remains in detection mode, with the array continuously resetting and latching new values during the specific time frame. If a particle triggers an avalanche inside the SiPM, the loop is interrupted, and all pixels of the APIX2LF are read and their content is stored. After a specific number of **N** events are detected by the SiPM, corresponding to a number of reading iterations for the sensor, the total number of counts per pixel is sent to the PC.
Below is provided the code for the interrupt handler function. The func-

tions *ReadAllArrayXEachEvent* and *printEntireArray* are the same as those described for the "AllON" measurement in Section 2.2.1.2.

```
static void handler(void *args) {
    ReadAllArrayXEachEvent();
    if(k>NR_TRIGGER){
        printEntireArray();     }
    xQueueSendToBackFromISR(gpio_evt_queue, &gpio, NULL);   }
```

2.2.2 Data transfer

The microcontroller's capabilities offer flexibility in data transmission options, allowing users to choose from various protocols for sending data to the computer. This ensures adaptability in data transfer and enables the probe to accommodate different measurement scenarios and environments. In the following paragraphs, a concise description of the three data transfer protocols, namely Wi-Fi, Bluetooth, and USB, is provided, along with their implementation in the firmware.

2.2.2.1 Wi-Fi data transfer

Wi-Fi is a wireless networking technology that allows devices such as computers, mobile devices, and other equipment to interface with the Internet allowing these devices to exchange information with one another, creating a network.
The ESP32 implements a TCP/IP and full 802.11 b/g/n Wi-Fi MAC protocol offering two operating modes, either in Station (STA) mode or in Access Point (AP) mode. When in Station mode, the microcontroller behaves like a device that connects to a router linked to the Internet, while in AP mode it behaves like a Wi-Fi network to which other devices can connect. Regardless of the Wi-Fi operating mode, a simple and reliable solution for communication between the computer and the microcontroller is the use of a TCP/IP socket application.
The designed firmware sets the microcontroller in AP mode with a user-defined SSID (ESP_WIFI_SSID), password (ESP_WIFI_PASS), and the computer connects to it. The code necessary for the Wi-Fi connection configuration and initialization on the ESP32 is presented at the beginning of the following page.
A socket is an abstraction through which an application may send and receive data allowing it to plug into a network (hence the name *socket*) and communicate with other applications that are plugged into the same network. There are distinct types of sockets corresponding to different underlying protocol suites and different stacks of protocols within a suite, as it is the TCP/IP protocol suite [41].

```
void wifi_init_softap(void) {
    ESP_ERROR_CHECK(esp_netif_init());
    ESP_ERROR_CHECK(esp_event_loop_create_default());
    esp_netif_create_default_wifi_ap();
    wifi_init_config_t cfg = WIFI_INIT_CONFIG_DEFAULT();
    ESP_ERROR_CHECK(esp_wifi_init(&cfg));
    ESP_ERROR_CHECK(esp_event_handler_register(
            WIFI_EVENT,ESP_EVENT_ANY_ID,&wifi_event_handler,NULL));
    wifi_config_t wifi_config = {
        .ap = {
            .ssid = ESP_WIFI_SSID,
            .ssid_len = strlen(ESP_WIFI_SSID),
            .channel = ESP_WIFI_CHANNEL,
            .password = ESP_WIFI_PASS,
            .max_connection = MAX_STA_CONN,
            .authmode = WIFI_AUTH_WPA_WPA2_PSK    },   };
    ESP_ERROR_CHECK(esp_wifi_set_mode(WIFI_MODE_AP));
    ESP_ERROR_CHECK(esp_wifi_set_config(ESP_IF_WIFI_AP, &wifi_config));
    ESP_ERROR_CHECK(esp_wifi_start());  }
```

The TCP/IP protocol suite, also known as the Internet Protocol (IP) suite, is a collection of different communication protocols designed to solve different sets of problems, in particular how data should be packetized, addressed, transmitted, routed, and received. It is organized into four abstract layers, (Application, Transport, Internet, Link Layer), each of them performing particular tasks. Transmission Control Protocol (TCP) is a transport protocol used on top of the IP that ensures reliable packet transmission. It is designed to detect and recover from losses, and identify other errors that may occur in the host-to-host channel provided by the IP. It is a connection-oriented protocol, meaning a connection is established before communication, involving an exchange of handshake messages between the TCP implementations on the two communicating devices. Another transport protocol is the User Datagram Protocol (UDP) which uses connectionless communication with no control over losses and other errors.
A TCP/IP socket is uniquely identified by an Internet address, an end-to-end protocol, and a port number. The one that originates the communication is called the client program, while the other side that responds to the originator's contact is called the server program. Initially, before the connection is established there is an important distinction between client and server: it is the client, at the beginning, that needs to know the server address and port. Afterward, there is no difference between the server and the client, which together compose the application. The types of sockets in TCP/IP which use TCP as the end-to-end protocol, therefore providing a reliable byte-stream service, are known as *stream sockets* while the ones which use UDP are known as *datagram sockets*.

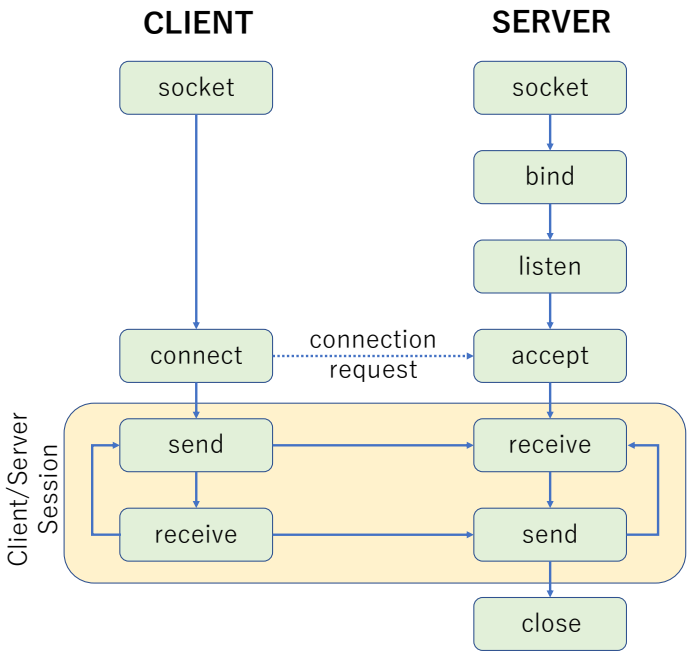


Figure 2.12. Socket Programming diagram.

After configuring the Wi-Fi connection, attention can be directed towards establishing the socket connection between the devices. The ESP32 is configured as the server that initiates the socket connection based on TCP protocol to guarantee reliable communication. The server sets up a communication endpoint and passively waits for a connection from the client. The computer, connected to the same network as the embedded device, acts as a client who connects to the server, thus establishing the connection. Data is sent and received as strings.
Figure 2.12 shows the general steps that must be followed for communication between the devices. The details of the connection steps are described in the following, along with the corresponding code inside the firmware.

- Create the socket by defining:
  - the type of communication (TCP or UDP)
  - the communication domain (IPv4, IPv6 or local)
  - the protocol (IP)

```
int sock = socket(AF_INET, SOCK_STREAM, IPPROTO_TCP);
```

- Assign a port number to the socket

```
#define S_PORT 3333
```

- Bind the socket (definition and port number)

```
struct sockaddr_in serverAddress;
serverAddress.sin_family = AF_INET;
serverAddress.sin_addr.s_addr = htonl(INADDR_ANY);
serverAddress.sin_port = htons(S_PORT);
int rc = bind(sock, (struct sockaddr *)&serverAddress,
        sizeof(serverAddress));
```

- Allow connections through that port, i.e., listen or wait for a client to connect

```
rc = listen(sock, 5);
```

- Accept the connection request establishing the connection. The client and server are now connected, and data can be exchanged bidirectionally.

```
struct sockaddr_in clientAddress;
socklen_t clientAddressLength = sizeof(clientAddress);
int clientSock = accept(sock, (struct sockaddr *)&clientAddress,
        &clientAddressLength);
char arrayNum[9];
char countString[50];
recv(socket, &arrayNum,sizeof(arrayNum),0);
send(socket, countString, strlen(countString), 0);
```

- Close the connection if data transfer is completed.

```
close(socket);
```

On the client side the stages of the setup are:

- create the socket (the same as for the server)
- connect to the server, data can be exchanged bidirectionally

Multiple options can be used on the PC to read sockets such as C, C++, Python programs, MATLAB environment, etc. In the following sections, further detail will be given about the computer programs used for receiving data coming from the microcontroller.

2.2.2.2 Bluetooth data transfer

Bluetooth is a wireless data protocol that connects devices over a short distance, from 1 to 100 meters, depending on the strength of the radio. Most Bluetooth devices operate up to a maximum of 10 meters to improve battery life, reducing the strength of the radio, and therefore saving power [42].
The ESP32 is capable of supporting Bluetooth protocols compliant with Bluetooth v4.2 Basic Rate (BR), Enhanced Data Rate (EDR), and Bluetooth Low Energy (BLE) specifications. To take advantage of its power management capabilities, the microcontroller was used in BLE mode. The firmware design uses the open-source BLE stack Apache Mynewt, specifically the NimBLE stack, which is fully compliant with Bluetooth specifications [43].
A BLE device can communicate with other devices in two ways [44].

- Broadcasting, which defines two separate roles:
  - broadcaster, sends connectionless advertising packets periodically to anyone ready to receive
  - observer, repetitively scans to receive any advertising packets currently being broadcasted.
- Connections are permanent, and periodical data exchange takes place between two devices. They distinguish between two separate roles:
  - peripheral (slave), sends connectable advertising packets periodically and accepts incoming connections, and exchanges data regularly;
  - central (master), continuously scans for connectable advertising packets and initiates a connection managing the timing of the periodical data exchange.

Broadcasting can be useful when a small amount of data is to be sent to multiple devices because it is fast and easy to use, but no security or privacy is guaranteed. Instead, connections are private and allow data transfer in both directions. In the developed firmware, connections are used and the PC is the central while the ESP32 is the peripheral.
As for the TCP/IP suite, Bluetooth also is described by a *stack* which refers to a collection of device drivers, development libraries, and user-level tools provided by the Bluetooth SIG organization [45]. This protocol stack is divided

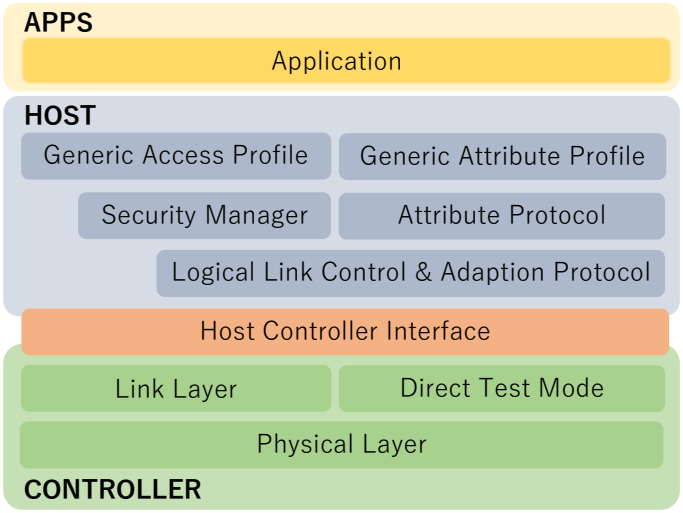


Figure 2.13. The BLE stack.

into three parts: controller, host, and application, as shown in Figure 2.13. Bluetooth BR, Bluetooth EDR, and Bluetooth LE, all separate the controller and host as different layers and are often implemented separately. The user application and operating system sit on top of the host layer.
From its foundation, a clear separation between protocols and profiles was introduced. Protocols are defined as the layers that implement the rules for packet formats, routing, and multiplexing that permit data to be sent effectively between peers. Profiles are considered functionalities that define how protocols should be used to achieve a particular goal [44]. There are profiles for remote controls, images, printers, cordless telephones, health devices, and hands-free devices [46].
The host control interface (HCI) layer provides communication between the host and controller via a standardized interface. Standard HCI commands and events are specified in the Bluetooth Core Spec. The HCI layer is a thin layer that transports commands and events between the host and controller.

```
ESP_ERROR_CHECK(esp_nimble_hci_and_controller_init());

nimble_port_init(); // Initialize the NimBLE host configuration
ble_hs_cfg.sync_cb = bleapix_on_sync;
ble_hs_cfg.reset_cb = bleapix_on_reset;
```

The link logical control and adaption protocol (L2CAP) layer provides data encapsulation services to the upper layers, allowing for logical end-to-end communication of data. The security manager (SM) layer defines the methods for

pairing and key distribution and provides functions for the other layers of the protocol stack to securely connect and exchange data with another device. The Generic Access Profile (GAP) handles connection and security, controlling how devices interact with each other at a lower level. GAP is configured inside the firmware to set up and initiate advertisement, and to connect the microcontroller to a computer.

```
ble_svc_gap_init();
```

The first step that the microcontroller must perform is to configure and start advertising.

```
struct ble_gap_adv_params adv_params;
memset(&adv_params, 0, sizeof(adv_params));
adv_params.conn_mode = BLE_GAP_CONN_MODE_UND;
adv_params.disc_mode = BLE_GAP_DISC_MODE_GEN;
rc = ble_gap_adv_start(ble_apix_addr_type, NULL, BLE_HS_FOREVER,
                       &adv_params, bleapix_gap_event, NULL);
```

In advertisement mode the device sends out periodic notifications of its existence and its willingness to connect. Another device, such as a computer or a smartphone, scans the area for possible devices. If this is the desired embedded device, the computer can request a connection. If the advertiser accepts, both devices enter a connected phase, where the embedded device will be the slave, and the initiator becomes the master.
The attribute protocol (ATT) allows a device to expose attributes to other devices. The Generic Attribute Profile (GATT) builds on the ATT and adds a hierarchy and data abstraction model on top of it, defining generic data objects that can be used by a variety of application profiles. It provides the reference framework for all *GATT-based profiles*, which covers precise use cases and ensures interoperability between devices from different vendors [44]. All data communications that occur between two devices in a BLE connection are handled through the GATT profile.

```
void gatt_svr_init(void) {
    ble_svc_gatt_init();
    ble_gatts_count_cfg(gatt_svr_svcs);
    ble_gatts_add_svcs(gatt_svr_svcs);
}
```

As already mentioned in the previous section, the client-server paradigm is the dominant communication pattern for network protocols. In the same way

as for socket communication, for Bluetooth connection, the embedded system will be the server, and the computer will be the client. The client can request information from the server, or the client can send data to the server. GATT starts by defining the roles that the interacting devices can adopt, precisely client or server. Within the GATT profile, data is encapsulated in *services* which consist of one or more *characteristics*. Each characteristic includes user data along with descriptive information about it. It has a Universally Unique Identifier (UUID), a 128-bit (16-byte) number, which for BLE can be either 16-bit or 32-bit. The characteristic is the user or application data transmitted from one device to another across the network and a specific UUID is used within the network to identify a specific characteristic that travels across the network.
In summary, a characteristic is a container of user data that has different properties such as read, write, notify, or indicate. The client reads these properties and knows which operations are allowed on each characteristic.

```
static const struct ble_gatt_svc_def gatt_svr_svcs[] = {
    {   /* Service: APiX Measurement */
        .type = BLE_GATT_SVC_TYPE_PRIMARY,
        .uuid = BLE_UUID16_DECLARE(GATT_APIX_UUID),
        .characteristics = (struct ble_gatt_chr_def[])
        { { /* Characteristic: APiX measurement */
                .uuid = BLE_UUID16_DECLARE(GATT_APIX_MEASUREMENT_UUID),
                .access_cb = gatt_svr_chr_access_apix_meas,
                .val_handle = &hrs_apix_handle,
                .flags = BLE_GATT_CHR_F_NOTIFY, },  }   },
    {   /* Service: Device Information */
        .type = BLE_GATT_SVC_TYPE_PRIMARY,
        .uuid = BLE_UUID16_DECLARE(GATT_DEVICE_INFO_UUID),
        .characteristics = (struct ble_gatt_chr_def[])
        { { /* Characteristic: * Manufacturer name */
                .uuid = BLE_UUID16_DECLARE(GATT_MANUFACTURER_NAME_UUID),
                .access_cb = gatt_svr_chr_access_device_info,
                .flags = BLE_GATT_CHR_F_READ,
            }, {/* Characteristic: Model number string */
                .uuid = BLE_UUID16_DECLARE(GATT_MODEL_NUMBER_UUID),
                .access_cb = gatt_svr_chr_access_device_info,
                .flags = BLE_GATT_CHR_F_READ,   },  }   },  };
```

When the client wishes to know the value of a characteristic, it will issue a *read indication* on the universally unique identifier (UUID) that specifies the desired characteristic. The server will respond with the value by returning a read confirmation. BLE features short data packets, up to 27 bytes, thus for large amounts of data, the response could be broken into multiple messages.
When the client wants to set the value of a characteristic, it sends a *write request* message to the server that includes the UUID of the characteristic

and the data to be written. The server then responds with a *write response* message to confirm that the write operation was successful.
When the client wishes to receive updates on a certain value in the server, it will issue a *subscribe request* that includes the UUID of the characteristic to be read. The server will respond with an acknowledgment, and then will stream data. This streaming could occur periodically, or it could occur whenever the value changes. In the designed firmware, notification messages are sent from server to client periodically. The client can request to start or stop receiving notifications from the server.

```
char countString[50];
om = ble_hs_mbuf_from_flat(countString, sizeof(countString));
rc = ble_gattc_notify_custom(conn_handle, hrs_apix_handle, om);
```

Various options can be used on the PC to read data sent from a Bluetooth device such as Python scripts, MATLAB environment, etc.

2.2.2.3 USB data transfer

A serial connection can be established between the computer and the ESP32 microcontroller using a USB-to-UART bridge. A terminal emulator on the computer can display data received from ESP32 as characters on the screen. The electrical circuit of the connection is shown in Figures 2.6 and 2.7. UART is also used to receive binary data used to flash the memory of the device to store new firmware to be executed. The serial connection based on the RS-485 standard also includes some control signals. In particular, two signals, RTS and DTR, if toggled perform the reset of the microcontroller causing the firmware to restart execution from the beginning.
The data transfer rate can be set manually between standard or custom baud rate values both on the microcontroller and the computer to the most suitable value for the kind of measurement performed. The limit is set by the CP2102 chip, whose maximum supportable baud rate is 921600 bit/s.

```
uart_set_baudrate(UART_NUM_0, 921600);
char countString[50];
printf("%s",countString);
```

USB data transfer was used when long and iterated characterization measurements were needed for a more reliable solution since no constraint of wireless communication is required for them. The baud rate used was in general 115200 bit/s. Only for specific fast data transmission baud rate was set to

Figure 2.14. A conceptual connection overview of the microcontroller as the interface between the sensor and the PC.

921600 bit/s. Several programs can be used on the computer for reading data coming from the serial port, such as ESP-IDF command prompt, Eclipse IDE, MATLAB, LabVIEW, Realterm, etc.

2.3 Data Acquisition Setup

Characterization measurements and data processing played a significant role in this research activity. Figure 2.14 illustrates the conceptual connection between the microcontroller, acting as an interface between the sensor and PC. The device was characterized by performing array readouts and storing data for various bias voltages or, equivalently, different excess voltages. An automatic setup was created within the MATLAB programming environment to control the power supply and read data from the microcontroller for the three distinct kinds of data transfer that were described in Section 2.2.2, save them to file, and plot heat maps and cumulative distribution curves of the arrays.
To properly characterize the chip, measurements were also performed inside a DY110C ACS climatic chamber, covering a nominal temperature range from -70°C to 180°C. An automatic setup that controls the climatic chamber, the power supply, and the microcontroller was developed in the LabVIEW programming environment. Data was sent via USB protocol and saved to files. The following sections provide an overview of the two developed frameworks.

2.3.1 MATLAB Environment

MATLAB is a multi-paradigm programming language and numeric computing environment that allows matrix manipulation, plotting of data, algorithm implementation, and device interfacing. It was widely used for characterization measurements performed at room temperature and for all the data processing and plotting. It is the main PC program that controls the power supply and the microcontroller.
The communication between the power supply was accomplished by employing a GPIB interface. The setup can be considered automatic because it proceeds

without any intervention from the user: as soon as a measurement is complete and data has been transferred from microcontroller to the PC, the bias voltage of the SPADs varies automatically within a specific user defined range.
When data are sent via USB, the *serialport* command is used, with the port name and the baud rate as arguments, to establish the connection between the ESP32 and the computer. Reading is performed using the *readline* command.
When data is sent via Wi-Fi, the computer (client) and the embedded device (server) must be connected to the same network in order to communicate with each other. The *tcpclient* command is used for socket connection specifying the server IP and the port number. Reading is performed using the *readline* command, the same as for the USB connection.
When communication is performed using Bluetooth, it is necessary to know the device address and the characteristic name and UUID that must be read from or written to. The computer acts as a central, or master, and scans for devices that are advertising. The two devices connect when the *ble* command specifying the Bluetooth peripheral device address is executed. Once the connection is established, the central chooses the characteristic that needs to be read. When the characteristic supports the *Notify* option, the master subscribes to that characteristic and the *read* command is used to get the latest data.
When the data transfer is completed and received data is written to files, for all the above protocols, the connection is closed by clearing the object assigned to it.

2.3.2 LabVIEW Environment

The LabVIEW graphical programming environment allows the creation of *Virtual Instruments* (VI) where functional blocks can be placed and connected together, while the execution order is determined by the flow of data through the interconnected lines between the blocks.
As already mentioned, for a complete characterization in terms of temperature, a full set of measurements were performed in a DY110C ACS climatic chamber, within a temperature range from -40°C to 70°C. The PC drives and controls the climatic chamber, the power supply, and the microcontroller.
The communication between the PC and both the power supply and the microcontroller is achieved by means of the USB protocol and the Virtual Instrument Software Architecture (VISA) API.
An Ethernet connection and the manufacturer's developed libraries are used to establish communication between the computer and the climatic chamber. The temperature is automatically set within a specific user-defined range, and a control is performed to ensure that the temperature inside the climatic chamber stays within the manufacturer tolerance range. Once the setpoint

temperature is reached, the characterization of the SPADs at the given temperature begins. Readouts and data transfer are performed continuously at different bias voltages, as specified by the user-defined interval. The resulting data is saved into files.

Chapter 3

Characterization campaign

Characterizing the APIX2LF chip is essential to understand its properties and sensitivity in dark conditions, enabling optimization of its performance in charged particle detection for medical imaging and other applications. By means of a thorough characterization, various aspects of DCR can be analyzed, such as susceptibility to crosstalk or the presence of random telegraph signal contributions. Understanding how these parameters vary with operating conditions can help optimize chip performance for specific applications, identify weaknesses for future improvements, and push the boundaries of CMOS SPAD array technology.
The first section of the chapter outlines the set of performed measurements with a brief overview of the chips that were tested.
The starting point in the characterization of a sensor is determining its breakdown voltage, i.e., the voltage at which the sensor transitions from off to on state. It typically depends on the geometry, material, and doping layers of the device. An accurate characterization of the breakdown voltage is essential for optimal sensor performance, as the choice of the operating voltage, and in particular of the excess voltage, affects the device sensitivity and its noise performance. The second section of the chapter presents the results of the breakdown voltage extraction for four single-layer and two dual-layer chips.
After the breakdown voltage, the next key parameter to characterize is the dark count rate, which is an important parameter for SPAD detectors. This is especially true for devices produced using standard CMOS technology, which may exhibit higher DCR values than those produced using custom technologies.
The remainder of this chapter presents the results of the DCR characterization, including the effects of bias voltage and temperature on DCR. Additionally, specific measurements were performed to investigate how crosstalk phenomena affect the sensor performance. The impact of Random Telegraph Signal

on the DCR was analyzed, including its behavior under different bias voltage and temperature conditions to gain insight into its effect on the device performance.
Within the research group, breakdown voltage was extracted for three single-layer chips and DCR was characterized as a function of the bias voltage for one dual-layer chip. All measurements were performed at room temperature. This work aims to conduct a more comprehensive characterization campaign on four single-layer and two dual-layer chips.

3.1 Measurement procedure

As described in Section 1.4, for characterization purposes, both single-layer and dual-layer chips were bonded in a commercial package. Two characterization boards were developed for device testing [19]. The characterization measurements presented in this chapter were all obtained under dark conditions. The ESP32 microcontroller was used to write and read signals from the sensor, as well as preprocess and send data via USB protocol to the computer. As previously described in Section 2.3, for measurements conducted at room temperature, data acquisition was completed in the MATLAB environment, while for measurements performed inside the climatic chamber, data were acquired using the LABView environment.
Table 3.1 lists the chips that were characterized and the corresponding labels that will be used to refer to them in the reminder of this manuscript. In total, there are six APIX2LF chips, comprising of four single-layer chips (two FATHERs and two SONs) and two dual-layer chips.
Every chip consists of four arrays with different pitches, sizes, signal storage, and quenching circuit topology, as explained in Section 1.3.1. Although measurements were performed for arrays 1, 3, and 4, only results of arrays 1 and 3 will be presented since their results are more significant.
As described in Section 2.2.1, several firmware versions were developed for conducting various types of measurements. Essentially, there is a fundamental distinction between them: measurements in which one pixel at a time is enabled, and measurements in which all pixels are enabled simultaneously.
To characterize the sensor, continuous readout is performed, allowing the SPADs to detect for a specific time frame as described in Sections 1.3.4 and

FATHER	F2	F3
SON	S1	S2
Dual	D1	D2

Table 3.1. Devices under test.

2.2.1. This procedure is iterated a certain number **N** of times to obtain a total integration time, hence the rate in Hertz. The choice of the time frame Δt is very important since it determines the maximum DCR that can be detected,

$$DCR_{MAX} = \frac{N}{N\Delta t} = \frac{1}{\Delta t} \tag{3.1}$$

and the minimum DCR that can be detected

$$DCR_{MIN} = \frac{1}{N\Delta t} \tag{3.2}$$

Considering that the dark count rate of a single-layer chip at room temperature is in the order of few kHz, a time frame of 10 µs was chosen, as stated in [24]. The number of iterations **N** used is 100000, resulting in an equivalent total integration time (TIT) of 1 s, unless otherwise specified. The maximum rate that can be measured is 100 kHz as per (3.1), while the minimum rate is 1 Hz as per (3.2).
For a dual-layer chip, which has a dark count rate in the order of few Hertz at room temperature, a time frame of 100 µs was chosen. The number of iterations (**N**) varied between 100000 and 300000, resulting in a total integration time of 10 s or 30 s, respectively, depending on the measurement type. The maximum rate that can be measured is 10 kHz as per (3.1), while the minimum rate is 1 Hz, or 33 mHz as per (3.2), depending on **N**.
Referring to Figure 1.11, the voltage applied to the gate of the transistors performing the quenching and clamping operations are $V_Q = 0.9\ V$ and $V_{CLAMP} = 1.8\ V$, respectively. The maximum overvoltage that can be applied is set by the clamping transistor connected to the anode of the SPAD sensor which is 3.3 V. Unless otherwise specified, the monostable duration was set to 2 ns, and parallel reading was enabled.

3.2 Breakdown voltage extraction

The breakdown voltage (V_{BD}) is a dominant parameter when an avalanche detector is employed since it determines the behavior of the photodiode. As described in Section 1.1, the detector works in a linear region if the bias voltage is kept below the breakdown voltage, being the output current proportional to the incoming light. If the diode is biased with a higher voltage than the breakdown voltage, even a single photon or a single charged particle can trigger an avalanche inside the device. Therefore, it is important to know the value of the breakdown voltage to properly bias the device in the desired operating region.
The breakdown voltage depends on the process used for device fabrication, the doping concentration, and the doping profile of the junction. Temperature

also significantly affects the breakdown voltage because it is responsible for the thermal vibration of the lattice atoms. For lower temperatures, the lattice thermal agitation is smaller, and the corresponding mean free path is longer so a free carrier traveling inside the junction has higher energy and is more likely to initiate impact ionization. Consequently, the breakdown voltage increases proportionally with temperature and its dependence can be considered linear according to

$$V_{BD} = V_{BD0}(1 + \beta \cdot \Delta T), \tag{3.3}$$

where V_{BD0} is the breakdown voltage at room temperature, ΔT is the temperature variation and β is the breakdown voltage temperature coefficient, which depends on the fabrication process and for silicon is generally in the order of $10^{-3}\,°C^{-1}$ [47].
Another important parameter concerning the breakdown voltage is its uniformity inside an array of SPADs like the APIX2LF chip, considering that the cathodes are common to all the devices and, therefore, the same bias voltage is applied to all the pixels. If the breakdown voltage is not acceptably uniform in the whole array, SPADs in different regions of the chip will present different sensitivity and DCR. High doping levels achieved thanks to the evolution of fabrication technologies enable low breakdown voltages, but yet, an increase in the dark count rate performance of the device is observed due to tunneling phenomena [48].
Premature edge breakdown (PEB) is an issue that concerns the breakdown voltage of a junction. Due to the non-uniform distribution of the electric field, corners and edges may be subjected to higher electric fields. As a result, there is a higher probability of triggering an avalanche there, rather than in the center of the multiplication region. To reduce this effect, a circular shape of the detector can be used. However, circular shapes may be forbidden in some CMOS processes [49]. The most commonly used techniques to prevent PEB are guard rings, such as shallow trench isolation and/or lowly doped regions at the periphery of the junction [1].
Since the anodes of the detectors are not reachable due to their co-integration with the readout circuits, direct measurement of the current is not possible, and current-voltage curves cannot be used to extract the breakdown voltage. Instead, the breakdown voltage for each SPAD was extracted from the dark count rate versus bias voltage curves, as described in [50].
Measurements for breakdown voltage extraction were performed enabling 9 pixels at a time using the "1-by-1" firmware. Taking into account the considerations outlined above, the breakdown voltage was determined for each pixel by subtracting $V_{DD}/2$ that corresponds to the threshold voltage of the first inverter of the chain shown in Figure 1.11, from the voltage at which the DCR vs VSPAD curve suddenly rises from zero, as described in [22].

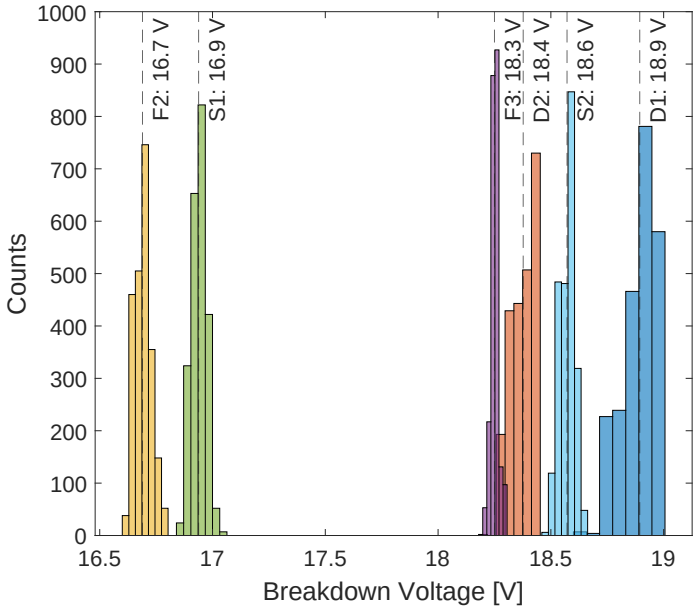


Figure 3.1. Average breakdown voltage distribution of array 1 (48×48 pixels) for D1, D2, F2, F3, S1, S2 chips. The measurements were performed at room temperature enabling one single SPAD at a time.

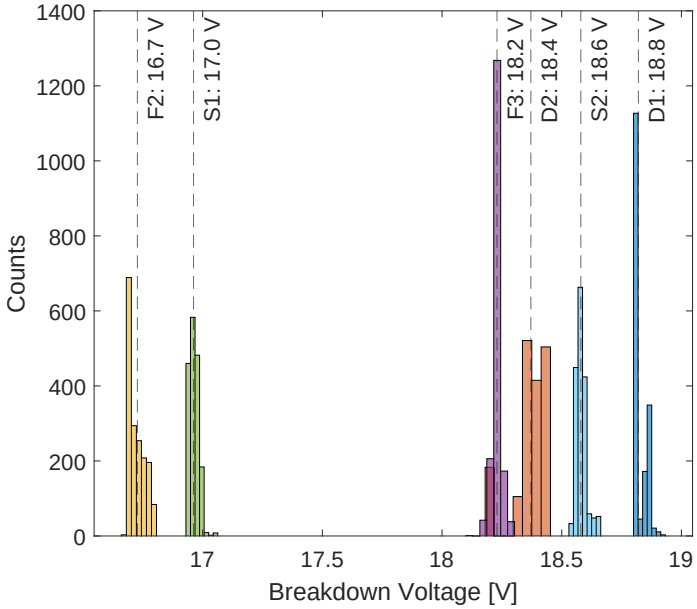


Figure 3.2. Average breakdown voltage distribution of array 3 (24×72 pixels) for D1, D2, F2, F3, S1, S2 chips. The measurements were performed at room temperature enabling one single SPAD at a time.

Depending on the breakdown voltage of each chip, measurements were performed on a 300 mV range with a resolution of 10 mV.
Figures 3.1 and 3.2 display the breakdown voltage distribution for the pixels in array 1 and array 3, respectively, for the six characterized chips, at room temperature. Table 3.2 also shows the average value and standard deviation of the distributions. The standard deviation of SPADs within the same array of single-layer chips, ranging from 20 to 38 mV, is comparable to that previously measured in SPADs with a similar structure and fabricated using the same technology as the devices tested in [21]. However, breakdown voltage values varied significantly among the different chips, ranging from 16.6 to 18.9 V. This difference may explain also the slightly higher standard deviation observed for the dual-layer chips, ranging between 30 and 77 mV.
To further investigate the behavior of the breakdown voltage, measurements for its extraction were performed at different temperatures, from -40°C to 70°C, within a climatic chamber for three single-layer chips, F2, S1, and S2.
Figures 3.3 and 3.4 show the mean breakdown voltage as a function of the temperature for array 1 and array 3, respectively. The breakdown voltage exhibits a linear dependence on temperature within the considered range, with a slope, i.e., temperature coefficient, between 15 and 18 mV/°C. This behavior is consistent with the physical mechanism of avalanche current. As the temperature increases, the carrier mean free path decreases, requiring a larger electric field to sustain the avalanche process. The observed temperature coefficient is compatible with an N-well doping level of a few $10^{16} cm^{-3}$ [51], which is considered reasonable for the SPAD device studied in this work.
Overall, these results provide valuable insights into the breakdown voltage characteristics of SPAD chips and their temperature dependence. Such information is important for understanding the performance of these devices in various applications.

	Array 1		Array 3	
Chip	Vbr [V]	σ[mV]	Vbr [V]	σ[mV]
D1	18.89	76.99	18.82	29.32
D2	18.38	54.86	18.37	71.14
F2	16.69	38.09	16.73	30.75
F3	18.25	19.48	18.23	20.93
S1	16.94	32.31	16.96	18.34
S2	18.57	35.35	18.58	23.56

Table 3.2. Mean breakdown voltage and its standard deviation for array 1 and array 3 of the measured chips.

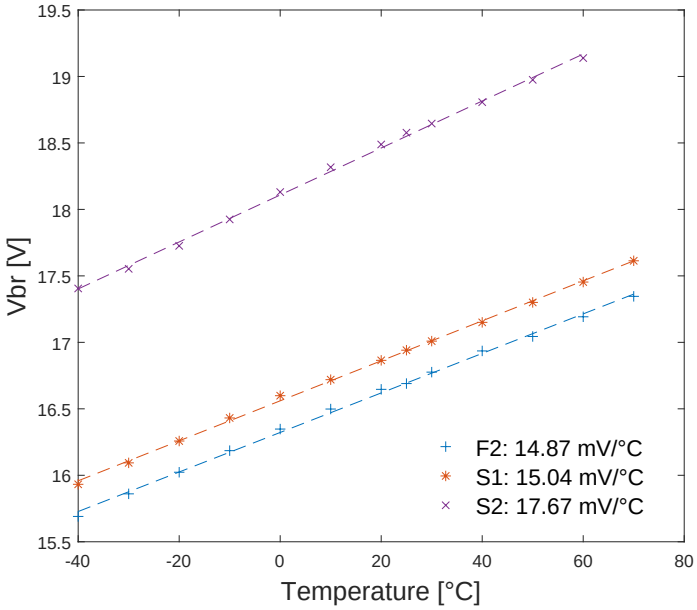


Figure 3.3. Average breakdown voltage as a function of temperature for array 1 (48×48 pixels) for F2, S1, S2 chips. The measurements were performed inside a climatic chamber enabling one single SPAD at a time.

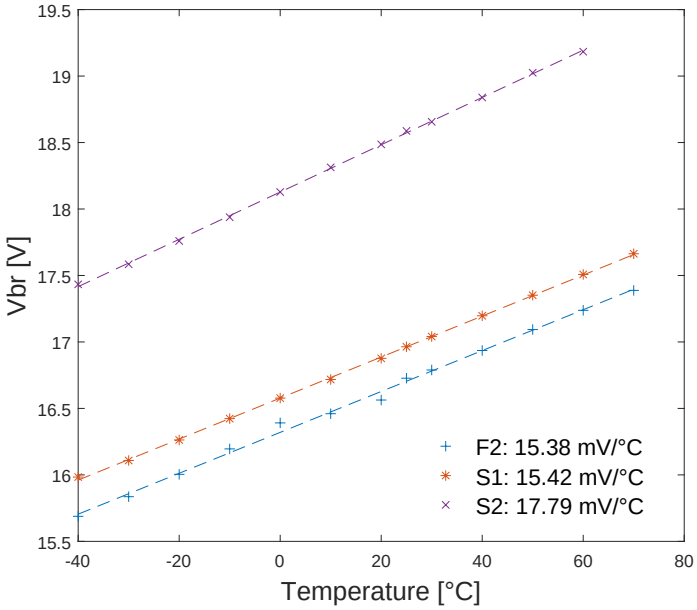


Figure 3.4. Average breakdown voltage as a function of temperature for array 3 (24×72 pixels) for F2, S1, S2 chips. The measurements were performed inside a climatic chamber enabling one single SPAD at a time.

3.3 Temperature effect on DCR

The following results are a subset of the measurements conducted on the DY110C ACS climatic chamber. F2, S1, and S2 chips were fully characterized in a temperature range from -40 to 70°C, while D1 and D2 were characterized from -40 to 50°C.
Figures 3.5 and 3.6 show cumulative curves of dark count rate distribution at different temperatures for SPADs of array 1 and 3 of chip F2 biased with 1.5 V of excess voltage. Similarly, Figures 3.7 and 3.8 display the DCR cumulative curves for array 1 and 3 of chip S2. As stated in Section 3.1, the maximum detectable rate is 100 kHz. However, to account for any lost counts that may occur during the defined time frame, the results were corrected using the assumption of a Poisson distribution of avalanche events, as described by the equation:

$$DCR = \frac{1}{\Delta t} \log \frac{1}{(1 - DCR_M \cdot \Delta t)}, \tag{3.4}$$

where Δt represents the time frame and DCR_M is the measured DCR.
As expected, for an increase of 10°C, dark count rate almost doubles as the temperature rises: the number of dark counts per second increases due to the fact that higher temperatures result in more thermal energy being available to the SPADs. Furthermore, as the temperature rises, more SPADs reach the

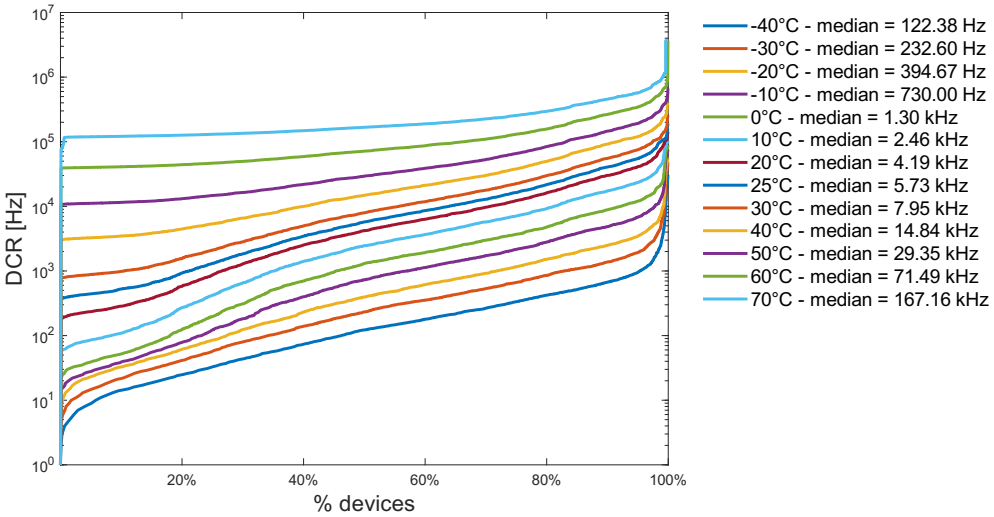


Figure 3.5. Cumulative curves for DCR of pixels in array 1 of F2 single-layer chip biased at 1.5 V excess voltage. The measurements were performed inside a climatic chamber.

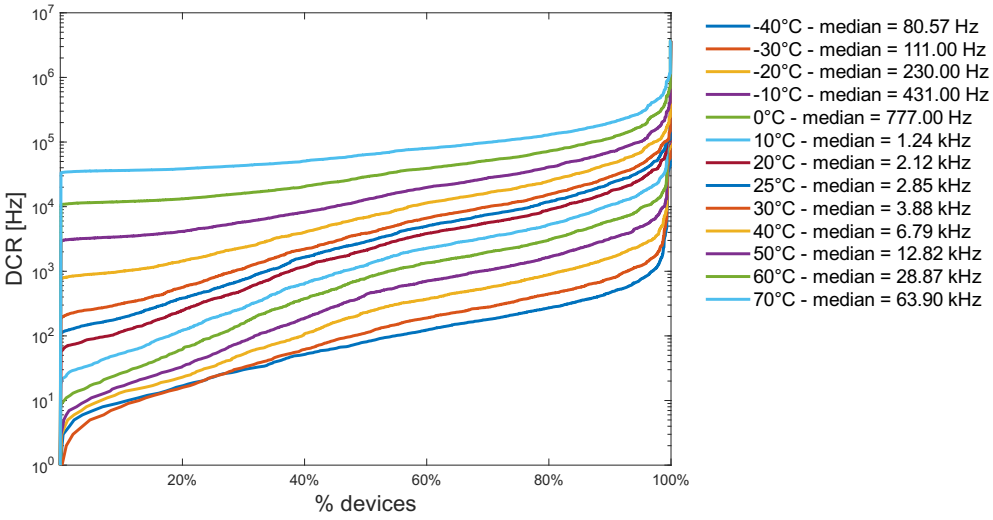


Figure 3.6. Cumulative curves for DCR of pixels in array 3 of F2 single-layer chip biased at 1.5 V excess voltage. The measurements were performed inside a climatic chamber.

maximum detectable rate of the measurement system, which is 100 kHz. This means that a larger proportion of SPADs are registering dark counts at the highest possible rate, indicating that the temperature is affecting the overall performance of the arrays. A more accurate measurement should be performed with a shorter detection frame for temperatures higher than 40°C to increase the highest detectable rate.
At 25°C, median value of DCR for array 1 of F2 is 5.6 kHz, while for chip S2 is 2.8 kHz. If the median value is normalized to the SPAD active area, which for array 1 is 70×52 μm^2, the resulting DCR values are 1.5 MHz/mm^2 and 769 kHz/mm^2, respectively. Equivalently, for SPADs of array 3, the median value of the DCR is 2.8 kHz for F2 chip and 1.8 kHz for S2 chip corresponding to 2.6 MHz/mm^2 and 1.7 MHz/mm^2, respectively, if normalized the median value to the SPAD active area, which for array 3 is 44×24 μm^2. By keeping the temperature lower than 0°C, rates lower than 1.5 kHz can be achieved.
Figures 3.9 and 3.10 display cumulative curves of DCR distribution at different temperatures for array 1 and array 3 of chip D1, respectively, while Figures 3.11 and 3.12 show results for array 1 and array 3 of chip D2, respectively. The SPADs were biased at 1.5 V of excess voltage and the lowest detectable rate corresponds to 33 mHz due to the 30 s integration time used in the measurements. The median value could not be calculated for temperatures below 20°C for array 1 of D1 and below 25°C for array 3, since less than 50% of the pixels exhibit dark count rate activity higher than the sensitivity. Additionally, at -20°C and -40°C, measurements were performed with a TIT

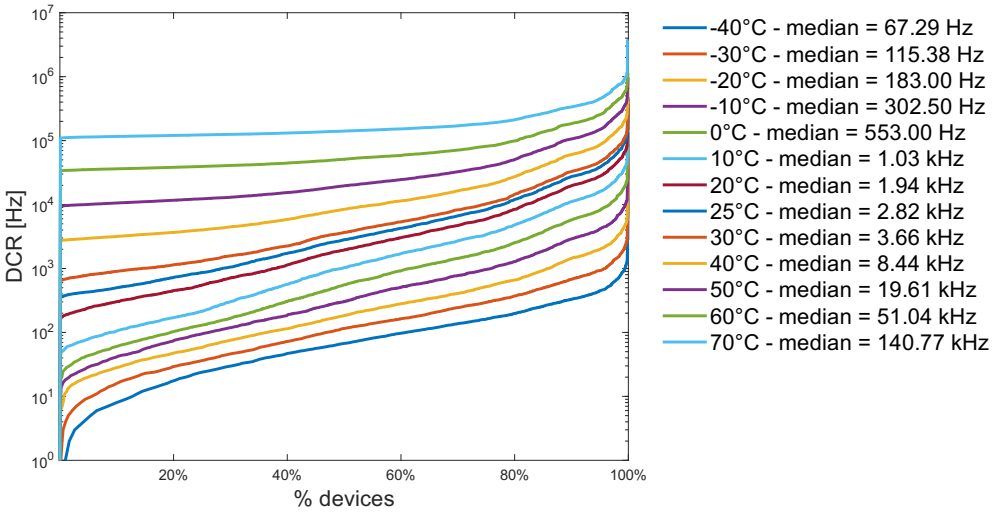


Figure 3.7. Cumulative curves for DCR of pixels in array 1 of S2 single-layer chip biased at 1.5 V excess voltage. The measurements were performed inside a climatic chamber.

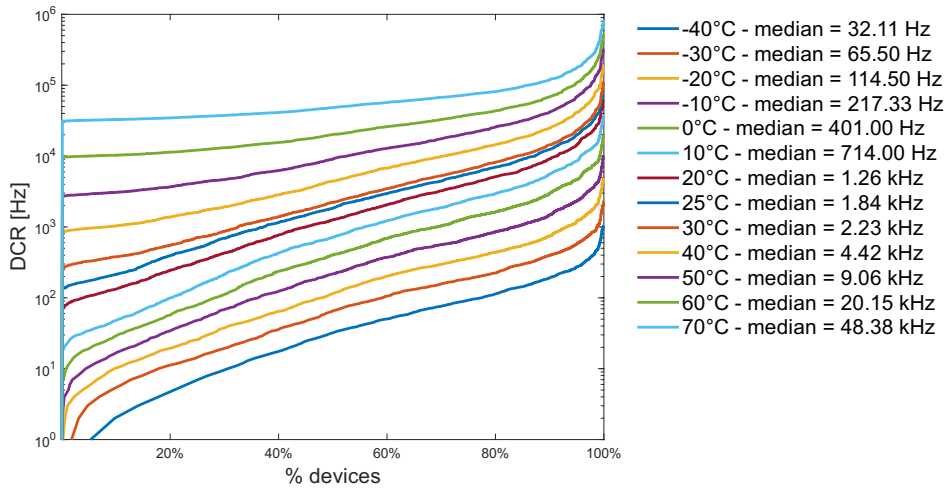


Figure 3.8. Cumulative curves for DCR of pixels in array 3 of S2 single-layer chip biased at 1.5 V excess voltage. The measurements were performed inside a climatic chamber.

of 90 s, lowering the sensitivity down to 1.1 mHz. However, for both D1 and D2, at -20°C, only 33% and 20% of the total pixels of array 1 and array 3, respectively, exhibit a higher DCR compared to the sensitivity, hence the median value could not be extracted in that case either.

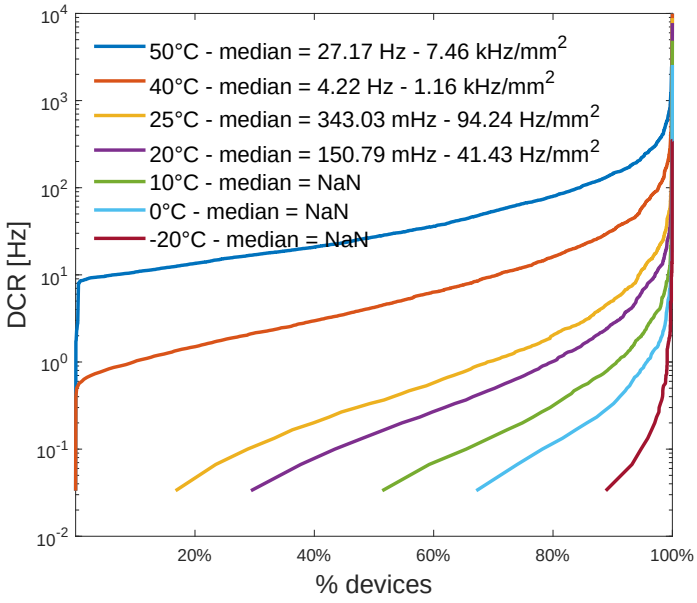


Figure 3.9. Cumulative curves for DCR of pixels in array 1 of D1 dual-layer chip biased at 1.5 V excess voltage. The measurements were performed inside a climatic chamber.

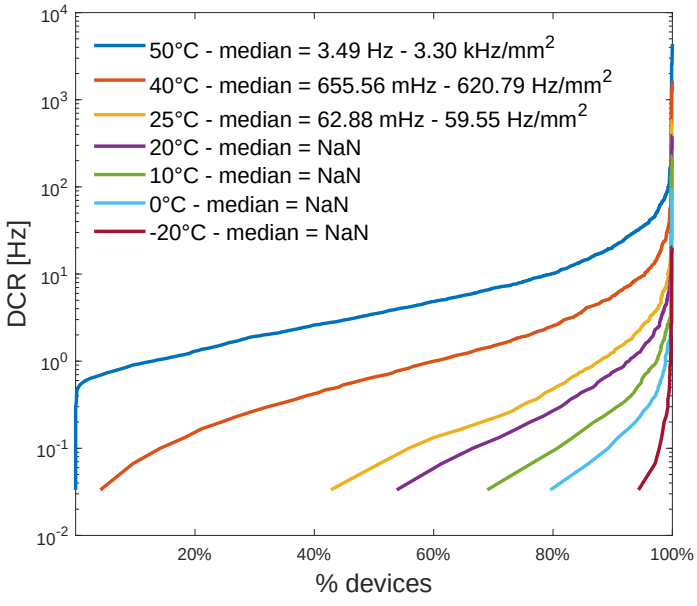


Figure 3.10. Cumulative curves for DCR of pixels in array 3 of D1 dual-layer chip biased at 1.5 V excess voltage. The measurements were performed inside a climatic chamber.

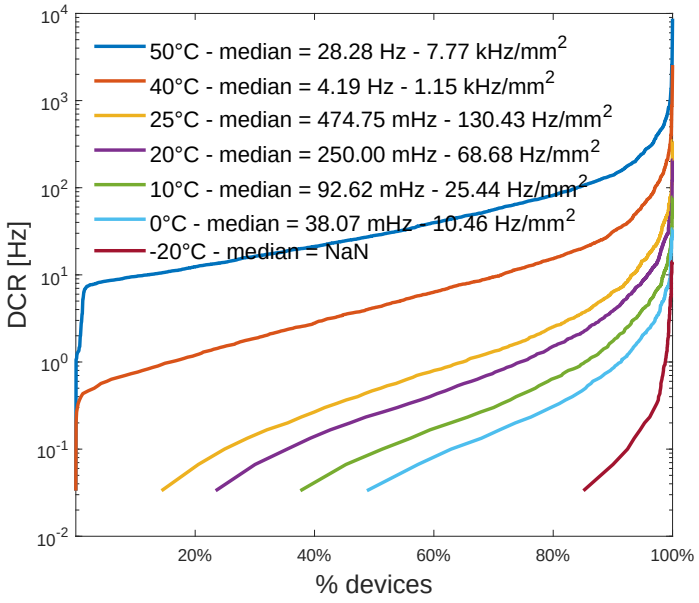


Figure 3.11. Cumulative curves for DCR of pixels in array 1 of D2 dual-layer chip biased at 1.5 V excess voltage. The measurements were performed inside a climatic chamber.

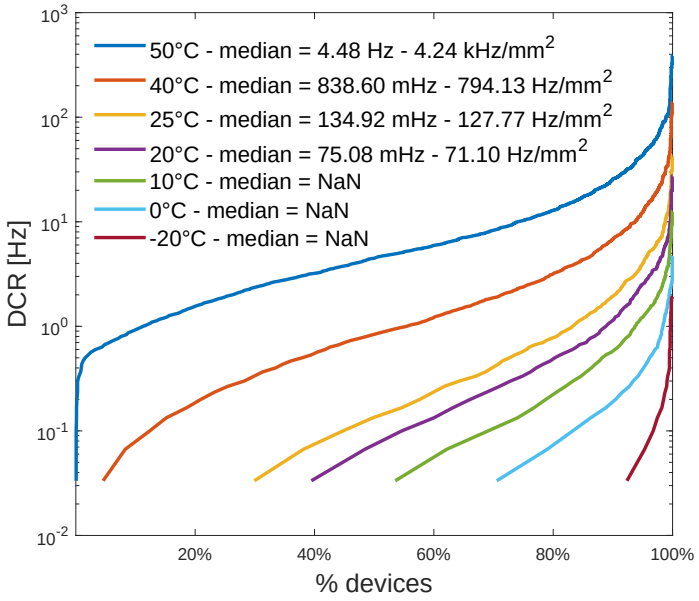
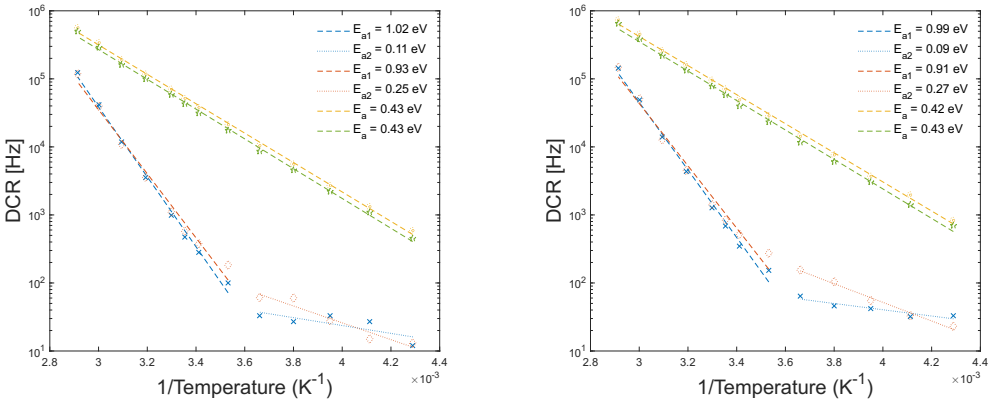


Figure 3.12. Cumulative curves for DCR of pixels in array 3 of D2 dual-layer chip biased at 1.5 V excess voltage. The measurements were performed inside a climatic chamber.

For array 1, at T = 25°C, the SPADs with DCR exceeding 10 Hz, (corresponding to 2.7 kHz/mm^2) are around 5% and 8% for D1 and D2 respectively. Similarly, for array 3, the SPADs with DCR exceeding 10 Hz, (corresponding to 9.5 kHz/ mm^2) are less than 1.5% for both D1 and D2 chips.
As the DCR in each layer doubles when the temperature increases by 10°C, this results in a fourfold increase in the coincidence dark count rate according to (1.1). However, for temperatures higher than 25°C, the temperature seems to affect the chips more significantly than at lower temperatures.
The Arrhenius equation provides a useful tool for modeling and predicting the temperature dependence of carrier generation and recombination processes of semiconductor detectors. As already explained in Chapter 1, in a semiconductor detector, ionizing radiation creates electron-hole pairs which can be detected as a current signal. This current signal depends on the number of electron-hole pairs created, which in turn depends on the energy of the incident radiation and the properties of the semiconductor material. However, the number of electron-hole pairs that recombine before they can be detected also depends on the temperature of the detector. The Arrhenius equation can be used to model the temperature dependence of the recombination process in the detector

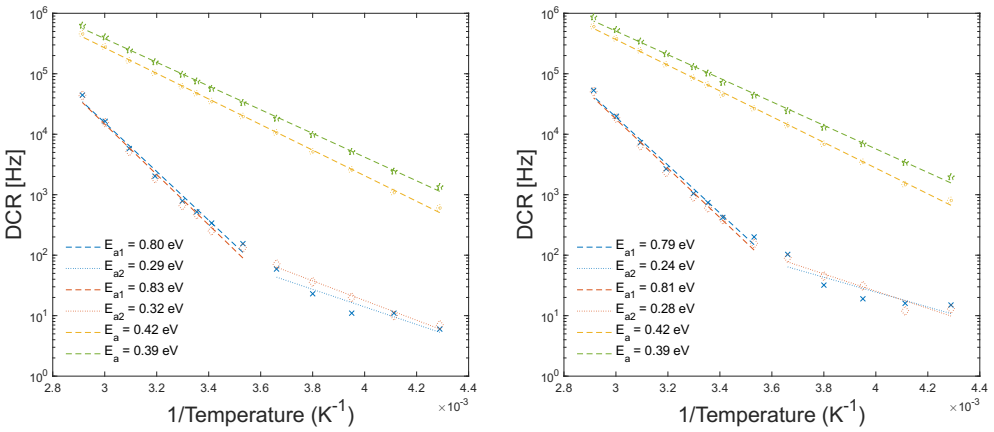
$$R = Ae^{-\frac{E_a}{k_B T}}, \tag{3.5}$$

where A represents the frequency of recombination events, E_a, i.e., the activation energy, represents the energy barrier that must be overcome for an electron-hole pair to recombine, T represents the temperature and k_B is the Boltzmann constant. The temperature dependence of the detector performance can be described by the rate constant R, which is proportional to the detector efficiency in detecting radiation. At higher temperatures, the rate constant increases, and the detector efficiency in detecting radiation may decrease due to increased recombination. Conversely, at lower temperatures, the rate constant decreases, and the detector efficiency may improve due to reduced recombination. Therefore, understanding the temperature dependence of a semiconductor detector performance is critical for optimizing its operation and obtaining accurate measurements.
The Arrhenius equation can be used to derive the activation energy and gain insights into the underlying mechanism for carrier generation inside the junction. The activation energy plays a crucial role in determining the dominant carrier transport mechanism in a semiconductor by comparing it to the silicon bandgap energy E_g.
Figures 3.13 and 3.14 show the Arrhenius plot, i.e., the logarithm of the DCR as a function of the reciprocal of the temperature expressed in Kelvin for four selected SPADs of array 1 and array 3, respectively, of the chip F2. The



(a) Vex = 1.5 V **(b)** Vex = 2 V

Figure 3.13. DCR as a function of the reciprocal of the temperature (Arrhenius plot) for a set of four SPADs of array 1 of chip F2.



(a) Vex = 1.5 V **(b)** Vex = 2 V

Figure 3.14. DCR as a function of the reciprocal of the temperature (Arrhenius plot) for a set of four SPADs of array 3 of chip F2.

activation energy for each pixel is shown in the legend, which is extracted interpolating DCR values measured at different temperatures with the Arrhenius equation. Pixels represented in green and yellow exhibit an activation energy smaller than $E_g/2$ indicating that trap-assisted tunneling is the dominant mechanism across the entire temperature range. For the other two pixels two mechanism can be distinguished: at low temperatures, below 0°C, the activation energy E_a is close to zero, suggesting that the primary mechanism is band-to-band tunneling, while at higher temperatures, where E_a is comparable to E_g, injection from the neutral region is the primary generation

mechanism [52], [53], [20]. Additionally, the excess voltage has a noticeable effect on the dark rate for temperatures lower than 0°C, while this effect is less significant at higher temperatures.

3.4 "AllON" and Crosstalk measurements

Single and dual layer chips were characterized at room temperature using the "AllON" measurement. All the SPADs are kept enabled during this measurement while the readout is carried out row by row as explained in Section 2.2.1.2. Figures 3.15 and 3.16 show the cumulative DCR distributions obtained from the characterization of array 1 in single and dual layer chips, respectively. The curves show the results for both measurements performed by enabling one pixel at a time and by enabling all pixels together. Similarly, Figures 3.17 and 3.18 show the cumulative DCR distribution for SPADs in array 3 of single and dual layer chips, respectively. All the SPADs are biased with 1.3 V of excess voltage, and a total integration time of 1 s and 30 s was used for single and dual-layer chips, respectively.
When measuring DCR at room temperature using the "AllON" method, it was observed that chip F2 had a higher DCR overall when all pixels were enabled compared to when pixels were enabled one by one, for both arrays 1 and 3 (Figures 3.15 and 3.17). The median value difference was around 1 decade. However, the other two single-layer chips, F3 and S2, showed less difference between the two measurement methods, with a difference of less than a factor of two. In the case of the dual-layer chips D1 and D2, a similar but more pronounced difference than in F2 was observed between the "1-by-1" and "AllON" curves for array 1, with a difference of 1 decade for D1 and almost 2 decades for D2. However, for array 3, the opposite difference was observed, with a difference of 2 decades for D1 and 1 decade for D2.
Additional analysis was conducted on the single-layer F2 chip to investigate how temperature might impact the "AllON" measurement. Tests were conducted within a climatic chamber, with temperatures ranging from -40°C to 25°C by enabling one pixel at a time ("1-by-1") and all at once ("AllON"). The results are presented in Figures 3.19 and 3.20 for array 1 and array 3, respectively.
The cumulative distribution curves of the dark count rate obtained from the "1-by-1" measurement showed a decrease in DCR with decreasing temperature. However, for the "AllON" measurement, the curves remained similar despite the decrease in temperature. Upon analyzing the heat maps of arrays 1 and 3, it was observed that certain pixels with a very high rate compared to the other pixels, called *Screamers*, were causing significant DCR degradation in the surrounding area due to optical crosstalk, as described in Section 1.1.5.

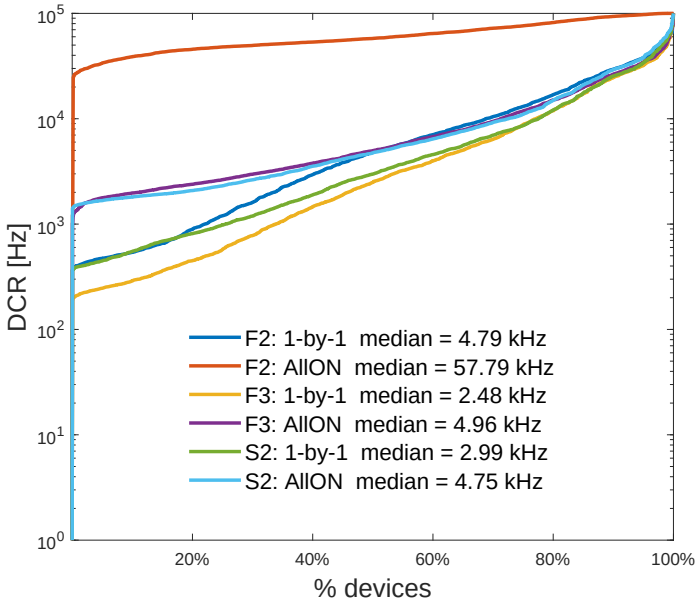


Figure 3.15. Cumulative curves for DCR of pixels in arrays 1 of F2, F3 and S2 single-layer chips biased at 1.3 V excess voltage. The measurements were performed at room temperature.

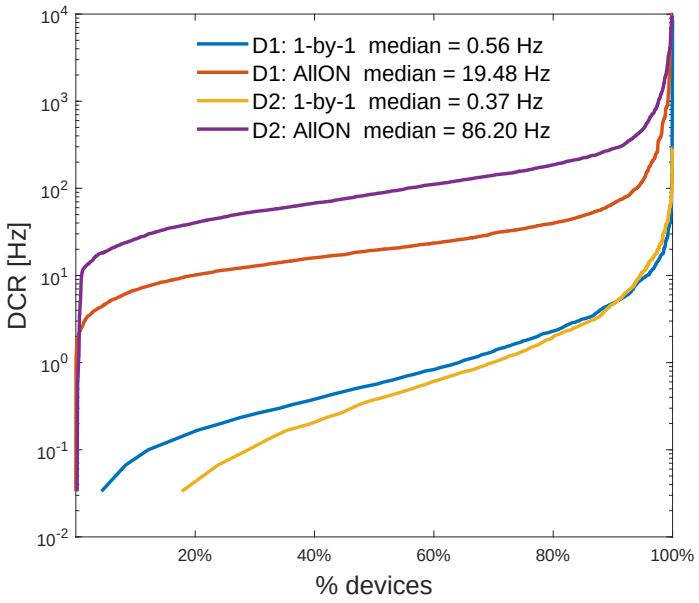


Figure 3.16. Cumulative curves for DCR of pixels in array 1 of D1 and D2 dual-layer chips biased at 1.3 V excess voltage. The measurements were performed at room temperature.

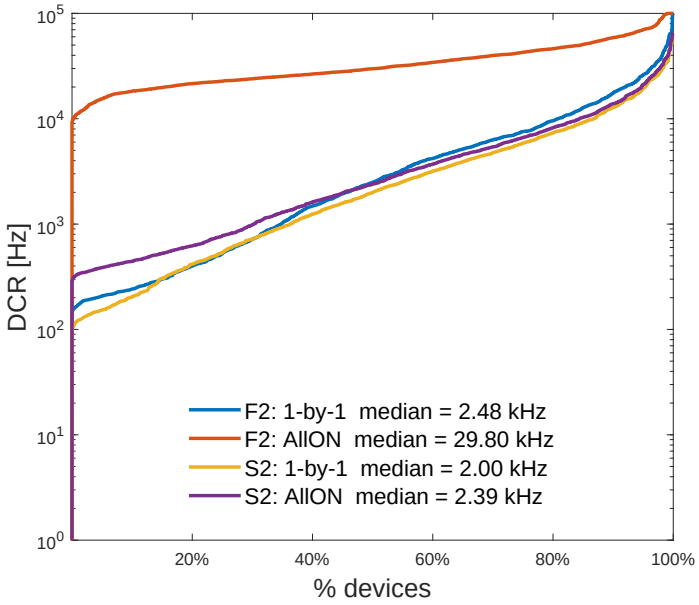


Figure 3.17. Cumulative curves for DCR of pixels in array 3 of F2 and S2 single-layer chips biased at 1.3 V excess voltage. The measurements were performed at room temperature.

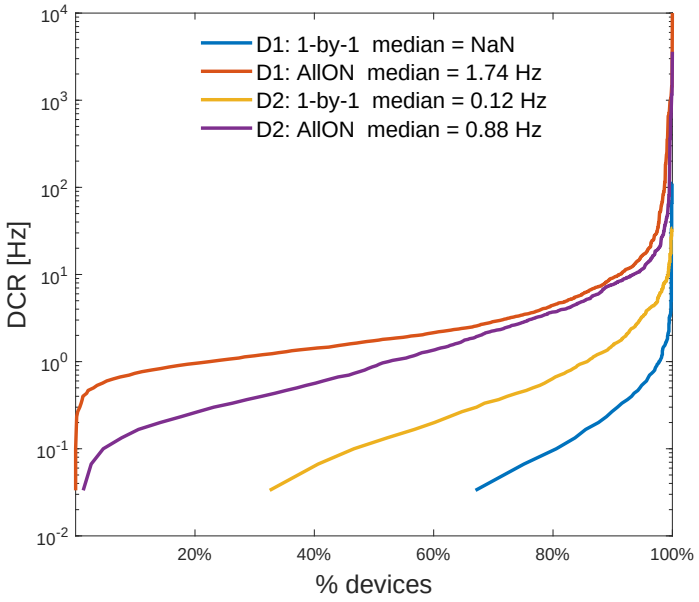


Figure 3.18. Cumulative curves for DCR of pixels in array 3 of D1 and D2 dual-layer chips biased at 1.3 V excess voltage. The measurements were performed at room temperature.

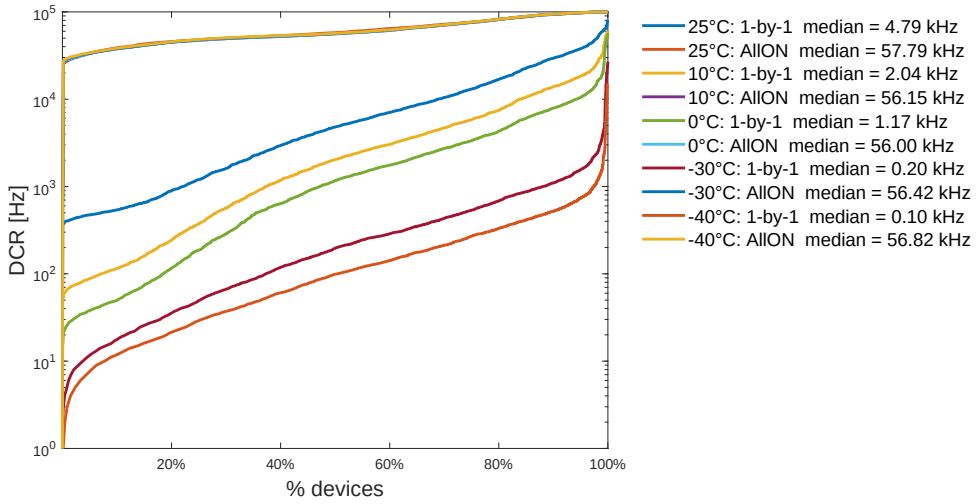


Figure 3.19. Cumulative curves for DCR of pixels in array 1 of the F2 single-layer chip biased at 1.3 V excess voltage. The measurements were performed at different temperatures inside a climatic chamber.

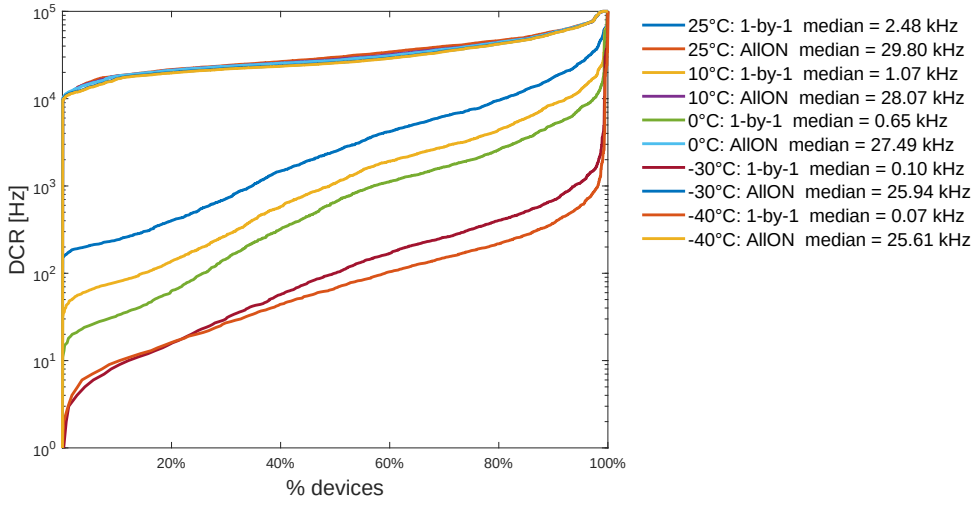


Figure 3.20. Cumulative curves for DCR of pixels in array 3 of the F2 single-layer chip biased at 1.3 V excess voltage. The measurements were performed at different temperatures inside a climatic chamber.

This phenomenon occurs when secondary photons emitted by SPADs during hot carrier relaxation are detected by other pixels in the array. Identifying and disabling these noisy pixels can be advantageous for reducing the global dark

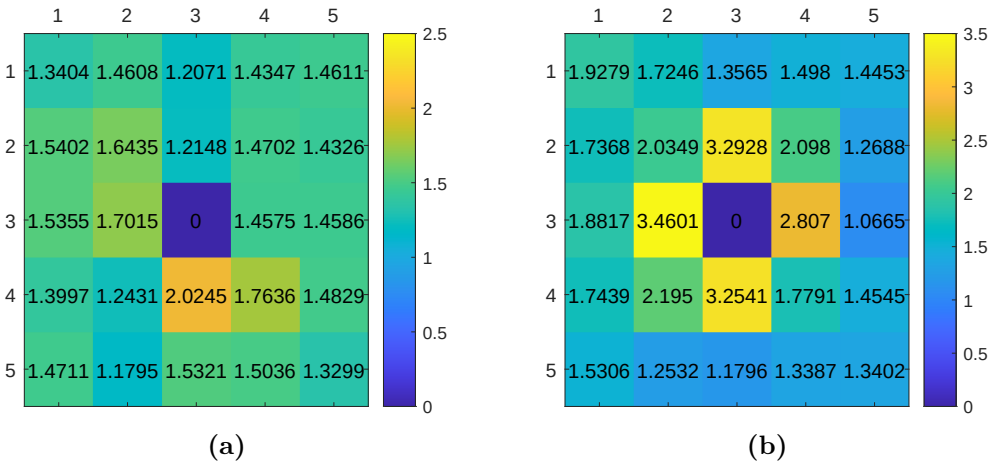
count rate of the detector [54], [55]. Crosstalk measurements, described in Section 2.2.1.3, were conducted with the high-DCR screamer pixels to observe its effect on neighboring pixels. As described in [56], the screamer pixel was used as the emitter of secondary photons, while 24 sorrounding SPADs are read out to detect the coincidence events. The crosstalk coefficient K was calculated as

$$K = \frac{CR_m - CR_t}{DCR_e + DCR_d} \tag{3.6}$$

where DCR_e and DCR_d are the dark count rates of the emitter and detector, respectively, CR_m represents the measured coincidence rate, and CR_t is the theoretical coincidence rate, obtained as:

$$CR_t = DCR_e \cdot DCR_d \cdot 2\Delta t, \tag{3.7}$$

with Δt the coincidence window, i.e., the width of the pulse coming from the monostable, which for these measurements is 2 ns.
Figure 3.21 shows the crosstalk coefficient map on a 5 × 5 subarray with the screamer pixel in the center, for array 1 (Figure 3.21a) and array 3 (Figure 3.21b). The effect of the screamer pixel on adjacent pixels is pronounced, while its effect decreases in the outer ring.
As described in [54], disabling screamer pixels can lead to a decrease in the dark count rate (DCR) of neighboring pixels. At -40°C and 25°C, the "AllON" measurement was performed again after disabling 15 pixels for array 1 and 10 pixels for array 3.
Figures 3.22 and 3.23 display the cumulative dark count rate distribution curves for the "1-by-1" measurement, the "AllON" measurement with screamers disabled, labeled in the legend as "PixOff", and the "AllON" measurement



(a) **(b)**

Figure 3.21. Crosstalk coefficient map of a *screamer* pixel for array 1 (a) and array 3 (b) of F2 chip.

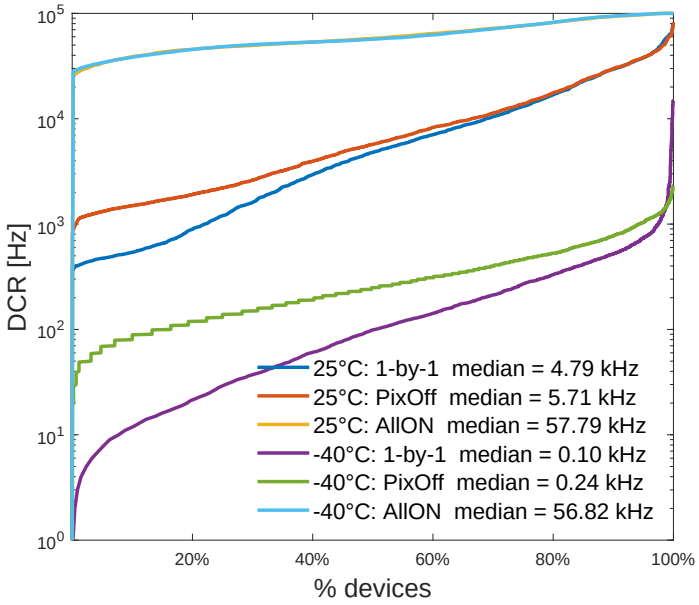


Figure 3.22. Cumulative curves for DCR of pixels in array 1 of the F2 single-layer chip biased at 1.3 V excess voltage. A specified number of very noisy pixels were disabled in the "PixOff" measurement. The two "AllON" measurements overlap with each other. The measurements were performed inside a climatic chamber.

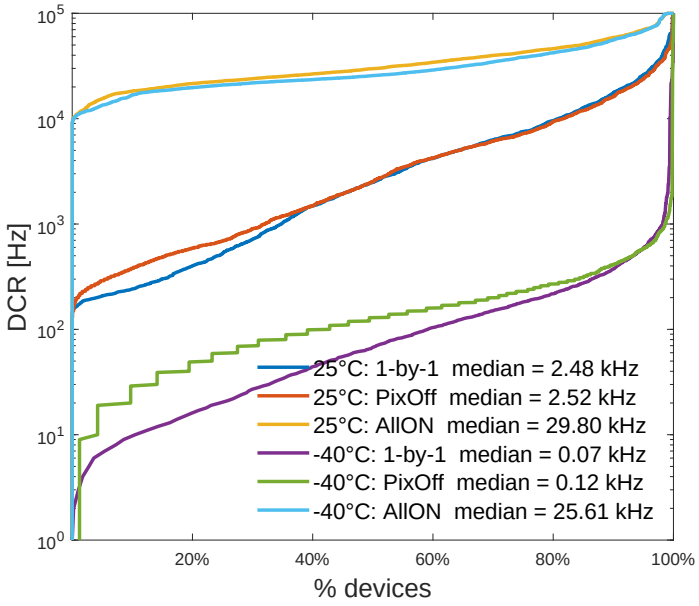


Figure 3.23. Cumulative curves for DCR of pixels in array 3 of F2 single-layer chips biased at 1.3 V excess voltage. A specified number of very noisy pixels were disabled in the "PixOff" measurement. The measurements were performed inside a climatic chamber.

with all the pixels enabled (including the screamers), for array 1 and 3, respectively, at temperatures of -40°C and 25°C. The "PixOff" measurement was carried out with the parallel readout disabled and with a TIT of 100 ms, the latter explaining the step behavior in the green curves.
The curves marked as "1-by-1" and "PixOff" display the expected DCR decrease with temperature decrease and they are very similar to each other. Therefore, disabling a few pixels, a significant decrease in the dark count rate activity of the sensor is obtained [55] [57].
The presented results suggest that *screamer* pixels can significantly impact the dark count rate of SPAD arrays. Disabling these pixels can result in a notable reduction in DCR. As these pixels make up less than 1% of the devices for both array 1 and array 3, disabling them does not significantly affect the spatial resolution. These observations have important implications for the designers of SPAD arrays employed in various applications, especially those requiring high sensitivity and low noise.

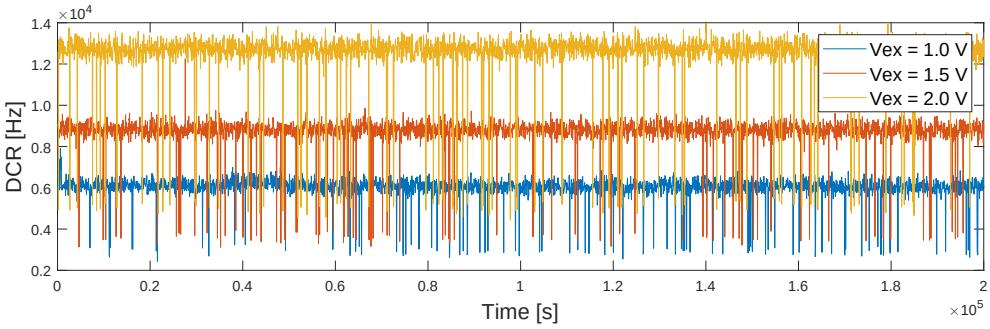
3.5 RTS Measurements

Defects within the bulk material or at interfaces present a major challenge for solid-state sensors with small areas. These defects occur during the manufacturing process, which includes steps such as etching or implantation. They can significantly degrade sensor performance by increasing the dark current, which can switch between two or more discrete levels, resulting in a phenomenon known as Random Telegraph Signal (RTS). This mechanism can have a significant impact on applications that require low and stable noise over long integration times, as it can cause calibration errors. Furthermore, RTS tends to increase in radiation environments, such as those encountered in space missions, nuclear physics experiments, or nuclear power plant monitoring. Both ionizing and non-ionizing radiation can create defects that increase the dark current and generate its associated random telegraph signal, thereby compromising the sensor performance. Therefore, understanding the fundamental mechanism can be helpful in designing strategies to mitigate its effects.
Despite the fact that the phenomenon of RTS was first observed many years ago, the underlying causes of RTS remain uncertain. There are several factors that can cause RTS, including bulk Shockley-Read-Hall (SRH) generation centers and defects at the silicon/oxide interface, which may or may not be associated with electric field enhancement [58], [59], [60]. RTS centers are metastable, and their discrete levels represent stable configurations where the center generates at a particular rate. If there is only one center in a pixel, the number of visible configurations is equal to the number of levels, and the amplitude differences between them indicate differences in the generation rates of

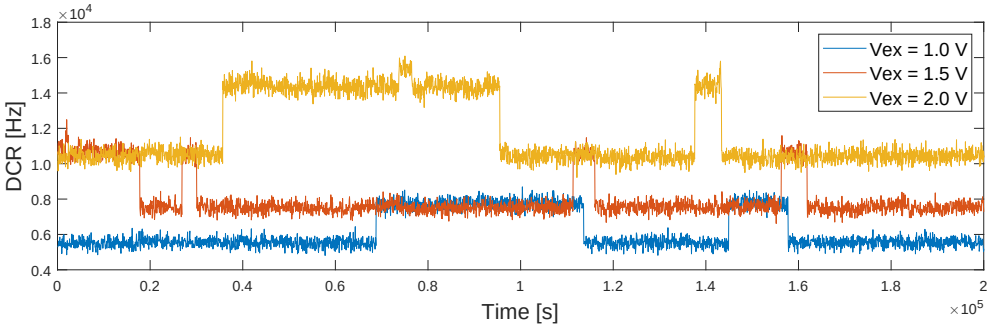
the center. Configuration stability can be determined by the time between two transitions, as centers that are more stable in a particular configuration will remain in it for a longer time [61]. Assuming that the state 1 represents the high level and the state 0 represents the low level, the times spent in states 0 and 1 are exponentially distributed, and the switching between the two states follows a Poisson process [62]. The capture time decreases with increasing bias voltage, because the current and the charge concentration increase, which increases the probability of capturing charge carriers in interface states. The emission time usually increases weakly because the surface potential is a logarithmic function of the current. Several theories link the discrete switching of the dark count rate to Flicker noise, also known as 1/f noise [63], [64].
In general, RTS events in SPADs can result from a superposition of several levels originating from multilevel sources, independent bi-level sources, or a combination of both [61]. The behavior of the majority of Random Telegraph Signals is highly complex because many devices exhibit multi-level RTS behavior. However, if the focus is on two-level RTSs, the following parameters can be used to characterize them:

- τ_{up}, which represents the average time spent in the high level;
- τ_{down}, which represents the average time spent in the low level;
- A_{RTS}, which is the amplitude of RTS switching between the high and low levels.

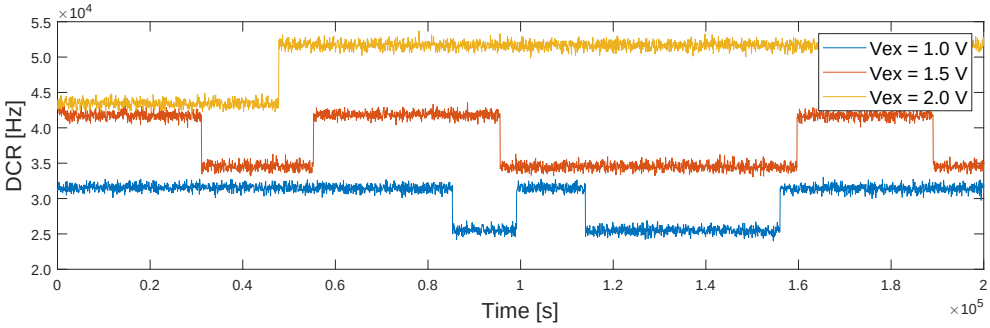
DCR was monitored over a time span of approximately four days in three single-layer chips, F2, S1, S2, inside a climatic chamber at 25°C. For each SPAD, DCR was acquired using the RTS firmware described in Section 2.2.1.4, with a time resolution of 62 seconds for array 1 (2304 SPADs) and 69.8 seconds for array 3 (1728 SPADs) for three different values of excess voltage Vex: 1 V, 1.5 V and 2 V. The following figures illustrate several types of RTS that have been observed in SPADs during characterization measurements.
Figure 3.24 shows the DCR as a function of time for four different pixels in array 1 of F2 chip. The time axis was limited for clarity to 2×10^5 s, though the entire measurement duration is around 3.5×10^5 s. Different behaviors can be observed: in Figure 3.24a two levels can be observed with fast transitions times, in the order of few minutes, while the other pixels (Figures 3.24b-d) show longer transition times, in the order of a few hours. In particular, the SPAD in Figure 3.24d, where three levels of RTS can be distinguished, exhibit the fast transition times when switching to the third level, while the other two levels have longer characteristic times. The average value of the difference between the two RTS DCR levels slightly increases with the SPAD excess volt-



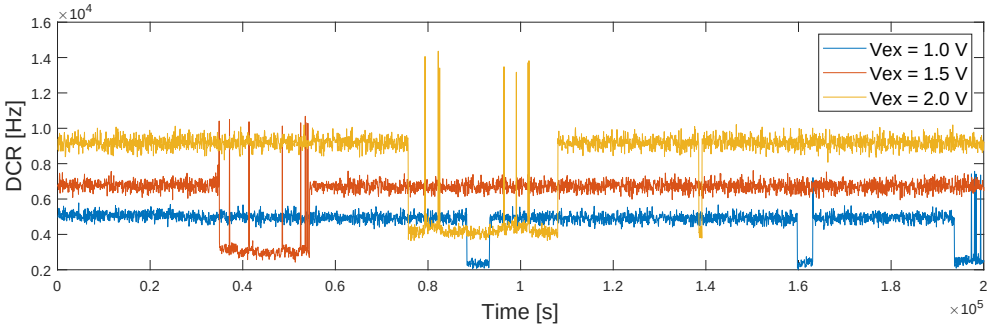
(a)



(b)



(c)



(d)

Figure 3.24. DCR vs time in pixels of array 1 exhibiting RTS behavior.

age, which is compatible with an increase in the avalanche-triggering probability resulting from the increasing field in the device junction. For the SPAD of Figure 3.24b, at 1 V and 1.5 V of excess voltage, the RTS shows a bi-level behavior, while at 2 V of excess voltage, a third level can be observed.
The number of levels can be distinguished more clearly from the histograms of the measured DCR, which are shown in Figure 3.25 for each of the SPADs shown in Figure 3.24, following the same order. In the case of a bi-level signal, each level corresponds to a Gaussian distribution, where the peak of the distribution corresponding to the mean value of the high and low levels of the RTS fluctuation. The separation between the two peaks represents the RTS amplitude. The presence, at each excess voltage, of a two-horned or multiply-horned distribution, confirms that the DCR is affected by a multi-level random telegraph signal fluctuation.
Similarly, Figure 3.26 displays the DCR over time for four different pixels in array 3 of the F2 chip, while Figure 3.27 displays the corresponding histograms

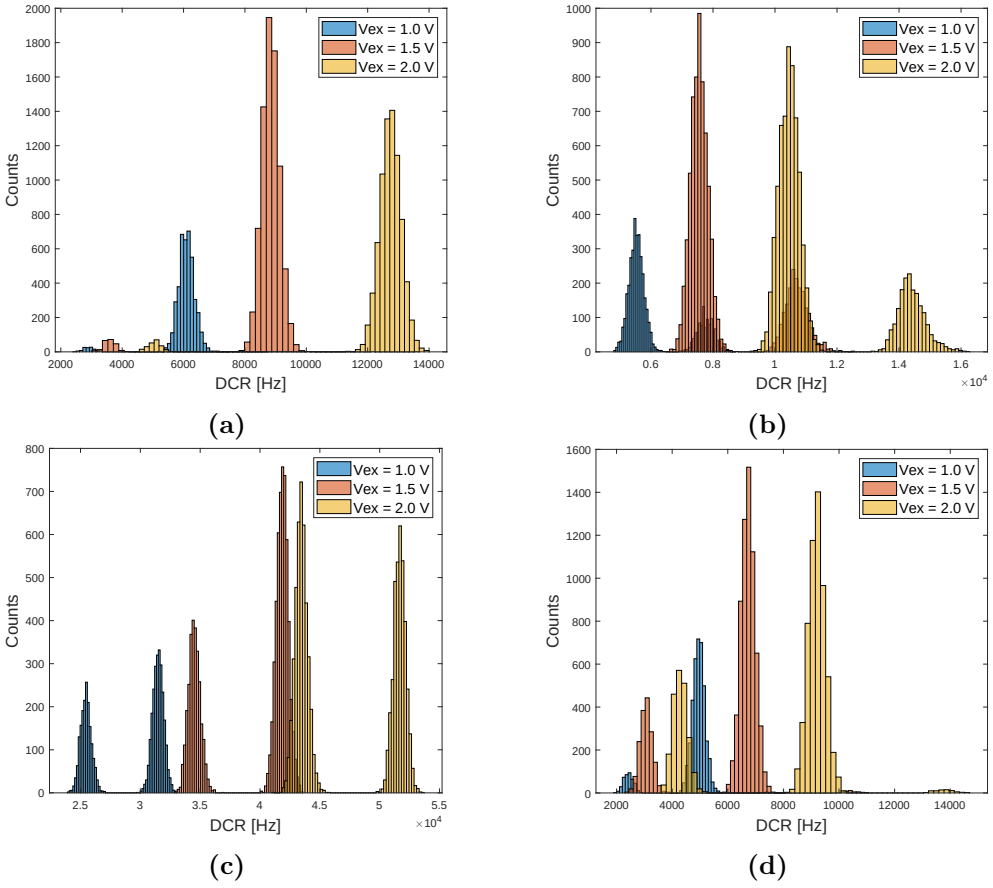


Figure 3.25. Amplitude distribution for pixels exhibiting RTS behavior.

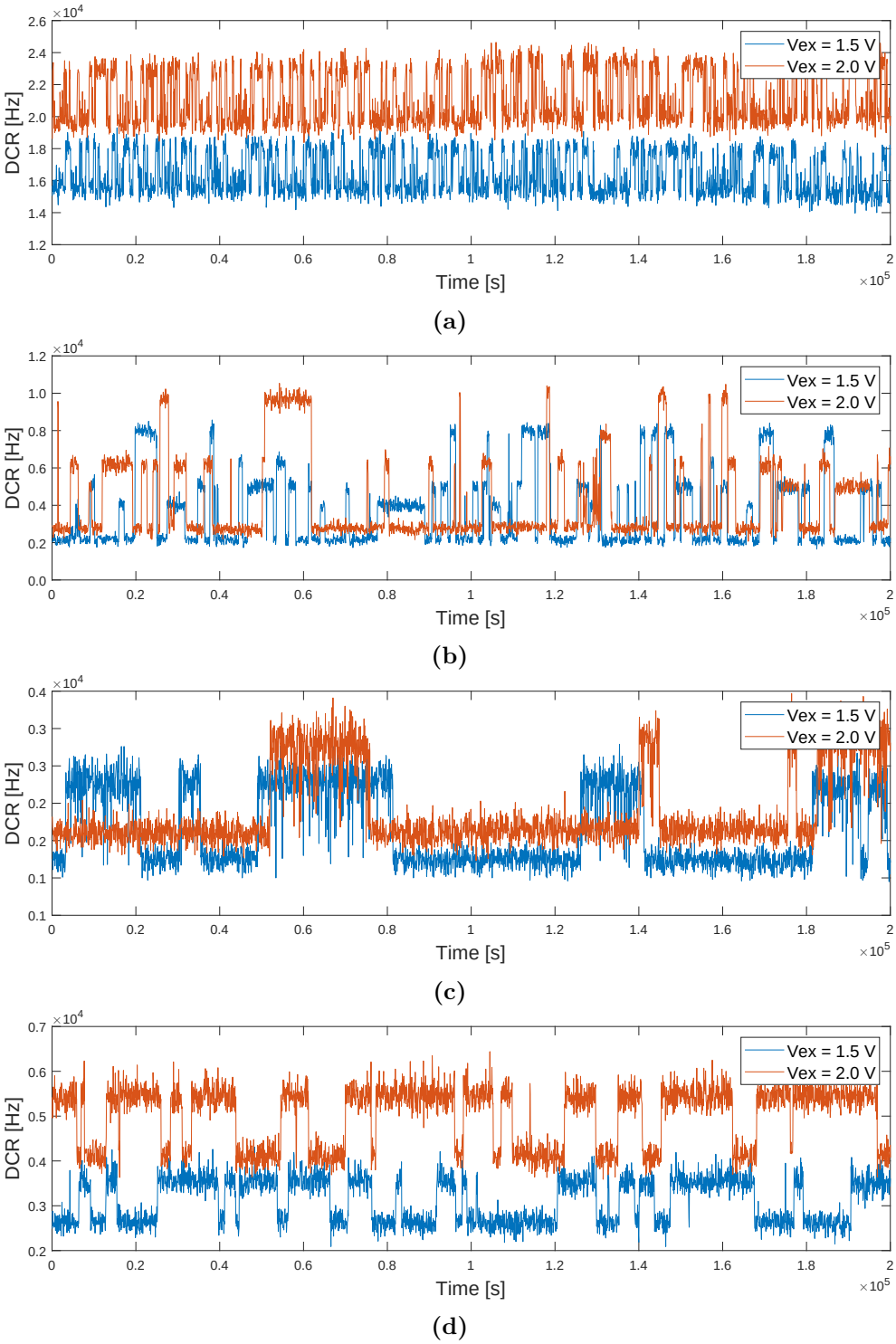


Figure 3.26. DCR vs time in pixels of array 3 exhibiting RTS behavior.

of the measured DCR. The SPADs in Figures 3.26a, 3.26c, and 3.26d exhibit a bi-level behavior with different characteristic times. The first pixel shows fast characteristic times with several transitions within the measurement duration, while the last pixel presents fewer transitions with longer characteristic times. A peculiar behavior can be observed from Figure 3.26b, which represents a multi-level RTS SPAD. At first glance it may seem as a four-level pixel, but upon observing its DCR distribution in Figure 3.27b, five levels can be distinguished. Figures 3.27c and 3.27d confirm that the last two SPADs of Figure 3.26 exhibit a bi-level RTS. Figure 3.27a reveals the emergence of a third level for 2 V of excess voltage in between the two levels.
As can be observed from the eight SPADs presented as examples, meticulous work is required in order to define whether a SPAD presents RTS behavior and to determine the number of levels per each pixel. Various methods, such as visual counting [59], histogram analysis [65], and Time Lag Plot [66], have

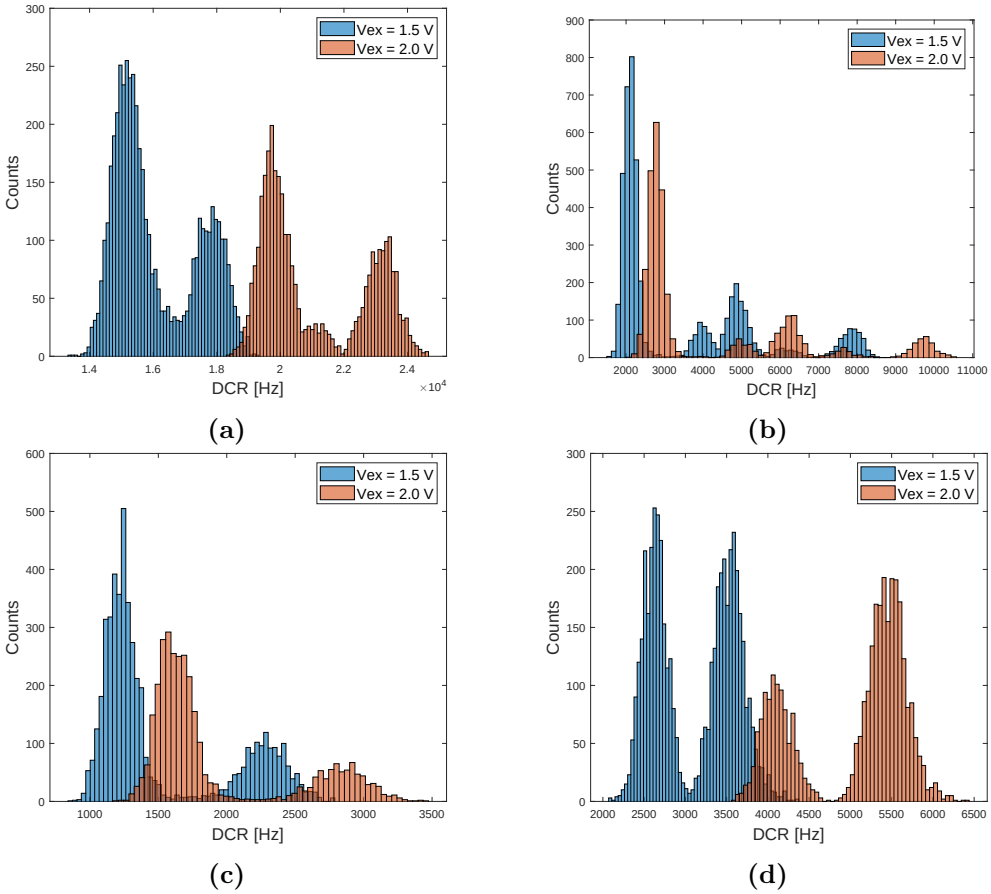


Figure 3.27. Amplitude distribution for pixels exhibiting RTS behavior.

been used to identify RTS features. An automatic algorithm that includes the above-mentioned methods, as well as threshold-based methods [60], [67], statistical properties analysis [68], and a step-shaped filter [58], is currently being developed. Due to the fact that the sampling time is not short enough for a detailed characterization of RTS with its characteristic times, these measurements were conducted to gain a general understanding of the number of pixels that may exhibit RTS behavior among all the pixels in the arrays. These chips were later exposed to neutron irradiation at the INFN Laboratori Nazionali di Legnaro in Italy to provide experimental data that supports and validates a model capable of predicting the distribution of DCR in a set of neutron-irradiated SPADs based on the particle fluence and the device active volume. Additionally, the mechanisms of bulk defect formation and the effects of neutron irradiation on the behavior of already present or newly appearing RTS contributions in the DCR will be investigated.
Tables 3.3 and 3.4 summarize the RTS features of SPADs of array 1 and 3, respectively. In array 1, about 9% of all SPADs exhibit random telegraph signal fluctuations in their DCR at three different excess voltages: 1 V, 1.5 V, 2 V. Among these RTS SPADs, bi-level RTS pixels are more common, accounting for approximately 92% of all RTS marked pixels, while SPADs with more than two RTS levels are only around 8% of all RTS marked pixels.
Array 3, in contrast, exhibits a higher percentage of SPADs that display RTS, with over 30% of the total pixels showing RTS behavior at two different excess voltages: 1.5 V and 2 V. While the majority of these pixels are bi-level RTS pixels, their percentage is lower than in array 1, accounting for approximately 77% of all RTS marked pixels. Additionally, approximately 23% of SPADs in array 3 exhibit more than two RTS levels. Preliminary investigations revealed similar results for another chip, indicating comparable behavior between ar-

Excess Voltage	2 levels	3 levels	4 levels	RTS pixels	Total SPADs	% of RTS SPADs
1.0 V	193	15	1	209	2304	9.1%
1.5 V	174	16	3	193	2304	8.4%
2.0 V	189	13	3	205	2304	8.9%

Table 3.3. RTS features for SPADs in array 1 of chip F2.

Excess Voltage	2 levels	3 levels	$\geq$4 levels	RTS pixels	Total SPADs	% of RTS SPADs
1.5 V	414	115	9	538	1728	31.1%
2.0 V	407	112	9	528	1728	30.6%

Table 3.4. RTS features for SPADs in array 3 of chip F2.

rays 1 and 3.
As explained in Section 1.3.1, pixels in arrays 1 and 3 have the same readout electronics, but different pitch, which determines their active area. Specifically, array 1 has a pitch of 75 µm, resulting in a SPAD active area of $70 \times 52 = 3640\ \mu m^2$, while array 3 has a pitch of 50 µm, with a SPAD active area of $44 \times 24 = 1056\ \mu m^2$.
The electric field and charge collection properties of SPADs may be influenced by shallow trench isolation (STI), potentially affecting the performance and the probability of observing RTS behavior in SPADs [62], particularly in those with a reduced active area such as pixels in array 3. Further research is underway to investigate these phenomena more thoroughly and gain a deeper understanding of their behavior.
As already discussed in Section 3.3, temperature plays a very important role in the performance of a semiconductor detector because it affects the mechanism of carrier generation inside the device. A temperature rise leads to a higher probability of DCR switching and an increased RTS amplitude. To conduct an extensive investigation of RTS behavior, a selection of 20 pixels from Array 1 of F2 and S2 chips was made. The chosen pixels were those with short characteristic times, such as the pixels illustrated in Figure 3.24a and 3.26a, to further examine the RTS fluctuations. The test was conducted in a climatic chamber at temperatures ranging from -40°C to 70°C and every pixel was read with a time resolution of 1.1 seconds. Characterization measurements were performed for each selected pixel at two different excess voltages, 1.5 V and 2 V, at each temperature point. The duration of each measurement was approximately 3 hours.
Among the chosen pixels, some with multiple level RTS is observed, especially for higher temperatures. For the sake of simplicity, for the following analysis,

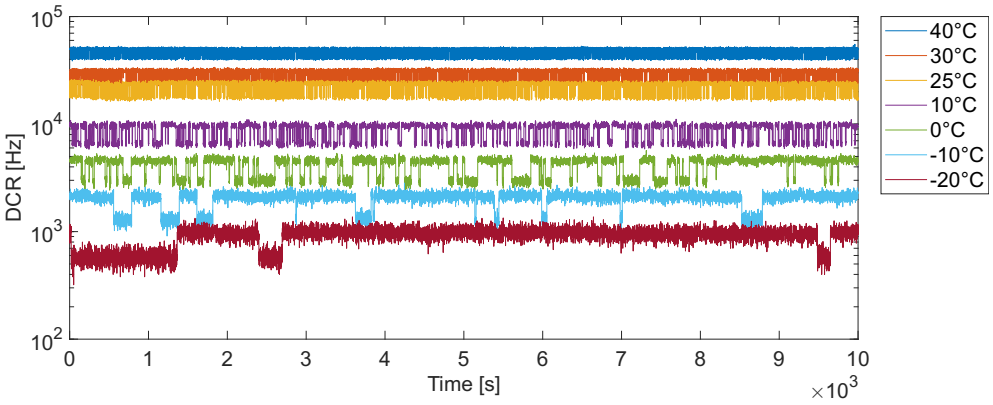


Figure 3.28. DCR as a function of time for pixel A of array 1 exhibiting RTS behavior measured at different temperatures with a 2 V excess voltage.

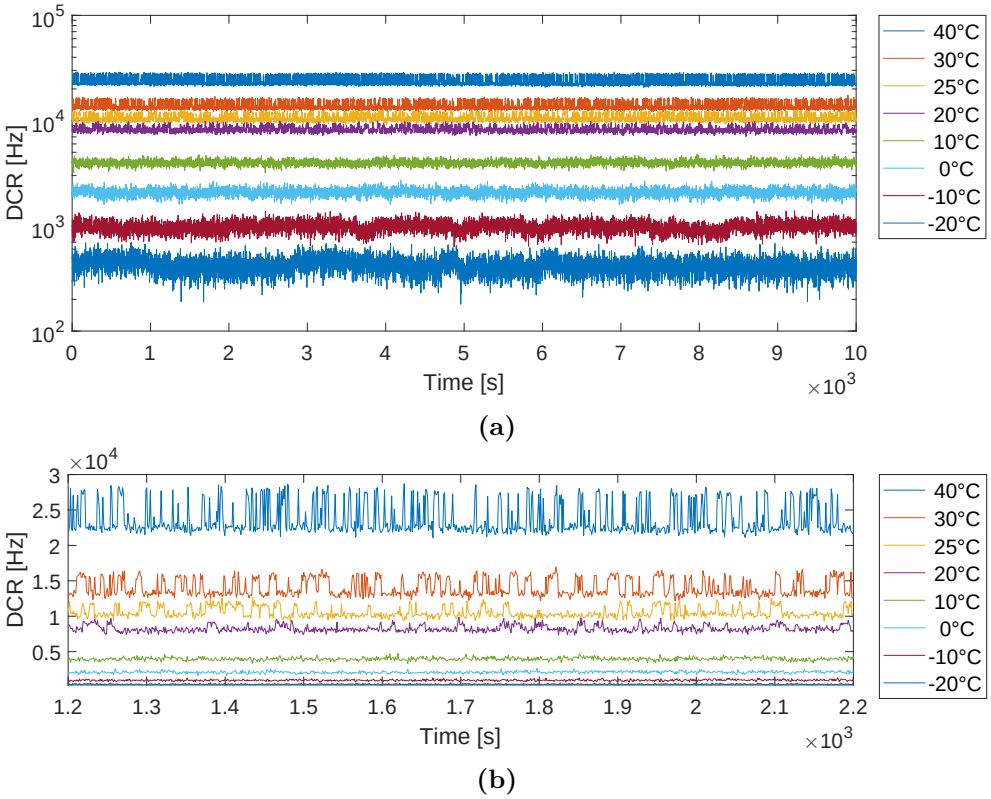


Figure 3.29. DCR as a function of time for pixel B of array 1 exhibiting RTS behavior measured at different temperatures with a 2 V excess voltage (a). In (b) a blow up of the same measurement in linear scale is shown.

the focus will be only on two bi-level RTS pixels.
Figure 3.28 displays the DCR as a function time for pixel A of array 1, biased with an excess voltage of 2 V, at different temperatures on a semi-logarithmic scale. As can be observed, the RTS amplitude and the number of transitions between the two levels increase with temperature.
Similarly, the measured DCR for pixel B, biased with a 2 V overvoltage, is shown for each temperature in Figure 3.29a. The number of transitions between the two levels during the measurement interval is larger than that observed in pixel A. This is particularly evident in Figure 3.29b, which provides a blow up of Figure 3.29a in a linear scale, and reveals some differences in amplitude and characteristic times. At temperatures lower than 10°C, RTS phenomena disappear.
As previously discussed, another way to determine whether a pixel exhibits RTS behavior is by examining the histogram of the measured DCR. Figure 3.30 displays the dark count rate distribution for pixel B at different excess

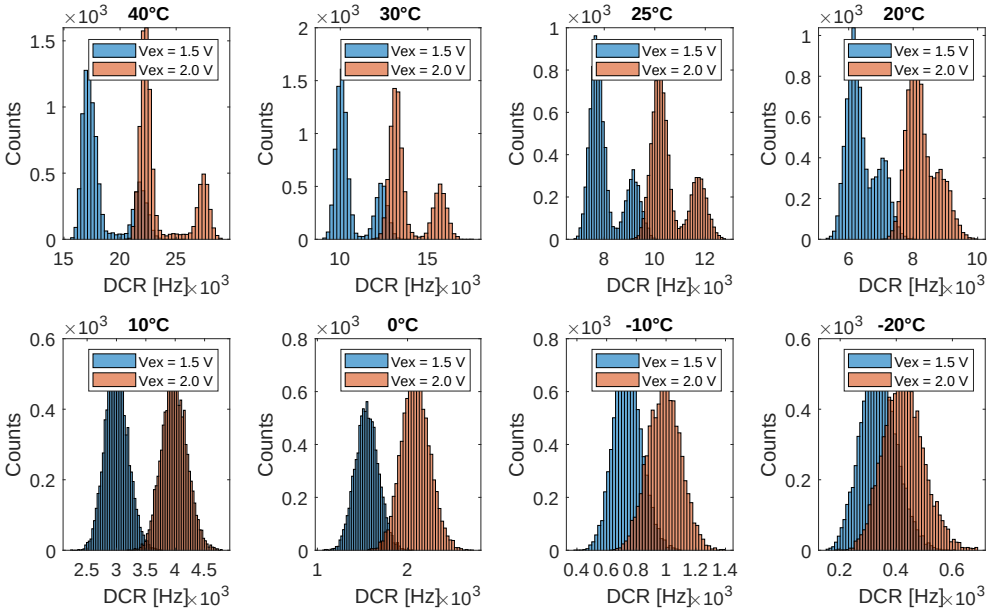


Figure 3.30. Dark Count Rate distribution for a selected pixel of array 1 exhibiting RTS behavior at different temperatures with a 1.5 V excess voltage.

voltages and temperatures. As expected, the excess voltage significantly affects the RTS levels and amplitudes. The histograms reveal the difference in amplitude as the temperature decreases, as the distance between the two-horned distributions tends to reduce. Consistently with the observations from the time plot, starting from 10°C, the histograms show that the RTS behavior disappears. Further studies on the activation energies for every RTS level of all the measured pixels are currently underway to provide a deeper understanding of the phenomenon.

In general, the average time spent in a level can be defined as the mean time spent in a particular level between two transitions, regardless of the next transition. For example, in a three-level RTS, there will be three distinct average times per level, and these times represent the mean of all dwell times that occur in each given level. On the other hand, a time constant is the mean time spent in a given level before a particular transition occurs [61].

For a bi-level RTS pixel, it is easier to extract the time constant because there are just two possible transitions, and the average time spent in a level coincides with the time constant. Figure 3.31 displays the distribution of time intervals at different temperatures and excess voltages for the lower level (down time) and the upper level (up time). The figures illustrate that the time intervals follow an exponential distribution, as expected for a Poissonian process [62].

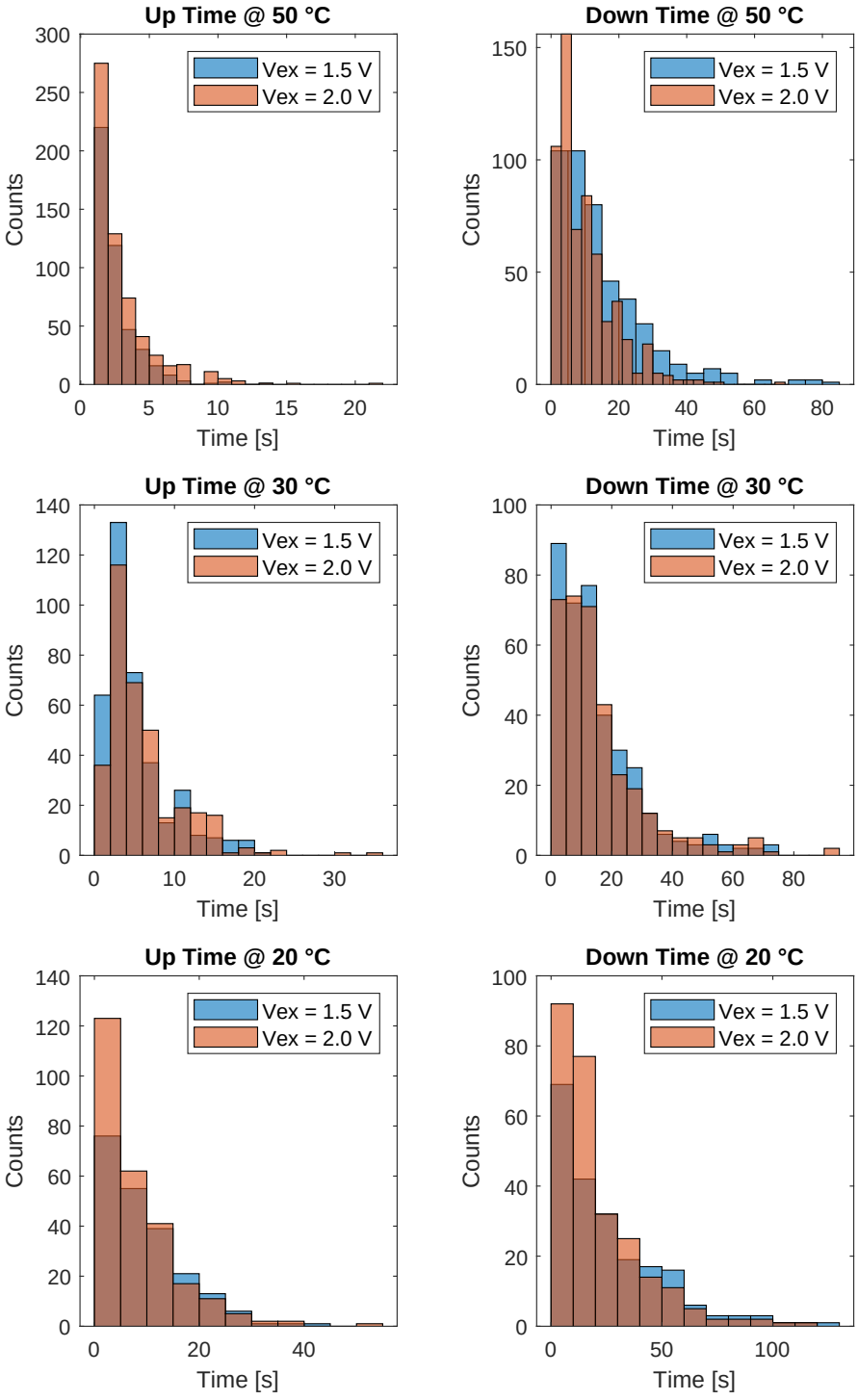


Figure 3.31. Up and down time distribution for a selected pixel of array 1 exhibiting RTS behavior at different temperatures with 1.5 V and 2 V excess voltage.

	Vex = 1.5 V			Vex = 2.0 V		
T [°C]	τ_{up} [s]	τ_{down} [s]	A_{RTS} [Hz]	τ_{up} [s]	τ_{down} [s]	A_{RTS} [Hz]
50	3.49	11.62	7000	2.43	11.39	8500
40	4.22	11.47	4800	3.35	11.44	5100
30	5.01	13.97	2200	5.75	16.26	2600
25	7.29	20.76	1500	7.26	20.32	1500
20	9.61	25.60	900	9.78	25.83	900

Table 3.5. RTS parameters for different excess voltages at different temperatures for pixel A of array 1 exhibiting bi-level RTS.

The excess voltage does not seem to have a noticeable effect on the time intervals. However, temperature has a significant impact on the time constants, as they decrease with increasing temperature.
Table 3.5 summarizes the RTS behavior parameters of pixel B for different excess voltages and temperatures, including up and down time constants and RTS amplitude (A_{RTS}), defined as the difference between the DCR levels in the case of a two-level RTS fluctuation. This SPAD exhibits a longer down time compared to the up time, and both time constants increase as the temperature decreases while not being significantly affected by the excess voltage. Developing a more efficient method for analyzing a large amount of data is crucial in order to fully exploit the potential of the measurements. This will likely involve creating custom software or scripts that can automatically analyze the data and extract the necessary parameters. This can save a significant amount of time and increase the accuracy and reproducibility of the results. Additionally, it may be useful to develop a standardized procedure for analyzing RTS behavior in SPADs to ensure consistency across different experiments and research groups.

Chapter 4

Particle Imaging Probe Characterization

A prototype board based on the APIX2LF chip was designed and developed as a detection probe for mapping the activity of laboratory sources or for medical applications [69]. The sensor is bonded on the top board of a custom-designed carrier composed of two printed circuit boards, while a SiPM (Advansid ASD-NUV4S-P) is mounted on the bottom board of the stack. As described in Chapter 2, the probe is intended to be an all-in-one solution that can be battery or USB powered. It includes all the necessary circuitry and a microcontroller that acts as an interface between the sensor and a PC, processing signals and transferring data wirelessly or through USB connection. Custom firmware was also developed for the microcontroller for different kinds of measurements to be performed, as discussed again in Chapter 2.
This chapter focuses on the results of the characterization of the APIX2LF chip, called from now on **D3**, mounted on the small carrier. Measurements were carried out through the prototype board described in Section 2.1. The first part of the chapter shows the characterization of the breakdown voltage and dark count rate performed inside a dark chamber. The second part of the chapter presents the results of measurements performed with a radioactive source at the Physics Section of the Department of Physical Sciences, Earth and Environment of the University of Siena.

4.1 Dark Count Rate Characterization

The D3 chip mounted on the small carrier had not been previously characterized. Therefore, a characterization campaign was necessary to study its properties. Dark count rate measurements were performed both enabling one pixel at a time and enabling all pixels. As already explained in Section 3.1,

for dual layer chips a time frame of 100 µs was used for all the measurements. Depending on the type of measurement performed on D3, the number of iterations **N** ranged between 10000 and 300000 that correspond to a total integration time of 1 s and 30 s, respectively. The maximum rate that can be measured is 10 kHz as per (3.1), while the minimum rate is 1 Hz, or 33 mHz as per (3.2), depending on the number of iterations **N**. As already outlined in Section 3.1, for the quenching and clamping operations, 0.9 V and 1.8 V were used, respectively. Unless otherwise specified, a coincidence window of 2 ns was set between the signals from the top and bottom chips.
During the characterization process, it was observed that there is a row of dead pixels (48 pixels) in array 1. However, they have minimal impact on the overall results of the characterization, as they account for only 1% of the total number of pixels.
The following sections will present the breakdown voltage extraction and DCR behavior for various bias voltages.

4.1.1 Breakdown voltage extraction

As explained in Section 3.2, the breakdown voltage (V_{BD}) is a crucial parameter for an avalanche detector, as it governs the detector behavior. When the bias voltage is maintained close to but below the breakdown voltage, the detector operates in the linear region. However, in the case of a SPAD, if the diode is biased with a higher voltage than the breakdown voltage, even a single photon can trigger an avalanche inside the device. The breakdown voltage for each SPAD was extracted from the dark count rate versus bias voltage curves, as described in [50].
The measurements were conducted at room temperature inside a dark chamber. The SPADs bias voltage was swept in steps of 50 mV between 19.6 V and 20.1 V. To obtain a reliable measurement, the procedure was repeated $N = 100000$ times, resulting in a total integration time of 10 s.
Figure 4.1 shows the breakdown voltage histogram measured for the array 1 of chip D3. The array presents a mean breakdown voltage of 18.8 V with a standard deviation of 75 mV. Figure 4.2 shows the heat map for the breakdown voltage in array 1. Similarly, Figure 4.3 shows the breakdown voltage histogram measured in the array 3 of chip D3. The array presents a mean breakdown voltage of 18.88 V with a standard deviation of 76 mV. Figure 4.4 shows the heat map for the breakdown voltage of array 3.
Although APIX2LF is treated as a single detector, one must not forget that it consists of two individual chips vertically interconnected. In this perspective, the obtained standard deviation in the range of 80 mV seems compatible with the characterization results of dual-layer chips presented in Section 3.2 and with data discussed in [50], [70].

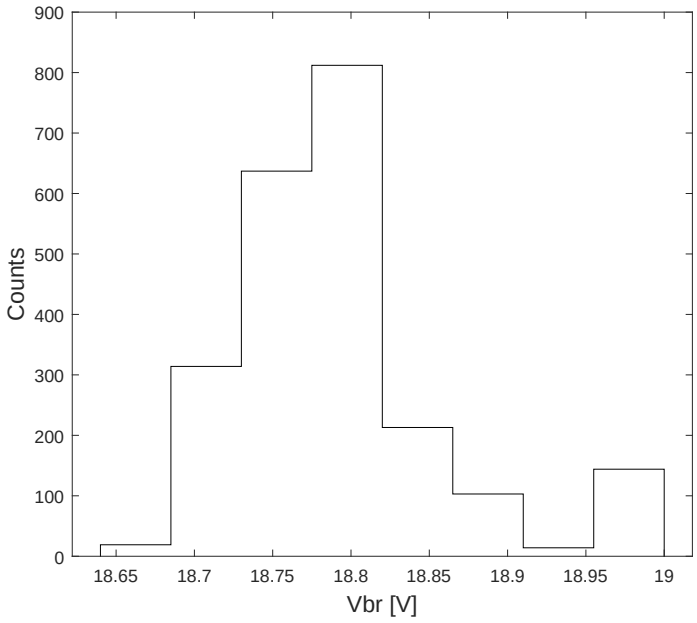


Figure 4.1. Breakdown voltage distribution of array 1 (48×48 pixels) for the D3 chip.

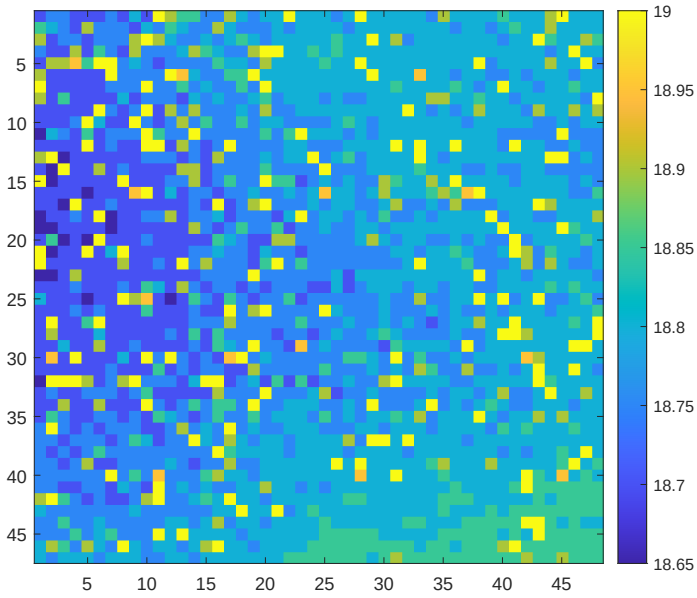


Figure 4.2. Heat map for the breakdown voltage in array 1 (48×48 pixels) of the D3 chip.

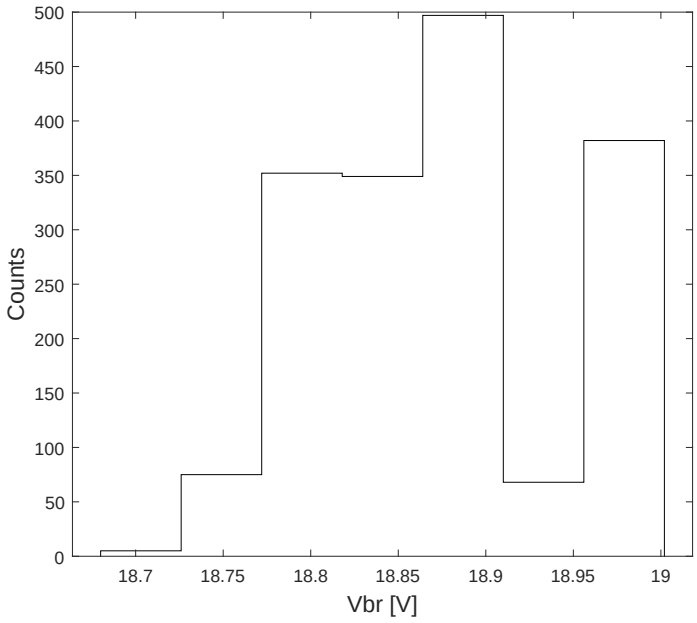


Figure 4.3. Breakdown voltage distribution of array 3 (24×72 pixels) for the D3 chip.

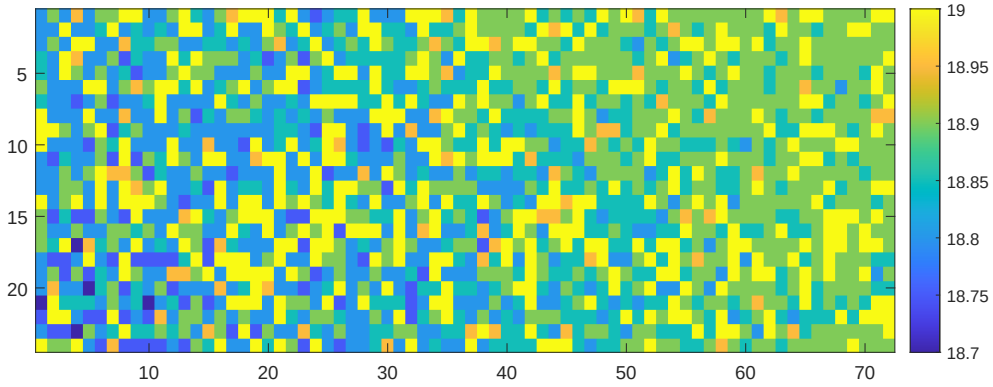


Figure 4.4. Heat map for the breakdown voltage in array 3 (24×72 pixels) of the D3 chip.

4.1.2 Dark Count Rate

As already discussed, DCR measurements are very important for devices like SPADs, since DCR sets the sensitivity performance of the device. Both array 1 and array 3 of chip D3 were characterized at different bias voltages with a step of 100 mV up to 2.8 V of overvoltage, corresponding to bias voltages

up to 21.6 V. The maximum overvoltage that can be applied is set by the clamping transistor connected to the anode of the SPAD sensor (Figure 1.11), which is 3.3 V, as explained in Section 3.1. Measurements were performed inside a dark chamber at room temperature with a detection time frame of 100 µs. The coincidence window between the signals coming from the top and bottom chip was set to 2 ns. As explained in Chapter 3, two other dual-layer chips, labeled D1 and D2, bonded in a CPGA144 package, were completely characterized using the benchtop boards described in Section 1.4 using the ESP32 microcontroller. Those results will be compared with the results obtained from the characterization of D3.
Figure 4.5 shows the cumulative distribution curves for SPADs of arrays 1 and 3 biased at 20 V ($V_{EX} = 1.3\ V$). A total of $N = 300000$ iterations were used for each measurement, with a corresponding integration time of 30 s. To measure each pixel, all the other SPADs were disabled, using the "1-by-1" approach described in the firmware functions section (2.2.1). The measurement process takes several hours to complete due to the large number of pixels in the arrays: array 1 contains 2304 pixels, while array 3 contains 1728 pixels.

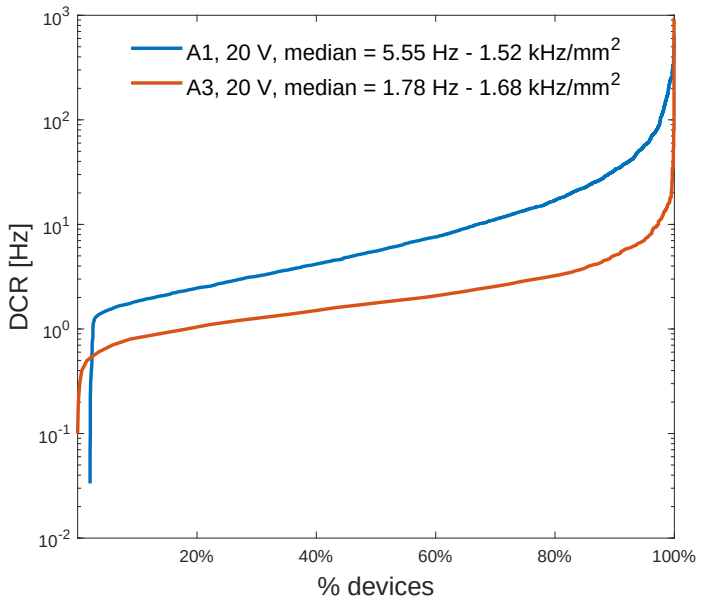


Figure 4.5. DCR cumulative curves for SPADs of arrays 1 and 3 of chip D3, biased at 1.3 V excess voltage, corresponding to 20 V of bias voltage. The measurement was performed at room temperature enabling one single SPAD at a time.

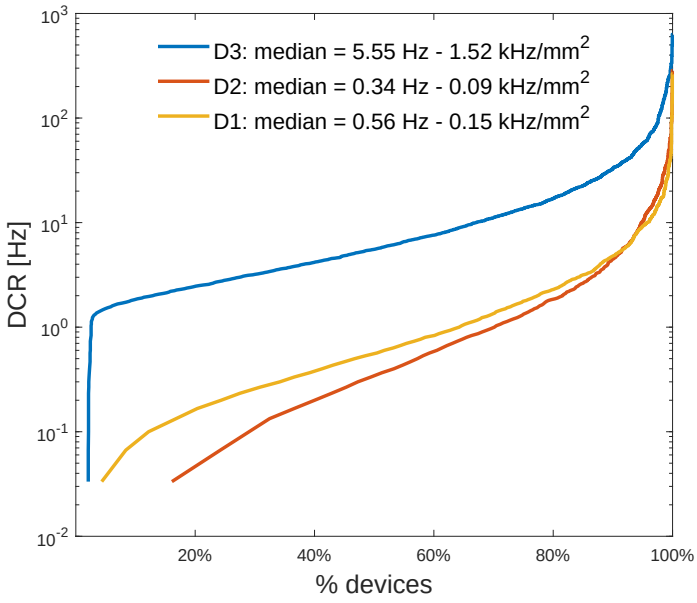


Figure 4.6. DCR cumulative curves for SPADs of array 1 of three dual-layer APIX2LF chips, D1, D2, and D3, biased at 1.3 V excess voltage. The measurement was performed at room temperature enabling one single SPAD at a time.

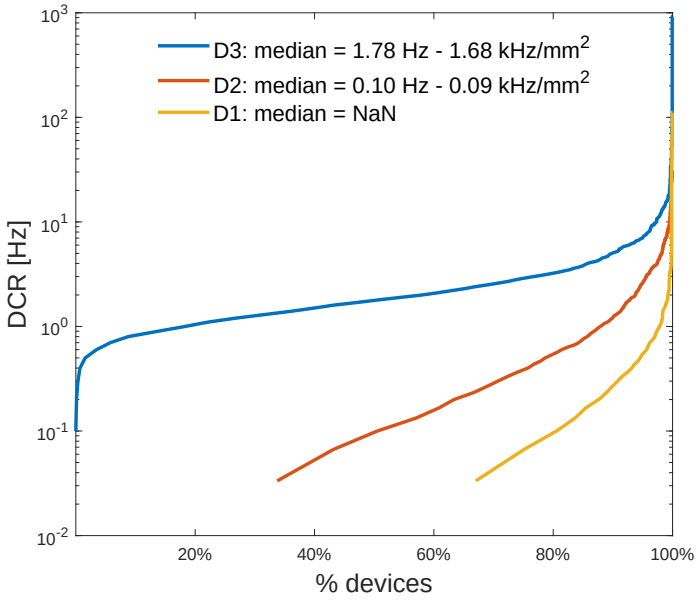


Figure 4.7. DCR cumulative curves for SPADs of array 3 of three dual-layer APIX2LF chips, D1, D2, and D3, biased at 1.3 V excess voltage. The measurement was performed at room temperature enabling one single SPAD at a time.

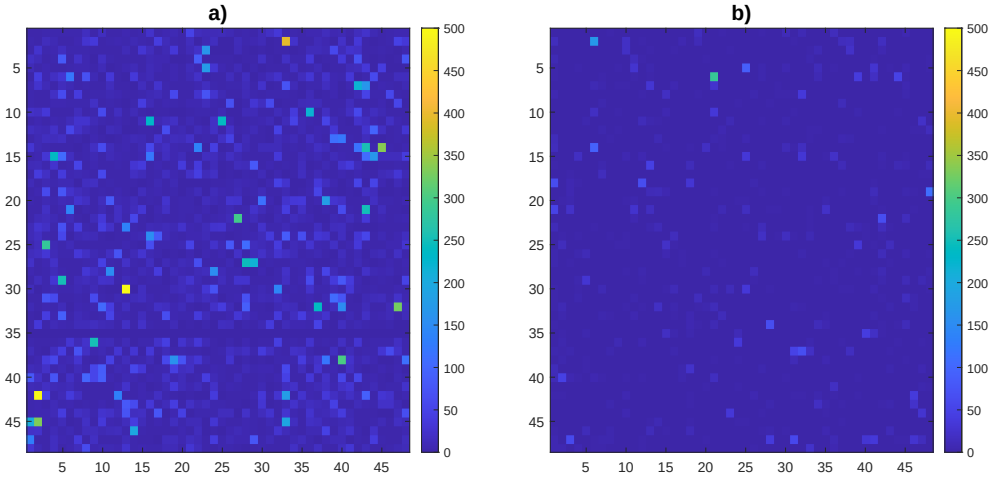


Figure 4.8. Heat map of the DCR of SPADs of array 1 biased at 1.3 V excess voltage for the D3 (a) and D2 (b) chips. As mentioned in Section 4.1, row 35 of chip D3 is a row of dead pixels. The measurement was performed at room temperature enabling one single SPAD at a time.

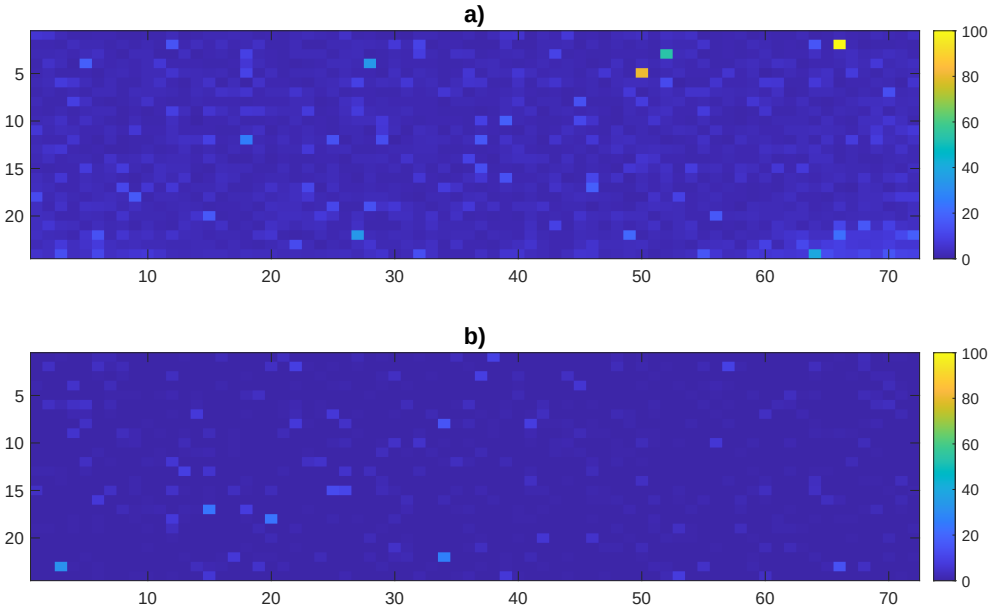


Figure 4.9. Heat map of the DCR of SPADs of array 3 biased at 1.3 V excess voltage for the D3 (a) and D2 (b) chips. The measurement was performed at room temperature enabling one single SPAD at a time.

When compared to the other two dual-layer chips, D1 and D2, the cumulative dark count rate in D3 is slightly higher. This can be observed in the cumulative distribution plots shown in Figure 4.6 for array 1 and Figure 4.7 for array 3, as well as their corresponding heat maps in Figures 4.8 and 4.9. The median value of array 3 in chip D3 (Figure 4.9) could not be extracted because it is smaller than the lowest detectable DCR (as determined by (3.2)), which corresponds to 33.3 mHz with the current measurement configuration. During the extended "1-by-1" measurement, an increase in temperature was observed, which may have contributed to the higher than expected dark count rate. Referring to Figure 1.11, a weak pull-up is connected to the NAND gate that produces the coincidence signal, allowing for separate characterization of the FATHER chip. This weak pull-up transistor consumes static current and contributes to the dissipated power, thus causing the temperature to rise. Because D3 is enclosed in a plastic case and bonded on a small PCB carrier, the heat dissipation is less efficient due to the small dimensions and the nature of the case.
Unfortunately, direct temperature measurement of the chip was not possible, and the plastic case could not be removed as it served to protect the bonding

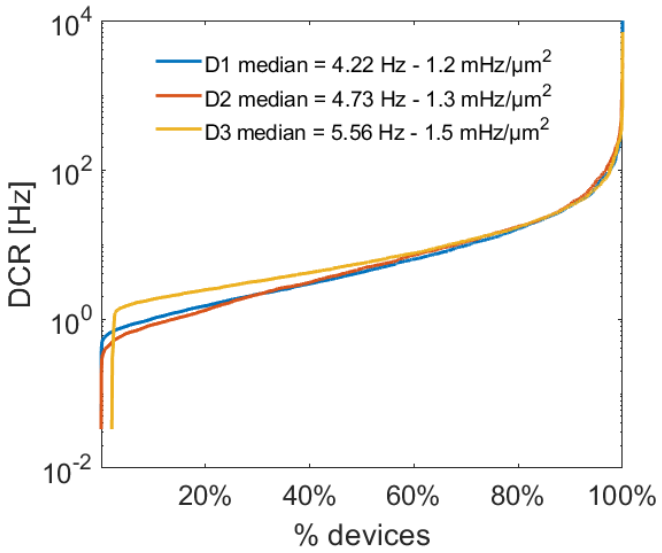


Figure 4.10. DCR cumulative curves for SPADs of array 1, biased at a 1.3 V excess voltage for three different dual layer chips. The measurement was performed by enabling one single SPAD at a time. D1 and D2 were characterized at 40°C inside a climatic chamber while D3 measurements were performed at room temperature.

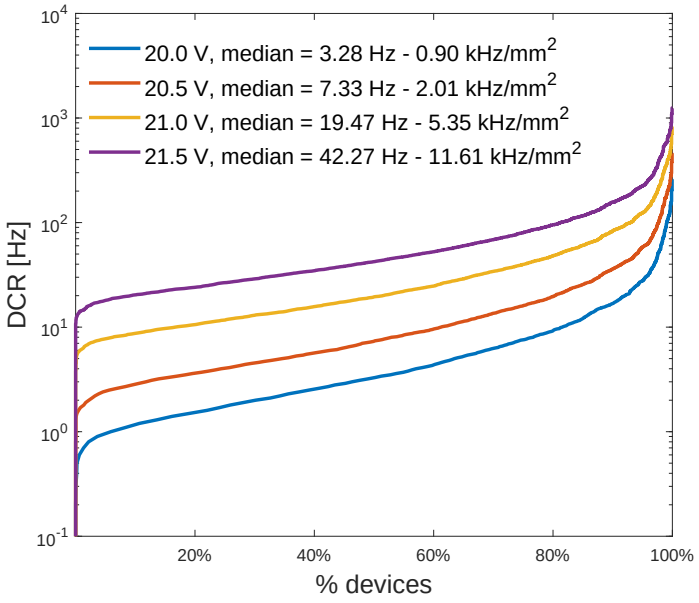


Figure 4.11. DCR cumulative curves for SPADs of array 1 of D3 chip, biased at different bias voltages. The measurement was performed by enabling all SPADs.

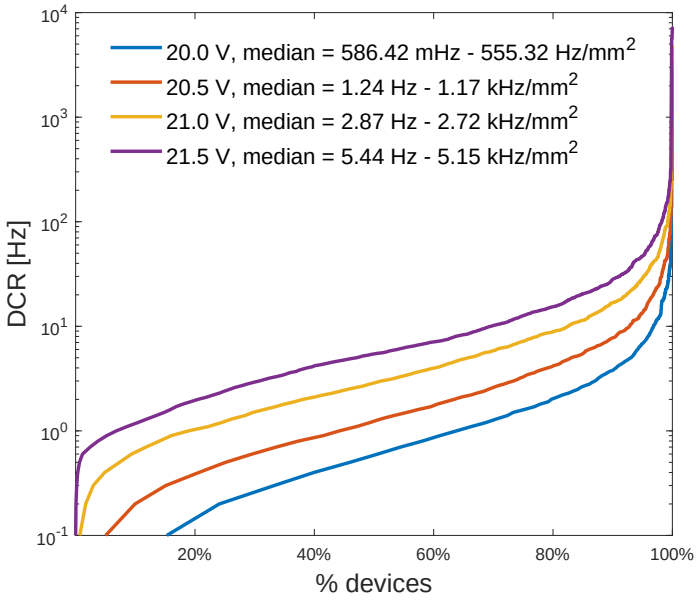


Figure 4.12. DCR cumulative curves for SPADs of array 3 of D3 chip, biased at different bias voltages. The measurement was performed by enabling all SPADs.

connections. To confirm that the temperature increase was indeed responsible for the observed DCR increase, D1 and D2 chips were characterized inside a climatic chamber (see Section 2.3) at a constant temperature of 40°C. Figure 4.10 shows the DCR cumulative curves for pixels of array 1 for these three different dual-layer chips, D3 characterized at room temperature, D1 and D2 at 40°C.
The similarity between the curves obtained from the D1 and D2 chips, strongly suggests that there is a difference of approximately 15°C between the chip in the small carrier and the chip in the CPGA144 package. To address this issue while ensuring sensor protection, alternative packaging solutions that facilitate heat dissipation are currently under investigation.
On the other hand, the "AllON" measurement, where all pixels are enabled simultaneously, takes only a few minutes to complete, so the temperature increase has a lesser effect on the measurement results. Figures 4.11 and 4.12 display the cumulative curves of SPADs in array 1 and 3, respectively, biased at different voltages, in particular 20, 20.5, 21 and 21.5 V, that correspond to excess voltages of 1.3, 1.8, 2.3 and 2.8 V respectively. The DCR almost doubles for both arrays every 500 mV increase in bias voltage.

4.2 Characterization with a Radioactive Source

To test the functionality of the miniaturized chip as a particle detector, measurements with a beta source were performed at the Physics Section of the Department of Physical Sciences, Earth and Environment of the University of Siena. A sealed (β, γ) disk shaped ^{106}Ru source (Figure 4.13) with a diameter of (25.654 ± 0.254) mm and a thickness of 3.175 mm was used. The source is placed at the center of the disc within a diameter of (6.35 ± 0.254) mm.
Ruthenium-106 is a pure β^- emitter with a half-life of 371.5 days that decays to the ground state of Rhodium-106 (^{106}Rh). The beta decay of Ru-106 produces a continuous spectrum of beta particles with energies ranging from zero up to a maximum energy of 3.54 MeV. However, the majority of beta particles emitted by Ru-106 have energies below 0.8 MeV, with peak energy around 0.38 MeV. In March 2020 the disk source had a 37 kBq activity. Considering its decay time, when the measurements were performed, in September 2022, its activity was estimated to be approximately in the range of 3.2 kBq.
The schematic measurement setup is shown in Figure 4.14. The probe prototype and the radioactive source were placed inside a dark chamber at room temperature. The distance between the source and the sensor was 2 cm and no collimator was used.
All measurements involving the radioactive source were conducted with all pixels of array 1 and array 3 enabled. Specifically, two types of measurements

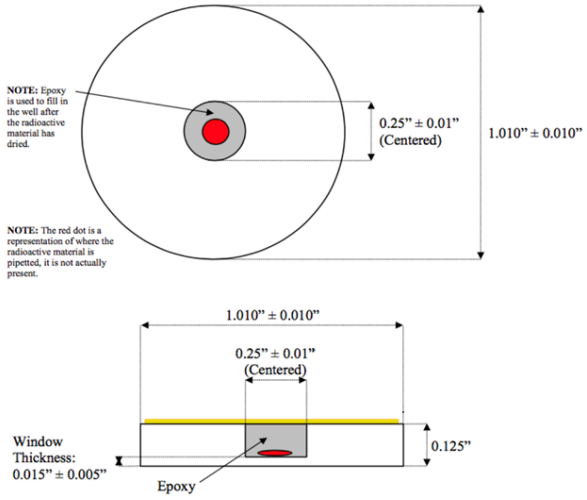


Figure 4.13. Schematic geometry of the sealed (β, γ) disk ^{106}Ru source used for the measurements. It has a diameter of (25.654±0.254) mm and a thickness of 3.175 mm.

were conducted using the source, which are related to the functions outlined in Section 2.2.1: "AllON" and SiPM-triggered measurements. The latter leverages the signal from the Advansid ASD-NUV4S-P SiPM to trigger the readout of arrays 1 and 3. In the "AllON" measurement, a specific number of readouts of arrays 1 and 3 is conducted within a specified time frame, resulting in a total integration time. It is worth noting that this same type of measurement was also used to characterize the dark count rate of the sensor as presented in the previous section.
Figure 4.15 displays the average current absorbed by the arrays during the

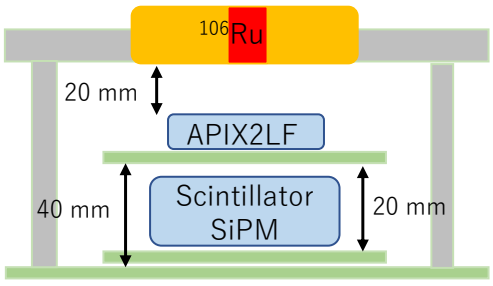


Figure 4.14. Measurement setup using the disk source with a distance of 2 cm from the APIX2LF chip (objects are not to scale). No collimator was used.

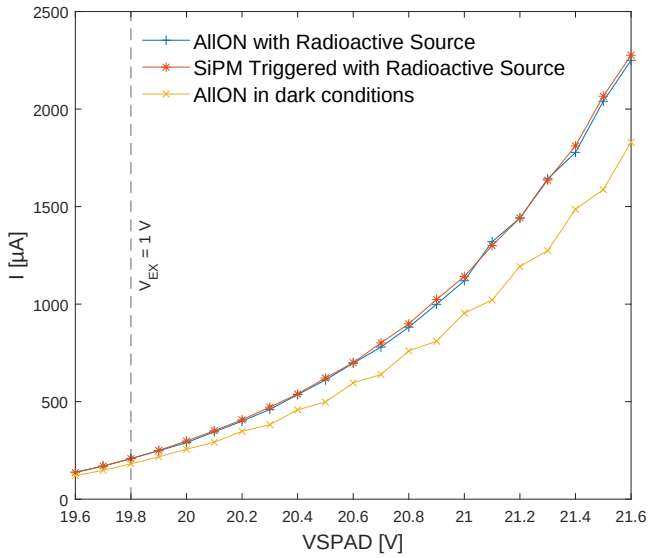


Figure 4.15. Current absorbed by chip D3 at different bias voltages in three specific measurement conditions, with and without a radioactive source.

various measurements. The dashed line denotes the value corresponding to 1 V of excess voltage. As expected, the current increases with the bias voltage, and the current is higher when the radioactive source is used than when the sensor is in a dark condition. The difference in current is more pronounced at higher voltages.
Subsequently, the outcomes of the two types of measurements performed using the radioactive source are presented.

4.2.1 "AllON" measurement results

"AllON" measurements, where all the pixels of arrays 1 and 3 are enabled, were performed in dark conditions for the characterization of the DCR and with a beta-emitting source to provide a first means to evaluate the performance of the sensor in particle counting applications. 100000 frames with 100 µs integration time were summed up to obtain a total integration time of 10 s. The coincidence window between the signals coming from the top and bottom chip was set to 2 ns. Figures 4.16, 4.17, 4.18 and 4.19 show the cumulative distribution curves of the measured hits without (N) and with (S) the radioactive source for 1.3, 1.8, 2.3 and 2.8 V of overvoltage. The median value of the cumulative curves and their corresponding rate per area is indicated in the legend. In particular, when the source is used, the median value varies between 1.4 and 25 kHz/mm^2 for array 1 and between 0.8 and 10 kHz/mm^2

for array 3, respectively.
The measurements indicate that there is only a small difference between the curves for both array 1 and array 3, usually around a factor of two. As can be observed from the medium current absorbed shown in Figure 4.15, the higher the excess voltage, the better the detection efficiency. The ratio between the measurement with and without the source increases as the bias voltage increases and this effect is clear on both arrays. Since the pixel fill factor is greater for array 1 than for array 3, which is 66% and 39% respectively, the ratio is higher for array 1 than array 3. Nevertheless, this difference tends to decrease as the bias voltage increases. These results suggest that while higher excess voltages lead to higher dark count rates, the overall detection efficiency is better than at lower excess voltages.
As already mentioned, the temperature may also significantly affect the behavior of the APIX2LF chip due to the small plastic housing case. A preliminary test has shown that DCR decreases significantly at temperatures below 10 °C. The high density of neighboring pixels on the array may cause cross-talk in the SPAD array. In previous measurements, as presented in Section 3.4, it was observed that a few pixels with a high DCR, which typically account for less than 1% of the total number of pixels, may significantly affect the global DCR distribution. Identifying and disabling these pixels, known as screamer pixels, can result in improved sensor performance in terms of DCR [54].
Besides noise, other factors contribute to the low detection efficiency, such as the thickness of the top chip (150 µm) whose substrate may absorb a fraction of emitted particles. Additionally, since no collimator was used, particles striking the detector with a large incidence angle are more likely to miss the second layer [21].
As previously mentioned, the majority of beta particles emitted by Ru-106 have energies below 0.8 MeV, which may not be sufficient to effectively trigger the avalanche inside both SPADs of the dual-layer device. Estimates of the ionizing radiation dose rate suggest that it is around 7.1 µSv/h, which may be comparable to the DCR of the SPADs of the array at room temperature. Furthermore, the size of the source is comparable to the size of the chip, which may result in a lower detection efficiency due to the insufficient number of particles emitted by the source reaching the SPADs.
Additional measurements should be conducted using sources with varying sizes, activities, and energies to obtain a more reliable assessment of the APIX2LF sensor performance as a charged particle detector and to determine the optimal energy spectrum for detection. These measurements can also provide information on the most suitable bias voltage to achieve the highest possible signal-to-noise ratio.

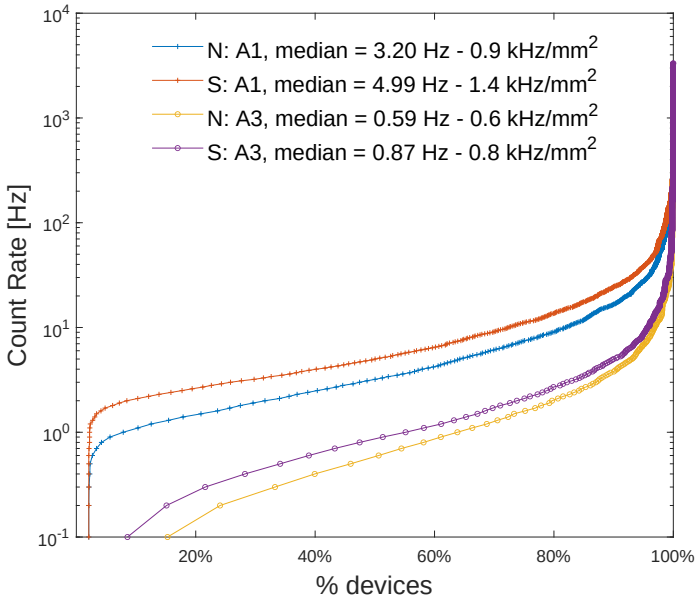


Figure 4.16. Cumulative DCR curves for pixels in arrays 1 and 3, biased at 1.3 V excess voltage. The measurement was performed by enabling all pixels with and without a beta-emitting source.

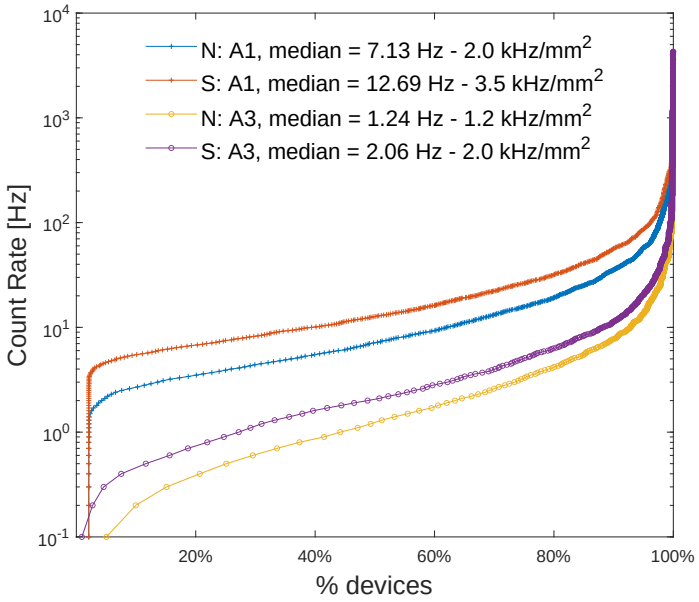


Figure 4.17. Cumulative DCR curves for pixels in arrays 1 and 3, biased at 1.8 V excess voltage. The measurement was performed by enabling all pixels with and without a beta-emitting source.

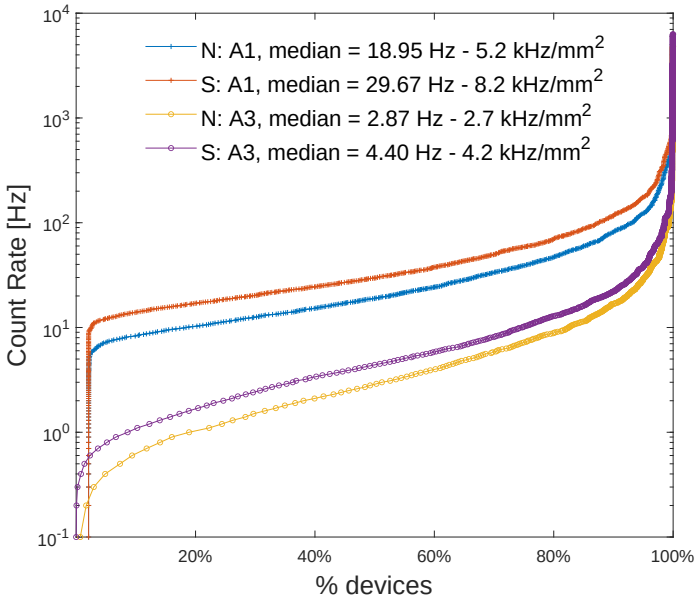


Figure 4.18. Cumulative DCR curves for pixels in arrays 1 and 3, biased at 2.3 V excess voltage. The measurement was performed by enabling all pixels with and without a beta-emitting source.

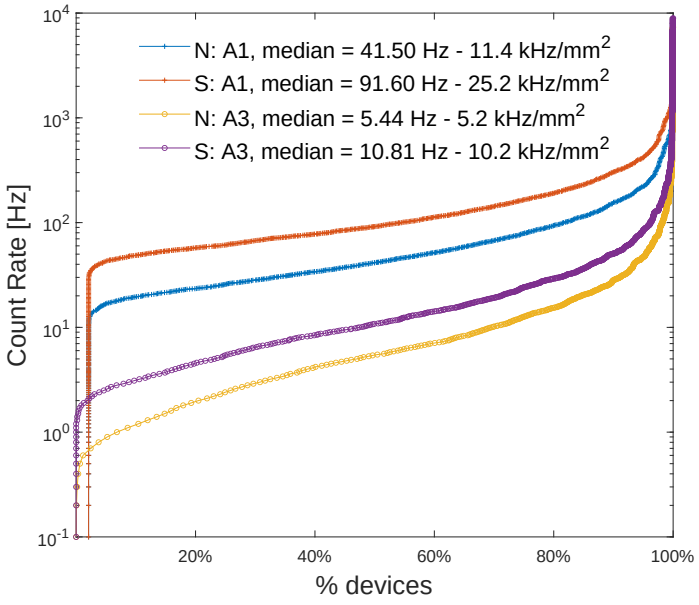


Figure 4.19. Cumulative DCR curves for pixels in arrays 1 and 3, biased at 2.8 V excess voltage. The measurement was performed by enabling all pixels with and without a beta-emitting source.

4.2.2 SiPM triggered measurement results

A different set of measurements was performed in triggered mode, based on the Advansid SiPM, as discussed in Section 2.1 and 2.2.1.5. In these measurements, the cathode of the SiPM was biased with 27.5 V ($V_{EX} = 2\ V$) while its anode is connected to a transimpedance amplifier (Figure 2.4). The output of the amplifier is then fed to a comparator whose output is connected to a pin of the microcontroller. This input is treated as an interrupt for the firmware: once the SiPM has detected a particle, a readout of the arrays is performed. This procedure is iterated until 10000 trigger signals are detected.
As described in the flowchart presented in Figure 2.11, the reset of the chip cell memory (MEMRB signal of the Trigger Latch of Figure 1.11) is continuously activated and released. The time between the release of the reset and the moment when a trigger signal is received from the SiPM is referred to as *live time*. During this time, a single cell, despite being able to detect and store a particle event, may also generate and store a dark event. The total live time per measurement was in the range of 10 ms.
Figures 4.20 and 4.21 display the heat maps of the SPADs in arrays 1 and 3 respectively, for different bias voltages, in particular 20, 20.5, 21 and 21.5 V, that correspond to excess voltages of 1.3, 1.8, 2.3 and 2.8 V respectively. By using the same scale for all maps, a slight increase in overall activity as the excess voltage rises can be observed as the pixel colors become brighter. This trend is more clearly illustrated in Figure 4.22, which displays the cumulative distribution curves for array 1. The rate was calculated based on the total live time of the measurement. Is worth noting that the median value displayed for the first three bias voltages is an interpolated value.
Table 4.1 summarizes the total number of hit counts for arrays 1 and 3 across different bias voltages. The hit counts per cell were corrected by subtracting the corresponding DCR level for the given live time from each count.
Upon examining the heat maps, it becomes noticeable that some SPADs exhibit higher levels of noise, as their hit count increases with higher bias voltages. The APIX2LF chip provides the flexibility to disable these pixels, which can significantly contribute to the dark count rate of the sensor and may also affect the behavior of adjacent pixels through crosstalk phenomena. This could potentially explain the higher hit count observed for array 1 at a bias voltage

Array	20 V	20.5 V	21 V	21.5 V
A1	4018	5050	6483	10032
A3	570	745	992	1619

Table 4.1. Total counts of arrays 1 and 3 (A1, A3) for the SiPM triggered measurement.

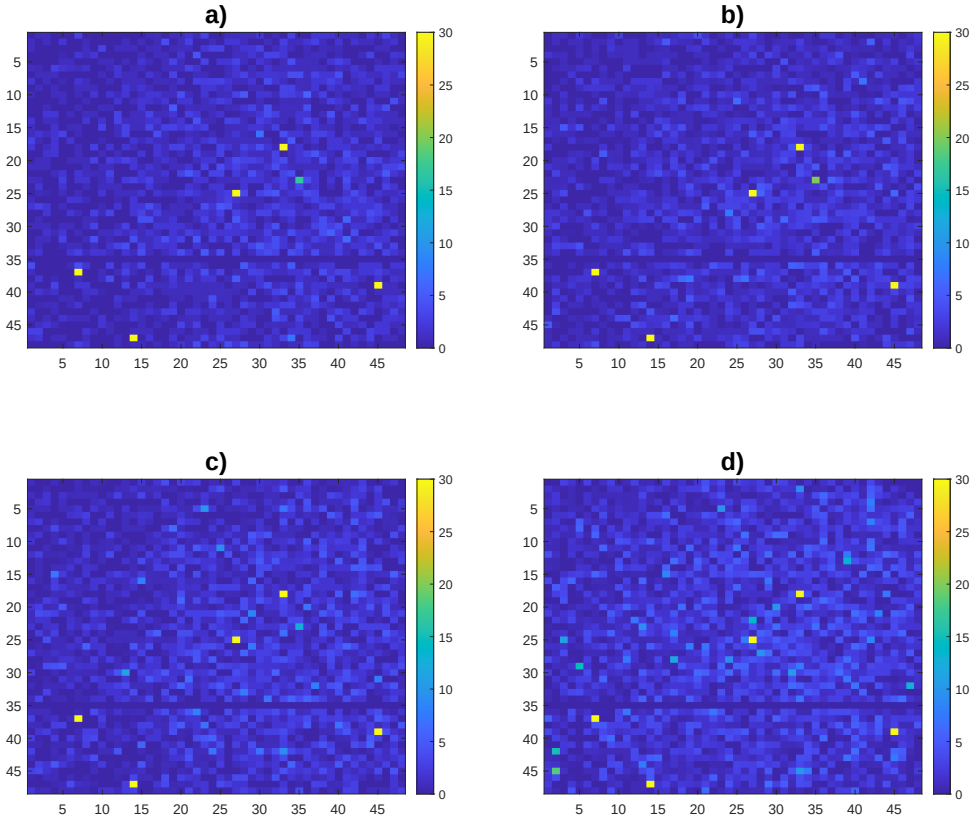


Figure 4.20. Heat map of pixel hits for array 1 obtained from the SiPM triggered measurement for a) $V_{EX} = 1.3\,V$, b) $V_{EX} = 1.8\,V$, c) $V_{EX} = 2.3\,V$, d) $V_{EX} = 2.8\,V$. As mentioned in Section 4.1, row 35 of chip D3 is a row of dead pixels.

of 21.5 V as displayed in Table 4.1.
In these trigger measurements, an increase in bias voltage results in a higher detection rate, as evidenced by the more pronounced difference in the cumulative distribution curves shown in Figure 4.22.
The rate of the disk-shaped ^{106}Ru source during the measurement was estimated to be 101 events/$(mm^2 s)$ based on the decay time. The SiPM, biased with a 2 V overvoltage, detected an average of 2.2 events/$(mm^2 s)$. Due to its placement beneath the APIX2LF chip, which is located further away from the source (as illustrated in Figure 4.14), there is a high probability that some particles do not reach the SiPM. As previously discussed for the "AllON" measurement, many factors contribute to the poor performance of the sensor with this radioactive source, such as the higher DCR caused by temperature increase and the energy levels of the source.

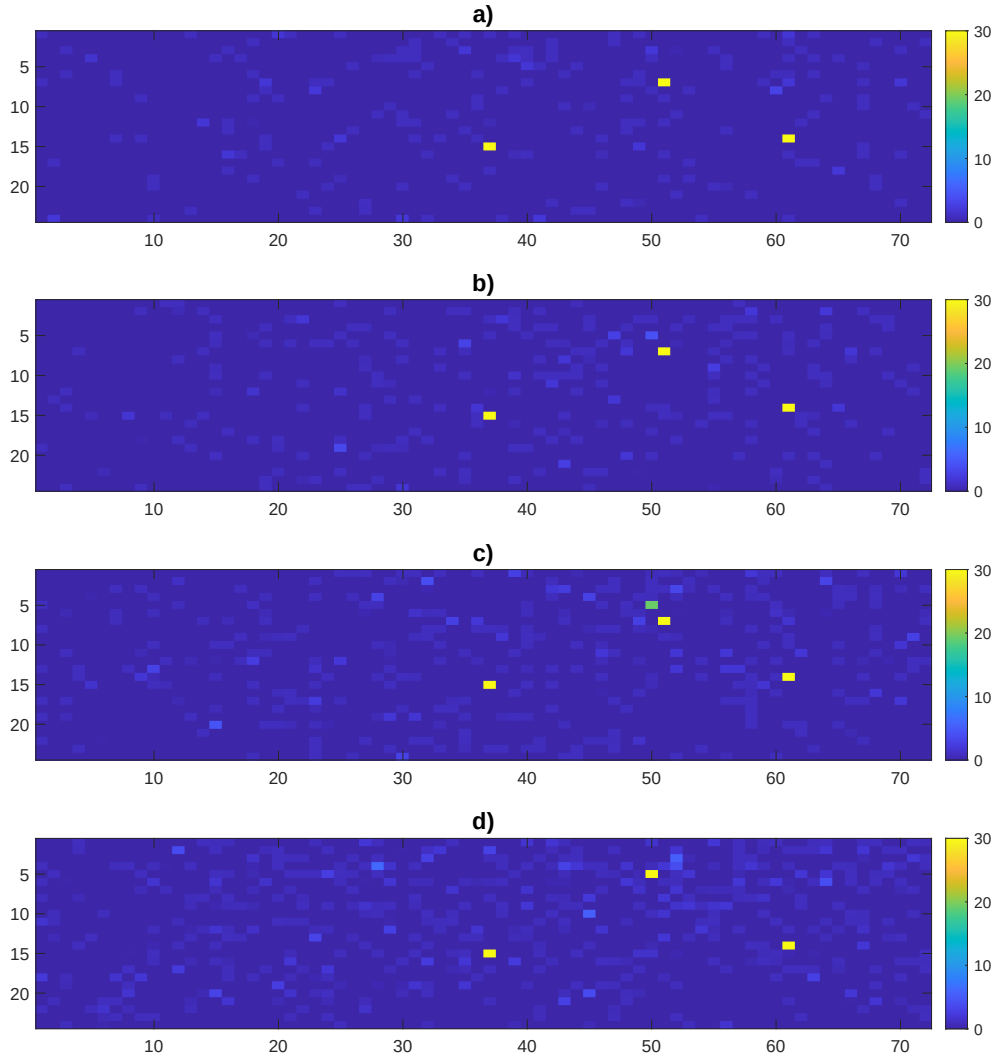


Figure 4.21. Heat map of pixel counts for array 3 obtained from the SiPM triggered measurement for a) $V_{EX} = 1.3\,V$, b) $V_{EX} = 1.8\,V$, c) $V_{EX} = 2.3\,V$, d) $V_{EX} = 2.8\,V$.

The results of these trigger measurements suggest that the APIX2LF chip has significant potential for use as a particle tracking sensor in medical applications. Using trigger signals, a better understanding of the performance of the chip at different bias voltages was obtained. However, in order to fully characterize the sensor and its capabilities, it is important to perform additional measurements with a greater number of trigger signals. By doing so, a longer live time can be obtained that is comparable to the TIT of the "AllON" mea-

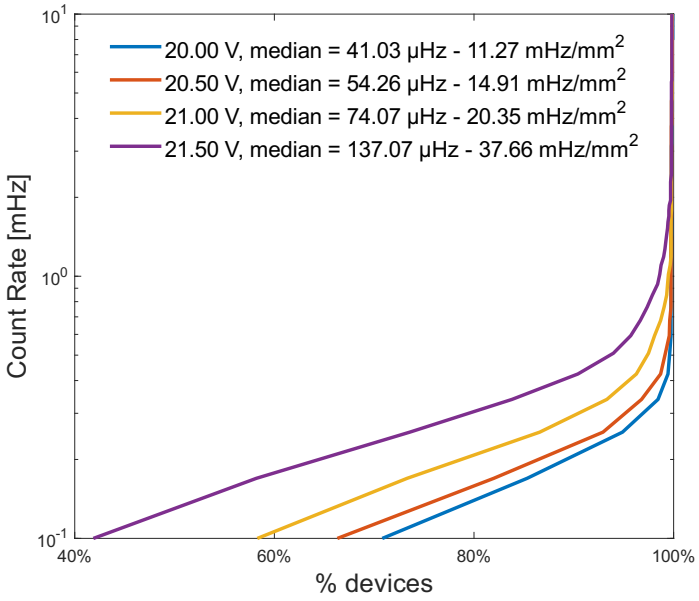


Figure 4.22. Count rate cumulative curves for SPADs of array 1 of D3 chip obtained from the SiPM triggered measurement for different excess voltages.

surement, allowing for more data to be gathered and for the sensor behavior to be analyzed in greater detail. Overall, these trigger measurements provide valuable insights into the performance of the APIX2LF chip and demonstrate its potential for use in a wide range of charged particle detector applications.

Conclusions

This dissertation presented the design and development of a charged particle imaging probe that employed the APIX2LF CMOS SPAD chip as the core sensor, the firmware developed for the microcontroller used to manage the probe and interface it to the PC, and the measurements carried out for testing the probe system functionality and the characterization of the CMOS SPAD detector.

The APIX2LF chip was developed as part of the APIX2/ASAP project, funded by the Italian Institute for Nuclear Physics (INFN), with the aim of creating a new generation of layered avalanche detectors for charged particles that reduce noise while having a low material budget. This position-sensitive detector, fabricated using 150 nm CMOS technology, comprises two-tier arrays of Single Photon Avalanche Diodes (SPADs) placed face-to-face and vertically interconnected through bump soldering joints. Due to the low probability of dark pulses simultaneously occurring in overlapping cells, the dark count rate is strongly reduced.

The imaging probe was designed to provide a flexible and all-in-one solution, with a battery-powered design that includes a microcontroller as an interface for wireless data transmission and the necessary circuitry for biasing, all integrated into the same board. Its application ranges from mapping the activity of laboratory sources to potential use in medical applications such as radio-guided surgery. Custom firmware was designed and developed to facilitate measurements of the APIX2LF chips, which were conducted using a custom-designed automatic data acquisition setup.

A comprehensive characterization campaign was conducted on six APIX2LF chips, comprising two dual-layer chips and four single-layer chips. The campaign aimed to extract the breakdown voltage as a function of temperature, measure the dark count rate at different temperatures, and investigate the contribution of crosstalk and Random Telegraph Signal (RTS) fluctuations to DCR.

The breakdown voltage extracted from the different chips ranged from 16.9 V to 18.9 V with a temperature coefficient of around 16 mV/°C, which is compatible with an N-well doping level of a few $10^{16} cm^{-3}$. Characterization measure-

ments carried out in a climatic chamber at temperatures ranging from -40°C to 70°C revealed that the dark count rate of the single-layer chips tended to double for every 10°C increase in temperature, while a higher ratio was observed for the dual-layer chips. A difference of almost three decades was found between the median values of the single-layer and dual-layer chips, demonstrating the benefits of the dual-layer structure. DCR measurements taken at different temperatures made it possible to extract activation energies at the single SPAD level. It was found that in SPADs with a high dark count rate, the dominant mechanism is trap-assisted tunneling, which was observed across the entire temperature range. Two predominant mechanisms were attributed to pixels with lower dark count rates: band-to-band tunneling at temperatures below 10°C and injection from the neutral region at higher temperatures. A few SPADs exhibiting high DCR were observed to significantly affect the DCR of the SPADs in the same array through crosstalk mechanisms. Identifying and disabling these pixels was beneficial for the overall performance of the device. RTS fluctuations were detected in the DCR of a significant number of SPADs, particularly in SPADs with the smaller size between the two that were considered in thesis work. The amplitude and time constants of the RTS fluctuations were found to be influenced by temperature.
A prototype board was developed and connected with a custom-designed carrier that houses a dual-layer APIX2LF chip. The breakdown voltage was extracted, and the dark count rate was characterized inside a dark chamber at room temperature. Additionally, tests were conducted using a ^{106}Ru beta-emitting source at the Physics Section of the Department of Physical Sciences, Earth and Environment of the University of Siena. The source activity at the time of measurement was estimated to be approximately 3.2 kBq, with beta particles having energies below 0.8 MeV. The measurements revealed a twofold difference between rate measurements with and without the source.
To ensure optimal performance of the APIX2LF in detecting low-energy particles, further measurements should be conducted at lower temperatures using a radioactive source with the developed setup. Moreover, three APIX2LF chips, including two single-layer and one dual-layer chips, were exposed to neutron radiation at the INFN Laboratori Nazionali di Legnaro. Measurements were also performed during the different steps of irradiation, thanks to the fast signal processing capabilities of the microcontroller. Currently, only a small portion of the data obtained from these measurements has been analyzed. In addition, post-irradiation measurements are also planned to be conducted using the developed setup to further investigate the effects of radiation and the underlying damage mechanism and to develop a model that predicts the distribution of DCR in SPADs.

Appendix A

Pin list of APIX2LF chip

Table A.1. Pin list.

#	Pad name	Function	Description
1	INIT1	Digital input	CSR1 inizialization signal
2	CK0	Digital input	RSR1 clock signal
3	INT0	Digital input	RSR1 inizialization signal
4	CONF	Digital input	RSR1 configuration signal
5	EN	Digital input	Enable pixel input signal
6	VDDIO1	Power	$1.8V$ for I/O circuits
7	GNDIO1	Power	GND for I/O circuits
8	DATARB	Digital input	Reset signal for the output latch (active low)
9	MEMRB	Digital input	Reset signal for the trigger latch (active low)
10	OUT0	Digital output	Bit0 pixel output signal - Array 1, rows 1-8
11	TRIG0	Digital output	Bit0 pixel trigger signal - Array 1, rows 1-8
12	OUT1	Digital output	Bit1 pixel output signal - Array 1, rows 9-16
13	TRIG1	Digital output	Bit1 pixel trigger signal - Array 1, rows 9-16
14	OUT2	Digital output	Bit2 pixel output signal - Array 1, rows 17-24
15	TRIG2	Digital output	Bit2 pixel trigger signal - Array 1, rows 17-24
16	VDDIO2	Power	$1.8V$ for I/O circuits
17	GNDIO2	Power	GND for I/O circuits
18	OUT3	Digital output	Bit3 pixel output signal - Array 1, rows 25-32
19	TRIG3	Digital output	Bit3 pixel trigger signal - Array 1, rows 25-32
20	OUT4	Digital output	Bit4 pixel output signal - Array 1, rows 33-40
21	TRIG4	Digital output	Bit4 pixel trigger signal - Array 1, rows 33-40
22	OUT5	Digital output	Bit5 pixel output signal - Array 1, rows 41-48
23	TRIG5	Digital output	Bit5 pixel trigger signal - Array 1, rows 41-48
24	VDD1	Power	$1.8V$ for circuits the Array 1
25	GND1	Power	GND for circuits the Array 1

26	GND3	Power	GND for circuits the Array 3
27	VDD3	Power	1.8V for circuits the Array 3
28	VSPAD1	Voltage reference	Cathode voltage for SPADs in the Array 1
29	VSPAD3	Voltage reference	Cathode voltage for SPADs in the Array 3
30	VDDIO3	Power	1.8V for I/O circuits
31	GNDIO3	Power	GND for I/O circuits
32	OUT6	Digital output	Bit6 pixel output signal - Array 3, rows 1-8
33	TRIG6	Digital output	Bit6 pixel trigger signal - Array 3, rows 1-8
34	OUT7	Digital output	Bit7 pixel output signal - Array 3, rows 9-16
35	TRIG7	Digital output	Bit7 pixel trigger signal - Array 3, rows 9-16
36	OUT8	Digital output	Bit8 pixel output signal - Array 3, rows 17-24
37	TRIG8	Digital output	Bit8 pixel trigger signal - Array 3, rows 17-24
72	VDD33	Power	3.3V for circuits in the Array 4 (active quenching structure)
73	GND33	Power	GND for circuits in the Array 4 (active quenching structure)
74	INIT3/INIT4	Digital input	CSR3/RSR2 inizialization signal
75	CK3/CK4	Digital input	CSR3/RSR2 clock signal
76	OUTTS	Digital output	Pixel output for the test structure
77	GNDIO4	Power	GND for I/O circuits
78	VDDIO4	Power	1.8V for I/O circuits
79	VSPAD4	Voltage reference	Cathode voltage for SPADs in the Array 4
80	VCLAMP	Voltage reference	Gate voltage of the clamping transistor (1.8V)
81	VQ	Voltage reference	Gate voltage of the quenching transistor
82	VSPAD2	Voltage reference	Cathode voltage for SPADs in the Array 2
83	VDD4	Power	1.8V for circuits the Array 4 (test structure)
84	GND4	Power	GND for circuits the Array 4 (test structure)
85	GND2	Power	GND for circuits the Array 2
86	VDD2	Power	1.8V for circuits the Array 2
87	OUTC0	Digital output	Bit0 counter output - Array 2
88	OUTC1	Digital output	Bit1 counter output - Array 2
89	OUTC2	Digital output	Bit2 counter output - Array 2
90	OUTC3	Digital output	Bit3 counter output - Array 2
91	OUTC4	Digital output	Bit4 counter output - Array 2
92	GNDIO5	Power	GND for I/O circuits
93	VDDIO5	Power	1.8V for I/O circuits
94	OUTC5	Digital output	Bit5 counter output - Array 2
95	OUTC6	Digital output	Bit6 counter output - Array 2
96	OUTC7	Digital output	Bit7 counter output - Array 2
97	OUTC8	Digital output	Bit8 counter output - Array 2
98	OUTC9	Digital output	Bit9 counter output - Array 2

99	INTEG/SPOFF0	Digital input	Counter logic integration signal/hold-off time control bit0
100	COLR/SPOFF1	Digital input	Counter column reset/hold-off time control bit1
101	TESTB	Digital input	Circuitry test signal (active low)
102	GNDIO6	Power	GND for I/O circuits
103	VDDIO6	Power	$1.8V$ for I/O circuits
104	ENRB	Digital input	Cells global reset (active low)
105	DATATX	Digital input	Data transmission signal
106	S1	Digital input	Output pulse duration control bit1
107	S0	Digital input	Output pulse duration control bit0
108	INIT2	Digital input	CSR2 inizialization signal
109	CK2	Digital input	CSR2 clock signal
144	CK1	Digital input	CSR1 clock signal

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