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Doctoral Thesis

Low-Noise Amplifiers for 60-GHz Wireless Communications in CMOS and BiCMOS Technologies

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Abstract

The continuous growth of high-speed wireless applications such as virtual reality, wireless HD video streaming, and short-range multi-gigabit data links has driven increasing interest toward millimeter-wave (mm-wave) communication systems operating in the unlicensed 60-GHz band (57–64 GHz). The large available bandwidth enables multi-Gbit/s data rates; however, the realization of compact, energy-efficient, and robust receiver front-ends at these frequencies presents significant circuit and layout challenges, including low supply voltage operation, noise optimization, impedance matching, electrostatic discharge (ESD) protection, linearity under strong blockers, and strict control of layout parasitics in advanced silicon technologies. This thesis presents the design, implementation, and experimental validation of 60-GHz integrated receiver front-end circuits in 28-nm CMOS and 130-nm SiGe BiCMOS technologies, addressing low-power/wideband operation and enhanced linearity, respectively. The first part of the thesis is focused on the design of a 60-GHz low-noise amplifier (LNA) for multigigabit/s communications in a 28-nm bulk CMOS technology by TSMC, featuring a 9-metal back-end-of-line (BEOL) stack including a 3.5-µm thick top metal layer and an Alucap option for low-loss passive integration. A pseudo-differential two-stage LNA topology is proposed as the best performance tradeoff (i.e., gain, frequency bandwidth, power consumption). Specifically, a power-efficient simultaneous noise and impedance matching (*PE-SNIM*) technique is adopted together with custom-designed stacked transformers providing impedance transformation, resonance tuning, and intrinsic ESD robustness. The LNA has been integrated as a stand-alone block for direct on-wafer experimental validation, by using a 50-Ohm buffer stage. Moreover, it has been used within a complete 60-GHz receiver to drive a fully differential on-off keying/amplitude shift keying (OOK/ASK) demodulator, enabling a data rate of about 3 Gbit/s at a sensitivity of -40 dBm with total power consumption below 15 mW by using a 0.9-V supply. Both the LNA and the complete receiver have been fabricated. Experimentally characterization through on-wafer measurements has been carried out for the LNA, which confirms a correct operation around 60 GHz (with about 6% frequency drift). On the other hand, a limited validation of the OOK receiver is available, due to a lack of some instruments for high-data rate modulation at 60 GHz. The second part of the thesis focuses on linearity enhancement through the design of a highly linear 60-GHz LNA implemented in 130-nm SiGe BiCMOS technology by Infineon Technologies, characterized by a 6-metal stack and high-speed heterojunction bipolar transistors (HBTs).

A novel two-path power-combining architecture is proposed, exploiting passive load redistribution and transformer-based current combining to improve large-signal performance without dynamic bias control. Post-layout simulations demonstrate up to 6-dB improvement in input 1-dB compression point (IP_{1dB}) compared to a conventional two-stage topology, while maintaining competitive gain, *NF*, and moderate power consumption. The layout has been completed and verified through electromagnetic and parasitic extraction simulations, and fabrication is currently in progress. Fabricated chips could be available for on-wafer experimental validation in a few months. Overall, this work demonstrates that advanced bulk CMOS and SiGe BiCMOS technologies can effectively address complementary challenges in 60-GHz receiver design (namely low-power operation in nanoscale CMOS and high linearity in SiGe BiCMOS implementations). The proposed circuit architectures and layout methodologies provide practical guidelines for the realization of compact, low-power, and blocker-tolerant mm-wave front-ends for next-generation high-data-rate wireless systems.

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1 Introduction

1.1 Motivation

Wireless communication has seen exponential growth in recent years, driven by the increasing demand for high-speed data transfer across various applications, including mobile networks, satellite communication, and wireless local area networks (WLANs). As the volume of data being transmitted continues to rise, new communication technologies are being explored to meet the requirements for higher data rates and reduced latency. The 60-GHz frequency band, due to its large available bandwidth (57 GHz to 64 GHz), offers a promising solution for enabling high-speed, short-range wireless communication.

The 60-GHz band has gained significant attention for its potential to support data rates in the gigabit-per-second (Gbit/s) range, making it ideal for high-performance applications such as wireless HD video streaming, virtual reality, and Internet of things (IoT) devices. Despite this potential, the implementation of receiver front-end circuits at 60 GHz presents several challenges. The realization of compact, energy-efficient, and reliable circuits at these frequencies requires addressing multiple design constraints simultaneously. These include operation under low supply voltage, noise optimization, impedance matching, and robustness against electrostatic discharge (ESD). In addition, maintaining linearity in the presence of strong interfering signals and managing layout parasitics in advanced silicon technologies further complicate the design process.

Different semiconductor technologies offer distinct advantages in addressing these challenges. Advanced CMOS technologies enable low-power and highly integrated solutions, making them suitable for energy-efficient receiver designs. On the other hand, SiGe BiCMOS technologies provide improved large-signal performance, which is beneficial for enhancing circuit linearity.

In this context, there is a need for circuit solutions that can effectively address both low-power operation and linearity requirements while maintaining compactness and robustness. This thesis is motivated by the design and validation of 60-GHz receiver front-end circuits in CMOS and BiCMOS technologies, aiming to explore their respective capabilities in meeting the demands of next-generation high-data-rate wireless systems.

1.2 Research Objectives

The main objective of this thesis is to design, implement, and experimentally validate 60-GHz receiver front-end circuits using advanced CMOS and SiGe BiCMOS technologies, with emphasis on low-power operation, wideband performance, and enhanced linearity.

To achieve this goal, the specific objectives of this work are summarized as follows:

- **Design of a CMOS-based 60-GHz LNA:** To develop a low-noise amplifier in 28-nm CMOS technology targeting multi gigabit-per-second communication, focusing on achieving an appropriate trade-off between gain, bandwidth, and power consumption.
- **Implementation of a complete receiver front-end:** To integrate the designed LNA within a 60-GHz receiver architecture, including a fully differential OOK/ASK demodulator, and demonstrate high data-rate operation with low power consumption and adequate sensitivity.
- **Adoption of advanced design techniques:** To employ simultaneous noise and impedance matching techniques and transformer-based passive structures to enhance circuit performance and ensure robustness, including intrinsic ESD protection.
- **Design of a highly linear BiCMOS LNA:** To develop a 60-GHz LNA in 130-nm SiGe BiCMOS technology with improved large-signal performance, using a two-path power-combining architecture based on passive load redistribution and transformer-based current combining.
- **Performance validation:** To evaluate the proposed circuits through post-layout simulations and experimental characterization, where available, to verify their operation at 60 GHz.
- **Technology comparison:** To investigate how CMOS and BiCMOS technologies address complementary challenges, particularly in terms of low-power operation and linearity performance.

1.3 Thesis Structure

This thesis is organized into seven chapters, each addressing a specific aspect of the design and analysis of mm-wave receiver front-end circuits for 60-GHz wireless communication systems.

Chapter 1 introduces the research context, outlining the motivation behind the work, the main objectives, and the overall organization of the thesis.

Chapter 2 presents a comprehensive literature review. It begins with an overview of high-speed wireless communication systems and the characteristics of the 60-GHz band. It then reviews state-of-the-art receiver architectures, with particular emphasis on CMOS implementations, and discusses key challenges such as power consumption, sensitivity, and robustness. The chapter also addresses ESD protection techniques in mm-wave CMOS integrated circuits.

Chapter 3 describes the system architecture and design considerations with primary emphasis on the proposed low-power wideband 60-GHz LNA. The chapter outlines the design methodology, including topology selection and the adoption of power-efficient simultaneous noise and impedance matching (*PE-SNIM*) technique. In addition, preliminary design investigations are presented to identify the most suitable architecture for the targeted LNA. In particular, single-stage and two-stage LNA topologies are analyzed and compared in terms of gain, bandwidth, noise performance, and power consumption, leading to the selection of the optimal design solution. Special attention is given to transformer-based passive components and layout-aware design strategies. Although the LNA is intended for integration within an OOK/ASK receiver, the focus remains on its capability to achieve an optimal trade-off between performance metrics while ensuring compatibility with subsequent stages.

Chapter 4 presents the implementation and performance evaluation of the proposed 60-GHz LNA. Detailed circuit design, layout considerations, and post-layout simulation results are discussed. A simplified OOK/ASK demodulator is considered only as a load to validate the ability of the LNA to effectively drive the next stage in a receiver chain. The analysis highlights the suitability of the proposed LNA for OOK-based receiver architectures, demonstrating its capability to operate under low-voltage and low-power constraints while maintaining adequate signal integrity.

Chapter 5 focuses on testing and experimental characterization. It describes the measurement setup, on-wafer testing procedures, and compares the measured results with post-layout simulations to validate the proposed designs.

Chapter 6 introduces a highly linear 60-GHz LNA implemented in 130-nm SiGe BiCMOS technology. It presents the proposed power-combining architecture, design methodology, and post-layout simulation results, emphasizing improvements in large-signal performance and linearity.

Chapter 7 concludes the thesis by summarizing the main contributions and findings. It also outlines potential directions for future research in the field of millimeter-wave integrated circuit design.

2 Literature Review

2.1 High-Speed Wireless Communication and the 60-GHz Band

2.1.1 Historical Context

The evolution of wireless communication has been marked by significant advancements over the past few decades, driven primarily by the growing demand for faster data transmission and more reliable connectivity. Early wireless communication systems, such as analog radio and early mobile networks, were limited in both data rate and coverage. However, with the development of digital modulation techniques and advancements in semiconductor technology, wireless communication has evolved to support increasingly higher data rates and more sophisticated applications [1, 2].

The transition from 2G to 3G introduced data-centric services, including basic mobile Internet. With the arrival of 4G, wireless communication achieved substantial improvements in speed, enabling mobile broadband and seamless multimedia streaming [3]. Now, as 5G networks are being deployed, the focus has shifted to ultra-high-speed data transmission, low latency, and support for a massive number of connected devices [4].

Amid these developments, high-speed applications such as HD video streaming, augmented and virtual reality (AR/VR), and the Internet of Things (IoT) have emerged as key drivers of innovation. To meet the stringent requirements of these applications, researchers have turned to the millimeter-wave (mm-wave) frequency spectrum, specifically the 60-GHz band, which offers large bandwidth and high data rates. This shift represents a fundamental change in wireless communication, as it aims to achieve multi Gbit/s data rates for short-range, high-speed connectivity [5].

2.1.2 60-GHz Band Characteristics

The 60-GHz frequency band, part of the mm-wave spectrum, has gained significant attention for high-speed wireless communication due to its unique characteristics and advantages. One of the primary reasons for its suitability is the large bandwidth available in this band. The 60-GHz band typically spans from 57 GHz to 64 GHz, offering up to 7 GHz of unlicensed spectrum in many regions, including the United

States and Europe [5]. This wide bandwidth enables the support of data rates in the multi Gbit/s range, making it highly attractive for applications requiring fast and reliable data transfer.

Key Features of the 60-GHz Band:

- High Data Rate Capability

The wide bandwidth of 7 GHz allows for the implementation of high-speed modulation schemes, such as on-off keying (OOK) and amplitude shift keying (ASK), which are essential for achieving data rates exceeding several Gbps [3]. This makes the 60-GHz band ideal for applications like wireless HD video streaming, virtual reality (VR), and high-speed data backhaul.

- Short-Range Communication

The 60-GHz signals experience significant atmospheric absorption, particularly by oxygen molecules, resulting in a propagation loss of approximately 15 dB/km. This natural limitation confines the effective range to a few meters, which is advantageous for short-range, high-capacity wireless links, such as indoor data transfer and device-to-device communication [1].

- Directional Communication and Spatial Reuse

The small wavelength (approximately 5 mm) at 60 GHz facilitates the design of compact antenna arrays that support highly directional beamforming. This property helps mitigate interference, improves signal quality, and allows for spatial reuse of the frequency band, enhancing overall network capacity [6].

- Unlicensed Spectrum and Regulatory Support

Many countries have allocated the 60-GHz band for unlicensed use, simplifying regulatory compliance for commercial applications. This has encouraged the development of standards such as IEEE 802.11ad and IEEE 802.11ay, which leverage the band for ultra-high-speed WiGig (wireless gigabit) communication [7].

2.1.3 Applications and Challenges

The 60-GHz band is highly suitable for applications that demand ultra-high data rates and minimal latency. Some of the prominent applications include:

- Wireless HD Video Streaming: The 60-GHz band's ability to handle multi Gbit/s data rates makes it ideal for streaming uncompressed or minimally compressed HD video content, especially in smart home setups and wireless docking stations [8].

- Virtual Reality (VR) and Augmented Reality (AR): The low latency and high data throughput are crucial for VR/AR applications, where real-time transmission of high-quality visual data is essential for immersive user experiences.

- Internet of Things (IoT): The short-range, high-speed connectivity provided by the 60-GHz band supports data-intensive IoT applications, including smart appliances and industrial automation [9].

- Wireless Backhaul: In cellular networks, the 60-GHz band can be used for short-range wireless backhaul links, connecting small cells to core networks with minimal latency [10].

- Wireless Personal Area Networks (WPANs): Standards such as IEEE 802.11ad and IEEE 802.11ay utilize the 60-GHz band to enable ultra-high-speed data transfer between personal devices in close proximity [11].

While the 60-GHz band offers substantial benefits, it also presents challenges such as high path loss, limited range, and sensitivity to obstacles. Addressing these issues requires efficient receiver design, robust modulation schemes, and advanced signal processing techniques to maintain reliable communication in real-world environments. The promising characteristics of the 60-GHz band, particularly its ability to support high data rates over short distances, make it an essential enabler for next-generation wireless communication systems.

2.2 State-of-the-Art in 60-GHz Receiver Architectures

The rapid advancement of wireless communication technologies has driven the need for high-speed data transmission over short distances [12]. The 60-GHz frequency band, with its wide bandwidth and unlicensed spectrum, has emerged as a promising solution for achieving multi Gbit/s data rates. To meet the performance and integration requirements of such applications, extensive research has focused on developing energy-efficient 60-GHz receiver architectures in CMOS technology. Designing such receivers in nanometer CMOS processes presents several challenges, including managing high-frequency signal integrity, minimizing power consumption, ensuring thermal stability, and achieving robustness against process-voltage-temperature (PVT) variations [13]. Nevertheless, the progressive scaling of CMOS technology to nodes below 28 nm has significantly improved its capability to operate at mm-wave frequencies, narrowing the performance gap with silicon-germanium (SiGe) technologies while enabling low-cost, high-volume integration [14].

Several receiver architectures have been explored to address these challenges [15]. Traditional heterodyne receivers offer excellent image rejection and frequency selectivity by down-converting the radio frequency (RF) signal to an intermediate frequency (IF), but they require high-frequency local oscillators (LOs) and complex filtering, leading to increased power consumption and implementation complexity [16]. Direct-conversion receivers simplify the architecture by directly down-converting the RF signal to baseband, which facilitates integration and supports wideband operation, though they suffer from DC offset, flicker noise, and I/Q imbalance [17]. Alternative approaches such as sliding-IF receivers offer a compromise between heterodyne and direct-conversion designs, but they face limitations such as spurious mixing and harmonic distortion [18]. Sub-sampling receivers further reduce complexity by sampling the RF signal directly at a fraction of the carrier frequency; however, they are sensitive to sampling jitter and require fast analog-to-digital converters (ADCs) [19].

Within this landscape, non-coherent OOK/ASK receivers have gained considerable popularity due to their inherent simplicity and low power consumption compared to coherent modulation schemes such as quadrature phase shift keying (QPSK) or quadrature amplitude modulation (QAM) [20]. OOK/ASK modulation, which transmits data through the presence or absence of the carrier signal, is compatible with low-complexity circuits and supports non-coherent demodulation. As a result, OOK/ASK-based receivers do not require a local oscillator (LO), while transmitters are free from the complexity of generating a stable RF carrier using a phase-locked loop (PLL) [21, 22]. This architectural simplicity makes OOK/ASK highly attractive for power-constrained applications, particularly in short-range mm-wave systems.

Many 60-GHz OOK receivers, implemented in both BiCMOS and CMOS technologies, adopt a widely used architecture consisting of a broadband low-noise amplifier (LNA) followed by an OOK demodulator, typically realized through an envelope detector (ED) and a baseband limiting amplifier [21, 23–28], as depicted in Figure 2.1. These designs focus on minimizing the energy per bit at the lowest acceptable input signal level, or sensitivity. State-of-the-art receivers achieve sensitivities between -35 dBm and -25 dBm at a bit error rate (BER) of 10^{-12}, with energy per bit values typically around 10 pJ/bit and best cases below 5 pJ/bit. Power consumption, which scales with data rate, remains below 20 mW in many efficient designs operating at Gbit/s speeds.

From a circuit perspective, single-ended topologies are frequently employed in the mm-wave front-end, including both the LNA and demodulator, to minimize power, reduce area, and avoid the need for single-ended to differential conversion at high frequencies. In contrast, baseband stages often leverage differential topologies for improved

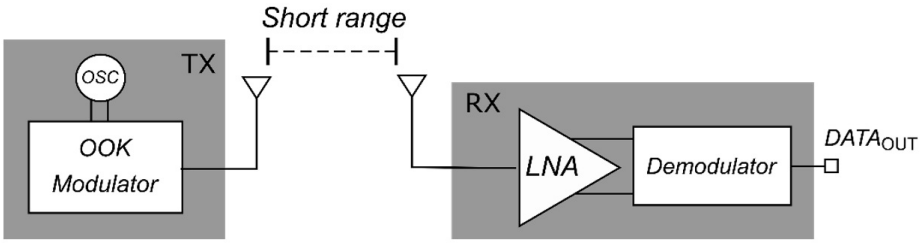


Figure 2.1: Typical block diagram of a 60-GHz OOK transceiver for Gbit/s communications.

common-mode noise rejection and power supply immunity. Modern LNA implementations rely on multi-stage designs [23, 26], sometimes with up to five or six stages to achieve high gain and broad bandwidth. These configurations, however, increase susceptibility to stability issues. Moreover, techniques such as g_m-enhancement are applied to partially mitigate the intrinsic transconductance limitations of nanometer CMOS devices, especially in bulk technologies.

Despite their performance, many published designs pay insufficient attention to robustness under real-world conditions, particularly regarding ESD protection and resilience to PVT variations. Calibration techniques are often employed to compensate for these non-idealities, yet they introduce additional complexity and may not be practical in low-cost or space-constrained implementations. Recent trends therefore emphasize design methodologies that inherently enhance robustness without relying on post-fabrication calibration. These include fully differential topologies to suppress common-mode disturbances, adaptive biasing schemes, and layout-aware techniques such as symmetrical routing, guard rings, and electromagnetic-aware placement to mitigate parasitic effects and substrate coupling. Post-layout optimization has become an essential step, enabling more accurate prediction of circuit behavior and preserving signal integrity.

In summary, the evolution of 60-GHz CMOS receivers reflects a clear trajectory toward low-power, compact, and highly integrated solutions. While various architectures, including heterodyne, direct-conversion, sliding-*IF*, and sub-sampling, offer different trade-offs, OOK-based receivers stand out for their simplicity and efficiency. As the demand for short-range, high-data-rate wireless links continues to grow, ongoing innovations in circuit design, process technology, and system integration will be pivotal in addressing the stringent requirements of next-generation mm-wave applications.

2.3 ESD Protection in Millimeter-Wave CMOS ICs

Electrostatic discharge (ESD) protection is a critical aspect of IC design, especially in high-frequency and mm-wave systems, where traditional ESD strategies may compromise *RF* performance. In CMOS technologies operating at mm-wave frequencies such as the 60-GHz band, designing robust ESD protection becomes increasingly challenging due to parasitic capacitance, inductance, and resistance associated with ESD structures, which can significantly degrade signal integrity and noise performance [29].

Integrated circuits are vulnerable to damage from electrostatic discharge events during manufacturing, packaging, testing, and field handling. ESD stress can result in catastrophic failure or latent damage, reducing product reliability. In mm-wave CMOS ICs, input/output (I/O) pads are particularly susceptible, necessitating the integration of ESD protection devices that can withstand human body model (*HBM*) and charged device model (CDM) discharges [30].

Traditional ESD protection structures, such as large diodes or thick-oxide MOS devices, introduce substantial parasitic capacitance and inductance. While acceptable in low-frequency designs, these parasitics can severely degrade signal integrity, bandwidth, and noise performance at mm-wave frequencies. Specific challenges include:

- High Parasitic Capacitance: Even a few femtofarads of added capacitance can significantly detune impedance matching networks and reduce the gain and noise performance of sensitive front-end components like LNAs.
- Inductive Effects: ESD structures can also add unwanted inductance, leading to resonances or impedance discontinuities at mm-wave frequencies.
- Layout Constraints: The physical placement of ESD structures must be carefully considered to minimize signal path discontinuities and maintain symmetry, especially in differential designs.
- Process Limitations: In advanced nodes such as 28-nm CMOS, the ESD robustness of thin-oxide devices is inherently lower, making effective ESD design even more critical.

Therefore, ESD protection in mm-wave CMOS ICs must be carefully co-optimized with the *RF* front-end. Common approaches include stacked diodes [31], embedded protection within passive structures such as transformers [32], and snapback-based schemes that balance ESD robustness with *RF* transparency [33]. These techniques must be validated through simulation and measurement to ensure both ESD reliability and *RF* performance.

3 System Architecture and Design Considerations

The design of high-performance, low-power mm-wave receivers strongly relies on the capabilities of the front-end LNA, which dominates the overall sensitivity, bandwidth, and power consumption of the system. In this work, the primary focus is on the design of a low-power wideband 60-GHz LNA in 28-nm CMOS technology, targeting short-range high-speed wireless communication applications.

Although the LNA is developed within the context of a 60-GHz OOK receiver, the emphasis of this chapter is on the LNA architecture and design methodology. The receiver is considered only to define system-level requirements and to validate the ability of the proposed LNA to effectively drive a subsequent demodulator stage. The design of the proposed LNA requires an accurate evaluation of the 28-nm bulk CMOS technology capabilities in terms of both active and passive components at mm-wave frequencies. Specifically, low-voltage-threshold (LVT) transistors were preferred, trading slightly reduced performance for improved reliability, while the "110G model" was adopted to ensure higher accuracy in circuit simulations, albeit with reduced flexibility in transistor sizing within the LNA design. For electromagnetic (EM) simulations, the authorized back-end-of-line (BEOL) description of the technology was employed for the design of passive components. Since no inductors or transformers are provided in the design kit (DK), custom passive components had to be developed. This required a preliminary study of the design rule manual (DRM) to ensure compliance with fabrication constraints and to enable the implementation of high-performance inductors and transformers suitable for mm-wave operation. The overall system includes an LNA followed by an OOK/ASK demodulator. However, the primary focus of this work is on the design and optimization of the LNA, which is responsible for achieving the required sensitivity, bandwidth, and power efficiency. The LNA is optimized for low *NF*, high gain, and proper input matching at 60 GHz, while ensuring compatibility with integrated ESD protection and the ability to directly drive the demodulator stage.

This chapter begins with a brief overview of the receiver architecture to define the system-level requirements. It then focuses on the design challenges and methodology of the proposed 60-GHz LNA, including the adoption of power-efficient simultaneous noise and impedance matching (*PE-SNIM*) technique and transformer-based passive structures. Finally, preliminary design investigations are presented, where single-stage

and two-stage LNA topologies are analyzed and compared to identify the most suitable architecture for a low-power wideband implementation capable of effectively driving an OOK/ASK demodulator.

3.1 Design Perspective on the 60-GHz Receiver Architecture

The target application of the proposed LNA is a low-power 60-GHz receiver operating in the unlicensed 57–64 GHz band, which supports multi-Gbit/s data rates and is well suited for short-range wireless communication applications such as high-speed chip-to-chip links, virtual/augmented reality systems, and wireless HD video streaming. In this work, OOK/ASK modulation schemes are adopted due to their inherent simplicity and suitability for ultra-low-power implementations, as discussed in Section 2.2. These modulation schemes enable non-coherent receiver architectures that avoid the need for local oscillators and frequency synthesis, significantly reducing system complexity and power consumption.

A preliminary high-level block diagram of the targeted receiver is shown in Figure 3.1. The architecture consists of a front-end LNA followed by an OOK/ASK demodulator. In this signal chain, the LNA plays a key role, as it must amplify the weak received *RF* signal while preserving signal integrity and minimizing noise degradation. From a system-level perspective, the LNA must satisfy several critical requirements. It must provide sufficient gain to ensure that the input signal of the demodulator exceeds the minimum detection threshold at the targeted sensitivity level. At the same time, it must guarantee a wide bandwidth to support multi-Gbit/s data rates, while maintaining a low noise figure (*NF*) to meet the required sensitivity of -40 dBm. In addition, the LNA must operate under strict power constraints (below 15 mW total receiver power) and be compatible with low-voltage operation (0.9 V supply). The signal chain begins with an antenna-coupled input, typically interfaced through an integrated transformer that provides impedance transformation and contributes to ESD protection. The amplified *RF* signal is then delivered to a simplified OOK/ASK demodulator, which performs envelope detection and baseband signal recovery. The internal implementation details of the demodulator are not the focus of this work and are therefore not discussed in detail, as it is only used to validate the capability of the proposed LNA to drive a realistic load.

The preliminary specifications of the receiver are summarized in Table 3.1. The system targets a data rate above 1 Gbit/s with a bit error rate of 10^{-12} at a sensitivity of -40 dBm, while operating from a 0.9-V supply with total power consumption below

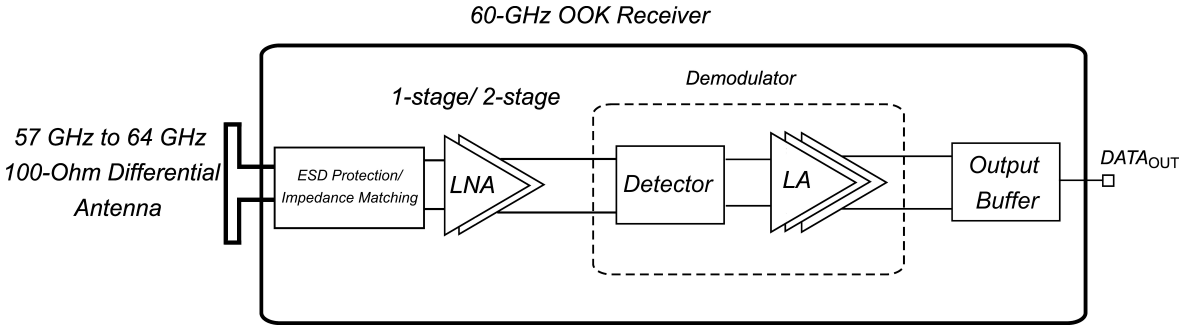


Figure 3.1: Simplified preliminary block diagram of the targeted 60-GHz OOK receiver.

15 mW. These requirements impose stringent constraints on the LNA design, particularly in terms of gain, bandwidth, noise performance, and power efficiency. Based on these system-level considerations, the design of the LNA becomes the key challenge, as it determines the achievable sensitivity, bandwidth, and overall performance of the receiver. The following section therefore focuses on the detailed design and optimization of the proposed 60-GHz LNA.

Table 3.1: Preliminary RX specifications.

Parameter	Value	Unit
Carrier Frequency	60	GHz
Data Rate	> 1	Gbit/s
Modulation	OOK	-
Bit Error Rate (BER)	10^{-12}	-
Sensitivity ($P_{\mathrm{IN,\,MIN}}$)	-40	dB
Maximum Input Signal ($P_{\mathrm{IN,MAX}}$)	-15	dBm
Supply Voltage (V_{DD})	0.9	V
Power Consumption	< 15	mW
Technology	28-nm bulk CMOS (by TSMC)	-
BEOL	8 Metals (M8–M7: 1.15-μm thick)	-
Differential Antenna	$R_{\mathrm{S}} = 100$	Ω
ESD Protection	Yes	-

3.2 60-GHz LNA Description

The LNA is a critical component in the front-end of any receiver system, especially in mm-wave applications where signal attenuation and noise are significantly pronounced. For the 60-GHz receiver presented in this thesis, the LNA is designed to provide high gain, low *NF*, and good input matching, all while maintaining ultra low power consumption in a 28-nm CMOS process. Therefore, the LNA must guarantee impedance

matching to the antenna and deliver sufficiently high signal to the demodulator, while producing the lowest possible degradation of the signal-to-noise ratio (*SNR*) at the constrained power budget. Theoretically, the minimal signal to noise ratio, SNR_{MIN}, required for correct OOK demodulation is 17 dB. Of course, a proper implementation margin of about 5 dB must be added when non-ideal OOK modulation is considered. In this context, the noise budget can be calculated by means of the well-known equation that predicts the receiver's sensitivity i.e., the minimum input signal, $P_{\mathrm{IN,\,MIN}}$ [dBm], that yields the SNR_{MIN} for correct OOK demodulation, that is reported below for the sake of completeness:

$$P_{\mathrm{IN,MIN}} = -174 \text{ dBm/Hz} + NF + 10\log(BW) + SNR_{\mathrm{MIN}} \tag{3.1}$$

being *NF* the receiver noise figure and *BW* its *RF* bandwidth. Considering the overall available 7-GHz unlicensed bandwidth, a sensitivity of -40 dBm, and a SNR_{MIN} of 23 dB, then a *NF* lower than 12.5 dB is required for the receiver. As far as the LNA gain is concerned, a value of 19-20 dB was calculated by considering the minimum signal level that must be delivered to the detector at sensitivity level.

The LNA topology is of utmost importance to optimize RX performance. Very compact one- or two-stage LNAs are preferable to more popular multi-stage topologies, being less sensitive to undesired oscillations in a complete receiver while achieving a higher 1-dB input compression point (IP_{1dB}). However, achieving sufficiently high gain and wide frequency bandwidth becomes more challenging when the number of amplification stages is low. The research activity was focused on the comparison between single-stage and two-stage LNA topologies, in view of the integration in the receiver architecture shown in Figure 3.1.

Most mm-wave CMOS LNAs use the single-ended architecture for lower power consumption and silicon area [34–36], but this choice does not guarantee enough robustness against common-mode noise coming from the substrate and/or voltage supply, while hardily facing the ESD issue. For this reason, only differential-like topologies were considered in the design. Moreover, traditional mm-wave CMOS LNA design techniques often overlook strict current budget constraints when achieving simultaneous noise and impedance matching. To address this limitation, a power-efficient simultaneous noise and impedance matching (*PE-SNIM*) technique with source impedance transformation has been proposed for the input stage of the LNA [37], as will be detailed in the following sections.

3.2.1 State-of-the-Art Design Strategies of *RF*/mm-Wave CMOS LNAs

The sensitivity of *RF*/mm-wave receivers is typically dominated by the LNA, especially by its first stage, which is directly connected to the antenna. Several trade-offs between *NF*, gain, impedance matching, linearity, and power consumption are involved in the LNA design [38]. In the literature, four design optimization techniques have been proposed: classical noise matching (*CNM*) [39], simultaneous noise input matching (*SNIM*) [40], power-constrained noise optimization (*PCNO*) [41], and power-constrained simultaneous noise input matching (*PCSNIM*) [42]. Although the reference topology for the LNA is the common-source (CS) amplifier, the cascode (CAS) topology, shown in Figure 3.2a, is widely adopted thanks to its large bandwidth, high gain, and especially high reverse isolation. In the following, LNA design optimization techniques are briefly discussed.

The *CNM* technique is aimed at achieving the lowest *NF* of the specified technology. However, it does not guarantee the input matching since the input impedance, Z_{IN}, is considerably different from the optimum noise impedance, Z_{OPT}, for both real and imaginary components. This drawback is overcome by the very popular *SNIM* technique. It is based on a proper choice of the CS transistor size (i.e., M_1 in Figure 3.2) and the inductive source degeneration, L_{S}, to set at the operating frequency both the real part of the optimum noise impedance, $R_{\mathrm{S,\,OPT}}$, and the real part of the input impedance, Z_{IN}, equal to the antenna resistance, R_{S}, (i.e., 50 Ω/ 100 Ω for a single-ended/ differential antenna), respectively, according to the following condition:

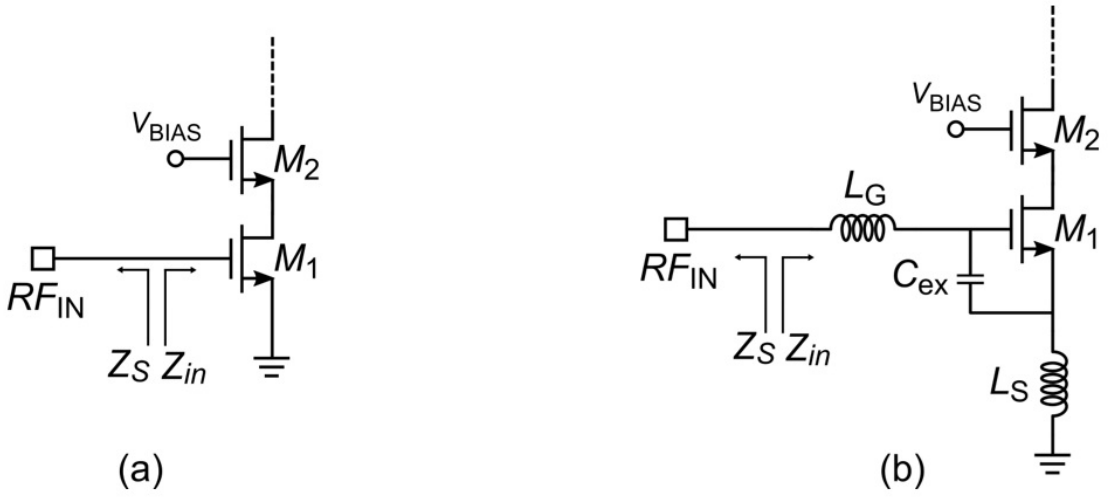


Figure 3.2: (a) Cascode LNA topology and (b) source-degenerated cascode LNA.

$$NF = NF_{\mathrm{MIN}} \qquad \text{if} \qquad R_{S,\mathrm{OPT}} = Re\left[Z_{\mathrm{IN}}\right] = R_S \tag{3.2}$$

The fulfillment of 3.2 guarantees the simultaneous noise and input matching since the imaginary part of Z_{IN} can be nullified by using a series gate inductance, L_{G}, as shown in Figure 3.2b. Thanks to the *SNIM* technique, the LNA is matched to the antenna and its *NF* is equal to the minimum noise figure, NF_{MIN}, at the same time, as stated by 3.2. Moreover, the NF_{MIN} can be further reduced by a proper setting of the M_1 gate-source voltage, V_{GS1}. It is worth noting that the required degeneration inductor value, L_{S}, decreases with the increasing of the operating frequency and is very low at mm wave frequencies, thus not appreciably degrading the NF_{MIN} of the LNA.

Nevertheless, the *SNIM* approach is useless for low-power LNA design since the current consumption is not a free design parameter, but it is a result of the design procedure. For low-power LNAs, *PCNO* and *PCSNIM* techniques have been proposed. The former is aimed at achieving the lowest *NF* at a given (low) power consumption. However, achievable *NF* values are considerably higher than the NF_{MIN} provided by the technology. On the other hand, the *PCSNIM* technique provides a low-power design alternative. It exploits an additional design parameter, i.e., the capacitor, C_{ex}, connected in parallel to the CS gate-source capacitance, C_{gs}. The capacitor C_{ex} is properly set to achieve condition 3.1 at the given current consumption of the LNA. However, this approach suffers at higher operating frequencies. The capacitor C_{ex} degrades the effective cut-off frequency, f_{T}, thereby reducing the gain of the LNA. For these reasons, the *PCSNIM* technique can be hardly used at mm-wave frequencies.

In the design of *RF*/mm-wave LNAs, ESD protection cannot be neglected. On the other hand, ESD protection often produces performance degradation in terms of both input matching and *NF*, especially at mm-wave frequencies. Two methods, namely co-design and "plug-and-play" design, exist for putting ESD protective features into practice. Large clamping components, such as diodes or grounded gate NMOS networks, frequently with a series resistor, which limits the current, can be added as a "plug-and-play" element for ESD protection in digital circuits. Unfortunately, these devices cannot be employed in an *RF* LNA due to their large *RC* parasitics, which highly affect both noise and input matching performance. On the other hand, the co-design method takes into account both the ESD components and the integrated circuit, thus recovering the flexibility required for cutting-edge circuit design. Employing inductors and transformers for co-design ESD protection has been proposed in the literature [43–45]. This allows for adequate ESD protection without compromising design flexibility. However, these solutions are quite space-consuming, which is undesirable in expensive nanoscale CMOS technology. To implement an ESD transformer without

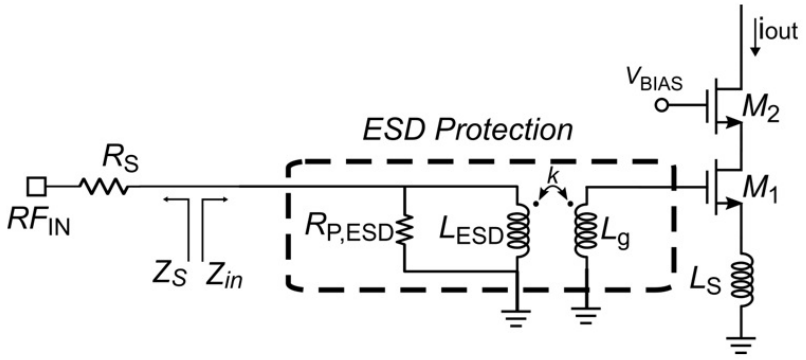


Figure 3.3: Cascode LNA with transformer-based ESD protection.

significant area penalty and prevent gate-oxide breakdown during an ESD incident, the ESD inductor, L_{ESD} and the LNA gate inductor, L_{g}, are built by means of interleaved coils. Additionally, the transformer galvanic isolation greatly attenuates the risk of residual voltage overshoots at the input, thus further enhancing ESD protection threshold. The parasitics of the ESD transformer can be included in the LNA input matching network by using the co-design approach. Figure 3.3 depicts a cascode LNA with transformer-based ESD protection.

The impact of the input ESD transformer on the *NF* can be evaluated by means of an additional noise term, F_{added} [40], as reported in 3.3,

$$F_{\mathrm{added}} = \frac{R_{PS}}{R_S} + \frac{R_{SS}}{n^2 R_S} \tag{3.3}$$

where R_{PS} and R_{SS} are the series resistances of the primary, L_{ESD}, and secondary, L_{g}, coils, respectively; n is the transformer turn ratio, i.e., $n = \sqrt{\frac{L_g}{L_{\mathrm{ESD}}}}$; and R_{S} is the source resistance. It is evident from 3.3 that the square of turn ratio reduces the noise contribution of the transformer-based ESD protection network. Therefore, it is advantageous to have a higher turn ratio to minimize the noise. Additionally, the input matching constraint of the LNA should not deteriorate at the operating frequency. For this reason, the equivalent parallel resistor of the ESD inductor, $R_{\mathrm{P,\,ESD}}$, as reported in 3.4, should be much higher than the source resistance $R_{\mathrm{P,S}}$, which is determined by the antenna:

$$R_{P,\mathrm{ESD}} = \omega Q_{\mathrm{ESD}} L_{\mathrm{ESD}} \tag{3.4}$$

where ω is the angular frequency and Q_{ESD} is quality factor of the ESD inductor, L_{ESD}. Therefore, the maximization of the quality factor of the transformer coil is required to reduce the *NF* degradation due to the ESD protection.

3.2.2 Power-Efficient *SNIM* with Source Impedance Transformation (*PE-SNIM*)

The main drawback of the *SNIM* technique, i.e., its poor suitability to low-power applications, can be overcome by applying the classical *SNIM* along with a proper source impedance transformation, namely power-efficient *SNIM* (*PE-SNIM*). In a traditional *SNIM* approach, condition 3.2 determines the W/L ratio of the CS transistor, M_1, and, hence, the LNA current consumption (i.e., drain current, I_{D1}), given optimum gate source voltage, V_{GS1}, that minimizes the NF_{MIN}. However, the value of I_{D1} required for *SNIM* can be significantly reduced if the source resistance, R_S, seen by the LNA is increased. This could be accomplished by using an additional input matching network. Since LNAs must include ESD protection, the ESD input transformer shown in Figure 3.3 can also be effectively exploited for the impedance transformation. To this aim, the turn ratio between primary and secondary windings is set to provide the required input impedance step-up transformation [46] without any additional component. For instance, with a 1:2 transformer ratio for an ideal transformer, an impedance transformation of 1:4 is obtained, which means a reduction in the required drain current, I_{D1}, by a factor of nearly four. Therefore, the application of the *PE-SNIM* to single ended LNAs with transformer based ESD protection allows a considerable reduction in current consumption by means of high-transformation-ratio mm-wave integrated transformers [47].

The *PE-SNIM* technique becomes mandatory when a differential configuration is adopted. Indeed, using the classical *SNIM* approach, the required value of the LNA input stage current is nearly doubled with respect to a single ended approach, since each amplifier branch must be designed for an $R_{S,OPT}$ equal to $R_S/2$. Since, differential like architectures are highly desirable at mm wave frequencies for their better robustness, the *PE-SNIM* is the answer to limit the LNA current consumption, as well as provide inherent input single-ended-to-differential conversion. The *PE-SNIM* technique has been used for the design of a pseudo-differential LNA for 60 GHz OOK receivers, as detailed in the following subsection.

3.2.3 *PE-SNIM* Design of the 60-GHz LNA

As previously introduced, several mm-wave CMOS LNAs adopt single-ended architectures due to their lower power consumption and smaller silicon area [34–36]. However, these configurations offer limited robustness against common-mode noise from the substrate and power supply and pose challenges for ESD protection. To address these issues, the proposed 60-GHz LNA adopts a compact 1-stage/2-stage pseudo-differential

architecture with transformer-based ESD protection. This topology, designed for direct connection to a differential OOK detector as shown in Figure 3.1, ensures improved noise immunity and higher reliability. In this section, the focus is on the implementation of a *PE-SNIM* strategy within this architecture to meet stringent performance and power constraints.

The LNA has been designed in a 28-nm bulk CMOS technology by TSMC with eight metal layers. The process provides low-voltage threshold (LVT) 0.9-V CMOS transistors that are suited for low-power and high-frequency operation. The available BEOL includes two top copper metal layers of about 1 µm, which can be exploited for the implementation of mm-wave inductive components.

The 1-stage LNA simplified schematic is shown in Figure 3.4. The amplifier is connected to a differential antenna ($R_{\mathrm{S}} = 100\,\Omega$) and an OOK detector (here represented by an equivalent RC load) at its input and output, respectively. The LNA adopts a single pseudo-differential CAS stage with integrated ESD protection provided by transformer T_{IN}. Despite the low supply voltage, V_{DD}, of 0.9 V, the CAS topology was preferred to the more popular common-source (CS) one. Indeed, CS-based amplifiers show slightly better noise performance but are affected by very poor input/output isolation that involves the design of input/output resonant networks and can also produce stability issues. The *PE-SNIM* technique has been adopted to reduce the current consumption, while guaranteeing simultaneous noise and impedance matching by means of inductive degeneration, L_{S}, and proper sizing of the W/L ratio of the $M_{1,2}$ pair. Specifically, transformer, T_{IN}, performs input impedance transformation (from R_{S} to $2R_{\mathrm{S}}$), thus allowing each LNA branch to be matched to R_{S} instead of $R_{\mathrm{S}}/2$ by means of a small inductive degeneration, L_{S} (i.e., 15–25 pH). Thanks to the *PE-SNIM* technique, the designed LNA has a current consumption of a 50 Ω matched single-ended stage (i.e., $I_{\mathrm{D1,2}} = 2.9$ mA).

The LNA is loaded by a resonant LC network made up of a transformer, T_{OUT}, and capacitor, C_{L}, which is also used to directly connect the LNA to the differential input of the OOK detector according to the scheme in Figure 3.1. A resonant transformer is preferred to a load inductor to enable simple biasing through the center-tap and optimum absorption of parasitics thanks to direct input/output connections, while avoiding series coupling capacitors that are critical at mm-wave frequencies. However, the proposed 1-stage LNA cannot guarantee a wide 3-dB bandwidth (BW_{3dB}) and therefore the maximum achievable data rate is limited especially with large PVT variations. On the other hand, enlarging the LNA bandwidth can be achieved by adding another amplification stage, as represented by Figure 3.5 which shows simplified schematics of the 1-stage (black) and 2-stage (black + blue) LNAs. For both topologies the dif-

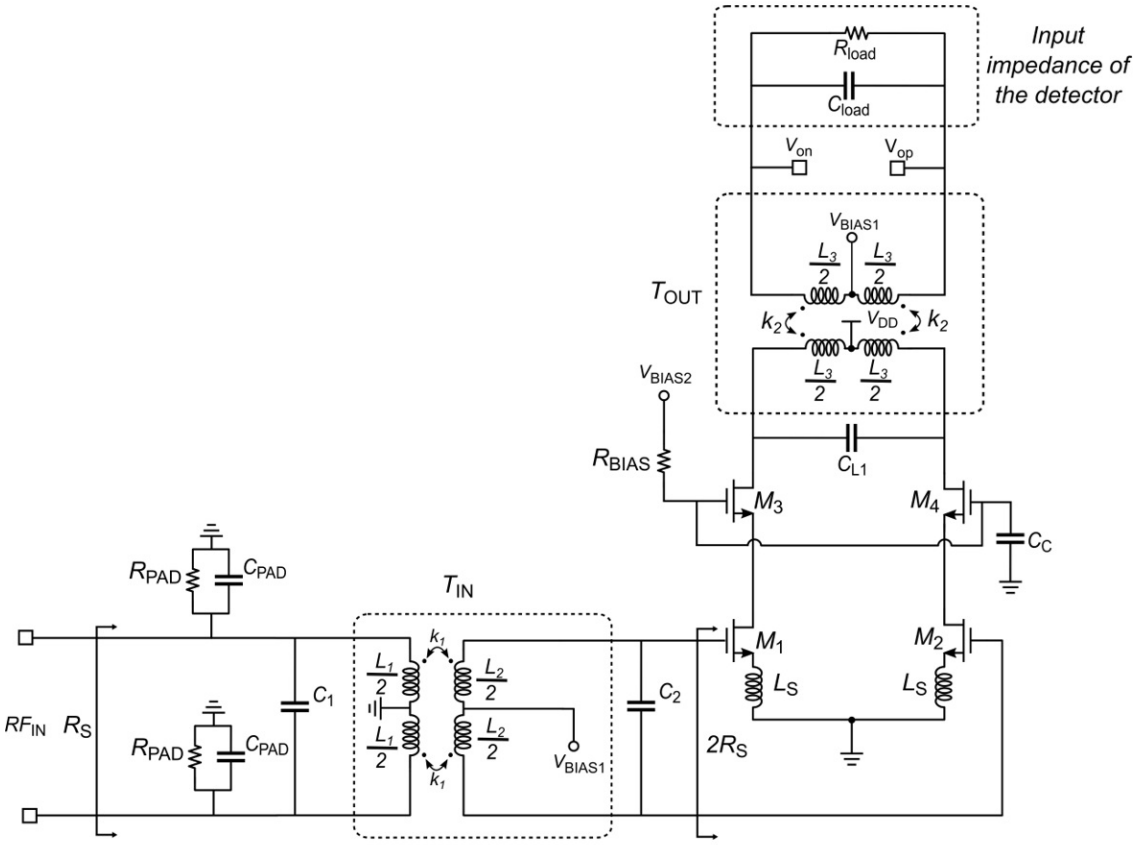


Figure 3.4: Simplified schematic of the proposed 1-stage 60-GHz LNA.

ferential outputs (i.e., V_{OUT1} or V_{OUT2}) are connected to an OOK demodulator that provides a very high impedance. The 2-stage LNA share the same pseudo-differential CAS topology for its first stage, except for the load transformer, T_{INT}, that is properly designed for the inter-matching to the amplifier second stage. To fully exploit the available voltage headroom and achieve better linearity, the second stage employs a CS topology. The 2-stage LNA also adopts a transformer-based resonant load at the output (i.e., T_{OUT2}, and C_{L2}), which is beneficial for the connection of the LNA to the differential OOK demodulator. Parallel capacitors, C_{L1} and $C_{\mathrm{L1}}/C_{\mathrm{L2}}$, in 1-stage and 2-stage LNAs, respectively, play a crucial role for gain and BW_{3dB} performance since they are used to properly set the resonance frequencies of the LC networks as shown in Figure 3.6 that compares 1-stage and 2-stage LNAs in terms of gain and BW_{3dB}. Adding the second stage extends BW_{3dB} up to three times more i.e. from 2 GHz to 6 GHz, with a 10 percent decrease in gain, from 21.4 dB to 19.3 dB.

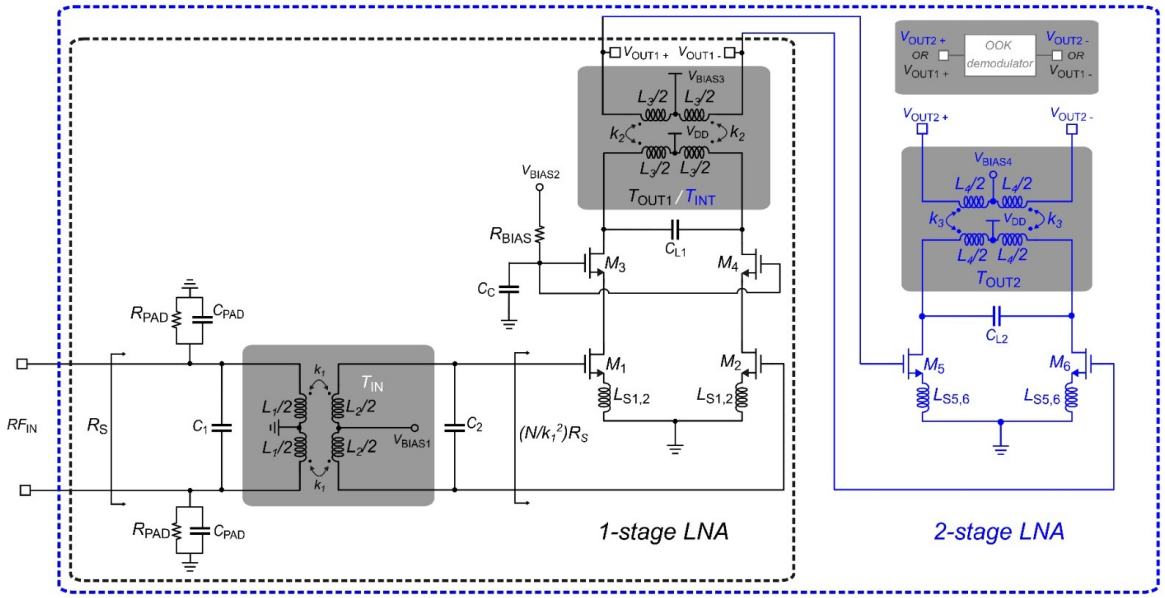


Figure 3.5: Simplified schematic of 1-stage (black) / 2-stage LNA (black+blue).

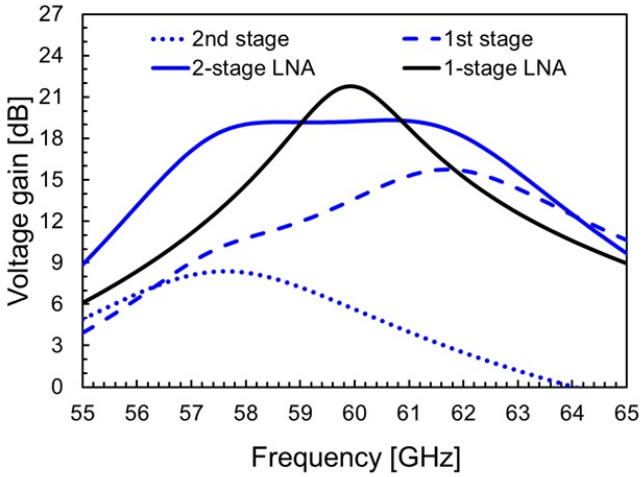


Figure 3.6: Simulated voltage gain of 1-stage/2-stage LNAs versus frequency.

3.3 Transformer Design

Integrated transformers are crucial for the design of the LNA, especially at mm-wave frequencies. An integrated transformer can be implemented by using four different topologies, i.e., tapped, interleaved, stacked, and interstacked [48–52]. The selection of the suited transformer topology is related to both the BEOL (i.e., thickness of the metals, intermetal oxide thickness, distance from the substrate, etc.) and circuit specifications. Moreover, ground shields are often included beneath the coils to reduce the substrate losses, but their effectiveness is poor at mm-wave frequencies [53, 54].

The proposed design of 1-stage/2-stage LNAs incorporates two types of integrated

transformers. The input transformer, T_{IN}, is used for input matching and ESD protection, while the load transformers, $T_{\mathrm{INT}}/T_{\mathrm{OUT1}}$ and T_{OUT2} handle interstage matching, gain, and BW_{3dB}. T_{IN} is identical in both designs, featuring an interleaved layout implemented in the topmost metal layer, $M8$, as shown in Figure 3.7a. This configuration ensures proper impedance transformation from 100 Ω to 200 Ω, which is essential for input/noise matching at lower current consumption using the *PE-SNIM* technique. The electromagnetic (EM) simulated inductance and Q-factor curves for both coils of transformer T_{IN} are depicted in Figure 3.8. The inductances of the primary, L_1, and secondary, L_2, coils are 151 pH and 225 pH, respectively, with a magnetic coupling factor, k, of about 0.4. Both T_{IN} windings achieve a Q-factor of about 23 at 60 GHz. Since the impedance transformation ratio $N{=}L_2/L_1$ is less than 2, the resonance frequency of the primary coil, L_1, is slightly higher than that of the secondary coil, L_2. Consequently, the magnetic coupling, k, of T_{IN} affects N in proportion to $\frac{1}{k^2}$, enabling higher impedance transformation, but at the cost of reduced efficiency of the input resonance network [46]. On the other hand, the load integrated transformers $T_{\mathrm{INT}}/T_{\mathrm{OUT1}}/T_{\mathrm{OUT2}}$ exploit stacked layout, as shown in Figure 3.7b, implemented on the top metal layers $M8/M7$, offering a higher k value compared to the interleaved design. Thanks to the same thickness of $M8/M7$, the coils inductances in both primary/secondary sides are identical. Concerning the 1-stage LNA, T_{OUT1} resonates with the load capacitor C_{L1} at 60 GHz providing the maximum gain, while T_{INT} and T_{OUT2} in 2-stage LNA are resonating with $C_{\mathrm{L1}}/C_{\mathrm{L2}}$ at different frequencies, around 61.8 GHz and 57.6 GHz, respectively, shown in Figure 3.6.

The geometrical parameters of the integrated transformers in both 1-stage/2-stage LNAs are reported in Table 3.2. By increasing the metal width, w, and spacing, s, the coils achieve a higher quality factor, Q-factor, and self-resonance frequency, SRF, exceeding the value of 15 and 120 GHz, respectively. On the other hand, the design rule manual (DRM) of the adopted 28-nm CMOS technology dictates a minimum width of 2.74 µm for both metal 8 and metal 7 to comply with an ESD current of about 1.3 A that is associated with the 2-kV human body model (HBM). Since a 4 µm metal width has been adopted to improve the transformer winding Q-factor, the design is fully compliant with ESD specifications in terms of current capability. For the sake of completeness, an HBM test has been also simulated. It has been carried out by connecting the LNA to the standard HBM consisting of a 100-pF capacitance with a series 1.5-kΩ resistance, which are the average body capacitance and skin resistance, respectively [55]. The LNA achieves the standard level of on-chip ESD protection of 2 kV [45], guaranteeing that the gate voltages of the input pair, $M_{1,2}$, are well below the breakdown voltage of 1 V. It is worth noting that in 2008, the ESD Industry

Council proposed a lower HBM protection level from 2 kV to 1 kV for scaled CMOS technologies [56] and therefore achieving 2-kV HBM protection in a 28-nm CMOS technology is an excellent result.

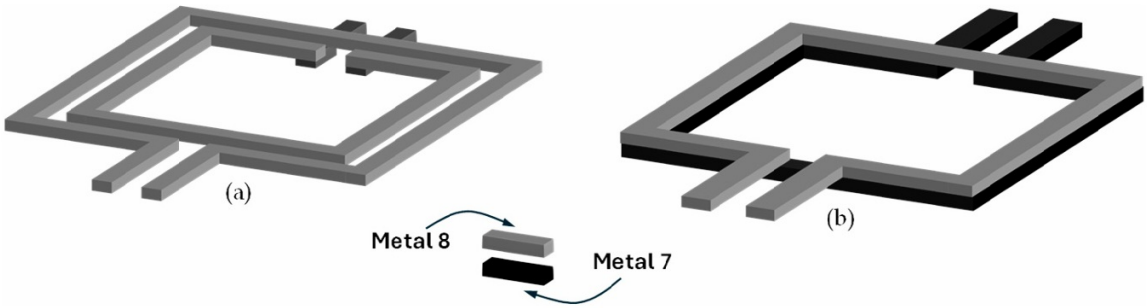


Figure 3.7: (a) Interleaved T_{IN} and (b) stacked $T_{\mathrm{INT}}/T_{\mathrm{OUT1}}/T_{\mathrm{OUT2}}$ transformers.

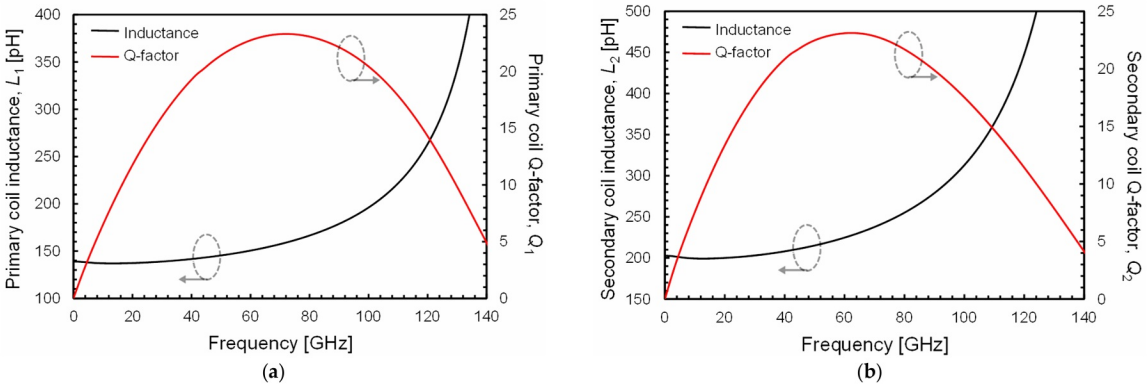


Figure 3.8: Primary (a) / secondary (b) coil inductance and Q-factor of T_{IN}.

Table 3.2: Electrical/Geometrical parameters of transformers for 60-GHz 1-stage/2-stage LNA.

Parameters	**1-stage LNA**		**2-stage LNA**			**Unit**
	T_{IN}	T_{OUT1}	T_{IN}	T_{INT}	T_{OUT2}	
Primary/secondary inductance @ 60 GHz	151/225	122	151/225	110	133	pH
Primary/secondary Q-factor @ 60 GHz	23	19	23	19/18	19/18	–
Magnetic coupling factor (k) @ 60 GHz	0.4	0.7	0.4	0.7	0.7	–
Self-resonance frequency (SRF)	150	140	150	150	135	GHz
Primary/secondary inner diameter (d_{IN})	50/68	40	50/68	38	42	μm
Metal width (w)	4	3	4	3	3	μm
Metal spacing (s)	5	–	5	–	–	μm

3.4 1-stage/2-stage 60-GHz LNA Performance Comparison

The LNAs performance of 1-stage/2-stage LNAs was assessed by using circuit/ electromagnetic simulations, including scattering (S)-parameters of the integrated transformers, as well as the dominant parasitic effects from the RF input pads and main transistors connections. Figure 3.9 shows the input matching of the LNAs through the S_{11} parameter, demonstrating values below -10 dB across the entire $BW_{3\text{dB}}$ centered at 60 GHz. On the other hand, thanks to the *PE-SNIM* technique, effective noise matching is achieved resulting in NF of 6.3 dB and 6.9 dB at 60 GHz, including the losses of T_{IN}, for the 1-stage and 2-stage LNAs, respectively, as shown in Figure 3.10. The voltage gain at 60 GHz is 21.4 dB for the 1-stage LNA and 19.3 dB for the 2-stage one, as demonstrated in Figure 3.10. Despite a 2-dB gain reduction in the 2-stage LNA, its $BW_{3\text{dB}}$ has significantly increased, extending up to three times more around 60 GHz, from 2 GHz to 6 GHz. Additionally, the linearity of the amplifiers is evaluated using the $IP_{1\text{dB}}$ parameter, as shown in Figure 3.11. The 2-stage amplifier exhibits better linearity with an $IP_{1\text{dB}}$ of -14.4 dBm, while the 1-stage LNA has lower $IP_{1\text{dB}}$ of about -19.4 dBm. Figure 3.12 depicts LNA output voltage with an input power of -40 dBm at different bit-rates. Both LNAs exhibit a peak-to-peak output voltage exceeding 80 mV_{PP}, ensuring adequate drive capability for the OOK demodulator. In the worst-case scenario, where the output voltage is reduced to approximately 40 mV_{PP} due to process variations, it remains sufficiently high to reliably drive the demodulator, confirming the system's robustness in various operating conditions.

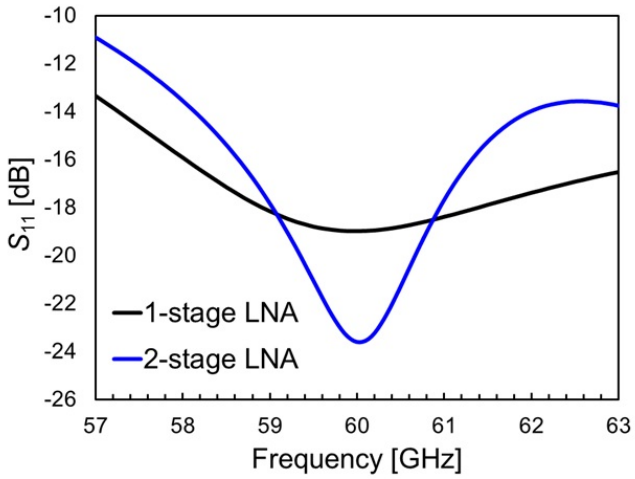


Figure 3.9: Simulated input matching of 1-stage/2-stage LNAs.

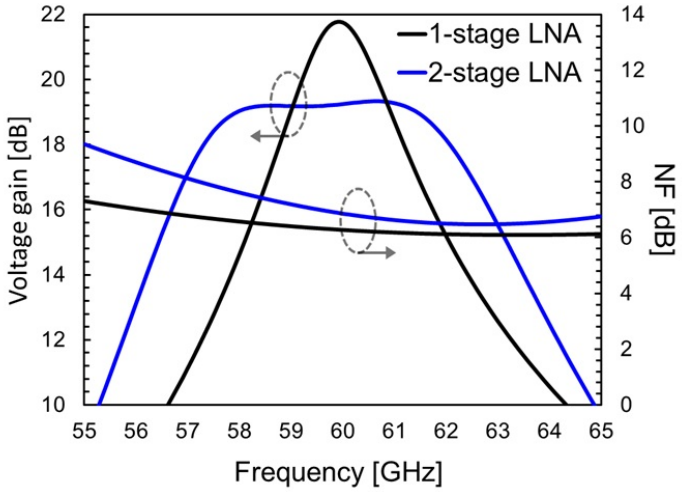


Figure 3.10: Simulated voltage gain and *NF* of 1-stage/2-stage LNAs.

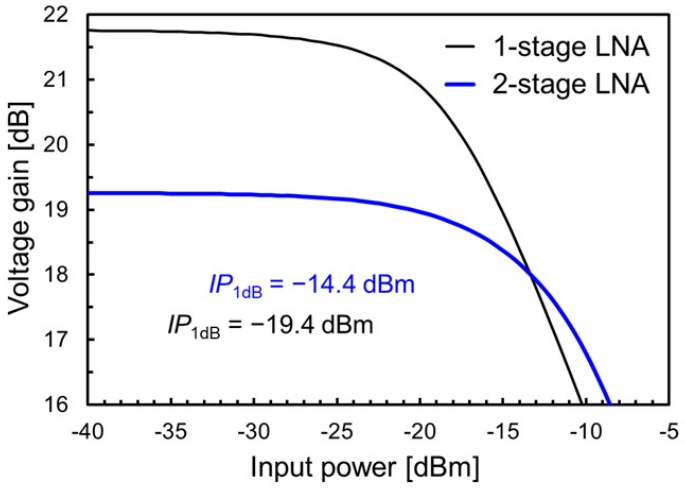


Figure 3.11: Simulated $IP_{1\text{dB}}$ of 1-stage/2-stage LNAs.

Table 3.3 compares the 1-stage and 2-stage LNAs performance with significant published works. The proposed LNAs achieve an outstanding balance between gain, noise, linearity, and power efficiency, despite the differential architecture and the inclusion of an integrated ESD protection balun. This is accomplished using only one/two stages and input/load integrated transformers, optimizing both performance and power consumption.

As a conclusion, two 60-GHz LNAs with one-stage and two-stage configurations were designed and compared as preliminary candidates, focusing on key performance parameters. Both LNAs employ an ESD-protected pseudo-differential topology and incorporate the *PE-SNIM* technique to achieve low power consumption while ensuring optimal simultaneous noise and input matching, making them well suited for high-speed mm-wave applications. Both architectures are capable of driving an OOK demodulator

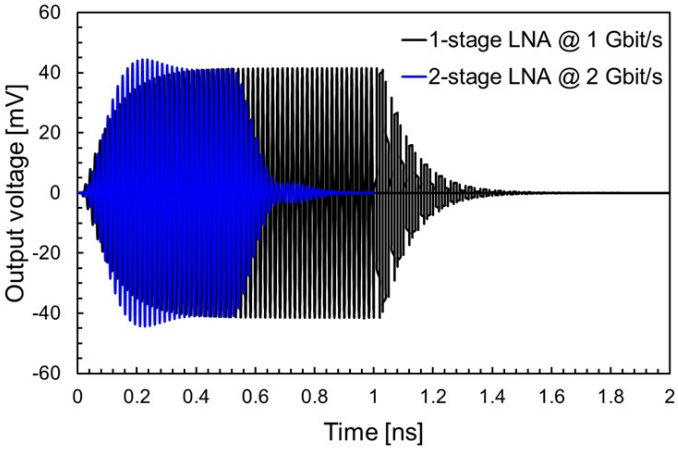


Figure 3.12: Simulated output voltage: 1-stage LNA at 1 Gbit/s, and 2-stage LNA at 2 Gbit/s.

Table 3.3: Performance comparison of 1-stage and 2-stage LNAs.

Parameters	**[57]**	**[[58]**	**[[30]**	**This work (Simulated)**		**Unit**
				1-stage LNA	2-stage LNA	
Number of stages	2	1	2	1	2	–
Single-ended (S) / Differential (D) topology	D	S	S	D	D	–
Voltage gain	16.1	14.1	10.2	21.4	19.3	dB
Frequency bandwidth, BW_{3dB}	15 (52–67)	6 (57–63)	10 (55–65)	2 (59–61)	6 (56.8–62.8)	GHz
Noise figure, NF	7.1	4.6	8.6	6.3	6.9	dB
1-dB input compression point, IP_{1dB}	-10	-13.5	-11	-19.4	-14.4	dBm
Operating frequency	60	60	60	60	60	GHz
Supply voltage, V_{DD}	1.2	2.5	1	0.9	0.9	V
Current consumption	58.3	9.6	30	5.8	9.18	mA
Power consumption, P_{DC}	70	24	30	5.2	8.3	mW
Energy efficiency	–	–	–	5	2.64	pJ/bit
CMOS process node	90	130	65	28	28	nm
HBM level	–	–	3	2	2	kV
FoM [59] $= \frac{Gain[dB] \times BW_{3dB}}{(NF[dB]-1) \times P_{DC}[mW]}$	0.57	0.98	0.45	1.55	2.36	–

with an output swing of 80-mV_{PP} at an input power of -40 dBm. Furthermore, the LNAs support data rates of up to 1 Gbit/s and 3 Gbit/s, with corresponding energy efficiencies of approximately 5 pJ/bit and 3 pJ/bit for the one-stage and two-stage configurations, respectively. Despite the promising performance of both structures, a clear trade-off emerges between power consumption and bandwidth. While the one-stage LNA offers slightly higher gain and lower power consumption, its limited bandwidth constrains the achievable data rate and reduces robustness against PVT variations. In contrast, the two-stage LNA provides a significantly wider bandwidth and improved high-speed performance, making it more suitable for multi-Gbit/s operation and for reliably driving the subsequent demodulator stage. Therefore, this chapter investigates one-stage and two-stage LNAs, selecting the two-stage architecture for final implementation. Its design and post-layout results are presented in Chapter 4.

4 60-GHz OOK Receiver: Implementation and Performance

The simplified block diagram of the proposed 60-GHz OOK receiver is shown in Figure 4.1 and represents the configuration adopted for the final RX chip, which features 50-Ω single-ended input and output terminations for direct on-wafer characterization. With regard to the antenna interface, a single-ended 50-Ω input was selected to comply with standard on-wafer measurements at 60 GHz using ground–signal–ground (GSG) probes. The use of differential ground–signal–signal–ground (GSSG) probes was strongly discouraged due to the poor reliability of the measurements at 60 GHz.

The first block of the receiver architecture provides ESD protection, impedance matching, and single-ended-to-differential conversion. The receiver adopts a fully differential architecture composed of a two-stage LNA followed by an OOK demodulator based on the topologies analyzed in the feasibility study. The demodulator exploits a seven-stage LA to achieve a sufficiently large demodulated signal amplitude. The final block performs differential-to-single-ended conversion and 50-Ω buffering of the recovered bit-stream signal. The receiver is designed to support a nominal data rate of approximately 3 Gbit/s with a target sensitivity of −40 dBm.

The proposed receiver has been implemented in the TSMC 28-nm bulk CMOS technology, using the customized BEOL stack introduced in Chapter 3. This BEOL comprises nine metal layers, including a 3.5-µm-thick top metal layer (M9) and an additional alucap layer (AP) with a thickness of 2.8 µm, to facilitate integration by University of Catania (UNICT) within the IC fabrication consortium. The process provides LVT CMOS transistors operating at a supply voltage of 0.9 V, which are suitable for low-power and high-frequency applications. Moreover, the design kit includes accurate transistor models extracted from measurements up to 110 GHz, with metal interconnections modeled up to the third metal layer. However, no dedicated

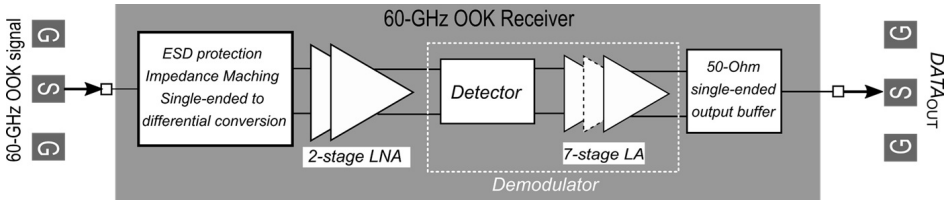


Figure 4.1: Simplified block diagram of the proposed 60-GHz OOK receiver for Gbit/s communications for the final RX chip.

inductive components are available in the process, and standard metal–oxide–metal (MOM) interdigitated capacitors exhibit poor quality factors at mm-wave frequencies. The absence of passive components suitable for the realization of low-loss LC resonant networks represents a major design challenge and motivates the customized design of both integrated transformers and capacitors. In the following subsections, the transistor-level schematics of the receiver blocks are presented and discussed together with the adopted design parameters for both active and passive components.

4.1 Circuit Implementation and Performance of the Standalone 2-Stage 60-GHz LNA

The choice of the LNA topology and its design strategy were addressed in Chapter 3. Based on those results, a two-stage pseudo-differential LNA with single-ended 50-Ω input and differential output driving the OOK demodulator has been implemented for the final receiver chip. This architecture represents the best trade-off between gain, bandwidth, power consumption, and robustness, while preserving compatibility with on-wafer measurements and integrated ESD protection.

The simplified schematic of the implemented LNA is shown in Figure 4.2. The proposed LNA includes two amplification stages and an output buffer stage. The simple two-stage topology is suited for a flat gain with a wide frequency bandwidth in the order of several gigahertz. On the other hand, adding a buffer stage provides 50-Ohm output matching for single-ended on-wafer measurements and integrated ESD protection. The differential input of the amplifier is connected to a 50-ohm single-ended antenna by means of the integrated input transformer, T_{IN}, which also provides impedance matching and ESD protection. The LNA adopts a pseudo-differential structure and consists of two amplification stages and an output buffer. Integrated transformers $T_{\mathrm{INT}}/T_{\mathrm{OUT}}$ are extensively exploited as resonant loads, while enabling simple inter-stage connections and biasing. Despite the low supply voltage, V_{DD}, of 0.9 V, for the input stage of the LNA, the CAS topology has been preferred to a more widely used CS one. Indeed, the CS-based configuration exhibits better noise performance, but suffers from extremely poor input/output isolation, which involves the design of input/output matching networks, and can also lead to instability. On the other hand, both second and buffer stages adopt the CS topology to exploit all the available voltage headroom and maximize LNA linearity. It is worth noting that inductive degeneration (i.e., L_{GND1}, L_{GND2} and L_{GND3}) models the parasitic path toward ground.

As proposed in Subection 3.2.2 , *PE-SNIM* technique is used for the first stage, given that conventional design methods for noise/impedance matching do not consider

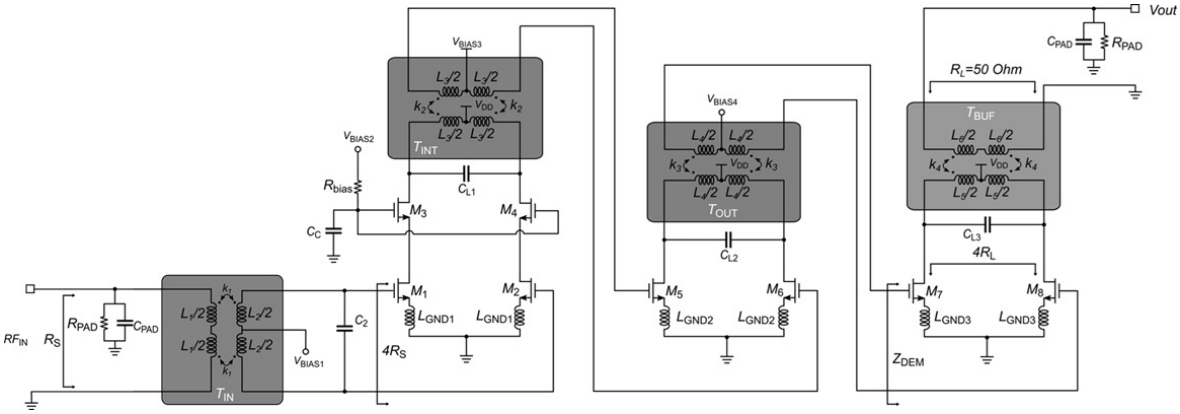


Figure 4.2: Simplified schematic of the proposed standalone 2-stage 60-GHz LNA.

the constraints of the current budget in mm-wave CMOS LNAs. *PE-SNIM* guarantees simultaneous noise and impedance matching at a low current level by means of inductive degeneration, L_{GND1}, and proper sizing of the W/L ratio of the $M_{1,2}$ pair. Specifically, an integrated transformer performs input impedance transformation, thus allowing each LNA branch to be matched to $2R_{\mathrm{S}}$ instead of $R_{\mathrm{S}}/2$ by means of inductive degeneration, L_{GND} (i.e., the parasitic path toward the ground plane). With a transistor bias current of only 2.6 mA, the first stage of the LNA achieves simultaneous noise/input matching thanks to the 1:4 input impedance step-up (i.e., from 50 Ω to 200 Ω) provided by the integrated transformer, T_{IN}. It is worth noting that the adoption of a traditional 1:1 input impedance ratio would require a differential stage with a current consumption about four times higher. As a result, the overall current required by the first differential stage (i.e., 5.2 mA) is almost the same as a single-ended amplifier, while guaranteeing superior robustness against common-mode noise/disturbances and ESD protection.

The second stage is essential to extend the BW_{3dB} of the amplifier in order to comply with multi Gbit/s applications. The first stage is connected to the second one by means of the integrated interstage transformer, T_{INT}, which not only provides the interstage matching, but also biases the following stage through its center-tap without requiring coupling capacitors. Indeed, series coupling capacitors are not effective due to their excessive losses at mm-wave frequencies. Flat gain and a large BW_{3dB} are achieved by properly tuning the load capacitors, C_{L1} and C_{L2}, which are in parallel with the two integrated transformers, T_{INT} and T_{OUT}, respectively. As the last stage, the buffer also exploits a CS pseudo-differential topology with a transformer load, T_{BUF}. The transformer has been designed to provide wideband 50-ohm output matching and differential-to-single-ended conversion resonating with capacitor C_{L3}. Moreover, the buffer provides high input impedance as the second-stage output load (i.e., Z_{DEM}) to preserve the voltage gain of the two-stage amplifier, as happens when the LNA is con-

nected to a demodulator. It is worth noting that an output passive matching network cannot provide buffering functionality. By choosing proper resonance frequencies of the three integrated transformers T_{INT}, T_{OUT} and T_{BUF}, a BW_{3dB} of nearly 7 GHz can be guaranteed.

4.1.1 Passive Components Design

Integrated transformers are crucial for the design of the proposed LNA. Generally, stacked windings provide the highest magnetic coupling factor, k, and optimal area efficiency. Interleaved or tapped structures suffer from larger footprints and lower k, while interstacked transformers can be effectively implemented if two equal metal layers are available. The choice of the most suitable transformer topology among tapped, interleaved, stacked and interstacked ones depends on the BEOL (i.e., thickness of the metals, intermetal oxide thickness, distance from the substrate, etc.) and circuit specifications. Although ground shields are often included beneath the coils to reduce the substrate losses, their effectiveness is quite poor at mm-wave frequencies and they reduce the *SRF*. For these reasons, no ground shields were adopted [53]. The very first design step was the definition of the transformer topology and winding geometries by means of paper-and-pencil calculations in order to meet circuit specs. Then, transformer optimization was carried out by means of EM simulations to maximize k, and the Q-factor at 60 GHz, while trading off the *SRF*.

As already explained, the input transformer, T_{IN}, is responsible for simultaneous noise/input matching based on the impedance transformation *PE-SNIM* technique, along with ESD protection. Specifically, a turn ratio, n, of about 2 is required to perform impedance transformation from R_{S} to $4R_{\mathrm{S}}$ (i.e., 50 Ω to 200 Ω). This means that the secondary coil inductance, L_2, should be about four times higher than the primary one L_1. Figure 4.3 depicts the transformer structure used to implement T_{IN}. It exploits an octagonal shape and the topmost and thickest metal layers, AP and M9 for L_1 and L_2, respectively, in order to reduce the resistive losses and minimize the capacitive parasitics of the coils toward the substrate, therefore maximizing both the Q-factor and *SRF*. The stacked configuration is adopted to take advantage of the high k, by choosing different metal widths, w, for primary and secondary spirals, as depicted in Figure 4.3a,b. Indeed, this configuration allows us to use one-turn and two-turn coils for primary and secondary windings, respectively, and thus to implement the turn ratio required for input impedance transformation, while preserving the stacked configuration, as shown in Figure 4.3c. Specifically, the primary coil adopts an alucap width of 8 μm that helps to improve the Q-factor without affecting the *SRF*. A lower width of 3 μm is instead used for the secondary coil that is built in metal 9. As far as

ESD protection is concerned, the adopted 28-nm CMOS technology defines a minimum AP width of 1.44 μm tolerating an ESD current of 1.3 A for the 2-kV HBM, which fully complies with the width of the primary coil of T_{IN}. Moreover, the LNA input is connected to a standard model for the HBM test consisting of a series resistor and a capacitor with the values of 1.5 kΩ (average skin resistance) and 100 pF (average body capacitance), respectively [21, 25]. A 2-kV ESD protection is achieved, guaranteeing that the gate voltages of the input pair, $M_{1,2}$, are well below the breakdown voltage of 1 V.

Based on 2D EM simulations with ADS Momentum$^{\mathrm{TM}}$, the primary, L_1, and secondary, L_2, inductance values of transformer T_{IN} are 47 pH and 143 pH at 60 GHz, respectively, while the k, is 0.59. It is well known that minimizing the input matching network loss requires equal resonance frequencies for both primary and secondary windings. In this case, regardless of the value of k, the impedance is transferred by the square of the turn ratio, $n^2 = L_2/L_1$, which is about 3 for the adopted T_{IN}. Therefore, to achieve the required impedance transformation, the primary-winding resonance frequency is set a little bit higher than the secondary one. Indeed, in this case, at the expense of slightly higher loss in the network, the impedance is theoretically transferred by the factor of $\left(\frac{n}{k}\right)^2$ [46]. The latter should be higher than 4 to compensate for non-idealities of the transformer and guarantee 1:4 impedance transformation. The

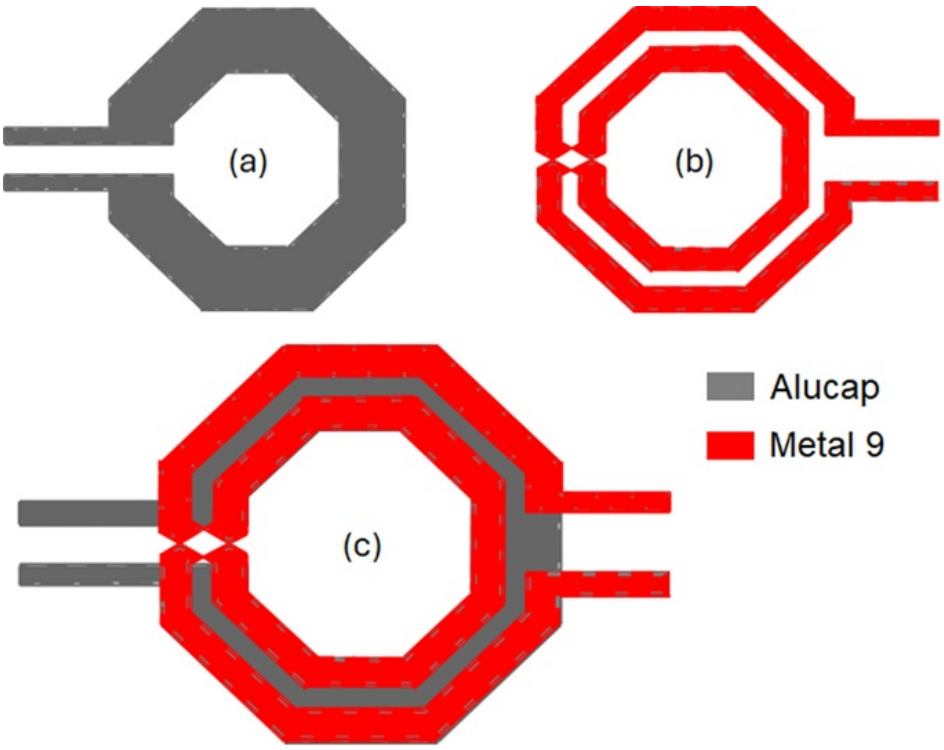


Figure 4.3: Transformer, T_{IN}: primary coil, L_1 (a); secondary coil, L_2 (b); stacked transformer (c).

first tuning of the input matching network is performed, while fine-tuning is carried out by using final post-layout EM simulations.

Both interstage and output transformers, T_{INT} and T_{OUT}, adopt a one-turn octagonal stacked topology by using M9 and AP layers for the primary and secondary spirals, respectively. The stacked configuration guarantees the highest values of the transformer characteristic resistance (TCR) thanks to a magnetic coupling factor as high as k values of 0.7, thus enabling better gain values for both stages. It is worth mentioning that due to the different thicknesses of AP and M9, there is a small difference in terms of the inductance and Q-factor between the primary and the secondary coils. For this reason, the primary coils, L_3 and L_4, of T_{INT} and T_{OUT}, respectively, are implemented on M9.

Finally, the 50-ohm output matching and differential-to-single-ended conversion are achieved by means of the integrated transformer, T_{BUF}. The latter adopts the same geometry of the input transformer T_{IN}. A summary of geometrical and EM-extracted parameters of the three integrated transformers is reported in Table 4.1.

The performance of the LNA is highly affected by the losses of the LC resonant networks formed by the above-described integrated transformers and capacitors (i.e., C_2, C_{L1}, C_{L2} and C_{L3}). In the adopted 28-nm CMOS technology, available standard MOM capacitors have very poor Q-factors at 60 GHz (i.e., about 15) along with very high process variations that impact both gain and frequency bandwidth performance. For this reason, customized differential metal–insulator–metal (MIM) capacitors have been designed to be used instead of MOM capacitors. These MIM capacitors are implemented by means of two top metal layers of AP and M9, as shown in Figure 4.4. Though not standard, MIM capacitors have been designed to be fully compatible with

Table 4.1: Geometrical/electrical parameters of the integrated transformers.

Parameters	$T_{\mathbf{IN}}$ ($T_{\mathbf{BUF}}$)	$T_{\mathbf{INT}}$	$T_{\mathbf{OUT}}$	**Unit**
Transformer topology	Stacked	Stacked	Stacked	–
Primary/secondary inner diameter (d_{IN})	22	58	63	μm
Primary/secondary metal width (w)	8/3	3/3	2/2	μm
Spacing (s)	–/2	–	–	μm
Number of turns (n)	1:2	1:1	1:1	–
Primary coil inductance @ 60 GHz	47	151	173	pH
Secondary coil inductance @ 60 GHz	143	155	178	pH
Primary coil Q-factor @ 60 GHz	15	23.6	23.5	–
Secondary coil Q-factor @ 60 GHz	16	19.6	19.7	–
Magnetic coupling factor (k) @ 60 GHz	0.58	0.72	0.74	–
Self-resonance frequency (SRF)	144	121	112	GHz

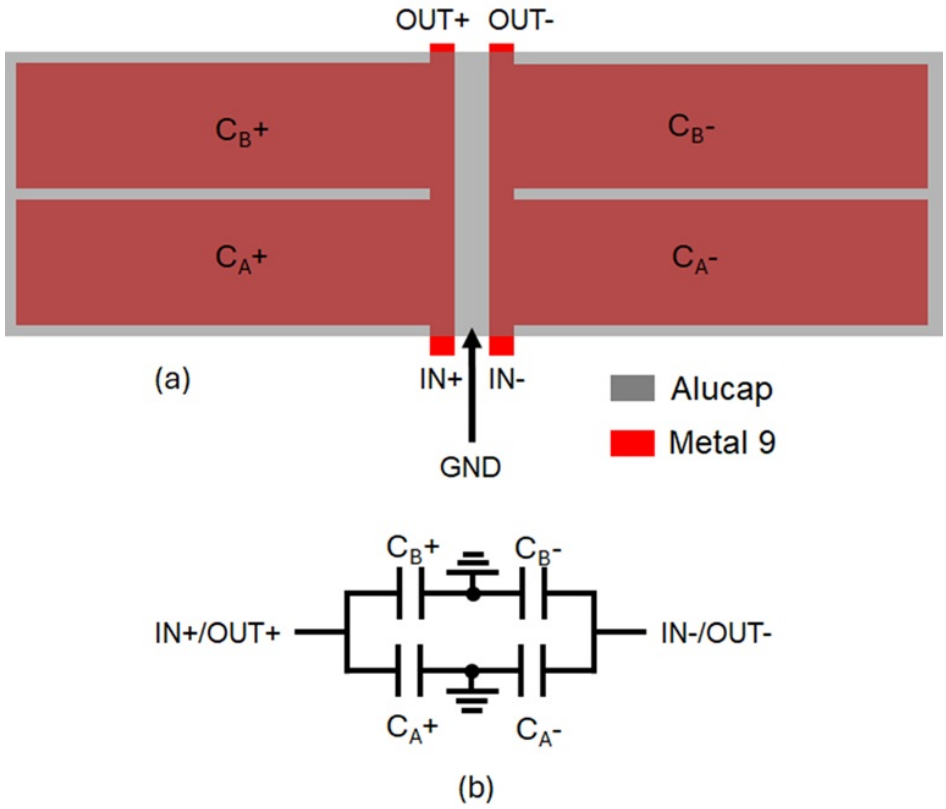


Figure 4.4: Differential MIM capacitor: layout (a) and equivalent circuit (b).

the TSMC 28-nm process, minimizing reliability risks. The EM-simulated Q-factor is as high as 100 at 60 GHz, which guarantees reduced losses of the resonant LC networks of the LNA.

4.1.2 Layout Description and Expected Performance

Layout and EM Post-Layout Analysis

Figure 4.5 depicts the layout of the 60-GHz LNA core, whose size is 445 μm $\times$ 140 μm (excluding PADs for measurement setup), main labels for the LC resonant networks (i.e., transformers and MIM capacitors) and the ground (GND) plane, also included for the sake of clarity. The chip has been drawn for on-wafer measurements through GSG *RF* probes at both input and output (east/west positions) by using a two-port network analyzer. Multicontact DC probes (north/south positions, not displayed in Figure 4.5) are instead adopted for DC biasing. As already detailed in the previous sections, on-chip ESD protection is provided at both *RF* input and output by means of transformers, T_{IN} and T_{BUF}. A metal GND plane was implemented by using the top alucap layer, while complying with the metal density rules of the adopted technology.

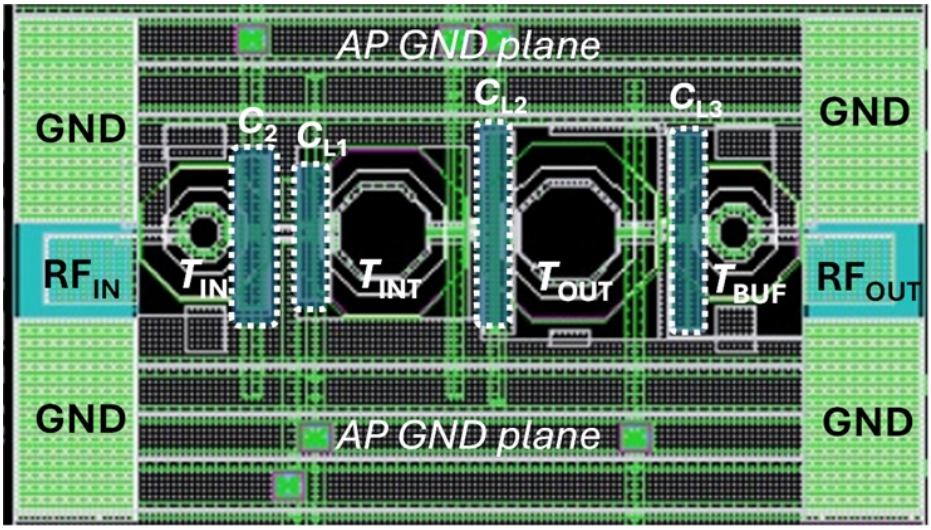


Figure 4.5: Layout of the proposed LNA.

At mm-wave frequencies, the layout parasitics highly affect circuit performance, and therefore, careful estimation is of utmost importance. In this design, the overall LNA layout, including integrated transformers (T_{IN}, T_{INT}, T_{OUT} and T_{BUF}), customized MIM capacitors (C_2, C_{L1}, C_{L2}, and C_{L3}), transistor connections, DC paths and the metal ground plane, has been EM-simulated with ADS Momentum$^{\mathrm{TM}}$ by using the substrate layer description provided by TSMC.

It is worth noting that despite the high computational complexity of such EM simulation, this is mandatory to properly estimate all the couplings taking place in the LNA, thereby helping to identify and eliminate potential sources of instability. However, a full EM simulation of the complete LNA layout was performed only at the final stage of the design process. Prior to this, iterative EM simulations of individual LNA sections—particularly the LC resonant networks were—conducted to guide the design according to the simplified procedure illustrated in Figure 4.6.

Expected Performance

Figures 4.7–4.9 illustrate the post-layout LNA performance at nominal supply voltage and room temperature. The overall LNA current consumption at a 0.9-V supply voltage is as low as 11.6 mA, including 3.2 mA for the output buffer. The input (S_{11}) and output (S_{22}) scattering parameters (S-parameters) are shown in Figure 4.7. They confirm the soundness of the adopted input/output transformer-based networks, which guarantee wideband matching centered at 60 GHz. Figure 4.8 depicts the voltage gain of the two-stage LNA, which is as high as 20 dB with a BW_{3dB} of more than 7 GHz, and compares it with the LNA power gain, S_{21} (i.e., 50 Ω input/output matching), including the output buffer. The amplifier achieves a power gain of 13.5 dB, while preserving a

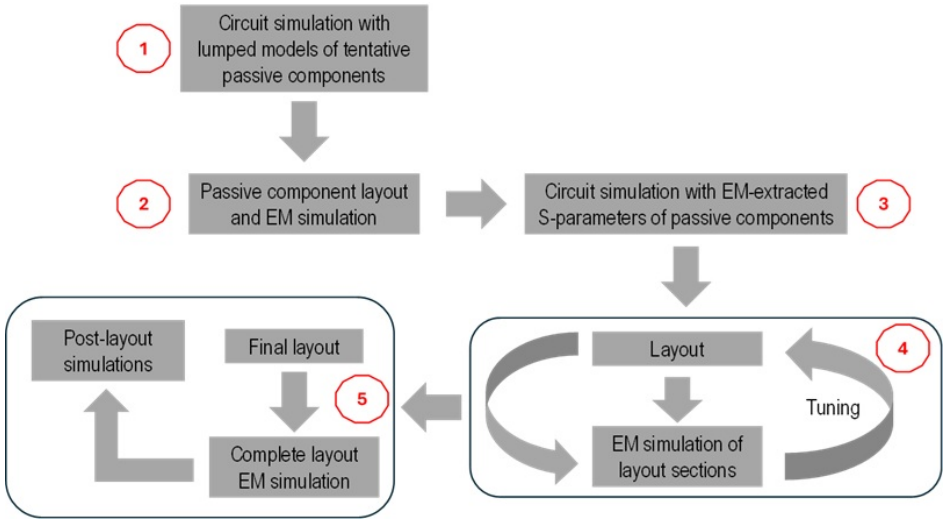


Figure 4.6: Simplified design procedure adopted for the 60-GHz LNA.

7-GHz $BW_{3\text{dB}}$ centered at 60 GHz.

The noise figure of the LNA is shown in Figure 4.9 and is primarily determined by the first two amplification stages. It reaches approximately 8.4 dB at 60 GHz and remains below 10.5 dB across the entire *ISM* frequency band. Notably, this performance is achieved with very low power consumption—approximately 10.4 mW—enabled by the *PE-SNIM* technique. It is worth mentioning that in an actual 60-GHz OOK receiver, such *NF* performance enables a sensitivity of about −40 dBm, which is better than typical sensitivity values reported in the state of the art. The linearity of the LNA is assessed using the $IP_{1\text{dB}}$, as illustrated in Figure 4.10. The LNA demonstrates

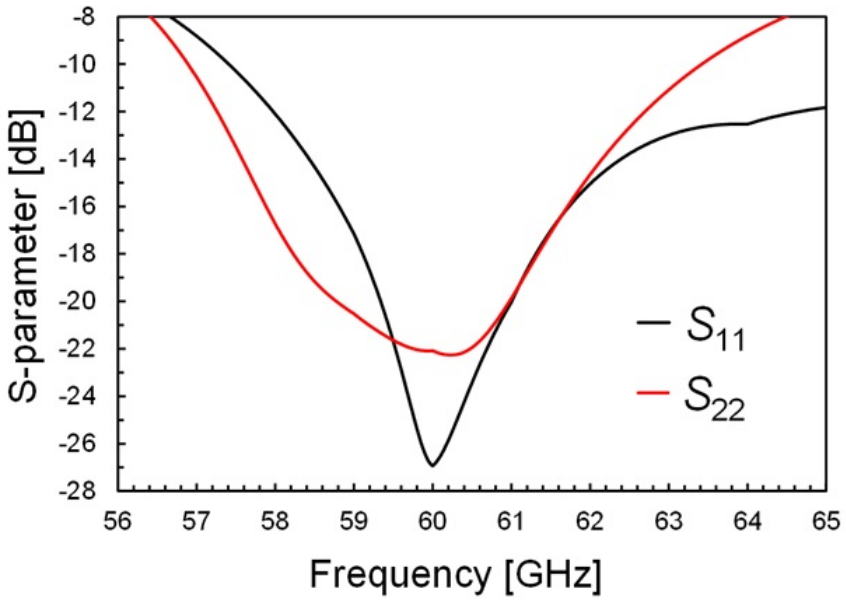


Figure 4.7: Post-layout input (S_{11}) and output (S_{22}) matching versus frequency.

an IP_{1dB} of around -15 dBm, which exceeds the maximum input levels encountered in typical application scenarios (i.e., about -25 dBm). The stability of the LNA, including layout parasitics, has been verified by using Rollett's stability factor. Simulations in nominal and worst-case conditions indicate that the amplifier is unconditionally stable.

For the sake of completeness, the sensitivity of the proposed LNA is verified by means of Monte Carlo (MC) simulations. Figure 4.11 summarizes the MC results for

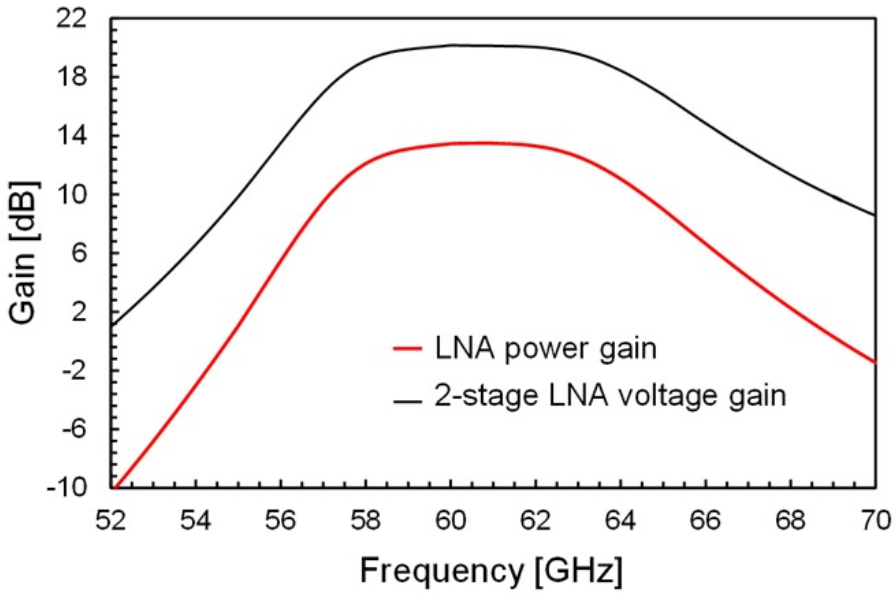


Figure 4.8: Post-layout two-stage LNA voltage gain and power gain, S_{21}, of the two-stage LNA with the buffer.

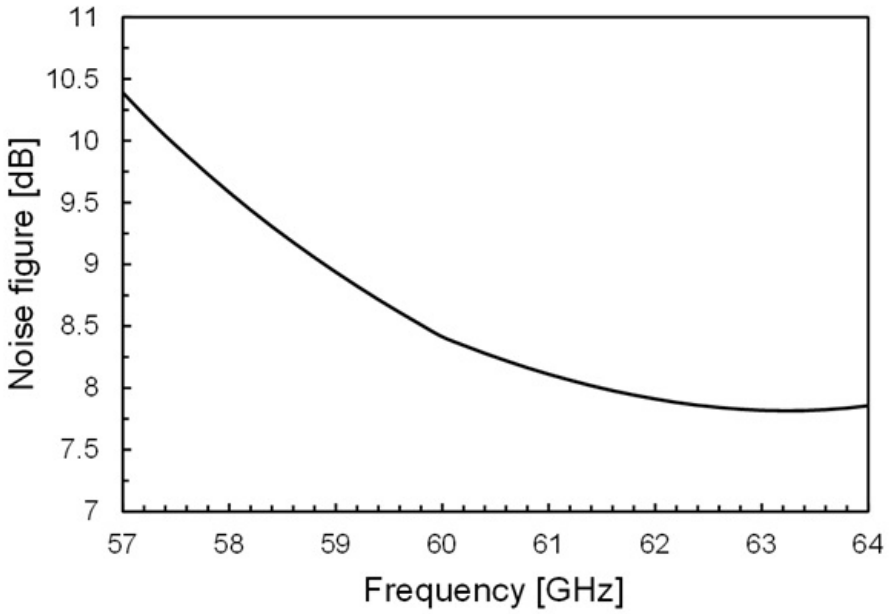


Figure 4.9: Post-layout noise figure, *NF*, versus frequency.

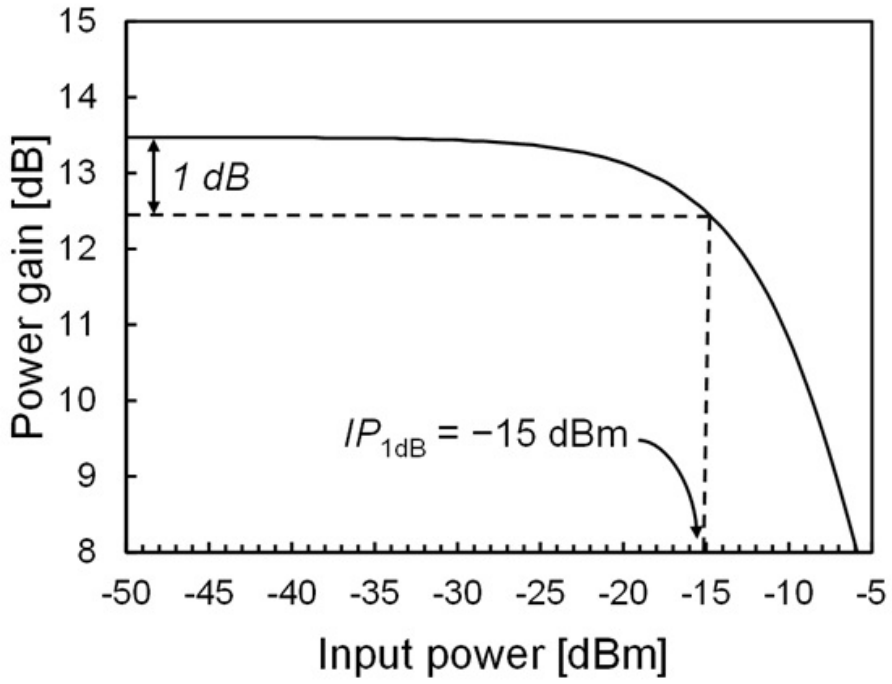


Figure 4.10: Post-layout LNA power gain versus input power.

the main LNA performance parameters, i.e., power gain, *NF*, S_{11}, S_{22}, BW_{3dB}, and IP_{1dB} at 60 GHz.

Table 4.2 presents a comparison between the proposed stand-alone 60-GHz LNA and recently reported state-of-the-art designs. It can be observed that the proposed architecture achieves a well-balanced trade-off among gain, *NF*, linearity, and power consumption. In particular, a power gain of 13.5 dB is obtained, which is comparable with several prior works [57, 58, 60], while maintaining a moderate bandwidth of 7 GHz centered around 60 GHz. The achieved *NF* of 8.4 dB is higher than that of some optimized low-noise designs [60, 61], mainly due to the inclusion of transformer-based ESD protection and the emphasis on robustness and full integration; however, it remains within an acceptable range for mm-wave receiver front-ends.

A key strength of the proposed LNA lies in the adoption of *PE-SNIM* technique, which enables low-power operation while preserving a fully differential architecture. This is particularly important at mm-wave frequencies, where differential topologies provide improved immunity to common-mode noise, substrate coupling, and supply disturbances. As a result, the proposed design achieves competitive linearity, with an IP_{1dB} of −15 dBm, without requiring increased power consumption. The circuit operates with a reduced supply voltage of 0.9 V and a current consumption of 11.6 mA, leading to a total power consumption of only 10.4 mW, which is among the lowest compared to the state of the art. Furthermore, the use of a 28-nm CMOS technology

enables a high level of integration and compactness compared to older technology nodes.

Overall, the proposed LNA demonstrates that the *PE-SNIM*-based design approach allows achieving an efficient trade-off between noise, gain, linearity, and power consumption, making it particularly suitable for low-power and highly integrated 60-GHz OOK receiver applications.

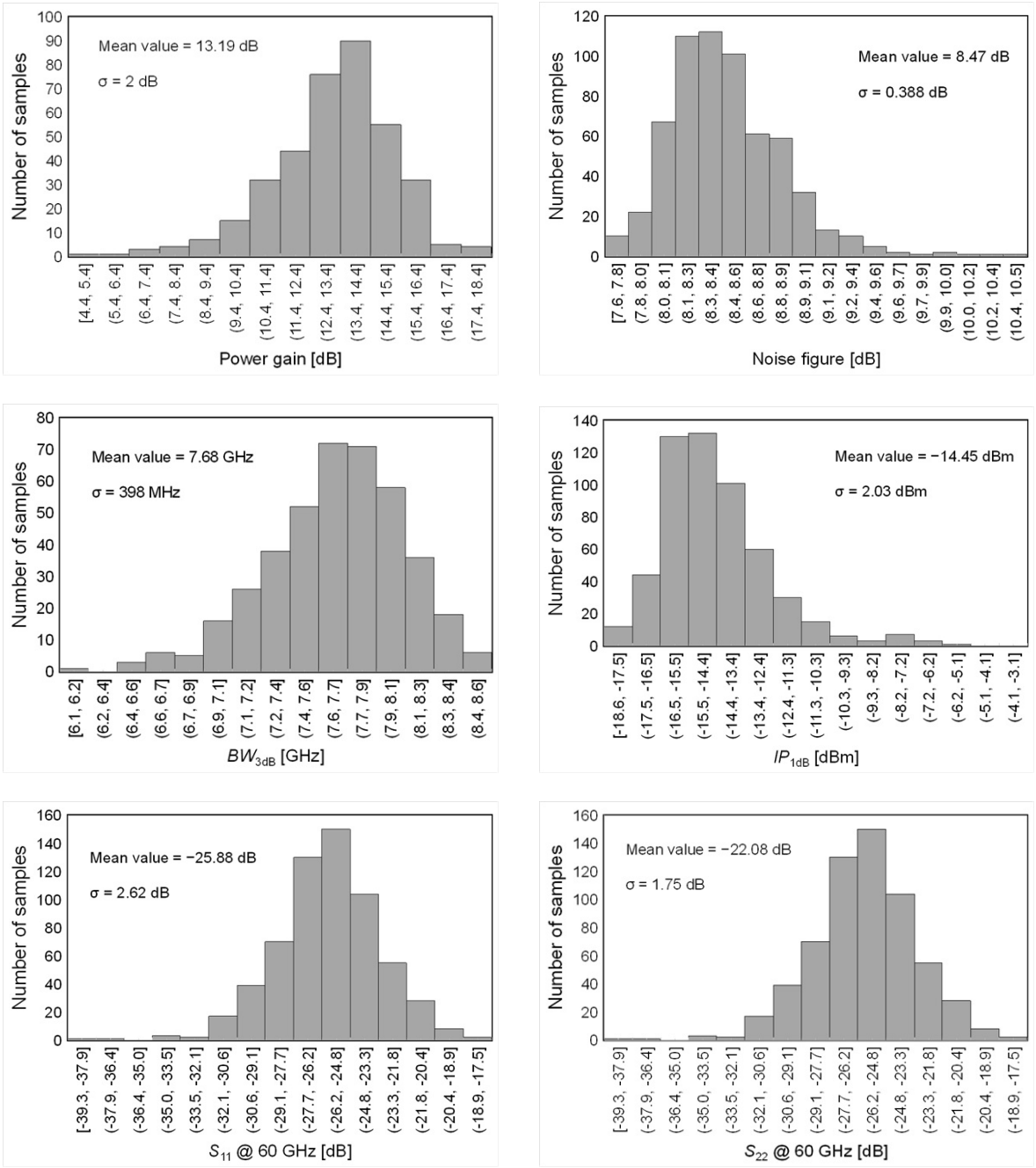


Figure 4.11: MC-simulated results for main LNA performance parameters.

Table 4.2: LNA Performance and Comparison with the State of the Art

Parameters	**[60] Han** TCAS II, 2024 (M)	**[62] Bierbuesse** RFIC, 2020 (M)	**[57] Cheng** MWC, 2021 (M)	**[61] Ke** ICTP, 2022 (P)	**[58] Nawaz** MTT, 2020 (M)	**[30] Lin** MTT, 2012 (M)	**This Work** (P)
No. stages/topology	1CAS-2CS	3CS	2CS	2CS	1CAS	2CAS	**1CAS-2CS**
Differential (d)/single-ended (s)	s	d	d	d	s	s	**d**
ESD protection/HBM level [kV]	NO	NO	NO	NO	NO	3	**2**
Center frequency [GHz]	60	60	60	58	60	60	**60**
NF @ center freq. [dB]	4.4	5	7.1 (S)	4.4	4.6	8.6	**8.4**
Power gain (S_{21}) @ center freq. [dB]	16.8	25	16.1	22.7	14.1	10.2	**13.5**
BW_{3dB} [GHz]	16.4 (50.6–67)	7.5 (53.5–61)	15 (52–67)	9 (54–63)	6 (57–63)	10 (55–65)	**7 (57.3–64.3)**
IP_{1dB} [dBm]	−13	−22	−10	−16.1	−13.5	−11	**−15**
Voltage supply [V]	1.2	1.3	1.2	–	2.5	1	**0.9**
Current consumption [mA]	27.5	36.5	58.3	–	9.6	30	**11.6**
Power consumption [mW]	33	47	70	29.9	24	30	**10.4**
CMOS process [nm]	40	65	90	40	130	65	**28**
FoM (Huang, MWC [59])	2.46	1	0.57	2.01	0.98	0.45	**1.10**
FoM_1 (Gramegna, JSSC [63])	0.29	0.25	0.06	0.43	0.31	0.05	**0.20**
FoM_2 (Hsu, APMC [64])	4.76	1.84	0.84	3.90	1.87	0.54	**1.38**
FoM_3 (Asgaran, TCAS I [65])	0.87	0.09	0.33	0.62	0.84	0.26	**0.37**
FoM_4 (Fritsche, MTT [66])	238.54	11.64	83.56	95.61	83.57	43.25	**43.53**

(S): simulations; (M): measurements; (P): post-layout simulations;

$FoM = (\text{Gain [dB]} \cdot BW_{3dB}\,\text{[GHz]})/((NF\text{[dB]} - 1) \cdot P_{DC}\,\text{[mW]})$;
$FoM_1 = \text{Gain [dB]}/(P_{DC}\,\text{[mW]} \cdot (F-1))$; $FoM_2 = (\text{Gain [dB]} \cdot BW_{3dB}\,\text{[GHz]})/((F-1) \cdot P_{DC}\,\text{[mW]})$;
$FoM_3 = (\text{Gain [dB]} \cdot Freq\,\text{[GHz]} \cdot IP_{1dB}\,\text{[mW]})/((F-1) \cdot P_{DC}\,\text{[mW]})$;
$FoM_4 = (\text{Gain [dB]} \cdot IP_{1dB}\,\text{[mW]} \cdot BW_{3dB}\,\text{[GHz]})/((F-1) \cdot P_{DC}\,\text{[mW]})$; F is the noise factor.

4.2 Demodulator Description

The design of OOK/ASK demodulators for mm-wave applications has attracted significant research interest due to the growing demand for multi-Gbit/s short-range wireless communications in the unlicensed 60-GHz band. At these frequencies, the demodulator must guarantee high sensitivity, wide bandwidth, robustness against PVT variations, and low power consumption, while maintaining compact silicon area and compatibility with highly integrated receiver front-ends.

Early implementations of high-speed OOK envelope detectors were realized in SiGe bipolar technologies. In [27], a bipolar envelope detector operating at 60 GHz was proposed, demonstrating excellent high-frequency performance thanks to the intrinsic device characteristics. However, this solution relies on RF baluns and produces a single-ended output, requiring additional circuitry for differential processing. Subsequent works migrated toward CMOS technologies to reduce cost and enable full system-on-chip integration. Byeon *et al.* proposed several CMOS OOK demodulators in scaled technologies [21, 24, 26], achieving competitive performance using compact architectures. Nevertheless, these implementations are mainly based on single-ended topologies, requiring additional conversion stages before differential baseband processing. Other CMOS implementations have explored adaptive biasing and feedback techniques to improve robustness against PVT variations [67], while more recent

approaches have investigated offset-compensation strategies to enhance detection accuracy [68]. Despite these advancements, most reported designs still rely on single-ended or pseudo-differential architectures, often requiring *RF* baluns or additional circuitry, which increases complexity, power consumption, and sensitivity to supply and substrate noise.

From this literature review, it can be observed that fully differential demodulator architectures are still limited, particularly for Gbit/s 60-GHz applications. Fully differential solutions are inherently more robust against common-mode disturbances and better suited for integration with differential mm-wave front-ends. In this work, a fully differential CMOS OOK/ASK demodulator is considered to validate the capability of the proposed two-stage LNA to effectively drive a realistic load in a complete 60-GHz receiver chain. The demodulator performs envelope detection and baseband amplification while preserving a differential signal path, improving robustness against noise and process variations. The simplified architecture of the adopted demodulator is shown in Figure 4.12. It consists of a fully differential square-law rectification stage, followed by a summing circuit and cascaded differential gain stages. Additional auxiliary circuits are included to enhance robustness against PVT variations and device mismatch. The demodulator is directly connected to the LNA output through a center-tapped transformer, enabling fully differential signal transfer without requiring *RF* baluns or additional conversion stages. The processed signal is then amplified and buffered to drive measurement interfaces. Thanks to the differential signal path, improved immunity to common-mode disturbances and supply noise is achieved, which is particularly important at mm-wave frequencies.

It is important to note that the demodulator is not the primary focus of this thesis and is introduced only at a system level without detailed circuit analysis. The circuit has been developed as part of a separate research activity and has been filed as a patent [69]. Therefore, the inclusion of the demodulator in this work mainly serves to demonstrate that the proposed two-stage LNA is capable of properly driving a 60-GHz

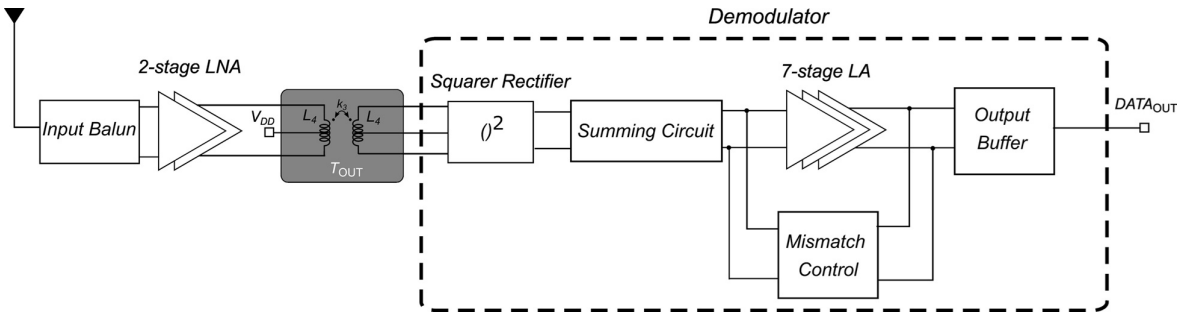


Figure 4.12: Simplified block diagram of the proposed fully differential OOK/ASK demodulator.

OOK/ASK demodulator within a fully integrated receiver, confirming the suitability of the adopted LNA design for low-power mm-wave applications. Overall, the adopted fully differential demodulator provides a compact and robust interface for the receiver chain, while confirming the suitability of the proposed LNA for low-power and highly integrated mm-wave applications.

4.3 Layout and Post-Layout Simulations

The layout of the receiver core, including the LNA and its interface to the demodulator, is shown in Figure 4.13. Figure 4.14 depicts the layout of the overall chip to be integrated in 28-nm CMOS by TSMC, whose overall size is 1300 μm $\times$ 1500 μm and includes both the 60-GHz receiver and a stand-alone 60-GHz LNA proposed in Section 4.1. The layout was designed to enable on-wafer characterization using GSG *RF* probes at both the input and output ports, while multi-contact DC probes are employed for biasing purposes. Conventional ESD protection structures have been integrated at the receiver output and DC pads to prevent potential transistor damage. At the 60-GHz receiver input, intrinsic ESD protection is inherently achieved through the LNA input transformer (T_{IN}), as discussed in Subsection 4.1.1.

The layout parasitics were primarily evaluated through EM simulations performed in ADS Momentum, using the substrate stack definitions provided by TSMC for the selected technology node. Conventional PLS tools were instead employed to extract and account for the RC parasitics within the demodulator blocks. A worst-case analysis was conducted considering both process corners and worst-case substrate configurations in ADS Momentum, with the objective of assessing the performance of the individual building blocks (i.e., the LNA and the demodulator) as well as the overall receiver.

All reported simulations were performed at nominal supply voltage and room temperature. Table 4.3 summarizes the expected performance of the overall receiver under nominal operating conditions at room temperature, whereas Table 4.4 reports the PLS results of the LNA when interfaced with the OOK demodulator. Figures 4.15–4.24 provide a comprehensive overview of the PLS performance of the proposed LNA when interfaced with the OOK demodulator and the complete receiver. In particular, Figures 4.15 and 4.16 illustrate the voltage gain and *NF* under nominal and worst-case process conditions, confirming that the LNA maintains sufficient gain and acceptable noise performance at the target sensitivity level. Figure 4.17 shows the gain compression behavior as a function of the input power, highlighting the linearity limits of the LNA and its ability to operate correctly within the targeted input signal range. The capability of the LNA to drive subsequent stages is further demonstrated in Figure

4.18, where the output voltage swing is evaluated versus input power at the maximum data rate. These results confirm that the LNA provides a sufficiently large output signal to ensure reliable demodulation. Stability considerations are addressed in Figure 4.19, where Rollett's stability factor is evaluated when the LNA is connected to the equivalent input impedance of the demodulator, confirming unconditional stability over the frequency range of interest. Figures 4.20 and 4.21 present the input and output matching of the complete receiver chain under nominal and worst-case conditions, indicating proper impedance matching and minimal signal reflection. The time-domain behavior of the system is illustrated in Figures 4.22 and 4.23, where the output signals at different data rates are shown, demonstrating correct demodulation and signal integrity even under worst-case conditions. Finally, Figure 4.24 reports the peak output signal as a function of the input power, confirming consistent system behavior and adequate signal levels across the expected operating range. Figure 4.25 verifies the stability of the complete receiver through the evaluation of Rollett's stability factor, K. Overall, these results validate that the proposed LNA, when integrated within the receiver chain, satisfies the required performance in terms of gain, bandwidth, linearity, and robustness, while effectively driving the OOK/ASK demodulator under realistic operating conditions.

Finally, local and global MC simulations were performed to evaluate the impact of device mismatch and process variations, respectively. Figure 4.26 illustrates the MC simulation results for the differential output of the final gain stage and the single-ended output voltage of the 50-Ω buffer, respectively. These results highlight the variability of the demodulated signal under statistical variations, providing insight into the robustness of the receiver chain. Despite these variations, the output signal maintains a consistent amplitude range, indicating reliable demodulation performance. It is important to note that the demodulator is included in this analysis primarily to emulate realistic loading conditions and to evaluate the overall signal propagation. Therefore, these results indirectly confirm that the proposed LNA is capable of delivering a sufficiently stable and robust signal to drive the subsequent stage under process and mismatch variations.

Table 4.3: RX expected performance in nominal conditions at room temperature.

Parameter	**Value**
Carrier frequency	60 GHz
Modulation	OOK
Max data rate	4 Gbit/s
Sensitivity ($P_{\mathrm{IN,MIN}}$)	-40 dBm
Maximum input signal ($P_{\mathrm{IN,MAX}}$)	-13 dBm
Supply voltage, V_{DD}	0.9 V
LNA power consumption	7.6 mW
Demodulator power consumption	2.5 mW
Total power consumption	10.1 mW (14.6 mW with buffer stage)
Technology	28-nm bulk CMOS (by TSMC) 9 metals: 2.8-μm thick ALUCAP, 3.5-μm thick M9

Table 4.4: Post-layout performance of the 60-GHz LNA connected to the OOK demodulator.

Parameters	**2-stage 60-GHz LNA**	**Unit**
Circuit topology	Pseudo-differential CAS+CS with transformer-based ESD protection	–
Center frequency	60	GHz
Noise figure @ 60 GHz	8.3	dB
Voltage gain	22.8	dB
BW_{3dB}	5.8 (58–63.8)	GHz
IP_{1dB}	-12.9	dBm
Output differential voltage to the demodulator (-40 dBm input power)	41 (peak)	mV
Voltage supply	0.9	V
Current consumption	8.4	mA
Power consumption	7.6	mW

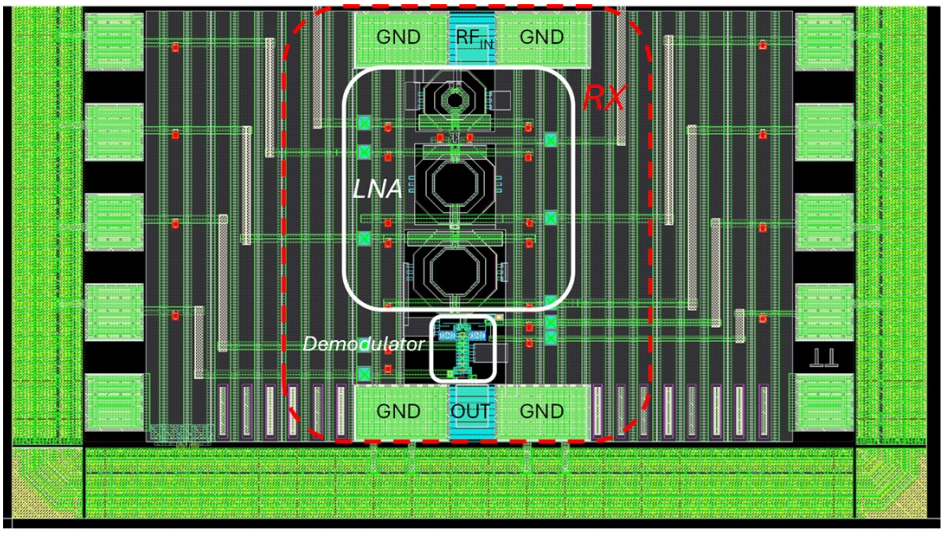


Figure 4.13: Layout of the 60-GHz OOK receiver for on-wafer testing.

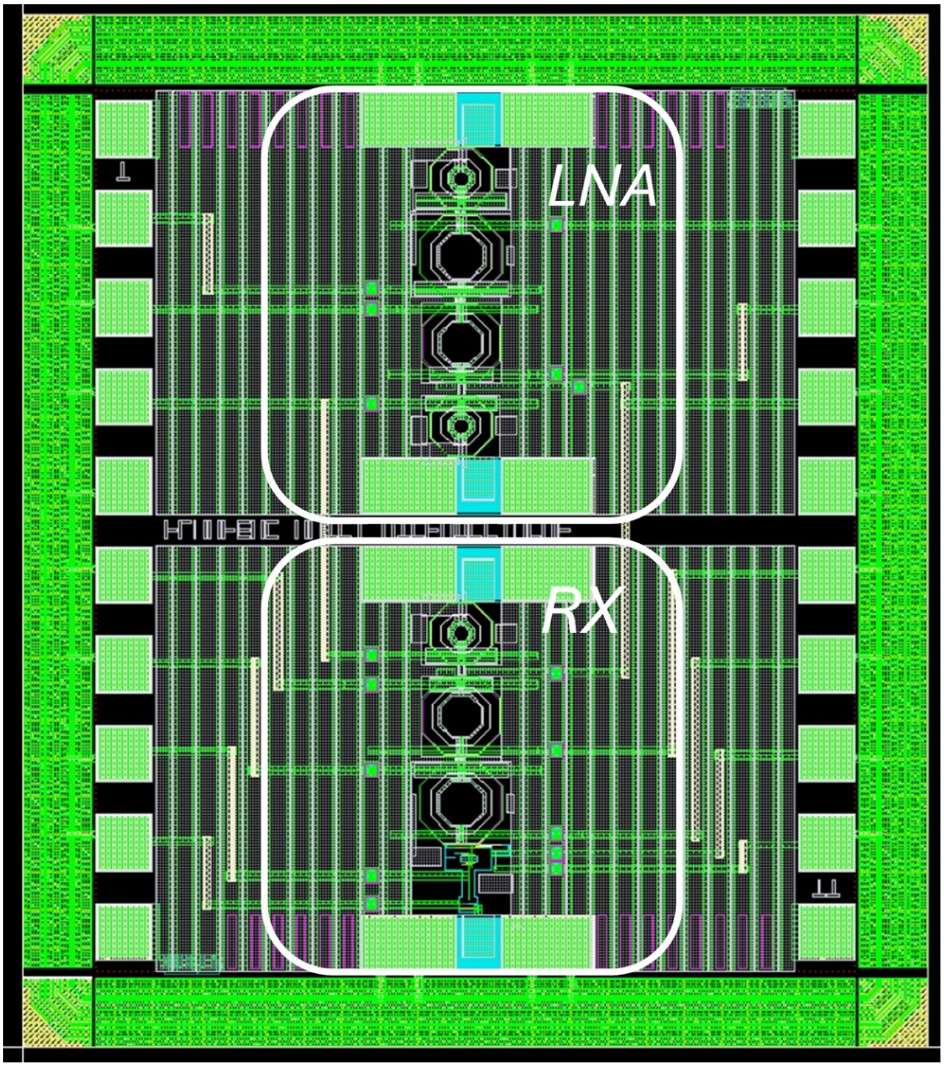


Figure 4.14: Layout of the overall chip to be integrated in 28-nm CMOS by TSMC.

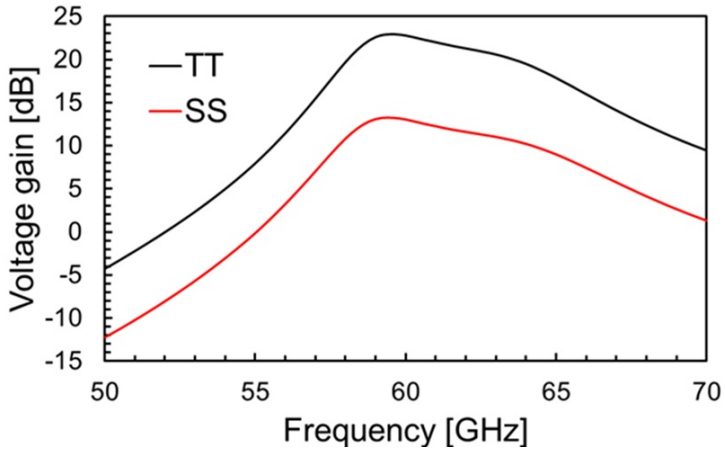


Figure 4.15: Post-layout LNA voltage gain in nominal (TT) / worst case (SS) at −40-dBm input power.

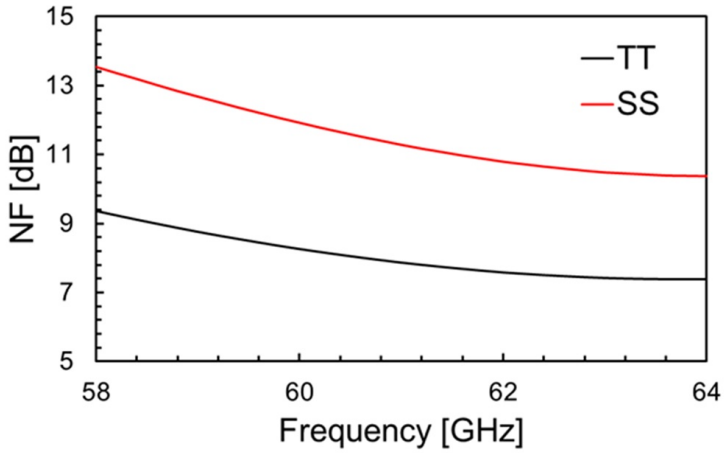


Figure 4.16: Post-layout LNA noise figure in nominal (TT) / worst case (SS) at −40-dBm input power.

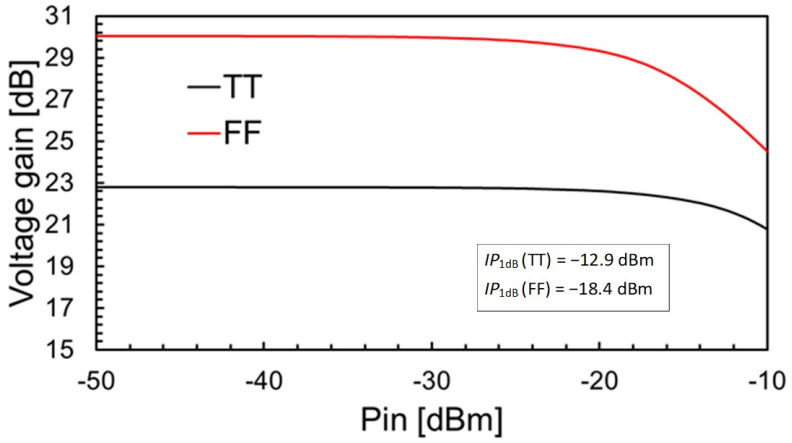


Figure 4.17: Post-layout LNA voltage gain @ 60 GHz vs. input power, P_{in}, in nominal (TT) / worst case (FF).

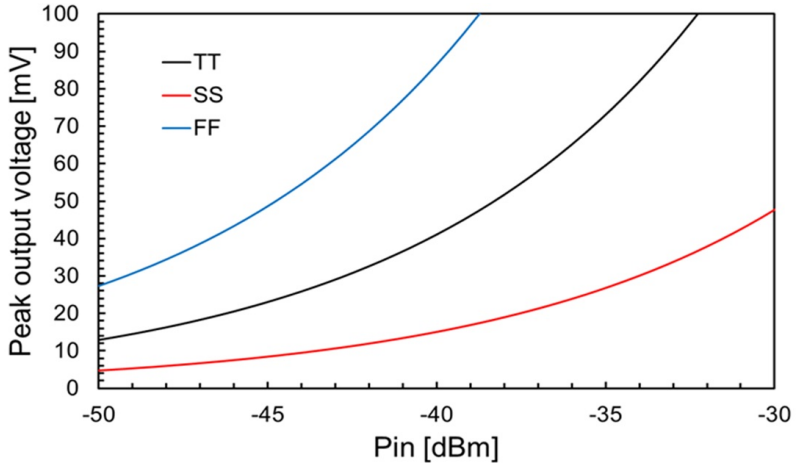
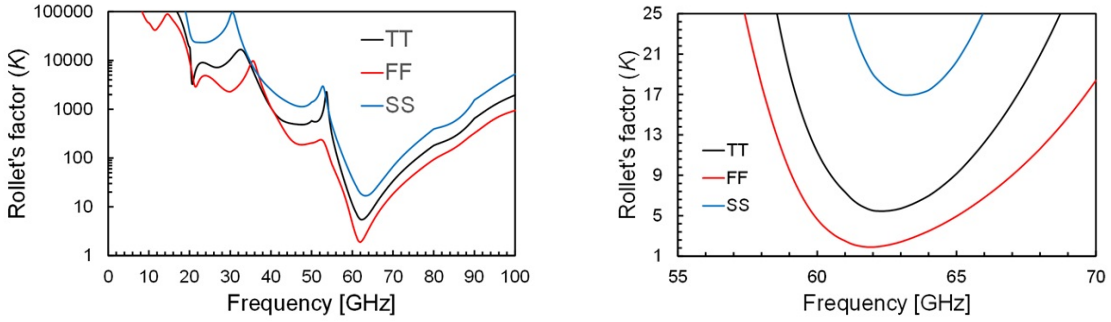


Figure 4.18: Post-layout LNA output peak voltage vs. input power, P_{in}, in nominal (TT) / worst case (SS – FF) at the maximum data rate (4 Gbit/s).



(a) (b)

Figure 4.19: Post-layout Rollett's stability factor simulation of the LNA closed to the equivalent input impedance of the OOK demodulator: (a) wideband simulation, (b) in-band simulation.

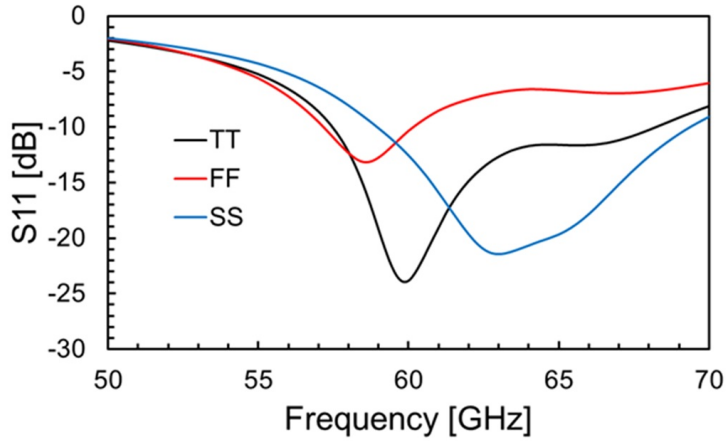


Figure 4.20: RX PLS: Input matching (S_{11}) in nominal/worst cases.

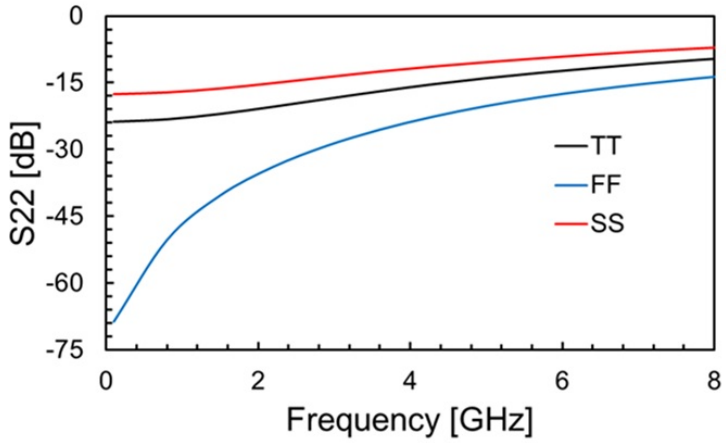


Figure 4.21: RX PLS: Output matching (S_{22}) in nominal/worst cases.

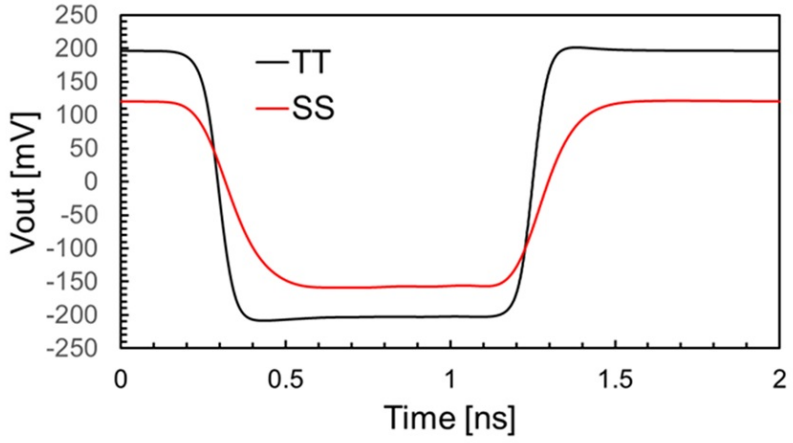


Figure 4.22: RX PLS: Output signal vs time at 1 Gb/s in nominal/worst case (P_{in}=−40 dBm).

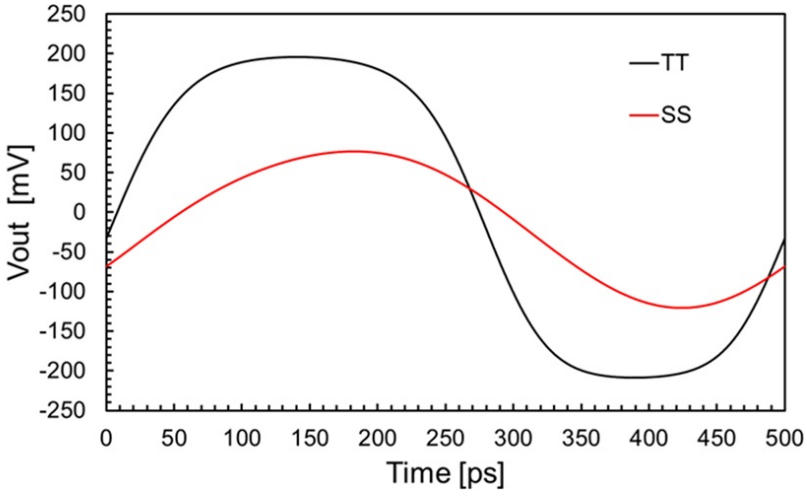


Figure 4.23: RX PLS: Output signal vs time at maximum data rate (4 Gbit/s) in nominal/worst case (P_{in}= −40 dBm).

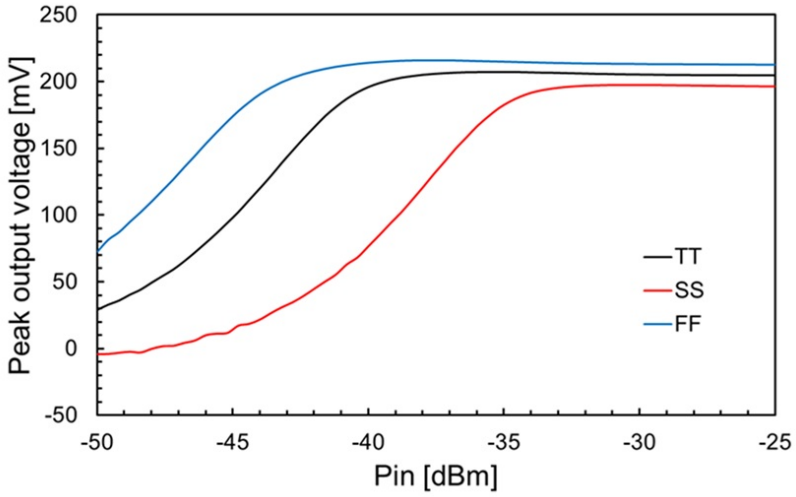
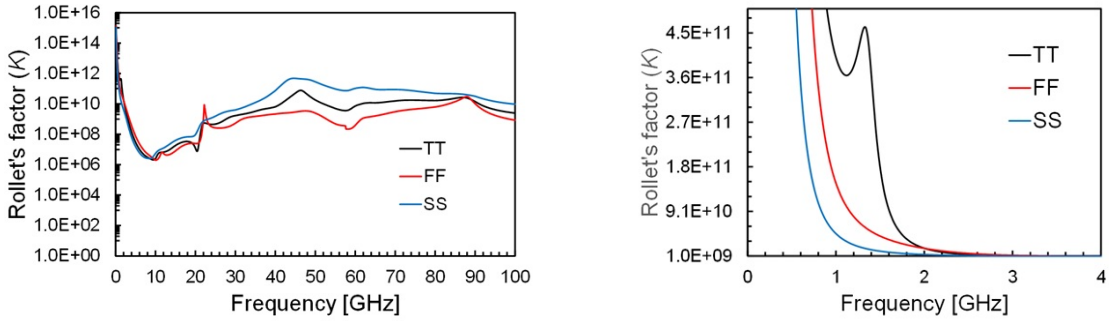
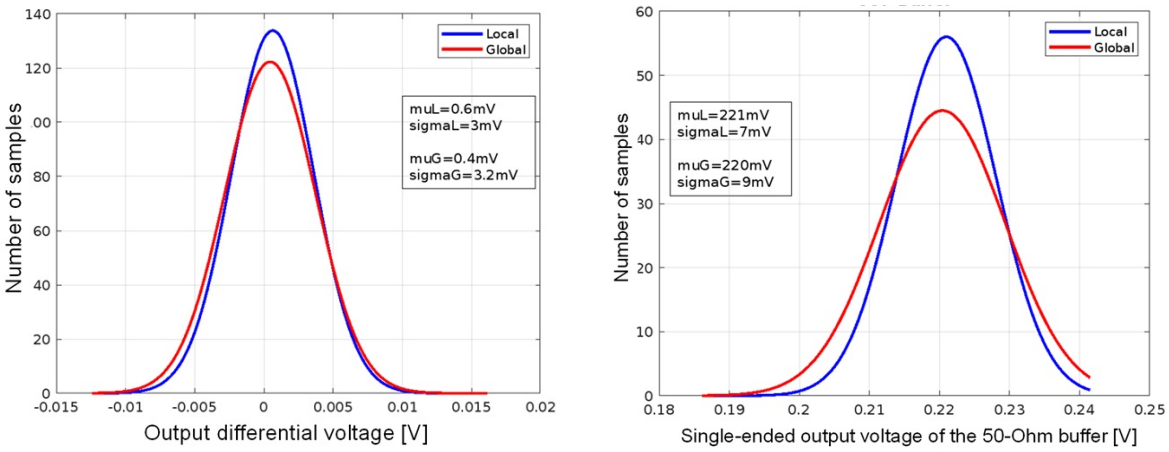


Figure 4.24: RX PLS: Peak output signal at maximum data rate (4 Gbit/s) vs input power (P_{in}).



(a) (b)

Figure 4.25: Post-layout Rollett's stability factor simulation of the receiver closed to 50-Ohm terminations: (a) wideband simulation, (b) in-band simulation.



(a) (b)

Figure 4.26: MC simulations: (a) differential output of the last gain stage; (b) single-ended output voltage of the 50-Ω buffer.

5 Testing and Experimental Characterization

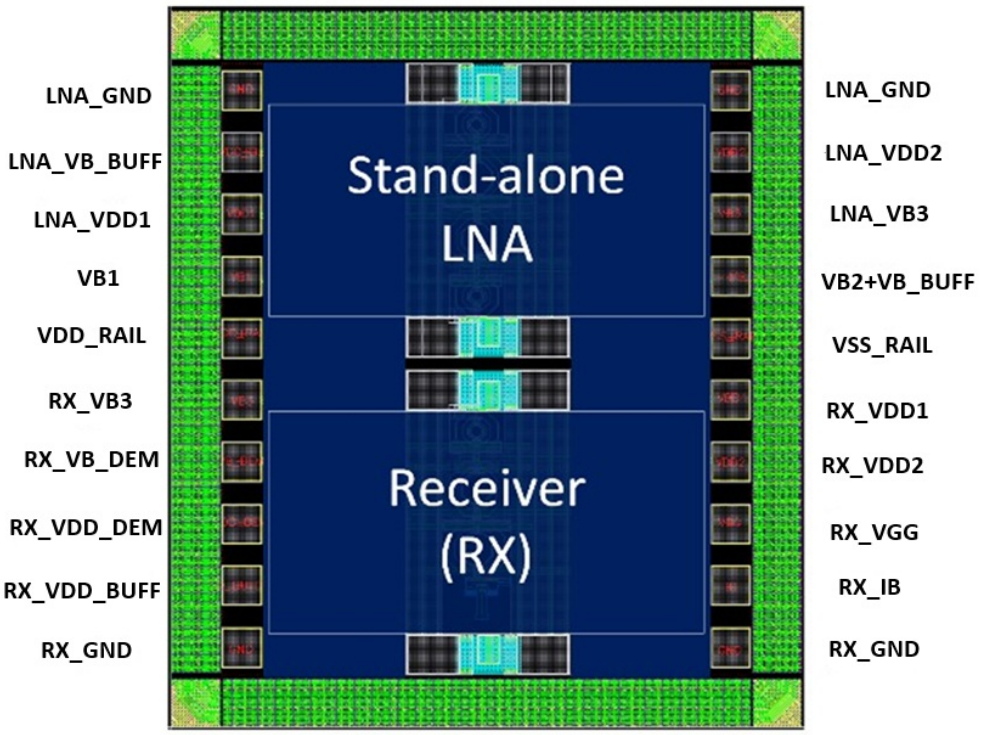
5.1 Test Setup and Measurement Techniques

The experimental validation of the proposed 60-GHz front-end has been carefully planned since the early design stages, with the objective of enabling independent characterization of both the complete OOK receiver and the stand-alone LNA while complying with technology and probing constraints. The fabricated chip occupies an overall area of 1300 µm × 1500 µm and and as shown in Figure 5.1 integrates two main blocks: the 60-GHz OOK receiver positioned in the lower section of the die and a stand-alone version of the LNA located in the upper section.

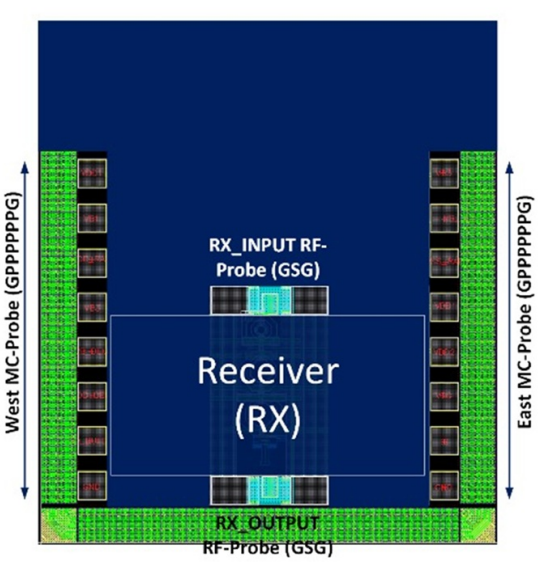
The adopted floorplan results from multiple design constraints. First, the die dimensions must satisfy the width and height limitations imposed by the TSMC process (as depicted in Figure 5.2). Second, the layout must be compatible with mm-wave on-wafer probing restrictions, particularly regarding probe pitch and mechanical clearance. Third, the placement of input and output *RF* pads must preserve symmetry and minimize routing parasitics. Finally, cost minimization and integration simplicity were also considered. The resulting arrangement enables independent electrical characterization of the receiver and the stand-alone LNA through appropriate probe configurations without modifying the chip layout.

On-wafer testing is performed using two GSG *RF* probes positioned on the north and south sides of the chip and two multi-contact DC probes placed on the east and west sides. To guarantee safe mechanical operation, a clearance distance exceeding 1000 µm has been introduced between the two vertical DC probe arrays. In the implemented design, a spacing of approximately 1032 µm, as shown in Figure 5.3, is adopted, which ensures that the *RF* probe tips can be positioned between the DC probes without interference. Mechanical verification performed in collaboration with MPI confirmed that this configuration provides sufficient margin, leaving about 130 µm of clearance on both sides of the *RF* ground tips. This careful mechanical planning prevents probe contact overlap and enables reliable mm-wave measurements.

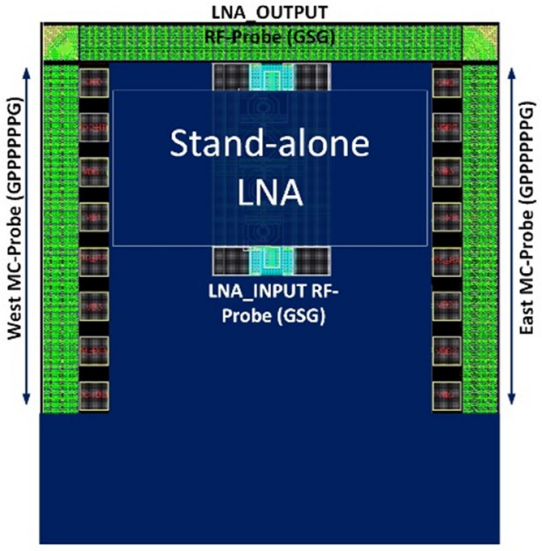
The proposed floorplan supports two distinct measurement configurations. In the first configuration, the complete 60-GHz OOK receiver is characterized, allowing evaluation of gain, sensitivity, and demodulation performance. In the second configuration,



(a)



(b)



(c)

Figure 5.1: Floorplan and measurement configurations: (a) labeled chip floorplan; (b) receiver testing configuration; (c) stand-alone LNA testing configuration.

the stand-alone LNA is measured independently, enabling accurate *RF* characterization without the influence of the demodulator load. This dual-configuration strategy

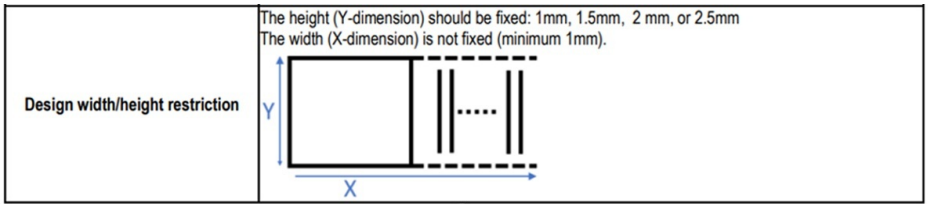
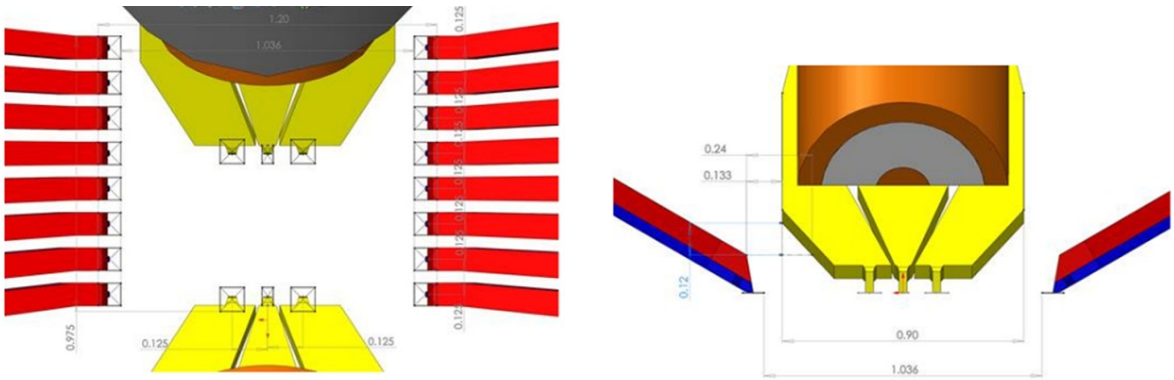


Figure 5.2: Design width/height restriction imposed by TSMC.



(a) (b)

Figure 5.3: Measurement probe setup: top view (a) and front cross-section (b).

allows precise comparison between block-level and system-level behavior.

The chip includes dedicated DC pad arrays on the east and west sides, each composed of ten pads, allowing independent biasing of the LNA stages, the receiver amplification stages, the demodulator core, and the output buffers. Separate ground domains are implemented for the LNA and the receiver sections to minimize coupling during measurements. The pad mapping has been designed to provide full flexibility in bias adjustment and debugging while preserving signal integrity.

The stand-alone LNA is characterized in the UNICT laboratories using a two-port R&S ZVA40 vector network analyzer (VNA) connected to Z90 mm-wave extension heads and mounted on an MPI TS200THZ probe station. This setup enables *S*-parameter extraction up to 90 GHz, compression point measurements, and stability analysis. The complete receiver characterization requires additional instrumentation to generate 60-GHz OOK-modulated signals. Such measurements are performed either through dedicated laboratory equipment that will available in the next months.

For wafer-level measurements, singularized dies are temporarily attached to a sacrificial wafer to facilitate probing. In addition, selected samples are packaged on customized printed circuit boards to allow board-level characterization. This dual approach ensures both controlled wafer-level *RF* evaluation and practical system-level validation.

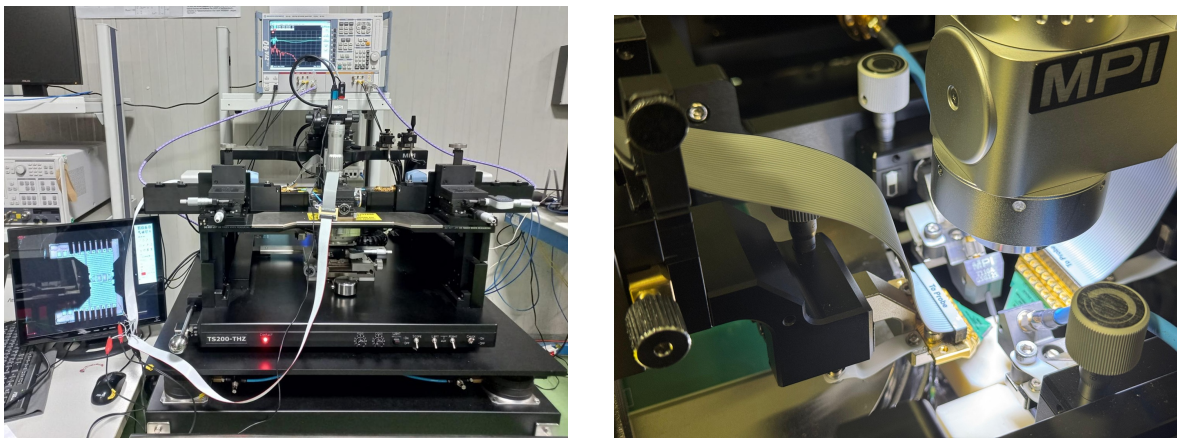
The experimental campaign aims to validate the main performance parameters

predicted by post-layout simulations, including gain, bandwidth, *NF*, linearity, power consumption, and demodulated output amplitude. Special attention is devoted to verifying the accuracy of electromagnetic simulations of the transformer-based matching networks and to assessing the robustness of the intrinsic ESD protection strategy implemented through the input transformer.

Overall, the testing methodology has been co-designed with the chip layout to ensure measurement reliability, mechanical compatibility with mm-wave probing equipment, and independent block-level validation. This strategy enables comprehensive experimental characterization of the proposed 60-GHz integrated front-end while preserving design flexibility and minimizing measurement uncertainty.

5.2 Performance Analysis and Comparison with Post-Layout Simulated Results

After validating the measurement setup described in the previous section, the fabricated chip was experimentally characterized through on-wafer measurements. Figure 5.4 shows photographs of the measurement environment and the probing configuration used during the experimental characterization. The measurements were performed using a probe station equipped with GSG *RF* probes connected to a VNA through calibrated coaxial cables. DC biasing was provided through multi-contact probes connected to external power supplies, allowing independent control of the bias voltages required by the LNA and receiver circuits.

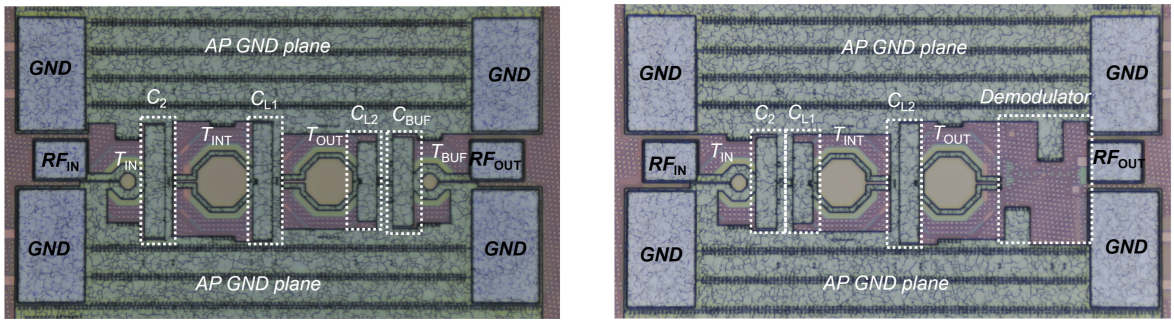


(a) (b)

Figure 5.4: Measurement environment (a) and probe configuration(b).

Figure 5.5 reports the microphotographs of the fabricated chips, including the standalone 60-GHz LNA and the complete 60-GHz OOK receiver implemented in the same

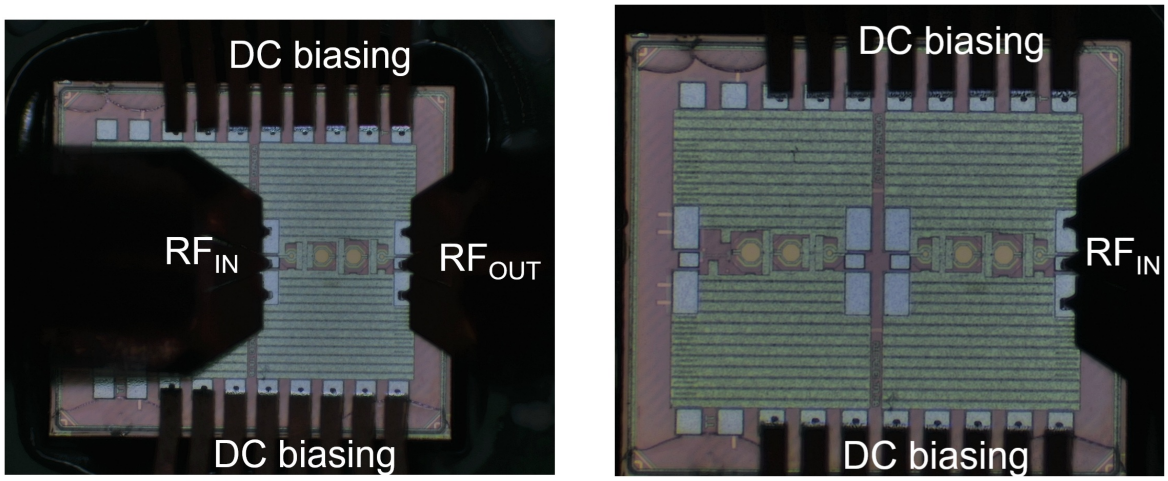
die. The LNA occupies the central portion of the structure and integrates the input transformer, interstage matching network, and output buffer. The receiver configuration additionally includes the fully differential OOK demodulator connected at the LNA output. Both structures were designed to enable direct on-wafer testing through *RF* input and output pads placed along the chip edges.



(a) (b)

Figure 5.5: Microphotographs of fabricated chips, standalone LNA(a) and 60-GHz OOK receiver(b).

The on-wafer probing configuration used for the measurements is illustrated in Figure 5.6. The *RF* input and output signals were applied through GSG probes connected to the corresponding pads of the device under test, while DC biasing was provided through dedicated probing pads located along the upper and lower sides of the chip. This configuration allowed accurate characterization of the *RF* performance of both the stand-alone LNA and the complete receiver front-end.

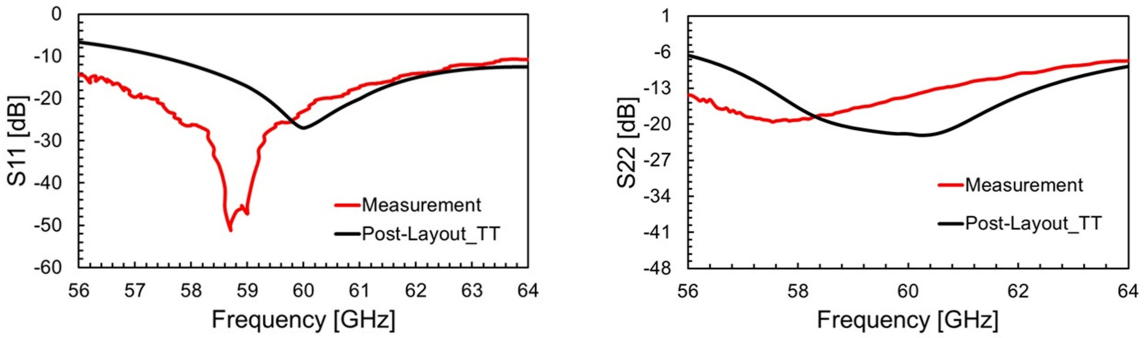


(a) (b)

Figure 5.6: On-wafer probing configuration for, standalone LNA(a) and 60-GHz OOK receiver(b).

The measured small-signal performance of the standalone LNA is reported in Figure

5.7. The measured input reflection coefficient S_{11} shows a clear resonance around 59 GHz, indicating proper operation of the input matching network implemented using the integrated transformer and LC tank. The measured minimum value of S_{11} reaches approximately -50 dB near the resonance frequency, demonstrating good impedance matching. The output matching parameter S_{22} is also reported and remains below approximately -10 dB in the operating band, confirming acceptable output impedance matching toward the following stages.



(a) (b)

Figure 5.7: LNA measured input (S_{11}) and output (S_{22}) matching versus frequency.

The measured power gain of the standalone LNA and post-layout simulations considering different process corners are shown in Figure 5.8. While simulations predicted a peak gain of approximately 13 dB around 60 GHz, the measured gain is lower beside of frequency drift. This behavior is mainly attributed to process variations and parasitic effects affecting the integrated passive components. In particular, the measured response suggests the presence of a slow–slow (SS) transistor corner combined with variations in the substrate parameters. In this condition, the effective capacitance of the LC tank of the first stage may increase by approximately 10–15%, shifting the resonance frequency toward lower frequencies. The increased capacitance also reduces the effective load impedance of the resonant network, resulting in a reduction of the overall voltage gain. The simulated response including the SS corner and an increased capacitance in the LC tank provides a trend that better follows the measured curve, confirming that the observed gain degradation is mainly related to process variations rather than circuit malfunction. In addition, the frequency shift observed in both S_{11} and S_{22} responses is consistent with the same capacitance increase affecting the input and output resonant networks.

Finally, the input matching of the complete receiver was experimentally evaluated and is shown in Figure 5.9. The measured S_{11} of the receiver follows a trend similar to that obtained for the stand-alone LNA, confirming that the receiver input impedance is

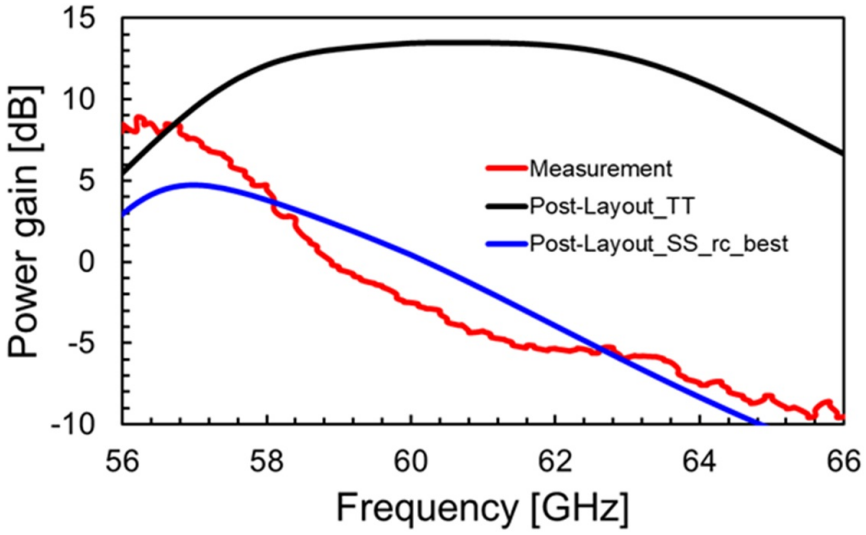


Figure 5.8: LNA measured power gain versus frequency.

dominated by the LNA matching network. This result validates the correct integration of the LNA and the demodulator blocks within the receiver architecture.

Table 5.1 summarizes the comparison between the post-layout simulations and the available experimental results of the standalone LNA. The measurements confirm the correct operation of the fabricated LNA, although a downward shift of the operating frequency and a reduction in peak gain are observed. These discrepancies are mainly attributed to process variations and parasitic effects affecting the integrated passive components, particularly the transformer-based matching networks. Despite these deviations, both the input and output matching remain satisfactory within the operating

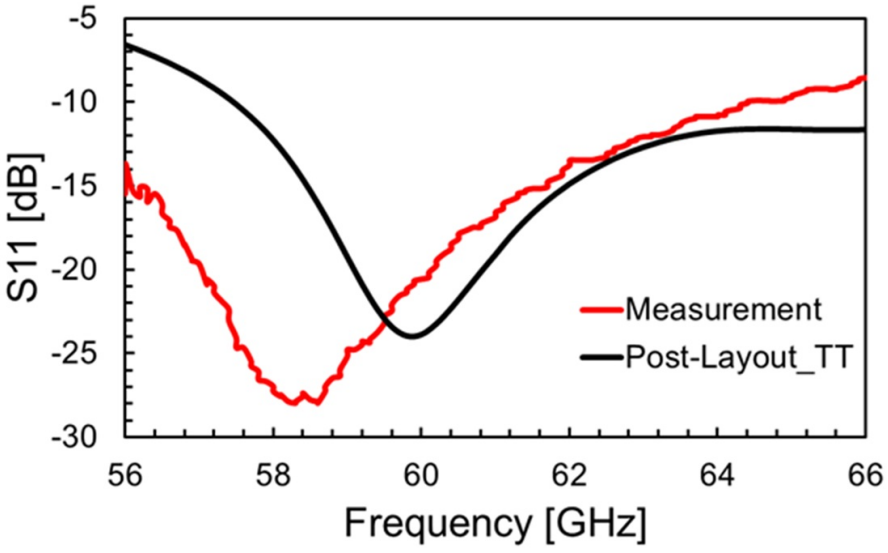


Figure 5.9: RX measured input matching (S_{11}) versus frequency.

Table 5.1: Quantitative comparison between post-layout simulated and experimentally measured performance of the fabricated 60-GHz standalone LNA.

Parameter	**Post-layout Simulation**	**Measurement**
Peak gain (S_{21})	13.5 dB @ 60 GHz	8.5 dB @ 56 GHz
Peak gain frequency	60 GHz	56 GHz
Input matching (S_{11})	≈–27 dB @ 60 GHz	≈–50 dB @ 58.8 GHz
Output matching (S_{22})	≈–22 dB @ 60 GHz	<–10 dB over the band
3-dB bandwidth (BW_{3dB})	7 (57.3–64.3) GHz	3 (54.6–57.6) GHz
Supply voltage	0.9 V	0.9 V
Power consumption	10.4 mW	10.4 mW
Noise Figure (NF)	8.4 dB	Not measured
IP_{1dB}	–15 dBm	Not measured

band, confirming the robustness of the proposed design methodology. The NF and the input IP_{1dB} could not be experimentally characterized. NF measurements at 60 GHz require a calibrated mm-wave noise measurement setup that was not available during the measurement campaign. Similarly, IP_{1dB} characterization requires high-power calibrated mm-wave signal generation together with suitable large-signal measurement instrumentation, which was also unavailable. Consequently, these performance metrics are reported only through post-layout simulations.

Full experimental characterization of the complete OOK receiver in terms of data rate, sensitivity, and bit error rate could not yet be performed due to the current lack of instrumentation capable of generating and analyzing 60-GHz high-data-rate modulation signals. Nevertheless, the available measurements confirm the correct operation of the RF front-end and validate the implemented design approach for mm-wave receiver circuits in 28-nm CMOS technology.

6 Highly Linear LNA for 60-GHz Wireless Communications

6.1 State-of-the-art of Linearization Techniques

The design of highly linear mm-wave LNAs has become increasingly critical as modern 60-GHz systems operate in dense spectral environments and face strong interferers at short distances. While small-signal linearity metrics such as *IIP3* remain important, the true bottleneck in practical receiver robustness is large-signal linearity, especially the $IP_{1\mathrm{dB}}$. When a nearby device or transmitter generates high-power bursts, the front-end LNA is the first circuit to encounter these large voltage swings. If the LNA compresses, both sensitivity and demodulation accuracy of the receiver degrade dramatically. Therefore, maintaining a high $IP_{1\mathrm{dB}}$ is essential for ensuring reliable operation in real-world 60-GHz use-cases, such as mm-wave radar, unlicensed-band coexistence, multi-antenna front-ends, and indoor high-data-rate links. Despite this importance, most linearity-enhancement techniques proposed in literature focus primarily on small-signal distortion reduction rather than on improving $IP_{1\mathrm{dB}}$. This mismatch between practical needs and available circuit techniques establishes a clear gap in state-of-the-art mm-wave LNA research and directly motivates the development of the high-linearity architecture introduced in the next section.

Traditional linearization strategies, such as the derivative superposition (DS) method shown in Figure 6.1, have historically been used to cancel third-order nonlinearity by combining transistors biased at different operating points [70]. Although DS is effective at lower *RF* frequencies, its applicability significantly deteriorates at mm-wave frequencies. Parasitic reactances disrupt the delicate phase and amplitude cancellation required for DS, while mismatch and PVT variations introduce additional error sources. Even modified DS techniques employing independent source inductors or auxiliary matching networks (Figure 6.2) [71] provide only limited benefit for 60-GHz LNAs and mainly improve *IIP3*, not $IP_{1\mathrm{dB}}$. Thus, they do not address blocker-induced compression, which is often the more critical requirement in mm-wave systems.

Other methods rely on bias optimization or transconductance shaping. Adjusting the bias point to minimize g_{m} curvature can improve weak-signal linearity but only within a narrow operating region and often at the expense of noise and gain [72]. These techniques are also rendered less effective by the reduced voltage headroom of

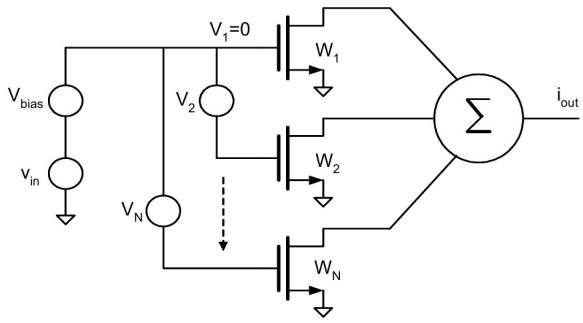


Figure 6.1: Derivative superposition (DS) technique [70].

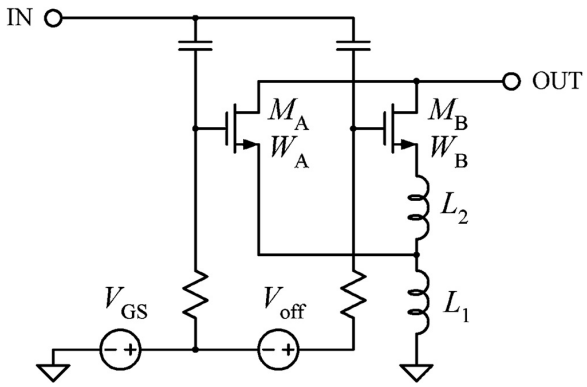


Figure 6.2: Modified DS method [71].

advanced CMOS technologies, which restricts bias programmability. Similarly, multi-tanh or complementary-g_{m} structures (Figure 6.3), while effective in bipolar or low-frequency CMOS designs, do not translate well to mm-wave implementations due to dominant parasitics and strict impedance-matching constraints [70]. Local feedback techniques such as inductive source degeneration, used in many mm-wave LNAs, introduce beneficial negative feedback that linearizes the g_{m} characteristic while also improving stability and input matching [70]. Source degeneration remains one of the strongest and most reliable linearization mechanisms available at 60 GHz. However, the improvement in $IP_{1\mathrm{dB}}$ remains modest because the degeneration inductor is intrinsically small at mm-wave frequencies and its linearizing effect saturates with increasing signal swing. Moreover, degeneration simultaneously reduces gain, creating a trade-off that limits its use as the primary means of boosting large-signal linearity.

Another branch of linearization research focuses on harmonic termination and impedance shaping, where the goal is to control the impedance seen by harmonic currents so that nonlinear interactions are suppressed. Well-designed harmonic terminations can improve gain and efficiency in power amplifiers and reduce distortion in LNAs (Figure 6.4), but implementing accurate impedance environments at 60 GHz is

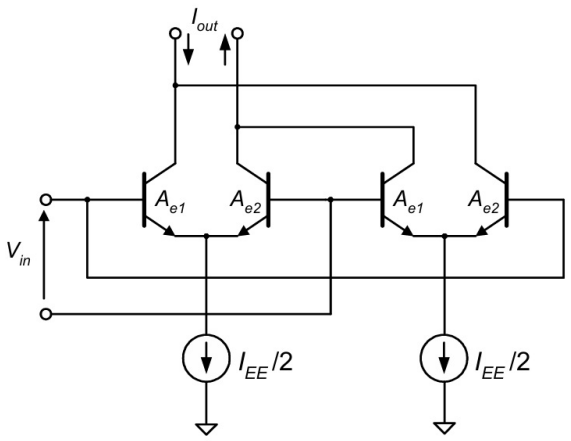


Figure 6.3: Multi-tanh method [70].

difficult [72]. At mm-wave frequencies, the transistor, interconnect, and layout parasitics all contribute significantly to the effective impedance profile, making fine control of higher-order harmonics challenging. Even when effective, harmonic termination primarily enhances *IIP3* and does not fundamentally increase the LNA's ability to handle large input blockers without compressing.

A related family of techniques uses output impedance shaping, which limits voltage swings at critical nodes. Excessive voltage buildup at the output exacerbates g_{m} collapse and early compression. Techniques such as transformer turn-ratio tuning, resonant-load shaping, or embedded band-stop structures have been employed in mm-wave designs to control output impedance [72]. These improve stability and distortion behavior but still fall short of delivering high $IP_{1\mathrm{dB}}$ performance. At lower frequencies, parallel preselect filters (PFs) divert blocker-induced currents away from the LNA core [73]. Although their active implementation is not scalable to 60 GHz,

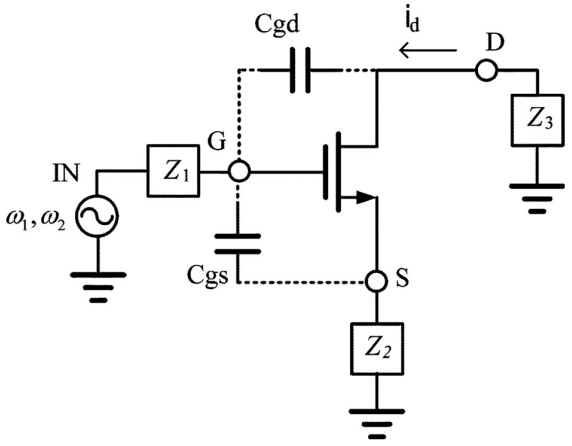


Figure 6.4: Harmonic termination method [72].

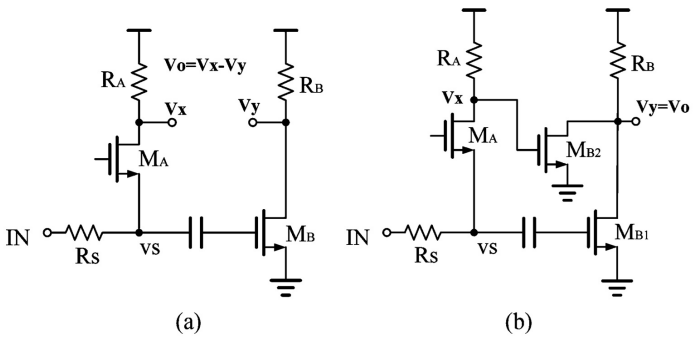


Figure 6.5: Noise/distortion cancellation method [72]. (a) differential output, (b) single-ended output.

the underlying principle inspires passive PF equivalents, such as stubs or frequency-selective transformer branches, which provide partial out-of-band current shunting. These structures help mitigate blocker-induced distortion but are limited by mm-wave passive losses and layout constraints. Noise/distortion cancellation architectures, combining common-source and common-gate stages (Figure 6.5), have demonstrated strong distortion reduction at lower *RF* frequencies [72]. Yet at 60 GHz, precise amplitude and phase matching is extremely difficult due to interconnect parasitics, device mismatch, and frequency-dependent path delays. As a result, distortion cancellation is rarely used in practical mm-wave LNAs.

Similarly, post-distortion and feedforward linearization techniques [72], including those demonstrated in [74–76], generate replicas of distortion signals to cancel them at the output (Figure 6.6). These methods require extremely accurate phase and amplitude control, making them unsuitable for compact, low-power 60-GHz receivers. Out-of-band (OOB) linearization techniques, illustrated in Figure 6.7, manipulate the impedance environment at harmonic or baseband frequencies to promote cancellation between direct and indirect *IM3* components [70]. Although passive OOB impedance shaping is feasible at 60 GHz, the resulting improvement is incremental and does not fundamentally address large-signal compression. Differential architectures inherently reduce even-order distortion and improve immunity to supply and substrate fluctuations. When combined with common-mode feedback (CMFB), they suppress low-frequency distortion and stabilize internal node voltages. However, while differential operation improves overall robustness, it does not deliver the dynamic load modulation needed for significant $IP_{1\mathrm{dB}}$ enhancement.

Finally, recent radar-oriented designs have explored cancellation loops, shown in Figure 6.8, that sense the amplitude and phase of residual TX spillover and inject a cancellation current at the LNA output [77]. Although these adaptive cancellation

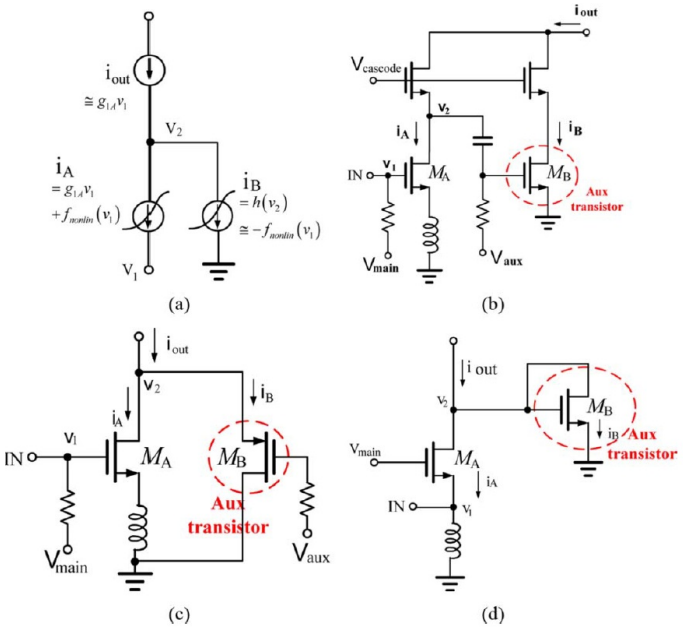


Figure 6.6: Post-distortion method [72]. (a) the concept of the method [74], (b) proposed in [75], (c) proposed in [76].

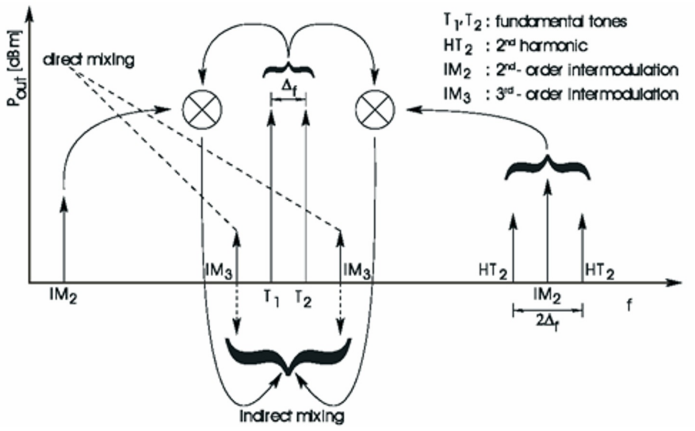


Figure 6.7: Out-of-band linearization technique [70].

loops provide impressive linearity benefits, implementing them at mm-wave frequencies is challenging due to the need for finely tuned delay and phase control. Nevertheless, the underlying principle, suppression of self-interference through auxiliary cancellation paths, inspires mm-wave designers to consider passive cancellation approaches, such as transformer-based nulling, that reduce the impact of TX leakage without requiring high-speed analog control loops.

A survey of published 60-GHz LNAs reveals a striking pattern: virtually all reported designs optimize *NF*, gain, or small-signal linearity, but almost none achieve a high $IP_{1\text{dB}}$, and no work demonstrates $IP_{1\text{dB}} \geq 0$ dBm at 60 GHz. This is partic-

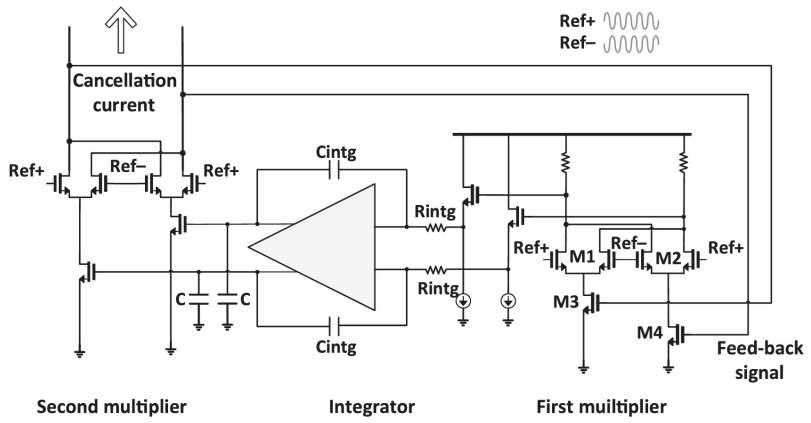


Figure 6.8: Cancellation loop schematic proposed in [77].

ularly notable because modern mm-wave environments, dense indoor networks, overlapping WLAN channels, proximity to phased-array transmitters, regularly expose the front-end to large blocker levels. Despite this, the literature shows very limited exploration of architectural solutions to improve large-signal linearity. This gap indicates that existing linearization methods are insufficient for next-generation mm-wave receivers, especially those targeting robust operation in interference-rich environments. The limitations of classical techniques highlight the need for new architectures capable of boosting $IP_{1\mathrm{dB}}$ without degrading *NF*, gain, or power consumption. In particular, approaches that exploit controlled load modulation, traditionally used in power amplifiers, offer a promising path but have not been widely explored in mm-wave LNAs. A fully differential architecture provides inherent cancellation of even-order distortion and creates a more favorable impedance environment under large swings. When combined with a modified power-combining configuration, it enables the gain expansion and dynamic load modulation required to significantly extend the linear input range.

This insight forms the foundation of the design introduced in Section 6.2: a 60-GHz highly linear LNA that leverages differential operation and load modulation to achieve a remarkable 6.5-dB improvement in $IP_{1\mathrm{dB}}$, exceeding 0 dBm at 60 GHz, an outcome not previously reported in the literature. Importantly, this enhancement is achieved while maintaining an excellent balance among gain, *NF*, power consumption, and area, demonstrating that high large-signal linearity at mm-wave frequencies does not require compromising other key performance metrics. The following section presents the proposed architecture in detail, highlighting the circuit techniques, passive structures, and trade-offs that enable this unprecedented level of linearity in a fully integrated 60-GHz LNA.

6.2 Proposed Architecture for Highly Linear LNA

The limitations of conventional linearization techniques discussed in Section 6.1 highlight the need for an architectural solution capable of significantly improving large-signal linearity, and in particular the IP_{1dB}, without compromising *NF*, gain, or power efficiency. To address this challenge, this work proposes a fully differential 60-GHz high-linearity LNA based on a power-combining architecture with load modulation, specifically re-engineered for mm-wave receiver front-ends. Indeed, the proposed architecture adapts the concept of load modulation to an LNA context with the goal of extending the linear input range. The fundamental idea is to modify the effective load impedance seen by the main amplification path as input signal level increases, thereby preventing early gain compression and enabling gain expansion under large-signal operation. Simulation results demonstrate that the proposed architecture achieves an overall improvement of approximately 6.5 dB in IP_{1dB}. The improvement in large-signal linearity relies on the inherent current-sharing and load-modulation behavior of the two-path structure. Under increasing input signal levels, the total *RF* current delivered to the output node is distributed between the two parallel amplification paths, while the power combining network reduces the effective load impedance (R_{eff}) seen by each path. As a result, for a given maximum voltage swing limited by the supply voltage, approximately twice the *RF* current is required to reach compression, leading to an overall four-fold increase in the allowable input power before compression, as demonstrated by (6.1). This corresponds to an improvement of approximately 6 dB in IP_{1dB} and pushing it beyond 0 dBm at 60 GHz, an unprecedented result for CMOS LNAs at this frequency.

$$\frac{P_{\text{1dB, two-path}}}{P_{\text{1dB, one-path}}} = 2 \times \left(\frac{R_{\text{eff}}}{R_{\text{eff}}/2} \right) = 4 \tag{6.1}$$

The same reasoning generalizes to a modular N-path structure: if the combining network shapes the large-signal effective load so that each path experiences R_{eff}/N, then the sustainable fundamental current per path scales approximately by N, and the corresponding compression-limited power capability can scale as N^2 (i.e., $10\log_{10}(N^2) = 20\log_{10}(N)$ dB), subject to practical limits such as passive losses, imbalance, and device headroom.

At 60 GHz, the dominant mechanism limiting IP_{1dB} is the collapse of transconductance and excessive voltage swing at critical nodes of the LNA core. Classical techniques such as source degeneration or harmonic termination offer only limited improvements, typically on the order of 1–2 dB, and are insufficient to address strong blocker scenarios commonly encountered in dense indoor mm-wave environments. The

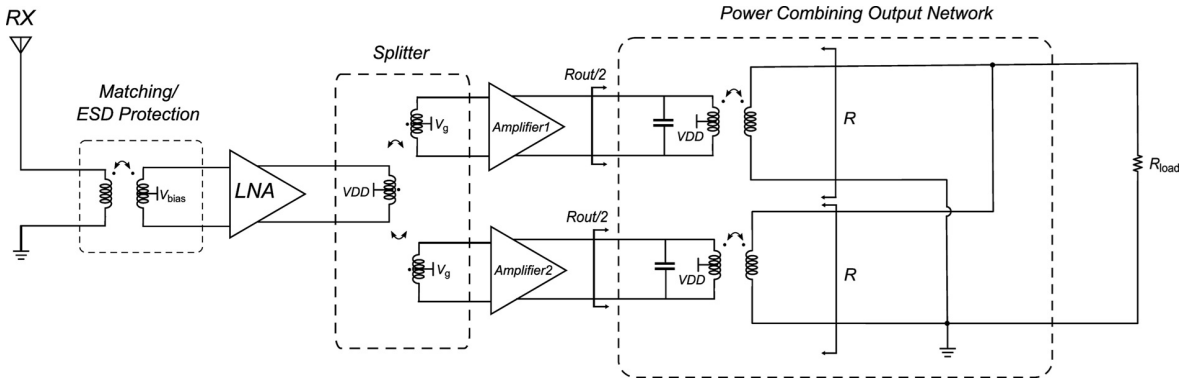


Figure 6.9: Proposed power-combining LNA block diagram.

load-modulation offers a fundamentally different approach by exploiting controlled current injection from an auxiliary path, which alters the load impedance of the main path in a signal-dependent manner.

In the proposed design, this principle is implemented through a two-path architecture, consisting of a main amplifier (Amplifier1) and an auxiliary amplifier (Amplifier2), as shown in Figure 6.9. The proposed LNA adopts a simplified implementation in which the auxiliary amplifier is permanently present and statically biased. In this way, the two paths work together independently from the input signal level. This design choice is intentional and aims to avoid the additional circuit complexity, power overhead, and sensitivity to PVT variations associated with adaptive biasing or envelope-controlled activation. This approach preserves the essential load modulation effect since the output network performs an impedance transformation, while ensuring a compact, robust, and layout-friendly implementation suitable for mm-wave operation.

The linearity advantage provided by the proposed load-modulated, power-combining LNA can be fully exploited only if the overall receiver compression is not limited by an earlier block (e.g., an input interface, a preceding amplifier stage, or any other front-end component). In a cascade, the first stage that enters compression effectively determines the maximum tolerable input level of the chain. Therefore, achieving a higher $IP_{1\mathrm{dB}}$ at the proposed LNA is beneficial only if upstream blocks maintain sufficiently high linearity margins and the gain distribution is selected so that subsequent blocks do not become the new compression bottleneck. This requires a careful gain/NF/linearity budget across the receiver chain, where the first stage is still optimized for low noise, while the overall gain is allocated to prevent downstream stages from compressing before the improved LNA $IP_{1\mathrm{dB}}$ is reached.

A key distinguishing feature of the proposed LNA is its fully differential architecture, which is uncommon in state-of-the-art mm-wave designs. Differential operation provides several advantages that are particularly beneficial at 60 GHz, including im-

proved immunity to substrate and supply noise, suppression of even-order distortion products, and enhanced isolation between input and output nodes. Despite adopting a differential topology, the proposed LNA maintains power efficiency comparable to a single-ended design by means of the use of the *PE-SNIM* technique. By exploiting transformer-based impedance transformation at the input, *PE-SNIM* enables optimal noise and input matching without requiring an increase in bias current. As a result, the LNA achieves high robustness and linearity without violating the strict power constraints typical of mm-wave receivers. The two-ways power-combining is realized through a transformer-based passive coupler that splits the amplified signal into main and auxiliary paths while providing the required phase relationship for effective current combining. The coupler is implemented as a compact multi-port transformer, co-designed with the interstage matching network to minimize loss and parasitic effects at 60 GHz. This passive structure simultaneously performs signal splitting, phase shifting, bias routing, and impedance transformation, eliminating the need for lossy coupling capacitors or active phase control circuitry. At the output, a transformer-based combining network performs differential-to-single-ended conversion, output matching, and current combining in a fully passive manner. All linearity enhancements are achieved without additional bias control loops, digital assistance, or adaptive tuning, ensuring robustness against PVT variations and simplifying integration. By combining a fully differential topology, *PE-SNIM* power optimization, passive transformer-based signal splitting, and load modulation, the proposed LNA achieves a level of large-signal linearity not previously reported at 60 GHz. The architecture demonstrates how power combining and load transformation principles can be successfully applied to mm-wave LNAs, overcoming the traditional trade-off between linearity, *NF*, and power consumption.

6.2.1 Highly Linear 60-GHz LNA Circuit Design

The proposed highly linear 60-GHz LNA has been designed in B11HFC 130-nm SiGe BiCMOS technology by Infineon Technologies featuring high-speed heterojunction bipolar transistors and a BEOL stack composed of 6 metal layers, including thick top metals for the realization of mm-wave passive components. In particular, the thickest top metal layer exhibits a thickness of approximately 2.9 µm, enabling the implementation of low-loss integrated transformers and transmission-line-based networks. This technology allows the realization of compact, high-quality passive structures, which are essential for efficient signal processing at 60 GHz. The circuit operates from a 2.5-V supply voltage and exploits the favorable transconductance efficiency of bipolar devices to achieve high linearity under large-signal excitation.

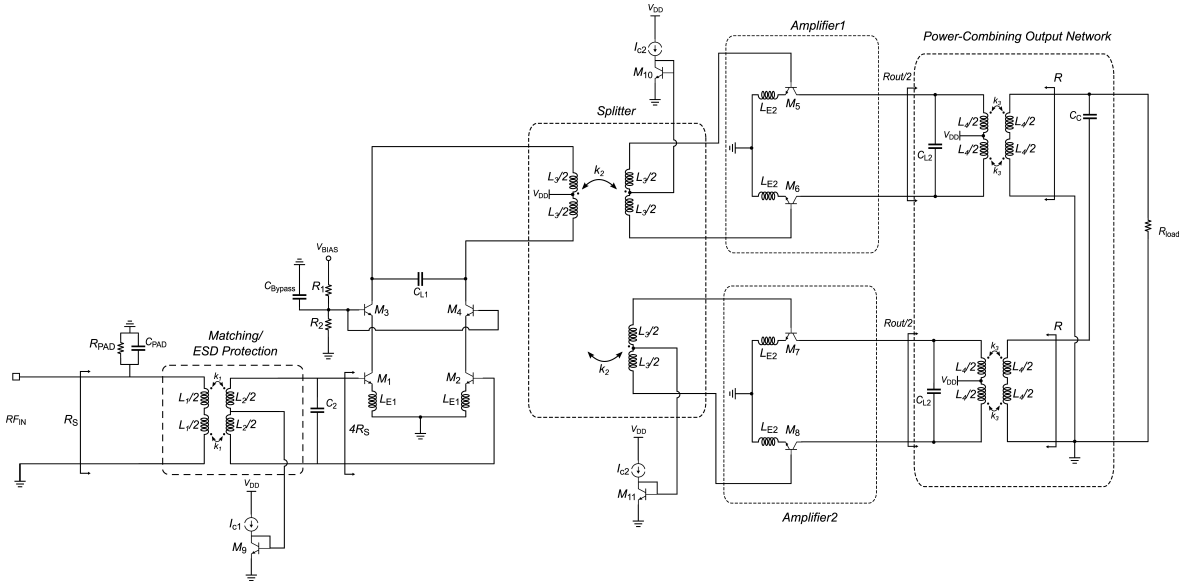


Figure 6.10: Proposed 60-GHz power-combining LNA schematic.

Figure 6.10 shows the schematic of the proposed 60-GHz power-combining LNA. The circuit adopts a fully differential structure and consists of an input balun stage, a splitter network, two amplification paths (Amplifier1 and Amplifier2), and a transformer-based output combining network. All matching, signal splitting, biasing, and phase-shifting functions are realized using integrated transformer structures in order to minimize the use of lossy capacitors and resistors at mm-wave frequencies.

The input stage is implemented as a pseudo-differential cascode LNA with resonant LC load. This topology provides high gain and good reverse isolation while ensuring stable operation at 60 GHz. The cascode configuration reduces the Miller effect associated with the base–collector capacitance, C_{bc}, and improves the voltage handling capability of the input devices. The input matching network is integrated within a stacked transformer that simultaneously performs single-ended to differential conversion, impedance matching, and ESD protection. Moreover, the transformer is designed according to the *PE-SNIM* technique as discussed in Subsection (3.2.2) by properly selecting the turn ratio, n, and coupling factor, k, allowing the input transistor pair to operate close to its optimum noise impedance without sacrificing power efficiency. All the transistors of the first amplification stage (M_1–M_4) are implemented using the hs1npn device, which is a high-speed heterojunction bipolar transistor available in the adopted SiGe BiCMOS technology. These devices are configured with a CBEBEBC geometry, corresponding to three base, two emitter, and two collector contacts. This multi-base, multi-emitter layout configuration is selected in order to reduce the effective base resistance of the input transistors. Since the base resistance directly contributes to the thermal noise of bipolar devices, its reduction leads to a lower equivalent input

noise and therefore to an improvement of the overall *NF*.

The differential signal at the output of the first stage is delivered to a three-port transformer acting as a passive splitter. This network divides the *RF* signal into two differential paths with controlled amplitude and phase relationships and distributes the DC bias to the subsequent stages through its center taps. By co-designing the splitter transformer with the resonant load of the input stage, the interstage matching function is inherently embedded in the passive structure. This approach reduces insertion loss and layout complexity and improves reproducibility at mm-wave frequencies.

The two amplification paths are implemented using pseudo-differential common-emitter, CE, stages with resonant LC loads. Both paths employ identical circuit topologies and transistor dimensions in order to ensure symmetrical operation and to facilitate current combining at the output network. In contrast to first stage, the transistors employed in the second amplification stage adopt a simpler BEC configuration, with a single base, emitter, and collector contact. This geometry is preferred for the output stage because it provides a more compact device layout and reduces the parasitic capacitances associated with multi-base structures. Consequently, this configuration facilitates output impedance matching and improves the robustness of the load network at 60 GHz, where parasitic effects play a dominant role. The two stages are biased using independent DC bias networks, allowing their operating points to be accurately set while sharing the same *RF* signal delivered by the splitter transformer. Each path is loaded by an LC tank tuned at 60 GHz, which provides frequency selectivity and maximizes the voltage gain at the operating frequency. The use of resonant loads also enables control of the voltage swing at the collectors while preserving sufficient headroom for large-signal operation.

The *RF* outputs of the two amplification paths are directly connected to the transformer-based output combining network. This network is realized by means of two identical stacked transformers and performs differential-to-single-ended conversion, output impedance matching, and current combining. The combining network is connected to the *RF* output pad and is co-designed with the load impedance required by the amplification stages in order to minimize insertion loss and preserve linear operation at high signal levels.

Figure 6.11 reports the simulated frequency response of the proposed LNA and separately shows the gain contribution of the first stage, and the main/aux amplification paths. The total gain exhibits a band-pass behavior with a peak of 12.5 dB around 60 GHz, confirming that all resonant networks are correctly tuned at the target operating frequency. The gain of the first stage with the value of about 10 dB provides the initial amplification required to reduce the noise contribution of the subsequent stages and

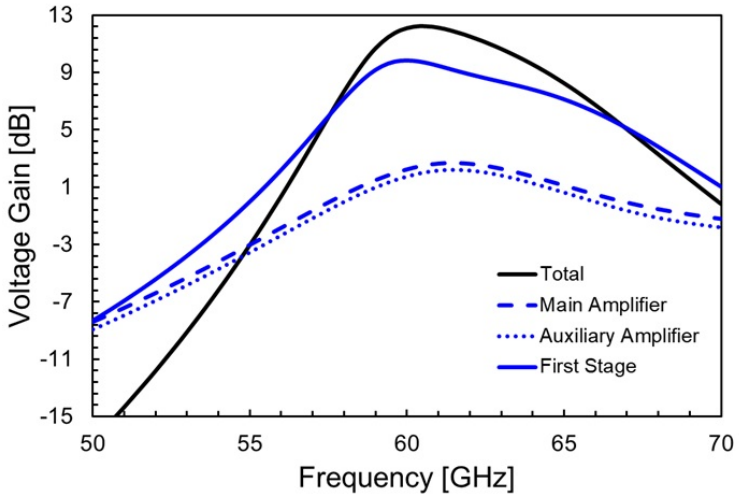


Figure 6.11: Simulated voltage gain of power-combining LNA versus frequency.

maximizing the IP_{1dB} of the whole LNA. The main and auxiliary paths exhibit similar frequency responses, indicating that both amplification branches are properly matched and resonated at the desired frequency. Their individual gains are lower than the total gain, since the overall response results from the combination of the two paths through the transformer-based output network. It can be observed that the total gain is higher than the gain of each individual path over the entire frequency range, demonstrating the effective current combining performed by the output network. Moreover, the 5.8 GHz BW_{3dB} (from 58.4 GHz to 64.2 GHz) of the overall LNA is mainly determined by the resonant behavior of the first stage and of the LC loads of the two amplification paths. The good alignment of the resonance frequencies of the three contributions confirms the consistency of the passive network design and the proper interstage matching between the input stage and the two-path amplification block.

6.2.2 Passive Components Design

The performance of the proposed power-combining 60-GHz LNA is strongly influenced by the characteristics of the integrated passive components, which play a critical role in impedance matching, signal splitting and combining, bias distribution, and frequency selectivity. At mm-wave frequencies, passive losses and parasitic effects become dominant, making the careful design of transformers and capacitors essential to achieve the desired trade-off among gain, bandwidth, *NF*, and linearity. All passive components have been implemented using integrated transformers and MIM capacitors available in the adopted SiGe BiCMOS technology. The use of transformer-based networks is preferred over lumped inductors and series coupling capacitors, as transformers allow multiple functions to be combined within a single passive structure, including

impedance transformation, differential signal generation, DC biasing through center taps, and absorption of parasitic capacitances.

Input Transformer , T_{IN}, Design

The input transformer, T_{IN}, is implemented as a stacked integrated transformer and serves as the *RF* interface between the single-ended 50-Ω input and the pseudo-differential input stage of the LNA, as shown in Figure 6.12 . The transformer is realized using the thick top metal layers of the BEOL stack in order to minimize series resistance and ohmic losses at mm-wave frequencies. In particular, the primary and secondary windings are implemented using the top aluminum metal layer (AlPad) and metal6 (M6), respectively, while the underlying metal layers are employed for routing and vertical interconnections. This choice allows maximizing the Q-factor of the transformer while preserving compactness and layout symmetry. The detailed geometrical dimensions and electrical characteristics are reported in Table 6.1. Additionally, the EM-simulated inductance and Q-factor responses of both primary and secondary coils of T_{IN} are shown in Figure 6.13. At the target operating frequency of 60 GHz, the primary coil exhibits an inductance of approximately L_P=52 pH with a quality factor, Q_P ≈17, while the secondary coil shows an inductance of L_S=163 pH and a quality factor Q_S≈19. The transformer is designed with a turn ratio of 1:2 and achieves a magnetic coupling factor of approximately k= 0.6. The *SRF* of the structure is around 130 GHz, which is well above the operating band and ensures stable operation without resonance-induced degradation of gain or noise performance.

From a noise perspective, the loss introduced by the input transformer represents a critical contribution to the overall *NF* of the receiver. Initial standalone EM simulations indicate an insertion loss of approximately 2.4 dB at 60 GHz. Through geometrical optimization of the metal widths, spacing, and inner diameter, the insertion loss of the standalone transformer is reduced to about 1.4 dB, significantly improving the noise performance of the front-end. When the transformer is connected to the GSG pads and the secondary shunt capacitance required for resonance tuning is included, the overall insertion loss increases to approximately 1.9 dB due to pad parasitics and additional metal interconnect losses. Despite this degradation, the adopted transformer design represents an effective compromise between noise performance, impedance transformation, ESD robustness, and layout compactness. Simulations indicate that, neglecting the input transformer loss, the intrinsic *NF* of the LNA core is approximately 5 dB, highlighting the dominant impact of the input passive network on the overall receiver sensitivity. Consequently, particular attention has been devoted to minimizing the loss of T_{IN}, as it directly determines the achievable *NF* of the complete LNA.

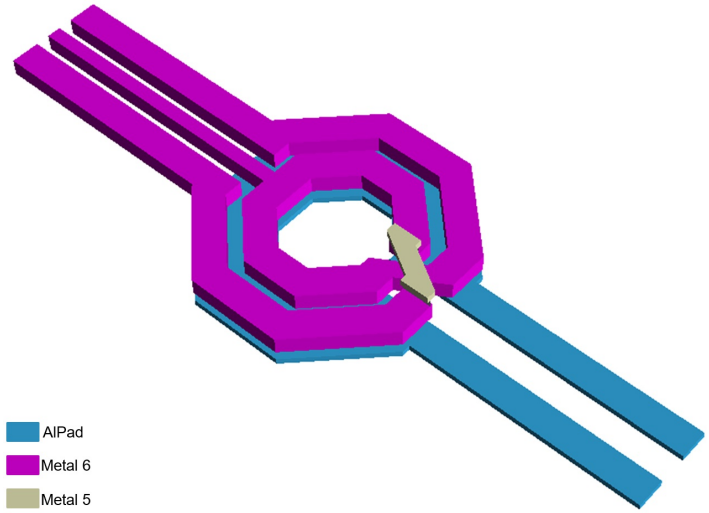
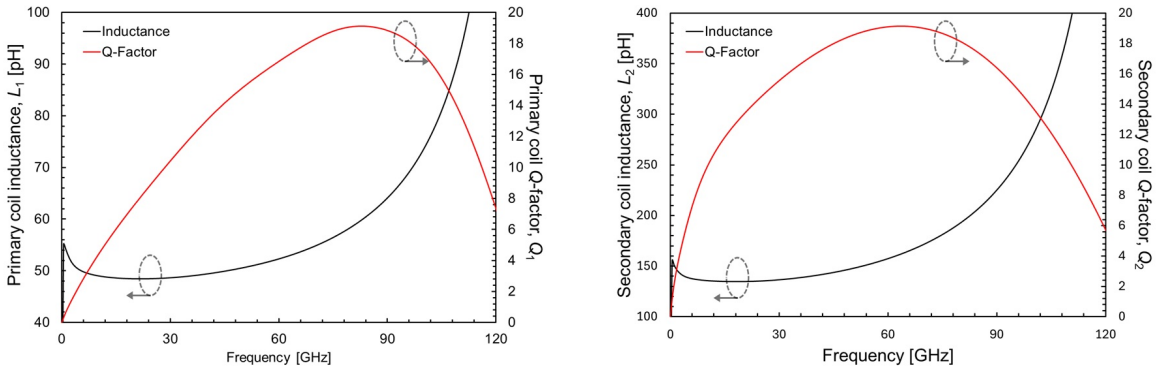


Figure 6.12: 3D T_{IN}/ T_{Combiner} up-side down view.



(a) (b)

Figure 6.13: Primary (a) / secondary (b) coil inductance and Q-factor of T_{IN}.

Table 6.1: Geometrical and electrical parameters of integrated transformers.

Parameters	$T_{\mathbf{IN}}$	$T_{\mathbf{Splitter}}$	$T_{\mathbf{Combiner}}$	**Unit**
Transformer topology	Stacked	Stacked	Stacked	–
Primary/secondary inner diameter (d_{IN})	22.3	14, 45	18.3	μm
Primary/secondary metal width (w)	16.4/7	17/7	5/12.4	μm
Spacing (s)	2.4	3	2.4	μm
Number of turns (n)	1:2	1:1	2:1	–
Primary coil inductance @ 60 GHz	52	63	131	pH
Secondary coil inductance @ 60 GHz	163	85/90	55	pH
Primary coil Q-factor @ 60 GHz	17	18	18	–
Secondary coil Q-factor @ 60 GHz	19	16/18	15	–
Magnetic coupling factor (k) @ 60 GHz	0.6	0.5	0.4	–
Self-resonance frequency (SRF)	130	130	170	GHz

Splitter Transformer, T_{Splitter}, Design

As illustrated in Figure 6.14, the splitter transformer, denoted as T_{Splitter}, is implemented as a three-port stacked transformer and is responsible for dividing the differential *RF* signal at the output of the first LNA stage into two balanced signals that drive the main and auxiliary amplification paths. The transformer is realized using the top three metal layers of the BEOL stack in order to maximize the magnetic coupling factor while minimizing series resistance and ohmic losses at mm-wave frequencies. This stacked implementation ensures high symmetry between the two output paths, which is essential for balanced operation and accurate current combining in the subsequent stages. As presented in Table 6.1, the transformer is designed with a unity turns ratio ($n = 1{:}1$) to preserve voltage gain while enabling efficient power splitting. At 60 GHz, the primary coil exhibits an inductance of approximately $L_{\text{p}} = 63$ pH with a quality factor $Q_{\text{p}} \approx 18$, while the secondary coils present inductance values of $L_{\text{s}} = 85$ pH and 90 pH with quality factors of approximately 16 and 18, respectively. The magnetic coupling factor is around $k = 0.5$, representing a suitable compromise between compact layout and efficient signal transfer. The *SRF* of the splitter transformer is approximately 130 GHz, ensuring reliable operation well beyond the target band.

In addition to signal splitting, T_{Splitter} provides a 180° phase difference between the two output paths, which is required to preserve the differential symmetry of the LNA architecture and to simplify the current combining mechanism at the output network. The primary winding of the transformer resonates with the load of the first amplification stage, enabling co-designed interstage matching and maximizing power transfer without the need for additional matching elements. The center taps of the secondary windings are exploited to deliver the DC bias to the main and auxiliary amplifiers, thereby eliminating the need for lossy series coupling capacitors or *RF* chokes. This approach significantly reduces insertion loss and parasitic effects, which are particularly critical at 60 GHz. As a result, the splitter transformer simultaneously performs signal splitting, interstage matching, phase inversion, and bias distribution, leading to a compact, layout-friendly, and low-loss implementation suitable for mm-wave operation.

Output Power Combiner Transformer, T_{Combiner}, Design

The output stage of the proposed LNA employs a transformer-based power combining network which constitutes the core of the power-combining-inspired output architecture. The network is implemented using two identical stacked transformers, denoted as T_{Combiner} (shown in Figure 6.12), arranged in parallel at the output node, enabling controlled current summation from the main and auxiliary amplification paths.

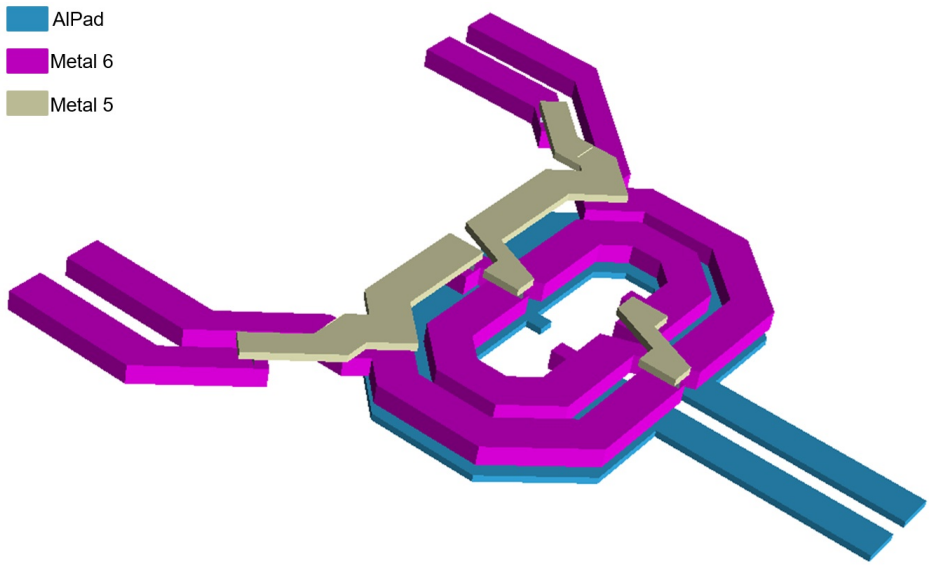


Figure 6.14: 3D T_{Splitter} up-side down view.

Each transformer is realized using the thick top metal layer (AlPad/Metal6) in order to reduce series resistance and enhance current handling capability. A turn ratio of $n = 2{:}1$ is adopted to provide the required impedance transformation between the differential amplifier output and the external 50 Ω load. At the operating frequency of 60 GHz, the primary inductance is approximately $L_{\text{p}} = 131$ pH with a quality factor $Q_{\text{p}} \approx 18$, while the secondary inductance reaches $L_{\text{s}} = 55$ pH with $Q_{\text{s}} \approx 15$, as reported in Table 6.1. The magnetic coupling factor is $k \approx 0.4$, which reflects a deliberate trade-off between compact layout and stable wideband behavior. The SRF of about 170 GHz ensures that the transformer operates well below its resonant limit, avoiding unwanted gain peaking or phase distortion near the band edges. The two transformers are separated by a physical distance of 65 μm to mitigate undesired magnetic interaction and preserve predictable load modulation behavior. This spacing was determined through electromagnetic simulations to balance isolation and layout compactness.

Beyond simple impedance transformation, the combiner network performs multiple essential functions. It converts the differential signal to a single-ended output suitable for GSG pad interfacing, provides output matching to 50 Ω, and enables in-phase current addition from the main and auxiliary branches. In the context of the power-combining operation described in Section 6.2, the output combining network operates with both amplification paths permanently active and statically biased. The interaction between the two paths occurs inherently through the passive transformer network, which defines the effective load seen by each branch. This approach preserves the intended load interaction between the main and auxiliary paths while maintaining

a simple and robust implementation suitable for mm-wave operation. The stacked transformer implementation allows bias routing through center taps while avoiding the insertion of series coupling capacitors, whose parasitic reactance would otherwise degrade performance at mm-wave frequencies. Full-wave electromagnetic simulations were employed to accurately capture metal losses, substrate coupling, and inter-winding parasitics, ensuring reliable prediction of gain, linearity, and efficiency in the post-layout design.

6.2.3 Expected Performance

The expected performance of the proposed highly linear 60-GHz LNA has been evaluated through extensive schematic- and EM-circuit co-simulations, including the extracted models of the input transformer, splitter, and power-combining network. The total current consumption of the proposed LNA is approximately 5.2 mA from a supply voltage of V_{DD}= 2.5 V, resulting in a total power consumption of 13 mW.

The input matching is ensured by the stacked transformer T_{IN}, which provides both single-ended to differential conversion and impedance transformation. As observed in Figure 6.15, the simulated S_{11} remains below -10 dB across the overal BW_{3dB}, confirming adequate matching to a 50-Ω source. At the output, the combiner transformer performs differential-to-single-ended conversion and impedance transformation. The simulated S_{22} remains below -10 dB around 60 GHz, demonstrating proper load matching, as shown in Figure 6.15.

The simulated small-signal gain of the proposed highly linear LNA is shown in

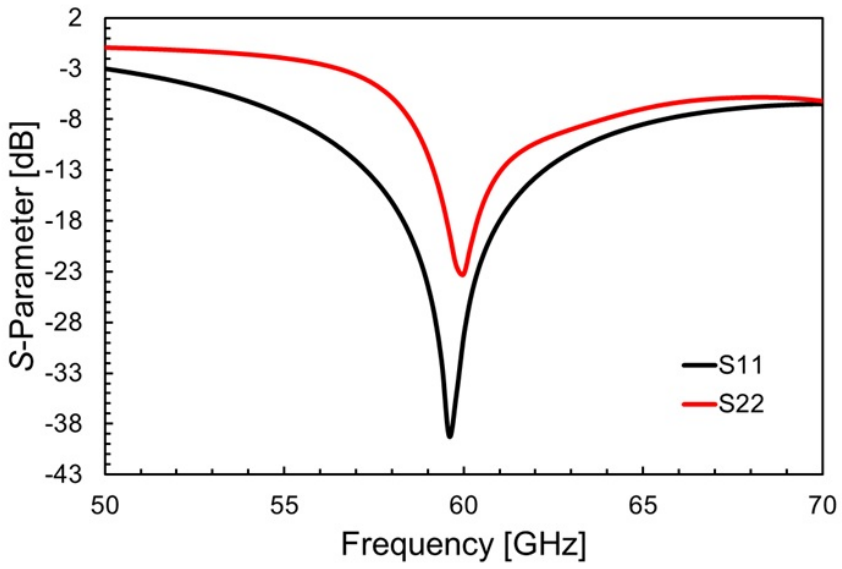


Figure 6.15: Simulated input (S_{11}) and output (S_{22}) matching versus frequency.

Figure 6.16. At the center frequency of 60 GHz, the total gain reaches approximately 12.5 dB. The 3-dB bandwidth extends from 58.4 GHz to 64.2 GHz, corresponding to 5.8 GHz. Additionally, the simulated *NF* of the proposed LNA at 60 GHz is 6.9 dB, depicted in Figure 6.16. As discussed previously, the overall *NF* is predominantly influenced by the insertion loss of the input matching network, while the intrinsic noise contribution of the LNA core remains significantly lower, around 5 dB. Despite the additional passive losses introduced by the transformer-based input interface and pad parasitics, the achieved *NF* remains compatible with short-range 60-GHz wireless applications. It is worth noting that the device sizing and bias conditions were not exclusively optimized for minimum noise performance. Instead, a balanced design strategy was adopted to preserve linearity and enhance $IP_{1\mathrm{dB}}$. As a consequence, the *NF* reflects a controlled compromise between noise efficiency and large-signal robustness. This trade-off is intentional and consistent with the primary objective of the highly linear architecture.

The large-signal behavior of the proposed highly linear LNA has been evaluated through power sweep simulations at 60 GHz. The results are reported in Figure 6.17, where the output gain compression characteristics of the proposed architecture are compared with those of a conventional two-stage LNA. The simulated $IP_{1\mathrm{dB}}$ of the proposed design shows an improvement of about 6.5 dB, from -6.2 dBm to 0.3 dBm with respect to the reference single-path implementation. This substantial enhancement confirms the effectiveness of the dual-path power-combining strategy in extending the linear operating range. As discussed before, the linearity improvement is achieved through passive load interaction within the output transformer network. By distributing the input signal across two branches, the voltage swing experienced by each individual transistor is reduced, mitigating early gain compression. Furthermore, the combiner transformer enables in-phase current summation, allowing higher output power delivery before saturation occurs. As a result, the proposed architecture successfully increases the allowable input signal level while preserving stable gain characteristics, thereby demonstrating a significant enhancement in $IP_{1\mathrm{dB}}$ without introducing additional biasing complexity.

The overall simulation results confirm that the proposed highly linear 60-GHz LNA successfully fulfills its primary design objective, namely the enhancement of large-signal robustness without sacrificing mm-wave performance. The adopted power-combining architecture, combined with passive current combining and gain expansion, enables an improvement of up to 6.5 dB in $IP_{1\mathrm{dB}}$ compared to a conventional two-stage implementation. This linearity enhancement is achieved without dynamic bias control, thereby preserving architectural simplicity and robustness against PVT variations. At the same

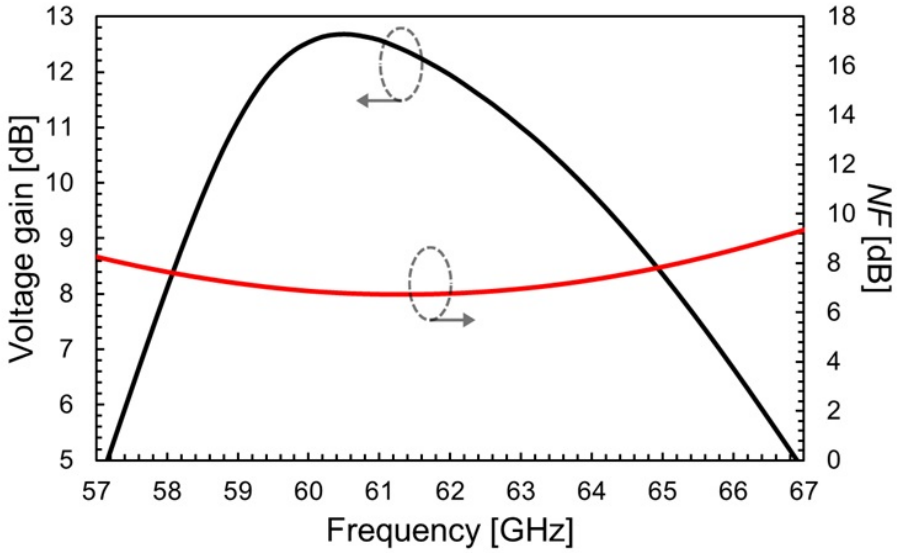


Figure 6.16: Simulated voltage gain and *NF* versus frequency.

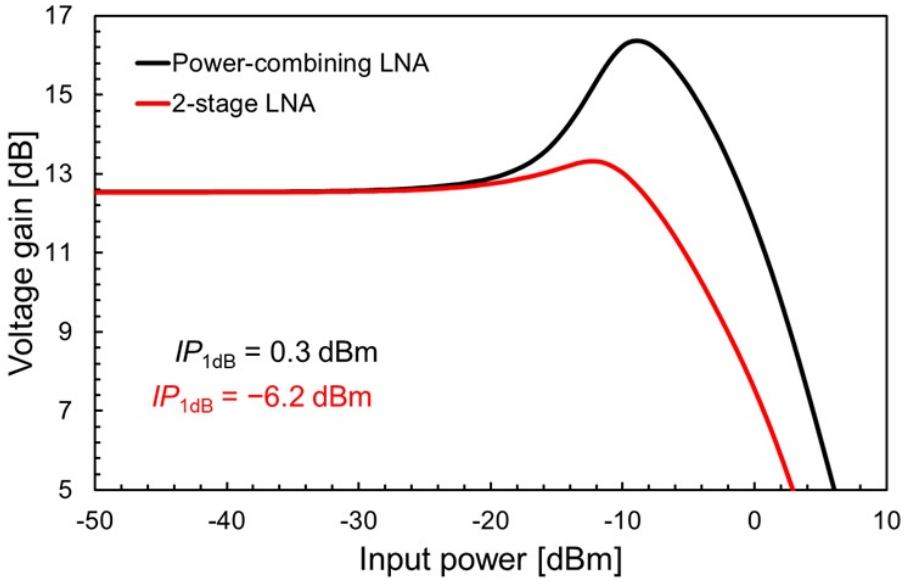


Figure 6.17: Simulated IP_{1dB} of the proposed power-combining LNA and the conventional 2-stage LNA.

time, the LNA maintains competitive gain, acceptable *NF*, and low power consumption, demonstrating a carefully balanced design strategy. The resulting trade-off among gain, *NF*, power efficiency, and linearity makes the proposed solution particularly suitable for blocker-tolerant 60-GHz receiver front-ends, where strong interferers can severely limit the dynamic range. Therefore, the presented architecture represents an effective approach for next-generation short-range mm-wave communication systems requiring enhanced resilience to large input signals.

6.2.4 Layout Description and Post-Layout Simulation Results

Layout Description

The layout of the proposed highly linear 60-GHz power-combining LNA is shown in Figure 6.18. The chip occupies an active area of 930×930 μm^2 (0.86 mm^2), including *RF* pads, DC pads, and bias routing networks. The floorplan follows a vertically symmetric architecture to ensure balanced signal propagation and minimize phase mismatch between the main and auxiliary amplification paths.

The *RF* signal enters the chip through the bottom GSG pads and is first processed by the input transformer T_{IN}, which performs single-ended to differential conversion and impedance transformation. The signal is then routed upward toward the splitter transformer, which divides the differential signal into the main and auxiliary branches. These two paths are laid out symmetrically on the left and right halves of the chip to preserve amplitude and phase balance. At the top of the layout, the combiner network collects the currents from both branches and performs differential-to-single-ended conversion before feeding the output GSG pads.

A total of 12 DC pads are implemented to independently bias the different circuit blocks. Specifically, dedicated pads are provided for the cascode bias of the input stage (VBIAS), supply voltages for the first and second stages (VDD1 and VDD2), and separate bias currents for the input pair (IB1), main amplifier (IB2), and auxiliary amplifier (IB3). Four GND pads are distributed along the chip periphery to provide low-impedance return paths and reduce ground inductance. A common VDD and VSS rail structure is used to ensure stable power distribution across the layout.

To minimize substrate noise coupling and enhance isolation at mm-wave frequencies, a dense ground plane implemented using Metal6 (M6) and Metal5 (M5) grid structures surrounds the active circuitry. The *RF* transformers are placed centrally along the vertical axis to reduce routing length and parasitic asymmetry, while DC routing is mainly realized using Metal5 (M5) and Metal4 (M4) layers to avoid interference with the top thick metal layers used for high-Q inductive components.

The placement of T_{IN}, splitter, and combiner in a vertical cascade minimizes inter-stage routing length and reduces parasitic series inductance. Furthermore, the symmetric layout of the main and auxiliary branches ensures consistent electrical behavior and predictable current combining at the output stage. The physical separation between *RF* structures and DC bias pads further improves isolation and mitigates unwanted coupling.

Overall, the layout has been carefully optimized to balance symmetry, isolation, routing compactness, and passive component quality, ensuring that the EM-simulated

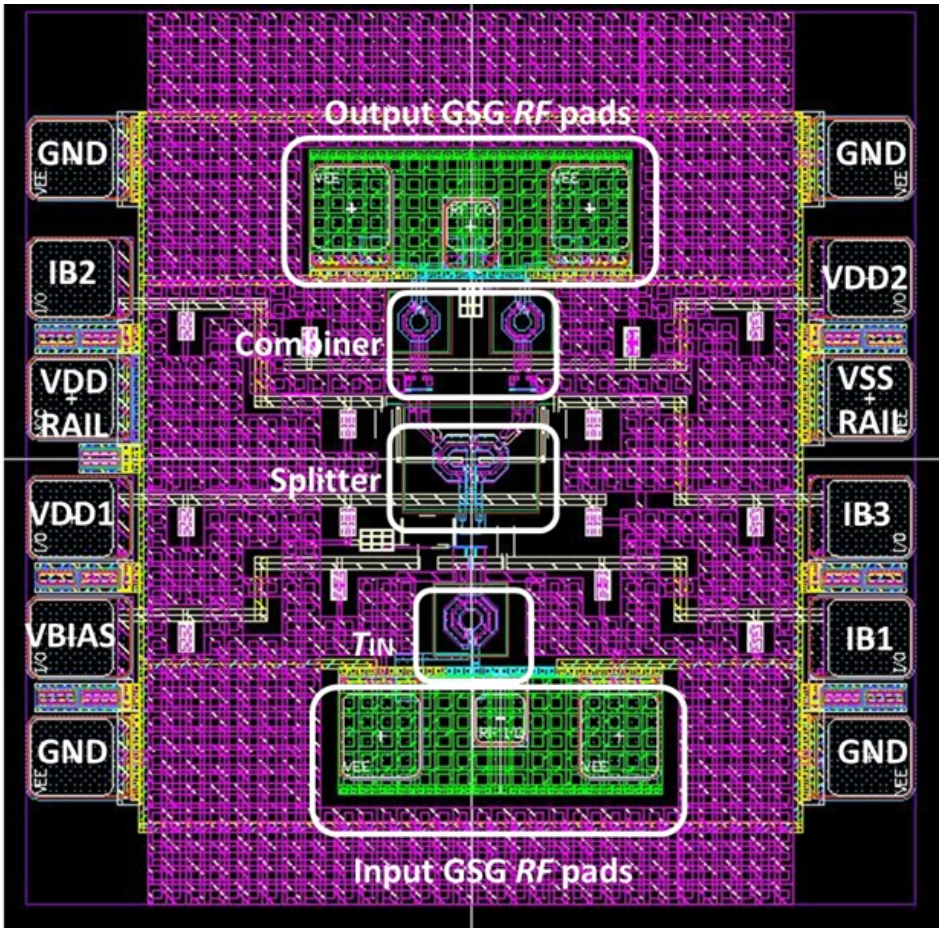


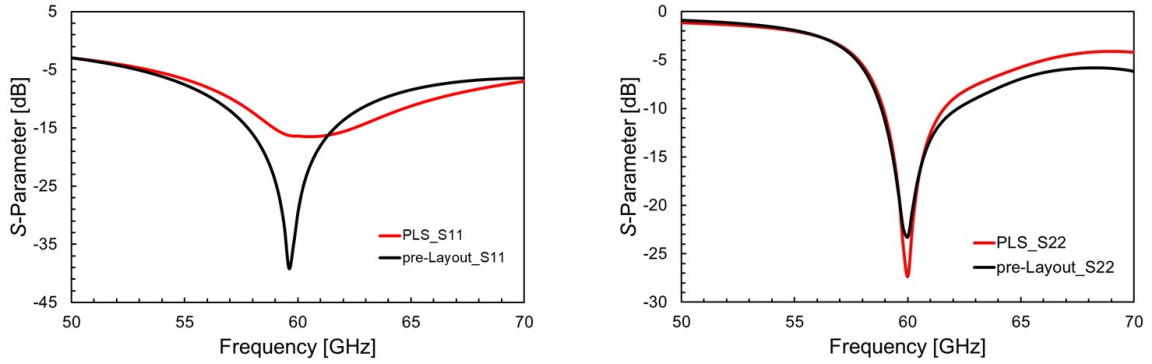
Figure 6.18: Layout of the proposed 2-path power-combining LNA.

performance closely matches the schematic-level expectations.

Post-Layout Simulation Results

The performance of the proposed power-combining LNA has been validated through full post-layout simulations including parasitic extraction of interconnects, pad structures, and passive components. EM-models of the transformers were co-simulated with the extracted layout in order to accurately capture metal losses, substrate coupling, and routing parasitics.

The simulated post-layout reflection coefficients are shown in Figure 6.19. The input reflection coefficient S_{11} remains below -10 dB around the operating frequency, confirming adequate input matching after layout implementation. The output matching S_{22} exhibits a minimum close to 60 GHz, reaching a return loss better than -25 dB at resonance. A slight degradation with respect to schematic-level simulations can be observed, mainly due to additional routing capacitances and series metal resistance introduced by the interconnect network and pad parasitics.



(a) (b)

Figure 6.19: Post/pre-layout input (S_{11}) (a) / output (S_{22}) matching (b) versus frequency.

The post-layout voltage gain, depicted in Figure 6.20, reaches 12.7 dB around 60 GHz, with the resonance frequency preserved close to the design target. The 3-dB bandwidth of approximately 5 GHz (58.4 GHz-63.4 GHz) remains centered around the operating frequency, indicating that the transformer-based matching network maintains its intended resonance behavior even after parasitic extraction. The simulated post-layout *NF* is about 6.9 dB across the operating band, which is consistent with the pre-layout results. This confirms that the layout implementation, including interconnect routing and pad integration, does not introduce significant additional noise degradation. The preservation of *NF* demonstrates that the transformer quality factor and passive insertion losses remain well controlled after EM extraction, validating the adopted layout strategy for mm-wave operation.

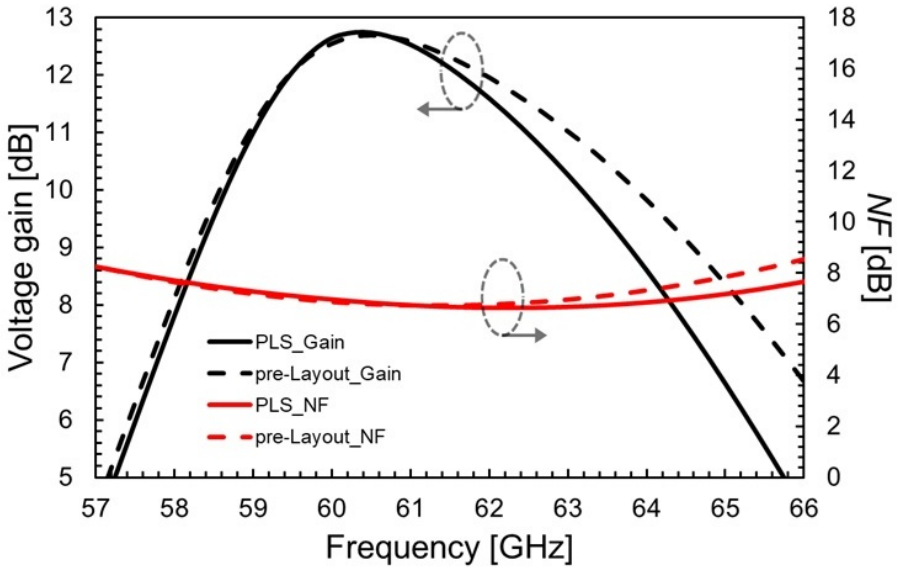


Figure 6.20: Post/pre-layout voltage gain and *NF* versus frequency.

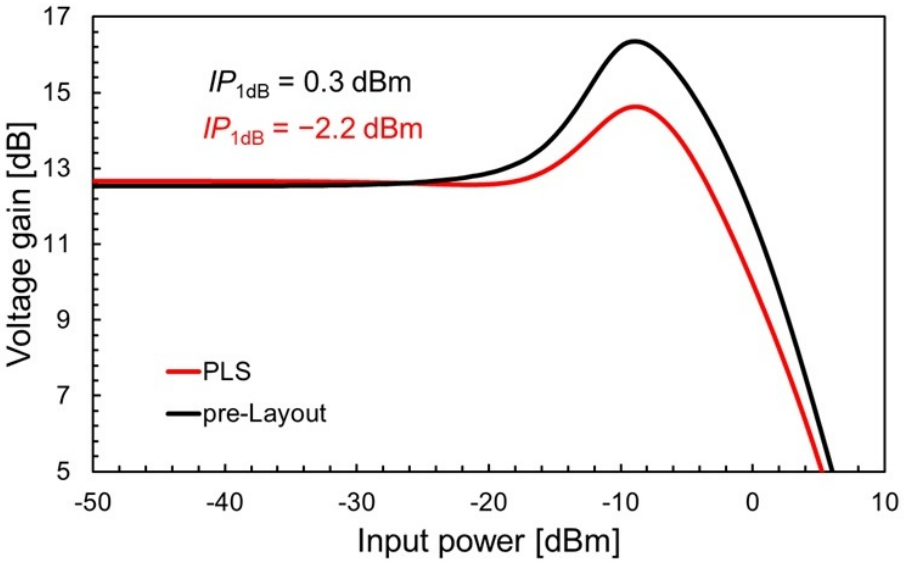


Figure 6.21: Post/pre-layout $IP_{1\text{dB}}$ of the proposed LNA.

The large-signal behavior after layout extraction is shown in Figure 6.21. The simulated post-layout input 1-dB compression point is $IP_{1\text{dB}} = -2.2$ dBm. Compared to pre-layout simulations, this corresponds to a reduction of about 2 dB. This degradation can be explained by layout-induced parasitic effects. The additional series resistance of metal interconnects reduces the effective voltage headroom available to the active devices, while the slightly reduced Q-factor of the transformers after EM extraction decreases the efficiency of current combining at high input power levels. Moreover, parasitic capacitances associated with routing and pad structures modify the effective load impedance seen by the main and auxiliary branches, leading to a less ideal load interaction than predicted at schematic level.

Despite these parasitic effects, the overall DC consumption remains very low. The total current drawn by the LNA is 5.6 mA from a 2.5 V supply voltage, resulting in a total power consumption of only 14 mW. This confirms that the proposed power-combining architecture achieves a significant linearity enhancement without incurring a substantial power penalty. The moderate current consumption demonstrates that the improvement in $IP_{1\text{dB}}$ is achieved primarily through architectural load interaction and current combining, rather than through aggressive bias scaling.

Overall, the post-layout results confirm that the proposed LNA maintains its targeted gain, bandwidth, and matching performance while preserving a strong linearity improvement and low power operation. The close agreement between schematic and extracted simulations validates the robustness of the design methodology and the effectiveness of the layout strategy at 60 GHz.

Corners and Monte Carlo (MC) analysis

A comprehensive corner analysis has been carried out on the PLS extracted design in order to evaluate the robustness of the proposed LNA against process variations. The analysis considers the typical–typical (TT), slow–slow (SS), and fast–fast (FF) process corners, which represent the main variability scenarios affecting both active devices and passive components.

The simulated post-layout input matching performance is reported in Figure 6.22, where the reflection coefficient S_{11} is shown versus frequency for all process corners. The results indicate that proper input matching is preserved across all conditions, with a minimum around the 60-GHz band. However, a noticeable frequency shift can be observed, particularly in the FF corner, where the resonance is shifted toward higher frequencies, while in the SS case it moves slightly toward lower frequencies. This behavior is mainly attributed to process-induced variations in both the effective capacitance and inductance of the input matching network, as well as changes in the transconductance of the input devices.

The post-layout output matching performance, shown in Figure 6.23, exhibits a similar trend. In the TT corner, a deep minimum of S_{22} is achieved close to 60 GHz, confirming optimal output impedance matching. In contrast, both SS and FF corners show a degradation and frequency shift of the matching condition. This effect is mainly

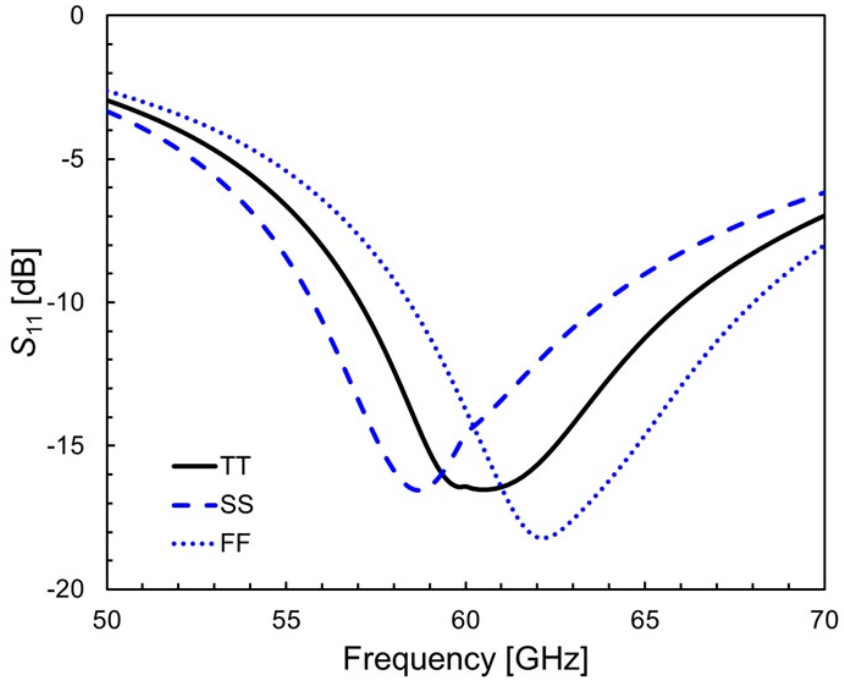


Figure 6.22: Post-layout input matching (S_{11}) versus frequency for different process corners.

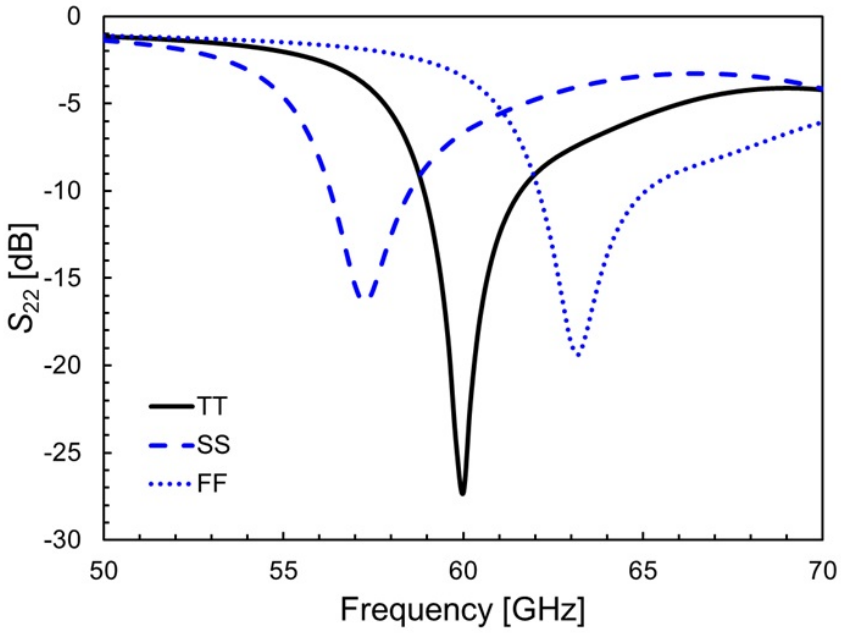


Figure 6.23: Post-layout output matching (S_{22}) versus frequency for different process corners.

related to variations in the resonant load network and transformer parameters, which are particularly sensitive to process fluctuations at mm-wave frequencies.

The impact of process variations on the post-layout small-signal gain is illustrated in Figure 6.24. The nominal TT condition provides a peak voltage gain around 60 GHz, while the SS and FF corners introduce both gain degradation and frequency shifts. In particular, the SS corner exhibits a lower gain and a shift toward lower frequencies due to reduced carrier mobility and increased effective capacitances. Conversely, the FF corner shows a shift toward higher frequencies with slightly higher peak gain, consistent with faster device operation and reduced parasitic effects.

The post-layout noise performance across process corners is presented in Figure 6.25. The *NF* remains within an acceptable range over the frequency band of interest, demonstrating the robustness of the proposed design. The minimum *NF* is achieved close to the resonance frequency for each corner, with variations mainly caused by changes in device noise parameters and matching conditions. Despite these variations, the overall *NF* degradation remains limited, confirming that the adopted design techniques effectively mitigate the impact of process fluctuations.

Finally, the post-layout large-signal behavior of the LNA is evaluated in Figure 6.26, which reports the power gain as a function of the input power for different process corners. The results show a noticeable variation in the IP_{1dB}, ranging from ap-

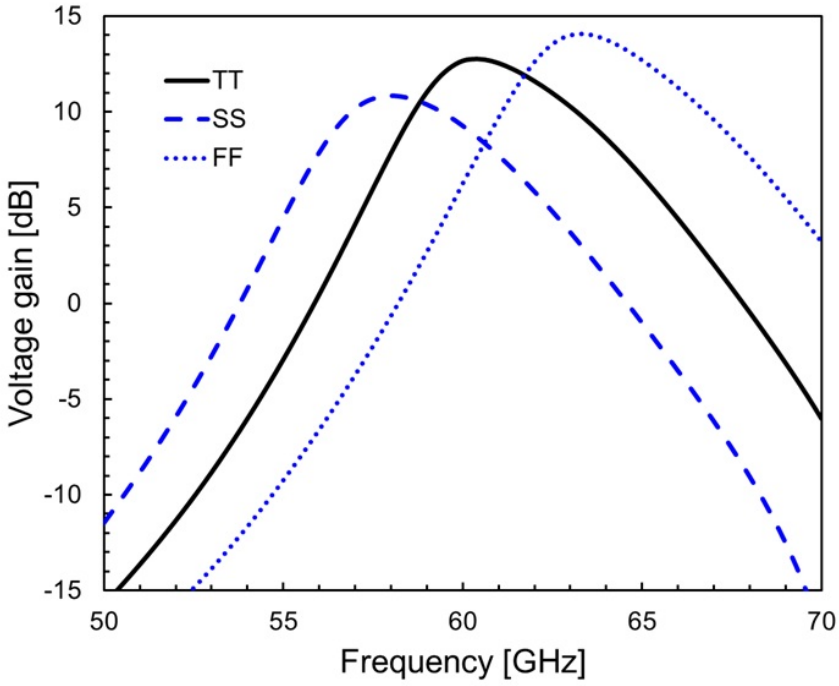


Figure 6.24: Post-layout voltage gain versus frequency for different process corners.

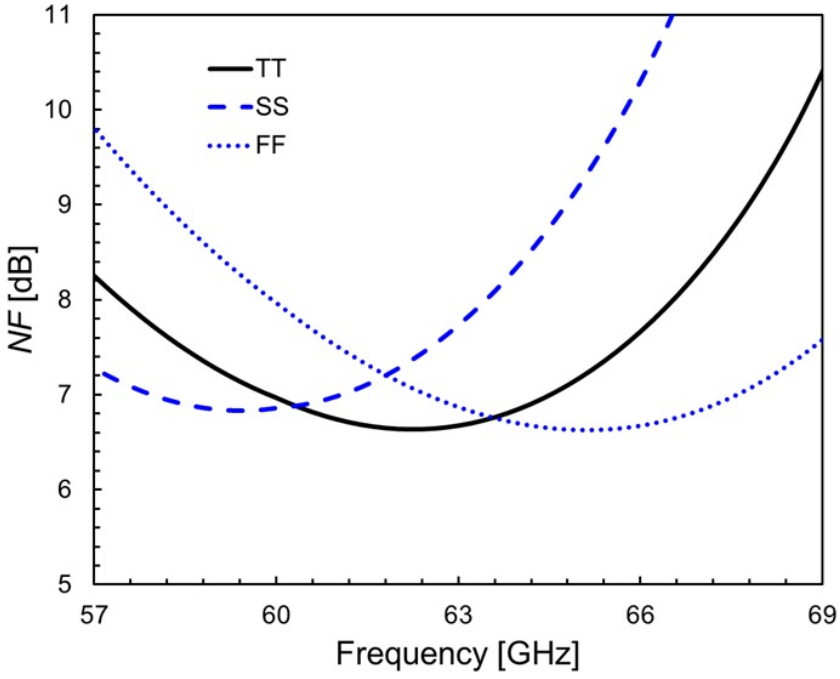


Figure 6.25: Post-layout *NF* versus frequency for different process corners.

proximately −2.2 dBm in the TT corner up to 3.4 dBm in the FF corner. At first glance, this variation may suggest a strong dependence of linearity on device characteristics, such as transconductance and bias conditions, with the FF corner benefiting

from higher current drive capability. However, it is important to note that the comparison is carried out at a fixed frequency of 60 GHz. Due to the corner-dependent shift of the gain peak, the LNA does not operate at its optimal condition in all cases. Consequently, part of the observed variation in IP_{1dB} is attributed to gain degradation at 60 GHz rather than purely reflecting intrinsic linearity differences. In addition to large-signal performance, the stability of the proposed LNA has been evaluated through the Rollett stability factor (K), as shown in Figure 6.27. The results confirm that K remains well above unity across the entire frequency range of interest for all process corners (TT, SS, and FF), indicating unconditional stability of the amplifier. Despite process-induced variations, the minimum value of the stability factor remains significantly higher than 1, ensuring robust operation even under worst-case conditions. The observed variations in k across corners are mainly attributed to changes in device parasitics and bias-dependent transconductance, which slightly affect the input and output matching conditions. Nevertheless, the overall stability margin is sufficiently large, demonstrating that the proposed architecture is inherently stable and resilient to process variations.

To further assess the robustness of the proposed LNA against process variations and device mismatch, MC simulations have been carried out, and the results are summarized in Figure 6.28. The statistical distributions of the main performance metrics, including S_{11}, S_{22}, power gain, NF, BW_{3dB}, gain mismatch between the two paths, and

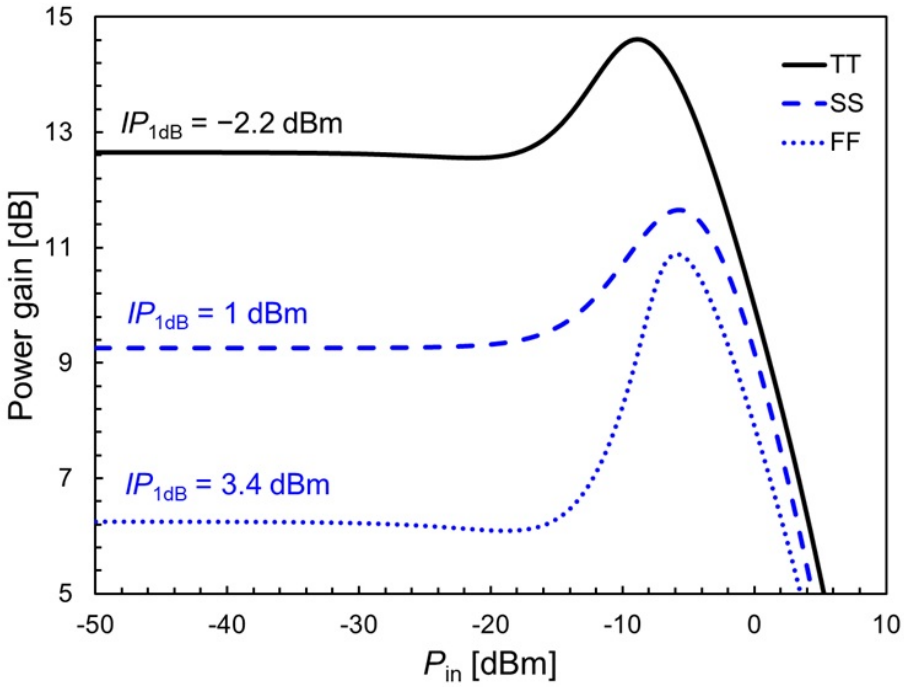


Figure 6.26: Post-layout IP_{1dB} at 60 GHz for different process corners.

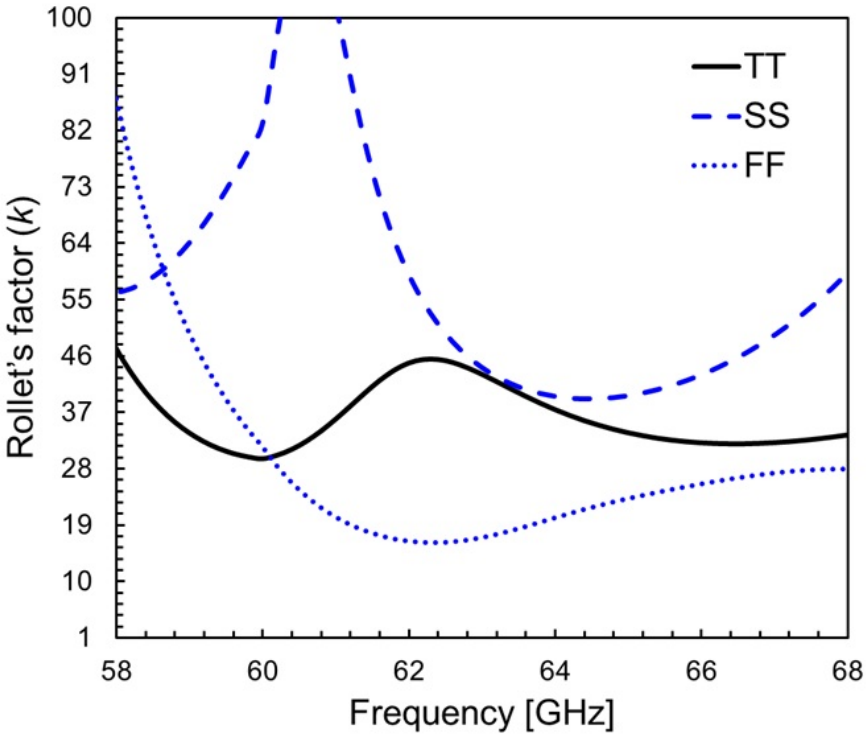


Figure 6.27: Post-layout Rollett's stability factor (K) versus frequency.

IP_{1dB}, demonstrate a stable and well-centered behavior around their nominal values.

In particular, the input and output matching remain well below -10 dB with limited standard deviation, confirming the robustness of the transformer-based matching network under process variations. The power gain exhibits a mean value of approximately 12.5 dB with a relatively small spread, indicating good immunity to mismatch effects. Similarly, the NF shows a narrow distribution around 7 dB, highlighting that noise performance is only weakly affected by device variations. The BW_{3dB} also remains tightly distributed, ensuring consistent frequency response across different samples. The gain imbalance between the two paths is maintained within a small range, validating the effectiveness of the symmetric layout and design strategy. Finally, the IP_{1dB} distribution shows moderate variation, with a mean value around -2.5 dBm, reflecting the sensitivity of large-signal performance to process variations while still preserving acceptable linearity.

Overall, the presented corner and Monte Carlo analyses confirm that the proposed LNA maintains stable operation and robust performance across process and mismatch variations. Although frequency shifts and moderate performance degradations are observed, the circuit preserves proper matching, gain, noise, and linearity characteristics within the target 60-GHz band. These results demonstrate the reliability and suitability of the proposed architecture for practical mm-wave receiver applications.

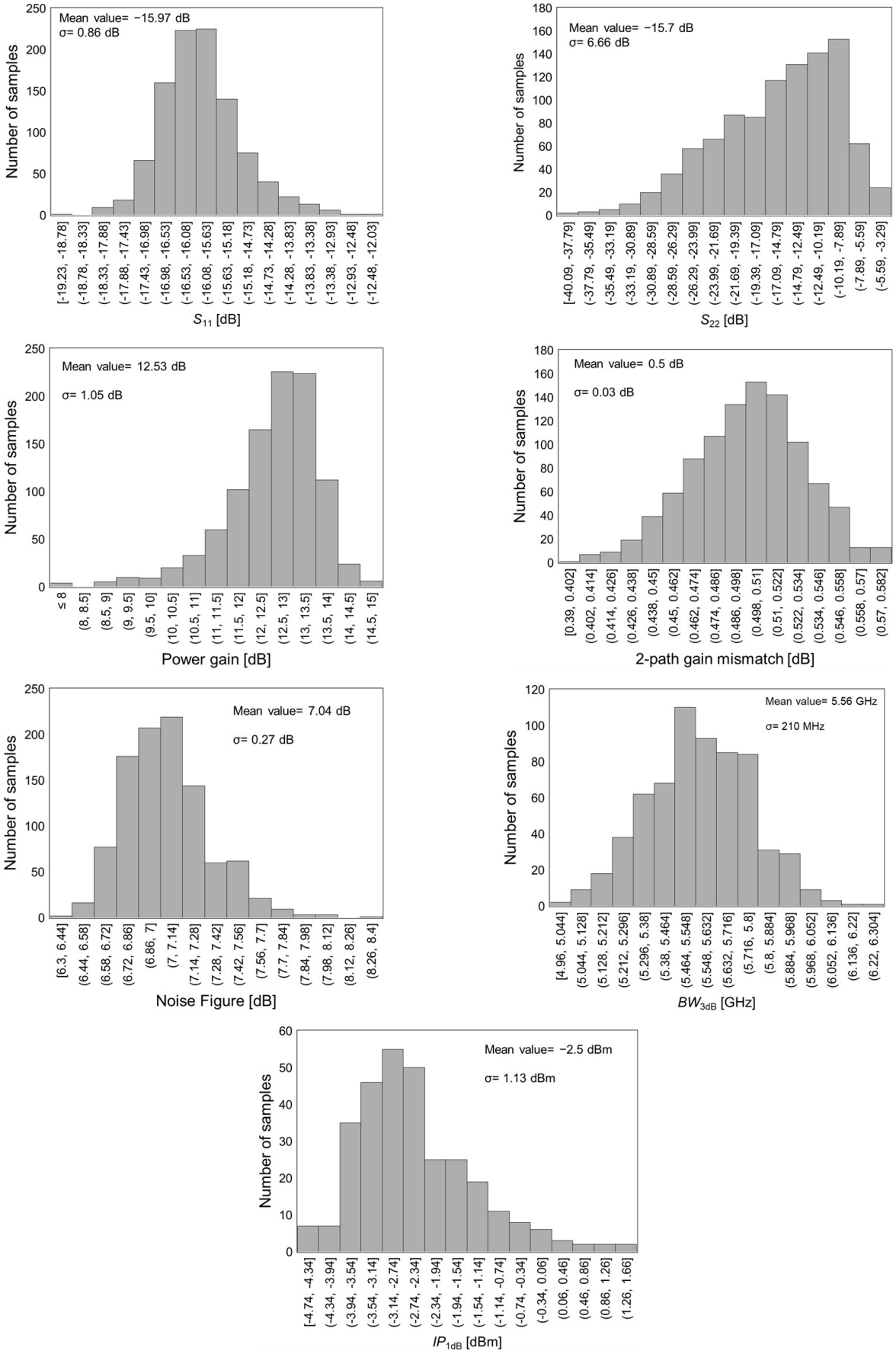


Figure 6.28: MC-simulated results for main LNA performance parameters.

Table 6.2 summarizes the performance of the proposed power-combining LNA and compares it with recently reported state-of-the-art designs. It can be observed that the proposed LNA achieves a competitive performance in terms of gain, *NF*, and bandwidth while operating at 60 GHz. In particular, the post-layout results show a voltage gain of 12.7 dB and a *NF* of 6.9 dB are obtained, which are in line with comparable CMOS and SiGe implementations. A key advantage of the proposed architecture is the significant improvement in linearity, achieving an $IP_{1\text{dB}}$ of approximately -2.2 dBm, which is higher than most reported CMOS LNAs and comparable to or better than several SiGe-based designs. This enhancement is achieved without increasing power consumption, as the proposed LNA operates with a current consumption of only 5.6 mA from a 2.5 V supply, resulting in a total power consumption of 14 mW. Furthermore, the figure-of-merit (FoM) of 8.41 demonstrates the efficiency of the proposed design, highlighting an excellent trade-off among gain, noise, linearity, and power consumption. Overall, the comparison confirms that the proposed power-combining LNA provides a highly competitive solution for blocker-tolerant 60-GHz receiver front-ends.

Table 6.2: LNA performance and comparison with the state of the art.

Parameters	[62] (M)	[78] (M)	[79] (M)	[80] (S)	[81] (S)	[82] (M)	[83] (M)	[84] (M)	[85] (M)	[86] (M)	[57] (M)	[58] (M)	[30] (M)	[21] (M)	[60] (M)	[61] (P)	**This work** (P)	**Unit**
Number of stages	3	4	3	2	2	2	3	3	2	2	2	1	2	6	3	2	**2**	–
Single-ended (S) / Differential (D)	D	S	S	S	S	S	S	S	S	D	D	S	S	S	S	D	**D**	–
Gain	25	12.5	30	20.3	20.19	14.6	24	20.4	18	10	16.1	14.1	10.2	24.5	16.8	22.7	**12.7**	dB
BW_{3dB}	7.5	6	9.5	–	15	–	12	7	4	6	15	6	10	14	16.4	9	**5 (58.4–63.4)**	GHz
Noise figure	4.8	5.4–6.5	4.6–6	6.3	4.8	5.5	5	8.6	6.7	3.8	7.1	4.6	8.6	4.9–6	4.4	4.4	**6.9**	dB
IP_{1dB}	−22 to −7	−16	−30.7 to −26	−22.5	−8	−16.4	−9.6	−20	−18	−4.6	−10	−13.5	−11	−27	−13	−16.1	−2.2	dBm
Operating frequency	60	60	60	60	60	58	60	60	60	60	60	60	60	60	60	60	**60**	GHz
Supply voltage	1.3	1	1	1.2	1.2	1.5	1	1.2	2.7	1.2	1.2	2.5	1	1.2	1.2	–	**2.5**	V
Current consumption	36.5	4.4	8.9	10	7.7	16	38	54.2	7.5	29.2	58.3	9.6	30	14	27.5	–	**5.6**	mA
Power consumption	47	4.4	8.9	12	9.2	24	38	65	20.25	35	70	24	30	16.8	33	29.9	**14**	mW
Technology	65 CMOS	90 CMOS	65 CMOS	130 CMOS	130 SiGe	90 CMOS	65 CMOS	130 CMOS	250 SiGe	65 CMOS	90 CMOS	130 SiGe	65 CMOS	90 CMOS	40 CMOS	40 CMOS	**130 SiGe BiCMOS**	–
FoM [65]	0.1	1.24	0.06	0.17	10.33	0.33	1.92	0.03	0.23	4.25	0.33	0.84	0.26	0.06	0.87	0.64	**8.41**	–

(1) Maximum gain; (2) at high-gain mode; S: Simulation results; M: Measurement results; P: Post-layout results.
FoM = [Gain(linear)×f (GHz)×IP_{1dB} (mW)] / [P_{DC}(mW)×$(F-1)$], where F is the noise factor.

7 Conclusions and Key Contributions

This thesis presents the design and validation of mm-wave low-noise amplifiers for 60-GHz wireless communication systems, with primary emphasis on low-power and wideband operation in advanced CMOS technology. A two-stage 60-GHz LNA has been designed, implemented, and experimentally validated in a 28-nm CMOS process. On-wafer measurements confirmed the correct operation of the fabricated standalone LNA around 60 GHz, validating the proposed design methodology despite a moderate frequency shift with respect to the post-layout simulations.

A key contribution of this work is the development of a power-efficient design methodology based on simultaneous noise and impedance matching (*PE-SNIM*), enabling an optimal trade-off among gain, bandwidth, *NF*, and power consumption. In addition, transformer-based passive structures have been systematically exploited for impedance transformation and resonance tuning, while also providing intrinsic electrostatic discharge (ESD) protection. This approach reduces the need for dedicated ESD devices and minimizes their impact on *RF* performance. The design of high-Q integrated passive components, including transformers and capacitors, further supports efficient operation at mm-wave frequencies in nanoscale CMOS technologies.

The proposed LNA has been specifically optimized to operate as the front-end stage of OOK/ASK receiver architectures. While a simplified demodulator is included in the system for validation purposes, its role is limited to demonstrating that the LNA is capable of effectively driving subsequent stages. Post-layout simulations of the complete receiver predict multi-Gbit/s operation with a sensitivity of -40 dBm while maintaining a total power consumption below 15 mW from a 0.9-V supply, demonstrating the suitability of the proposed front-end architecture for low-power, high-speed wireless communication systems.

In addition to the CMOS implementation, this thesis investigates linearity enhancement through the design of a 60-GHz LNA in 130-nm SiGe BiCMOS technology. A novel two-path power-combining architecture is proposed to improve large-signal performance. Post-layout simulations predict an improvement of up to 4 dB in the input 1-dB compression point ($IP_{1\mathrm{dB}}$) compared to conventional solutions, while maintaining competitive gain and noise performance. Experimental validation of this circuit is planned after chip fabrication.

Overall, this work demonstrates that CMOS and SiGe BiCMOS technologies offer complementary advantages for mm-wave circuit design. The standalone CMOS LNA

has been experimentally validated through on-wafer measurements, whereas the complete receiver and the highly linear SiGe BiCMOS LNA have been validated through post-layout simulations. Schematic-level simulations were employed during the design exploration phase to compare alternative circuit topologies and guide the final architectural choices. The proposed circuit techniques and design methodologies contribute to the development of compact, energy-efficient, and robust front-end solutions for next-generation high-data-rate wireless communication systems.

The outcomes of this research have been disseminated through four conference papers [87–90], four journal publications [37, 91–93], and a patent [69].

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