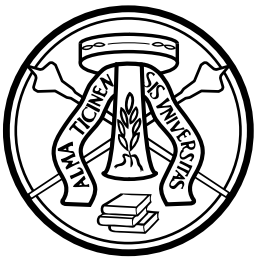

UNIVERSITÀ
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PH.D. SCHOOL IN MICROELECTRONICS
CYCLE XXXV

Current-mode processing based Temperature-to-Digital Converters for MEMS applications

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IMS^2

"Be', noi... lavoriamo nella meccanica di precisione: tecnologie avanzate al servizio di progettazioni particolari e specifiche. Non so... hardware e quelle cose, cioè... creiamo dei supporti che poi serviranno per progettare grosse situazioni, non so mecc... proprio... strumenti di precisione per una svolta magari futura anche della meccanica... Eh? Non so se mi spiego?"

"Sì, insomma... abbiamo un negozio di ferramenta. Cioè, non è che il negozio di ferramenta è nostro...noi ci lavoriamo come commessi, come... galoppini, insomma."

Aldo, Giovanni e Giacomo

Abstract

Current-mode processing based Temperature-to-Digital Converters for MEMS applications

by Antonio Aprile

This thesis presents novel Temperature-to-Digital Converters (TDCs) designed and fabricated in CMOS technology. These integrated smart temperature sensing circuits are widely employed in the Micro-Electro-Mechanical Systems (MEMS) field in order to mitigate the impact of the ambient temperature on their performance. In this framework, the increasingly stringent demands of the market have led the cost-effectiveness specification of these compensation solutions to an higher and higher level, directly translating into the requirement of more and more compact designs (< 0.1 mm^2); in addition to this, considering that the great majority of the systems whose thermal drift needs to be compensated is battery supplied, ultra-low energy-per-conversion (< 10 nJ) is another requirement of primary importance. This thesis provides a detailed description of two different test-chips (*mas fuerte* and *es posible*) that have been designed with this orientation and that are the result of three years of research activity; for both devices, the conception, design, layout and testing phases are all described in detail and are supported by simulation and measurement results.

Acknowledgements

I firmly think that the possibility to work on a whole microelectronic system starting from its conception, to develop it during all its phases (design → layout → testing) and get to hold a piece of silicon on which to conduct some measurements is the reason why the PhD experience is a golden opportunity; since it comes once in a lifetime, in the past three years, I did my best to get the most out of every day as a PhD candidate.
Besides marking the end of my PhD journey, actually, this doctoral thesis concludes an intense educational path of about 21 years; starting from the primary school, I have always been lucky enough to be surrounded by extraordinary people that made me who I am today. Considering that my family and my loved ones will find space later, I would like to focus on teachers and professors; I have always been fascinated by the art of teaching and I have always believed the knowledge transfer to be of huge value. For this reason, along my path, I have had great esteem for many of them, far as to say they changed my life; I would like to mention Cecilia Radic (Cello teacher, 2010-2016), Giorgio Guarnieri (History and Philosophy professor, 2011-2014) and Federico Montecchi (Electronics II professor, 2016-2017). Taking this further, I would like to spend few words for my PhD advisors, prof. Edoardo Bonizzoni and prof. Piero Malcovati. Their teachings went above and beyond technical matters, training my way of thinking, my way of facing problems and my way of achieving goals. In particular, I would like to thank Piero for his steady optimistic attitude, for his straight pointing to targets and for his massive expertise and knowledge. About Edo, instead, I would like to highlight his exceptional teaching talent, his greatness of soul and his constant orientation at quality. I really felt educated at quality in all that I did in these three years.
In this scenario, my family simply was the necessary condition for all this route being possible. I always felt loved and appreciated and the chemistry with my parents and brothers is one of the most precious things I have. I also recognise that several of my character traits, that helped me during my PhD, come from my parents: I owe determination and stakhanovism to my father while speed of thinking and efficiency to my mother. Dinho and Ste, my bros, are simply magnificent and are my best friends; their outstanding unselfishness, the mutual respect and esteem we have and our continuously being on the same page is something really unique.
In all this, there is one person that supported me more than anyone else during these years: Ari. Her constant encouragements gave me the energy needed to overcome the obstacles that I inevitably encountered and her presence reminds me every day the beauty of life; I truly feel honored to share my life with her.
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Thank You

Antonio

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Introduction

On-chip temperature measurements have acquired an increasingly important role over the past two decades. The growing computational power of modern microprocessors has given rise to a higher criticality in their thermal management process [1]; for instance, dynamic voltage and frequency scaling (DVFS), a commonly used approach in this framework [2], requires responsive temperature tracking to allow an effective control on the thermal status of the microprocessor and, furthermore, the cooling fans' speed regulation is also based on a continuous temperature monitoring [3–5]. Another field that has featured a remarkable advance in recent years is the Micro-Electro-Mechanical Systems (MEMS) one [6]; their growing employment has led the research focus to more and more robust devices with respect to the influence of environmental effects. One of the main challenges is, indeed, to mitigate the impact of the ambient temperature on their performance; for this reason, high-precision MEMS devices also require a temperature tracking to compensate for the drift of their parameters [7–11]. Integrated temperature sensors are also used for clinical applications [12–14]; devices that provide a high accuracy monitoring in the human body temperature range are needed for the detection of atypical biomedical conditions. Lastly, since temperature is a fundamental physical parameter of both industry and everyday life, on-chip temperature measurements are also combined with radio-frequency identification (RFID) tags in several applications: monitoring of the food cold chain [15, 16], environmental monitoring [17, 18], supply chain management of healthcare products [19], animal healthcare monitoring [20] and many more.

Among all these cases, this thesis focuses on TDCs designed for the temperature compensation of MEMS-based motion sensors, in particular accelerometers and gyroscopes. In the framework of the current tech industry, these devices are employed for a wide variety of prominent applications as shown in Fig. A:

- Augmented Reality (AR)
- Drones
- Head Mounted Displays (HMD)
- High performance Internet of Things (IoT)
- Image stabilization
- Robotics
- Smartphones, Tablets and Wearables
- True Wireless Stereo (TWS)
- Virtual Reality (VR)

It is clear that, in the majority of these cases, a considerable deviation from the expected value of the sensed quantity (acceleration and angular velocity, respectively) is not tolerable as it may cause the failure of the desired function.

FIGURE A: Main applications employing MEMS-based motion sensors in the current tech industry.

Fig. B shows a pair of 3D layouts of MEMS devices used for motion sensing featuring a size on the order of a few hundred of micrometers; one can easily imagine that the thermal expansion of the visible micro-structures has a significant impact on the accuracy of the desired measurement. This means that temperature variations result in a drift of the outputs of these devices and, therefore, in high-precision applications, a compensation system is absolutely essential. Considering that in all the reported examples digital domain signals are handled, given their numerous advantages in terms of reproducibility, storability and processing, also the thermal compensation system should provide digital temperature information and consequently it is referred to as *Temperature-to-Digital Converters (TDC)* or *smart temperature sensor*.

This thesis presents two different TDCs designed for this purpose (*mas fuerte* and *es posible*) with an innovative approach both from the architectural and circuital point of view; both devices, indeed, employ an oversampled Successive Approximation Register (SAR) analog-to-digital conversion process and, in addition, *es posible*, an evolution of *mas fuerte*, also includes a noise shaping (NS) mechanism to achieve a better energy efficiency. Moreover, the two chips have been completely designed with a current-mode approach instead of the conventional voltage domain alternative; this choice allows op-amp-less signal processing because adding (Kirchhoff's Current Law) and scaling (current mirrors) is immediate. Considering that most of the applications of Fig. A are mobile and therefore generally rely on the supply of a battery, in order to minimize the impact of the proposed TDCs on the battery lifetime, the first crucial design target has been ultra-low energy-per-conversion (< 10 nJ). Secondly, according to the increasingly stringent demands of the market, particular attention has been devoted to the TDCs occupied silicon area to obtain compact designs (< 0.1 mm^2) ensuring an adequate cost-effectiveness.

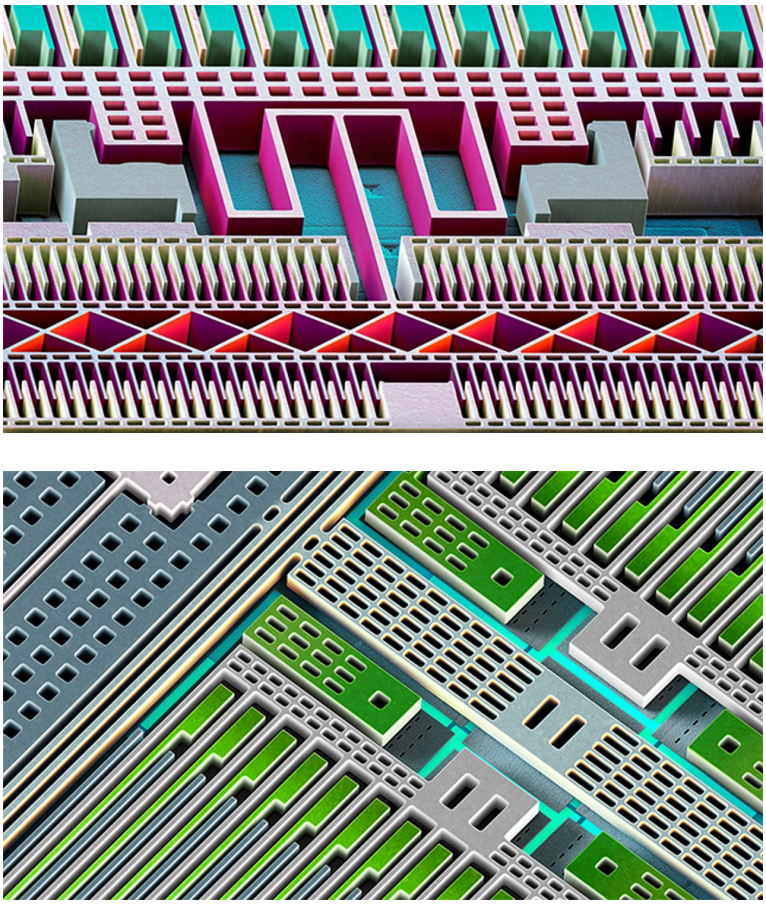


FIGURE B: 3D layouts of MEMS devices used for motion sensing.

With a distinguished focus on these targets, the proposed TDCs have been designed and fabricated in a standard 180-nm CMOS process; their development and testing is described in detail in two dedicated chapters (Chap. 3 and Chap. 4, respectively) of this doctoral thesis. In addition, Chap. 1 and Chap. 2 preliminarily present the current TDC's framework addressing some theoretical concepts, illustrating the main design techniques typically exploited, reviewing the State-of-the-Art and showing the main design trends that have developed in the last two decades. Lastly, Chap. 5 concludes the thesis providing a recap of its main highlights.

Chapter 1

Theory and Design Techniques

THERE are a lot of applications requiring on-chip temperature sensing, as seen in the introduction, and concern several systems in the microelectronics field; despite their wide range, all the reported examples [3–5,7–20] have one important feature in common: they provide temperature information in the form of digital data. This is fundamental as it makes them compatible for a direct communication with digital signal processing (DSP) circuits that can easily handle the needed temperature information and at the same time reduces the complexity of the system they are inserted in; for this reason, they are often referred to as *smart temperature sensors* [21] or as *Temperature-to-Digital Converters (TDCs)*. It is important to specify that this category of temperature sensors was born with a cost-minimization perspective and that its development in the past two decades has consequently followed this line; even if, in principle, these fully integrated temperature sensors have significant limitations in terms of accuracy and sensing range with respect to other existing discrete sensors, their great success is related to their compatibility with large-scale production of low-cost products being integrated within the system in which they are operated. Fig. 1.1 shows the conceptual diagram of a TDC.

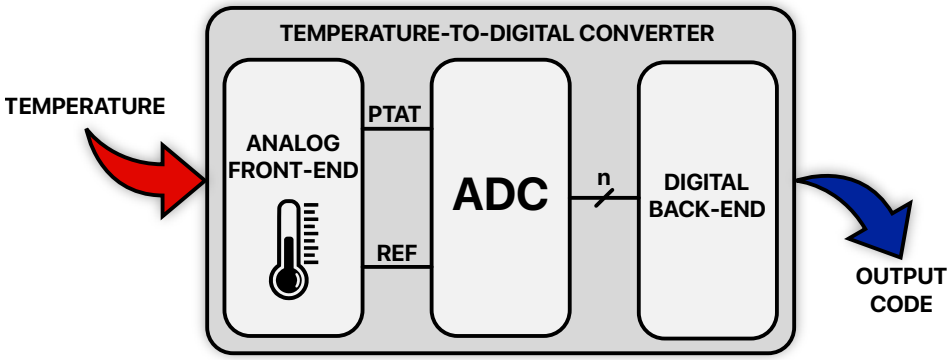


FIGURE 1.1: Conceptual diagram of a Temperature-to-Digital Converter.

It is composed of an Analog Front-End (AFE), an Analog-to-Digital Converter (ADC) and a Digital Back-End (DBE). The TDC's input signal is temperature; the AFE, the first block of the chain, is responsible to sense it achieving an electrical form for it (either in the voltage or in the current domain) and to generate at its output the signals needed for the Analog-to-Digital conversion: a proportional-to-absolute-temperature (PTAT) signal which contains the information to be converted and a reference (REF) signal, which in principle is a Zero-Temperature-Coefficient (ZTC) signal, with respect to which the conversion is carried out. Those signals enter the ADC which produces PTAT digital words with an intrinsic n-bit resolution and with a data rate (f_S) that depends on the converter architecture; this operation is typically performed without the use of sample

and hold (S/H) circuits because of the relative slowness of the temperature signal with respect to the common conversion rates of ADCs.
The n-bit codes are then processed by the DBE that, in fact, acts as an oversampler; it refines their intrinsic resolution performing decimation and filtering with a certain OverSampling Ratio (OSR) in order to obtain the output codes of the TDC which feature a higher resolution at the cost of a lower data rate (f_S/OSR). The resulting time interval required to perform a single Temperature-to-Digital conversion is therefore given by

$$T_{conv} = \frac{1}{f_S \cdot OSR}. \tag{1.1}$$

Considering the TDC's minimum working supply voltage (V_{sy}) and the current drained from it (I_{sy}), its conversion energy can be defined as

$$E_{conv} = V_{sy} \cdot I_{sy} \cdot T_{conv}. \tag{1.2}$$

It is a parameter of paramount importance together with the TDC's resolution (Res) which is the minimum temperature difference that can correctly be detected and which is determined by the quantization noise of the ADC, by the electronic noise (thermal, flicker, etc.) and by T_{conv} itself. Another parameter of interest is the temperature inaccuracy (IA); in absolute form, it is a statistical evaluation of the worst case (or $\pm 3\sigma$) temperature error and, introducing the TDC conversion range (T_{range}), its relative form can be expressed as

$$IA_{rel} = \frac{IA}{T_{range}}. \tag{1.3}$$

This quantity is strongly dependent on the number of controlled temperatures at which the TDC gets trimmed (n_{trim}) [22,23], an unavoidable procedure in most applications; the trimming process, which basically consists of calibrating the sensed temperature error, is a cost of great relevance in the TDC framework as heating and cooling the devices to be trimmed is a very time consuming operation. For this reason, n_{trim} should be minimized to preserve the cost-effectiveness of the sensor.

Due to the presence of this great variety of parameters of interest, several Figures of Merit (FoMs) have been introduced to provide TDC performance metrics in a synthetic way and from specific perspectives:

$$FoM_{Res} = E_{conv} \cdot (Res)^2, \tag{1.4}$$

$$FoM_{IA} = E_{conv} \cdot (IA_{rel})^2, \tag{1.5}$$

$$FoM_{\$} = (1 + n_{trim}) \cdot \sqrt{\frac{Area}{F^2}}, \tag{1.6}$$

$$FoM_{global} = \frac{E_{conv} \cdot Res \cdot IA}{{T_{range}}^2} \cdot (1 + n_{trim}) \cdot \sqrt{\frac{Area}{F^2}}. \tag{1.7}$$

(1.4) and (1.5), presented in [24], involve the TDC conversion energy together with its resolution or its inaccuracy, respectively. (1.6), instead, addresses only the production cost of the TDC ($Area$ is the active silicon area of the device, F is the feature size of the adopted technological process) while (1.7) provides a global overview of the TDC performance [25].

Several ADC architectures have been used, in literature, to be included in TDCs; there are examples of Flash-based TDCs [26,27], of SAR-based ones [11,28], of $\Sigma\Delta$-based ones [5,14], of time/frequency-domain-based ones [22,29] or of hybrid solutions [30,31].

It is important to notice that even if, conceptually, Flash ADCs and SAR ADCs are faster for a given quantization noise and clock frequency, to overcome the limits imposed by the presence of thermal noise, their output codes still need to be processed by the DBE and therefore, for the same amount of power consumption, are not automatically at a higher energy efficiency level with respect to the ΣΔ-based or the time/frequency-domain-based alternatives. Actually, thanks to their versatility, ΣΔ converters are the most used ones in the case of AFEs generating static temperature-dependent signals while time/frequency-domain-based ADCs are preferred in the case of dynamic temperature-dependent signals.

It makes sense to classify TDCs on the basis of the sensing device/technique adopted within the AFE; four main categories can be identified: BJT-based TDCs (Section 1.1), MOS-based TDCs (Section 1.2), resistor-based TDCs (Section 1.3) and Thermal Diffusivity (TD) based TDCs (Section 1.4). The next sections address in detail the peculiarities of each of these sensing techniques.

1.1 BJT-based TDCs

On-chip temperature sensing can be achieved exploiting the thermal behaviour of the base-to-emitter voltage (V_{BE}) of bipolar transistors operated in the forward-active region [4,5,11,13,16,19,26,32–47]. It can be expressed as

$$V_{BE} = \frac{kT}{q} ln\left(\frac{I_C}{I_S}\right) \tag{1.8}$$

where k is the Boltzmann constant, T is the absolute temperature, q is the magnitude of the elementary charge, I_C is the collector current and I_S is the bipolar saturation current which, typically, is in the fA to pA range, is proportional to the emitter area and exhibits a strong temperature dependence (as a rule of thumb, it doubles for every 5 K rise). This provides a complementary-to-absolute-temperature (CTAT) voltage variation with the well-known average slope of about -2 mV/K. Considering a pair of BJTs operating at different collector currents and/or having different emitter areas, a PTAT signal is obtained taking the difference of their base-to-emitter voltages into account.

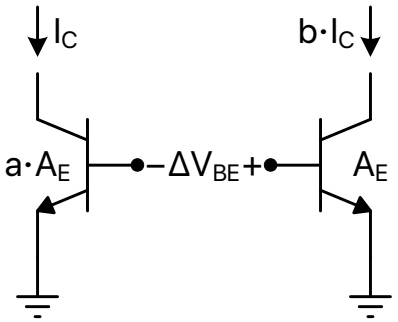


FIGURE 1.2: BJT pair for ΔV_{BE} signal generation.

According to the scheme and the notations of Fig. 1.2, the following expression holds:

$$\Delta V_{BE} = \frac{kT}{q} ln(a \cdot b) \tag{1.9}$$

where a and b are the emitter areas and collector currents ratios, respectively. Referring to Fig. 1.1, a ΔV_{BE}-dependent signal can be used as the PTAT one while the REF signal can

be generated by means of a proper combination of V_{BE}-dependent and ΔV_{BE}-dependent contributions [48].

BJT-based TDCs are the most common ones thanks to the good intrinsic accuracy of bipolar transistors [49]; this leads to temperature sensors requiring at most one trimming point to achieve inaccuracy values which other sensing techniques implement after two trimming points or more. This feature is essential from the cost-effectiveness point of view and, together with the availability of bipolar transistors (even if parasitic) within most CMOS processes, is the reason for the great employment of these kinds of devices for on-chip temperature sensing.

1.2 MOS-based TDCs

Another possibility for integrated temperature sensing is to rely on the thermal variations related to MOS devices; an option is to exploit the significant temperature dependence offered by the gate-to-source voltage (V_{GS}) of transistors operated in the subthreshold region [29, 50–53]:

$$V_{GS} = V_{th} + \frac{nkT}{q} ln\left(\frac{I_D}{I_{D0}}\right) \tag{1.10}$$

where V_{th} is the threshold voltage, n depends on the MOS structure and I_{D0} is the drain current for $V_{GS} = V_{th}$. Besides being directly proportional to the transistor aspect ratio (W/L), I_{D0} increases with temperature almost parabolically giving rise to a CTAT behaviour for V_{GS}; in absolute value, it exhibits a slightly lower average slope (about -1.5 mV/K [49]) with respect to the previously introduced V_{BE} slope (about -2 mV/K). Similarly to the BJT case, considering a pair of MOSFETs biased at different drain currents and/or having different aspect ratios, a PTAT signal is obtained taking the difference of their gate-to-source voltages into account.

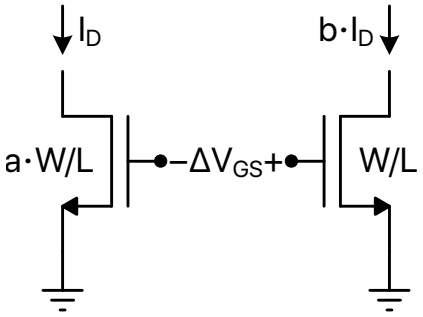


FIGURE 1.3: MOSFET pair for ΔV_{GS} signal generation.

According to the scheme and the notations of Fig. 1.3, the ΔV_{GS} signal can be expressed as

$$\Delta V_{GS} = \frac{nkT}{q} ln(a \cdot b) \tag{1.11}$$

where a and b are the W/L and drain currents ratios, respectively. It is interesting to notice that the PTAT sensitivity offered by subthreshold operated MOS devices benefits from the presence of the n coefficient if compared to the bipolar case; considering that this technology dependent parameter is intrinsically larger than 1, for the same a and b ratios, the ΔV_{GS} temperature sensitivity is intrinsically higher than the ΔV_{BE} one [49]. Also in this case, a reference signal can be generated by combining V_{GS}-dependent and ΔV_{GS}-dependent contributions.

Another option to exploit the temperature dependence of MOS devices for on-chip sensing is to consider the propagation time (t_p) of CMOS inverters; as shown in (1.12), this parameter depends on many variables such as the adopted supply voltage (V_{DD}), the threshold voltage (V_{th}) and the size (W,L) of the devices constituting the inverter, the carriers mobility (μ), the oxide capacitance (C_{ox}) and the capacitance (C_L) of the load to be driven:

$$t_p = f(V_{DD}, V_{th}(T), \mu(T), W, L, C_{ox}, C_L). \tag{1.12}$$

In particular, V_{th} and μ are a function of the temperature that, if properly exploited, may lead to an effective sensing.

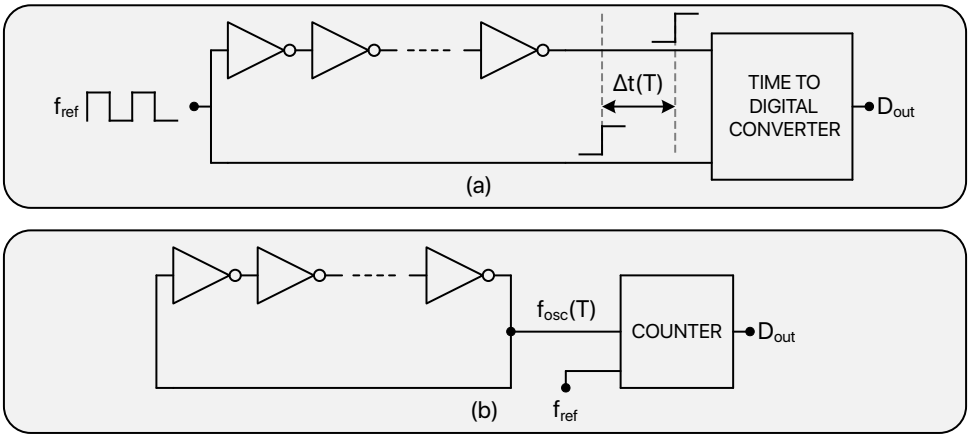


FIGURE 1.4: Main circuits that exploit the temperature dependency of the propagation time of CMOS inverters to achieve a Temperature-to-Digital conversion: delay line based TDC (**a**), ring oscillator based TDC (**b**).

The first way to achieve a t_p-based temperature to digital conversion is to rely on a delay line [29, 30, 54–57] as shown in Fig. 1.4a. A clock signal running at a reference frequency (f_{ref}) is passed through a delay line composed by N inverters and is compared with an undelayed version of itself; this gives rise to temperature dependent time intervals which can be expressed as

$$\Delta t(T) = N \cdot t_p(T), \tag{1.13}$$

and which are processed by a time-to-digital converter that, hence, generates temperature dependent digital words (D_{out}).

The second possibility, instead, is to exploit the thermal behaviour of ring oscillators [22, 52, 53, 58–64] as shown in Fig. 1.4b in which the t_p temperature dependence impacts the oscillation frequency (f_{osc}) as shown by the following expression:

$$f_{osc}(T) = \frac{1}{2t_p(T)N}. \tag{1.14}$$

The signal produced by the oscillator gets processed by a counter (clocked at f_{ref}) which generates temperature dependent digital codes (D_{out}) depending on the oscillations count.

In addition to this, in 2019, new interesting MOS-based techniques were proposed, opening the doors for sub-nW TDCs design. An innovative temperature sensing principle based on the gate-leakage current of MOS devices was adopted in [65, 66], resulting in an exceptionally low power consumption.

The t_p-based and the leakage-based approaches offer outstanding performance in terms of energy/conversion but typically exhibit poor linearity and accuracy.

1.3 Resistor-based TDCs

Also integrated resistors exhibit a significant thermal variability that makes them suitable for on-chip temperature sensing. Considering a first order approximation, their resistance value can be expressed as

$$R = R_0(1 + TC \cdot \Delta T), \tag{1.15}$$

where R_0 is the resistance value at a reference temperature T_0, TC is the temperature coefficient and

$$\Delta T = T - T_0. \tag{1.16}$$

Tab. 1.1 and Tab. 1.2 report realistic TC values for some kinds of resistors in 0.18-µm and 65-nm CMOS processes, respectively.

Resistor Type	**TC [K^{-1}]**
n+ diffusion	$+1.5 \cdot 10^{-3}$
p+ diffusion	$+1.5 \cdot 10^{-3}$
n-poly	$-1.5 \cdot 10^{-3}$
n-well	$+3.0 \cdot 10^{-3}$

TABLE 1.1: First order TCs of different resistor types in a standard 0.18-µm CMOS process [67].

Resistor Type	**TC [K^{-1}]**
n+ diffusion with salicide	$+2.2 \cdot 10^{-3}$
n+ diffusion without salicide	$+1.6 \cdot 10^{-3}$
n+ poly with salicide	$+2.2 \cdot 10^{-3}$
n+ poly without salicide	$+1.2 \cdot 10^{-3}$
n-well under oxide diffusion	$+2.5 \cdot 10^{-3}$
n-well under shallow trench isolation	$+2.0 \cdot 10^{-3}$
p+ diffusion with salicide	$+2.4 \cdot 10^{-3}$
p+ diffusion without salicide	$+1.3 \cdot 10^{-3}$
p+ poly with salicide	$+2.4 \cdot 10^{-3}$
p+ poly without salicide	$-3.2 \cdot 10^{-3}$

TABLE 1.2: First order TCs of different resistor types in a standard 65-nm CMOS process [68].

In the last decade, three main techniques have been exploited to electronically benefit from the temperature dependence of such resistors: Wheatstone bridges, RC filters and Wien-bridge filters. Fig. 1.5 illustrates the basic schemes of these sensing possibilities.

TDCs based on Wheatstone bridges [28,31,69–72] typically rely on the combined effect of a positive TC resistor (R_p) and of a negative TC one (R_n).

$$R_p = R_0(1 + \alpha\Delta T),\ \alpha > 0, \tag{1.17}$$

$$R_n = R_0(1 + \beta\Delta T),\ \beta < 0. \tag{1.18}$$

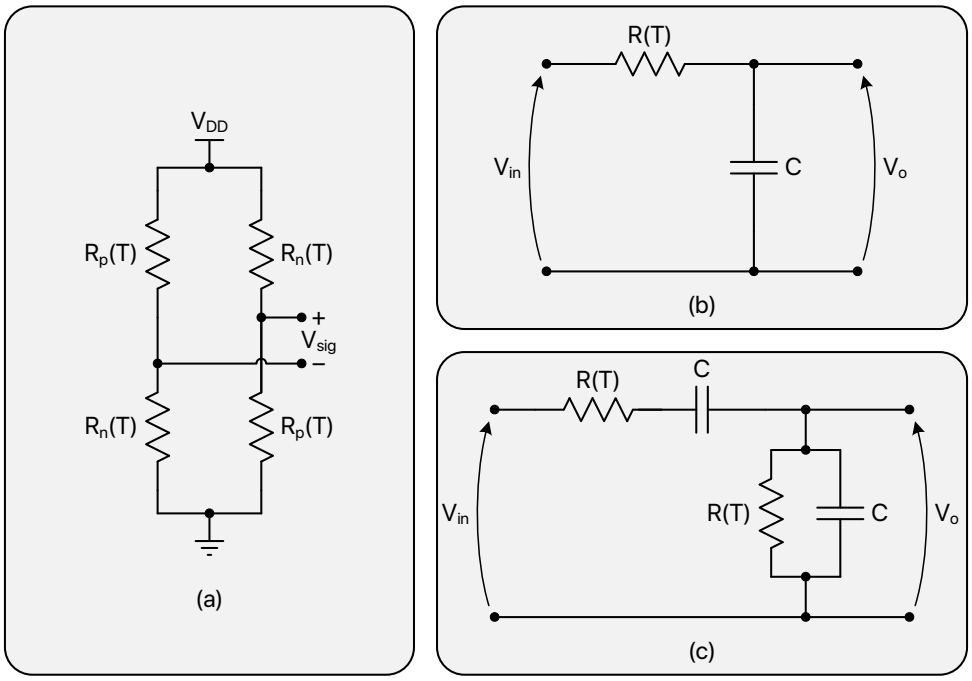


FIGURE 1.5: Main circuits used to extract temperature information from the thermal behaviour of integrated resistors: Wheatstone bridge (**a**); RC filter (**b**); Wien-bridge filter (**c**).

According to Fig. 1.5a, temperature information is contained in the V_{sig} voltage, which can be expressed as

$$V_{sig} = \frac{R_p - R_n}{R_p + R_n} \cdot V_{DD} = \frac{(\alpha - \beta)\Delta T}{2 + (\alpha + \beta)\Delta T} \cdot V_{DD}. \tag{1.19}$$

Fig. 1.6 shows V_{sig} as a function of temperature for several $(|\alpha|;|\beta|)$ combinations in a symmetrical 100 K ΔT range; to maximize the Wheatstone bridge temperature sensitivity, the $|\beta|/|\alpha|$ ratio should be selected as high as possible according to the resistor availability of the adopted technology. On the other hand, as pointed out by Tab. 1.3 and as can be easily derived from (1.19), the linearity of the thermal response degrades moving away from the $|\alpha| = |\beta|$ optimal case (it is important to mention that the reported considerations do not take any second or higher order contribution to the resistance temperature variability into account).

α [K^{-1}]	β [K^{-1}]	Sensitivity [mV/K]	Nonlinearity [1] [mV]
$+1.5 \cdot 10^{-3}$	$-3.0 \cdot 10^{-3}$	2.25	126
$+1.5 \cdot 10^{-3}$	$-2.25 \cdot 10^{-3}$	1.88	52.44
$+1.5 \cdot 10^{-3}$	$-1.5 \cdot 10^{-3}$	1.5	0
$+1.5 \cdot 10^{-3}$	$-0.75 \cdot 10^{-3}$	1.13	31.46

[1] Evaluated as norm of residuals between V_{sig} and its linear fit across the considered ΔT range.

TABLE 1.3: Additional details regarding the curves of Figure 4.3.

TDCs based on RC [68,73,74] and Wien-bridge [67,75–78] filters, instead, take advantage of the temperature variations of their transfer functions; in both cases, as can be deduced from Fig. 1.5b,c, the temperature dependence of the employed resistors causes an

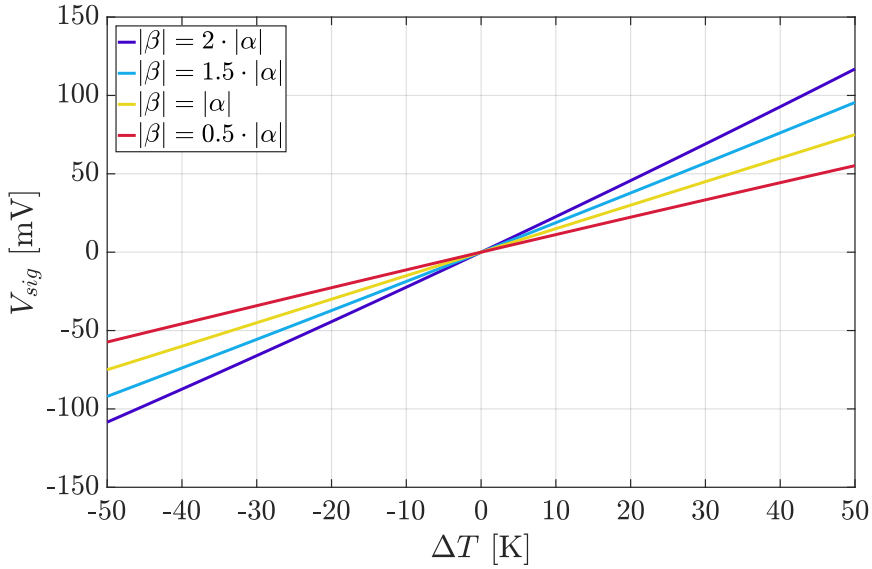


FIGURE 1.6: V_{sig} as a function of ΔT in different $(|\alpha|;|\beta|)$ conditions for $\alpha = +1.5 \cdot 10^{-3}$ K^{-1}, realistic value for n+ diffusion integrated resistors.

alteration of their phase response that can be exploited to achieve the desired temperature-to-digital conversion; this is achieved by driving the considered structures with signals oscillating close to the fundamental frequency of the filters ($\omega_0 = 1/R(T)C$ in both cases) at room temperature and processing their output by means of appropriate phase-to-digital conversion circuits.
Given the RC transfer function,

$$H(j\omega) = \frac{1}{1 + j\omega R(T)C}, \tag{1.20}$$

its temperature-dependent phase shift can be expressed as

$$\phi(j\omega) = -\arctan\left(\omega R(T)C\right). \tag{1.21}$$

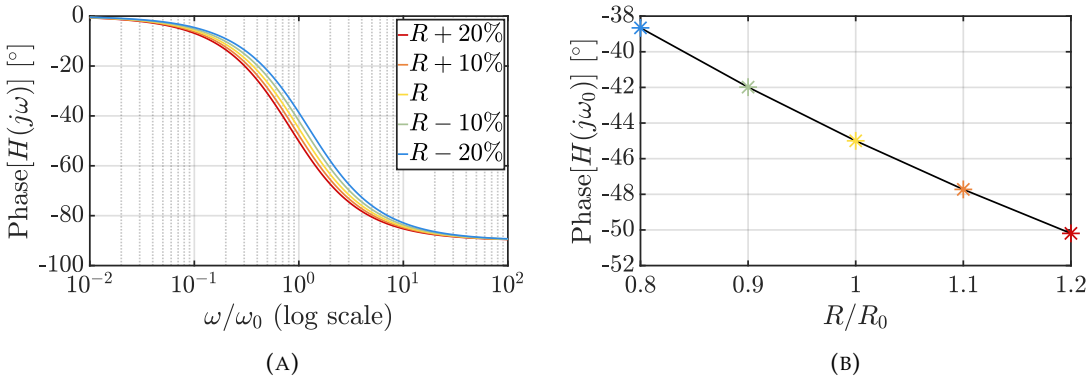
Fig. 1.7a shows the RC phase response for different resistance values in the $\pm 20\%$ range where the selected colors conceptually refer to a positive TC resistor (the warmer the color, the higher the temperature); since the most effective temperature phase impact occurs at $\omega = \omega_0$, Fig. 1.7b reports the phase shift generated by the RC filter as a function of the resistance variation with respect to the room temperature value (R_0).
The Wien-bridge transfer function is instead given by

$$H_{WB}(j\omega) = \frac{j\omega R(T)C}{1 - \omega^2 R^2(T)C^2 + 3j\omega R(T)C}, \tag{1.22}$$

and its temperature-dependent phase shift can be expressed as

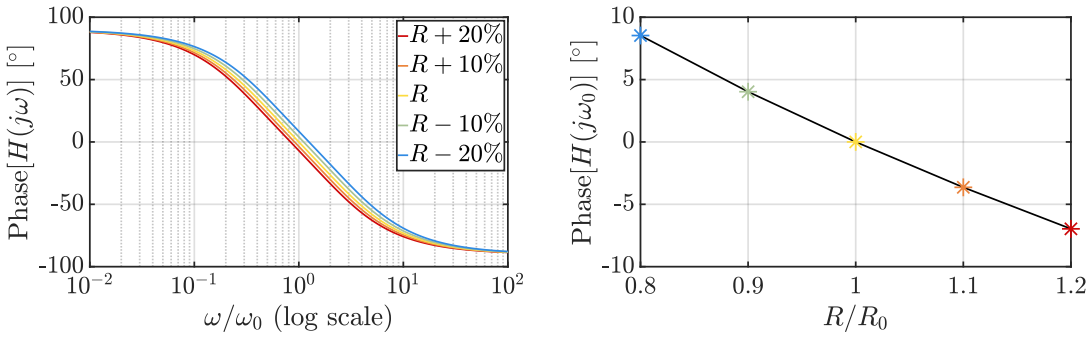
$$\phi_{WB}(j\omega) = -\arctan\left(\frac{\omega^2 R^2(T)C^2 - 1}{3\omega R(T)C}\right). \tag{1.23}$$

Fig. 1.8a shows the Wien-bridge phase response for the same resistance variation range considered for the RC case while Fig. 1.8b reports the resulting phase shift at ω_0.



(A) (B)

FIGURE 1.7: Phase dependency on resistance variations for an RC filter: impact on the phase response of the filter (**a**) and phase shift at ω_0 as a function of the resistance variation (**b**).



(A) (B)

FIGURE 1.8: Phase dependency on resistance variations for a Wien-bridge filter: impact on the phase response of the filter (**a**) and phase shift at ω_0 as a function of the resistance variation (**b**).

For the same resistance variation and capacitor value (C), the Wien-bridge filter achieves a better phase sensitivity to temperature and linearity if compared to the RC one at the cost of a double occupied area; considering that, typically, the size of the filter is not the limiting element in the TDC area breakdown, Wien-bridge filters are the preferred choice over RC ones.

As will be addressed in Chapter 2, the TDCs exploiting the presented resistor-based temperature sensing techniques are undoubtedly the best in class from the energy efficiency point of view but typically are less accurate than BJT-based solutions and more power hungry than MOS-based solutions.

1.4 TD-based TDCs

The last considered category is that of thermal diffusivity TDCs [79–84]. These on-chip sensors exploit measurements of the thermal diffusivity of silicon (D_{Si}) which exhibits a considerable temperature dependence and, moreover, does not suffer from process spread variations. This quantity can be sensed by means of the electrothermal filter (ETF) shown in Fig. 1.9.

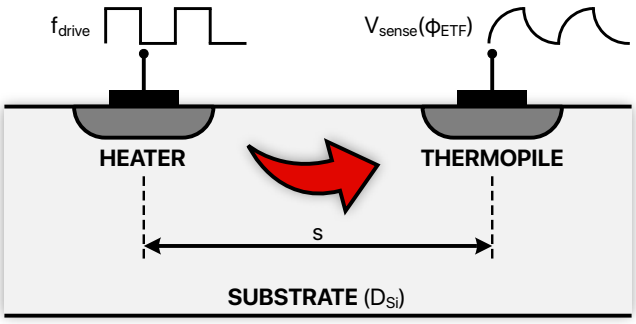


FIGURE 1.9: Electrothermal filter for thermal diffusivity measurement.

A heater that can be realized by a diffusion resistor is driven by a square wave (at a f_{drive} frequency) and, consequently, generates heat pulses which diffuse to a neighboring thermopile placed at a distance s; these pulses are affected by a delay and by an attenuation which are determined by D_{Si} which, in turn, is a function of the temperature ($\propto T^{1.8}$) [81]. For this reason, the phase of the voltage sensed by the thermopile (V_{sense}) is sensitive to temperature and, according to [84], can be expressed as

$$\phi_{ETF}(T) = -s \cdot \sqrt{\frac{f_{drive}}{2D_{Si}(T)}}. \tag{1.24}$$

With similar phase-to-digital conversion solutions as the ones needed for the previously introduced RC-based and Wien-bridge-based TDCs, ϕ_{ETF} can be digitized, thus generating temperature dependent digital codes. The major drawback of this kind of sensing technique is the large amount of power (>1 mW) burnt to drive the heater: its energy inefficiency makes it unsuitable for the majority of battery-powered applications. Nevertheless, TD-based TDCs offer a really remarkable accuracy performance, especially considering that, in many cases, no trimming procedure is required; this aspect will be further explored in Chapter 2.

Chapter 2

State-of-the-Art Review and Design Trends

OVER the past two decades, more than 150 TDC works have been published, each of which can be assigned to one of the four categories introduced in Chapter 1. A really valuable survey [85] that keeps track of all these works has been made available by prof. Makinwa from TU Delft and has been adopted as dataset for all the following analysis and considerations. The time evolution and the performance peculiarities of the four considered TDC types are investigated in the next sections, each addressing a primary parameter of interest of TDCs: resolution (Section 2.1), inaccuracy (Section 2.2), conversion energy (Section 2.3), energy efficiency (Section 2.4) and silicon area (Section 2.5). All the reported trend-lines have been produced by a log-scale adapted smoothing spline method based on the geometric mean of the considered parameter values for each year.

2.1 Resolution

As introduced in Chapter 1, the resolution of a TDC is the minimum temperature difference that can correctly be detected; it is a function of the intrinsic quantization noise of the ADC used to perform the temperature-to-digital conversion, of the amount of electronic noise that affects the TDC output and of the DBE processing type.

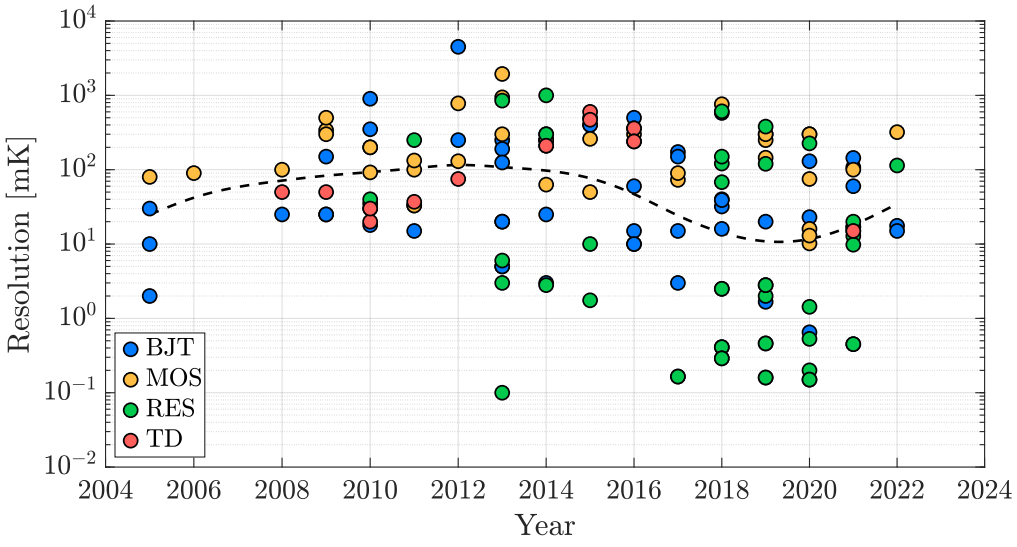


FIGURE 2.1: TDC resolution time evolution in the last two decades.

Fig. 2.1 reports the resolution of the considered works as a function of the publication year for all of the four studied categories of sensors; it can be noticed that the resolution performance of TDCs is basically trend-less since its requirements are strongly application-dependent: the resolution specification is of prime importance in the cases in which the sensing goal is to precisely detect temperature variations but a moderate value can be acceptable in the case of accuracy-oriented designs, in favour of a conversion energy saving. In addition to this, it can be observed that the first examples of resistor-based TDCs have been introduced just starting from 2010 and, a few years later, a series of high resolution works exploiting this sensing approach has been proposed, actually showing their greater potential regarding the resolution parameter.

This feature can be further appreciated, considering Fig. 2.2; the resolution of each item shown in Fig. 2.1 has been collected to build a bar plot organized on the basis of five decades: maintaining the sensing-type distinction, it provides an overview of how the resolution performance of all the considered works is distributed, confirming the advantage of resistor-based TDCs. It should be taken into account that, in principle, resolution can always be improved by increasing the DBE OSR at the cost of a higher conversion time (1.1) and that, therefore, the performance limitation of the other kinds of sensing approaches is actually related to their worse energy efficiency, a parameter that will be addressed in detail in Section 2.4.

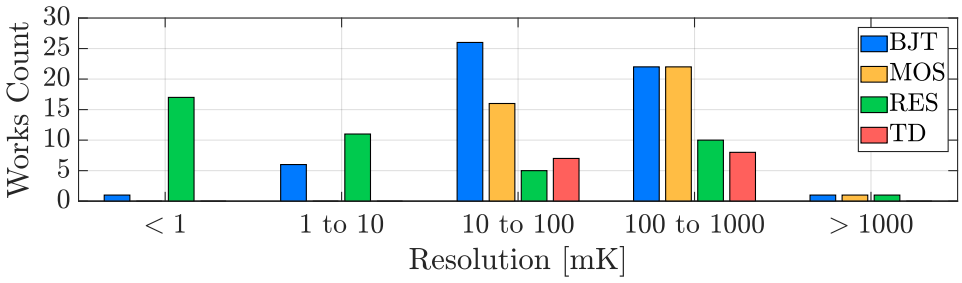


FIGURE 2.2: TDC resolution performance distribution with sensing-type distinction.

2.2 Inaccuracy

In the same vein of what was presented for resolution, Fig. 2.3 shows the relative inaccuracy, defined in (1.3), as a function of the publication year for the TDCs surveyed in [85]. Also in this case, a trend-less behaviour can be noticed, once again because of the application-dependency of the accuracy specification of TDCs. For example, the ones designed for clinical applications require absolute inaccuracy values on the order of ±0.1 °C, while the ones used to track the temperature status of microprocessors or to compensate for the thermal drift in MEMS resonators typically require an inaccuracy of about ±1 °C or even worse. In order to evaluate the accuracy performance potential of the four considered sensing techniques, it is of paramount importance to take the number of trimming points into account since, as a rule of thumb, the transition to the 1-point trimming condition from the untrimmed one typically provides a benefit of at least a factor two to the accuracy of the sensor, while the addition of a trimming point at a second temperature generally improves the TDC accuracy of at least an extra factor four. For this reason, the inaccuracy bar plot, analogous to the resolution one of Fig. 2.2, has been split into three plots: Fig. 2.4 addresses the untrimmed works, Fig. 2.5 focuses on the TDCs

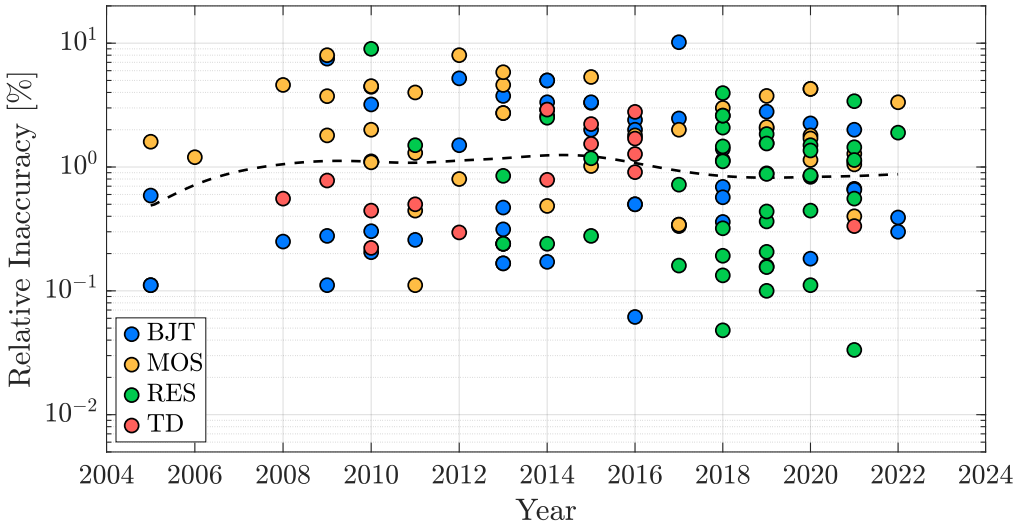


FIGURE 2.3: TDC inaccuracy time evolution in the last two decades.

with a single-temperature trimming, while Fig. 2.6 considers the works with at least two trimming points.

It can be seen that, from the accuracy point of view, the TD-based TDCs are the best in class, followed by the BJT-based ones; they are, indeed, the only types of sensors that can achieve relatively good accuracy without the need of being trimmed (Fig. 2.4), a huge advantage in terms of cost-effectiveness. MOS-based TDCs and resistor-based TDCs, instead, require at least one trimming point (in most cases 2-pts, Fig. 2.6) to offer acceptable performance and therefore are undesirable for accuracy-oriented designs. On top of this, it is important to remember that, in addition to the spread due to the sensing element, inaccuracy is also determined by the spread of all the components present in the device [49] and consequently it may not be limited by the sensing technique choice but by the matching performance of the entire circuitry of the AFE and of the ADC. In this framework, a key element to take into account is the silicon area size of the TDC (addressed in Section 2.5): the smaller its active area, the tougher the achievement of acceptable accuracy values.

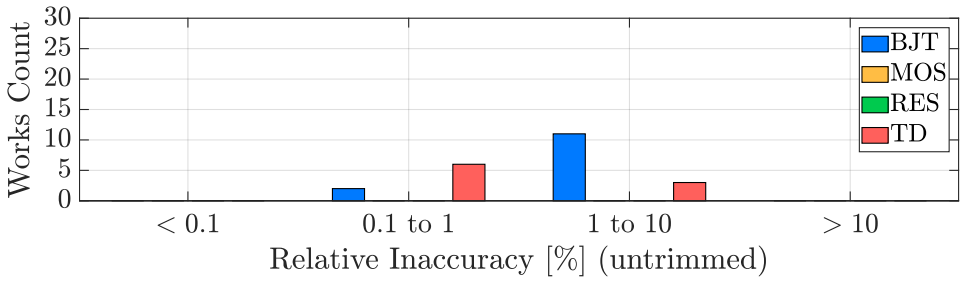


FIGURE 2.4: Untrimmed TDC inaccuracy performance distribution with sensing-type distinction.

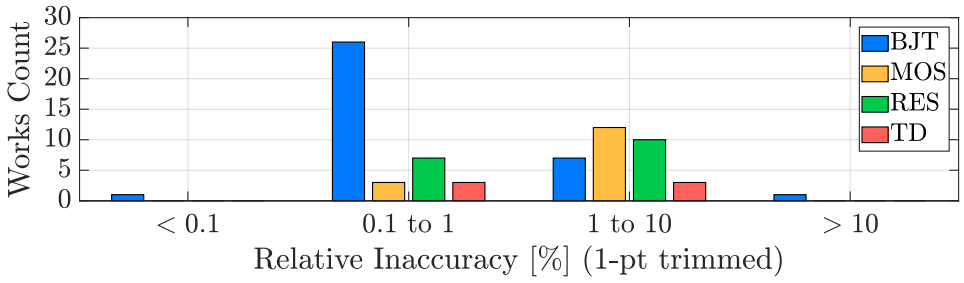


FIGURE 2.5: 1-pt trimmed TDC inaccuracy performance distribution with sensing-type distinction.

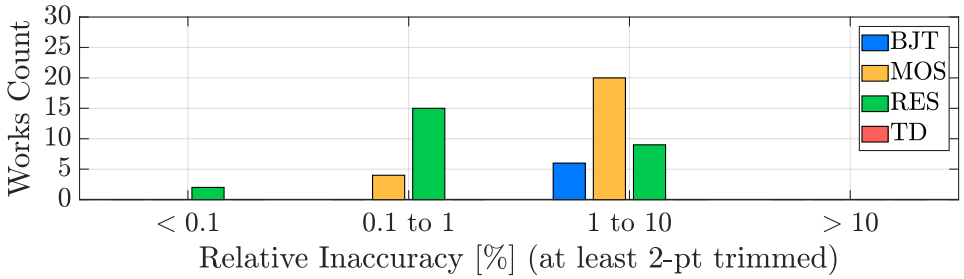


FIGURE 2.6: 2-pt (or more) trimmed TDC inaccuracy performance distribution with sensing-type distinction.

2.3 Conversion Energy

The growth of the IoT market and the increasing number of battery-powered systems requiring on-chip temperature sensing have induced a really strong trend when it comes to TDC conversion energy (1.2). This parameter, which is a full-fledged measure of the energy price to pay to achieve a single temperature-to-digital conversion, is crucial to ensure the highest battery lifetime possible or even to allow the operation of energy-harvesting-based devices such as [86], in which temperature-dependent digital codes are generated with just a few picojoules of energy.

Fig. 2.7 reports the conversion energy values of the same works analyzed in the previous sections as a function of their publication year. In this case, a trend towards lower values is definitely visible; the TDC conversion energy exhibits a reduction of about a factor 10 every five years, a clear direction that allows for predicting the future evolution of these kinds of devices.

As reported for the resolution and the inaccuracy cases, Fig. 2.8 shows the conversion energy performance distribution across four orders of magnitude and with the different sensing-types taken into account. It can be noticed that, undoubtedly, TD-based TDCs, due to the power consumed by the heater, require the highest conversion energy while the other three types exhibit quite similar performance. Similarly to the resolution discussion (Section 2.1), it is important to consider that, naturally, the conversion energy can be reduced by accepting a poorer temperature resolution and therefore, also in this case, the reported conversion energy values are linked to the efficiency of the different sensing techniques that will be addressed in the next Section.

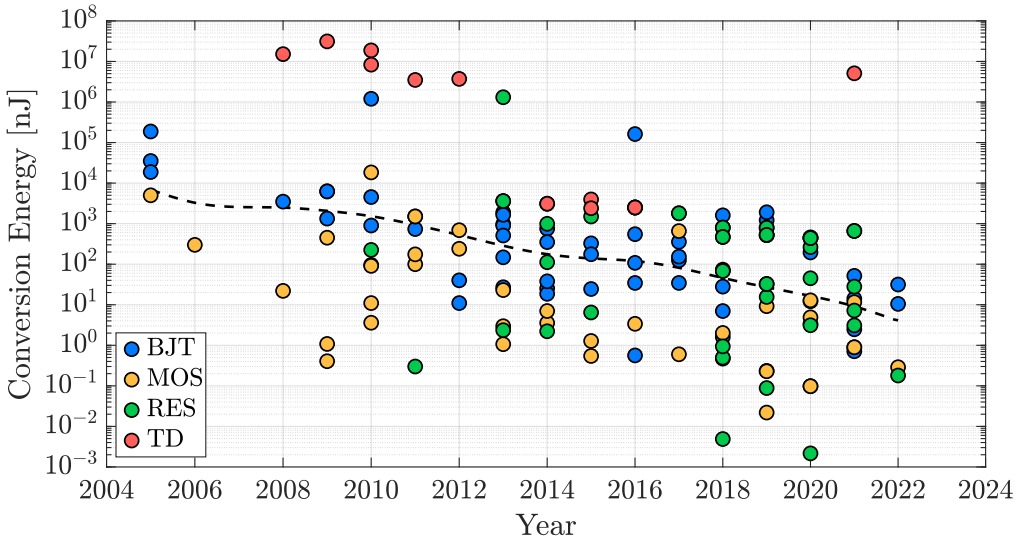


FIGURE 2.7: TDC conversion energy time evolution in the last two decades.

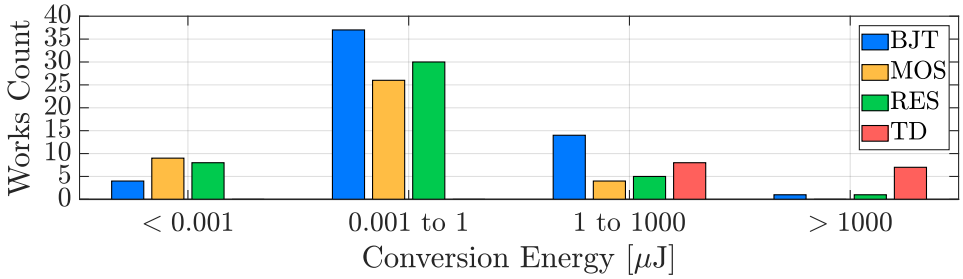


FIGURE 2.8: TDC conversion energy performance distribution with sensing-type distinction.

2.4 Energy Efficiency

Both Sections 2.1 and 2.3 have introduced the resolution vs. conversion energy trade-off. The energy efficiency of a TDC is a metric of what resolution can be achieved for a given conversion energy or, on the other hand, what conversion energy is needed to achieve a target resolution. To determine what the trade space of a certain TDC is and, consequently, to determine its energy efficiency, it is useful to consider the resolution FoM introduced in (1.4), in which *Res* is squared because it is usually limited by thermal noise and therefore, to achieve an improvement of a factor two of it, a four times larger conversion time is required and so on. Fig. 2.9 shows the time evolution of the energy efficiency of the same considered works of the previous subsections. Three different phases can be identified: at first, approximately until 2010, there is a horizontal phase in which the novelty of such kind of integrated sensors has resulted in TDCs without the primary target of energy efficiency but simply aiming at a proper operation of the device (functionality phase). Then, from 2010 to 2019, the trend starts to bend down, taking a definite direction with an improvement of about a factor 10 every 3 years (performance phase); lastly, from 2020 onwards, a significant breaking of the trend-line can be observed, which indicates the difficulty for a further progress of the TDC energy efficiency (saturation phase).

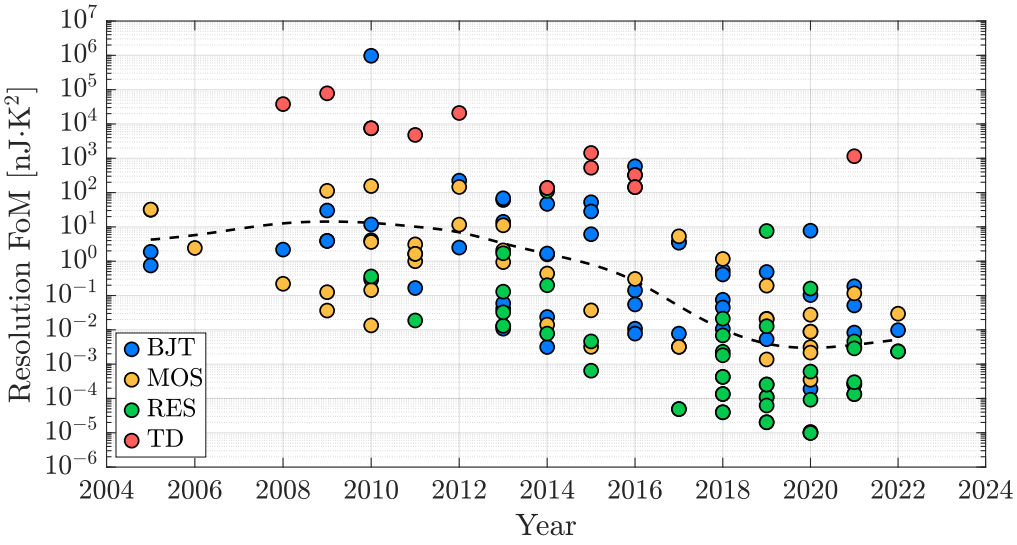


FIGURE 2.9: TDC energy efficiency time evolution in the last two decades.

Similarly to what has been proposed for the previously analyzed TDC parameters of interest, the bar plot of Fig. 2.10 provides an overview of how the different kinds of considered sensing techniques are distributed in terms of energy efficiency. It is clear that, from this point of view, the best performing sensors are the resistor-based ones; BJT-based and MOS-based TDCs offer quite similar performance while, as previously introduced, TD-based TDCs are the most energy-inefficient ones.

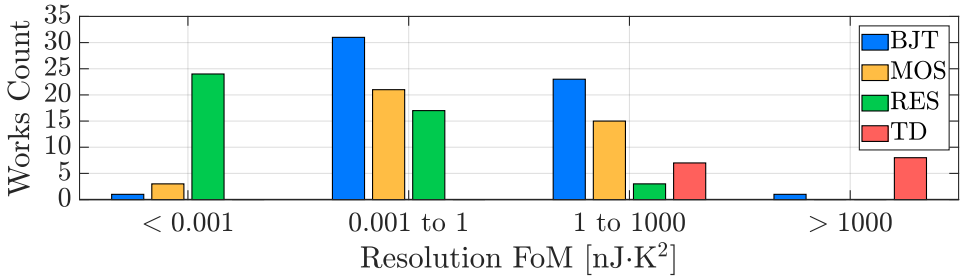


FIGURE 2.10: TDC energy efficiency performance distribution with sensing-type distinction.

2.5 Silicon Area

Finally, the occupied silicon area of the considered TDC works is taken into account; still bearing in mind that it usually offers a direct trade-off with the temperature sensing accuracy performance, the compactness of the TDC is a fundamental requirement considering a production cost minimization perspective. Accordingly, in the last two decades, the size reduction trend has been pretty significant and is shown in Fig. 2.11: it can be observed that the silicon areas of the oldest reported works in the range of 1 mm^2 have progressively given way to designs featuring active areas reaching a few hundred of μm^2.

Once more, Fig. 2.12 shows how the considered TDCs are distributed in terms of active area and sensing-type. In this case, as will become clearer in the wrap-up proposed in Section 2.6, the sensors that, on average, offer the best compactness are the MOS-based ones, followed by the TD-based ones; resistor-based and BJT-based devices, even if there are exceptional cases as [87] or [28], generally require a larger area.

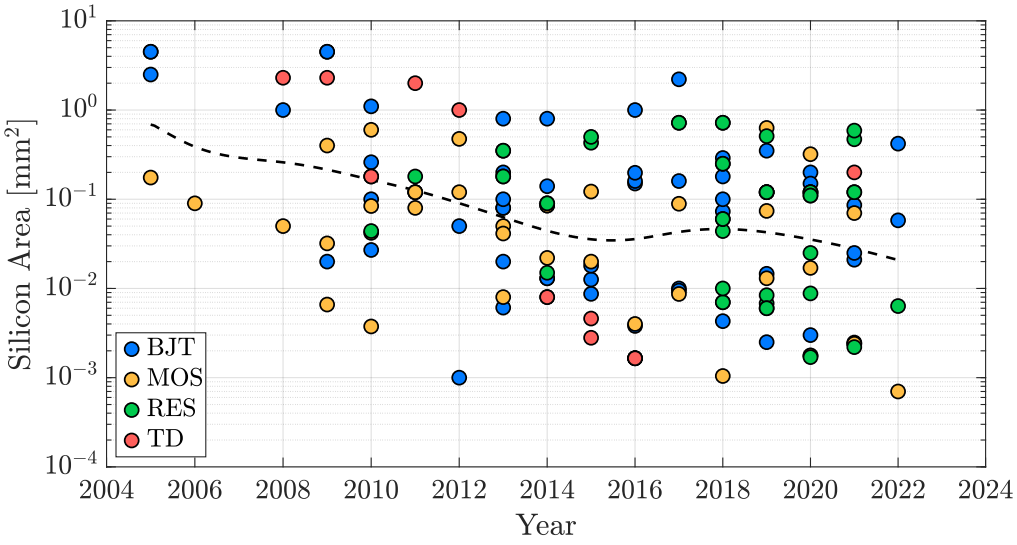


FIGURE 2.11: TDC silicon area time evolution in the last two decades.

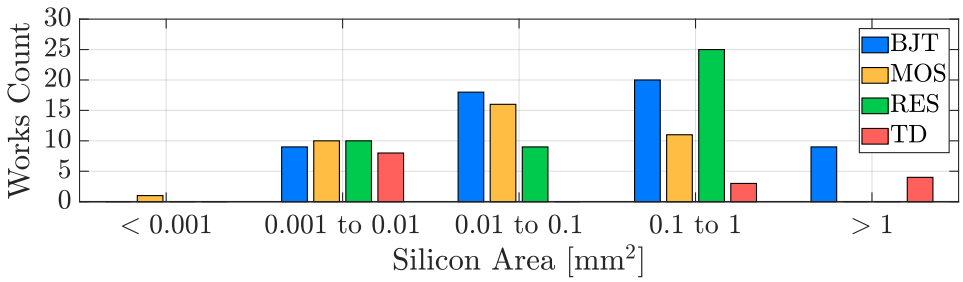


FIGURE 2.12: TDC silicon area distribution with sensing-type distinction.

2.6 Wrap-up

To summarize the proposed considerations, Tab. 2.1 reports performance indicators for each of the four studied sensing techniques and for each of the parameters of interest previously analyzed, with inaccuracy differentiated according to the number of adopted trimming points. For every entry, the geometric mean of the corresponding values of the TDC works discussed in the previous Sections has been computed and considered as a meaningful indicator being based on two decades of research activity. For each parameter, the best indicator has been highlighted in green so that the most attractive features of each sensing category could be easily identified; it is interesting to note that, on the

basis of a TDC design specifications, each of the sensing techniques could be the optimal choice. Indeed, BJT-based sensors exhibit the best 1-pt trimmed inaccuracy indicator, MOS-based sensors have the lowest conversion energy one and offer the highest degree of compactness, resistor-based sensors feature the best resolution, energy efficiency and accuracy after at least 2 trimming points, while TD-based sensors exhibit the lowest untrimmed inaccuracy.

	BJT	**MOS**	**Resistor**	**TD**
Resolution	48 mK	125 mK	**5 mK**	112 mK
Inaccuracy (untrimmed)	1.95 %	/	/	**0.77 %**
Inaccuracy (1-pt trimmed)	**0.46 %**	2.10 %	1.21 %	0.98 %
Inaccuracy (at least 2-pt trimmed)	3.47 %	1.59 %	**0.45 %**	/
Conversion Energy	195 nJ	**12 nJ**	51 nJ	121 µJ
Resolution FoM	0.45 nJ·K^2	0.18 nJ·K^2	**1.43 fJ·K^2**	1.53 µJ·K^2
Silicon Area	0.085 mm^2	**0.033 mm^2**	0.073 mm^2	0.038 mm^2

TABLE 2.1: Performance recap of the different TDC sensing types.

Starting from the results collected in Tab. 2.1, it has been possible to build a spider chart (Fig. 2.13) to provide a graphical representation of the considerations presented in this Chapter to intuitively and immediately figure out the strengths and the weaknesses of the different categories of TDCs.

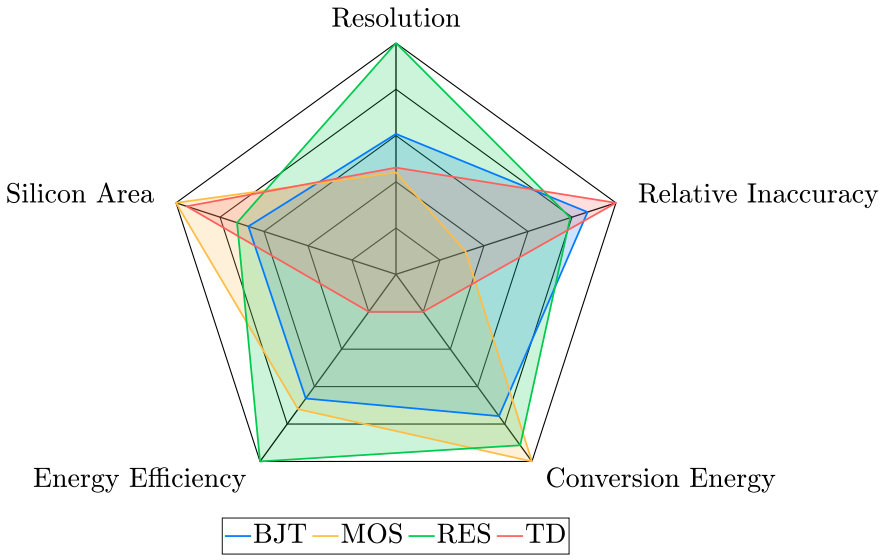


FIGURE 2.13: Spider chart summarizing the peculiarities of the four studied categories of TDCs.

To effectively design the spider chart, all the values reported in Tab. 2.1 have been normalized with respect to the best one for each parameter of interest (the relative inaccuracy values have been merged according to the coefficients of the rule of thumb introduced in Section 2.2); then, considering that all the parameters are of the lower-is-better kind, they have been converted to a higher-is-better mode with a simple inversion and, finally, have been plotted adopting log-scaled axes to make differences of orders of magnitude still appreciable. Given the extent of the corresponding pentagon, the chart clearly illustrates how promising resistor-based TDCs are and motivates the high number of works

exploiting this sensing technique published in the last four years as shown in this Chapter. Nevertheless, these kinds of TDCs have considerable linearity issues and, in most cases [28,31,67,68,70–72,76–78], the employment of nonlinearity polynomial error correction techniques is mandatory; this limit, considering that linearity is a crucial parameter for example in MEMS thermal drift compensation applications, may guide the sensing-type choice to the presented alternatives.

Chapter 3

mas fuerte test chip

As presented in the Introduction, the MEMS field has experienced a remarkable growth in the last years, due to the increasing exploitation of MEMS devices in everyday life sensors, supported by a concurrent technological development, thus driving the research target toward systems with higher robustness with respect to environmental effects.
One of the main challenges in this framework is, indeed, to overcome the impact of the ambient temperature on the performance of MEMS-based motion sensors, considering that the micro-structures used as sensing elements are characterized by particularly fast temperature variations, that result in a significant degradation of the reliability of the sensed quantity. Therefore, in order to cancel this effect in high precision applications, these devices require a responsive and energy-efficient monitoring of the temperature, to compensate for the drift of the parameters of interest.
This Chapter presents a NPN-based Temperature-to-Digital Converter (TDC) designed and fabricated for this application and called *mas fuerte*; its development has been carried out according to the following design specifications.

- **Conversion energy < 10 nJ**
  This requirement quantifies the minimization of the energy impact of the TDC on the battery lifetime of the motion sensing device it has to work with.
- **Silicon area < 0.1 mm^2**
  This degree of compactness ensures the adequate cost-effectiveness of the TDC with respect to the system it is inserted in.
- **Temperature range = $-40\,^\circ$C to $125\,^\circ$C**
  Even if the actual range of interest is from $0\,^\circ$C to $80\,^\circ$C, the extended range requirement has been set for robustness checks on the TDC.
- **Resolution < 200 mK**
  This requirement comes from the noise performance at the output of the motion sensor that makes such a resolution level sufficient.
- **Inaccuracy < 2 %**
  Due to the compensating nature of the TDC, relative temperature variations are what really matters; for this reason such a moderate accuracy target has been set (2 % corresponds to a $\pm 1.65\,^\circ$C error in the considered temperature range).
- **Trimming Points < 2**
  This specification is strictly related to the cost-effectiveness of the TDC: as introduced in Chapter 1, heating and cooling the TDC for calibration is a cost of great relevance in the production framework.

- **Technology = TSMC 180-nm CMOS**
  The choice of the technology process for the TDC design is bound by the one adopted for already existing circuits designed to process the motion sensor's output.

- **Nominal supply voltage = 1.8 V**
  This is the standard V_{DD} level corresponding to the adopted technology; however, the possibility to supply the TDC at a lower supply voltage is not precluded and may be explored to reduce its power consumption.

3.1 TDC Architecture

The proposed TDC is based on a fully current-mode processing approach: except for the digital output stage, every signal is in the form of an electrical current. Considering the extreme simplicity in summing and scaling signals in the current domain, this approach allows sparing several adding and amplifying circuits, inherently required in its voltage-domain counterpart. Moreover, it opens the possibility to operate with reduced supply voltage constraints, making it suitable for more scaled fabrication technologies. Fig. 3.1 shows the block diagram of the TDC. It consists of an Analog Front-End (AFE) circuit followed by an oversampled SAR ADC.

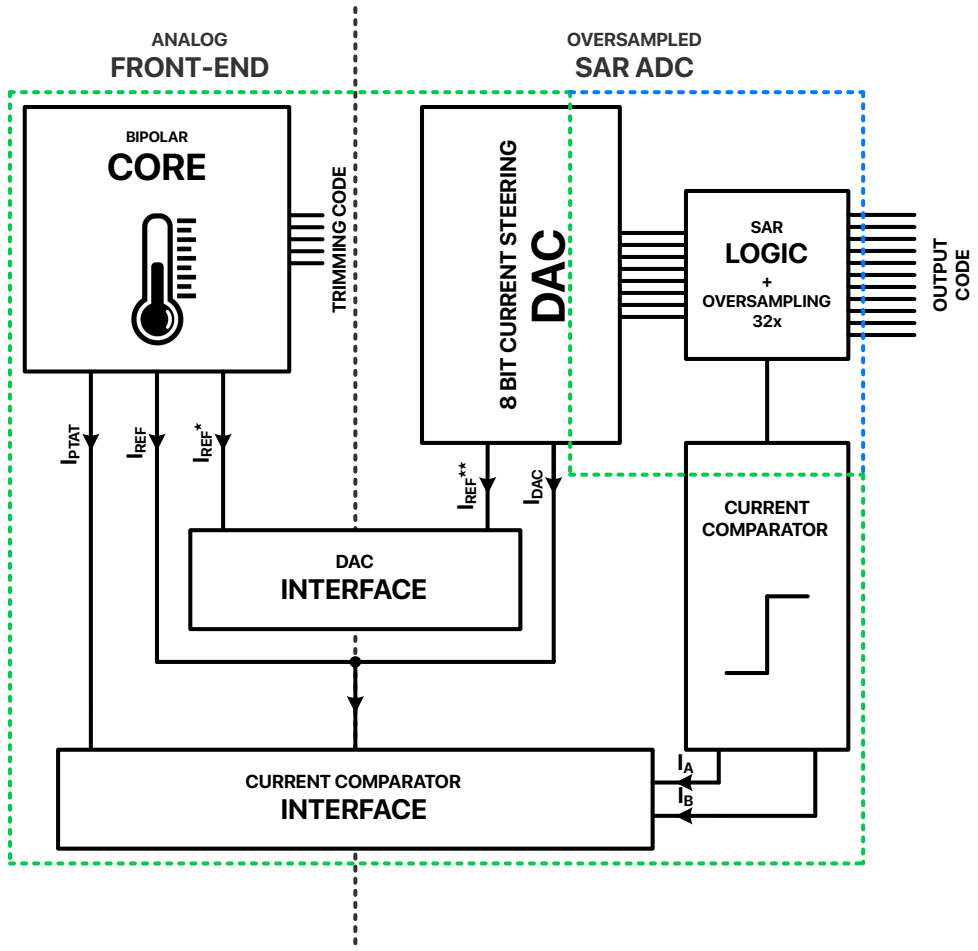


FIGURE 3.1: *mas fuerte* TDC block diagram.

Two dedicated interface circuits, which are basically n-type current mirrors, connect the AFE circuit to the ADC. The main block of the AFE circuit is the bipolar core, which is responsible for the generation of all the signals needed for the temperature-to-digital conversion: a PTAT signal, which contains the information to be converted, and two differently weighted replicas of a reference signal, with respect to which the A/D conversion is carried out. The ADC consists of an 8-bit current steering DAC, a current comparator and a SAR logic circuit, whose output code is decimated to achieve the desired resolution. The majority of the blocks process signals in the current domain (green frame), while just the logic part (blue frame) operates in the voltage domain.

3.2 Bipolar Core

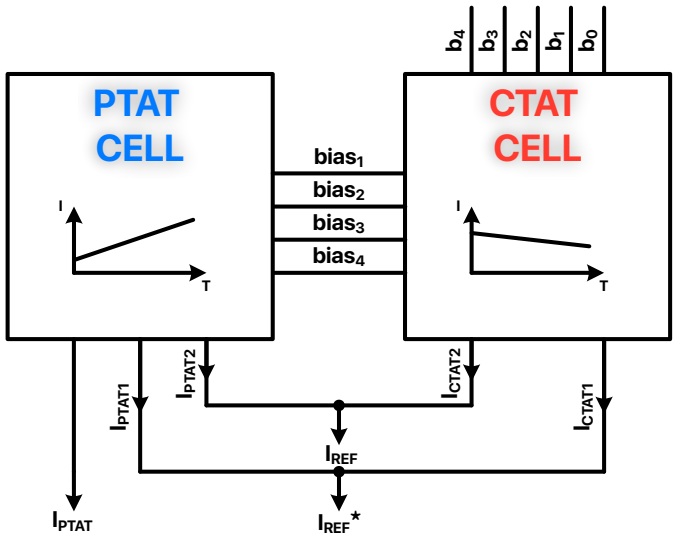


FIGURE 3.2: Conceptual block diagram of the bipolar core circuit.

Fig. 3.2 shows the conceptual block diagram of the bipolar core circuit; it is composed of two cells called *PTAT Cell* and *CTAT Cell*, respectively. The first provides three replicas (I_{PTAT}, I_{PTAT1}, I_{PTAT2}) of a PTAT current, while the second provides two replicas (I_{CTAT1}, I_{CTAT2}) of a CTAT current. These two cells share four bias voltages which are generated within the *PTAT Cell* and are used to drive the *CTAT Cell*. This configuration gives rise to two main advantages: at first, the static start-up circuit (not shown, [88]) used to wake the *PTAT Cell* up, automatically brings also the *CTAT Cell* to the desired operating condition and then, being the temperature measurement implemented in the *mas fuerte* chip of ratiometric nature as will be clearer in the next Section, it ensures a better robustness to process spread of its output code as the variations affecting the *PTAT Cell* are tracked by the *CTAT* one. In addition, as will be explained in Section 3.4, 5 trimming bits are provided as input to the *CTAT Cell* to perform the TDC calibration.

Fig. 3.3 shows the complete schematic diagram of the bipolar core. It can be noticed that both the *PTAT Cell* and *CTAT Cell* are NPN-based; the choice of employing BJTs as temperature sensing elements has been done as they offer better linearity and to achieve the 2 % inaccuracy target with more ease and adequate power consumption with respect to the sensing alternatives presented in Chapter 2.

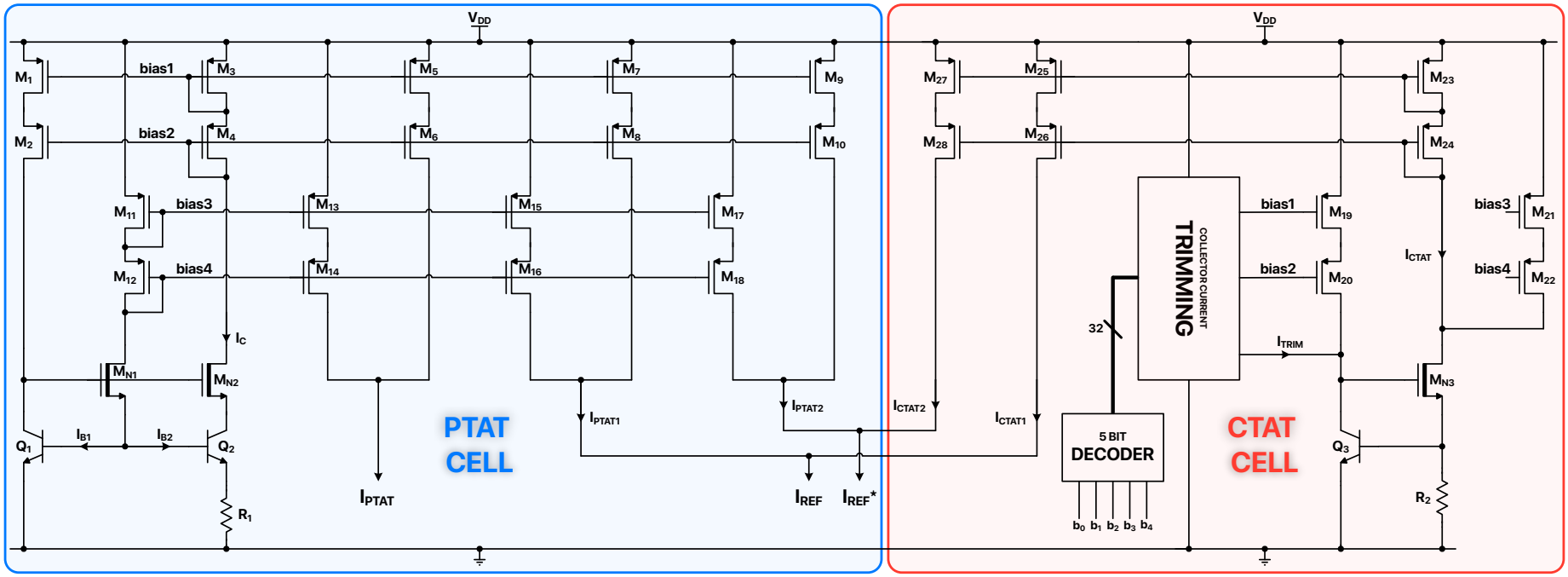


FIGURE 3.3: Schematic diagram of the bipolar core circuit.

Transistors Q_1 and Q_2 have been designed with a $1:8$ emitter area ratio, implying that the current flowing into R_1 is PTAT according to (1.9). The value of the β factor of the bipolar transistors available within the adopted technology is quite poor and lies between 6 and 7. This makes a base current recovery mechanism necessary, considering that the linearity over temperature of the $\Delta V_{BE}/R_1$ signal degrades significantly at the collector, due to the thermal behavior of the base current and to its relative weight. Therefore, a reconstruction scheme has been implemented to make a replica of the emitter current of Q_2 available to be processed. The native transistors M_{N1} and M_{N2} have been used as current buffers and to bias the collectors of both Q_1 and Q_2 at the same voltage. Transistor M_{N1} senses the sum of I_{B1} and I_{B2}, while M_{N2} senses I_C. In both cases, a cascode structure mirrors these contributions, which are then recombined at the output with a proper scaling factor (α), according to

$$I_{PTAT} = \alpha I_C + \frac{\alpha}{2}\left(I_{B1} + I_{B2}\right), \tag{3.1}$$

where the additional scaling factor $1/2$ for the second term has been selected to implement the average of I_{B1} and I_{B2}. Consequently, the analytical expression of the signal containing the temperature information to be converted is well approximated by

$$I_{PTAT} = \alpha \cdot \frac{\Delta V_{BE}}{R_1}. \tag{3.2}$$

The same approach has been adopted also for the generation of I_{PTAT1} and I_{PTAT2}, which are replicas of I_{PTAT}, needed for the generation of the reference currents for the ADC.

Current I_C is also mirrored (M_3-M_4/M_{19}-M_{20}) to bias Q_3, the NPN transistor on which the *CTAT Cell* is based. In addition to this, a 5-bit trimming structure has been implemented to make this biasing current programmable, according to the idea presented in Section 3.4. Moreover, the same base current recovery contribution discussed above is mirrored (M_{11}-M_{12}/M_{21}-M_{22}) and injected into the drain of M_{N3}, to make current I_{CTAT} equal to V_{BE}/R_2. Two replicas of I_{CTAT} (I_{CTAT1} and I_{CTAT2}) are obtained by means of two additional cascode current mirrors and summed to the corresponding PTAT signals, to obtain the two reference signals (I_{REF} and $I^{\star}_{REF}$) required for the temperature-to-digital conversion.

$$I_{REF} = \beta \cdot \frac{\Delta V_{BE}}{R_1} + \gamma \cdot \frac{V_{BE}}{R_2}, \tag{3.3}$$

$$I^{\star}_{REF} = \frac{\beta}{k_1} \cdot \frac{\Delta V_{BE}}{R_1} + \frac{\gamma}{k_1} \cdot \frac{V_{BE}}{R_2}, \tag{3.4}$$

where β and γ are the scaling factors selected to implement the desired I_{REF} and $I^{\star}_{REF}$ temperature dependence (shown in the next Section) and where the attenuation factor k_1 present in (3.4) has been designed to reduce the power consumed by the DAC interface. (3.5) reports the implementative equations of the scaling factors at stake.

$$\begin{cases} \alpha = \dfrac{(W/L)_5}{(W/L)_3} = 2 \cdot \dfrac{(W/L)_{13}}{(W/L)_{11}} \\ \beta = \dfrac{(W/L)_7}{(W/L)_3} \\ \gamma = \dfrac{(W/L)_{25}}{(W/L)_{23}} \\ k_1 = \dfrac{(W/L)_7}{(W/L)_9} = \dfrac{(W/L)_{25}}{(W/L)_{27}} \end{cases} \tag{3.5}$$

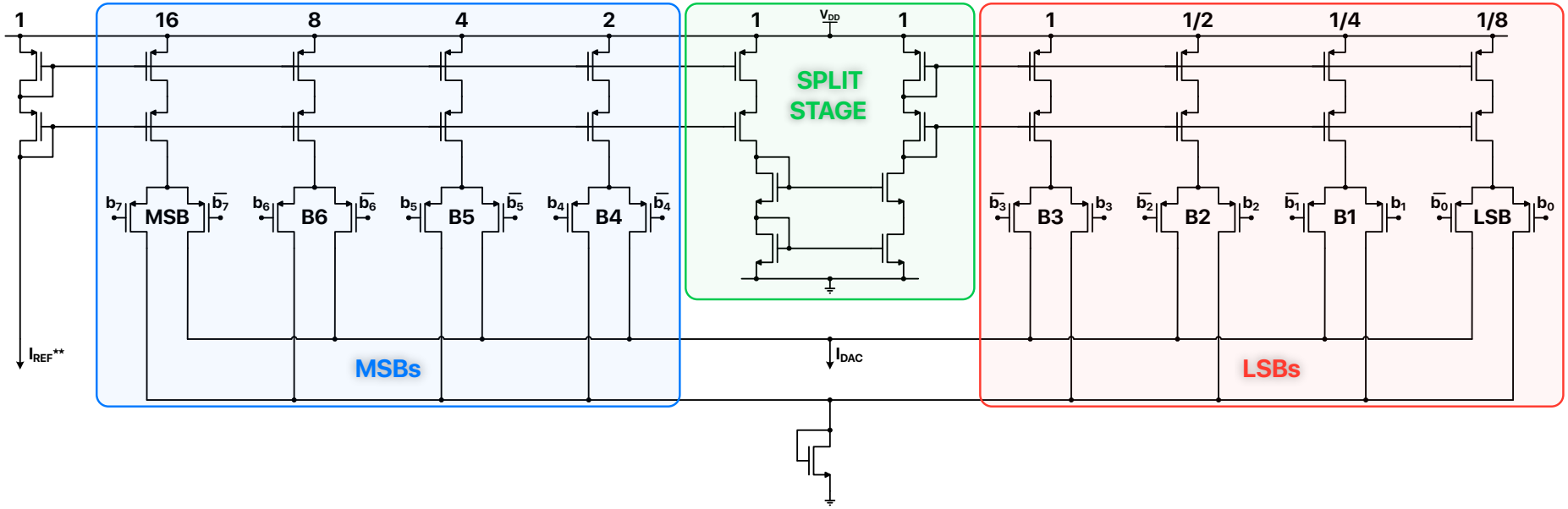


FIGURE 3.4: Schematic diagram of the pMOS cascode current-steering DAC with split stage.

3.3 Temperature-to-Digital Conversion

Referring to Fig. 3.1, the signals generated by the bipolar core circuit are collected by two interface circuits (DAC interface and current comparator interface), which are basically nMOS current mirrors. Consequently, respectively according to (3.6) and to (3.7), $I^{\star\star}_{REF}$ is a $1/k_2$-scaled version of $I^{\star}_{REF}$ while I_A and I_B are η-scaled replicas of I_{PTAT} and $I_{REF} + I_{DAC}$, respectively, I_{DAC} being the DAC output current.

$$I^{\star\star}_{REF} = \frac{I^{\star}_{REF}}{k_2} \tag{3.6}$$

$$\begin{cases} I_A = \eta \cdot I_{PTAT} \\ I_B = \eta \cdot (I_{REF} + I_{DAC}) \end{cases} \tag{3.7}$$

Current $I^{\star\star}_{REF}$ is provided as reference to a pMOS 8-bit cascode current steering DAC, whose schematic diagram is shown in Fig. 3.4, in which every branch is marked with its mirroring factor with respect to the reference. This circuit is controlled by the binary code provided by the SAR logic: depending on the configuration of $(b_0, b_1, \cdots, b_7)$, a larger or smaller replica of $I^{\star\star}_{REF}$ is provided as output current (I_{DAC}), while a smaller or larger replica is absorbed by a diode connected transistor. To optimize the area of the circuit and the matching among the branches corresponding to the different binary weights, this mechanism has been implemented with the three sections highlighted in Fig. 3.4. The *Split Stage* block has been introduced to obtain a size restoration passing from the *MSBs* to the *LSBs* section. The maximum required mirroring factor with this solution (16) is indeed 16 times smaller with respect to a standard 8-bit binary approach (256). Moreover, with this solution, the matching requirements of the DAC have been achieved with more ease. In addition, the DAC, inherently restores the k_1 and k_2 scaling factors implemented within the generation of $I^{\star}_{REF}$ and $I^{\star\star}_{REF}$; indeed, by design,

$$k_1 \cdot k_2 = 32, \tag{3.8}$$

so that the full-scale I_{DAC} current turns out to be equal to the previously discussed I_{REF} current.

The operation of the ADC is based on a successive approximation algorithm run at a 4 MHz clock frequency: the subsequent decisions of the current comparator about the sign of the $I_A - I_B$ difference drive the SAR logic block, which controls the 8-bit current steering DAC. The schematic diagram of the current comparator employed in the *mas fuerte* TDC is shown in Fig. 3.5; it features p-type current inputs accepting the I_A and I_B currents. It is composed by a reset switch driven by the ϕ_1 signal, four complementary switches pairs driven by the ϕ_2 signal, two diode-connected pMOS transistors, a pMOS latched pair, an nMOS latched one and a set-reset latch at the output; its operation is structured in three phases (A, B, C), resulting from the disoverlapped rising edge of ϕ_1 with respect to the falling edge of ϕ_2 according to the waveforms of Fig. 3.6.
During phase A, which lasts 115 ns, the reset switch is on, it forces $V_{LPL} = V_{RPL}$ while currents I_A and I_B are absorbed by the two sides of the pMOS latched pair which stays balanced; the nMOS latched pair is pulled to ground with $V_{LNL} = V_{RNL} = 0$. As soon as phase B begins, since ϕ_1 gets high, the pMOS latched pair is free to unbalance depending on which of I_A and I_B is more instense: if $I_A > I_B$, V_{LPL} falls while V_{RPL} moves towards V_{DD}, viceversa if $I_A < I_B$. After 25 ns, when the direction of V_{LPL} and V_{RPL} is well defined, phase B gives way to phase C, which lasts for the remaining 110 ns of the comparison cycle.

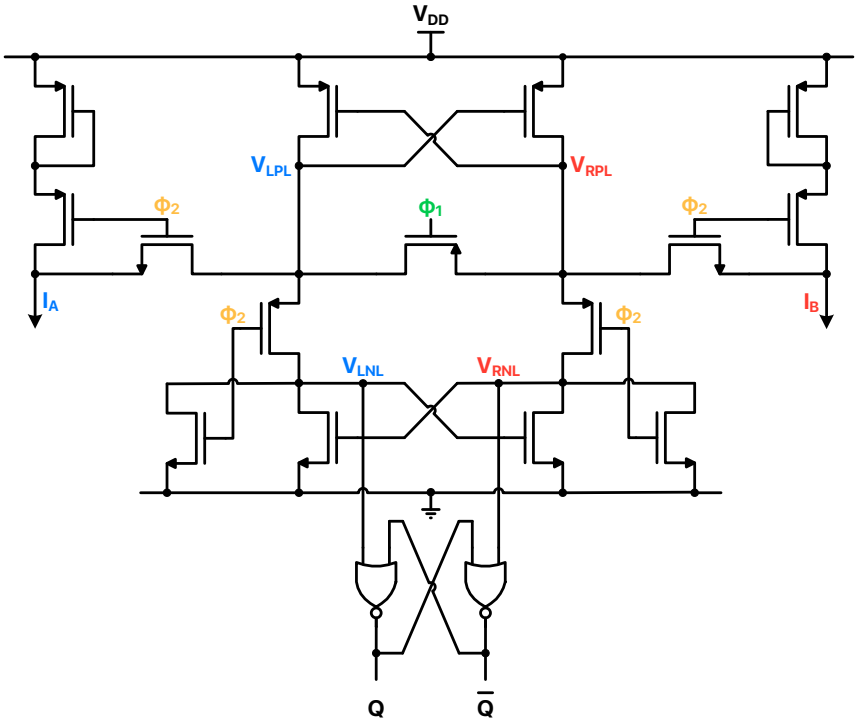


FIGURE 3.5: Schematic diagram of the current comparator.

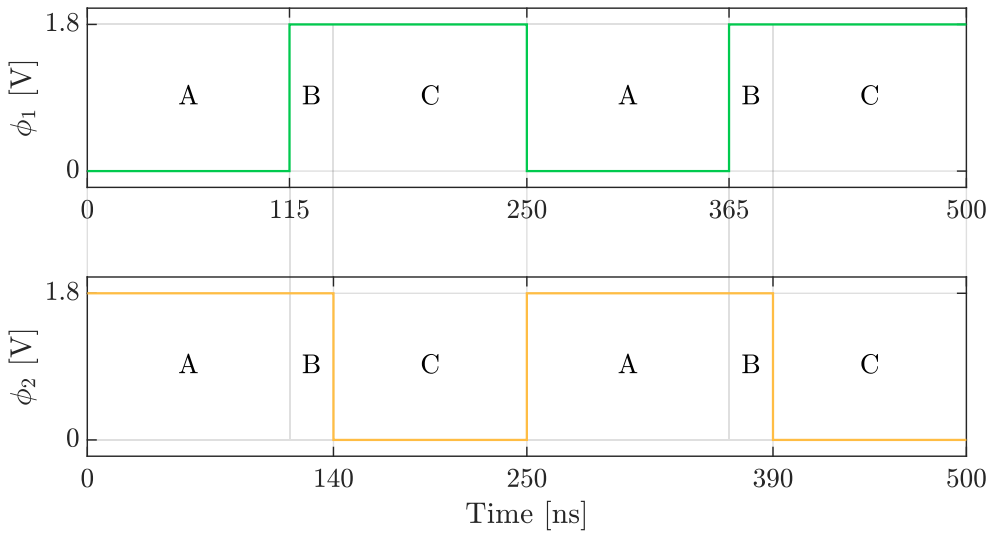


FIGURE 3.6: ϕ_1 and ϕ_2 timing diagrams.

At this point, as ϕ_2 turns low, currents I_A and I_B are deviated to the diode-connected pMOS transistors to avoid their influence on the decision transfer from the pMOS latched pair to the nMOS one which, implementing an additional positive-feedback gain stage, squares it at nodes V_{LNL} and V_{RNL}; the information about the sign of $I_A - I_B$ is now available at these nodes and is finally processed by a simple set-reset latch which has the task of keeping the comparator's decision stored also during phase A and B of the next cycle and updating it only at the occurence of phase C.

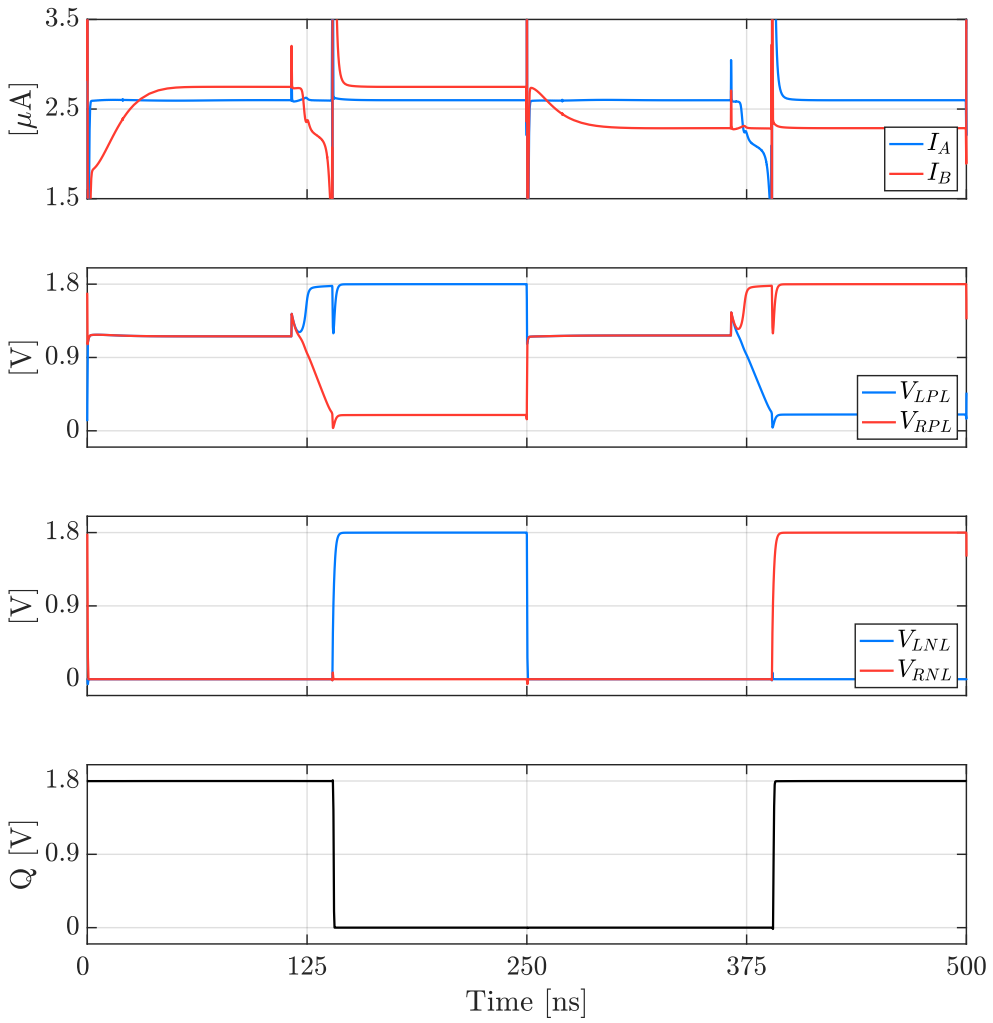


FIGURE 3.7: Waveforms of the main signals of the current comparator (simulation results).

Fig. 3.7 reports some transient analysis results of the current comparator simulated at room temperature (27 °C), confirming the previously described behaviour. It is important to specify that the output branches of the current comparator interface have been designed to be identical in order to avoid a detrimental systematic offset within the comparator itself that may have compromised its proper operation.

Referring again to Fig. 3.1, Fig. 3.8 shows I_{PTAT} and $I_{REF} + I_{DAC}$ as a function of the temperature in the all-zeros DAC input condition (left) and in the all-ones one (right); taking (3.8) and Fig. 3.4 into account, $I_{DAC}(00) = 0$ while $I_{DAC}(FF) = 255/256 \cdot I_{REF}$. It can be noticed that $I_{REF} + I_{DAC}$, with respect to which the temperature-to-digital conversion is carried out, is not a ZTC signal but exhibits a slight positive slope; this feature has purposely been designed in order to improve the linearity of the TDC output according to [89]. In addition, comparing the room temperature value of the I_{PTAT} line of Fig. 3.8 with the I_A waveform of the first strip of Fig. 3.7, observant readers can derive that the η parameter introduced in (3.7) has been selected equal to $1/2$.

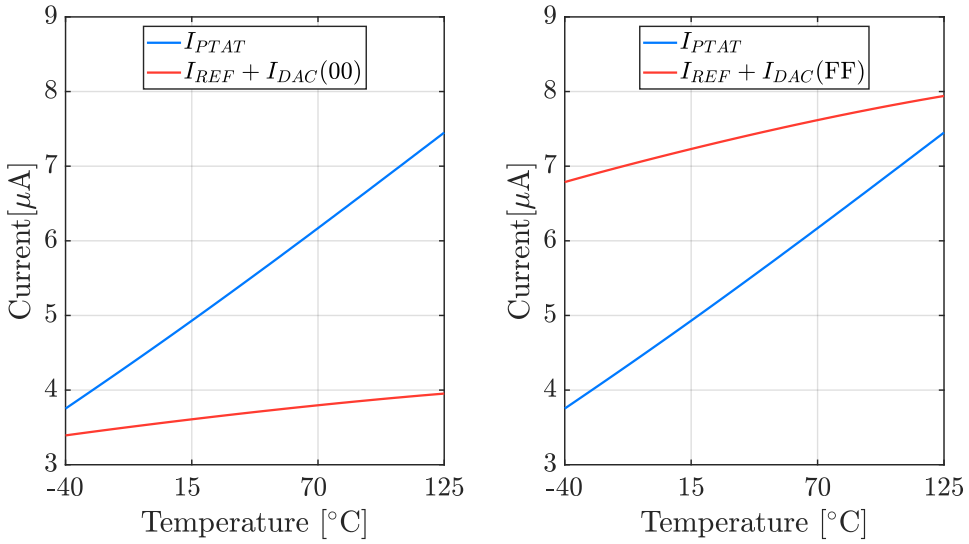


FIGURE 3.8: Temperature characteristics of I_{PTAT} and $I_{REF} + I_{DAC}$ at the two extremes of the DAC input range (simulation results).

As introduced before, the subsequent decisions of the current comparator determine the input code of the DAC according to a SAR algorithm; it is iterated on for 8 clock cycles as shown in Fig. 3.9, resulting in 8-bit digital codes generated in 2 µs. The bits obtained with this procedure, in fact, make up digital words that track the PTAT input signal downshifted by I_{REF}. Consequently, the normalized TDC digital output (μ) depends on the ratio between $I_{PTAT} - I_{REF}$ and the full-scale DAC current which is nothing but I_{REF} again according to (3.8). Recalling (3.2) and (3.3),

$$\mu = \frac{I_{PTAT} - I_{REF}}{I_{REF}} = \frac{I_{PTAT}}{I_{REF}} - 1 = \frac{\alpha \cdot \frac{\Delta V_{BE}}{R_1}}{\beta \cdot \frac{\Delta V_{BE}}{R_1} + \gamma \cdot \frac{V_{BE}}{R_2}} - 1. \tag{3.9}$$

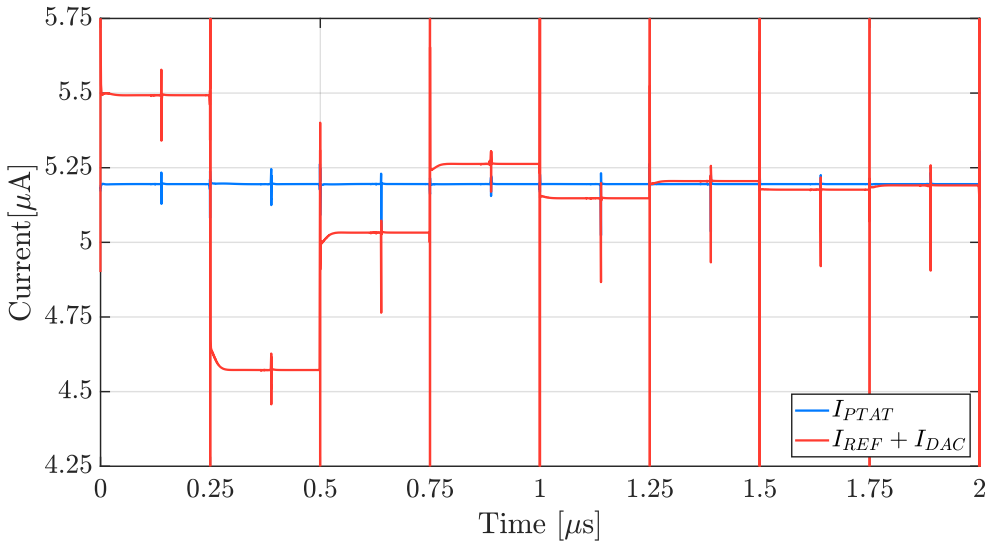


FIGURE 3.9: SAR algorithm on I_{PTAT} and $I_{REF} + I_{DAC}$ (simulation results).

The ADC output binary codes (D_{OUT}) are proportional to μ:

$$D_{OUT} \propto \mu, \tag{3.10}$$

where the proportionality factor depends on the number of bits (in this case it is given by $2^8 - 1 = 255$). This is fully confirmed by Fig. 3.10 where the TDC temperature characteristic is shown. The pre-conversion computed D_{OUT} (blue curve) is compared with the actual ADC output code (red curve) as a function of the temperature; a matched behaviour is clearly appreciable. Moreover, it can be noticed that the conversion range is not exactly equal to the $-40\,^{\circ}\mathrm{C}$ to $125\,^{\circ}\mathrm{C}$ one defined in the specifications but it is a little bit wider: it exhibits some margin both at the low end and at the high one. This design choice has been made because, as will be clearer in Section 3.7, mismatch effects and process variations cause offset and gain errors to the temperature characteristic and, moving it, may saturate the ADC output; for this reason the nominal conversion range has been designed to be from $-55\,^{\circ}\mathrm{C}$ to $140\,^{\circ}\mathrm{C}$.

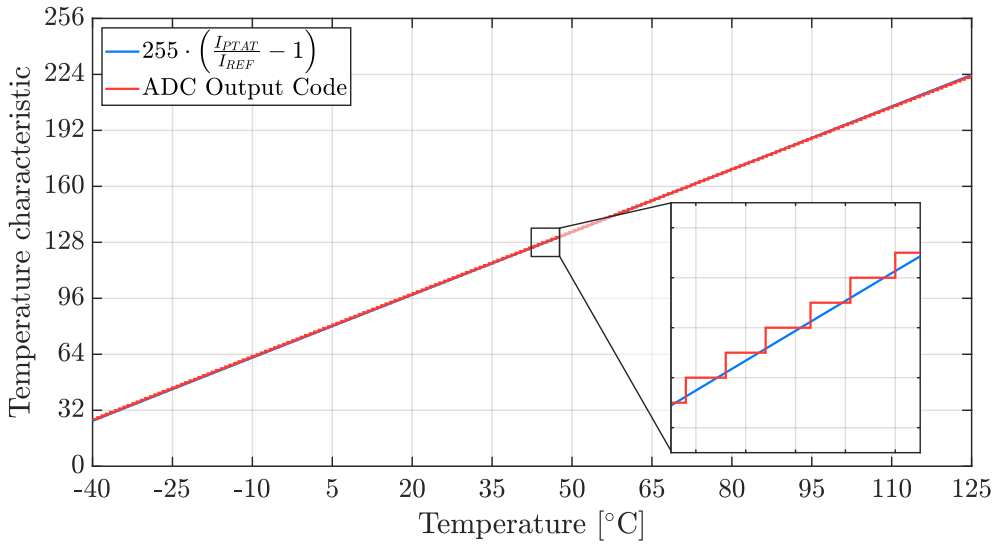


FIGURE 3.10: Simulated TDC temperature characteristics: pre-conversion (blue) and post-conversion (red).

According to the described temperature-to-digital conversion process, the TDC resolution is equal to 8 bits which correspond to about 762 mK; since this value does not meet the design specifications asking for a better than 200 mK resolution, an oversampling procedure has been introduced at the output of the TDC (as indicated in the block diagram of Fig. 3.1). This approach, which requires the quantity to be processed to exhibit some variability, has been possible thanks to the presence of electronic noise in the TDC; to support this, Fig. 3.11 shows the result of a noise transient simulation which has been carried out taking the same signals of Fig. 3.9 into account. It can be noticed that the first decisions of the comparator are not affected by the noise presence and, indeed, the SAR algorithm runs exactly as in Fig. 3.9; the last decisions, instead, are basically random as the comparator is no longer able to discriminate between I_{PTAT} and $I_{REF} + I_{DAC}$. This effect results in output codes affected by a certain degree of uncertainty even considering a fixed temperature and this allows to implement an oversampling procedure with the goal of improving the TDC resolution. In particular, in the *mas fuerte* TDC, this is done by collecting the results of 32 different 8-bit conversions on which a decimation is carried

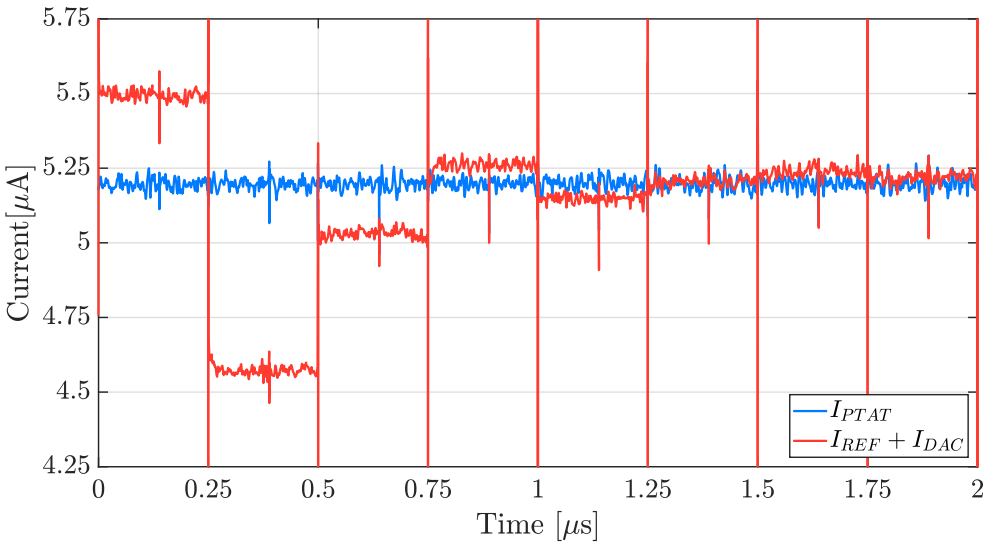


FIGURE 3.11: SAR algorithm on I_{PTAT} and $I_{REF} + I_{DAC}$ with noise enabled (simulation results).

out (the decimation filter has been left off-chip for testing flexibility). The number of collected codes on the basis of which higher resolution digital words are built corresponds to the OSR defined in Chapter 1 and, obviously, gives rise, in this case, to a 32 times longer conversion time (therefore equal to 64 µs). Theoretically, considering only the thermal noise contribution and an ideal decimation filter, this approach should ensure a benefit of a factor $\sqrt{2}$ for every doubling of the OSR to the resolution of the sensor in accordance with:

$$Res_{OS} = \frac{Res_i}{\sqrt{OSR}}, \tag{3.11}$$

where Res_i[1] is the intrinsic resolution while Res_{OS} is the oversampled one. The fact that the presence of noise is a benefit for the sensor's resolution may sound paradoxical at first glance. However it is important to notice that, if there was no variability within the 8-bit codes produced by the TDC, the quantization noise would completely mask the analog temperature value which is instead extractable with averaging or decimation processes as can be done in the proposed TDC.

3.4 Process Spread Trimming

The impact of process variations on the accuracy performance of the TDC was studied in detail and a single temperature trimming circuit was specifically designed for this purpose. This study was structured considering the process corners corresponding to the three kinds of device used for the TDC design:

- MOSFETs - TT, FF, SS, FS, SF
- BJTs - TT, FF, SS
- Resistors - TT, FF, SS

[1] In this case, Res_i does not correspond to the previously introduced 762 mK value because it should include the effect of noise. That value was proposed just for the ideal case but the real one is estimated to be around 900 mK.

The analysis of the resulting 45 combinations was carried out monitoring the spread of the temperature sensitivity of the sensor's output (μ) which is directly related to the system inaccuracy. It immediately became apparent that MOSFETs are the less impactful devices as their are everywhere employed as current mirrors; the process variations equally impact the two mirroring branches without producing any effect on the current scaling factor they offer (which indeed is given by the ratio of the MOSFETs' form factor and therefore makes current mirrors substantially immune to process variations). With a special focus on the temperature dependence of BJTs and resistors it is possible to analyze the contribution of their process spread on the sensor's accuracy starting from the μ expression introduced in Section 3.3:

$$\mu(T) = \frac{\alpha \cdot \frac{\Delta V_{BE}(T)}{R_1(T)}}{\beta \cdot \frac{\Delta V_{BE}(T)}{R_1(T)} + \gamma \cdot \frac{V_{BE}(T)}{R_2(T)}} - 1. \tag{3.12}$$

R_2, by design, has been composed by an integer number (n) of modules equal to R_1 to strengthen the R_2/R_1 ratio against temperature and process variations; to a first approximation it can therefore be written that

$$R_2(T) = n \cdot R_1(T), \tag{3.13}$$

where edge effects of the resistors' layout are being neglected.
Combining (3.12) with (3.13) and performing some algebraic manipulation the following expression can be achieved:

$$\mu(T) = \frac{\alpha}{\beta + \frac{\gamma}{n} \cdot \frac{V_{BE}(T)}{\Delta V_{BE}(T)}} - 1, \tag{3.14}$$

where it can be noticed that the only temperature-dependent terms (V_{BE} and ΔV_{BE}) concern BJTs, thus resulting as the main responsibles for the process-depentent temperature inaccuracy of the TDC.
This result is further confirmed by the simulation results reported in Fig. 3.12; the temperature sensitivity of the sensor is reported as a function of the collector current of the CTAT Cell BJT (the choice of this variable will be clearer in a while) for all the 45 considered corners. The clusters of five dots confirm that the impact of MOSFETs is definitely irrelevant; furthermore, it can be seen that, as expected, the larger effect on the sensitivity is due to the BJTs spread, while the resistors impact is limited to the edge effects of their layout.

Let us now focus on BJTs due to their primary relevance in this framework; (1.8) and (1.9) have shown in Chapter 1 the different temperature dependencies of the V_{BE} and ΔV_{BE} voltages. There is a substantial difference in terms of how process-related variations impact on these two voltages of interest: being ΔV_{BE} a signal of differential nature, the effect of the spread of the variables on which it depends is far smaller if compared to the V_{BE} case. Indeed, in equation (1.8) the process process spread of I_C and I_S directly results in a spread of the V_{BE} voltage and of its thermal behaviour while, within equation (1.9), being a and b ratios, the process variations tend to cancel out.
For this reason, a trimming technique that allows to effectively suppress the process spread of the temperature dependence of the V_{BE} voltage (which in this TDC is provided by the CTAT Cell BJT) has been designed. This technique, which, in general, is useful to improve the batch-to-batch inaccuracy of BJT-based temperature processing circuits, is shown to be effective by means of simulations carried out on a trimming structure designed in the same 180-nm CMOS process adopted for the *mas fuerte* chip and, for the

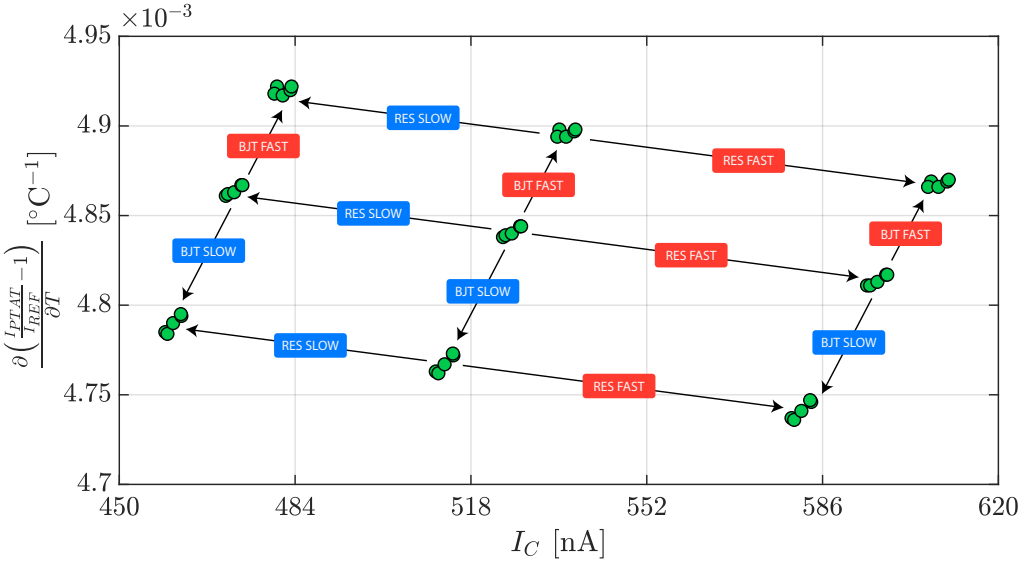


FIGURE 3.12: TDC sensitivity as a function of the collector current of Q_3 (I_C) in the 45 considered process corners.

sake of generality, is described with regard to a simpler but similar circuit with respect to the actual one employed within the CTAT Cell (Fig. 3.3).

The proposed trimming procedure is based on two phases; at first a reading operation is required to get information about the process condition of the sample under examination, then the actual calibration action is digitally implemented to achieve the desired trimming. The following sections explain how both steps are carried out according to the presented technique.

3.4.1 Trimming Reading

Let us consider a diode connected npn transistor (Q_1) biased with a certain collector current (I_C) by means of a mirroring structure as shown in Fig. 3.13 (the same procedure holds also for the dual circuit exploiting a diode connected pnp transistor).

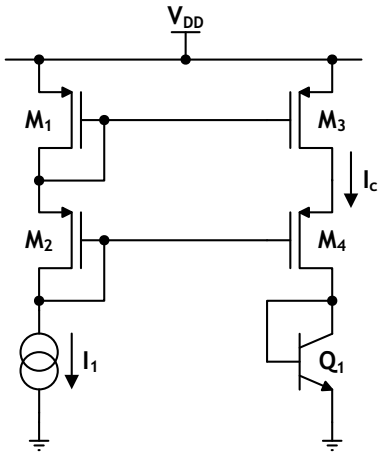


FIGURE 3.13: Basic biasing structure.

As introduced earlier, the crucial parameter to keep under control to get a robust to process variations accuracy performance of a BJT-based temperature processing circuit is the thermal behaviour of the base-to-emitter voltage, specifically its slope with respect to temperature; therefore, to perform a proper calibration of this parameter, the first requirement is to obtain this information from the sample under test. An important consideration is that, intrinsically, this quantity can be computed starting from at least two temperature points but, due to the higher costs of multiple point trimming procedures, a one-point calibration is often a requirement; this constraint, however, does not preclude to succeed in effectively trimming the V_{BE} slope as long as a strongly correlated and measurable at a single temperature parameter is found.

A possibility in this direction is to choose the V_{BE} value at room temperature as the quantity to read to perform the calibration. Fig. 3.14 shows, indeed, that this parameter exhibits a really strong correlation ($r = 0.998$) with the V_{BE} temperature slope for a given collector current; this means that measuring the V_{BE} value at a well controlled temperature, information about its thermal behaviour in a determined process condition is obtained.

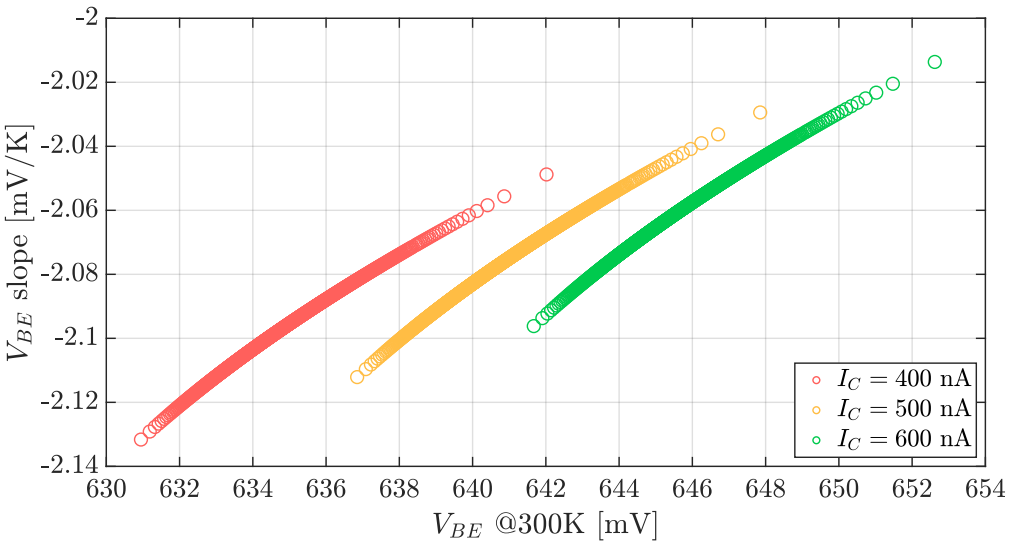


FIGURE 3.14: V_{BE} slope correlation to V_{BE} value @300K (1000 MonteCarlo process runs).

Once the V_{BE} voltage has been measured for the number of available samples, the average value is computed and is used as a target ($V_{BE-TRIM}$ from now on) for the calibration procedure: the correlation shown in Fig. 3.14 grants that measuring the V_{BE} voltage @300K, taking the collector current into account, makes a control on the V_{BE} slope of each sample possible.

3.4.2 Trimming Implementation

The proposed technique to trim the V_{BE} voltage is a current-domain trimming method based on the basic concept presented in [90]; the base-to-emitter voltage of Q_1 is controlled by making its bias current (I_C) programmable. This means that the V_{BE} calibration is achieved passing trough the well-known characteristic of forward-active region

operated bipolar transistors reported in (3.15) where V_T is the thermal voltage.

$$V_{BE} = V_T \cdot \ln\left(\frac{I_C}{I_S}\right) \tag{3.15}$$

Considering the previously introduced target voltage referred to as $V_{BE-TRIM}$, let us call γ_V the proper scaling factor to be applied to I_C to obtain that specific voltage value as shown in (3.16).

$$V_{BE-TRIM} = V_T \cdot \ln\left(\frac{\gamma_V \cdot I_C}{I_S}\right) \tag{3.16}$$

Combining (3.15) with (3.16) and performing some algebraic manipulation a relationship between the scaling factor (γ_V) and the read base-to-emitter voltage (V_{BE}) is derived.

$$\gamma_V = exp\left(\frac{V_{BE-TRIM} - V_{BE}}{V_T}\right) \tag{3.17}$$

This equation tells what the ideal value of γ_V is to bring the measured V_{BE} exactly to the desired $V_{BE-TRIM}$ value.
Thanks to the correlation of Fig. 3.14, there exists a linear transformation (3.18) that allows to pass from γ_V to the proper scaling factor (γ) needed to trim the V_{BE} slope instead of the V_{BE} value @300K.

$$\gamma = A \cdot exp\left(\frac{V_{BE-TRIM} - V_{BE}}{V_T}\right) + B \tag{3.18}$$

The coefficients of this linear transformation can be obtained empirically by means of a preliminary analysis carried out monitoring the behaviour of the V_{BE} slope and checking what the value of the proper scaling factor to trim this quantity is with respect to γ_V; Fig. 3.15 shows the trend of the so computed γ with respect to γ_V and confirms the already mentioned correlation ($r = 0.998$). Once A and B have been identified, the monitoring of the slope is no more needed and each sample can be trimmed at a single

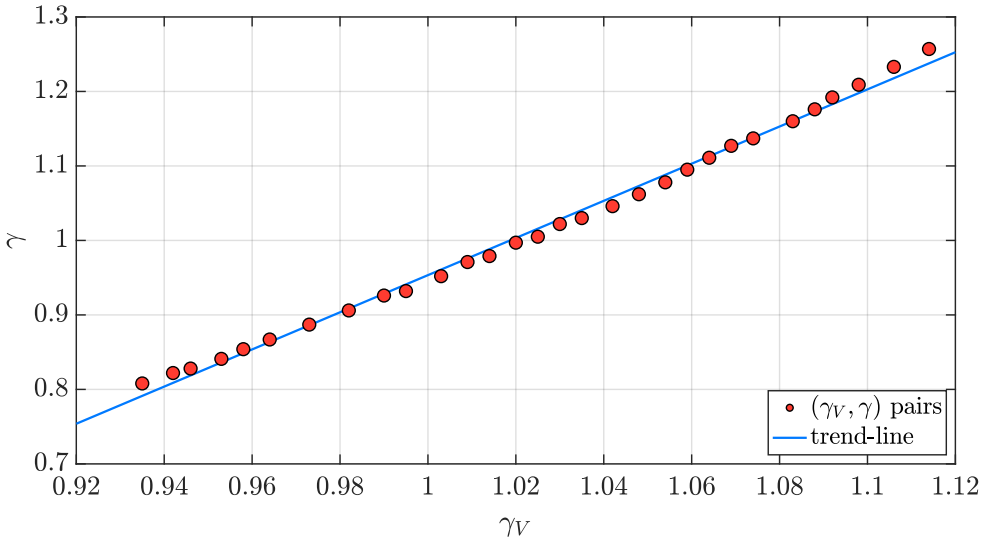


FIGURE 3.15: γ as a function of γ_V.

temperature thanks to the V_{BE} reading.

The idea of the proposed trimming technique is to scale I_C by making the M_1M_2-M_3M_4 mirroring factor of Fig. 3.13 programmable in a way to reproduce the behaviour of the γ function reported in (3.18); this is achieved with a smart modularization and sizing of the transistors which constitute this current mirror according to the scheme of Fig. 3.17 in which M_3 and M_4 of the basic biasing structure have been decomposed into three different sections that will be discussed further. In this way, it is possible to achieve an effective calibration of the V_{BE} temperature slope; a residual error is however still present mainly due to the following reasons:

- the presented technique is based on a digital trimming, thus it has a finite resolution given by the number of dedicated bits.
- the practical implementation of the collector current scaling has to comply with several constraints of discrete nature that derive from the features of the mirroring structure that, actually, prevent the exact implementation of the γ function.

In accordance with these constraints, the concept of the proposed technique is, as visualized in the conceptual representation of Fig. 3.17, to approximate the γ function splitting its V_{BE} range of interest into two sub-intervals, considering a linear fit in each of them and imposing the same value in correspondence of X so that the two resulting straight lines get connected. This approach allows to match the discrete constraints mentioned above but is significantly better than the full range linear fit alternative; Fig. 3.16 shows the approximation error made on the exponential behaviour of γ in the two cases, highlighting the benefit of the adopted solution.

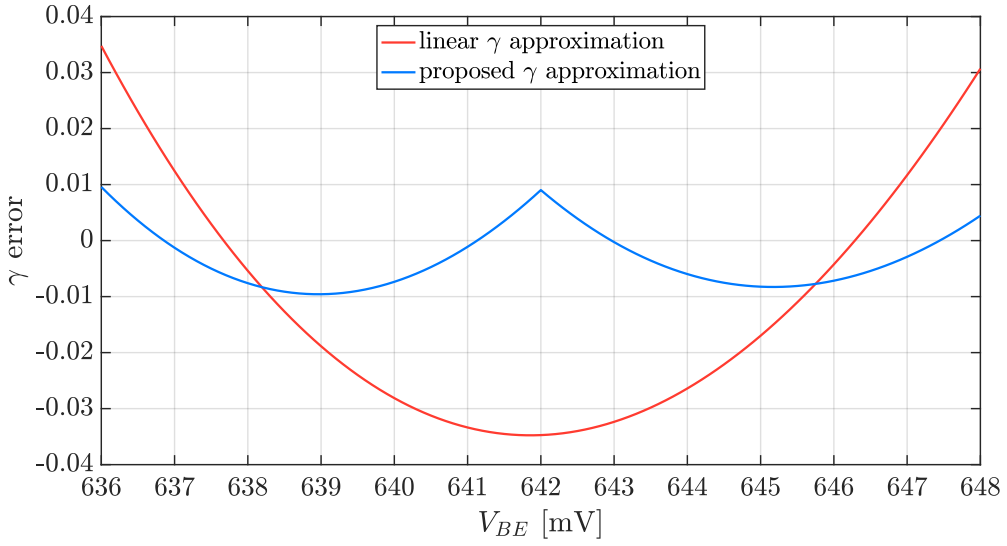


FIGURE 3.16: γ error comparison between linear and proposed approximation.

Let us define a as a parameter proportional to the slope of the γ approximation in the right sub-range and b in the left sub-range; moreover let us suppose to implement the programmability of the current mirror of Fig. 3.13 employing n bits and exploiting exclusively the multiplicity of the involved transistors to obtain a well matched structure whose layout may be designed with a high rate of modularity. Considering the extreme values of γ in the range of interest which will be referred to as γ_{max} and γ_{min}, a proper sizing and programmability of the M_1M_2-M_3M_4 cascode current mirror can be achieved.

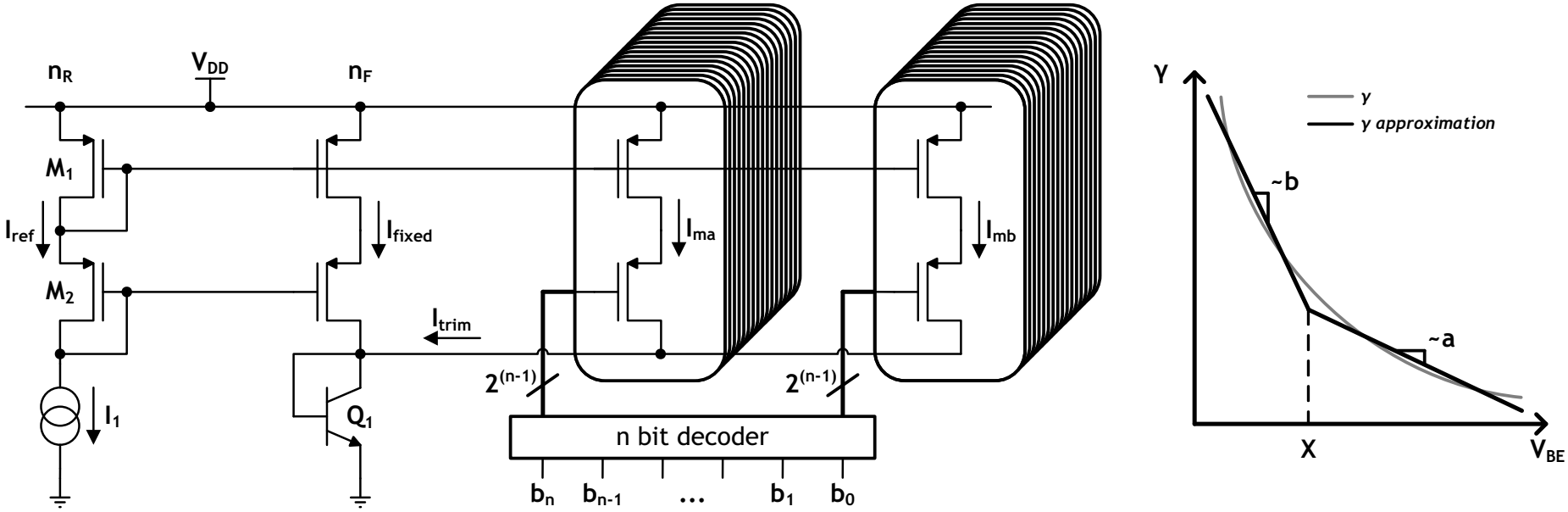


FIGURE 3.17: Proposed trimming structure with conceptual representation of the considered γ approximation.

The idea of the resulting structure which is the core of the proposed trimming technique is depicted in Fig. 3.17; it is composed of four different sets of transistors:

- the reference transistors of multiplicity n_R
- some always-on transistors of multiplicity n_F
- a programmable section of $2^{(n-1)}$ branches with multiplicity proportional to a
- a programmable section of $2^{(n-1)}$ branches with multiplicity proportional to b

The choice of the multiplicity of each branch of the two programmable sections ensures a faithful reproduction of the approximated γ function discussed before. An n-bit decoder controls the activation of each of those branches providing V_{DD} as output to prevent the contribution to I_{TRIM} or providing the proper cascode bias voltage to allow it, depending on the input digital code: the higher the value of the digital word the higher the number of activated branches; in addition to this, crossing the half range of the trimming codes, a slope variation to emulate the exponential behaviour of (3.18) occurs in a proportion of $a : b$. Given the constraints of what γ_{max} and γ_{min} are according to the V_{BE} variability range, it is possible to derive the exact values of n_F and n_R to match the trimming range with the desired γ range as follows.

$$\begin{cases} \gamma_{max} = \dfrac{n_F + a \cdot 2^{(n-1)} + b \cdot 2^{(n-1)}}{n_R} \\ \gamma_{min} = \dfrac{n_F}{n_R} \end{cases} \tag{3.19}$$

These conditions force the desired γ_{max} to correspond to the case when every programmable branch is on and, at the same time, the desired γ_{min} to the all off case.
From (3.19), the expressions for n_F and n_R can be obtained.

$$n_F = \frac{(a+b) \cdot 2^{(n-1)}}{\frac{\gamma_{max}}{\gamma_{min}} - 1} \tag{3.20}$$

$$n_R = \frac{(a+b) \cdot 2^{(n-1)}}{\gamma_{max} - \gamma_{min}} \tag{3.21}$$

With these results, the design procedure of the proposed trimming technique is complete; the next subsection proves the effectiveness of this method showing simulation results obtained with a practical application of the presented idea.

3.4.3 Simulation Results

To show the strength of the proposed technique, a 6-bit version of the scheme presented in Fig. 3.17 has been designed as an example in the same 180-nm CMOS process adopted for the *mas fuerte* chip. The size of every unit transistor of each section of the trimming structure has been selected to be the minimum allowed for the adopted technology and only the multiplicity has been exploited to get a highly modular design; the values chosen for this implementation are reported in Tab. 3.1 and have been determined following all the steps described in the previous Section.

The trimming procedure has been carried out starting from 30 MonteCarlo process runs in which the V_{BE} value @300K has been read; for each of these runs, once the previously introduced $V_{BE-TRIM}$ value has been determined, the ideal γ factor has been computed by means of (3.18). After that, the trimming code corresponding to the closest

I_1	n	a	b	γ_{max}	γ_{min}	n_F	n_R	A	B
500 nA	6	4	5	1.605	0.4375	108	246	2.274	−1.444

TABLE 3.1: Relevant quantities of the proposed design example.

value of gamma made available by the 6-bit exponential-approximated circuit implementation has been selected and applied as input of the decoder (A and B have been derived a priori).
The resulting V_{BE} slope statistic is shown in Fig. 3.18 where the pre-trimming histogram is compared with the post-trimming one. It is evident that a huge difference in terms of standard deviation is present; indeed, once the presented calibration method is carried out, the σ of the considered distribution is reduced by about 90 % proving the effectiveness of the presented technique. Furthermore, this standard deviation can be reduced even more simply increasing the number of dedicated bits at the cost of a higher number of modules; regarding the *mas fuerte* chip, n has been selected equal to 5 according to the relative weight of the process-dependent inaccuracy with respect to the mismatch-dependent one.

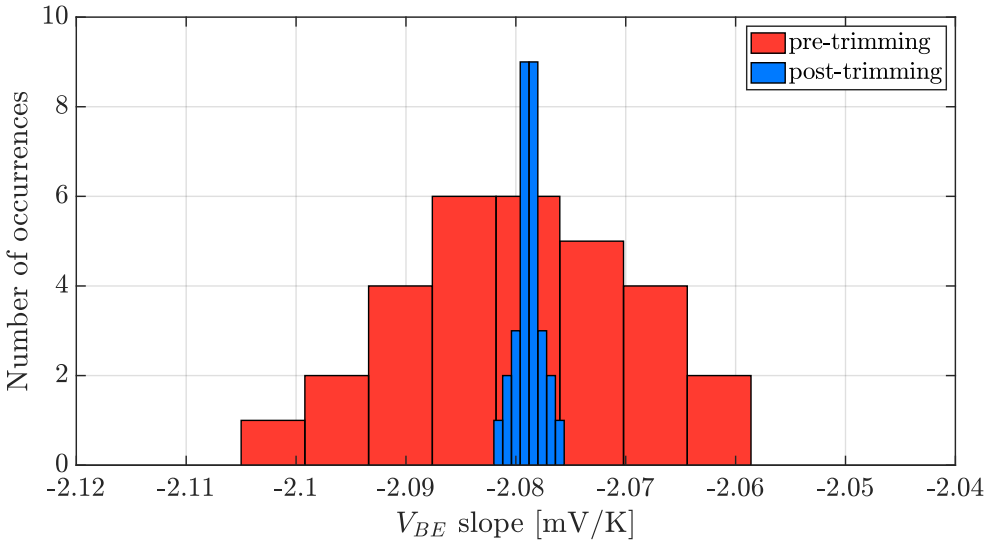


FIGURE 3.18: Comparison between pre-trimming and post-trimming V_{BE} slope spread.

3.5 Layout and Fabrication

The layout of the *mas fuerte* test chip has been carried out with the utmost care in order to achieve the highest degree of compactness in accordance with the silicon area requirement of the project. Fig. 3.19 shows the complete layout of the TDC, the shape of which is a 298 µm x 268 µm rectangle (corresponding to an area of 79 864 µm^2); it can be noticed that every block perfectly fits into to the neighboring ones giving rise to a particularly efficient arrangement. This has been possible taking a whole picture of the design into account throughout the entire layout process instead of focusing on a block at a time; this approach turned out to be crucial for meeting the compactness specification of a smaller than 0.1 mm^2 area.

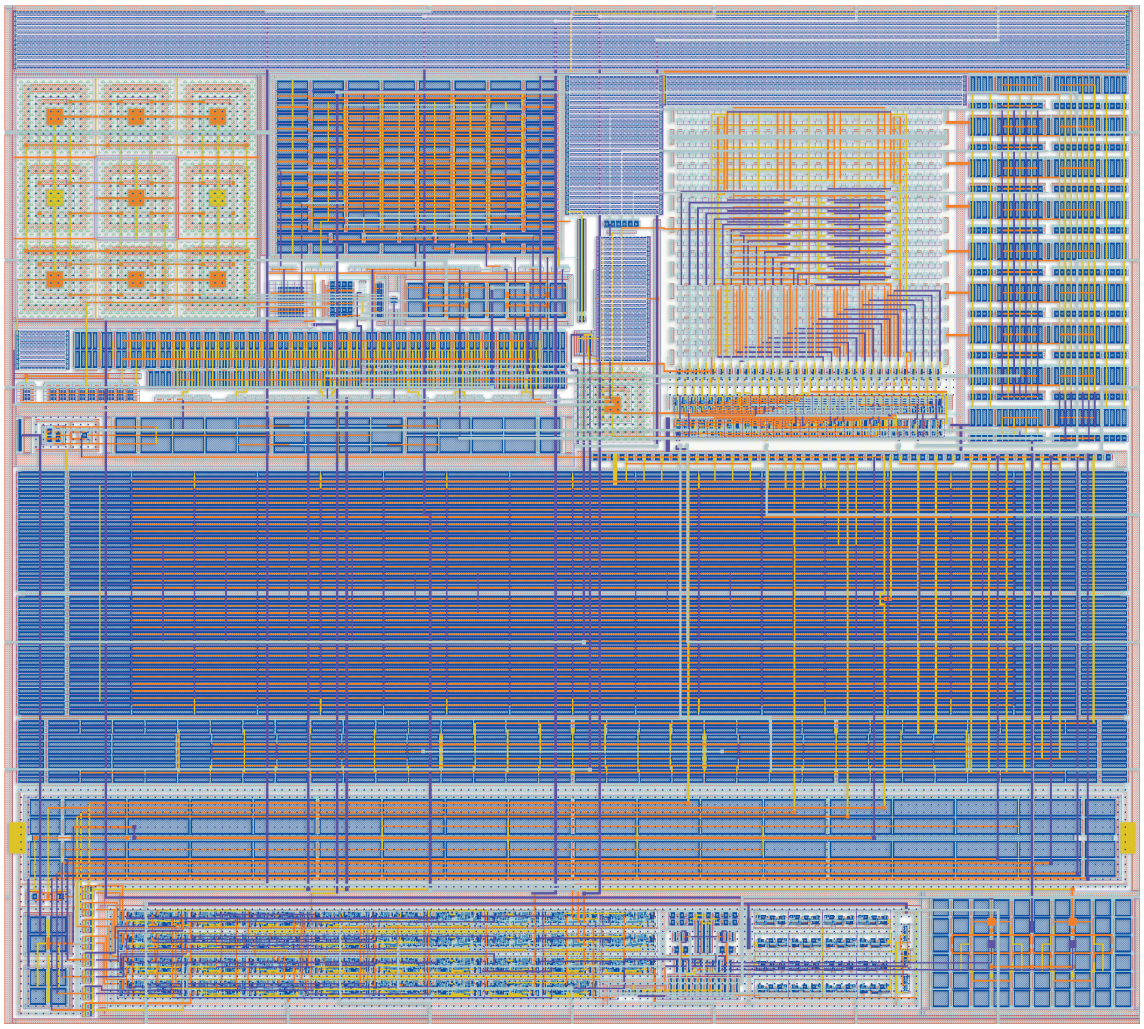


FIGURE 3.19: *mas fuerte* layout.

As anticipated, the device has been fabricated in a standard 180-nm CMOS process. Fig. 3.20 shows the chip micrograph with a magnification of its active area (which corresponds to the one presented in Fig. 3.19) with its breakdown. Including pads, the die area is equal to 1700 µm × 1700 µm which means that it is pad-limited: the free space around the core has been exploited to insert some filtering capacitors connected to the supply voltages[2] that can be seen at the four corners of the active area. The lanes between the capacitors have been reserved for the metal lines connecting the signals of interest to the pads.

Focusing now on the active area breakdown, the arrangement of the main blocks of the TDC can be seen; the static start-up circuit [88] has been placed on top close to the *PTAT Cell* and the *CTAT Cell* according to the discussion of Section 3.2. It can be noticed that, inside the *PTAT Cell*, transistors Q_1 and Q_2 (designed in a 1 : 8 ratio) have been arranged in a common-centroid configuration. Moreover, it is clear that the cascode current steering DAC is the more area consuming block due to the matching constraints of its branches; lastly, the bottom part of the core is occupied by the SAR logic and the current comparator.

[2] As will be mentioned in the next page, the core is supplied by two different voltages: *avdd* for the AFE and *dvdd* for the ADC.

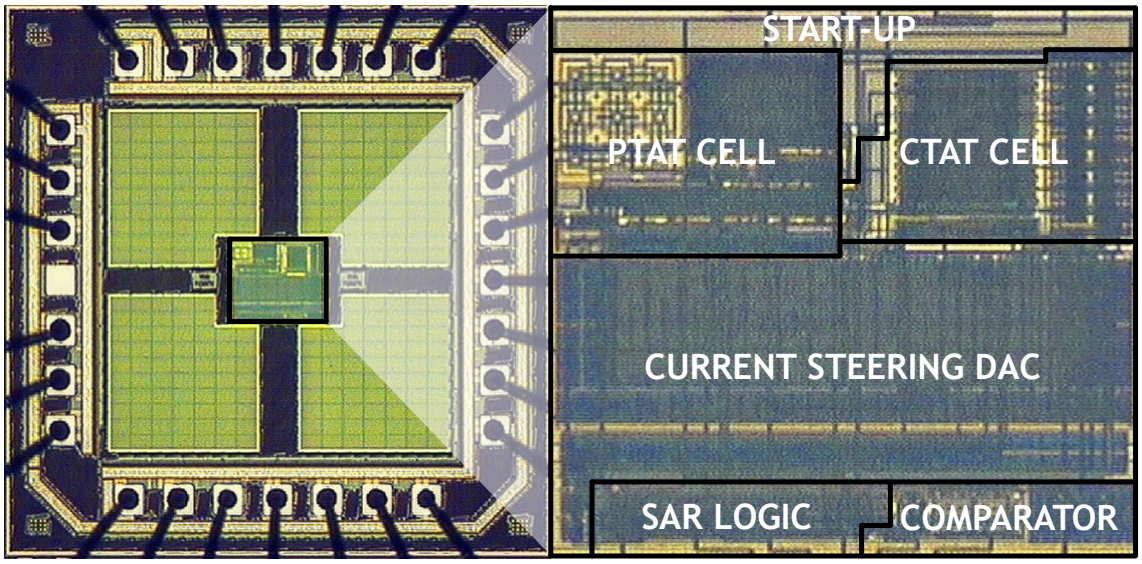


FIGURE 3.20: *mas fuerte* chip micrograph with magnified view of the active area with its breakdown.

The pad ring of the chip has been structured according to a 7x4 square scheme in accordance with the choice of a DIL28 packaging for each sample. Fig. 3.21 shows the pinout diagram of the *mas fuerte* chip. Regarding the supply voltages, there are three different $V_{DD} - V_{SS}$ pairs: *avdd* and *avss* power the AFE, *dvdd* and *dvss* power the ADC while *vddio* and *vssio* are used to supply the pads and the protection circuits and buffers they embed. Four analog outputs are present: I_A and I_B, if enabled, offer replicas of the homonymous signals introduced in Section 3.3 while *base* and *emitter* allow the reading of the V_{BE} of transistor Q_3 for trimming purposes (Section 3.4).
Except for an unused pin (which correspond to the unused center-left pad in Fig. 3.20),

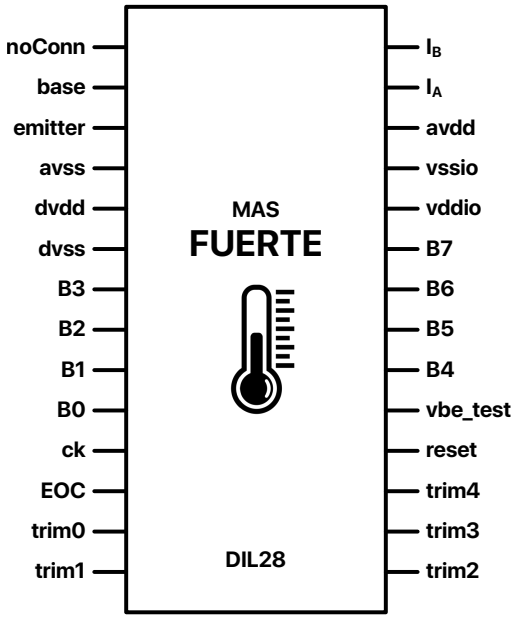


FIGURE 3.21: *mas fuerte* pinout.

the remaining 17 pins are all digital: 8 are inputs while 9 are outputs. The digital inputs include the 5 trimming bits used to calibrate the TDC (*trim*0 to *trim*4), the system clock (*ck*) which is provided from outside, the *reset* signal to control the running of the temperature-to-digital conversion process and the enable pin (*vbe_test*) of the V_{BE} trimming test mode. The digital outputs are the 8 bits generated by the TDC (*B*0 to *B*7) to be processed by the off-chip decimation filter and an end-of-conversion (*EOC*) signal whose falling edge declares the end of the 8-bit conversion.

3.6 Testing Procedure

In order to test the fabricated samples, a printed circuit board (PCB) has been designed and manufactured: its 3D model is illustrated in Fig. 3.22. Its scheme is quite simple; a zero insertion force (ZIF) DIL28 socket is located in the middle (only its footprint is visible in Fig. 3.22) to accomodate and easily replace the device under test (DUT). This component is of primary importance especially for the inaccuracy tests which, being of statistical nature, require the testing of several devices the replacement of which should be immediate. The supply and analog pins of the DUT are connected to some banana connectors housings while for each digital signal a simple pin is present. In addition, the digital inputs are configurable by means of some jumpers, with the exception of the clock signal for which a BNC connector is present (again, only its footprint is visible in Fig. 3.22).

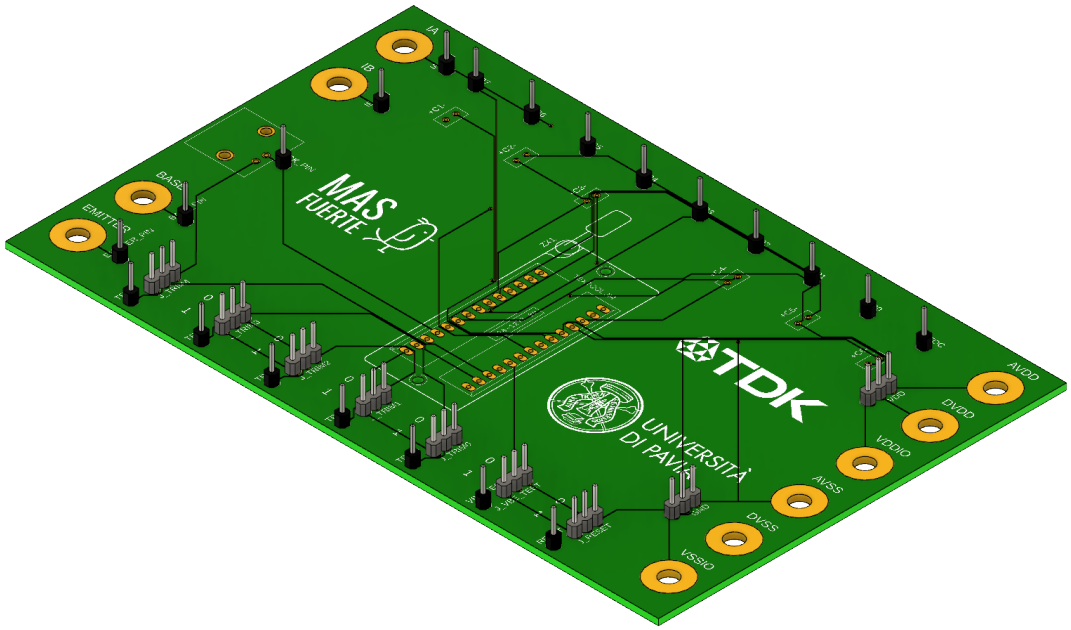


FIGURE 3.22: *mas fuerte* test PCB.

The testing procedure has been automated thanks to the employment of a data acquisition (DAQ) system (Fig. 3.23) controlled by a LabVIEW program specifically developed for the *mas fuerte* chip.

FIGURE 3.23: Data acquisition (DAQ) system employed for the testing of the *mas fuerte* chip.

Fig. 3.24 shows the front panel of the program designed as user interface for the monitoring and the control of the measurements status; it features a *Chip ID* selection knob to distinguish the different samples under test, a *Trimming status* panel showing the configuration of the five calibration bits previously introduced, a thermometer showing the real-time temperature inside the thermal chamber and a panel showing the measured I_A and I_B currents.

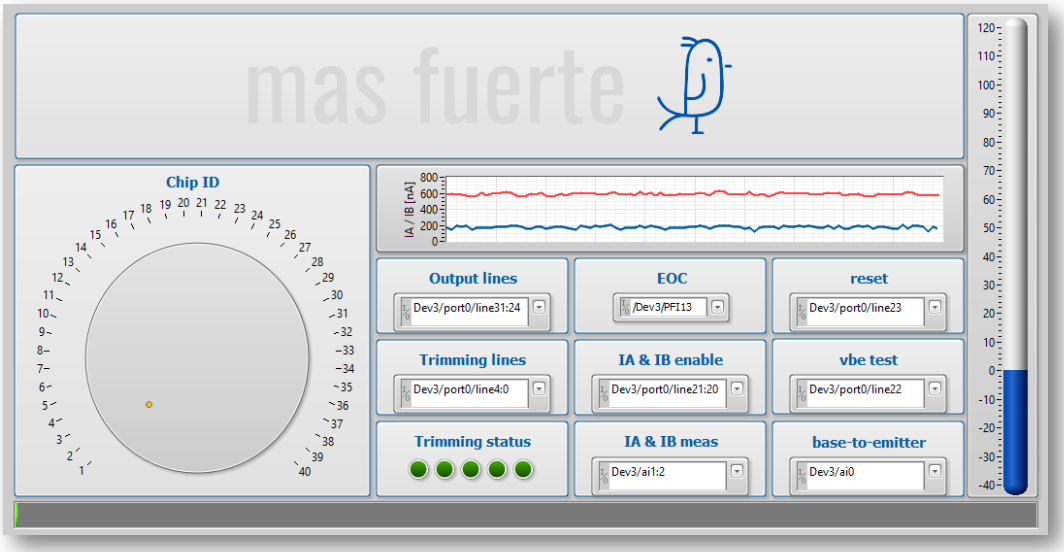


FIGURE 3.24: *mas fuerte* LabView program front panel.

Moreover some panels to properly manage the input/output lines of the DAQ system are present to read/write the right signals of interest: the *Output lines* correspond to the 8 bits generated by the TDC, the *EOC* channel is used to synchronously trigger the reading of a digital sample, the *reset* controls the start and the stop of the temperature-to-digital conversion process while *IA & IB enable* and *vbe test* respectively enable the measurements on the *IA & IB meas* and *base-to-emitter* channels. At the bottom of the panel a progress bar is present to track the waiting time between the achievement of the set-point temperature inside the thermal chamber and the actual start of the measurement process that has been introduced to ensure a proper settling of the silicon temperature; since for this measurement campaign a one-hour waiting time has been selected, the progress bar introduction turned out to be particularly convenient to understand when something interesting would have happened. The LabVIEW code behind the described front panel implements the routine which is conceptually summarized by the diagram of Fig. 3.25.

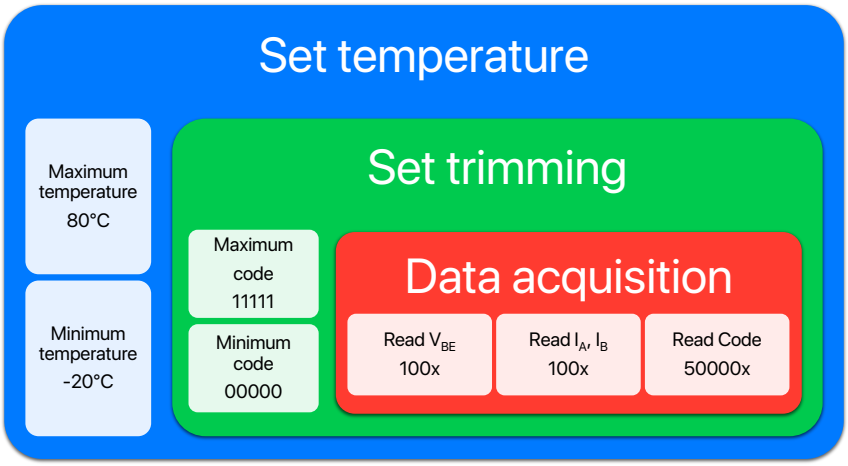


FIGURE 3.25: *mas fuerte* testing routine scheme.

The testing routine carried out on each sample is organized on the basis of three loops that correspond to the shown colored boxes: each operation in an inner box is carried out for each condition present at the upper levels. This means that, the data acquisition task that will be described in a while, is executed for all the 32 possible trimming codes, in turn, also for all the considered temperatures and finally also for each *mas fuerte* chip. Consequently, the global measurement time of the whole campaign can be estimated accornding to

$$t_{global} = n_{chips} \cdot \left(1 + \frac{T_{range}}{T_{step}}\right) \cdot (t_{wait} + 2^{trim_bits} \cdot t_{DAQ}), \tag{3.22}$$

where t_{DAQ} is the data acquisition time, $trim_bits$ is the number of trimming lines, t_{wait} is the waiting time for the settling of the chip temperature, T_{range} is the temperature range, T_{step} is the temperature step size and n_{chips} is the number of samples to be tested. For instance, considering 40 samples, a $-40\,^{\circ}\mathrm{C}$ to $125\,^{\circ}\mathrm{C}$ range, steps of $5\,^{\circ}\mathrm{C}$, a waiting time of 1 h, 5 trimming bits and a T_{DAQ} of 1 s, t_{global} turns out to be equal to almost 1400 hours! For this reason, some choices have been made to reduce the duration of the measurement campaign: considering that the actual range of interest for the application at stake is from $0\,^{\circ}\mathrm{C}$ to $80\,^{\circ}\mathrm{C}$, the temperature range have been shrunk to $-20\,^{\circ}\mathrm{C}$ to $80\,^{\circ}\mathrm{C}$ also taking into account that for higher than $110\,^{\circ}\mathrm{C}$ temperatures, the available cables would have started melting. Then, temperature steps of $10\,^{\circ}\mathrm{C}$ have been chosen in accordance with

the majority of published works in this field and, finally, a total of 20 chips were tested considering the resulting statistical distribution meaningful. The result has been a t_{global} of about 222 hours, still demanding but considerably more convenient. Focusing now on the data acquisition box, three different readings are performed:

- the V_{BE} voltage is read 100 times and its average value is stored since it is needed for the technique presented in Section 3.4.
- by means of simple shunt resistors, the I_A and I_B currents are read 100 times and their average value is stored to monitor if at the AFE levels are as expected.
- 50 000 8-bit digital samples are stored; considering the oversampling procedure described in 3.3, this quantity offers more than 1500 (50000/32) high-resolution samples to employ for the resolution evaluation.

3.7 Measurement Results

As introduced in the previous Section, 20 different samples were characterized in a thermal chamber in which a temperature sweep from −20 °C to 80 °C with steps of 10 °C has been carried out. First of all, the power consumption of the device has been measured; it draws about 13 µA from the *avdd* supply and about 9 µA from the *dvdd* supply; considering that it is clocked at 4 MHz and that both supplies are at 1.8 V, this means that the conversion energy of a digital sample refined with a 32x oversampling process is equal to about 2.5 nJ according to (1.1) and (1.2). This is a definitely good result considering that the primary design requirement is that of a lower than 10 nJ conversion energy. Fig. 3.26 shows the power breakdown among the main blocks of the TDC. The power consumption of the interface circuits has been added to the neighboring blocks, while the SAR logic power consumption has been omitted, considering that its contribution is negligible; in total the device consumes 39.6 µW.

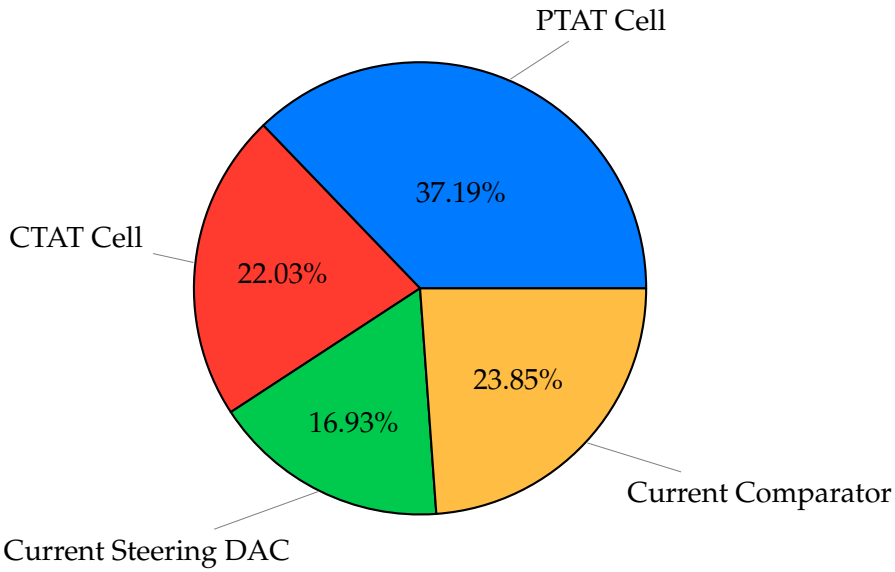


FIGURE 3.26: Power consumption breakdown of the *mas fuerte* TDC.

The measurements have been focused on the evaluation of the inaccuracy and resolution parameters of the TDC and are discussed respectively in Subsection 3.7.1 and 3.7.2.

3.7.1 Inaccuracy

As introduced in Chapter 1, the inaccuracy of a TDC is a statistical measure of its temperature error. Consequently, the starting point for the *mas fuerte* inaccuracy analysis, is the set of twenty temperature characteristics collected according to the testing procedure introduced in the previous Section. Fig. 3.27 (left) shows the untrimmed thermal response of the TDC in the $-20\,^{\circ}\mathrm{C}$ to $80\,^{\circ}\mathrm{C}$ temperature range in which the average output code of 20 different samples is considered; on the right, the correspondent temperature errors[3] with the $\pm 3\sigma$ limits are reported.

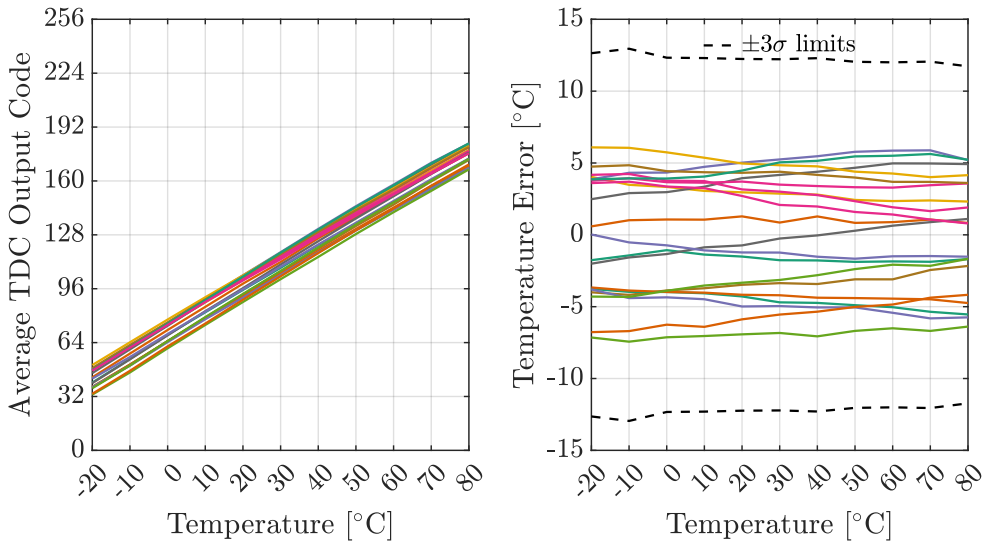


FIGURE 3.27: Measured untrimmed temperature characteristics (left) and correspondent temperature errors (right) of 20 *mas fuerte* chips.

It can be noticed that, due to mismatch effects among the considered samples, a considerable spread exist across the measured characteristics that, consequently, translates into a considerable temperature error. Tab. 3.2 reports the untrimmed inaccuracy summary both with the peak-to-peak evaluation method and with the 3σ one.

Untrimmed Inaccuracy	Absolute	Relative
peak-to-peak	± 6.76 K	13.52%
3σ	± 12.95 K	25.91%

TABLE 3.2: Untrimmed *mas fuerte* inaccuracy summary.

Since this inaccuracy values are somewhat scarce, especially if compared with the design specifications, the introduction of at least one trimming point is substantially mandatory. In this direction, the most straightforward technique is simply to compensate for the offset present among the measured code-vs-temperature curves operating at room temperature ($30\,^{\circ}\mathrm{C}$).
The results achieved with this approach are reported in Fig. 3.28. It can be noticed that a significant compaction occurs to the temperature characteristics; however, the resulting

[3] Temperature errors are obtained as the difference, in the temperature domain, between a target characteristic and the measured one for the considered sample; the target characteristic has been simply obtained as the average of the twenty measured ones.

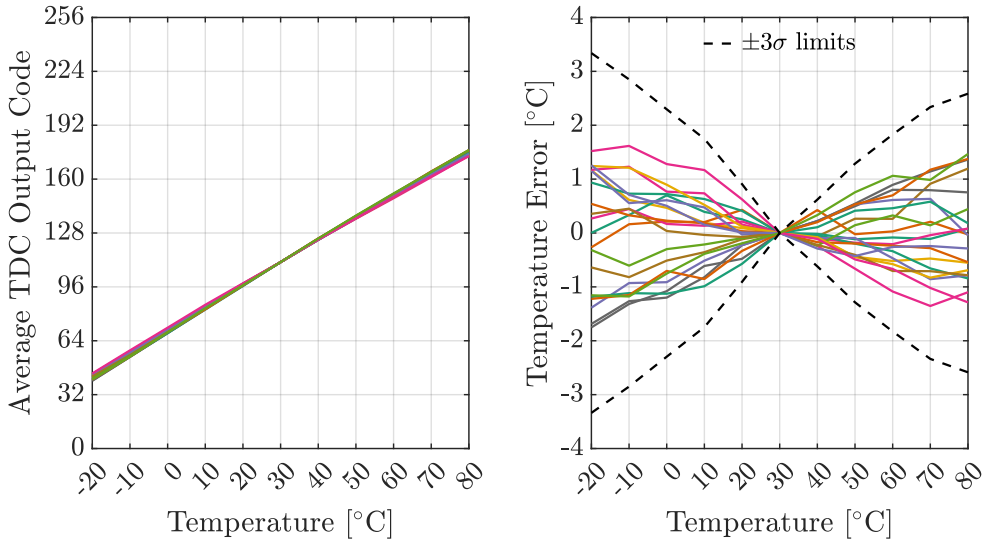


FIGURE 3.28: Measured 1-pt offset compensated temperature characteristics (left) and correspondent temperature errors (right) of 20 *mas fuerte* chips.

inaccuracy values, summarized in Tab. 3.3, do not comply with the sensor's requirements. To further improve the TDC accuracy while keeping a single temperature trimming, the correlation of the trimming technique introduced in Section 3.4 could be exploited.

1-point Offset Compensated Inaccuracy	Absolute	Relative
peak-to-peak	±1.68 K	3.37%
3σ	±3.34 K	6.68%

TABLE 3.3: 1-pt offset compensated *mas fuerte* inaccuracy summary.

Unfortunately, since all the available samples have been fabricated within the same batch, they all are in the same process condition; this means that the inaccuracy of Fig. 3.28 is almost fully dependent on mismatch effects[4] and the method described in Section 3.4 does not apply. Consequently, the only way to get an extra inaccuracy reduction is to introduce a calibration technique based on the information read at an additional temperature; this has been carried out still exploiting the on-chip trimming structure to program the collector current of Q_3 but with a different approach with respect to the previously introduced one. Besides the measurement at room temperature, indeed, the TDCs have been trimmed on the basis of the measurement at the upper bound of the considered temperature range (80 °C); being thus able to derive for each of the measured characteristics its slope with respect to temperature, the best 5-bit code to approach a pre-defined target slope has been selected for each sample.
Fig. 3.29 shows the results obtained with this approach; the compactness of the set of code-vs-temperature curves is clearly further improved as it is also demonstrated by the temperature error chart on the right.
Tab. 3.4 reports the inaccuracy summary with this trimming approach; it can be observed that the relative inaccuracy value is now well below the 2 % target with a peak-to-peak

[4] As will be proven in the next Chapter, the main responsible for this effects is the current-steering DAC.

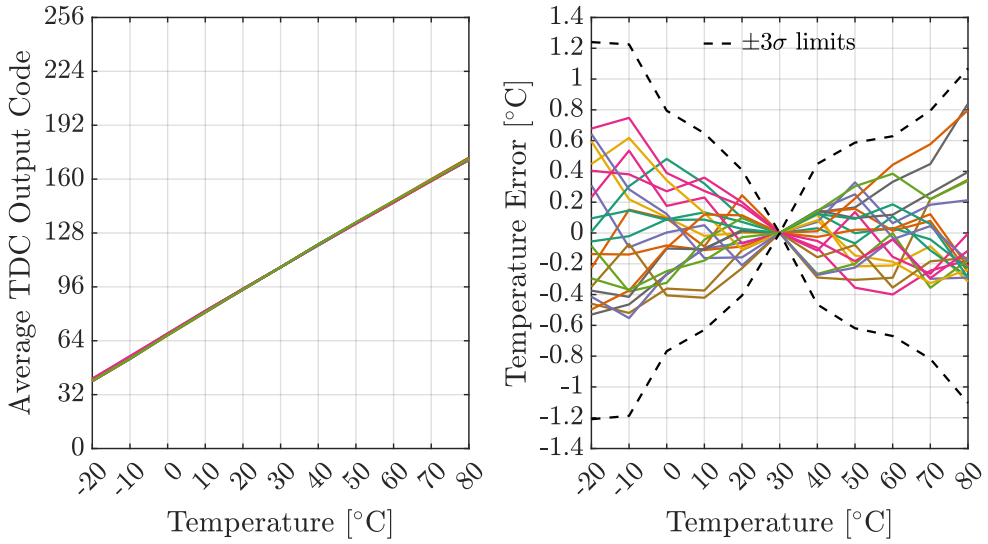


FIGURE 3.29: Measured slope compensated temperature characteristics (left) and correspondent temperature errors (right) of 20 *mas fuerte* chips.

approach. Considering the amount of measured samples, it has not been read too much into the 2.45 % relative inaccuracy achieved with a 3σ approach.

Slope Compensated Inaccuracy	Absolute	Relative
peak-to-peak	±0.7 K	1.39%
3σ	±1.23 K	2.45%

TABLE 3.4: Slope compensated *mas fuerte* inaccuracy summary.

3.7.2 Resolution

To evaluate the *mas fuerte* resolution performance, the 50 000 acquired samples discussed in Section 3.6 have been processed and analyzed at a fixed temperature and for a fixed trimming code[5]. As presented in Section 3.3, the collected samples have been processed by an off-chip decimation filter to study the proposed resolution refining process; considering 32 as the adopted oversampling factor, it was possible to examine more than 1500 refined samples. Since the resolution parameter is a measure of the minimum detectable temperature variation or, from another perspective, it corresponds to the uncertainty of the sensor's output for a fixed temperature, such a high number of samples has made the proposed results particularly reliable. In the case of TDCs dominated by quantization noise, [91] [92] for instance, resolution is simply given by the full-scale temperature range divided by 2^n, being n the number of bits of the temperature-dependent codes generated by the ADC. More generally, actually in the majority of works in this field, resolution is determined by the effect of thermal and 1/f noise rather than by quantization noise! In this situation, which is the case for the device under consideration, it should be evaluated

[5]Some brief analysis on the impact of the temperature and of the trimming configuration have been carried out. Since minimal variations have been observed, the room temperature (30 °C) with mid-range trimming code (10000) results have been considered as exhaustive.

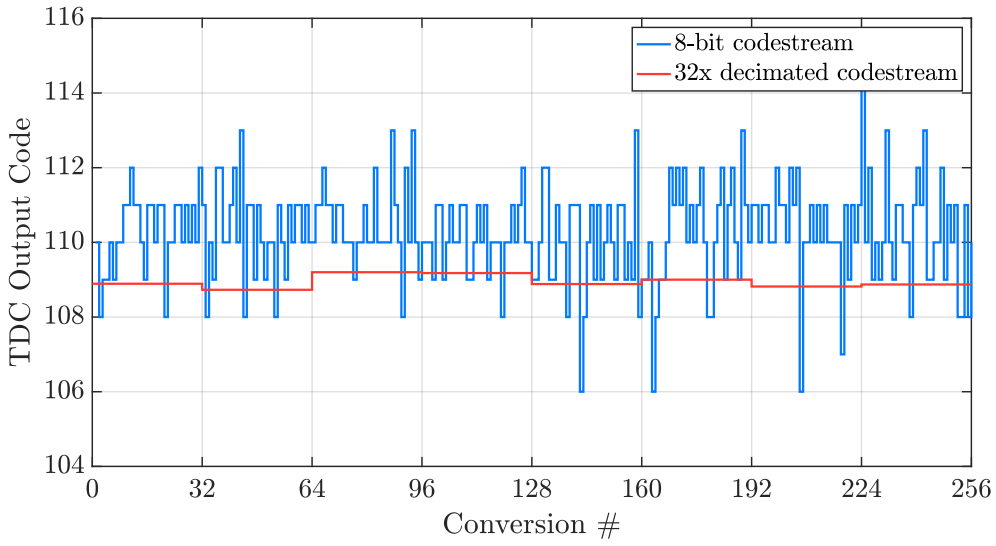


FIGURE 3.30: Measured *mas fuerte* TDC output: 8-bit codestream (blue) and 32x decimated codestream (red).

computing the standard deviation of the TDC's output codestream, thus exctracting an RMS value.

Fig. 3.30 shows the result of 256 8-bit room temperature conversions as an example (blue curve); moreover, the refined codestream achieved by means of a decimation by a factor 32 is superimposed (red curve); the reduced variability of the refined samples is clearly noticeable and confirms the effectiveness of the proposed technique. Taking all 50 000 8-bit conversions into account, their measured non-oversampled RMS resolution turns out to be equal to 902 mK; considering instead all the available refined samples whose complete statistical distribution is shown in Fig. 3.31, their resolution is equal to

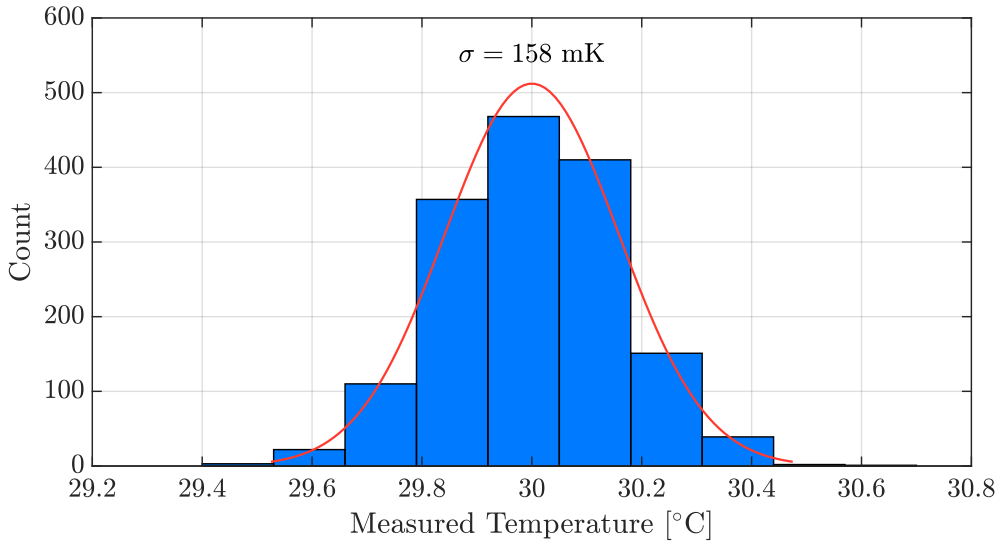


FIGURE 3.31: *mas fuerte* temperature resolution evaluation considering an oversampling factor of 32.

158 mK. This confirms that the proposed technique is well-modeled by (3.11).

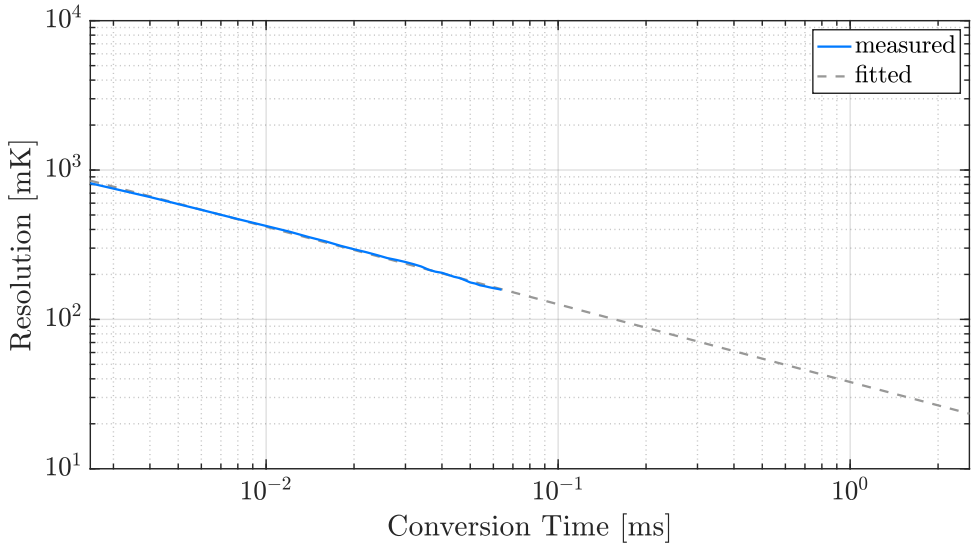


FIGURE 3.32: *mas fuerte* measured resolution as a function of the conversion time.

Another interesting graph is shown in Fig. 3.32, in which the measured resolution is plotted as a function of the conversion time. This result has been achieved by a sweep of the oversampling factor; starting with an OSR equal to 1 (corresponding to a 2-µs conversion time, that is of single 8-bit conversions) at the left boundary, the shown curve is well approximated by a straight-line considering log-scaled axes. This validates even more the rule expressed within (3.11) and is further supported by the power-spectral density shown in Fig. 3.33 which is purely white and will be readdressed in Chapter 5.

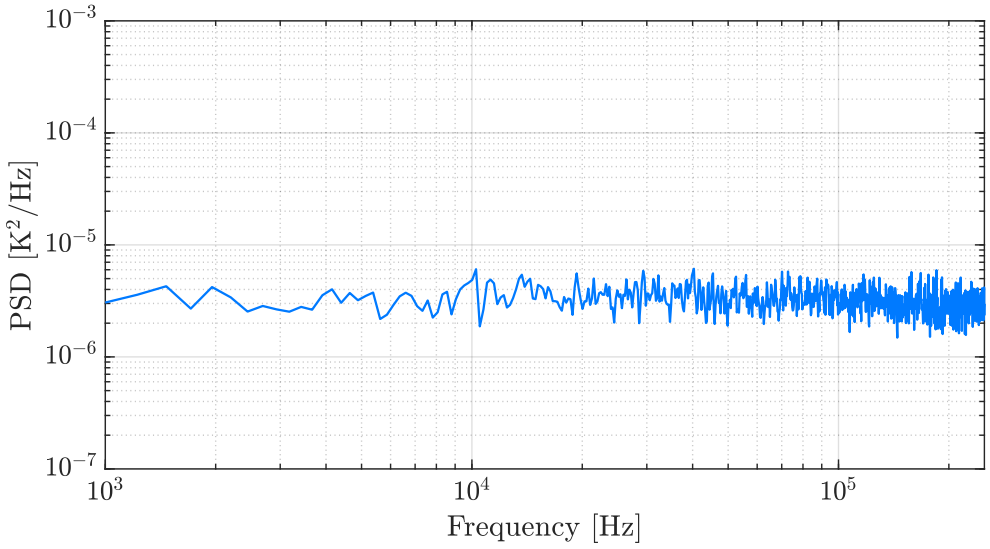


FIGURE 3.33: Measured PSD of the *mas fuerte* output codestream (Hanning window, 2048 samples, 16x averaging).

	[40] ISSCC 2017	[93] Sens. J. 2018	[92] ISSCC 2018	[42] TCAS-I 2018	[44] TCAS-II 2019	[46] JSSC 2020	[5] TCAS-I 2020	[91] TCAS-II 2020	[47] TCAS-II 2021	**mas fuerte 2021**
ADC Type	ΣΔ1	ΣΔ2	SAR	ΣΔ2	ΣΔ1	ΣΔ2	ΣΔ1	SAR	DCM	OS-SAR
Technology [nm]	28	180	22	130	55	160	65	180	130	180
Area [mm^2]	0.01	0.18	0.004	0.29	0.01	0.15	0.003	0.12	0.09	0.08
Temperature Range [°C]	-25 to 125	0 to 100	-30 to 120	-40 to 125	-40 to 125	-40 to 180	-10 to 110	-10 to 100	-40 to 125	-20 to 80
Supply Voltage [V]	1.8	1.0	1.0	3.3	1.0	1.8	1.3	1.0	1.2	1.8
Measured Samples	76	15	38	16	12	24	25	15	16	20
Relative Inaccuracy [%]	2.47	0.36	1.43	0.57	2.06	0.18	2.25	4.27	0.65	1.39
Trimming Points	0	1	1	1	0	1	2	1	1	2
Power [µW]	18.8	0.7	50	313.5	37	9.8	111.8	0.0005	39.7	39.6
Conversion Time [ms]	8.2	40	0.032	5.12	32.8	20	4.1	200	1.3	0.064
Conversion Energy [nJ]	150	28	1.6	1605	1214	195	460	0.098	52	2.5
Resolution [mK]	150	40	580	16	20	23	130	590	60	158
Resolution FoM [$pJ \cdot K^2$]	3500	45	538	411	486	103	7774	34	187	63

TABLE 3.5: *mas fuerte* performance summary and comparison with state-of-the-art BJT-based TDCs.

3.8 State-of-the-Art Comparison

Tab. 3.5 reports a wide state-of-the-art comparison with recently published BJT-based works in the TDC framework; the rightmost column inherently presents a performance summary of the *mas fuerte* chip presented in this Chapter.
According to the *ADC Type* row, it can be noticed that this work is the only one combining the resolution refining advantage of an oversampling approach as in [5, 40, 42, 44, 46, 93] with the low energy per conversion advantage of a SAR approach as in [91, 92]; this results in a *Resolution FoM* of only 63 pJ·K^2. In addition, considering the *Area* of the reported works fabricated in similar technology processes with respect to the 180-nm CMOS adopted for the proposed design [44, 46, 47, 91, 93], it can be seen that its compactness its competitive. The weak spot of this design concerns undoubtedly its accuracy performance; indeed, the employment of two *Trimming Points* is rather limiting the cost-effectiveness of the device but was necessary to meet the sensor's requirements and, under these conditions, the achieved 1.39 % is not that great. Nevertheless, the overall performance of the *mas fuerte* chip turns out to be quite satisfactory and adequate for the application of interest.

Chapter 4

es posible test chip

THE resolution refining process of the *mas fuerte* chip described in Chapter 3 exploits the random variability of the TDC output codes caused by the presence of thermal noise in the system; this approach gives rise to a good energy efficiency corresponding to a resolution FoM of 63 pJ·K^2; in this Chapter, an evolution of this concept, that gave birth to a new test chip called *es posible*, will be presented.
The basic idea is to introduce a deterministic process regulating the variability of the output datastream instead of processing a random flow, still running a SAR algorithm to generate the temperature-dependent digital codes; this is done introducing an error-feedback scheme within the TDC implementing a noise shaping (NS) on the output datastream. The attractiveness of NS-SAR ADCs strongly emerged in the last decade [94–99] as they combine the advantages of standard SAR solutions with the advantages of ΣΔ-based architectures and was never exploited before within a TDC system; moreover, considering that the same *Bipolar Core* of the *mas fuerte* chip has been employed in this new design, the current-mode processing approach has been mantained giving life to the first NS-SAR ADC fully designed in the current domain with the huge advantage of being op-amp-less. For this design, considering the noise level measured at the output of the *mas fuerte* chip (Fig. 3.30) the main responsible of which is the *Bipolar Core*, the resolution of the codes generated in each SAR conversion cycle has been reduced from 8 bits to 4 bits. This has been necessary to bring the system into a quantization noise dominated condition to make the deterministic variability of the sensor's output, achieved with the error-feedback scheme, effective. Besides being essential for the noise shaping implementation, the transition to a 4-bit architecture offered three significant side benefits:

- the current-steering DAC matching, responsible for the insufficient inaccuracy performance with a sigle trimming point in the *mas fuerte* test chip, has been improved; it has been possible to remove the *Split Stage* having a much lower maximum mirroring factor to handle within the DAC.
- the current-steering DAC area, the largest according to the breakdown of Fig. 3.20, has been drastically compacted thanks to the reduced mirroring constraints.
- for the same clock frequency, the duration of a single SAR conversion has been reduced as a consequence of the reduced amount of decisions to be taken by the comparator.

The *es posible* test chip has been designed for the same application and with the same goals and requirements presented at the beginning of Chapter 3; as will be presented in the following Sections and summarized in the last Chapter of this thesis, it provides a significant boost to its predecessor (*mas fuerte*) succeeding in meeting all the design specifications.

4.1 TDC Architecture

The block diagram of the proposed NS-SAR based TDC is shown in Fig. 4.1. The BJT Core, composed by PTAT and CTAT current sources is exactly the same as the one described in the previous Chapter. Its output signals are delivered to the Current-Mode NS-SAR by means of three interface circuits, an n-type current mirror and two current buffers. While the n-type current mirror performs the same function of the *DAC Interface* of Fig. 3.1 with a different scaling factor, the current buffers (which are simple common-gate structures) substitute the *Current Comparator Interface* of the *mas fuerte* TDC. In fact, both the Current Comparator and the Noise Shaper blocks have been designed with n-type inputs: the comparator corresponds to a flipped version of the one shown in Fig. 3.5 while the shaper will be described in Section 4.3.

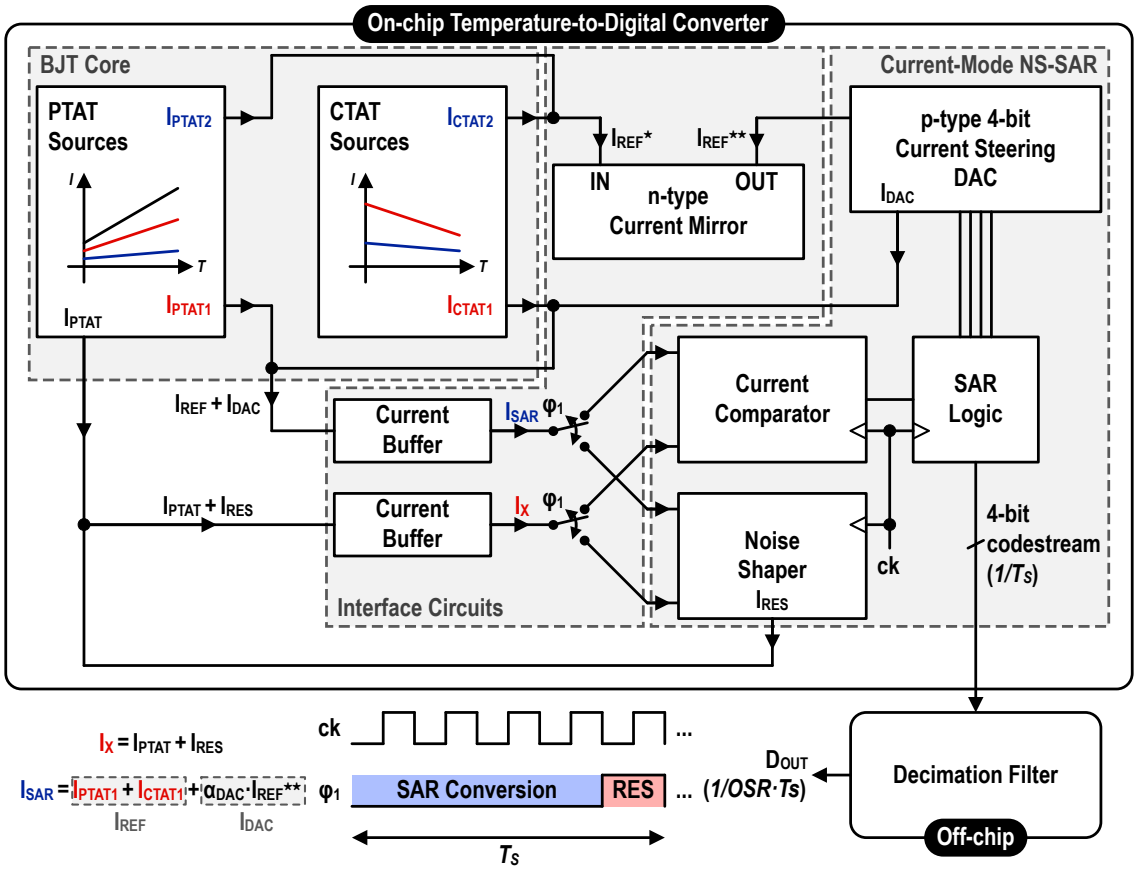


FIGURE 4.1: Proposed NS-SAR based TDC with fully current-mode architecture.

The signals involved in the temperature-to-digital conversion generated by the BJT Core are I_{PTAT}, $I^{\star}_{REF}$ and I_{REF}, the first one containing the temperature information to be converted. $I^{\star}_{REF}$ gets replicated as $I^{\star\star}_{REF}$ and is provided as a reference signal to a binary p-type 4-bit current steering DAC, which scales it sequentially according to a successive approximation algorithm:

$$I_{DAC} = \alpha_{DAC} \cdot I^{\star\star}_{REF}, \tag{4.1}$$

where I_{DAC} is the DAC output current while α_{DAC} is the scaling factor it implements.

$$I_{REF} = I_{PTAT1} + I_{CTAT1} \tag{4.2}$$

is used to set the proper conversion range upshifting I_{DAC} in order to obtain

$$I_{SAR} = I_{REF} + I_{DAC}. \tag{4.3}$$

Each 4-bit conversion is carried out in 4 clock cycles, in which the subsequent decisions of the current comparator about the polarity of the ADC input signals (I_X and I_{SAR}) are processed by the SAR logic; then, in a dedicated clock period, as shown in the conceptual timing diagram of Fig. 4.1 (bottom), a noise shaper generates a residue current (I_{RES}) that is fed-back to the ADC input and added to I_{PTAT} to form

$$I_X = I_{PTAT} + I_{RES}. \tag{4.4}$$

The 4-bit codestream obtained by a cyclic operation of the described conversion process is finally delivered to a decimation filter which, for testing flexibility reasons, has been kept off-chip. Depending on the selected oversampling-ratio (OSR), it generates more refined digital codes with a $1/(\mathrm{OSR}\cdot T_s)$ rate, where T_s is equal to 5 clock periods.

4.2 Current-mode Noise Shaping Concept

The current-mode error-feedback mechanism, designed to implement a first-order quantization noise shaping, is described in detail in Fig. 4.2. Considering $I_{RES} = 0$ as initial condition, during the RES_1 phase, at the end of the first conversion cycle, both I_X and

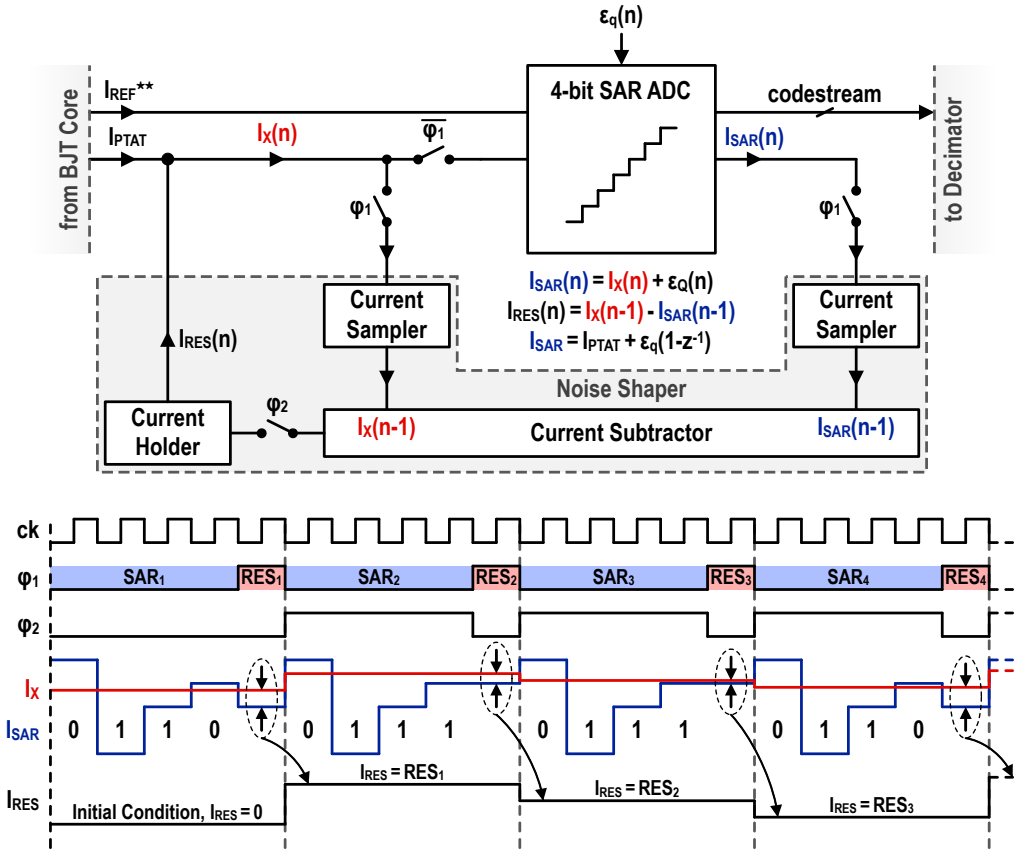


FIGURE 4.2: Detail of the current-mode error-feedback scheme (top) and focus on the first conversion cycles (bottom).

the final I_{SAR} current value are stored by means of two current samplers, while a current subtractor computes their difference; the obtained residue current is then held by a current holder for the entire following conversion cycle until the next I_{RES} current is ready to be added to I_{PTAT}.
Taking the n-th conversion cycle into account,

$$I_{RES}(n) = I_X(n-1) - I_{SAR}(n-1) \tag{4.5}$$

thanks to the combined memory function of the current samplers and the current holder. Moreover, $I_{SAR}(n)$, which is nothing but a quantized version of $I_X(n)$, can be written as

$$I_{SAR}(n) = I_X(n) + \epsilon_q(n) \tag{4.6}$$

$$\overset{\mathcal{Z}}{\Longrightarrow}$$

$$I_{SAR}(z) = I_X(z) + \epsilon_q(z) \tag{4.7}$$

where ϵ_Q is the quantization error and where a $\mathcal{Z}$-transformed version is also shown, needed for the following of this Section. In addition, it can be deduced from Fig. 4.2 that

$$I_X(n) = I_{PTAT} + I_{RES}(n) \tag{4.8}$$

where I_{PTAT} is treated as a constant because a fixed temperature is being considered. Combining (4.5) with (4.8), a new expression for $I_X(n)$ is derived:

$$I_X(n) = I_{PTAT} + I_X(n-1) - I_{SAR}(n-1) \tag{4.9}$$

$$\overset{\mathcal{Z}}{\Longrightarrow}$$

$$I_X(z) = I_{PTAT} + I_X(z) \cdot z^{-1} - I_{SAR}(z) \cdot z^{-1} \tag{4.10}$$

where its $\mathcal{Z}$-transform is reported since the next steps will be carried on in this domain. Isolating $I_X(z)$ in (4.10),

$$I_X(z) = \frac{I_{PTAT} - I_{SAR}(z) \cdot z^{-1}}{1 - z^{-1}}. \tag{4.11}$$

Incorporating (4.11) in (4.7),

$$I_{SAR}(z) = \frac{I_{PTAT} - I_{SAR}(z) \cdot z^{-1}}{1 - z^{-1}} + \epsilon_q(z). \tag{4.12}$$

Manipulating this equation and performing the straightforward cancellation, the final expression for $I_{SAR}(z)$ is achieved:

$$\begin{aligned} I_{SAR}(z) \cancel{- I_{SAR}(z) \cdot z^{-1}} &= I_{PTAT} \cancel{- I_{SAR}(z) \cdot z^{-1}} + \epsilon_q(z) \cdot (1 - z^{-1}) \\ I_{SAR}(z) &= I_{PTAT} + \epsilon_q(z) \cdot \underbrace{(1 - z^{-1})}_{NTF}. \end{aligned} \tag{4.13}$$

Since a one-to-one correspondence between the values of I_{SAR} at the end of each conversion cycle and the 4-bit output codes exists ($I_{SAR} \leftrightarrow D_{OUT}$), it follows that a first order noise shaping is achieved as proven by the noise transfer function (NTF) highlighted in (4.13). This, in the time domain and for a given temperature, results in a determined code pattern involving adjacent 4-bit codes that, processed by the decimation filter, provides higher resolution digital samples. Fig. 4.3 supports this concept with some system-level post-layout simulation results (the noise shaper circuit implementation and the full TDC layout will be discussed in Section 4.3 and 4.4, respectively) in which the NS-SAR ADC

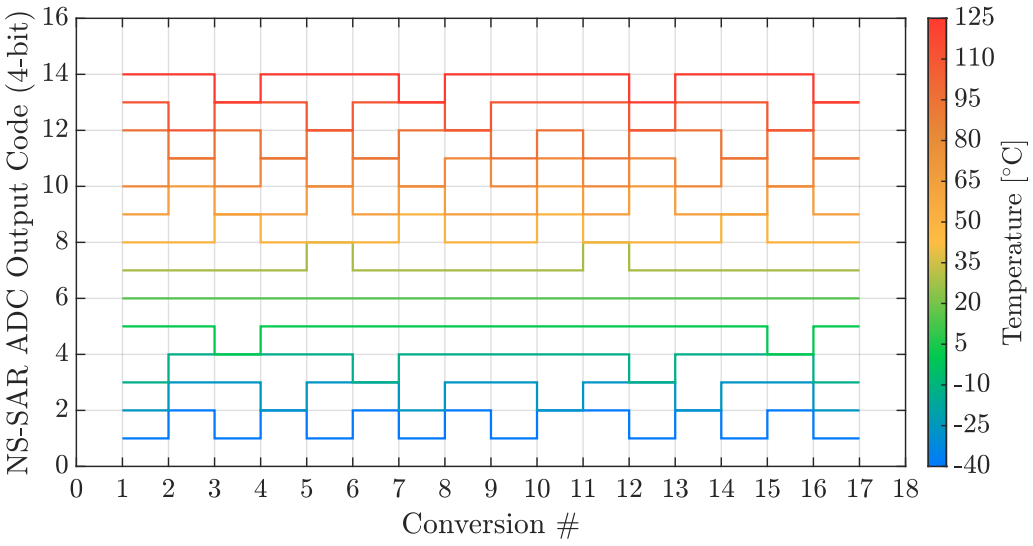


FIGURE 4.3: NS-SAR output code patterns as a function of temperature (post-layout simulation results).

response for 16 consecutive conversions is shown as a function of temperature in the $-40\,^{\circ}\mathrm{C}$ to $125\,^{\circ}\mathrm{C}$ range with steps of $15\,^{\circ}\mathrm{C}$: besides the previously mentioned patterns, it can be noticed that the temperature-to-digital conversions take place in the same dynamic range of the *mas fuerte* chip and still according to (3.9) since the BJT Core is the same in the two designs.

4.3 Current-mode Noise Shaper Design

Fig. 4.4 reports the schematic (top) and timing (bottom) diagrams of the noise shaper circuit; after reset, this circuit is first operated at the end of the initial SAR conversion phase. While ϕ_1 is high, the current samplers collect I_X and I_{SAR} into two cascode mirroring structures in which every transistor is equipped with a gate voltage sampling capacitor (C); these capacitors have been sized to keep this information for a full conversion cycle. The input currents are thus replicated at the subtractor input that, exploiting a p-type current mirror, generates their difference as output:

$$I^*_{RES} = I^*_X - I^*_{SAR}. \tag{4.14}$$

Once this process has been completed, ϕ_1 turns low while ϕ_2 turns high; the obtained residue current gets passed to the holder and, with an additional mirroring step, it generates I_{RES}, which is the desired error-feedback current. A key point of the noise shaper circuit is its timing; the current-mode noise shaping implementation is possible thanks to the synchronous current storing feature of the samplers and the holder. During the n-th SAR conversion ($\phi_1 = 0$) the samplers are disconnected from the input signals and maintain information about the (n-1)-th input values. Their difference is delivered to the holder that, in turn, provides it as feedback for the TDC; the holder role, instead, is essential when $\phi_2 = 0$: it holds the residue corresponding to the just finished n-th conversion, $I_{RES}(n)$, while the generation of the one needed for the (n+1)-th conversion, $I_{RES}(n+1)$, is carried out; this is necessary considering that $I_{RES}(n+1)$ should be determined on the

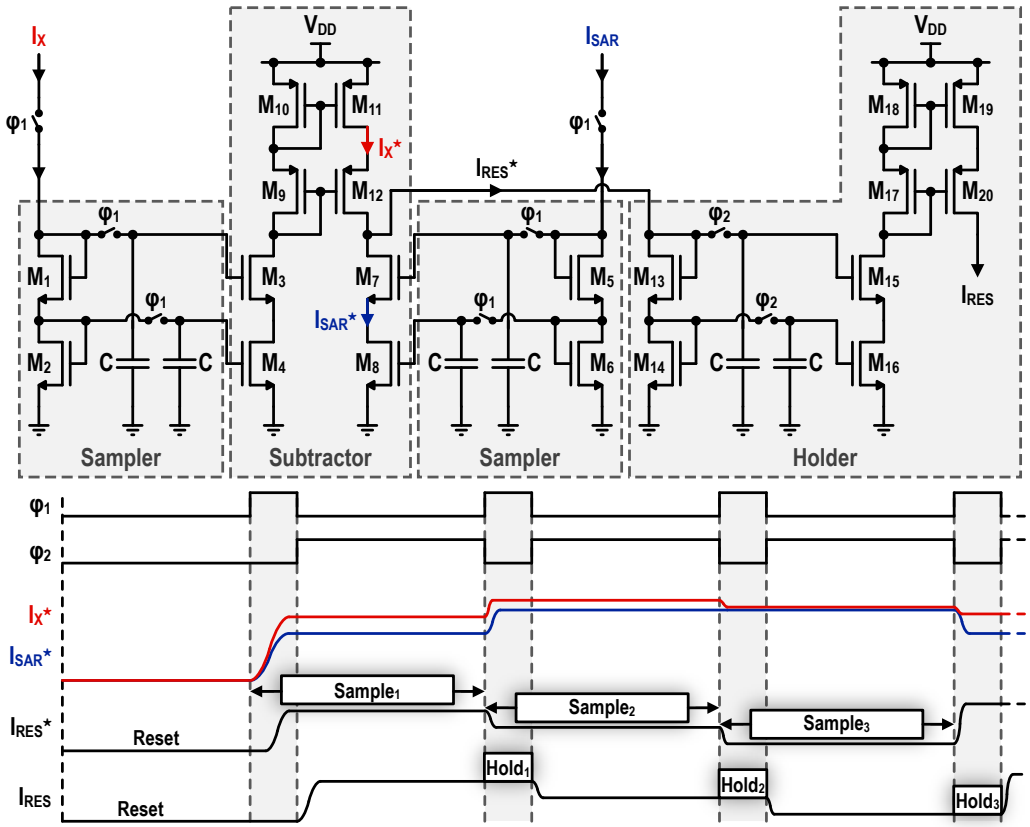


FIGURE 4.4: Schematic (top) and timing (bottom) diagrams of the noise shaper circuit.

basis of $I_{RES}(n)$ and, therefore, it is fundamental that this step occurs without $I_{RES}(n)$ being affected by the evaluation process by the subtractor of $I_{RES}(n+1)$.
It can be observed that, according to the circuit of Fig. 4.4, the residue current has to be unipolar: this is the case of the *es posible* system since the employed ADC approximates the analog input current always by defect and therefore I_X is always larger than I_{SAR}. This can be seen considering the comparator implementation (n-type version of the one shown in Fig. 3.5) and considering that, during the *RES* phase, the final digital word obtained with the SAR algorithm is applied to the DAC to properly compute I_{RES}.

4.4 Layout and Fabrication

The complete layout of the *es posible* test chip is shown in Fig. 4.5. Its shape is a 298 µm x 192 µm rectangle (corresponding to an area of 57 216 µm^2) and, compared with its predecessor whose layout is depicted in Fig. 3.19, a significant area reduction can be observed[1]. The upper part of the layout, which corresponds to the BJT Core equipped with its start-up circuit, has been re-used from the previous design since both chips employ the same circuit (Fig. 3.3); the lower part, instead, is exclusively present in this design and consequently has the merit of providing the clear area reduction. The device has been fabricated in a standard 180-nm CMOS process and, according to [85] this is the most compact BJT-based temperature sensor designed in such a mature technology node so far.

[1]Fig. 3.19 and Fig. 4.5 have exactly the same scale thus can be directly compared.

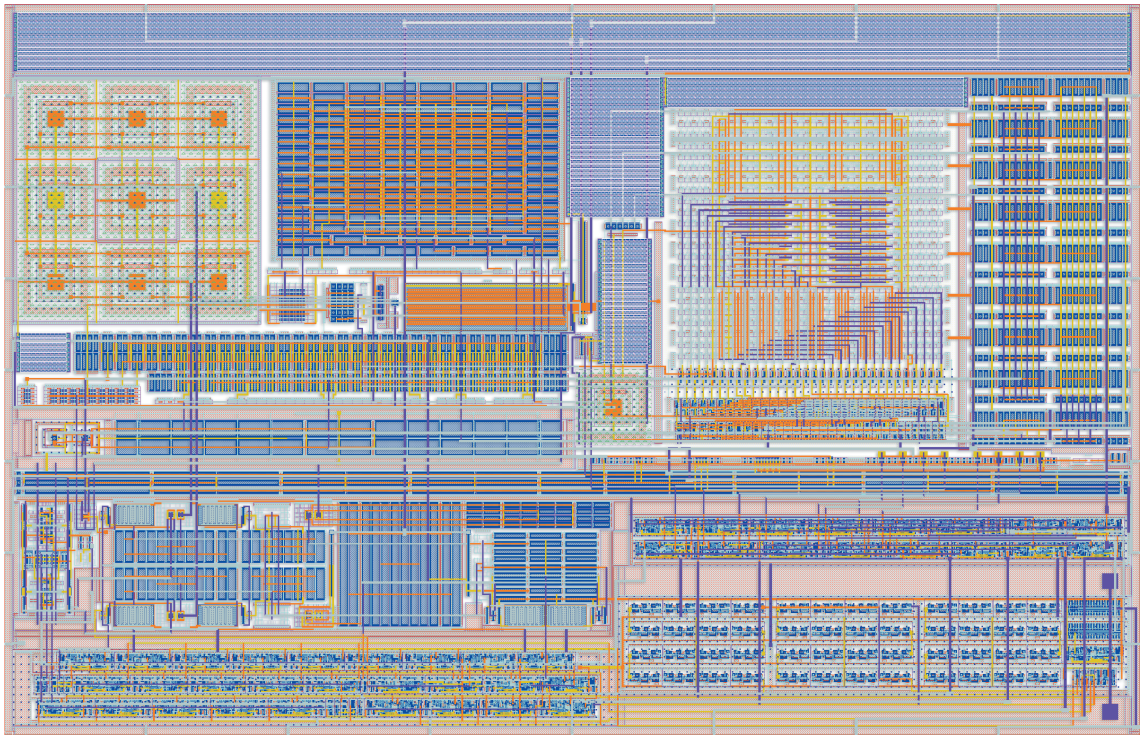


FIGURE 4.5: *es posible* layout.

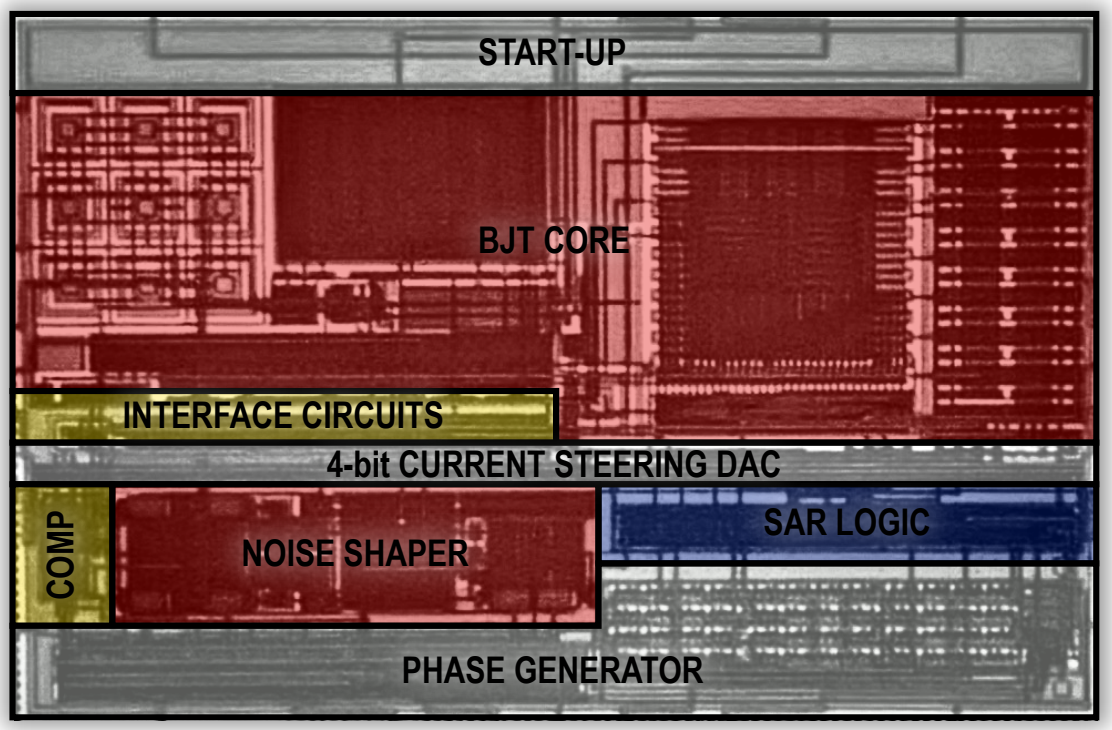


FIGURE 4.6: *es posible* chip micrograph with area breakdown.

A micrograph of the active area of the chip is shown in Fig. 4.6. It can be noticed that the majestic 8-bit current steering DAC of the *mas fuerte* chip has given way to a really compact 4-bit DAC while in the lower part of the die the comparator, the noise shaper, the SAR logic and a phase generator that governs the operation of the whole system have been placed.

Also in this case, a DIL28 package has been selected to encapsulate the fabricated dies according to the pinout scheme of Fig. 4.7. The supply strategy is equal to the one chosen for the *mas fuerte* device with the *avdd-avss*, *dvdd-dvss* and *vddio-vssio* pairs while an additional analog output has been introduced to monitor the residue current described in the previous Section (I_{RES}). The remaining pins correspond to 11 digital inputs, 5 digital outputs and one analog input. The set of digital outputs contains the 4 bits generated by the TDC ($B0$ to $B3$) and an EOC signal that notifies the end of the temperature-to-digital conversion process. The digital inputs are the same as those present in the *mas fuerte* pinout with the addition of $filter$, NS and $ctrl_en$; $filter$ allows the activation of a low-pass filter on the BJT Core output, NS enables or disables the noise shaping basically opening the loop of Fig. 4.2 while $ctrl_en$ gives access the the $ctrl$ analog input which is simply an emergency pin (since these pins actually have never been used during the *es posible* measurement campaign, no further details are provided).

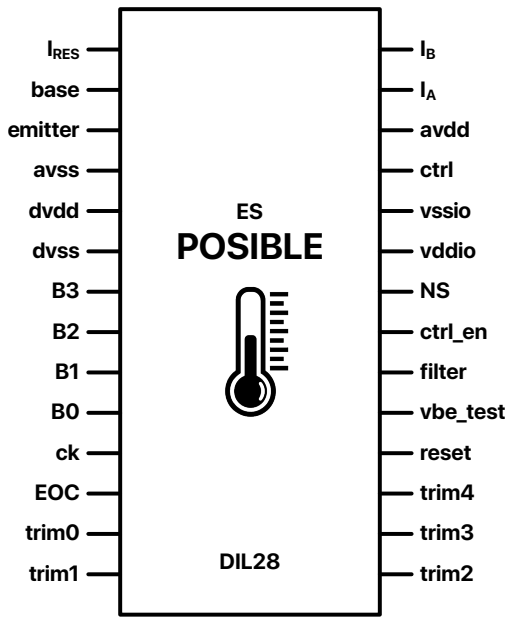


FIGURE 4.7: *es posible* pinout.

4.5 Testing Procedure

The *mas fuerte* testing procedure, presented in Section 3.6, has the disadvantage of a particularly long duration because one sample at a time gets tested: this has forced through some countermeasures such as the reduction of the swept temperature range to shorten the overall measurement time (3.22). In order to overcome this issue, a new PCB has been designed and manufactured in order to make the *es posible* measurement campaign more efficient; instead of having a single ZIF socket, 8 of these have been employed so that the testing routine could be performed on 8 samples at once. The 3D model of the board

is depicted in Fig. 4.8; it can be noticed that, besides the 8× parallelism, a more convenient management of the input/output (I/O) lines has been carried out thanks to the introduction of two 40-pins and 50-pins connectors used for the analog and digital tests, respectively. The jumpers to manually configure the digital inputs have been maintained given their usefulness for preliminary tests while 5 LEDs have been added to make the trimming status of the DUTs clearly visible.

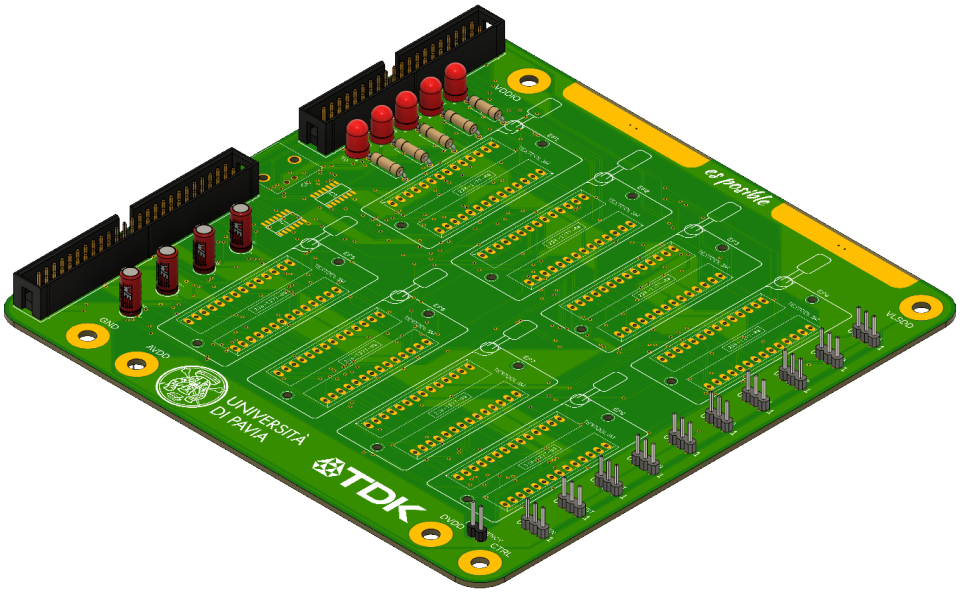


FIGURE 4.8: *es posible* test PCB.

Thanks to this new approach, more extensive measurements have been possible; indeed, the *es posible* chips has been tested over the −50 °C to 110 °C temperature range (with steps of 10 °C) instead of over the shrunk −20 °C to 80 °C one. In addition, a smarter data acquisition has been implemented with a view to have more exhaustive resolution measurements. Since the trimming configuration has no impact on this parameter, for every trimming code except for the mid-range one[2] (at every temperature and for each tested sample) just 2048 acquisitions of the TDC digital output have been performed to extract their average and derive the temperature characteristics needed for the accuracy analysis; in correspondence of the standard trimming code, instead, as many as 2^{20} digital readings have been carried out, resulting in more reliable spectrums (Fig. 4.15) and wider-range resolution versus conversion time curves (Fig. 4.16).
The testing routine, that for the rest is similar to the one carried out for the *mas fuerte* chip, is conceptually summarized in Fig. 4.9 where the three colored boxes have the same meaning as in the previous Chapter. The code behind this scheme has been developed in the LabVIEW environment and the same DAQ system mentioned in Section 3.6 has been employed.

[2]Considering that the same 5-bit trimming circuitry of the previous design has been used, the mid-range code is 10000.

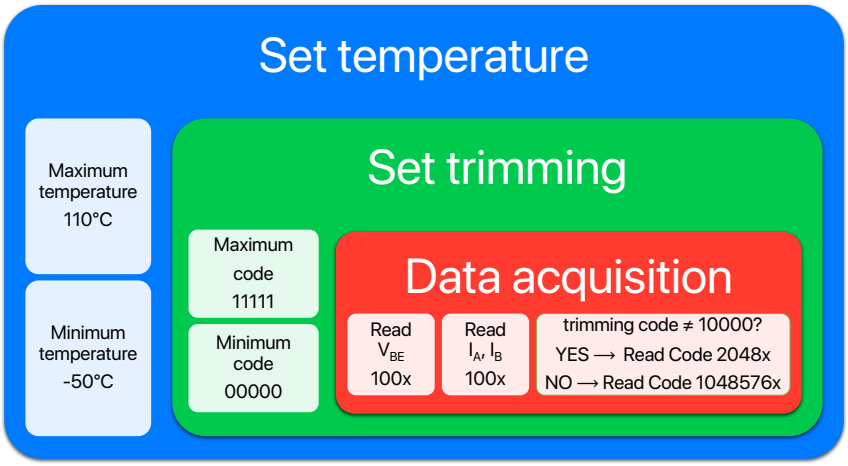


FIGURE 4.9: *es posible* testing routine scheme.

4.6 Measurement Results

During the *es posible* measurement campaign, 25 different samples were tested in a climatic chamber over the −50 °C to 110 °C temperature range with steps of 10 °C. The AFE and the current-mode NS-SAR draw about 14 µA and 20 µA from the 1.8-V supply, respectively, resulting in a total power of 61.2 µW. Accordingly, with an OSR of 64[3], the conversion energy is equal to 4.9 nJ considering that each 4-bit conversion cycle lasts 1.25 µs at a 4 MHz clock frequency. This result meets the requirement of a lower than 10 nJ energy per conversion and is achieved with a better energy efficiency with respect to the *mas fuerte* chip thanks to the first order noise shaping introduction[4].

[3]The choice of this oversampling factor will be motivated in Subsection 4.6.2.

[4]The reported conversion energy of the *mas fuerte* TDC (2.5 nJ) is lower just because it is operated with a lower OSR (32); running the *es posible* TDC with a 32x oversampling factor would offer a 2.45 nJ conversion energy but with a better resolution (130 mK vs 158 mK) as will be clearer in Chapter 5.

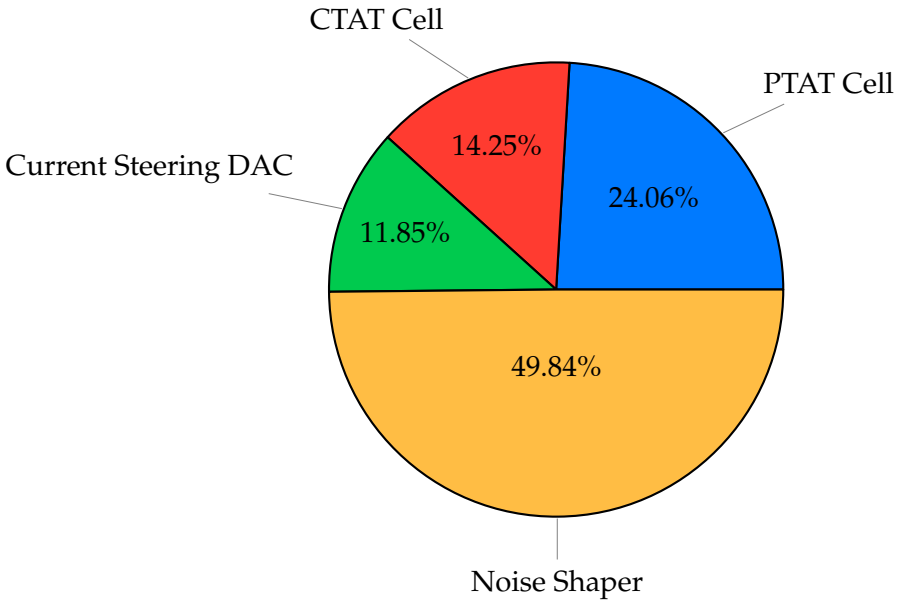


FIGURE 4.10: Power consumption breakdown of the *es posible* TDC.

Fig. 4.10 shows the power breakdown among the main blocks of the *es posible* TDC. It can be noticed that the Noise Shaper slice is predominant because this circuit (Fig. 4.4), in order to generate the previously discussed residue current, collects and replicates all the current contributions coming from the other blocks; in this design no attenuations have been implemented but the shaper can definitely be optimized in future works to reduce its impact on the device power consumption. On the other hand, comparing this breakdown with the one of Fig. 3.26, the employment of simple current buffers in place of the interface employed in the previous design (Fig. 3.1) has made the current comparator consumption merely dynamic making it negligible in the overall breakdown; this has been possible at the cost of a simple flip of the comparator scheme (Fig. 3.5) whose input transistors have passed from being p-type to n-type.

4.6.1 Inaccuracy

An inaccuracy analysis has been carried out on 25 *es posible* samples adopting a similar approach to the one used for the *mas fuerte* chips. The measured untrimmed temperature characteristics, in which the average 4-bit output code of 2048 acquisitions is considered, are shown in Fig. 4.11 where the correspondent temperature errors with the $\pm 3\sigma$ limits are also reported.

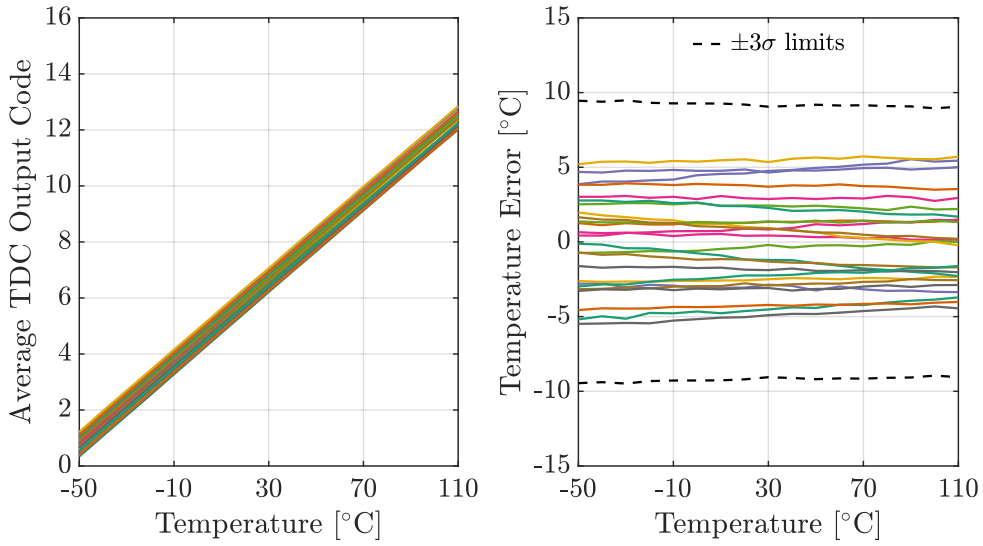


FIGURE 4.11: Measured untrimmed temperature characteristics (left) and correspondent temperature errors (right) of 25 *es posible* chips

Once again, due to mismatch effects among the considered samples the measured curves exhibit a considerable spread corresponding to a considerable temperature error; Tab. 4.1 reports the untrimmed inaccuracy summary.

Untrimmed Inaccuracy	Absolute	Relative
peak-to-peak	±5.61 K	7.01%
3σ	±9.48 K	11.85%

TABLE 4.1: Untrimmed *es posible* inaccuracy summary.

.

These untrimmed inaccuracy values are slightly better than the one collected from the *mas fuerte* chips but still are a far cry from the 2 % target. For this reason, also in this case, at least a room temperature (30 °C) offset compensation is absolutely required and is what is shown in Fig. 4.12.

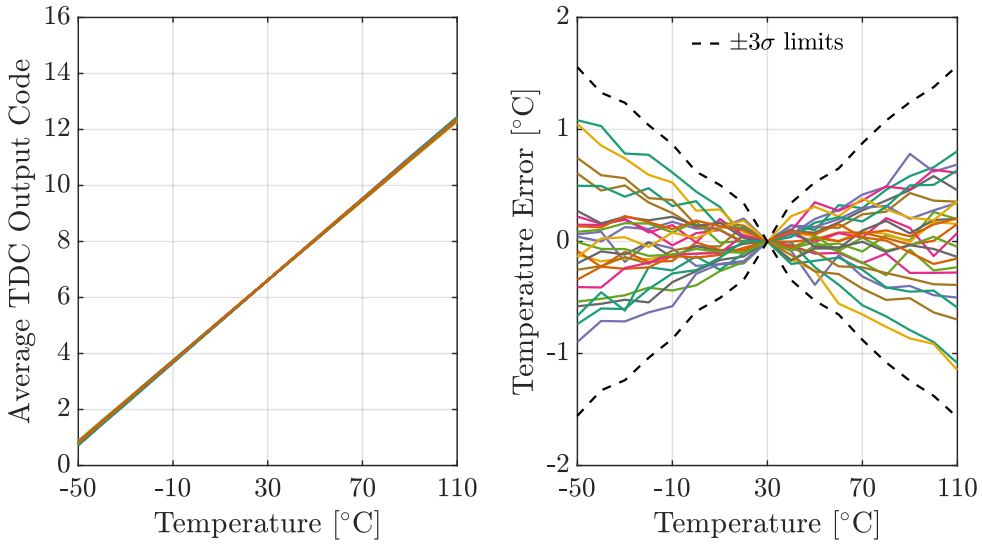


FIGURE 4.12: Measured 1-pt offset compensated temperature characteristics (left) and correspondent temperature errors (right) of 25 *es posible* chips.

The accuracy improvement is clearly noticeable and further confirmed by the values summarized in Tab. 4.2.

1-point Offset Compensated Inaccuracy	**Absolute**	**Relative**
peak-to-peak	±1.11 K	1.39%
3σ	±1.57 K	1.96%

TABLE 4.2: 1-pt offset compensated *es posible* inaccuracy summary.

As can be observed taking the analogous inaccuracy summary that was presented for the *mas fuerte* TDC (Tab. 3.3) into account, the offset compensation is significantly more effective for the *es posible* chip. This is motivated by the change in the DAC employed within this new TDC; the 8-bit current steering DAC with split stage of the previous design, indeed, has given way to a better-matched 4-bit DAC in which the maximum mirroring factor is as low as 4 and inherently the reference current is 4 times bigger. This improved mismatch performance results in lower gain errors of the DAC that consequently provides a reduced spread to the temperature characteristics' slopes; this explains why the relative offset compensated inaccuracy performance of the two TDCs presented in this thesis features a significant gap in favour of the *es posible* device[5].
More importantly, the inaccuracy values reported in Tab. 4.2 fully match the 2 % maximum inaccuracy design specification both with a peak-to-peak approach and with a 3σ one; finally, the calibration at a single temperature is a huge advantage from the cost-effectiveness point of view.

[5]Since the offset compensated temperature error mainly depends on the temperature characteristics' slope spread and since the two devices have been measured in different temperature ranges the right term of comparison is the relative inaccuracy.

4.6.2 Resolution

As anticipated in Section 4.5, the *es posible* resolution analysis has been carried out to the tune of $2^{20}(= 1048576)$ samples for each available device and for each temperature of the considered sweep[6]. Once again, according to a preliminary analysis, the temperature impact on the resolution performance turned out to be substantially negligible; therefore room temperature (30 °C) results are reported and considered as exhaustive.

As shown in the block diagram of Fig. 4.1, the measured 4-bit words have been processed by an off-chip decimation filter to study the proposed error-feedback resolution refining process. Fig. 4.13 shows 256 measured 4-bit room temperature conversions as an example and is directly comparable with Fig. 3.30.

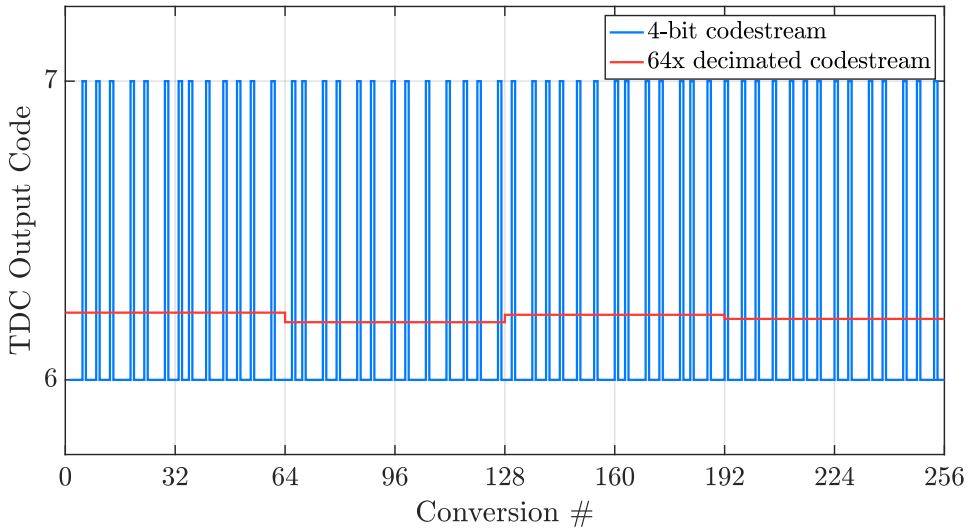


FIGURE 4.13: Measured *es posible* TDC output: 4-bit codestream (blue) and 64x decimated codestream (red).

It can be clearly noticed that the TDC output, as expected, bounces between adiacent codes (0110 and 0111 in this case) in agreement with the discussion of Section 4.2 because, with respect to the random behaviour observed for the *mas fuerte* chip, the *es posible* output datastream is mainly determined by an error-feedback algorithm. The refined codestream, plotted and superimposed in Fig. 4.13 (red curve), has been achieved by means of a decimation by a factor 64: sets of 64 4-bit samples, filtered, give rise to enhanced-resolution samples which, indeed, clearly exhibit a reduced variability. The choice of an OSR equal to 64 will be motivated in the following of this Section.

To evaluate the RMS resolution performance of the *es posible* chip, a statistical analysis of the measured refined samples has been carried out. The resulting distribution is shown in Fig. 4.14 and exhibits a standard deviation of only 92 mK. Compared with the 158-mK resolution achived with the *mas fuerte* device (Fig. 3.31), this improved result comes not only from the employment of a double oversampling factor but also from the feedback action of the noise shaper circuit; indeed, even adopting an OSR equal to 64 in the decimation process of the 8-bit codes generated by the *mas fuerte* TDC, according to Fig. 3.32, a resolution of about 111 mK would result. This means that the *es posible* digital samples are generated with a significantly higher degree of efficiency.

[6]The considered temperature sweep ranges from −50 °C to 110 °C with steps of 10 °C.

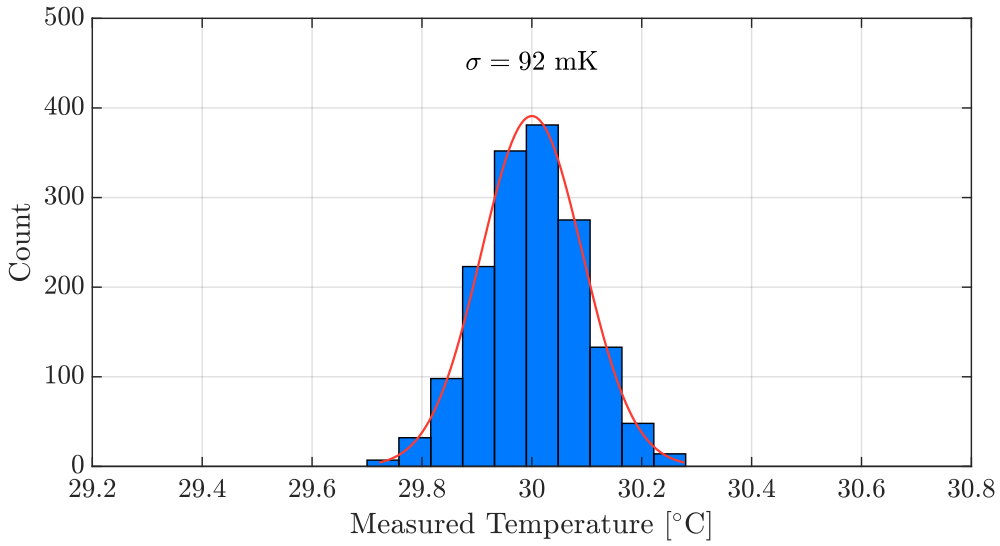


FIGURE 4.14: *es posible* temperature resolution evaluation considering an oversampling factor of 64.

Fig. 4.15 shows the PSD of the *es posible* output codestream, obtained by processing all the 2^{20} available room-temperature samples of the same device of which, in Fig. 4.13, the time-domain operation has been shown and commented. From this perspective, the noise shaping effect can be appreciated at best; its impact can be noticed starting from 10 kHz. The quantization noise spectral behaviour gets altered in agreement with the high-pass NTF derived in Section 4.2: its low frequency contribution gets pushed at high frequency reducing its in-band impact. The band of interest, which is determined by the decimation filter, depends on the conversion time and on the oversampling factor: the intrinsic conversion time (without oversampling or, in other words, with OSR=1)

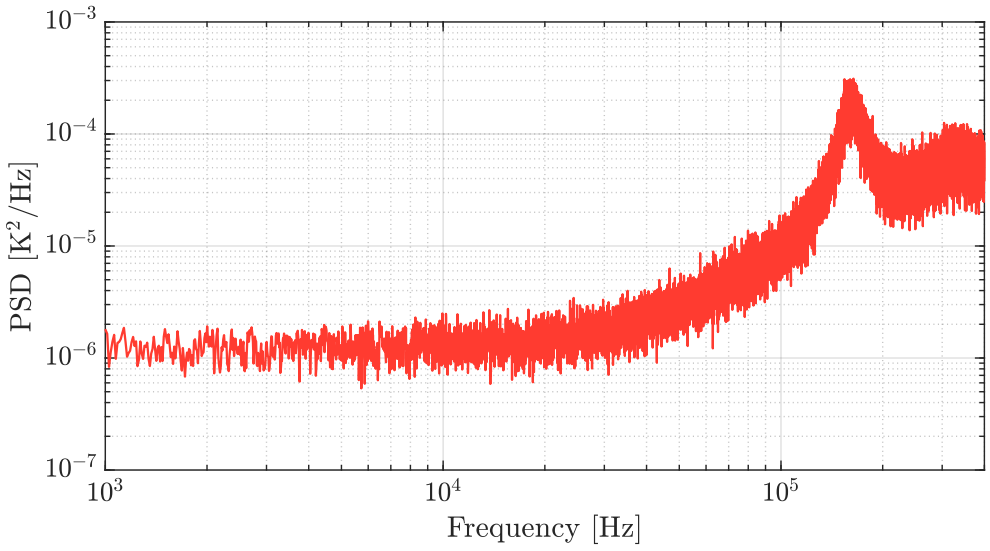


FIGURE 4.15: Measured PSD of the *es posible* output codestream (Hanning window, 65536 samples, 16x averaging).

corresponds to its Nyquist-equivalent frequency (in this case 1.25 µs ↔ 400 kHz) and, from then on, for every doubling of the oversampling factor the band gets halved.

Finally, Fig. 4.16 shows the measured resolution as a function of the conversion time. It can be noticed that the curve exhibits a steeper slope for lower conversion times as a consequence of the progressive outfiltering of the shaped quantization noise. This gives rise to a *q-noise zone* on the left part of the graph and to a *th-noise zone* on the right. The proper conversion time and, consequently, the proper oversampling factor should be chosen in the transition zone in the middle; choosing a conversion time in this range, indeed, ensures to get the most from the noise-shaping benefit and achieve the higher conversion efficiency possible according to the noise constraints of the device. This approch led to the 64x oversampling choice for the *es posible* TDC which results to be the best option with an energy efficiency optimization perspective.

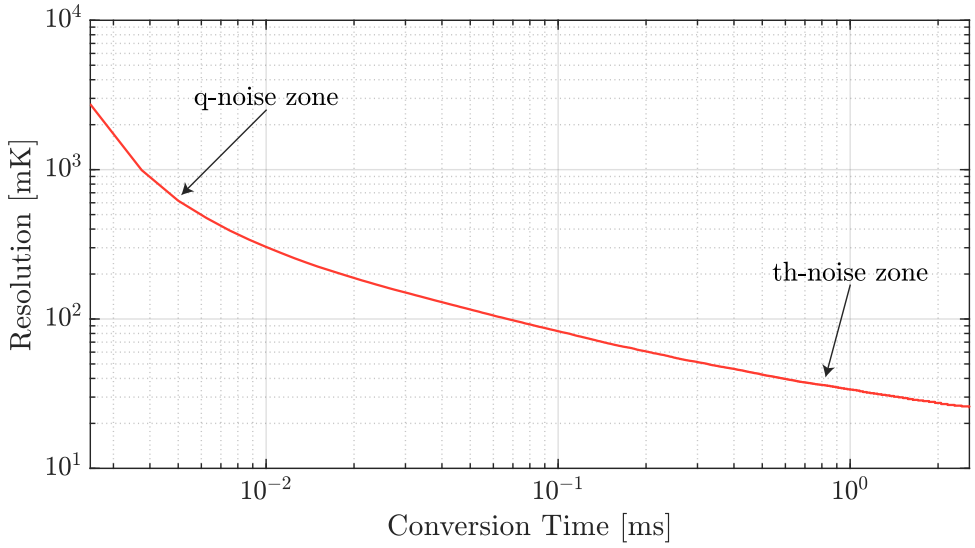


FIGURE 4.16: *es posible* measured resolution as a function of the conversion time.

4.7 State-of-the-Art Comparison

Tab. 4.3 summarizes the performance of the *es posible* TDC and reports a comparison with state-of-the-art BJT-based ones. This work is positioned as an intermediate solution between resolution-oriented designs [42,44,46,47,93] and ultra-low energy-per-conversion-oriented ones [91,92]; the firsts offer a better resolution but require a significantly higher conversion energy and vice versa considering the lasts. This results in an excellent resolution FoM of 41 pJ·K^2. The area reduction with respect to the *mas fuerte* TDC, further confirms that, as anticipated in Section 4.4, this works features the lowest area comparing it with the reported works fabricated in similar technology processes [44, 46, 47, 91, 93]. Finally, the overall performance level of this TDC is competitive and matches the requirements for the targeted application.

	[40] ISSCC 2017	[93] Sens. J. 2018	[92] ISSCC 2018	[42] TCAS-I 2018	[44] TCAS-II 2019	[46] JSSC 2020	[5] TCAS-I 2020	[91] TCAS-II 2020	[47] TCAS-II 2021	**es posible 2022**
ADC Type	ΣΔ1	ΣΔ2	SAR	ΣΔ2	ΣΔ1	ΣΔ2	ΣΔ1	SAR	DCM	NS-SAR
Technology [nm]	28	180	22	130	55	160	65	180	130	180
Area [mm^2]	0.01	0.18	0.004	0.29	0.01	0.15	0.003	0.12	0.09	0.06
Temperature Range [°C]	-25 to 125	0 to 100	-30 to 120	-40 to 125	-40 to 125	-40 to 180	-10 to 110	-10 to 100	-40 to 125	-50 to 110
Supply Voltage [V]	1.8	1.0	1.0	3.3	1.0	1.8	1.3	1.0	1.2	1.8
Measured Samples	76	15	38	16	12	24	25	15	16	25
Relative Inaccuracy [%]	2.47	0.36	1.43	0.57	2.06	0.18	2.25	4.27	0.65	1.39
Trimming Points	0	1	1	1	0	1	2	1	1	1
Power [µW]	18.8	0.7	50	313.5	37	9.8	111.8	0.0005	39.7	61.2
Conversion Time [ms]	8.2	40	0.032	5.12	32.8	20	4.1	200	1.3	0.08
Conversion Energy [nJ]	150	28	1.6	1605	1214	195	460	0.098	52	4.9
Resolution [mK]	150	40	580	16	20	23	130	590	60	92
Resolution FoM [$pJ \cdot K^2$]	3500	45	538	411	486	103	7774	34	187	41

TABLE 4.3: *es posible* performance summary and comparison with state-of-the-art BJT-based TDCs.

Chapter 5

Conclusions

THIS thesis, after a couple of introductory sections about TDC theory and state-of-the-art review, presented two current-mode processing based TDCs designed for the compensation of the thermal drift of MEMS devices. Given the specifications of this application, the two devices have both been designed combining the advantages of a SAR conversion process (low energy per conversion) with the benefits arising from oversampling techniques (high resolution). In addition, in both cases, the minimization of the active area of the device played a key role to achieve the desired cost-effectiveness. The first chip, called *mas fuerte*, exploits the presence of thermal noise in the TDC to oversample 8-bit temperature-dependent digital words in order to achieve a 158-mK resolution; the second one, instead, called *es posible*, implements an error-feedback mechanism to achieve a noise-shaping on the 4-bit output codestream of the TDC obtaining a resolution of 92 mK.

Tab. 5.1 reports a performance comparison of the two devices in which the best results are highlighted in green.

	mas fuerte	**es posible**
ADC Type	OS-SAR	**NS-SAR**
Technology	180-nm CMOS	180-nm CMOS
Area	0.08 mm^2	**0.06 mm^2**
Temperature Range (designed)	-55 °C to 140 °C	-55 °C to 140 °C
Temperature Range (measured)	-20 °C to 80 °C	**-50 °C to 110 °C**
Supply Voltage	1.8 V	1.8 V
Measured Samples	20	**25**
Relative Inaccuracy	1.39%	1.39%
Trimming Points	2	**1**
Power Consumption	**39.6 µW**	61.2 µW
Conversion Time	**64 µs**	80 µs
Conversion Energy	**2.5 nJ**	4.9 nJ
Resolution	158 mK	**92 mK**
Resolution FoM	63 pJ·K^2	**41 pJ·K^2**

TABLE 5.1: Performance comparison of the two TDCs presented in this thesis.

It can be noticed that the *es posible* TDC significantly improves the overall performance with respect to the *mas fuerte* one. It offers a 25 % active area reduction and exhibits the same accuracy level but with a trimming at a single temperature: thus, from a cost-effectiveness perspective, it is definitely better. Moreover, besides having been measured in a significantly wider temperature range, it offers a considerably better RMS resolution

and an improved energy efficiency (as proven by the 41 pJ·K^2 resolution FoM) achieved thanks to the noise-shaping introduction.
The only points against the *es posible* device concern the consumed energy; the noise shaper circuit, in fact, increases its power consumption that results in a higher conversion energy also considering that the selected conversion time is quite longer.

In order to recap the temperature-to-digital conversion approaches in the two cases, it is pretty interesting to compare the output PSDs of the two devices and is what is shown in Fig. 5.1.

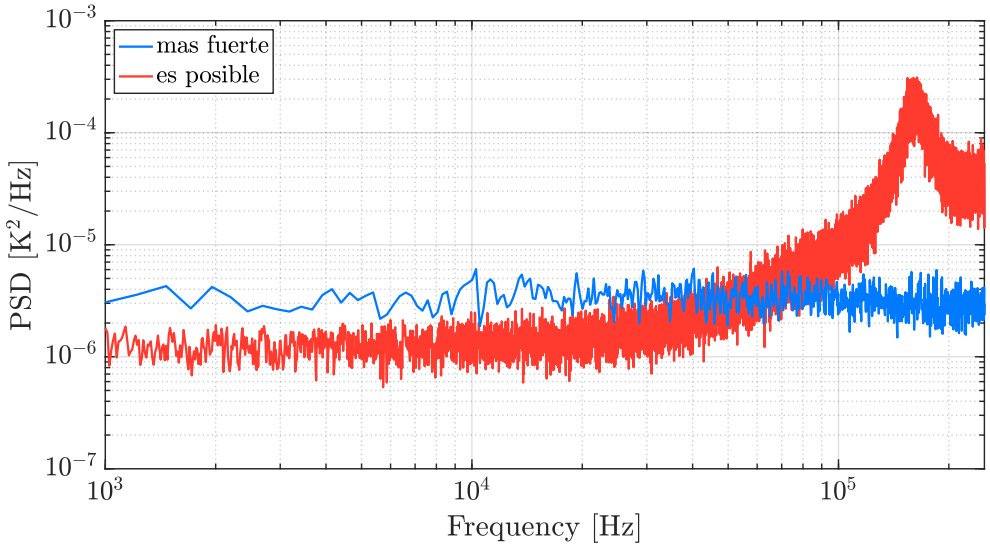


FIGURE 5.1: *mas fuerte* and *es posible* output PSD comparison.

It can be observed that the two spectra exhibit a significantly different behaviour. The *mas fuerte* one is purely white and its level on the vertical axis depends on a mixture of thermal and quantization noise; the *es posible* one, instead, clearly exhibit a shaped behaviour: the quantization noise contribution is pushed at high frequency (according to the NTF discussed in Section 4.2) and gets outfiltered by the decimation filter which processes the output datastream. This means that the achieved resolution depends on the in-band noise level that, being distilled from the quantization noise contribution, is lower with respect to the *mas fuerte* case[1]. This further motivates the better energy efficiency of the *es posible* design.

Finally, Fig. 5.2 shows the measured resolution in the two cases as a function of the conversion time. For conversion times below 5 µs the best resolution is achieved by the *mas fuerte* TDC; this happens because, for low OSR values, the effect of oversampling is too little to turn the tables of the built-in 8-bit resolution of this device with respect to the 4-bit one of the *es posible* chip. After that crossing point, instead, the removal of the in-band quantization noise operated in the *es posible* TDC and achieved thanks to the sufficiently high oversampling factor in this zone, makes it superior with respect to the *mas fuerte* design. It can be noticed that, due to the lower number of acquisitions carried out in the *mas fuerte* measurement campaign (50 000 vs 2^{20}), the correspondent measured curve is interrupted at 64 µs; consequently, a fitted trend line is also reported in order to extend the comparison range.

[1]This comparison is reasonable because both devices employ the same Bipolar Core (Fig. 3.3) which is the main responsible for the electronic noise level in these TDCs.

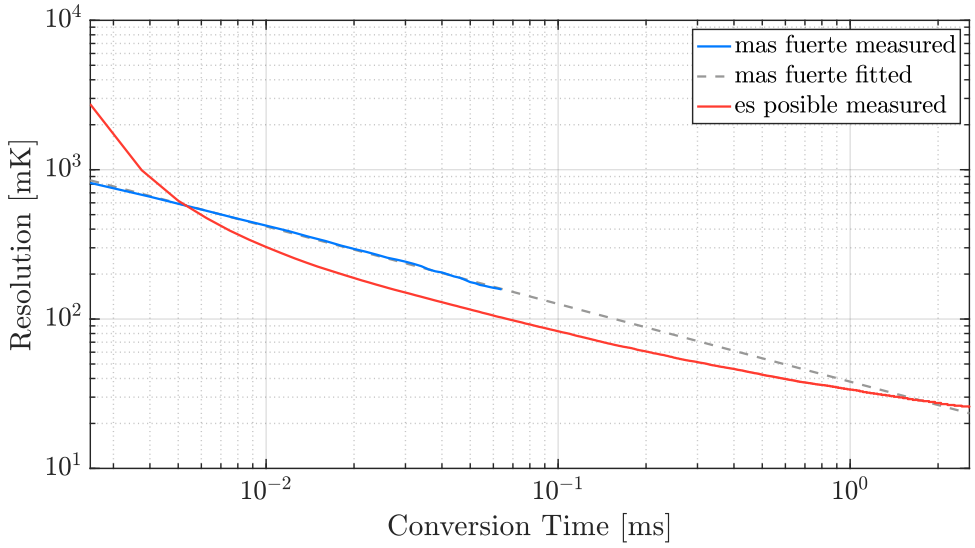


FIGURE 5.2: Measured resolution as a function of the conversion time: *mas fuerte* vs *es posible* comparison.

It can be seen that, in correspondence of a conversion time of 1.75 ms the two curves cross again: this is just because, the fitted curve does not take the flicker noise effect into account which instead is included in the measured red one. In reality, the *mas fuerte* curve behaviour is expected bend so as to follow the *es posible* curve continuing alongside for increasing conversion times.

In conclusion, the results presented in this thesis may be considered satisfactory because the achieved experimental results (Tab. 5.1), especially in the second of the two proposed designs, fully meet the pre-estabilished targets and are perfectly in line with the application of interest.

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List of Abbreviations

ADC	**A**nalog-to-**D**igital **C**onverter
AFE	**A**nalog **F**ront-**E**nd
AR	**A**ugmented **R**eality
BJT	**B**ipolar **J**unction **T**ransistor
BNC	**B**ayonett **N**eill-**C**oncelman
CMOS	**C**omplementary **M**etal-**O**xide-**S**emiconductor
CTAT	**C**omplementary-**T**o-**A**bsolute-**T**emperature
DAQ	**D**ata **A**c**Q**uisition
DBE	**D**igital **B**ack-**E**nd
DIL	**D**ual **I**n-**L**ine
DSP	**D**igital **S**ignal **P**rocessing
DUT	**D**evice **U**nder **T**est
DVFS	**D**ynamic **V**oltage and **F**requency **S**caling
EOC	**E**nd **O**f **C**onversion
ETF	Electro**T**hermal **F**ilter
FoM	**F**igure **o**f **M**erit
HMD	**H**ead **M**ounted **D**isplay
IA	**I**n**A**ccuracy
INL	**I**ntegral **N**on**L**inearity
I/O	**I**nput/**O**utput
IoT	**I**nternet **o**f **T**hings
MEMS	**M**icro-**E**lectro-**M**echanical **S**ystem
MOSFET	**M**etal-**O**xide-**S**emiconductor **F**ield-**E**ffect **T**ransistor
NS	**N**oise **S**haping
NTF	**N**oise **T**ransfer **F**unction
OSR	**O**ver**S**ampling **R**atio
PCB	**P**rinted **C**ircuit **B**oard
PSD	**P**ower **S**pectral **D**ensity
PTAT	**P**roportional-**T**o-**A**bsolute-**T**emperature
REF	**REF**erence
RFID	**R**adio-**F**requency **ID**entification
SAR	**S**uccessive **A**pproximation **R**egister
S/H	**S**ample and **H**old
TC	**T**emperature **C**oefficient
TD	**T**hermal **D**iffusivity
TDC	**T**emperature-to-**D**igital **C**onverter
TWS	**T**rue **W**ireless **S**tereo
VR	**V**irtual **R**eality
ZIF	**Z**ero **I**nsertion **F**orce
ZTC	**Z**ero-**T**emperature-**C**oefficient

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List of Publications

I Aprile, A.; Gardino, D.; Malcovati, P.; Bonizzoni, E. Linearity Boosting Technique Analysis for a Modified Current-Mode Bandgap Reference. In Proceedings of the 27th IEEE International Conference on Electronics, Circuits, and Systems (**ICECS**), Glasgow, UK, 23–25 November 2020; pp. 1–4.

II Aprile, A.; Moisello, E.; Bonizzoni, E.; Malcovati, P. An Extensive Investigation and Analysis of Temperature-to-Digital Converter FoMs. In Proceedings of the 28th IEEE International Conference on Electronics, Circuits, and Systems (**ICECS**), Dubai, United Arab Emirates, 28 November–1 December 2021; pp. 1–4.

III Aprile, A.; Folz, M.; Gardino, D.; Malcovati, P.; Bonizzoni, E. A One-Point Exponential Trimming Technique for an Effective Suppression of Process Spread in BJT-based Temperature Processing Circuits. In Proceedings of the 2022 IEEE International Symposium on Circuits and Systems (**ISCAS**), Austin, TX, USA, 28 May–1 June 2022; pp. 881–884.

IV Aprile, A.; Folz, M.; Gardino, D.; Malcovati, P.; Bonizzoni, E. A Compact 2.5-nJ Energy/Conversion NPN-Based Temperature-to-Digital Converter with a Fully Current-Mode Processing Architecture. In Proceedings of the 48th European Solid-State Circuits Conference (**ESSCIRC**), Milan, Italy, 19–22 September 2022; pp. 473–476.

V Aprile, A.; Moisello, E.; Bonizzoni, E.; Malcovati, P. Performance Comparison of BJT and MOS Devices as Temperature Sensing Elements. In Proceedings of the 29th IEEE International Conference on Electronics, Circuits, and Systems (**ICECS**), Glasgow, UK, 24–26 October 2022; pp. 1–4.

VI Aprile, A.; Bonizzoni, E.; Malcovati, P. Temperature-to-Digital Converters' Evolution, Trends and Techniques across the Last Two Decades: A Review. ***Micromachines*** 2022, *13*, 2025.

VII Aprile, A.; Folz, M.; Gardino, D.; Malcovati, P.; Bonizzoni, E. A 0.06-mm^2 Current-Mode Noise-Shaping SAR based Temperature-to-Digital Converter with a 4.9-nJ Energy/Conversion. In Proceedings of the 2023 IEEE Custom Integrated Circuits Conference (**CICC**), San Antonio, TX, USA, 23–26 April 2023; pp. 1–2.