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ANALYSIS AND DESIGN OF TRANSIMPEDANCE AMPLIFIERS FOR LOW-POWER, SHORT-REACH OPTICAL COMMUNICATIONS IN FINFET TECHNOLOGY

PhD Supervisor:
Prof. Danilo Manstretta

PhD Coordinator:
Prof. Piero Malcovati

PhD Candidate:
Alessio De Prà

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- Where I have consulted the published work of others, this is always clearly attributed.
- Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work.
- I have acknowledged all main sources of help.
- Where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself.

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Abstract

Analysis and Design of Transimpedance Amplifiers for Low-Power, Short-Reach Optical Communications in FinFET Technology

by Alessio De Prà

In this thesis, the feasibility of using advanced Fin-Field-Effect-Transistors (FinFET) technology nodes to implement broadband, low-noise transimpedance amplifiers (TIA) for low-power, short-reach optical communications was investigated. The candidate technology platform was chosen to be the 12 nm LP+ FinFET technology from GlobalFoundries. After a preliminary technology characterization and comparison with older nodes, a theoretical analysis of inverter-based shunt-feedback TIA topologies was carried out, supported by schematic-level simulations. Such analysis aimed at finding the best TIA sizing and peaking scheme to minimize power consumption while also achieving the desired bandwidth and noise performances. Once the targets were achieved in circuit simulations, the design layout was completed and a chip was fabricated. The chip was experimentally tested, showing good performances, albeit some discrepancies with the simulations were observed. The designed chip proves the feasibility of broadband, low-noise TIA for low-power, short-reach optical links in advanced FinFET nodes.

Within the context of the research activities for the present thesis, a Mach-Zehnder modulator driver for coherent optical communications was experimentally tested, whose design, based on novel closed-loop topologies, had been previously carried out by another PhD student at the University of Pavia. Finally, a first design exploration of another optical TIA in GlobalFoundries' 22 nm Fully-Depleted Silicon-On-Insulator (FDSOI) technology to be used with graphene-based photodetectors was carried out as well. The complete designed is actively being finalized by another PhD student.

Acknowledgments

First and foremost, I want to express all my gratitude and affection to my family for the unwavering support throughout my academic journey. I can't imagine wishing for greater love than the one I received from you time and time again during the past years, which gave me strength even in the darker days.

I want to thank Irene as well, for believing in me, even when I couldn't do it myself, and for keeping all my pieces together, even at your own expenses. For what it's worth, this PhD title is yours as much as it is mine.

I cannot forget to mention all my friends, for sharing the joy and the sadness. Life is hard when you don't have good friends, and I certainly know I must be grateful for what I have.

Special thanks to my lab mates, for the fruitful discussions and insights, both technical and not. If I'm a better engineer and man than when I started my PhD, I owe that one to you as well. Hold on tight there: "some day, this pain will be useful to you."

Finally, I have to thank the University of Pavia, my supervisor, and Huawei Technology Italy S.r.l. for the great opportunity of using the expensive FinFET technology. So long, academia, and thanks for all the fish.

Chapter 1

Introduction

In recent years, data retrieval, processing and storage has been at the core of the latest and boldest human inventions, like the Internet and Artificial Intelligence (AI). In 2006, British mathematician and entrepreneur Clive Humby stated that "data is the new oil," which was later expanded by adding that "like oil, data is valuable, but if unrefined it cannot really be used." In the data domain nowadays, data centers act as the place where drilling, refining and stocking take place. Large machine learning models crunch through huge amounts of data while moving it back and forth between countless arrays of memories and graphical processing units (GPUs) which may or may not be located within the same data center. As such, the interconnections between the multiple components which make up the Internet backbone need to satisfy ever more challenging requirements on speed and signal integrity.

AI algorithms most of the time elaborate information which is located within the framework of the same data center where the processing itself is taking place. Data movement and processing which does not leave the data center is called intra-data-center (ID) traffic. Indeed, ID traffic has increased recently to the point where it accounts for up to 70% of the total Internet traffic[1], as it can be seen in Figure 1.1. If data-center-to-data-center (D2D) traffic is taken into the picture as well, the sum of the two accounts for more than 80% of the total Internet traffic. A big share of D2D traffic is actually linked to data centers which are in close proximity to one another, typically less than $2 \div 10$ km. The interconnections that carry the data for both ID and D2D traffic are called short-reach communications.

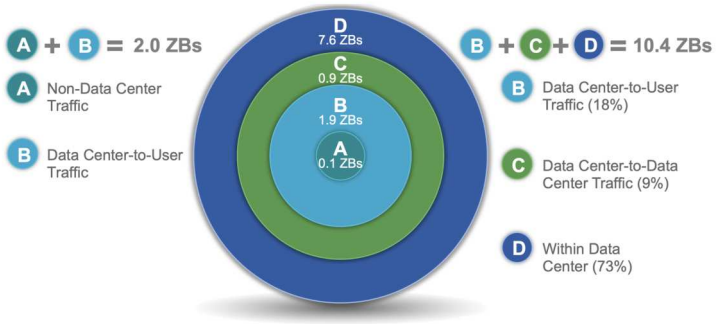


Figure 1.1: Breakdown of Internet data traffic (from [1]). Notice that almost three quarters are due to traffic that does not leave the data center where it originates.

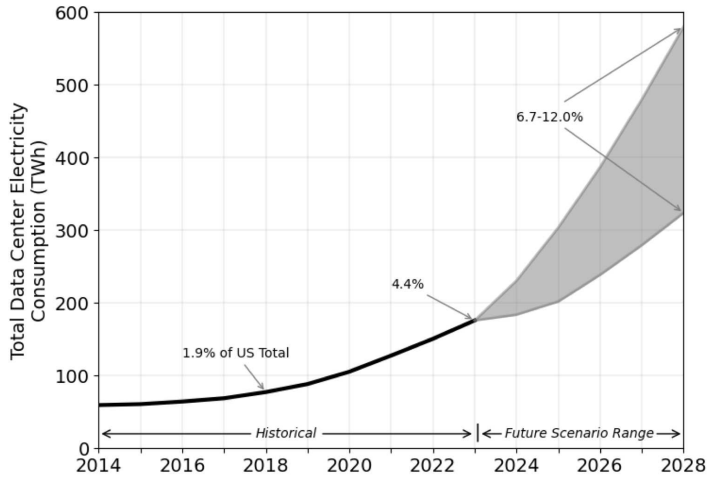


Figure 1.2: Increase in data centers power consumption in the United States from 2014 to 2023 (from [3]), with possible future scenarios up to 2028.

1.1 Data centers power consumption

The increasing trend of data processing inevitably needs to take power consumption into the picture. Data centers have become more power hungry than ever, accounting for up to 1.5% of the global electricity use [2]. Their power consumption is tightly linked to the current AI boom, as displayed in Figure 1.2, where it can be noticed that a twofold increase occurred in just the five year span from 2018 to 2023, and an even bigger increase is expected in the following years.

Given this trend, the design of every electronic component inside data centers needs to minimized, particularly Central Processing Units (CPUs) and

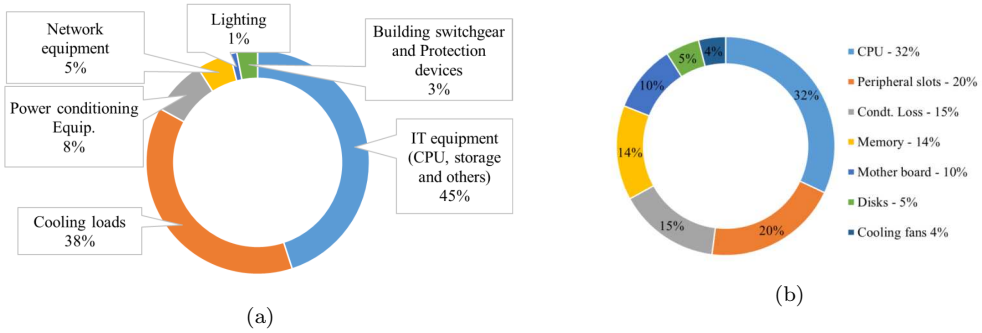


Figure 1.3: (a) Power breakdown of a typical data center; (b) Power breakdown of a typical data server inside a data center (from [4].

network devices, as can be evinced from Figure 1.3a and Figure 1.3b, where the power breakdowns of a typical data center and data server, respectively, are shown [4]. When considering a data center as a whole, 45% of its power consumption comes from IT equipment, while in a single data server 20% of its consumption comes only from peripheral slots, which accounts for network and input/output devices such as switches, routers and optical interconnections. This is the biggest share of the power drawn by a typical server after the CPUs themselves.

All of this clearly points towards the need to decrease the power consumption of network devices, particularly short-reach optical interconnections (SROI) which carry most of the Internet traffic globally. SROI are defined by the imperative to minimize power while also increasing data speeds without compromising on signal integrity. Both requirements on speed and signal integrity are more relaxed than the ones for long-reach optical interconnections (LROI, $>2 \div 10$ km distance), while the power link budget is tighter then in the LROI case.

1.2 Long-Reach vs. Short-Reach Optical Links

LROI cover links like the intercontinental communications enabled by optical fiber cables placed on the sea floor. They typically employ coherent optical transceivers, which leverage complex signal modulation formats, such as 16-Quaternary-Amplitude-Modulation (16-QAM), to dramatically increase the data rate per lane. This can be achieved thanks to their use of in-phase

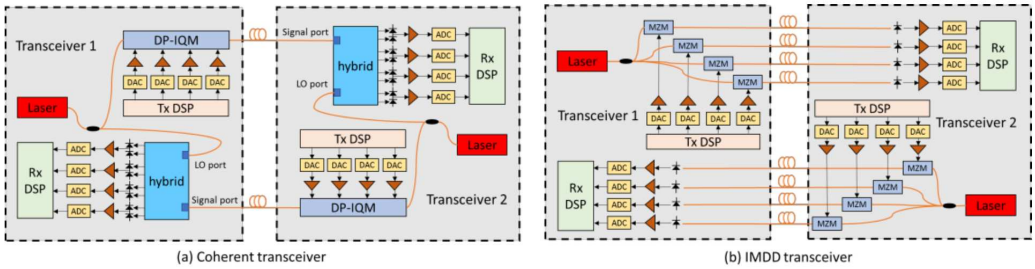


Figure 1.4: Comparison between the typical architectures of coherent and IM-DD transceivers (from [6]).

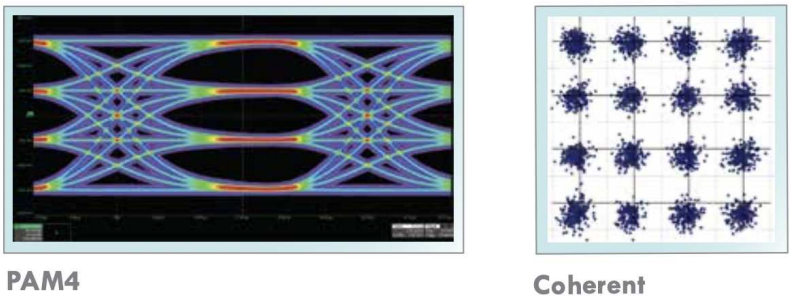


Figure 1.5: Comparison between the 4-PAM (left) and 16-QAM (right) schemes (from [2]).

and 90° phase-shifted versions of the signal, a technique called phase diversity, alongside simultaneously employing multiple polarizations of the electrical field carrying the signal inside the optical fibers, called polarization diversity [5].

SROI instead typically employ simpler signal modulation schemes, such as Non-Return-to-Zero (NRZ) or 4-levels Pulse Amplitude Modulation (4-PAM), with multiple parallel lanes of transceivers using the Intensity Modulation-Direct Detection (IM-DD) architecture to increase the overall link data rate. IM-DD configuration is characterized by the use of electric fields with a single phase and a single polarization state which are only amplitude modulated by the transmitter and are detected by a single photodetector (PD) which directly converts it into an electrical signal that will be the input of the receiver. A comparison between the typical architectures of coherent and IM-DD transceivers is reported in Figure 1.4 while a visual comparison between a 4-PAM and a 16-QAM modulation format is shown in Figure 1.5.

Despite the energy efficiency of coherent transceivers progressing steadily, up to the point of being considered candidate and used for short-distance applications [6], IM-DD is still the dominant architecture for intra-data-center

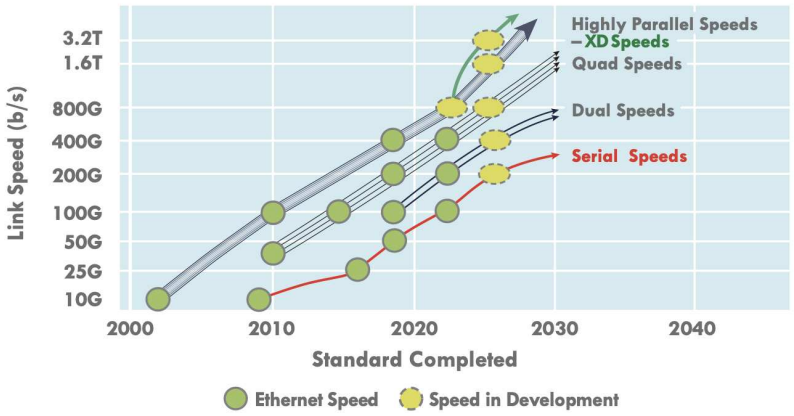


Figure 1.6: Evolution of standards for optical link speed over the years (from [2]).

optical links. The main reasons for this are link budget and reduced sensitivity to noise, distortion and interferences, thanks to simpler modulation schemes employed [7]. IM-DD transceivers employs fewer optical devices, most notably one PD per receiver, and require less electrical power to operate. This inevitably comes at the expense of lower data rate when compared to coherent transceivers. To compensate this, multiple parallel lanes are used in the same link, and every lane has its own optical analog front-end. The latest standards are now moving towards 800 Gb/s link speeds with four lanes each transmitting and receiving at 200 Gb/s, as shown in Figure 1.6.

200 Gb/s per lane can be achieved in IM-DD transceivers by using 4-PAM. This implies a baud rate of 100 GBd/s and an analog front-end bandwidth of about 50 GHz. Usually, this can be achieved in such transceivers by employing a digital-oriented architecture, where analog blocks are only used when interfacing to the optical device and digital techniques involve most of the signal integrity. Analog-oriented architecture, where a bigger share of the signal amplification and recovery is delegated to the analog front-end, is usually associated to coherent receivers. Moving beyond 200 Gb/s per lane is extremely challenging and multiple solutions are actively being considered at the moment [8].

Digital-oriented architectures offer the advantage of more robust signaling and greater ease in using advanced equalization techniques, such as Feed-Forward Equalization and Decision-Feedback Equalization, but usually come

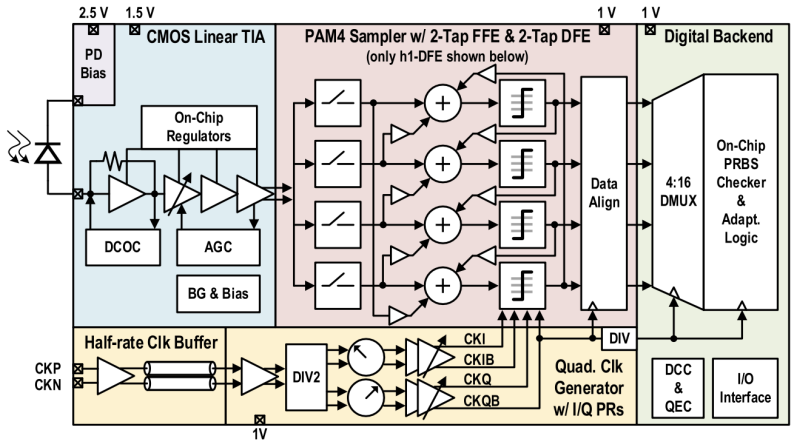


Figure 1.7: Example of a digital-oriented architecture for a 100 Gb/s 4-PAM optical receiver in 28 nm CMOS technology (from [10]). Most of the power is consumed by the equalization section, which operates in the digital domain.

at the expense of greater system complexity and possibly higher power consumption as well [9][10]. An example of a digital-oriented architecture for a 100 Gb/s 4-PAM optical receiver is shown in Figure 1.7[10]. It can be noticed that most of the receiver complexity is linked to the sampling and equalization section, which consumes the most power as well, while the analog front-end, albeit still crucial, has a lower prominence. The analog TIA in this case has actually a lower bandwidth (20 GHz) than the one theoretically needed for 100 Gb/s PAM-4 (25 GHz), since it leads to a lower integrated noise and any inter-symbol interference (ISI) between adjacent symbols due to the bandwidth limitation will be mitigated by the digital equalization.

Analog-oriented architectures have a much lower system complexity but require advanced analog bandwidth-extension techniques which may be more sensitive to process, voltage and temperature (PVT) variations than their digital counterparts [11][12]. Equalization can still be used in analog-oriented architecture, and has been suggested as a way to break the noise-bandwidth trade-off[13]. Figure 1.8 shows an example of an analog-oriented architecture for a 42 GHz coherent optical receiver in 28 nm CMOS technology [11]. It can be seen that no equalization is envisioned for the TIA, which employs sophisticated analog techniques such as inductive peaking and gate cross-coupling to boost the high-frequency content of the signal up to 42 GHz without heavily compromising on noise. However, it should be noted that power consumption

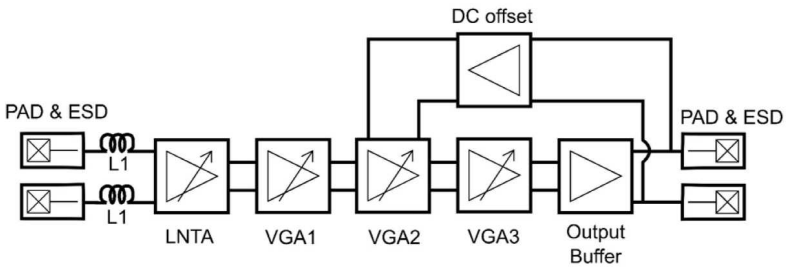


Figure 1.8: Example of an analog-oriented architecture for a 42 GHz optical receiver in 28 nm CMOS technology (from [11]). No digital equalization is foreseen.

is close to the digital-oriented receiver in Figure 1.7.

In order to reduce cost and allow for deeper system integration, CMOS technologies are the main choice for IM-DD receivers. While historically high-frequency broadband signaling has been the domain of BiCMOS technologies, advanced CMOS nodes such as Fin-Field-Effect-Transistor (FinFET) and Fully-Depleted-Silicon-On-Insulator (FDSOI) show promising frequency performances [14][15], albeit at a high silicon cost. In particular, FinFET technologies are promising candidates in bridging the gap between analog- and digital-oriented architectures, allowing both for large analog bandwidths and high-speed digital equalization techniques within the same chip.

Reducing system costs in SROI also entails minimizing the number of optical devices necessary for the system to operate. IM-DD achieve this by avoiding the use of local oscillator lasers and polarization beam splitters (used in coherent architectures for phase and polarization diversity, respectively), as well as balanced photodetectors (necessary to detect the beat between signal and local oscillator in coherent receivers)[5]. This implies the use of a single photodetector directly connected to the single-ended input of the analog front-end. Since a differential output is needed at the output of any optical receiver to interface with the rest of the system, a single-ended-to-differential conversion is needed along the receiver chain and its placement is subject to careful design trade-offs which will be analyzed later.

Within the framework of this PhD thesis, the feasibility of implementing 200Gb/s+ analog front-ends for IM-DD optical receivers has been explored, with focus on low power consumption and low noise, specifically less than 100 mW and 15 pA/$\sqrt{Hz}$, respectively.

Chapter 2

Technology Characterization

In this chapter, the 12 nm LP+ FinFET technology by GlobalFoundries is characterized, evaluated and compared to previous technology nodes. This is a necessary and invaluable step when moving to a new technological node of which there is no previous know-how. The technology has been characterized under a variety of conditions, with particular regard for, but not limited to, cut-off frequency f_T, self gain $g_m r_o$, and channel noise factor γ against g_m/I_D.

g_m/I_D measures how efficiently the current flowing into the device channel is being used, that is how much of it is actually controlled by the signal voltage at the gate (as a matter of fact, it is sometimes called the "transconductor efficiency"). Plotting the aforementioned technological figures of merit against g_m/I_D is useful when comparing to previous nodes, since g_m/I_D is only linked to the overdrive voltage $V_{OV} = V_{GS} - V_{TH}$, "normalizing" to any technological parameter like channel length or oxide material. It can also be used as a unified approach in sizing FETs which is valid for all the operating regions of the device, known as the "g_m/I_D methodology", since the transconductor efficiency is a universal characteristic of all the transistors belonging to the same process node [16]. Such methodology assumes a semi-log plot of the normalized drain current $I_D/(W/L)$ vs. g_m/I_D is available, since:

$$\frac{g_m}{I_D} = \frac{1}{I_D}\frac{\partial I_D}{\partial V_{GS}} = \frac{\partial[log(I_D)]}{\partial V_{GS}} = \frac{\partial[log(I_D/(W/L))]}{\partial V_{GS}} \tag{2.1}$$

Assuming a square-law device, it is well known that g_m/I_D is constant in the weak inversion region while it is inversely proportional to the overdrive

voltage in the strong inversion region:

$$\frac{g_m}{I_D} = \frac{1}{I_D}\frac{\partial I_D}{\partial V_{GS}} = \begin{cases} \frac{1}{nV_T} \text{ in weak inversion} \\ \frac{2}{V_{OV}} \text{ in strong inversion} \end{cases} \tag{2.2}$$

More accurately, the current-law of a sub-micron device in strong inversion becomes:

$$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}\frac{V_{OV}^2}{1+\theta V_{OV}} \tag{2.3}$$

where θ is a technological factor accounting both for mobility degradation and carrier velocity. More advanced effects like drain-induced barrier lowering (DIBL) would excessively complicate the equations to get meaningful design insights. From Equation 2.3 it can be sees that in strong inversion g_m/I_D becomes:

$$\frac{g_m}{I_D} = \frac{2+\theta V_{OV}}{V_{OV}(1+\theta V_{OV})} \approx \begin{cases} \frac{2}{V_{OV}} \text{ if } \theta V_{OV} \ll 1 \\ \frac{1}{V_{OV}} \text{ if } \theta V_{OV} \gg 2 \end{cases} \tag{2.4}$$

Equation 2.4 shows that for high vertical and lateral channel electric fields ($\theta V_{OV} \gg 2$), g_m/I_D starts to decrease less than in the square-law model. This is even more true for advanced FinFET nodes, where higher order effects make the current equation in strong inversion less than quadratic, almost linear.

Equation 2.3 also shows the origin of some of the distortion in MOS analog circuits. If V_{GS} distortion is assumed to be dominant (small V_{DS} amplitude, even if this is arbitrary in deeply scaled nodes, given the current's high dependence on the lateral channel field due to effects like DIBL), the second- and third-order harmonics of the output current are directly linked to the second- and third-order derivatives of Equation 2.3, which are:

$$g_{m2} := \frac{\partial^2 I_D}{\partial V_{GS}^2} = \mu C_{ox}\frac{W}{L}\frac{2}{(1+\theta V_{OV})^3} = \frac{4I_D}{V_{OV}^2(1+\theta V_{OV})^2} \tag{2.5}$$

$$g_{m3} := \frac{\partial^3 I_D}{\partial V_{GS}^3} = \mu C_{ox}\frac{W}{L}\frac{-12\theta}{(1+\theta V_{OV})^4} = \frac{-12\theta I_D}{V_{OV}^2(1+\theta V_{OV})^3} \tag{2.6}$$

In differential receivers, where even-numbered harmonics are heavily attenuated and g_{DS} distortion can be neglected, g_{m3} is the main cause for distortion. From Equation 2.6, it can be seen that the only way to reduce g_{m3} distortion is to increase the overdrive of the device.

Beyond the strong inversion regime, the equations are not as intuitive and useful for analog design. It can be seen from circuit models that g_m/I_D for high overdrive voltages drops until it reaches a low-level plateau.

The cut-off frequency f_T of a MOSFET is defined as the frequency at which the current gain between the drain current and the gate current source becomes unitary. It can be demonstrated that[17]:

$$f_T \approx \frac{g_m}{2\pi(C_{GS} + C_{GD})} \tag{2.7}$$

The noise of a MOSFET at high frequencies is dominated by the white noise, while the flicker or $1/f$ noise can be neglected (more specifically, this is true for all frequencies above the corner frequency beyond which the flicker noise is less than the white noise). The white thermal channel noise of a MOSFET can be expressed as [18]:

$$\frac{\overline{I_{n,ch}^2}}{\Delta f} = 4kT\gamma g_{ds0} \approx 4kT\gamma g_m \tag{2.8}$$

where g_{ds0} is the drain-source conductance at $V_{DS} = 0V$, which for long-channel devices is equal to g_m[19], and γ is the channel noise factor, a technological parameter which is roughly equal to 2/3 for long-channel devices but can be much higher for short-channel devices, depending on bias conditions. γ is the key parameter, alongside f_T and self gain, to characterize a new technological node. Other noise source, such as gate resistance noise and induced gate noise, albeit important for low-noise amplifier design, are not usually part of a technology characterization.

The test-bench circuit to obtain the cut-off frequency f_T and channel noise factor γ is reported in Figure 2.1. The resistance r is equal to either 0 Ω for the f_T test or 1 Ω for the γ test, the latter acting as a normalized load through which the output noise current will flow.

2.1 TSMC 28 nm HPC+

The first node to compare to is TSMC 28 nm HPC+ (TSMC28), a bulk CMOS technology. Albeit quite old, it is still an extremely used node in RF circuits research thanks to its good trade-off between performances, cost, reliability and number of available tape-out dates. It has multiple metal stack options and

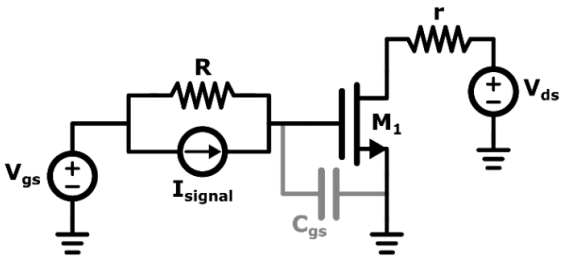


Figure 2.1: Circuit simulation setup to obtain the device cut-off frequency f_T and channel noise factor γ. r is set to 0 Ω (ideal short) for f_T testing while it is set to 1 Ω for γ testing.

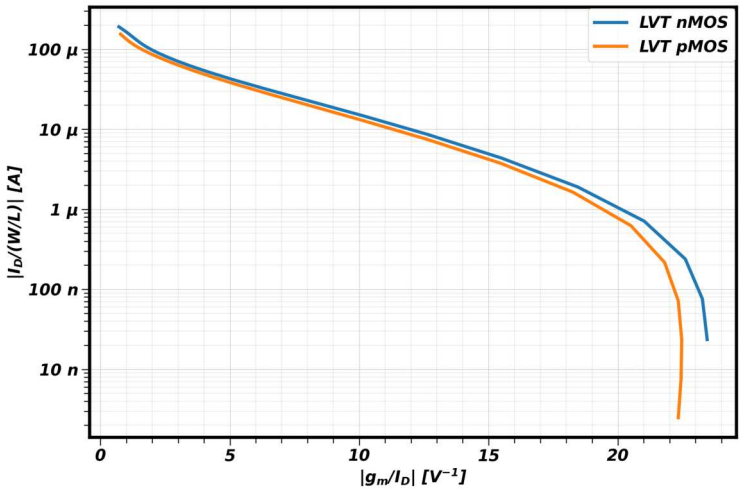


Figure 2.2: Normalized drain current $I_D/(W/L)$ of LVT nMOS and pMOS in TSMC's 28 nm HPC+ technology against g_m/I_D

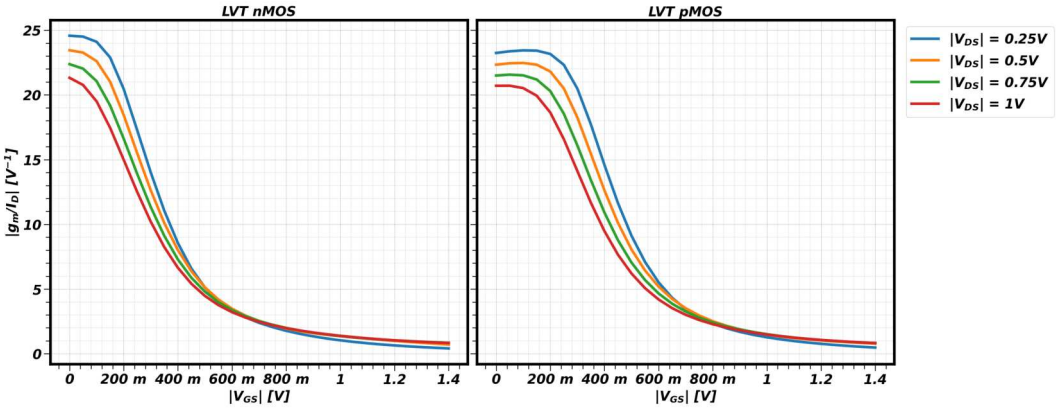


Figure 2.3: g_m/I_D vs. V_{GS} of LVT nMOS and pMOS in TSMC's 28 nm HPC+ technology for multiple V_{DS} values.

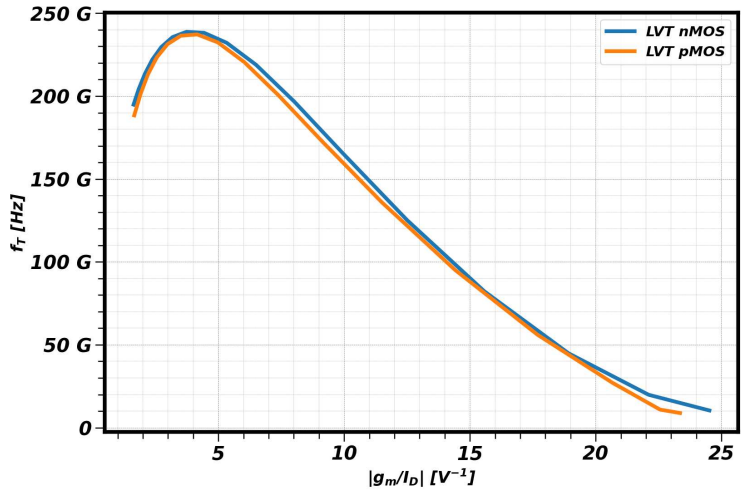


Figure 2.4: Cut-off frequency f_T of LVT nMOS and pMOS in TSMC's 28 nm HPC+ technology against g_m/I_D.

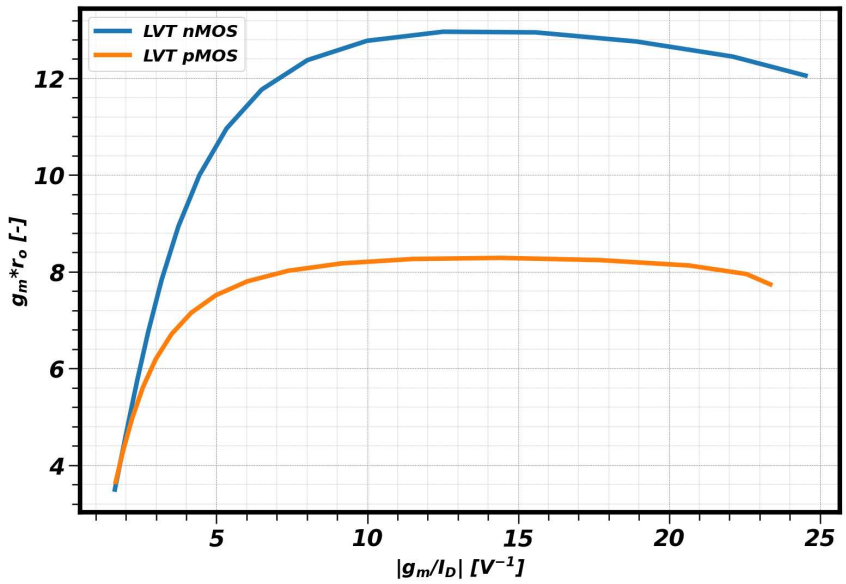


Figure 2.5: Self gain $g_m r_o$ of LVT nMOS and pMOS in TSMC's 28 nm HPC+ technology against g_m/I_D.

FETs with four different voltage thresholds available, as well as accurate RF models. A consolidated know-how about the technology was already present within the research laboratory at the start of the PhD activity, hence it has been considered as a benchmark to compare more advanced nodes to. The metal stack used in previous projects had 8 metal levels, the last of which was ultra-thick, and the most used FETs were the Low-Voltage-Threshold (LVT)

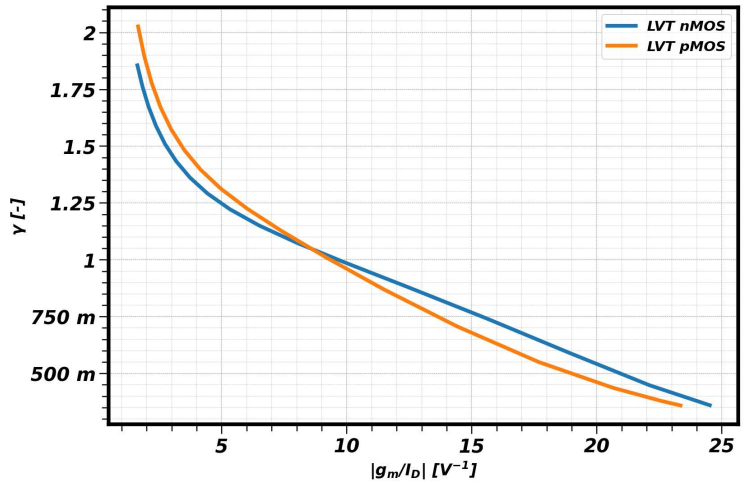


Figure 2.6: Channel noise factor γ of LVT nMOS and pMOS in TSMC's 28 nm HPC+ technology against g_m/I_D.

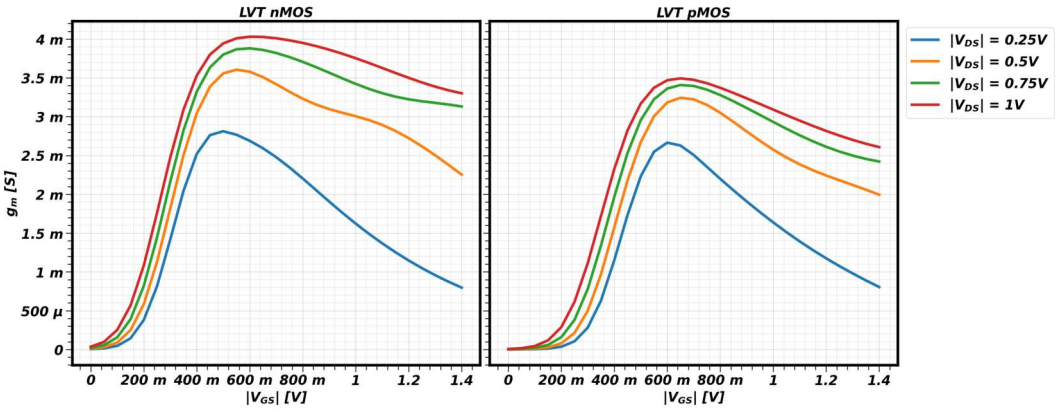


Figure 2.7: Transconductance g_m of LVT nMOS and pMOS with $W/L = 500/30$ in TSMC's 28 nm HPC+ technology against V_{GS} for multiple V_{DS} settings.

ones.

Figure 2.2 shows the normalized drain current $I_D/(W/L)$ against g_m/I_D, which is the necessary to apply the g_m/I_D methodology[16], while Figure 2.3 shows the transconductor efficiency vs. gate-source voltage for multiple drain-source voltage values of LVT nMOS and pMOS in TSMC's 28 nm HPC+ technology. Using different thresholds would simply laterally shift the curves in Figure 2.3.

Figures 2.2 and 2.3 help in choosing the right g_m/I_D for a given current consumption target and the proper gate-source voltage bias, hence the voltage supply, for the selected transconductor efficiency point, respectively. According

to the g_m/I_D methodology, from g_m/I_D, the cut-off frequency, self-gain and channel noise factor are then evaluated: if they fit the design targets, the design procedure can move on to the actual circuit design, otherwise a new g_m/I_D point has to be chosen, an successive-approximation iterative procedure [16].

The f_T, $g_m r_o$, and γ vs. g_m/I_D plots are reported in Figures 2.4, 2.5, and 2.6, respectively. As it can be seen, while the frequency and noise performances of the technology are well balanced, there's a significant difference in terms of self gain between nMOS and pMOS which needs to be take into consideration during the design procedure.

From Figure 2.4, it can be seen that f_T has a peak when the device is pushed into overdrive. The bias point for high-frequencies designs inevitably has to be close to such point. However, from Figure 2.5 it can be seen that $g_m r_o$ has almost the opposite behavior, plateauing around its maximum for small overdrive values. This inevitably leads to a trade-off in choosing the bias point, which is informed by Figure 2.6 as well. A g_m/I_D between 5 and 10 V^{-1} is typical for high-frequency designs. As a reference, g_m vs. V_{GS} for different V_{DS} values for LVT devices sized with $W/L = 500/30$ is reported in Figure 2.7.

2.2 GlobalFoundries 22 nm FDX FDSOI

Fully-Depleted Silicon-On-Insulator technologies are becoming increasingly used in RF designs for their versatility, performances, and trade-off with cost: usually more expensive than bulk CMOS but less than FinFET, they offer frequency performances close if not superior to both but cannot afford the same level of integration with digital structures as FinFET. The FDSOI technology considered here is the 22 nm FDX by GlobalFoundries (GF22)[15]. No previous know-how was present within the laboratory at the start of the PhD activities, so the characterization of such technology was intended both as a comparison for FinFET and a useful reference for future designs. Indeed, within the framework of this PhD, the design of a Low-Noise Amplifier for optical receivers in GF22 technology was analyzed, and a full optical receiver is actively being designed by another PhD student starting from such preliminary analysis, which

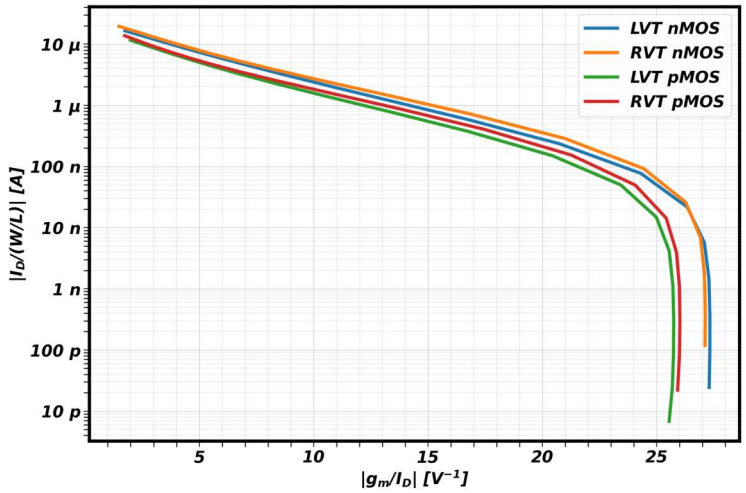


Figure 2.8: Normalized drain current $I_D/(W/L)$ of LVT/RVT nMOS and pMOS in GlobalFoundries' 22 nm FDSOI technology against g_m/I_D

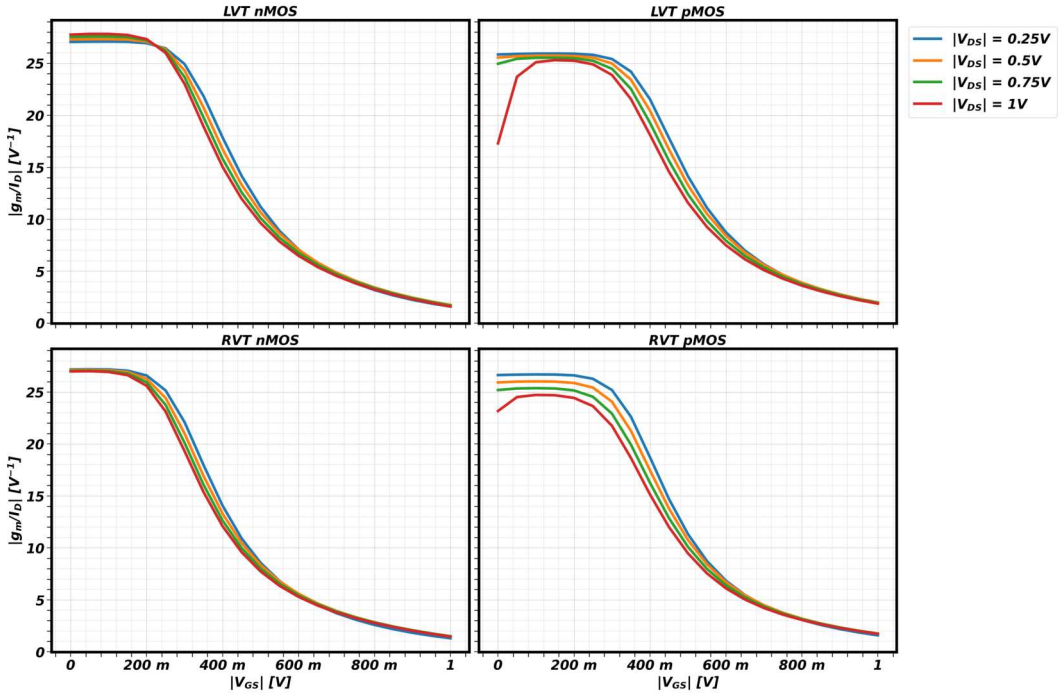


Figure 2.9: g_m/I_D vs. V_{GS} of LVT/RVT nMOS and pMOS in GlobalFoundries' 22 nm FDSOI technology for multiple V_{DS} values.

is reported later in this thesis.

GF22, like TSMC28, offers multiple back-end-of-the-line (BEOL) metallization options (the one available for the characterization had 10 metals) and FETs with four different voltage threshold. It also offers both RF and

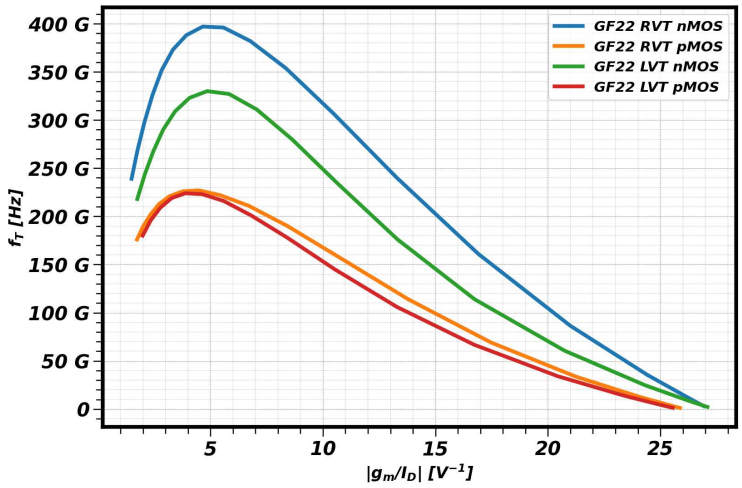


Figure 2.10: Cut-off frequency f_T of LVT/RVT nMOS and pMOS in GlobalFoundries' 22 nm FDSOI technology against g_m/I_D.

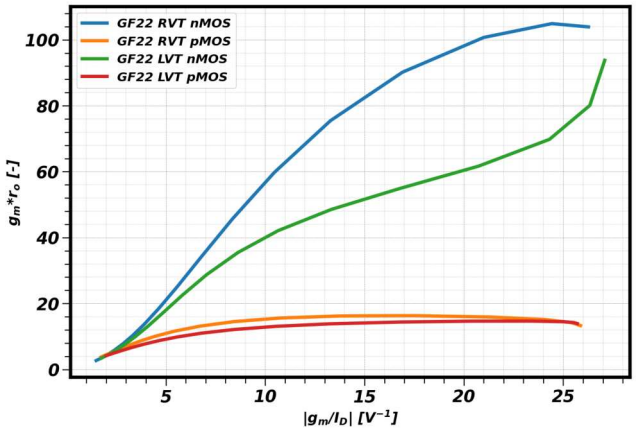


Figure 2.11: Self gain $g_m r_o$ of LVT/RVT nMOS and pMOS in GlobalFoundries' 22 nm FDSOI technology against g_m/I_D.

millimeter-wave FET models, the latter being extremely accurate in frequency performances when compared to post-layout simulations. For this reason, the results reported below where obtained from millimeter-wave models.

Figure 2.8 reports the normalized drain current vs. g_m/I_D while Figure 2.9 reports the transconductor efficiency against the gate-source voltage. The cut-off frequency, self gain, and channel noise factor are plotted against g_m/I_D in Figures 2.10, 2.11, and 2.12, respectively, while Figure 2.13 shows the devices' transconductances against V_{GS} for multiple V_{DS} settings and $W/L = 4000/20$, as a design reference.

It can be seen that, while the nMOSFETs performances are extremely

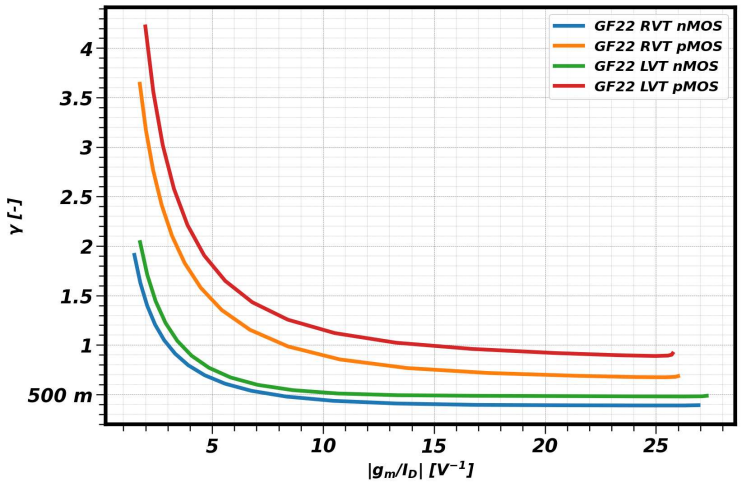


Figure 2.12: Channel noise factor γ of LVT/RVT nMOS and pMOS in GlobalFoundries' 22 nm FDSOI technology against g_m/I_D.

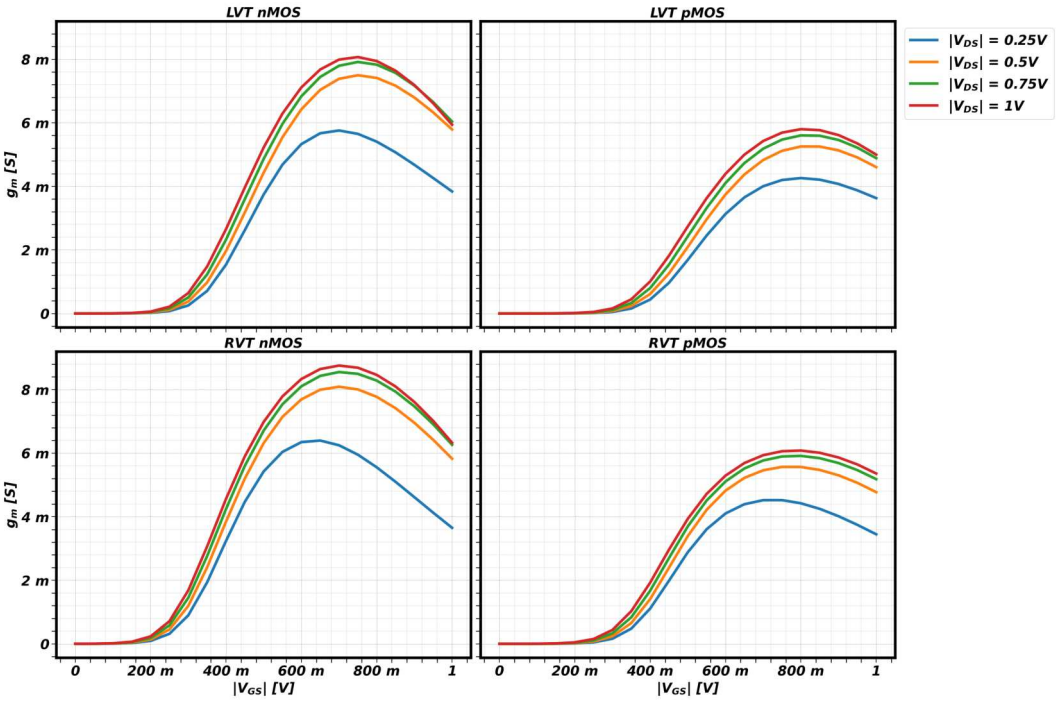


Figure 2.13: Transconductance g_m of LVT/RVT nMOS and pMOS with $W/L = 4000/20$ in GlobalFoundries' 22 nm FDSOI technology against V_{GS} for multiple V_{DS} settings.

good, there is a huge gap between nMOS and pMOS, both in terms of cut-off frequency and self-gain (Figures 2.10 and 2.11). This makes it difficult to design inverter-based topologies, making n-only topologies more likely to be used, thanks to the excellent performances of the nMOS. However, in broad-

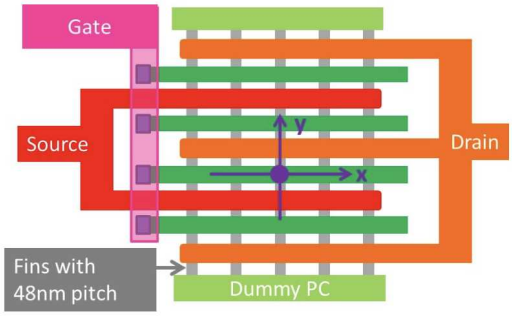


Figure 2.14: Top view graphical representation of a typical Fin-Field-Effect-Transistor (from [14]).

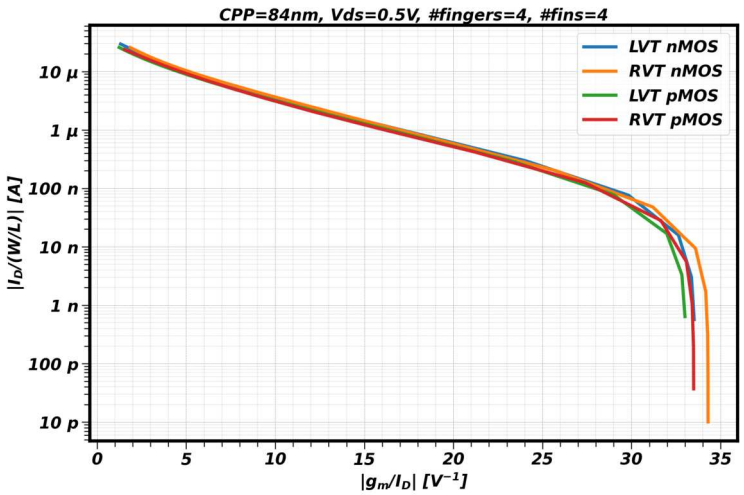


Figure 2.15: Normalized drain current $I_D/(W/L)$ of LVT/RVT nMOS and pMOS in GlobalFoundries' 12 nm FinFET technology against g_m/I_D

band high-frequency amplifier design, inverters are usually the best choice in terms of gain, power consumption and bandwidth.

2.3 GlobalFoundries 12 nm FinFET

FinFET technologies are becoming more popular as access to advanced nodes (such as 16 or 12 nm), which are not on the cutting edge anymore, is encouraged by foundries. As entry costs barriers soften, more and more researchers are reporting promising results for FinFET RF/HF designs, pointing towards a possible wider adoption of such technologies beyond VLSI digital chips. The chosen technology was GlobalFoundries' 12 nm LP+ FinFET (GF12)[14]. Like

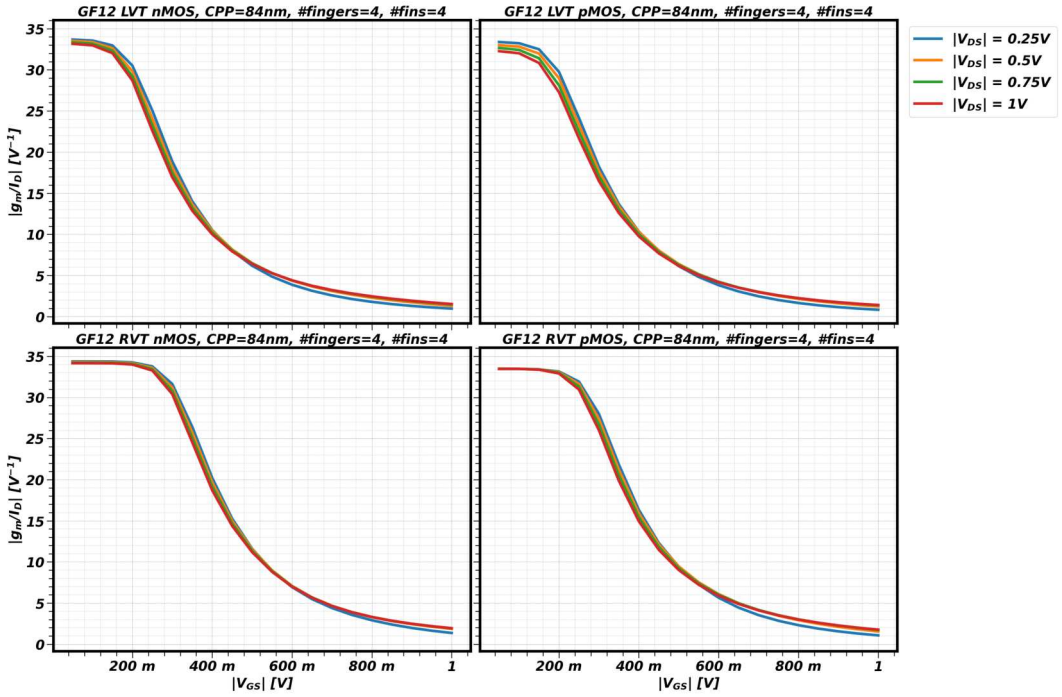


Figure 2.16: g_m/I_D vs. V_{GS} of LVT/RVT nMOS and pMOS in GlobalFoundries' 12 nm FinFET technology for multiple V_{DS} values.

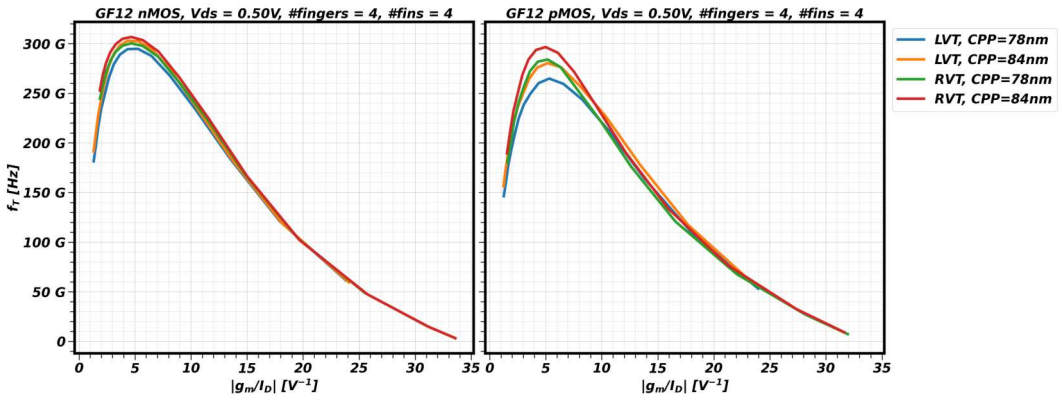


Figure 2.17: Cut-off frequency f_T of LVT/RVT nMOS and pMOS in GlobalFoundries' 12 nm FinFET technology against g_m/I_D.

the previous technologies, GF12 offers multiple BEOL metallization options and devices with four different threshold voltages. The metal stack which was used for the subsequent design has 13 metals, of which the two top metals are low-resistivity and identical to each other, which helps in creating two distributed metal planes, one for ground and the other one for V_{DD}, that greatly reduce parasitic resistances and inductances on the supplies.

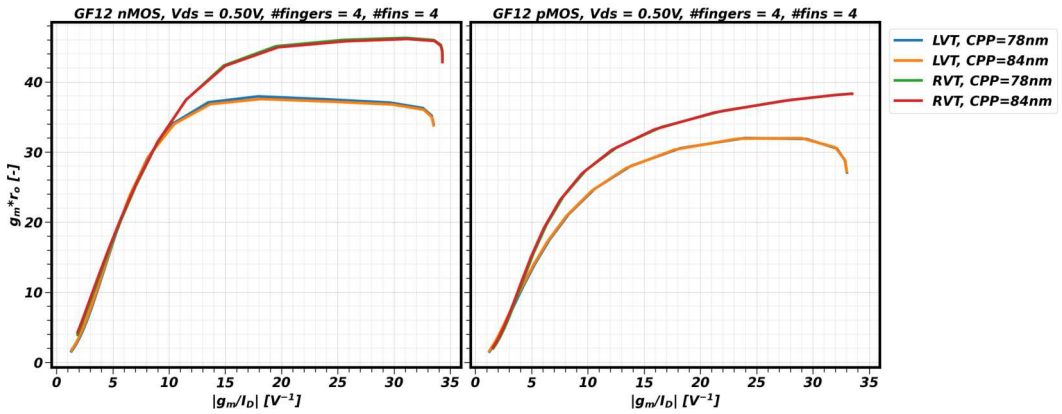


Figure 2.18: Self gain $g_m r_o$ of LVT/RVT nMOS and pMOS in GlobalFoundries' 12 nm FinFET technology against g_m/I_D.

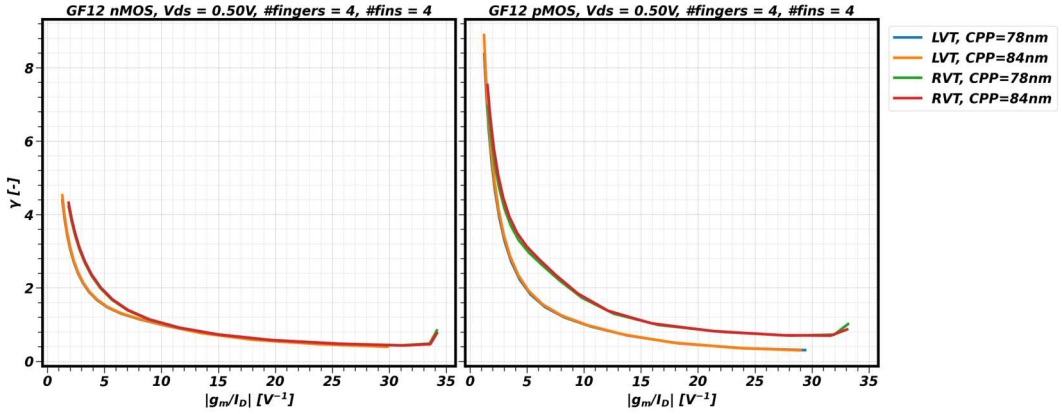


Figure 2.19: Channel noise factor γ of LVT/RVT nMOS and pMOS in GlobalFoundries' 12 nm FinFET technology against g_m/I_D.

As for GF22, no previous know-how was available within the laboratory. Unlike GF22, however, GF12 do not offer access to RF models. More so, the available models are extremely inaccurate if a software switch, called "pre-layout switch", is not correctly activated by adding a design variable in the simulation tool called "pre_layout_switch" and setting it to 1. Such software switch ensures the device model accounts for additional contact and metal parasitics which greatly impact the device performances and cannot be avoided anyway.

Figure 2.14 shows the top view of a typical FinFET device. To get an intuitive understanding of the functioning of FinFET with respect to bulk CMOS, one can think of FinFET as being made of multiple fixed-length conductive channels which are located at every intersection of the gate fingers and the

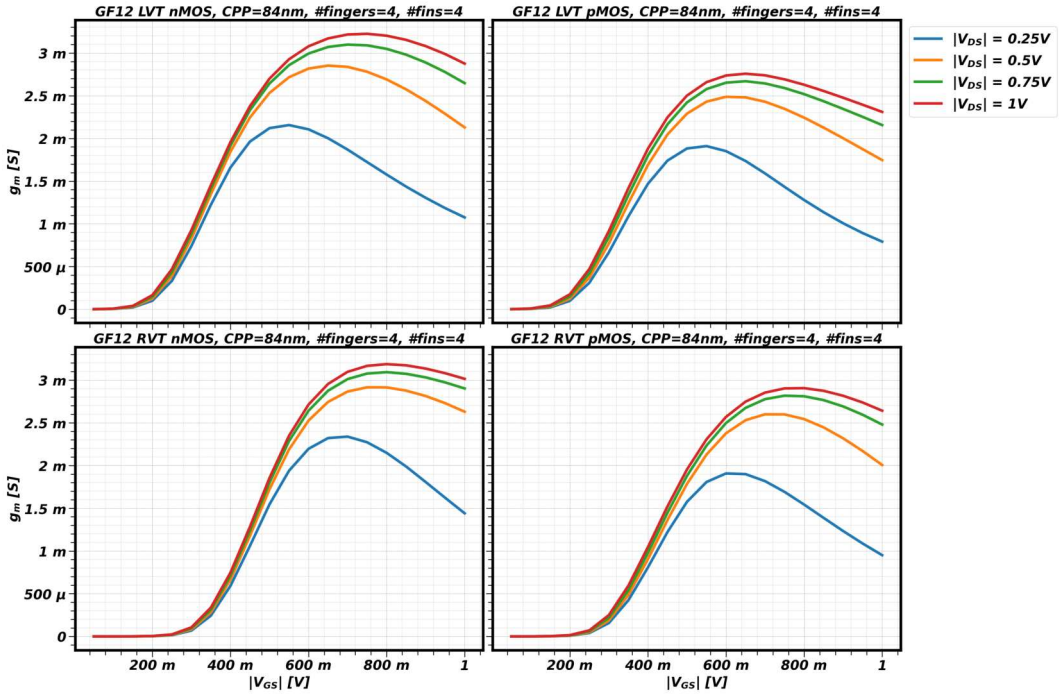


Figure 2.20: Transconductance g_m of LVT/RVT nMOS and pMOS with $W/L = 4000/20$ in GlobalFoundries' 12 nm FinFET technology against V_{GS} for multiple V_{DS} settings.

fins. The length of such channels is fixed to 14 nm from the device properties, while the total device width is determined by the number of fingers times the number of fins multiplied by the fin spacing, which is fixed to 48 nm. Hence, a device with four fingers and four fins will have an aspect ratio of $W/L = 4 * 4 * 48nm/14nm$. The distance between the gate fingers is called "Contacted Poly Pitch" (CPP) and can be set to either 78 or 84 nm. The greater the CPP, the better the frequency performances of the device but also the less dense the layout will inevitably be.

Due to self-aligned double patterning (SADP) in the fins, poly and lower metals fabrication, the fin width will be subject to a long-short-long-short pattern. To compensate such variations, it is necessary to always use an even number of fins greater than four at least. However, using more than 10 fins imply an excessive finger width, hence gate resistance and its associated noise. This then means that the only possible numbers of fins is 4, 6, or 8, the first of which will be the default choice from here on unless otherwise stated.

Figure 2.15 reports the normalized drain current vs. g_m/I_D while Figure 2.16 reports the transconductor efficiency against the gate-source volt-

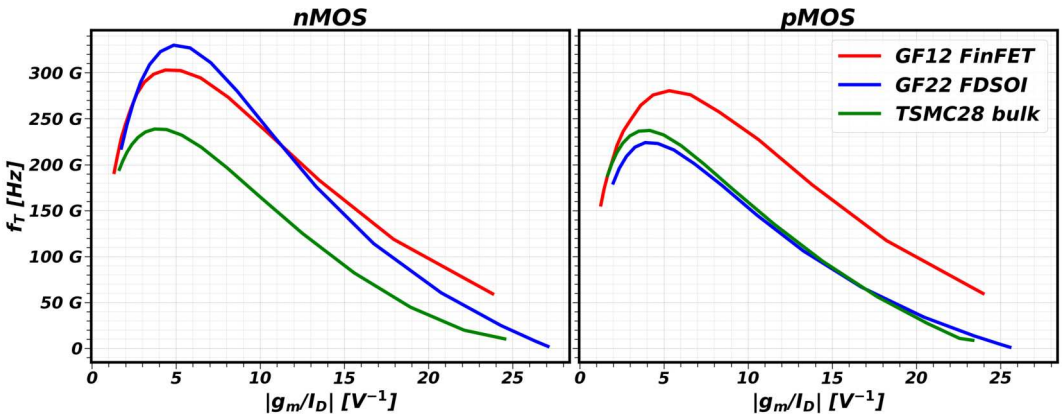


Figure 2.21: Comparison of the cut-off frequency f_T against g_m/I_D for TSMC's 28 nm HPC+ bulk CMOS and GlobalFoundries' 22 nm FDX FDSOI and 12 nm LP+ FinFET LVT devices.

age. The cut-off frequency, self gain, and channel noise factor are plotted against g_m/I_D in Figures 2.17, 2.18, and 2.19, respectively, while Figure 2.20 shows the devices' transconductances against V_{GS} for multiple V_{DS} settings and $W/L = 4 * 4 * 48/14$, as a design reference. These figures show that the pMOS and nMOS devices are better balanced than in the GF22 case. As it can be seen from the f_T plot in Figure 2.17, choosing CPP=84 nm is mandatory for high-frequency designs, as it leads to an increase in the peak cut-off frequency, particularly for pMOS, even if it leads to a lower self gain, as it can be seen from Figure 2.18. Choosing CPP=84 nm leads to a lower channel noise factor as well (see Figure 2.19).

2.4 Technologies Comparison

To better compare the three aforementioned technologies, the f_T, $g_m r_o$, and γ vs. g_m/I_D plots are reported here for each node beside one another in Figures 2.21, 2.22, and 2.23, respectively. Only the LVT devices have been used. It can be seen that GF12 provides a substantial peak f_T and maximum self gain increase with respect to TSMC28 and GF22 pMOS. GF22 nMOS outperforms GF12 nMOS, however the FinFET technology provides a more balanced compromise between nMOS and pMOS. The channel noise factor is higher than both TSMC28 and GF22, instead. All considered, GF12 is a promising candidate for high-frequency designs.

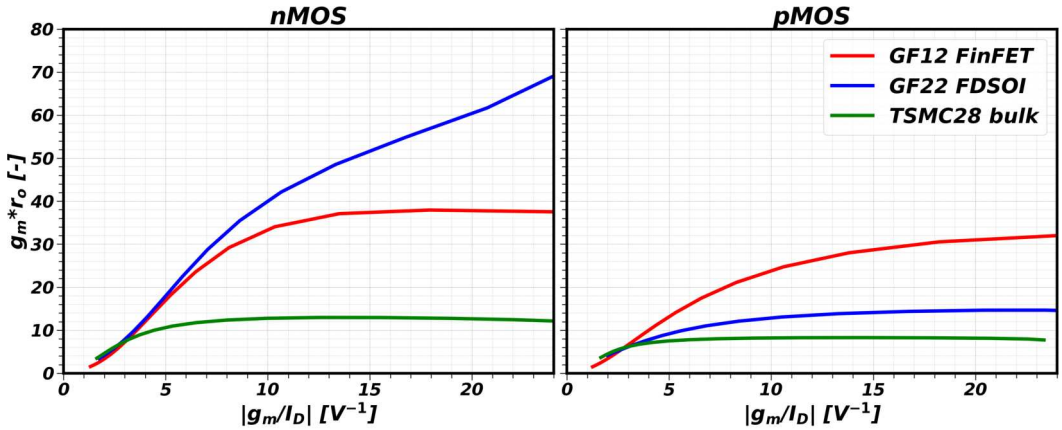


Figure 2.22: Comparison of the self gain $g_m r_o$ against g_m/I_D for TSMC's 28 nm HPC+ bulk CMOS and GlobalFoundries' 22 nm FDX FDSOI and 12 nm FinFET LVT devices.

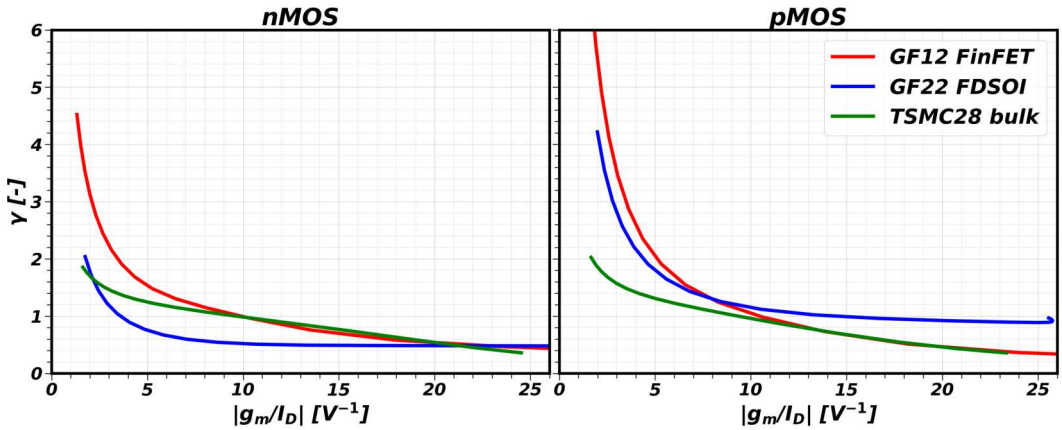


Figure 2.23: Comparison of the channel noise factor γ against g_m/I_D for TSMC's 28 nm HPC+ bulk CMOS and GlobalFoundries' 22 nm FDX FDSOI and 12 nm FinFET LVT devices.

Chapter 3

Analysis of Shunt-Feedback TIA

In this chapter, the CMOS shunt-feedback (SF) LNTA will be analyzed, with focus on peaking techniques to extend the bandwidth without compromising on noise. Among the multiple TIA topologies which are used for CMOS LNTAs, this is by far the most popular alongside the common-gate (CG) TIA. The SF TIA is more common in CMOS LNTAs thanks to its (usually) lower noise and its higher compatibility with the voltage scaling associated with more advanced technological nodes, albeit loop stability has to be taken into the design picture[20]. Indeed, the loop core amplifier in SF TIAs can easily be implemented with CMOS inverters, while CG TIAs require at least three stacked MOSFETs. The SF TIA analysis carried out here can also be applied to the Cherry-Hooper voltage amplifier topology, a cascade of a transconductor stage, which can be implemented with inverters, and a transimpedance stage[21]. This is because the input source of the LNTA is a high-impedance current source, which can also be said of Cherry-Hooper voltage amplifier if a cascode topology is used as transconductor, which boosts its output impedance.

Figure 3.1 shows the inverter-based (IB) SF LNTA which will be analyzed in this chapter. Figure 3.1 does not show any bandwidth extension technique, which will be dealt with later in this chapter. The PD is connected to the input of the LNTA through a pad protected with an ESD diode, which presents a certain parasitic capacitance to ground.

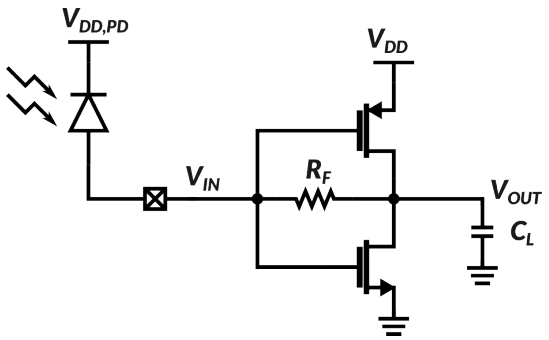


Figure 3.1: Considered LNTA circuit with photodiode (PD).

3.1 Photodiode Model

Before analyzing the circuit, it can be beneficial to take a look at the small-signal behavior of the photodiode. A PD is essentially a strongly reversed-biased diode which, thanks to its high depletion region electric field, accelerates towards the anode/cathode the charge carriers promoted to the conduction (valence) energy band by the incident light from the optical fiber. In this way, an electrical current proportional to the optical signal power is created, flowing into the oRX AFE. Being a reversed-biased diode, it can be approximated as a capacitance which is proportional to the depletion region dimensions. However, this simple picture gets complicated by parasitic elements linked to the packaging of the PD and the finite carrier speed inside the PD medium.

The complete PD small-signal model is shown in Figure 3.2 on the left, where C_{PD} is the PD capacitance, R_S the PD contact parasitic series resistance, L_{WB} the parasitic inductances of the PD's cathode and anode connections. The PD current, I_{PD}, can be approximated as a first-order low-pass filtered version of the input current, I_{IN}, due to the finite carrier transit time τ_t in the PD junction depletion region. I_{IN} is linked to the optical input power through the PD responsivity R, a technological constant that depends on the optical signal wavelength λ_{opt}:

$$I_{PD} = \frac{I_{IN}}{1 + s/\omega_t} = \frac{R \cdot P_{IN,opt}}{1 + s\tau_t} \tag{3.1}$$

where ω_t is the angular frequency associated to the PD carrier transit time τ_t (assumed to be equal to 1.77 ps).

A Norton equivalent circuit of the photodiode can be used to simplify circuit analysis, as shown on the right in Figure 3.2. The Norton equivalent

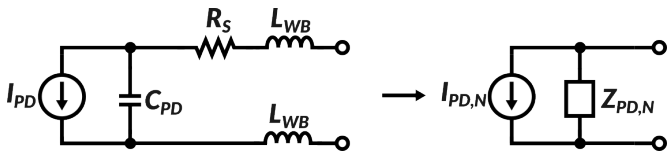


Figure 3.2: Norton equivalent circuit of the PD small-signal model.

short-circuit current and impedance are equal to:

$$I_{PD,N} = \frac{I_{PD}}{1 + sR_SC_{PD} + s^2 2L_{WB}C_{PD}} \tag{3.2}$$

$$Z_{PD,N} = \frac{1 + sR_SC_{PD} + s^2 2L_{WB}C_{PD}}{sC_{PD}} \tag{3.3}$$

where I_{PD} in Equation 3.2 is the photodiode current in Equation 3.1. If R_S and L_{WB} are not taken into account, then $I_{PD,N} = I_{PD}$ and $Z_{PD,N} = 1/sC_{PD}$, as expected. As it can be seen, without even considering the LNTA, $I_{PD,N}/P_{IN,opt}$ is already a third-order function. The effect of the PD model would be shown later in this chapter.

3.2 Circuit Analysis Without Bandwidth Extension

To alleviate the complexity so as to focus on the TIA circuit design, a simplified PD model is considered, without τ_t, R_S and L_{WB}. The new small-signal circuit is shown in Figure 3.31, where $C_{IN} = C_{PD} + C_{PAD} + C_{ESD} + C_{GS,n} + C_{GS,p}$ accounts for the photodiode, pad and ESD diode parasitic capacitances, as well as the gate-source capacitances of the nMOS and pMOS of the inverter, $C_F = C_{GD,n} + C_{GD,p}$ accounts for the gate-drain capacitances within the inverter, $G_m = g_{m,n} + g_{m,p}$ is the inverter transconductance, and $R_L = r_{o,n}//r_{o,p}$ is the inverter output resistance.

The value for the small-signal parameters used in simulations is reported in Table 3.1, except for the parameters which have been swept to see their effect on the transfer function and noise. These values are close to the ones used for the chip design in the next chapter, and are the result of careful consideration over the project targets set by the partner company which will be explained later. For now, they simply constitute the starting point for the simulations.

Small-signal parameter	Default value
C_{PD}	25 fF
$C_{PAD+ESD}$	50 fF
G_m	160 mS
R_F	140 Ω
R_L	100 Ω
C_L	145 fF
C_F	35 fF
C_G	60 fF

Table 3.1: Default values of the small-signal parameters in the circuit reported in Figure 3.3. C_G stands for the parasitic capacitance between the gate of the inverter and ground, and will be useful later on in section 3.3.

The direction of the small-signal photodiode current is assumed to be as displayed in Figure 3.3 for convenience, so as to have avoid a negative sign in front of the transimpedance transfer function. However, if assumed to be the opposite, it suffices to apply a negative sign in front of the transimpedance results reported later.

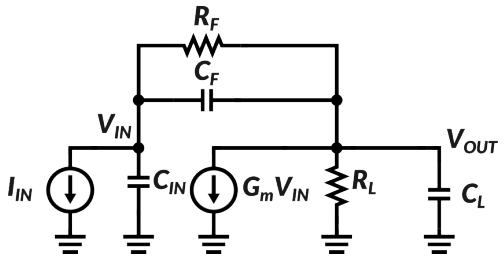


Figure 3.3: Simplified small-signal circuit of the considered TIA.

Low-Frequency Behavior

At low frequencies, the TIA loop gain G_{LOOP}, input resistance R_{IN}, output resistance R_O and transresistance R_T are:

$$G_{LOOP} = G_m R_L \tag{3.4}$$

$$R_T = \frac{V_{OUT}}{I_{IN}} = R_L \frac{G_m R_F - 1}{1 + G_m R_L} = \frac{G_{LOOP}}{1 + G_{LOOP}} \left(R_F - \frac{1}{G_m} \right) \tag{3.5}$$

$$R_{IN} = \frac{V_{IN}}{-I_{IN}} = \frac{R_F + R_L}{1 + G_m R_L} = \frac{R_F + R_L}{1 + G_{LOOP}} = \frac{G_{LOOP}}{1 + G_{LOOP}} \cdot \frac{R_F + R_L}{G_m R_L} \tag{3.6}$$

$$R_O = \left.\frac{V_O}{I_O}\right|_{I_{IN}=0} = \frac{R_L}{1 + G_m R_L} = \frac{R_L}{1 + G_{LOOP}} = \frac{G_{LOOP}}{1 + G_{LOOP}} \cdot \frac{1}{G_m} \tag{3.7}$$

Equation 3.7 can be inserted into Equation 3.5 so as to obtain:

$$R_T = R_O(G_m R_F - 1) \tag{3.8}$$

If $G_m R_L \gg 1$, $G_m R_F \gg 1$ and $R_L \gg R_F$, the above equations simplify to $R_T \approx R_F$, $R_{IN} \approx 1/G_m$ and $R_O \approx 1/G_m$, which are well-known results.

High-Frequency Behavior

At higher frequencies, the TIA loop gain G_{LOOP}, input impedance Z_{IN}, output impedance Z_O and transimpedance Z_T can be expressed as:

$$\begin{aligned} G_{LOOP} = G_m R_L \cdot \frac{(1 + sR_F C_F)}{1 + s[R_L(C_{IN} + C_L) + R_F(C_{IN} + C_F)] +} \cdots \\ \cdots \frac{}{+ s^2 R_L R_F (C_L C_F + C_L C_{IN} + C_F C_{IN})} \end{aligned} \tag{3.9}$$

$$Z_T = R_L \frac{G_m R_F - 1}{1 + G_m R_L} \cdot \frac{1 - s\frac{R_F C_F}{G_m R_F - 1}}{1 + s(R_F C_F + \frac{R_L C_L + R_L C_{IN} + R_F C_{IN}}{1 + G_m R_L}) + s^2 R_L R_F \frac{C_L C_F + C_F C_{IN} + C_L C_{IN}}{1 + G_m R_L}} \tag{3.10}$$

$$Z_{IN} = \frac{R_F + R_L}{1 + G_m R_L} \cdot \frac{1 + s(R_F // R_L)(C_F + C_L)}{1 + s(R_F C_F + \frac{R_L C_L + R_L C_{IN} + R_F C_{IN}}{1 + G_m R_L}) + s^2 R_L R_F \frac{C_L C_F + C_F C_{IN} + C_L C_{IN}}{1 + G_m R_L}} \tag{3.11}$$

$$Z_O = \frac{R_L}{1 + G_m R_L} \cdot \frac{1 + sR_F(C_F + C_{IN})}{1 + s(R_F C_F + \frac{R_L C_L + R_L C_{IN} + R_F C_{IN}}{1 + G_m R_L}) + s^2 R_L R_F \frac{C_L C_F + C_F C_{IN} + C_L C_{IN}}{1 + G_m R_L}} \tag{3.12}$$

From Equation 3.10, it can be seen that Z_T has two complex poles at:

$$\omega_{p1,2} = \sqrt{\frac{1 + G_m R_L}{R_L R_F (C_L C_F + C_F C_{IN} + C_L C_{IN})}} \tag{3.13}$$

with quality factor:

$$Q = \frac{\sqrt{(1 + G_m R_L) R_L R_F (C_L C_F + C_F C_{IN} + C_L C_{IN})}}{R_F C_F (1 + G_m R_L) + R_F C_{IN} + R_L (C_L + C_{IN})} \tag{3.14}$$

which are the poles of Z_{IN} and Z_O as well. If we disregard the zero, then it can be demonstrated that the -3 dB bandwidth (that is, the frequency at which $|Z_T(f)|^2 = Z_{T0}^2/2$, where Z_{T0} is the mid-band gain in Equation 3.5) is linked to $\omega_{p1,2}$ and Q as:

$$BW = \frac{\omega_{p1,2}}{2\pi}\sqrt{1 - \frac{1}{2Q^2} + \sqrt{1 + \left(1 - \frac{1}{2Q^2}\right)^2}} \tag{3.15}$$

If $G_m R_L \gg 1$:

$$\omega_{p1,2} \approx \sqrt{\frac{G_m}{R_F(C_L C_F + C_F C_{IN} + C_L C_{IN})}} \tag{3.16}$$

$$Q_{1,2} \approx \frac{\sqrt{G_m R_F(C_L C_F + C_F C_{IN} + C_L C_{IN})}}{G_m R_F C_F + C_L + C_{IN}\left(1 + \frac{R_F}{R_L}\right)} \tag{3.17}$$

Further approximations of equations 3.16 and 3.17 can lead to arbitrary choices due to C_L being close to the value of C_{IN} in practical implementations and C_F being close to half of C_G in advanced FinFET nodes. However, it can be noticed that if $G_m R_F$ is high enough (which is desirable to maximize the transimpedance gain), then $Q_{1,2}$ is approximately proportional $1/\sqrt{G_m R_F}$, which points to a trade-off between the transimpedance gain and the poles' Q.

Equation 3.10 also shows that Z_T has one right-hand-plane (RHP) zero at the frequency $\omega_z = (G_m R_F - 1)/(R_F C_F)$, which is much higher than $\omega_{p1,2}$. Hence, if $G_m R_F, G_m R_L \gg 1$, Z_T can be approximated as:

$$Z_T \approx \frac{R_F}{1 + s(R_F C_F + \frac{C_L + C_{IN}}{G_m} + \frac{R_F C_{IN}}{G_m R_L}) + s^2 R_F \frac{C_L C_F + C_F C_{IN} + C_L C_{IN}}{G_m}} \tag{3.18}$$

G_{LOOP}, Z_{IN} and Z_O also has one zero each, albeit always on the left-hand side of the complex plane, unlike Z_T. However, the zero frequencies are close enough to the poles that no approximations can be done like in the Z_T case.

3.2.1 Transfer Function Plots with Ideal Model

The circuit in Figure 3.3 was computer simulated with ideal components in order to see the effect of every single small-signal parameter, particularly the parasitic capacitances of the inverter, which would have been otherwise impossible to tune without changing the other parameters as well. Figures 3.4, 3.5,

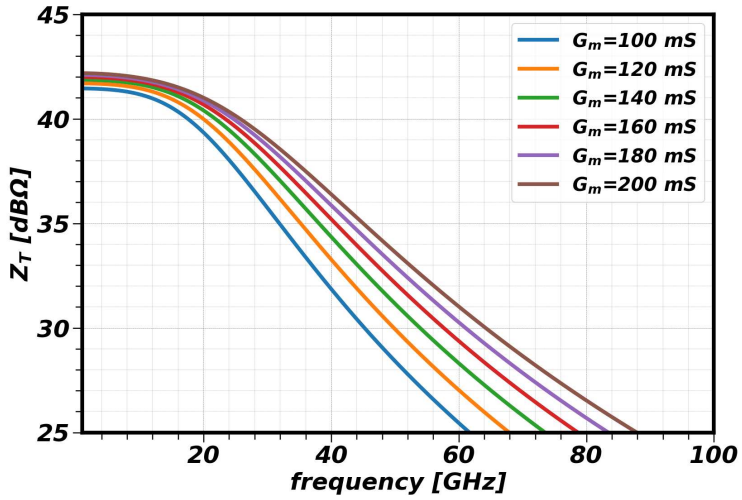


Figure 3.4: Frequency behavior of transimpedance gain of the circuit in Figure 3.3 when varying G_m. All the other small-signal parameters are set to default values reported in Table 3.1.

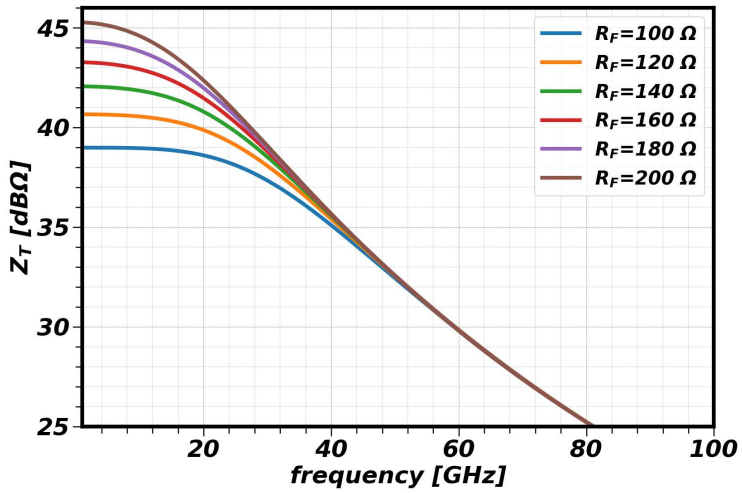


Figure 3.5: Frequency behavior of transimpedance gain of the circuit in Figure 3.3 when varying R_F. All the other small-signal parameters are set to default values reported in Table 3.1.

and 3.6 reports the effect on the transconductance gain frequency behavior of G_m, R_F, and R_L, respectively.

While analyzing a circuit to understand its behavior, it is often useful to use scalar figures of merit. Figures 3.7, 3.8, and 3.9 report what happens to the -3 dB bandwidth and DC (mid-band) gain when G_m, R_F, and R_L are swept, respectively. The vertical axis scale is not the same for all the plots. From these figures, it is easy to see that R_L plays a minor role, while R_F is crucial,

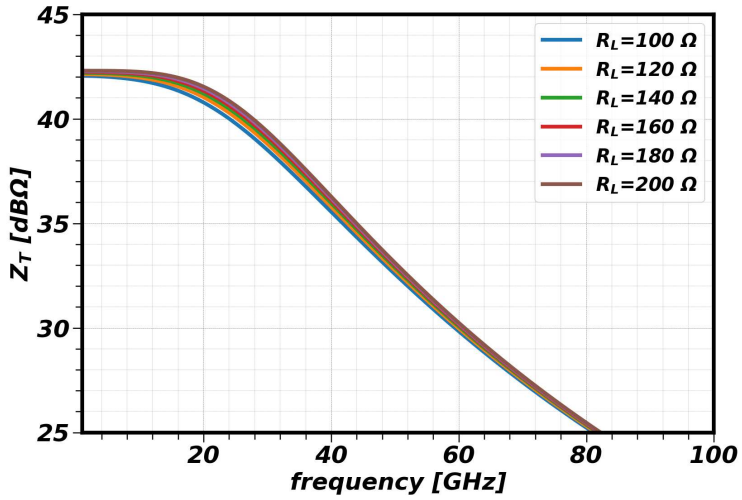


Figure 3.6: Frequency behavior of transimpedance gain of the circuit in Figure 3.3 when varying R_L. All the other small-signal parameters are set to default values reported in Table 3.1.

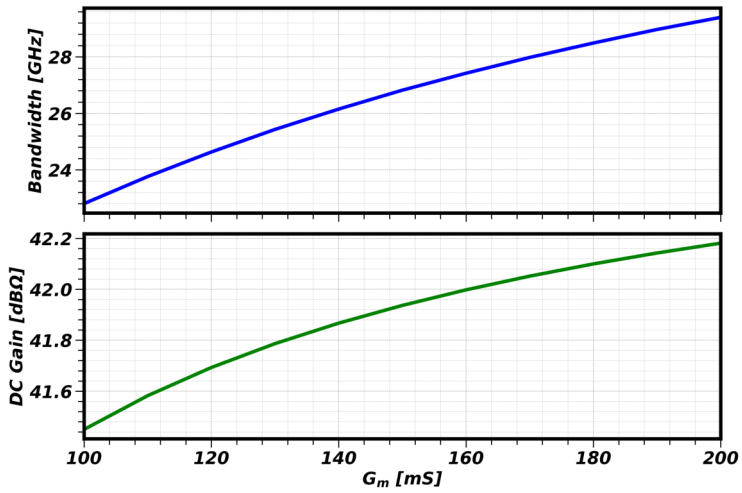


Figure 3.7: Bandwidth and DC Gain of the transfer function of the circuit in Figure 3.3 when varying G_m. All the other small-signal parameters are set to default values reported in Table 3.1.

as expected, and G_m impacts more the bandwidth than the DC gain, due to input and output impedances being approximately $1/G_m$.

The parasitic capacitances of course affect the circuit frequency behavior, albeit some more than others. Figures 3.10, 3.11, and 3.12 reports the effect on the transconductance gain frequency behavior of C_{IN}, C_L, and C_F, respectively. It can be noticed how the C_F produces the most visible effect on the transfer function, pushing the poles closer to the imaginary axis as it becomes

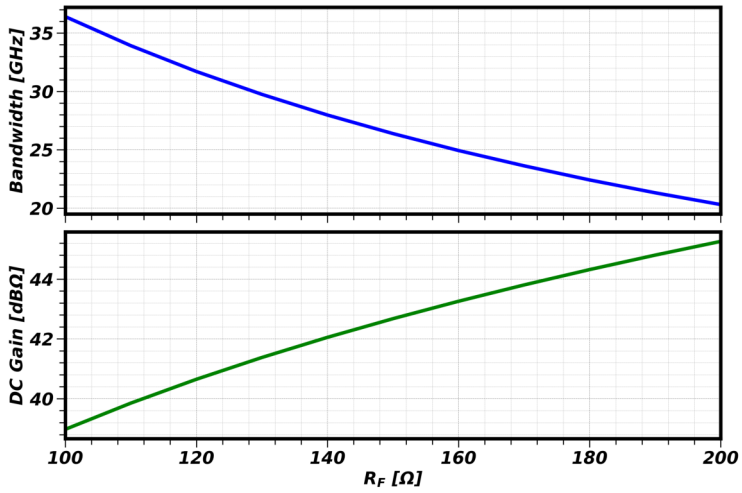


Figure 3.8: Bandwidth and DC Gain of the transfer function of the circuit in Figure 3.3 when varying R_F. All the other small-signal parameters are set to default values reported in Table 3.1.

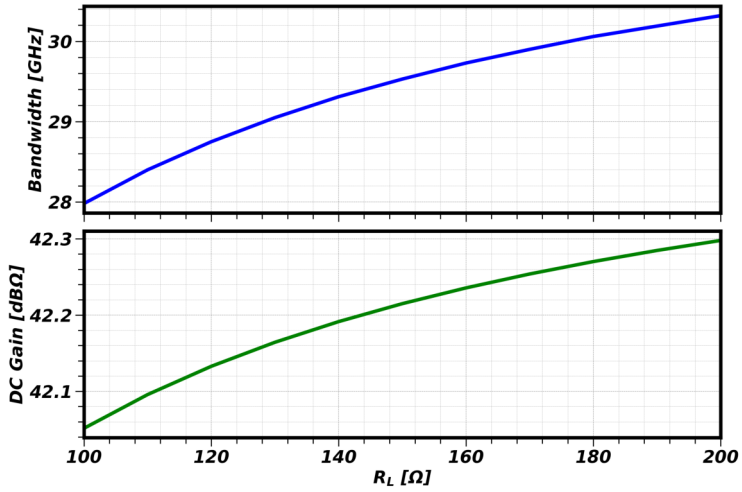


Figure 3.9: Bandwidth and DC Gain of the transfer function of the circuit in Figure 3.3 when varying R_L. All the other small-signal parameters are set to default values reported in Table 3.1.

lower and lower. This is even more evident when looking at how the -3 dB bandwidth changes when varying C_{IN}, C_L, and C_F, reported in Figures 3.13, 3.14, and 3.15, respectively.

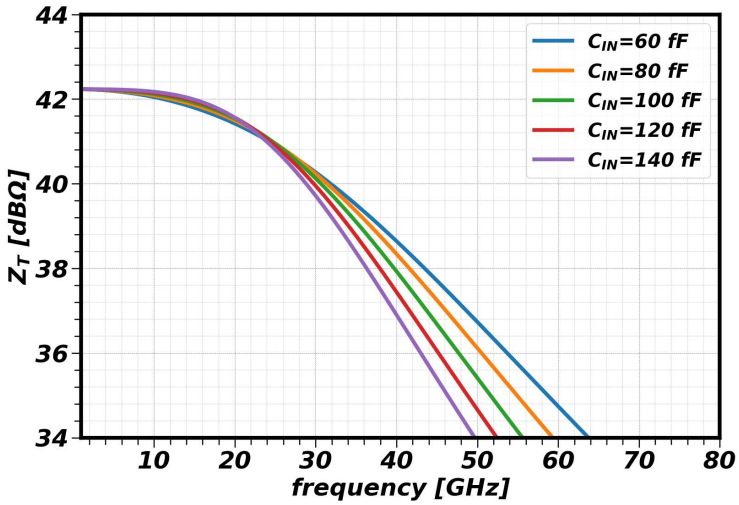


Figure 3.10: Frequency behavior of transimpedance gain of the circuit in Figure 3.3 when varying C_{IN}. All the other small-signal parameters are set to default values reported in Table 3.1.

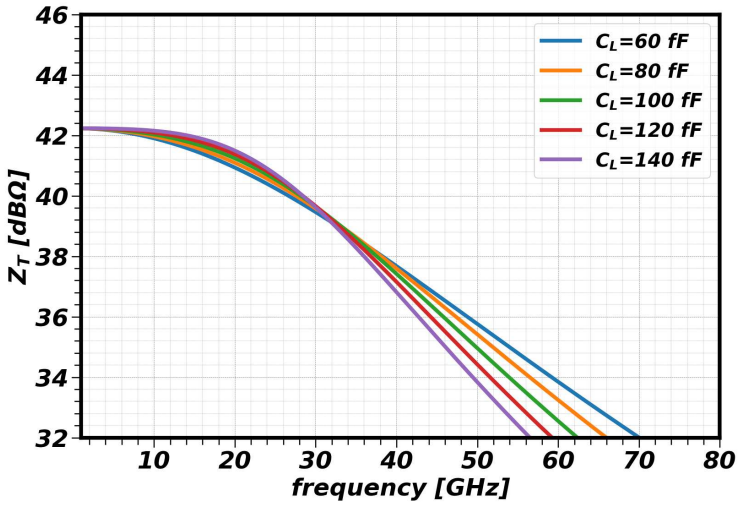


Figure 3.11: Frequency behavior of transimpedance gain of the circuit in Figure 3.3 when varying C_L. All the other small-signal parameters are set to default values reported in Table 3.1.

3.2.2 Transfer Function Plots with Circuit Simulations

The previous plots were obtained with an ideal model that implemented the circuit in Figure 3.3. The same plots vary slightly when obtained from circuit simulations using a real technology Process-Design-Kit (PDK), not only because of non-linear effects but also because some of the parameters used above are not directly accessible anymore without affecting other parameters as well.

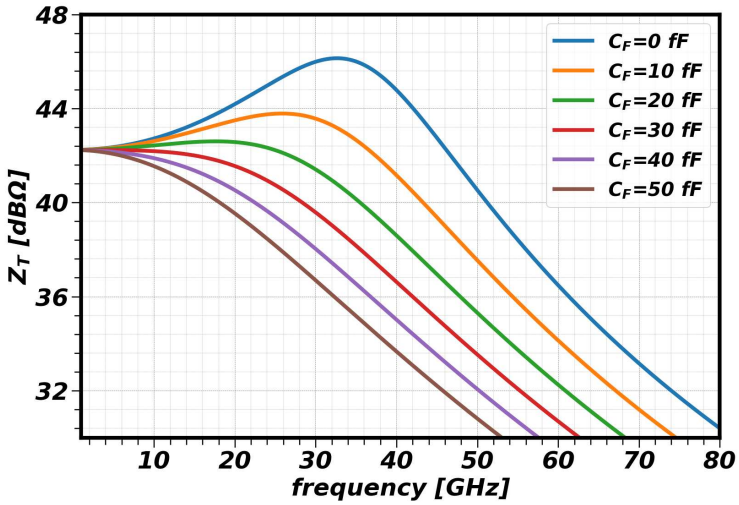


Figure 3.12: Frequency behavior of transimpedance gain of the circuit in Figure 3.3 when varying C_F. All the other small-signal parameters are set to default values reported in Table 3.1.

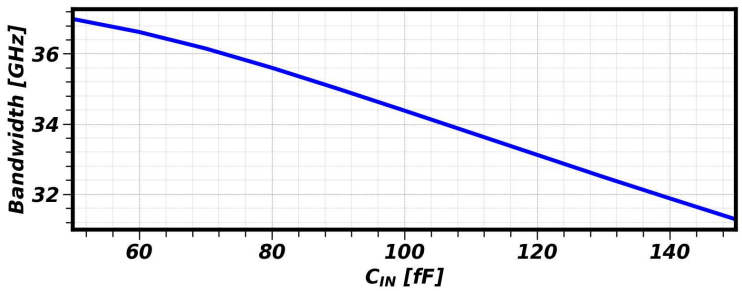


Figure 3.13: Bandwidth and DC Gain of the transfer function of the circuit in Figure 3.3 when varying C_{IN}. All the other small-signal parameters are set to default values reported in Table 3.1.

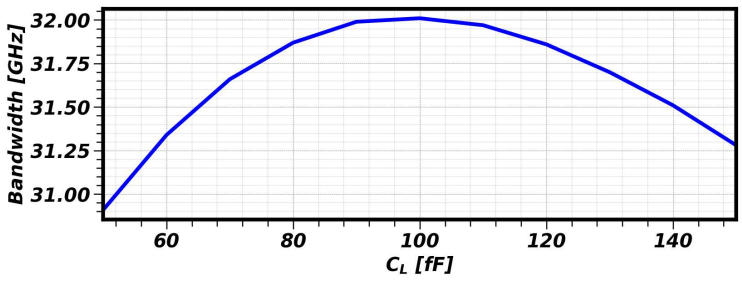


Figure 3.14: Bandwidth and DC Gain of the transfer function of the circuit in Figure 3.3 when varying C_L. All the other small-signal parameters are set to default values reported in Table 3.1.

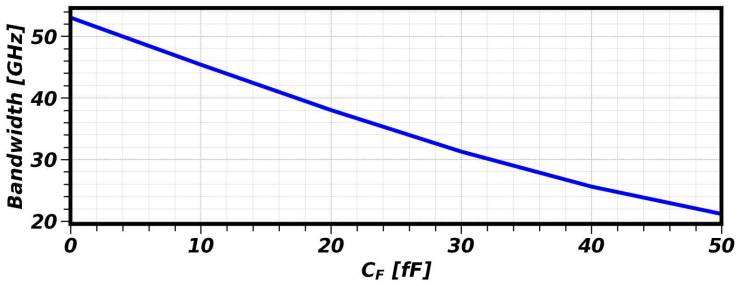


Figure 3.15: Bandwidth and DC Gain of the transfer function of the circuit in Figure 3.3 when varying C_F. All the other small-signal parameters are set to default values reported in Table 3.1.

Small-signal parameter	Default value
C_{PD}	25 fF
$C_{PAD+ESD}$	50 fF
V_{DD}	1 V
R_F	140 Ω
C_L	145 fF
L_{MOS}	14 nm
W_{MOS}	24.5 μm

Table 3.2: Default values of the parameters in the circuit reported in Figure 3.1.

In this subsections, the same plots will be obtained from circuit simulations using the GlobalFoundries' 12 nm LP+ FinFET technology. For every plot, the default values of the small-signal operating point parameters not affected by the sweep itself will be as close as possible to the ones reported in Table 3.1. The channel length of the inverter MOSFETs will always be minimum size, while the MOSFETs channel width will be swept, as well as the inverter supply. The default values for the parameters of the circuit in Figure 3.1 are reported in Table 3.2. The choice of these values will be justified in the next chapter.

The DC current absorption from the supply of the LNTA in SROI applications is a major concern, since most of the times the LNTA has the biggest share of the total power consumption among the oRX AFE blocks. Figure 3.16 reports how the DC supply current varies when changing the MOSFETs' chan-

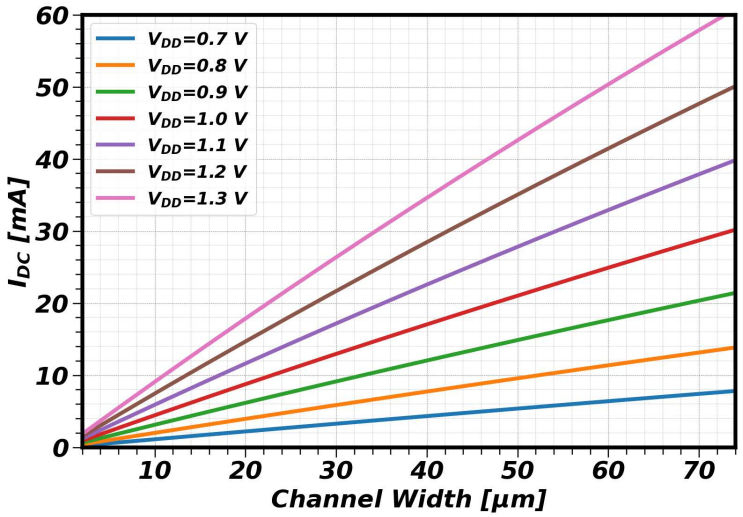


Figure 3.16: DC current absorption of the circuit in Figure 3.1 when varying the channel width W of the MOSFETs and the voltage supply.

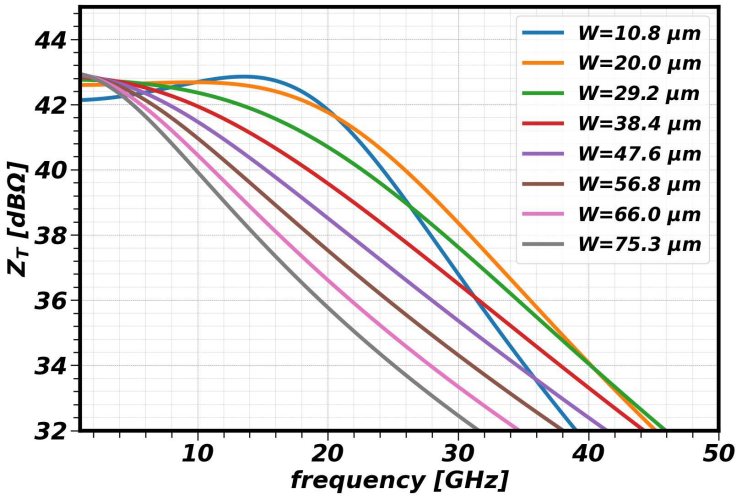


Figure 3.17: Frequency behavior of transimpedance gain of the circuit in Figure 3.1 when varying channel width. All the other circuit parameters are set to the default values reported in Table 3.2.

nel width and the supply voltage itself. As expected, it depends linearly on W and almost quadratically on V_{DD}, which is equal to $2V_{GS}$.

The frequency behavior of the transimpedance gain while sweeping W and V_{DD} is reported in Figures 3.17 and 3.18, respectively. As it can be seen, the channel width has a much more profound effect on the transfer function, since it affects the MOS parasitic capacitances much more than V_{DD}. This is all the more evident when looking at the contour plot of the bandwidth when varying

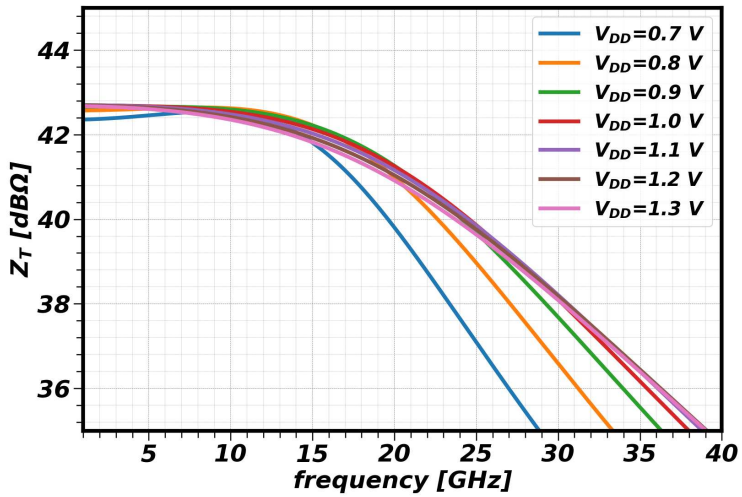


Figure 3.18: Frequency behavior of transimpedance gain of the circuit in Figure 3.1 when varying V_{DD}. All the other circuit parameters are set to the default values reported in Table 3.2.

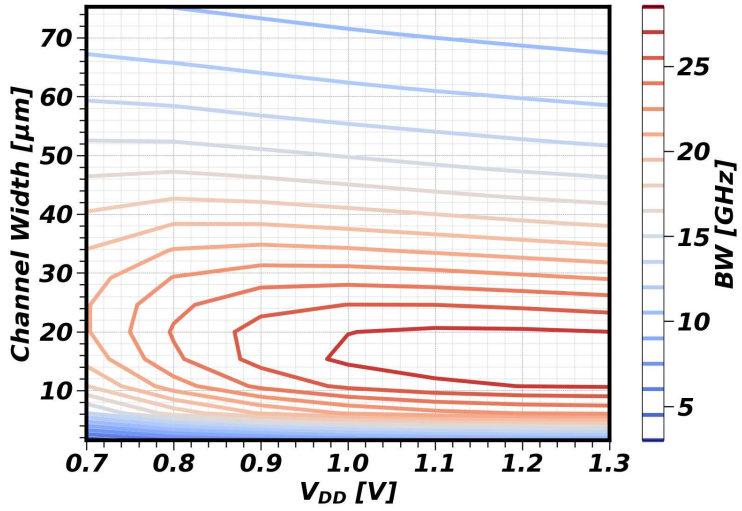


Figure 3.19: Contour plot of the -3 dB bandwidth of the circuit in Figure 3.1 when varying both W and V_{DD}. All the other circuit parameters are set to the default values reported in Table 3.2.

both W and V_{DD} together, shown in Figure 3.19.

3.2.3 Transimpedance Limit

The poles Q is usually chosen to be equal to $1/\sqrt{2}$, which provides a maximally flat transfer function while still boosting the circuit bandwidth. If no peaking in the transfer function is required ($Q \leq 1/\sqrt{2}$), then it can be shown from

Equation 3.15 that for a second-order transfer function like Equation 3.10 (disregarding the RHP zero) it must be $BW_{-3dB} \leq \omega_{p1,2}/2\pi$[22], that is:

$$BW^2 \leq \frac{1 + G_m R_L}{4\pi^2 R_L R_F (C_L C_F + C_F C_{IN} + C_L C_{IN})} \tag{3.19}$$

Since, from Equation 3.5, the mid-band transimpedance gain can be written as:

$$Z_{T0} = \frac{G_{LOOP,0}}{1 + G_{LOOP,0}} \left(R_F - \frac{1}{G_m} \right) \approx \frac{G_{LOOP,0} R_F}{1 + G_{LOOP,0}} \tag{3.20}$$

with $G_{LOOP,0} = G_m R_L$ standing for the mid-band loop gain, we can rewrite Equation 3.19 as:

$$Z_{T0} \leq \frac{G_{LOOP,0}}{4\pi^2 BW^2 R_L (C_L C_F + C_F C_{IN} + C_L C_{IN})} \tag{3.21}$$

which is a well-known results called the "transimpedance limit"[22]. The most important implication of Equation 3.21 is the fact that the mid-band transimpedance gain is inversely proportional to the *square* of the bandwidth. If C_F is ignored and if we assume that the output pole $1/(2\pi R_L C_L)$ sets the open-loop bandwidth f_A of the core inverter amplifier, then we have:

$$Z_{T0} \leq \frac{G_{LOOP,0} f_A}{2\pi BW^2 C_{IN}} \approx \frac{f_T}{2\pi BW^2 C_{IN}} \tag{3.22}$$

where the approximation $G_{LOOP,0} f_A = G_m/(2\pi C_L) \approx f_T$ was used, since C_L represents the input capacitance of the next stage which, if implemented with inverters, will be more or less proportional to $C_{GS} + C_{GD}$. Equation 3.22 is the most famous form of the transimpedance limit [22]. It can be demonstrated that, when assuming a constant R_F design methodology, a noise optimum (i.e. minimum) is reached if the capacitance at the input of the LNTA without C_{PD} is set to be equal to C_{PD} itself, that is $C_{IN,opt} = 2C_{PD}$ [23]. This is a very common design strategy for this circuit, and if used, then Equation 3.22 simplifies to $Z_{T0} BW^2 \leq f_T/(4\pi C_{PD})$. The right-hand side of the equation is a constant which depends only on the capabilities of the used technologies, both CMOS (f_T) and optical (C_{PD}). The result stems from multiple approximations but it is nonetheless extremely important as it states that, without bandwidth extension techniques, only advances in technology fabrication processes can improve the performances of state-of-the-art LNTAs.

3.2.4 Simplifying the Equations

Equations 3.9, 3.10, 3.11 and 3.12 can be simplified by defining $Z_G := 1/sC_{IN}$, $Z_F := R_F/(1 + sR_FC_F)$ and $Z_L := R_L/(1 + sR_LC_L)$, from which:

$$G_{LOOP} = \frac{G_m Z_L}{1 + \frac{Z_L + Z_F}{Z_G}} \tag{3.23}$$

$$Z_T = Z_L \frac{G_m Z_F - 1}{1 + G_m Z_L} \cdot \frac{1}{1 + \frac{1}{Z_G} \cdot \frac{Z_F + Z_L}{1 + G_m Z_L}} \tag{3.24}$$

$$Z_{IN} = \frac{Z_F + Z_L}{1 + G_m Z_L} \cdot \frac{1}{1 + \frac{1}{Z_G} \cdot \frac{Z_F + Z_L}{1 + G_m Z_L}} \tag{3.25}$$

$$Z_O = \frac{Z_L}{1 + G_m Z_L} \cdot \frac{1 + Z_F/Z_G}{1 + \frac{1}{Z_G} \cdot \frac{Z_F + Z_L}{1 + G_m Z_L}} \tag{3.26}$$

By recognizing that:

$$\frac{G_{LOOP}}{1 + G_{LOOP}} = \frac{G_m Z_L}{1 + G_m Z_L} \cdot \frac{1}{1 + \frac{1}{Z_G} \cdot \frac{Z_F + Z_L}{1 + G_m Z_L}} \tag{3.27}$$

equations 3.24, 3.25 and 3.26 can be rewritten as:

$$Z_T = \frac{G_{LOOP}}{1 + G_{LOOP}} \left(Z_F - \frac{1}{G_m} \right) \tag{3.28}$$

$$Z_{IN} = \frac{G_{LOOP}}{1 + G_{LOOP}} \cdot \frac{Z_F + Z_L}{G_m Z_L} \tag{3.29}$$

$$Z_O = \frac{G_{LOOP}}{1 + G_{LOOP}} \cdot \frac{1}{G_m} \cdot \frac{Z_F + Z_G}{Z_G} \tag{3.30}$$

where the term $(Z_F + Z_G)/Z_G$ accounts for the voltage divider at the gate of the inverter. Equations 3.28, 3.29 and 3.30 show remarkable similarities with equations 3.5, 3.6 and 3.7.

Alternatively, by defining the quantities:

$$Z_{IN,LOOP} := \frac{Z_F + Z_L}{1 + G_m Z_L} \tag{3.31}$$

$$Z_{O,LOOP} := \frac{Z_F + Z_G}{1 + G_m Z_G} \tag{3.32}$$

equations 3.25 and 3.26 can also be rewritten as:

$$Z_{IN} = \frac{Z_G \cdot Z_{IN,LOOP}}{Z_G + Z_{IN,LOOP}} = Z_G // Z_{IN,LOOP} \tag{3.33}$$

$$Z_O = \frac{Z_L \cdot Z_{O,LOOP}}{Z_L + Z_{O,LOOP}} = Z_L // Z_{O,LOOP} \tag{3.34}$$

$Z_{IN,LOOP}$ and $Z_{O,LOOP}$ can be interpreted as the input and output impedances of the TIA loop when it is not loaded by any impedance at the input and output nodes, respectively.

3.2.5 Noise

The main noise sources within the LNTA circuit shown in Figure 3.1, excluding the noise coming from the PD, are the thermal noise of the feedback resistor $\overline{I^2_{n,R_F}}/\Delta f = 4kT/R_F$ and the thermal channel noise of the MOSFETs $\overline{I^2_{n,G_m}}/\Delta f = 4kT\gamma G_m$. Induced gate current noise, its correlation to the channel noise, as well as shot and flicker noise, will not be considered here for the sake of simplicity, although R_F and channel noises are the dominant noise sources anyway [23] (such complexities are tackled in other publications [23] [24] [18]).

The output impedance of the LNTA, Z_O, reported in Equation 3.12 can be used for noise calculations, as it is the transfer function of I_{n,G_m} to the output noise voltage $V_{n,out}$, while the transfer function of I_{n,R_F} to $V_{n,out}$ is:

$$\begin{aligned} Z_{I_{n,R_F}} =& R_F \frac{G_m R_L}{1+G_m R_L} \frac{1+sC_{IN}/G_m}{1+s\left(R_F C_F + \frac{R_F C_{IN}+R_L C_L+R_L C_{IN}}{1+G_m R_L}\right)+} \cdots \\ & \cdots \frac{}{+s^2 R_L R_F (C_{IN}C_F + C_{IN}C_L + C_F C_L)} \end{aligned} \tag{3.35}$$

$Z_{I_{n,R_F}}$ shows remarkable similarities with the transimpedance gain in Equation 3.10. Indeed, if the zeroes are ignored (which are placed at much higher frequencies than the poles) and if $G_m R_F \gg 1$, then $Z_{I_{n,R_F}} \approx Z_T$.

From this, the input-referred noise (IRN) current power spectral density (PSD) is:

$$I^2_{n,in}(f) = \frac{1}{Z^2_{T0}} \left[\left| Z_{I_{n,R_F}}(f) \right|^2 \frac{4kT}{R_F} + \left| Z_O(f) \right|^2 4kT\gamma G_m \right] \tag{3.36}$$

where Z_{T0} is the mid-band transimpedance gain in Equation 3.5. Carrying out the calculations, it is well known that the resulting input-referred noise current PSD has a white and violet colored component proportional to f^2 [23]:

$$I^2_{n,in}(f) = I^2_{n,0} + K_2 f^2 \tag{3.37}$$

Then the total averaged input-referred noise (AIRN) current density is[25]:

$$\frac{\overline{I_{n,in}}}{\Delta f} = \sqrt{\frac{1}{Z^2_{T0} BW} \int_0^{+\infty} \left| Z_{I_{n,R_F}}(f) \right|^2 \frac{4kT}{R_F} + \left| Z_O(f) \right|^2 4kT\gamma G_m df} \tag{3.38}$$

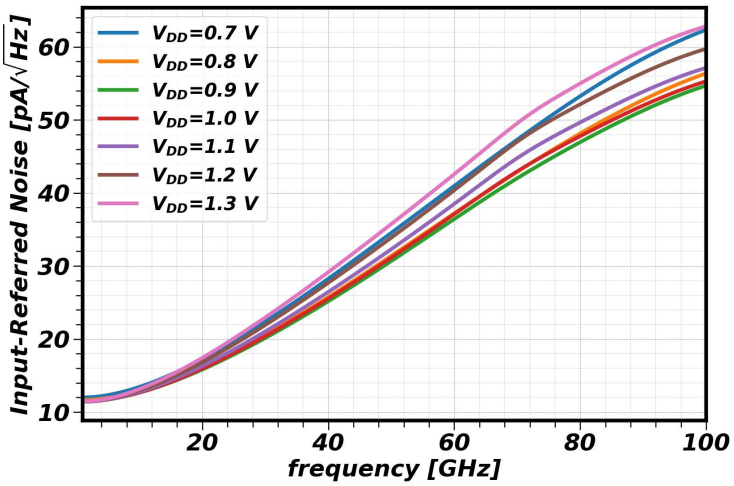


Figure 3.20: Frequency behavior of input-referred noise current density of the circuit in Figure 3.1 when varying V_{DD}. All the other circuit parameters are set to the default values reported in Table 3.2.

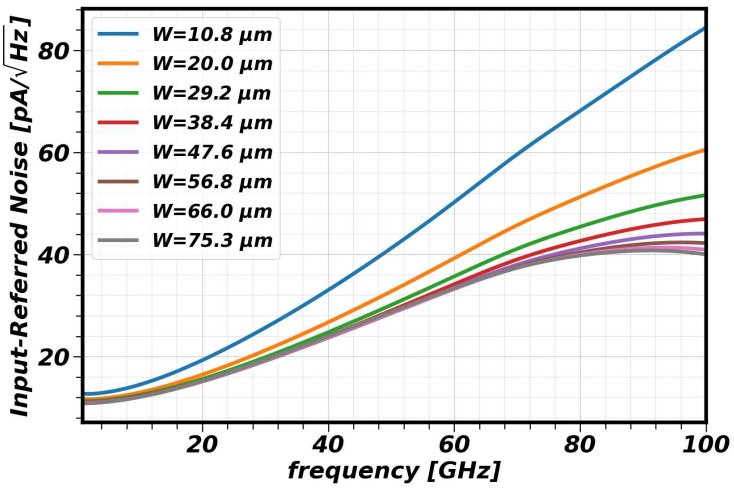


Figure 3.21: Frequency behavior of input-referred noise current density of the circuit in Figure 3.1 when varying channel width. All the other circuit parameters are set to the default values reported in Table 3.2.

where BW is the -3 dB bandwidth in Equation 3.15. If integration upper limit is fixed to the -3 dB bandwidth, then from Equation 3.37 we have:

$$\frac{\overline{I_{n,in}}}{\Delta f} = \sqrt{I_{n,0}^2 + \frac{K_2}{3} BW^2} \tag{3.39}$$

However, limiting the upper integration limit to BW can lead to substantial errors, and noise bandwidths should be used instead [23].

To plot the behavior of the IRN current changing some small-signal param-

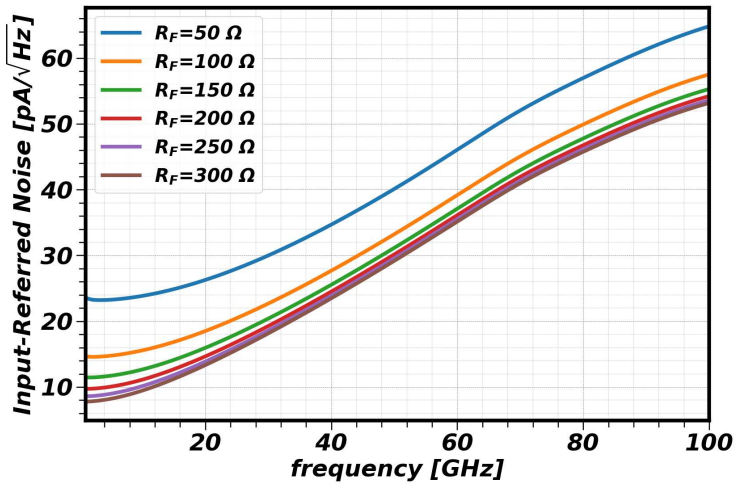


Figure 3.22: Frequency behavior of input-referred noise current density of the circuit in Figure 3.1 when varying R_F. All the other circuit parameters are set to the default values reported in Table 3.2.

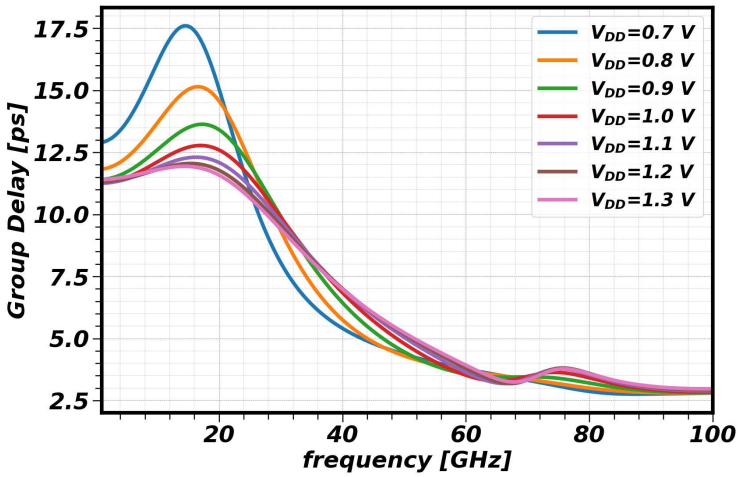


Figure 3.23: Frequency behavior of the group delay of the circuit in Figure 3.1 when varying V_{DD}. All the other circuit parameters are set to the default values reported in Table 3.2.

eters, the ideal model was not used, and circuit simulations with the GF 12 LP+ FinFET technology were run, so as to best capture all the noise sources in the device models. The frequency behavior of input-referred noise current density of the circuit in Figure 3.1 when varying V_{DD}, W, and R_F is reported in Figures 3.20, 3.21, and 3.22, respectively. Later in this section, the AIRN plots will also be shown.

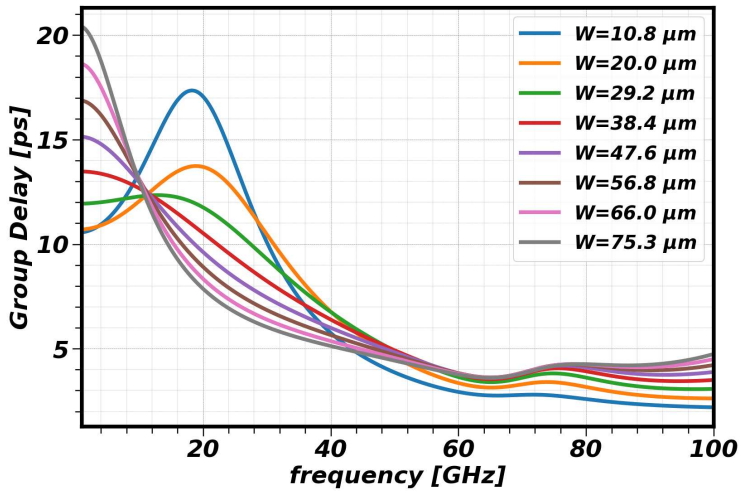


Figure 3.24: Frequency behavior of the group delay of the circuit in Figure 3.1 when varying channel width. All the other circuit parameters are set to the default values reported in Table 3.2.

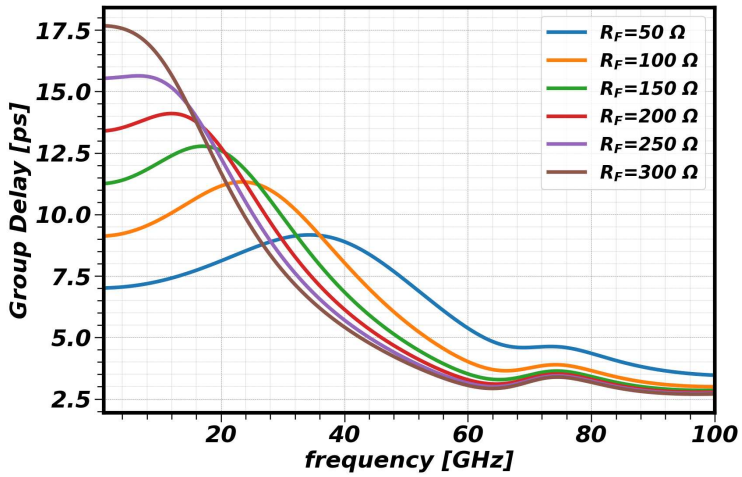


Figure 3.25: Frequency behavior of the group delay of the circuit in Figure 3.1 when varying R_F. All the other circuit parameters are set to the default values reported in Table 3.2.

3.2.6 Group Delay

The group delay $\tau_g := -\partial\phi/\partial\omega$ (where ϕ is the phase of the transimpedance gain in Equation 3.10) and its variation (GDV) across the TIA bandwidth is an important figure of merit in a AFE design, because the GDV is directly linked to the jitter of the output bit-stream[25]. Hence, it is instructive to see how the group delay is affected by V_{DD}, W, and R_F, which is reported in Figures 3.23, 3.24, and 3.25, respectively. It can be noticed that the larger R_F,

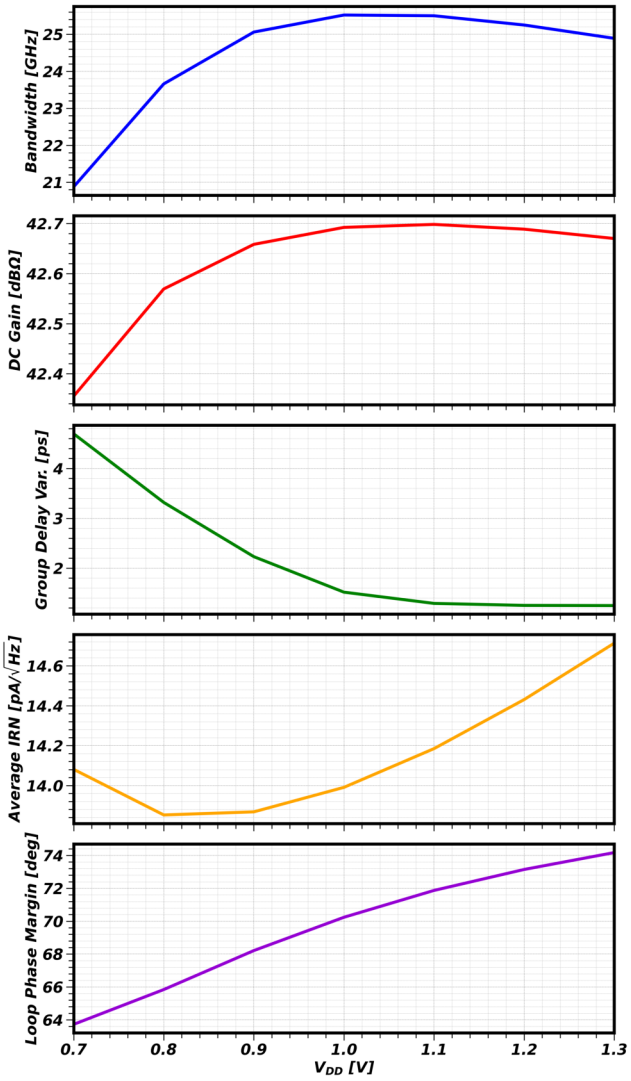


Figure 3.26: BW, DC Gain, GDV, AIRN, and Phase Margin of the circuit in Figure 3.1 when varying V_{DD}. All the other circuit parameters are set to the default values reported in Table 3.2.

the lower the GDV; similarly for V_{DD}, while varying W shows an optimum value. Later in this section, the GDV plots will also be shown.

3.2.7 BW, DC Gain, GDV, AIRN, and Phase Margin Plots

It can be useful to summarize the effects on every parametric sweep by plotting on top of one another, sharing the x-axis, the bandwidth (BW), DC (mid-band) gain, Group Delay Variation (GDV), and Average Input-Referred

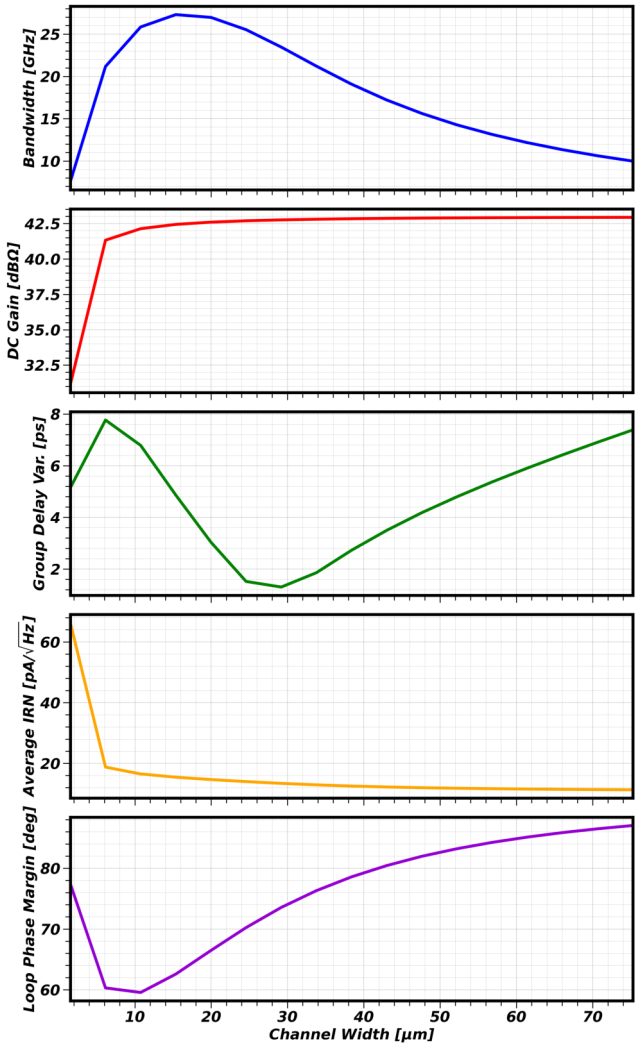


Figure 3.27: BW, DC Gain, GDV, AIRN, and Phase Margin of the circuit in Figure 3.1 when varying channel width. All the other circuit parameters are set to the default values reported in Table 3.2.

Noise (AIRN) current density, as well as the phase margin (PM) of the shunt-feedback loop to check on the stability. The plots for the aforementioned figures of merit while varying V_{DD}, W, and R_F, are reported in Figures

3.3 Passive Inductive Bandwidth Extension

Once an optimal sizing of the circuit in Figure 3.1 is achieved, bandwidth extension without compromising on noise and gain can be achieved by carefully placing and sizing passive planar inductors inside the circuit. Figure 3.29

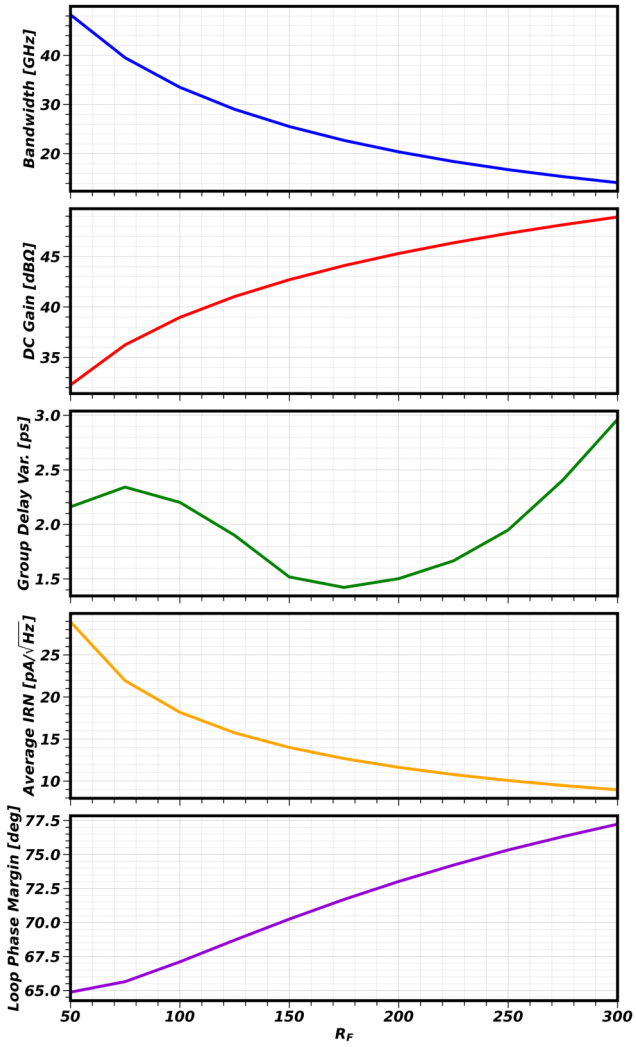


Figure 3.28: BW, DC Gain, GDV, AIRN, and Phase Margin of the circuit in Figure 3.1 when varying R_F. All the other circuit parameters are set to the default values reported in Table 3.2.

shows the considered circuit with photodiode (PD) wirebonded at the input and multiple inductors placed around the loop. Figure 3.30 shows the small-signal circuit with the complete PD small-signal model as well, where $C_G = C_{GS,n} + C_{GS,p}$ now stand for the equivalent parasitic capacitances connected to the gate of the inverter, which is split from $C_{IN} = C_{PD} + C_{PAD} + C_{ESD}$ by the action of L_{IN}, L_G or both. To ease the computational burden, a simplified PD model is used, made of only the parasitic capacitance C_{PD}, as shown in Figure 3.31. The effect of wirebonding parasitic inductances will be analyzed later.

L_{IN}, L_G and L_{OUT} are placed inside the TIA to extend the bandwidth and reduce the in-band noise. Another possibility would be to place an inductor in series with R_F, but it does not yield the same benefits with respect to area consumption due to heavy deQ'ing from R_F itself. Hence, it is not considered here.

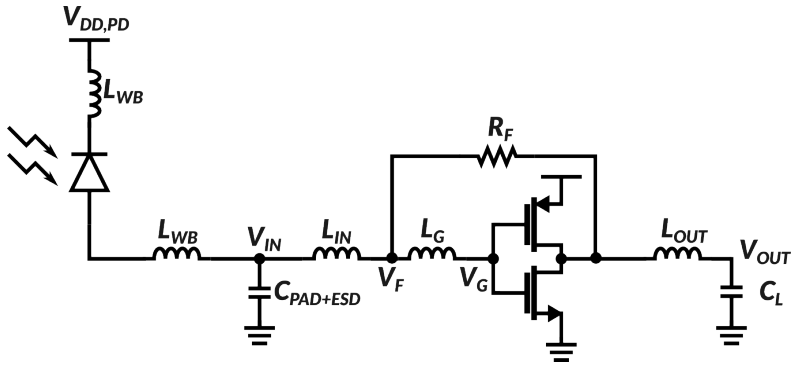


Figure 3.29: Considered LNTA circuit with photodiode (PD) and passive bandwidth extensions inductances.

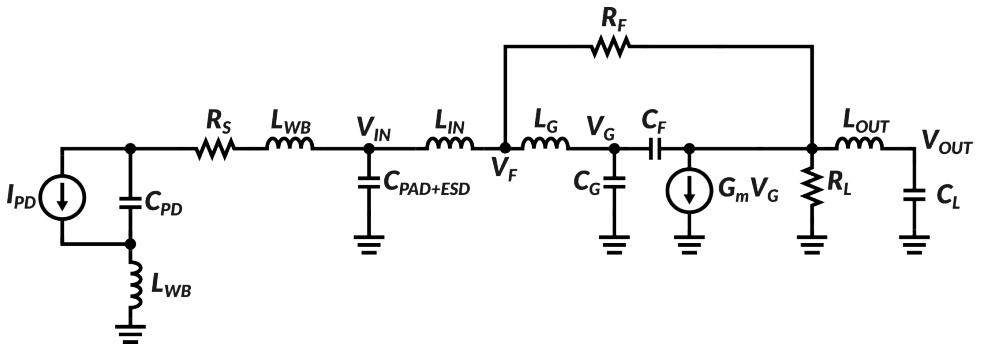


Figure 3.30: Small-signal circuit of the LNTA with passive bandwidth extensions inductances and PD small-signal model as well.

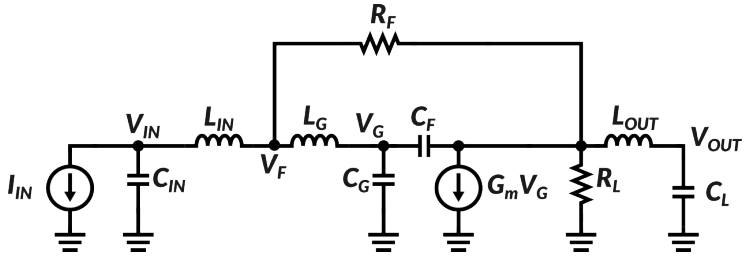


Figure 3.31: Small-signal circuit of the TIA with a simplified PD small-signal model.

3.3.1 Effect of L_{IN} Alone

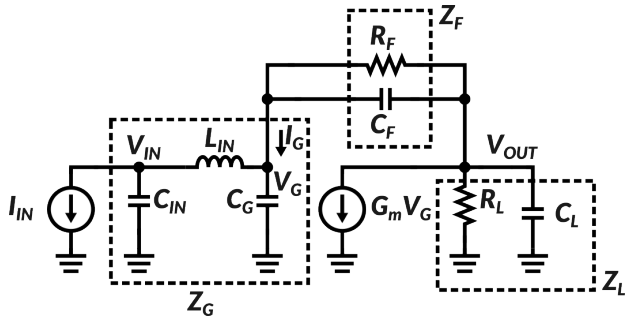


Figure 3.32: TIA small-signal model with simplified PD small-signal model and L_{IN} only.

Let's analyze the circuit in Figure 3.31 without L_G and L_{OUT}. The considered circuit is shown in Figure 3.32 Introducing an input inductor L_{IN} separates $C_{IN} = C_{PD} + C_{PAD} + C_{ESD}$ from C_G. Let's redefine Z_G as the impedance connected between the gate node V_G and ground when turning off the input current source I_{IN}:

$$Z_G := \left.\frac{V_G}{I_G}\right|_{I_{IN}=0} = \frac{1}{sC_G} // \left(sL_{IN} + \frac{1}{sC_{IN}}\right) = \frac{1 + s^2 L_{IN} C_{IN}}{s(C_G + C_{IN})\left(1 + s^2 L_{IN} \frac{C_G C_{IN}}{C_G + C_{IN}}\right)} \tag{3.40}$$

Using Equation 3.40, the G_{LOOP} and Z_O equations are identical to Equation 3.23 and Equation 3.26, respectively. On the other hand, Z_T and Z_{IN} equations differ from the previous case. When considering the effect of L_{IN}, the transimpedance gain and the input impedance can be expressed as:

$$Z_T = \frac{G_{LOOP}}{1 + G_{LOOP}} \left(Z_F - \frac{1}{G_m}\right) \frac{1}{1 + s^2 L_{IN} C_{IN}} \tag{3.41}$$

$$Z_{IN} = \frac{1}{sC_{IN}} // \left(sL_{IN} + \frac{1}{sC_G} // Z_{IN,LOOP}\right) \tag{3.42}$$

where $Z_{IN,LOOP}$ was defined in Equation 3.31.

The complete equations are:

$$\begin{aligned} G_{LOOP} =& G_m R_L \frac{(1+sR_FC_F)(1+s^2L_{IN}C_{IN})}{1+s[R_F(C_F+C_G+C_{IN})+R_L(C_L+C_G+C_{IN})]+} \cdots \\ & \cdots \frac{}{+s^2[L_{IN}C_{IN}+R_FR_L(C_FC_L+(C_F+C_L)(C_G+C_{IN}))]+} \cdots \\ & \cdots \frac{}{+s^3L_{IN}C_{IN}[R_F(C_F+C_G)+R_L(C_L+C_G)]+} \cdots \\ & \cdots \frac{}{+s^4L_{IN}C_{IN}R_FR_L(C_FC_L+C_LC_G+C_FC_G)} \end{aligned} \tag{3.43}$$

$$\begin{aligned} Z_T =& R_L \frac{G_mR_F-1}{1+G_mR_L} \frac{1-s\frac{R_FC_F}{G_mR_F-1}}{1+s\left[R_FC_F+\frac{R_LC_L}{1+G_mR_L}+\frac{(R_F+R_L)(C_G+C_{IN})}{1+G_mR_L}\right]+} \cdots \\ & \cdots \frac{}{+s^2\left[L_{IN}C_{IN}+\frac{R_LR_F(C_LC_F+(C_G+C_{IN})(C_F+C_L))}{1+G_mR_L}\right]+} \cdots \\ & \cdots \frac{}{+s^3L_{IN}C_{IN}\left(R_FC_F+\frac{R_LC_L+R_FC_G+R_LC_G}{1+G_mR_L}\right)+} \cdots \\ & \cdots \frac{}{+s^4\frac{L_{IN}C_{IN}R_FR_L(C_LC_F+C_GC_F+C_GC_L)}{1+G_mR_L}} \end{aligned} \tag{3.44}$$

$$\begin{aligned} Z_{IN} =& \frac{R_F+R_L}{1+G_mR_L} \frac{1+s\left[(R_F//R_L)(C_F+C_L)+L_{IN}\frac{1+G_mR_L}{R_F+R_L}\right]+}{1+s\left[R_FC_F+\frac{R_LC_L}{1+G_mR_L}+\frac{(R_F+R_L)(C_G+C_{IN})}{1+G_mR_L}\right]} \cdots \\ & \cdots \frac{+s^2L_{IN}\left[C_G+\frac{R_LC_L+R_FC_F(1+G_mR_L)}{R_F+R_L}\right]+}{+s^2\left[L_{IN}C_{IN}+\frac{R_LR_F(C_LC_F+(C_G+C_{IN})(C_F+C_L))}{1+G_mR_L}\right]+} \cdots \\ & \cdots \frac{+s^3L_{IN}(R_F//R_L)(C_FC_L+C_GC_F+C_GC_L)}{+s^3L_{IN}C_{IN}\left(R_FC_F+\frac{R_LC_L+R_FC_G+R_LC_G}{1+G_mR_L}\right)+} \cdots \\ & \cdots \frac{}{+s^4\frac{L_{IN}C_{IN}R_FR_L(C_LC_F+C_GC_F+C_GC_L)}{1+G_mR_L}} \end{aligned} \tag{3.45}$$

$$Z_O = \frac{R_L}{1+G_mR_L}\frac{1+sR_F(C_F+C_G+C_{IN})+s^2L_{IN}C_{IN}+s^3L_{IN}C_{IN}R_F(C_F+C_G)}{1+s\left[R_FC_F+\frac{R_LC_L}{1+G_mR_L}+\frac{(R_F+R_L)(C_G+C_{IN})}{1+G_mR_L}\right]+} \cdots$$
$$\cdots \frac{}{+s^2\left[L_{IN}C_{IN}+\frac{R_LR_F(C_LC_F+(C_G+C_{IN})(C_F+C_L))}{1+G_mR_L}\right]+} \cdots$$
$$\cdots \frac{}{+s^3L_{IN}C_{IN}\left(R_FC_F+\frac{R_LC_L+R_FC_G+R_LC_G}{1+G_mR_L}\right)+} \cdots$$
$$\cdots \frac{}{+s^4\frac{L_{IN}C_{IN}R_FR_L(C_LC_F+C_GC_F+C_GC_L)}{1+G_mR_L}} \tag{3.46}$$

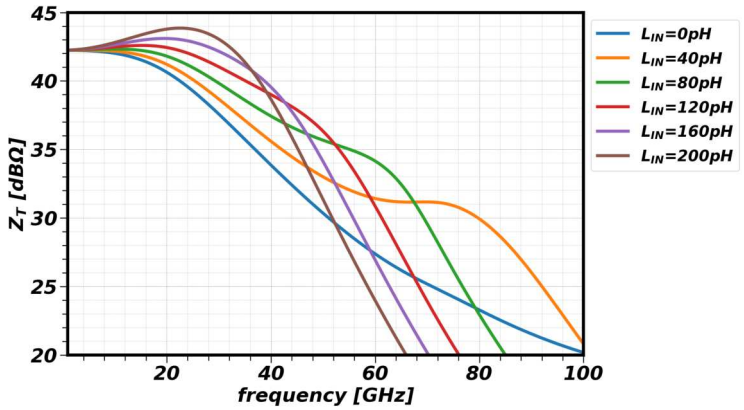


Figure 3.33: Frequency behavior of the transimpedance gain of the circuit in Figure 3.32 when varying L_{IN}. Circuit parameters are set to the default values reported in Table 3.2.

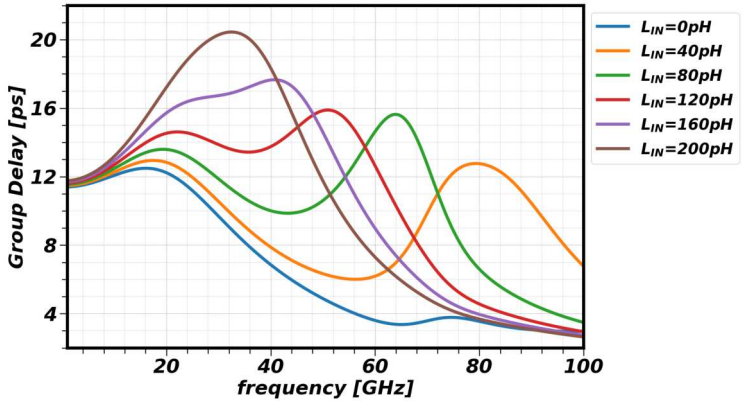


Figure 3.34: Frequency behavior of the group delay of the circuit in Figure 3.32 when varying L_{IN}. Circuit parameters are set to the default values reported in Table 3.2.

The effect of L_{IN} on the transimpedance gain, group delay, and input-referred noise current density is reported in Figures 3.33, 3.34, and 3.35, re-

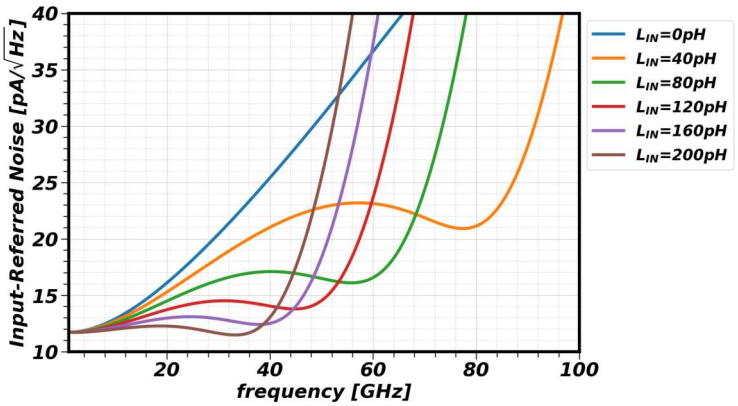


Figure 3.35: Frequency behavior of the input-referred noise current density of the circuit in Figure 3.32 when varying L_{IN}. Circuit parameters are set to the default values reported in Table 3.2.

spectively. Figure 3.36 shows how the BW Extension Ratio (BWER, defined as the ratio in percentage between the circuit BW with a certain L_{IN} value and the BW when L_{IN} is not present, which is approximately 25.1 GHz with the values in Table 3.2), Peaking, GDV, and AIRN change when varying L_{IN}. As it can be seen, L_{IN} is extremely effective in reducing the input-referred noise.

3.3.2 Effect of L_G Alone

Let us now consider the circuit in Figure 3.30 without L_{IN} and L_{OUT} this time. The considered circuit is shown in Figure 3.37. The gate inductor L_G separates $C_{IN} = C_{PD} + C_{PAD} + C_{ESD}$ from C_G like L_{IN} does, but it also alters the loop structure itself, since C_F is not in parallel to R_F anymore. Hence, some of the simplified results reported in the L_{IN} case do not apply anymore. Equations 3.43, 3.44, 3.45 and 3.46 now become:

$$\begin{aligned} G_{LOOP} = & G_m R_L \frac{1 + sR_F C_F + s^2 L_G (C_F + C_G)}{1 + s[R_F(C_F + C_G + C_{IN}) + R_L(C_L + C_G + C_{IN})] + \cdots} \cdots \\ & \cdots \frac{}{+ s^2[L_G(C_F + C_G) + R_F R_L(C_F C_L + (C_F + C_L)(C_G + C_{IN}))] + \cdots} \cdots \\ & \cdots \frac{}{+ s^3 L_G[C_{IN}(R_L + R_F)(C_L + C_G) + R_L(C_F C_L + C_L C_G + C_F C_G)] + \cdots} \cdots \\ & \cdots \frac{}{+ s^4 L_G C_{IN} R_F R_L (C_F C_L + C_L C_G + C_F C_G)} \end{aligned} \tag{3.47}$$

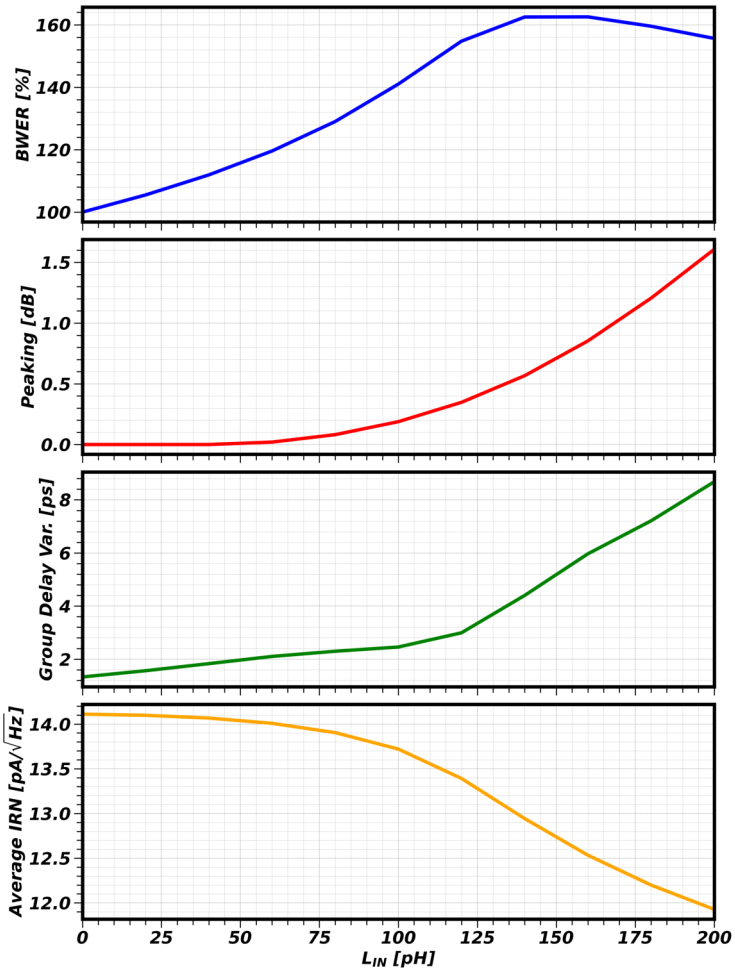


Figure 3.36: BW Extension Ratio, Peaking, GDV, and AIRN of the circuit in Figure 3.32 when varying L_{IN}. Circuit parameters are set to the default values reported in Table 3.2.

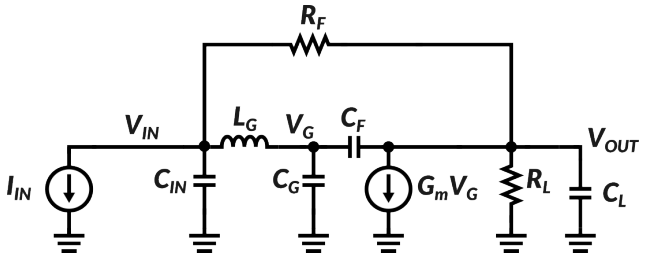


Figure 3.37: TIA small-signal model with simplified PD small-signal model and L_G only.

$$Z_T = R_L \frac{G_m R_F - 1}{1 + G_m R_L} \frac{1 + s\frac{R_F C_F}{G_m R_F - 1} + s^2 \frac{L_G(C_F + C_G)}{G_m R_F - 1}}{1 + s\left[R_F C_F + \frac{R_L C_L}{1 + G_m R_L} + \frac{(R_F + R_L)(C_G + C_{IN})}{1 + G_m R_L}\right] + \cdots} \cdots$$

$$\cdots \frac{}{+ s^2\left[L_G C_F + \frac{L_G C_G + R_L R_F (C_L C_F + (C_G + C_{IN})(C_F + C_L))}{1 + G_m R_L}\right] + \cdots} \cdots$$

$$\cdots \frac{}{+ s^3 L_G \left[C_{IN} R_F C_F + \frac{C_{IN}(R_F C_G + R_L C_G + R_L C_F) + R_L (C_F C_L + C_G C_F + C_G C_L)}{1 + G_m R_L}\right] + \cdots} \cdots$$

$$\cdots \frac{}{+ s^4 \frac{L_G C_{IN} R_F R_L (C_L C_F + C_G C_F + C_G C_L)}{1 + G_m R_L}} \tag{3.48}$$

$$Z_{IN} = \frac{R_F + R_L}{1 + G_m R_L} \frac{1 + s(R_F//R_L)(C_F + C_L) + s^2 L_G(C_F + C_G + C_F G_m(R_F//R_L) + \cdots}{1 + s\left[R_F C_F + \frac{R_L C_L}{1+G_m R_L} + \frac{(R_F+R_L)(C_G+C_{IN})}{1+G_m R_L}\right] + \cdots}$$
$$\cdots \frac{+s^3 L_G(R_F//R_L)(C_F C_L + C_F C_G + C_G C_L)}{+s^2\left[L_G C_F + \frac{L_G C_G + R_L R_F (C_L C_F + (C_G + C_{IN})(C_F + C_L))}{1+G_m R_L}\right] + \cdots}$$
$$\cdots \frac{}{+s^3 L_G\left[C_{IN} R_F C_F + \frac{C_{IN}(R_F C_G + R_L C_G + R_L C_F) + R_L(C_F C_L + C_G C_F + C_G C_L)}{1+G_m R_L}\right] + \cdots}$$
$$\cdots \frac{}{+s^4 \frac{L_G C_{IN} R_F R_L (C_L C_F + C_G C_F + C_G C_L)}{1+G_m R_L}} \tag{3.49}$$

$$Z_O = \frac{R_L}{1 + G_m R_L} \frac{1 + sR_F(C_F + C_G + C_{IN}) + s^2 L_G(C_G + C_F) + \cdots}{1 + s\left[R_F C_F + \frac{R_L C_L}{1+G_m R_L} + \frac{(R_F+R_L)(C_G+C_{IN})}{1+G_m R_L}\right] + \cdots}$$
$$\cdots \frac{+s^3 L_G C_{IN} R_F (C_F + C_G)}{+s^2\left[L_G C_F + \frac{L_G C_G + R_L R_F (C_L C_F + (C_G + C_{IN})(C_F + C_L))}{1+G_m R_L}\right] + \cdots}$$
$$\cdots \frac{}{+s^3 L_G\left[C_{IN} R_F C_F + \frac{C_{IN}(R_F C_G + R_L C_G + R_L C_F) + R_L(C_F C_L + C_G C_F + C_G C_L)}{1+G_m R_L}\right] + \cdots}$$
$$\cdots \frac{}{+s^4 \frac{L_G C_{IN} R_F R_L (C_L C_F + C_G C_F + C_G C_L)}{1+G_m R_L}} \tag{3.50}$$

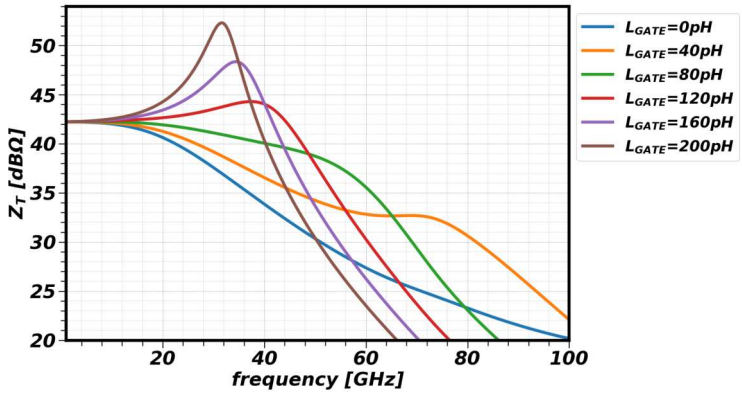


Figure 3.38: Frequency behavior of the transimpedance gain of the circuit in Figure 3.37 when varying L_G. Circuit parameters are set to the default values reported in Table 3.2.

The effect of L_G on the transimpedance gain, group delay, and input-referred noise current density is reported in Figures 3.38, 3.39, and 3.40, respectively. Figure 3.41 shows how the BW Extension Ratio, Peaking, GDV,

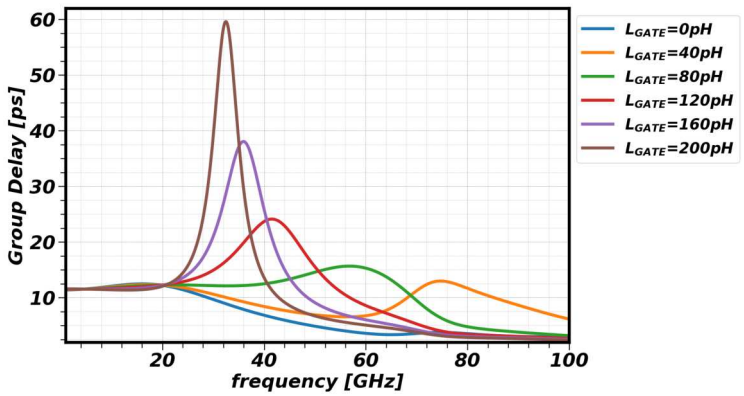


Figure 3.39: Frequency behavior of the group delay of the circuit in Figure 3.37 when varying L_G. Circuit parameters are set to the default values reported in Table 3.2.

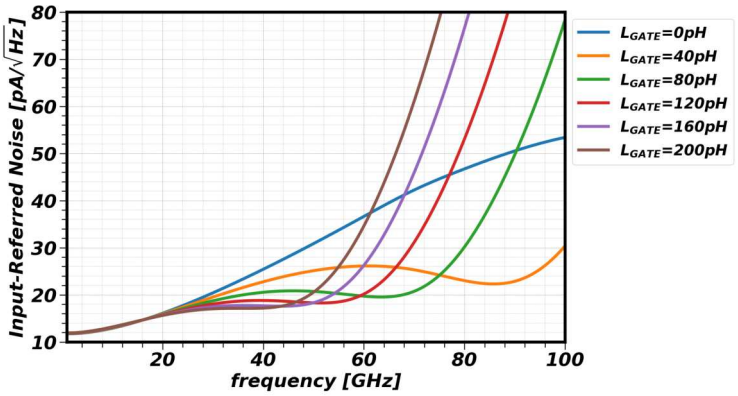


Figure 3.40: Frequency behavior of the input-referred noise current density of the circuit in Figure 3.37 when varying L_G. Circuit parameters are set to the default values reported in Table 3.2.

and AIRN change when varying L_G. It can be seen that L_G is much more effective at extending the BW without altering the peaking and GDV excessively. However, it does not help with the noise, and the optimization needs to be much more careful, as tiny changes in inductance value can rapidly lead to excessive peaking and GDV, much more so than with L_{IN}.

Inserting an inductor on a high-impedance node within a loop raises stability concerns inevitably. Figures 3.42 and 3.43 report the gain & phase and the phase & gain margin of the TIA loop, respectively. As it can be seen, the loop stability is never threatened by the gate inductor for the whole design space, although the gain margin is somewhat low.

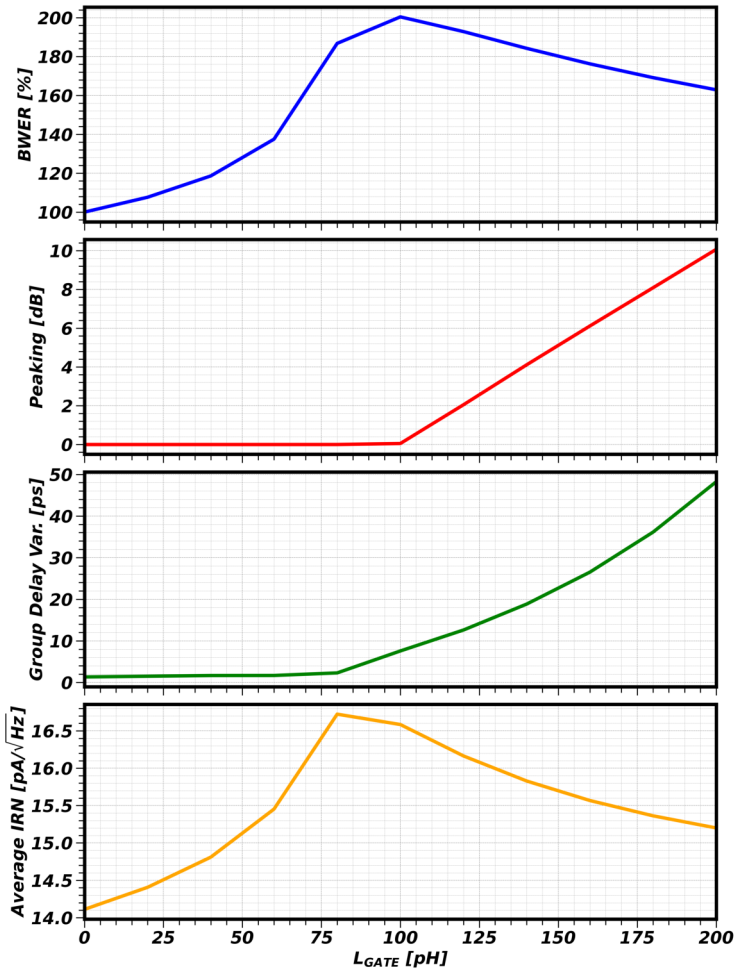


Figure 3.41: BW Extension Ratio, Peaking, GDV, and AIRN of the circuit in Figure 3.37 when varying L_G. Circuit parameters are set to the default values reported in Table 3.2.

3.3.3 Effect of L_{OUT} alone

When compared to the previous two techniques, L_{OUT} is a fairly standard series inductive peaking technique to extend the bandwidth by resonating with the loading capacitance. However, it is mostly ineffective in reducing the noise, since the pole at the input of the LNTA is usually at a lower frequency than the one at the output, hence the thermal channel noise currents from the MOSFETs will still be able to flow directly into the input node, creating the violet colored noise component, as it happened in the LNTA circuit without inductors. Also, C_{IN} and C_G are not split anymore, so they can be merged together in a single C_{IN} capacitance again.

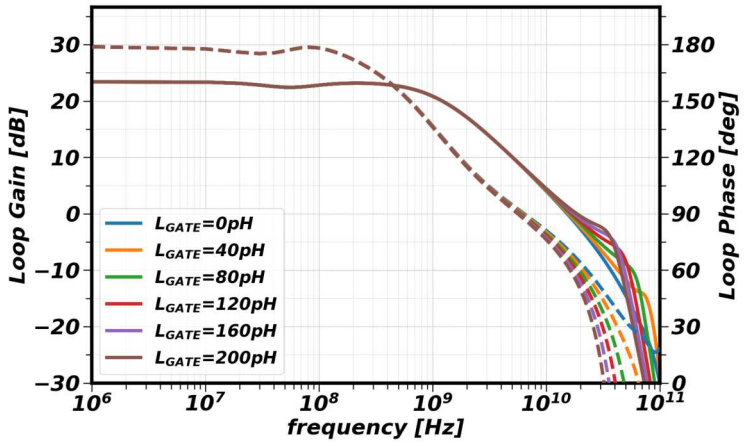


Figure 3.42: TIA loop gain (continuous, left-hand axis) & phase (dashed, right-hand axis) of the circuit in Figure 3.37 when varying L_G. Circuit parameters are set to the default values reported in Table 3.2.

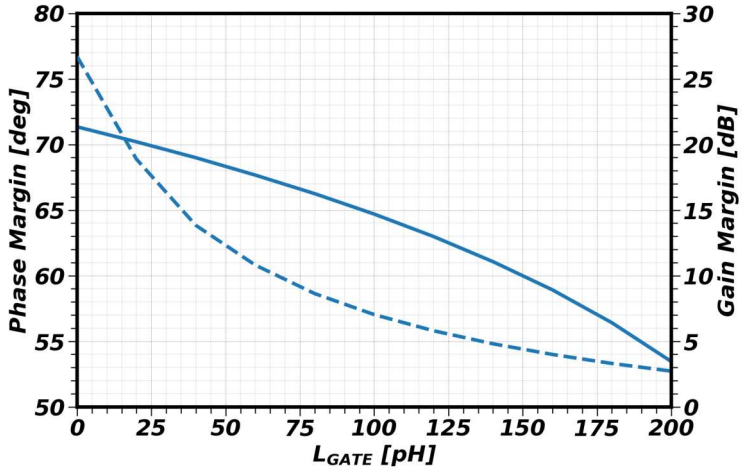


Figure 3.43: TIA loop phase (continuous, left-hand axis) and gain (dashed, right-hand axis) margins of the circuit in Figure 3.37 when varying L_G. Circuit parameters are set to the default values reported in Table 3.2.

G_{LOOP}, Z_T, Z_{IN}, and Z_O in this case become:

$$\begin{aligned} G_{LOOP} =& G_m R_L \frac{(1+sR_FC_F)(1+s^2L_{OUT}C_L)}{1+s[R_F(C_F+C_{IN})+R_L(C_L+C_{IN})]+} \cdots \\ & \cdots \frac{}{+s^2[L_{OUT}C_L+R_FR_L(C_FC_L+C_FC_{IN}+C_LC_{IN})]+} \cdots \\ & \cdots \frac{}{+s^3L_{OUT}C_L(R_FC_F+R_LC_{IN}+R_LC_{IN})+} \cdots \\ & \cdots \frac{}{+s^4L_{OUT}C_LR_FR_LC_FC_{IN}} \end{aligned} \tag{3.51}$$

$$
\begin{aligned}
Z_T =& R_L \frac{G_m R_F - 1}{1 + G_m R_L} \frac{1 - s\frac{R_F C_F}{G_m R_F - 1}}{1 + s\left[R_F C_F + \frac{R_L C_L + (R_F + R_L) C_{IN}}{1 + G_m R_L}\right] +} \cdots \\
& \cdots \frac{}{+ s^2\left[L_{OUT} C_L + \frac{R_L R_F (C_L C_F + C_{IN} C_F + C_{IN} C_L)}{1 + G_m R_L}\right] +} \cdots \\
& \cdots \frac{}{+ s^3 L_{OUT} C_L \left(R_F C_F + \frac{(R_L + R_F) C_{IN}}{1 + G_m R_L}\right) + s^4 \frac{L_{OUT} C_L R_F R_L C_{IN} C_F}{1 + G_m R_L}}
\end{aligned}
\tag{3.52}
$$

$$
\begin{aligned}
Z_{IN} =& \frac{R_F + R_L}{1 + G_m R_L} \frac{1 + s(R_F // R_L)(C_F + C_L)}{1 + s\left[R_F C_F + \frac{R_L C_L + (R_F + R_L) C_{IN}}{1 + G_m R_L}\right] +} \cdots \\
& \cdots \frac{+ s^2 L_{OUT} C_L +}{+ s^2\left[L_{OUT} C_L + \frac{R_L R_F (C_L C_F + C_{IN} C_F + C_{IN} C_L)}{1 + G_m R_L}\right] +} \cdots \\
& \cdots \frac{+ s^3 L_{OUT} (R_L // R_F) C_L C_F}{+ s^3 L_{OUT} C_L \left(R_F C_F + \frac{(R_L + R_F) C_{IN}}{1 + G_m R_L}\right) + s^4 \frac{L_{OUT} C_L R_F R_L C_{IN} C_F}{1 + G_m R_L}}
\end{aligned}
\tag{3.53}
$$

$$
\begin{aligned}
Z_O =& \frac{R_L}{1 + G_m R_L} \frac{1 + s\left[R_F(C_F + C_{IN}) + \frac{L_{OUT}}{R_L}(1 + G_m R_L)\right] +}{1 + s\left[R_F C_F + \frac{R_L C_L + (R_F + R_L) C_{IN}}{1 + G_m R_L}\right] +} \cdots \\
& \cdots \frac{+ s^2 \frac{L_{OUT}}{R_L}[(R_L + R_F) C_{IN} + R_F C_F (1 + G_m R_L)] +}{+ s^2\left[L_{OUT} C_L + \frac{R_L R_F (C_L C_F + C_{IN} C_F + C_{IN} C_L)}{1 + G_m R_L}\right] +} \cdots \\
& \cdots \frac{+ s^3 L_{OUT} C_{IN} R_F C_F}{+ s^3 L_{OUT} C_L \left(R_F C_F + \frac{(R_L + R_F) C_{IN}}{1 + G_m R_L}\right) + s^4 \frac{L_{OUT} C_L R_F R_L C_{IN} C_F}{1 + G_m R_L}}
\end{aligned}
\tag{3.54}
$$

The effect of L_{OUT} on the transimpedance gain, group delay, and input-referred noise current density is reported in Figures 3.44, 3.45, and 3.46, respectively. Figure 3.47 shows how the BW Extension Ratio, Peaking, GDV, and AIRN change when varying L_{OUT}. As it can be seen, L_{OUT} is ineffective in reducing the input-referred noise and the BWER is limited.

3.3.4 Comparison of L_{IN}, L_{OUT}, and L_G

As it can be seen from the equations in the previous subsections, adding even only one inductance without disregarding some of the parasitic capacitances (typically C_F) complicates the equations beyond the point of easy and intuitive analytical insight. Therefore, adding multiple inductances together into the

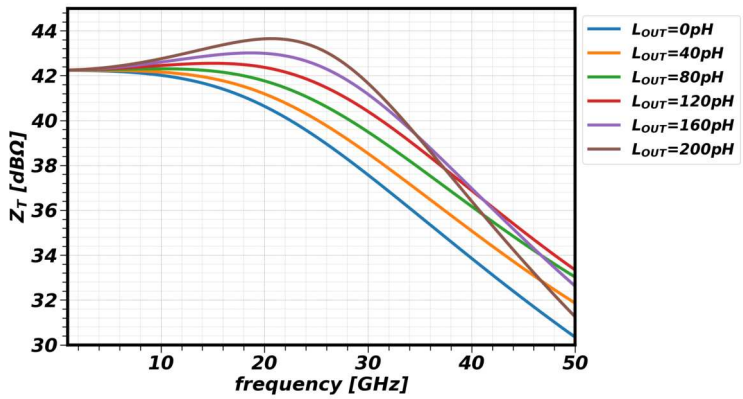


Figure 3.44: Frequency behavior of the transimpedance gain of the TIA circuit with only the output inductor when varying L_{OUT}. Circuit parameters are set to the default values reported in Table 3.2.

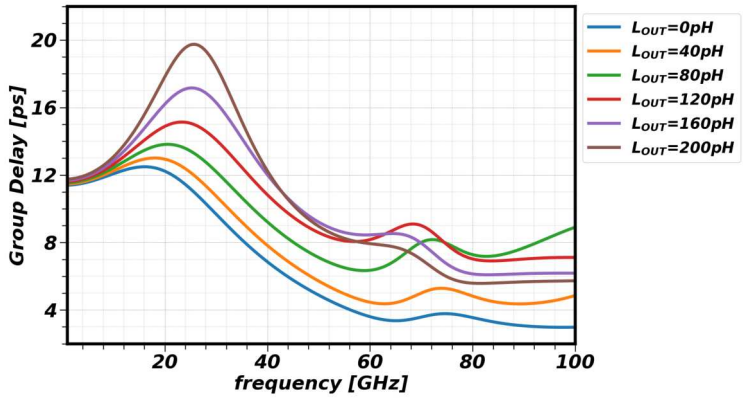


Figure 3.45: Frequency behavior of the group delay of the TIA circuit with only the output inductor when varying L_{OUT}. Circuit parameters are set to the default values reported in Table 3.2.

mix would not give any mathematical benefit. Here thereafter, only simulation results are reported, hoping to gain intuition from visual inspection of the multiple curves obtained from parametric sweeps.

Figure 3.48 shows the comparison of the effect the L_{IN}, L_G, and L_{OUT} techniques have on BW Extension Ratio, Peaking, GDV, and AIRN when used separately. As it can be seen, the gate inductor is the most effective in extending the bandwidth, while the input inductor is the best candidate in reducing high-frequency noise. This suggests that a combination of the two can potentially yield the best results in both domain without excessively increasing peaking and GDV. Indeed, Figure 3.49 show huge gains in BW and noise-reduction when L_{IN} and L_G are used together. The output inductor

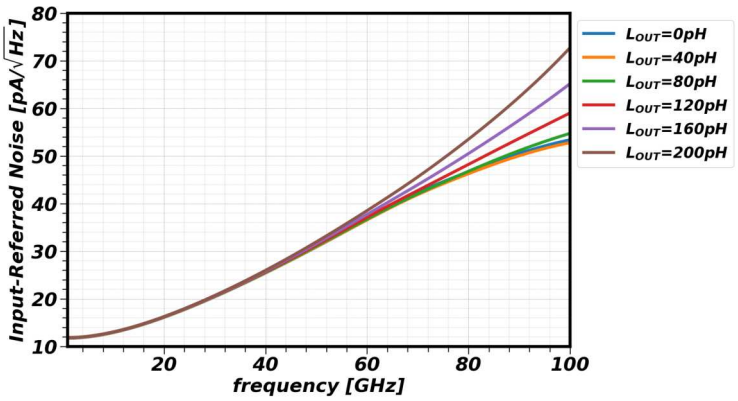


Figure 3.46: Frequency behavior of the input-referred noise current density of the TIA circuit with only the output inductor when varying L_{OUT}. Circuit parameters are set to the default values reported in Table 3.2.

instead is not as effective in either domain, but can be helpful in boosting the high-frequency components of the signal if properly used alongside one or more inductors.

Hence, of particular interest is the comparison between the effects of L_G and L_{IN}. From Equation 3.44 and Equation 3.48, it can be noticed that the denominators (hence the transimpedance poles) are quite similar to each other. The first-order and forth-order terms, in particular, are identical except for L_{IN} instead of L_G and vice versa. The same can be said for the poles of the loop gain. Regarding the numerators, in the L_{IN} case Z_T has one right-hand-plane (RHP) zero and G_{LOOP} has one real left-hand-plane (LHP) zero and two complex LHP zeroes, while in the L_G case Z_T has two complex LHP zeroes and G_{LOOP} has only two complex LHP zeroes.

If the low-frequency value of the loop gain, $G_m R_L$, is assumed to be so large that all the terms divided by $1+G_m R_L$ at the denominator of Z_T become negligible, then the transimpedance equations become (assuming $G_m R_F \gg 1$ as well):

$$Z_{T,L_{IN}} \approx \frac{R_F}{1 + sR_FC_F + s^2L_{IN}C_{IN} + s^3L_{IN}C_{IN}R_FC_F + s^4L_{IN}\frac{C_{IN}R_F(C_LC_F+C_GC_F+C_GC_L)}{G_m}} \tag{3.55}$$

$$Z_{T,L_G} \approx \frac{R_F}{1 + sR_FC_F + s^2L_GC_F + s^3L_GC_{IN}R_FC_F + s^4L_G\frac{C_{IN}R_F(C_LC_F+C_GC_F+C_GC_L)}{G_m}} \tag{3.56}$$

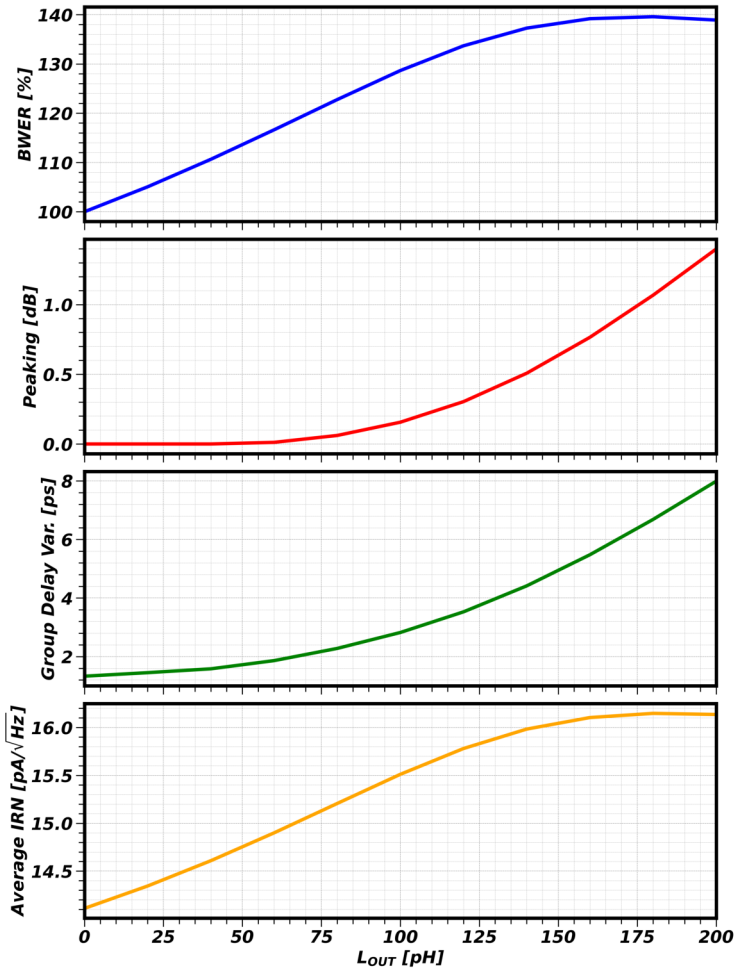


Figure 3.47: BW Extension Ratio, Peaking, GDV, and AIRN of the TIA circuit with only the output inductor when varying L_{OUT}. Circuit parameters are set to the default values reported in Table 3.2.

where the zeroes have been ignored due to their frequency being much higher than the poles frequency. It can be noted that even in the L_G case, the poles location is mainly determined by $L_G C_{IN}$, contrary to intuition which would suggest it to be linked to $L_G C_G$ instead. However, such a result is only a limit case from approximations which cannot be assumed to be true in a more realistic scenario.

If C_F is assumed to be negligible, the transimpedance equations for L_{IN} and L_G now become (assuming $G_m R_L, G_m R_F \gg 1$ and ignoring the zeroes

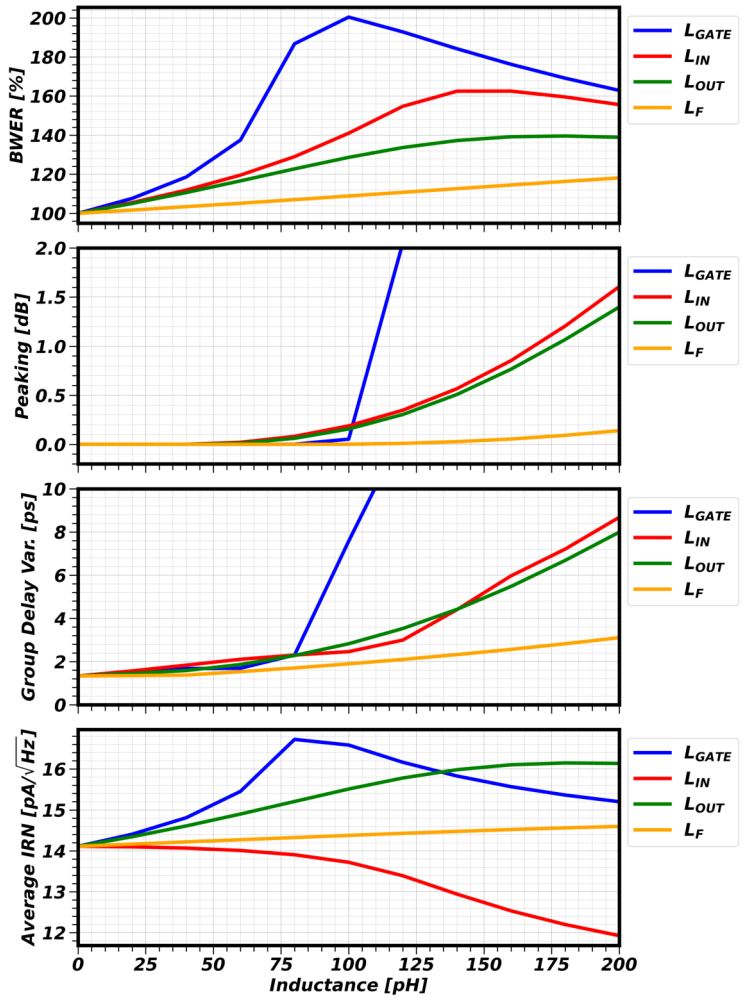


Figure 3.48: Comparison of the effect the L_{IN}, L_G, and L_{OUT} techniques have on BW Extension Ratio, Peaking, GDV, and AIRN when used separately. Circuit parameters are set to the default values reported in Table 3.2.

again):

$$Z_{T,L_{IN}} \approx \frac{R_F}{1 + s\frac{R_L C_L + (R_F+R_L)(C_G+C_{IN})}{G_m R_L} + s^2\left[L_{IN}C_{IN} + \frac{R_L C_L R_F (C_G+C_{IN})}{G_m R_L}\right] + \cdots} \cdots$$
$$\cdots \frac{}{+ s^3 L_{IN} C_{IN} \frac{R_F C_G + R_L C_G + R_L C_L}{G_m R_L} + s^4 \frac{L_{IN} C_{IN} R_F C_G C_L}{G_m}} \tag{3.57}$$

$$Z_{T,L_G} \approx \frac{R_F}{1 + s\frac{R_L C_L + (R_F+R_L)(C_G+C_{IN})}{G_m R_L} + s^2 \frac{L_G C_G + R_L C_L R_F (C_G+C_{IN})}{G_m R_L} + \cdots} \cdots$$
$$\cdots \frac{}{+ s^3 L_G C_G \frac{R_F C_{IN} + R_L C_{IN} + R_L C_L}{G_m R_L} + s^4 \frac{L_G C_{IN} R_F C_G C_L}{G_m}} \tag{3.58}$$

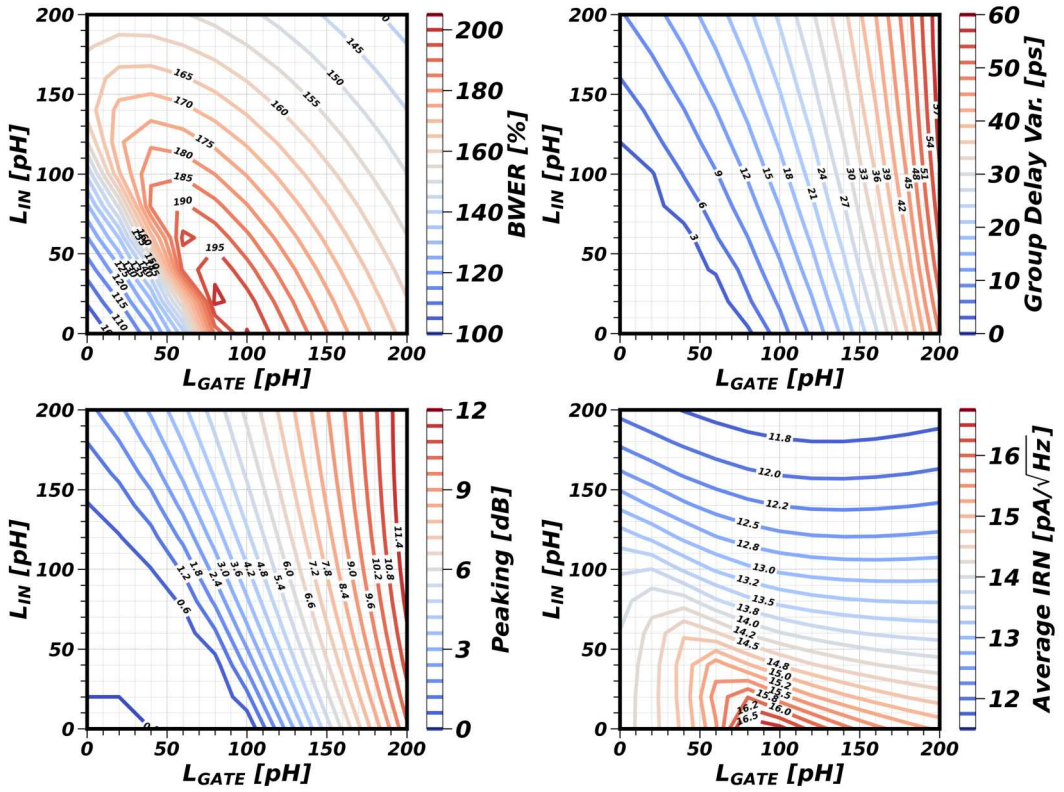


Figure 3.49: BW Extension Ratio, Peaking, GDV, and AIRN contours when varying L_{IN} and L_G together. Circuit parameters are set to the default values reported in Table 3.2.

Equations 3.57 and 3.58 are remarkably similar, with C_{IN} and C_G trading places in the L_{IN} and L_G case, respectively. The only difference is linked to the second-order term at the denominator, where $L_G C_G$ is divided by $1+G_m R_L$ in Z_{T,L_G} while $L_{IN} C_{IN}$ is not in $Z_{T,L_{IN}}$.

Without any approximation, it can be noticed how the second-order term at the denominator of Z_{T,L_G} in Equation 3.48 is most likely lower than the one in $Z_{T,L_{IN}}$ in Equation 3.44, since the difference between the two is linked to the $L_{IN} C_{IN}$ factor in $Z_{T,L_{IN}}$, which becomes $L_G(C_F + C_G/(1 + G_m R_L))$ in Z_{T,L_G} (the input capacitance is usually much larger than the sum of the gate-drain capacitances of the MOSFETs). This entails that one of the two or both pairs of complex poles of the transimpedance transfer function will have a higher quality factor in the L_G case than in the L_{IN} case. Hence, for a given ripple in the transfer function, Z_{T,L_G} will have a greater bandwidth than $Z_{T,L_{IN}}$. This is proven with circuit simulations, as shown in Figure 3.50, where the Bandwidth Extension Ratio (BWER) is plotted against the transfer function peaking. The

result has been obtained by sweeping the value of the single inductances and then by creating and plotting BWER and peaking arrays for every inductance value, after sorting the resulting arrays by increasing peaking values.

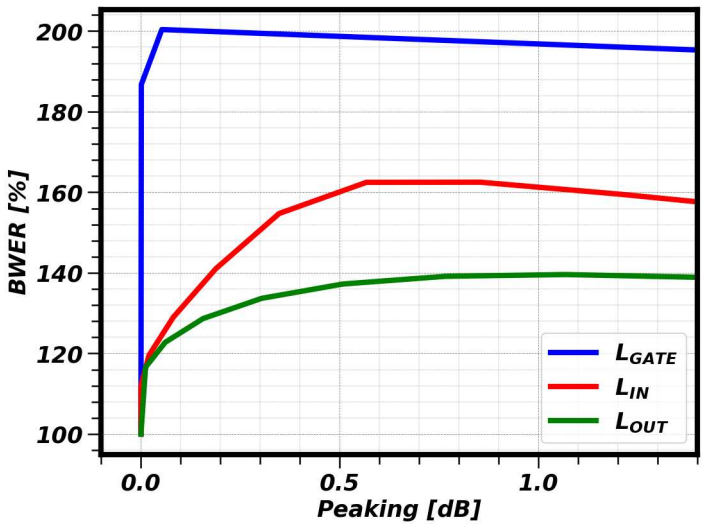


Figure 3.50: Bandwidth Extension Ratio vs. Peaking for the three considered peaking schemes obtained from circuit simulations.

All three curves show multiple data points at the 0-dB peaking point, particularly the L_G curve. This is because the peaking has been defined as the difference between the global maximum of the transfer function and the value it assumes at the lowest local minimum within the -3 dB bandwidth frequency range. If no local minimum exists (which is the case for a monotonically decreasing transfer function), then the peaking is assumed to be zero. Hence, until a local minimum appears in the transimpedance, all the BWER points will be aligned on the 0-dB peaking axis.

Such results become more complicated if a more accurate photodiode model is considered, with wire-bonding inductors as well. The impedance of the Norton equivalent of the photodiode from Equation 3.3 should be used in parallel to the capacitance of pad and ESDs, along with Equation 3.2 instead of constant current source. A mathematical model would give little to no insights in such case. Circuit simulations show that if wire-bonding inductors of 150 pH are added, then the transimpedance transfer function has higher BWER for lower peaking values when using L_{IN} instead of L_G, as reported on the left in Figure 3.51, which is the opposite of what is shown in Figure 3.50.

Also displayed in Figure 3.51, the combination of L_{IN} and L_G shows the best results in the presence of wire-bonding inductors, approaching 180% BWER at around 1 dB peaking. The starting point for all curves is slightly above 0 dB because a relatively small amount of peaking is linked to the wire-bonding inductor itself. The average IRN instead is only affected by L_{IN}, as reported on the right in Figure 3.51, the combination of L_{IN} and L_G being almost identical while L_G by itself is not as effective.

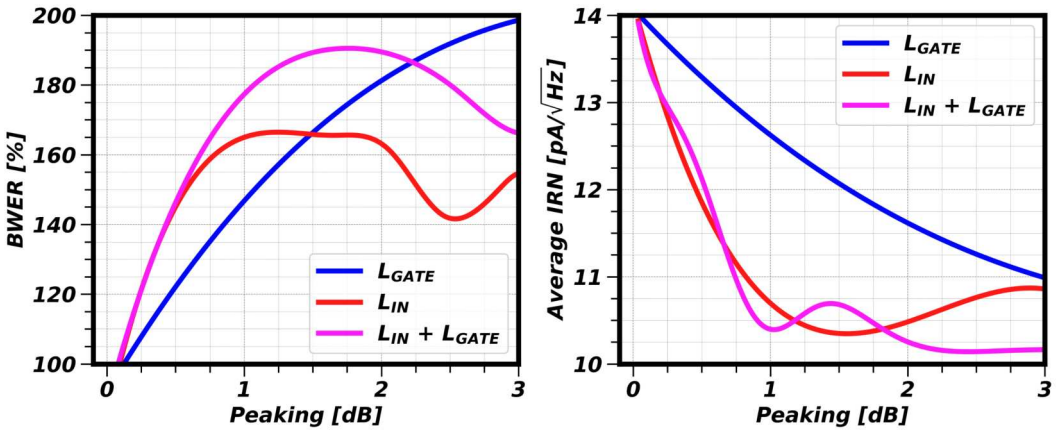


Figure 3.51: Bandwidth Extension Ratio (left) and Average IRN (right) vs. Peaking for the L_G and L_{IN} peaking schemes and the combination of the two obtained from circuit simulations with wire-bonding inductors as well.

3.4 Effect of Photodiode Model

The photodiode (PD) model heavily impacts the achievable performances of the receiver. The most known PD parasitic is its junction capacitance, which is inextricably linked to the IN limit, as seen in Equation 3.22[22]. However, it is not the only important aspect: the wire-bond parasitic inductance is extremely relevant as well, so much as to motivate costly research on flip-chip packaging in order to minimize it. In this section, all the parasitic elements in Figure 3.2 will be tuned to gain intuition on their interaction with the TIA. The starting point will be the LNTA circuit shown in Figure 3.29 with the circuit parameters reported in Table 3.2 and $L_{IN} = 70pH$, $L_G = 20pH$, and $L_{OUT} = 0pH$. Such values are the result of the circuit design which will be explained in the next chapter but for now they only constitute a starting point

PD model parasitic	Default value
C_{PD}	25 fF
L_{WB}	150 pH
R_S	20 Ω
τ	2 ps

Table 3.3: Default values of the parasitics in the PD model reported in Figure 3.2.

to show the impact of the PD parasitics.

Table 3.3 reports the default values of the PD model parasitics which will be used, except for the one subject to parametric sweep. These values are the result of fitting of the s-parameter measurements of a commercial photodiode supplied by the partner company.

Impact of L_{WB}

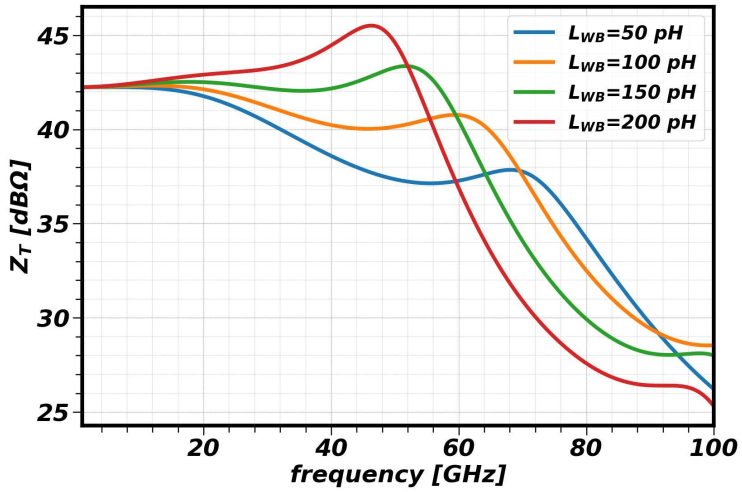


Figure 3.52: Frequency behavior of the transimpedance gain of the TIA circuit in Figure 3.29 with the complete PD model in Figure 3.2 when varying L_{WB}. Circuit parameters and PD parasitics are set to the default values reported in Table 3.2 and Table 3.3, respectively, while $L_{IN} = 70pH$, $L_G = 20pH$, and $L_{OUT} = 0pH$.

The wirebonding inductance heavily alter the high-frequency component of the signal, as shown in Figure 3.52 and Figure 3.53. The noise is deeply affected as well, as it can be seen in Figure 3.54. This is to be expected, since

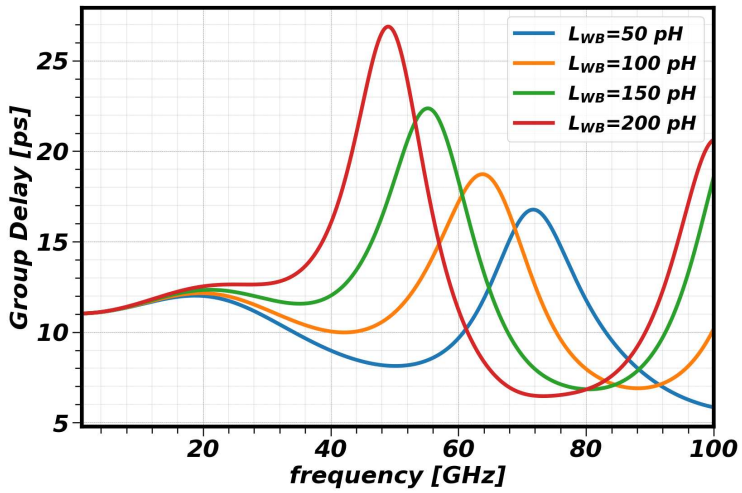


Figure 3.53: Frequency behavior of the group delay of the TIA circuit in Figure 3.29 with the complete PD model in Figure 3.2 when varying L_{WB}. Circuit parameters and PD parasitics are set to the default values reported in Table 3.2 and Table 3.3, respectively, while $L_{IN} = 70pH$, $L_G = 20pH$, and $L_{OUT} = 0pH$.

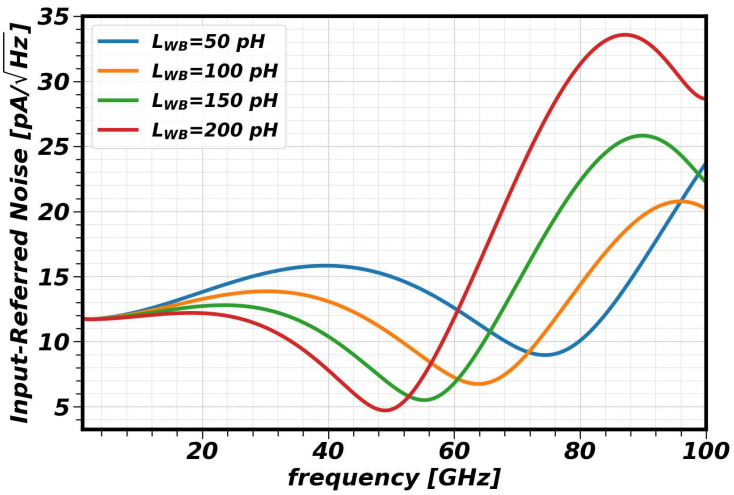


Figure 3.54: Frequency behavior of the input-referred noise current density of the TIA circuit in Figure 3.29 with the complete PD model in Figure 3.2 when varying L_{WB}. Circuit parameters and PD parasitics are set to the default values reported in Table 3.2 and Table 3.3, respectively, while $L_{IN} = 70pH$, $L_G = 20pH$, and $L_{OUT} = 0pH$.

L_{WB} splits C_{PD} from the pad & ESD parasitic capacitance, much like L_{IN} does with C_{IN} and C_G. Indeed, the effect of these two inductances is quite similar to each other, since they are placed closed to each other at the input of the LNTA. This implies that the presence of L_{WB} needs to be accounted for since the inception of the chip design. Tolerances on the wire-bonding length,

hence inductance, needs to be tightly controlled as well, since any change could heavily impact the transfer function. For this reason, it is industry practice to foresee some kind of on chip analog equalization, i.e. peaking control, to counterbalance the variation of L_{WB} within some margin.

Impact of C_{PD}

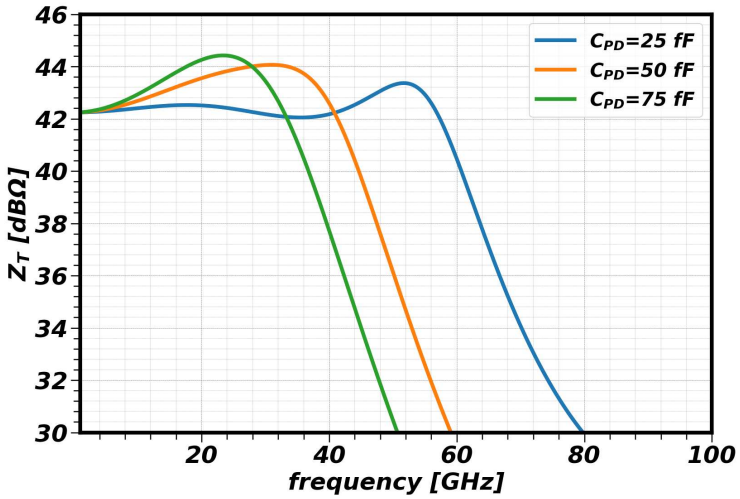


Figure 3.55: Frequency behavior of the transimpedance gain of the TIA circuit in Figure 3.29 with the complete PD model in Figure 3.2 when varying C_{PD}. Circuit parameters and PD parasitics are set to the default values reported in Table 3.2 and Table 3.3, respectively, while $L_{IN} = 70pH$, $L_G = 20pH$, and $L_{OUT} = 0pH$.

The parasitic PD capacitance is the most known undesired side effect of using photodiodes as photodetectors. The most obvious and visible impact is one the TIA bandwidth, but the transfer function shape and the group delay are affected as well, as shown in Figure 3.55 and Figure 3.56, respectively. However, since the bandwidth reduces, the GDV from 1 GHz to the -3 dB frequency is in reality not changing too much. The noise is only affected by the reduction of bandwidth, that pushes the white-to-violet transition at a lower frequency. In summary, C_{PD} only affects the transfer function bandwidth and shape.

Impact of R_S

The series resistance is an often disregarded parasitic of a photodiode, but it controls the quality factor of the poles associated to the resonance of L_{WB},

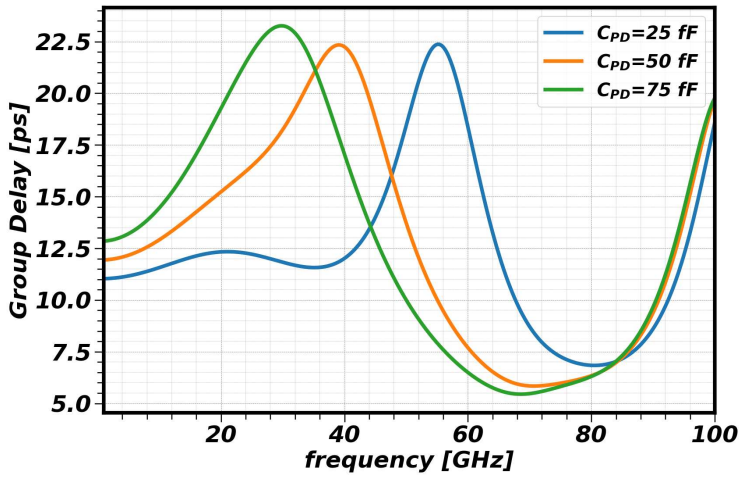


Figure 3.56: Frequency behavior of the group delay of the TIA circuit in Figure 3.29 with the complete PD model in Figure 3.2 when varying C_{PD}. Circuit parameters and PD parasitics are set to the default values reported in Table 3.2 and Table 3.3, respectively, while $L_{IN} = 70pH$, $L_G = 20pH$, and $L_{OUT} = 0pH$.

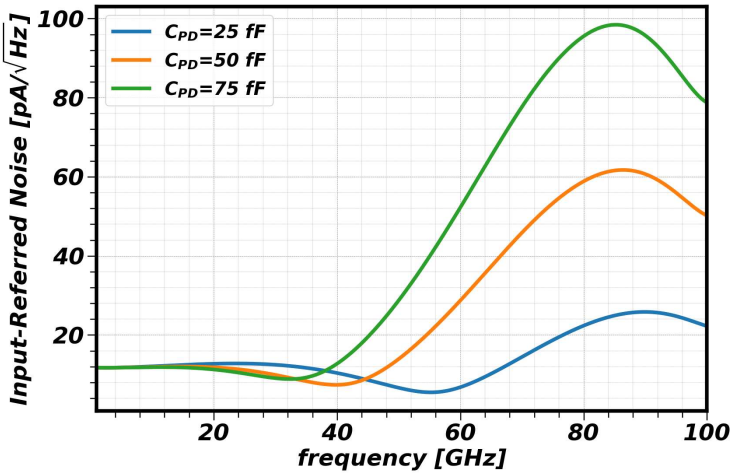


Figure 3.57: Frequency behavior of the input-referred noise current density of the TIA circuit in Figure 3.29 with the complete PD model in Figure 3.2 when varying C_{PD}. Circuit parameters and PD parasitics are set to the default values reported in Table 3.2 and Table 3.3, respectively, while $L_{IN} = 70pH$, $L_G = 20pH$, and $L_{OUT} = 0pH$.

hence the high-frequency peaking in the transfer function, as it can be seen in Figure 3.58: the higher the value, the lower the peaking, but also possibly the bandwidth. Inevitably, the group delay is impacted as well, as shown in Figure 3.59, reducing the GD peak and the GDV up to the -3 dB frequency. Figure 3.60 displays how the noise minimum lowers with lower R_S values, but this is compensated by a greater transfer function bandwidth over which the

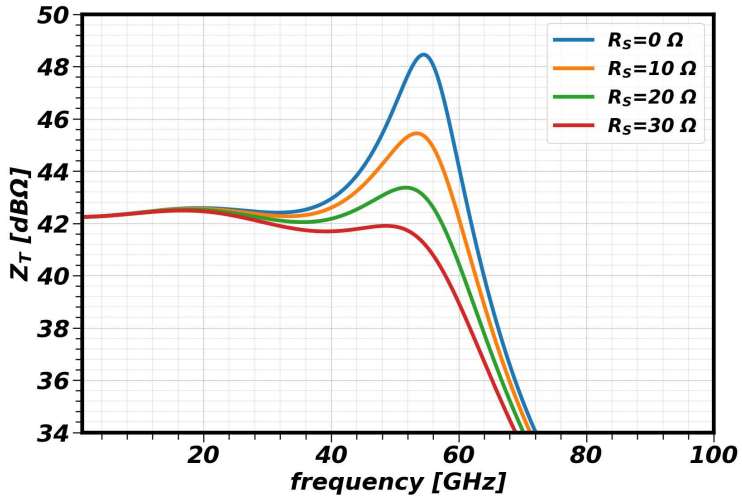


Figure 3.58: Frequency behavior of the transimpedance gain of the TIA circuit in Figure 3.29 with the complete PD model in Figure 3.2 when varying R_S. Circuit parameters and PD parasitics are set to the default values reported in Table 3.2 and Table 3.3, respectively, while $L_{IN} = 70pH$, $L_G = 20pH$, and $L_{OUT} = 0pH$.

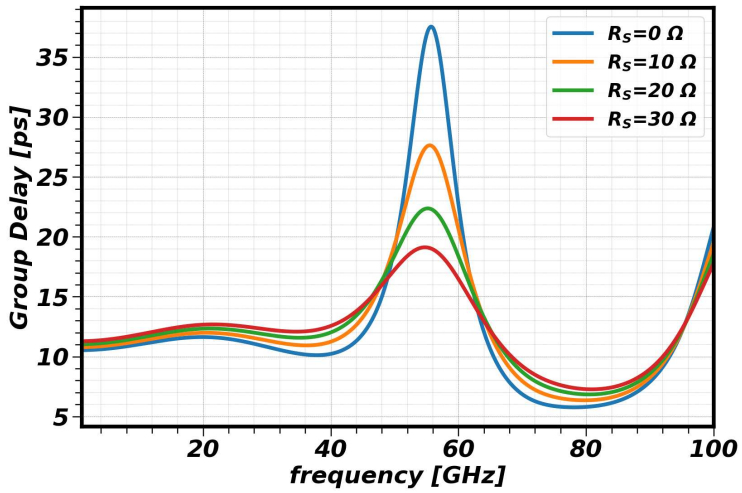


Figure 3.59: Frequency behavior of the group delay of the TIA circuit in Figure 3.29 with the complete PD model in Figure 3.2 when varying R_S. Circuit parameters and PD parasitics are set to the default values reported in Table 3.2 and Table 3.3, respectively, while $L_{IN} = 70pH$, $L_G = 20pH$, and $L_{OUT} = 0pH$.

average noise is integrated.

Impact of carrier transit time

The PD carrier transit time (see Equation 3.1) is a technological parameter which is not part of the packaging, but much like C_{PD} is linked to the photonic

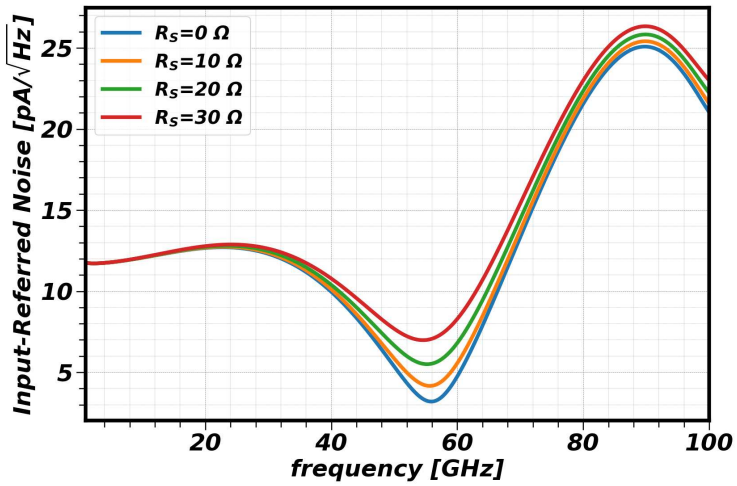


Figure 3.60: Frequency behavior of the input-referred noise current density of the TIA circuit in Figure 3.29 with the complete PD model in Figure 3.2 when varying R_S. Circuit parameters and PD parasitics are set to the default values reported in Table 3.2 and Table 3.3, respectively, while $L_{IN} = 70pH$, $L_G = 20pH$, and $L_{OUT} = 0pH$.

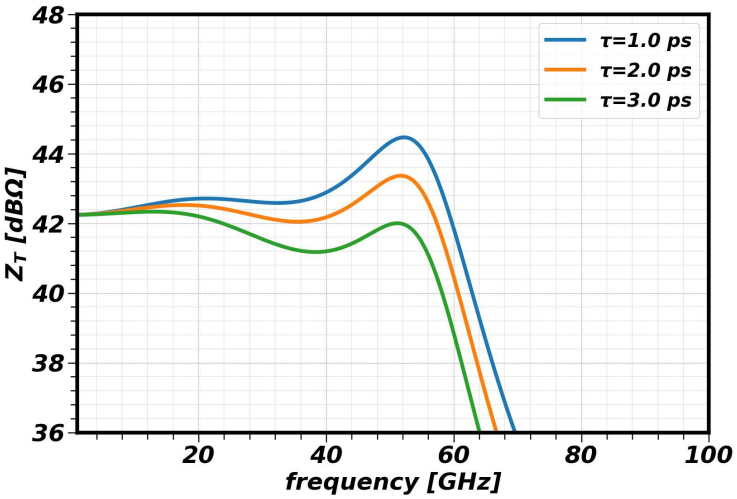


Figure 3.61: Frequency behavior of the transimpedance gain of the TIA circuit in Figure 3.29 with the complete PD model in Figure 3.2 when varying the carrier transit time. Circuit parameters and PD parasitics are set to the default values reported in Table 3.2 and Table 3.3, respectively, while $L_{IN} = 70pH$, $L_G = 20pH$, and $L_{OUT} = 0pH$.

technology being used. Its impact on the transfer function, group delay, and noise is shown in Figures 3.61, 3.62, and 3.63, respectively. Its impact is somewhat similar to the one of L_{WB}, boosting or attenuating the high-frequency signal components, although without affecting the bandwidth too much. Conversely, the group delay only changes in the low-frequency range. Overall, with

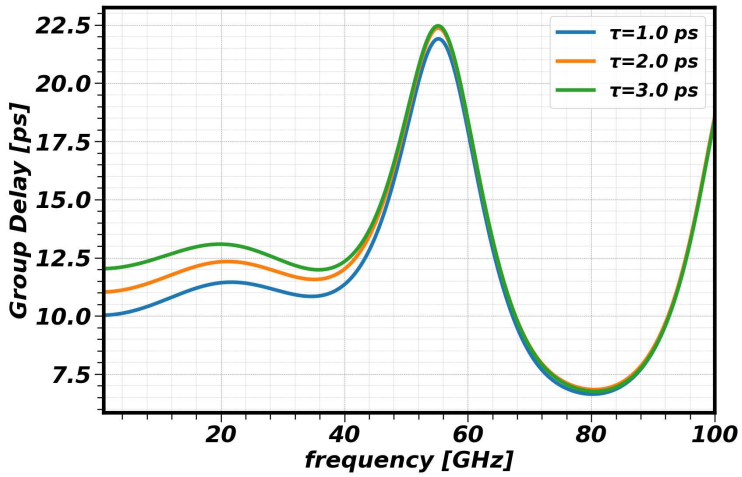


Figure 3.62: Frequency behavior of the group delay of the TIA circuit in Figure 3.29 with the complete PD model in Figure 3.2 when varying the carrier transit time. Circuit parameters and PD parasitics are set to the default values reported in Table 3.2 and Table 3.3, respectively, while $L_{IN} = 70pH$, $L_G = 20pH$, and $L_{OUT} = 0pH$.

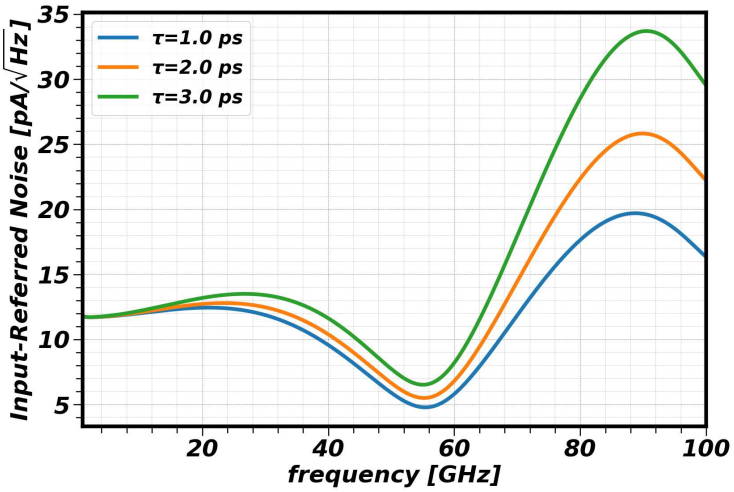


Figure 3.63: Frequency behavior of the input-referred noise current density of the TIA circuit in Figure 3.29 with the complete PD model in Figure 3.2 when varying the carrier transit time. Circuit parameters and PD parasitics are set to the default values reported in Table 3.2 and Table 3.3, respectively, while $L_{IN} = 70pH$, $L_G = 20pH$, and $L_{OUT} = 0pH$.

increasing transit time, the bandwidth reduces mildly, as does the GDV, while average IRN slightly increases.

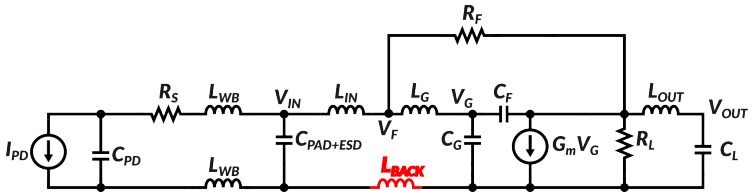


Figure 3.64: Small-signal circuit of the LNTA with passive bandwidth extensions inductances and PD small-signal model as well, as in Figure 3.30, but with parasitics (L_{BACK}) highlighted in red on the signal current return path.

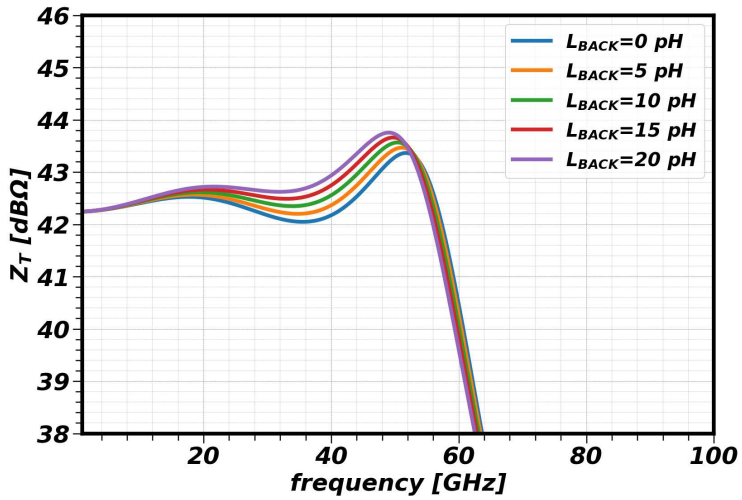


Figure 3.65: Frequency behavior of the transimpedance gain of the TIA circuit in Figure 3.64 when varying L_{BACK}. Circuit parameters and PD parasitics are set to the default values reported in Table 3.2 and Table 3.3, respectively, while $L_{IN} = 70pH$, $L_G = 20pH$, and $L_{OUT} = 0pH$.

3.5 Impact of Supply Parasitic Inductance

Supply voltages and ground are electrically connected to the chip through long wire-bonds that present parasitic inductances much higher than the one previously addressed when observing the impact of L_{WB} in the photodiode model, in the order of nH. While they guarantee an extremely low resistance in DC, at high-frequencies, where the signal operates, they act as open-circuits. For differential circuits, this would not affect the differential signal as long as layout is taken care of properly. However, in SROI AFE design, one or more stages in the signal chain will inevitably be single-ended. This in particular means that signal current will flow into the single-ended LNTA and then back into the photodiode, in this way closing the circuit and forcibly passing through

any parasitic that such connection may present. A resistive component would cause source degeneration on the inverter, lowering the DC transimpedance and loop gains, but it can easily be counterbalanced with proper layout of such sensitive interconnections. An inductive component, however, is trickier. Displayed in red and labeled L_{BACK} in the small-signal circuit of the LNTA in Figure 3.64, it is only one inductance since it is assumed that big shunting capacitors between and V_{DD} and ground are used, as is customary in high-frequency design, so as to guarantee that V_{DD} is AC ground, which implies that only the ground parasitics are perceived by the signal.

The effect of L_{BACK} on the transfer function of the LTNA is shown in Figure 3.65, where it can be seen that the ripple in the transimpedance magnitude increases with increasing inductance values. The effect on GD and IRN (not shown) is negligible. Since peaking in the transfer function badly affects the eye diagram, this means that L_{BACK} must minimized in layout design by employing distributed metal planes for supply/ground distribution from the pads to the chip's active area.

Chapter 4

Design and Testing of a 224 Gbps PAM-4 Low-Power Transimpedance Amplifier in 12 nm FinFET

A typical optical receiver (oRX) analog front-end (AFE) for short-reach optical interconnections (SROI) is made of signal amplification chain of multiple cascaded stages. The first of such stages is a Low-Noise Transimpedance Amplifier (LNTA), directly wirebonded to a single photodiode (PD), that amplifies the signal current coming from the PD and converts it in an output voltage while adding the lowest amount of noise possible. A series of one or more voltage amplifiers comes after, the last of which is usually a low-gain buffer designed to drive and match the 50 Ω output differential transmission lines. In practice, having more than four amplifying stages after the LNTA is uncommon, due to possibly excessive power consumption and to the well known effect that lowers the chain bandwidth when N stages with equal -3 dB frequency are cascaded one after another (the chain bandwidth decreases by approximately $\sqrt{N}$)[20]. Since the overall AFE converts the input current into an output voltage, it is also confusingly called TIA or opto-TIA (oTIA), even if the only actual TIA in the AFE chain is the LNTA.

The previous chapter showed that careful design of a LNTA in 12 nm FinFET using an inverter-based shunt-feedback topology with passive inductive

bandwidth extension techniques can provide a transimpedance transfer function with >40 dBΩ DC gain, >60 GHz bandwidth, <10 ps group-delay variation (GDV) and <15 pA/$\sqrt{Hz}$ average input-referred noise (IRN) current. In this chapter, based on the analysis carried out in chapter 3, the design and implementation in 12 nm FinFET technology of a transimpedance amplifier (TIA) chip for 224 Gbps PAM-4 low-power, short-reach optical interconnections (SROI) will be reported, as well as it experimental measurement results, which will be compared to simulations.

The design and fabrication of the PD was not part of the present project. Experimentally measured s-parameters of a commercially available PD were provided by the project partner company, Huawei Italy S.r.L. Such PD s-parameters, hereafter often called "PD model", have been used as the inalterable project starting point and performances of the oRX AFE were always evaluated when coupled to the given PD model.

4.1 Variable Gain Amplifier

Gain variation is necessary to allow for a range of input signal amplitude in which the receiver can operate. It can be achieved in the LNTA, the following voltage amplifiers or both. However, tuning the gain at either the LNTA or the output buffer demands great design care, as it can easily lead to higher noise (as it implies additional devices that add their own noise to the mix), lower bandwidths (more devices means possibly higher parasitic capacitances) and/or output impedance mismatch. For this reason, it is more common to relegate gain variation to the voltage amplifier(s) between the LNTA and the output buffer, hence called variable gain amplifiers (VGA, although sometimes they can be called limiting amplifiers)[20].

A VGA needs to amplify the signal typically by 10 dB while allowing a tuning range of 5÷10 dB (hence, it amplifies the signal by 0÷10 dB). There are multiple ways in which this can be achieved[20], however low-voltage supplies heavily compress the available design space. In such scenario, inverter-based topologies are most likely the best candidate, thanks to their good behavior with voltage scaling. Unfortunately, inverters do not offer many knobs with which to control the gain, except for the voltage supply, which is typically not

tunable.

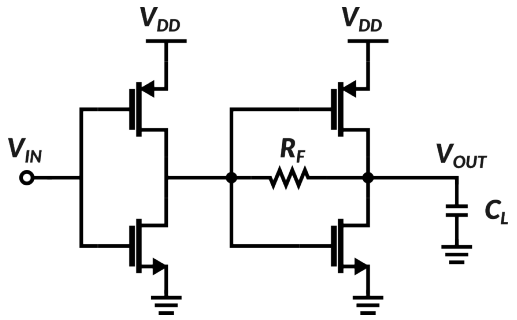


Figure 4.1: Single-ended Cherry Hooper voltage amplifier topology.

A topology which easily lends itself to inverter-based design is the Cherry-Hooper voltage amplifier[21]. Shown in Figure 4.1, it is made of an inverter transconductor (TC), which converts the input voltage signal into the output current and injects into the following shunt-feedback (SF) transimpedance amplifier (TIA) that converts it back into the output voltage of the amplifier. Approximately, then, the gain of this amplifying stage is the product of TC transconductance and TIA feedback resistance. The SF TIA was analyzed in greater details in the previous chapter: here, much of the previous results will be reused without running through the computations again.

The key principle for Cherry-Hooper amplifiers to work properly is to ensure that the output impedance of the TC is much higher than the input impedance of the TIA, so that all the signal current from the TC flows only into the feedback resistance. Using inverters, this is readily achieved, since the output impedance of the TC is $\approx r_{o,TC}/2$ (where $r_{o,TC}$ is the drain-source small-signal resistance of the MOS transistors that make up the TC) while the input impedance of the TIA is $\approx 1/2g_{m,TIA}$ (where $g_{m,TIA}$ is the small-signal transconductance of the MOS transistors that make up the TIA). This means that the voltage swing at the node between the TC and the TIA is much smaller when compared to the output voltage, hence it can be approximated as a virtual ground, since the gain from V_{IN} to such node is $\approx g_{m,TC}/g_{m,TIA}$ (which can also be smaller than one depending on the ratios between the TC's and the TIA's inverters) while the stage gain is $\approx g_{m,TC}R_F$. Any Miller effect on the gate-drain capacitance of the TC is also suppressed in this way, lowering the capacitive burden on the previous stage. If the TC has high output impedance, it means that it resembles an ideal voltage-controlled current

source. Then, the small-signal equivalent circuit of the Cherry-Hooper amplifier is qualitatively identical to the one in Figure 3.30, i.e. a SF TIA with an ideal input current source.

The Cherry-Hooper amplifier in Figure 4.1 offers the possibility of gain tuning by changing the feedback resistance. This can be achieved by placing a transistor in parallel to R_F, properly biased so as to reduced the resulting total feedback resistance, hence the stage gain. Since the node between the TC and the TIA is a virtual ground and its bias is known ($\approx V_{DD}/2$), by using an nMOS with the drain connected to the output and selecting the gate bias voltage so as to place it in triode region, a linear tunable resistance is achieved. Since no DC current flows though such transistor, its dimensions can be optimized so as to reduce its capacitive impact, which is however unavoidable and is one of the drawbacks of such technique, alongside a rapidly increasing signal distortion with lowering of the gain.

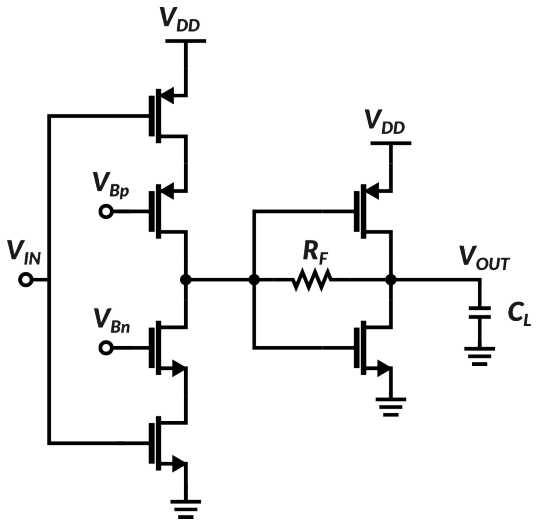


Figure 4.2: Single-ended Cherry Hooper voltage amplifier topology with cascoded inverter as transconductor.

The output impedance of the TC can be increased even more by using a cascode inverter structure as transconductor, as shown in Figure 4.2, since its output impedance is $\approx g_m r_o^2/2$[19]. While more design intensive due to reduced voltage headroom, it can nonetheless be achieved with careful selection of voltage biases of the common-gate transistors. Using cascoded inverters now offers one more knob to tune the gain: by lowering/raising the gate bias voltage of the common-gate nMOS/pMOS, the drain voltage of the input

common-source nMOS/pMOS below/above will be pushed down/up by the same amount (source-follower principle). Eventually, the input transistors will be pushed into triode region, where their transconductance will be diminished. The gate bias voltage of the common-gate nMOS and pMOS will need to move in opposite directions, in a specular way with respect to $V_{DD}/2$. Such technique has already been used successfully in Mach-Zehnder Modulator drivers for coherent optical transmitters[12][26], where it has been shown that pushing the input transistors into triode region leaves the Total Harmonic Distortion (THD) flat for most of the gain tuning range. Even more, such technique can afford to push the VGA gain down to the point of *attenuating* the signal, i.e. negative dB gain, still without excessively affecting the THD. For this reason, this topology was chosen in the designed chip.

To extend the bandwidth of the Cherry-Hooper VGA, the same techniques discussed in chapter 3 can be used. However, in this case the capacitive loading at the input node of the TIA is much lower, mainly coming from the TIA itself, while C_L may or may not be the dominant pole depending on the stage coming after. For this reason, it was found that a single gate inductance L_G could sufficiently boost the high-frequency signal.

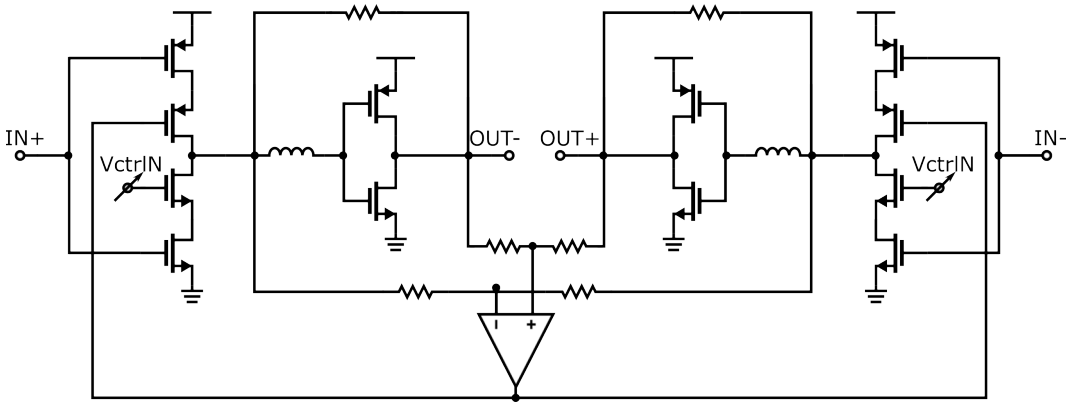


Figure 4.3: Differential Cherry Hooper voltage amplifier topology with local CMFB.

To make the circuit in Figure 4.2 differential, it would be sufficient to replicate it in a specular way. However, since inverters are highly affected by voltage and process variations, a local common-mode feedback (CMFB) loop must be added. Such loop can be implemented as shown in Figure 4.3. The loop ensures that the output and input common-mode voltages of the TIA within the Cherry-Hooper topology are identical, so that no common-

mode current flows through the feedback resistances, which would otherwise unbalance the DC bias. The two common-mode voltages are compared by an OPAMP which then controls gate bias voltage of the common-gate pMOS transistors of the cascode transconductors. In this way, only the gate of the common-gate nMOS transistors will need to be controlled to tune the gain, and the local CMFB loop will take care of the pMOS transistors bias while also ensuring proper common-mode biasing of the stage. The CMFB was designed to achieve more >30 dB of loop gain and >70° of phase margin. Of course, such technique has the drawback of not working properly over heavily skewed corners in which pMOS transistors are much weaker than the nMOS, since it greatly reduces the loop gain.

4.2 Single-Ended-to-Differential Conversion

The need for differential transmission lines at the output of the AFE stems from the fact that the system components coming after it are usually placed at a distance much bigger than the smallest signal wavelength. Differential signaling in such cases allow for higher tolerance to common-mode noise and interferences, but since the oRX input is single-ended (only one PD is used, as mentioned in section 1.2), this entails that a single-ended-to-differential (S2D) conversion is necessary along the signal chain. Since moving from a single-ended to a differential signal implies replicating the single-ended signal onto a new electrical conductor but with 180° phase shift, the new differential signal will theoretically have twice the amplitude and the same phase of the original single-ended signal, i.e. a 6 dB gain increase. In practice, achieving a wideband S2D conversion without deviating from an ideal flat-phase response is a challenging task. The S2D conversion placement is subject to a trade-off: the closer to the output buffer, the lower the AFE power consumption due to the reduced number of differential stages; the closer to the LNTA, the lower the effect of parasitic impedances on the supply and ground connections.

One possible way of implementing an S2D conversion is shown in Figure 4.4, where the first limiting amplifier (i.e. VGA) is a differential stage that senses the LNTA output at one of its two inputs while the other input is a fixed bias, that is AC ground. While cheap and easy to implement, this technique

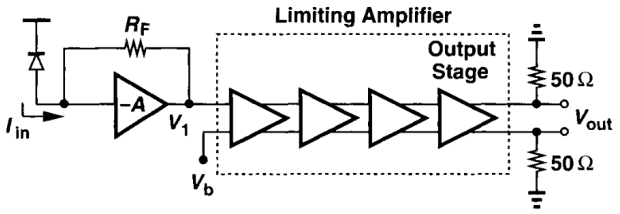


Figure 4.4: S2D conversion technique using a bias replica at the first limiting amplifier (only its V_b bias is shown)[20].

has the drawback of not creating a really differential signal at the output of the first VGA, since one of the two inputs is actually only a DC bias fixed in time. This means that the output signal will have a substantial common-mode component as well as distortion coming from even-order harmonics which would be rejected by a true differential signaling. Such technique relies on the common-mode rejection of the differential stages to create a proper differential signal at the output of the chain, and it can also be implemented anywhere along the chain, even before the LNTA (which would then be a differential topology). The bias voltage V_b could be provided by a DC offset compensation (DCOC) loop that ensures that no differential offset at DC is present at the output of the chain.

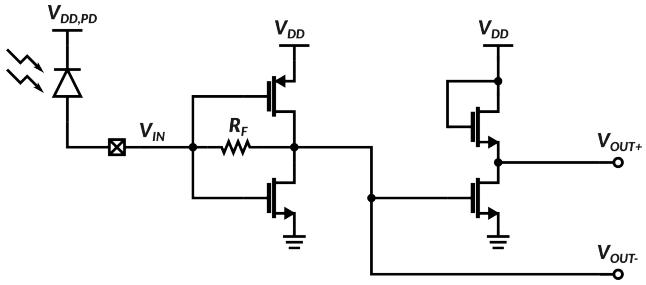


Figure 4.5: S2D conversion technique using an n-over-n -1 gain stage placed after the LNTA.

Another possible S2D topology requires actively creating the opposite polarity signal. Shown in Figure 4.5, it requires inserting a -1 gain stage, i.e., an inverting circuit with unitary gain. This can be achieved by using a "n-over-n" topology, that is a common-source nMOS loaded by a diode-connected nMOS with identical sizing. Since the impedance of a diode-connected is $1/g_m$, assuming that the two nMOS have identical transconductance, that DC gain of such stage is $g_{m,down}/g_{m,up} \approx -1$. The gain expression of this stage can be

approximated as:

$$H_{-1stage}(f) = -\frac{1}{1 + s\frac{C_{GS}+C_L}{g_m}} \tag{4.1}$$

where C_{GS} and g_m are the gate-source capacitance and the transconductance of the diode-connected nMOS, respectively, and C_L is the loading capacitance from the next stage connected at V_{OUT+} in Figure 4.5.

The sizing of the two transistors is subject to a trade-off: too small, and the common-source nMOS will not have enough current to charge the loading capacitance from the next stage sufficiently fast (the stage does not have enough bandwidth); too large, and the previous stage will be affected by the input capacitance of the -1 stage. This trade-off is even more severe for the phase of the output inverted signal: while a small amplitude imbalance can be tolerated (also because the roll-off in Equation 4.1 is quite mild), a phase imbalance would invalidate the whole concept of S2D conversion (and the phase changes much faster, already losing 45° at $g_{m,up}/(C_{GS,up} + C_{LOAD})$).

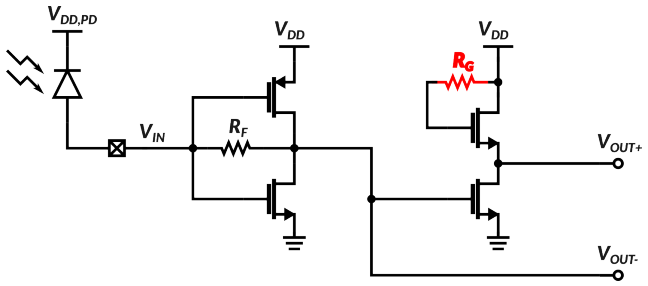


Figure 4.6: S2D conversion technique using an active inductor -1 gain stage placed after the LNTA.

A possible solution would be to place a resistor on the gate of the diode-connected nMOS, implementing an active inductor[27]. Shown in Figure 4.6, the transfer function of such circuit would now become:

$$H_{-1stage}(f) = -\frac{1 + sR_G(C_{GD} + C_{GS})}{1 + s\left(R_G C_{GD} + \frac{C_{GS}+C_L}{g_m}\right) + s^2\frac{R_G}{g_m}(C_{GS}C_{GD} + C_{GS}C_L + C_{GD}C_L)} \tag{4.2}$$

As it can be seen from Equation 4.2, the transfer function now has a zero and two complex poles. If the value of R_G is selected properly, a flat response with a large bandwidth and minimal group delay variation can be achieved without the use of area-intensive inductors.

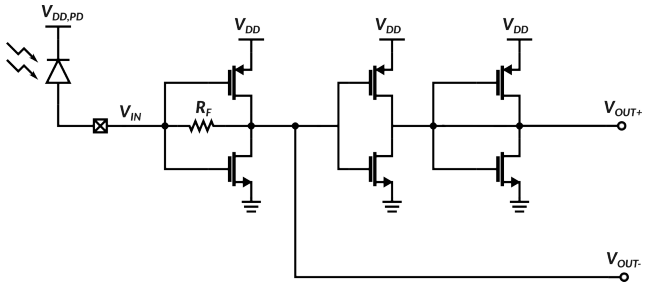


Figure 4.7: S2D conversion technique using an unitary gain Cherry-Hooper as -1 gain stage placed after the LNTA.

Figure 4.7 shows another way to implement the -1 stage by using a Cherry-Hooper topology with a short instead of a feedback resistance. If the transconductor and the diode-connected TIA are sized identically, then a $-g_m/g_m$ gain is obtained, much like for the n-over-n circuit in Figure 4.5. This technique has the added benefit of being inverter-based, which makes it highly compatible with oRX AFE in scaled CMOS nodes, which are usually made of chain of inverters (that is, they spread with voltage and corners in the same way). Also, if a loop is placed around the single-ended LNTA to make sure that no DC current flows into its feedback resistance, then the transconductor is already properly biased by design, having diode-connected inverters both at the input and at the output.

The only drawback of such topology is the capability of compensating phase imbalances like seen in Figure 4.6 with the use of the active inductor. It can be achieved by using passive inductors to extend the bandwidth like it was discussed in chapter 3, but it would consume much more area.

4.3 Buffer

The last stage in an AFE signal chain, the buffer only needs to drive the 50 Ω output differential transmission lines without excessively loading the previous stages with its input capacitance. Some additional gain would be a plus, but it is not strictly required. This makes the buffer design look deceptively simple, while in reality is just as challenging as the other chain blocks.

Since output matching is required, it is not common to implement buffers with inverters. The most common topology is the standard differential pair

with 50 Ω passive resistive loads. However, such topology suffers strict trade-offs due to the low load impedance (50 Ω differential, 25 Ω single-ended due to the 50 Ω external loads being in parallel to internal 50 Ω loads of the differential pair itself). This normally requires the differential pair transistors to be quite huge, hence heavily loading the previous stage and drawing a lot of power which can easily end up having the biggest share of the total AFE power consumption.

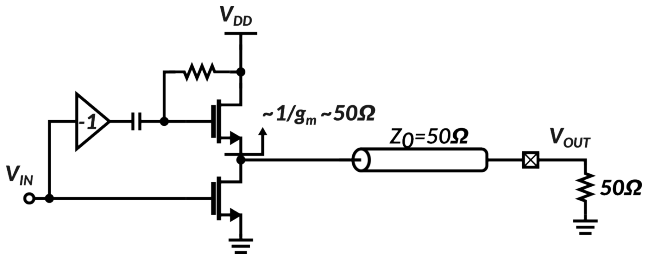


Figure 4.8: Single-ended buffer driving a 50 Ω transmission line with impedance matching achieved with a source-follower.

An alternative solution is to use source followers for output matching. Shown in Figure 4.8, it uses a common-source transistor to drive the load and source-follower for impedance matching. This requires $g_m \approx 20$ mS for the source-follower. The only advantage of such technique with respect to a passive resistive load is that it enables low-voltage design, thanks to the fact that now the current - voltage headroom trade-off is much more relaxed. Also shown in Figure 4.8 is a -1 stage AC coupled to the gate of the source follower, which boosts the stage gain by a linear +1 by injecting the signal on the gate of the source follower without having to increase the stage power consumption. A source follower being non inverting, the input signal polarity must be inverted, hence the -1 stage, in order to have gain boost instead of a gain compression. In a differential stage, the opposite polarity signal is readily available at the other half of the stage, avoiding the use of the -1 block altogether, which has been successfully used in a coherent optical receiver[11].

The circuit in Figure 4.8 lends itself much more easily to inverter-based design. Both the common-source and the source-follower can be made complementary, as shown in Figure 4.9, where the circuit has been made differential as well. It can be seen that the source followers AC coupling takes the signal from the opposite polarity of the input, creating a cross-coupling structure.

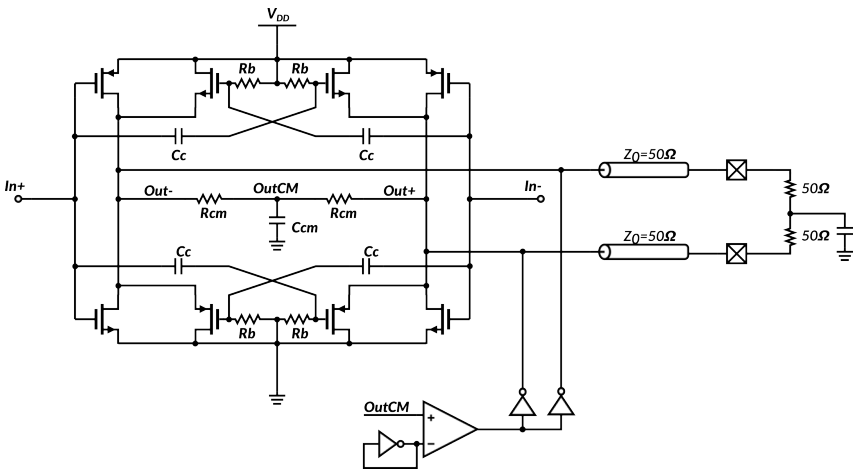


Figure 4.9: Differential inverter-based buffer driving 50 Ω differential transmission lines with impedance matching achieved with complementary source-followers.

Such topology is also effective in lowering the power consumption of the buffer without compromising neither on gain nor on matching, thanks to the linear +1 gain boost offered by the AC coupling on the source followers and the doubling of the transconductance obtained with the inverters.

4.4 Full Signal Chain

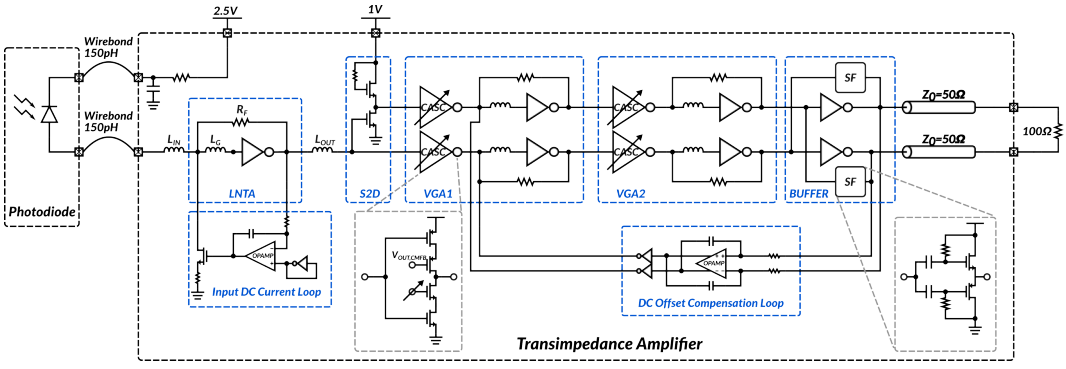


Figure 4.10: Complete chain topology of the designed 224 Gb/s PAM-4 low-power TIA.

Given all the aforementioned discussions, Figure 4.10 shows the complete chain topology of the designed 224 Gb/s PAM-4 low-power TIA in 12 nm FinFET. The TIA is designed to deliver a linear 500 mV peak-to-peak differential output voltage swing on a 100 Ω differential load with output matching. The maximum gain is 71 dBΩ continuously tunable down to 46 dBΩ while keeping

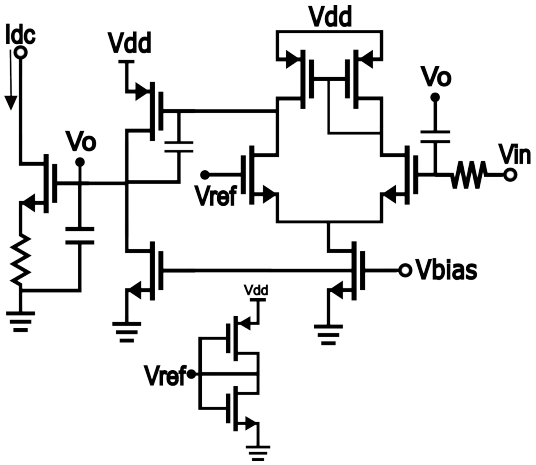


Figure 4.11: Schematic of the Input DC Current Loop block in Figure 4.10.

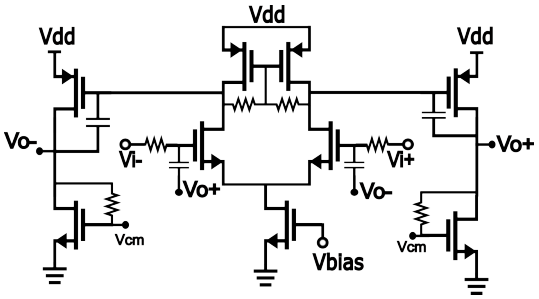


Figure 4.12: Schematic of the DC Offset Compensation loop block in Figure 4.10.

the THD lower than 5% for the whole range. The supply is 1 V for all the stages.

The single-ended input is sensed by a 42 dBΩ (R_F = 142 Ω) LNTA, with multiple bandwidth extension techniques, and then immediately converted into a differential signal with the S2D conversion made by an active inductor - 1 stage. The choice was made to move to differential signaling as soon as possible, so as to reduce as much as feasible the impact of supply parasitics and common-mode noise. Two 10 dB Cherry-Hooper VGAs follow, with gain tuning achieved in the cascoded inverter transconductors, and a final complementary buffer with source followers ensures wideband output impedance matching.

The PD needs to be reversed-biased with a high-voltage that is not compatible with 1 V supply of the chip. In order to reduce the parasitic wire-bond inductance, the PD takes its 2.5 V power supply from inside the TIA chip: an internal routing links the pad where the PD wire-bond lands to another

pad which is then connected to an external supply, separated from the TIA supply. However, the parasitics of such internal connection could also affect the high-frequency behavior of the chip. To avoid it, an AC coupling scheme was implemented so that the connection is AC ground at high frequencies.

Since the PD average current is not zero (the PD current varies between a low non-zero value, called dark current, and a high value maximum current), a loop, labeled Input DC Current Loop (IDCL), is placed around the LNTA to absorb it, otherwise the DC bias point of the LNTA itself would be completely altered. Shown in Figure 4.11, the IDCL is made of an integrator which compares the output voltage of the first stage to a diode-connected scaled replica of the LNTA and then drives a current-sinking nMOS that draws the PD mean current, in this way ensuring no DC current flows into the feedback resistance of the LNTA. By using resistive degeneration at the source of the current-sinking nMOS, the channel noise of such nMOS is greatly reduced, which would otherwise affect the input-referred noise of the whole receiver.

As mentioned in section 4.2, using a n-over-n S2D conversion stage will inevitably be badly affected by process, voltage and temperature variations (PVT), since it spreads differently with respect to inverter-based stages. Given that multiple gain stages come after the conversion, even a small offset could completely unbalance the differential chain. For this reason, a DC Offset Compensation (DCOC) stage must be inserted. Reported in Figure 4.11, the DCOC is made of a differential integrator that senses the chain differential output at low frequency and compensates it by implementing a negative feedback loop which is closed inside the first VGA stage. The point where the loop is closed was chosen to be the virtual ground node between the transconductor and the TIA of the first VGA, so as to be as close as possible to the S2D conversion without affecting the noise performance of the LNTA. The cut-off frequency of the integrator should be as low as technologically possible, as it creates a low-frequency -3dB cut-off for the signal itself, which can significantly alter the behavior of the receiver for longer bit sequences. The gain of the DCOC needs to be sufficiently high to compensate the differential offset for the whole gain tuning range, as the loop comprises two VGA stages inside.

The designed chip obtained a 72 dBΩ gain continuously tunable down 46 dBΩ with a 59.7 GHz bandwidth. The normalized transfer functions (TF) of

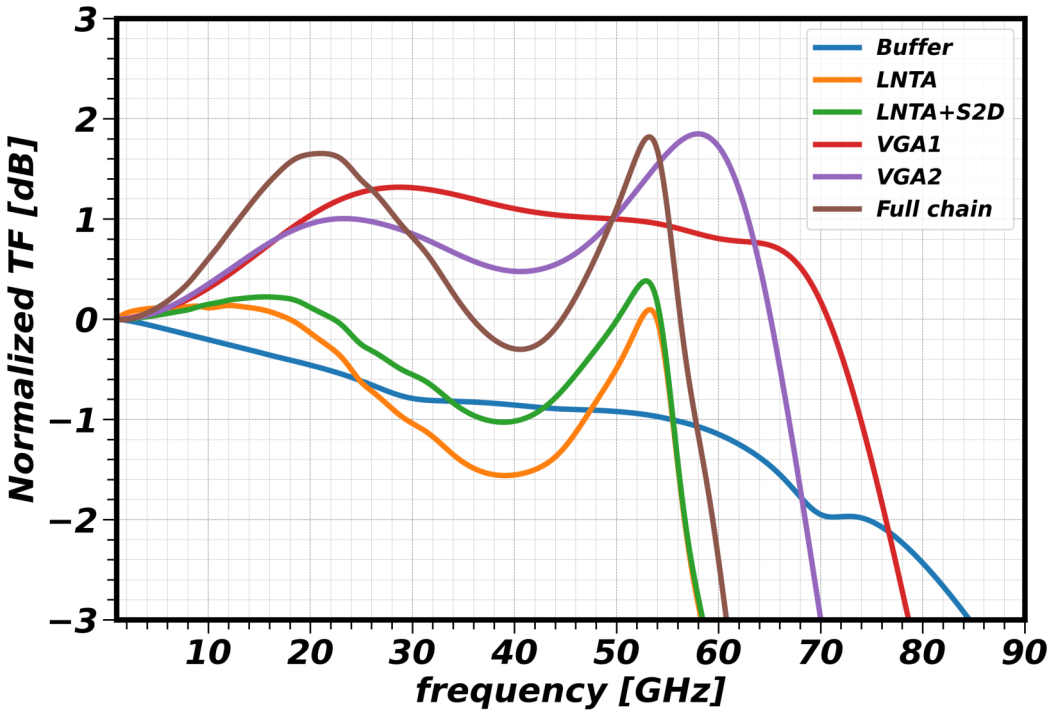


Figure 4.13: Normalized transfer functions of the various signal chain block from post-layout simulations of the designed TIA in Figure 4.10.

the various blocks along the signal chain obtained from post-layout simulations are shown in Figure 4.13. It can be seen that the total gain (black) has around 1.5 dB ripple while the bandwidth is ultimately limited by the LNTA. The VGAs have a much larger bandwidth while boosting the mid-frequency signal components (20÷40 GHz) where the LNTA has a local minimum. The buffer has the largest bandwidth, although its gain is steadily declining over frequency.

Figure 4.14 shows the input-referred noise current density for the full TIA, which presents a local minimum that was also observed in chapter 3 and is linked to the presence of L_{WB} and L_{IN} (see Figures 3.54 and 3.35).

Figure 4.15 reports the THD behavior for a 15 GHz fundamental as the gain is swept for the whole tuning range. As it can be seen, as the gain is decreased while keeping the output amplitude fixed, i.e. the input amplitude is increased, the THD initially *decreases*, which is beneficial and opposite the behavior traditionally expected from the harmonic distortion. After a certain threshold, the THD starts increasing, eventually at minimum gain becoming

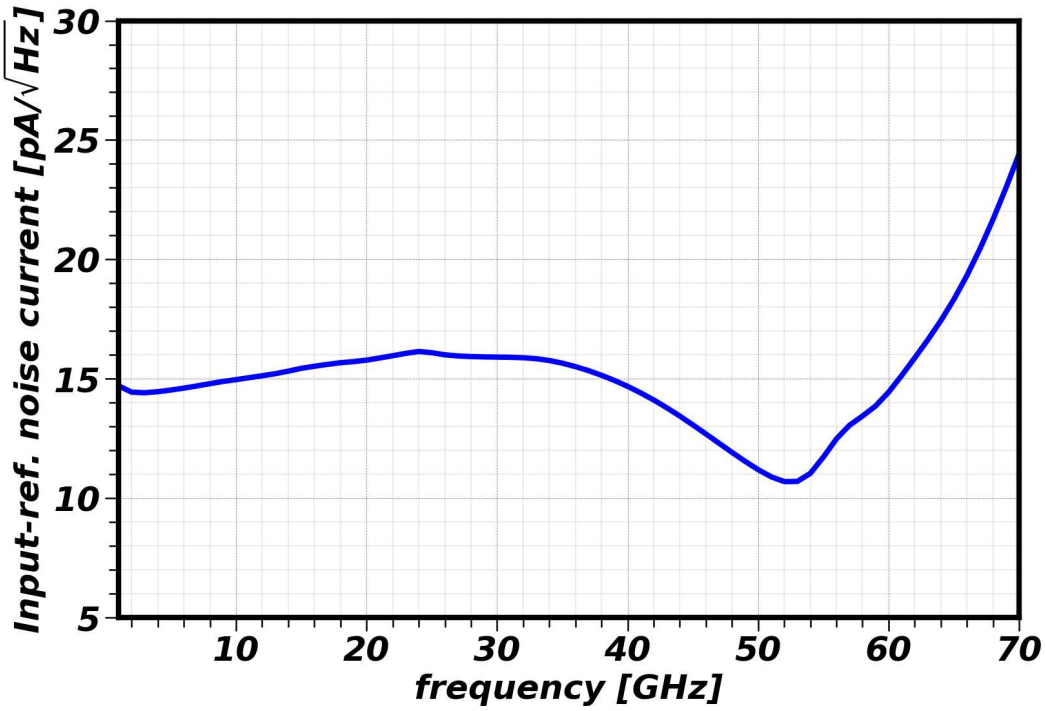


Figure 4.14: Input-referred noise current from post-layout simulations of the designed TIA in Figure 4.10.

higher the value at maximum gain. This can be explained in the following way: as the VGAs reach the bottom of their gain tuning range (which is 13 dB each), they are attenuating rather than amplifying, hence the buffer input amplitude is actually lower than the LNTA output amplitude. At such high amplitudes values, the LNTA distortion, which would usually be negligible when compared to the buffer distortion, becomes dominant.

Figures 4.16 and 4.17 show the 112 Gb/s NRZ and 224 Gb/s PAM-4 eye diagrams, respectively, both obtained from PRBS15 post-layout simulations. While some distortion is present (linked to in-band TF ripple more than anything else), the eye diagrams show good aperture. Since this chip was designed as an AFE for SROI oRX, a small amount of digital equalization is usually foreseen in such scenario, also enabled by the use of FinFET technology, and it would undoubtedly benefit the eye diagrams.

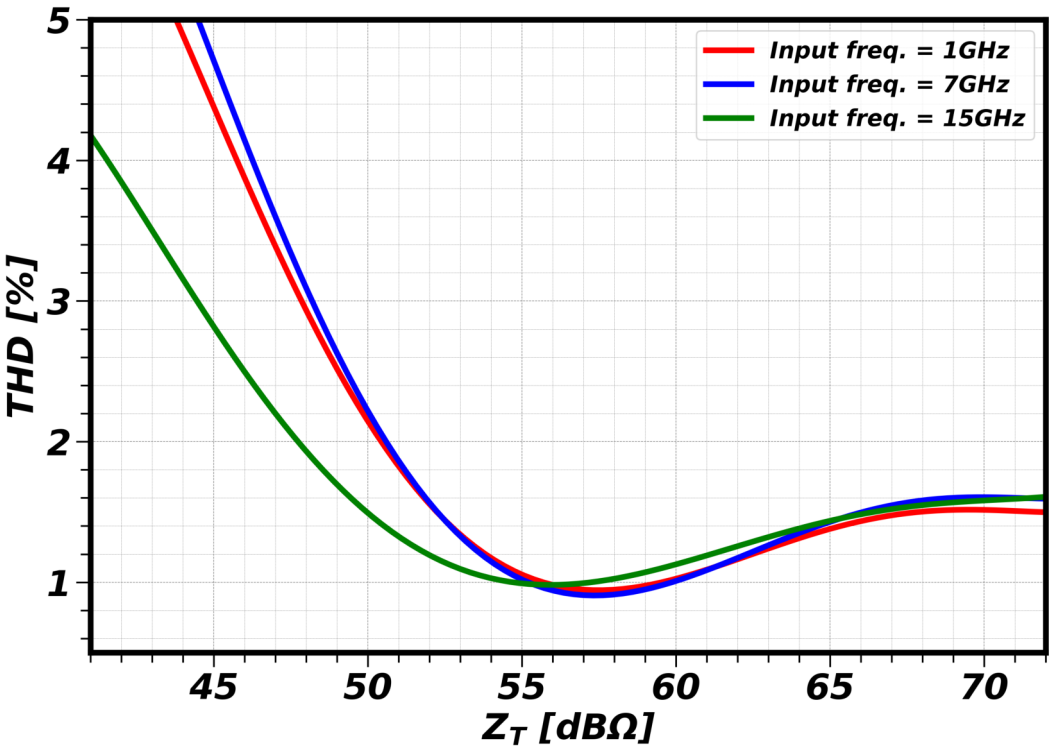


Figure 4.15: THD vs. TIA gain at fixed 500 mVpp differential output amplitude from post-layout simulations of the designed TIA in Figure 4.10.

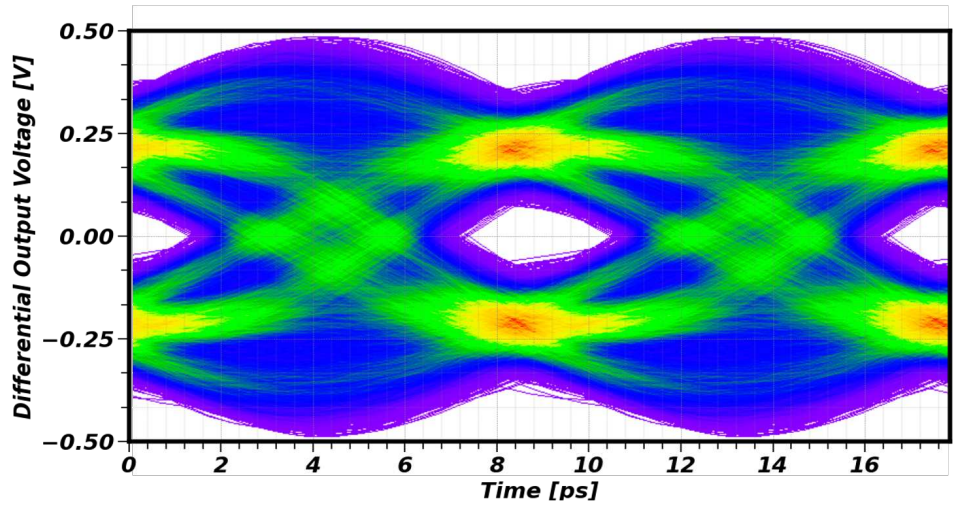


Figure 4.16: 112 Gb/s NRZ eye diagram from PRBS15 post-layout simulations of the designed TIA in Figure 4.10.

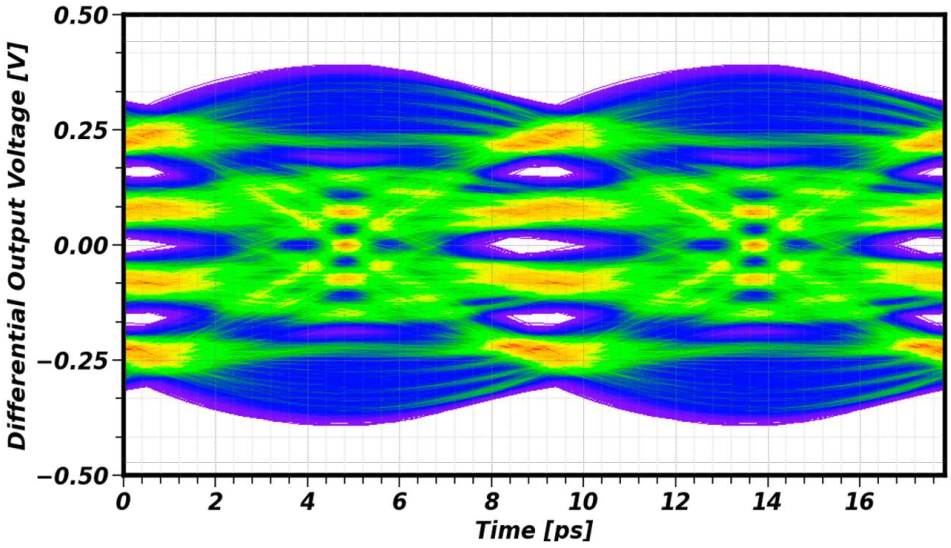


Figure 4.17: 224 Gb/s PAM-4 eye diagram from PRBS15 post-layout simulations of the designed TIA in Figure 4.10.

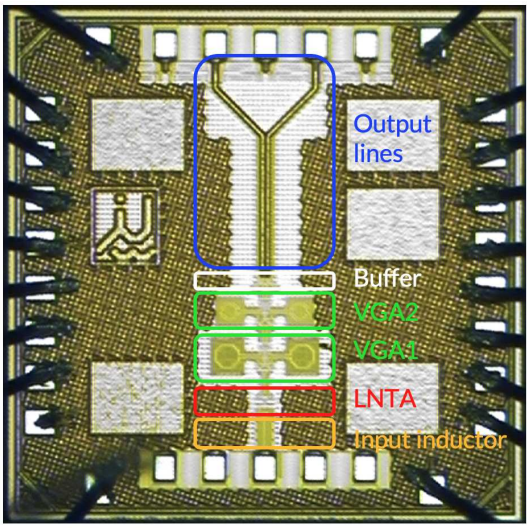


Figure 4.18: Microphotograph of the chip implementing the oRX AFE in Figure 4.10 in 12 nm FinFET with various stages highlighted.

4.5 Chip Layout

The oRX AFE described in the previous section was implemented in GlobalFoundries 12 nm LP+ FinFET technology. The microphotograph of the chip is reported in Figure 4.18. The die area is 1 mm^2, although the active area is much smaller, around 0.054 mm^2. Indeed, as it can be seen from the

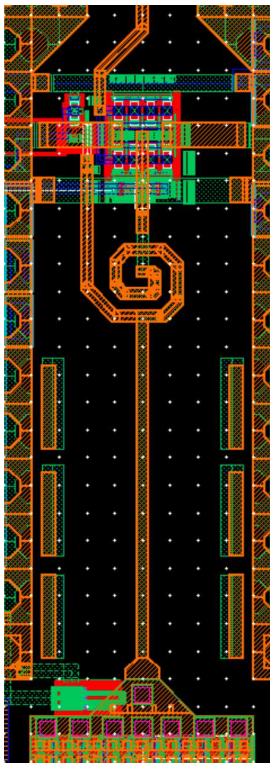
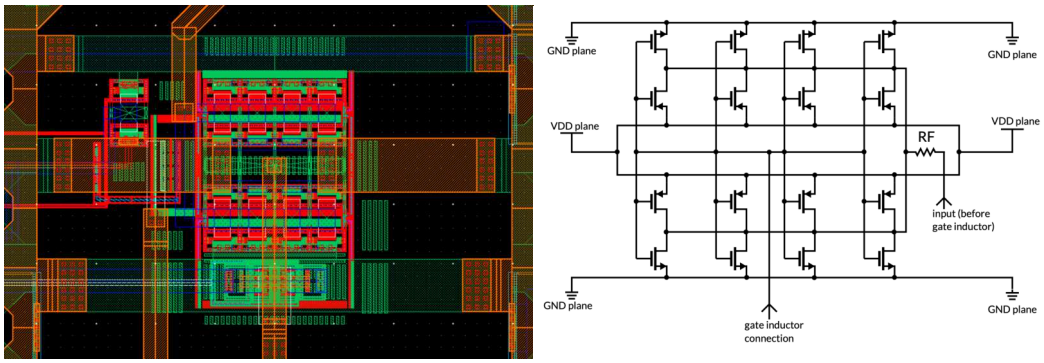


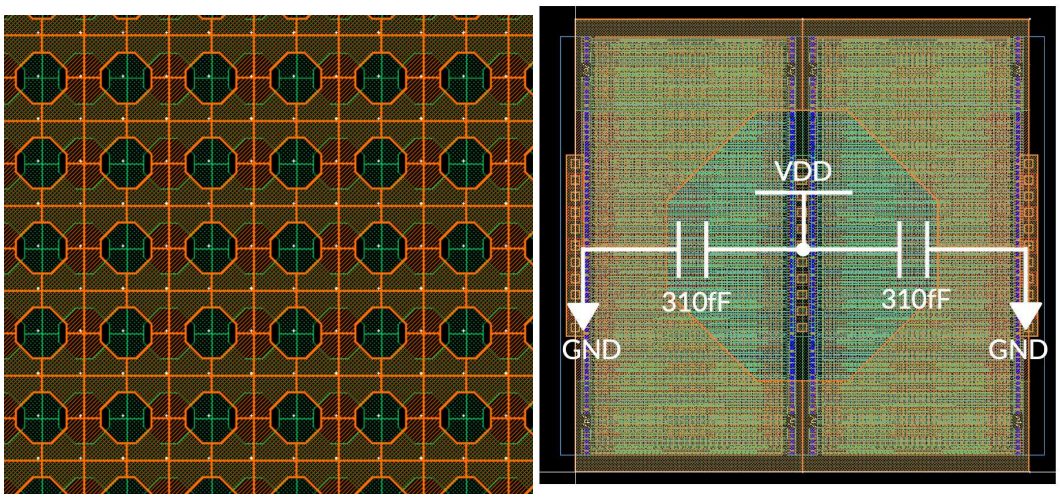
Figure 4.19: Close-up view of the input and gate inductor layout, with the LNTA on the top.



(a) (b)

Figure 4.20: (a) Close-up view of the LNTA layout; (b) visual explanation of the geometrical placement of the constituent elements in the LNTA layout.

highlighted blocks, more than half of the chip is empty, with the output transmission lines running for almost half of the die length. Beyond this, the input inductor L_{IN} in Figure 4.10 was unrolled in a straight line in the layout to gain vertical space, so as to avoid excessively long output lines, which would have otherwise self-resonated close to the chip's bandwidth. The input and



(a) (b)

Figure 4.21: (a) Close-up view of the layout of the ground (orange) and V_{DD} (green) distributed planes; (b) Single GND/VDD plane tile with filtering capacitors embedded within with graphical explanation.

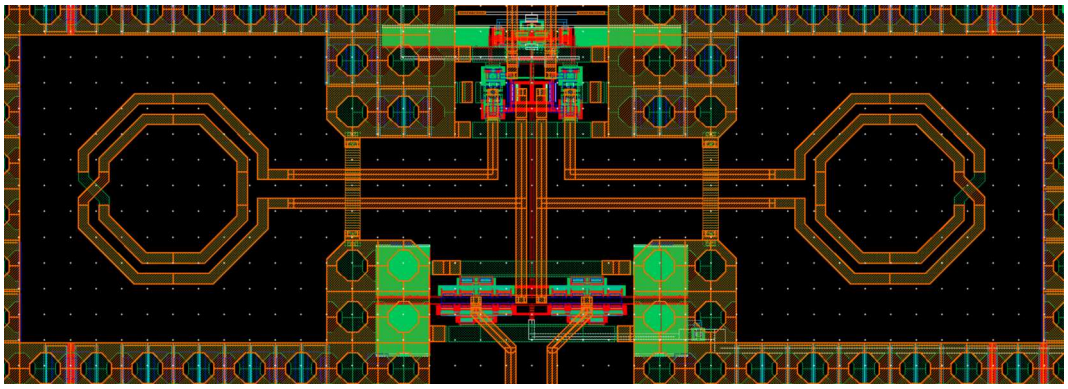


Figure 4.22: Close-up view of the layout of the second VGA, with the gate inductors clearly visible.

gate inductors layout close-up view is reported in Figure 4.19, where it can be seen that a long, straight line (implementing L_{IN}) connects the central, single-ended signal pad to a rolled inductor (implementing L_G) which then connects to the gate of the inverter in the SF LNTA stage. Before L_G, another metal trace departs to bring the signal to the feedback resistance R_F of the SF LNTA. Such connection inevitably will also have a parasitic inductance which ends up in series to R_F. However, the impact of such inductance has been determined to be negligible. Indeed, a feedback inductor is a possible peaking scheme, although a rather weak one due to heavy deQing from R_F, as

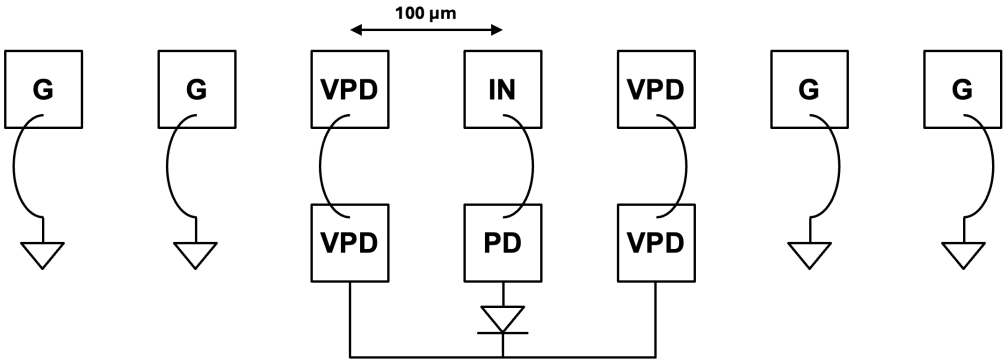


Figure 4.23: Graphical representation of the foreseen way to connect a photodiode to the input of the chip.

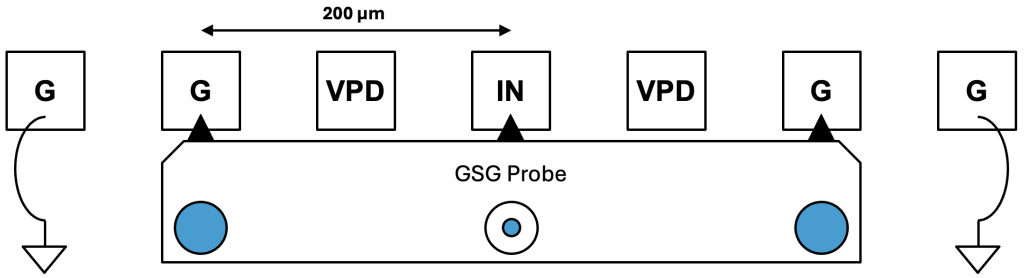


Figure 4.24: Graphical representation of the foreseen way to connect a 200μm-pitch GSG probe to the input of the chip.

previously mentioned in chapter 3.

A close-up view of the LNTA layout is shown in Figure 4.20a. The geometrical placement of the constituent elements in the LNTA was arranged so as to display a common-centroid symmetry, as graphically explained in Figure 4.20b, where the nMOS/pMOS pairs making up the LNTA's inverter have been split in two groups and placed one above the other on the plane y axis, so that the input signal distributes from the center of such structure in a radial way using a grid of lower metals. The feedback resistance is placed on the left side of this structure. This approach was used for all the SF TIAs present in the chain.

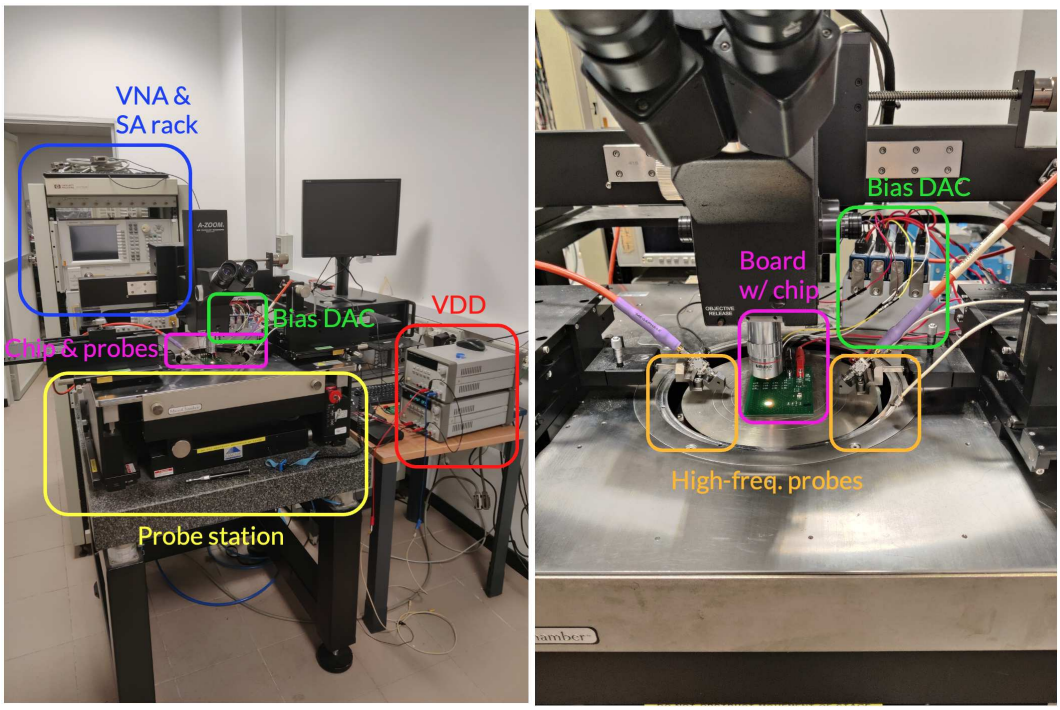
The ground and V_{DD} connections of the LNTA in Figure 4.20a are the large horizontal lines jutting out of the adjacent distributed planes. By bringing the planes as close as possible to the active area devices with large and thick metal lines, parasitic resistance and inductance on the supplies are reduced to

the minimum. Such technique was used for every stage in the signal chain. A section of the planes is shown in Figure 4.21a, where it can be seen that the ground (orange, metal "G2", highest in the stack) and V_{DD} (green, metal "G1", second to highest in the metal stack) planes are identical (also in terms of resistivity, which is the lowest possible in the metal stack of GF12LP+), each made of 10 μm^2 tiles, but with a half-tile offset with respect to each other, so as to create an interlocking scheme that allows access to the upper ground plane from below, using the holes in the V_{DD} plane. Such holes are necessary to not violate the maximum G1/G2 density design rule, but should be as small as possible so as to electromagnetically approximate a continuous plane.

Embedded within the ground/V_{DD} plane tiles are filtering capacitors which short the 1 V supply voltage to ground for all the frequencies of interest, as shown in Figure 4.21b. Every tile has two $\approx$ 310 fF capacitors that contact the V_{DD} tile in the same point and then contact the ground tile by using the two adjacent holes in the V_{DD} plane. Each capacitor is highly-dense MOM capacitance that uses the lower 9 out of the 13 metals in the metal stack of the technology. This scheme was used so that no technology design rule would be violated when placing multiple identical instances of such GND/VDD tiles with embedded filtering capacitors next to each other. In this way, every part of the die where there are no active devices is filled with filtering capacitors that all together implement a $\approx$ 2 nF distributed filtering capacitor between ground and V_{DD}, while also simultaneously satisfying much of the minimum local metal densities design rules.

Figure 4.22 shows the layout of the second VGA in the signal chain in Figure 4.10 (the layout of the first VGA is qualitatively identical, much like their schematics). It can be seen that the layout is split in two distinct parts: a bottom section, which is the cascoded inverter acting as transconductor, and an upper section, which is the inverter-based SF TIA. In between the two symmetrical gate inductors are placed. Their placement is critical, since they cannot be too close to the active area devices to avoid excessive electromagnetic coupling, but cannot be too far away either, since the metal lines between the inductors and the transistors would lower the resonance quality factor.

The chip was designed to allow the possibility for both electrical-only and



(a) (b)

Figure 4.25: Measurement setup used to test the chip with various equipment highlighted: (a) overall view; (b) probe station close-up view.

opto-electrical measurements. To achieve this, the input padset (the bottom pads in Figure 4.18) adopts a hybrid scheme which is different from the standard Ground-Signal-Ground (GSG) used for probe-tested chips (the output padset, the upper pads in Figure 4.18, uses the standard differential GSGSG scheme instead, with two additional ground pads at each corner). The input scheme is Ground-V_{PD}-Signal-V_{PD}-Ground, where V_{PD} refers to the pad where the anode wirebond of the photodiode lands to receive the photodiode 2.5 V voltage supply from the internal routing inside the chip, as explained previously in section 4.4. Figure 4.23 graphically explains the intended way to connect a photodiode to the input of the chip. For electrical-only tests, a GSG probe with 200 μm pitch would need to be used as shown in Figure 4.24.

4.6 Measurements

The implemented chip has been tested for both small-signal and large-signal performances. The chip was wire-bonded to a printed circuit board (PCB)

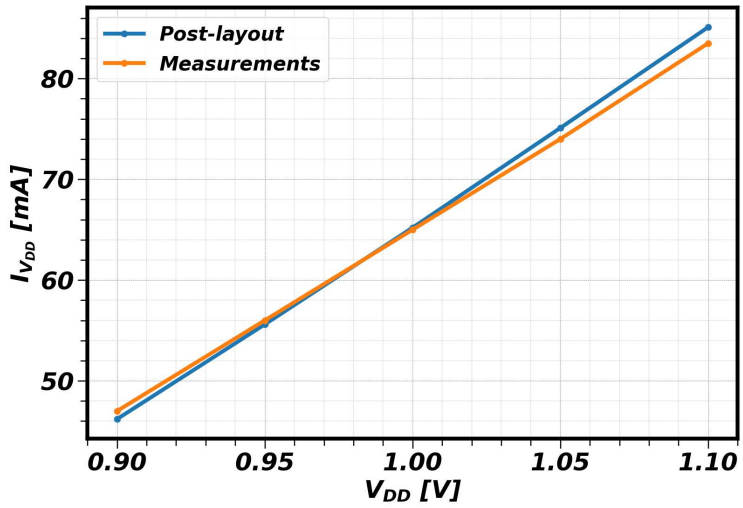


Figure 4.26: Measured current consumption from the 1 V power supply of the chip compared to post-layout simulations when varying the V_{DD} itself.

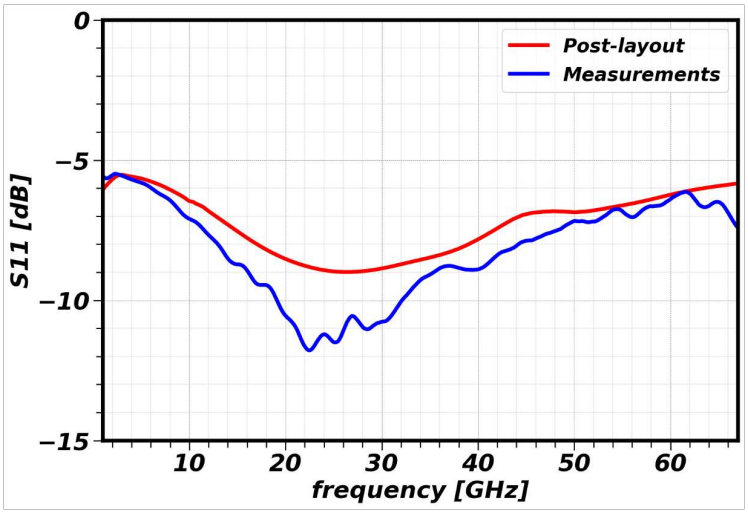


Figure 4.27: Measured S11 of the chip compared to post-layout simulations.

with on-board bias filters and an LDO to supply the 1 V V_{DD}. The wirebond connections only carry low-frequency biases, which are supplied by a voltage unit (only for V_{DD}) and a National Instruments' 9185 DAQ, all of which were controlled via MATLAB either through GPIB or TCP/IP. The high-frequency signal is instead connected with high-performance MPI Titan 67 GHz probes (200-μm-pitch single-ended at the input, 100-μm-pitch differential at the output). 67 GHz RF cables from Megaphase and 65 GHz bias-tees from Marki have been used both at the input and at the output, to simultaneously detect the signal and the DC biasing. An overall view of the measurement setup

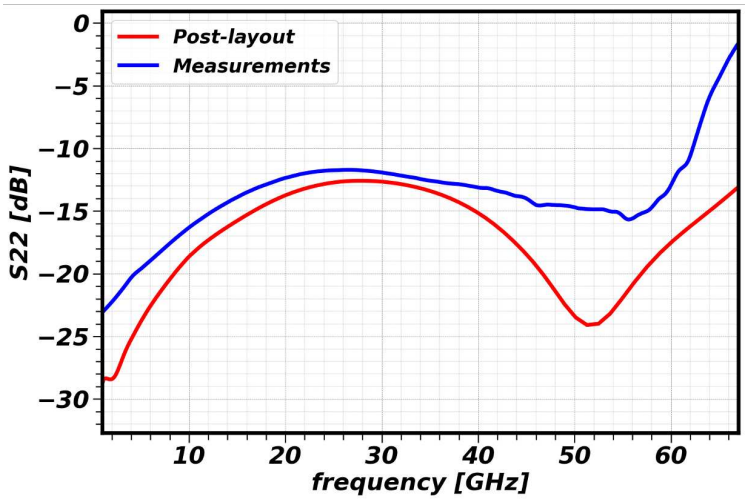


Figure 4.28: Measured S22 of the chip compared to post-layout simulations.

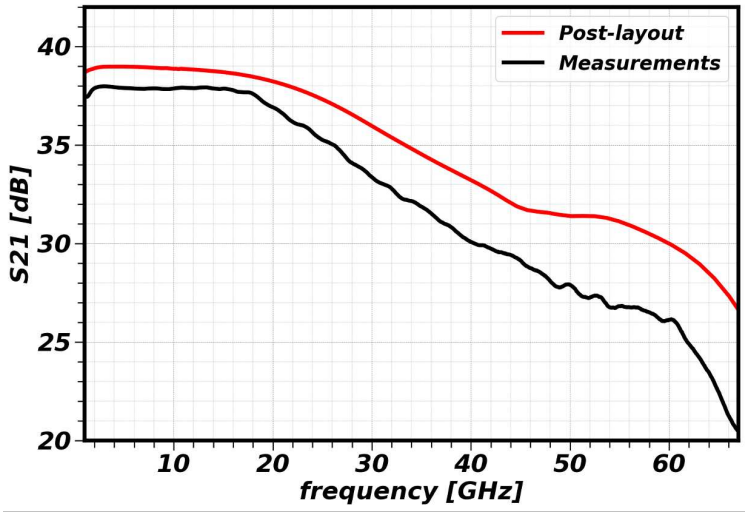


Figure 4.29: Measured S21 of the chip compared to post-layout simulations.

with its components highlighted is reported in Figure 4.25a, while Figure 4.25b shows a close-up view of the PCB with the chip placed on the probe station, with the probes at the sides. The measured DC current absorption of the chip from the 1 V power supply in Figure 4.26 show perfect agreement with post-layout simulations, with 65 mW total power consumption.

S-parameters have been measured with a Agilent E8361C 67 GHz Vector Network Analyzer (VNA). The measured s_{11} is reported in Figure 4.27. There is good agreement between measurements and simulations except in the 20÷30 GHz range, where the measured s_{11} is lower. This is reflected in the z_{11} as an increase in input impedance, as seen in Figure 4.31. Similarly, the measured

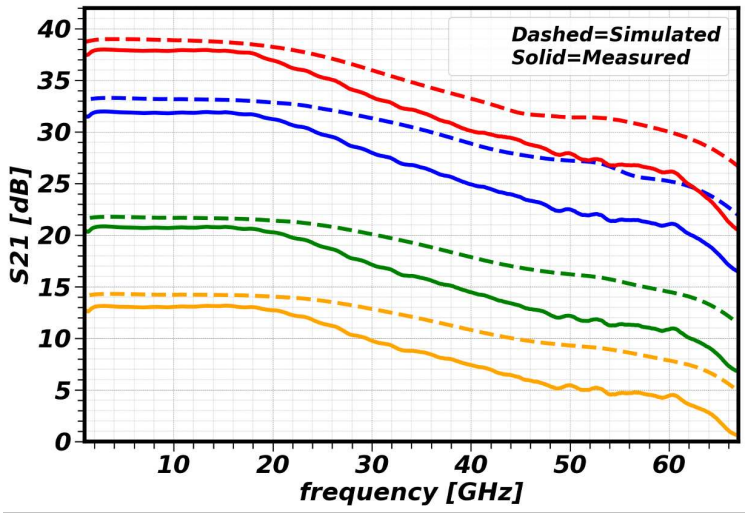


Figure 4.30: Measured S21 of the chip compared to post-layout simulations demonstrating continuous gain variability.

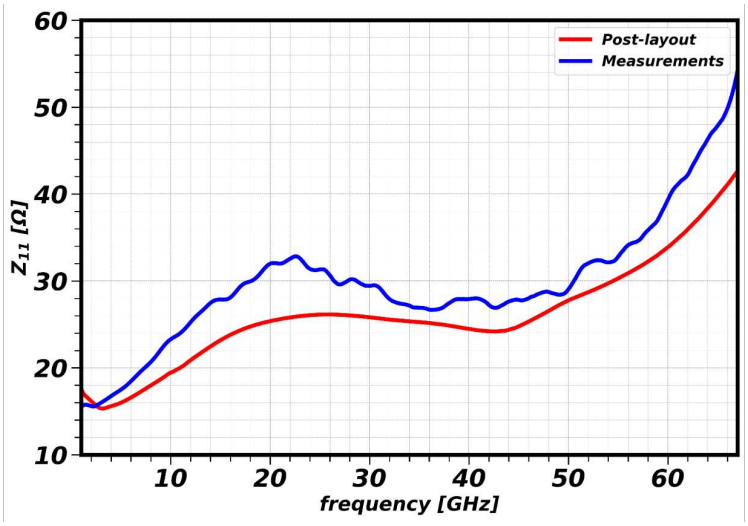


Figure 4.31: Z11 obtained from the measured s-parameters of the chip compared to post-layout simulations.

s_{22}, hence the z_{22} is close to the post-layout simulations results, as shown in Figures 4.28 and 4.32, even if the high-frequency resonance at 52 GHz is much attenuated. Nonetheless, the s_{22} stays below -10 dB up to 62 GHz, which is higher than the signal bandwidth. The s_{12}, albeit not reported, is always much lower than the forward gain.

The s_{21} is reported in Figure 4.29, while Figure 4.30 shows the continuous gain variation capability. While close to post-layout results up to 20 GHz (with constant 1 dB difference), the gap between measurements and simulations

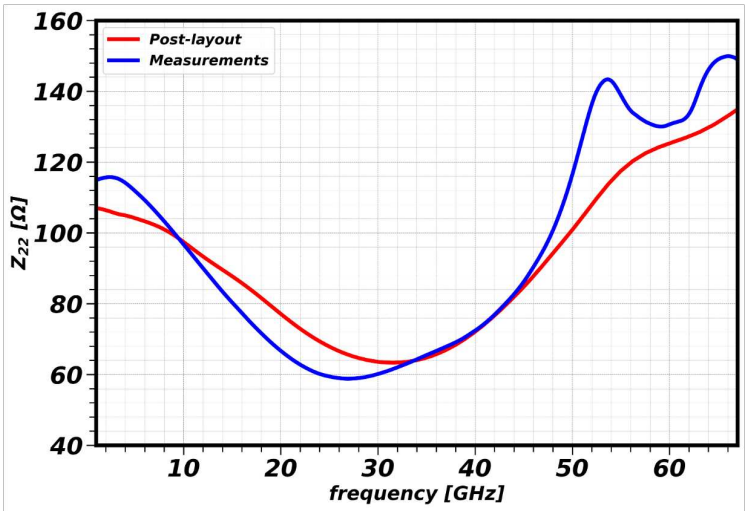


Figure 4.32: Z22 obtained from the measured s-parameters of the chip compared to post-layout simulations.

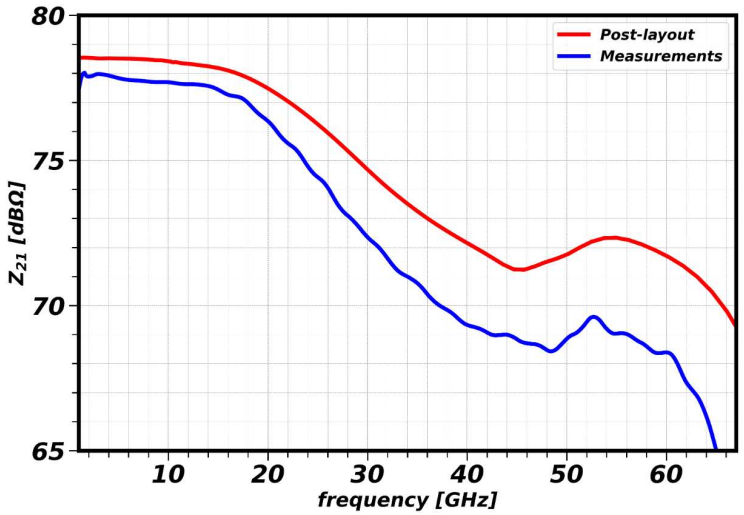


Figure 4.33: Z21 obtained from the measured s-parameters of the chip compared to post-layout simulations.

starts widening after that point, becoming 4÷5 dB between 50 and 60 GHz. The "knee" which is evident is post-layout at 50 GHz, where the curve flattens for ≈10 GHz (associated with the adopted bandwidth extension techniques), is much lower when measurements. Inevitably, the z_{21} shows a similar behavior in Figure 4.33.

When coupled with the photodiode model, the measured s-parameters of the chip yield the transimpedance gain shown in Figure 4.34. As for the s_{21}, the Z_T lacks the high-frequency boost that was expected at the edge of the

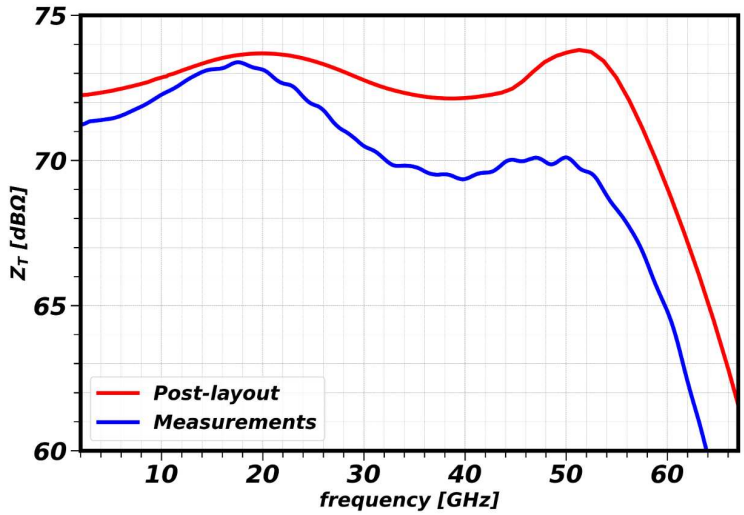


Figure 4.34: Transimpedance gain obtained from the measured s-parameters of the chip with photodiode model compared to post-layout simulations.

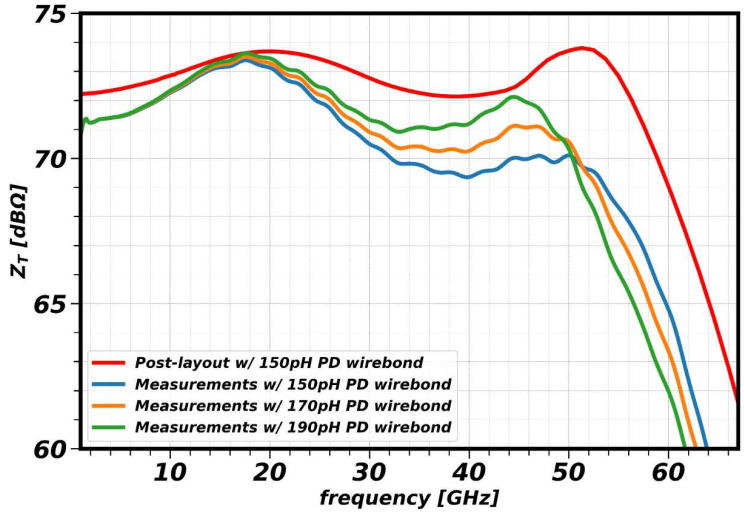


Figure 4.35: Transimpedance gain obtained from the measured s-parameters of the chip with photodiode model varying the wire-bonding inductance value.

bandwidth. The cause of this, despite all efforts, has not been ascertained yet. Since there is good agreement between measurements and simulations for DC power consumption, s_{11}, and s_{22}, it is believed to be linked to a lower than expected quality factor in some of the bandwidth extensions techniques adopted, though it could not be confirmed yet. Nonetheless, the chip reports 71 dBΩ maximum gain tunable down to 46 dBΩ with a 56 GHz bandwidth, compared to the expected post-layout results of 72 dBΩ up to 60 GHz.

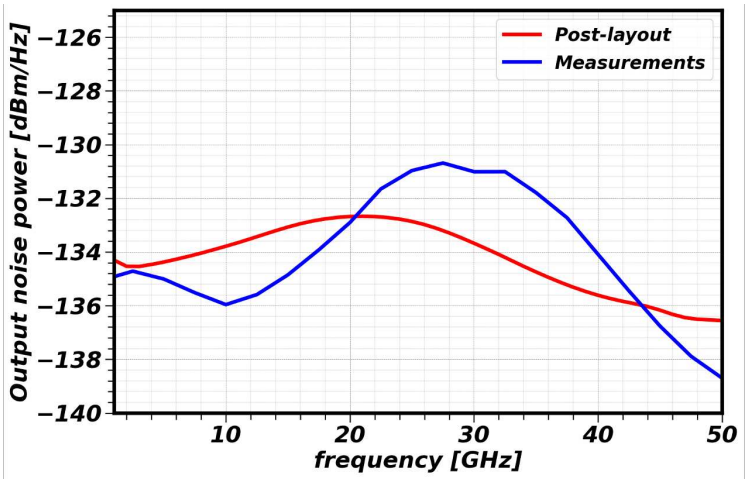


Figure 4.36: Measured output noise power spectrum of the chip compared to post-layout simulations.

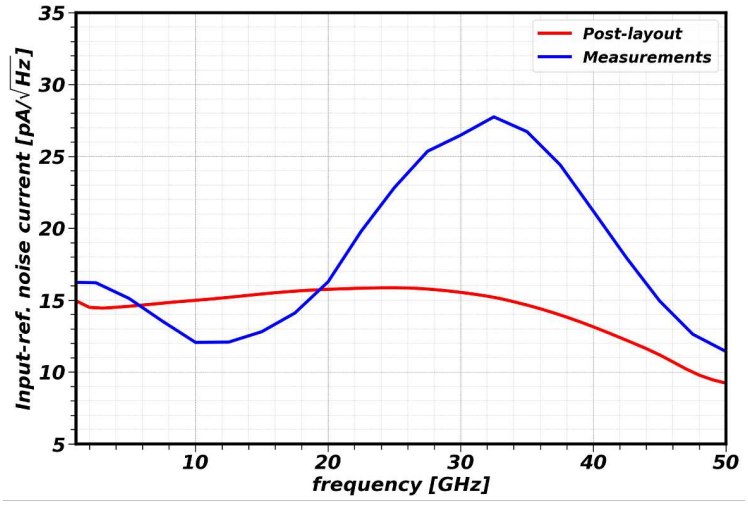


Figure 4.37: Measured IRN current density of the chip compared to post-layout simulations.

Noise performances have been measured with a Agilent PXA N9030 50 GHz spectrum analyzer (SA) with the input of the chip left floating. The measured output noise power spectrum and input-referred noise current density are reported in Figures 4.36 and 4.37, respectively. Inevitably, the same gain loss observed in the s_{21} affects the noise as well, which shows a much more pronounced peak between 20 and 40 GHz. For this reason, when integrated from 1 to 50 GHz, the measured average input-referred noise current density is 18 pA/$\sqrt{Hz}$, against the expected 14.3 pA/$\sqrt{Hz}$ from post-layouts. It should be noted that the bandwidth of the analyzer (50 GHz) is smaller

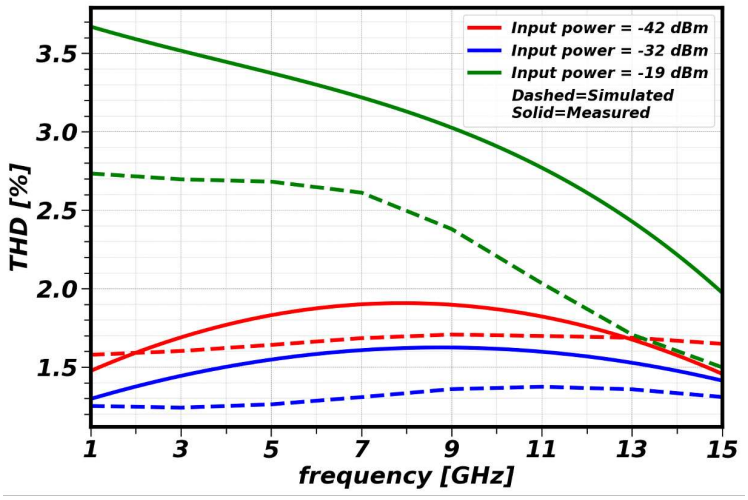


Figure 4.38: Measured THD of the chip vs. fundamental frequency while varying the input power compared to post-layout simulations. The output power is always fixed at -5 dBm while the input power changes with changing chip gain.

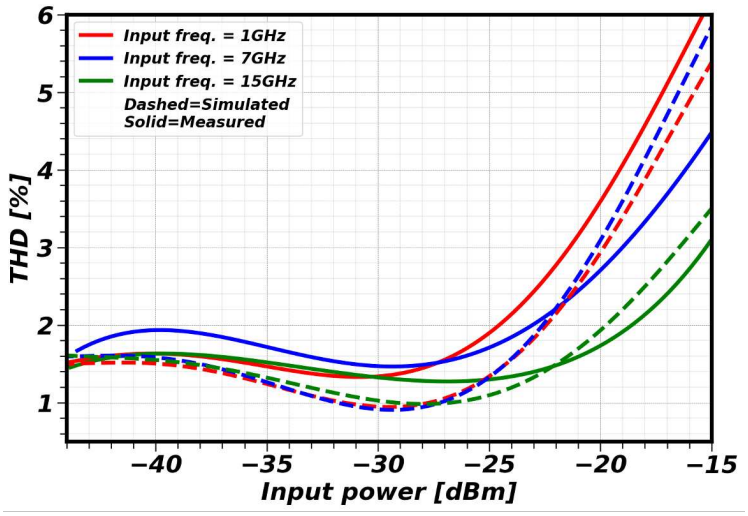


Figure 4.39: Measured THD of the chip vs. input power while varying the fundamental frequency compared to post-layout simulations. The output power is always fixed at -5 dBm while the chip gain changes with changing input power.

that the bandwidth of the chip (56 GHz), and that a local minimum in the noise current is clearly visible at the edge of the instrument frequency range in Figure 4.37, which could likely decrease the average IRN current density. Indeed, when integrated to from 1 to 60 GHz, which is the simulated bandwidth of the chip, the post-layout result is 13.6 pA/$\sqrt{Hz}$ instead of 14.3 pA/$\sqrt{Hz}$ previously mentioned.

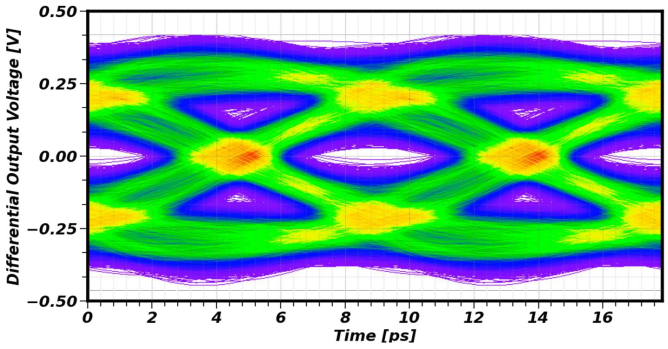


Figure 4.40: 112 Gb/s NRZ PRBS-15 eye diagram from the measured chip s-parameters without equalization.

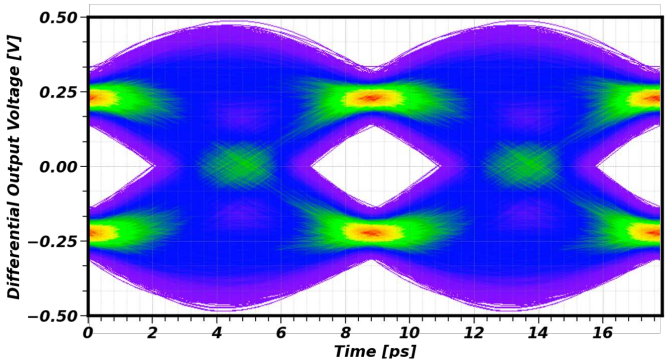


Figure 4.41: 112 Gb/s NRZ PRBS-15 eye diagram from the measured chip s-parameters with 6-tap FFE applied.

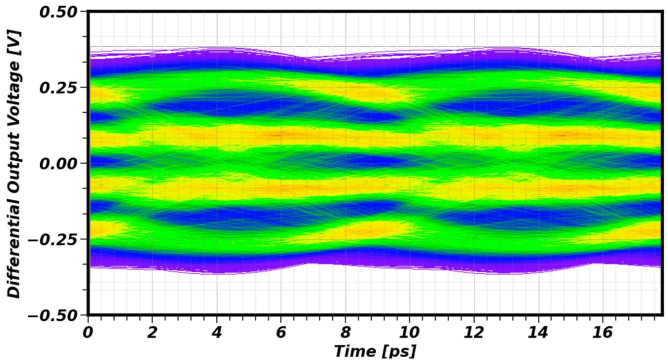


Figure 4.42: 224 Gb/s PAM-4 PRBS-15 eye diagram from the measured chip s-parameters without equalization.

Total Harmonic Distortion (THD) measurements were performed with the same SA as well, using an Agilent E8257D 67 GHz signal generator (SG)

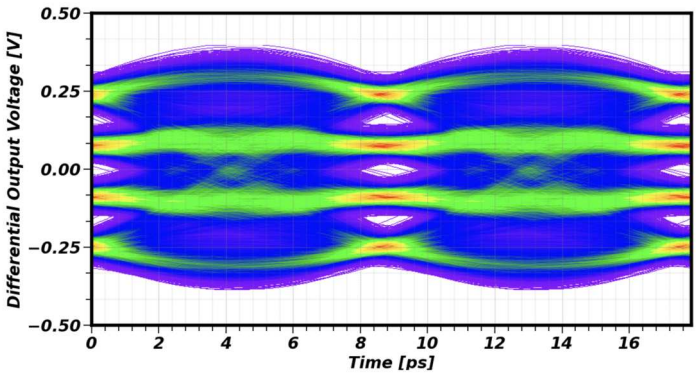


Figure 4.43: 224 Gb/s PAM-4 PRBS-15 eye diagram from the measured chip s-parameters with 6-tap FFE applied.

	This work	JSSC 2019 [28]	SSCL 2024 [29]	JSSC 2023 [30]	VLSI 2024 [31]
Technology	12nm FinFET	16nm FinFET	28nm CMOS	16nm FinFET	12nm FinFET
Modulation	NRZ / PAM-4	PAM-4	PAM-4	PAM-4	PAM-4
Datarate [Gb/s]	112 / 224	106	100	112	90
BW_{-3dB} [GHz]	56	27	32	32	25
Z_T [dBΩ]	46÷71	57÷78	50	56÷63	65
Output Swing [mVpp]	500	600	660	450	120**
THD [%]	<5	1.8	3.4	8	<9
AIRN[1] [$pA/\sqrt{Hz}$]	18	16.7	32.9	16.9	13.4
Active Area [mm^2]	0.054	0.197	0.41	0.016	0.046
Supply [V]	1	1.8	1.1	0.9	0.9/1.2
Power [mW]	65	61	56	77	29
Energy Eff. [pJ/bit]	0.56 / 0.28	0.57	0.56	0.69	0.32

* AIRN=Average Input-Referred Noise Current Density

** Estimated from measured eye diagrams

Table 4.1: Comparison with the State of the Art.

connected at the input of the chip for precise frequency and power control of the fundamental harmonic. Sweeping both frequency and power of the input sinusoid can be displayed with two plots: either the THD is plotted against the fundamental frequency with multiple curves for each power point (Figure 4.38), or the it is plotted against the input power with multiple curves for each frequency point (Figure 4.39). For both cases, the output power is kept fixed at -5 dBm (which translates to the targeted 500 mV peak-to-peak differential output swing), which implies that input power and gain are varied accordingly. As is often the case, the measured distortion is higher than in simulations. In Figure 4.38, measurements are close to simulations for the whole frequency range when the input power is not excessively high. In Figure 4.39, the flat or decreasing trend of the THD for much of the input power range is confirmed in measurements, which behave similarly to post-layout simulations. Overall, the THD is always lower than 5% for the whole gain tuning range.

Eye diagrams for the measured chip have been co-simulated, i.e. obtained from photodiode and chip measured s-parameters. This inevitably cannot take into account neither noise nor distortion, albeit the latter has been observed to be quite low. Figures 4.40 and 4.41 show the 112 Gb/s NRZ PRBS-15 eye diagrams without and with 6-tap Feed-Forward Equalization (FFE), respectively, while Figures 4.42 and 4.43 show the 224 Gb/s PAM-4 PRBS-15 eye diagrams without and with 6-tap Feed-Forward Equalization (FFE), respectively. As it can be seen, the high-frequency gain loss badly affects the eye diagrams when compared to the expected post-layout results in Figures 4.16 and 4.17 for the NRZ and PAM-4 case, respectively. While the NRZ eye without equalization from the measured s-parameters is open with a Signal-to-Noise-Ratio (SNR) of 11.4 dB, the PAM-4 equivalent is completely closed, showing how critical the ripple in the transfer function is for proper performance results. With 6-tap FFE applied, the NRZ eye is wide open and the PAM-4 eye approaches the expected post-layout result. This demonstrates that some sort of equalization for this kind of applications should always be foreseen, be it digital like FFE or analog like CTLE. This however does not invalidate the chip's proof of concept, as the usage of advanced FinFET nodes enables efficient digital equalization with adaptive algorithms that can compensate such undesired effects within a certain limit.

To summarize, Table 4.1 reports the comparison with the state of the art. When considering NRZ modulation, 112 Gb/s with 65 mW power consumption translates to 0.56 pJ/bit energy efficiency, which is one of the best among the reported in the literature for CMOS optical TIAs with S2D conversion. It lowers to 0.28 pJ/bit when considering PAM-4 modulation, which is the lowest in the literature to the best of the author's knowledge.

Chapter 5

Testing of a Mach-Zehnder Driver for Coherent Optical Communication Based on Closed-Loop Topologies

Within the context of the PhD activities, a Mach-Zehnder Modulator (MZM) driver for coherent optical communications was tested. The design, implemented in TSMC 28 nm CMOS technology, had already been taped out before the start of the activities by another PhD candidate. The design key ideas and the measurements results have already been presented in at 2024 IEEE International Conference on Electronic Circuits and Systems (ICECS) in Nancy, France [26]. Here the key results will be reported.

Mach-Zehnder modulators are interferometer-based optical devices which allow for precise optical amplitude modulation based on the change of the device's material refractive index when a voltage signal is applied to it. Optical needs impose a large voltage swing for the driving signal, while complex coherent modulation require very low distortion and high bandwidth. All of these challenging requirements trade off with each other, which is the reason why MZM driver circuit designer face many difficulties, particularly when using CMOS technologies.

CMOS MZM drivers for coherent optical communications are essentially voltage amplifiers that typically need to deliver $1 \div 2$ V peak-to-peak output

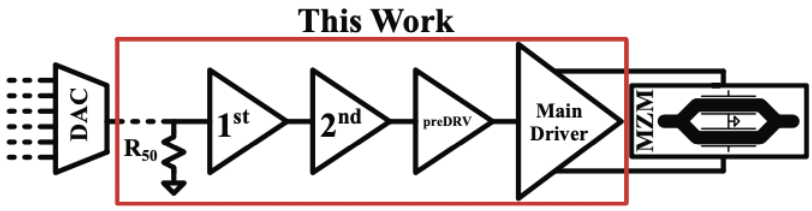


Figure 5.1: Typical open-loop topology of a MZM driver for coherent optical communications (from [12]).

differential swing to a 50 Ω load up to 50+ GHz with a THD below 2%. The standard architecture is made of one or more VGAs, one pre-driver and a final driver stage. The pre-driver needs to ease the capacitive burden of the previous stages while handling the huge input capacitance of the final driver. Figure 5.1 shows an example of such typical open-loop topology. However, an open-loop architecture has a inevitably a strict distortion-output amplitude trade-off: the THD rises sharply with increasing output swing, with an approximately quadratic behavior if the third harmonic of the signal is the dominant source of distortion[20].

An improvement can be obtained if closed-loop topologies are used instead, where the distortion of the output signal is attenuated by a factor proportional to the loop gain [32]. This is the key idea behind the MZM driver that has been tested, that is to achieve large output swings with very low THD by implementing the driver as a linear transconductor, followed by a closed-loop transimpedance amplifier (TIA), similar to a Cherry-Hooper voltage amplifier [21], that directly drives the MZM.

5.1 Architecture

Figure 5.2 shows the architecture of the tested MZM driver for coherent optical communications based on closed-loop topologies. The driver has been designed in 28 nm CMOS technology with pseudo-differential stages with a single 2.4 V supply. The driver is differential, but the block diagram shows the single-ended equivalent for the sake of clarity. A first stage G_{m1}, a variable transconductor, converts the input signal to current with controllable transconductance gain. The input is AC-coupled to a 50Ω transmission line (not shown) which guar-

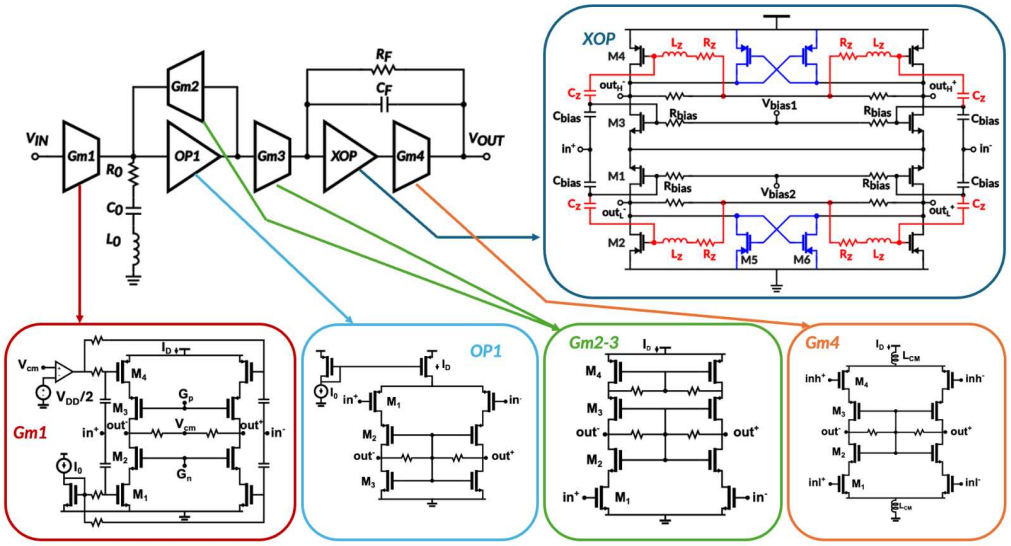


Figure 5.2: Single-ended equivalent of the architecture of the tested MZM driver for coherent optical communications based on closed-loop topologies (from [26]).

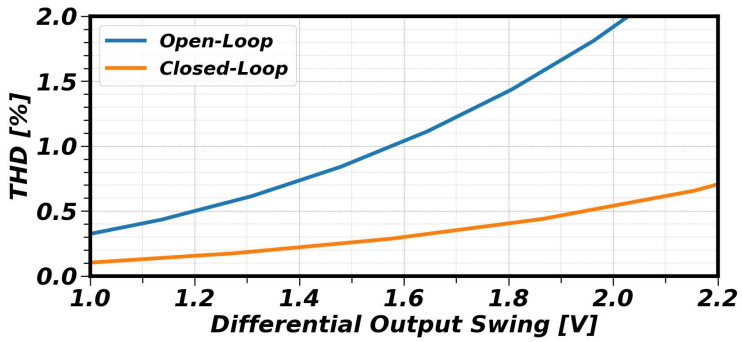


Figure 5.3: Simulated pre-layout THD at 1 GHz vs. differential output swing for the proposed topology at maximum gain when compared to the distortion of G_{m4} used open-loop.

antees wide-band matching. The "triode" gain variation technique already described in section 4.1 has been used here as well in order to continuously reduce the gain without increasing the THD[12].

G_{m3}, G_{m2}, and OP_1 follow, implementing an active current mirror that increases the output current of G_{m1} by the mirror ratio G_{m3}/G_{m2} without affecting the linearity. This is achieved by using an identical topology for G_{m2} and G_{m3}, except for the transistor sizes. The active current mirror is essentially a current-current amplifier with gain G_{m3}/G_{m2}. G_{m2} absorbs all the signal current injected into the loop by G_{m1} as the output of G_{m2} is a

low impedance node thanks to the negative feedback. This ensures that the both the input and the output nodes of G_{m1} see very little voltage swing. The output node of G_{m3} is a low impedance node as well, since XOP, G_{m4}, R_F and C_F implement the output closed-loop TIA. Having the same topology and working in similar conditions, G_{m2} an G_{m3} replicates each other. Hence, the non-linearities in G_{m2} and G_{m3}, to first order, cancel out each other.

A two-stage amplifier is used in the TIA to boost the loop gain, hence ensuring high linearity. The first stage, XOP, is a voltage pre-amplifier that drives a complementary cascoded transconductor, G_{m4}, which provides current to the MZM load. XOP is the only AC-coupled stage of the entire chain. This is because it has to provide two separated differential outputs for the G_{m4} stage, in order to help splitting its big capacitive loading. In order to achieve this, two pseudo-differential amplifiers (M1-2 and M3-4) have been placed in a current-reuse stacked configuration to reduce the current consumption. This implies that each amplifier has a reduced $V_{DD}/2$ voltage headroom. XOP stands for Cross-OPAMP because cross-coupled pairs have been used to create local negative impedance and boost the gain without increasing the supply headroom. G_{m4}, the second stage in the TIA, uses the same topology as G_{m1} but it consumes much more current to provide the required large voltage swing to the low impedance load.

Assuming that the loop gains in the active current mirror and the TIA are large enough, the DC voltage gain of the complete driver can be expressed as:

$$\frac{V_{OUT}}{V_{IN}} \approx G_{m1}\frac{G_{m3}}{G_{m2}}R_F \tag{5.1}$$

Complementary p-n cascode topologies has been chosen both to compensate for the relative transconductance weakness of MOS transistors when compared to bipolar transistors, and to increase the output resistance of the transconductors, thus ensuring that the assumptions behind Equation 5.1 hold.

In an open-loop configuration, G_{m4} would usually dominate the distortion due to the large output voltage swing. In a closed-loop configuration instead, this source of non-linearity is reduced by the loop gain. Fig.5.3 shows the simulated pre-layout THD vs. differential output swing for both the closed-loop topology of the output TIA in Figure 5.2 and G_{m4} when used stand-alone in an open-loop configuration (*Open-Loop* curve). The distortion in the closed-

loop solution is strongly reduced when compared to the amount of distortion that would be generated by an open-loop approach. Equivalently, a larger differential output swing can be obtained for the same THD with a closed-loop approach compared to an open-loop one.

Classic circuit theory and system theory also tell us that, in a closed-loop voltage amplifier, the bandwidth of the system is increased once the phase-margin of the transimpedance loop is reduced, since the quality factor Q_P of the poles in the closed-loop transfer function increases with the low-frequency value of the loop gain [19]. Careful circuit design can therefore reduce the phase margin of a closed-loop system in order to have peaking in the transfer function without the need for inductors in the signal path.

The preceding concepts show that high linearity and large bandwidths are possible with closed-loop topologies, which are hence good candidates for coherent optical communications transmitters' drivers. This comes at the price of ensuring loop stability for extremely large bandwidths, which may require challenging frequency compensation. In the active current-mirror, a series RLC circuit is introduced at the output of $\mathrm{G_{m1}}$. At low frequencies, the capacitance C_0 lowers the dominant pole. A simple resistor R_0 in series with C_0 would create a zero and parasitic pole at $\omega_{p1} = 1/[(R_{out1}//R_0)C_{out1}]$, where C_{out1} and R_{out1} are the output capacitance and resistance of $\mathrm{G_{m1}}$, respectively. The resistor R_0 together with the series inductor L_0 pushes the parasitic pole at $\omega_p = 1/\sqrt{L_0C_0}$, above the loop unitary-gain bandwidth (UGBW), ensuring a good phase margin. This also keeps a low impedance at the output of $\mathrm{G_{m1}}$ for a larger bandwidth. In the closed-loop TIA, to compensate the effect of the input parasitic capacitance of XOP, a Miller compensation capacitance C_F is introduced in parallel to R_F. In the XOP, to further increase the loop bandwidth, a zero implemented with $\mathrm{R_z}$ and $\mathrm{C_z}$ (highlighted in red in Fig. 5.2) doubles the transconductance at higher frequencies by injecting the signal in the gate of M2 as well. Two complex conjugate poles at $\omega_p = 1/\sqrt{L_zC_z}$ introduce peaking in the equivalent transconductance of M1 and M2, further extending the UGBW while keeping sufficient phase-margin.

Since the MZM impedance is connected to a closed-loop structure, the impedance of the modulator affects the loop performance and its stability, which is one additional constraint to be accounted for in the design process.

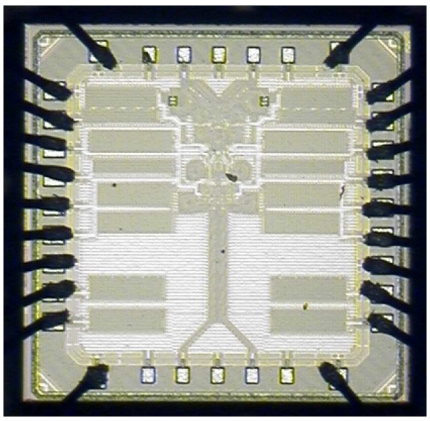


Figure 5.4: Microphotograph of the fabricated 1 mm^2 MZM driver chip.

To ensure optimal performance for different values of the load impedance, a variable feedback resistance would be required, which was not implemented in this prototype.

The overall driver was designed to provide a 1.5 V_{ppd} output swing to a 50Ω MZM (100Ω differential load) with 20 dB gain, continuously tunable down to 10 dB by varying the small-signal transconductance of G_{m1}. Introducing gain variability in the first stage ensures that the rest of the circuit sees a constant signal swing, independent from the input signal level, which helps keeping good linearity at low gain levels (i.e. large input signal). The simulated electrical bandwidth is 34 GHz while the simulated THD at 12 dB gain and 1.5 V_{ppd} for a 1 GHz fundamental is 0.44%. The overall simulated post-layout current absorption from V_{DD} is 83 mA, for a total DC power consumption of 200 mW.

5.2 Measurement Results

The chip has been fabricated in 28 nm CMOS technology. Fig. 5.4 shows the microphotograph of the 1mm^2 die. The measured driver consumes 85.2 mA from the single 2.4 V supply, for a total power consumption of 204 mW.

S-parameters measurements were performed with a 2-port 67 GHz VNA, 65 GHz baluns both at the input and at the output for single-ended-to-differential conversion, and two 65 GHz DC-blocks at the output for AC-coupling. Fig. 5.7 shows the comparison between simulated and measured s_{11} and s_{21} of the fabricated chip. s_{21} is reported for different gain settings as well. The mea-

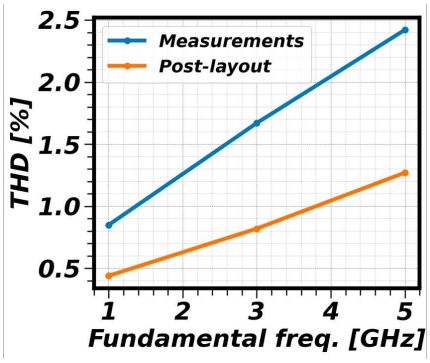


Figure 5.5: Simulated and measured THD of the driver vs. input fundamental frequency at min. gain and 1.5 Vpp differential output swing.

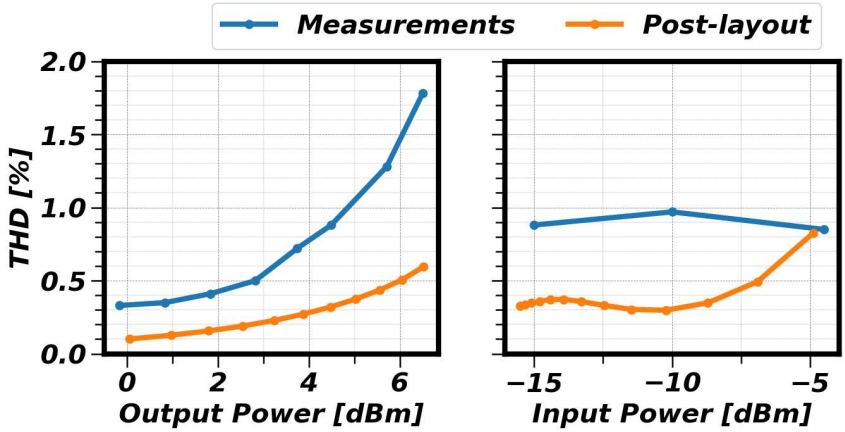


Figure 5.6: Comparison between simulated and measured THD at 1 GHz against output power sweep at max. gain (left) and input power sweep at 1.5 V_{ppd} (4.5 dBm) output swing (right).

surements show qualitative agreement with the post-layout simulations. s_{11} ensures good input matching up to 40 GHz. At maximum gain the electrical bandwidth is 33 GHz. The 4-levels Pulse-Amplitude-Modulation (PAM-4) eye diagram at 112 Gb/s has been derived from the measured S-parameters of the chip with a PRBS-22, as it can be seen in Fig. 5.8. The eye diagram shows good aperture and transient response without the need for any equalization.

THD measurements have been performed with a 67 GHz signal generator and a 50 GHz spectrum analyzer. Fig. 5.5 reports the comparison between simulated and measured THD of the driver. As it can be seen, distortion is extremely low at 1 GHz, 0.85%. It should be noted that the reported THD in this plot is at minimum gain setting, where the input swing is the highest. The discrepancy between simulation and measurement can be explained with a

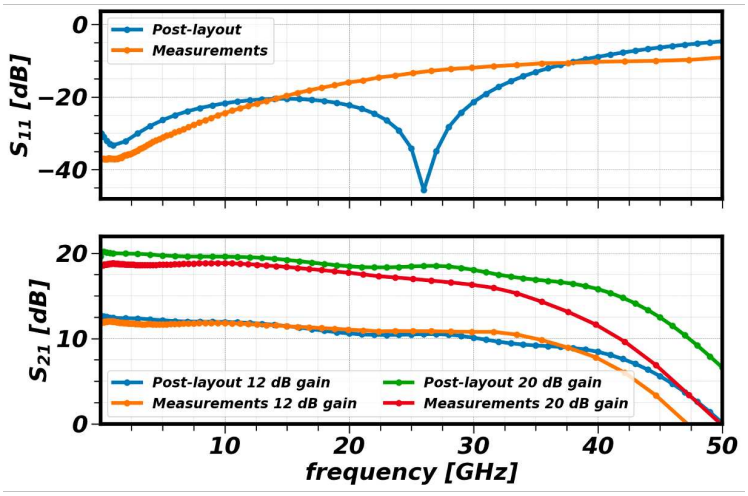


Figure 5.7: Comparison between simulated and measured S_{11} and S_{21} of the driver, also for different gain settings.

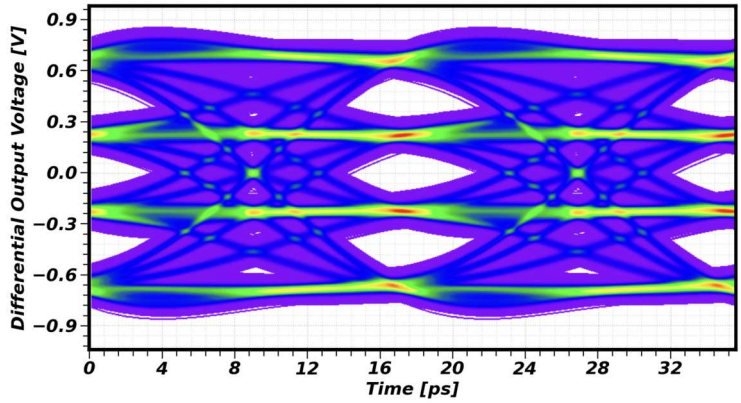


Figure 5.8: 112 Gb/s PAM-4 PRBS-22 eye diagram without any equalization derived from the measured chip S-parameters.

slightly lower DC gain in measurements (≈18.5 dB) due to parasitic IR drops, that is compensated by a larger input signal level, leading to higher distortion in the input transconductor. Fig. 5.6 shows the measured and the simulated THD both for different output (left) and input (right) power levels. The THD is lower than 2 % even at ≈6.5 dBm output power (≈2 V_{ppd}), while also being relatively flat for different gain settings, thanks to the gain variation technique in G_{m1}.

Table 5.1 shows the comparison with the State of the Art of MZM CMOS drivers. The proposed driver has the lowest THD at 1 GHz both for 1.5 V_{ppd} and 2 V_{ppd} output swing while also having one of the lowest DC power con-

	This work	ESSCIRC 2022 [12]	ISSCC 2020 [33]	ECOC 2017 [34]
Technology	28nm CMOS	28nm CMOS	65nm CMOS	65nm CMOS
Elec. BW [GHz]	33	58	48	56
DC Gain [dB]	10÷20	10÷20	13÷22	13÷20
Differential Output Swing [Vpp]	1.5 / 2	1.5	1.5	2
THD@1GHz [%]	0.8 / 1.8	1.8	2.2	3.8
Supply [V]	2.4	2.4	2.6	2.5
Power [mW]	204	297	225	180

Table 5.1: Comparison with the State of the Art of CMOS MZM Drivers.

sumption, which demonstrates the validity of the novel topological approach.

Chapter 6

Preliminary studies for a 112 Gb/s NRZ oRX AFE with graphene-based photodetector

Within the context of the PhD activities, a 112 Gb/s NRZ opto-receiver (oRX) analog front-end (AFE) designed to work with graphene-based photodetectors was also evaluated. The design was carried out only within the preliminary design phase, and it is actively being finalized by another PhD candidate at the time of writing. Here, only the preliminary results will be reported. The project goal was to study the feasibility of implementing a high-performance receiver coupled with a graphene-based photodetector (gPD). The design and fabrication of the gPD, realized by the project partner company CamGraPhIC Italy S.r.L, was not part of the present study.

Multiple studies have demonstrated the promising properties of graphene as a material with high photoconductivity for terahertz optical communications [35][36][37][38]. The gPD considered for this project was the result of CamGraPhIC's R&D efforts, which have been successfully published in the literature [39][40][41], and it leverages the photothermoelectric (PTE) effect (hence, they are part of the PTE-based photodetectors family). PTE-based PDs produce an output voltage which is proportional to the power of the incident light:

$$V_{PH} = S\Delta T \tag{6.1}$$

where S is the material Seebeck coefficient of graphene and $\Delta T = \overline{T}_{HC} - T_0$

is the difference between of the hot carrier's (HC) temperature averaged over the device graphene channel ($\overline{T}_{HC}$), which is proportional to the absorbed optical power, and the graphene lattice temperature (T_0)[41]. The incident light on the gPD creates a temperature gradient in the structure due to the photothermal effect which is then converted into an electrical voltage through the thermoelectrical (Seebeck) effect.

From an electrical point of view, gPDs behave differently from photodiodes: they can be modeled as voltage sources with a series real source impedance whose value can be engineered to be 50 Ω or even lower. This different scenario dramatically alters the requirements on the oRX AFE, as the input becomes a low-impedance voltage source instead of a high-impedance (capacitive) current source. Hence, the oRX AFE is not a Transimpedance Amplifier (TIA) anymore, rather a voltage amplifier, and its first stage is not a Low-Noise TIA (LNTA) but a Low-Noise Amplifier (LNA). Since photodetectors are supposed to be placed as close as possible to the oRX, no input impedance matching requirement is imposed on the LNA, which means that noise matching can be fully exploited to minimize the receiver noise figure (NF) [18].

The considered gPD must not have a voltage drop across its terminals to properly function [41]. Hence, AC coupling at the input of the oRX AFE must be foreseen and its impact on the performances must be carefully evaluated.

To reduce power consumption and increase future integrability with the gPD, which is fabricated in a Silicon-On-Insulator (SOI) process, the adopted technology was the 22 nm FDX Fully-Depleted-Silicon-On-Insulator (FDSOI) by GlobalFoundries, which has already been characterized in section 2.2. Such technology offers millimeter-wave (MMW) device models which showed to be highly accurate when confronted with post-layout simulations. Hence, only MMW device models were used in the preliminary study here reported.

As observed in section 2.2, the 22 nm FDSOI technology shows a considerable performance gap between nMOS and pMOS which cannot be neglected in the design phase. For this reason, the choice of the first stage topology rapidly converged on a pseudo-differential n-only common-source amplifier with AC coupling at the input and triple resonance peaking (TRP) to extend the bandwidth, a well known peaking scheme [20]. Figure 6.1 reports the considered schematic with the gPD small signal model, PAD & ESD parasitic capaci-

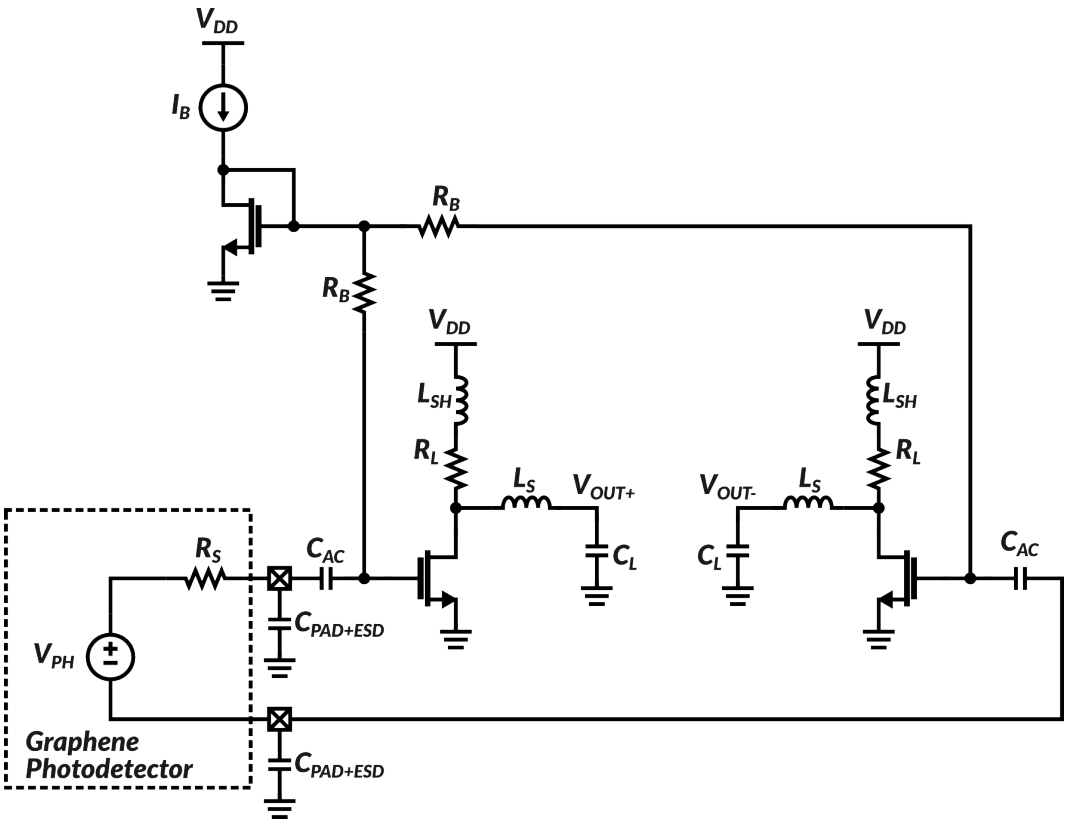


Figure 6.1: Evaluated topology of the LNA acting as first stage in the oRX AFE with graphene-based photodetector.

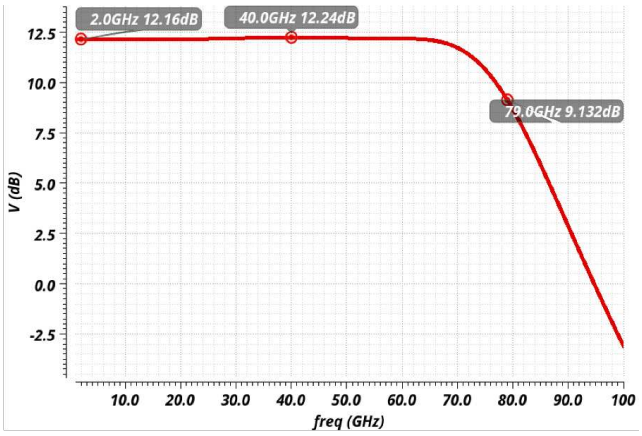


Figure 6.2: Transfer function magnitude frequency behavior of the circuit in Figure 6.1.

tances, input AC coupling (C_{AC}), low-frequency biasing (R_B and the diode connected nMOS) and TRP (L_S and L_{SH}). The source impedance of the gPD was assumed to be 50 Ω. The nMOS are sized $\approx 7.48\mu m/20nm$ and $R_L = 81\Omega$, $L_S = 270pH$, and $L_{SH} = 70pH$. The circuit is biased with a 1.8 V voltage

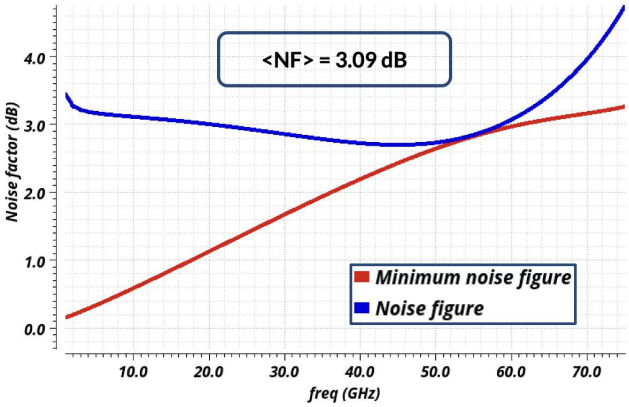


Figure 6.3: Noise figure frequency behavior of the circuit in Figure 6.1 (blue), next to the minimum noise figure for such topology (red). The average noise figure is 3.09 dB.

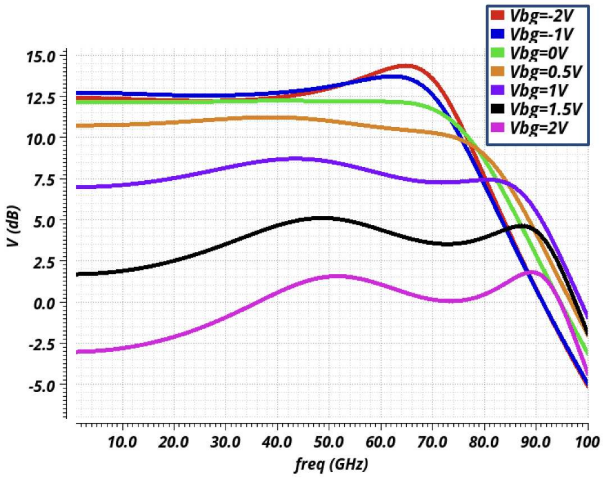


Figure 6.4: Transfer function magnitude frequency behavior of the circuit in Figure 6.1 varying the gate by sweeping the back-gate voltage of the nMOS FDSOI transistors.

supply, a 720 μA bias current I_B, and has a total power consumption of 56.1 mW. THe input AC coupling cut-off frequency was set to be 1.9 MHz.

The resulting transfer function magnitude for the circuit in Figure 6.1 is shown in Figure 6.2, displaying a very flat behavior with 12 dB DC gain over a 79 GHz bandwidth. Such large bandwidth does not compromise the noise performances of the LNA, whose Noise Figure (NF) frequency behavior is reported in Figure 6.3 (blue curve). The LNA minimum NF is also plotted (red curve), showing that in the 50÷60 GHz range, the NF of the circuit almost coincides with the minimum achievable.

FDSOI technologies offer precise control of the threshold voltage of the

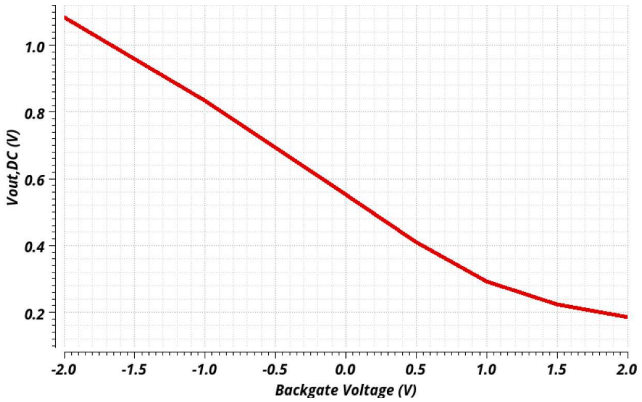


Figure 6.5: DC output voltage of the circuit in Figure 6.1 varying the gate by sweeping the back-gate voltage of the nMOS FDSOI transistors.

devices through the back-gate terminal, which biases the body voltage[42]. By sweeping the back-gate voltage V_{BG}, the gain of the stage can be varied over a wide range, as reported in Figure 6.4, which shows that this topology in FDSOI technologies could also be used for VGAs. However, varying the threshold voltage of the nMOS transistors entails varying their drain currents, which inevitably alters the output DC bias voltage of the stage, as shown in Figure 6.5. If such gain variation technique is used, AC coupling between this stage and the next must then be foreseen.

Conclusions and Future Works

In this thesis, a broadband, 224 Gb/s PAM-4 low-noise transimpedance amplifier for low-power optical communications receivers has been analyzed, designed and tested in 12 nm FinFET technology. A Mach-Zehnder Modulator driver in 28 nm CMOS technology for coherent optical applications has also been experimentally tested. A preliminary study of the first stage of an optoreceiver analog front-end for graphene-based photodetectors in 22 nm FDSOI technology has been carried out as well, and the design of such receiver is currently being finalized by another PhD candidate. All of these activities testify the level of maturity reached by CMOS technologies within the field of optical communications, once reserved to BiCMOS technologies.

The 224 Gb/s PAM-4 TIA in 12 nm FinFET has shown good performances, reaching 56 GHz bandwidth with 71 dBΩ of DC transimpedance gain, 18 pA/$\sqrt{Hz}$ of average input-referred noise current density, and a THD always below 5%. Unfortunately, measurements also showed a discrepancy with the post-layout simulations, as the high-frequency signal boost was much weaker than expected, leading to increased ripple in the transfer function, hence PAM-4 eye corruption. The cause for such performance gap will need to be addressed in the future.

The PAM-4 eye diagram has been recovered by applying digital equalization. As FinFET technologies enable efficient equalization schemes within the receiver, future research should strive to implement schemes like Feed-Forward Equalization and/or Decision-Feedback Equalization after the analog front-end implemented here, possibly with some adaptive algorithm to ensure smooth performance under any circumstances.

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