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Analysis and development of novel supply and driving features for high efficiency power switches

Ph.D. Student: Claudio Villani

University Supervisor: Prof. Piero Malcovati

Company Supervisor: PhD Ing. Stefano Ruzza

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Abstract

This dissertation consists of two main topics that address the challenges and opportunities in the field of power electronics.

Firstly, the development and characterization of low gate energy power switches is presented, focusing on power MOSFETs and IGBTs, designed to address the challenges of modern power electronics. The study highlights the integration of a 68 nF silicon capacitor (SilCap) into a compact QFN package co-packaging low gate energy power MOSFETs and gate driver, enabling efficient bootstrap circuit operation and reducing passive component sizes. Experimental results demonstrate the module's ability to handle rated currents up to 2 A across various PWM frequencies, including transient overload conditions up to 1.5 times the nominal current. The analysis has been also extended to a novel low gate energy IGBT with a gate voltage of 1.5 V, allowing significant reduction of conduction and switching losses compared to conventional IGBTs. Challenges such as parasitic turn-on events are mitigated through advanced gate driver architectures, including Miller clamps and custom voltage regulation. The findings underscore the potential of these technologies for future power electronic systems, with recommendations for further improvements and applications.

The second part introduces a novel methodology for driving Silicon Carbide (SiC) power switches using a current source gate driver, exploring two distinct driving strategies: single-level and multi-level current source driving. The single-level approach simplifies implementation and enables open-loop control of voltage slew rate, independent of load current, leading to a significant reduction of switching losses. Conversely, the multi-level strategy, though more complex, allows nanosecond-scale gate current variation during switching events, minimizing both switching losses and electromagnetic interference (EMI). This approach also defines a novel transfer function between switching losses and EMI, a critical trade-off for power electronic designers. Focusing primarily on the turn-on transition, the study presents a detailed analysis of obtained experimental results, highlighting the benefits and challenges of the proposed driving strategies. The findings underscore the importance of advanced driving techniques in maximizing the efficiency and reliability of SiC power switches, particularly in high-power density and high-efficiency applications such as electric vehicles. This research contributes to the ongoing development of optimized control methods for SiC-based systems, addressing the growing demand for high-performance

power electronics

The findings of this research have the potential to make life easier, safer, and greener by enabling the development of more efficient and reliable power electronic systems. By advancing the state-of-the-art in power electronics, this dissertation contributes to the creation of innovative solutions for a wide range of applications, including renewable energy systems, electric vehicles, and industrial power supplies.

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Chapter 1

Introduction

Power electronic converters are the backbone of modern energy systems, playing a crucial role in renewable energy integration, electric transportation and high-efficiency industrial drives. As the demand for higher power density and efficiency grows [1], the performance of switching devices and their gate-driving strategies becomes increasingly important. This thesis addresses these challenges by exploring device-level advancements and gate-driving techniques, with a focus on the reduction of the switching losses, management of electromagnetic interference (EMI), and controllability improvement of critical switching dynamics.

1.1 Background and motivation

Silicon carbide (SiC) power devices have enabled substantial gains in efficiency and switching speed. However, their fast transitions exacerbate EMI and place stringent demands on gate drivers and layout parasitics. Conventional resistive gate driving (Rg) provides simplicity but offers limited dynamic control of current and voltage slew rates and can leave performance exposed to device and operating condition variations. In contrast, current-source gate driving and waveform shaping of the gate current open the door to precise control of di/dt and dv/dt, enabling an optimized trade-off between switching losses and EMI. Within this context, the thesis emphasizes the turn-on transition, which is often the dominant contributor to both switching losses and radiated/conducted interference, warranting focused analysis and optimization.

This research not only explores advancements in gate-driving methodology but also delves into device-level innovations, including superjunction (SJ) Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) and low gate energy Insulated Gate Bipolar Transistors (IGBT) with novel gate cell designs. Power MOSFETs are gaining popularity in low-power, low-cost applications, replacing IGBTs due to their ability to optimize efficiency at light loads. SJ MOSFETs, in particular, offer significant advantages over traditional power MOSFETs, in-

cluding reduced parasitic capacitance and gate charge. The decrease in gate charge has a substantial impact on reducing driving losses, enabling the miniaturization of both the gate driver and the external passive components required for the gate driver circuitry.

The need for further improvements in IGBT technology has become increasingly urgent due to the competition from Wide Band Gap technologies and the ongoing demand for high efficiency and power density. In response, the low gate energy IGBT has been developed, featuring innovative gate cell designs that promise to significantly reduce conduction and switching losses. However, the low gate-energy IGBT also presents some challenges, including its susceptibility to parasitic turn-on. Solutions to address this issue are discussed, highlighting the importance of careful design and optimization.

These emerging technologies are of particular interest due to their potential for integration, and their impact on system partitioning is a key area of focus. By exploring the benefits and challenges of these device-level innovations, this research aims to provide a comprehensive understanding of their potential to improve efficiency, reduce losses, and enhance overall system performance.

By combining these system-level and device-level approaches, the goal is to achieve significant improvements in efficiency and EMI mitigation, all while maintaining robustness and reliability.

1.2 Research objectives

The primary objectives of this research are to:

- Demonstrate that SJ MOSFETs can influence the current system partitioning by enabling the integration of discrete components belonging to the supply network, thereby potentially simplifying the system design.
- Develop and validate a novel gate driver architecture that is capable of meeting the unique gate requirements of low gate energy IGBTs, ensuring their efficient and reliable operation.
- Investigate and confirm the effectiveness of the current source gate driving technique in minimizing switching losses in SiC MOSFETs, which is crucial for improving the overall efficiency of power electronic systems.
- Verify that the current source gate driving technique can enhance the controllability of the drain current and drain-source voltage slew rates (di/dt and dv/dt), allowing for more precise control over the switching behavior of power devices.
- Demonstrate that the current source gate driving technique, through active gate shaping, can optimize the trade-off between EMI and switching losses, enabling the design of power electronic systems that balance these competing requirements.

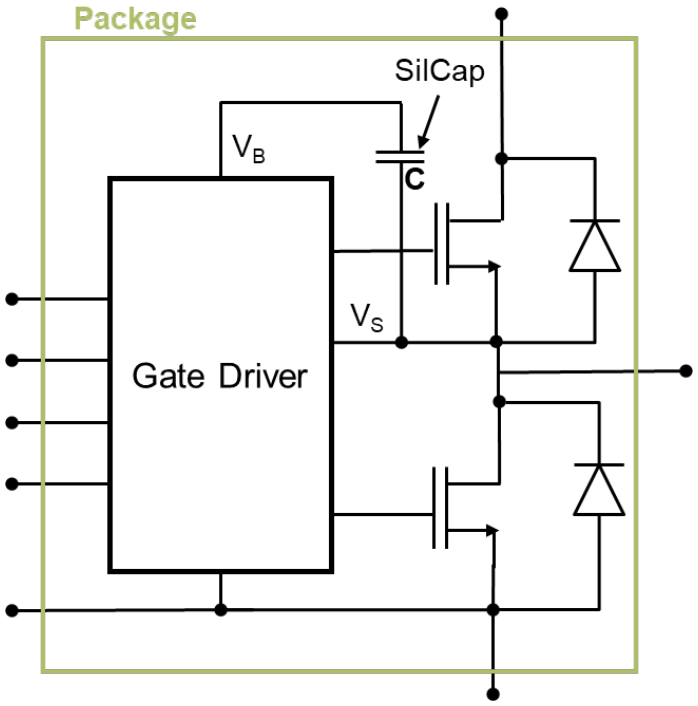


Figure 1.1: Simplified module structure

1.3 Approach and scope

The thesis is divided into two main parts. The first part presents and evaluates a single-supply high-voltage module that integrates two SJ MOSFETs, a gate driver, and an on-silicon capacitor serving as a bootstrap supply as shown in Figure 1.1. The primary objective of this analysis is to demonstrate that the on-silicon capacitance can supply the device with the same performance and reliability as multi-layer ceramic capacitance (MLCC) typically used as bootstrap supply capacitors.

A design methodology is provided for sizing under-voltage lockout (UVLO) capacitors across various operating points, ensuring reliable operation in practical converters. The feasibility of this approach is evaluated through:

- Bootstrap circuit design and characterization
- Application-oriented tests under both negative and positive load currents

The subsequent part of the work focuses on the characteristics of low gate energy IGBTs and the development of a new gate driver architecture. The objective of this activity is to enable the adoption of this new IGBT technology

and to expand the concept of integrated on-silicon capacitance to include this technology, thereby exploring its potential benefits and applications.

The gate driver and two low gate energy IGBTs are integrated into the same package platform used for the single-supply high-voltage module, leveraging the close proximity guaranteed by this platform. The effectiveness of the proposed gate driver is assessed through:

- Standalone gate driver characterization
- Module-level characterization

The second part of the thesis develops and validates a current-source gate-driving methodology specifically designed for SiC devices, incorporating both single-level and multi-level gate current profiles. A dedicated "gate shaping demonstrator" is utilized to generate programmable gate current patterns and empirically study their impact on switching trajectories, EMI, and loss. The driver hardware features practical current mirror source and sink stages, which form the core of the design, allowing for the realization of defined gate current waveforms during turn-on and turn-off.

The methodology is evaluated across various aspects, including:

- Single-level current-source driving, with a focus on sensitivity to reverse-recovery charge and parasitic elements in the commutation loop
- Extensions to IGBT devices, illustrating the generality and boundary conditions of the approach
- Multi-level gate current profiles, including algorithmic gate-current pattern optimization and experimental validation
- An EMI analysis toolchain, which links gate-current profiles, device dynamics, and spectral content, supporting design trade-offs and optimization.

1.4 Significance and impact

The incorporation of an on-silicon capacitance as a bootstrap capacitance offers module designers a new degree of design flexibility, as it eliminates the need for dedicated supply pins in the module outline. This innovation enables the development of more compact and efficient power modules.

Furthermore, the insights gained from laboratory demonstrations can be readily translated into application-ready driver modules and sizing rules, such UVLO capacitor sizing, thereby accelerating the transition from concept to deployment.

The gate driver architecture developed for low gate energy IGBTs serves as a valuable example of how standard gate driver architectures can be modified to accommodate low gate energy devices. This design may potentially become

a reference for gate driver architectures for low gate energy switches in general, providing a useful guideline for designers working with these devices.

The current-source gate-driving strategy provides a means to simultaneously reduce switching losses and manage EMI, two metrics that are often in conflict in fast-switching SiC-based power converters. The results of this research provide designers with practical methods to:

- Actively control switching waveforms by shaping the gate current, allowing for more precise control over the switching process.
- Balance EMI compliance and efficiency targets without relying solely on passive filtering or excessively slowing down the switching process.
- Account for parasitic effects and reverse-recovery phenomena during the design stage, thereby improving the predictability and robustness of the system.

By providing these actionable methods, this research enables designers to create more efficient, reliable, and EMI-compliant power converters, which is essential for a wide range of applications.

1.5 Thesis organization

The thesis is structured as follows:

- Chapter 2 introduces the concept of low gate energy power switches and delves into the development and characterization of a single-supply high-voltage module. The latter part of the chapter focuses on the design and development of a new gate driver architecture tailored to meet the requirements of low gate energy IGBTs. The gate driver is thoroughly characterized and then integrated with two low gate energy IGBTs in a package, with the module's characterization results presented.
- Chapter 3 explores the gate shaping methodology and demonstrator, commencing with single-level current-source driving and its sensitivity to reverse-recovery charge and parasitics, as well as extensions to IGBTs. The chapter then progresses to discuss multi-level gate current profiles, gate-current pattern optimization, experimental validations, and the EMI analysis tool. Particular emphasis is placed on controlling the rates of change of current (di/dt) and voltage (dv/dt), as well as the turn-on transition, which is identified as the primary contributor to losses and EMI.
- Chapter 4 provides a comprehensive synthesis of the findings, highlighting the synergistic role of current-source gate driving and low gate-energy device design in minimizing losses and enhancing EMI performance. The chapter offers guidance for future developments, providing a roadmap for advancing the field of power electronics.

Together, these chapters provide a comprehensive framework for achieving high-efficiency, EMI-aware switching in modern power electronic systems. The thesis covers the entire spectrum, from device-level design to driver architecture and experimental validation, offering a holistic approach to optimizing power electronic systems.

Chapter 2

Low Gate Energy Power Switches

The scale down trend is impacting not only CMOS devices, but also the technologies used for power switches. The reduction of gate oxide thickness, the scaled lithography and the adoption of wide bandgap (WBG) technologies is heavily impacting the gate driving requirements for new coming generation of power switches with two clear directions: the reduction of the gate energy (E_G) required for switching the device on and off and the reduction of the threshold voltage (V_{th}), as reported in Table 2.1.

Technology	Q_G **[nC]**	**Saturation / Full Enhancement Voltage [V]**	V_{TH} **[V]**	E_G **[nJ]**
TrenchStop^{TM} 10A 600V RCD2	48	13	5	360 at 15 V
CoolMOS™ 600V PFD7 SJ	6	10	4	45 at 15 V
Low E_G IGBT	30	1.5	0.5	22.5 at 1.5 V
600V GaN HEMT	1.6	5	1.7	4 at 6 V

Table 2.1: Comparison of Different Technologies

The reduction of E_G is of particular interest because it allows reducing the gate driver supply and, especially for low power application, it potentially allows integrating the passive components required to supply the gate driver at module level. The reduction of V_{th} introduces challenges in the driving of the power

switches since they become more prone to parasitic turn on (PTO) events: this aspect forces the use of more advanced gate driver architecture where Miller clamp feature and/or negative gate driver supply are required to mitigate this issue [2]. This chapter aims to address these challenges, exploring the design, the implementation, and the characterization of low E_G power switches.

2.1 Low Gate Energy Power MOSFET

Power MOSFETs are increasingly being adopted in low-power, low-cost applications, supplanting IGBTs due to their ability to optimize efficiency at light loads. This is attributed to the ohmic behavior of power MOSFETs, which reduces conduction losses.

In recent years, super junction (SJ) power MOSFETs have emerged as the technology of choice for various power electronic applications. Compared to traditional power MOSFETs, SJ MOSFETs offer significant advantages, including lower Rdson values for the same voltage class, faster switching times due to reduced parasitic capacitance and gate charge (Q_g) [3]. This is due to their particular structure that allows to overcome the silicon limit, Figure 2.1. The decrease in gate charge has a profound impact on reducing driving losses, enabling the miniaturization of both the gate driver and the external passive components required for the gate driver circuitry. For instance, this allows for the use of very low capacitance values in the bootstrap circuit, facilitating the integration of such components at silicon level and enabling the integration at module level.

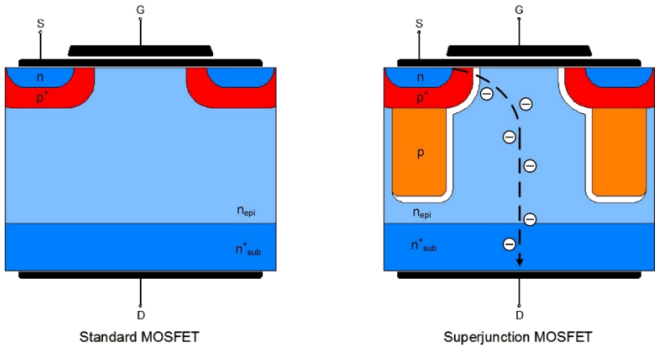


Figure 2.1: SJ MOSFET Cross Section

As a result, a silicon capacitor with a capacitance [4] of 68 nF has been integrated, along with CoolMOS^{TM} PFD7 SJ MOSFETs and a SOI gate driver, into a compact quad flat no-lead (QFN) package measuring 8x9 mm^2. The subsequent sections of this chapter present the characterization procedure for the module, with a particular focus on the bootstrap circuit and on the performance of the on-silicon integrated capacitance.

2.1.1 Single Supply High Voltage Module

The package platform selected for this module is the same 8x9 mm^2 QFN package platform adopted for the low gate enrgy IGBT. The module demonstrator integrates the following chips in a half bridge configuration and its internal structure is shown in Figure 2.2:

- two 1 ohm, 600V Infineon PFD7 CoolMOS^{TM} (Q_1, Q_2);
- one dual channel 650V Infineon Silicon On Insulator (SOI) gate driver with integrated high voltage bootstrap diode (U_1);
- one 68 nF Infineon silicon capacitance (SilCap) as bootstrap capacitor (U_2).

The current and voltage ratings for this module are 2 A (limited by package thermal dissipation) and 600 V. As it is possible to see in Figure 2.2, the size

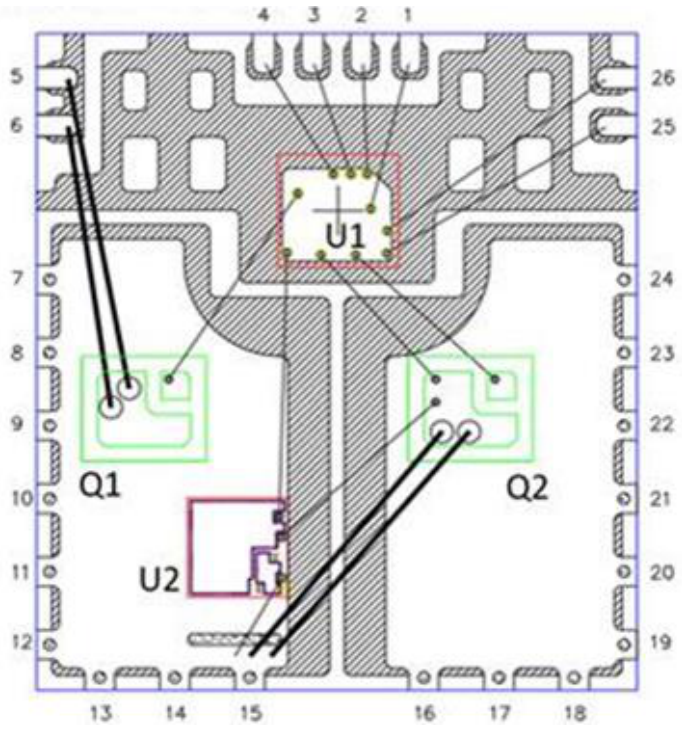


Figure 2.2: Single supply module internal structure

of the leadframe is not optimized for the selected chipset. However using an already existing package platform has allowed building engineering samples in a short time frame and perform the feasibility assessment for the SilCap integration. A half bridge (HB) topology has been considered as the most convenient

for the prototype, but this integration idea can be easily extended to H-bridge and three phase solutions. Furthermore, as it possible to see from Figure 2.2, two monitoring pins (pin 25 and 26) are present in the package outline to monitor the SilCap voltage during the module characterization. Pin 25/26 are not directly bonded to the SilCap to avoid bonding wires to cross leadframe areas with different voltage domains. For this reason, a dedicated gate driver with monitoring V_B and V_S pads has been designed. Pins 7–15 and 16–24 are internally shorted by the leadframe, respectively, and conduct the application current. Only pins 1-4 are available for the supply and the control of the HB. In the next paragraphs, the bootstrap circuit design, the bootstrap circuit characterization and the applicative test results are presented.

2.1.2 Gate Driver Supply

For low power, low cost applications, level-shift gate drivers are a common choice. This kind of gate drivers are generally characterized by a monolithic solution able to guarantee the functional isolation between the high-side and low-side domains through specific technology construction [5]. A typical way of supplying the high side of a level-shift gate driver is by using a bootstrap circuit. This circuit is made of a high voltage diode and a capacitor (Figure 2.3), which allows the energy transfer from the low-side domain to the high-side domain [6]. The gate driver supply rating generally matches the V_{GS} rating, that is typically

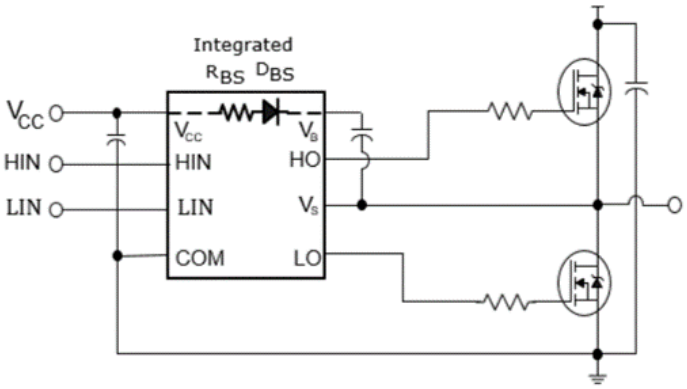


Figure 2.3: Example of bootstrap circuit in level-shift gate driver

15 V for silicon technologies. For this reason, the bootstrap capacitance has to be designed in order to be able to deliver the required Q_G while maintaining the V_{BS} voltage (e.g. the gate voltage) to a value high enough to guarantee the full enhancement of the power MOSFET and to avoid the triggering of the under voltage lockout protection (UVLO). The UVLO protection feature ensures that the gate driver drives the external power switch with a sufficiently high gate voltage. If the gate driver supply voltage goes below the selected threshold voltage, the power switch is turned off to avoid an excessive heat

dissipation due to the degraded on-state characteristics. For the demonstrator, the UVLO threshold has been set by design at 7.85 V. The CoolMOS^{TM} devices have less Q_G than IGBTs and they are fully enhanced at 10 V. This means that variation up to 5 V can be accepted on the gate driver supply without significant performance worsening of the switch (e.g. R_{DSON} degradation and increased thermal dissipation). For this reason, the size of the bootstrap capacitance can be drastically reduced from uF to tens of nF and this enables the usage of silicon based capacitors [4].

2.1.3 Bootstrap Circuit Design

The bootstrap circuit has been designed in order to have a residual V_BS voltage of 10 V when the module is working under the following conditions:

- $T_J = 125$ °C;
- $I_{PHASE} = 2$ Apk;
- $DutyCycle = 95$ %;
- $f_{PWM} = 4$ kHz.

The duty cycle and the pulse width modulation (PWM) frequency have been selected considering low power motor drive as target application. For this application, it is not common to have a switching frequency smaller and a duty cycles higher than the values specified above. The duty cycle has to be intended as the percentage of the PWM period in which the high-side power switch is on. Large duty cycles are critical for bootstrap supplied gate drivers since the bootstrap capacitance has to supply the high-side domain for long times without being recharged [6]. The CoolMOS^{TM} parameters required for the bootstrap sizing have been obtained from the datasheet of the discrete part [7]. Since the gate driver integrated in this module was not available as standalone part during the IPM design phase, the relevant parameters have been obtained both from the datasheet of a similar gate driver already available in the market [8] and from Electronic Design Automation (EDA) simulations. Regarding the power switch, a junction temperature of 125 °C has been considered during the design, since the CoolMOS^{TM} relevant parameters are specified at this temperature in the datasheet. Nevertheless, both the gate driver and the power switch are rated for 150 °C. The minimum value for the bootstrap capacitance (C_{BTS}) has been calculated with the following formula:

$$C_{BTS} \geq \frac{Q_{TOT}}{\Delta V_{BS}} \tag{2.1}$$

where

$$Q_{TOT} = Q_G + Q_{LS} + (I_{QBS} + I_{LKGS} + I_{LK} + I_{LKDIODE}) \cdot T_{HON} \tag{2.2}$$

and

$$\Delta V_{BS} = V_{CC} - V_F - V_{GSmin} - V_{DSon} \tag{2.3}$$

with:

- Q_G as the gate charge required for the turn on of the power switch;
- Q_{LS} as the charge required by the level shifter stage of the gate driver;
- I_{QBS} as the floating section quiescent current;
- I_{LKGS} as the gate-source leakage current;
- I_{LK} as the floating section leakage current;
- $I_{LKDIODE}$ as the bootstrap diode leakage current;
- T_{HON} as high side on time;
- V_{CC} as the low side supply voltage;
- V_F as the forward voltage of the bootstrap diode;
- V_{GSmin} as the required minimum bootstrap capacitor voltage;
- V_{DSon} as the voltage drop on the low side power MOSFET.

Parameter	**Value**
Q_G [nC]	9.5
Q_{LS} [nC]	1
I_{QBS} [µA]	212
I_{LKGS} [nA]	1000
I_{LK} [µA]	12.5
$I_{LKDIODE}$ [µA]	20
T_{HON} [µs]	237.5

Table 2.2: Charge-related parameters

Parameter	**Value**
V_{CC} [V]	15
V_F [V]	0.9
V_{GSmin} [V]	10
$R_{DSon_{125C}}$ [ohm]	1.5

Table 2.3: Voltage related parameters

Substituting the values specified in Table 2.2 and Table 2.3 in Equation 2.2 and Equation 2.3 and applying Equation 2.1, the minimum required capacitance value is equal to 62.6 nF. For this reason, the SilCap with a capacitance value of 68 nF was selected for the integration into the module.

2.1.4 Bootstrap Circuit Characterization

During the module operation, the bootstrap circuit can be charged either when the power MOSFET is conducting (gate signal applied to the gate of the switch and current entering the drain, Figure 2.4) or when the body diode is conducting (gate signal not applied and current entering the source of the switch, Figure 2.5). The charging condition depends on the sign of the current; in the rest of the paper, the current exiting the switch node of the HB is considered as positive load current, while the current entering the switch node of the HB is considered as negative load current. The voltage across the bootstrap capacitor at the end of the charging phase depends on the sign of the load current. The equations for positive and negative load currents are provided here below:

- Positive load current:

$$V_{BS} = V_{CC} - V_F + V_{Fbody} \tag{2.4}$$

- Negative load current:

$$V_{BS} = V_{CC} - V_F - R_{DSon} * I_{phase} \tag{2.5}$$

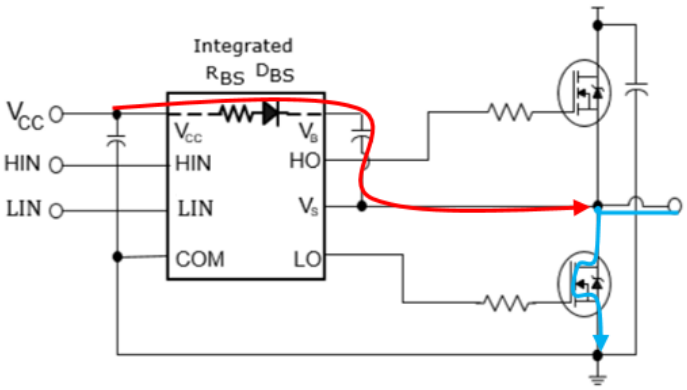


Figure 2.4: Bootstrap charging phase with negative load current

As it is possible to see from Equation 2.4 and Equation 2.5, the charging phase with positive load current is beneficial for the bootstrap supply, since the voltage drop on the body diode of the power MOSFET results added to the supply voltage. The charging phase with negative load current is instead more severe for the bootstrap supply since the voltage drop on the R_{DSon} of the power MOSFET is reducing the initial supply voltage. The module bootstrap circuit has been characterized with both positive and negative currents. The test has been executed by applying a PWM pattern with fixed duty cycle and fixed frequency to the HB, while the load current has been controlled by applying the proper R-L load. The number of PWM cycles has been calculated to guarantee

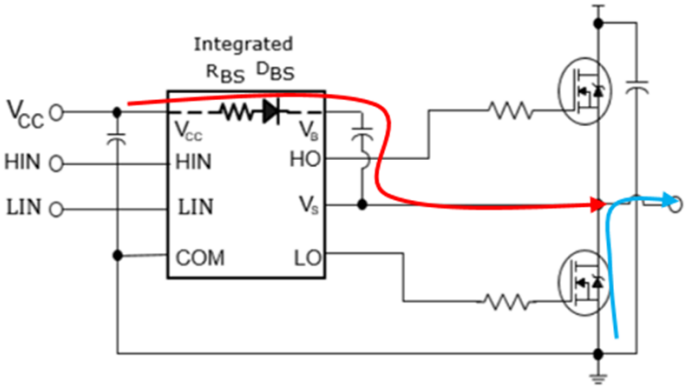


Figure 2.5: Bootstrap charging phase with positive load current

the R-L circuit to reach the steady state condition. The test has been executed for under different working conditions summarized here below:

- $DC+ = 300$ V;
- $I_{LOAD} = 1/2/3$ A;
- $T_J = 25/125/150$ °C (125 °C has been selected just to verify the design, a complete characterization was not executed for this junction temperature);
- $f_{PWM} = 2/4$ kHz.

The aim of the test is to verify that the bootstrap circuit is fulfilling the design criteria and to verify the ruggedness of the design by looking for the limit working condition that the module can guarantee without triggering the UVLO protection of the gate driver.

2.1.5 Experimental Test for Negative Load Current

The setup for negative load current is a typical double pulse setup with the R-L load connected between the $DC+$ and the V_S node (Figure 2.6). The duty cycle has been kept constant at 95% and different R-L load values have been selected to regulate the load current.

A preliminary test with $T_J = 125$ °C, $I_{LOAD} = 2$ A and $f_{PWM}= 4$ kHz has been executed to verify the bootstrap capacitance design. As it is possible to see from Figure 2.7, the V_{BS} voltage reaches 10.16 V at the end of the discharge phase (V_{BSend} in Figure 2.7). This value is in line with the expected value of 10 V and it is proving that the bootstrap circuit is behaving as expected.

After this preliminary test, the characterization has been carried out according to the conditions specified in paragraph 2.3 and it was possible to observe that the device is not showing any UVLO event even with a load current of 3 A when a f_{PWM} of 4 kHz is applied with $T_J = 150$ °C (see Figure 2.8). The

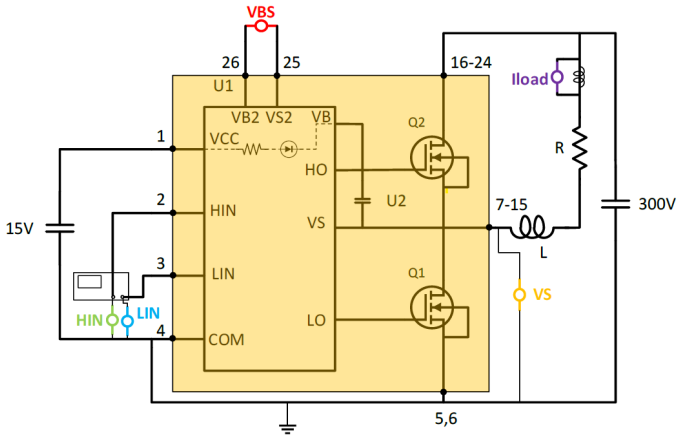


Figure 2.6: Negative load current setup with probe position and colors scheme

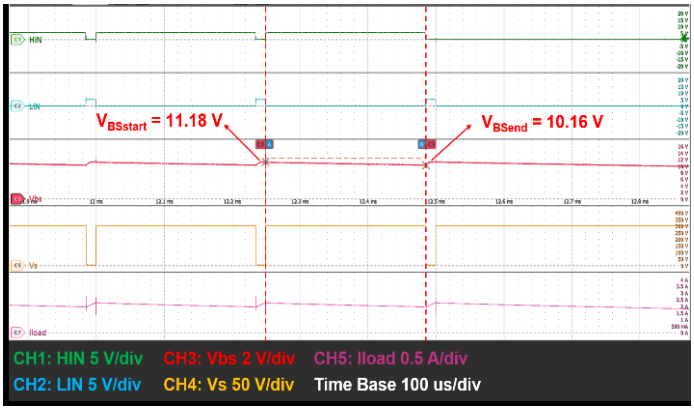


Figure 2.7: Bootstrap circuit design validation, negative load current: T_J = 125 °C, I_{LOAD} = 2 A, f_{PWM} = 4 kHz

voltage at the end of the discharge phase (V_{BSend}) is equal to 8.33 V: the power MOSFET is no longer fully enhanced, therefore this working condition is not recommended as a steady-state working condition. However, with this test, it has been possible to demonstrate that the module is able to withstand a transient overload condition with a load current up to 1.5 times the nominal current without entering any fault state.

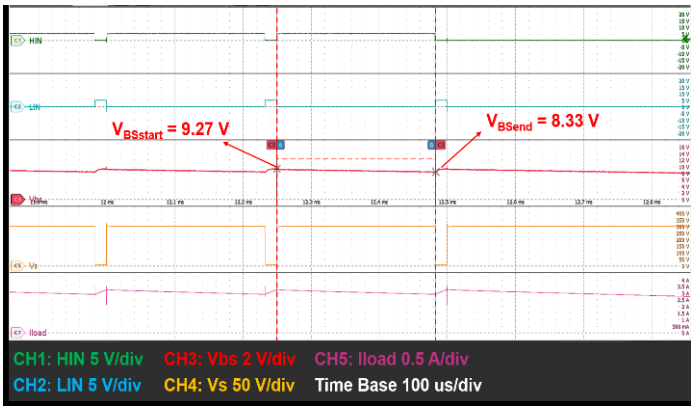


Figure 2.8: Bootstrap circuit characterization, negative load current: $T_J = 150$ °C, $I_{LOAD} = 3$ A, $f_{PWM} = 4$ kHz

In order to find the limit working condition for the module, the switching frequency has been reduced from 4 kHz to 2 kHz, meaning that the on time has been doubled. Even with such f_{PWM} value and $T_J = 150$ °C, the module is still capable to provide the rated current (2 A) with a $V_{BS} = 9.12$ V at the end of the discharge phase. The CoolMOS^{TM} is no longer fully enhanced but the R_{DSon} increase is not expected to be significant. Eventually, when the load current has been increased to 3 A while keeping $f_{PWM} = 2$ kHz and $T_J = 150$ °C, a UVLO event has been detected: as shown in Figure 2.9, the V_{BS} voltage reduces until it reaches 7.84 V ($V_{BS_{UVLO}}$) and from that moment onwards the power switch is turned off by the gate driver. The UVLO threshold was characterized for the specific device under test; however, a detailed discussion is beyond the scope of this work.

The complete characterization results are reported in Table 2.4 and Table 2.5.

I_{LOAD} [A]	$T_j = 25\,°\text{C}$		$T_j = 150\,°\text{C}$	
	$V_{\text{BS, start}}$ [V]	$V_{\text{BS, end}}$ [V]	$V_{\text{BS, start}}$ [V]	$V_{\text{BS, end}}$ [V]
1	12.85	11.94	12.18	11.39
2	12.01	11.1	10.69	9.97
3	11.07	10.16	9.27	8.33

Table 2.4: Characterization results, negative load current at $f_{PWM} = 4$ kHz

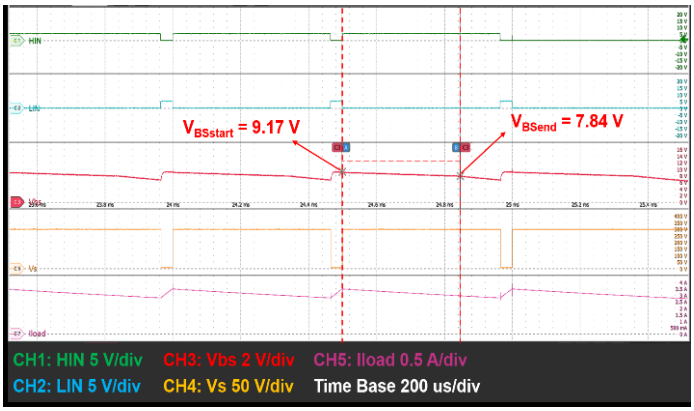


Figure 2.9: Bootstrap circuit characterization, negative load current: $T_J = 150$ °C, $I_{LOAD} = 3$ A, $f_{PWM} = 2$ kHz; UVLO event detected

I_{LOAD} [A]	$T_j = 25\,^{\circ}\text{C}$		$T_j = 150\,^{\circ}\text{C}$	
	$V_{\text{BS, start}}$ [V]	$V_{\text{BS, end}}$ [V]	$V_{\text{BS, start}}$ [V]	$V_{\text{BS, end}}$ [V]
1	12.66	10.99	12.24	10.56
2	12.14	10.18	10.76	9.12
3	11.16	9.31	9.28	< 7.84

Table 2.5: Characterization results, negative load current at $f_{PWM} = 2\,\text{kHz}$

2.1.6 Experimental Test for Positive Load Current

The setup for the positive load current makes use of an auxiliary HB to implement an H-bridge configuration. The HB under test has been switched with a constant duty cycle of 95% while the PWM of the auxiliary HB has been operated to regulate the load current. The R-L load has been connected between the two middle points of the H-bridge (Figure 2.10).

As described by Equation 2.4 , the bootstrap circuit working condition is much less severe with a positive load current. In this case, the bootstrap capacitor is able to provide the correct supply to the gate driver high side domain also in case of $T_J = 150$ °C, $I_{LOAD} = 3$ A and $f_{PWM} = 2$ kHz (see Figure 2.11). In particular, all the analyzed working conditions are showing quite a significant margin both from the UVLO threshold (7.85 V) and from the lower limit of the full enhancement region (10 V). The results are summarized in Table 2.6 and Table 2.7.

2.1.7 Application Test

The aim of the application test is to verify that the module is working properly in real application conditions. For this purpose, three HBs have been mounted on a dedicated printed circuit board (PCB) to implement a three-phase inverter

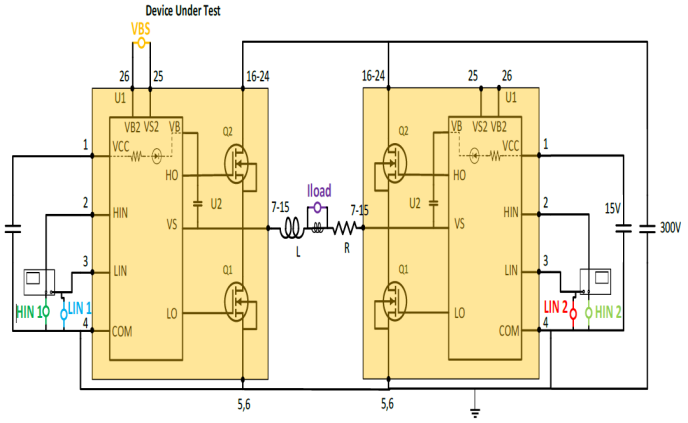


Figure 2.10: Positive load current setup with probe position and colors scheme

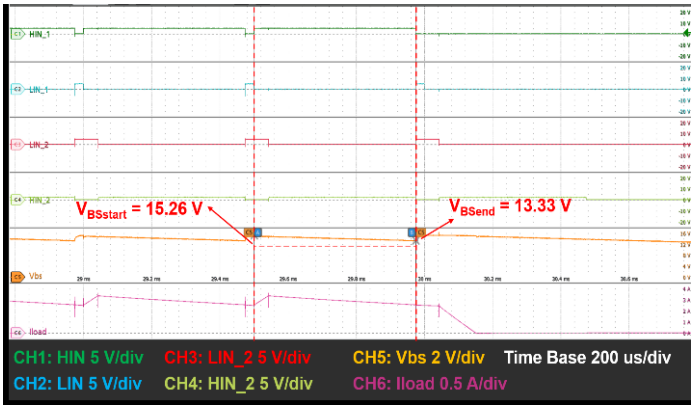


Figure 2.11: Bootstrap circuit characterization, positive load current: T_J = 150 °C, I_{LOAD} = 3 A, f_{PWM} = 2 kHz

I_{LOAD} [A]	$T_J = 25\,^{\circ}\mathrm{C}$		$T_J = 150\,^{\circ}\mathrm{C}$	
	V_{Bstart} [V]	V_{Bsend} [V]	V_{Bstart} [V]	V_{Bsend} [V]
1	14.47	13.57	14.53	13.67
2	14.94	13.78	14.90	13.91
3	14.28	14.00	14.96	14.10

Table 2.6: Characterization results, positive load current at $f_{PWM} = 4$ kHz

$I_{\mathbf{LOAD}}$ [A]	$T_J = 25\,^{\circ}\mathrm{C}$		$T_J = 150\,^{\circ}\mathrm{C}$	
	$V_{B\mathrm{start}}$ [V]	$V_{B\mathrm{end}}$ [V]	$V_{B\mathrm{start}}$ [V]	$V_{B\mathrm{end}}$ [V]
1	14.52	12.58	14.68	12.94
2	14.85	12.88	14.90	13.00
3	15.06	13.24	15.19	13.29

Table 2.7: Characterization results, positive load current at $f_{PWM} = 2$ kHz

(Figure 2.12) used to drive a permanent magnet surface mount (PMSM) motor. The PCB is a three layer, 2 oz PCB. The system has been controlled using a dedicated motor control solution [9] from Infineon. During the test, both

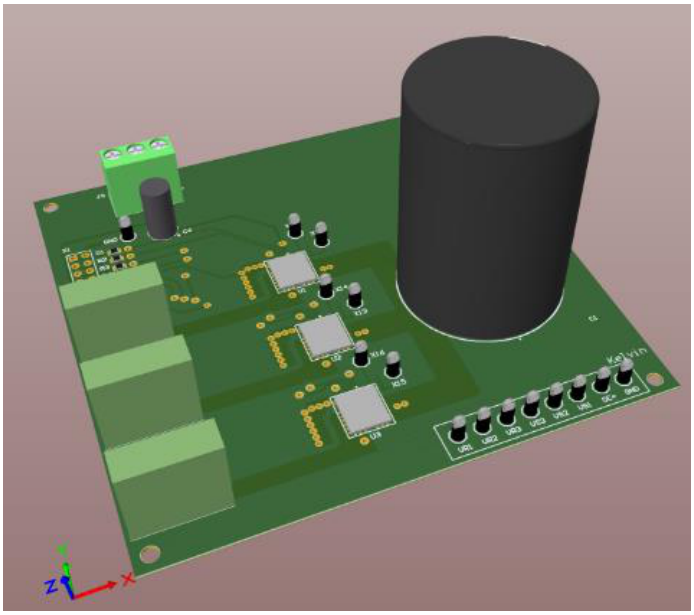


Figure 2.12: PCB for motor run test

the V_{BS} voltage and the case temperature have been monitored. The case top temperature (T_{Ctop}) has been measured using a thermal camera and, with this measurement, it has been possible to evaluate the current capability of the

device in real application conditions. The test has been performed under the following conditions:

- $DC+ = 300$ V;
- $f_{PWM} = 4/10/20$ kHz.

The test has been stopped once the steady state T_{Ctop} has reached 150 °C. For QFN heatsink-less module, the T_{Ctop} can be considered as a good approximation of the junction temperature [10] [11]. The test results are reported in Table 2.8, while an example of thermal measurement and electrical quantities are provided in Figure 2.13 and Figure 2.14 respectively.

f_{PWM} [kHz]	I_{PHASE} [$\mathrm{A_{rms}}$]	V_{BS} [V]
4	1.176	10.44
10	1.012	10.90
20	0.78	11.32

Table 2.8: Maximum phase current and minimum V_{BS} voltage as a function of the PWM frequency, $T_{Ctop} = 150$ °C

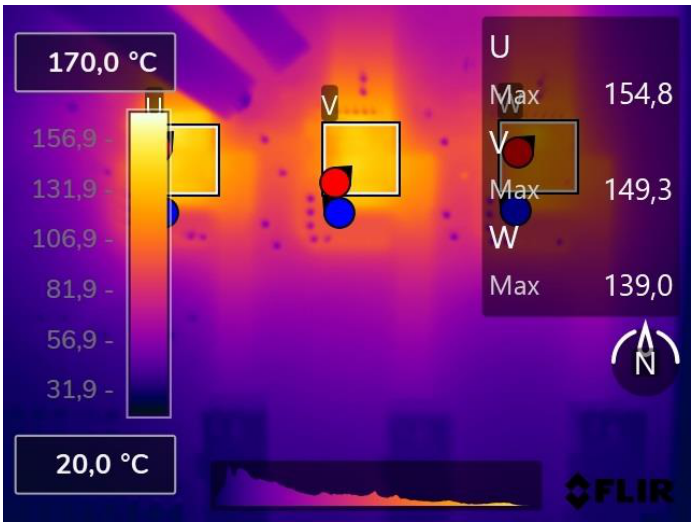


Figure 2.13: Measurement of T_{Ctop} for $f_{PWM} = 4$ kHz and $I_{PHASE} = 1.176$ A_{rms}

Since the low PWM frequencies are causing a deeper dis-charge of the bootstrap capacitor, which could lead to performance degradation, the test with $f_{PWM} = 4$ kHz has been repeated with three HBs in which the bootstrap capacitance has been not integrated in the module. A standard approach has been used and a 1 uF Multi-Layer Ceramic Capacitor (MLCC) has been soldered on

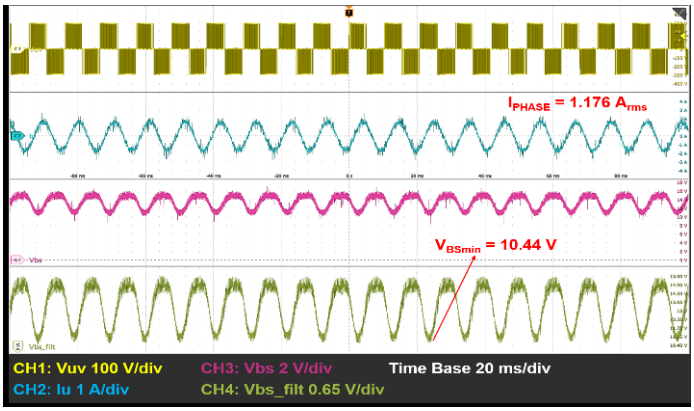


Figure 2.14: Electrical quantities for $f_{PWM} = 4$ kHz and $I_{PHASE} = 1.176$ A_{rms}

the PCB and connected to pin 25 and 26 of the device. It is possible to see from Figure 2.16 that $V_{BSmin} = 12.65$ V when a 1 uF MLCC capacitor is connected externally; this value is 2.21 V higher than the value measured with the integrated SilCap (Figure 2.14). Nevertheless, the temperature difference between the modules with external MLCC capacitor (Figure 2.15) and the modules with the integrated SilCap (Figure 2.13) is negligible. In both cases, the power MOSFET are fully enhanced and the deeper discharge of the SilCap is not affecting the power dissipation.

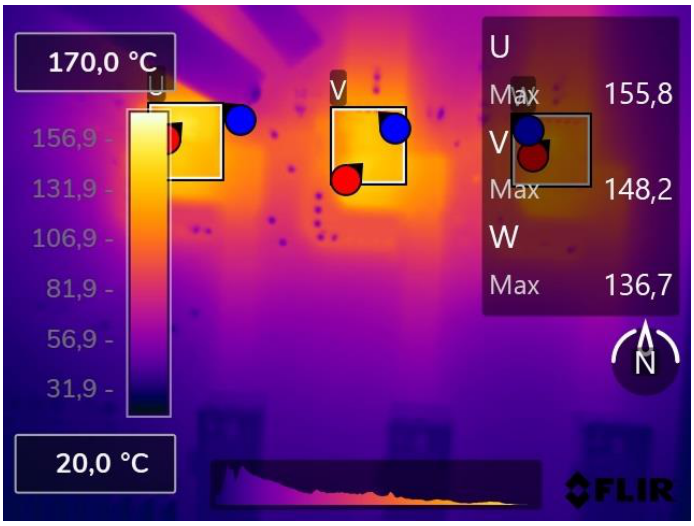


Figure 2.15: Measurement of T_{Ctop} for $f_{PWM} = 4$ kHz and $I_{PHASE} = 1.176$ A_{rms} with external MLCC

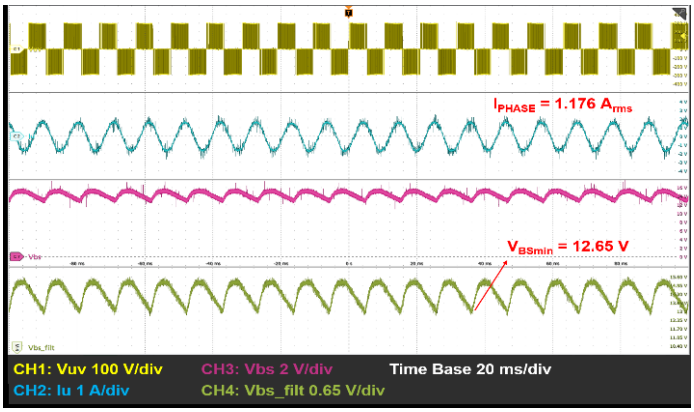


Figure 2.16: Electrical quantities for $f_{PWM} = 4$ kHz and $I_{PHASE} = 1.176$ A_{rms} with external MLCC

2.1.8 Low Gate Energy Power MOSFET Conclusion

In the proposed demonstrator, thanks to the low Q_G needs of the CoolMOS^{TM} power MOSFET, a SilCap with a capacitance value equal to 68 nF has been copackaged. The proposed bootstrap circuit solution has been first characterized with dedicated tests which recreate the typical working conditions and then running a real motor drive application. The measurements have shown that the module is able to provide the rated current of 2 A for a PWM frequency of both 4 kHz and 2 kHz. With $f_{PWM} = 4$ kHz, the module is even able to safely provide a transient overload current up to 1.5 times the nominal current. With $f_{PWM} = 2$ kHz, even if the nominal current is still delivered, the power MOSFET are no longer fully enhanced leading to degraded on characteristic and potential higher dissipation. Eventually the module with the integrated bootstrap network has been compared to a standard module with external bootstrap network and their behavior has been proven to be very similar. The study of the SilCap integration advantages, its reliability and its combination with other power switch technologies can be the scope of future work.

2.2 Low Gate Energy IGBT

The Insulated Gate Bipolar Transistor (IGBT) has been a cornerstone of power electronics for decades, offering a unique combination of high current handling capability and low switching losses. However, as the demand for more efficient and compact power conversion systems continues to grow, the need for further improvements in IGBT technology has become increasingly pressing. In response to this challenge, a new generation of IGBTs has been developed, featuring innovative gate cell designs that promise to significantly reduce conduction and switching losses.

One such device is the low gate energy IGBT developed by Infineon Technologies, which is characterized by a number of advantages over its conventional counterparts. This new technology enables reduced conduction losses and turn-off losses, resulting in improved overall efficiency. The key to these benefits lies in the innovative gate cell design of the device, which has been carefully optimized to reduce the energy losses.

However, as with any new technology, the low gate-energy IGBT also presents some challenges. One of the most significant of these is its susceptibility to parasitic turn-on, a phenomenon in which the device is inadvertently switched on by the commutation of the complementary switch. This leads to the need of developing a dedicated gate driver solution to mitigate this issue.

The results of the experiments demonstrate the effectiveness of the new gate driver circuit in correctly driving the low gate energy IGBT.

Once the stand-alone gate driver has been characterized and its functionalities has been proven, a module, integrating the low-gate-energy IGBT and the new gate driver circuit, has been assembled. The module has been tested under various operating conditions and the results are reported.

The results of the module characterization activity indicate that the current implementation of the low gate energy IGBT exhibits considerable potential, but it also reveals certain limitations that need to be addressed. Some weaknesses in the process have been identified that can affect the performance and reliability of the device. However, these issues are expected to be addressed in future versions of the device, and the results of this work provides valuable insights and guidance for future developments.

2.2.1 Low Gate Energy IGBT Characteristics

One of the key features of the low-gate-energy IGBT is its ability to operate with a significantly reduced gate voltage, requiring only 1.5 V to be fully saturated. This value is 10 times lower than that of today's IGBTs. The reduced gate voltage range is related to the design of its gate cell. Although studies on 5 V gate IGBTs have been reported in the literature [12][13][14], the implementation of an IGBT with a gate voltage of 1.5 V is a completely new development.

The adoption of this new gate cell (Figure 2.17) allows to reach conduction losses comparable to Silicon Carbide (SiC) MOSFET as it is possible to observe from the simulation results in Figure 2.18.

Furthermore, the new gate cell approach employed in the low gate energy IGBT enables a reduction in turn-off losses, attributed to the diminished plasma density within the device just before the turn-off event, thereby mitigating the characteristic current tail effect commonly observed in state-of-the-art IGBTs. Specifically, the turn-off energy of the low gate energy IGBT is found to be 25% lower than that of its state-of-the-art counterpart, underscoring the efficacy of this design approach in minimizing switching losses.

The reduced gate voltage of the low gate-energy IGBT results in a significant decrease in the device's gate energy. Notably, despite having a gate charge (Q_G) comparable to that of state-of-the-art IGBTs (Table 2.1), the energy required

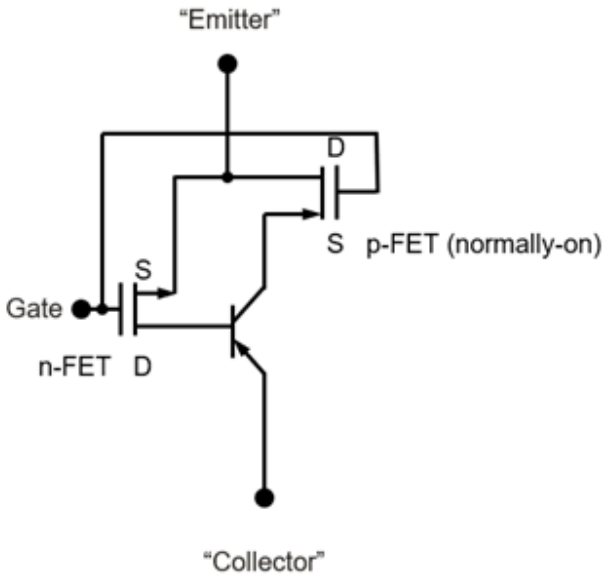


Figure 2.17: Low Gate Energy IGBT simplified circuit

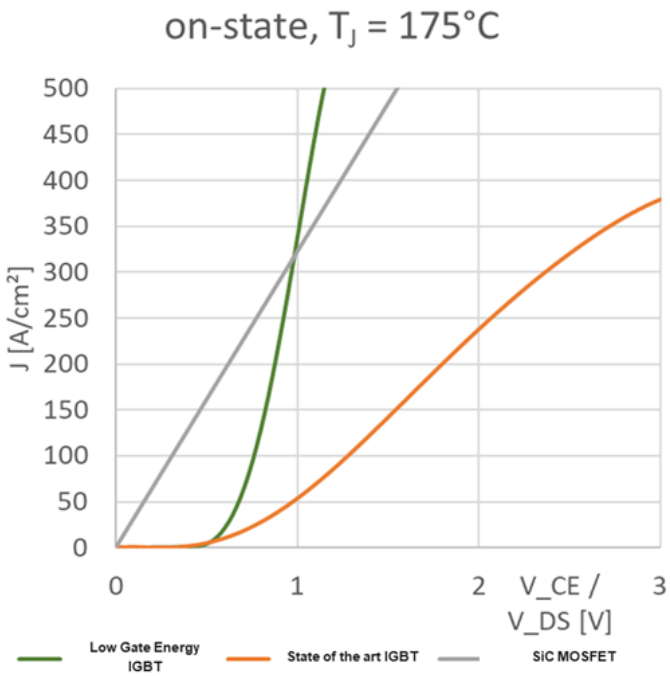


Figure 2.18: On-State Loss comparison among different technologies

for switching is directly proportional to the gate voltage. Consequently, the low gate energy IGBT exhibits a tenfold reduction in gate energy consumption compared to standard IGBTs. This characteristic enables a substantial decrease in the power consumption of the gate circuitry, thereby enhancing the overall system efficiency.

The threshold voltage of the low gate energy IGBT is typically around 0.5 V. The extremely low threshold voltage necessitates a close interaction between the IGBT and the gate driver integrated circuit (IC), making the low gate energy IGBT an attractive candidate for integrated solutions. In such a scenario, the stray inductance between the IGBT and the gate driver IC can be minimized and controlled. In contrast, a discrete approach, where the gate driver IC and IGBT are housed in separate packages, introduces stray inductance due to the package leads and PCB traces. This can lead to PTO events. Furthermore, the PCB design is customer-specific and outside the direct control of the device manufacturer. To mitigate PTO events in discrete configurations, a negative turn-off voltage is required, which, however, introduces additional turn-on delay, ultimately impacting the system's efficiency.

The low gate voltage requirements of this IGBT pose a challenge for users accustomed to standard IGBTs. Currently, most commercially available gate driver supplies operate within the 15-20 V range, whereas solutions capable of generating the specific voltage required by the low gate energy IGBT are scarce. Notably, this IGBT was designed as a cost-effective alternative to wide bandgap semiconductors, targeting the home appliance market. In this context, the use of additional converters to step down the voltage to the required range is not feasible. To address this issue, a custom gate driver has been developed, which internally scales down the voltage to the level required by the IGBT without the need for external components. Furthermore, this gate driver provides a low-impedance path to ensure safe turn-off and prevent PTO events, even when the turn-off voltage is set to 0 V, thereby enabling the use of a unipolar gate driver supply.

Ultimately, the ability to maintain a standard gate driver supply voltage (e.g., 15 V) in conjunction with the reduced gate energy enables the downsizing of the passive components required to supply the gate driver.

2.2.2 Gate Driver Specifications and Architecture

The gate driver plays a crucial role in determining the dynamic behavior of the power switch, as its output characteristics directly impact the turn-on and turn-off transitions of the driven power switch. Notably, in the context of an integrated solution, the gate driver is designed to interface directly with the power switch, precluding the use of any intermediate passive components. Consequently, the output stage of the gate driver must be carefully designed to meet the specific requirements of the low gate energy IGBT and the application in question. Given that this new IGBT technology is targeted at home appliance applications, a motor drive application was selected as a suitable test platform, as it necessitates slow and well-controlled voltage slew rates to pre-

vent premature failure of the motor winding insulation. The product requirements for the low gate energy IGBT driver are summarized in Table 2.9. To investigate the turn-off characteristics of the IGBT, three distinct gate driver configurations were implemented, each differing in their turn-off equivalent resistance. Specifically, three turn off resistance values - 50 ohm, 100 ohm, and 200 ohm - were selected to systematically evaluate the turn-off performance of the IGBT, thereby facilitating a comprehensive analysis of the device's behavior under varying impedance conditions. The gate driver architecture is based on

Parameter	**Value**	**Note**
Output Source Current [mA]	4	V_{inmin} = 0.86 V, Target dv/dt = 5 V/ns
	2.5	V_{inmin} = 0.86 V, Target dv/dt = 3 V/ns
Output Sink Path Impedance [ohm]	200	Different impedance values are required to evaluate the turn off performance of the low gate energy IGBT in different conditions
	100	
	50	
Miller Clamp Impedance [ohm]	8	Value to avoid parasitic turn on
Miller Clamp Threshold [mV]	350	Miller clamp threshold must be lower than the IGBT threshold, not to influence the turn off procedure ($V_{th,typ,IGBT}$ = 0.5 V)
UVLO Rising Threshold [V]	8	Limited by the gate driver, not by the switch technology
UVLO Falling Threshold [V]	7	Limited by the gate driver, not by the switch technology
Output Voltage [V]	1.5	
Supply Voltage [V]	15	

Table 2.9: Gate Driver Requirement

a monolithic dual-channel level-shifter integrated circuit [15], which enables the simultaneous control of both the high-side and low-side switches in a half-bridge configuration, Figure 2.19. The development of this gate driver leverages SOI technology, which features a buried oxide layer and deep trenches (Figure 2.20) that effectively isolate the various voltage domains, enhancing the robustness

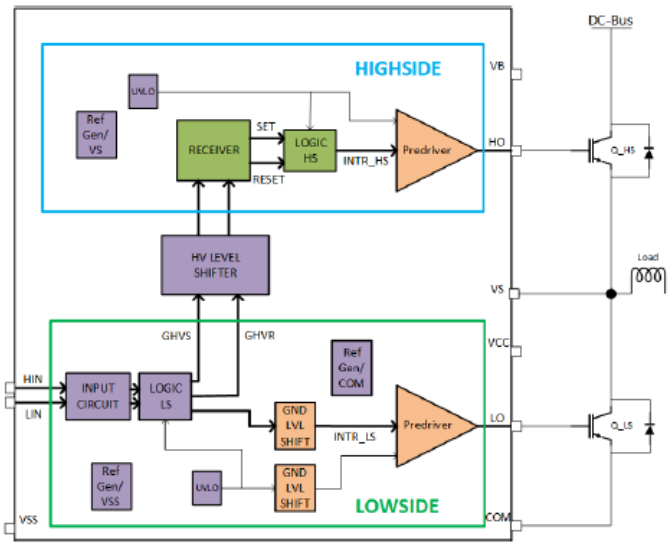


Figure 2.19: Gate Driver Block Diagram

against latch-up events, and provide functional isolation between the different voltage domains, ensuring reliable operation. Additionally, this technology allows the integration of a high-voltage bootstrap diode, eliminating the need for external high-voltage components. The primary distinction between this gate

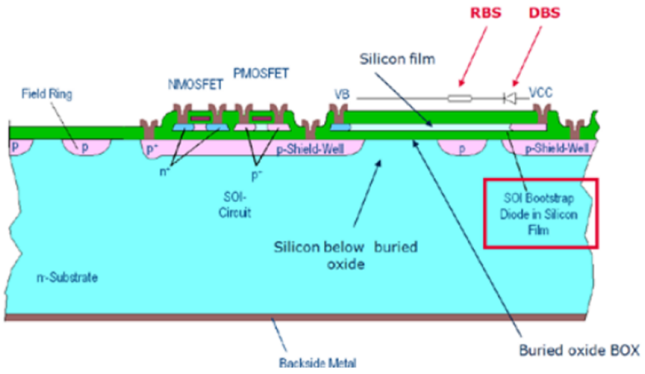


Figure 2.20: SOI technology Cross Section[16]

driver and standard devices based on the same technology is the design of the output stage. In contrast to conventional gate drivers, which typically employ a CMOS output stage to achieve rail-to-rail output voltage, the gate driver developed for the low gate energy switch features a closed-loop voltage regulator. This regulator ensures that the gate-emitter voltage of the IGBT remains below

1.5 V. A high-level block diagram of the gate driver is presented in Figure 2.21.

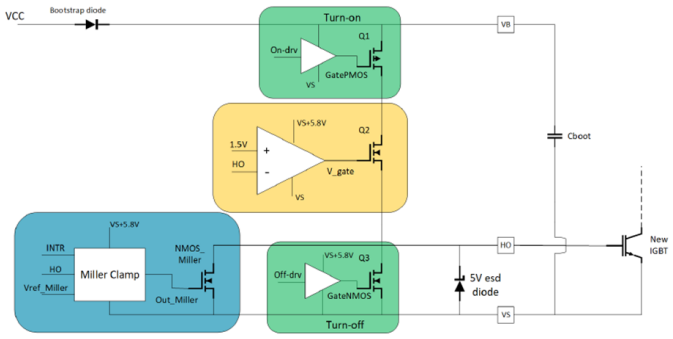


Figure 2.21: Gate Driver Architecture

2.2.3 Gate Driver Characterization

Prior to integrating the IC into the module assembly, the stand-alone gate driver underwent characterization to verify its functionality. The results of this activity indicate that both channels of the gate driver are capable of providing a regulated voltage of 1.5 V (Figure 2.23). Although voltage peaks of up to 1.64 V were observed on the high-side channel, this value remains below the absolute maximum gate-emitter voltage of 1.7 V.

The source current was found to meet the requirement of 4 mA (Figure 2.25), and the Miller clamp threshold was correctly set at 350 mV. While the Miller clamp impedance was slightly higher than the target value of 8 ohm (Figure 2.24), it falls within the typical process spread for SOI gate driver processes. The Miller-clamp impedance and the turn-off NMOS impedance were estimated by monitoring the discharge of a 2.2 µF ceramic capacitor directly connected to the gate driver output stage. Specifically, the NMOS resistance was obtained using (2.6), whereas the Miller-clamp resistance was derived using (2.7). The corresponding test setup is shown in Figure 2.22.

$$R_{\mathrm{NMOS}} = -\frac{\Delta t}{C \ln\left(\frac{V(t)}{V(0)}\right)} \tag{2.6}$$

$$R_{\mathrm{MC}} = \frac{R_{\mathrm{NMOS}}\, R_{\mathrm{eq}}}{R_{\mathrm{NMOS}} - R_{\mathrm{eq}}} \tag{2.7}$$

2.2.4 Low Gate Energy IGBT Module

Upon successful verification of the standalone gate driver characteristics, the assembly of the module was initiated. A QFN 8x9 mm^2 package platform

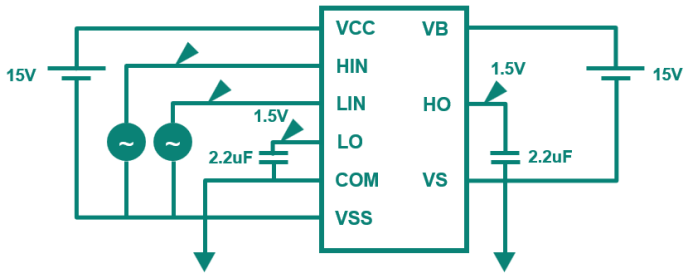


Figure 2.22: Test Setup for NMOS and Miller clamp Resistance Measurement

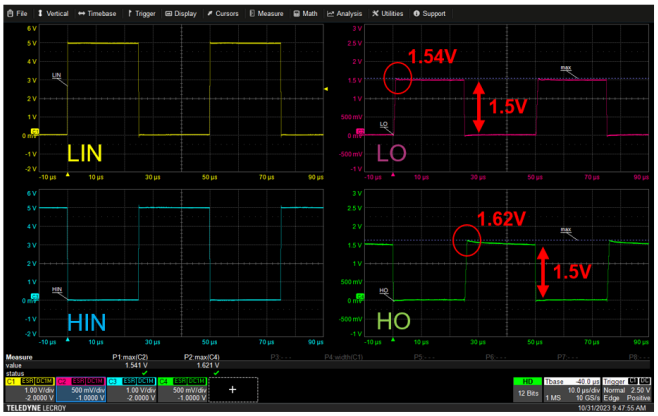


Figure 2.23: Gate Driver Output Voltage

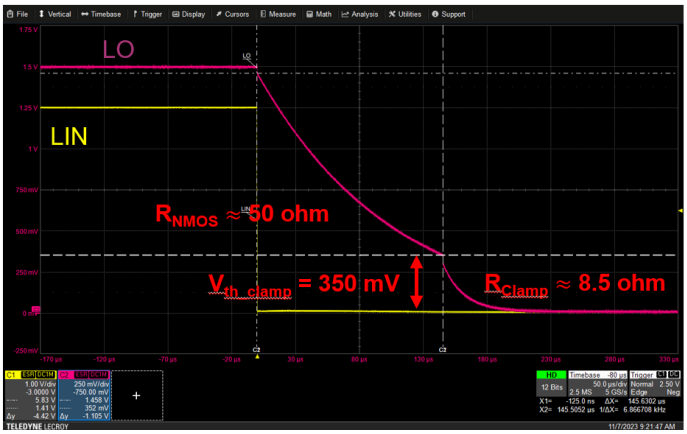


Figure 2.24: Gate Driver Turn Off Parameters

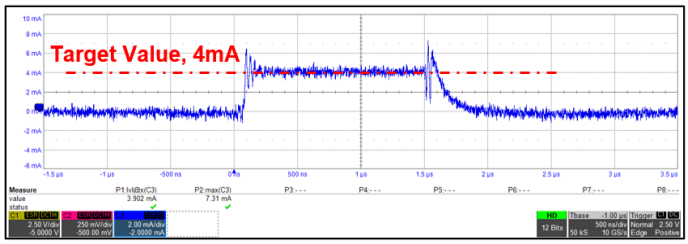


Figure 2.25: Gate Driver Output Current

already available in the market was chosen for this purpose [17], notwithstanding its less-than-ideal suitability for the current rating of the integrated IGBTs. The primary motivation behind this selection was the availability of a QFN fast prototyping line, which enables the rapid generation of samples. Secondly, these samples were intended solely for evaluating the gate driver's capability to properly drive the low gate energy IGBTs in a closely packed environment, thereby minimizing stray inductance, but they are not meant to be used in a real application environment. The bonding diagram of the device under investigation is illustrated in Figure 2.26. The module demonstrator integrates the following chips in a half bridge configuration:

- two 10 A, 650V Infineon Low Gate Energy IGBTs (Q_1, Q_2);
- one dual channel 650V Infineon SOI gate driver with integrated high voltage bootstrap diode (U_1);
- two 6A, 600V Infineon EC3 Rapid diodes (D_1, D_2).

The module in question has been characterized by a current rating of 2A, which is primarily limited by the thermal dissipation constraints of the package, and a voltage rating of 600V. Notably, the diode's current rating is not commensurate with the full current handling capability of the IGBT. This discrepancy can be attributed to the overriding priority of rapid prototyping, which necessitated the selection of readily available components. Furthermore, the package's inherent limitations would have precluded the continuous testing of the IGBT's full current rating, thereby rendering the diode's reduced current rating a pragmatic compromise. The HB topology has been selected to simplify the characterization of the module, however the concept can be extended to three phase topologies.

2.2.5 Low Gate Energy IGBT Module Characterization

The characterization of the module has been concentrated on its dynamic parameters, prompting the execution of a double pulse test (DPT). The DPT is a standard test methodology employed to evaluate the dynamic behavior of a half-bridge switching cell and verify the correct and safe operation of the switching cell itself. During the DPT, various parameters can be measured, including:

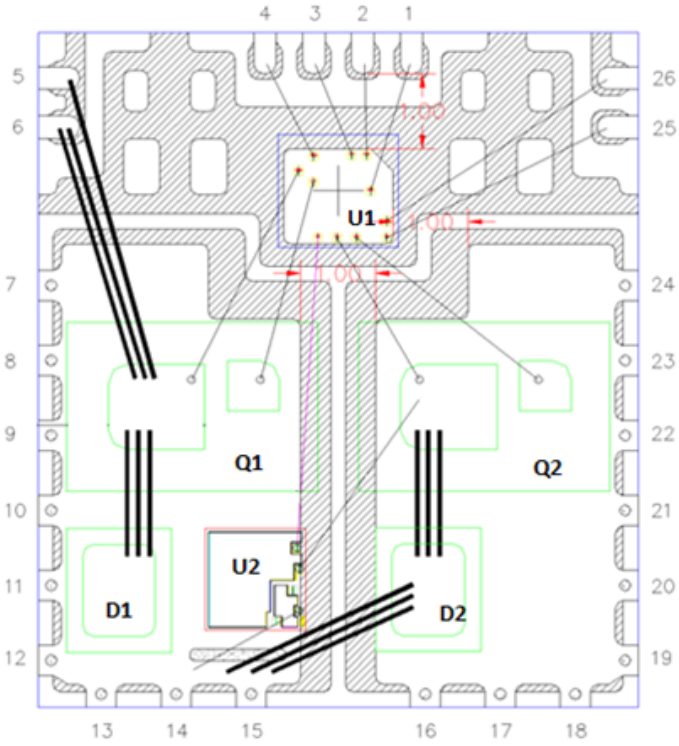


Figure 2.26: Nano IGBT IPM bonding diagram

- the turn-on and turn-off energies of the power switch; ;
- the power switch timings;
- the gate driver timings.

The DPT protocol involves applying two pulses to the gate of the low-side switch in the half-bridge configuration. An inductive load is connected between the high-voltage source and the low-side switch, while the high-side switch of the half-bridge operates as a freewheeling diode during the interval between the two pulses. The first pulse initiates the rise of current in the inductor from zero to the desired value. Subsequently, the low-side power switch is turned off, and the turn-off event parameters are measured. Following a brief time interval of several microseconds, the second pulse is applied to the gate of the low-side power switch, and the turn-on event parameters are measured. Notably, this turn-on event occurs with a current equal to the desired value, as the current in the inductor remains relatively unchanged. A simplified schematic of the DPT test setup is illustrated in Figure 2.27, while general guidelines for hardware design and measurements are presented in [18]. The characterization has been

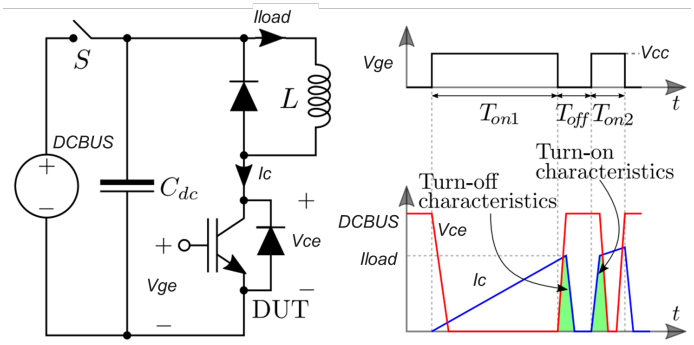


Figure 2.27: DPT schematics and approximate waveforms showing DPT principle

performed soldering the module to a dedicated PCB with 1.6 mm FR4 thickness and 2 oz copper. The PCB substrate is shown in Figure 2.28.

Low Gate Energy IGBT Module Double Pulse Test Results

The DPT has been conducted under the following conditions:

- DCBUS = 300 V;
- I_{LOAD} = 0.1/0.25/.../9/10 A;
- T_J = 25/150 °C;

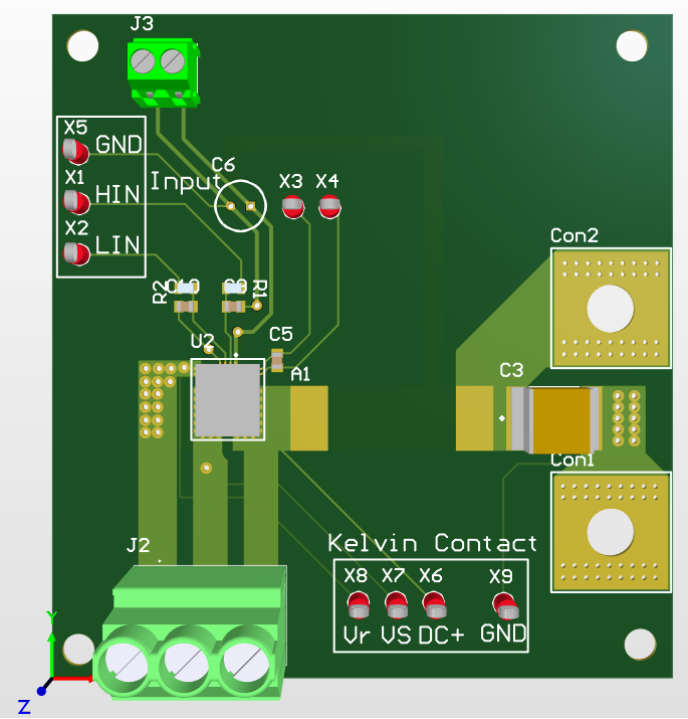


Figure 2.28: Double Pulse Test PCB

- DUT = N1-1 (R_{off} = 50 ohm), N2-1 (R_{off} = 100 ohm), N3-1 (R_{off} = 200 ohm) (Table 2.9).

It is worth noting that all gate driver variants exhibit the same turn-on current and Miller clamp impedance. The DPT test results for two current values (4 A and 10 A) are presented for N1-1 in Figures 2.29, 2.32, for N2-1 in Figures 2.30, 2.33, and for N3-1 in Figures 2.31, 2.34. The results at the IGBT nominal current with Tj = 150 °C can be observed in Figures 2.35, 2.36, and 2.36. As evident from the measurement results, all gate driver variants are capable of correctly turning on and off the low gate energy IGBT up to the nominal current. However, turn-off weaknesses are observed on N1-1 (Figure 2.29b) and on N2-1 (Figure 2.30b) at Tj = 25 °C, and on all variants at Tj = 150 °C (Figures 2.35b, 2.36b, 2.37b). The reason for the turn-off weakness has been identified as an issue with the IGBT manufacturing process, and improvement actions will be taken to correct this behavior. Since the low gate energy IGBT is still in the pre-development phase, the manufacturing processes are not yet finalized.

Furthermore, the turn-on event exhibits differences among the analyzed variants. An analysis of the assembly revealed that the original IGBT position on the wafer could be traced, and it was found that the three tested samples are characterized by IGBTs from different areas of the wafer, suggesting a manufacturing issue with the IGBT. Gate driver part-to-part variation is unlikely to be the cause of the different turn-on behavior, as the gate driver technology is a released technology with high yields. For the N2-1 variant, a PTO event is likely to occur; although the Miller clamp is the same for all gate drivers, it is not guaranteed that all IGBTs have the same gate characteristics because of the afore mentioned process spread among the wafer, leading to parasitic turn-on.

To mitigate these issues, two containment actions have been taken:

- improvement of the front-end IGBT manufacturing;
- implementation of a Miller clamp with lower impedance to avoid PTO.

Ultimately, it has been observed that the turn-off energy decreases for higher R_{off} values; this is due to the particular gate structure of the low gate energy IGBT. When higher turn-off impedance values are used, the plasma removal from the drift region is maximized, and the turn-off di/dt is higher (Table 2.12), leading to lower losses (Table 2.10). The results are not confirmed at high current and high temperature because of the turn off weakness creating distortion on the voltage and current waveforms (Table 2.13, Table 2.11).

I_{load} = **4 A**	**Turn On Energy [uJ]**		**Turn Off Energy [uJ]**	
	25deg	**150deg**	**25deg**	**150deg**
N1-4	48.56	73.86	39.33	66.34
N2-4	42.66	62.83	34.72	55.52
N3-4	45.12	61.90	27.63	45.56

Table 2.10: Switching energy values for different temperatures at $I_{load} = 4$ A

I_{load} = **10 A**	**Turn On Energy [uJ]**		**Turn Off Energy [uJ]**	
	25deg	**150deg**	**25deg**	**150deg**
N1-4	209.97	216.44	113.10	182.86
N2-4	106.53	128.97	103.70	171.42
N3-4	97.56	135.97	73.22	171.43

Table 2.11: Switching energy values for different temperatures at $I_{load} = 10$ A

I_{load} = **4 A**	**Turn On di/dt [A/us]**		**Turn Off di/dt [A/us]**	
	25deg	**150deg**	**25deg**	**150deg**
N1-4	400.36	384.61	69.17	48.41
N2-4	332.85	299.17	95.12	133.80
N3-4	283.67	256.39	112.30	448.67

Table 2.12: Turn On and Turn Off di/dt values for different temperatures at $I_{load} = 4$ A

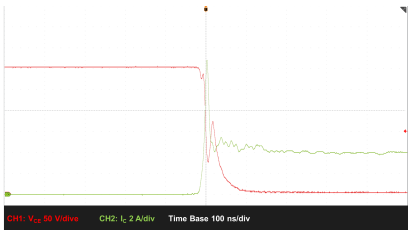
I_{load} = **10 A**	**Turn On di/dt [A/us]**		**Turn Off di/dt [A/us]**	
	25deg	**150deg**	**25deg**	**150deg**
N1-4	690.81	675.52	476.86	168.49
N2-4	677.12	502.41	769.68	664.90
N3-4	551.92	448.67	525.04	528.30

Table 2.13: Turn On and Turn Off di/dt for different temperatures at $I_{load} = 10$ A

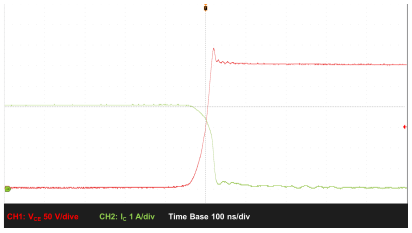
(a)

(b)

Figure 2.29: N1-1 turn on (a) and turn off (b) at 4 A, 25 °C



(a)



(b)

Figure 2.30: N2-1 turn on (a) and turn off (b) at 4 A, 25 °C

(a)

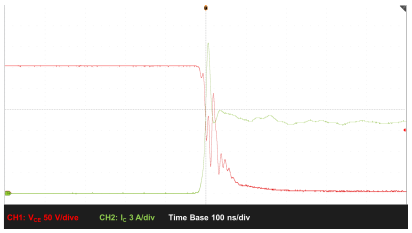
(b)

Figure 2.31: N3-1 turn on (a) and turn off (b) at 4 A, 25 °C

(a)

(b)

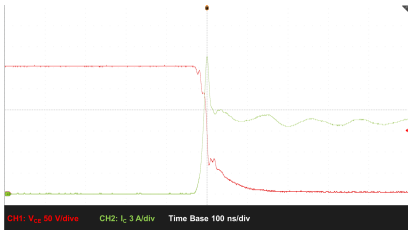
Figure 2.32: N1-1 turn on (a) and turn off (b) at 10 A, 25 °C



(a)

(b)

Figure 2.33: N2-1 turn on (a) and turn off (b) at 10 A, 25 °C



(a)

(b)

Figure 2.34: N3-1 turn on (a) and turn off (b) at 10 A, 25 °C

(a)

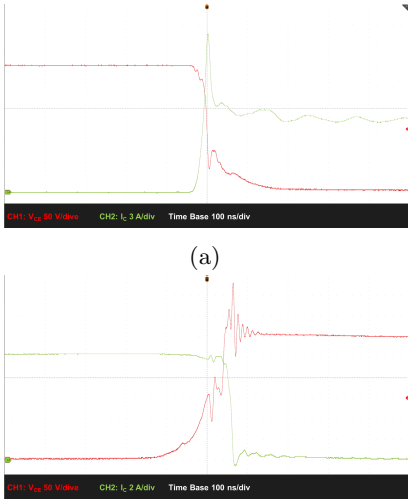
(b)

Figure 2.35: N1-1 turn on (a) and turn off (b) at 10 A, 150 °C

(a)

(b)

Figure 2.36: N2-1 turn on (a) and turn off (b) at 10 A, 150 °C



(a)

(b)

Figure 2.37: N3-1 turn on (a) and turn off (b) at 10 A, 150 °C

Chapter 3

Gate Shaping

Silicon carbide (SiC) has emerged as a highly advanced material in the development of power switches, which are critical components in a wide range of applications, including renewable energy systems, electric vehicles, and industrial power supplies. The unique properties of SiC power switches, such as their high breakdown voltage and low on-resistance, offer several advantages over traditional silicon-based switches, including higher switching frequencies, lower losses, and improved thermal management. However, to fully exploit the potential of SiC power switches and maximize their efficiency, the development of advanced driving techniques is essential.

The distinct characteristics of SiC power switches necessitate specialized driving methods to optimize their performance. Conventional driving techniques, which were developed for silicon-based switches, may not be suitable for SiC power switches, as they can lead to reduced efficiency, increased losses, and even device failure. In contrast, advanced driving techniques can help to minimize switching losses, reduce electromagnetic interference (EMI), and improve the overall reliability of the system. These techniques may include optimized gate driving, active gate control, and other methods that are specifically designed to leverage the unique properties of SiC power switches.

The need for advanced driving techniques in SiC power switches is further underscored by the increasing demand for high-power density and high-efficiency systems. In applications such as electric vehicles, for example, power electronic systems must be able to handle high currents and voltages while minimizing energy losses and heat generation. SiC power switches, with their superior performance characteristics, are well-suited for these applications, but their full potential can only be realized with the use of advanced driving techniques. The development of advanced driving techniques for SiC power switches is an active area of research, with many scientists and engineers exploring new methods and technologies to optimize the performance of these devices [19] [20] [21] [22].

This dissertation presents a novel methodology for driving SiC power switches utilizing a current source gate driver. The concept and implementation of the gate driver are initially introduced, followed by a comprehensive examination

of the experimental results. Two distinct driving strategies have been identified and investigated: single-level current source driving and multi-level current source driving. The experimental results are then analyzed to evaluate the performance of these driving strategies, with a particular focus on their impact on switching losses and EMI. Additionally, a software tool for EMI analysis has been developed to assess the electromagnetic emissions of the driving strategies, providing a comprehensive understanding of their effects on the overall system performance.

The subsequent sections of this chapter primarily focus on the turn-on transition, as it is the dominant contributor to both switching losses and EMI. A detailed analysis of the experimental results and their implications for power electronic design is presented, with a particular emphasis on the benefits and challenges associated with the proposed driving strategies.

3.1 Gate Shaping Demonstrator

A custom-designed current source gate driver was developed to overcome the limitations of commercial gate drivers, which are typically based on voltage source architectures and lack the flexibility to modify voltage or current levels during switching events. The concept representation of this device is provided in Figure 3.1. The bespoke gate driver was constructed using discrete components,

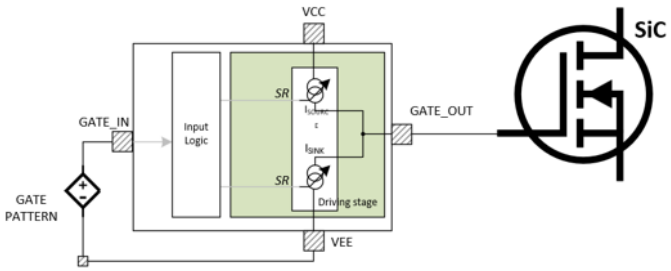


Figure 3.1: Current source gate driver concept

with its core functionality provided by two current mirrors: one for sourcing current to the gate of the SiC MOSFET (Figure 3.2), and one for sinking current from the gate (Figure 3.3). These current mirrors were implemented using bipolar junction transistors (BJTs) in a four-transistor Wilson configuration while the output stage has been implemented with two BJTs in parallel to provide a current gain $\frac{I_{OUT}}{I_{REF}}$ equal to 2.

The current mirror for sourcing current to the SiC gate has been implemented by PNP BJTs while the current mirror for sinking current has been implemented using NPN BJTs. The sink branch is characterized by an additional mirror based on PNP BJTs serving as a level-shifter. Indeed, the reference current for both current mirrors is created using a BJT in an emitter follower configuration, which enables the generation of a current signal by applying a

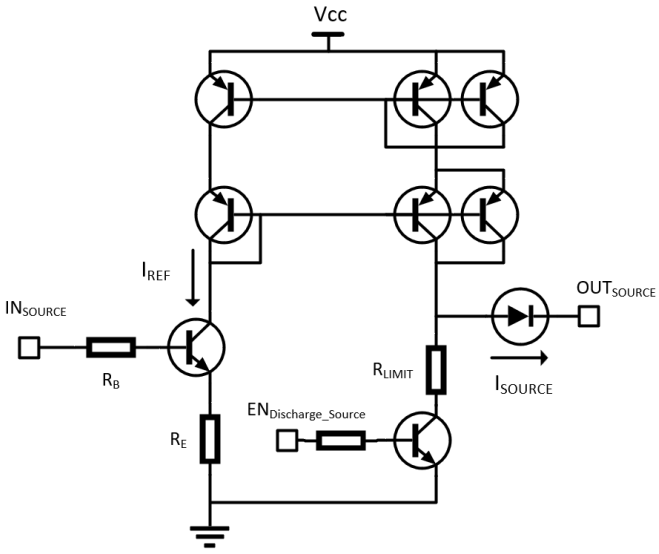


Figure 3.2: Current Mirror Source Stage

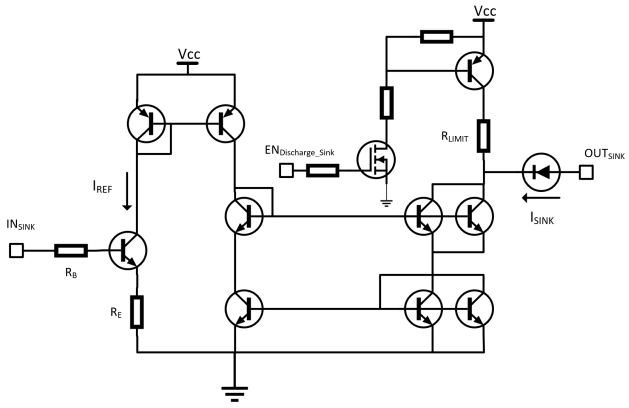


Figure 3.3: Current Mirror Sink Stage

voltage signal to the base of the emitter follower BJT according to Equation 3.1. An arbitrary function generator can be used to apply an arbitrary signal to the base of the emitter follower, allowing for the implementation of complex driving strategies. Eventually, the BJT in emitter follower configuration plays a crucial role in determining the dynamic performance of the entire source and sink structure. For this purpose, a NPN BJT with high current gain bandwidth product has been selected [23].

$$i_C = \frac{(V_{IN} - V_{BE})\beta}{R_B + R_E(\beta + 1)} \tag{3.1}$$

The two BJTs in parallel in the output stage allow to reduce the overall current consumption and the dissipation is spread across two devices in parallel reducing the stress on the single device. Furthermore, the Wilson configuration provides an output resistance that is 0.5β time higher than the output resistance of the single BJT (Equation 3.2); this is essential for maintaining a stable gate voltage and minimizing the dependency of the output current on the output voltage.

$$R_O = \beta r_O/2 \tag{3.2}$$

Furthermore, the four transistors connection allows to reduce the process error of the BJTs on the input to output current ratio.

To achieve the correct operation, additional circuitry was incorporated into the gate driver design. Specifically, two dedicated circuits were implemented to enhance the performance of the mirror output stage. These circuits serve to remove minority carriers from the output stage, thereby preventing cross-conduction between the sink and source branches. These two circuit are implemented respectively with a NPN BJT for the source stage and with a PNP BJT for the sink stage; a current limiting resistor (R_{LIMIT}) is included to avoid excessive stress on the switches. These two circuits are activated during the dead time between the source and the sink branch operation according to Figure 3.4. Logic ports were employed to synchronize the various sub-circuits with the input signals, ensuring coordinated operation and optimal performance of the gate driver.

Compared to existing solutions [19] [20] [21] [22], the proposed approach offers a simpler implementation, relying solely on analog components and avoiding the need for digital signal processing (DSP) or field-programmable gate array (FPGA) technology. However, its suitability for practical applications is limited, making it less viable for real-world implementation. Nevertheless, the bespoke gate driver provides a unique platform for investigating the benefits and challenges of current source driving in power electronic applications, enabling the exploration of complex driving strategies and their effects on SiC MOSFET performance.

Consequently, the proposed solution has been primarily employed for double-pulse testing (DPT), where its simplicity and analog nature provide a suitable framework for experimental evaluation.

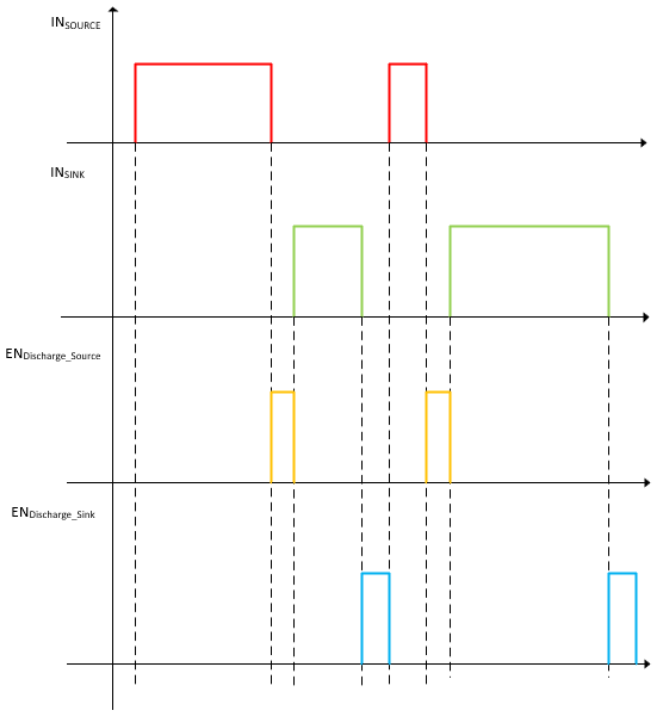


Figure 3.4: Timing of the demonstrator sub-circuits

The actual implementation of the gate driver is illustrated in Figure 3.5 , which provides a detailed visualization of the proposed approach.

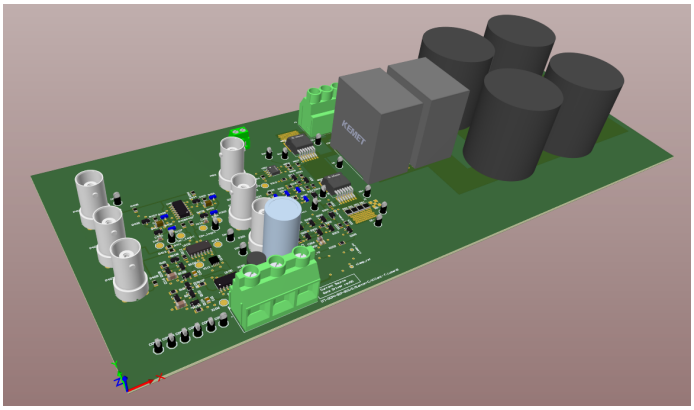


Figure 3.5: Gate Shaping demonstrator board

The gate driver design underwent an initial development phase, where it was created, optimized, and thoroughly tested in a Simulation Program with Integrated Circuit Emphasis (SPICE) environment. This simulation-based approach enabled the refinement of the design and the verification of its performance prior to physical implementation.

Following the successful simulation and optimization, a demonstrator was fabricated to validate the design in a practical setting. The demonstrator was constructed on a 1.6 mm thick FR4 substrate, which was configured with a four-layer stack-up.

The printed circuit board (PCB) assembly features a half-bridge (HB) configuration with two SiC MOSFETs, as well as electrolytic and film capacitors for the high-voltage supply and a ceramic snubber capacitor. The current source gate driver is connected to the low-side SiC MOSFET, while the high-side switch is driven by a standard single-channel isolated gate driver [24]. The SiC MOSFET used in this experiment is a 1200 V CoolSiC^{TM} Gen2 MOSFET with an on-resistance ($R_{DS_{ON}}$) of 40 mohm [25].

To minimize the effects of the inductive DC bus capacitor bank, a snubber capacitor was incorporated into the design as represented in Figure 3.6. The snubber capacitor dynamically decouples the commutation loop from the DC bus capacitor bank constituted by the electrolytic and film capacitors. This capacitor bank is essential for achieving the required capacitance value to sustain the test, however it introduces stray inductance that would be part of the commutation loop in case the ceramic snubber is not employed. By using a snubber capacitor, the commutation loop's stray inductance is significantly reduced, measuring 18.3 nH, compared to 37.5 nH without the snubber. The mitigation of the parasitic inductance on the commutation loop enables a more accurate assessment of the current source gate driver's performance.

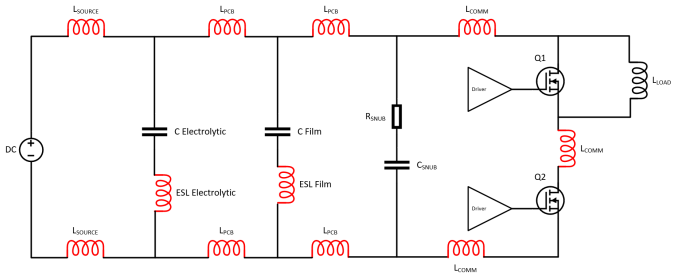


Figure 3.6: Schematic representation of PCB components and connections, components in red are parasitic

This physical implementation allowed for the experimental evaluation of the gate driver's performance and the assessment of its feasibility in a real-world context.

3.2 Single Level Current Source Results

The single-level current source driving approach is characterized by its simplicity of implementation and enables open-loop control of the voltage slew rate, rendering it independent of the load current. This feature yields a significant reduction in switching losses. With this driving method, a constant current (I_G) is injected into the gate of the power switch during the turn on transition as shown in Figure 3.7.

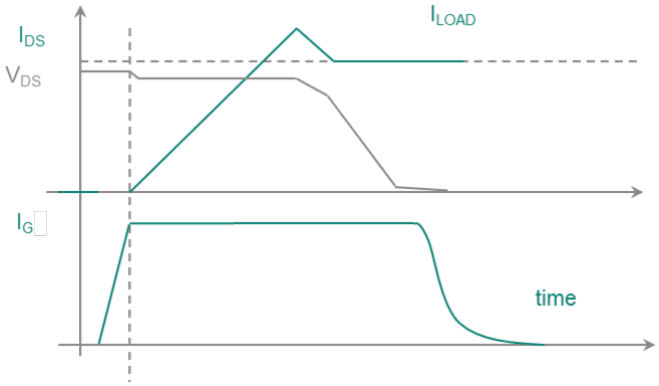


Figure 3.7: Single Level Current Source Waveforms

The current source approach has been tested doing a DP test for current values from 5% up to the 100% of the nominal current of the power switch. The nominal current for the select SiC MOSFET is 20 A. In particular, the DP test has been executed under the following conditions:

- $DCBUS = 800$ V;
- $V_{CC} = 20$ V;
- $I_G = 100, 200, 400$ mA.

Although the SiC MOSFET used in this experiment is rated for 1200 V, the DC bus voltage was intentionally limited to 800 V to provide a safety margin against potential voltage overshoots and prevent device breakdown.

The gate driver supply voltage (V_{CC}) was set to 20 V to compensate for the voltage drop across the current mirror and ensure a minimum gate-to-source voltage (V_{GS}) of 18 V at steady state.

The voltage slew rate (dv/dt) was measured for each current value, and the results are presented in Figure 3.8. This parameter was measured between the 80% and 20% points of the falling edge of the drain-to-source voltage of the device under test. The voltage slew rate is defined as the rate of change of the voltage with respect to time, and it is calculated as follows:

$$\frac{dv}{dt}80\% - 20\% = \frac{0.8 \times DCBUS - 0.2 \times DCBUS}{t_{80\%} - t_{20\%}} \tag{3.3}$$

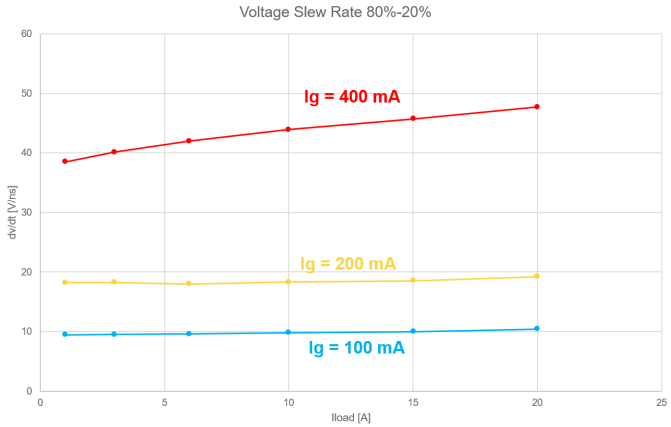


Figure 3.8: Slew rate value as function of the load current for different gate current values with snubber capacitance

Observations reveal that when the gate current I_G is set to 100 mA and 200 mA, the respective slew rates are approximately 10 V/ns and 18.5 V/ns. Notably, under these conditions, the slew rate remains independent of the load current. However, when the gate current is increased to 400 mA, a different behavior is observed, where the slew rate exhibits a dependence on the load current, increasing as the load current increases.

The observed behavior can be attributed to two primary factors:

- the reverse recovery charge of the complementary switch (Q1 in Figure 3.6);

- the parasitic elements present in the commutation loop.

A comparative analysis was conducted between the proposed driving solution and a conventional voltage source gate driver solution, which utilizes a gate resistance (Rg) between the driver output and the power switch gate to regulate the switching speed. The Rg values were selected to match the voltage slew rate achieved with the current-source gate driving approach at low load current. This sizing strategy is commonly adopted in slew rate sensitive applications, such as motor drives. To ensure a fair comparison, a dedicated PCB was designed for the voltage source driving method, featuring identical parasitic components. As illustrated in Figure 3.9, the current source solution exhibits a more consistent slew rate compared to the standard driving method. This nearly constant switching speed results in a reduction of turn-on losses of up to 17 %, as demonstrated in Figure 3.10.

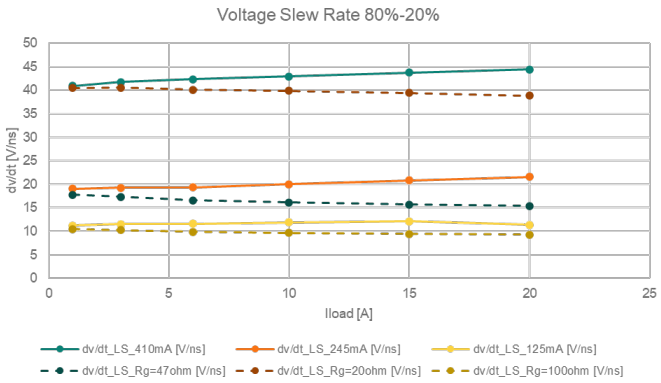


Figure 3.9: Slew rate value for current source (continuous lines) and voltage source driving methods (dotted lines), both with snubber capacitor

3.2.1 Effect of Reverse Recovery Charge and Parasitic on Single Level Current Source

The configuration depicted in Figure 3.5 features a snubber capacitor located at the bottom of the PCB. This ceramic capacitor serves as a dynamic shield, mitigating the effects of parasitic elements on the board and the capacitor bank, thereby providing a low-inductance commutation loop for the half-bridge under evaluation. However, when the snubber capacitor is removed, its shielding effect is lost, and the stray capacitance of the PCB tracks connecting the half-bridge to the electrolytic capacitor, as well as the electrolytic capacitors themselves, become integral to the commutation loop as depicted in Figure 3.11. As a result, the removal of the snubber capacitor causes the commutation loop inductance to increase significantly, from 18.3 nH to 37.5 nH. Figure 3.12 illustrates that, in the absence of a snubber capacitor, the single-level current source is unable

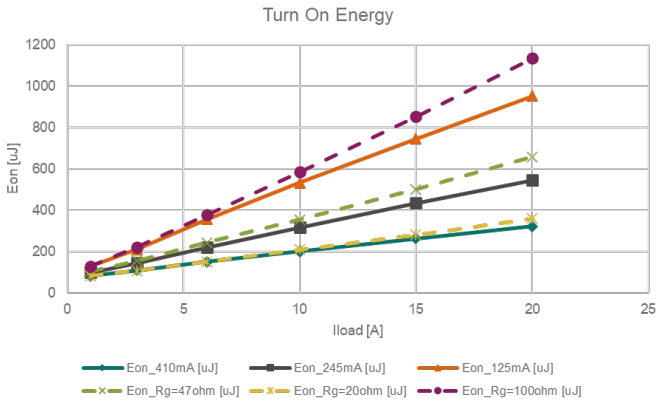


Figure 3.10: Turn on energy value for current source and voltage source driving methods, both with snubber capacitor

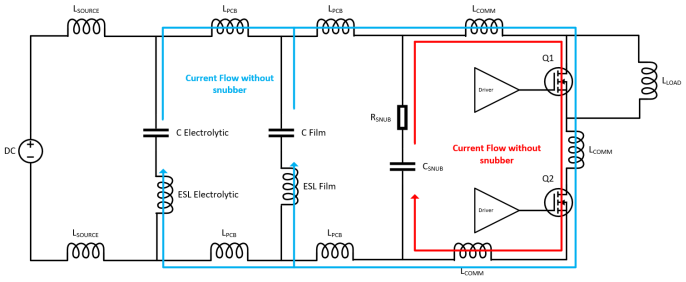


Figure 3.11: Current path with (red line) and without (blue line) snubber capacitor

to maintain control over the slew rate, particularly at high switching speeds and high load current values. During the reverse recovery of the complemen-

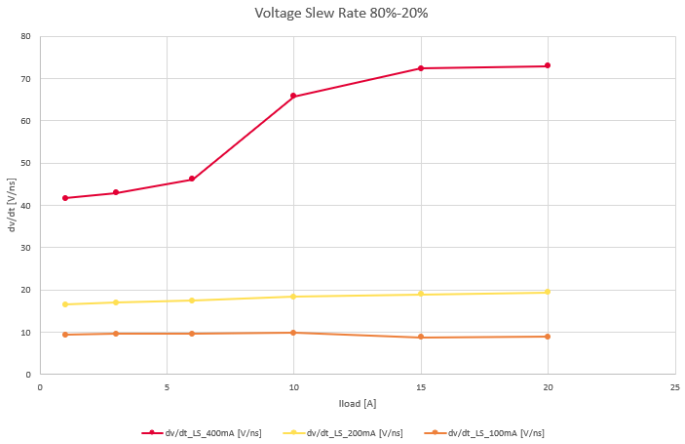


Figure 3.12: dv/dt behavior without snubber

tary switch, a supplementary current, resulting from plasma removal and space charge formation, flows through the low-side switch that is turning on. At this stage, the low-side switch operates in the linear region, where the drain current (i_D) is directly proportional to the drain-source voltage (V_{DS}), as described by the relationship $i_D = g_M v_{DS}$. The additional current generated by the reverse recovery process causes an increase in the gate voltage. However, as the complementary switch begins to block voltage, the drain current of the switch under test starts to decrease, and consequently, the gate-source voltage (V_{GS}) must also decrease in accordance with the aforementioned relationship. As a result, a portion of the charge stored in the gate-source capacitance (C_{GS}) of the SiC MOSFET flows through the gate-drain capacitance (C_{GD}), causing the voltage slew rate (dv/dt) to be steeper than expected until the negative di/dt phase of the reverse recovery peak is completed. This phenomenon is exacerbated by the current source nature of the gate driver, whereas it is partially alleviated by the Rg driving method, as illustrated by Equation 3.4 and Equation 3.5.

$$CurrentSourceDriving : i_{GD} = I_G - \frac{C_{GS}}{g_M}\frac{di_D}{dt} \tag{3.4}$$

$$R_G driving : i_{GD} = \frac{V_{CC} - (\frac{i_D}{g_M} + V_{th})}{R_G} - \frac{C_{GS}}{g_M}\frac{di_D}{dt} \tag{3.5}$$

where:

- i_{GD} is the gate current injected in the C_{GD} capacitance;
- I_G is the current provided by the current source gate driver;
- C_{GS} is the gate to source capacitance of the power switch;

- g_M is the trasconductance of the power switch;
- di_D/dt is the slope of the power switch drain current during the falling edge of the reverse recovery peak;
- R_G is the gate resistance employed in the Rg driving method.

An examination of Equation 3.4 reveals that, during the negative di/dt phase of the reverse recovery current, the term di_D/dt becomes negative, and the second term of the equation adds to the current provided by the gate driver (I_G), resulting in $i_{GD} > I_G$. In contrast, Equation 3.5 shows that the Miller plateau increase (described in the first part of the equation) acts as a negative feedback mechanism, reducing the current provided by the gate driver and thereby limiting the increase in voltage slew rate during the falling edge of the reverse recovery current.

Moreover, this effect becomes more pronounced when the commutation loop inductance is higher. The increase in parasitic inductance in the commutation loop causes the negative di/dt phase of the recovery peak to slow down, as evident from the experimental results presented in Figure 3.13 and Figure 3.14. This phenomenon highlights the impact of commutation loop inductance on the reverse recovery current and the subsequent effect on the voltage slew rate.

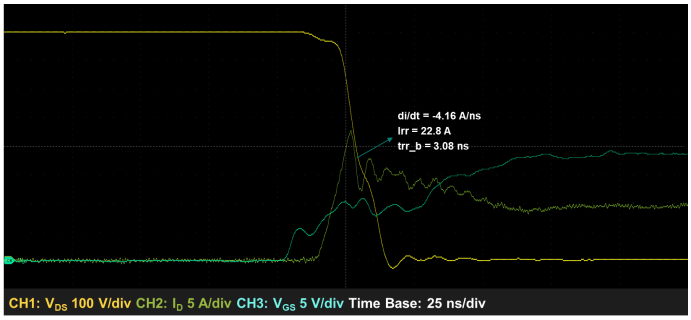


Figure 3.13: Falling edge of the reverse recovery peak with snubber

When the absolute value of the negative di/dt decreases, the drain current requires a longer time to stabilize at the load current value. As a consequence, the current flowing through the C_{GD} capacitance remains higher than the value imposed by the gate driver for an extended period, resulting in the steeper portion of the dv/dt lasting for a larger fraction of the commutation event. This, in turn, causes the average dv/dt measured between 80 % and 20 % to be higher than anticipated.

These findings indicate that a low commutation loop inductance, combined with a reduced reverse recovery charge, is essential to fully leverage the benefits of the single-level current source gate driver.

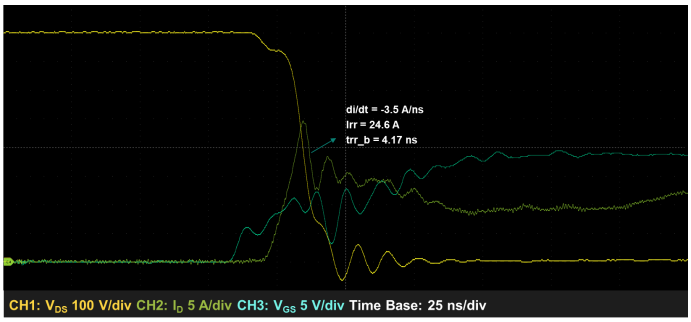


Figure 3.14: Falling edge of the reverse recovery peak without snubber

3.2.2 Single Level Current Source Gate Driver with IGBTs

In addition to its evaluation with SiC MOSFETs, the single-level current source gate driver has also been tested with the 1200V IGBT7 S7 from Infineon Technologies [26]. To facilitate this testing, the hardware setup illustrated in Fig 3.5 was modified to accommodate the 40 A, 1200 V IGBT device in a TO-247 package. The DP test has been executed under the following conditions:

- $DCBUS = 800$ V;
- $V_{CC} = 17$ V;
- $I_G = 460$ mA.

The load current was incrementally increased from 2 A to 30 A, although it was not possible to reach the nominal current of the power switch due to limitations inherent to the setup. The performance of the current source gate driver was then compared to that of the Rg driving method, with the results of this comparison being presented in Figure 3.15 and Figure 3.16. The results indicate that the single-level current source driving method enables a dv/dt that is less sensitive to load current, particularly at high load currents, resulting in a reduction of turn-on losses of up to 17 %. Furthermore, an additional test was conducted with a gate current (I_G) of 230 mA, as shown in Figure 3.17. Although the dv/dt is less flat compared to the results obtained with SiC MOSFETs, this test demonstrates that the single-level current source driving method still allows for configuring the slew rate by adjusting the gate current value.

3.3 Multi Level Current Source Driving

The multi-level current source driving technique is founded on the concept of modulating the current injected into the gate of the power switch during the turn-on commutation event, as illustrated in Figure 3.18. This approach enables the simultaneous optimization of both EMI and power switch losses. However,

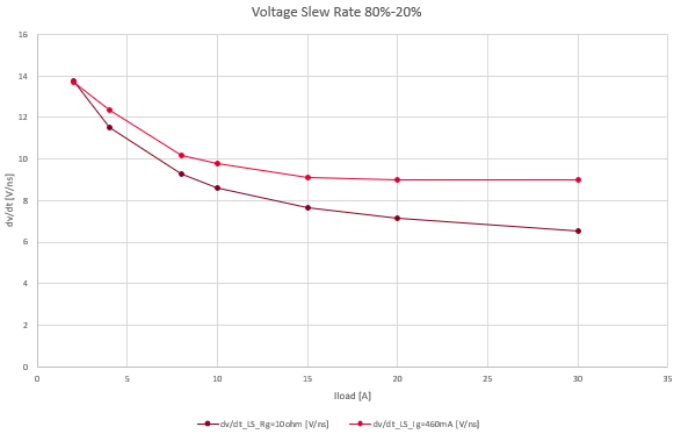


Figure 3.15: dv/dt behavior with IGBT7 S7

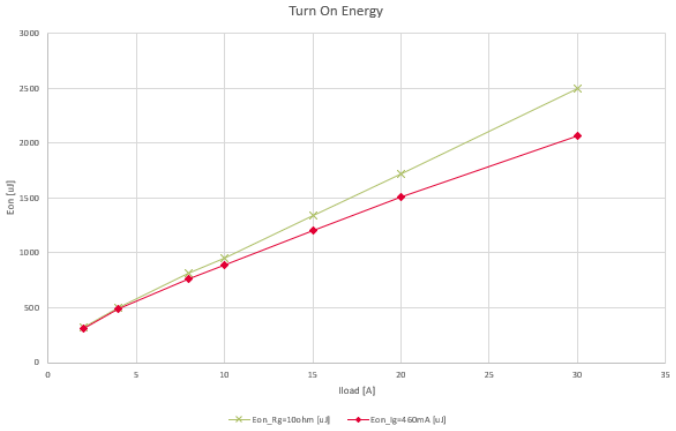


Figure 3.16: Turn On Energy with IGBT7 S7

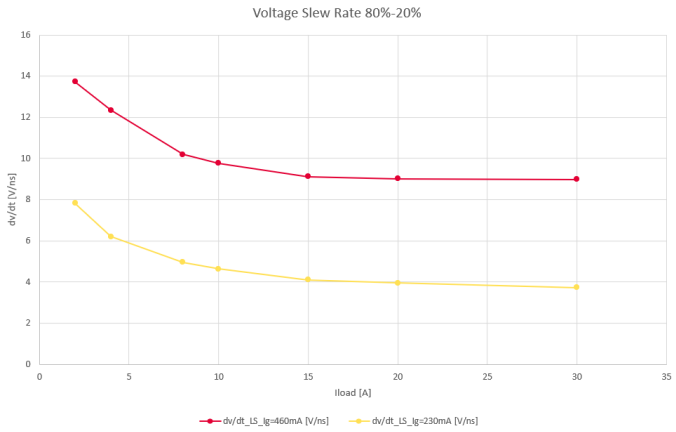


Figure 3.17: dv/dt behavior for different gate current values

its implementation necessitates a more sophisticated control strategy, as the variation in gate current level must be achieved with a high temporal resolution, on the order of nanoseconds. Although the proposed gate driver demonstrator

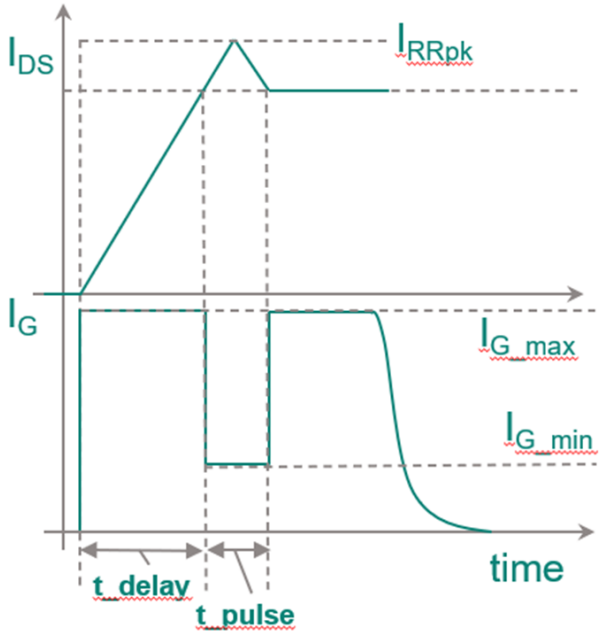


Figure 3.18: Multi level current pattern

is capable of producing any gate signal, the gate current pattern presented

in Figure 3.18 is considered a favorable compromise between complexity and effectiveness. This conclusion is also supported by other researchers, as reported in [27] and [28].

The underlying principle of this driving strategy is to locally decrease the rate of change of the drain current (di/dt) immediately prior to the onset of the reverse recovery phase; the working principle is presented in Figure 3.18.

The rate of change of the SiC MOSFET drain current during the turn-on transition can be described by Equation 3.6, which states:

$$\frac{di_D}{dt} = g_M \frac{i_G}{C_{GS}} \tag{3.6}$$

This equation indicates that the current slew rate can be controlled by adjusting the gate current supplied by the gate driver. As noted by [29], the current slew rate is one of the key parameters, along with forward current, reverse blocking voltage, and junction temperature, that determines the amplitude of the reverse recovery peak. Additionally, experimental results have shown that the reverse recovery amplitude is primarily influenced by the di/dt magnitude near the beginning of the reverse recovery phase. Therefore, it is possible to optimize the switching performance by maximizing the di/dt at the start of the transition to reduce switching losses, then reducing the gate current at the appropriate time near the reverse recovery event to minimize the reverse recovery peak, and finally increasing the gate current again to maximize the dv/dt phase and minimize switching losses.

By applying the gate current pattern presented in Figure 3.18, it is possible to obtain three beneficial outcomes:

- reduce the EMI generation due to the reduction of the reverse recovery peak (Irr) [30];
- improve the slew rate controllability;
- reduce the turn on losses.

In particular, it becomes possible to establish a novel transfer function between the reverse recovery current (I_{RR}) and the turn-on energy (E_{ON}), which is situated below the typical transfer function obtained using a single-level current source driving approach. This implies that the proposed driving strategy enables the creation of a new Pareto front for the I_{RR}-E_{ON} trade-off, offering an improved balance between these two critical parameters.

3.3.1 Gate Current Pattern Optimization

The proposed driving solution exhibits high sensitivity to three primary parameters, as illustrated in Figure 3.18:

- I_{Gmin} amplitude;
- delay time before starting reducing the current, t_{delay};

- length of the pulse, t_{pulse}.

To determine the optimal combination of the three aforementioned parameters, a genetic multi-objective algorithm based on differential evolution was utilized in a SPICE simulation environment. The outcomes of this optimization process are presented in Figure 3.19, which illustrates the resulting Pareto front. The

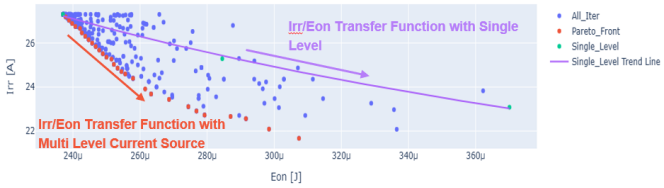


Figure 3.19: Optimization algorithm results

points that comprise the Pareto front are characterized by a delay time (t_{delay}) ranging from 32 ns to 35 ns and a pulse duration (t_{pulse}) ranging from 1 ns to 9 ns. Notably, the solutions that form the Pareto front are distributed according to their t_{pulse} values, with this parameter increasing as the reverse recovery current (Irr) decreases and the turn-on energy (Eon) increases. This relationship can be attributed to the fact that a longer t_{pulse} results in a lower di/dt, which in turn reduces Irr, but also decreases the voltage slew rate, leading to an increase in Eon. In contrast, the t_{delay} parameter remains relatively stable, as the test was conducted at a single load current value, and the rise time of the current, which marks the start of the reverse recovery phase, remains nearly constant. The points that comprise the Pareto front are distinguished by I_{Gmin} of 0 A. This characteristic enables the achievement of maximum I_{RR} reduction without requiring prolonged t_{pulse} values, which could potentially have a negative impact on the E_{ON} values.

The optimization process also reveals that an incorrect combination of timing parameters can lead to a degraded system response, resulting in increased I_{RR} and turn-on losses.

A comparative analysis was conducted from an electromagnetic interference perspective, focusing on two points with identical E_{ON} values. This comparison was facilitated by a specialized software tool, which was developed to assess EMI characteristics based on double-pulse events. As illustrated in Figure 3.20, the results indicate that the multi-level current source driving method yields a significant reduction of approximately 60 % in the EMI peak at 65 MHz, compared to the alternative approach.

However, generating timings with nanosecond-scale precision is a challenging task with current integrated technologies; while the feasibility has been demonstrated [27] [28], the complexity and anticipated high cost of the proposed solutions render them impractical for implementation in real-world applications. Furthermore, it is still unclear which parameters need to be monitored to accurately calculate these timings in real-world application conditions. The devel-

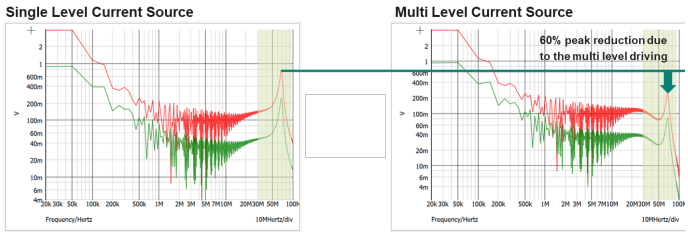


Figure 3.20: EMI comparison between single level and multi level current source driving

opment and implementation of this driving method are the subject of ongoing research at Infineon Technologies.

3.3.2 Multi Level Current Source Experimental Validation

The multi-level current source driving technique was experimentally evaluated using the Gate Shaping demonstrator, with the gate current pattern illustrated in Figure 3.18 applied to the same SiC MOSFET that was previously used to test the single-level current source driving. The multi-level current source driving was tested under the following specific conditions:

- $DCBUS = 800$ V;
- $V_{CC} = 20$ V;
- $I_{Gmax} = 400$ mA;
- $I_D = 15$ A.

The results of the experimental characterization are reported in Figure 3.21.

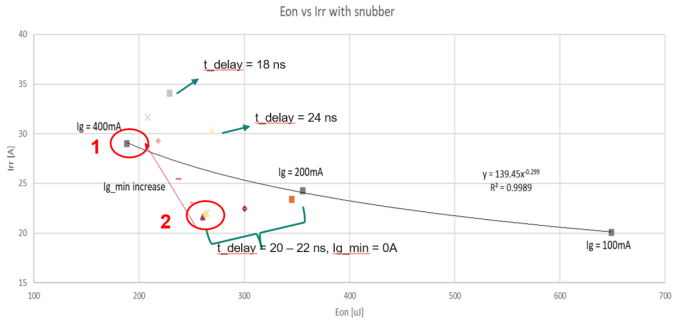
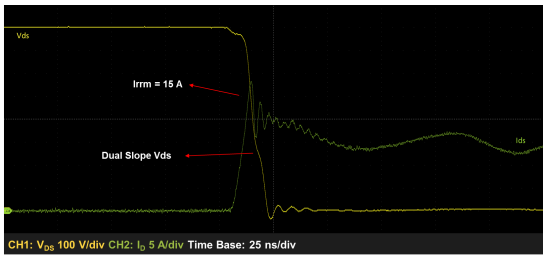


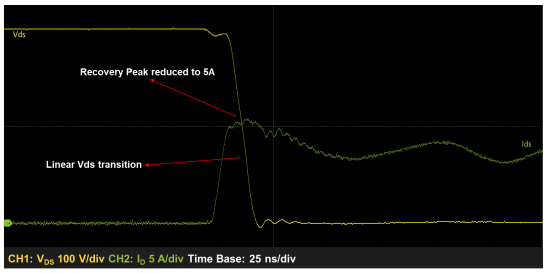
Figure 3.21: Multi Level Current Source Experimental Results

The experimental results are in agreement with the outcomes of the optimization algorithm, indicating that the optimal delay time (t_{delay}) falls within the range of 20-22 ns. Notably, even minor deviations from this optimal range, such as $t_{delay} = 18$ ns or $t_{delay} = 24$ ns, result in a significant degradation of the driving method's performance. In contrast, the pulse duration (t_{pulse}) has a negligible impact on the driving performance, as different measurements with varying t_{pulse} values yield overlapping results. In a similar manner to the optimization results presented in the preceding paragraph, the optimal balance between turn-on energy and reverse recovery current was achieved when the I_{Gmin} was set to 0 A.

The impact of this driving method on the switching waveforms is illustrated in Figure 3.22a and Figure 3.22b. A comparison of the two figures reveals that, with multi-level approach, the recovery peak is reduced by 8 A, and the V_{DS} waveform exhibits a linear transition, devoid of the double slope characteristic of the single-level current source driving method. As mentioned in the single level current source paragraph, this double slope can potentially lead to an uncontrolled dv/dt if the commutation loop inductance is not optimized, highlighting the benefits of the multi-level current source driving approach.



(a)



(b)

Figure 3.22: Switching waveform for single level current source (a) and for multi level current source (b)

3.3.3 EMI Analysis Tool

A simulation tool has been developed to quantify the effects of parasitic on conducted EMI. It is based on a SPICE simulator, incorporating all the primary components of a real power conversion system. Specifically, the model includes the following parameters: package parasitic (resistive, inductive, and capacitive components), gate driver model, PCB parasitic, DCBUS capacitor bank with its associated equivalent series resistance (ESR) and equivalent series inductance (ESL), and the line impedance stabilization network (LISN) model. A half-bridge configuration has been simulated, and the various components of the model are depicted in Figure 3.23.

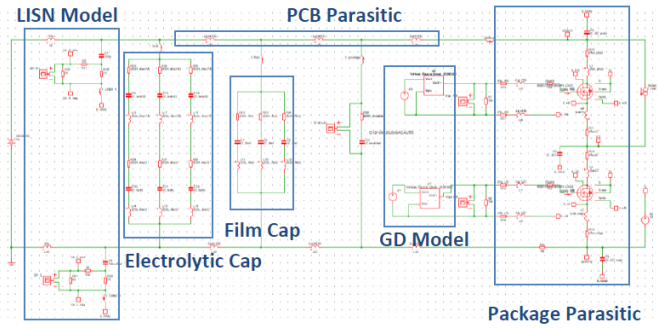


Figure 3.23: Power conversion system schematic representation

A complete pulse-width modulation (PWM) cycle, including both the turn-on and turn-off transitions, has been simulated to estimate the conducted EMI associated with the selected package. The signal induced by the commutation events on the LISN has been analyzed in the frequency domain, and the EMI has been quantified with a single number representing the total power dissipation on the LISN itself [31] over a certain frequency spectrum. The total EMI power is calculated using Equation 3.7:

$$TotalEMIPower = \frac{\sum_{i=150kHz}^{100MHz} V_{iLISN}^2}{R_{LISN}} \tag{3.7}$$

As indicated in Equation 3.7, the total EMI power is considered within the frequency range from 150 kHz to 100 MHz. According to current regulations, the range of interest for conducted emissions is from 150 kHz to 30 MHz [32]; however, the relevant frequencies have been extended to 100 MHz to include the frequency range of the reverse recovery current peak [30]. The main advantage of this simulation method is the ability to quantify the electromagnetic interference caused by the commutation of power switches with a single number. This tool is neither intended to replace an EMI compliance test nor to provide a real EMI value, but it enables an easy and rapid comparisons between different package platforms, power switch technologies and driving speeds that can be used to optimize the system design.

3.4 Gate Shaping Conclusion

In summary, this chapter has presented a comprehensive exploration of Gate Shaping techniques for SiC power switches, focusing on the development and experimental validation of both single-level and multi-level current source gate drivers. The results demonstrate that the proposed gate driver topologies significantly reduce switching losses and EMI, particularly through the optimization of gate current patterns. The single-level current source approach was shown to maintain consistent voltage slew rates and reduce turn-on losses by up to 17 %, while the multi-level current source technique achieved a notable 60 % reduction in EMI peaks at 65 MHz. Additionally, the implementation of an EMI analysis tool provided a valuable framework for quantifying and comparing the electromagnetic emissions of different driving strategies. Despite these advancements, challenges remain, particularly in achieving nanosecond-scale timing precision and integrating these methods into practical applications. Nevertheless, the findings underscore the potential of current source gate driving as a key enabler for unlocking the full performance of SiC power switches in high-power density and high-efficiency systems. Future research should focus on addressing the implementation complexities and further optimizing these driving techniques to meet the demands of real-world applications.

Chapter 4

Conclusion and Future Work

This dissertation investigated innovative gate-driving techniques and device-level advancements aimed at minimizing switching losses, enhancing electromagnetic compatibility (EMI), and optimizing the efficiency of power electronic systems. The research focused on three primary areas:

1. the development of a current-source gate-driver methodology tailored for silicon carbide (SiC) power switches;
2. the integration of an on-silicon capacitance within a module, leveraging the characteristics of low gate energy power switches;
3. the design and characterization of a specialized gate-driver architecture for a new generation of insulated gate bipolar transistors (IGBTs).

4.1 Low Gate-Energy Power Switches

Chapter 2 begins by exploring the advantages and challenges of utilizing low gate energy power switches. The discussion then proceeds to the integration of a bootstrap on-silicon capacitance within a QFN module, which utilizes 600 V CoolMOS^{TM} power switches and a SOI gate driver. The chapter provides an in-depth examination of the power supply foundation for a level-shifter gate driver system and validates the assembly's performance under realistic operating conditions.

The second part of the chapter introduces a new IGBT technology, with a focus on its distinct gate characteristics and the benefits it offers compared to current state-of-the-art IGBTs. A novel gate driver architecture is then presented, along with a detailed definition of the gate driver. To demonstrate its performance and feasibility, the gate driver was experimentally tested in a QFN module, in combination with the newly developed IGBT technology.

4.1.1 Single Supply High Voltage Module

The module features an integrated high-voltage bootstrap network, which supplies the high-side driver in a half bridge topology. A custom gate driver IC layout was designed to provide access to the bootstrap node (V_B) and the switch node (V_S), allowing for accurate observation of the bootstrap behavior during operation.

The bootstrap capacitor is implemented using a 68 nF Infineon silicon capacitor (SilCap), chosen for its temperature stability, low leakage current, and minimal equivalent series resistance (ESR).

An analytical analysis of the bootstrap behavior was conducted, and it was found that the high-side supply voltage V_{BS} can be approximated using compact relations that depend on the current direction. These expressions reveal the primary voltage drops that reduce V_{BS}, including the bootstrap diode forward voltage V_F during positive current conditions and the low-side device's on-resistance drop during negative current conditions. These relations provide a practical foundation for sizing the under-voltage lockout (UVLO) capacitor across various operating points, ensuring reliable operation and efficient design.

The bootstrap network has been characterized across representative operating points to verify design criteria and identify the stress conditions that could trigger UVLO.

To capture the worst-case voltage drop and undervoltage lockout (UVLO) margins, data were recorded at both the beginning and end of the pulse-width modulation (PWM) cycle. The analysis revealed the complex interplay between PWM frequency, load current, temperature, and current polarity in determining the bootstrap headroom and capacitor stress. The measurements confirmed the validity of the closed-form relations presented in (2.4)–(2.5). Notably, the analysis demonstrated that the current bootstrap design is capable of supplying the high-side portion of the gate driver under the specified design conditions. Additionally, the design was found to function correctly even when the PWM frequency was reduced to half of the design frequency, although the power switches were no longer fully enhanced.

The bootstrap circuit was further tested in a motor drive application, and its performance was compared to the standard approach of connecting a multilayer ceramic capacitor (MLCC) at the module terminal. A thermal analysis of the devices revealed that there is no discernible difference between the integrated solution and the standard approach, indicating that the integrated solution supplies the high side of the gate driver with equivalent performance to an external MLCC capacitor.

4.1.2 Low Gate Energy IGBT

A new technology has been developed, known as the low gate energy IGBT, which is distinguished by a nominal gate voltage of 1.5 V and a typical threshold voltage of 0.5 V. These unique characteristics necessitate a specialized gate architecture and a close proximity between the gate driver IC and the IGBT

die. To address this requirement, a novel gate driver with a new output stage architecture has been designed and integrated alongside the low gate energy IGBT within a QFN package.

The low gate energy IGBT offers significant advantages in terms of conduction and switching losses, which are presented in detail. The new gate driver was initially characterized in a standalone configuration, and the results confirmed that it meets the required specifications. Once its standalone functionality was verified, the characterization was extended to the module level, with a primary focus on the dynamic performance of the device.

The characterization results demonstrate that the gate driver is capable of correctly turning on and off the low gate energy IGBT. Additionally, it was found that the turn-off losses decrease as the turn-off impedance increases, which may seem counterintuitive but is consistent with the specific design of this IGBT. However, turn-off instabilities were observed in some devices, particularly at high junction temperatures. Further investigation revealed that these instabilities are related to the IGBT fabrication process. As the low gate energy IGBT is still a relatively new technology, process improvements are necessary to make it suitable for mass production.

4.2 Gate Shaping

Chapter 3 presents the development of current-source gate-driving techniques for silicon carbide (SiC) power switches, encompassing both single-level and multi-level gate current shaping methods. These techniques are enriched with a comprehensive electromagnetic interference (EMI) analysis using a dedicated framework, which takes into account the realistic package and printed circuit board (PCB) parasitics present in a half-bridge configuration. The primary objectives of this work are to minimize switching losses, improve the controllability of the drain current and voltage slew rates (di/dt and dv/dt), and optimize the trade-off between EMI and switching losses.

A custom-designed current-source driver was implemented to deliver the prescribed currents to the gate of the power switch. The driver employed a four-transistor Wilson configuration to minimize process-induced errors in the input-to-output current ratio, enabling both constant-current (single-level) and time-sequenced (multi-level) gate current profiles. This architecture provided fine control over the gate charge trajectory during the most sensitive switching intervals. The reference current was generated using a NPN BJT in an emitter follower configuration, which was selected for its high current gain-bandwidth product to ensure high dynamic performance.

The single-level current source driver demonstrated improved slew rate controllability, resulting in a turn-on energy reduction of approximately 17 % at the nominal current. However, at high slew rate values, the regulation partially lost its effectiveness, and the dv/dt increased with the load current. A detailed analysis of the waveforms revealed that this behavior was related to the reverse recovery characteristics and the commutation loop inductance.

This chapter provides a comprehensive analysis of how reverse recovery charge and loop inductance influence the turn-on energy and slew rate behavior, both with and without snubbers. The results show that a suitably designed snubber can effectively limit the increase in voltage slew rate during the falling edge of the reverse recovery current.

Furthermore, the single-level current source driving method was also tested with IGBTs, resulting in a turn-on energy reduction of around 16 % and a flatter dv/dt with respect to the load current. This demonstrates the versatility and effectiveness of the single-level current source driving approach in reducing switching losses and improving slew rate controllability in various power switch technologies.

A more complex multi-level gate-current pattern was subsequently introduced, with the aim of achieving three primary objectives:

- reducing electromagnetic interference (EMI) generation by minimizing the reverse-recovery peak current (I_{rr});
- improving slew-rate controllability;
- decreasing turn-on losses.

This advanced driving method was first analyzed through simulations and then experimentally tested using the same demonstrator that was implemented for the single-level current source gate driver.

The results of this study highlight that the effectiveness of this driving solution is highly sensitive to three key parameters (Figure 3.18:

- the amplitude of the minimum gate current (I_{Gmin});
- the delay time before reducing the current (t_{delay});
- the length of the initial pulse (t_{pulse}).

An optimization study revealed that setting I_{Gmin} to 0 A can provide a favorable balance between turn-on energy and reverse-recovery current under the tested conditions. However, it is essential to carefully tune t_{delay} and t_{pulse} to avoid performance and EMI penalties across different operating points.

The chapter also notes that generating timings with nanosecond-scale precision on silicon is a challenging task. While it is technically feasible, the high complexity and cost currently limit its practicality. Furthermore, it remains unclear which real-time observables are most informative for determining these timings in actual applications. As a result, related developments are ongoing topics of industrial research.

To connect gate-current shaping with system-level noise, a PSpice-based EMI analysis environment models a half-bridge including device/package parasitics, PCB ESL, the DC-link capacitor bank (with ESR/ESL), and an LISN model. Conducted EMI is collapsed to a single figure of merit by integrating the LISN power across the 150 kHz – 100 MHz band:

$$TotalEMIPower = \frac{\sum_{i=150kHz}^{100MHz} V_{iLISN}^2}{R_{LISN}} \tag{4.1}$$

This metric facilitates consistent comparisons of various snubber configurations, loop inductance values, and gate-current patterns, providing clarity on how passive networks and active gate control collectively influence conducted electromagnetic interference (EMI).

The combined experimental and modeling results demonstrate that current-source gate driving, when combined with meticulous management of parasitic elements and the strategic use of snubbers, can effectively reduce switching losses while enhancing control over the rates of change of current (di/dt) and voltage (dv/dt). Furthermore, multi-level gate-current patterns offer additional benefits, but require precise tuning of key parameters, including I_{Gmin}, t_{delay} and t_{pulse}, to ensure robust performance across various operating conditions and device variations.

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