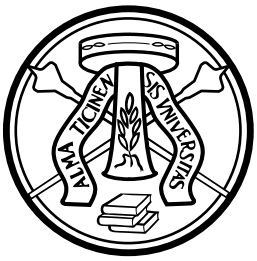

UNIVERSITÀ
DI PAVIA

DEPARTMENT OF ELECTRICAL, COMPUTER AND BIOMEDICAL ENGINEERING

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CYCLE XXXVIII

Generation and Distribution of Low-Jitter Clock Signals for SerDes Applications

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ACADEMIC YEAR 2025/2026

Declaration of Authorship

I, Valentina Marazzi, declare that this thesis titled, "Generation and Distribution of Low-Jitter Clock Signals for SerDes Applications" and the work presented in it are my own. I confirm that:

- This work was done wholly or mainly while in candidature for a research degree at this University.
- Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated.
- Where I have consulted the published work of others, this is always clearly attributed.
- Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work.
- I have acknowledged all main sources of help.
- Where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself.

"Μέγα βιβλίον, μέγα κακόν"
Καλλίμαχος ὁ Κυρηναῖος

Abstract

Generation and Distribution of Low-Jitter Clock Signals for SerDes Applications

by Valentina Marazzi

In the last 20 years, electro-optical communications have been developing more challenging requests, halving specifications on noise and power each year. As any electrical circuit would have efficiency and speed limits, it's crucial to quantify and improve as much as possible such performance in every application. It becomes even more important in SerDes (Serializer-Deserializer) transceivers as they implement the wire enabling people to connect, store and access data, which are everyday activities, necessary for most jobs, errands and leisure. Recently, this need appeared even more evident with the advent of 5G and Internet of Things (IoT). Being clock about half the total power consumption in VLSI chips, it is fundamental to optimize the clock signal generation and distribution. In this thesis, clock in transmitters PLL will be dealt with. In particular, clock distribution becomes a huge design aspect for large chips, whose lengths span from 1 mm to 10 mm. Distribution usually requires half the power consumption and adds up noise as well, thus the focus of this work is to optimize the clock management through a distributed oscillator architecture. The traditional trade-off power-phase noise (PN) is examined and a new solution is proposed through in-phase coupling [1]. This thesis is organised into six parts: first a brief introduction, which will deal with the specific application and the main difference between a stand alone and a distributed oscillator, i.e., the solution proposed in this work, followed by a first chapter about the state of the art by providing an oscillator panoramic and some information about the main oscillators metrics, such as PN and FoM, and their main characteristics. After these introductory parts, further details are provided about coupled oscillators, in particular specifying how the coupling mechanism works and how to deal with coupling main issues, for example FoM penalty and mode stability. First, these issues will be addressed for a simplified dual-core system, then a solution for the same problems is presented for a four-core oscillator. In the third chapter, the proposed architecture is introduced, with a focus on the adopted FinFET technology and some layout information. In the end, the fourth chapter presents the test-chip measurements and the fifth one contains the conclusion.

Contents

Introduction

When dealing with very large scale integration (VLSI) systems, nowadays one of the toughest issues resides in minimizing the power consumption. More in detail, as in a generical VLSI chip about half the power is reserved for clocking architecture [1], [2], the real problem is to optimize the clock power consumption, as shown in Figure 1. Also, a great deal of power is employed by memories and digital elaboration circuitry. Over the years, digital elaboration has become more and more demanding in power and has dictated a technology scaling which does not benefit analog parts at all. Consequently, analog circuits such as clock references need even further attention when it comes to performance.

Clocking architecture addresses all the electronic structures generating and distributing the clock signal in a general chip. As explained in later subsections, generation and distribution may be implemented with the same architecture or with two different circuits. This work proposes a new hybrid topology to solve this traditional trade-off.

In order to understand the range of applications, the specific VLSI systems will be introduced to explain which specifications are required and which are the crucial challenges for the clocking department. In this introduction, there will be a brief overview of the application and the main players in definying the power and noise performance. The final aim is proposing a winning strategy of analysis and design for these two parameters optimisation.

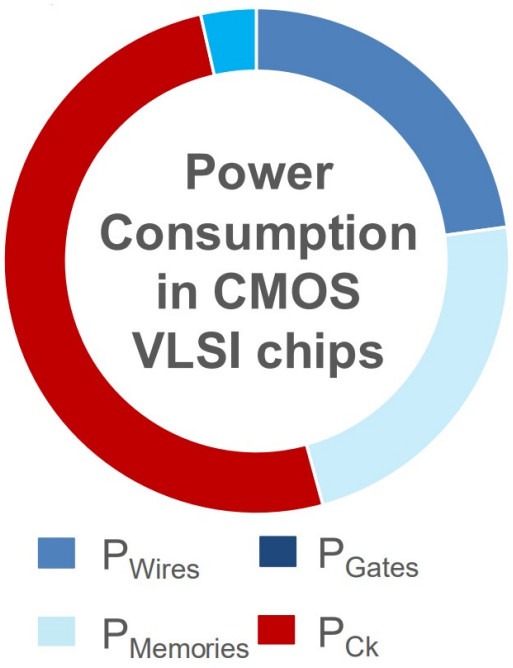

FIGURE 1: Power distribution in VLSI chips.

0.0.1 SerDes high-speed applications

This work revolves around clock generation and distribution for high-speed data transmission, in particular for modern SerDes applications. Serializer-Deserializer (SerDes) structures are employed to minimize the number of I/O interconnections. In particular, in distributed data processing they guarantee the advantage of both the speed of parallel chips connections and the reduced power hungry of serial implementations (Figure 6). As rough explanation, the data to be transmitted are delivered through parallel branches to the serializer, then fed to the transmitter in series. Transmitted data are modulated and sent across the channel, then demodulated and again parallelized through the deserializer block at the receiver [3]. To sum up, SerDes architectures save power and area by reducing the number of pins and leaving just one data path; consequently, they are commonly used for wireless network routers, wireline and optical communications and even for data storage.

Technology scaling and techniques such as bit interleaving and new modulations, for example PAM-4, allowed SerDes to play an important role in enhancing the data-rate speed in the last years. In particular, Figure 8 depicts the trend of the last 20 years. Namely, from 2010s the data-rate has been increasing non-stop, also thanks to the introduction of PAM modulation. In most recent years, a tremendous impulse to boost velocity came from the advent of AI (artificial intelligence). AI both stressed speed and power, as a result nowadays the most rapid networks deployed are at 200Gps per-lane and above [4].

Therefore, data-rate vs jitter requirements have been doubling every year. As there is also a remarkable trade-off for power vs jitter in clocking, the power optimization proposed in this project appears crucial in this context.

To be more specific, from 2020 on AI work loads have been in need of great I/O bandwidths (BW) and data-rates which are more than 50 Gpbs [5], as illustrated in Figure 3. Consequently, necessary BW is limited by increasing signal attenuation and dispersion, thus calling for a PAM 4 modulation which allows from 56 Gpbs to 112 Gpbs links to respect the BW constraints of the channels. Despite PAM 4 modulation weaknesses, such as increased sensitiveness to noise, non-linearities and intersymbol interference (ISI), the advancement is worth the additional complexity. To face the complexity, transceiver design evolved and incorporated more and more digital signal processing (DSP) for better efficiency at the cost of increasing power hunger.

By exploiting the continuous CMOS technology scaling and the ongoing optimization of ADC architectures [6], [7] the DSP power issues are mitigated. The countereffects is that technology scaling favours digital structures at the expense of analog design, whose complexity is exploding. In the last decade, SAR became one of the most adopted ADC architectures thanks to its energy efficiency [5]. As the digital part burns the majority of its power, the capacitors matching must be really precise and, in bigger structures, the mismatches between parallel SAR are to be corrected through digital procedures and calibrations [8]. Both these mechanisms are benefitted by technology scaling. On the other hand, nowadays ISI is mitigated through ophisticated equalizers combined with digital error correction protocols, like FEC -which stands for "forward error correction". This arising complexity will originate trade-offs speed, robustness, power, area and latency [5].

Regarding wireline links, for instance from packaged chips to optical structures, wireline transceivers cover a variety of applications and standards Figure 4. Starting from short connections, like intra-chips and modules-to-chip copper traces on a PCB, the smaller

links go from 0 to few centimeters at most. As these connections present relatively negligible parasitic, they will not be addressed further. A more challenging structure is implemented for XSR/VSR links as they must respect the standards set by optical interworking forum–common electrical I/O (OIF-CEI) definitions and sometimes even Ethernet specs (e.g., attachment unit interface, AUI) [5]. Backplane and midplane connections, called "MR/LR class" are longer copper routes, going from few centimeters up to 1 m. Under the same definition you may find passive cables up to 3 m for rack links. MR/LR class displays considerable losses thus equalization is often added. For instance, a standard like 802.3 Ethernet backplane PHYs may be used as a reference. In order to cover longer distances, like 100-200 m, optical fibers start becoming advantageous, only to become an absoluted necessity for lengths approaching 0.5-10 km. The difference resides in the link complexity as in the first case, for data-center reach, vertical-cavity surface-emitting lasers (VCSELs) or multi-mode fibers are employed; in the second application single-mode fibers with directly -or externally- modulated lasers are preferred. To differentiate between reaches, a channel of 100 Gps per wavelength may be DR, FR or LR. DR extends till 0.5 km, FR from 0.5 km to 2 km, while LR covers up to 10 km. Beyond 10 km till 100 km coherent optical transceivers with advanced modulation and power-expensive DSP are needed, for instance a 400ZR for data-center interconnections [5]. The two main

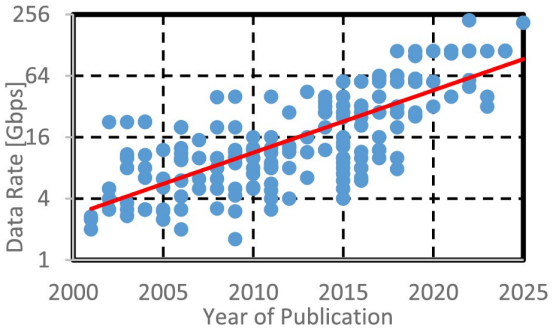

FIGURE 2: Data-rate requirements from [5]

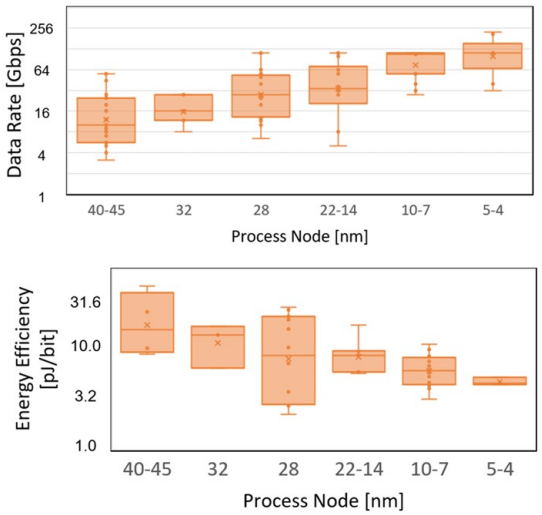

FIGURE 3: Process nodes achievable data-rate and energy efficiency from [5]

standards for high data-rate transceivers are: Ethernet and PCI Express (PCIe). Both are suitable for data-centers applications, but PCIe is more frequently adopted as it guarantees lower latency and more efficient equalization, timing recovery and FEC. The target remains modern compute systems with a lot of links transporting data for relatively short distances for in-drawer or in-package communication. When covering small distances, such as few meters, electrical links are preferred and transceivers are optimized for top energy efficiency. Architectures are expected to deliver the desired signal over channels with losses inferior to 15 dB [5].

In a typical transceiver, transmission and reception are carried out as depicted in Figure 6, whereas for a more detailed image of transmitter (TX) and receiver (RX) you can refer to Figure 7. RX is composed of an analog front-end (AFE), a wideband matching network, a continuous-time linear equalizer (CTLE) and a variable gain amplifier (VGA). The correct design of CTLE and VGA allows slicers, i.e., specific analog comparators, to sample the waveform and to eventually produce symbols. These slicers may be embedded with a decision feedback equalizer (DFE) with a single or multiple taps to mitigate ISI. Sampling should respect Nyquist law, its frequency may be a half of a symbol rate or exploit four phases of a quarter-rate clock, which appears to be the trending in latest designs. Regarding TX, segmentation technique is frequently employed for a smoother analog modulation in PAM 4 transmissions and for a more precise waveform-shaping through FIR filters, which are meant to work as feed-forward equalizers (FFEs). A more detailed description of TX is provided in the next subchapters. The most delicate part of the architecture is the last stage of data serialization as producing high symbol-rate data might be complex. Thus, it is required to carefully manage the fan-outs between multiplexers (MUXs) and drivers.

This excursus was meant to provide a general panorama of possible interconnection strategies, but the focus of this work must remain on inter-data-centers links (from centimeter to hundreds of meters) as the most data traffic interests these connections [9], as reported in Figure 5.

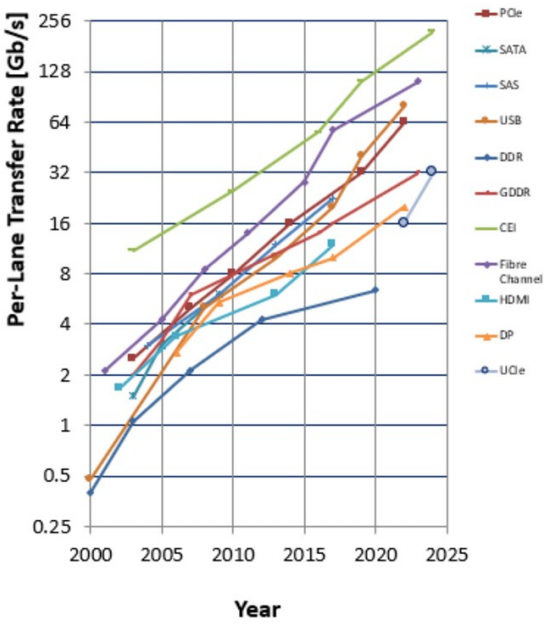

FIGURE 4: Wireline transceivers standards from [5]

Note that in the last years also technology scaled fast, with a significant step from planar to FinFET and another giant change ahead with gate-all-around fets, another aspect to be treated afterwards. As a rule of thumb, in the last decade the most scaled technologies used in commercial products have ranged from 12 to 2 nm. The proposed architecture has been validated through a 12 nm test-chip, thus making it a competitive and updated project.

As highlighted in Figure 6, the presented work will focus on the transmitter side, especially on its clocking. Looking at the transmitter chain, SerDes blocks precede the analog interface in electrical and optical transceivers, for instance [4] and [10]. Both transmitter and SerDes are served by the same PLL, whose requirements will be further explored in the next subchapter.

0.0.2 Transmitter PLL

For SerDes applications, a typical PLL features a PFD (phase/frequency detector) with its CP (charge pump) and LP filter, plus the controller oscillator and the divider. The described structure is usually a type II PLL. Being a type II, the traditional trade-off noise-bandwidth is partially mitigated with respect to the simplest type I but the design is sensibly less heavy and complex than a type III. Being type II a good compromise, it is a widely employed structure, with the well-known building shown in Fig.15. PFD is required in order to lock the PLL as f_{ref} must be close to f_{div}, thus placing a constraint on the reference whose phase and frequency have to be compared fairly with the divider output. On the other hand, also the divider should respect stringent specifications, especially in high frequency architectures. Most used topologies require discrete band at very high frequency and perform a division by 2 or by 4. Their PN must be well below the PN of the oscillator, which is the block defining noise and band limitation of the entire PLL. VCO is also a heavy power consumer inside the PLL loop, thus its optimisation regarding topology and performance will be the focus of this thesis. Another critical aspect for the PLL, especially for VCO and divider is the operation over PVT. At the state of the art, it is reasonable to have a 26.5GHz structure with >25tuning range over PVT [4]. Regarding the divider, a delta-sigma dithered multimodulus divider for fractional-N operation guarantees excellent performance at the price of enlarged area and heavier design complexity [4] with respect to other topologies [11], [12] providing integer divisions. If the fractional-N mode flexibility is privileged, delta-sigma may prove a winning choice as its noise folding will be reduced if the charge pump forces an offset between the reference and the feedback signals. Eventually, also the VCO topology must be correctly studied to guarantee good performance, robustness (for instance pn structures are favourable) and power efficient [13]. Recently, the most used topologies are Class C and Class B+Tail for the single VCOs and RTWO as distributed oscillator. Also, distribution network is a heavy contribution to the VCO performance, particularly for power -about 50% of the

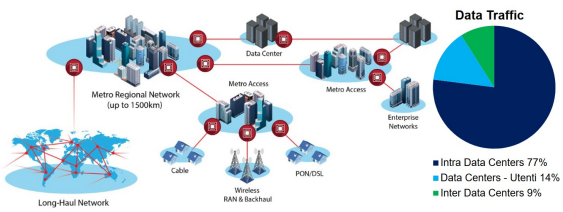

FIGURE 5: Data traffic according to CISCO.

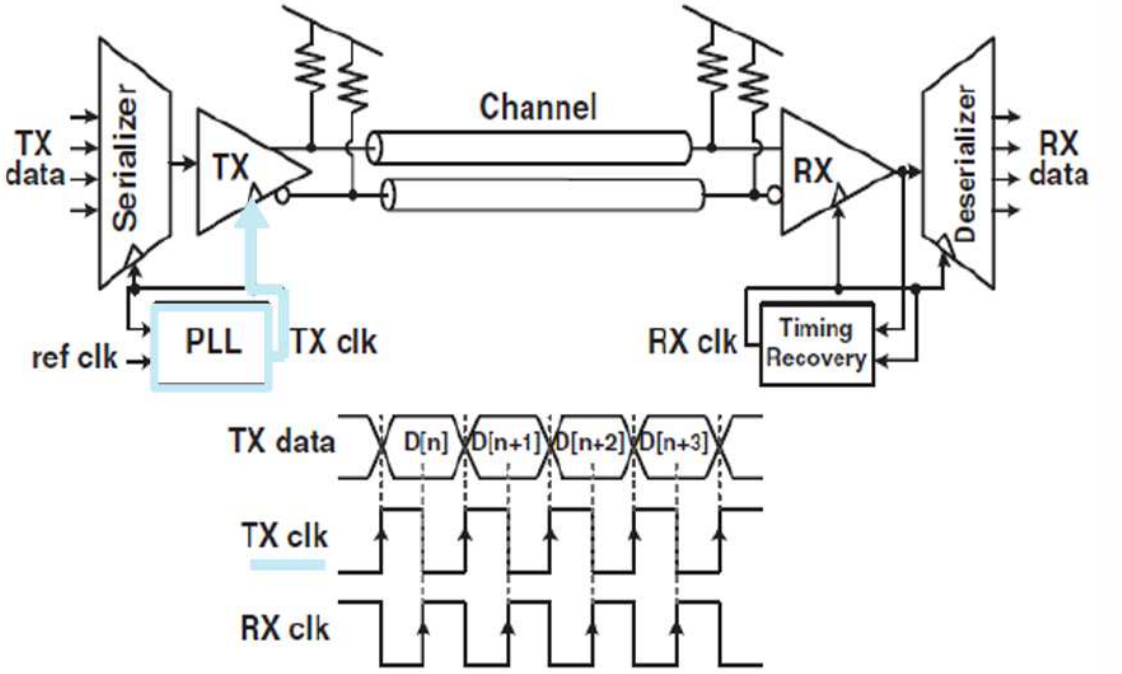

FIGURE 6: SerDes architecture.

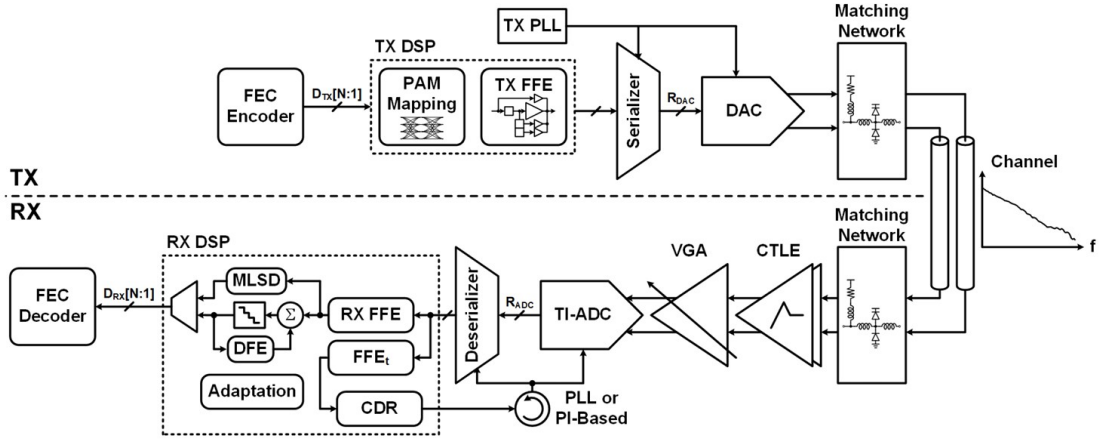

FIGURE 7: TX and RX schematics from [5].

total- and noise [1]. In brief, PLL trade-offs may be addressed through compromise between design complexity and performance and by carefully balancing all the component blocks inside the loop. Note that in an integer PLL, the most worrying source of noise is the oscillator [15]. As more complex structures, fractional PLLs must struggle with three noise components: VCO PN, modulator quantization noise and the reference PN. If the loop bandwidth is shrinked, so do the second and third noise contributors, while the first increases; in general the trade-off between VCO PN and modulator quantization noise is the true issue [16].

For a more general overview, synthetizing a clock signal is a challenging operation, which may start from a reference signal (usually a crystal oscillator) or from a received

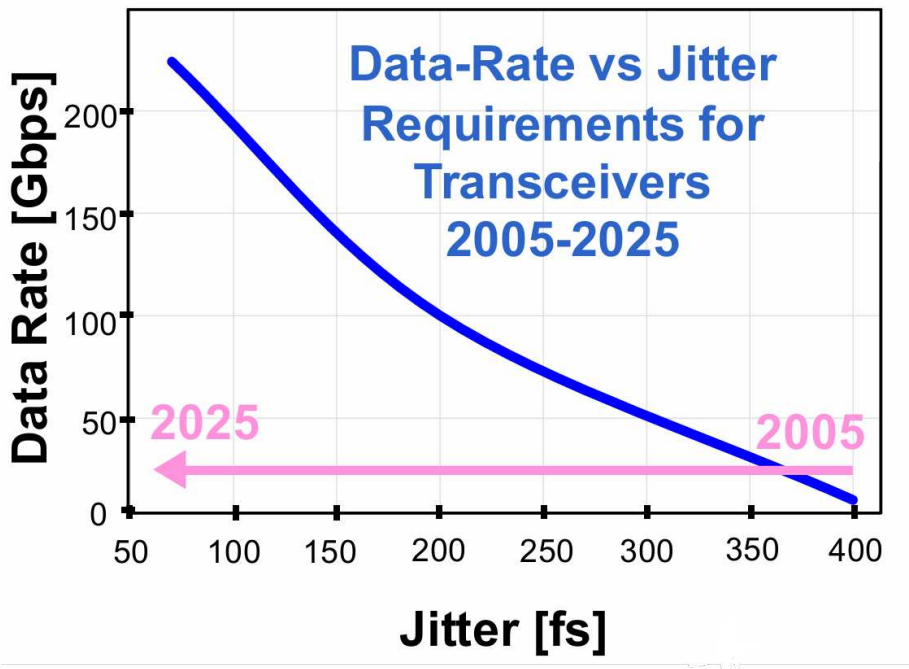

FIGURE 8: Data-rate vs Jitter requirements.

data sequence (RX clock recovery). Such an operation is carried out with a PLL for cleanliness, stability and preciseness. A type II is usually preferred as it can track both phase and frequency, thus closing the loop even if the reference and the output frequencies are not really really close. In a type II there are due integrators, hence two poles inthe open-loop transfer function, one from the loop filter and one from the VCO. Consequently, PLL may be seen as a low-pass (LP) filter for reference clock jitter: its limitation resides in rejecting only jitter of its own internal VCO below PLL frequency. Equivalently, PLL may be considered as a high-pass (HP) filter with respect to the VCO phase [1]. As LP filter it will provide jitter transfer, whereas as HP will perform jitter generation, producing the jitter transfer function shown in Figure 9.

In complex systems like [4], the PLL at TX and RX can be seen as in Figure 10, highlighting the problem of having TX and RX to be identical. The issue is reconstructing efficiently the clock signal at the receiver through clock recovery [21], [22]. Obtaining the same clock signal at both TX and RX is possible even without data recovery, but it takes a more complex method, i.e., an error extraction strategy based on cyclostationarity [23]. In such complex systems, there are multiple lanes, like in Figure 11, with a common lane featuring a clean PLL, requiring a big area and higher power with respect to the rest, which provides a clock reference for all the other lanes. This PLL usually has a low BW and it is used to scale the reference frequency to a suitable value and to filter its noise. By cleaning the upstream noise, as shown in Figure 12, the jitter transfer function will change as in Figure 13. Thus, high performance PLLs filter the reference PN, provides a low jitter clock signal to all data lanes, which gain benefits in terms of noise at the cost of additional area and power. In short, the clean PLL in common lane generates a fixed frequency which is then distributed to the data lanes as reference for local TX PLLs. The main advantages of this approach are:lane frequency independence,clean clock, at fixed frequency -or with a small TR-, low power in clock distribution from common to data lanes. On the other hand, each local PLL frequency independence is paid with bigger area and higher power consumption, while the crosstalk between TX PLLs of different

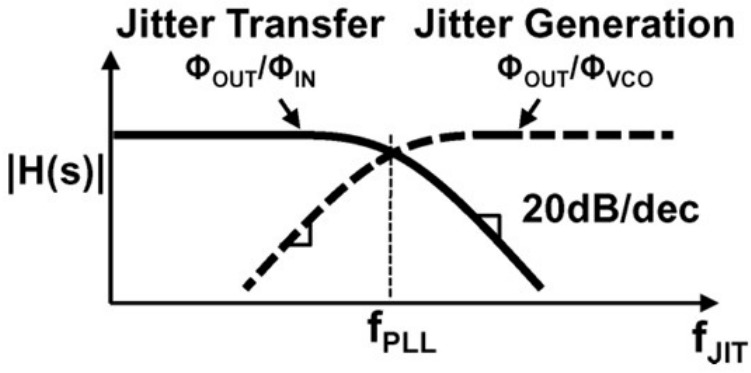

FIGURE 9: Type II PLL jitter transfer function.

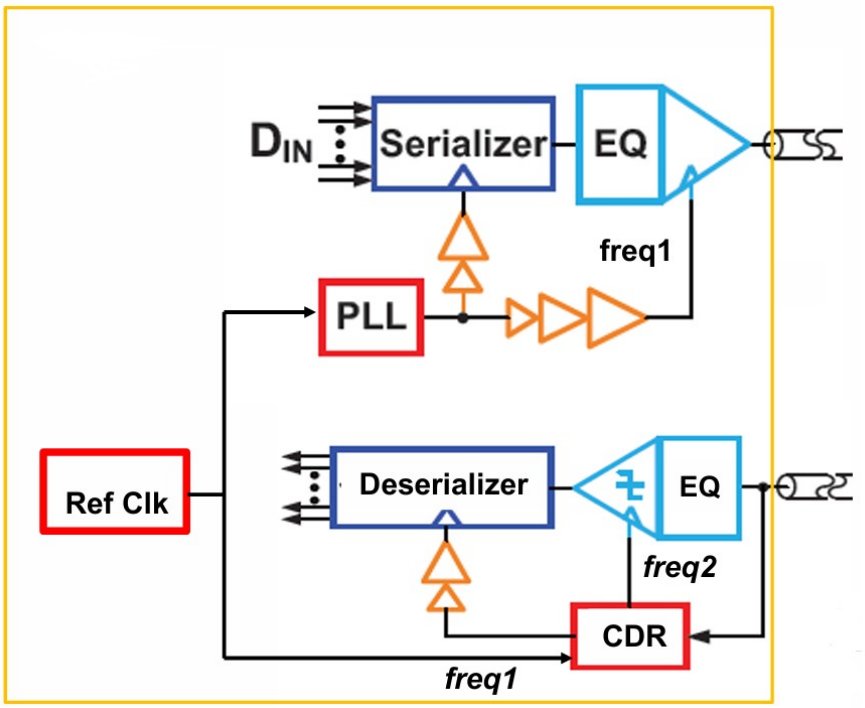

FIGURE 10: TX and RX PLL simplified schematic.

lanes needs to be handled [24]. If lane independence is not a spec, then area and power can be saved as no PLL would be present in the data lanes. But clock distribution from common lane to data lanes would remain demanding in terms of power hunger. Adopting this strategy, all transmitters need to work at the same frequency -or another PLL in the common lane will be required. At high frequency, clean PLL programmability and clock distribution are still a true challenge [24].

As mentioned before, two poles may lead to instability, why a zero is usually added by inserting a resistor in series with the loop filter capacitance. To study the degree of stability of the PLL, the damping coefficient is calculated [17]. As the PLL is a very sensitive architecture, it needs to be designed for elevated robustness across process, voltage and temperature variations (PVT). In particular, the VCO gain and especially the charge pump may strongly vary with PVT. In an attempt to mitigate such an issue, PLL may be

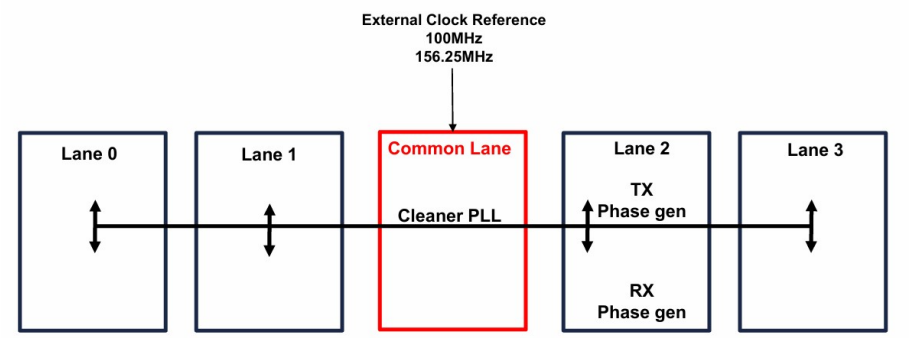

FIGURE 11: Multiple lanes PLL system.

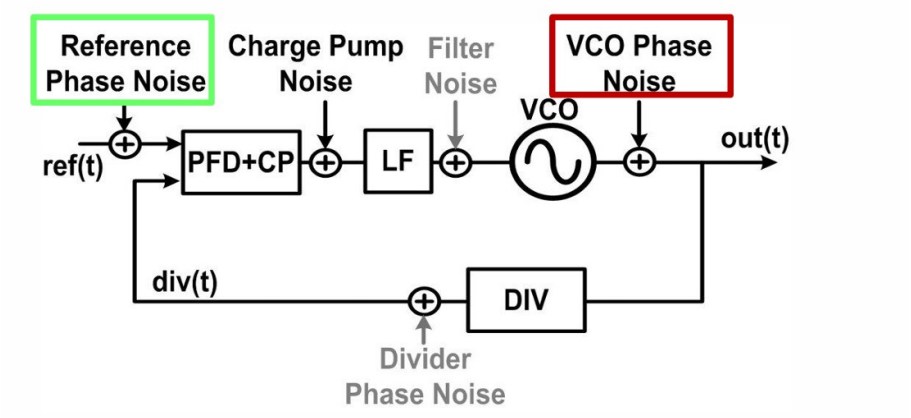

FIGURE 12: PLL noise schematic.

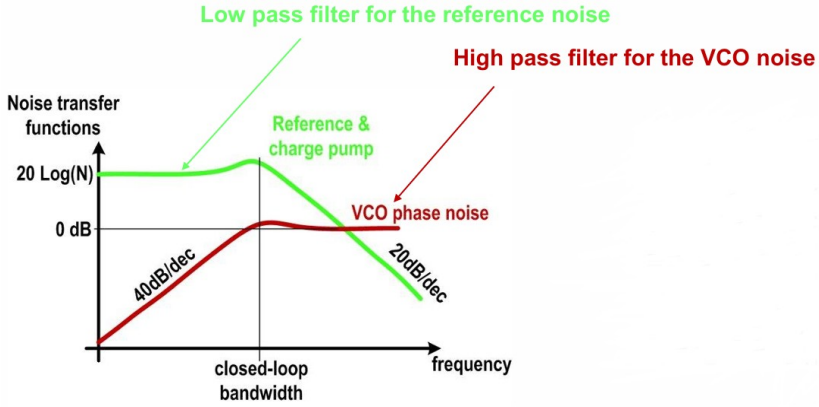

FIGURE 13: Clean PLL jitter transfer function.

adjusted to depend on reference clok -which is stable by definition- and a capacitive ratio -by controlling charge pump current through VCO bias voltage [1]. The same technique may be employed for the loop filter zero. For further details about this topic, you can look at [17].

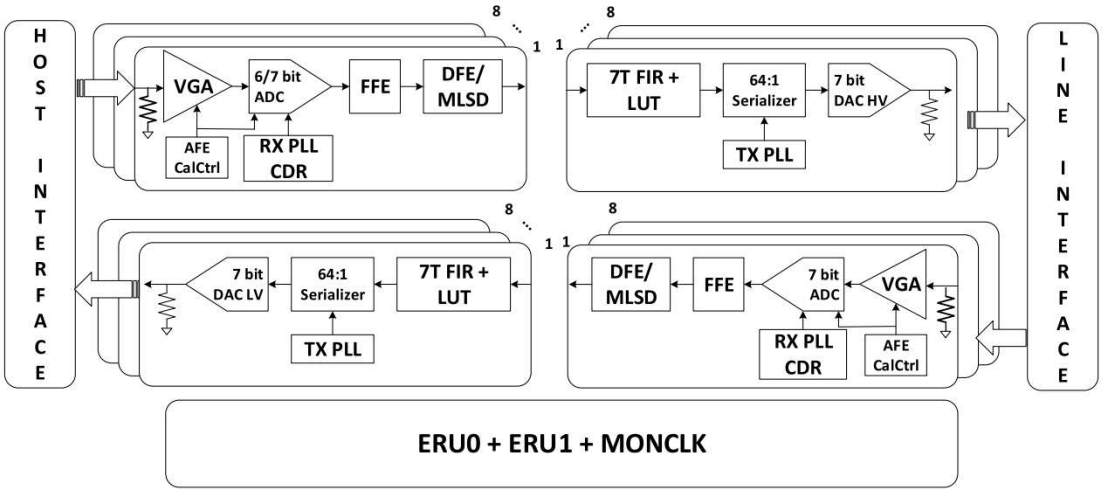

FIGURE 14: Transmitter architecture from [4].

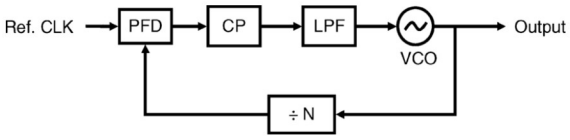

FIGURE 15: Type II PLL block diagram.

0.1 Clock Distribution Options

Clock distribution is an important feature in both TX and RX as it ensures the correct delivery of the clock signal and thus the proper operation of the entire transceiver. The distribution may be implemented as a separate structure [18] or as a part of the clock generating architecture [20]. Both solutions are viable and currently employed. In general, as shown in Figure 19, the first solution includes a stand-alone VCO -or a cluster of coupled oscillators- whose output is delivered to the users through a distribution network, whereas the second is made of transmission lines connecting distributed active elements for traditional architectures [20] or multiple cores in the case of hybrid solutions [80], [81]. The first option provides an additional degree of freedom as implementing two separate architectures for generation and distribution grant the opportunity to optimize both; in particular, for the stand-alone oscillator the quality factor -and thus the PN- may be greatly enhanced. On the other hand, two structures will be expensive in terms of area, power and noise. From the area point of view, the stand-alone VCO will require a large inductor in order to improve the Q. Coupled oscillators will need even more space if their coupling is structured as to minimize the passives couplings and optimize the oscillator coupling strength [39]. Furthermore, the distribution network consumes as much power as the VCO, as a rule of thumb. When it comes to noise, the designer must be careful that the clock signal PN is not too impaired by the distribution, but this network will inevitably contribute. Regarding the second solution, i.e., distributed oscillators, there are many possible implementation, such as travelling waves [19],stationary waves [20], rotary waves [30] and hybride distributed oscillators [80], but all have a common advantage: the power budget for distribution and generation is the same, thus making it a power-friendly alternative. The same principle holds for noise, although the total PN

will be worsened by the fact that transmission lines have an intrinsically lower Q with respect to traditional resonators [38].

Now, the first solution will be examined. To state the obvious, transporting the clock signal -especially at high frequency- is quite a challenge as a state-of-the-art signal can range from few GHzs to 30GHz or more, spread across several millimeters. In a multiple lane system as the one previously depicted, timing blocks serve different lanes thus must deliver the same clock signal to all the users, facing many issues. For instance, per-bit deskew in high-speed parallel links is a common occurrence, but not the most serious one as clock jitter and duty-cycle errors severely impairs the distribution network performance [1].

In fact, there exist many strategies to implement a proper distribution network. The first and simplest methodology is an unregulated inverter. Through inverters, a buffer chain can be realized. Inverter-based solution are easy to implement and to port and also power-friendly. In a CMOS process current is only drawn from the supply during clock transitions. In usual implementations, chains of buffers drive multiple interconnections, whose maximum length is determined by clock frequency and line characteristics [25]. Despite simple and powerful, these architectures are highly sensitive to supply noise. For example, under the approximation that the delay is small compared to the noise period, if supply noise is within 5-10%, then the jitter may be in the order of 1-2 ps, calculated with the 1/ delay - 1/ supply rule of thumb [1]. The issue arises if the jitter spectrum falls within the BW of the clock recovery mechanism, hence degrading the timing margin. In order to mitigate this heavy dependance on voltage supply, one can consider different designs trading supply sensitivity with power. The two main cathegories are: regulated delay cells and CML-based VCOs [1]. Concerning the first topology, regulation costs additional power but guarantees delay regulation exploiting PLL or timing loops. The additional power is spent on the additional buffers, which may be pretty demanding, and sometimes even wasted on parasitics due to complex routing between control voltage to the buffers. Regulated architectures -both inverters and SL CML buffers- are more sensitive to control voltage, as shown in Figure 16 [1]. A proper shielding is thus necessary to ensure that the jitter performance improvement due to regulation is counterbalanced by excessive sensitivity. A third possibility is to employ a CML buffer with fixed resistor load, thus implementing a fixed delay RC which is indipendent of supply noise, at least in first approximation. But CML buffers represent a power-consuming solution as they always draw current, even when not switching.

On the other hand, transmission lines (t-lines for short) allows a power efficient clock distribution and are less sensitive to supply noise. T-lines are able to distribute a high-frequency clock -several GHz- for millimeters [40]. As clock is slow-sing, the RX must be designed carefully not to introduce more jitter then the amount suppressed with this repeaterless approach. T-lines are not exclusively for generation and distribution, but they can be used for distribution only when clock signal comes externally [41]. This kind of strategy reuses the power of the external driver, so it does not cost any additional on-chip power [1]. Alongside the trade-off between jitter and power, one must consider the clock bandwidth and the amplification of input jitter and duty-cycle error. As a practical way, to minimize clock power one could assume that the clock is efficient up to a treshold frequency, then it could be recovered at higher frequency -when amplitude is attenuated- using a level converter. For a more rigorous approach, BW should be studied by extracting the jitter impulse response. For instance, injecting a jitter impulse in a Cadence simulations, the jitter can be tracked, thus providing a feasible description of jitter behaviour. As a practical reference, one can look at Figure 17 for understanding. Furthermore, the normalized jitter impulse response as a function of frequency is qualitatively shown in Figure 18, representing both DCA, i.e., duty-cycle amplification, and

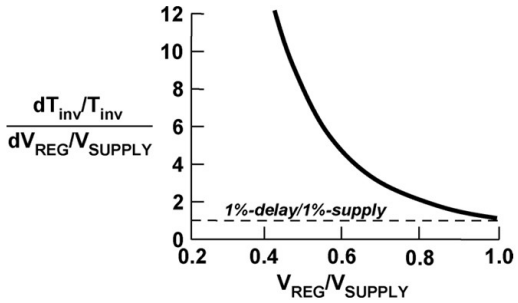

FIGURE 16: Inverter delay sensitivty to noise on regulated voltage normalized to supply voltage, from [1].

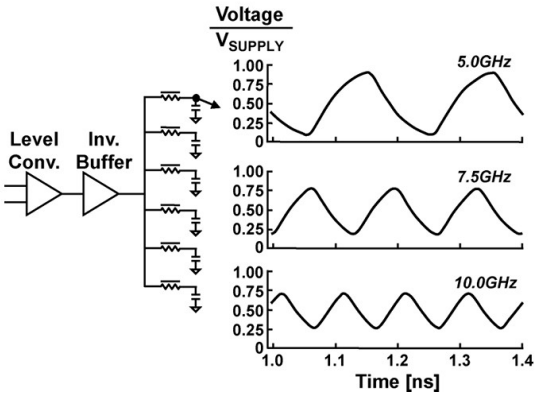

FIGURE 17: Clock output waveforms with a low-swing differential input clock and inverter-driven clock tree driver, from [1].

RJA, i.e., random jitter amplification. The data must be taken into account as an example as they come from Casper work [1]. The winning strategy consists of a proper modeling of system clock jitter.

Regarding data-link applications, multiple hybrid solutions have been developed to distribute the active part along t-line [20], to connect multiple VCOs with t-lines [80], to implement self-oscillating clock networks [42]. Another efficient idea is to design injection-locked oscillators to filter and delay the clock [43], [44], [45]. A further panoramic of t-lines different topologies will be given later. The aim of embedding VCO inside clock path is to break off the trade-off power versus jitter, which is exactly the target of this work.

Clock distribution has always been a pressing matter, ever since the early 2000s [20] as it has a great impact on power and noise of the whole PLL. As the distribution requires the same amount of power as the clock generation and the same assumption can be advanced regarding PN [1], distribution deserves as much attention as the oscillator. Unfortunately, while publications about VCOs flourised throughout the years, distribution received considerably less academical study, while remaining a eyesore for industrial application. Among the different solutions, it is worth mentioning CML distribution and buffering. As CML require CML to CMOS converters [28], [29] which could be further expensive in terms of complexity and power. Buffer distribution is most commonly adopted for industrial applications and academia. Despite having no particular development during the latest years, buffer clock distribution enables some key advantages: first

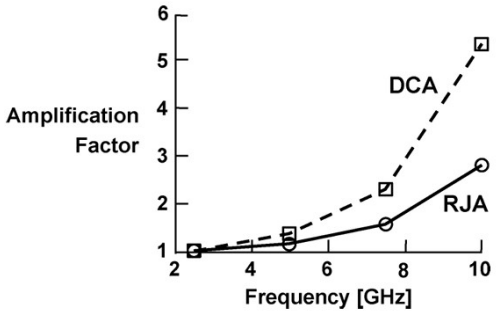

FIGURE 18: RJA and DCA in function of frequency, from [1].

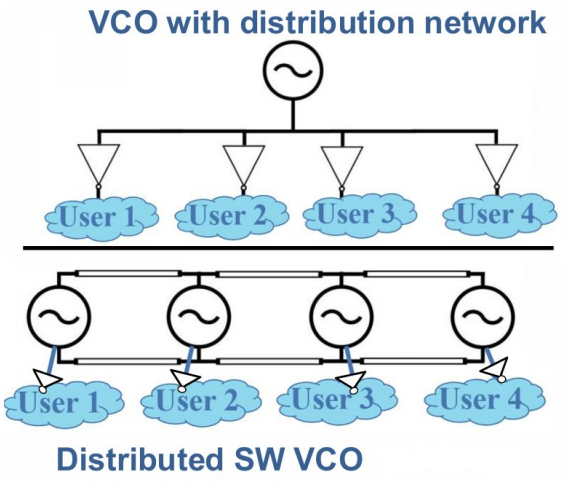

FIGURE 19: Comparison between stand-alone and distributed oscillators.

it allows the implementation -and thus the optimization- of any kind of oscillator topology, second it guarantees that a good quality factor is maintained in the overall structure, at the cost of power consumption, third buffering is a super scalable option, enabling the signal to be generated virtually everywhere inside the chip, even if some smart layout should be advisable. On the other hand, distributed architectures became a thing around twenty years ago, gaining popularity as they allowed to generate and distribute the clock signal within the same power budget, at the cost of a reduction in Q and of a more rigid area allocation, suitable for their shape. As the specifications evolved through the years, most distributed topologies disappeared from academical researchs, except for the rotary structures [30], for RF applications; while they remained "in fashion" for area-constrained applications [36]. Despite the number of published papers, clock distribution stayed a hot topic and became even more pressing in the 2020s with the advent of AI, which further exacerbated the dicotomy stand-alone versus distributed oscillator.

0.1.1 Stand-Alone Oscillator

Considering a single unit VCO as a basic piece of a clock generation architecture, an excursus on stand-alone oscillator is written to introduce the main trade-offs of this block. As this unit must be closed into a working PLL, several characteristics should be taken into account: power, tuning range (TR), portability, random and deterministic jitter. By

integrating jitter, it can be reconducted to PN [46]. For simplicity, successive considerations will be made based on PN. For a wide panoramic across stand-alone oscillators, some popular types are to be mentioned. For example, ring oscillators -shown in Figure 20- belong to the low complexity implementation cathegory. Their main advantages lie in their robustness, wide TR (one order of magnitude or more) and power which can be easily predicted as it scales quadratically with frequency, provided that there is a linear voltage regulator [1]. Their most notable flaws are the high VCO gain, resulting a high biasing noise sensitivity, and a poor phase. Mark that a wide TR will generally correspond to high sensitivity to supply and bias noise, while relatively poor PN -once fixed the power- heavily depends on a relatively low Q if compared to LC oscillators [47]. Even if newer topologies proposed multi-phase ring oscillators [49], the phase still remains a consistent limitation. To solve the phase issue, a designer can turn to resonant oscillators. Also, rings need linear regulators acting as unity gain buffer to reject supply noise by the loop gain. Unfortunately, this block may consume 3-5 times more power than the VCO itself [50].

Proceeding with increasing complexity, there exist oscillators based on CML-based delay cells with active loads, depicted in Figure 21. Instead of active load, the same architecture may drive a combination of saturated and diode-connected devices forming a voltage-tuned resistive load, called "symmetric load". The strength of this structure resides in the fact that the current versus voltage transfer function remains symmetric and its resistance can be tuned to cover a wide TR [51]. The main disadvantages are: the magnitude of the delay gain being comparable to the gain of a regulated inverter delay cell, having a remarkable sensitivity to bias and supply noise, requiring a regulator for voltage bias and to avoid excessive dependance on supply noise. In addition, such an architecture also has a power scaling with frequency. Given the above-mentioned characteristics, CML-VCOs share many of the ring oscillators flaws, that is why LC tank oscillators seem a winning choice -and are in fact the standard- for our target application.

In fact, LC VCOs -shown in Figure 22- are a robust architecture, enriched by many different topologies which are being discussed in chapter 1. The concept behind LC tank oscillators is that the frequency is selected by the inductance-capacitance pair, according to $\omega = \frac{1}{\sqrt{LC}}$, then the frequency is swept across the TR by varying the switched capacitors. As frequency depends on the square root of the total LC, the TR will be generally smaller than a RC oscillator. In order to expand the TR, the switched capacitors will include not only varactors, but also digitally-controlled tuning capacitor banks. Depending on the specifications, such banks may include coarse and fine tuning or even multiple tuning levels; the important aspect is that their spacing enables analog fine-tuned varactor spanning any two coarse-tuning codes. Analogously, all fine-tuned digitally-controlled capacitors must be at least as big as a coarse-tuned capacitance. In performative designs, a margin is usually considered. Compared to ring and CML-VCOs, LC-based oscillators presents a much lower sensitivity to supply and bias noise, deriving from their improved Q. Consequently, they also display lower PN for given power [52]. Regarding power, it does not scale with frequency with the same rule as rings and CMLs, but it rises with the amount of negative transconductance required due to the LC tank losses. According to [1], power consumption increases at lower frequencies as Q reduces when frequency is shrinked. On the other hand, voltage swing does not strongly depend on frequency, unlike the previously adaptive-biased VCOs. Many attempts have been made to digitize the PLL loop [53], [54] to reduce analog loop components, especially charge pump and loop filters. A digital loop allows a consistent reduction of loop filter area and a minor sensitivity to analog device characteristics. It also eases digital reconfigurability and calibration. However, due to the many challenges of digital PLLs, for instance minimizing

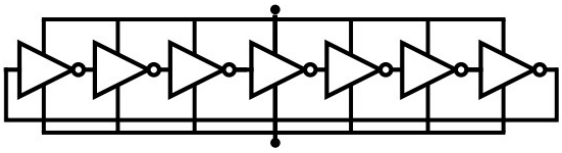

FIGURE 20: Ring oscillator schematic from [48].

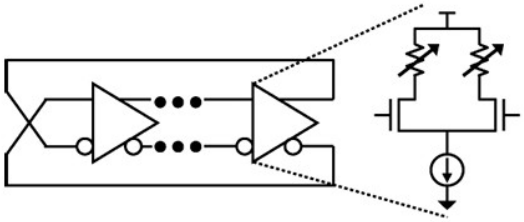

FIGURE 21: CML-based VCO with tunable load from [1].

quantization jitter and implementing low-power, high-resolution time-to-digital converters and digitally-controlled oscillators (DCOs) [53], the most adopted solution is now a digitally-assisted PLL with analog LC tank VCO. In particular, different LC VCO topologies have been studied to ensure the best performance and the most convenient fitting inside these complex PLL architectures.

0.1.2 Distributed Oscillator

Distributed oscillators allow to resolve the issue of clock distribution as they both generate and distribute the clock signal within the same power budget. For PN improvement, coupling remains a good strategy as t-lines allow easy and robust coupling between multi-cores. As a low power alternative to stand-alone oscillators, they gained popularity in the early 2000s [20] despite their intrinsic Q limit. It has been proved that a t-line will always have an inferior quality factor with respect to a single inductor at the same frequency. Consequently, distributed architectures generally exhibit lower PN and FoM performance with respect to stand-alone VCOs as papers never report clock distribution costs in terms of power, noise or even area. Although attempts were made to mitigate such an issue -for instance tapering t-lines [20]- the limitation remained not

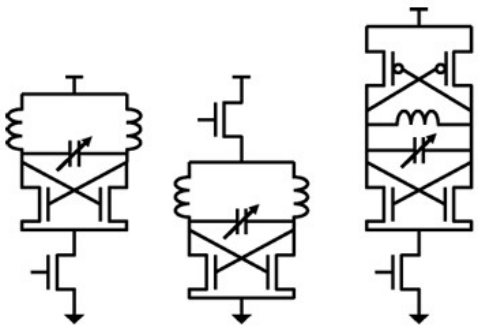

FIGURE 22: LC tank VCOs from [1].

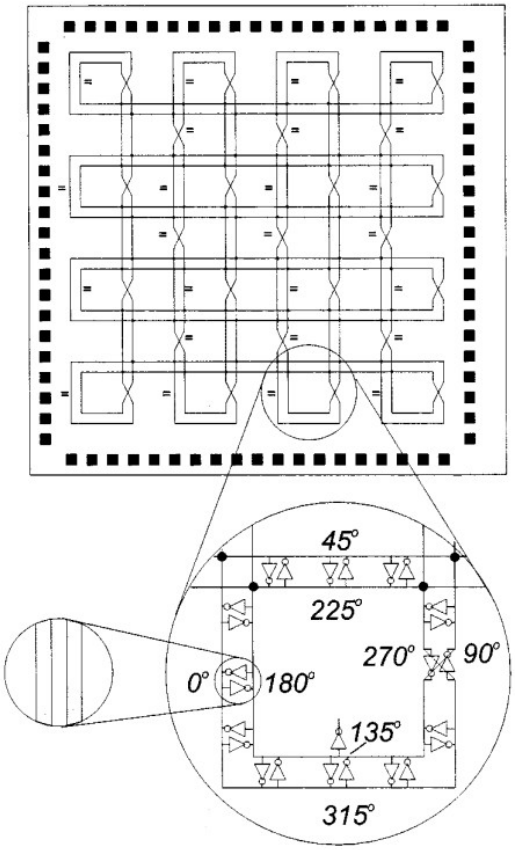

FIGURE 23: RW oscillator schematic from [31].

negligible. Due to this drawbacks, distributed solutions remained a viable alternative for industries but became much less popular in papers. Only from the late 2010s [30], rotary architectures made a come-back for restricted applications.

In general, there are three kinds of distributed architectures: travelling wave oscillators, rotary wave oscillators and standing wave oscillators. A fourth category may include hybrid solutions.

Travelling wave oscillators (TW) are based on travelling waves by definition, i.e., the wave propagating changes along t-lines, thus creating multiple phase outputs. TW oscillators are an excellent choice for multi-phase oscillators or for huge TR and can also usually offer better PN than the RTW. However, when only one phase is required, they may be a sub-optimal choice due to the design complexity. In fact, the direction of wave propagation can be random, requiring additional circuitry for control. TW may be employed

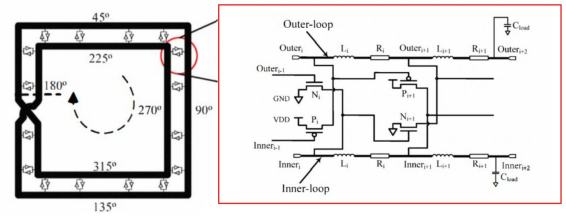

FIGURE 24: RW oscillator schematic with push-pull from [27].

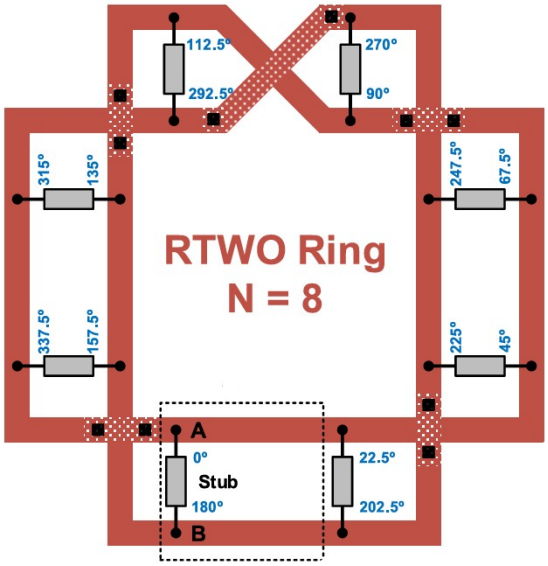

FIGURE 25: RW oscillator schematic with stubs from [32].

for wireless transceivers and phase arrays for communications systems and radars. In particular, multiple phases oscillators are key blocks for phase shifting, quadrature frequency conversion, sub-harmonic mixing, sideband or image rejection [26].

Most TW are RW as their shape allows good implementation for travelling waves. This structure is often called "RTW" [30]. The second topology, the rotary wave (RW) oscillator, presents good performance in terms of power and it is the more balanced structure as each core sees the same impedance inside the ring, whereas the main disadvantage is the area occupation. RW structures differs from TWs for their characteristic shape resembling a closed ring, which forces the wave path in a periodic boundary condition. Another strong difference is that outputs can be taken in multiple point along the loop, while TX outputs are at the t-lines ends. Rotary wave requires a ring shape which is not always compatible with product layouts, thus limiting this solution to few applications and academic papers [30]. The concept of RW is to create a rotating traveling wave within a closed-loop differential t-line with distributed CMOS inverters working as amplifiers and latches for the oscillation continuation and the rotational clock. As load capacitance is absorbed into the t-line characteristics, the energy is recirculated with an adiabatic quality and multiphase square waves are produced directly [31]. This kind of architecture can be closed as to form rotary oscillator arrays in order to distribute a phase-locked clock over a large chip. The main advantage is its scalability -even for very high clock frequencies (even), while the main disadvantages regard area, interconnections and field couplings which risk dominating the design process for RWs [31].

For an improvement in power consumption, consider that most RWs are inverter-based and consequently consuming short circuit power as technology keeps shrinking. By implementing a Push-Pull cell based traveling wave oscillator (PPTWO) -as observable in Figure 24-, it is possible to both save short-circuit power and control the rotation direction of the clock signal effectively. Thanks to [27] approach, up to 6.6% power may be saved without additional circuitery. Another significant problem is flicker noise up-conversion due to t-lines dispersion causing the higher-order harmonics to travel faster than the fundamental one. To address this an issue, [32] proposes to add distributed stubs along the t-line (Figure 25) such that tuning capacitors on the stubs manage to

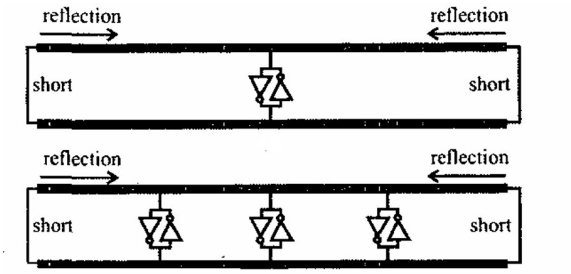

FIGURE 26: SW oscillator schematic with single or distributed Gm from [33].

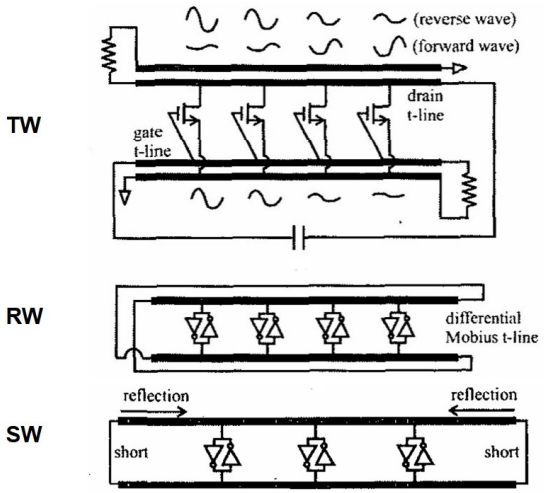

FIGURE 27: Difference between TW, RW, SW oscillator basic schematics from [33].

slow down the travel speed of higher-order harmonics relative to the fundamental and finally succeed in lowering the phase shifts due to dispersion. Both power and dispersion improvements require additional complexity, which -united to its area and shape limitations- make RW not the primary choice when it comes to distributed architectures.

On the other hand, standing wave oscillators (SW) are based on the standing wave created by two waves travelling in opposite directions. The main physical differences between the three topologies are in how waves proceed along t-lines and how t-lines are terminated, as observable in Figure 27. SW oscillators must feature t-lines of lengths equal or multiple to $\frac{\lambda}{4}$, thus restraining the area requirements of this structures. Furthermore, coupling multiple cores requires forcing mode elements, to ensure the correct oscillation modes, for instance a small resistors [80].

For a more precise understanding, what happens is that in a differential t-line is connected to a pair of cross-coupled inverters at one end and then it is shorted at the other end in a such a way that the energy will be injected as forward waves by the inverters and then reflected into reverse waves at the short. In steady state, the forward and reverse waves superpose to create standing waves [33]. As boundary conditions allow SW modes at multiples of $n\frac{\lambda}{4}$ with $n = 1, 3, 5, ...$, the higher odd modes are negligible with respect to the fundamental mode $d = \frac{\lambda}{4}$ because of a substantial high-frequency loss. Under the condition $d = \frac{\lambda}{4}$, voltage and current amplitudes vary monotonically with distance (z): at the short end ($z = d$), the voltage has a minimum, i.e., $V(z = d) = 0$,

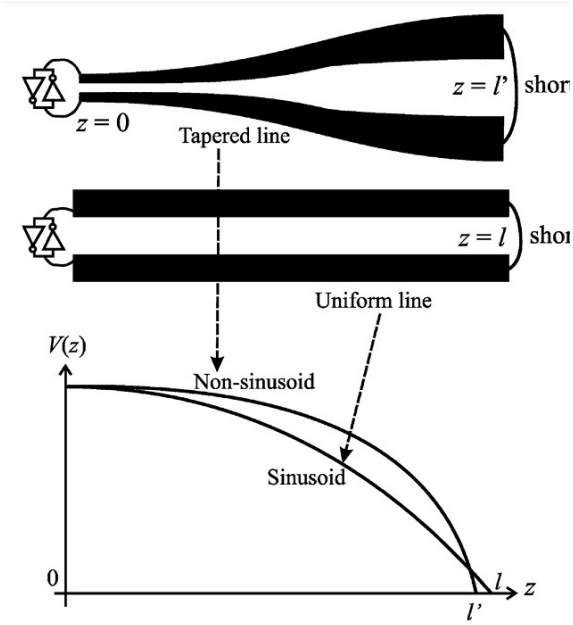

FIGURE 28: Difference between SW traditional and tapered transmission lines and their voltages from [20].

and the current reaches its maximum; at the other end ($z = 0$), the voltage has a maximum and the current a minimum. Analogously, other SWs may be built, for example a $\frac{\lambda}{2}$ architecture, which can be seen as a natural extension -or simply the sum- of a $\frac{\lambda}{4}$.

This topology is not suited for multi-phase operation or length-constrained layout but ensures good power and PN performance and robustness. As the same phase is maintained along the line it can be a preferrable option with respect to clock distribution networks for applications were phase constance is crucial. Along t-lines, the active elements -Gm- may be stationed every $\frac{\lambda}{4}$ or distributed along the line for better PN and design flexibility, at the cost of additional power. PN depends on the shape of the electromagnetic wave: a simple linear pulse oscillator has less phase noise than a sinusoidal standing-wave oscillator, mainly due to SW nature [34]. As all t-lines-based structures, SW suffer from modest Q of t-lines; to mitigate this issue, multiple solutions were proposed, for example tapered t-lines [20] and a mix of lumped LC and t-lines [81]. SW adaptive tapered t-lines enhance Q, thus lowering PN, through loss-reducing shaping of the transmission lines, such that Q becomes position-dependent, as well as amplitudes of the waves. Naturally, the quality factor peaks when the distance between t-lines is the largest, resembling a lumped inductor. The main disadvantage of this design resides in its complexity, in particular in the difficult approximation process. As tapering makes the wave amplitude no longer sinusoidal, as shown in Figure 28, because the wave velocity in a tapered line is not uniform and L, C are position-dependent, the tapered t-line is not optimized for the non-sinusoidal amplitude profile, thus a time-consuming iteration process is needed to optimize t-line parameters [20].

A further cathegory, the hybrid solution, mixes the flaws and the advantages of each topology. For example, in [80], SW and RW coexists to achieve low power at very high frequency ($> 50GHz$) in millimeter-wave transceivers. [80] uses RW for its multiple phases and then to couple four cores with no additional power and PN expense.

As we want to combine advantages from SW and stand-alone oscillators, in this work we will propose a hybrid with multiple stand-alone cores (Gm with their tank) coupled

through standing wave transmission lines [81]. The goal is to achieve the stand-alone PN performance without additional power for clock distribution. This strategy will relieve the Q mitigation due to t-lines and grant a simple, robust and relatively low-area solution.

Chapter 1

Oscillators

Stand-alone oscillators are a wide class and include a variety of topologies, in this work the focus will be on LC oscillator with transistor cross-couple due to the target application. In particular, high Q LC oscillators were selected as an efficient and extremely low PN architecture for modern communication systems, where clock should be impeccable. As implementing a good tank guarantees a satisfying Q and PN, also robustness is required, which is the reason why CMOS complementary pn is chosen. Even if pn halves the output amplitude, it will ensure that the mosfet can not break easily due to overvoltage [13]. CMOS technology is the standard, nowadays industry works with FinFETs due to digital requirements, but analog blocks usually performs better with older technology nodes. This scaling often negatively affects noise -especially flicker components-, whereas it has a positive impact on power. As a matter of fact, power, area, noise, frequency and complexity are the main parameters to work with.

General oscillators are mainly composed of a resonant part -LC tank- and a regenerative component -transistor made- as shown in Figure 1.1, while additional components may be included to implement further improvements, for instance a second LC tank for the tail. LC tank will define the frequency through the well-known relation $\omega = \frac{1}{\sqrt{LC}}$ and the quality factor (Q), defined as the ratio $\frac{2\pi stored-energy}{dissipated-energy-in-a-cycle}$. Through Q, LC tank will heavily impact phase noise (PN), according to the formula

$$PN(\Delta\omega) \propto \frac{kT\omega}{CQV_{out}^2(\Delta\omega)^2} \tag{1.1}$$

from [37]. Considering that $V_{out} \propto Q$, then $PN(\Delta\omega) \propto \frac{1}{Q^3}$. Such an expression provides useful insights on the main contributors to PN, whose minimization is a crucial point. The most effective element to reduce PN is frequency, hence minimizing $\frac{\omega}{\Delta\omega}$ would considerably improve the noise performance. As high frequency is a set parameter for our target application, the only exploitable leverage are C and Q. Under this regard, stand-alone oscillators offer great freedom in optimizing the quality factor through passive shapes [82], topology and area. To get more insight, Q can also be defined as the weighted average of the passive elements quality factors [38]. Another key trade-off is the one between PN and power. As a rule of thumb, a 3dB PN improvement may be obtained at the cost of doubling the power consumption; as a result the FoM remained unvaried. In the same way, by coupling multiple cores the FoM stays the same while PN shrinks and power increases, as explained in the following sub-chapter concerning coupling. Evaluating VCO overall performance with the figure of merit (FoM) ensures a practical and efficient way to compare oscillators by taking into account noise, power and frequency.

$$FoM(\Delta\omega) = 10log(\frac{(\frac{\omega}{\Delta\omega})^2}{P * 10^{-0.1PN(\Delta\omega)}}) \tag{1.2}$$

Note that power (P) should be expressed in mW. The same expression may be rewritten as a function of power efficiency and quality factor [13], taking into account that the maximum feasible figure of merit is limited by $10log(2Q^2)$ with Q obviously being a function of frequency.

Regarding the active part, it will be pn, as mentioned above, and it has a further degree of freedom, i.e., choosing whether the gm-controlling variable will be voltage or current. By employing a pn structure, performance -in particular output swing and PN- will change as indicated in Figure 1.3.

When choosing between voltage or current biasing for oscillators, it is important to remark that both present their perks and flaws and that there exist voltage-bias and current-bias limits but the ultimate limit is, after all, noise [13]. More in general, current-biasing seems appealing for improved PVT and PN performance, but the current generator adds noise and complexity. In this work, voltage-biasing technique was adopted as it erases the need of a current generator, thus lowering PN and increasing power efficiency, at the cost of enhanced frequency pushing. To further enhance power efficiency, one may be tempted to obtain large voltage swings, which also reduces phase sensitivity to device noise, but this condition would facilitate device entering triode region and loading the tank, with the subsequent PN degradation.This defines a supply versus PN trade-off, partially solvable with a low supply voltage, sufficient to avoid that transistors enter triode region [13]. On the other hand, the use of a low supply voltage makes the performances very sensitive to supply voltage variations, hence requiring a LDO, with area and power rising again [35].

In order to evaluate gm performance, especially with respect to power, the definition of power efficiency may be used. Power efficiency η_P is the product of current and voltage efficiencies, with voltage efficiency being the ratio between the voltage effectively falling on the tank -called V_{RF} - and the total voltage headroom, i.e., the supply. The same holds for current, as current efficiency is defined as the ratio between the current spent on the tank (I_{RF}) and the total current drawn from the supply. Depending on different topologies, the maximum efficiency varies.

Beyond FoM, another efficient way of comparing different oscillators -especially different topologies, is the ENF. To get to ENF, first one must rewrite the FoM formula as in [13].

$$FoM(\Delta\omega) = 173.8dBc/Hz + 10log(\frac{\eta_P Q^2}{\Gamma_{T,rms} + \alpha\Gamma_{M,rms}}) \tag{1.3}$$

Now, FoM expression depends on power efficiency and quality factor, on noise factor α, on rms ISF for tank ($\Gamma_{T,rms}$) and transistors ($\Gamma_{M,rms}$) [13], under the hypothesis that all noise is thermal, plus a noise floor (173.8dBc/Hz). To maximize the figure of merit, one can act on tank and transistors, on Q and on impulse sensitivity function (ISF). Ideally, power power efficiency can be brought up to 100% and transistors can be made noiseless, neglecting any other noise contribution, so to get the maximum FoM FoM_{max}.

$$FoM_{max} = 173.8dBc/Hz + 10log(2Q^2) \tag{1.4}$$

In this expression, it is clear the FoM dependance on noise floor and tank quality factor, which represents the ultimate performance limit. Then, the actual difference between the figure of merit and its maximum can be defined as the excessive noise factor (ENF), symbolizing how far a VCO is from its physical limit. As per FoM, every topology has its maximum ENF [13], shown in Figure 1.2.

$$ENF = FoM - FoM_{max} \tag{1.5}$$

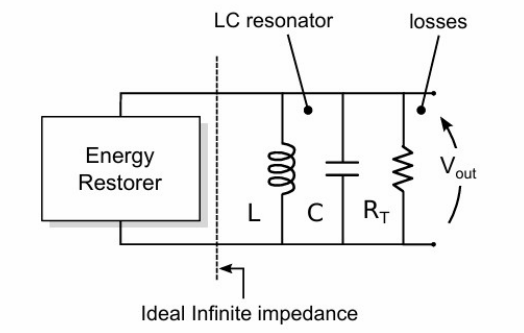

FIGURE 1.1: Oscillator main components from [13].

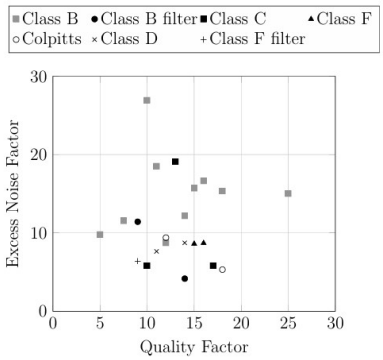

FIGURE 1.2: ENF used as benchmark for different VCO topologies from [13].

1.1 Oscillators Topologies

When it comes to optimizing performance, it is important to understand the phyical limits of a given structure and here topology classification becomes fundamental in selecting fast and reasonably a good VCO. Various methods of VCO classifications have been proposed in the last decades, in this work only two will be adopted: topology and purpose classifications. In this sub-chapter, topology classication will be dealt with.

Regarding topologies, [13], [60] presents an efficient method to sort out different architectures by evaluating their power efficiency, defined as previously explained. Most classical topologies -Class B, B+Tail, C, D, F- have been considered while other newer

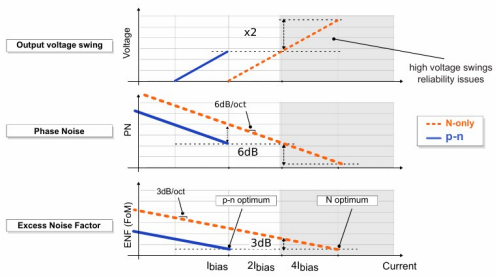

FIGURE 1.3: Output swing, PN and ENF for pn and n-only VCOs from [13].

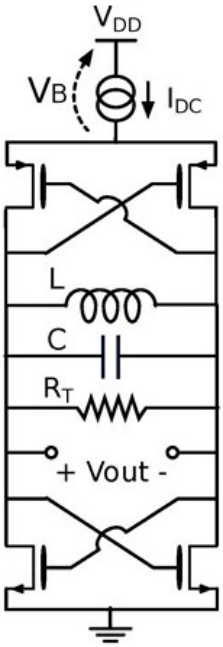

FIGURE 1.4: Class B VCO from [13].

structures like Class E [62] are not included. Nonetheless, in table 1.1 all topologies have been analyzed and the conclusion is that the best power efficiency belongs to Class B+Tail.

Out of fairness, one must note that Class B is a simple, robust, efficient architecture, whose performance may be improved through AC biasing [13]. Class B, depicted in Figure 1.4, can be regarded as the basic building block for this kind of VCOs. Due to its simplicity and robustness is often used for high-performance implementations [55], [56].

Class B + Tail, shown in Figure 1.5, is an evolution of class B as it features better energy efficiency and additional PN filtering thanks to the tail tank, whose resonance is put at twice the oscillting frequency. Thanks to the tail tank, the ratio between gm and current is optimized for the transistors, whose source can go even beyond supply, staying in saturation and maximizing η_P [14]. Of course, as there is another tank necessary, it requires additional area and complexity. If the second tank is intertwined with the first, area can be saved whereas complexity explodes due to the magnetic coupling between main and tank inductors [63]. Another variation to save area is to implement both main and tail LC with the same physical tank, realizing an implicit tail as in [57].

As this is a truly versatile topology, it will be adopted in our work and discussed more in detail in later subchapters. The limit resides in the unavoidable link between main and tail inductances, as the first is the differential mode (DM) inductance of the physical L, while the second is the common mode (CM) one. Being DM and CM strictly related, it is difficult to correctly tune the tail at high frequency.

If tail is not tuned properly, it reveals destructive for PN performance. Consequently, Q and PN of class B with implicit tail will be limited, as shown in Figure 1.6. Another issue is the tail robustness, even if it can be increased through additional design complexity [58].

Class C (Figure 1.7) is a topology that can combine AC biasing with a tail filtering capacitor, which consistently shapes the current, thus improving its efficiency. With a bigger tail capacitor, the power saving will also be more consistent; the capacitor also

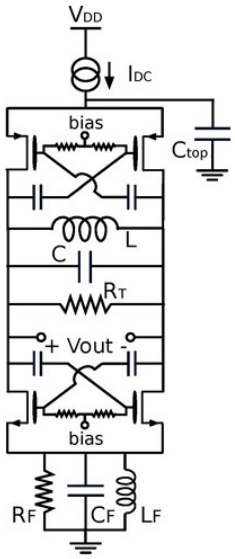

FIGURE 1.5: Class B + tail VCO from [13].

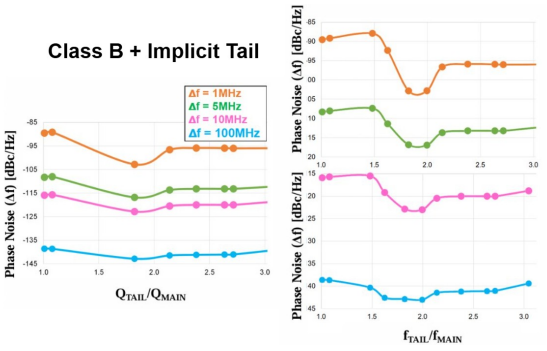

FIGURE 1.6: Q and PN performance in a class B + implicit tail VCO.

filters noise at twice the oscillating frequency. Its main drawback resides in its difficult start-up, which is why hybrid Class B/Class C topologies have been proposed [64].

Class F (Figure 1.8) is somehow similar to Class B + Tail as it is a topology exploiting a second resonance, but -instead of filtering second harmonic- it focuses on PN at the third harmonic, thus having the additional tank at three times the oscillating frequency [65]. Although it is a robust topology, its power efficiency is inferior to the Class B + Tail. The same area considerations hold for Class F. In an attempt to improve its performance, new hybrid topologies have been proposed [66], [67] to get both Class F and Class B + Tail advantages.

Class D [61] is another topology, often transformer-based, as shown in Figure 1.9, and its output voltage, instead, can go up to three times the supply. Despite the large oscillation amplitude impact on reducing the phase noise, the fact that transistors are employed as switches, operating in deep triode, aims at achieving negligible resistance for lower phase noise. Such a low resistance may be extremely difficult to be realised in practical implementations. By reaching such a great output amplitude, there is also the risk of destroying the transistors and of SOA failures.

Class E (Figure 1.10) is a high power efficient topology with a relatively simple complexity, featuring a specially designed resonant load network aiming at zero-voltage -and

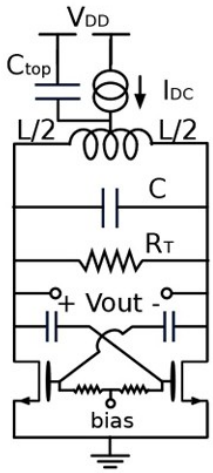

FIGURE 1.7: Class C VCO from [13].

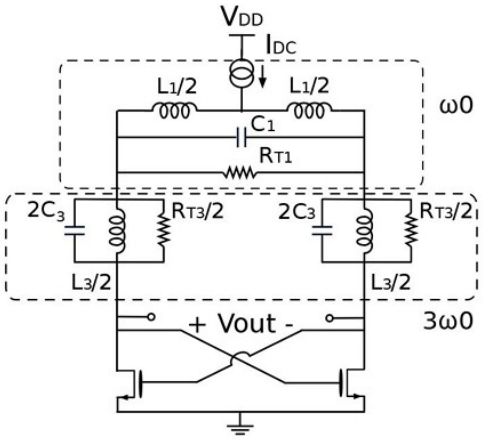

FIGURE 1.8: Class F VCO from [13].

ideally zero-voltage-slope- switching, thus minimizing switching losses. As other VCOs, it can oscillates in two modes: free-running and synchronized (or injection-locked oscillation) modes. Synchronization grants both higher overall efficiency and oscillation stability [62]. All these names come from the power amplifiers classification and were later adopted for oscillators too.

1.1.1 Oscillators State of the Art

A second classification, focused on architectural purposes, is presented: many recent oscillators (2022-25) oscillators have been analyzed and divided into three categories, huge tuning range, multi-core and extremely high-frequency oscillators.

The first category include VCOs with huge TR, generally more than 50/, which are designed to cover large band and to serve multi-purpose systems. Their high TR -in some cases close to 100/ [75], [76]- derives from their being multi-bands oscillators, as in Figure 1.12. The cost of a huge TR is often area and, more importantly, unusual shapes (Figure 1.13) which make difficult to couple multiple core, thus making these structures weaker under the PN aspect.

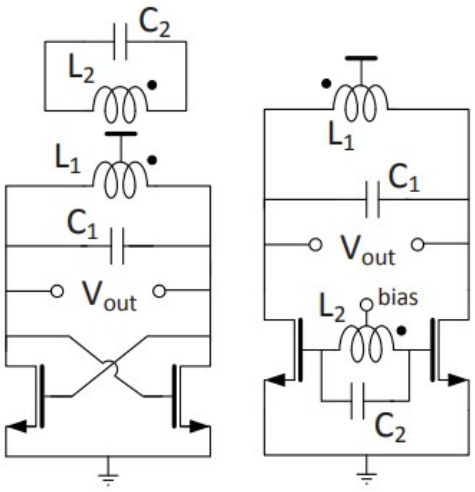

FIGURE 1.9: Class D VCO from [60].

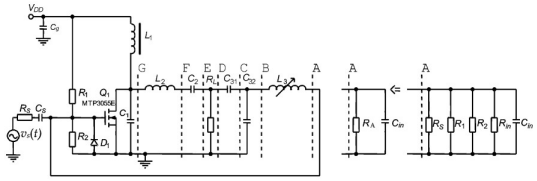

FIGURE 1.10: Class E VCO from [62].

The second category is denominated multi-cores as comprehends all those architectures preoccupied with lowering PN, thus coupling from 2 to indefinite number of cores; although it is rather unusual to have more than 16 cores, also due to power and area considerations. Apart from that, this label indicates various oscillators, different in both topologies and applications. Under this tag, we will include also the present work. During latest years, this category has been the most studied and each stand-alone oscillator has been meticolously optimized till FoM of nearly 200 (seen in Figure 1.14), approaching the physical limits.

Even if it is not a multi-core architecture, also series tank oscillators may be included in this category as it is a strategy to break the well-known power-noise trade-offs in oscillators. Although most of the series tank related works revolves around single core VCOs [68], [77], there are some attempts to couple multiple series tank [79] and this already prefigures as the way to further push the efficiency of this topology. The biggest

TABLE 1.1: Topologies Efficiency.

	Class B	**Class B + Tail**	**Class C**	**Class F**	**Class D**	**Class E**
current efficiency	$\frac{\sqrt{2}}{\pi}$	$\frac{\sqrt{2}}{\pi}$	$\frac{1}{\sqrt{2}}$	$\frac{\sqrt{2}}{\pi}$	$\frac{\sqrt{2}}{\pi}$	$\frac{\sqrt{2}}{\pi}$
voltage efficiency	$\sqrt{2}(1-\frac{V_B}{V_{DD}})$	$\frac{\pi}{\sqrt{2}}(1-\frac{V_B}{V_{DD}})$	$\frac{1}{\sqrt{2}}$	$\frac{4\sqrt{2}}{\pi}(1-\frac{V_B}{V_{DD}})$	$\sqrt{2}$	$\frac{1}{\sqrt{2}}$
power efficiency	$\frac{2}{\pi}(1-\frac{V_B}{V_{DD}})$	$(1-\frac{V_B}{V_{DD}})$	$\frac{1}{2}$	$\frac{8}{\pi^2}$	$\frac{2}{\pi}$	$\frac{1}{\pi}$

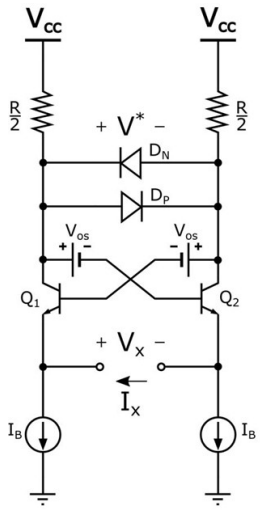

FIGURE 1.11: Implementation of series resonator from [68].

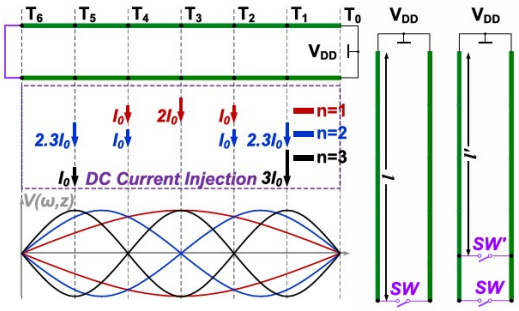

FIGURE 1.12: Implementation of large TR VCO with multiple bands from [75].

flaw of series resonator resides in its start-up difficulty, often solved by employing bjt instead of mosfet transistors, as in Figure 1.11.

The last category regars extremely high-frequency oscillators, i.e., overcoming 80GHz. The applications are usually areospace, defense or very specific industrial products, thus robustness is a prority compared to performance. In fact, due to such elevated frequencies, Q and FoM will drop significantly with respect to the previous categories.

These categories performance may be observed in Table 1.2.

In conclusion, as shown from these classifications, stand-alone oscillators cover a wide variety of different structures, whose characteristics have been long studied, but after the clock generation the bottleneck remains its distribution, which risks endangering all the mentioned advantages.

1.2 Coupling Methods

Coupling is a key method to improve PN performance as it allows to efficiently trade-off noise versus power: if the number of coupled oscillators doubles, then PN is lowered by 3dB. In reality, such a neat exchange between PN and power happens only if the coupling is perfect, i.e., there is no magnetic coupling between inductors or other interferences

TABLE 1.2: Recent Oscillators Topologies.

	Mazzanti [68]	**Jia [69]**	**Gong [70]**	**Guo [71]**	**Shu [72]**	**Wu [73]**	**Zhan [74]**	**Kang [75]**	**Ge [76]**	**Chen [77]**	**Guo-Qin [78]**
year	2022	2022	2022	2023	2023	2023	2023	2024	2024	2025	2025
type	series	multi-core	huge TR	very high freq	multi-core	multi-core	multi-core	huge TR	huge TR	series	series
technology	55nm	22nm	22nm	65nm	40nm	65nm	65nm	40nm	65nm	28nm	65nm
cores	1	16	2	4	4	2	4	1	4	1	1
frequency [GHz]	10	53.6	16.8	83.3	30.3	14.3	25.8	21.9	41.5	9.9	9.12
TR [%]	9	11.6	80.6	20.9	17.59	21.7	18.2	84.4	101	20	17.7
P [mW]	600	107	13.5	63.7	12	5.6	19.7	14.8	8.8	36.3	164
PN(Δf) [dBc/Hz]	-138 (1MHz)	-136 (10MHz)	-128.7 (10MHz)	-124 (10MHz)	-136.4 (10MHz)	-119.2 (10MHz)	-138 (10MHz)	-131.1 (10MHz)	-124.4 (10MHz)	-124 (1MHz)	-152.89 (10MHz)
FoM(Δf) [dB]	190 (1MHz)	186.7 (10MHz)	185.1 (10MHz)	184.3 (10MHz)	194 (10MHz)	192.8 (10MHz)	193.3 (10MHz)	184.8 (10MHz)	184.4 (10MHz)	191.4 (1MHz)	190 (10MHz)

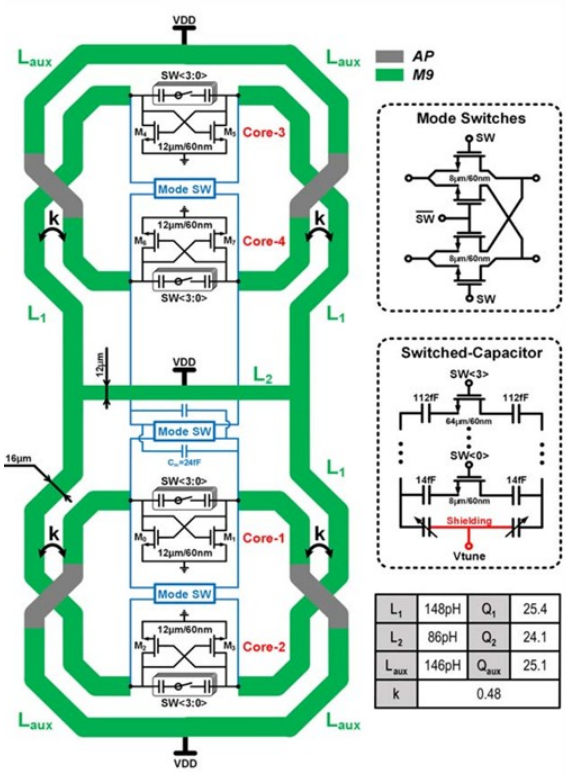

FIGURE 1.13: Implementation of large TR VCO with unusual inductor shape from [76].

ruining the 3dB gain. In order to realize an efficient coupling, multiple factors should be considered: first, if the coupling is to be active or passive due to power consumption, second, the area involved in the coupling, third, any eventual magnetic or capacitive coupling.

First, an active coupling is banally power consuming, while a passive coupling requires no additional power, thus making this the optimal choice for our target. It can be proved that active coupling may be more advantageous than passive one in terms of PN under certain conditions, as shown in Figure 1.15 [56]. Second, the area involved is up to the coupling strategy, in this subchapter some examples will be presented. Third, magnetic and capacitive couplings are a concrete risk: magnetic couplings depend on a coupling factor (k) which is a function of the two nearby inductors and their mutual inductance, the closer the inductors, the higher k will be; capacitive coupling is much less common and is mainly due to parasitics.

Nowadays. as jitter specifications become more and more demanding, coupling a great number of oscillators represents a valid solution to significantly lower PN [39], [55]. Doubling the number of oscillators ensures a 3dB PN reduction if perfectly handled, this is the case of shorted VCOs [55]. Shorting oscillators is an efficient passive coupling method as it is simple but robust, therefore widely adopted. The only possible drawbacks are that the inductors may have a high k if they are too close or, alternatively, if the shorting line is too long it may add parasitic resistance, which is usually negligible if much smaller than the tank resistance [55]. As these coupling resistances should be kept low, VCOs usually does not occupy a large area.

In general, passive coupling may be implemented through small resistors -i.e., shorts-, t-lines (in which case the oscillator is no longer a stand-alone but a hybrid topology

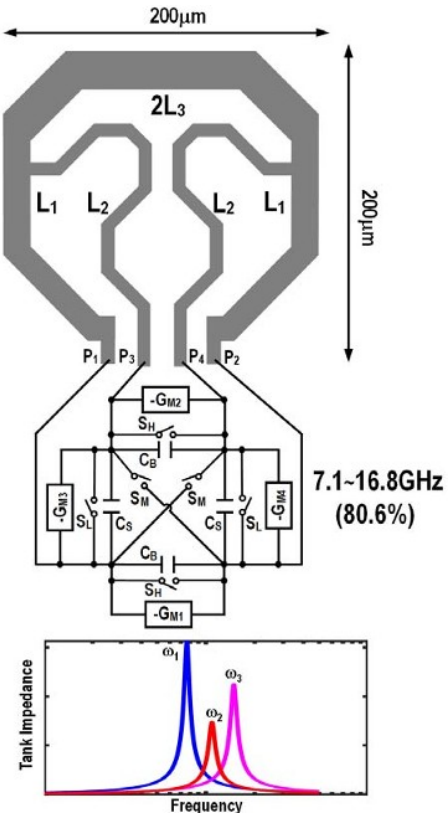

FIGURE 1.14: Implementation of multi-core high-FoM VCO from [70].

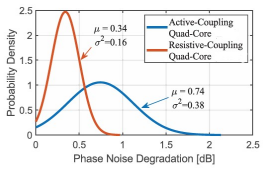

FIGURE 1.15: Probability density function of phase noise degradation due to passive or active VCO coupling from [56].

at the very least) or inductive-coupling [59]. Small resistors ensures highest efficiency but they are not always possible, especially because oscillators may disturb each others when they are too close; in order to avoid such an occurrence, "flower-coupled" VCOs have been designed [39]. Although "flower-coupled" structures grant excellent Q and great performance, their area occupance is not negligible and their unusual shape makes them unsuitable for most of commercial products due to the space requirements. Another valuable solution is inductive-coupling, despite the higher possibility of mismatches and losses in the 3dB improvements. To have a visive and intuitive comparison between these topologies, you can observe [55] in Figure 1.16, [59] in Figure 1.19, [39] in Figure 1.18.

Active coupling may be seen as an intermediate solution as it trades off some power for PN and it can be more flexible regarding area as VCOs are not so close to risk inductive couplings nor so distant to have significant parasitic resistance. [56] is a good example of successful active coupling for multiple cores, as shown in Figure 1.17.

Instead, hybrid topologies may share the distributed architectures foe, i.e., the more modest Q. For instance, t-line coupling does degrade the overall quality factor -and thus

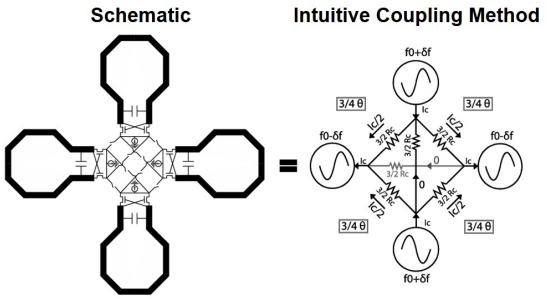

FIGURE 1.16: Resistive coupled VCOs from [55].

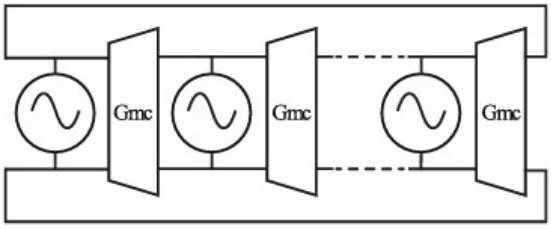

FIGURE 1.17: Active coupled VCOs from [56].

PN- but does not impact power and allows clock distribution in different area extensions. The area can be linear [20], [81] or a square [80], [30] or can be modified as it fits the chip. The distribution feature plus its flexibility makes it a viable solution, despite Q degradation and eventual couplings shown in Figure 1.20.

1.3 PN Mechanisms and Limitations

Phase noise (PN) is the frequency transposition of clock jitter. Looking at the frequency spectrum, a general noisy clock presents symmetrical skirts of noise around the center frequency, i.e, the car rier and PN is defined as the ratio of sideband noise energy -measured at a certain frequency offset from the carrier- to the peak carrier energy [1]. Its unit of measurement is decibels relative to the carrier, dBc/Hz, as the sideband energy is integrated over a 1Hz BW. Clock jitter depends on random components and deterministic clock spurs; the first is to be determined through PN analysis, while the second -even if relevant- is to be studied separatedly. Generally, there are both phase and amplitude noise contributions in a VCO, but most oscillators manage to suppress the amplitude noise near the carrier frequency [52], thus making PN the most significant contribution. As previously described, PN is the ratio of noise skirts with respect to the carrier, as shown in Figure 1.21, and its spectrum can be theoretically divided into three major regions: a 30dB/dec region, a 20dB7dec region and a flat region. The first region displays a slope of 30dB/dec as it is mainly composed of flicker noise, which depends on the inverse of the carrier frequency. The second region slope is 20dB/dec as it is mainly influenced by thermal noise, which is linked to the first region through a flicker corner. Finally, the third region exhibits a flat line as it represents white noise which is not modulated by the carrier.

Traditionally, PN can be modeled through Leeson's formula, one of whose semplified form,

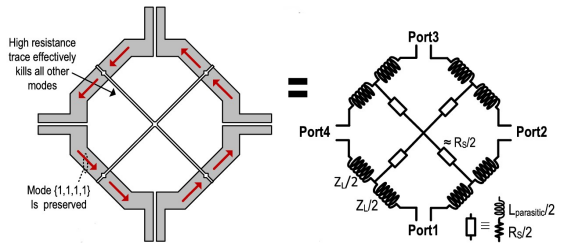

FIGURE 1.18: "Flower"-coupled VCOs from [39].

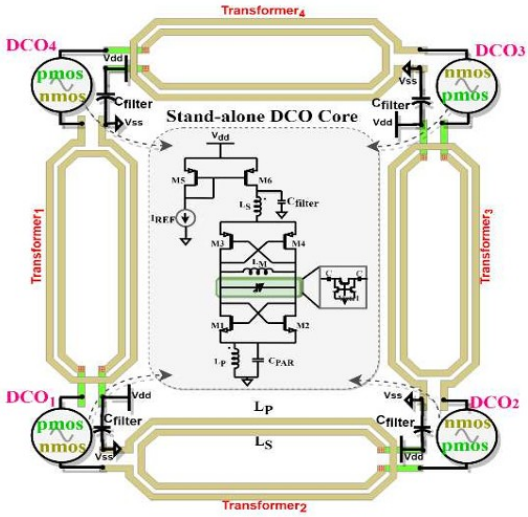

FIGURE 1.19: Inductive coupled VCOs from [59].

$$L(\Delta\omega) = 10log(\frac{2FkT}{P}((\frac{\omega}{2Q\Delta\omega})^2 + 1)(\frac{\omega_C}{\Delta\omega})) \tag{1.6}$$

which takes into account the major players and provide the flicker and thermal components defining PN spectrum three regions. In this equation, *omega* stands for the oscillating frequency, whereas $\Delta\omega$ for the frequency offset and ω_C represents the flicker corner. To consider it qualitatively, this expression can be simplified as $PN(\Delta\omega) \propto \frac{kT\omega}{CQV_{out}^2(\Delta\omega)^2}$. PN, thus, is scaled by a factor F, i.e., a circuit specific noise factor, which is specific for each oscillator topology in terms of device sizes, current, and other circuit parameters [37]. To analyze -at least intuitively- of PN in an oscillator works, start considering an ideal LC tank, composed of an inductor (L) and a capacitor (C). In this case, the noise factor (F) is 1 as an ideal tank is lossless, thus the oscillator has zero PN due to the infinite tank Q. Unfortunately, real LC tanks do have losses, symbolized by a finite Q, therefore an active element realizing a negative resistance is necessary for oscillation. For instance, one can refer to a class B oscillator for simplicity. As explained in [37], tank losses are expressed through a finite resistor (R) parallel to LC, while the compensating negative resistance (-R) is provided by a gm element, i.e., the transistor crosscouple. Noise contributions from R and -R are equal but uncorrelated, causing the factor 2 in Leeson's formula. The average negative resistance over a full cycle is equal to the tank loss even if it might be operative only over small portions of the oscillation cycle [37]. Supposing that F relative to the non-linear circuit realizing -R is γ, then F relative to the

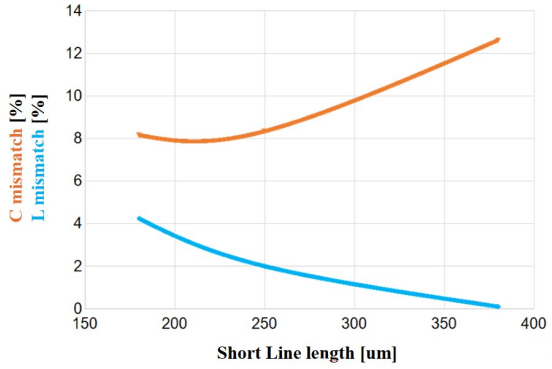

FIGURE 1.20: Mismatches due to inductive and capacitive couplings in t-line coupled VCOs.

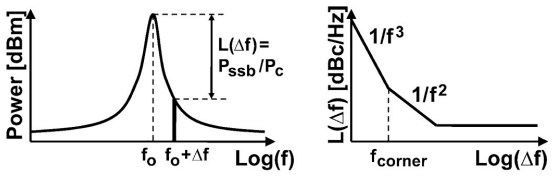

FIGURE 1.21: Clock power spectrum and PN characteristics from [1].

whole oscillator must be $F = 1 + \gamma$. Once defined this noise factor, one should not forget about the biasing circuits, which may significantly contribute to F.

In a tuned oscillator, if the -gm, provided by transistors, becomes higher than the positive loss conductance the natural response of the circuit is a growing oscillation, which will be eventually limited in amplitude by the oscillator non-linearities. Their origin may be different due to biasing -voltage or current-, leading to current-limited or voltage-limited modes [37], even if the ultimate limit remains noise. As proved in [83], Leeson's oscillator's noise factor is

$$F = 1 + \frac{4\gamma IR}{\pi V_{out}} + \frac{4}{9}\gamma g m_{bias} R \tag{1.7}$$

where I and gm_{bias} comes from the biasing circuit, R represents the tank losses, while γ is the channel noise coefficient of the transistor, traditionally set at $\frac{2}{3}$ for long-channel FETs and larger for shorter channel FETs. F comprehends three main noise contributions, from the tank, the transistor cross-couple and the biasing circuitery, with the second contribution being independent of the FETs sizing. Usually LC oscillators achieves a high quality factor, making the biasing the heaviest contribution. By neglecting the third contribution and considering that $V_{out} \propto RI$, then F is reduced to its minimum, i.e., $F_{min} = 1 + \gamma$. F_{min} reflects the situation where the circuit is in steady state. In this condition, the noise spectral density is the same as for a linear resistor and the noise can be written as $\hat{i_n^2} = \frac{4kT\gamma}{R}$. In general, F third term is not to be neglected as it can raise the noise factor up to 75% [37].

In general, PN may be described through models like the Hajimiri's model [52], based on the impulse sensitivity function (ISF), and the Demir's model [84], based on the decomposition of noise perturbations into phase and orbital components. Hajimiri has been more succesful during the years. As Class B + Tail pn VCO was previously selected as

one of the most efficient topologies for our purpose, some result for this architecture will be reported. ISF theory deals with a linear time-variant (LTV) noise-to-phase-noise conversion. Then, consider the phase error ($\Delta\phi_{in}$), a function of the time instant (t) when the charge pulse is injected, proportional to the Impulse Sensitivity Function (Γ_{in}).

$$\Delta\phi_{in} = \frac{\Gamma_{in}(\omega t)\Delta q}{q_{max}} \tag{1.8}$$

In the above equation, Δq represents the charge applied across one of the capacitors, producing a steady state phase error in the oscillator, q_{max} is the maximum charge across the capacitor placed between the nodes of interest, a normalizing factor. Instead, the ISF can be expressed in terms of state-space vectors as in [85]. Also, $\mathbf{X}$ is defined as in [85].

$$\Gamma_{in} = \omega \frac{q_{max}}{\Delta q} \frac{\Delta \mathbf{X}_{in}\mathbf{X}}{|\mathbf{X}|^2} \tag{1.9}$$

Once noise to PN, ISF and noise sources phase responses have been studied, a general expression for phase noise given by a white current noise source in a LC oscillator is proposed:

$$L(\Delta\omega) = 10log(\frac{\Gamma^2_{in,rms}\frac{\hat{i}^2_n}{\Delta f}}{2(q_{max}\Delta\omega}^2) \tag{1.10}$$

.

As reported in [13], this formula, referring to a single lossy LC tank, can be extended to the case of multiple tanks. In particular, in the case of a pn Class B + tail VCO, where the two tanks are the main (LC) and the tail ($(LC)_{tank}$), the ISF state-space vectors will be the following [13].

$$\mathbf{X} = [V_{out}, \sqrt{\frac{L_{tank}}{C_{tank}}}I_{tank}, \sqrt{\frac{C_{tail,n}}{C_{tank}}}V_{tail,n}, \sqrt{\frac{L_{tail,n}}{C_{tank}}}I_{tail,n}, \sqrt{\frac{C_{tail,p}}{C_{tank}}}V_{tail,p}, \sqrt{\frac{L_{tail,p}}{C_{tank}}}I_{tail,p}] \tag{1.11}$$

$$\mathbf{x}_{in} = [V_{out}\sin(\omega t),\ V_{out}\cos(\omega t),\ V_{tail,n}\sqrt{\tfrac{C_{tail,n}}{C_{tank}}}\cos(2\omega t),\ V_{tail,n}\sqrt{\tfrac{C_{tail,n}}{C_{tank}}}\sin(2\omega t),\ -V_{tail,p}\sqrt{\tfrac{C_{tail,p}}{C_{tank}}}\cos(2\omega t),\ -V_{tail,p}\sqrt{\tfrac{C_{tail,p}}{C_{tank}}}\sin(2\omega t)] \tag{1.12}$$

Thus, ISF for nmos and pmos transistors from the active part can be rewritten as in the following expressions.

$$L_n(\Delta\omega) = 10log(\frac{4kT\gamma_n I_{out}}{2(\Delta\omega)^2 V_{out}} \frac{(\frac{1}{4} + \frac{4V^2_{tail,n}C_{tank}Q_{tail,n}}{V_{out}C_{tank}Q_{tail,n}})}{(V_{out}C_{tank})^2(1 + 4\frac{C_{tail,n}}{C_{tank}}(\frac{V_{tail,n}}{V_{out}})^2 + 4\frac{C_{tail,p}}{C_{tank}}(\frac{V_{tail,n}}{V_{out}})^2)}) \tag{1.13}$$

$$L_p(\Delta\omega) = 10log(\frac{4kT\gamma_p I_{out}}{2(\Delta\omega)^2 V_{out}} \frac{(\frac{1}{4} + \frac{4V^2_{tail,p}C_{tank}Q_{tail,p}}{V_{out}C_{tank}Q_{tail,p}})}{(V_{out}C_{tank})^2(1 + 4\frac{C_{tail,p}}{C_{tank}}(\frac{V_{tail,p}}{V_{out}})^2 + 4\frac{C_{tail,p}}{C_{tank}}(\frac{V_{tail,p}}{V_{out}})^2)}) \tag{1.14}$$

Note that the FETs noise is proportional to the noise of the main tank by γ_n, γ_p, and other factors depending on the VCO design. These formulas account only thermail noise, from [13] it can be found an expression reporting not only thermal but also flicker noise, i.e., $L_{tot}(\Delta\omega)$. For more analysis concerning flicker noise, read [86].

$$L_{tot}(\Delta\omega) = 10log(\frac{kT}{2P}(\frac{\omega}{\Delta\omega Q_{tank}})^2 \frac{1 + \frac{\gamma_n+\gamma_p}{2}(1 + 16\frac{C_{tail}}{C_{tank}}\frac{Q_{tank}}{Q_{tail}}(\frac{V_{tail}}{V_{out}})^2) + 16\frac{C_{tail}}{C_{tank}}\frac{Q_{tank}}{Q_{tail}}(\frac{V_{tail}}{V_{out}})^2}{(1 + 8\frac{C_{tail}}{C_{tank}}(\frac{V_{tail}}{V_{out}})^2)^2}) \tag{1.15}$$

Practical PN measurements, instead, can be performed in different ways: direct or indirect measurement. As observable in Figure 1.21, direct measurement is conceptually simple but it does require the spectrum analyzer to operate at a setting with enough dynamic range to cover the carrier peak and the sidebands [1]. This kind of instrument trades off frequency range for resolution, thus it needs to be really expensive to guarantee good resolution and good frequency span. The other viable strategy, here called "indirect measurement", consists of mixing the carrier frequency down to an IF or baseband, while at the same time attenuating the carrier peak to reduce the necessary dynamic range. Nowadays, complex PN measurements are automated by modern spectrum analyzers and phase-noise meters and signal, nevertheless it remains a critical procedure [1].

1.4 Oscillators Mathematical Model

When it comes to understanding the oscillators behaviour, the easiest way is to develop a model, which can be used not only for explanations, but also for simulations and previsions. Once developed a model, then it can be applied to different architectures and topologies. In particular, three models were selected for their efficiency in describing three main aspect of a VCO: oscillation mode, stability and PN penalty. Now, we will proceed with the general introduction of these models, then use them to describe a particular case, i.e., two oscillators coupled through resistors, as in [55]. This represents the simplest -and strongest- coupling both conceptually and mathematically. Therefore, resistive coupling may be considered a starting point for the development and the understanding of coupled oscillators structures.

1.4.1 Mode Analysis Strategy

Mode analysis permits to calculate which modes exist for multiple coupled oscillators and to evaluate which one better suits our target. It can be carried out through the development of a mathematical model which examines the multiple cores and their coupling network. Once studied the different modes, in frequency and amplitude, one can understand which one may start up by applying Barkhausen conditions. In order to grasp the methodology, a designer may look at [39], where the coupling network is modeled throguh a Y matrix, while each VCO core is represented by a Y_{load} matrix. As shown in Figure 1.22, the load representing a VCO core is made of capacitive, C_T, and inductive part,L_T, of the tank, its resistive part,R_T, accounting for the tank losses, and the active element, g_m , representing the transistor cross-couple which acts as regeneration element. Out of simplicity, parasitic capacitance from transistors, i.e., active element, C_{MOS}, is included into the capacitive element of the tank, C_T. It is important as very often $C_{MOS} \approx C_T$, especially in FinFET technology. Regarding the model derivation, it is banal in this case as VCO core has a classic modelisation, while the coupling network consists of a single resistor R_L; on the contrary, more complex coupling networks requires other mathematical models which will be examined in the next chapters, when the necessity arises. In general, this model may be applied when controlled oscillators, represented by admittance y_T, are connected through passive networks, modeled with admittance matrix $\mathbf{Y}$, which is loaded by the N cores, i.e., $\mathbf{Y_L} = \mathbf{Y} + \mathbf{y_T}\mathbf{I}$, where $\mathbf{I}$ stands for the identity

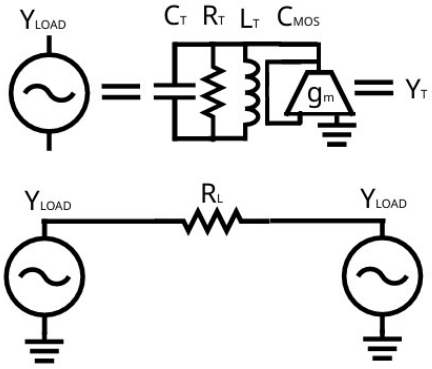

FIGURE 1.22: Resistance coupled oscillators model for mode analysis from [39].

matrix of sizing nxn. In this case, $N = 2$ to keep things simple and provide a clearer explanation. This model is general and describes a COs system accurately but its main limit resides in the calculation complexity and loss of intuitiveness when N explodes or the difficulty of modelling the coupling network increases. Following the previous equation, the condition for the system to work properly is oscillation and it is met when $Y_L V = \lambda V$, where the vector V is the tank voltage and λ is an eigenvalue. By definition, a $N - th$ order system has N possible oscillation modes, corresponding to N couples of eigenvalues and eigenvectors.

Therefore, oscillation condition can be rewritten as equation: $(Y_L - \lambda I)V = 0$. Such a condition may appear strange, but thinking at it from an intuitive prospect, you can understand that this condition points to oscillation as it indicates the area where active and passive elements balance each others or, more rigorously, where $R_{TANK} - R_{MOS} = 0$, hence causing oscillation. Moving forward, this expression may once again be rearranged into:

$$det(Y_L - \lambda I) = 0 \tag{1.16}$$

and from this equation it is possible to calculate each oscillation mode eigenvalue. As here $N = 2$, the calculation is easened by the fact that only two eigenvectors are feasible, i.e., $V = [1 \pm 1]$.

First, start by considering that the coupling is performed through R_L, so the load $[Y]_{R_L}$-or simply Y_L- can be computed as the following matrix.

$$[Y]_{R_L} = \frac{1}{R_L} \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix} \tag{1.17}$$

By solving the determinant equation, the next results may be found. It is important to remark that the equation should be divided into imaginary and real parts, with the imaginary part ultimately providing the oscillation frequency for each mode and the real part leading to the quality factor computation by giving an insight about each mode corresponding losses.

Eventually, the two possible solutions are denominated as phase (P), i.e., voltage vector equal to $[11]^T$, and counterphase (CP), i.e., voltage vector equal to $[1 - 1]^T$. Each one has its own corresponding eigenvalue (λ_i) and eigenvector. For the R_L coupling case, these expressions are reported below.

$$\lambda_P = 0 \tag{1.18}$$

$$\lambda_{CP} = \frac{2}{R_L} \tag{1.19}$$

$$\omega_P = \frac{1}{\sqrt{L_T C_T}} \tag{1.20}$$

$$\omega_{CP} = \frac{1}{\sqrt{L_T C_T}} \tag{1.21}$$

$$Re[Y_P] = \frac{1}{R_T} \tag{1.22}$$

$$Re[Y_{CP}] = \frac{1}{R_T} + \frac{2}{R_L} \tag{1.23}$$

By looking critically at the results, you may understand that the resistor-coupling network is a peculiar case as both P and CP share the same oscillation frequency despite being two entirely different modes. This happens thanks to their imaginary parts being exactly the same. On the contrary, their real parts appear different: P real part is given by the tank admittance, i.e., $\frac{1}{R_T}$, while CP has an additional contribution coming from half of the coupling admittance, i.e., $\frac{2}{R_L}$. You may immediately grasp that $Q_P > Q_{CP}$, hence P mode is the only feasible mode, being CP unable to start due to its bigger losses. Intuitively, you may see P mode as the natural oscillation mode of the single CO core as during P mode only the single VCO is to be considered, whereas in CP mode it is like having an equivalent tank made of the VCO plus half of the coupling resistor, meaning that during CP there is a parallel: $L_T//C_T//R_T//\frac{R_L}{2}$ for what concerns the losses.

The strength of resistive coupling, therefore, resides not only in its simplicity and robustness, but also in its being free of any mode ambiguity; from a theorical point of view, even if $N \to \infty$, the only effectively oscillating mode remains P. In general, you may affirm that the winning mode is always the one with the best quality factors, Q, even when $\omega_C \neq \omega_{CP}$. For different coupling methods, the issue of mode ambiguity represents a consistent issue, which will be further addressed in the next chapters, especially regarding Q and ω relationships.

1.4.2 PN Penalty Analysis Strategy

Coupling oscillators is mainly done to achieve a PN advantage, namely getting $3dB$ gain every time the number of cores doubles, which is why monitoring the PN performance is key design strategy for multi-core COs. Due to coupling non-idealities such as inductive or capacitive couplings or coupling network losses, the canonical $3dB$ may be reduced. As the additional power per core is not reduced, the trade-off between noise and power should always be considered in order to gain from multi-cores coupling. To monitor the behavior of coupled cores, a model like [55] can be adopted. To describe the cores behaviour, one can look at phase noise -or alternatively at FoM. PN is simpler to look at but FoM provides a global insight over the system performance, including not only noise but also power and frequency [81]. Beginning with PN-centered system shown in [55], noise degradation may be accounted for as a $30log(a_{tt})$ loss, where a_{tt} stands for attenuation due to imperfect coupling. This attenuation factor accounts for the coupling strenght with respect to the tank, as it -in facts- depends on the ratio between coupling and tank impedances. In this case, impedances are reduced to resistances.

$$PN_{2cores} = PN_{1core} - 3dB - 30log(a_{tt}) \tag{1.24}$$

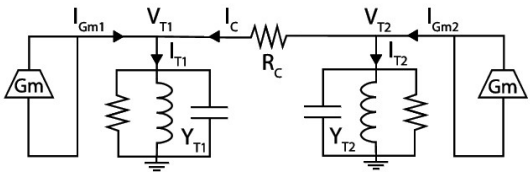

FIGURE 1.23: Resistively coupled oscillators model from [55].

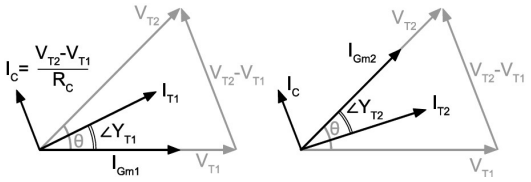

FIGURE 1.24: Voltage and current phasors in the resistively coupled oscillators system from [55].

$$a_{tt} = 1 + \frac{R_T}{R_L} - \frac{R_T}{R_L}\sqrt{1 - (sin(\theta_{12}))^2} \tag{1.25}$$

Such formulas can be validated through model Figure 1.23. As this model represents a system, coupling may be also different from resistive type shown here. As per tradition, tank is modelled through a parallel of $R_T//L_T//C_T$ and R_L is the coupling resistor, while G_m is the cross-coupled pair realizing the $-R_T$ necessary for oscillation.

Two of these tank models are employed to realize a dual core CO system. Now suppose that each tank have its own oscillating frequency, being f_1, f_2. As these frequencies come from similar tanks, they are extremely close but still different, i.e., $f_1 \approx f_2$. Even so, they can be roughly approximated as $f_1 \approx f_2 \approx f_0$. A mismatch $f_1 - f_2$ affects the oscillators, but it is so small that the oscillators are still locked, even if both working out of their natural resonance. The consequence is that the phase of Y_1 is not zero (Figure 1.24), but has a little error which can be neglected if the mismatch is small enough. Thus, in steady state the two cores are in phase, meaning that no current flows in the coupling path, hence the oscillation amplitude can be written as $A = \eta_I I_{DC} R_T$ [55]. The conclusion drawn from these affirmations is that the circuit is independent of the coupling resistance R_L provided that the frequency mismatch can be considered negligible. To look at the system in more detail, one can consider the formulas from [55], where the tank admittance is reported and approximated for negligible frequency mismatch. It is stated that frequency mismatch should be regarded as negligible as long as the true oscillation frequency of the system, i.e., $f_{osc} = \frac{f_1+f_2}{2}$, is close to the natural oscillating frequency of the system without mismatch. In mathematical terms, if $f_0 - f_{osc} << f_0$ holds true, then all the following approximations are valid.

$$Y_T = \frac{1}{R_T} + j\frac{Q}{R_T}\left(\frac{f_{osc}}{f_0} - \frac{f_0}{f_{osc}}\right) \approx \frac{1}{R_T} + j\frac{2Q}{R_T}\frac{f_{osc} - f_0}{f_0} \tag{1.26}$$

Although the mismatch is small, it still causes the tank voltage (V_T) and the tank current (I_T) to be phase-shifted. Being the tank current the sum of the transconductor contribution, which is in phase with V_T, and of the coupling current, it can be written as $I_T = \eta_I I_{DC} + \frac{V_{T1}-V_{T2}}{R_L}$. In order for the second component to be different from zero, the phase shift between the tank voltages V_{T1}, V_{T2} must be non-null as well. Such shift is

given by $\theta_{12} = arcsin(Kr)$ where $r = \frac{R_L}{R_T}$ and $K = Q\frac{f_0 - f_{osc}}{f_0}$. When COs are locked, then the steady state condition applies and the tank current may be calculated as $I_T = \eta_I I_{DC} + \frac{V_{T1} - V_{T2}}{R_L} = Y_T V_T$. Consequently, one can find the amplitude of the two tank voltages ($V_{T1} \approx V_{T2} \approx V_T$) and the corresponding attenuation (a_{tt}) as reported before.

$$V_T = a_{tt} A \tag{1.27}$$

$$a_{tt} = 1 + \frac{1}{r} - \frac{\sqrt{1 - (Kr)^2}}{r} \tag{1.28}$$

The key to this analysis is the ratio between the coupling and the tank impedances, r, whose value affects the frequency mismatch between the cores, the oscillation swing and a phase difference between the two tank voltage waveforms. All these behaviours are impacted by how big is r; if this ratio is small, meaning that $R_L << R_T$ then the alterations in phase and swing and the mismatch all become negligible and the system is comparable to a perfectly coupled double core system, oscillating at f_0.

Considering r, and thus a_{tt} non-negligible, then the oscillation amplitude will be reduced and the phase shift enhanced, with both leading to PN, and eventually FoM, penalty. The effect of the amplitude reduction can be roughly approximated as proportional to $\frac{1}{a_{tt}^2}$, while the effect of phase shift accounts for an additional $\frac{1}{a_{tt}}$. In conclusion, PN penalty is proportional to $\frac{1}{a_{tt}^3}$ and the same holds for FoM penalty, as reported in the formulas above. These non-idealities also impact the Impulse Sensitivity Function (ISF). Further details may be grasped by looking at current and voltage vectors and their precise evaluation in [55].

1.4.3 Stability Analysis Strategy

The last aspect to be examined in this text for the simplest CO coupling is their stability, althought this should be the first issue addressed in a real life situation as the oscillator system ought to be stable in its oscillating frequency. As mentioned before, the golden rule for starting the oscillation is to respect Barkhausen conditions, i.e., having a gain which is at least one and a phase shift being equal π or multiples, but wheather the starting oscillation will maintain and will not be changed is to be calculated. Intuitively, one can see that in a n cores system, there will be n possible oscillation modes, but not all of them will respect Barkhausen. A robust and trustworthy model to examine these oscillation mode and find out which one will prevail and which ones may be worrysome was provided by [87]. Looking at model in Figure 1.25, two identical cores are represented: each one has its own impedence and its own active part plus the coupling linking them together. Before analysing this model, which is the simplest way to study the stability of oscillation modes in dual cores CO systems, let us take a step back. First, picture two cores like the one shown in Figure 1.26 and consider each of them as having a complex current injected into the tank, i.e., $I_{inj} e^{j\theta_{inj}}$. Under this current injection condition, amplitude and phase of the tank impedance are depicted in Figure 1.26. Being this injection a sinusoidal input voltage, the result is a square-wave current with a fundamental peak of amplitude $\frac{4I}{\pi}$ [87]. Out of simplicity, all higher order harmonics -which are attenuated by the tank filtering properties- are neglected here, thus leaving only the contribution from the fundamental component. Without any injection, the VCO oscillates at its natural frequency given by $\omega_0 = \frac{1}{\sqrt{L_T C_T}}$ with an amplitude $\frac{4R_T I}{\pi}$, hence being a free-running oscillator. On the other hand, when an injection occurs, both oscillation amplitude and

phase appear disturbed, thus voltage gets this shape: $Ae^{j\theta_{inj}}$ with both A, θ_{inj} being functions of time. At the same time, the square wave current gets like this: $\frac{4I}{\pi}e^{j\theta_{inj}}$. By applying a KCL at the tank, the following equation is derived. Mark that $A = A(t)$ and $\theta = \theta(t)$.

$$\frac{Ae^{j\theta}}{R_T} + C_T\frac{d}{dt}(Ae^{j\theta}) + \frac{1}{L_T}\int Ae^{j\theta}dt\,dt = \frac{4I}{\pi}e^{j\theta} + I_{inj}e^{j\theta_{inj}} \tag{1.29}$$

This formula is called generalised Adler's equation and it can be further simplified in the less generatl case of weak injection.

$$\frac{d\theta}{dt} = \omega_0 + \frac{\omega_0}{2Q}\frac{I_{inj}\pi}{4I}sin(\theta_{inj} - \theta) \tag{1.30}$$

In our case, the first equation will be used to explain multi-core couplings as a special case of injection locking. First, a geometrical interpratation from [87] will be provided to gain deeper understanding of the subject, then some mathematical formulas -which can be easily generalised and applied to this work- will be presented. First, for some geometrical insights, the starting assumption is that injection at the natural oscillating frequency of the tank is strong enough to lock the two oscillators together. To follow this intuitive analysis, look at Figure 1.25, where currents from the tanks are represented as vectors. In particular, the total current in the tank, (I_t), is mathematically a $tan(\phi)$ afar from the tank voltage, which -in turns- causes an in-phase current of $\frac{4I}{\pi}$. It can be proved that -under these conditions- locking is successful if the injection signal is strong enough compared to the current I. The mathematical condition for locking is reported below.

$$\frac{I_{inj}}{I} \geq \frac{4}{\pi}\frac{|\Delta\omega|}{\sqrt{\Delta\omega^2 + (\frac{\omega_0}{2Q})^2}} \tag{1.31}$$

In the case of the dual core system, there exist two possible solutions, reported with "a" and "b" in Figure 1.27. Now, there are three possible cases: both of them are stable -which causes another problem: mode ambiguity-, none of them is -hence the system can not oscillate- or just one is stable. The third case is actually true as only the first mode can obtain a stable oscillation. To get a geometrical proof, one can insert a perturbation and look at the system response: if a small, positive disturbance is injected, a stable system will respond with a small, negative reaction to counterbalance the perturbation, whereas an unstable system will have a positive response or none at all. In the figure, one can observe that if the oscillation voltage is advanced by a small angle, then the first mode reduces the angle and the rate of rotation of tank voltage phasor slows down in opposition to the disturbance. On the other hand, when facing the same injection, the second mode has the tank voltage enhance its speed and it keeps on getting far away from its original phase. The obvious conclusion is that only the first mode is stable and this should be verified by applying the generalized Adler's equation. Of course, the inserted disturbance should be small, meaning that it cannot exceed the stability region indicated as figure "c" in Figure 1.27.

Second, this subchapter will move on to the mathematical explanation of stability regions, referring to the model in Figure 1.25. Starting from generalized Adler's equation, the balance of currents will be rewritten by considering that each core has its own amplitude and phase, hence first core has $V_1 = A_1e^{j\theta_1}$, while second core has $V_2 = A_2e^{j\theta_2}$. By assuming that the cores are the same and coupled, it may be drawn that $A_1 = A_2 = A(t) \approx A$ which can be considered as time-invariant in first approximation, although injection locking makes $\theta_1 \neq \theta_2$. Then. the transconductor-provided currents may be written as: $I_{gm_1} = I_{T1}Y_{12}V_2$ and $I_{gm_2} = I_{T_2}Y_{21}V_1$. Again, by assuming that the two tanks

are identical, the consequence is that $I_{gm_1} = I_{gm_2} = I_{gm}$, $I_{T1} = I_{T2} = I_T$, $Y_{12} = Y_{21}$. Proceeding by semplifying the KCL, the following equation is found.

$$\frac{V_1}{R_T} + C_T\frac{dV_1}{dt} + \frac{F}{L_T} + Y_{11}V_1 + Y_{12}V_2 = \frac{4I}{\pi} \tag{1.32}$$

In this equation, currents from the tank, i.e., currents over R_T, C_T, L_T, from the transconductor and the coupling are reported and their sum should be equated to $\frac{4\pi}{I}$, as explained in [55]. In particular, this formula can be rearranged by considering that F is the integral contribution of the current flowing over R_T, C_T, L_T, as written in Adler's equation. As the integral would be mathematically tricky, an alternative expression was provided by [88], which noted that this current looks like the differential equation of an RC LP filter, thus solved it by approximating the term F as $F \approx \frac{jA}{\omega_0^2}(\frac{d\theta_1}{dt} - 2\omega_0)$. Therefore, the previous equation may be rearranged as it follows.

$$\frac{A}{R_T} + C_T\frac{dA}{dt} + jC_TA\frac{d\theta_1}{dt} + \frac{F}{L_T} + Y_{11}A + Y_{12}Ae^{\theta_2-\theta_1} = \frac{4I}{\pi} \tag{1.33}$$

As this system features a resistive coupling, the admittance matrix is symmetrical and it has $Y_{11} = Y_{22} = \frac{1}{R_L}$ and $Y_{12} = Y_{21} = -\frac{1}{R_L}$. By substituting and applying the given approximations, Adler's formula looks like this.

$$\frac{A}{R_T} + jC_TA\frac{d\theta_1}{dt} + \frac{jA}{\omega_0^2L_T}(\frac{d\theta_1}{dt} - 2\omega_0) + \frac{A}{R_L} - \frac{Ae^{\theta_2-\theta_1}}{R_L} = \frac{4I}{\pi} \tag{1.34}$$

Then, real and imaginary parts should be split as in [88]. The results highlights the dependance of the voltage amplitude and the phase from the relative phase shifts between the tanks, i.e., $\theta_2 - \theta_1$.

$$A = \frac{4}{\pi}\frac{R_LR_TI}{R_L + R_T[1 - cos(\theta_2 - \theta_1)]} \tag{1.35}$$

$$\frac{d\theta_1}{dt} = \omega_0 + \frac{\omega_0}{2Q}R_TY_{11}sin(\theta_2 - \theta_1) \tag{1.36}$$

$$\frac{d\theta_2}{dt} = \omega_0 + \frac{\omega_0}{2Q}R_TY_{12}sin(\theta_2 - \theta_1) \tag{1.37}$$

At this point, the thing to do is to search for the oscillation modes. Being the system a dual core, two oscillation modes are expected, in order to find them, let us equate $\theta_1 = \omega_0 t$ and $\theta_2 = \omega_0 t + \psi$, where $\psi = \theta_2 - \theta_1$, and substitute them into expressions $\frac{d\theta_1}{dt}$ and $\frac{d\theta_2}{dt}$. Then, by solving these expressions for ψ, the two modes are found: phase oscillation mode (P), with the cores oscillating together with zero phase shift, i.e., $\psi = 0$, and counterphase mode (CP), with the two COs oscillating with opposite phases, i.e., $\psi = \pi$. Consequently, also their amplitude are different.

After finding P and CP modes, the proper stability analysis is to begin. As explained in [87], to understand whether a mode is stable or unstable, the simplest procedure is to inject a small, positive disturbance into the tank and then look if the system has a negative response. Mark that the system response is mathematically calculated as the derivative of the disturbance, i.e., $\frac{d\theta_d}{dt}$. For instance, consider the first tank and inject a disturbance θ_d, with $\theta_1 0\omega_0 t + \theta_d$ and $\theta_d << 1$. The corresponding result is that $\frac{d\theta_d}{dt}$ is always negative for P and always positive for CP. Therefore, phase mode is the only stable oscillation mode, while CP could never start nor take over. The same procedure may be applied to

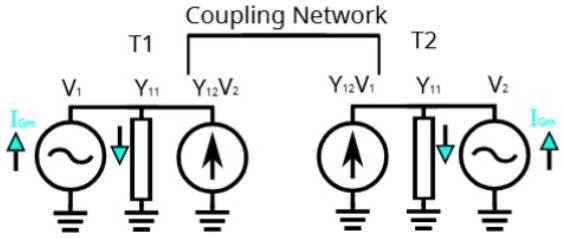

FIGURE 1.25: Two VCO core system for oscillation stability analysis from [87].

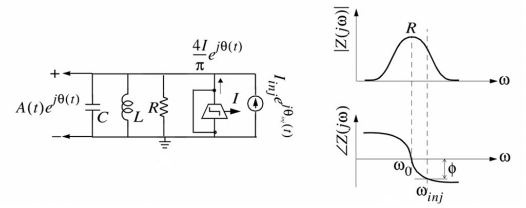

FIGURE 1.26: Single core under current injection with its amplitude and phase impedance behaviors from [87].

the second tank or, as a proof, one can apply simmetrical disturbances θ_{d1}, θ_{d2} and then observe $\frac{d(\theta_{d1}-\theta_{d2})}{dt}$.

As demonstrated here, this is a fast and secure way to prove the existance and the stability of an oscillation mode. Contrary to the geometrical intuitive view, the mathematical analysis may be easily applied to more complex systems, where stability regions can be found by applying the disequation $\frac{d\theta_d}{dt} < 0$ for a positive injected disturbance whose modulus remains way below unitary. For further details, studies and calculations from [89] and [90] may be examined.

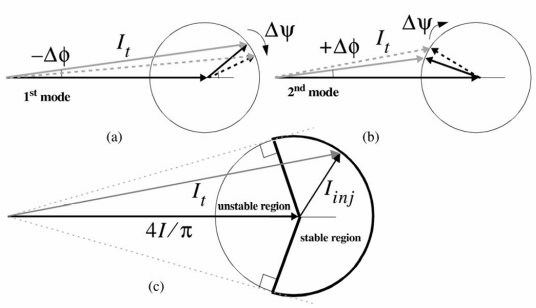

FIGURE 1.27: Geometrical representation of intuitive stability analysis for dual core system oscillating modes from [87].

Chapter 2

Coupled Oscillators Analysis

After reporting how a resistance-coupled dual-core system may be examined, other passive coupling networks are considered and looked into. All the considered couplings may be seen as a case of weak coupling from a mathematical point of view, thus it is fundamental to study the coupling network to ensure the robustness of the whole architecture. The presented analysis come from an engineering background, but a more rigorous and purely mathematical background may be adopted as well, under the hypothesis of a symmetrical weak-coupled multi-cores system. In this chapter, the analysis will be more focused on simplified -possibly through convenient approximation such as short coupling line and low loss approximations- systems in order to provide an intuitive and fast way of designing and understanding multi-cores oscillators.

2.1 Two-Cores Oscillator

In this chapter, the main subject will be how two cores can be coupled in a different way than resistive-coupling as the main goal of this work is to realize a robust, power saving oscillator with no mode ambiguity. First, some options for the coupling will be introduced and examined for what it concerns existing oscillation modes, FoM penalty and stability. Then, the focus will shift to the four cores as all the analysis for a dual core system may be extended to a n cores system. For simplicity, the dual core may be considered as the unitary piece for the construction of a more complex CO coupling system. Thus, the target is to show that by studying two cores one can intuitively understand how n cores will behave and avoid heavy computations with matrices and complex equations. In particular, our two cores will focus on some selected cases: resistive coupling -only mentioned as it was examined in the previous chapter-, small connections, which can be modelled through T or Π models, with resistors, capacitors and inductors, and longer connection, modelled as transmission lines (t-lines), starting from the classical mathematical modelling for these architectures. Note that all these models -T, Π and t-lines- have the advantage of being scalable, hence the procedure may be to characterise a dx of the total lenght of the coupling connection and then to step it for the length of the total link. By adopting such a method, the designer would be ready for any change -be it minimal or extensive- of its coupling structure.

Other couplings, for example through capacitors or inductors only, may be seen as a simplified T or Π models connections, where only a type of passive and two symmetrical resistive elements are placed. For instance, [59] may be modelled in this manner. Instead, rotary wave architecture might adopt the more sophisticated t-line model but with the additional care of considering the first and the n-th tanks connected together to form a circle.

TABLE 2.1: Two Core with different Coupling Networks

Y Model	**General Results**		
	λ_P	ω_P	$Re[Y_P]$
R_L	0	$\frac{1}{\sqrt{L_T C_T}}$	$\frac{1}{R_T}$
T	$\frac{1}{Z_L+2Z_C}$	$\sqrt{\frac{2C_TL_T+C_LL_L-\gamma}{2L_TL_LC_TC_L}}$	$\frac{1}{R_T}+\frac{R_T(\omega C_L)^2(2R_C+R_L)}{4}$
Π	$\frac{1}{Z_C}$	$\frac{1}{\sqrt{L_T(C_T+C_L)}}$	$\frac{1}{R_T}+\frac{(\omega+C_L)^2R_C}{1+(\omega R_C C_L)^2}$
SWL*	$\frac{Y_0}{tanh(\gamma d)}-\frac{Y_0}{sinh(\gamma d)}$	$\frac{1}{\sqrt{((2C_T+C_L)\frac{L_T}{2})}}$	$\frac{1}{R_T}+\frac{R_L d}{4Z_0^2}$

$\gamma=\sqrt{(-2C_TL_T-C_LL_T-C_LL_L)^2-8C_TC_LL_TL_L}$.

Y Model	**General Results**		
	λ_{CP}	ω_{CP}	$Re[Y_{CP}]$
R_L	$\frac{2}{R_L}$	$\frac{1}{\sqrt{L_T C_T}}$	$\frac{1}{R_T}+\frac{2}{R_L}$
T	$\frac{1}{Z_L}$	$\sqrt{\frac{L_T+L_L}{L_TL_L(C_T+C_L)}}$	$\frac{1}{R_T}+\frac{R_L}{R_L^2+(\omega L_L)^2}$
Π	$\frac{2Z_C+Z_L}{Z_CZ_L}$	$\sqrt{\frac{2L_T+L_L}{L_TL_L(C_T+C_L)}}$	$\frac{1}{R_T}+\frac{R_LR_C+R_L^2+(\omega L_L)^2}{R_C(R_L^2+(\omega L_L)^2)}$
SWL*	$\frac{Y_0}{tanh(\gamma d)}+\frac{Y_0}{sinh(\gamma d)}$	$\sqrt{\frac{2L_L+L_T}{2L_LL_TC_T}}$	$\frac{1}{R_T}+\frac{R_L}{(\omega L_L)^2}$

* = These results come from low losses approximation.

Therefore, this three step analysis may be considered exhaustive -as it combines multiple different studies cited previously and takes the best results out of them- and applicable to all kind of coupled VCOs systems, including the ones listed in the first chapters. This analysis precedes the actual architecture review in order to lay the foundations for some of the design choices.

2.1.1 Mode Analysis

As stated before, mode analysis permits to calculate which modes exist for multiple coupled oscillators and to evaluate which one better suits our target. In this chapter, mode analysis will be carried out through the development of a mathematical model for a transmission-line, which examines two cores connected through T, Π and a t-line model, acting as their coupling network. Once studied the different modes, in frequency and amplitude, the target is finding the dominant mode which will surely start up and keep on oscillating.

The methodology, reported in [39], where the coupling network is modeled throguh a Y matrix, while each VCO core is represented by a Y_{load} matrix, is here applied to three different cases: T, Π and a t-line model. The table below reports their corresponding eigenvalues and oscillation frequencies.

Now let us take a step back and remind how the table results were calculated. As shown in Figure 1.22 and mentioned before, the load representing a VCO core is made of capacitive, C_T, and inductive part,L_T, of the tank, its resistive part,R_T, accounting for the tank losses, and the active element, g_m , representing the transistor cross-couple which acts as regeneration element. Out of simplicity, parasitic capacitance from transistors, i.e., active element, C_{MOS}, is included into the capacitive element of the tank, C_T. Regarding the model derivation, the VCO core has a classic modelisation, while the coupling network consists of a single resistor for the first case, i.e., resistive coupling R_L, of two identical inductors and a capacitor in the second case, i.e., the T model, and analogously for the Π model, the third case, which includes two identical capacitors and an inductance. Obviously, each passive element -be it capacitor or inductor- has its own associated resistance, representing their losses, in order for the model to be realistic. The

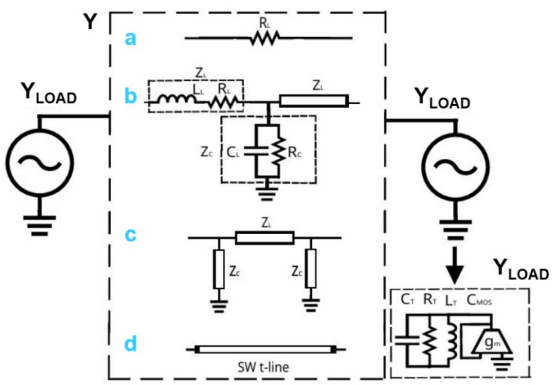

FIGURE 2.1: Frequency Model for different coupling methods: a) resistive coupling R_L, b) Π model, c) T model, d) SW t-line coupling.

fourth case, on the other hand, is a transmission line model which is computed starting from Conciauro's classic model, similarly to [91], [92].

As general introduction, it is correct to assert that this generical model may be applied when controlled oscillators, represented by admittance y_T, are connected through passive networks, modeled with admittance matrix $\mathbf{Y}$, which is loaded by the N cores, i.e., $\mathbf{Y_L} = \mathbf{Y} + \mathbf{y_T I}$, where $\mathbf{I}$ stands for the identity matrix of sizing nxn. In this case, $N = 2$ to keep things simple and provide a clearer explanation as this model main limit resides in the calculation complexity and loss of intuitiveness when N explodes or the difficulty of modelling the coupling network increases. The condition for the system to work properly is oscillation and it is met when $Y_L V = \lambda V$, where the vector V is the tank voltage and λ is an eigenvalue. By definition, a $N - th$ order system has N possible oscillation modes, corresponding to N couples of eigenvalues and eigenvectors.

Therefore, oscillation condition can be rewritten as equation: $(Y_L - \lambda I)V = 0$. Such a condition may appear strange, but thinking at it from an intuitive prospect, you can understand that this condition points to oscillation as it indicates the area where active and passive elements balance each others or, more rigorously, where $R_{TANK} - R_{MOS} = 0$, hence causing oscillation. Moving forward, this expression may once again be rearranged into:

$$det(Y_L - \lambda I) = 0 \tag{2.1}$$

and from this equation it is possible to calculate each oscillation mode eigenvalue. As here $N = 2$, the calculation is easened by the fact that only two eigenvectors are feasible, i.e., $V = [1 \pm 1]$.

According to Figure 2.2, the fourth cases previously described can be now visualized.In general, it can be stated that the coupling is performed through an impedance Z_L, which is different for each of the four cases, so the load Y_L- can be computed as the following admittance matrix.

$$[Y]_{Z_L} = \frac{1}{Z_L}\begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix} \tag{2.2}$$

By solving the determinant equation, the table results may be found. It is important to remark that the equation should be divided into imaginary and real parts, with the imaginary part ultimately providing the oscillation frequency for each mode and the real

part leading to the quality factor computation by giving an insight about each mode corresponding losses.

Even if the four cases are different from each other, all these equations have only two possible solutions, denominated as phase (P), i.e., voltage vector equal to $[11]^T$, and counterphase (CP), i.e., voltage vector equal to $[1-1]^T$. Each one has its own corresponding eigenvalue (λ_P or λ_{CP}) and eigenvector.

In other terms, when considering second, third and fourth cases, they are three different methods to model and represent transmission lines, with different complexity. The first two models have the advantage of being scalable and simples, while t-line model is more accurate but more complex. When it comes to t-line coupling the admittance matrix is a 2x2 matrix where, due to reciprocity and symmetry, $y_{11} = y_{22}$ and $y_{12} = y_{21}$. The eigenvalues of $\mathbf{Y}$ are easily found by solving the previously described equation. The resulting eigenvalues are $\lambda_P = y_{11} + y_{12}$ and $\lambda_{CP} = y_{11} - y_{12}$. λ_P correspond to an eigenvector $\mathbf{v} = [v_1 v_2]$. The corresponding $\lambda_{P,CP}$ are the eigenvalues of $\mathbf{Y}$, such that the given equation can be rewritten as $(\lambda_{P,CP} + y_T\mathbf{I})\boldsymbol{v} = \mathbf{0}$. For two cores there are two λ values satisfying such a condition. Every two core oscillating system has a phase (P) and a counterphase (CP) model, solving the equation for a vector $\boldsymbol{v}$. As explained in [81], P all oscillators have the same polarity, i.e., $\boldsymbol{v} = [1,1]^{\mathbf{T}}$,while in CP they have different ones, thus $\boldsymbol{v} = [1,-1]^{\mathbf{T}}$.

As said before, this work will focus on reciprocal and symmetrical networks, where $y_{11} = y_{22}$ and $y_{12} = y_{21}$ and consequently $\lambda_{P,CP} = y_{11} \pm y_{12}$. Oscillation frequency is calculated with $Im[Y_{tot}] = 0$, i.e. $\frac{-1}{\omega L_T} + \omega C_T + Im[\lambda_{P,CP}] = 0$, while quality factor also depends on $Re[Y_{tot}]$. Various case studies are reported in Table I, starting from the cores connected through R_L resistance [55] to our case, with SW t-lines. Mark that Π and T are just models for SW t-line. They proved their usefulness in granting a more intuitive and simpler to handle representation. Note that CP mode presents higher frequency and lower Q as in a parallel between the core RLC and the coupling network RLC, while P has lower frequency and higher Q. In P, Q is approximately the same as the single core as long as the t-line is relatively small compared to λ. The approximations gradually fades as the t-line length (d) gets bigger. When the lines can no longer be considered "short", but the low loss approximation still holds, frequency and Q may be found as graphical solutions to the following formulas, retrieving frequency from (2), (3) and real part from $\frac{1}{R_T} + \frac{Y_0^2 R_L d}{2cos(\omega_P\sqrt{L_L C_L}d)+2}$ for P and $\frac{1}{R_T} + \frac{Y_0^2 R_L d}{4} csc^2(\omega_{CP}\sqrt{L_L C_L}\frac{d}{2})$ for CP. In Fig.2.4, these equations are compared to SW t-line simulations.

$$\omega_P^2 C_T L_T + \omega_P L_T Y_0 tan(\omega_P\sqrt{L_L C_L}d) - 1 = 0 \tag{2.3}$$

$$\omega_{CP}^2 C_T L_T - \omega_{CP} L_T Y_0 cotan(\omega_{CP}\sqrt{L_L C_L}\frac{d}{2}) - 1 = 0 \tag{2.4}$$

According to the previous calculations, once chosen the desired oscillation mode the distance may be calculated according to the oscillation frequency. The corresponding lengths are given before for both P and CP, respectively, as shown in Figure 2.4.

$$d_P = \frac{\lambda_0}{\pi}\frac{\omega_T}{\omega_P} arctan(\frac{Z_T}{Z_0}(\frac{\omega_T}{\omega_P} - \frac{\omega_P}{\omega_T})) \tag{2.5}$$

$$d_{CP} = \frac{\lambda_0}{\pi}\frac{\omega_T}{\omega_{CP}} arctan(\frac{\frac{Z_T}{Z_0}}{(\frac{\omega_T}{\omega_P} - \frac{\omega_P}{\omega_T})}) \tag{2.6}$$

Note that, for the distance considered in this work, i.e., lower than 1.9mm, $Q_P >> Q_{CP}$ due to the t-line being relatively short, which favors P mode oscillation. To provide

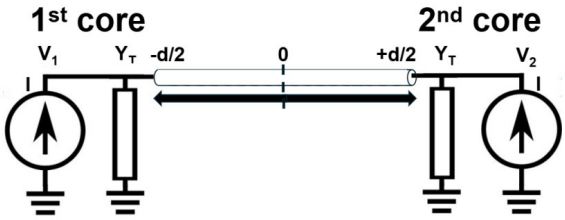

FIGURE 2.2: Model for two coupled oscillators for P, CP waves

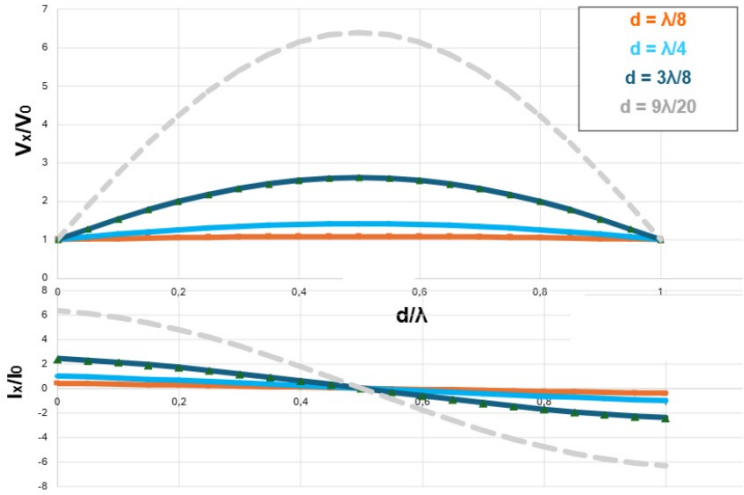

FIGURE 2.3: Voltage and current along SW t-line.

the numbers used in these calculations, the tank has $L_T = 140pH, C_T = 140fF, Q_T = 8.5$, while t-line has $Z_0 = 80\Omega, Q_L = 4$ at $27GHz$. From a more rigorous point of view, the Q and mode analysis may start from model in Figure 2.2. For P mode, the oscillators are connected to two $\frac{d}{2}$ shorted stubs, whereas the cores are connected to two $\frac{d}{2}$ open stubs in CP. Considering a t-line of total length d, the canonic voltage equation is found, which must be equal in amplitude and equal or opposite in phase -depending on the mode- in $x = 0$ and $x = d$. By equating the two expressions and solving, voltage amplitude along t-line is found, with $\psi = 0$ in P and $\psi = \pi$ in CP. Note that θ stands for the angle between the current vectors [55] and $V_0 = V^+ + V^-$.

Quality factor is defined as the ratio between ω_0 energy per cycle and power loss. In addition, Q can be calculated in different ways, for instance as the ratio between imaginary and real part of the total impedance (see the table). The results are the same and the formulas matches the simulations. In order to simplify the calculations, some approximation have been performed. In particular, if Q is calculated from the table formulas, the low loss approximation has been adopted; here it is the dispersion-less approximation. Same calculations may be carried out for the current, starting from $I(x) = \frac{V^+}{Z_0}e^{-j\frac{2\pi x}{\lambda}} - \frac{V^-}{Z_0}e^{j\frac{2\pi x}{\lambda}}$ till $I(x) = \frac{V_0}{Z_0 cos(\theta - \frac{\psi}{2})} jsin((\theta - \frac{\psi}{2})(1 - \frac{2x}{d}))$. These waveforms are reported in Figure 2.3.

In both cases, if no approximation is allowed the quality factor should be calculated as a weighted average of tank and transmission line contributions [38].

$$V(x) = V^+ e^{-j\frac{2\pi x}{\lambda}} + V^- e^{j\frac{2\pi x}{\lambda}} \tag{2.7}$$

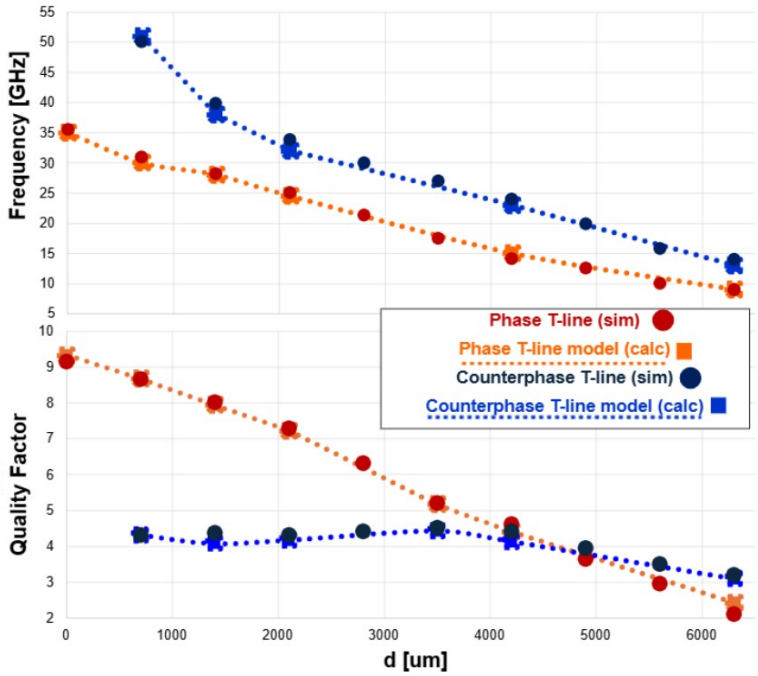

FIGURE 2.4: Frequency and Quality Factor (Q) for SW-tlines.

$$V(x) = \frac{V_0 cos((\theta - \frac{\psi}{2})(1 - \frac{2x}{d}))}{cos(\theta - \frac{\psi}{2})} \tag{2.8}$$

$$Q_P = \omega_P \frac{2C_T + \frac{C_L}{cos(\theta)}}{\frac{2}{R_T} + \frac{G_L}{cos(\theta)}} \tag{2.9}$$

$$Q_{CP} = \frac{G_L}{\omega_{CP}(C_L + C_T)cos(\theta) + \frac{2}{\omega_{CP} R_T (C_T + C_L)}} \tag{2.10}$$

By looking critically at the results, you may understand that the resistor-coupling network is a peculiar case as both P and CP share the same oscillation frequency despite being two entirely different modes, while the othe three cases have different amplitudes in P and CP modes. By comparing real and imaginary part, one can not only grasp the quality factor but also understand the main players. By playing with resistors and other passive elements, a designer may understand how to favour one mode over the other. In general, the target of this work is to favour P mode by making CP unable to start due to its bigger losses. Intuitively, you may see P mode as the natural oscillation mode of the single CO core as during P mode only the single VCO is to be considered, thus P mode has always a better quality factor than CP mode. On the other hand, CP mode may be seen as having an equivalent tank made of the VCO plus half of the coupling impedance Z_L, therefore incrementing the losses. The strength of P coupling, therefore, resides not only in its simplicity and robustness, but also in its superior quality factor. For coupling methods different than R_L, the issue of mode ambiguity represents a consistent issue, which will be further addressed in the next chapters.

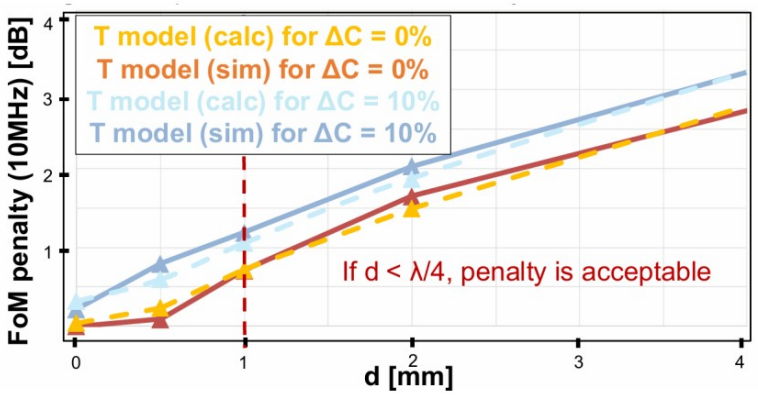

FIGURE 2.5: FoM penalty (10MHz) due to both mismatch and t-line.

2.1.2 FoM Penalty Analysis

Regarding the performance, as explained in the first chapter, the figure of merit (FoM) is the safest and most reasonable parameter to have a complete understanding of power, PN and frequency. As FoM does not decrease nor increase with multi-core couplings, provided that the coupling is ideal, thus giving the $3dB$ improvement in PN. For non-ideal couplings, the FoM is indeed reduced as the overall perfomance will worsen. As reported in the previous chapter, an empirical formula allows to estimate the FoM penalty based on the total line length (d) and the occurred mismatch [81].

$$FoM = FoM_{1core} + 30log(a_{tt}) \tag{2.11}$$

$$a_{tt} \approx 1 + r(1 + \frac{k}{2}) \tag{2.12}$$

$$r \approx \frac{R_L}{R_T + \frac{\omega L_L}{2}} \tag{2.13}$$

In particular, the above equation quantifies the penalty, where a_{tt} represents the attenuation factor, i.e., (17). Factor r is derived by the ratio between the tank and the t-line impedance. Instead, k is the coupling between the cores [87]. Generically, coupling is derived from Adler's formula: the following equations show how to calculate the coupling factor for both P and CP.

$$k_P \approx \frac{|\Delta\omega|}{\omega + 2Q|\Delta\omega|} \tag{2.14}$$

$$k_{CP} \approx \frac{|\Delta\omega|}{\omega - 2Q|\Delta\omega|} \tag{2.15}$$

Due to mismatches, the Figure of Merit is impaired as aforementioned, but also the output waveforms may have a slight phase shift (ξ), which is small enough that the Phase condition, i.e., $\psi \approx 0$, still holds true. In order to evaluate ξ, some calculations were performed with the entire mismatch (C_M) placed on core 2 for the sake of simplicity. Consequently, Q_{T2} is different from those of the other tanks. In particular, FoM attenuation is verified through Cadence simulations, as shown in Figure 2.5.

FoM penalty may be impaired by both mismatch and the nature of the transmission life itself, which represent a mismatch as the considered structure is not perfectly symmetrical, as it is not a rotary wave. Note that not even an enormous mismatch (e.g., 40%) may produce a significant ξ, such that P mode cannot change to CP due to mismatches.

$$\xi \approx k_c Q_{T2} \frac{R_L}{R_L + R_T} \tag{2.16}$$

$$k_c \approx \frac{C_M}{\sqrt{(C_T + C_L)(C_T + C_L + C_M)}} \tag{2.17}$$

$$Q_{T2} = \omega R_T (C_T + C_M) \tag{2.18}$$

Such formulas can still be validated through model Figure 1.23. As this model represents a system, coupling may be also different from resistive type shown here. As per tradition, tank is modelled through a parallel of $R_T//L_T//C_T$ and R_L is the coupling resistor, while G_m is the cross-coupled pair realizing the $-R_T$ necessary for oscillation. Two of these tank models are employed to realize a dual core CO system. Now suppose that each tank have its own oscillating frequency, being f_1, f_2. As these frequencies come from similar tanks, they are extremely close but still different, i.e., $f_1 \approx f_2$. Even so, they can be roughly approximated as $f_1 \approx f_2 \approx f_0$. A mismatch $f_1 - f_2$ affects the oscillators, but it is so small that the oscillators are still locked, even if both working out of their natural resonance. The consequence is that the phase of Y_1 is not zero (Figure 1.24), but has a little error which can be neglected if the mismatch is small enough. Thus, in steady state the two cores are in phase, meaning that no current flows in the coupling path, hence the oscillation amplitude can be written as $A = \eta_I I_{DC} Z_T$ [55]. The conclusion drawn from these affirmations is that the circuit is independent of the coupling impedance Z_L provided that the frequency mismatch can be considered negligible. It is the same as the resistive coupling case examined in [55], therefore -even if the provided formulas are empirical- the attenuation may be calculated through a rigorous procedure by taking into account the angles created by current and voltage vectors, like in Figure 1.24.

As for the tline coupling case, the frequency mismatch should be regarded as negligible as long as the true oscillation frequency of the system, i.e., $f_{osc} = \frac{f_1+f_2}{2}$, is close to the natural oscillating frequency of the system without mismatch. In mathematical terms, if $f_0 - f_{osc} << f_0$ holds true, then all these approximations are valid.

Although the mismatch is small, it still causes the tank voltage (V_T) and the tank current (I_T) to be phase-shifted. Phase-shift is here represented as ξ, depicted in Figure 2.6.

Even for t-line coupling, it can still be written that $\theta_{12} = arcsin(Kr)$ where $r = \frac{Z_L}{Z_T}$ and $K = Q\frac{f_0 - f_{osc}}{f_0}$. The main is that, for t-line case, it is more complex to write r and Q, which is the reason why empirical formulas were proposed. When COs are locked, then the steady state condition applies and the two tank voltages can still be approximated as $V_{T1} \approx V_{T2} \approx V_T$, with their corresponding attenuation being $V_T = a_{tt} A$, as before.

It still holds true the following formula too.

$$a_{tt} = 1 + \frac{1}{r} - \frac{\sqrt{1 - (Kr)^2}}{r} \tag{2.19}$$

The key to this analysis is the ratio between the coupling and the tank impedances, r, whose value affects the frequency mismatch between the cores, the oscillation swing and a phase difference between the two tank voltage waveforms. All these behaviours are impacted by how big is r; if this ratio is small then the alterations in phase and swing and

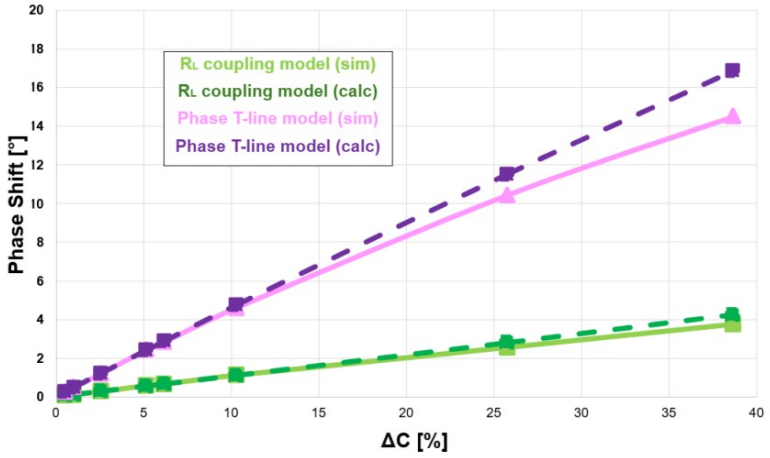

FIGURE 2.6: Phase shift ξ due to mismatch in both resistive and SW t-line coupling cases.

the mismatch all become negligible and the system is comparable to a perfectly coupled double core system, oscillating at f_0.

Considering r, and thus a_{tt} non-negligible, then the oscillation amplitude will be reduced and the phase shift enhanced, with both leading to PN, and eventually FoM, penalty. As for t-line the penalty is rarely negligible due to the presence of a line whose resistance is usually bigger than that of a simple R_L, PN and FoM penalties are proportional to $\frac{1}{a_{tt}^3}$. This proportionality makes simpler to estimate the impact of a t-line over a whole architecture. Also the Impulse Sensitivity Function (ISF) is impacted by a_{tt}^3. So, if another description of the entire system is required, ISF study can be conducted as well, with very similar results, as in [13].

2.1.3 Stability Analysis

Regarding the stability, now the study will explore the t-line case, which is the most relevant for this work. As mentioned before, the golden rule for starting the oscillation is to respect Barkhausen conditions, i.e., having a gain which is at least one and a phase shift being equal π or multiples, but wheather the starting oscillation will maintain and will not be changed is to be calculated. A robust and trustworthy model to examine these oscillation mode and find out which one will prevail is to be identified in Figure 1.25, as before. Here two identical cores are represented: each one has its own impedence and its own active part plus the coupling linking them together. Before analysing this model, which is the simplest way to study the stability of oscillation modes in dual cores CO systems, let us take a step back. First, picture two cores like the one shown in Figure 1.26 and consider each of them as having a complex current injected into the tank, i.e., $I_{inj}e^{j\theta_{inj}}$. Under this current injection condition, amplitude and phase of the tank impedance are depicted in Figure 1.26. Being this injection a sinusoidal input voltage, the result is a square-wave current with a fundamental peak of amplitude $\frac{4I}{\pi}$ [87]. Out of simplicity, all higher order harmonics -which are attenuated by the tank filtering properties- are neglected here, thus leaving only the contribution from the fundamental component. Without any injection, the VCO oscillates at its natural frequency given by $\omega_0 = \frac{1}{\sqrt{L_T C_T}}$ with an amplitude $\frac{4R_T I}{\pi}$, hence being a free-running oscillator. By applying a KCL at the tank, $\frac{Ae^{j\theta}}{R_T} + C_T \frac{d}{dt}(Ae^{j\theta}) + \frac{1}{L_T}\int Ae^{j\theta}dt\,dt = \frac{4I}{\pi}e^{j\theta} + I_{inj}e^{j\theta_{inj}}$ -called generalised Adler's equation -

is derived. By adapting Adler's formula to the given model, this equation may be rewritten as $\frac{A}{R_T} + jC_T A\frac{d\theta_1}{dt} + \frac{F}{L_T} + \frac{A}{R_L} - \frac{Ae^{\theta_2-\theta_1}}{R_L} = \frac{4I}{\pi}$ with $V_1 = A_1 e^{j\theta_1}$and $V_2 = A_2 e^{j\theta_2}$. It is assumed that $A_1 = A_2 = A(t) \approx A$, $I_{gm_1} = I_{gm_2} = I_{gm}$, $I_{T1} = I_{T2} = I_T$, $Y_{12} = Y_{21}$, under the hypothesis that the cores are the same and coupled. Note that F is the integral contribution of the current flowing over L_T, approximated as the output of a LP filter as in [88]. As asseted in the mode analysis, the admittance matrix is symmetrical for t-lines and it has $Y_{11} = Y_{22} = \frac{1}{R_L}$ and $Y_{12} = Y_{21} = -\frac{1}{R_L}$. By substituting and applying the given approximations, Adler's formula is transformed into the following equation, which represents the starting point for this stability analysis.

$$\frac{A}{R_T} + jC_T A\frac{d\theta_1}{dt} + \frac{jA}{\omega_0^2 L_T}(\frac{d\theta_1}{dt} - 2\omega_0) + \frac{A}{R_L} - \frac{Ae^{\theta_2-\theta_1}}{R_L} = \frac{4I}{\pi} \tag{2.20}$$

For t-lines, equation for Y_{11} and Y_{12} are reported below. As in the mode analysis, here the low loss approximation was applied, taking into account that, even if transmission line may be long, its losses must be negligible in the overall system for the coupling to be strong. Also, these approximated formulas come from Conciauro's classical low losses model as in [92]. Still, t-lines have a symmetrical admittance matrix with $Y_{11} = Y_{22}$ and $Y_{12} = Y_{21}$. Note that α and β represent the t-line losses as defined in [92].

$$Y_{11} \approx Y_0[\frac{\alpha d}{sin(\beta d)^2} - j\frac{1}{tan(\beta d)}] \tag{2.21}$$

$$Y_{12} \approx Y_0[\frac{-\alpha d cos(\beta d)}{sin(\beta d)^2} + j\frac{1}{sin(\beta d)}] \tag{2.22}$$

As in [87], the single tank oscillates at ω_0 (free-running frequency) with an amplitude of $\frac{4}{\pi}R_T I$. Once injected a current at a different frequency, the pulling causes a time variation in both frequency and amplitude. The output current of the first core can be written as $A(t)e^{j\theta_1(t)}$ [87]. Supposing that the oscillator locks to injection frequency, the dependance on time is overlooked, as mentioned previously, according to [87], thus $A(t) \approx A$. By applying KCL to the given stability model, the previously reported equation is obtained, then parted into real and imaginary parts to get A and ω. Then, the phase difference between core 1 and core 2 is called ψ. As P and CP are the only viable modes for a two-core oscillator, $\psi = 0, \pi$. In this chapter, modes are already known thanks to mode analysis explained before, thus the first passage from [87], studying which are the existing mode, will not be reported. The results are the same as in the mode analysis. Now, in order to study the stability, a small, positive disturbance $\hat{\theta} << 1$ is added to understand whether the oscillation mode is stable or not. In the first case, the system reaction should be negative,

$$\frac{d\hat{(\theta)}}{dt} = \frac{\omega}{sin(\beta d)}\frac{2sin(\beta d) - \omega L_T Y_0[cos(\psi) - cos(\beta d) - \alpha d cot(\beta d)sin(\psi)]}{1 + \omega^2 C_T L_T} < 0. \tag{2.23}$$

$$\frac{d\hat{(\theta)}}{dt} = -\omega + \frac{\omega}{sin(\beta d)}\frac{2sin(\beta d) - \omega L_T Y_0[cos(\psi) - cos(\beta d) - \alpha d cot(\beta d)sin(\psi)]}{1 + \omega^2 C_T L_T} < 0. \tag{2.24}$$

By substitutions, stability ranges are found for both P and CP. By putting the derivative of the injected disturbance smaller than zero, it is implied that the system is stable.

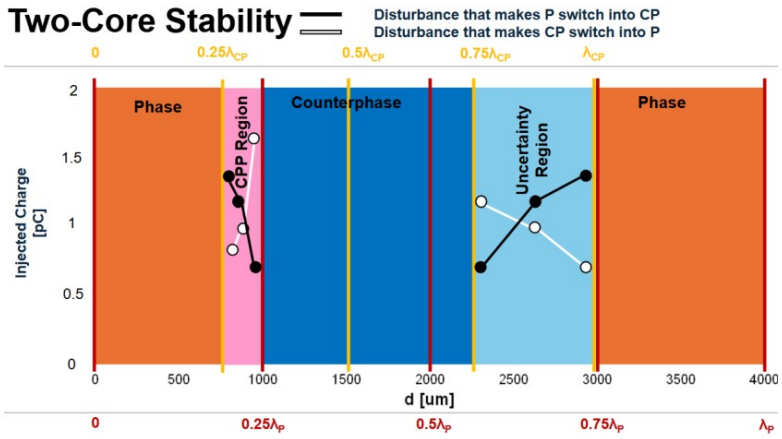

FIGURE 2.7: Stability regions for two VCOs coupled through SW t-lines.

$$\frac{d\theta_1}{dt} = \omega \frac{2sin(\beta d) - \omega L_T Y_0 (cos(\psi) - cos(\beta d) - \alpha d cot(\beta d) sin(\psi))}{sin(\beta d)(1 + \omega^2 C_T L_T)} \tag{2.25}$$

Note that $\alpha \approx \frac{R_L}{2Z_0} << 1$ and $\beta \approx \omega\sqrt{L_L C_L}$ due to canonical low loss approximation. Hence, by substitution, it can be calculated the stability range, respectively for P and CP. Remind that $\psi = 0$ for P, $\psi = \pi$ for CP.

$$\begin{cases} -\alpha d cot(\beta d)\hat{\theta_1} < 0 & if \quad sin(\beta d) > 0 \\ -\alpha d cot(\beta d)\hat{\theta_1} > 0 & if \quad sin(\beta d) < 0 \end{cases} \tag{2.26}$$

$$\begin{cases} +\alpha d cot(\beta d)\hat{\theta_1} < 0 & if \quad sin(\beta d) > 0 \\ +\alpha d cot(\beta d)\hat{\theta_1} > 0 & if \quad sin(\beta d) < 0 \end{cases} \tag{2.27}$$

These conditions result in the following range of stability: $d \in (0, \frac{\lambda_P}{4}) \cup (\frac{3\lambda_P}{4}, \lambda_P)$ for P, $d \in (\frac{\lambda_{CP}}{4}, \frac{\lambda_{CP}}{2}) \cup (\frac{\lambda_{CP}}{2}, \frac{3\lambda_{CP}}{4})$ for CP. Special points such as $\frac{\lambda}{2}, \frac{3\lambda}{4}$ has been studied and there CP is the only possible mode; while for $d = 0$ there is a short between the two cores and for $d = \lambda$ there is no coupling anymore as the two cores stand on two zero voltage amplitude points. Analogously, taking the real part leads to the output amplitude, i.e., the following equations for P and CP. As $\alpha << 1$, amplitude may be coarsely approximated as $A_P \approx A_{CP} \approx \frac{4}{\pi} R_T I$.

$$A_P = \frac{\frac{8}{\pi} R_T I}{2 + Y_0 \alpha d csc^2(\frac{\beta d}{2})} \tag{2.28}$$

$$A_{CP} = \frac{\frac{8}{\pi} R_T I}{2 + Y_0 \alpha d sec^2(\frac{\beta d}{2})} \tag{2.29}$$

Here Figure 2.7 depicts all the possible intervals for the two-core oscillators. Note that the intervals are periodic with λ and that $\lambda_P \neq \lambda_{CP}$. As λ is frequency-dependent, by playing with L_T, C_T, L_L, C_L each region can be shrinked or enlarged. Mark that Figure 2.7 describes four different regions: P, CCP, CP and Uncertainty region. Phase region is where P mode is always stable; the same concept holds for Counterphase region. CPP region is where theoretically both P and CP can be stable as long as they start up. If a large charge is injected, the operation mode may switch from P to CP or viceversa. A similar

phenomenon happens in Uncertainty region where P can swap into CP and the opposite, but none is stable according to theory, hence it is an unstable region. From the feasibility point of view, the first P region appears the optimum as it guarantees good stability and no mode ambiguity. The second P region has the disadvantage of worse losses due to the considerable line length. CP mode may also be a good choice for high frequencies at the expenses of Q, while CPP is not advisable unless a forcing mode element is applied as the initial conditions must be fixed and the possible disturbance must be contained within a fixed threshold. Uncertainty region must be avoided. CPP and Uncertainty region are intuitively similar as P and CP can both oscillate, but the second is more disadvantaged as t-lines are longer. For the considered application, requiring $d < \frac{\lambda_P}{2}$, just the first three regions might be examined. Note that Figure 2.7 refer to the numbers used for this work when practically implemented, as explained in the later chapters. The procedure, though, is general and valid for any t-line.

2.2 Four-Cores Oscillator

After reporting how a dual-core system may be examined, a further step is considered: going from two to four cores, which is the target of the proposed work. As stated before, all the shown couplings may be seen as a case of weak coupling from a mathematical point of view, thus it is fundamental to study the coupling network to ensure the robustness of the whole architecture; the presented analysis come from an engineering background, but a more rigorous and purely mathematical background may be adopted as well, under the hypothesis of a symmetrical weak-coupled multi-cores system. In this subchapter, the analysis will be more focused on the four cores analysis, simplified by the fact that the four coupled VCOs are just an extension of the two cores case. As before, the analysis is carried out through convenient approximation such as short coupling line and low loss approximations in order to provide an intuitive and fast way of designing and understanding multi-cores oscillators. The main subject will be how the four cores can be coupled through SW transmission lines to realize a robust, power saving oscillator with no mode ambiguity, which is scalable and adaptable to the application described in the introduction. In this part, four cores t-line coupling will be examined for what it concerns existing oscillation modes, FoM penalty and stability. All the analysis for a four core system may be extended to a n cores system but it will not be shown to avoid repetitivity and uselessness as the only thing changing from four to n cores is the mathematical complexity for the provided formulas and matrices. For simplicity, the dual core may be considered as the unitary piece for the construction of a more complex CO coupling system. Thus, the target is to show that even by studying a simplified case one can intuitively understand how n cores will behave. Note that all the presented models have the advantage of being scalable, hence the procedure may be to characterise a dx of the total lenght of the coupling connection and then to step it for the length of the total link. By adopting such a method, the designer would be ready for any change -be it minimal or extensive- of its coupling structure.

As stated at the beginning of the chapter, this three step analysis may be considered exhaustive -as it combines multiple different studies cited previously and takes the best results out of them- and applicable to all kind of coupled VCOs systems, including the ones listed in the first chapters. Therefore, the four core analysis may be considered a solid foundation for the designing of a robust and efficient four core VCOs architecture.

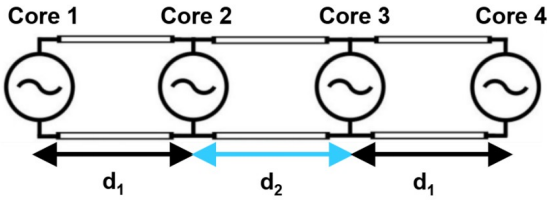

FIGURE 2.8: Proposed four cores architecture.

2.2.1 Mode Analysis

Mode analysis will be conducted exactly as before, starting from [39] methodology and then applying it to the four cores case. The reference structure is the one depicted in Figure 2.8.

In particular, the challenging aspect of this design is the number of existing modes and their ambiguity, especially when the oscillator architecture extends over long distances, such as few mms. This feature is a complex problem in modern chips with a lot of hardware and very strict requirements on power and jitter [4]. In order to cover such long distances, multiple units of two core VCOs should be stepped, considering the traditional trade-offs between power and PN and inter-core distance and FoM penalty. Regarding this work, our design target was to cover about 2mm which made 4 cores the best solution. All the previous considerations may be extended to 4 cores.

For what concerns the frequency model, matrices $\mathbf{Y}$ and $y_{LOAD}\mathbf{I}$ are just extended to 4x4, keeping in mind that core 1 and core 4 are identical as well as core 2 and core 3. Therefore, the Y matrix becomes tridiagonal:

$$\mathbf{Y} = \begin{bmatrix} y_{11} & y_{12} & 0 & 0 \\ y_{21} & y_{22} & y_{23} & 0 \\ 0 & y_{32} & y_{33} & y_{34} \\ 0 & 0 & y_{43} & y_{44} \end{bmatrix} \tag{2.30}$$

with $y_{11} = y_{44}, y_{12} = y_{21} = y_{23} = y_{32} = y_{34} = y_{43}, y_{22} = y_{33}$.

There are four eigenvalues: $\lambda_P, \lambda_{CP}, \lambda_{CPP}, \lambda_{MP}$. Consequently, four oscillation mode exist: Phase, Counterphase, Counter-counterphase, Mixed Phase, as shown in Figure 2.9. In Phase mode, the four oscillators operate with the same polarity (++++), as in the two-core case. In Counterphase mode, two VCOs have opposity polarity and then they are mirrored, i.e., the signs are + - - + (or the opposite). In Counter-counterphase, two VCOs have opposite polarity and then the series goes on, i.e., signs being + - + -. In Mixed Phase, two cores have ++ signs, two - -.

Calculations for frequency and quality factor may be carried out accordingly to the two-cores case. For instance, ω may be calculated starting from $\frac{-1}{\omega L_T} + \omega C_T + Im[\lambda_i] = 0$.

In the simplest case, with the four cores connected through resistors R_L the corresponding matrix elements become $y_{11} = \frac{1}{Z_L}, y_{12} = y_{23} = \frac{-1}{Z_L}, y_{22} = \frac{2}{Z_L}$ and the corresponding four eigenvalues become as reported in the equations below.

$$\lambda_P = 0 \tag{2.31}$$

$$\lambda_{CP} = \frac{2}{Z_L} \tag{2.32}$$

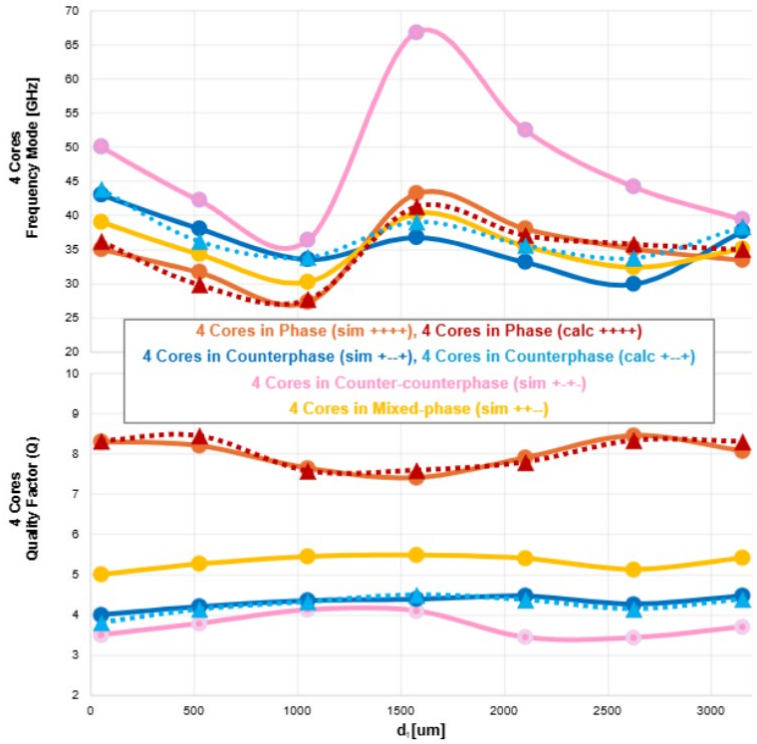

FIGURE 2.9: Frequency and Quality Factor (Q) for 4 cores SW t-line coupled VCOs.

$$\lambda_{CPP} = \frac{2+\sqrt{2}}{Z_L} \tag{2.33}$$

$$\lambda_{MP} = \frac{2-\sqrt{2}}{Z_L} \tag{2.34}$$

Same goes for the eigenvectors, still reported below.

$$v_P = [1,1,1,1]^{\mathbf{T}} \tag{2.35}$$

$$v_{CP} = [\frac{1}{\sqrt{2}}, -\frac{1}{\sqrt{2}}, -\frac{1}{\sqrt{2}}, \frac{1}{\sqrt{2}}]^{\mathbf{T}} \tag{2.36}$$

$$v_{CPP} = [cos(\frac{3\pi}{8}), -cos(\frac{\pi}{8}), cos(\frac{\pi}{8}), -cos(\frac{3\pi}{8})]^{\mathbf{T}} \tag{2.37}$$

$$v_{MP} = [cos(\frac{\pi}{8}), cos(\frac{3\pi}{8}), -cos(\frac{3\pi}{8}), -cos(\frac{\pi}{8})]^{\mathbf{T}} \tag{2.38}$$

In a more general case, considering four cores connected through three t-lines of generical lengths d_1, d_2 as represented in Fig.Figure 2.8, it is still true that $y_{11} = y_{44}, y_{12} = y_{21} = y_{23} = y_{32} = y_{34} = y_{43}, y_{22} = y_{33}$ with $y_{11} = \frac{-j}{Z_0 tan(\beta d_1)}, y_{12} = \frac{j}{Z_0 sin(\beta d_1)}, y_{23} = \frac{j}{Z_0 sin(\beta d_2)}, y_{22} = \frac{-j}{Z_0 tan(\beta d_1)} + \frac{-j}{Z_0 tan(\beta d_2)}$. The eigenvalues are now a little different, as written below.

$$\lambda_1 = \frac{1}{2}[y_{11} + y_{22} + y_{23} + \sqrt{(y_{11} - y_{22} - y_{23})^2 + (2y_{12})^2}] \tag{2.39}$$

$$\lambda_2 = \frac{1}{2}[y_{11} + y_{22} + y_{23} - \sqrt{(y_{11} - y_{22} - y_{23})^2 + (2y_{12})^2}] \tag{2.40}$$

$$\lambda_3 = \frac{1}{2}[y_{11} + y_{22} - y_{23} + \sqrt{(y_{11} - y_{22} - y_{23})^2 + (2y_{12})^2}] \tag{2.41}$$

$$\lambda_4 = \frac{1}{2}[y_{11} + y_{22} - y_{23} - \sqrt{(y_{11} - y_{22} - y_{23})^2 + (2y_{12})^2}] \tag{2.42}$$

The same principle holds for their corresponding eigenvectors, i.e., $v_{1,2}$ and $v_{3,4}$, which are expressed as the following formulas, with $r = \frac{\lambda_i - y_{11}}{y_{12}}$.

$$v_{1,2} = \frac{1}{\sqrt{2(1+r^2)}}[1, r, r, 1]^{\mathbf{T}} \tag{2.43}$$

$$v_{3,4} = \frac{1}{\sqrt{2(1+r^2)}}[1, r, -r, -1]^{\mathbf{T}} \tag{2.44}$$

As $i = 1, 2$ denote symmetric modes, while $i = 3, 4$ stand for anti-symmetric modes, 1 represents P mode, 2 MP, 3 CP and 4 CCP. These are the general formulas for any couple of (d_1, d_2).

Now look at some particular cases: $d_1 = d_2$ and $d_1 = 2d_2$. Starting with $d_1 = d_2$, the matrix elements become $y_{11} = \frac{-j}{Z_0 tan(\beta d_1)}, y_{12} = y_{23} = \frac{j}{Z_0 sin(\beta d_1)}, y_{22} = \frac{-j2}{Z_0 tan(\beta d_1)}$. By imposing the aforementioned equation and low loss approximation, frequency in the three oscillation modes is found: $\omega_P \approx \frac{1}{\sqrt{C_T L_T}}$, $\omega_{MP} \approx \frac{1}{\sqrt{C_T \frac{L_T L_L}{L_L + 2L_T}}}$, $\omega_{CP} \approx \frac{1}{\sqrt{C_T \frac{L_T L_L}{L_L - L_T}}}$, $\omega_{CCP} \approx \frac{1}{\sqrt{C_T \frac{L_T L_L}{L_L + 2L_T(1+\sqrt{2})}}}$.

If $d_1 = 2d_2$ -as in this work- then the eigenvalues may be rewritten as

$$\lambda = \begin{bmatrix} \frac{-jY_0}{2}\left[\frac{1}{\tan(\beta d_1)} - \frac{1}{\sin(\beta d_1)} - \frac{1}{\sin\left(\frac{\beta d_1}{2}\right)} + \sqrt{\left(\frac{1}{\tan(\beta d_1)} + \frac{1}{\sin(\beta d_1)} + \frac{1}{\sin\left(\frac{\beta d_1}{2}\right)}\right)^2 + 4\left(\frac{1}{\tan(\beta d_1)}\right.\right.\right. \\ \frac{-jY_0}{2}\left[\frac{1}{\tan(\beta d_1)} - \frac{1}{\sin(\beta d_1)} - \frac{1}{\sin\left(\frac{\beta d_1}{2}\right)} - \sqrt{\left(\frac{1}{\tan(\beta d_1)} + \frac{1}{\sin(\beta d_1)} + \frac{1}{\sin\left(\frac{\beta d_1}{2}\right)}\right)^2 + 4\left(\frac{1}{\tan(\beta d_1)}\right.\right.\right. \\ \frac{-jY_0}{2}\left[\frac{1}{\tan(\beta d_1)} - \frac{1}{\sin(\beta d_1)} + \frac{1}{\sin\left(\frac{\beta d_1}{2}\right)} + \sqrt{\left(\frac{1}{\tan(\beta d_1)} + \frac{1}{\sin(\beta d_1)} + \frac{1}{\sin\left(\frac{\beta d_1}{2}\right)}\right)^2 + 4\left(\frac{1}{\tan(\beta d_1)}\right.\right.\right. \\ \frac{-jY_0}{2}\left[\frac{1}{\tan(\beta d_1)} - \frac{1}{\sin(\beta d_1)} + \frac{1}{\sin\left(\frac{\beta d_1}{2}\right)} - \sqrt{\left(\frac{1}{\tan(\beta d_1)} + \frac{1}{\sin(\beta d_1)} + \frac{1}{\sin\left(\frac{\beta d_1}{2}\right)}\right)^2 + 4\left(\frac{1}{\tan(\beta d_1)}\right.\right.\right. \end{bmatrix} \tag{2.45}$$

while the eigenvectors are

$$\mathbf{v} = \begin{bmatrix} 1 & r & r & 1 \\ 1 & r & r & -1 \\ 1 & r & -r & -1 \\ 1 & -r & -r & 1 \end{bmatrix} \tag{2.46}$$

where
$r(\lambda_i) = \frac{\lambda_i + \frac{jY_0}{2}\frac{1}{tan(\beta d_1)}}{\frac{jY_0}{2}\frac{1}{sin(\beta d_1)}}$.

For a low-loss and short t-line approximation, equations for ω_i are written below, respectively for P, MP, CP and CPP. The good matching of these formulas is shown in Figure 2.9.

$$\omega_P \approx \sqrt{\frac{4L_L + 4L_T}{L_T L_L (4C_T + C_L)}} \tag{2.47}$$

$$\omega_{MP} \approx \sqrt{\frac{4L_L + 2L_T}{L_T L_L (4C_T + 3C_L)}} \tag{2.48}$$

$$\omega_{CP} \approx \sqrt{\frac{6L_L + 6L_T}{L_T L_L (4C_T + C_L)}} \tag{2.49}$$

$$\omega_{CCP} \approx \sqrt{\frac{4L_L + 6L_T}{L_T L_L (4C_T + 3C_L)}} \tag{2.50}$$

Regarding Q, it is the same as before for both P and CP modes under the hypothesis that the four cores share the same voltage amplitude, while core 2 and 3 have bigger currents; the resulting frequency shift is divided along the chain as $f_0 \approx \frac{f_{core1}+f_{core2}+f_{core3}+f_{core4}}{4}$ [55]. Qualitatively, Q_{MP} is in between Q_P and Q_{CP} as the power loss in the t-line decreases with respect to the CP due to the fact that core 1 and 2 are in phase, as well as core 3 and 4. Accordingly, Q_{CCP} is the worst among the four modes as the power loss in t-line is maximized as there are no adjacent cores in phase. CCP and MP modes deserve no particular analysis as they do not satisfy Barkhausen conditions for start-up in case-study. Figure 2.8 shows the four modes from ac simulations -the transient behaves accordingly- and approximated calculations.

From Figure 2.8 the proposed four cores architecture is shown: there is an ulterior degree of freedom which is the length of the t-lines. There are multiple possible choices for d_1 and d_2. Choosing $d_1 = 2d_2$ guarantees a good FoM and an enhanced phase stability, as it will be better explained in the later chapters.

2.2.2 FoM Penalty Analysis

From the point of view of shifting from two to four cores, the FoM penalty analysis is the simplest one as no change occurs. The only difference between these two cases is qualitative as the attenuation factors will be increased by the presence of additional cores and coupling networs. To be more precise, FoM does not decrease nor increase with multi-core couplings, provided that the coupling is ideal, thus a non-ideal coupling will reduce the FoM and consequently the overall perfomance will worsen. As reported in the previous chapter, the empirical formula allowing to estimate the FoM penalty based on the total line length (d) and the occurred mismatch [81] is reported below.

$$FoM = FoM_{1core} + 30log(a_{tt}) \tag{2.51}$$

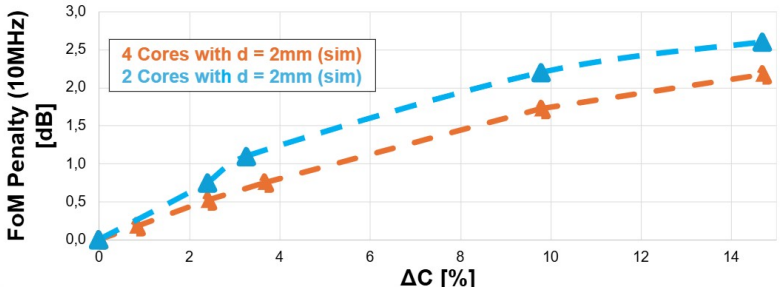

FIGURE 2.10: FoM penalty for dual-core VCO system vs for a four-core VCO system in Phase mode.

$$a_{tt} \approx 1 + r(1 + \frac{k}{2}) \tag{2.52}$$

$$r \approx \frac{R_L}{R_T + \frac{\omega L_L}{2}} \tag{2.53}$$

In particular, the above equation quantifies the penalty, where a_{tt} represents the attenuation factor and parameter r is derived by the ratio between the tank and the t-line impedance. Instead, k is the coupling between the cores [87]. Generically, coupling is derived from Adler's formula: the following equations show how to calculate the coupling factor for both P and CP.

$$k_P \approx \frac{|\Delta\omega|}{\omega + 2Q|\Delta\omega|} \tag{2.54}$$

$$k_{CP} \approx \frac{|\Delta\omega|}{\omega - 2Q|\Delta\omega|} \tag{2.55}$$

Due to mismatches, the Figure of Merit is impaired as aforementioned, but also the output waveforms may have a slight phase shift (ξ), which is small enough that the Phase condition, i.e., $\psi \approx 0$, still holds true. In order to evaluate ξ, some calculations were performed with the entire mismatch (C_M) placed on core 2 for the sake of simplicity. Consequently, Q_{T2} is different from those of the other tanks. Obviously, there are modes MP and CCP, though they were neglected due to the fact that they never start up considering the current conditions adopted in this work, as confirmed through Cadence simulations.

It is still valid that FoM penalty may be impaired by both mismatch and the nature of the transmission life itself, which represent a mismatch as the considered structure is not perfectly symmetrical, as it is not a rotary wave. The same applies to the fact that not even an enormous mismatch (e.g., 40%) may produce a significant ξ, such that P mode cannot change to CP due to mismatches. In reality, this robustness is even more true in a four cores than in a two cores structure as coupling multiple P mode cores makes CP or other modes even less probable. This is especially true for the case adopted in this work, i.e., with t-lines lenght being $d_1 = 2d_2$. For this t-line lengths, the FoM penalty for four cores is reduced if compared to the FoM penalty of the dual-core system, as shown in Figure 2.10.

Still, phase shift ξ can be calculated as it follows, considering that there is an impairment between the first core (Q_1) and the second core (Q_2), under the hypothesis that the first and the fourth cores are identical ($Q_1 = Q_4$) and so are the second and the third

($Q_2 = Q_3$). This applies to the considered work; for more complex mismatches -for instance when all the four cores have different quality factors- the phase shift should be calculated for every couple of cores and then put together.

$$\xi \approx k_c Q_{T2} \frac{R_L}{R_L + R_T} \tag{2.56}$$

$$k_c \approx \frac{C_M}{\sqrt{(C_T + C_L)(C_T + C_L + C_M)}} \tag{2.57}$$

$$Q_{T2} = \omega R_T (C_T + C_M) \tag{2.58}$$

Such formulas can still be validated through model Figure 1.23. Its procedure is unchanged, but now four cores are required and current vectors must be drawn for each core, as in [55].

2.2.3 Stability Analysis

Stability analysis is again carried out starting from Adler's generalised formula applied to the tank, then proceeding with the derivative of disturbance for each mode. Again, it is already known that, for our structure, depicted in Figure 2.8, exist four operation modes, i.e., CP, CCP, MP, P, but only two out of four can start up according to Barkhausen's conditions. In order to save time and useless efforts, Adler's formula will be used only to calculate the derivative of the disturbance in P and CP modes as they are the only possible modes. Whether one may want to verify the existance of MP and CCP or their stability range -which is non-existent- obviously Adler's generalised formula would be a good starting point and the above-mentioned procedure still applies.

As in Figure 2.8, the four core system features an additional complexity, i.e., the relation between d_1 and d_2. As mentioned in the previous subchapter, the interesting case for this work is the one with $d_1 = 2d_2$ which guarantees better FoM and stability performance. Intuitively, one can say that these qualities are gained by coupling multiple cores oscillating in P, thus reinforcing the system. For a more detailed explanation, wait the next chapter. For what concerns stability, it is important to remark that, depending on the ratio between d_1 and d_2, Counterphase or Counter-counterphase are favoured. By selecting $d_1 = 2d_2$, Counterphase and Phase are the only two possible modes thanks to Barkhausen if $d_1 \geq d_2$. For different d_1 and d_2 ratios, even MP or CCP may start up and become the main modes. As these cases are not applicable to this work, they will be neglected. If any interest for MP or CCP modes might arise, then this procedure and models would still hold. Returning to our case, i.e., $d_1 = 2d_2$, it allows to consider only CP and P as, in order for Mixed Phase to oscillate, the condition is $d_2 >> d_1$, similarly for Counter-counterphase d_2 should be at least slightly bigger than d_1. In our case, having just P and CP, our target is still to favour P as in general P mode is always the one providing the best quality factor: in fact this is the most similar condition to having a single core CO oscillating at f_0.

Previously, the dual core system was analysed with the model reported in Figure 2.11: out of brevity, it could be described as featuring an active part, I_{Gm}, a tank, $Y_T + Y_{11}$, and a coupling element, $Y_{12}V_2$ for each core. Being the system simmetrical, the model simplifies as $Y_{11} = Y_{22}$ and $Y_{12} = Y_{21}$. The same rules apply to the amplitude A, the tank own impedance Y_T and the active part I_{Gm}. Going from the two VCOs to the four VCOs model means shifting from two cores to four cores, but here the symmetry of the system was exploited in order to simplify the model and get an half model instead of a full model -depicted in Figure 2.12 - for clearer and easier calculations. In fact, the system

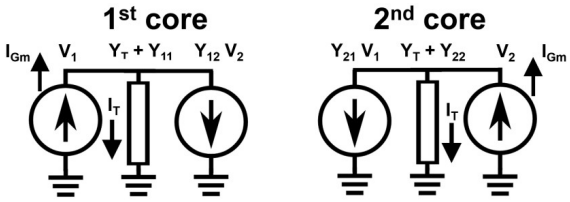

FIGURE 2.11: General Model of two coupled oscillators for stability.

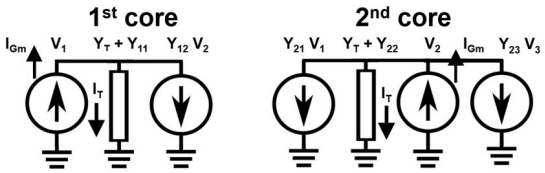

FIGURE 2.12: Half-circuit model of four coupled oscillators for stability.

is still symmetrical as the first and the fourth core are identical and the same goes for the second and the third. As the two cores model may be extended to a four-core solution by exploiting the symmetry of the structure, just half the circuit may be studied, thus the resulting conditions are derived with the same method as the two cores but now d_2 line is considered as a load.

The model from Figure 2.12 shows an additional contribution due to the third core, which is the same as the second core. As every core sees a load equivalent to $\frac{d_1}{2} \pm \frac{d_2}{4}$ and $d_1 = 2d_2$, Adler's generalised equation applied to the tank is rewritten as it follows.

$$\frac{A}{R_T} + jCA\frac{d\theta_1}{dt} + \frac{jA}{\omega^2 L_T}\left(\frac{d\theta_1}{dt} - 2\omega\right)e^{j(\theta_2-\theta_1)} + A\left(Y_{11} + \frac{3}{2}Y_{12}\right) = \frac{4}{\pi}I \tag{2.59}$$

As P mode is the target, each oscillator should see the same load: the four cores should compensate each other. Now $\frac{3}{2}Y_{12}$ is considered to take into account not only $\frac{d_1}{2}$,i.e., Y_{12}, but also $\frac{d_2}{2}Y_{12}$, i.e., $\frac{Y_{12}}{2}$. Such simplification is possible thanks to the relationship between the two t-line lengths, otherwise a general dependence on third core should be written.

Under these hypotheses, Phase region is enforced. Thus, the stability regions remain similar to the two-core case, as shown in Figure 2.13. By choosing such sizing for the t-lines, the uncertainty region near λ_P is wiped out as P is favored as the load of each core is minimized by selecting a small d_2. Regarding longer t-lines, CP is empirically dominating until λ_{CP} but it is advisable to only use it until $\frac{\lambda_{CP}}{2}$.

In order to get into some more details regarding the calculations, let us take a brief step back and recall the KCL for the four cores system as it is written above. Maintaining the same approach as per the dual-core system, the KCL is rewritten with a new Y_{12} for the four-core case. Consequently, the stability condition becomes a system like the one reported for P and CP in the dual-core stability analysis subchapter. Thus, the range of stability for four cores is: $d \in (0, \frac{\lambda_P}{2}) \cup (\frac{3\lambda_P}{4}, \lambda_P)$ for P,

$$d \in \left(\frac{\lambda_{CP}}{2}, \lambda_{CP}\right)$$

for CP.

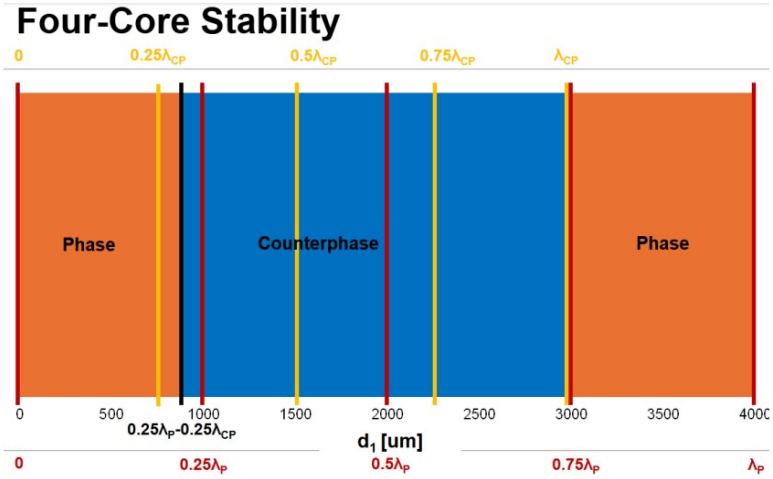

FIGURE 2.13: Stability region for the proposed four cores architecture.

The disturbance derivative becomes as reported below.

$$\frac{d\hat{(\theta)}}{dt} = -\omega + \omega[\frac{4sin(\beta d) + \omega^2 L_T Y_0(2cos(\beta d) - 3cos(\psi) + \frac{3}{2}\alpha d arctan(\beta d) sin(\hat{\theta_1}))}{2sin(\beta d)(\omega^2 C_T L_T)}] < 0 \tag{2.60}$$

On the other hand, the amplitudes in P, CP are now changed too, as in the following equations. Amplitudes change as the load is different of a factor $\pm\frac{d2}{4}$.

$$A_P = \frac{\frac{8}{\pi} R_T I}{2 + Y_0 \alpha d(3cos(\beta d) + 2)csc(\beta d)^2} \tag{2.61}$$

$$A_{CP} = \frac{\frac{8}{\pi} R_T I}{2 - Y_0 \alpha d(3cos(\beta d) - 2)sec(\beta d)^2} \tag{2.62}$$

In conclusion, despite these differences being far from ideal, the P mode is still to be favoured in order to get a better quality factor and a good stability. By staying in the first P mode range, the quality factor is maximized and the system is guaranteed to have no mode ambiguity.

Chapter 3

Proposed Architecture

In this architecture chapter, the proposed design is finally explained and the choices that were meekly accepted before are now to be motivated. Some of them came out of practical necessities while others were adopted due to theorical reasons. In the previous chapters, the motivation of this work was presented and it was highlighted the need of a power and area efficient distributed oscillator adopting SW transmission lines as both distribution network and coupling method. Also, some theory about coupling was explained, the same principle holds for mode analysis and stability investigation. After carrying out these analysis, the design is sure to be stable, with no mode ambiguity.

In the following subchapters, the proposed design is to be explained for what concerns the technology -which was a consequence of the application- and the topology. Also, some details about design and layout will be added in order to gain a better understanding of the structure and to foresee some of the measurement results. Before proceeding to the next chapters, note that the test-chip to verify the goodness of the proposed design was a stand-alone oscillators, thus in order to get some results, also a divider by two was designed. The divider was inserted into an output chain featuring some buffers and a multiplexer allowing to switch from the signal at maximum frequency, i.e., around $27GHz$, to the signal at frequency divided by two. This was done in order to see both the signal at its own frequency and the signal divided by two in order to perform the measurement with more ease.

After the design presentation, this work will procede to the measurement and the comparison with the state of the art.

3.1 Technology Node

As reported in the introduction, the main purpose for this design is to serve as efficient oscillator for SerDes application, which are notoriously requiring great performance in terms of speed.

To match these criteria, the only way is to adopt a great deal of digital elaboration to improve the quality of the signal for both transmission and reception and this is possible only thanks to a scaled technology. Nowadays, scaled technology means FinFET, i.e., a fin field-effect transistor, a multigate device built on a substrate where the gate is placed on two -or more- sides of the channel, forming a double -or multi gate- structure. In this work, single gate transistors were employed.

A more sophisticated and more performing version of MOSFET do exist, i.e., gate all around, featuring a gate wrapped around the channel. For now, the majority of industrial production still use the FinFET, while the gate all around technology represents the near future. Therefore, in this work a FinFET technology was employed, more in particular the $12nm$ technology node.

GLOBALFOUNDRIES MPW Pricelist	Standard EUR / mm²	Discounted EUR / mm²
GLOBALFOUNDRIES SiGe 8XP	5,060 [1]	4,600 [1]
GLOBALFOUNDRIES 130 nm BCDlite	1,760 [1]	1,600 [1]
GLOBALFOUNDRIES 55 nm BCDlite	5,720 [2]	5,200 [2]
GLOBALFOUNDRIES 45RFE	10,230 [1]	9,300 [1]
GLOBALFOUNDRIES 45RFSOI	10,230 [1]	9,300 [1]
GLOBALFOUNDRIES 45nm SPCLO -Silicon Photonics (price per fixed block 5mm x 5mm)	242,000	220,000
GLOBALFOUNDRIES 28 nm SLPe	12,430 [3]	11,300 [3]
GLOBALFOUNDRIES 22 nm FDSOI	18,975 [3]	17,250 [3]
GLOBALFOUNDRIES 12 nm LP+	31,240 [3]	28,400 [3]
GLOBALFOUNDRIES 180 MCU (Open PDK)	913 [4]	830 [4]

FIGURE 3.1: Today pricing list from Global Foundries official website.

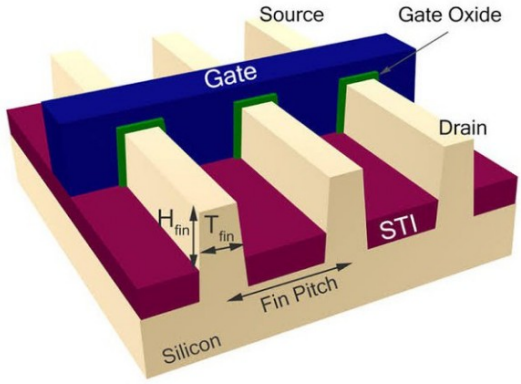

FIGURE 3.2: Standard structure of a general FinFET transistor.

To get more technical info and a better understanding of the adopted node, one can refer to [93], where a $12nm$ transistor was analyzed. The results regarding threshold voltage variations and stress performance are reported respectively in Figure 3.7 and Figure 3.6, while graphs shown in Figure 3.5, Figure 3.4 and Figure 3.3 depict the characterization of a typical transistor in this process node.

In general, FinFET devices -shown in Figure 3.2- are called like this due to their shape, as the region between source and drain forms fins on the silicon surface. The FinFET devices exhibit significantly faster switching times and higher current density than planar CMOS technology, thus granting enhanced performance and power efficiency, which is the reason why they spread so thoroughly. To give a little history excursus, chips employing FinFET FinFET technology became commercialized in the first half of the 2010s with $14nm, 10nm, 7nm$ processes. Even if their debut dates back to more than ten years ago, these nodes are still in use. Another crucial aspect is that they are still expensive, as reported in Figure 3.1, which shows the prices for Global Foundries technology, which was used for this work.

Note that FinFET technology was adopted for analog designs out of necessity as analog and digital architectures are required to coexist in the same chip. In fact, scaled technology does not benefit analog design as parasitics become more and more relevant at every new node and the flicker problem is accentuated too. Another drawback of FinFET, which is shared by the adopted node, is the lack of extra-thick metal layer. In older

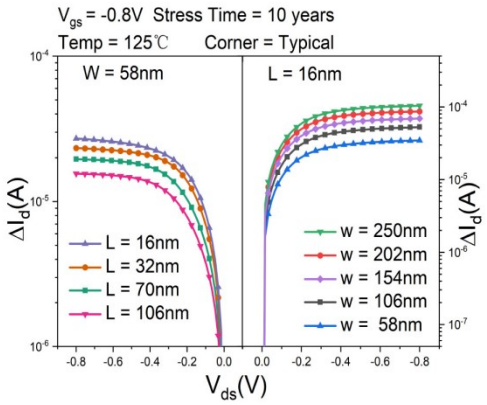

FIGURE 3.3: Simulation results of ΔI_D variation with V_{DS} from [93].

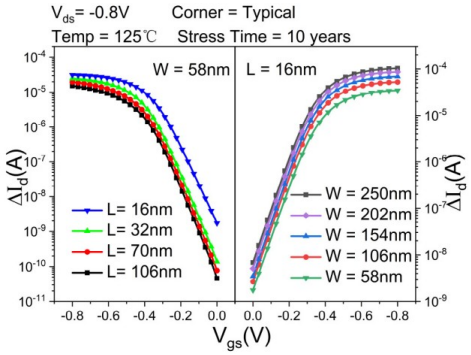

FIGURE 3.4: Simulation results of ΔI_D variation with V_{GS} from [93].

technology processes -which work better for analog architectures- there were extra thick layers used for inductors and very sensitive structures. Oppositely, in FinFET a designer should just abide with the thick layers. For reference, a similar stack is provided in Figure 3.8.

3.2 SW Hybrid Topology

When dealing with topology matters, the first thing is to identify the specifications that the given topology should satisfy. As already mentioned, in the last 20 years, electro-optical communications have been developing more challenging requests, halving specifications on noise and power each year, therefore it's crucial to quantify and improve as much as possible such performance for SerDes (Serializer-Deserializer) transceivers as they implement the wire enabling people to connect, store and access data, which are everyday activities, necessary for most jobs. Recently, this need appeared even more evident with the advent of 5G and Internet of Things (IoT). Being clock about half the total power consumption in VLSI chips, it is fundamental to optimize the clock signal generation and distribution. In this thesis, clock distribution becomes a huge design aspect for large chips, whose lengths span from 1 mm to 10 mm. Distribution usually requires half the power consumption and adds up noise as well, thus the focus of this work is to optimize the clock management through a distributed oscillator architecture. The traditional

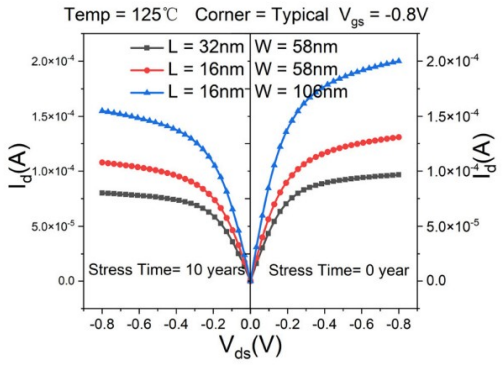

FIGURE 3.5: Simulation results of output characteristic curve from [93].

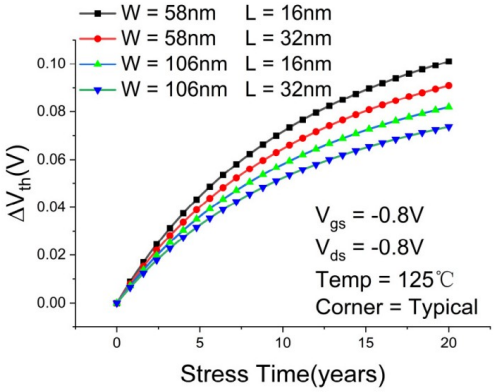

FIGURE 3.6: Simulation results of stress impact over 12*nm* a transister from [93].

trade-off power-phase noise (PN) is examined and a new solution is proposed through in-phase coupling. Given a length which spans from 1 mm to 10 mm, a target length is set around 2 mm as it responds to two needs: first, it is enough to prove the concept and realise a large distributed system, second, it is not as huge and expensive as buying 10 mm of area as FinFET cost is non-negligible as shown in the previous subchapter. Thus, the area at our disposal was a rectangle of 2 mm per 2.5 mm, which is a realistic space inside a high-speed SerDes chip product. Other main specifications include a maximum frequency at 27 GHz, a total power -meaning both clock generation and distribution- under 10 mW and a PN mask with a slope of 20 dB/dec and a value of -124 dB at 10 MHz. For this specifical application, no particular TR is required. Therefore, once provided these specifications, it is time to define the adopted topology. As it is now clear, for a power efficient oscillator architecture, a Standing Wave distributed oscillator was chosen but it was not a traditional SW structure, but a hybrid solution. In fact, having multiple cores coupled through SW t-lines allow to combine the low power advantage from distributed systems and the higher quality factor typical of single VCOs. In order to persuade the reader of the goodness of this assumption, simulations were carried out showing that inserting discrete COs core inside SW t-lines does provide a great advantage in terms of FoM. Again, Figure of Merit was chosen as a complete metric as it compares all the main parameters (frequency, power, PN) for a fair comparison. As shown in Figure 3.9, in the

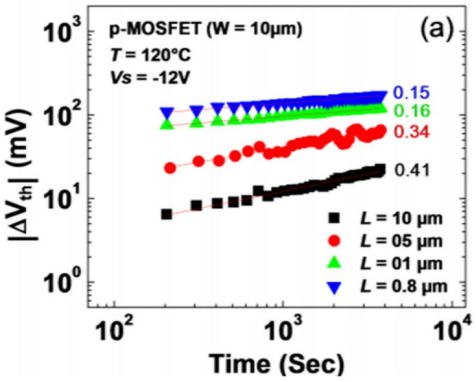

FIGURE 3.7: Measured results reported from [93].

considered range, i.e., for short transmission lines, the hybrid solution guarantees much better performance, in the order of 3 dB and more, than the traditional $\frac{\lambda}{4}$ distributed oscillator.

The four cores adopted in this work are a consequence of the previous analysis. In fact, Phase mode can maintain itself with no mode ambiguity in a range between 0 and $\frac{\lambda_{CP}}{4}$, corresponding -for a frequency of 27 GHz in this technology node- to a range from 0 to $0.750mm$, which are not enough for the target legnth of 2 mm. At the same time, FoM penalty results acceptable -i.e. less than 10%- if the total t-line lenght is lower than $\frac{\lambda_P}{4}$, which is also less than the target 2 mm. As the goal is to have a symmetrical structure, the natural move is to extend from a dual-core, which is the basic unit for this kind of architecture, to a four-core VCO system, whose length should approach the desired 2 mm. Thus, the structure becomes as the one depicted in Figure 2.8, where the cores are connected by transmission lines of lenghts d_1, d_2 with each of them being less than $\frac{\lambda_{CP}}{4}$, i.e., $d_1, d_2 < \frac{\lambda_{CP}}{4}$, to ensure both Phase mode stability and reduced FoM penalty. When shifting to four cores, the stability -as studied in the previous chapter- is proved to be granted in a range going from 0 to $\frac{\lambda_P}{4} - \frac{\lambda_{CP}}{4}$ for P mode. Considering a structure with the same oscillating frequency and the same t-line, a fair comparison with the proposed topology may be carried out. The FoM of the proposed topology is superior with respect to a classic $\frac{\lambda}{4}$ architecture [20] due to the improved PN performance deriving from the presence of the LC tanks. This four-core structure guarantees more flexibility and scalability and optimized performance at the cost of additional area. In conclusion, the four cores in P seems to enhance both the stability and the FoM thanks to the strenghtening of the coupling due to adding multiple cores oscillating in P.

Phase mode -as mentioned in previous chapters- is a key player for this structure as it allows the quality factor to be $Q_{system} \approx Q_T$ where Q_T is the quality factor of the single tank, assuming that the four cores are identical. Virtually, the four cores are indeed identical, but due to process mismatches -and even mismatches that were purposely introduced during measurements- the reality is closer to $Q_{T1} \approx Q_{T2} \approx Q_{T3} \approx Q_{T4}$.

Another crucial aspect -which was hinted at in the previous chapters- is the ratio between d_1 and d_1. As depicted in Figure 3.10, there are infinite possible combinations for d_1 and d_1, therefore a choice is to be done taking into consideration three main aspects: first, the purpose of this work is to build a distribution network, i.e., at least one between d_1 and d_1 shoulde be big compared to the tank sizing, second, the structure ought to be efficient in terms of power and PN at high frequency, hence FoM should be maximized,

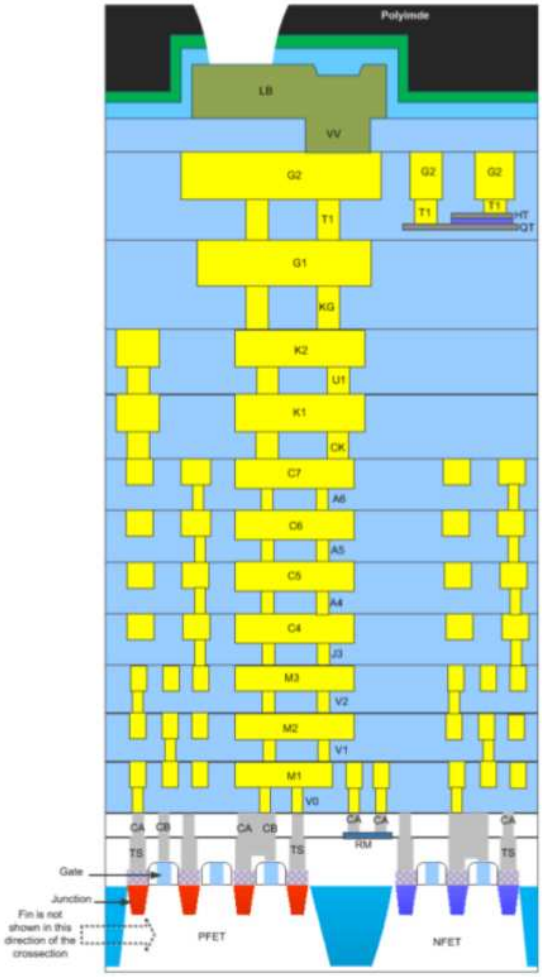

FIGURE 3.8: Fac-similar of a FinFET metal stack.

third, the calculations about mode stability are to be verified as well, thus it would be preferrable to have at least one between d_1 and d_1 close to the P mode stability limit, which is 0.750 mm. With these three conditions in mind, some options for the ratio between d_1 and d_1 were selected and simulated in Cadence virtuoso to compare their FoM. Such a comparison is shown in Figure 3.11, where the selected couples are $d_1 = 2d_2$, $d_1 = \frac{d_2}{2}$, $d_1 = 0$ and $d_2 = 0$. Now, consider that the couples $d_1 = 0$ and $d_2 = 0$ are taken as extremes in order to understand the general behavior as they are non-physical. In fact, realizing $d_1 = 0$ would mean having the first core and the second core overlapped, with zero length between the two, and the same for the third and the fourth core. Even if the two can be shorted together, there would be a trade-off between the length of the "short" connection and the coupling of the two inductor, especially when large inductors are used to enhance the Q of the structure, as in this case. The same principle holds for the case $d_2 = 0$, where the overlapped cores would be the third and the second. Therefore, these cases can be used as examples but their FoM would drop for a realistic implementation. The conclusion drawn from $d_1 = 0$ and $d_2 = 0$ can though be helpful. The remaining cases, $d_1 = 2d_2$ and $d_1 = \frac{d_2}{2}$, are then to be compared. In this work, $d_1 = 2d_2$ was selected as the best option as it is the realisable implementation featuring the best Figure of Merit and also respecting the three conditions provided above.

By looking at Figure 3.12, the proposed architecture with $d_1 = 2d_2$ is shown, with

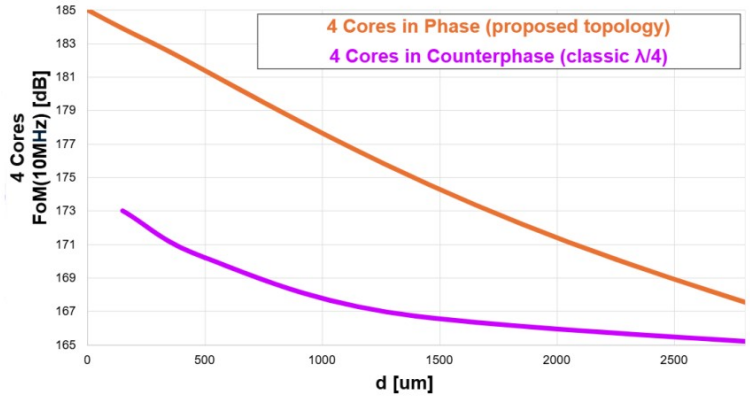

FIGURE 3.9: FoM penalty comparison between the proposed solution and a classic $\frac{\lambda}{4}$ distributed architecture.

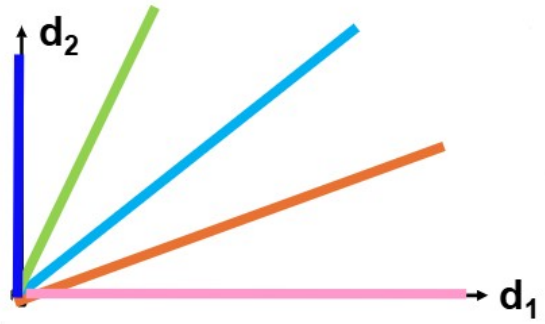

FIGURE 3.10: Graphical representation of the different existing combinations of d_1, d_2.

particular attention to the lengths being $d_1 = 0.718mm$ and $d_2 = 0.286mm$. It is important to highlight that $d_1 = 0.718mm$ is quite close to P mode stability limit, i.e., $0.750mm$ for this architecture.

To sum up, the proposed four-core oscillator features four LC VCOs coupled through SW t-lines oscillating in Phase mode. To briefly state the next steps, first, the t-line design must be performed carefully in order to respect the calculations previously done for mode analysis, stability and FoM penalty, then, each core should be considered. For this kind of structure, layout is a key player as it may add too many parasitic: their estimation is crucial to do correct calculations. The last aspect to be taken into account is the output chain, which must work in order for the measurements to be carried out effectively.

3.3 Tranmsission Lines Design

In this subchapter, some further details will be given about transmission lines implemented in this test-chip. One of the main strength of the proposed architecture is that now transmission lines are no longer confined to $\frac{\lambda}{4}$ length. Instead, for the proposed structure there is a range, namely between 0 and $\frac{\lambda}{4}$, allowing both stability with no mode ambiguity and good FoM peformance, which makes the design more robust and flexible.

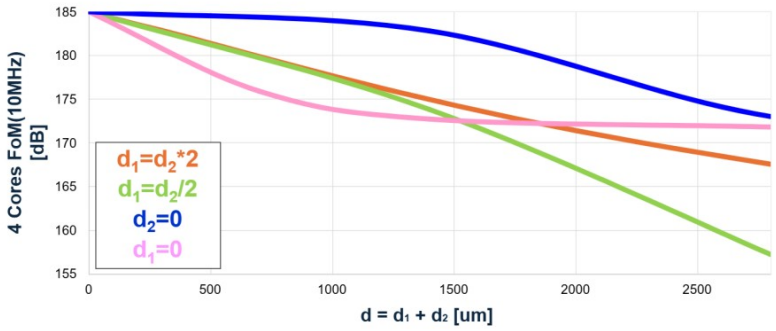

FIGURE 3.11: Four cores FoM(10MHz) for different combinations of d_1, d_2.

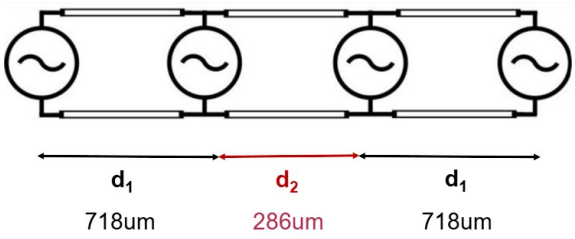

FIGURE 3.12: Four cores proposed architecture with $d_1 = 2d_2$.

Given the advantage of the improved flexibility and robustness, the design of t-lines become easier but still there exist major difficulties. In particular, it is important that the total impedance of the t-lines is much lower than the impedance of the single tank for the proposed hybrid solution, i.e., $Z_L << Z_T$. Due to both the impedances being complex, the condition may be translated into multiple conditions regarding L_L, C_L and R_L. As a rule of thumb, in this design the applied criteria were $C_L < \frac{C_T}{4}$, $L_L < L_T$ and $R_L << R_T$. To gain a more practical insight, one can look at the table below.

According to [92], different lengths may be considered as an important design parameters: for the present conditions, the best option is $d_1 = 2d_2$. Given the lengths of the t-lines, then the remaining part is to ensure that their design is optimal. More in details, the distance between the transmission lines must not be too small otherwise there will be a huge parasitic capacitance. Regarding the parasitic resistance, special care must be taken when it comes to layout as the chosen metal must be extra-thich -or at least thick- to minimize the total R_L. Also, inductance is to be taken into account, even if it is the least predictable parameter.

To gain a good understandin of the t-lines issue, the best approach is to start designing two short central transmission lines -which will constitute just a small piece of the final distribution- and extract them (for this work, EMX extractor was used) to get a traditional model featuring R_L, C_L, L_L, G_L. In first approximation, for low losses t-line it can be stated that G_L is negligible. Instead of R_L and G_L one can simply refer to the parasitic resistance connected to the inductor, i.e., R_L, and the parasitic resistance relative to the t-line capacitance, i.e., R_C, as reported in the table. After the extraction of the characterisation of the transmission line, it would be wise to make it a dx of the total t-line and to built the structure by stepping multiple dx of line. To understand the situation, one can visualize a dual-core architecture as the one depicted in Figure 2.2. Then, it ought to be multiplied by two as our reference structure is a four-core VCOs architecture.

TABLE 3.1: T-line Models

	Longer T-line	Shorter T-line
d [um]	718	286
L_L [pH]	426	200
R_L [Ω]	12	10
C_L [fF]	66	20
R_C [Ω]	∞	∞

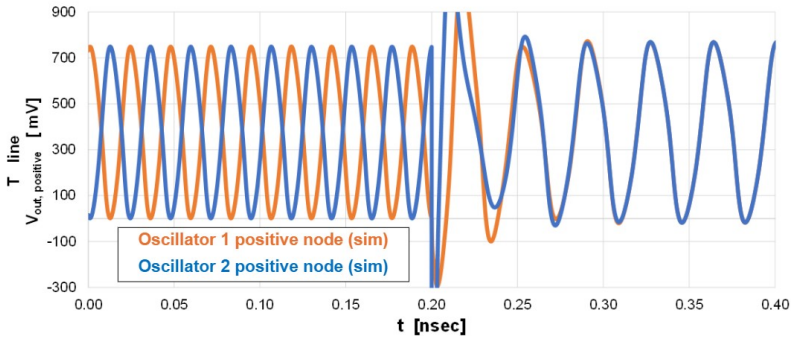

FIGURE 3.13: Voltage from the four oscillators positive nodes from each core.

In this kind of application, the main t-lines -acting as coupling network- must be surrounded by a vertical and horizontal shields, with the first one being connected to the second, which in turns is linked to ground in this work (if convenient, it would be analogous the case where the shield is connected to the positive supply). As both the shields are critical for the design, they must be realized in thick metal layers. As a matter of fact, the presence of the shield will seriously impair the total Q, though it is an unavoidable presence due to the big disturbance that an oscillator may provide to other circuits in a product chip. As the shield is usually non-negligible in terms of parasitics, it must be eventually included in the final design and modelled together with the main t-lines. An advisable strategy is to consider the shield and the main t-lines into the same extraction for dx and then to step them together. To figure out how the entire t-lines ensamble is built, Figure 3.14 can serve as a reference, with the main t-lines being the central green structures and the grounded shield depicted in blue (vertical shield) and orange (horizontal shield).

By respecting the previous calculations -in short, by ensuring that $Z_L << Z_T$- not only the performance, but also the stability is guaranteed. Even if the oscillators might start up in the wrong conditons due to disturbances or other unpredictable events, then the system is robust enough to change into P mode, which is the dominant oscillation mode, as shown in Figure 3.13. In fact, Figure 3.13 shows the positive voltage from each core, taking into account that the cores are strongly coupled two by two, therefore only two waveforms are showed. In other words, there might exist a condition when CP starts

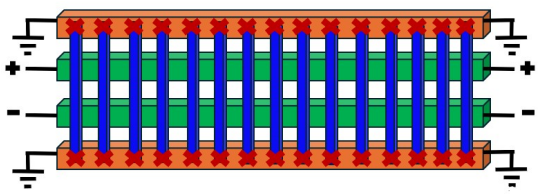

FIGURE 3.14: Proposed transmission line.

up, but then it will surely be followed by a spontaneous transition into P mode.

3.4 Single Core Design

When it comes to the single topology, a careful design should be performed as in P structure, ultimately $Q_T \approx Q_{system}$. Even if the presence of a shield around the main inductor will eventually reduce the original Q_T, obtaining a good quality factor is one of the main goal for the single VCO. The second main target is to ensure that the single CO is power efficient, as to respect the provided spec of having a consumption not overcoming $2.5mW$ for each core.

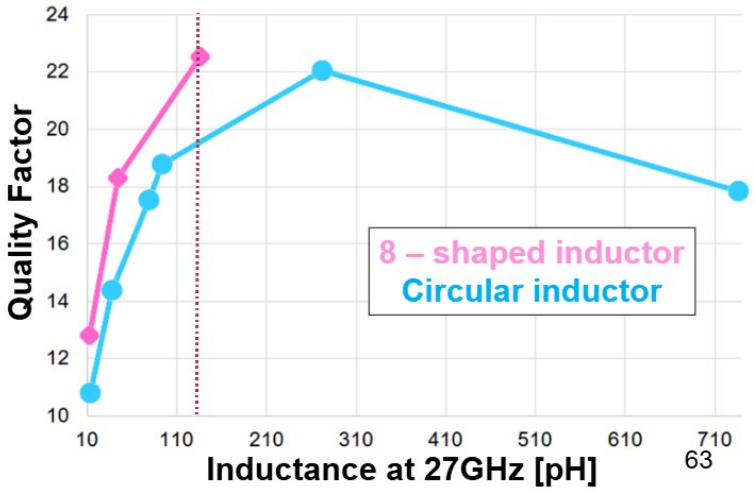

FIGURE 3.15: Voltage from the four oscillators positive nodes from each core.

To respond to the Q instance, a 8-shaped main inductor was adopted as this design guarantees good quality factor and low inductance even at high frequency [94]. In general, getting a low inductance value at high frequency is not banal as both inductance and quality factor tend to rise with frequency. To solve this issue, it is possible to put two circular inductor in parallel, in order to maintain the same high Q and to halve the inductance value. To give some numbers, some Cadence simulations were carried out and the results can be seen in Figure 3.15, where a circular and an 8-shaped inductor, both at $27GHz$, are compared. As depicted, the quality factor of the second is much higher for the same inductance value, hence qualifying the 8-shaped inductor as the best performing design in terms of Q and L_T value, at the cost of doubling the area. Given the abundant vertical area provided in our test-chip, the 8-shaped was the most convenient choice.

Usually, a single circular inductor is chosen as circular shape does guarantee the best quality factor, however due to the specific technology node DRC rules it is often the case that the perfect circle is not allower, therefore it is to be substituted by similar shapes, such as exagons, octagons or other poligons. This is the reason why, in this work, an octagonal shape was employed, as depicted in Figure 3.16, where L_T is represented by the orange poligon.

Regarding the efficiency aspect, the single VCO can be classified as a Class B+Tail. This topology was selected due to its enhanced power efficiency (η_P) and its PN filtering property [13], which were described before. In particular, the PN filtering is performed

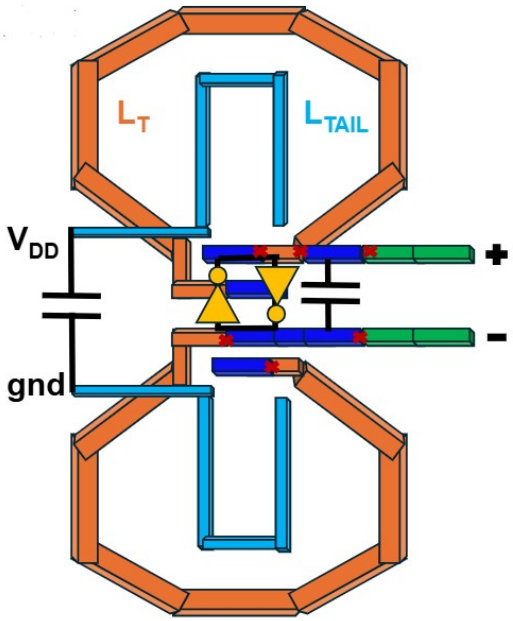

FIGURE 3.16: Single core for the proposed architecture.

through a second tail, called tank tail. Due to the very high frequency of this project, the tank tail was reduced to a single inductor, L_{TAIL}. As there is only one inductor, it is more difficult to tune the tail and respect the condition $f_{TAIL} = 2f_0$ over the entire TR, however the tuning range of this design is small, under 10%, therefore this could not be considered a major disadvantage. Also, by avoiding additional C_{TAIL}, the overall parasitic capacitance is reduced. On the other hand, the tail inductor becomes a complexity when the main inductor is a 8-shaped poligon as the two inductors should not couple, i.e., $k_{T,TAIL} \approx 0$. To guarantee that their coupling factor is as close to zero as possible, the tail inductor was designed in an unconventional shape, a rectangle, which allowed to reduce the coupling at the cost of a significant reduction in Q_{TAIL}. This also made the layout much easier, as shown in Figure 3.16. Despite the layout complications due to L_{TAIL}, an explicit tail was preferrable to an implicit tail [57] due to its superior FoM performance. This proves that, even though Q_{TAIL} is not of primary importance, it does impact the overall performance in a non-negligible way, as shown in Figure 3.18.

It is important to remark that the presence of L_{TAIL} does not impair all the previous calculations for mode and stability as the tail impedance is negligible compared to both the main tank and the transmission line impedances. The tail does impact only the single CO topology and efficiency, which in turn is reflected in the total FoM performance, hence it does affect the FoM penalty.

Another main aspect regards the tank capacitance, i.e., C_T. In a normal VCO, the overall capacitance should be divided into three main terms: switched capacitance, varactor capacitance, parasitic capacitance from the active part -the cross-coupled Gm-, parasitic capacitance from all the other structures attached to or surrounding the core. Because this is a test-chip and there is no PLL to be closed, varactor capacitance was neglected out of simplicity. In turn, switched capacitance was organized in three blocks -fine, small and big capacitors. If small and big are traditionally used, fine capacitors were chosen only for mismatch measurements to be performed later as they provide a capacitance so small -around $2fF$ - to be of little use in practical situations. To put it briefly, extra fine

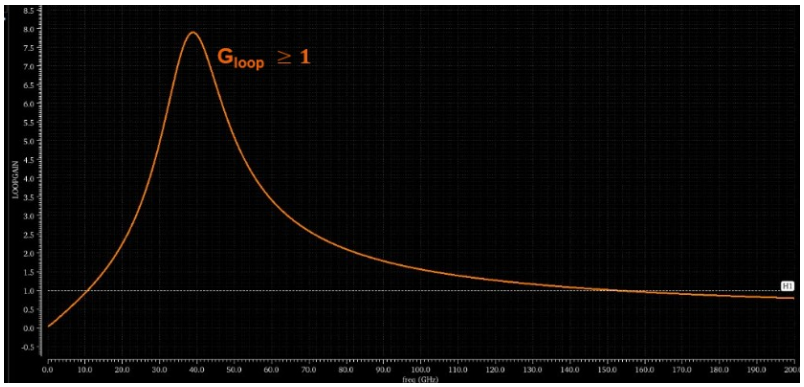

FIGURE 3.17: Stability simulation for loop gain.

FIGURE 3.18: PN performance of a Class B+Tail VCO based on the ratio $\frac{Q_{TAIL}}{Q_T}$.

capacitors mimic mismatches due to process or other uncontrollable variables. As a rule of thumb, the sum of all the extra fine capacitors should overcome the value of a single small capacitors and the same principle applies to small and big capacitors. This is done to guarantee that, in a real product, PLL architecture can close and work properly. This condition was respected in the test-chip. As there was no novelty in switched capacitance structures, the reader can refer to [13] for further details. Switched capacitors are represented also in Figure 3.16, where it can be seen how they are attached to the main core.

In addition, the active part is to be considered too in the design of the single VCO as it does provide the positive R_T counterbalancing the tank resistance and granting oscillation at f_0. As customary, the active part was realised as a cross-couple, adopting both p and nmos transitor to have a major robustness, typical of CMOS designs. Their design is relatively simple as they just have to satisfy Barkhausen conditions to guarantee the start-up. In terms of Cadence simulations, a stability simulation can be performed by opening the loop and obtaining gain and phase. An example of the stability simulation for G_{loop} is provided in Figure 3.17. Two main aspects are to be highlighted when it comes to the active part: the best positive supply and the start-up threshold. First, one may think that the best positive supply is the highest that the technology node may tolerate but this is wrong, especially for the given topology. As the ratio $\frac{I_D}{G_m}$ is optimised

while staying in the transistors saturation region for both p and nmos couples, the best voltage is usually in between the start-up threshold and the maximum tolerable voltage. Second, the start-up threshold, i.e., the minimum voltage guaranteeing the start-up, can be estimated through simulation if the parasitic capacitances are correctly pointed out. As the parastics from Gm cross-coupled can be quite heavy -especially for FinFET designs- optimizing the layout becomes a crucial aspect. After estimating this threshold, it is a good practice to leave at least 5% to 10% margin to guarantee the start-up of the VCO system even in the case of parasitic wrong estimation, especially for this kind of architecture where parasitic capacitances come not only from the active part but also from the SW t-lines. To give some numbers, the overall parasitic capacitance from the active part was estimated around $100fF$, while the total switched capacitance is around $150fF$. For this test-chip, the estimated threshold for the single core start-up was $0.5V$ while the optimum supply was around $0.75V$, with the nominal supply being $1V$.

In conclusion, the single VCO is a Class B + Tail with a 8-shaped main inductor for enhanced efficiency and PN performance. A pn active part was chosen out of robustness and no additional switched capacitor was attached to the tail not to further increase the parasitic contributions. Also, the small programmed TR guarantees that the tail is always well-positioned.

3.4.1 Layout Implementation

As remarked before, layout is a crucial aspect in many designs and especially so for distributed architecture like the proposed one. For this test-chip, the metal stack was the one of the $12nm$ technology node from Global Foundries, as illustrated above. The layout of the single core VCO and of the transmission lines have already been displayed in this thesis, in the previous subchapters, respectively in Figure 3.14 and Figure 3.16.

The legenda regarding the metal layer, anyway, is missing. Now it is reported in Figure 3.19. The figure illustrates the top metal layers, which unfortunately are thick layers as extra-thick layers do not exist in $12nm$ node. This lack of extra-thick layers negatively impact the overall Q.

The layers granting the best Q is aluminum, i.e., LB, the light-blue layer in Figure 3.19. Even though it gives the best quality factor, it was not adopted for the main inductors nor the t-lines -which are the most critical parts of the design concerning the Q- nor for the supplies due to antenna problems. In fact, antenna problems do appear in huge structure and can be solved by inserting a bridge in a higher metal but there is no metal higher than the LB. This is why lower metals were used. The main inductor was implemented in M12, the second highest metal, reaching an area of $102x108\mu m$, while the inner inductor, i.e., L_{TAIL} was realized in aluminum, covering an area of $42x13\mu m$. Regarding the t-lines, the central t-lines from Figure 3.14 have a distance of $28\mu m$, whereas the shielding lines have a distance of $60\mu m$. The main t-lines, instead, were designed in M11 as M12 was reserved to the grounded shield lines, connected through vias (red x symbols as depicted in Figure 3.19) to the vertical shield, done in M10. By selecting a lower metal, the parasitic capacitance from the t-lines may have been minimized but at the cost of an ulterior Q reduction. As in this design, the main parasitic contribution comes from the cross-couple and $C_{MOS} >> C_L$, M10 was selected. Also, choosing M11 for the inner lines and M12 for the horizontal shield made connections much easier as shown in Figure 3.16, thus avoiding ulterior parasitic that vias in the most sensitive spots may have provided. As mentioned just now, the most sensitive spot for the layout are V_+ and V_-. Unfortunately, they are also where all the main elements, i.e., the active part, the switched capacitance, the t-lines, the main and the tail inductors, must be connected.

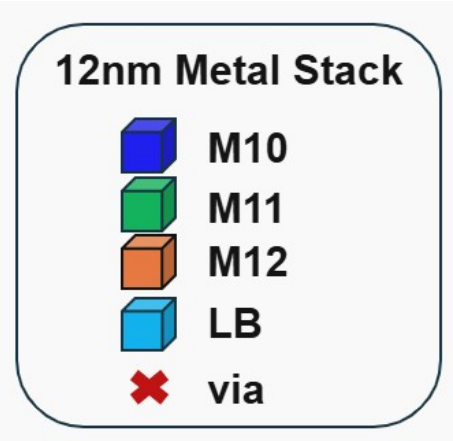

FIGURE 3.19: Partial metal stack layers for 12nm.

FIGURE 3.20: Distribution pattern unit for positive and negative supplies in the test-chip.

Supplies were distributed through a pattern showed in Figure 3.20. This design allowed to avoid major antenna problems and to efficiently distribute and attach the supplies to the block. It is important to note that -to avoid unnecessary disturbances- there exist two different positive supplies, i.e., V_{DD} which is dedicated to the VCO exclusively and V_{DDD} which is used for the digital blocks -like the shift register and the inverters- and for the analog parts of the output chain, like the divider. This strategy served the multiple purpose of protecting the VCO structure, which is easily affected by the smallest disturbance as the design is a voltage-controlled oscillator, and isolating the architecture power consumption contribution from the output chain to get a clearer measurement.

Figure 3.20 only show V_{DD} , the positive voltage supply for the VCO architecture and gnd, the ground (or negative voltage supply) shared by all the blocks. For the ground it was chosen the M12, the orange layer, while for V_{DD} M11 was adopted. Placed under gnd , V_{DDD} is realised in M10, that was the highest remaining metal available.

Once supplies and critical design parts were layouted, the remaining blocks were assigned lower metals, with Gm going from M0 to M11 to perform the metal connection directly on V_+ and V_-.

More detailed information about layout techniques and main issues can be read at [95] and [96], which was used as reference during the realisation of this test-chip layout, mainly to avoid undesired effects which are most common in FinFET layouts.

3.5 Output Chain

This minor subchapter serve the purpose of reminding the reader of the presence of an output chain, whose main goal is to allow the measurement of the VCO output signal. This chain is composed by multiple buffers, a multiplexer and a divider by 2. The multiplexer allows the user to choose between the exit, brought to the output pad directly at 27GHz, and the output signal divided by 2, which is easier to measure and offer a better PN performance. The division by two was chosen as it was the simplest and, at the same time, was considered enough to grant a safe measure. To implement the path selection,

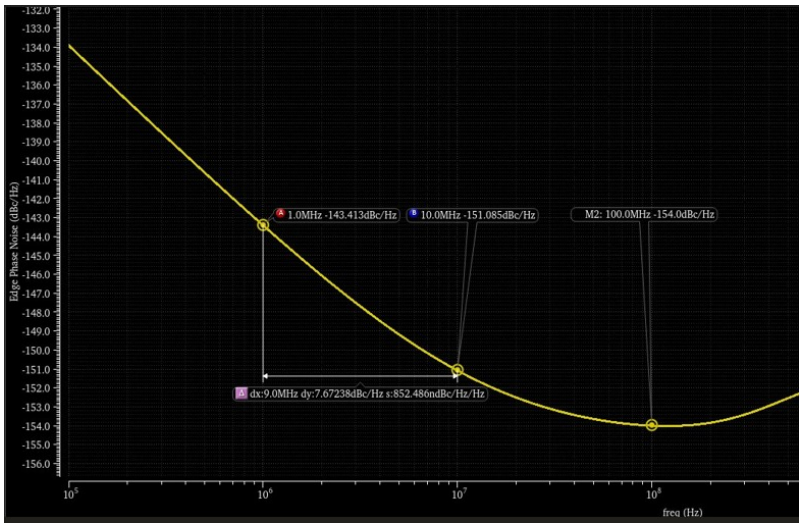

FIGURE 3.21: Cadence simulation to evaluate output chain PN at $27GHz$.

conceptually the user may program a bit in the shift register, which is the same used to control the C_T established through the switched capacitors blocks. In reality, to guarantee a further degree of freedom, used to perform mismatch measurements, there are two shift registers (SRs), one for the first and the second core, one for the third and the fourth core. Their design is identical and they were placed according to a central symmetry. The same degree of freedom obviously applied to C_T as well.

Inside the output chain, there are multiple buffers, which are inverter based. Two different types of buffers where realised: a more performing buffer, called RF buffer, and another one, simply addressed as buffer. The main difference between the buffer and the RF buffer are the layout architecture, with the second being more sophisticated and time-consuming, and the power consumption. In fact, to ensure that the output chain would not produce a significant contribution in terms of PN -thus degrading the overall performance- a great power was provided through the digital supply V_{DDD}. It was estimated -and later confirmed during measurements- that the four output chains consumes around $100mW$ of power. As mentioned before, each VCO core has its own output chain to ensure that the system measurement may be performed from each core.

In order to guarantee that the output chain would not impair the VCO architecture performance, not only two separate supplies were implemented, but also the structures were kept separate in area as well. Another important aspect is the PN performance, which was estimated for the entire output chain, as reported in Figure 3.21. In particular, Figure 3.21 is the result of a Cadence virtuoso simulation carried out for an output chain at $27GHz$ -the maximum operating frequency- connected to a resistance of 50Ω to mimic the load of the output pads. Note that the output chain phase noise contribution at $10MHz$ is $151.10dB$, i.e., $27dB$ below the target PN for the four-core oscillator. In Figure 3.21 there is a rising in PN profile at high frequency, this is just a fake effect coming from the pss calculations, which tend to bet not so accurate. In transient noise, this effect is not observed.

This PN plot shows clearly that PN contribution from the output chain is much less than the PN from the distributed oscillator. As a rule of thumb, the output chain should provide at least $10dB$ less PN than the main architecture, calculated in the worst conditions, in order for the design to be safe.

3.5.1 Divider by 2 Design

Design del divisore pro e contro, metti confronto con altre topologie

In this subchapter, there will be given some more details regarding the design of the divider by two implemented into the output chain. It is preceded by a RF buffer and followed by a simple buffer to restore the signal level.

The division by two was chosen as it was the simplest and, at the same time, was considered enough to grant a safe measure. Multiple designs were studied for this block, starting from Razavi's classical architecture [98] and going through newer proposals [99], [100]. In the end, despite the validity of such structures, a single ended structure like the one proposed in [97] was adopted thanks to its robustness and simplicity, which is mirrored in a layout simplicity that made it the winning choice as the author designed and layouted the structures.

When validating the design in Cadence virtuoso, mainly transient and pss (plus pnoise) simulations were carried out, showing that the PN performance was satisfying. The phase noise contribution from the divider and the remaining blocks of the output chain can be seen in Figure 3.21 at $27GHz$. As mentioned before, the whole output chain is expected to consume $100mW$ with the divider eating up to 40% of the total power consumption. As the divider is never switched off but only excluded from the main signal path, the power consumption of the chain never changes substantially.

The divider was simulated to cover a range from $15GHz$ up to $40GHz$ to demonstrate its robustness, even if the real TR is much smaller. As a matter of fact, the real division that this block is called to perform stays around $27GHz$ with a TR $< 10\%$. In conclusion, the divider is a robust and reusable block that shows no innovation and eats a lot of power, but it carries out its duty. During measurement, its performance was confirmed.

Chapter 4

Measurements and Results

This chapter is dedicated to the measurements. First, the measurement setup is to be introduced and commented, including the instrumentation used, the board prepared for the test-chip and the code written specifically to use these boards. Second, the exact measurements will be presented and commented to see whether the targets were respected and whether any issue did arise and the motivations behind.

The main goal of this section is to highlight that the test-chip overcame the tests and proved the concept behind its realisation. Our goal was to prove the effectiveness of the proposed four-core in-phase oscillators system and to demonstrate that it does provide a robust clock signal with no mode ambiguity and good FoM and PN performance.

In addition, the setup prepared for the test chip was good and easy enough to be able to adapt to other chips and to lay the foundation for other measurements, more complex than the one peformed during this round.

4.1 Measurement Setup

In this subchapter, the way the test-chip will be studied is to be explained. First of all, the chip is to be bonded over a testing board, called RF board, connected to a DC board. The test-chip itself appears as in Figure 4.1. Its partial floorplan can be seen in Figure 4.2.

As it appears from the images above, the test-chip presents four main lines of pads, two horizontal and two vertical ones. Starting from the vertical ones, they represent the RF pads from the first and the fourth cores. They are also the output pads which were mainly used during the presented measurements thanks to them being easier to access with respect to the other output pads. Also, the central series of pads feature RF pads for cores number two and three. Among each series of RF pads, the central one and the two

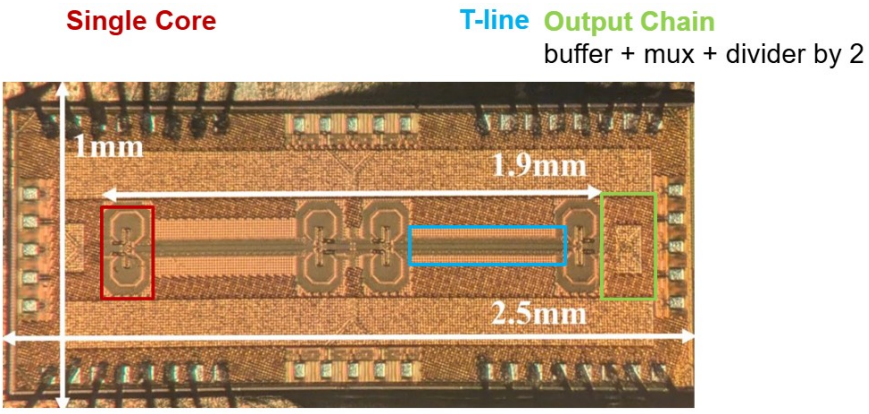

FIGURE 4.1: Photograph of the test-chip.

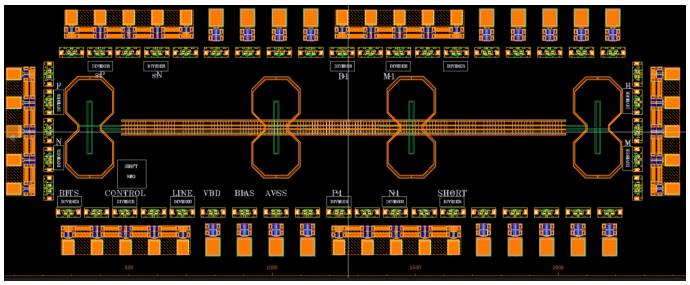

FIGURE 4.2: Partial floorplan for the test-chip.

lateral pads are used for the ground, while the remaining two are used for the real output signal.

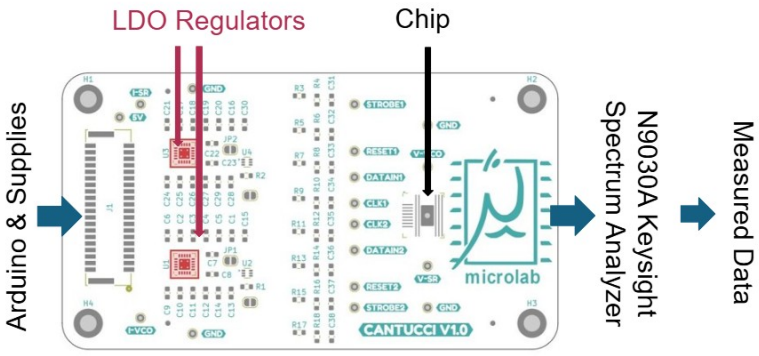

FIGURE 4.3: RF board for the test-chip.

The output pads are where the RF probes land (and slightly scratch the pads surface). Due to the pads surface being touched and a little damaged by every measurement landing, having four different spots for the same measurement ensure its repeatibility. The other set of pads, i.e., the remaining horizontal pads are used below for the SR signals and above for the two positive supplies. All the left pads are used for ground as it is crucial to equally and efficiently distribute it in the test-chip.

Once understood how the chip is connected to the external world, i.e., through probing for the output and through bonding wires for the inputs, the next step is to deal with the boards. Now, the measurement setup will be presented and discussed. First of all, the test-chip, which is the center of our attention- was bonded over a tiny golden area above a testing board, called RF board and shown in Figure 4.3.

The DC board is shown in Figure 4.4. It is the board where the Arduino was placed in order to provide both supplies and input bits for SRs and mux.

Next, it is important to explain how the measurements were carried out. First, a DC measuring campaign took place, in order to ensure that the chip was working properly. The board connections is shown in Figure 4.5. This step can be performed by simply connecting the boards -which were previously tested alone, with no chip bonded on them, throgh an oscillator- to a function generator which can sense the power consumption. The same thing can be done -even if in a more risky way- through a voltmeter. Once checked that the consumption from the VCO supply was under $10mW$ and the digital consumption was around $100mW$ as expected, this step was over. If one have good instruments at his disposal, it can be checked that the VCO power consumption varies

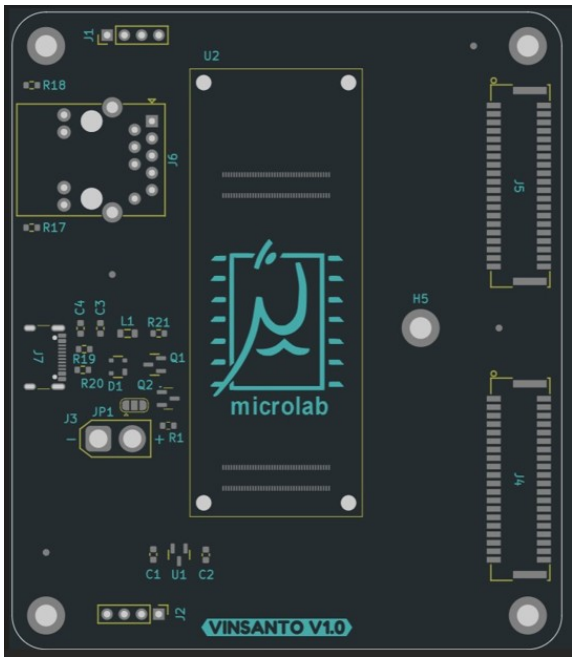

FIGURE 4.4: DC board for Arduino.

when changing the oscillating frequency f_0 through the switched capacitors controlled from the Arduino.

Then, a RF proper campaign was the subsequent step. The RF board was then mounted on the probe station, where there are the probes ready for descending. Then, the probed are linked to the Spectrum Analyzer through high-quality and low-reflections cables and a balun, as shown in Figure 4.6, Figure 4.7 and Figure 4.8. During the RF campaign two main configurations were tested: the first with an external battery as supply and the second -the campaign reported in the following subchapters- with the supplies coming from the LDOs. The second set of measurements achieved better PN performance due to the VCO supply being cleaner.

As it will appear even more clearer with the following results, one of the main disadvantage of the proposed architecture resides in its need for an extremely precise and clean analog supply. During the RF campaign, whose results will be shown in the following paragraphs, the output spectrum was obtained to test the VCO's oscillating frequency, its TR and its robustness to introduced mismatches and eventually its PN performance, from which the FoM will be calculated.

4.1.1 PCB

In this subchapter, the boards are to be explained in a little more detail. First of all, the chip is to be bonded over a testing board, called RF board, connected to a DC board. Once understood how the chip is connected to the external world, i.e., through probing for the output and through bonding wires for the inputs, the next step is to deal with the boards. Now, the measurement setup will be presented and discussed. First of all, the test-chip, which is the center of our attention- was bonded over a tiny golden area above a testing board, called RF board and shown in Figure 4.3.

As depicted in Figure 4.3, the chip is placed on the right side to facilitate the probe descending, while the connections to the input are performed on the left side through connectors. Bonded on the chip, there are several elements, including two LDOs to clean

FIGURE 4.5: RF and DC boards connected, ready for measurement.

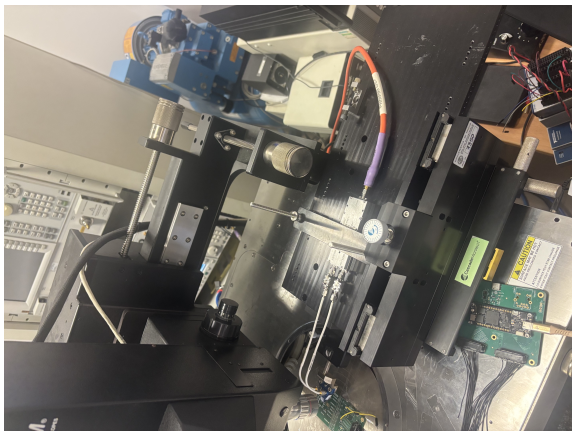

FIGURE 4.6: RF measurement setup.

the supply and many filtering capacitors. All these components was soldered on the board. To give anothe degree of freedom, the LDOs may be easily disconnected by cutting their connection to the chip and substituted by an external supplies provided through the metallic holes, where a pin can easily be soldered by hands in a few minutes. The RF board is called "Cantucci" after an Italian variety of cookies which are meant to be eaten with a type of wine called "Vinsanto".

Indeed, "Vinsanto" is the DC board connected to the RF board. The DC board is shown in Figure 4.4. It is the board where the Arduino was placed, more specifically in the area where the Microlab symbol is carved. The Arduino is a recent version featuring lots of pads, thus is a little bit of an overkill for this kind of application; nevertheless it was chosen as to permit the DC board to be reused also for more complex measurement setups.

The main purpose of the Arduino, connected to this author's personal laptop through a simple USBc cable, is to bring both the supplies and the input bits for the shift registers and the multiplexers to the RF board. It is important to remark that the supplies can also be delivered to the RF board through external sources, for example a battery, while the bits only way-in is represented by the connection through the Arduino. Therefore, the Arduino is fundamental to set the system oscillating frequency through the switched capacitors block and the output path by commanding the multiplexer for each VCO.

Note that the Arduino is simple to use but it is fundamental to correctly initialise and

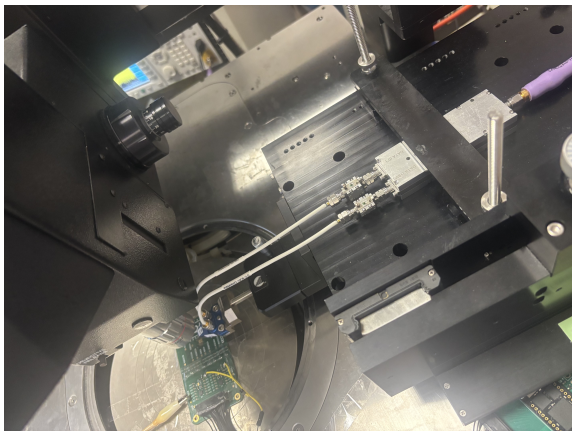

FIGURE 4.7: RF measurement setup.

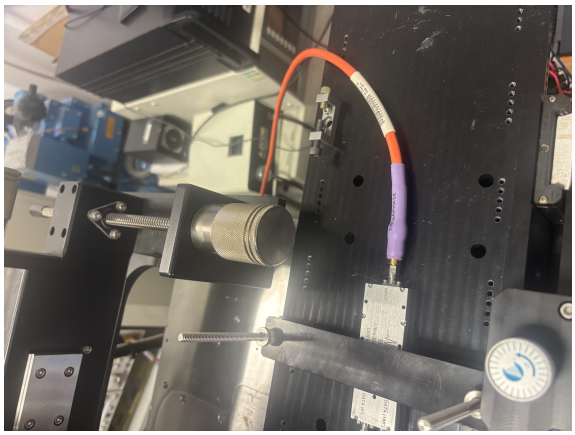

FIGURE 4.8: RF measurement setup.

set all the used pins. This goal was obtained by physically verifying the connections for the desired pins and then doing a proper code for initialization. The code for the Arduino Portenta is reported in the following box.

LISTING 4.1: Code for Vinsanto

```
1
2   //#include <Arduino_PortentaBreakout.h>
3
4   /************ I/O PINS ************/
5   #define CLK1_GPIO     GPIOC
6   #define CLK1_PIN      GPIO_PIN_6
7   #define DATAIN1_GPIO     GPIOC
8   #define DATAIN1_PIN      GPIO_PIN_7
9   #define CLK2_GPIO     GPIOI
10  #define CLK2_PIN      GPIO_PIN_1
11  //#define DATAIN2_GPIO     GPIOC
12  //#define DATAIN2_PIN      GPIO_PIN_3
13  #define DATAIN2_GPIO     GPIOJ
14  #define DATAIN2_PIN      GPIO_PIN_9
15
16  //#define STROBE1_GPIO     GPIOJ
17  //#define STROBE1_PIN      GPIO_PIN_11
```

```
18  #define STROBE1_GPIO    GPIOD
19  #define STROBE1_PIN     GPIO_PIN_5
20  #define STROBE2_GPIO    GPIOG
21  #define STROBE2_PIN     GPIO_PIN_9
22  //#define RESET1_GPIO    GPIOG
23  //#define RESET1_PIN     GPIO_PIN_7
24  #define RESET1_GPIO    GPIOA
25  #define RESET1_PIN     GPIO_PIN_8
26  #define RESET2_GPIO    GPIOC
27  #define RESET2_PIN     GPIO_PIN_2
28
29
30  #define SEL1_GPIO GPIOB
31  #define SEL1_PIN GPIO_PIN_4
32  #define SEL2_GPIO GPIOB
33  #define SEL2_PIN GPIO_PIN_15
34  #define SEL3_GPIO GPIOB
35  #define SEL3_PIN GPIO_PIN_14
36  #define SEL4_GPIO GPIOD
37  #define SEL4_PIN GPIO_PIN_7
38  #define SEL5_GPIO GPIOD
39  #define SEL5_PIN GPIO_PIN_6
40  #define SEL6_GPIO GPIOB
41  #define SEL6_PIN GPIO_PIN_8
42  #define SEL7_GPIO GPIOH
43  #define SEL7_PIN GPIO_PIN_13
44  #define SEL8_GPIO GPIOB
45  #define SEL8_PIN GPIO_PIN_6
46  #define SEL9_GPIO GPIOB
47  #define SEL9_PIN GPIO_PIN_7
48  #define SEL10_GPIO GPIOB
49  #define SEL10_PIN GPIO_PIN_2
50  #define SEL11_GPIO GPIOE
51  #define SEL11_PIN GPIO_PIN_2
52  #define SEL12_GPIO GPIOA
53  #define SEL12_PIN GPIO_PIN_10
54
55  /* SEL1 = 50mV SEL2 = 100mV SEL3 = 200mV
56  SEL4 = 400 mV SEL5 = 800mV SEL6 = 1.6V
57  If jumper on
58  SEL1 = 25mV SEL2 = 50mV SEL3 = 100mV
59  SEL4 = 200mV SEL5 = 400 mV SEL6 = 800mV */
60
61  /************ END I/O PINS ************/
62
63  byte array1[4] = {0b10101010, 0b11001100, 0b11110000,
        0b00001111};
64  byte array2[4] = {0b10101010, 0b11001100, 0b11110000,
        0b00001111};
65
66  /************* SETUP *****************/
67  void setup() {
68
69    Serial.begin(115200);
70    delay(3000);
71    // while(!Serial.available()){}
72    Serial.println("Welcome␣to␣VINSANTO␣Board!");
```

```
73      MX_GPIO_Init();
74      // Init GPIO with HAL STM32
75      initCycleCounter();
76      pinMode(LEDB, OUTPUT);
77      pinMode(LEDR, OUTPUT);
78      pinMode(LEDG, OUTPUT);
79      digitalWrite(LEDG, LOW); //ACTIVE LOW
80    }
81    /************* END SETUP *****************/
82
83    /************* LOOP **************/
84    void loop() {
85
86      stateMachine();
87
88    }
89    /*************** END LOOP *************/
90
91    /****************** FUNCTIONS *************/
92
93    /*************** LOAD DATA *************/
94
95    void load_data() {
96      byte buffer[5];
97      int result = 0;
98
99      if (Serial.available()){
100
101       result = Serial.readBytesUntil('\n', buffer, 5);
102       Serial.print("Number␣of␣read␣byte:␣");
103       Serial.println(result);
104       Serial.print("The␣string␣is:␣");
105       for (int i = 0; i < 4; i++){
106         Serial.print(buffer[i]);
107       }
108       Serial.println("");
109       Serial.println("END");
110       // delay(100);
111
112     }
113
114   }
115   /*************** END LOAD DATA *************/
116
117   /*********** STROBE ***********/
118
119   void strobe(GPIO_TypeDef *strobePort, uint16_t strobePin){
120     HAL_GPIO_WritePin(strobePort, strobePin, GPIO_PIN_SET);
121     delayCycles(800000);
122     HAL_GPIO_WritePin(strobePort, strobePin, GPIO_PIN_RESET);
123     delayCycles(800000);
124   }
125   /*********** END STROBE ***********/
126
127   /************* RESET **************/
128   void reset(GPIO_TypeDef *resetPort, uint16_t resetPin,
        GPIO_TypeDef *clkPort, uint16_t clkPin){
```

```
129     HAL_GPIO_WritePin(resetPort, resetPin, GPIO_PIN_RESET);
130     delayCycles(800000);
131     HAL_GPIO_WritePin(clkPort, clkPin, GPIO_PIN_SET);
132     delayCycles(800000);
133     HAL_GPIO_WritePin(clkPort, clkPin, GPIO_PIN_RESET);
134     delayCycles(800000);
135     HAL_GPIO_WritePin(resetPort, resetPin, GPIO_PIN_SET);
136   }
137   /************** END RESET **************/
138
139   /*************** WRITE SR ***************/
140   void write_SR(byte *array, int size, GPIO_TypeDef *dataPort,
        uint16_t dataPin, GPIO_TypeDef *clkPort, uint16_t clkPin) {
141     int bit = 0;
142     DWT->CYCCNT = 0;
143     noInterrupts();
144
145     for (int i = 0; i < size; i++) {
146       for (int j = 7; j >= 0; j--) {
147         bit = (array[i] >> j) & 1;
148          (GPIO_PIN_SET or GPIO_PIN_RESET)
149         HAL_GPIO_WritePin(dataPort, dataPin, (bit)
150          GPIO_PIN_SET : GPIO_PIN_RESET);
151         //delayCycles(40000000);
152         //delayCycles(16000000);
153         delayCycles(800000);
154         // Clock impulse
155         HAL_GPIO_WritePin(clkPort, clkPin, GPIO_PIN_SET);
156         //delayCycles(40000000);
157         delayCycles(12800000);
158         HAL_GPIO_WritePin(clkPort, clkPin, GPIO_PIN_RESET);
159         //delayCycles(40000000);
160         //delayCycles(1600000);
161         delayCycles(12800000);
162       }
163     }
164     interrupts();
165     Serial.println("Bits␣have␣been␣written");
166   }
167   /*************** END WRITE SR ***************/
168
169   /*************** STATE MACHINE ************/
170   void stateMachine(){
171
172     if (Serial.available()){
173
174       String command = Serial.readStringUntil('\n');
175       command.trim();
176       //Serial.println(command);
177       digitalWrite(LEDG, HIGH); //ACTIVE LOW
178       digitalWrite(LEDB, LOW); //ACTIVE LOW
179       digitalWrite(LEDR, HIGH); //ACTIVE LOW
180
181
182
183
184       // Understand the command and execute
```

```
185
186       if (command == "STROBE1") {
187         Serial.println("STROBE1ACK");
188         strobe(STROBE1_GPIO, STROBE1_PIN);
189       } else if (command == "RESET1"){
190         Serial.println("RESET1ACK");
191         reset(RESET1_GPIO, RESET1_PIN, CLK1_GPIO, CLK1_PIN);
192       }  else if (command == "STROBE2"){
193         Serial.println("STROBE2ACK");
194         strobe(STROBE2_GPIO, STROBE2_PIN);
195       }  else if (command == "RESET2"){
196         Serial.println("RESET2ACK");
197         reset(RESET2_GPIO, RESET2_PIN, CLK2_GPIO, CLK2_PIN);
198       } else if (command == "WRITE1"){
199         Serial.println("WRITE1ACK");
200         //write_SR(array1, 4, DATAIN1_GPIO, DATAIN1_PIN,
                CLK1_GPIO, CLK1_PIN);
201         while (Serial.available() < 4);  // wait for all 4 bytes
202         byte data[4];
203         for (int i = 0; i < 4; i++) {
204           data[i] = Serial.read();
205         }
206         write_SR(data, 4, DATAIN1_GPIO, DATAIN1_PIN, CLK1_GPIO,
                CLK1_PIN);
207       } else if (command == "WRITE2"){
208         Serial.println("WRITE2ACK");
209         //write_SR(array2, 4, DATAIN2_GPIO, DATAIN2_PIN,
                CLK2_GPIO, CLK2_PIN);
210         while (Serial.available() < 4);  // wait for all 4 bytes
211         byte data[4];
212         for (int i = 0; i < 4; i++) {
213           data[i] = Serial.read();
214         }
215         write_SR(data, 4, DATAIN2_GPIO, DATAIN2_PIN, CLK2_GPIO,
                CLK2_PIN);
216       }  else if (command == "PIN1_ON"){
217         Serial.println("PIN1ACK_ON");
218         HAL_GPIO_WritePin(SEL1_GPIO, SEL1_PIN, GPIO_PIN_SET);
219       } else if (command == "PIN1_OFF"){
220         Serial.println("PIN1ACK_OFF");
221         HAL_GPIO_WritePin(SEL1_GPIO, SEL1_PIN, GPIO_PIN_RESET);
222       }   else if (command == "PIN2_ON"){
223         Serial.println("PIN2ACK_ON");
224         HAL_GPIO_WritePin(SEL2_GPIO, SEL2_PIN, GPIO_PIN_SET);
225       } else if (command == "PIN2_OFF"){
226         Serial.println("PIN2ACK_OFF");
227         HAL_GPIO_WritePin(SEL2_GPIO, SEL2_PIN, GPIO_PIN_RESET);
228       }   else if (command == "PIN3_ON"){
229         Serial.println("PIN3ACK_ON");
230         HAL_GPIO_WritePin(SEL3_GPIO, SEL3_PIN, GPIO_PIN_SET);
231       } else if (command == "PIN3_OFF"){
232         Serial.println("PIN3ACK_OFF");
233         HAL_GPIO_WritePin(SEL3_GPIO, SEL3_PIN, GPIO_PIN_RESET);
234       }   else if (command == "PIN4_ON"){
235         Serial.println("PIN4ACK_ON");
236         HAL_GPIO_WritePin(SEL4_GPIO, SEL4_PIN, GPIO_PIN_SET);
237       } else if (command == "PIN4_OFF"){
```

```
238         Serial.println("PIN4ACK_OFF");
239         HAL_GPIO_WritePin(SEL4_GPIO, SEL4_PIN, GPIO_PIN_RESET);
240       }   else if (command == "PIN5_ON"){
241         Serial.println("PIN5ACK_ON");
242         HAL_GPIO_WritePin(SEL5_GPIO, SEL5_PIN, GPIO_PIN_SET);
243       } else if (command == "PIN5_OFF"){
244         Serial.println("PIN5ACK_ON");
245         HAL_GPIO_WritePin(SEL5_GPIO, SEL5_PIN, GPIO_PIN_SET);
246       }   else if (command == "PIN6_ON"){
247         Serial.println("PIN6ACK_ON");
248         HAL_GPIO_WritePin(SEL6_GPIO, SEL6_PIN, GPIO_PIN_SET);
249       } else if (command == "PIN6_OFF"){
250         Serial.println("PIN6ACK_ON");
251         HAL_GPIO_WritePin(SEL6_GPIO, SEL6_PIN, GPIO_PIN_SET);
252       }   else if (command == "PIN7_ON"){
253         Serial.println("PIN7ACK_ON");
254         HAL_GPIO_WritePin(SEL7_GPIO, SEL7_PIN, GPIO_PIN_SET);
255       } else if (command == "PIN7_OFF"){
256         Serial.println("PIN7ACK_OFF");
257         HAL_GPIO_WritePin(SEL7_GPIO, SEL7_PIN, GPIO_PIN_RESET);
258       }   else if (command == "PIN8_ON"){
259         Serial.println("PIN8ACK_ON");
260         HAL_GPIO_WritePin(SEL8_GPIO, SEL8_PIN, GPIO_PIN_SET);
261       } else if (command == "PIN8_OFF"){
262         Serial.println("PIN8ACK_OFF");
263         HAL_GPIO_WritePin(SEL8_GPIO, SEL8_PIN, GPIO_PIN_RESET);
264       }   else if (command == "PIN9_ON"){
265         Serial.println("PIN9ACK_ON");
266         HAL_GPIO_WritePin(SEL9_GPIO, SEL9_PIN, GPIO_PIN_SET);
267       } else if (command == "PIN9_OFF"){
268         Serial.println("PIN9ACK_OFF");
269         HAL_GPIO_WritePin(SEL9_GPIO, SEL9_PIN, GPIO_PIN_RESET);
270       }   else if (command == "PIN10_ON"){
271         Serial.println("PIN10ACK_ON");
272         HAL_GPIO_WritePin(SEL10_GPIO, SEL10_PIN, GPIO_PIN_SET);
273       } else if (command == "PIN10_OFF"){
274         Serial.println("PIN10ACK_OFF");
275         HAL_GPIO_WritePin(SEL10_GPIO, SEL10_PIN, GPIO_PIN_RESET);
276       }   else if (command == "PIN11_ON"){
277         Serial.println("PIN11ACK_ON");
278         HAL_GPIO_WritePin(SEL11_GPIO, SEL11_PIN, GPIO_PIN_SET);
279       } else if (command == "PIN11_OFF"){
280         Serial.println("PIN11ACK_ON");
281         HAL_GPIO_WritePin(SEL11_GPIO, SEL11_PIN, GPIO_PIN_SET);
282       }   else if (command == "PIN12_ON"){
283         Serial.println("PIN12ACK_ON");
284         HAL_GPIO_WritePin(SEL12_GPIO, SEL12_PIN, GPIO_PIN_SET);
285       } else if (command == "PIN12_OFF"){
286         Serial.println("PIN12ACK_ON");
287         HAL_GPIO_WritePin(SEL12_GPIO, SEL12_PIN, GPIO_PIN_SET);
288       }
289
290
291       else {
292         digitalWrite(LEDG, HIGH); //ACTIVE LOW
293         digitalWrite(LEDR, LOW); //ACTIVE LOW
294         digitalWrite(LEDB, HIGH); //ACTIVE LOW
```

```
295         Serial.println("Command␣not␣recognized");
296       }
297
298       Serial.println("");
299       Serial.println("END");
300       delay(1000);
301       digitalWrite(LEDG, LOW); //ACTIVE LOW
302       digitalWrite(LEDR, HIGH); //ACTIVE LOW
303       digitalWrite(LEDB, HIGH); //ACTIVE LOW
304     }
305
306   }
307   /*************** END STATE MACHINE ***********/
308
309   /****************** INIT CYCLE COUNTER ******************/
310   // Call this function once (for example, in setup()) to enable
        the DWT cycle counter
311   void initCycleCounter() {
312     // Enable TRC (Trace Control)
313     CoreDebug->DEMCR |= CoreDebug_DEMCR_TRCENA_Msk;
314     // Reset the cycle counter
315     DWT->CYCCNT = 0;
316     // Enable the cycle counter
317     DWT->CTRL |= DWT_CTRL_CYCCNTENA_Msk;
318   }
319   /****************** END INIT CYCLE COUNTER ******************/
320
321   /****************** DELAY CYCLES *************/
322   // Busy-wait delay for a given number of CPU cycles.
323   static inline void delayCycles(uint32_t cycles) {
324     uint32_t start = DWT->CYCCNT;
325     while ((DWT->CYCCNT - start) < cycles) {
326       // busy-wait loop
327     }
328   }
329   /****************** END DELAY CYCLES *************/
330
331   /************** GET BIT ************/
332   byte getBit(byte *array, int bitPosition) {
333     int byteIndex = bitPosition / 8;       // find the
          corrispondig bit
334     int bitIndex = 7 - (bitPosition % 8);  // find the bit's
          position
335     return (array[byteIndex] >> bitIndex) & 1;
336   }
337   /************** END GET BIT ************/
338
339   void provaLDO(){
340
341
342
343     HAL_GPIO_WritePin(SEL1_GPIO, SEL1_PIN, GPIO_PIN_SET);
344
345
346
347     delay(1000);
348
```

```
349
350
351     HAL_GPIO_WritePin(SEL2_GPIO, SEL2_PIN, GPIO_PIN_SET);
352
353
354
355     delay(1000);
356
357
358
359     HAL_GPIO_WritePin(SEL3_GPIO, SEL3_PIN, GPIO_PIN_SET);
360
361
362
363     delay(1000);
364
365
366
367     HAL_GPIO_WritePin(SEL4_GPIO, SEL4_PIN, GPIO_PIN_SET);
368
369
370
371     delay(1000);
372
373
374
375     HAL_GPIO_WritePin(SEL5_GPIO, SEL5_PIN, GPIO_PIN_SET);
376
377
378
379     delay(1000);
380
381
382
383     HAL_GPIO_WritePin(SEL6_GPIO, SEL6_PIN, GPIO_PIN_SET);
384
385
386
387     delay(1000);
388
389
390
391     HAL_GPIO_WritePin(SEL7_GPIO, SEL7_PIN, GPIO_PIN_SET);
392
393
394
395     delay(1000);
396
397
398
399     HAL_GPIO_WritePin(SEL8_GPIO, SEL8_PIN, GPIO_PIN_SET);
400
401
402
403     delay(1000);
404
405
```

```
406
407     HAL_GPIO_WritePin(SEL9_GPIO, SEL9_PIN, GPIO_PIN_SET);
408
409
410
411     delay(1000);
412
413
414
415     HAL_GPIO_WritePin(SEL10_GPIO, SEL10_PIN, GPIO_PIN_SET);
416
417
418
419     delay(1000);
420
421
422
423     HAL_GPIO_WritePin(SEL11_GPIO, SEL11_PIN, GPIO_PIN_SET);
424
425
426
427     delay(1000);
428
429
430
431     HAL_GPIO_WritePin(SEL12_GPIO, SEL12_PIN, GPIO_PIN_SET);
432
433
434
435     delay(1000);
436
437
438
439   }
440
441
442
443
444   /************** MX GPIO INIT ***********/
445   void MX_GPIO_Init(void)
446   {
447
448     GPIO_InitTypeDef GPIO_InitStruct = {0};
449
450     /* GPIO Ports Clock Enable */
451     __HAL_RCC_GPIOA_CLK_ENABLE();
452     __HAL_RCC_GPIOG_CLK_ENABLE();
453     __HAL_RCC_GPIOD_CLK_ENABLE();
454     __HAL_RCC_GPIOI_CLK_ENABLE();
455     __HAL_RCC_GPIOH_CLK_ENABLE();
456     __HAL_RCC_GPIOC_CLK_ENABLE();
457     __HAL_RCC_GPIOE_CLK_ENABLE();
458     __HAL_RCC_GPIOK_CLK_ENABLE();
459     __HAL_RCC_GPIOJ_CLK_ENABLE();
460
461     /*Configure GPIO pin Output Level */ //SEL1, 6
462     HAL_GPIO_WritePin(GPIOB, GPIO_PIN_4|GPIO_PIN_8, GPIO_PIN_SET);
```

```
463
464     /*Configure GPIO pin Output Level */ //SEL2,3
465     HAL_GPIO_WritePin(GPIOB, GPIO_PIN_15|GPIO_PIN_14,
            GPIO_PIN_SET);
466
467     /*Configure GPIO pin Output Level */ //SEL4,5
468     HAL_GPIO_WritePin(GPIOD, GPIO_PIN_7|GPIO_PIN_6, GPIO_PIN_SET);
469
470     /*Configure GPIO pin Output Level */ //SEL7
471     HAL_GPIO_WritePin(GPIOH, GPIO_PIN_13, GPIO_PIN_SET);
472
473     /*Configure GPIO pin Output Level */ //SEL8,9
474     HAL_GPIO_WritePin(GPIOB, GPIO_PIN_7|GPIO_PIN_6, GPIO_PIN_SET);
475
476     /*Configure GPIO pin Output Level */ //SEL10
477     HAL_GPIO_WritePin(GPIOB, GPIO_PIN_2, GPIO_PIN_SET);
478
479     /*Configure GPIO pin Output Level */ //SEL11
480     HAL_GPIO_WritePin(GPIOE, GPIO_PIN_2, GPIO_PIN_SET);
481
482     /*Configure GPIO pin Output Level */ //SEL12
483     HAL_GPIO_WritePin(GPIOA, GPIO_PIN_10, GPIO_PIN_SET);
484
485     /*Configure GPIO pin Output Level */
486     HAL_GPIO_WritePin(GPIOG, GPIO_PIN_10|GPIO_PIN_3, GPIO_PIN_SET);
487
488     /*Configure GPIO pin Output Level */
489     HAL_GPIO_WritePin(GPIOG, GPIO_PIN_9, GPIO_PIN_RESET);
490
491     /*Configure GPIO pin Output Level */ //EX PIN G7, RESET1
492     HAL_GPIO_WritePin(GPIOI, GPIO_PIN_0, GPIO_PIN_RESET);
493
494     /*Configure GPIO pin Output Level */
495     //HAL_GPIO_WritePin(GPIOD, GPIO_PIN_5|GPIO_PIN_4,
            GPIO_PIN_SET);
496
497     /*Configure GPIO pin Output Level */
498     HAL_GPIO_WritePin(GPIOI, GPIO_PIN_1, GPIO_PIN_RESET);
499
500     /*Configure GPIO pin Output Level */ //DATAIN2
501     HAL_GPIO_WritePin(GPIOJ, GPIO_PIN_9, GPIO_PIN_RESET);
502
503     /*Configure GPIO pin Output Level */
504     HAL_GPIO_WritePin(GPIOH, GPIO_PIN_15|GPIO_PIN_10|GPIO_PIN_6,
            GPIO_PIN_SET);
505
506     /*Configure GPIO pin Output Level */
507     HAL_GPIO_WritePin(GPIOC, GPIO_PIN_15|GPIO_PIN_13,
            GPIO_PIN_SET);
508
509     /*Configure GPIO pin Output Level */
510     HAL_GPIO_WritePin(GPIOE, GPIO_PIN_3, GPIO_PIN_SET);
511
512     /*Configure GPIO pin Output Level */
513     HAL_GPIO_WritePin(GPIOC,
            GPIO_PIN_7|GPIO_PIN_6|GPIO_PIN_2|GPIO_PIN_3,
            GPIO_PIN_RESET);
```

```
514
515     /*Configure GPIO pin Output Level */
516     HAL_GPIO_WritePin(GPIOK, GPIO_PIN_1, GPIO_PIN_SET);
517
518     /*Configure GPIO pin Output Level */
519     //HAL_GPIO_WritePin(GPIOJ, GPIO_PIN_11, GPIO_PIN_RESET);
520     HAL_GPIO_WritePin(GPIOA, GPIO_PIN_8, GPIO_PIN_RESET);
521
522     /*Configure GPIO pin Output Level */
523     HAL_GPIO_WritePin(GPIOD, GPIO_PIN_5, GPIO_PIN_RESET);
524
525     /*Configure GPIO pin Output Level */
526     HAL_GPIO_WritePin(GPIOJ, GPIO_PIN_7, GPIO_PIN_SET);
527
528     /*Configure GPIO pins : PG10 PG3 */
529     GPIO_InitStruct.Pin = GPIO_PIN_10|GPIO_PIN_3;
530     GPIO_InitStruct.Mode = GPIO_MODE_OUTPUT_OD;
531     GPIO_InitStruct.Pull = GPIO_NOPULL;
532     GPIO_InitStruct.Speed = GPIO_SPEED_FREQ_LOW;
533     HAL_GPIO_Init(GPIOG, &GPIO_InitStruct);
534
535     /*Configure GPIO pins : PG9 */
536     GPIO_InitStruct.Pin = GPIO_PIN_9;
537     GPIO_InitStruct.Mode = GPIO_MODE_OUTPUT_PP;
538     GPIO_InitStruct.Pull = GPIO_NOPULL;
539     GPIO_InitStruct.Speed = GPIO_SPEED_FREQ_VERY_HIGH;
540     HAL_GPIO_Init(GPIOG, &GPIO_InitStruct);
541
542     /*Configure GPIO pins : PD3 */ //PRIMA ERA G7, PIN RESET1
543     GPIO_InitStruct.Pin = GPIO_PIN_3;
544     GPIO_InitStruct.Mode = GPIO_MODE_OUTPUT_PP;
545     GPIO_InitStruct.Pull = GPIO_NOPULL;
546     GPIO_InitStruct.Speed = GPIO_SPEED_FREQ_VERY_HIGH;
547     HAL_GPIO_Init(GPIOD, &GPIO_InitStruct);
548
549     /*Configure GPIO pins : PD5 PD4 */
550     //GPIO_InitStruct.Pin = GPIO_PIN_5|GPIO_PIN_4;
551     //GPIO_InitStruct.Mode = GPIO_MODE_OUTPUT_OD;
552     //GPIO_InitStruct.Pull = GPIO_NOPULL;
553     //GPIO_InitStruct.Speed = GPIO_SPEED_FREQ_LOW;
554     //HAL_GPIO_Init(GPIOD, &GPIO_InitStruct);
555
556     /*Configure GPIO pins : PD5 */ //STROBE
557     GPIO_InitStruct.Pin = GPIO_PIN_5;
558     GPIO_InitStruct.Mode = GPIO_MODE_OUTPUT_PP;
559     GPIO_InitStruct.Pull = GPIO_NOPULL;
560     GPIO_InitStruct.Speed = GPIO_SPEED_FREQ_VERY_HIGH;
561     HAL_GPIO_Init(GPIOD, &GPIO_InitStruct);
562
563     /*Configure GPIO pins : PD5 */ //DATAIN2
564     GPIO_InitStruct.Pin = GPIO_PIN_9;
565     GPIO_InitStruct.Mode = GPIO_MODE_OUTPUT_PP;
566     GPIO_InitStruct.Pull = GPIO_NOPULL;
567     GPIO_InitStruct.Speed = GPIO_SPEED_FREQ_VERY_HIGH;
568     HAL_GPIO_Init(GPIOJ, &GPIO_InitStruct);
569
570     /*Configure GPIO pin : PI1 */
```

```
571     GPIO_InitStruct.Pin = GPIO_PIN_1;
572     GPIO_InitStruct.Mode = GPIO_MODE_OUTPUT_PP;
573     GPIO_InitStruct.Pull = GPIO_NOPULL;
574     GPIO_InitStruct.Speed = GPIO_SPEED_FREQ_VERY_HIGH;
575     HAL_GPIO_Init(GPIOI, &GPIO_InitStruct);
576
577     /*Configure GPIO pins : PH15 PH10 PH6 */
578     GPIO_InitStruct.Pin = GPIO_PIN_15|GPIO_PIN_10|GPIO_PIN_6;
579     GPIO_InitStruct.Mode = GPIO_MODE_OUTPUT_OD;
580     GPIO_InitStruct.Pull = GPIO_NOPULL;
581     GPIO_InitStruct.Speed = GPIO_SPEED_FREQ_LOW;
582     HAL_GPIO_Init(GPIOH, &GPIO_InitStruct);
583
584     /*Configure GPIO pins : PC15 PC13 */
585     GPIO_InitStruct.Pin = GPIO_PIN_15|GPIO_PIN_13;
586     GPIO_InitStruct.Mode = GPIO_MODE_OUTPUT_OD;
587     GPIO_InitStruct.Pull = GPIO_NOPULL;
588     GPIO_InitStruct.Speed = GPIO_SPEED_FREQ_LOW;
589     HAL_GPIO_Init(GPIOC, &GPIO_InitStruct);
590
591     /*Configure GPIO pin : PE3 */
592     GPIO_InitStruct.Pin = GPIO_PIN_3;
593     GPIO_InitStruct.Mode = GPIO_MODE_OUTPUT_OD;
594     GPIO_InitStruct.Pull = GPIO_NOPULL;
595     GPIO_InitStruct.Speed = GPIO_SPEED_FREQ_LOW;
596     HAL_GPIO_Init(GPIOE, &GPIO_InitStruct);
597
598     /*Configure GPIO pins : PC7 PC6 PC2 PC3 */
599     GPIO_InitStruct.Pin =
          GPIO_PIN_7|GPIO_PIN_6|GPIO_PIN_2|GPIO_PIN_3;
600     GPIO_InitStruct.Mode = GPIO_MODE_OUTPUT_PP;
601     GPIO_InitStruct.Pull = GPIO_NOPULL;
602     GPIO_InitStruct.Speed = GPIO_SPEED_FREQ_VERY_HIGH;
603     HAL_GPIO_Init(GPIOC, &GPIO_InitStruct);
604
605     /*Configure GPIO pin : PK1 */
606     GPIO_InitStruct.Pin = GPIO_PIN_1;
607     GPIO_InitStruct.Mode = GPIO_MODE_OUTPUT_OD;
608     GPIO_InitStruct.Pull = GPIO_NOPULL;
609     GPIO_InitStruct.Speed = GPIO_SPEED_FREQ_LOW;
610     HAL_GPIO_Init(GPIOK, &GPIO_InitStruct);
611
612     /*Configure GPIO pin : PJ11 */
613     //GPIO_InitStruct.Pin = GPIO_PIN_11;
614     GPIO_InitStruct.Pin = GPIO_PIN_8;
615     //OCCHIO
616     GPIO_InitStruct.Mode = GPIO_MODE_OUTPUT_PP;
617     GPIO_InitStruct.Pull = GPIO_NOPULL;
618     GPIO_InitStruct.Speed = GPIO_SPEED_FREQ_VERY_HIGH;
619     //HAL_GPIO_Init(GPIOJ, &GPIO_InitStruct);
620     HAL_GPIO_Init(GPIOA, &GPIO_InitStruct);
621
622     /*Configure GPIO pin : PJ7 */
623     GPIO_InitStruct.Pin = GPIO_PIN_7;
624     GPIO_InitStruct.Mode = GPIO_MODE_OUTPUT_OD;
625     GPIO_InitStruct.Pull = GPIO_NOPULL;
626     GPIO_InitStruct.Speed = GPIO_SPEED_FREQ_LOW;
```

```
627     HAL_GPIO_Init(GPIOJ, &GPIO_InitStruct);
628
629     /*Configure GPIO pin : PB4 (SEL1,6) */
630     GPIO_InitStruct.Pin = GPIO_PIN_4|GPIO_PIN_8;
631     GPIO_InitStruct.Mode = GPIO_MODE_OUTPUT_OD;
632     GPIO_InitStruct.Pull = GPIO_NOPULL;
633     GPIO_InitStruct.Speed = GPIO_SPEED_FREQ_LOW;
634     HAL_GPIO_Init(GPIOB, &GPIO_InitStruct);
635
636     /*Configure GPIO pin : PB15 (SEL2) */
637     GPIO_InitStruct.Pin = GPIO_PIN_15;
638     GPIO_InitStruct.Mode = GPIO_MODE_OUTPUT_OD;
639     GPIO_InitStruct.Pull = GPIO_NOPULL;
640     GPIO_InitStruct.Speed = GPIO_SPEED_FREQ_LOW;
641     HAL_GPIO_Init(GPIOB, &GPIO_InitStruct);
642
643     /*Configure GPIO pin : PB14 (SEL3) */
644     GPIO_InitStruct.Pin = GPIO_PIN_14;
645     GPIO_InitStruct.Mode = GPIO_MODE_OUTPUT_OD;
646     GPIO_InitStruct.Pull = GPIO_NOPULL;
647     GPIO_InitStruct.Speed = GPIO_SPEED_FREQ_LOW;
648     HAL_GPIO_Init(GPIOB, &GPIO_InitStruct);
649
650     /*Configure GPIO pin : PD7 (SEL4,5) */
651     GPIO_InitStruct.Pin = GPIO_PIN_7|GPIO_PIN_6;
652     GPIO_InitStruct.Mode = GPIO_MODE_OUTPUT_OD;
653     GPIO_InitStruct.Pull = GPIO_NOPULL;
654     GPIO_InitStruct.Speed = GPIO_SPEED_FREQ_LOW;
655     HAL_GPIO_Init(GPIOD, &GPIO_InitStruct);
656
657     /*Configure GPIO pin : H13 (SEL7) */
658     GPIO_InitStruct.Pin = GPIO_PIN_13;
659     GPIO_InitStruct.Mode = GPIO_MODE_OUTPUT_OD;
660     GPIO_InitStruct.Pull = GPIO_NOPULL;
661     GPIO_InitStruct.Speed = GPIO_SPEED_FREQ_LOW;
662     HAL_GPIO_Init(GPIOH, &GPIO_InitStruct);
663
664     /*Configure GPIO pin : PB6,7 (SEL8,9) */
665     GPIO_InitStruct.Pin = GPIO_PIN_7|GPIO_PIN_6;
666     GPIO_InitStruct.Mode = GPIO_MODE_INPUT;
667     GPIO_InitStruct.Pull = GPIO_NOPULL;
668     GPIO_InitStruct.Speed = GPIO_SPEED_FREQ_LOW;
669     HAL_GPIO_Init(GPIOB, &GPIO_InitStruct);
670
671     /*Configure GPIO pin : PB2 (SEL10) */
672     GPIO_InitStruct.Pin = GPIO_PIN_2;
673     GPIO_InitStruct.Mode = GPIO_MODE_OUTPUT_OD;
674     GPIO_InitStruct.Pull = GPIO_NOPULL;
675     GPIO_InitStruct.Speed = GPIO_SPEED_FREQ_LOW;
676     HAL_GPIO_Init(GPIOB, &GPIO_InitStruct);
677
678     /*Configure GPIO pin : PE2 (SEL11) */
679     GPIO_InitStruct.Pin = GPIO_PIN_2;
680     GPIO_InitStruct.Mode = GPIO_MODE_OUTPUT_OD;
681     GPIO_InitStruct.Pull = GPIO_NOPULL;
682     GPIO_InitStruct.Speed = GPIO_SPEED_FREQ_LOW;
683     HAL_GPIO_Init(GPIOE, &GPIO_InitStruct);
```

```
684
685     /*Configure GPIO pin : PA10 (SEL12) */
686     GPIO_InitStruct.Pin = GPIO_PIN_10;
687     GPIO_InitStruct.Mode = GPIO_MODE_OUTPUT_OD;
688     GPIO_InitStruct.Pull = GPIO_NOPULL;
689     GPIO_InitStruct.Speed = GPIO_SPEED_FREQ_LOW;
690     HAL_GPIO_Init(GPIOA, &GPIO_InitStruct);
691
692     /*AnalogSwitch Config */
693     HAL_SYSCFG_AnalogSwitchConfig(SYSCFG_SWITCH_PC2,
           SYSCFG_SWITCH_PC2_CLOSE);
694
695     /*AnalogSwitch Config */
696     HAL_SYSCFG_AnalogSwitchConfig(SYSCFG_SWITCH_PC3,
           SYSCFG_SWITCH_PC3_CLOSE);
697
698   }
699   /************** END MX GPIO INIT ***********/
```

After the Arduino is connected to the laptop and properly initialize, the DC board should be connected to the RF board with the prepared cables. After then, another code is to be run. This time, it is a Python code that provides a graphical interface to select the bits for SRs and mux and to select the desired supply as LDOs output. As shown in Figure 4.3, there are two LDOs on the RF board: one for V_{DD} and one for V_{DDD}, meaning the analog VCO supply and the digital one. Each LDO can provide an output from $0.8V$ to $2V$. As the latter is far too high for this test-chip, the Python code does not allow the LDO to go that far but sets a maximum voltage limit at $1.2V$. Here in the following box, the Python code is reported.

LISTING 4.2: Python code

```
1
2     import ttkbootstrap as ttk
3     from ttkbootstrap.constants import *
4     import serial
5     import serial.tools.list_ports
6     import pandas as pd
7     from tkinter import filedialog
8     from tkinter.scrolledtext import ScrolledText
9
10    # Global serial object and mapping dictionaries for the two
          shift registers
11    ser = None
12    mapping1 = {}  # Mapping for Shift Register 1
13    mapping2 = {}  # Mapping for Shift Register 2
14
15    def load_mapping(file_path):
16    """
17␣␣␣␣Load␣bit␣scrambling␣mappings␣for␣two␣shift␣registers␣from␣an␣
      Excel␣file.
18␣␣␣␣The␣Excel␣file␣must␣contain␣4␣columns:
19␣␣␣␣'SR1_Bit',␣'SR1_MappedPosition',␣'SR2_Bit',␣
      'SR2_MappedPosition'
20␣␣␣␣"""
21    try:
22    df = pd.read_excel(file_path)
```

```
23      required_columns = ['SR1_Bit', 'SR1_MappedPosition',
            'SR2_Bit', 'SR2_MappedPosition']
24      for col in required_columns:
25      if col not in df.columns:
26      raise ValueError(f"Missing␣required␣column:␣{col}")
27
28      # Drop any rows missing data in these columns
29      df.dropna(subset=required_columns, inplace=True)
30
31      # Convert the required columns to integers
32      df = df.astype({
33        'SR1_Bit': 'int',
34        'SR1_MappedPosition': 'int',
35        'SR2_Bit': 'int',
36        'SR2_MappedPosition': 'int'
37      })
38
39      map1 = {}
40      map2 = {}
41      for _, row in df.iterrows():
42      sr1_bit = row['SR1_Bit']
43      sr1_mapped = row['SR1_MappedPosition']
44      sr2_bit = row['SR2_Bit']
45      sr2_mapped = row['SR2_MappedPosition']
46
47      # Validate that the bit numbers and mapped positions are
            within 0-31
48      if not (0 <= sr1_bit < 32 and 0 <= sr1_mapped < 32):
49      raise ValueError(f"Invalid␣SR1␣mapping:␣Bit␣{sr1_bit}␣->␣
            {sr1_mapped}.␣Must␣be␣in␣0-31.")
50      if not (0 <= sr2_bit < 32 and 0 <= sr2_mapped < 32):
51      raise ValueError(f"Invalid␣SR2␣mapping:␣Bit␣{sr2_bit}␣->␣
            {sr2_mapped}.␣Must␣be␣in␣0-31.")
52
53      map1[sr1_bit] = sr1_mapped
54      map2[sr2_bit] = sr2_mapped
55
56      return map1, map2
57
58      except Exception as e:
59      ttk.messagebox.showerror("Excel␣Error", f"Error␣loading␣
            mapping:␣{e}")
60      return {}, {}
61
62      def scramble_bits(bits, mapping):
63      """
64  ␣␣␣␣Rearrange␣bits␣based␣on␣the␣provided␣mapping.
65  ␣␣␣␣'bits'␣is␣a␣list␣of␣32␣values␣(0␣or␣1)␣and␣'mapping'␣is␣a␣
        dictionary␣mapping␣original
66  ␣␣␣␣bit␣positions␣to␣new␣positions.
67  ␣␣␣␣"""
68      scrambled = [0] * len(bits)
69      for i, bit in enumerate(bits):
70      target_index = mapping.get(i, i)  # if no mapping is provided
            for a bit, keep it in place
71      if target_index < 0 or target_index >= len(scrambled):
```

```
72      raise IndexError(f"Target␣index␣{target_index}␣for␣bit␣{i}␣is␣
            out␣of␣range.")
73      scrambled[target_index] = bit
74      return scrambled
75
76      def send_data(register):
77      """
78  ␣␣␣␣Send␣bit␣data␣for␣the␣specified␣register␣(1␣or␣2)␣to␣the␣
        serial␣port.
79  ␣␣␣␣Each␣register␣is␣represented␣by␣32␣bits.
80  ␣␣␣␣"""
81      if register == 1:
82      bits = [var.get() for var in checkbox_vars1]
83      cmd = "WRITE1"
84      current_mapping = mapping1
85      elif register == 2:
86      bits = [var.get() for var in checkbox_vars2]
87      cmd = "WRITE2"
88      current_mapping = mapping2
89      else:
90      return
91
92      if len(bits) != 32:
93      ttk.messagebox.showerror("Data␣Error", "Each␣register␣must␣
            have␣exactly␣32␣bits.")
94      return
95
96      scrambled = scramble_bits(bits, current_mapping) if
            current_mapping else bits
97      value = sum(bit << (31 - i) for i, bit in enumerate(scrambled))
98
99      if ser and ser.is_open:
100     try:
101     ser.write((cmd + "\n").encode())
102     ser.write(value.to_bytes(4, byteorder='big'))
103     except Exception as e:
104     ttk.messagebox.showerror("Serial␣Error", f"Failed␣to␣send␣data␣
            for␣{cmd}:␣{e}")
105     else:
106     ttk.messagebox.showerror("Serial␣Error", "Serial␣port␣not␣
            connected.")
107
108     def choose_file():
109     """Select␣and␣load␣an␣Excel␣mapping␣file␣for␣both␣shift␣
            registers."""
110     file_path = filedialog.askopenfilename(
111     title="Select␣Excel␣Mapping␣File",
112     filetypes=[("Excel␣files", "*.xlsx␣*.xls")]
113     )
114     if file_path:
115     global mapping1, mapping2
116     mapping1, mapping2 = load_mapping(file_path)
117     if mapping1 and mapping2:
118     status_label.config(text="Mapping␣loaded␣successfully.")
119     else:
120     status_label.config(text="Failed␣to␣load␣mapping.")
121
```

```
122     def connect_serial():
123     """Connect␣to␣the␣selected␣serial␣port."""
124     global ser
125     port = port_combo.get()
126     baud = baud_entry.get()
127     try:
128     ser = serial.Serial(port, int(baud), timeout=1)
129     connection_status.config(text="Connected", bootstyle="success")
130     except Exception as e:
131     ttk.messagebox.showerror("Serial␣Error", f"Error␣opening␣
            serial␣port:␣{e}")
132     connection_status.config(text="Not␣connected",
            bootstyle="danger")
133
134     def send_command(cmd):
135     """Send␣a␣command␣string␣to␣the␣serial␣port."""
136     if ser and ser.is_open:
137     try:
138     ser.write((cmd + "\n").encode())
139     except Exception as e:
140     ttk.messagebox.showerror("Serial␣Error", f"Failed␣to␣send␣
            {cmd}:␣{e}")
141     else:
142     ttk.messagebox.showerror("Serial␣Error", "Serial␣port␣not␣
            connected.")
143
144     # --- Build the GUI ---
145     root = ttk.Window(themename="superhero")
146     root.title("Arduino␣Control␣GUI")
147     root.geometry("600x800")  # Increased height to accommodate
            the serial output box
148
149     # Serial Port Selection Frame
150     serial_frame = ttk.Frame(root, padding=10)
151     serial_frame.pack(pady=10, fill='x')
152
153     ports = [p.device for p in serial.tools.list_ports.comports()]
154     port_combo = ttk.Combobox(serial_frame, values=ports,
            state="readonly")
155     port_combo.grid(row=0, column=1, padx=5)
156     if ports:
157     port_combo.current(0)
158     else:
159     port_combo.set("No␣ports␣found")
160
161     ttk.Label(serial_frame, text="Serial␣Port:").grid(row=0,
            column=0, padx=5)
162     ttk.Label(serial_frame, text="Baud␣Rate:").grid(row=0,
            column=2, padx=5)
163
164     baud_entry = ttk.Entry(serial_frame, width=10)
165     baud_entry.insert(0, "115200")
166     baud_entry.grid(row=0, column=3, padx=5)
167
168     connect_button = ttk.Button(serial_frame, text="Connect",
            command=connect_serial, bootstyle="primary")
169     connect_button.grid(row=0, column=4, padx=5)
```

```
170
171     connection_status = ttk.Label(serial_frame, text="Not␣
            connected", bootstyle="danger")
172     connection_status.grid(row=0, column=5, padx=5)
173
174     # Command Buttons
175     cmd_frame = ttk.Frame(root, padding=10)
176     cmd_frame.pack(pady=10)
177
178     commands = ["STROBE1", "RESET1", "STROBE2", "RESET2"]
179     for i, cmd in enumerate(commands):
180     ttk.Button(cmd_frame, text=cmd, command=lambda c=cmd:
            send_command(c), bootstyle="success-outline")\
181     .grid(row=i // 2, column=i % 2, padx=5, pady=5, sticky="ew")
182
183     # Registers UI: two separate groups for the two shift registers
184     def create_register_ui(title, var_list, send_func):
185     reg_frame = ttk.Labelframe(root, text=title, padding=10)
186     reg_frame.pack(pady=10)
187
188     for i in range(32):
189     cb = ttk.Checkbutton(reg_frame, text=f"{i}",
            variable=var_list[i], bootstyle="round-toggle")
190     cb.grid(row=i // 8, column=i % 8, padx=2, pady=2)
191
192     ttk.Button(reg_frame, text="Send", command=send_func,
            bootstyle="primary")\
193     .grid(row=5, column=0, columnspan=8, pady=5)
194
195     checkbox_vars1 = [ttk.IntVar() for _ in range(32)]
196     checkbox_vars2 = [ttk.IntVar() for _ in range(32)]
197     create_register_ui("Shift␣Register␣1␣(WRITE1)",
            checkbox_vars1, lambda: send_data(1))
198     create_register_ui("Shift␣Register␣2␣(WRITE2)",
            checkbox_vars2, lambda: send_data(2))
199
200     def toggle_pin(pin, var):
201     """Invia␣il␣comando␣per␣attivare␣o␣disattivare␣un␣pin␣
            specifico."""
202     if ser and ser.is_open:
203     try:
204     state = var.get()
205     cmd = f"PIN{pin}_{'ON'␣if␣state␣else␣'OFF'}"
206     ser.write((cmd + "\n").encode())
207     except Exception as e:
208     ttk.messagebox.showerror("Serial␣Error", f"Failed␣to␣send␣
            {cmd}:␣{e}")
209     else:
210     ttk.messagebox.showerror("Serial␣Error", "Serial␣port␣not␣
            connected.")
211
212     # UI per il controllo dei pin
213     pin_control_frame = ttk.Labelframe(root, text="Pin␣Control",
            padding=10)
214     pin_control_frame.pack(pady=10, fill='x')
215
216     pin_vars = [ttk.IntVar() for _ in range(13)]
```

```
217
218     for i in range(1,13):
219     pin_button = ttk.Checkbutton(
220     pin_control_frame, text=f"Pin␣{i}", variable=pin_vars[i],
221     command=lambda p=i, v=pin_vars[i]: toggle_pin(p, v),
            bootstyle="round-toggle"
222     )
223     pin_button.grid(row=i // 6, column=i % 6, padx=5, pady=5)
224
225     # Mapping Load Button
226     load_mapping_button = ttk.Button(root, text="Load␣Excel␣
            Mapping", command=choose_file, bootstyle="info")
227     load_mapping_button.pack(pady=5)
228     status_label = ttk.Label(root, text="No␣mapping␣loaded.")
229     status_label.pack(pady=5)
230
231     # --- Serial Incoming Messages Box ---
232     output_frame = ttk.Frame(root, padding=10)
233     output_frame.pack(side="bottom", fill="both", expand=True)
234     serial_output = ScrolledText(output_frame, height=10,
            state="disabled", wrap="word")
235     serial_output.pack(fill="both", expand=True)
236
237
238
239     def poll_serial():
240     """Periodically␣poll␣the␣serial␣port␣for␣incoming␣messages␣and␣
            display␣them."""
241     global ser
242     if ser and ser.is_open:
243     try:
244     bytes_waiting = ser.in_waiting
245     if bytes_waiting:
246     incoming = ser.read(bytes_waiting).decode('utf-8',
            errors='replace')
247     serial_output.configure(state="normal")
248     serial_output.insert("end", incoming)
249     serial_output.see("end")
250     serial_output.configure(state="disabled")
251     except Exception as e:
252     print(f"Error␣reading␣from␣serial:␣{e}")
253     root.after(100, poll_serial)
254
255     poll_serial()
256     root.mainloop()
```

The RF board is meant to be small and portable, easy to insert on top of the bonding machine and the probe station, but big enough not to cause unbalances when probe descend. RF board should be done for each topology of test-chip in order to select the most suitable LDOs and filtering. On the other hand, the DC board just features the Arduino controller and some connector, hence it is convenient to connect to many kinds of RF boards and it can be used for different types of measurement. In this work, only few connectors were soldered, in particular the USB connector linking the external supply -in this case the laptop- to the DC board and the connectors from the DC to the RF board. But, in general, other connectors were included -and left unsoldered- to grant a wider variety of uses for this board.

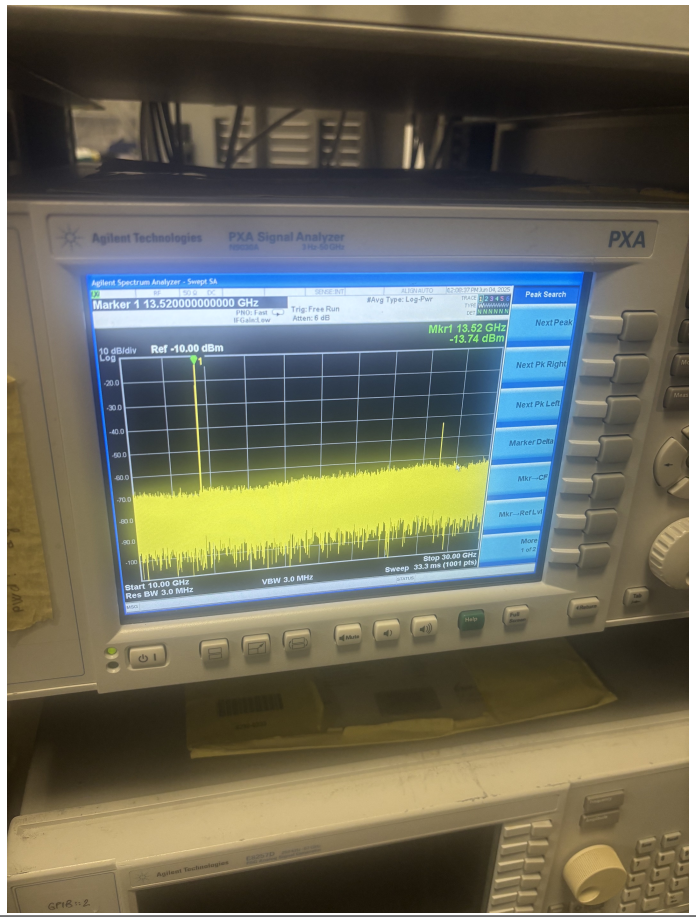

FIGURE 4.9: Proposed architecture spectrum measurement.

4.2 Measurement Results

All the previously illustrated calculations and Cadence simulations have been verified through a test-chip in 12nm FinFET shown in Figure 4.1. Testing has been carried out by controlling the voltage supply and the switched capacitors code through Arduino then probing the results and analyzing the subsequent PN with a N9030A Keysight Spectrum Analyzer. The chip occupies an area of $0.21mm^2$, with the inductor being 102um x 108um and the longest t-line, i.e. d_1, 718um x 70um.

The proposed topology oscillates from 24.8GHz to 27.2GHz and dissipates from 7.20 to 10.4mW from a 0.8V supply. A typical spectrum is shown in Figure 4.9. Compared to the expected threshold start-up, 0.5V, and the expected optimal VCO supply, 0.75V, the values obtained from measurements are respectively 0.6V and 0.8V. Even though 0.8V is the optimal supply, the chip can correctly operate from 0.6V, the start-up point, to 1.2V, i.e, the technology limit. Being a voltage-controlled oscillator, the structure requires a very clean supply due to its sensitiveness.

Figure 4.10 depicts PN measurement by sweeping the VCO supply within an advisable operating range (from 0.8 to 1V); in particular maximum, minimum and central frequency are highlighted. Figure 4.11 shows PN measurement at 0.8V from 13.5GHz, i.e., oscillating frequency of 27GHz divided by 2, achieving $-127.15dBc/Hz$ at 10MHz offset.

Compared to the target, i.e., PN(10MHz) = -124dBc/Hz at 27GHz, the outcome seems satisfying, but take into account that the number of PN(10MHz) = -124.15 dBc/Hz at 27GHz is not the actual performance as it is affected by the LDO. Given an integrated

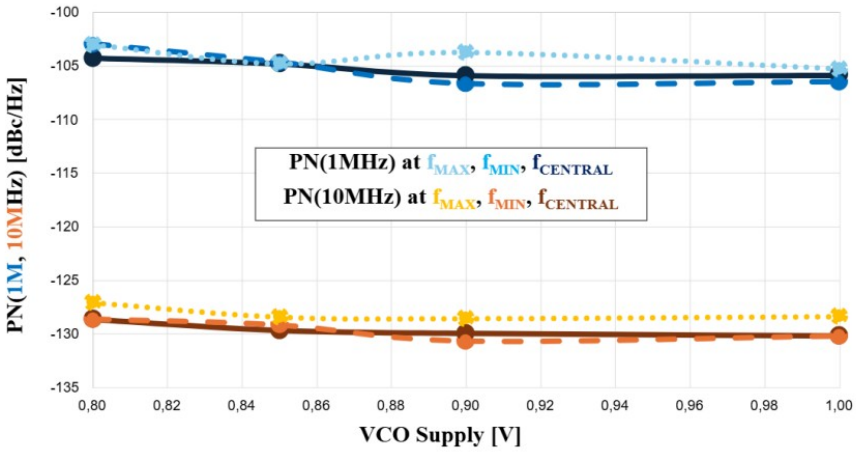

FIGURE 4.10: Measured PN for different VCO supplies.

LDO, the results would have matched the simulations, as shown in the pink line in Figure 4.11.

Through the test-chip, the stability of Phase mode has been verified even in presence of strong mismatches (Figure 4.13) , due to the fact that $d_1 << \lambda_P$. Slight (Figure 4.12) to more pronounced (Figure 4.13) mismatches have been applied through Arduino code, without changing the oscillation modes.

In particular, these tests were possible due to the fact there were 3 kind of custom MOM switched capacitors: fine, small and big.Figure 4.12 is obtained by only touching fine capacitor arrays; the single fine capacitance value is approximately 2fF. On the other hand, Figure 4.13 was obtained by touching the biggest capacitors.

Overall, the test-chip achieved a good performance -evaluated through FoM_D for a fair comparison- despite some major drawbacks such as the absence of an extra-thick metal layer, the intertwined tail inductor and the presence of a bulky external LDO. For the State of the Art Comparison the following table may be considered.

In particular, the external LDO contributed a significant PN worsening (Figure 4.11) due to the huge supply-sensitivity of this structure. A simple way to definitely solve such issues would have been to implement a current-controlled oscillator in each core and to put an on-chip LDO. Acceptable output noise depends on $\frac{outnoise*\Delta f}{2\pi V_{out,peak} K_{VCO}}$. Thus, from this formula an acceptable noise at various frequency may be obtained and then compared with the LDO output noise. A similar approach may be adopted when it comes to the output stage, i.e. buffer, multiplexer and divider. Another improvement would have been a different tail, for example another 8-shaped inductor to prevent couplings between the main and the intertwined inductors. The drawback of such a solution is the great layout complexity.

FoM_D is a complete figure of merit taking into account both the oscillator and the distribution network, which allegedly consumes the same power as the VCO. The proposed solution has good PN, low power and no mode ambiguity without adding an external forcing element or fixing the t-line lengths. This represents a breakthrough with respect to previous designs [80], [20], where d should be exactly $\frac{\lambda}{4}$. Despite some layout-related issues and the external LDOs, the overall performance is good. Note that the limited TR was a specification for this application. In general TR may be enlarged, but it will always be limited by C_L, therefore a careful sizing of d_1, d_2 will be required.

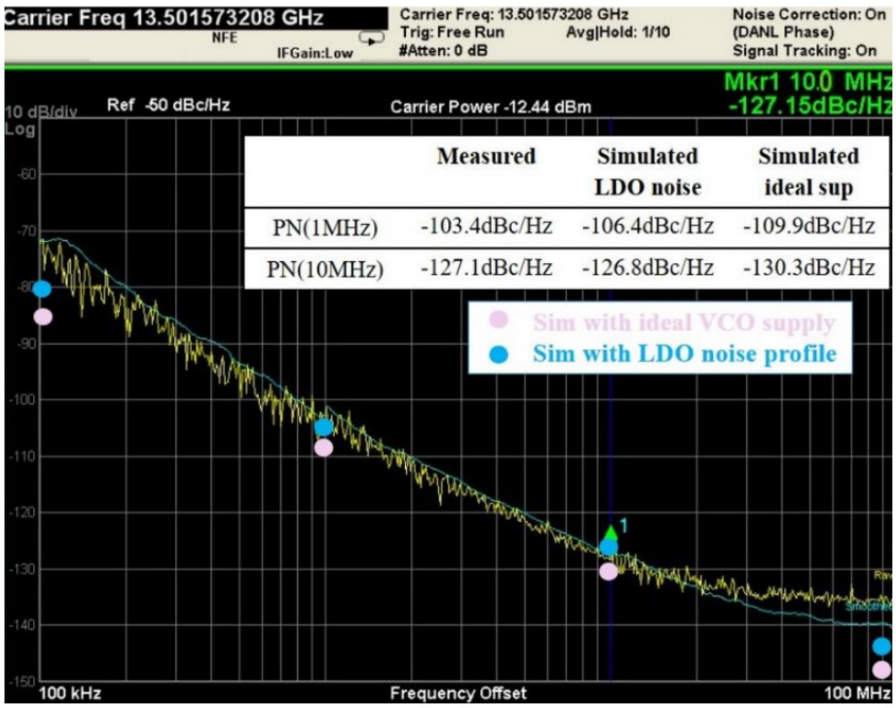

FIGURE 4.11: Measured PN compared with simulations.

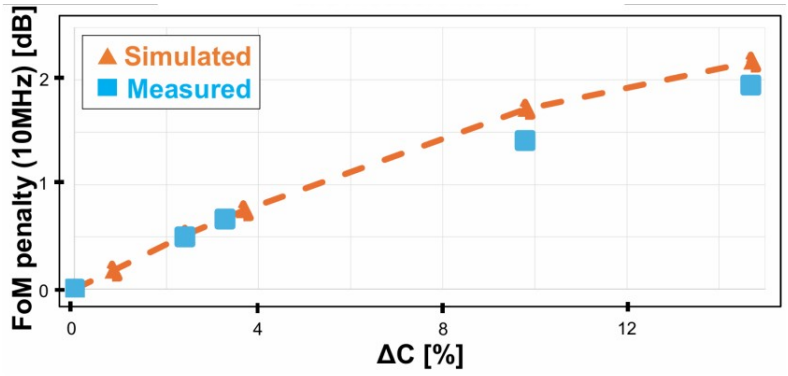

FIGURE 4.12: FoM(10MHz) degradation due to added small capacitive mismatch.

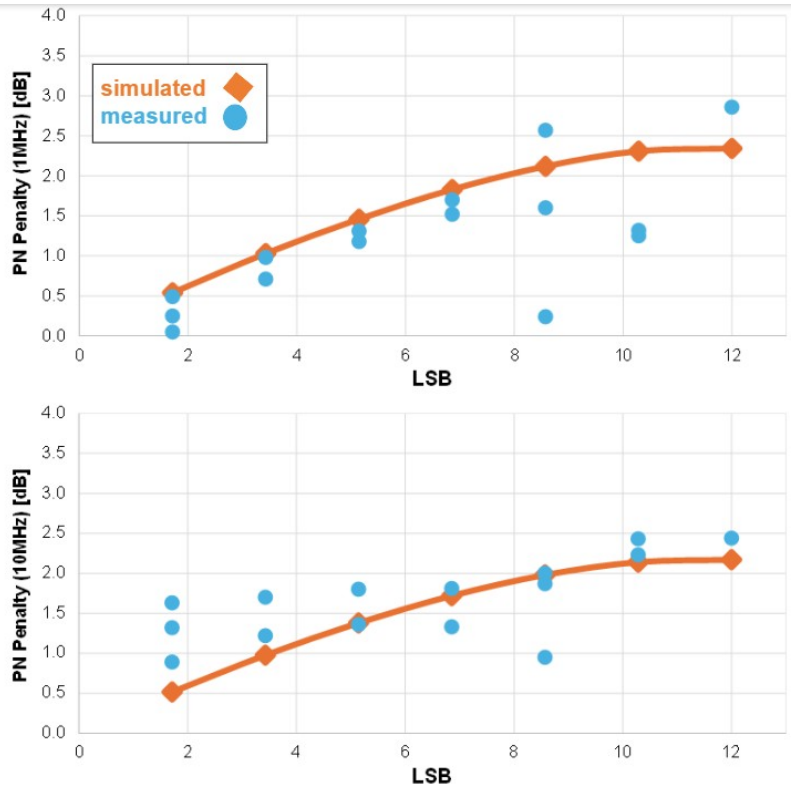

FIGURE 4.13: FoM(10MHz) degradation due to added big capacitive mismatch.

TABLE 4.1: State of the Art Comparison

	This Work	[80]	[39]	[101]	[36]
freq [GHz]	24.80	54.20	25	5.69**	23.60
TR [%]	9.23	8.49	26.07	31.80	6.57**
Supply [V]	0.80	1.00	0.95	0.73	1.80
Power [mW]	7.20	144.00	16.06	8.03**	70.20
PN(1MHz) [dBc/Hz]	-98.31	-85**	-110	-115.05**	-105.22
PN(10MHz) [dBc/Hz]	-122.67	-131	-130**	-130.05**	-112**
# Cores	4	4	4	1	4
Topology	SW Class B + Tail	HWO	Class B	Class B+Tail	RTW
Process	12nm	65nm	40nm	28nm	0.18μm
Core Area [mm^2]	0.21	0.055	0.1	0.033	0.36
FoM(1MHz) [dB]	/	/	186	181	/
FoM(10MHz) [dB]	/	/	187	185**	/
FoM$_D$(1MHz) [dB]	178	181	183*	178*	174
FoM$_D$(10MHz) [dB]	182	184	184*	182*	164

FoM_D = FoM with clock distribution included.
$*$ FoM reduced by 3 dB for clock distribution; $**$ calculated from the paper.

Chapter 5

Conclusions

To sum up, the target for the proposed work was a robust and fast CO for SerDes (Serializer-Deserializer) transceivers, the structures responsible for implementing the wire enabling people to connect, store and access data. Recently, the advent of 5G and Internet of Things (IoT) made VCO requirements even more stringent, especially as the clock eats about half the total power consumption in VLSI chips, thus it is fundamental to optimize the clock signal generation and distribution. In this thesis, clock distribution becomes a huge design aspect for large chips, whose lengths span from 1 mm to 10 mm. Distribution usually requires half the power consumption and adds up noise as well, thus the focus of this work is to optimize the clock management through a distributed oscillator architecture. The traditional trade-off power-phase noise (PN) is examined and a new solution is proposed through in-phase coupling [1].

To realize such a performing architecture, the proposal was to realize four VCO cores coupled through SW transmission lines operating at Phase oscillating mode. An analysis for operating mode, stability and FoM penalty was presented and then validated thanks to the measurement of the test-chip, which was described in the previous chapters. Now, the state of the art comparison will be presented and the results will be evaluated through both the traditional Figure of Merit (FoM) and a new distributed FoM, called FoM_D, was developed to guarantee a fair comparison. As described before, the FoM_D accounts for the 3dB cost of distributing the clock signal in terms of power; note that the further dB due to the PN cost were not added as they would be more difficult to estimate. The table below reports the state of the art comparison.

As highlighted in the state of the art comparison table, presented in the fourth chapter, the specifications for frequency, TR, power and PN were met. Considering that the comparison is not completely fair as the PN contribution for some distribution network is still missing and that the test-chip measurements were impaired by the external LDO, the results appear promising. Despite the noise introduced by the off-chip regulator and the limitations of the metal stack used in this design, which has no ultra-thick metal, the achieved performance is close to the State of the Art for both distributed and lumped oscillator arrays.

In conclusion, this thesis presents a multi-core distributed Phase Coupled oscillator with no mode ambiguity. The stability calculations have been shown and proved through a test-chip in 12nm FinFET technology. The main strength of the proposed approach consists in its scalability united with its simplicity: if designed within the given limit, the distributed VCO guarantees stability and good performance even for long lengths such as few millimeters.

In order to combine advantages from SW and stand-alone oscillators, in this work a hybrid structure with multiple stand-alone cores (Gm with their tank) coupled through standing wave transmission lines [81] was proposed. The goal is to achieve the stand-alone PN performance without additional power for clock distribution. This strategy

relieves the Q mitigation due to t-lines and grants a simple, robust and relatively low-area solution.

The proposed architecture features a Phase mode quad-core VCO. As P mode is the target, each oscillator should see the same load: the four cores should compensate each other, meaning that Phase region is enforced if a symmetrical system is built, with each VCO seeing about half of the t-line connecting it to the other cores. In particular, with the selected sizing for the t-lines, the P mode is favoured until $0.25\lambda_P - 0.25\lambda_{CP}$, which represents the practical limit for our optimized architecture.

Regarding longer t-lines, CP is empirically dominating until λ_{CP} but it is advisable to only use it until $\frac{\lambda_{CP}}{2}$.

When dealing with future works, it would be proper to mention the study of CP t-lines for longer connections at even lower power, even at the cost of a PN performance worsening. Another promising project is a hybrid architecture featuring a switch in the middle of the transmission line, enabling the structure to shift from a P mode operation to a CP mode oscillation by changing the load seen from each core. This would present multiple advantage and would also solve the intrinsic limitation of TR due to the heavy contribution of parasitic capacitances.

Regarding future works focused on the proposed test-chip optimization, the main two tasks to be accomplished are the design of an on-chip integrated LDO allowing proper PN measurement and the porting of the same design in another technology with extra-thick metals. If the first is motivated by the need for PN improvement, the second suggestion is to guarantee a fair comparison and to better evaluate the proposed topology.

In the end, a robust and competitively performing 1.9 mm clock generation and distribution network was designed, analysed and tested in a FinFET test-chip. Future works include improvements in measurements by implementing more sophisticated output chains -for instance including new LDOs- and by performing more exhaustive measurements for high temperatures or prolonged stress.

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List of Abbreviations

ADC	**A**nalog-to-**D**igital **C**onverter
AR	**A**ugmented **R**eality
A/D	**A**nalog to **D**igital
BCD	**B**ipolar **C**MOS **D**MOS
BJT	**B**ipolar **J**unction **T**ransistor
BW	**B**and**W**idth
CDAC	**C**apacitive **D**igital-to-**A**nalog **C**onverter
CK	**C**loc**K**
CMOS	**C**omplementary **M**etal-**O**xide-**S**emiconductor
CTAT	**C**omplementary-**T**o-**A**bsolute-**T**emperature
DAC	**D**igital-to-**A**nalog **C**onverter
DFT	**D**esign **F**or **T**estability
DRC	**D**esign **R**ule **C**hecking
DSP	**D**igital **S**ignal **P**rocessing
DR	**D**ynamic **R**ange
DUT	**D**evice **U**nder **T**est
EMC	**E**lectro-**M**agnetic **C**ompatibility
ENOB	**E**ffective **N**umber **O**f **B**its
FIR	**F**inite **I**mpulse **R**esponse
FF	**F**eed-**F**orward
FFT	**F**ast **F**ourier **T**ransform
FoM	**F**igure **o**f **M**erit
FS	**F**ull-**S**cale
GBW	**G**ain **B**and**W**idth product
IC	**I**ntegrated **C**ircuit
IIR	**I**nfinite **I**mpulse **R**esponse
INL	**I**ntegral **N**on**L**inearity
I/O	**I**nput/**O**utput
IoT	**I**nternet **o**f **T**hings
LF	**L**oop-**F**ilter
LDE	**L**ayout **D**ependent **E**ffect
LDO	**L**ow **D**rop **O**ut
LSB	**L**east **S**ignificant **B**it
LVS	**L**ayout **V**ersus **S**chematic
MOSFET	**M**etal-**O**xide-**S**emiconductor **F**ield-**E**ffect **T**ransistor
MSB	**M**ost **S**ignificant **B**it
NS	**N**oise **S**haping
NTF	**N**oise **T**ransfer **F**unction
OSR	**O**ver**S**ampling **R**atio
PA	**P**re**A**mplifier
PCB	**P**rinted **C**ircuit **B**oard
PSD	**P**ower **S**pectral **D**ensity

PSRR	**P**ower **S**upply **R**ejection **R**atio
PTAT	**P**roportional-**T**o-**A**bsolute-**T**emperature
PVT	**P**rocess **V**oltage **T**emperature
RA	**R**esidue **A**mplifier
REF	**REF**erence
RFID	**R**adio-**F**requency **ID**entification
RMS	**R**oot **M**ean **S**quare
SAR	**S**uccessive **A**pproximation **R**egister
SFF	**S**ingle **F**requency **F**iltering
SMD	**S**urface **M**ounted **D**evice
SNDR	**S**ignal to **N**oise and **D**istortion **R**atio
SNR	**S**ignal to **N**oise **R**atio
SQNR	**S**ignal to **Q**uantization-**N**oise **R**atio
SotA	**S**tate **O**f **T**he **A**rt
STF	**S**ignal **T**ransfer **F**unction
S/H	**S**ample and **H**old
THD	**T**otal **H**armonic **D**istortion
THD+N	**T**otal **H**armonic **D**istortion + **N**oise
THT	**T**hrough **H**ole **T**echnology
ZCR	**Z**ero **C**rossing **R**ate

Bibliography

[1] B. Casper and F. O'Mahony, "Clocking Analysis, Implementation and Measurement Techniques for High-Speed Data Links—A Tutorial," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 56, no. 1, pp. 17-39, Jan. 2009, doi: 10.1109/TCSI.2008.931647.

[2] Dake Liu and Svensson, C., "Power consumption estimation in CMOS VLSI chips", in IEEE Journal of Solid-State Circuits, vol. 29, no. 6, pp. 663-670, 1994, doi: 10.1109/4.293111.

[3] A. K. A., Seoud et. al., "Analog IC design of high-speed serial link transceiver for 10 GbaseKR standard using a 65 nm CMOS process".

[4] C. Nani *et al.*, "A 5-nm 60-GS/s 7b 64-Way Time Interleaved Partial Loop Unrolled SAR ADC Achieving 35.2dB SNDR up to 32 GHz," in IEEE Journal of Solid-State Circuits, vol. 60, no. 4, pp. 1210-1222, April 2025, doi: 10.1109/JSSC.2024.3517333.

[5] T. Chan Carusone, T. O. Dickson, S. Palermo, S. Shekhar and M. Mansuri, "Modern Wireline Transceivers," in IEEE Journal of Solid-State Circuits, vol. 61, no. 2, pp. 395-422, Feb. 2026, doi: 10.1109/JSSC.2025.3642231.

[6] M. Tambussi et al., "A Quasi-Passive 78-dB DR 14.9- µW Noise-Shaping SAR A/D Converter for Audio Activity Detection Applications," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 72, no. 12, pp. 1852-1856, Dec. 2025, doi: 10.1109/TCSII.2025.3590625.

[7] J. A. Fredenburg et al., "A 90-MS/s 11-MHz-Bandwidth 62-dB SNDR Noise-Shaping SAR ADC," IEEE Journal of Solid-State Circuits, vol. 47, no. 12, pp. 2898–2904, 2012.

[8] P. Schvan et al., "A 24GS/s 6b ADC in 90nm CMOS," in Proc. IEEE Int. Solid-State Circuits Conf.-Dig. Tech. Papers, San Francisco, CA, USA, Feb. 2008, pp. 544–634.

[9] V. Marazzi, "Analysis of a dynamic bias low power comparator in 5nm Finfet technology", 2022.

[10] Ahmed, Abdelrahman H. and Moznine, Abdellatif El and Lim, Daihyun and Ma, Yangjin and Rylyakov, Alexander and Shekhar, Sudip, "A Dual-Polarization Silicon-Photonic Coherent Transmitter Supporting 552 Gb/s/wavelength", in IEEE Journal of Solid-State Circuits, vol. 55, no. 9, pp. 2597-2608, 2020, doi: 10.1109/JSSC.2020.2988399.

[11] A. Ghilioni, U. Decanis, E. Monaco, A. Mazzanti and F. Svelto, "A 6.5mW inductorless CMOS frequency divider-by-4 operating up to 70GHz," 2011 IEEE International Solid-State Circuits Conference, San Francisco, CA, USA, 2011, pp. 282-284, doi: 10.1109/ISSCC.2011.5746319.

[12] H. Razavi and B. Razavi, "A 27-73 GHz Injection-Locked Frequency Divider," 2021 Symposium on VLSI Circuits, Kyoto, Japan, 2021, pp. 1-2, doi: 10.23919/VLSICircuits52068.2021.9492457.

[13] M. Garampazzi et al., ”An Intuitive Analysis of Phase Noise Fundamen tal Limits Suitable for Benchmarking LC Oscillators,” in IEEE Journal of Solid-State Circuits, vol. 49, no. 3, pp. 635-645, March 2014, doi: 10.1109/JSSC.2014.2301760.

[14] M. Garampazzi, P. Mendes, N. Codega, D. Manstretta and R. Castello, "A 195.6dBc/Hz peak FoM P-N class-B oscillator with transformer-based tail filtering," ESSCIRC 2014 - 40th European Solid State Circuits Conference (ESSCIRC), Venice Lido, Italy, 2014, pp. 331-334, doi: 10.1109/ESSCIRC.2014.6942089.

[15] Y. Zhao, M. Forghani and B. Razavi, "A 20-GHz PLL With 20.9-fs Random Jitter," in IEEE Journal of Solid-State Circuits, vol. 58, no. 6, pp. 1597-1609, June 2023, doi: 10.1109/JSSC.2022.3225105.

[16] Y. Zhao, O. Memioglu, L. Kong and B. Razavi, "A 56-GHz Fractional-N PLL With 110-fs Jitter," in IEEE Journal of Solid-State Circuits, vol. 58, no. 1, pp. 57-67, Jan. 2023, doi: 10.1109/JSSC.2022.3220547.

[17] B. Razavi, Phase-Locking in High-Performance Systems: From De vices to Architectures. Hoboken, NJ: Wiley, 2003.

[18] D. Pfaff et al., "A 224 Gb/s 3 pJ/bit 40 dB Insertion Loss Transceiver in 3-nm FinFET CMOS," in IEEE Journal of Solid-State Circuits, vol. 60, no. 1, pp. 9-22, Jan. 2025, doi: 10.1109/JSSC.2024.3466092.

[19] Z. Bai, X. Zhou, R. D. Mason and G. Allan, "Low-Phase Noise Clock Distribution Network Using Rotary Traveling-Wave Oscillators and Built-In Self-Test Phase Tuning Technique," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 62, no. 1, pp. 41-45, Jan. 2015, doi: 10.1109/TCSII.2014.2362743.

[20] W. F. Andress and D. Ham, "Standing wave oscillators utilizing wave-adaptive tapered transmission lines," in IEEE Journal of Solid-State Circuits, vol. 40, no. 3, pp. 638-651, March 2005, doi: 10.1109/JSSC.2005.843600.

[21] Y. -T. Yang, H. -C. Hong and K. -H. Cheng, "A Reference-less All-digital BPSK-based Clock and Data Recovery Circuitry for Die-to-Die Interfaces," 2025 IEEE International Symposium on Circuits and Systems (ISCAS), London, United Kingdom, 2025, pp. 1-5, doi: 10.1109/ISCAS56072.2025.11043885.

[22] Ming-ta Hsieh and G. E. Sobelman, "Clock and data recovery with adaptive loop gain for spread spectrum SerDes applications," 2005 IEEE International Symposium on Circuits and Systems (ISCAS), Kobe, Japan, 2005, pp. 4883-4886 Vol. 5, doi: 10.1109/ISCAS.2005.1465727.

[23] Z. Shang, X. Chen, H. Huan, X. Quan, J. Zhan and S. Zhang, "A Cyclostationarity-Based Method for Time Interval Error Extraction Without Clock Recovery in SerDes Links," in IEEE Transactions on Instrumentation and Measurement, vol. 74, pp. 1-8, 2025, Art no. 5505708, doi: 10.1109/TIM.2025.3575976.

[24] M. Pisati et al., "A 243-mW 1.25–56-Gb/s Continuous Range PAM-4 42.5-dB IL ADC/DAC-Based Transceiver in 7-nm FinFET," in IEEE Journal of Solid-State Circuits, vol. 55, no. 1, pp. 6-18, Jan. 2020, doi: 10.1109/JSSC.2019.2936307.

[25] R. Ho, K. Mai, and M. Horowitz, “The future of wires,” Proc. IEEE, no. 4, pp. 490–504, Apr. 2001.

[26] Z. Kang, M. Yang and L. Wu, "A 5-mW 30-GHz Quasi-Rotary Traveling-Wave Oscillator With Extrinsic-Q-Enhanced Transmission Line," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 70, no. 10, pp. 3867-3878, Oct. 2023, doi: 10.1109/TCSI.2023.3303457.

[27] Y. Xu and S. Chen, "PPTWO: Push-Pull cell based Traveling Wave Oscillator," 2010 IEEE Asia Pacific Conference on Circuits and Systems, Kuala Lumpur, Malaysia, 2010, pp. 644-647, doi: 10.1109/APCCAS.2010.5774835.

[28] G. Balamurugan et al., "A Scalable 5–15 Gbps, 14–75 mW Low-Power I/O Transceiver in 65 nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 43, no. 4, pp. 1010-1019, April 2008, doi: 10.1109/JSSC.2008.917522.

[29] M. Kossel et al., "LC PLL With 1.2-Octave Locking Range Based on Mutual-Inductance Switching in 45-nm SOI CMOS," in IEEE Journal of Solid-State Circuits, vol. 44, no. 2, pp. 436-449, Feb. 2009, doi: 10.1109/JSSC.2008.2011041.

[30] M. A. Shehata, M. Keaveney and R. B. Staszewski, "A 184.6-dBc/Hz FoM 100-kHz Flicker Phase Noise Corner 30-GHz Rotary Traveling-Wave Oscillator Using Distributed Stubs in 22-nm FD-SOI," ESSCIRC 2019 - IEEE 45th European Solid State Circuits Conference (ESSCIRC), Cracow, Poland, 2019, pp. 103-106, doi: 10.1109/ESSCIRC.2019.8902916.

[31] J. Wood, T. C. Edwards and S. Lipa, "Rotary traveling-wave oscillator arrays: a new clock technology," in IEEE Journal of Solid-State Circuits, vol. 36, no. 11, pp. 1654-1665, Nov. 2001, doi: 10.1109/4.962285.

[32] M. A. Shehata, M. Keaveney and R. B. Staszewski, "A Distributed Stubs Technique to Mitigate Flicker Noise Upconversion in a mm-Wave Rotary Traveling-Wave Oscillator," in IEEE Journal of Solid-State Circuits, vol. 56, no. 6, pp. 1745-1760, June 2021, doi: 10.1109/JSSC.2020.3044278.

[33] W. Andress and D. Ham, "Recent developments in standing-wave oscillator design: review," 2004 IEE Radio Frequency Integrated Circuits (RFIC) Systems. Digest of Papers, Forth Worth, TX, USA, 2004, pp. 119-122, doi: 10.1109/RFIC.2004.1320545.

[34] X. Li, O. O. Yildirim, W. Zhu and D. Ham, "Phase Noise of Distributed Oscillators," in IEEE Transactions on Microwave Theory and Techniques, vol. 58, no. 8, pp. 2105-2117, Aug. 2010, doi: 10.1109/TMTT.2010.2053062.

[35] T. Brown, F. Farhabakhshian, A. Guha Roy, T. Fiez, and K. Mayaram, “A 475 mV, 4.9 GHz enhanced swing differential colpitts VCO with phase noise of-136 dBc/Hz at a 3 MHz offset frequency,” IEEE Journal of Solid-State Circuits, vol. 46, no. 8, pp. 1782–1795, 2011.

[36] Y. Y. Peng, X. P. Yu, J. M. Gu, W. M. Lim and W. Q. Sui, "An Area-Efficient CRLH (Composite Right/Left-Handed)-TL Approach to the Design of Rotary Traveling-Wave Oscillator," in IEEE Microwave and Wireless Components Letters, vol. 23, no. 10, pp. 560-562, Oct. 2013, doi: 10.1109/LMWC.2013.2252424.

[37] J. J. Rael and A. A. Abidi, "Physical processes of phase noise in differential LC oscillators," Proceedings of the IEEE 2000 Custom Integrated Circuits Conference (Cat. No.00CH37044), Orlando, FL, USA, 2000, pp. 569-572, doi: 10.1109/CICC.2000.852732.

[38] S. D. Toso et al., ”A thorough analysis of the tank quality factor in LC oscillators with switched capacitor banks,” Proceedings of 2010 IEEE International Symposium on Circuits and Systems, Paris, France, 2010, pp. 1903-1906, doi: 10.1109/ISCAS.2010.5537949.

[39] D. Murphy and H. Darabi, "A 27-GHz Quad-Core CMOS Oscillator with No Mode Ambiguity," in IEEE Journal of Solid-State Circuits, vol. 53, no. 11, pp. 3208-3216, Nov. 2018, doi: 10.1109/JSSC.2018.2865460.

[40] F. O'Mahony, M. Mansuri, B. Casper, J. Jaussi, and R. Mooney, “A low-jitter PLL andrepeaterless clock distribution network for a 20 Gb/s link,” in IEEE Symp. VLSI Circuits Dig. Tech. Papers, Jun. 2006, pp. 36–37.

[41] K. Chang, S. Pamarti, K. Kaviani, E. Alon, X. Shi, T. J. Chin, S. Jie, G. Yip, C. Madden, R. Schmitt, C. Yuan, F. Assaderaghi, and M. Horowitz, “Clocking and circuit design for a parallel IO on a first generation CELL processor,” in ISSCC 2005 Dig. Tech. Papers, pp. 526–527.

[42] S. Chan, P. Restle, T. Bucelot, S. Weitzel, J. Keaty, J. Liberty, B. Flachs, R. Volant, P. Kapusta, and J. Zimmerman, “A resonant global clock distribution for the cell broadband-engine processor,” in ISSCC 2008 Dig. Tech. Papers, pp. 512–513.

[43] L. Zhang, B. Ciftcioglu, M. Huang, and H. Wu, “Injection-locked clocking: A new GHz clock distribution scheme,” in Proc. IEEE Custom Integrated Circuits Conf., 2006, pp. 785–788.

[44] B. Razavi, "A study of injection locking and pulling in oscillators," in IEEE Journal of Solid-State Circuits, vol. 39, no. 9, pp. 1415-1424, Sept. 2004, doi: 10.1109/JSSC.2004.831608.

[45] H. Choi and S. Cho, "19.1 A 7.5GHz Subharmonic Injection-Locked Clock Multiplier with a 62.5MHz Reference, -259.7dB FoMJ, and -56.6dBc Reference Spur," 2024 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2024, pp. 348-350, doi: 10.1109/ISSCC49657.2024.10454375.

[46] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," in IEEE Journal of Solid-State Circuits, vol. 33, no. 2, pp. 179-194, Feb. 1998, doi: 10.1109/4.658619.

[47] B. Razavi, “A study of phase noise in CMOS oscillators,” IEEE J. Solid-State Circuits, vol. 31, no. 3, pp. 331–343, Mar. 1996.

[48] G. Rodrigues, R. Borralho, T. Rabuske and J. Fernandes, "Stacked Ring Oscillators with Fractional Injection Lock," 2025 IEEE International Symposium on Circuits and Systems (ISCAS), London, United Kingdom, 2025, pp. 1-5, doi: 10.1109/ISCAS56072.2025.11043468.

[49] P. C. Pereira, A. C. Pinto, L. B. Oliveira and J. R. Fernandes, "Generic Model for Multi-Phase Ring Oscillators," 2018 IEEE International Symposium on Circuits and Systems (ISCAS), Florence, Italy, 2018, pp. 1-4, doi: 10.1109/ISCAS.2018.8351777.

[50] E.Alon,J.Kim,S.Pamarti,K.Chang,andM.Horowitz,“Replicacom pensated linear regulators for supply-regulated phase-locked loops,” IEEE J. Solid-State Circuits, vol. 41, no. 2, pp. 413–424, Feb. 2006.

[51] J. Maneatis, “Low-jitter process-independent DLL and PLLbased self biased techniques,” IEEE J. Solid-State Circuits, vol. 31, no. 11, pp. 1723–1732, Nov. 1996.

[52] T. Lee, The Design of CMOS Radio-Frequency Integrated Circuits. Cambridge: Cambridge University Press, 1998, ch. 15 and 17.

[53] R. B. Staszewski, J. Wallberg, S. Rezeq, C.-M. Hung, O. Eliezer, S. Vemulapalli, C. Fernando, K. Maggio, R.Staszewski,N. Barton, M.-C. Lee, P. Cruise, M. Entezari, K. Muhammad, and D. Leipold, “All-dig ital PLL andGSM/EDGEtransmitterin90nmCMOS,”inISSCC2005 Dig. Tech. Papers, pp. 316–317.

[54] L. Vercesi, L. Fanori, F. De Bernardinis, A. Liscidini and R. Castello, "A dither-less all digital PLL for cellular transmitters," 2011 IEEE Custom Integrated Circuits Conference (CICC), San Jose, CA, USA, 2011, pp. 1-8, doi: 10.1109/CICC.2011.6055301.

[55] L. Iotti *et al.*, "Insights into Phase-Noise Scaling in Switch-Coupled Multi-Core LC VCOs for E-Band Adaptive Modulation Links," in IEEE Journal of Solid-State Circuits, vol. 52, no. 7, pp. 1703-1718, July 2017, doi: 10.1109/JSSC.2017.2697442.

[56] D. Riccardi, A. Franceschin and A. Mazzanti, "$1/f^2$ Phase Noise Analysis in Active-Coupling LC-Tank Oscillators With Frequency Mismatch," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 69, no. 2, pp. 319-323, Feb. 2022, doi: 10.1109/TCSII.2021.3094937.

[57] D. Murphy, H. Darabi and H. Wu, "Implicit Common-Mode Resonance in LC Oscillators," in IEEE Journal of Solid-State Circuits, vol. 52, no. 3, pp. 812-821, March 2017, doi: 10.1109/JSSC.2016.2642207.

[58] D. Xu et al., "A VCO With Robust Implicit Common-Mode Resonance Against Non-ideal Decoupling Network," in IEEE Solid-State Circuits Letters, vol. 7, pp. 171-174, 2024, doi: 10.1109/LSSC.2024.3399228.

[59] I. Apostolina and D. Manstretta, "A 14.5-17.9 GHz Harmonically-Coupled Quad-Core P-N Class-B DCO with -117.3 dBc/Hz Phase Noise at 1 MHz Offset in 28-nm CMOS," 2022 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Denver, CO, USA, 2022, pp. 211-214, doi: 10.1109/RFIC54546.2022.9863180.

[60] D. Manstretta and R. Castello, "An intuitive analysis of phase noise fundamental limits in LC oscillators," 2015 International Conference on Noise and Fluctuations (ICNF), Xi’an, China, 2015, pp. 1-6, doi: 10.1109/ICNF.2015.7288610.

[61] J. Yin, P. -I. Mak and R. P. Martins, "A Periodically Time-Varying Inductor Applied to The Class-D VCO for Phase Noise Improvement," ESSCIRC 2021 - IEEE 47th European Solid State Circuits Conference (ESSCIRC), Grenoble, France, 2021, pp. 307-310, doi: 10.1109/ESSCIRC53450.2021.9567840.

[62] M. K. Kazimierczuk, V. G. Krizhanovski, J. V. Rassokhina and D. V. Chernov, "Injection-locked class-E oscillator," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 53, no. 6, pp. 1214-1222, June 2006, doi: 10.1109/TCSI.2006.875176.

[63] H. An, H. Nam, S. Kim, Y. Lim and H. Yoon, "An Area-Efficient CMOS Cross-Coupled LC-VCO Using Nested Intertwined Tail Inductors," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 72, no. 1, pp. 143-147, Jan. 2025, doi: 10.1109/TCSII.2024.3485921.

[64] M. T. Amin, J. Yin, P. -I. Mak and R. P. Martins, "A 0.07 mm 2 2.2 mW 10 GHz Current-Reuse Class-B/C Hybrid VCO Achieving 196-dBc/Hz FoM A ," in IEEE Microwave and Wireless Components Letters, vol. 25, no. 7, pp. 457-459, July 2015, doi: 10.1109/LMWC.2015.2427582.

[65] S. Zhang et al., "A 49.7-fs, 10.29-to-12.75 GHz Fractional-N ADPLL with a New Quad-Core Class-F3 Oscillator," 2025 IEEE International Symposium on Circuits and Systems (ISCAS), London, United Kingdom, 2025, pp. 1-5, doi: 10.1109/ISCAS56072.2025.11044043.

[66] D. -X. Ni, L. Zhou, Z. Ren and J. Pang, "A W-Band Low-Phase-Noise Class-F23 VCO With Common-Mode Expansion Based on a Coupling-Coexisting Transformer," in IEEE Microwave and Wireless Technology Letters, vol. 35, no. 6, pp. 706-709, June 2025, doi: 10.1109/LMWT.2025.3552632.

[67] C. C. Lim, H. Ramiah, J. Yin, P. -I. Mak and R. P. Martins, "An Inverse-Class-F CMOS Oscillator With Intrinsic-High-Q First Harmonic and Second Harmonic Resonances," in IEEE Journal of Solid-State Circuits, vol. 53, no. 12, pp. 3528-3539, Dec. 2018, doi: 10.1109/JSSC.2018.2875099.

[68] A. Franceschin, D. Riccardi and A. Mazzanti, "Ultra-Low Phase Noise X-Band BiCMOS VCOs Leveraging the Series Resonance," in IEEE Journal of Solid-State Circuits, vol. 57, no. 12, pp. 3514-3526, Dec. 2022, doi: 10.1109/JSSC.2022.3202405.

[69] H. Jia, R. Ma, W. Deng, Z. Wang and B. Chi, "A 53.6-to-60.2GHz Many-Core Fundamental Oscillator With Scalable Mesh Topology Achieving -136.0dBc/Hz Phase Noise at 10MHz Offset and 190.3dBc/Hz Peak FoM in 65nm CMOS," 2022 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2022, pp. 154-156, doi: 10.1109/ISSCC42614.2022.9731581.

[70] J. Gong, B. Patra, L. Enthoven, J. van Staveren, F. Sebastiano and M. Babaie, "A 0.049mm2 7.1-to-16.8GHz Dual-Core Triple-Mode VCO Achieving 200dB FoMA in 22nm FinFET," 2022 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2022, pp. 1-3, doi: 10.1109/ISSCC42614.2022.9731752.

[71] H. Guo, Y. Chen, Y. Huang, P. -I. Mak and R. P. Martins, "8.4 An 83.3-to-104.7GHz Harmonic-Extraction VCO Incorporating Multi-Resonance, Multi-Core, and Multi-Mode (3M) Techniques Achieving -124dBc/Hz Absolute PN and 190.7dBc/Hz FoMT ," 2023 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2023, pp. 152-154, doi: 10.1109/ISSCC42615.2023.10067832.

[72] Y. Shu, Z. Deng and X. Luo, "8.3 A 28GHz Scalable Inter-Core-Shaping Multi-Core Oscillator with DM/CM-Configured Coupling Achieving 193.3dBc/Hz FoM and 205.5dBc/Hz FoMA at 1MHz Offset," 2023 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2023, pp. 150-152, doi: 10.1109/ISSCC42615.2023.10067826.

[73] Q. Wu et al., "8.1 An 11.5-to-14.3GHz 192.8dBc/Hz FoM at 1MHz Offset Dual-Core Enhanced Class-F VCO with Common-Mode-Noise Self-Cancellation and Isolation Technique," 2023 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2023, pp. 7-9, doi: 10.1109/ISSCC42615.2023.10067672.

[74] X. Zhan, J. Yin, P. -I. Mak and R. P. Martins, "8.2 A 22.4-to-26.8GHz Dual-Path-Synchronized Quad-Core Oscillator Achieving -138dBc/Hz PN and 193.3dBc/Hz

FoM at 10MHz Offset from 25.8GHz," 2023 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2023, pp. 148-150, doi: 10.1109/ISSCC42615.2023.10067277.

[75] Z. Kang, C. Yu and L. Wu, "19.3 An 8.9-to-21.9GHz Single-Core Oscillator with Reconfigurable Class-F-1 and Enhanced-Colpitts Dual-Mode Operation Achieving 209dBc/Hz FoMT," 2024 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2024, pp. 1-3, doi: 10.1109/ISSCC49657.2024.10454525.

[76] H. Ge, H. Jia, W. Deng, R. Ma, Z. Wang and B. Chi, "19.5 A 13.7-to-41.5GHz 214.1dBc/Hz FoMT Quad-Core Quad-Mode VCO Using an Oscillation-Mode-Splitting Technique," 2024 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2024, pp. 356-358, doi: 10.1109/ISSCC49657.2024.10454356.

[77] J. Chen, K. Xu, T. Siriburanon and R. B. Staszewski, "19.4 An 8.1-to-9.9GHz Single-Core Pseudo-Series-Resonance Oscillator Achieving -128.7dBc/Hz PN at 1MHz," 2025 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2025, pp. 1-3, doi: 10.1109/ISSCC49661.2025.10904613.

[78] J. Guo et al., "A Differential Series-Resonance CMOS VCO with Pole-Convergence Technique Achieving 202.1 dBc/Hz FoMTA at 10MHz Offset," 2025 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2025, pp. 332-334, doi: 10.1109/ISSCC49661.2025.10904629.

[79] S. Dash, S. Kumar, T. Siriburanon and R. B. Staszewski, "Trifilar-Transformer-Coupled Series-Resonance Oscillator with Enhanced Tuning Range," 2025 IEEE International Symposium on Circuits and Systems (ISCAS), London, United Kingdom, 2025, pp. 1-5, doi: 10.1109/ISCAS56072.2025.11043857.

[80] A. Moroni, R. Genesi and D. Manstretta, "Analysis and Design of a 54 GHz Distributed “Hybrid” Wave Oscillator Array With Quadrature Outputs," in IEEE Journal of Solid-State Circuits, vol. 49, no. 5, pp. 1158-1172, May 2014, doi: 10.1109/JSSC.2014.2311803.

[81] V. Marazzi, L. Porcheddu, M. Garampazzi, E. Temporiti and D. Manstretta, "A 27 GHz Phase-Coupled Distributed Quad-Core Oscillator in 12 nm FinFET," 2025 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), Busan, Korea, Republic of, 2025, pp. 1-5, doi: 10.1109/APCCAS67402.2025.11376735.

[82] P. Guan et al., "8-Shaped Inductors: An Essential Addition to RFIC Designers' Toolbox," in IEEE Open Journal of the Solid-State Circuits Society, vol. 4, pp. 131-146, 2024, doi: 10.1109/OJSSCS.2024.3455269.

[83] J. J. Rael and A. A. Abidi, “Physical processes of phase noise in differential LC oscillators,” in Proc. IEEE Custom Integrated Circuits Conf., Orlando, FL, 2000, pp. 569–572.

[84] A. Demir, A. Mehrotra, and J. Roychowdhury, “Phase noise in oscillators: a unifying theory and numerical methods for characterization,” IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, vol. 47, no. 5, pp. 655–674, 2000.

[85] P. Andreani and X. Wang, “On the phase-noise and phase-error performances of multiphase LC CMOS VCOs,” IEEE Journal of Solid-State Circuits, vol. 39, no. 11, pp. 1883–1893, 2004.

[86] F. Pepe and P. Andreani, "Still More on the 1/f2 Phase Noise Performance of Harmonic Oscillators," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 63, no. 6, pp. 538-542, June 2016, doi: 10.1109/TCSII.2016.2530438.

[87] A. Mirzaei, M. E. Heidari and A. A. Abidi, "Analysis of Oscillators Locked by Large Injection Signals: Generalized Adler's Equation and Geometrical Interpretation," IEEE Custom Integrated Circuits Conference 2006, San Jose, CA, USA, 2006, pp. 737-740, doi: 10.1109/CICC.2006.320928.

[88] A. Mirzaei, M. E. Heidari, R. Bagheri, S. Chehrazi and A. A. Abidi, "The Quadrature LC Oscillator: A Complete Portrait Based on Injection Locking," in IEEE Journal of Solid-State Circuits, vol. 42, no. 9, pp. 1916-1932, Sept. 2007, doi: 10.1109/JSSC.2007.903047.

[89] A. Mirzaei and M. E. Heidari, "On the mode analysis of coupled oscillators," 2009 52nd IEEE International Midwest Symposium on Circuits and Systems, Cancun, Mexico, 2009, pp. 819-822, doi: 10.1109/MWSCAS.2009.5235894.

[90] P. Andreani, "Some Results on Oscillation Stability in Multi-Mode Harmonic Oscillators," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 70, no. 3, pp. 860-864, March 2023, doi: 10.1109/TCSII.2022.3216895.

[91] P. Arcioni, M. Bressan and G. Conciauro, "A new algorithm for the wide-band analysis of arbitrarily shaped planar circuits," in IEEE Transactions on Microwave Theory and Techniques, vol. 36, no. 10, pp. 1426-1437, Oct. 1988, doi: 10.1109/22.6091.

[92] Y. Cassivi, L. Perregrini, K. Wu and G. Conciauro, "Low-Cost and High-Q Millimeter-Wave Resonator Using Substrate Integrated Waveguide Technique," 2002 32nd European Microwave Conference, Milan, Italy, 2002, pp. 1-4, doi: 10.1109/EUMA.2002.339390.

[93] J. -A. Zhang et al., "An Equivalent Circuit Model of 12 nm P-FinFET for NBTI Effect," in IEEE Transactions on Device and Materials Reliability, vol. 25, no. 2, pp. 247-252, June 2025, doi: 10.1109/TDMR.2025.3543863.

[94] S. -L. Jang *et al.*, "Area-Efficient Standing-Wave Oscillator with a Double-8-shaped Inductor," 2023 Asia-Pacific Microwave Conference (APMC), Taipei, Taiwan, 2023, pp. 34-36, doi: 10.1109/APMC57107.2023.10439806.

[95] A. Rossoni et al., "Layout experiments and test structures to characterize Local Layout Effects due to mechanical stress in FinFET transistors," 2025 IEEE 37th International Conference on Microelectronic Test Structures (ICMTS), San Antonio, TX, USA, 2025, pp. 1-4, doi: 10.1109/ICMTS63811.2025.11068908.

[96] Q. Lin, H. Pan and J. Chang, "Test structures for debugging variation of critical devices caused by layout-dependent effects in FinFETs," 2018 IEEE International Conference on Microelectronic Test Structures (ICMTS), Austin, TX, USA, 2018, pp. 3-6, doi: 10.1109/ICMTS.2018.8383751.

[97] J. Yun, H. Kim, H. Seo and J. -S. Rieh, "A 140 GHz single-ended injection locked frequency divider with inductive feedback in SiGe HBT technology," 2012 IEEE 12th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, Santa Clara, CA, USA, 2012, pp. 61-64, doi: 10.1109/SiRF.2012.6160135.

[98] H. Razavi and B. Razavi, "A 27-73 GHz Injection-Locked Frequency Divider," 2021 Symposium on VLSI Circuits, Kyoto, Japan, 2021, pp. 1-2, doi: 10.23919/VLSICircuits52068.2021.9492457.

[99] A. Ghilioni, U. Decanis, E. Monaco, A. Mazzanti and F. Svelto, "A 6.5mW inductorless CMOS frequency divider-by-4 operating up to 70GHz," 2011 IEEE International Solid-State Circuits Conference, San Francisco, CA, USA, 2011, pp. 282-284, doi: 10.1109/ISSCC.2011.5746319.

[100] W. -C. Lai, S. -L. Jang, Y. -W. Huang and M. -H. Juang, "Divide-by-2 Injection-Locked Frequency Divider Using 3-path Transformer-Coupled Resonator," 2020 27th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Glasgow, UK, 2020, pp. 1-4, doi: 10.1109/ICECS49266.2020.9294876.

[101] H. An, H. Nam, S. Kim, Y. Lim and H. Yoon, "An Area-Efficient CMOS Cross-Coupled LC-VCO Using Nested Intertwined Tail Inductors," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 72, no. 1, pp. 143-147, Jan. 2025, doi: 10.1109/TCSII.2024.3485921.

List of Publications

I V. Marazzi, E. Monaco, C.Nani and D.Manstretta,"Analysis and Design of a Low Power Double Tail Comparator with Dynamic Bias in 5nm FinFET Technology", 2023 18th Conference on Ph.D Research in Microelectronics and Electronics(PRIME), Valencia, Spain, 2023, pp. 29-32, doi : 10.1109/PRIME58259.2023.10161758.

II V. Marazzi, E. Monaco, C. Nani, D. Manstretta (2024), "A 0.94V Dynamic Bias Double Tail Comparator for High-Speed Applications in 5nmTechnology". In : Bellotti, F., et al. Applications in Electronics Pervading Industry, Environment and Society. ApplePies 2023. Lecture Notes in Electrical Engineering, vol 1110. Springer, Cham. https://doi.org/10.1007/978-3-031-48121-5-10.

III V. Marazzi, L. Porcheddu, M. Garampazzi, E. Temporiti, D. Manstretta, "A 27GHz Phase-Coupled Distributed Quad-Core Oscillator in 12nm FinFET", 2025, IEEE Asia Pacific Conference On Circuits and Systems (APCCAS), Busan, South Korea, 2025.

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