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Ph.D. School in Microelectronics

5G SAW-less FDD architecture design

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Abstract:

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by Simone Lecchi

This thesis introduces a new Full-Duplex (FD) architecture for mobile communication standards, eliminating the need for external Surface Acoustic Wave (SAW) filters. It starts with a review of standard requirements, an analysis of overall architecture constraints and presentation of simulation results, this work proposes a two-path noise-cancelling architecture. In this architecture, the main receiver captures the input signal from the antenna, while the auxiliary receiver captures noise leakage from the transmitter. The noise cancellation is performed in the digital domain through an adaptive digital filter.

A main receiver topology based on a positive translational feedback loop is chosen for its excellent attributes, including high linearity and low noise. The forward path includes a low-noise transconductance amplifier (LNTA), four phase passive mixers and third-order filtering transimpedance amplifiers. A tunable RC feedback path is loaded at the baseband output, followed by additional four-phase passive up-conversion mixers, enabling tunable, frequency-selective input matching. An analytical model of the structure alongside measurement results will be provided in the dedicated chapter.

The auxiliary receiver is designed specifically to increase the ratio between its compression point and its noise figure, with minimal power consumption. The architecture chosen is a LNTA-first with a second-order baseband filter. Thanks to the high input impedance of this receiver it can be placed at the transmitter output without adding considerable loading effects. Measurement results of this auxiliary receiver are presented at the end of the chapter.

For the observation of noise cancellation, a Field-Programmable Gate Array (FPGA) is programmed in order to acquire signals from the receivers. The design includes a Clock and Data Recovery (CDR) module, a storage memory and a Universal Asynchronous Receiver-Transmitter (UART) interface for signal transmission to a computer. The design is subsequently validated, demonstrating signal cancellation in MATLAB through the use of an adaptive digital filter employing the Least Mean Squares (LMS) algorithm.

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Introduction

In the last few years the field of Radio Frequency (RF) telecommunications is in a non-stop growing trend due to the release of new communication standards and market's requirements. These improvements are point to increasing the speed of services and set up more reliable wireless communication. The design of RF systems, which of course involves the development of transmitters and receivers, meets different challenges and opportunities persecuting growing demands for speed and user capacity while trying to reach ever lower power consumption and high performance.

A significant influencing factor in the evolution of RF design is the spread of the Internet of Things (IoT) and the starting of the 5G communications era. This convergence will lead to a wide and various network of connected devices across numerous domains: from portable devices to industry, but also healthcare, smart homes and cities or autonomous vehicles. These applications increase the request to access larger bandwidth, reaching a lower latency, while increasing both reliability of the overall connected network. To achieve these targets, new RF systems must be developped with the aim of supporting multiple frequency bands ranging from sub-6 GHz to millimeter-wave. This involves advanced techniques such as massive Multiple-Input Multiple-Output (MIMO), beamforming and network slicing.

Regarding LTE-Advanced mobile communication standard, wireless receivers heavily rely on robust front-end filtering to prevent signal degradation. Even though Surface Acoustic Wave (SAW) off-chip filters are commonly employed, they present challenges such as scalability limits, significant area demands and limited tunability. As the number of frequency bands and antennas increases, these challenges are becoming more and more important in the considerations related to system area and costs. This leads to a growing

interest for a wide-band receiver solution that can operate without the use of an external SAW filters, often referred to as a SAW-Less receiver.
The thesis is organized as follows:

Chapter 1 explains the fundamental metrics used in the analysis of wireless receivers, outlining their importance and application within the wider domain of RF design.

Chapter 2 introduces the main challenges in facing SAW-Less Receivers design and the necessity of introducing Self-Interference Cancellation (SIC) architectures. The chapter describes the proposed Frequency Division Duplex (FDD) receiver which architecture includes a Main receiver and an Auxiliary receiver. The Auxiliary receiver senses the transmitter (TX) output in the Main receiver band of interest and sends this signal to the digital signal processing block, where Self-Interference Cancellation (SIC) is performed. The proposed architecture is validated by MATLAB® simulations, demonstrating the effectiveness of SIC.

Chapter 3 presents the Main receiver, including an analytic analysis of the positive translational loop architecture and a description of the receiver's building blocks. The chapter also presents results obtained from measurements of the 28 nm prototype.

Chapter 4 deals with the Auxiliary receiver, whose design is focused on achieving high linearity and low noise. The chapter introduces target performances and in the end results obtained from measurements of the 28 nm chip prototype are presented.

Chapter 5 outlines the Field-Programmable Gate Array (FPGA) design, which includes a Clock and Data Recovery (CDR) module, a storage memory and a Universal Asynchronous Receiver-Transmitter (UART) interface for signal transmission to a computer. The chapter describes the design and its implementation, validating it and demonstrating initial signal cancellation through the use of an adaptive digital filter employing the Least Mean Squares (LMS) algorithm.

Chapter 1

Basic Concepts in RF design

Wireless communication standards change as fast as the request of increasing demand of speed and number of users. This leads to a push for improvement the performances of wireless transmitters and receivers, with more complex design and new system architectures. In this chapter the main useful metrics used to described wireless receivers are defined.

1.1 Communication metrics

The telecommunications industry is characterized by a constant increase in the development of standards and technologies. Continuous improvements in the performance of transmitters and receivers, both in wireline and wireless communication, are required due to the rapid pace of the wordwide market.

As such, the design of all devices becomes more and more complex, often employing new architectures to meet users' increasing demands for speed and capacity.

In this chapter the focus will be in radio frequency (RF) communication standards, considering the set of parameters required for evaluating the performance of wireless devices, outlining their meaning and application within the RF systems.

1.1.1 Sensitivity and noise figure

The signal that must be sensed by the receiver is drawn in a noisy environment. The smallest input power level that meets or exceeds the requirements for the specified reference measurement channel by the receiver, ensuring a sufficient Signal-to-Noise Ratio (SNR), is defined sensitivity [1] and is described by the relation

$$P_{sens}|_{dBm} = P_{RS}|_{dBm/Hz} + 10\log_{10} BW + NF|_{dB} + SNR|_{dB} \tag{1.1.1}$$

where P_{RS} is the noise Power Spectral Density (PSD) of the source, BW is the channel bandwidth, NF is the receiver noise figure and, SNR is the required Signal-to-Noise Ratio. The receiver Noise Figure (NF) is defined as the ratio between the SNR at the input and the output of the receiver as

$$NF|_{\mathrm{dB}} = 10\log_{10}\frac{SNR_{in}}{SNR_{out}} \tag{1.1.2}$$

If the input impedance of the receiver is matched with the antenna then

$$P_{sens}|_{\mathrm{dBm}} = -174\,\mathrm{dBm/Hz} + 10\log_{10}\mathrm{BW} + NF|_{\mathrm{dB}} + SNR_{min}|_{\mathrm{dB}} \tag{1.1.3}$$

where the source, i.e. the antenna, is considered a white noise source resistance of $50\,\Omega$ at temperature of $300\,\mathrm{K}$.

Equation 1.1.3 can be represented as shown in Figure 1.1.1 once rewrite as

$$P_{sens}|_{\mathrm{dBm}} = N_{floor}|_{\mathrm{dBm}} + SNR_{min}|_{\mathrm{dB}} \tag{1.1.4}$$

where

$$N_{floor}|_{\mathrm{dBm}} = -174\,\mathrm{dBm/Hz} + 10\log_{10}\mathrm{BW} + NF|_{\mathrm{dB}} \tag{1.1.5}$$

1.1.2 Nonlinearity

Under a linear small-signal model, the input-output characteristic of a circuit can be approximated with a polynomial

$$y(t) \approx \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \ldots \tag{1.1.6}$$

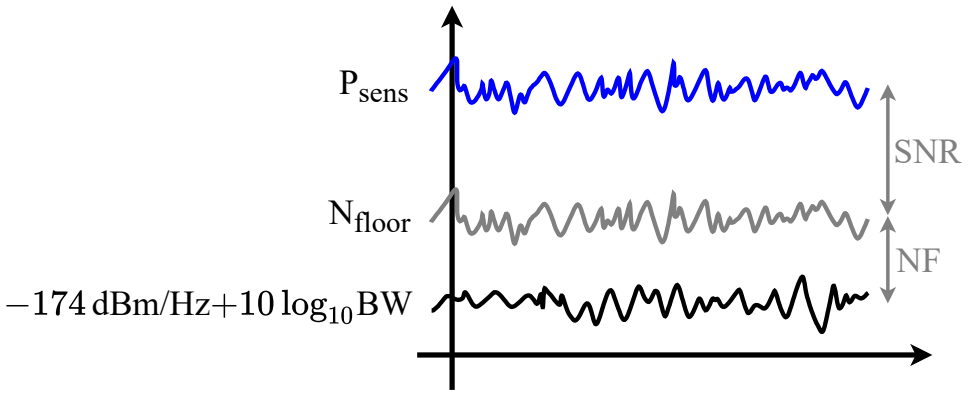


Figure 1.1.1: Simplified description of the link between noise floor, NF, SNR and sensitivity.

where the coefficients α_j can be also function of the time.

Considering applying an input sinusoidal signal $x(t) = A\cos(\omega t)$, the output shows the contribution of the fundamental tone ω plus frequency component that are integer multiples (harmonics) of the input frequency. Neglecting all the contributions higher than the third terms, from Equation 1.1.6 it gets

$$\begin{aligned} y(t) &= \alpha_1 A\cos(\omega t) + \alpha_2(A\cos(\omega t))^2 + \alpha_3(A\cos(\omega t))^3 + \\ &= \alpha_1 A\cos(\omega t) + \frac{\alpha_2 A^2}{2}(1+\cos 2\omega t) + \frac{\alpha_3 A^3}{4}(3\cos\omega t + \cos 3\omega t) \\ &= \frac{\alpha_2 A^2}{2} + \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right)\cos\omega t + \frac{\alpha_2 A^2}{2}\cos 2\omega t + \frac{\alpha_3 A^3}{4}\cos 3\omega t \end{aligned} \tag{1.1.7}$$

From Equation 1.1.7 it is obtained that even-order non-linearity, resulting from α_j with even j, introduces DC offsets if the system is not fully differential. Equation 1.1.7 shows also that the amplitude related with the fundamental frequency is given by $\alpha_1 + 3\alpha_3 A^3/4$, so it is function of the cubic of the amplitude of the input signal.

Now, the sign of the product $\alpha_1 \cdot \alpha_3$ determines the expansive or decreasing behaviour of the system. RF circuits typically suffers from compression [1], showing a reduction of the gain of an input signal $x(t) = A\cos\omega t$ as A increases, as shown in Figure 1.1.2. This effect is quantified by the 1 dB compression point, defined as the input signal level that causes the gain to

deviate by 1 dB from the ideal behavior.

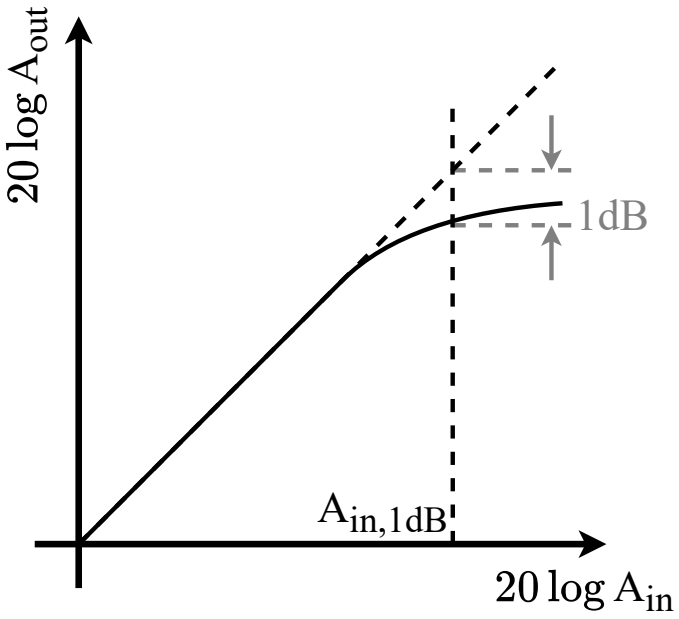


Figure 1.1.2: Visual representation of 1 dB compression point

The 1 dB compression point can be derived imposing equality between the ideal gain α_1 reduced by one and the second coefficient from 1.1.7

$$20\log|\alpha_1| - 1\,\text{dB} = 20\log\left|\alpha_1 + \frac{3}{4}\alpha_3 A_{in,1dB}^2\right| \tag{1.1.8}$$

from which

$$A_{in,1dB} = P_{1dB} = \sqrt{0.145\left|\frac{\alpha_1}{\alpha 3}\right|} \tag{1.1.9}$$

where P_{1dB} is an other notation of the 1 dB compression point.

The compression gain effect is particularly important when the received or transmitted signal contain amplitude information, like in Amplitude Modulation (AM), that can be distorted by compression.

Another negative consequence of compression is related when a large interferer is sensed with the desired signal. Despite the small level of the targeted signal, the high excursions created by the interferer lower the receiver gain and caused the so called desensitization. This effect reduces the

SNR at the receiver output and is crucial even when the signal includes no amplitude information [1].

1.1.3 Intermodulation

The transmission of modulation from the strong interferer to the weak signal is another occurrence that happens when the system is nonlinear. Of particular interest is the case of two interferers received with the desired signal. Considering two interferers at frequencies ω_1 and ω_2 applied to a nonlinear system represented by the Equation 1.1.6, then the output is exhibits also contributions that are a mixing of them. This is called intermodulation (IM) and can be calculated considering an input signal $x(t) = A_1 \cos \omega_1 t + A_2 \cos \omega_2 t$, leading to

$$\begin{aligned} y(t) =& \alpha_1 \left(A_1 \cos \omega_1 t + A_2 \cos \omega_2 t\right) + \alpha_2 \left(A_1 \cos \omega_1 t + A_2 \cos \omega_2 t\right)^2 \\ &+ \alpha_3 \left(A_1 \cos \omega_1 t + A_2 \cos \omega_2 t\right)^3 \end{aligned} \tag{1.1.10}$$

Before expanding the Equation 1.1.10 it is taken into account that, if ω_1 and ω_2 are close to each other, then $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ result to be close to ω_1 and ω_2 too. Consequently, if the working frequencies of a receiver is such that $\omega_0 = 2\omega_1 - \omega_2$, the presence an interferer at $2\omega_1 - \omega_2$ fall into the targetted signal channel, corrupting the signal as shown in Figure 1.1.3.

Expanding now the Equation 1.1.10, the third-order intermodulation products (IM3) at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ are

$$\begin{aligned} y(t) =& \cdots + \frac{3\alpha_3 A_1^2 A_2}{4} \cos\left(2\omega_1 + \omega_2\right)t + \frac{3\alpha_3 A_1^2 A_2}{4} \cos\left(2\omega_1 - \omega_2\right)t + \ldots \\ & \cdots + \frac{3\alpha_3 A_1 A_2^2}{4} \cos\left(2\omega_2 + \omega_1\right)t + \frac{3\alpha_3 A_1 A_2^2}{4} \cos\left(2\omega_2 - \omega_1\right)t + \ldots \end{aligned} \tag{1.1.11}$$

A common method of IM3 characterization is the “two-tone” test , where two sinusoids ω_1 and ω_2 of equal amplitudes A are applied to the input such that $\omega_0 = 2\omega_1 - \omega_2$.

From Equation 1.1.11 if the amplitude of each input tone increases by 6 dB, the amplitude of the IM3 products ($\propto A^3$) rises by 18 dB and hence the relative IM3 by 12 dB. As shown in Figure 1.1.4, the input level at which

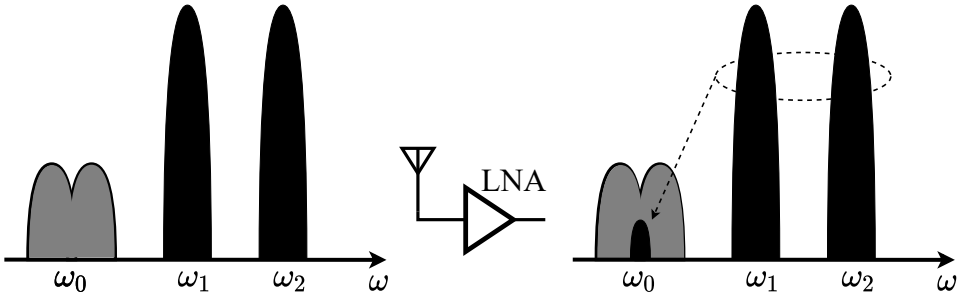


Figure 1.1.3: Corruption due to third-order intermodulation [1]

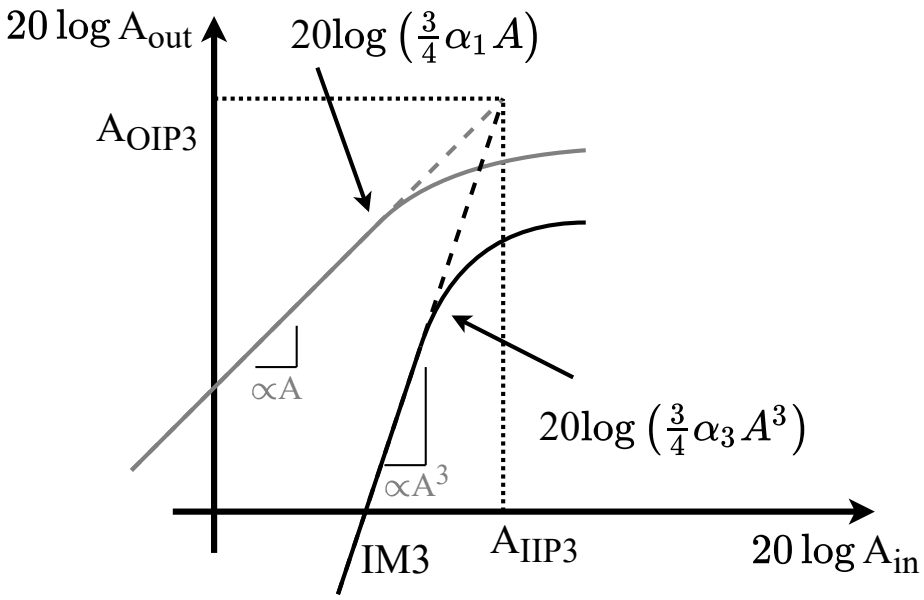


Figure 1.1.4: Fundamental and IM3 behaviour in relation to input power [1]

the amplitude of the IM3 products becomes equal to that of the fundamental tones at the output is called the input third intercept point (IIP_3). While, the corresponding output is defined as OIP_3.

The $IIP3_3$ is determined equating the fundamental and the IM3 amplitudes

$$|\alpha_1 A_{IIP3}| = \left|\frac{3}{4}\alpha_3 A_{IIP3}^3\right| \tag{1.1.12}$$

which brings to

$$A_{IIP3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|} \tag{1.1.13}$$

From Equation 1.1.9 and 1.1.13 results in a theorical value of IIP_3 9.6 dB higher than P_{1dB}. This brings to the fact that the third intercept point is not observable because increasing the input interferer power results in reaching the compression level and also producing higher order non-linearities which make the fundamental and IM3 slope from their theoretical one.

The IIP_3 must be extrapolate from the fundamental and the IM3 plots following the slopes (1 and 3 in a log-log scale) at very low input level, where higher order nonlinearities are negligible. This leads to Equation 1.1.14

$$IIP_3|_{\text{dBm}} = \frac{\Delta P}{2} + A_{in}|_{\text{dBm}} \tag{1.1.14}$$

where A_{in} is the input interferer power and ΔP is defined as

$$\Delta P = \frac{A_{in}|_{\text{dBm}} - A_{IM3}|_{\text{dBm}}}{2} \tag{1.1.15}$$

1.1.4 Effect of reciprocal mixing

In RF receivers, oscillators are crucial for generating stable reference frequencies needed for signal processing.

Considering an ideal oscillator, it generates a perfectly periodic output $x(t) = A\cos(\omega_c t)$ which crosses the zero at integer multiples of $T_c = \frac{2\pi}{\omega_c}$. In reality the noise from oscillator devices randomly perturbs these zero crossings, leading to an output spectrum as in Figure 1.1.5 .

To take this perturbation into account, the output can be represented as $x(t) = A\cos(\omega_c t + \varphi_n(t))$, where $\varphi_n(t)$ denotes a minor random phase deviation that shifts the zero crossings from integer multiples of T_c [1].

This phenomenon derives from various factors within the receiver system, including oscillator mismatch, noise in the frequency synthesizer and environmental factors such as temperature variations.

Nevertheless, the frequency division or the use of multiple oscillator stages, which are technics commonly used in RF receiver architectures, can introduce additional phase noise. Dividers, for example, are often employed to generate lower frequency reference signals from higher frequency oscillators, but they can contribute to phase noise due to their intrinsic non-ideal characteristics.

Reciprocal mixing occurs when the phase noise of an oscillator interacts with an incoming signal, negatively affecting the performance of the receiver.

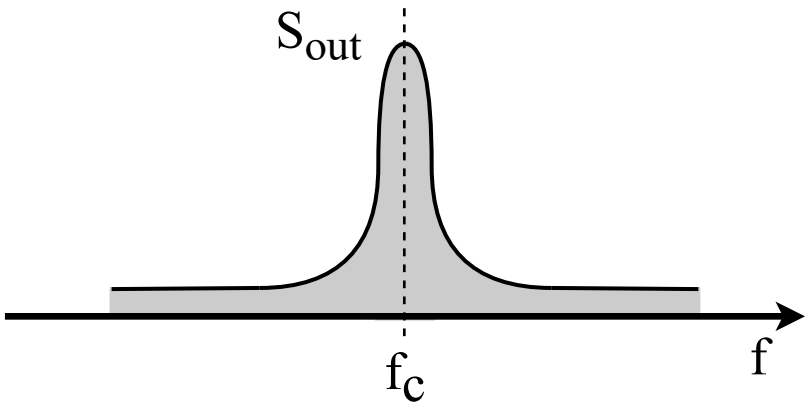


Figure 1.1.5: Output PSD of a noisy oscillator

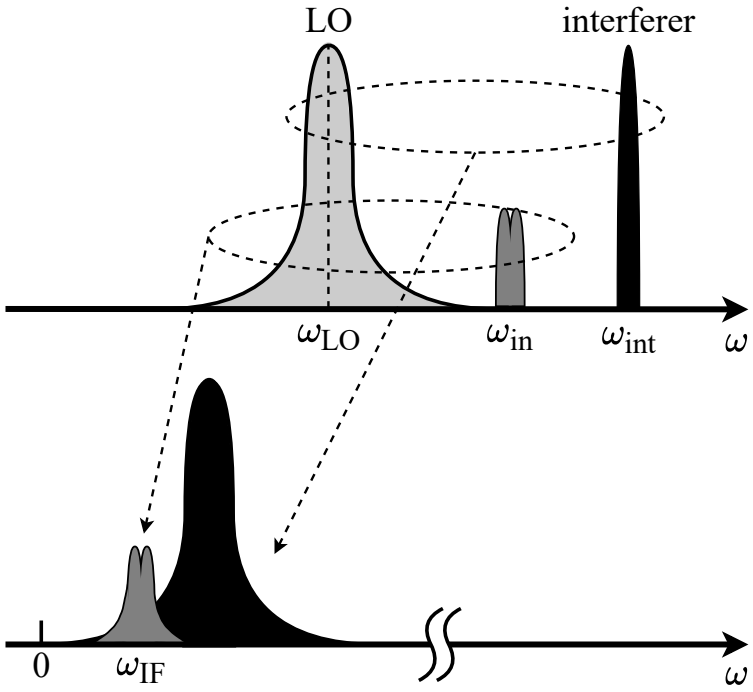


Figure 1.1.6: Downconversion with a noisy LO (reciprocal mixing)

This interaction leads to the convolution of the desired signal and the interferer with the noisy LO spectrum, which causes the expansion of spectrum of the downconverted interferer. A representation of this effect is shown in Figure 1.1.6.

This broadening effect shows as a noise skirt, which results in an in-

creasing of the noise floor in the desired IF signal bandwidth, as shown in Equation 1.1.16 [1]

$$N_{floor-RM}|_{\mathrm{dBm}} = 10\log\left(10^{N_{floor}|_{\mathrm{dBm}}/10} + 10^{P_{int}|_{\mathrm{dBm}}+S_{n-LO}|_{\mathrm{dBc/Hz}}}\right) \quad (1.1.16)$$

where N_{floor} is the noise floor from Equation 1.1.5, P_{int} is the interferer power and S_{n-LO} is the LO phase noise at the interferer frequency off-set.

Chapter 2

FDD SAW-less architecture

The demand for increased channel bandwidths has highlighted the need to design receivers that do not require the use of Surface Acoustic Wave (SAW) filters. This chapter briefly introduces the main difficulties in adopting SAW-Less Receivers and the need to introduce Self-Interference Cancellation (SIC) architectures. In Section 2.2, the proposed Frequency Division Duplex (FDD) receiver is described and the system is validated by MATLAB® simulations demonstrating the actual effectiveness of SIC.

2.1 SAW-Less Receivers

The evolution of wireless communication standards has been driven by the need to provide an increasing number of connected users while maintaining high service quality. To meet these demands, numerous enhancements have been introduced to optimize the transmission and reception of data, leading to greater system complexity in wireless transceiver design.

The Frequency Division Duplex (FDD) architecture utilizes separate channels for uplink and for downlink transmissions, facilitating full duplex communication. However, achieving this capability particularly care must be taken in mitigating signal interference, particularly from Out-Of-Band (OOB)

signals and self-interference originating from the transmitter. This necessity is depicted in Figure 2.1.1. Typically, Surface Acoustic Wave (SAW) off-chip filters are utilized to address these challenges, selectively filtering frequencies to prevent signal corruption and significantly relaxing linearity performance of the receiver [2].

However, these filters present drawbacks such as high cost and area occupation, due to the fact that they cannot be integrated on silicon. Furthermore, they have poor tunability, covering a limited number of bands. As mobile systems increasingly incorporate multiple frequency bands and utilize multiple antennas (MIMO), these filtering components are poised to become dominant factors influencing both the area and cost of such systems.

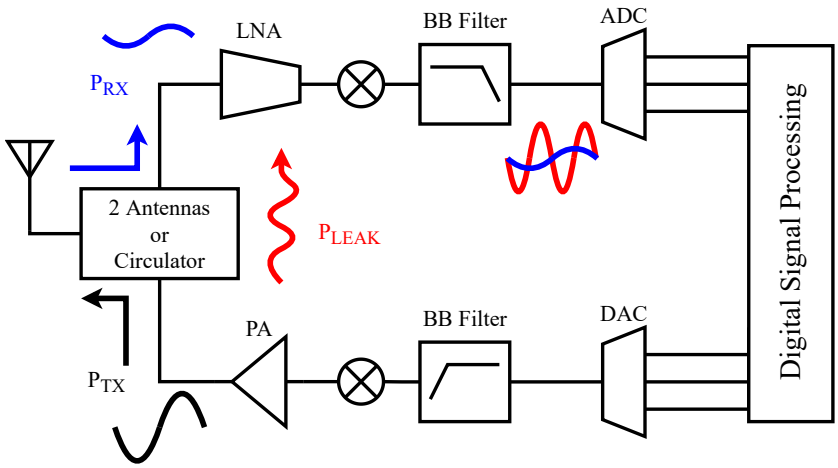


Figure 2.1.1: A generic Frequency Division Duplex (FDD) transceiver. The transmitted and received signals are shown in black and blue, respectively. In red, the TX-leakage in the RX path.

It must consider the fact that antenna isolation typically ranges between $30-40\,\text{dB}$ [3–5]. Consequently, issues such as receiver linearity and reciprocal mixing with the phase noise of receiver's local oscillator (LO) become important when the level of filtering between the transmitter (TX) and receiver (RX) is reduced [6–11].

Therefore, it becomes imperative to reduce the LO phase noise by one dB for every dB of filter attenuation removed at the interferer's frequency, as shown in Equation 1.1.16. These dual mechanisms dictate an increased requirement for receiver linearity and blocker tolerance, while simultaneously

reducing the phase noise of the LO signals.

Another factor contributing to sensitivity degradation is the noise generated by the TX in the receive band that leaks to the RX. This effect takes on greater importance when external duplexers are substituted with passive on-chip solutions like the hybrid transformer [12–15], which isolate the receiver from the transmitter through electrical balancing, thereby providing minimal TX out-of-band (OOB) emission filtering.

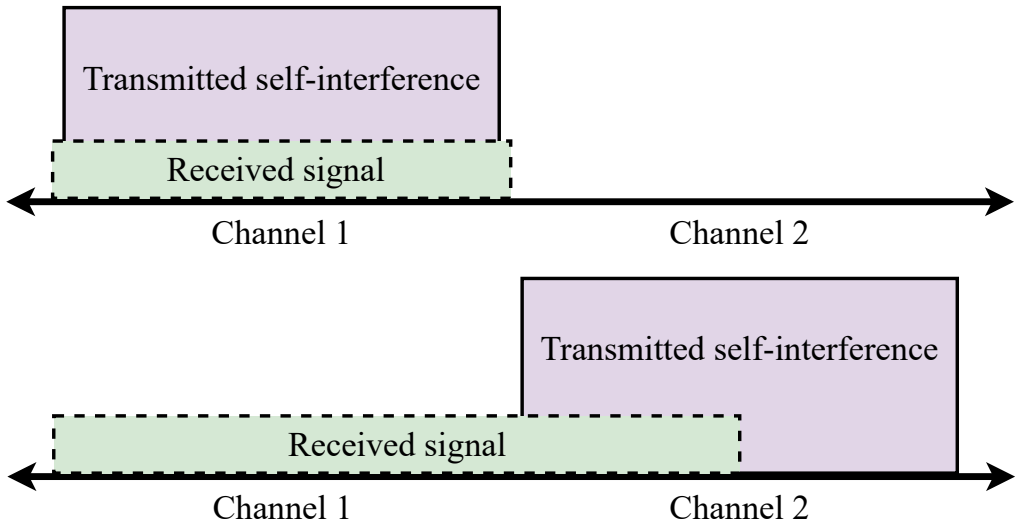


Figure 2.1.2: SIC can be applied to in-band Full Duplex (FD) and adaptive FDD [16]

Utilizing Self-Interference Cancellation (SIC) techniques offers the potential to relax stringent requirements on Surface Acoustic Wave (SAW) filters [17–19]. SIC has the potential to support and improve the development of fifth-generation (5G) technologies, especially in the future, when networks are going to become more and more crowd and heterogeneous.

Therefore, SIC has potential for reaching true full-duplex communication in wireless systems, theoretically doubling link capacity [16]. As shown in Figure 2.1.2, SIC operates independently of frequency, facilitating more than just in-band full-duplex functionality. It essentially works as a software-configurable adaptive duplexer, making easier transmission and reception on arbitrary separate channels. Consequently, this simplifies RF front-end complexities, especially for applications like carrier aggregation and helps the creation of radios featuring smaller, lighter and more efficient filters [16].

In recent years, the SIC technique has garnered considerable attention for addressing these challenges, particularly in systems employing FD [20, 21] and FDD [22, 23], which involve simultaneous transmission and reception.

Given that the frequency gap between transmit and receive bands can extend into the hundreds of megahertz range, achieving high isolation between TX and RX ($ISO_{TX—RX}$) in both bands poses a significant challenge [15, 24–28] for meeting rigorous standards [29].

2.2 Proposed FDD architecture

The following section provides a system analysis of Frequency Division Duplex (FDD) with transmitter leakage cancellation. Figure 2.2.1 illustrates the comprehensive system block diagram of the proposed FDD receiver, highlighting the noise levels at various points within the system.

In this architecture, transmission and reception occur simultaneously across distinct frequency bands. A filter, potentially realized with a hybrid transformer, is incorporated to mitigate Self-Interference (SI) originating from the transmitter (TX) to the primary receiver (MAIN RX).

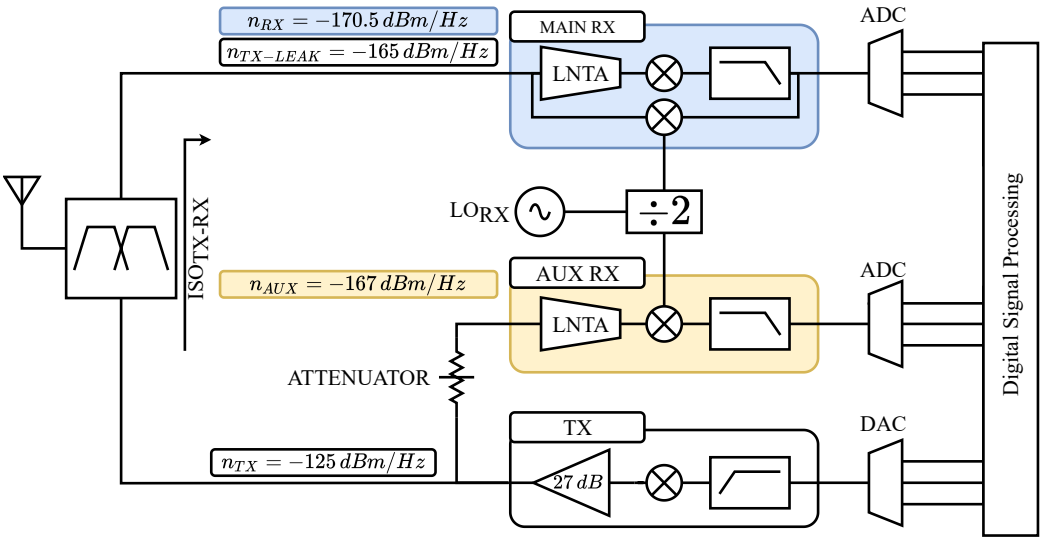


Figure 2.2.1: Block diagram of the proposed FDD architecture

As depicted in Figure 2.2.1, unlike architectures featuring a SIC circuit in the RF domain, as described in prior work [22, 30], in the proposed design

SIC occurs subsequent to the MAIN RX in the digital domain. Consequently, the leakage signal originating from the TX encounters only one stage of attenuation. It's crucial that this leakage signal does not compromise the performance of the MAIN RX in terms of gain and noise, ensuring degradation does not exceed 1 dB. This defines the target 1 dB compression point (P1dB) of the MAIN RX as follows:

$$P1dB_{MAIN} = TX_{OUT} - ISO_{TX-RX} + 6\,dB \tag{2.2.1}$$

Here, TX_{OUT} represents the maximum signal power of the transmitter, typically 27 dBm [29] and ISO_{TX-RX} denotes the insertion loss of the TX signal in the RX band. Additionally, the Peak-to-Average Power Ratio (PAPR) is taken into account, introducing a 6 dB increment.

Reciprocal mixing emerges as a critical difficulty in receivers that can potentially detect high-level interferers [1]. The target 1 dB NF expansion can be determined using the equation

$$NF1dB_{MAIN} = TX_{OUT} - ISO_{TX-RX} \tag{2.2.2}$$

resulting in a value 6 dB lower than P1dB.

Figure 2.2.2 illustrates the expected noise figure of the Main receiver as a function of isolation ISO_{TX-RX}. The Main receiver input-referred noise, here -170.5 dBm/Hz, will be discussed in Section 3.1.1, while TX output signal and noise levels, respectively 27 dBm and -152 dBc/Hz, are considered from the standards [29]. As discussed in Section 1.1.4, the reciprocal mixing effect can be quantified as an increase in the noise figure, given by the equation

$$\begin{aligned} NF_{M-w/o\,SIC} =& 174\,dBm/Hz + 10\log_{10}\big(10^{NF_{M0}/10} + & (1)\\ & 10^{(PN+TX_{OUT-PWR}-ISO_{TX-RX})/10} + & (2)\\ & 10^{(TX_{OUT-NOISE}-ISO_{TX-RX})/10}\big) & (3) \end{aligned} \tag{2.2.3}$$

where (1) is the MAIN RX NF, (2) indicates the reciprocal mixing effect due to the divider's phase noise PN and the TX leakage signal and (3) accounts for the TX leakage noise.

As depicted in Figure 2.2.2, the noise figure could increase by more than 6.5 dB due to the reciprocal mixing effect. These outcome depends on the

difference between $TX_{OUT-PWR}$ power and ISO_{TX-RX} and of the phase noise of the divider. Consequently, it becomes imperative to introduce a Self-Interference Cancellation to maintain a reasonable level of RX noise figure.

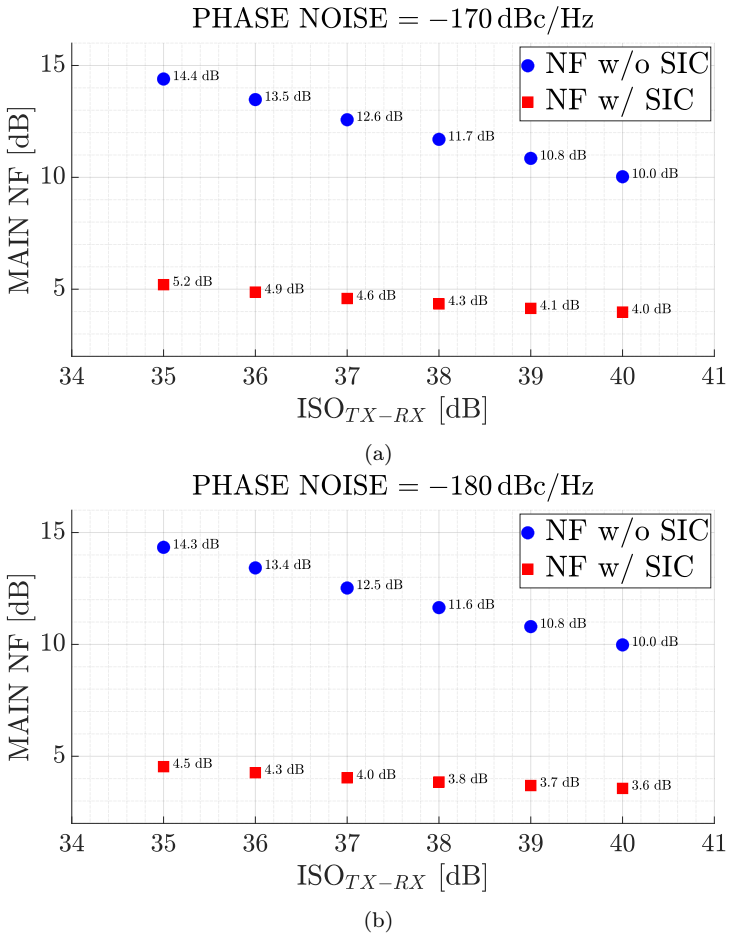


Figure 2.2.2: Main receiver NF w/o and w/ SIC as a function of $ISO_{TX—RX}$ for −170 dBc/Hz (a) and −180 dBc/Hz (b) divider's phase noise

An auxiliary receiver (AUX RX) is introduced to sense the TX output in the MAIN RX band and transmit this signal to the Digital Signal Processing (DSP) block, where the Self-Interference Cancellation is performed. While it is assumed that the DSP could achieve perfect cancellation of correlated noise, such as the noise of the TX sensed by the two receivers, the noise introduced by the auxiliary receiver itself is uncorrelated and cannot be canceled by the adaptive digital filters. Consequently, the noise of the AUX

RX is considered to be 15 dB lower than the TX output noise, resulting in $-167\,\mathrm{dBm/Hz}$ with an attenuation $\mathrm{ATT_{TX\text{-}AUX}}$ equal to 27 dB.

Applying the Self-Interference Cancellation, the resulting noise figure of the main path has two contributors: the reciprocal mixing effect and the auxiliary receiver residual noise, as shown in the following equation:

$$\begin{aligned} NF_{M-w/\,SIC} =& 174\,dBm/Hz + 10\log_{10}\big(10^{NF_{M0}/10} + \quad (1)\\ & 10^{(PN+TX_{OUT-PWR}-ISO_{TX-RX})/10} + \quad (2)\\ & 10^{NF_A/10}\big) \quad (3) \end{aligned} \tag{2.2.4}$$

Here, (1) represents the MAIN RX NF, (2) defines the reciprocal mixing effect due to the divider PN and the TX leakage signal and (3) represents the AUX RX NF defined by the equation:

$$\begin{aligned} NF_A =& 174\,dBm/Hz + 10\log_{10}\big(10^{NF_{A0}/10} + \\ & 10^{(PN+TX_{OUT-PWR}-ATT_{TX-AUX})/10}\big) \end{aligned} \tag{2.2.5}$$

where $\mathrm{ATT_{TX\text{-}AUX}}$ is the attenuation between the transmitter and the auxiliary receiver, as depicted in Figure 2.2.1.

In fact, the auxiliary receiver is also affected by the reciprocal mixing effect experienced by the Main receiver. The level of the attenuator depends on the blocker tolerance of the auxiliary receiver. Therefore, the design of the AUX RX must prioritize optimizing the ratio between noise figure expansion and the 1 dB compression point.

2.2.1 Phase-Shift Keying Simulation

In this section, a system validation is conducted based on the considerations outlined in Section 2.2 and employing the additive white gaussian noise (AWGN) channel model. A generic received waveform $r(t)$ can be expressed as

$$r(t) = s_m(t) + n(t) \tag{2.2.6}$$

Here, $s_m(t)$ represents one of the M possible transmitted signals or symbols and $n(t)$ characterizes a zero-mean white Gaussian noise with a power spectral density of $N_0/2$.

For the specific scenario of an even number of symbols, corresponding to a square constellation, an exact expression for the error probability of a Quadrature Amplitude Modulation (QAM) can be derived [31] as

$$\begin{aligned} P_{e,M-QAM} =& 2\left(1-\frac{1}{\sqrt{M}}\right) Q\left(\sqrt{\frac{3\log_2 M}{M-1}BNR}\right) \\ & \times\left(\frac{1}{\sqrt{M}} Q\left(\sqrt{\frac{3\log_2 M}{M-1}BNR}\right)\right) = \text{BER} \end{aligned} \tag{2.2.7}$$

where BNR is the ratio of the energy of one bit $\mathcal{E}_{bavg}$ to $N_0/2$ and $Q(x)$ represents the Q-function, which denotes the probability that a normal (Gaussian) random variable will exceed a value greater than x standard deviations. This function is defined as

$$\begin{aligned} Q(x) &= \frac{1}{2}\left(\frac{2}{\sqrt{\pi}}\int_{x/\sqrt{2}}^{\infty}\exp\left(-t^2\right)dt\right) \\ &= \frac{1}{2}\text{erfc}\left(\frac{x}{\sqrt{2}}\right) \end{aligned} \tag{2.2.8}$$

The modulation scheme of four-phase Phase Shift Keying (PSK) involves relative phase shifts of 0°, 90°, 180°and 270° between successive intervals, which could correspond, for example, to the information bits 00, 01, 11 and 10, respectively. Once received, the signal is demodulated and detected to one of the M possible transmitted symbols.

This Quadrature Phase-Shift Keying (QPSK) can be performed by representing symbols in the constellation diagram using sine and cosine waves

$$s_{RX-n}(t) = \sqrt{\mathcal{E}_{bavg}}\left(b_{2n}\cos\omega_c t + b_{2n+1}\sin\omega_c t\right) \tag{2.2.9}$$

Here, b_{2n} and b_{2n+1} are respectively even-numbered and odd-numbered bits and ω_c is the carrier frequency. Since $\cos\omega_c t$ and $\sin\omega_c t$ are orthogonal, the signal can be detected uniquely and the bits b_{2n} and b_{2n+1} can be separated without corrupting each other [1]. Note that the symbol rate of the signal $s_{RX-n}(t)$ of QPSK is half of its bit rate.

Alternatively, assuming that b_{2n} and b_{2n+1} are pulses with a height of ± 1, the transmitted signal from the receiver's perspective can be expressed as

$$s_{RX-n} = s_n(t) = \sqrt{\mathcal{E}_{bavg}}\left(I_n + jQ_n\right) \tag{2.2.10}$$

where I_n (in-phase) and Q_n (quadrature) denote the demodulated points of the constellation corresponding to the n-transmitted symbol.

Equation 2.2.6 illustrates that the received signal $r(t)$ is the combination of the information bits $s(t)$ and the cumulative effect of all independent noise sources $n(t)$. The ratio between $s(t)$ and $n(t)$ defines the Symbol-to-Noise Ratio (SyNR), equivalent to the SNR of the receiver.

Viewing QPSK modulation as a form of 4-QAM with a square constellation, the Bit Error Rate (BER) is derived from Equation 2.2.7 with $M = 4$:

$$\begin{aligned} \mathrm{BER}_{BNR} &= Q\left(\sqrt{2BNR}\right)\left(\frac{1}{2}Q\left(\sqrt{2BNR}\right)\right) \\ &= \frac{1}{2}\mathrm{erfc}\left(\sqrt{Q\left(\sqrt{BNR}\right)}\right) \end{aligned} \tag{2.2.11}$$

where $\mathrm{erfc}(x)$ denotes the Complementary Error Function evaluated for x as defined in Equation 2.2.8.

Figure 2.2.3 portrays the simulated Bit Error Rate (BER) as a function of the SNR. The black line represents the theoretical BER derived from Equation 2.2.11, while the red dots depict the simulated BER for the receiver with an input-referred noise of $-170.5\,\mathrm{dBm}$ and a bandwidth of $20\,\mathrm{MHz}$.

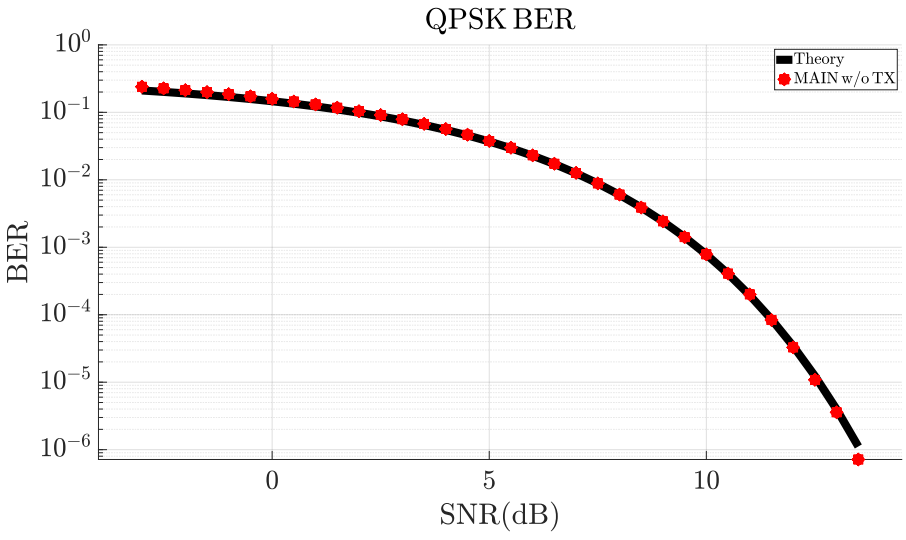


Figure 2.2.3: QPSK BER resulting (black) from Equation 2.2.11, (red) considering only the receiver noise.

2.2.2 LMS filter MATLAB simulation

As shown in Figure 2.2.2, the presence of leakage noise coming from the transmitter contributes to an increasing noise floor captured by the Main receiver. It has been demonstrated in [31] that any orthogonal basis can be employed to expand a zero-mean white Gaussian process, resulting in independent and identically distributed (IID) zero-mean Gaussian random variables with a variance of $N_0/2$ as the coefficients of expansion.

Consequently, considering the Main receiver, the Auxiliary receiver and the Transmitter as three independent noise sources, the signal at the receiver's input is represented as:

$$r(t) = s_m(t) + n_{RX}(t) + n_{TX-leak}(t) \tag{2.2.12}$$

Here n_{RX} and $n_{TX-leak}$ denote zero-mean white Gaussian noise with power spectral densities corresponding to the Main RX and the TX, respectively. A similar assumption is applied to compute the signal sensed by the Auxiliary Receiver. Once the signals from the two receivers are sampled, Noise Cancellation (NC) can be performed.

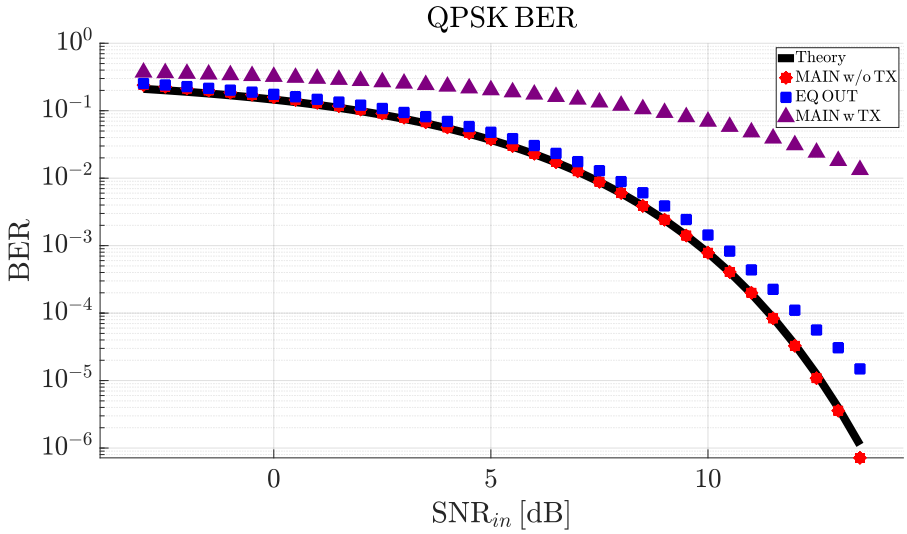


Figure 2.2.4: QPSK BER resulting from Equation 2.2.11 (black), considering only the RX noise (red), resulting from the adaptive filter cancellation (blue) and considering RX noise and the TX leakage (purple).

The results shown in this section don't take into account any Intersymbol Interference (ISI) or Reciprocal Mixing effects.

Figure 2.2.4 illustrates the expected BER when digital filtering is implemented (in blue) or not (in purple) within the system. This plot is generated by simulating the system outlined in Figure 2.2.1, considering 2^{22} symbols sampled with an oversampling factor of $K = 10$. The Adaptive Filter utilized is a linear equalizer from the comm.LinearEqualizer System object™ [32], which consists of a tapped delay line that stores samples from the input signal. Once per symbol period, the equalizer produces a weighted sum of the values in the delay line and updates the weights to prepare for the next symbol period. For this simulation, the Least Mean-Square (LMS) algorithm serves as the adaptive algorithm applied to a 10-tap line. A block diagram of the Linear Equalizer is shown in Figure 2.2.5.

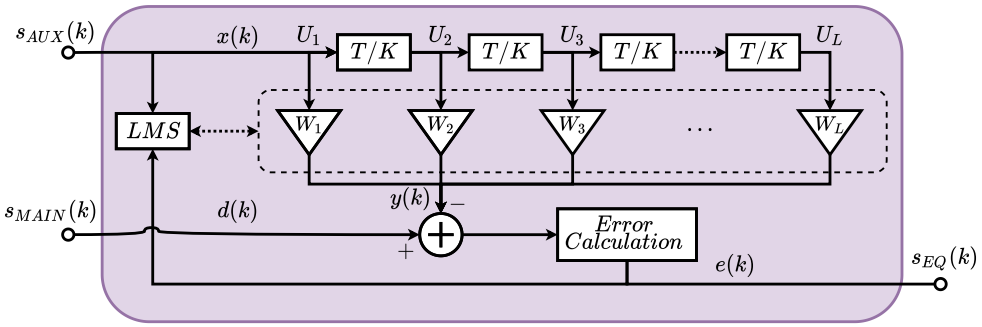


Figure 2.2.5: Block diagram of the Linear Equalizer with L weights, a symbol period of T and K samples per symbol.

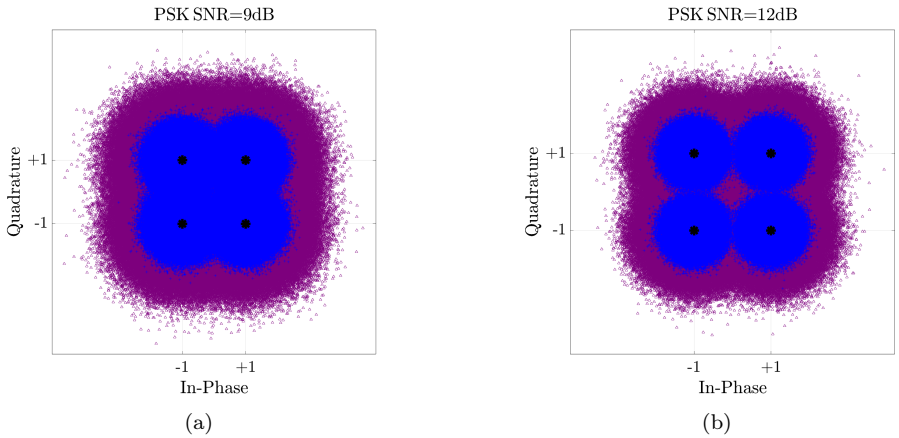


Figure 2.2.6: Main receiver signal with (blue) and without (purple) Noise Cancellation for an SNR of 9 dB (a) and 12 dB (b).

The signal $s_{AUX}(k)$, which has one correlated noise component and one uncorrelated with the noise that needs to be eliminated from the desired signal $d(k)$, is introduced into the adaptive filter. Adaptive filters function by adjusting their coefficients to minimize the difference between $y(k)$ and $d(k)$, thereby generating a clean signal in $e(k)$. This process continues as long as the input noise to the filter remains associated with the unwanted noise accompanying the desired signal. Notably, in this application, the error signal converges to the input data signal rather than converging to zero.

Figure 2.2.6 depicts the resulting constellation (shown in blue) after the suppression of the leakage noise.

Chapter 3

Main receiver architecture

This chapter introduces the Main receiver. In Section 3.2 an analytic analysis of the positive translational loop architecture is presented. In Section 3.3 the Low-Noise Transconductance Amplifier (LNTA) is detailed while Section 3.5 describbes the three stages Transimpedance Amplifier, analyzing the main design constraints. Eventually, Section 3.6 shows the results obtained from measurements conducted on the first prototype.

3.1 SAW-Less Receivers

The wireless receivers in LTE-Advanced heavily depend on high-linearity upfront filtering to prevent signal corruption. Commonly utilized Surface Acoustic Wave (SAW) off-chip filters, while effective, present challenges such as elevated costs, wide area occupation and limited tunability. As the number of frequency bands and antennas (MIMO) increases, these challenges are likely to become predominant in the area and cost considerations of mobile devices. Consequently, there is a growing demand for a wide-band receiver solution capable of operating without external SAW filters, commonly referred to as SAW-Less receivers.

The direct downconversion approach offers a valid solution, enabling the implementation of multiple standards with a single receiver while reducing

power consumption and system complexity. An essential advantage lies in eliminating intermediate frequency passband filtering, replaced by a low-pass filtering stage. This replacement not only improves performance but also allows easier integration into standard semiconductor technologies [33, 34].

Recently, mixer-first architecture has been adopted widely in on-chip receivers demonstrating excellent out-of-band (OOB) linearity performance [35–37]. However, combining high linearity and low NF in mixer-first receivers typically leads to high power dissipation in baseband filter and in the frequency divider [38, 39]. On the other hand, adopting a low noise amplifier (LNA-first receivers) approach offers the potential to achieve a sub 3 dB NF [40, 41], thanks to the smaller mixer switches which consequently leads to reduced power consumption in the LO generation chain. It's important to note that while this approach enhances noise performance, it does come with a trade-off as the LNA imposes limitations on the maximum achievable linearity.

For this application, the Main receiver shown in Figure 2.2.1 must exhibit robust interference tolerance and low noise, necessitating a careful consideration of input impedance matching to align with the characteristic impedance of the antenna. To further enhance the receiver linearity to meet the high IIP3 requirement for a SAW-less receiver, techniques outlined in [42, 43] offer a practical approach for achieving out-of-band (OOB) selectivity. In particular, employing a translational feedback loop with frequency-dependent input matching can provide advantages such as excellent OOB linearity and low noise figure (NF) at low power consumption.

3.1.1 Linearity requirements

Intermodulation between the strongly modulated TX signal and the continuous wave (CW) blocker may interferer in the target signal band, thereby affecting SNR. This issue becomes more and more evident when the isolation between transmitting (TX) and receiving (RX) components decreases.

According to the 3rd Generation Partnership Project (3GPP) standards report [29] for 5G New Radio (NR), the reference sensitivity power level (REFSENS) is defined as the minimum mean power applied to the antenna

at which the throughput meets or exceeds the requirements for the specified reference measurement channel.

Considering a channel bandwidth of 20 MHz in band n1 (2110−2170 MHz) and employing QPSK modulation with a code rate of 1/3, the REFSENS power is specified at −94 dBm [29]. This sensitivity threshold guarantees that the throughput achieves 95% of the maximum achievable data rate, corresponding to a SNR of −1 dB [44].

To determine the target noise figure and the linearity level of the RF receiver, it is considered REFSENS as the sum of two equal contributors: sensitivity defined by receiver noise and sensitivity defined by Non-Linearity Contribution (NLC)

$$\begin{aligned} REFSENS &= SENS_{noise} + SENS_{NLC} \\ &= 10\log_{10}\left(2 \cdot 10^{-97\,\mathrm{dBm}/10}\right) = -94\,\mathrm{dBm} \end{aligned} \tag{3.1.1}$$

From Equation 1.1.4, the $SENS_{noise}$ contribution is defined as

$$REFSENS = N_{floor}|_{\mathrm{dBm}} + SNR_{min}|_{\mathrm{dB}} + 1.5\,\mathrm{dB} = -97\,\mathrm{dBm} \tag{3.1.2}$$

Here, a margin of 1.5 dB is considered. This results from Equation 1.1.5 in the targeted noise figure for the Main receiver being 3.5 dB.

Considering the Non-Linearity Contribution $SENS_{NLC}$ solely due to the third-order intermodulation products, the minimum target IM3 is defined as

$$IM3_{min} = SENS_{NLC}|_{\mathrm{dBm}} = -97\,\mathrm{dBm} \tag{3.1.3}$$

This determines an IIP3 calculated as

$$IIP3_{min} = \frac{(P_{CW} - ISO) + 2\,(P_{TX} - ISO) - IM3_{min}}{2} = 8\,\mathrm{dBm} \tag{3.1.4}$$

Here, $P_{CW} = -15\,\mathrm{dBm}$ represents the power level of the closest continuous wave (CW) [29], $P_{TX} = 27\,\mathrm{dBm}$ is the maximum transmitter output power and $ISO = 40\,\mathrm{dB}$ is the insertion loss in the receiver bandwidth.

3.1.2 Translational feedback receiver

Two translational feedback front-end topologies proposed in the literature are depicted in Figure 3.1.1. Figure 3.1.1a shows the architecture proposed in [45] featuring a negative translational feedback loop that reduces the input impedance. This design has the potential to significantly decrease the power consumption of the Low Noise Transconductance Amplifier (LNTA) while relaxing the linearity requirements of the baseband filter. However the high OOB input impedance may lead to compression linearity issues in the front-end due to substantial voltage swings. Furthermore, the flexible and well-controlled loop gain, directly determined by the feedback resistance R_{FB}, is a notable advantage of this approach.

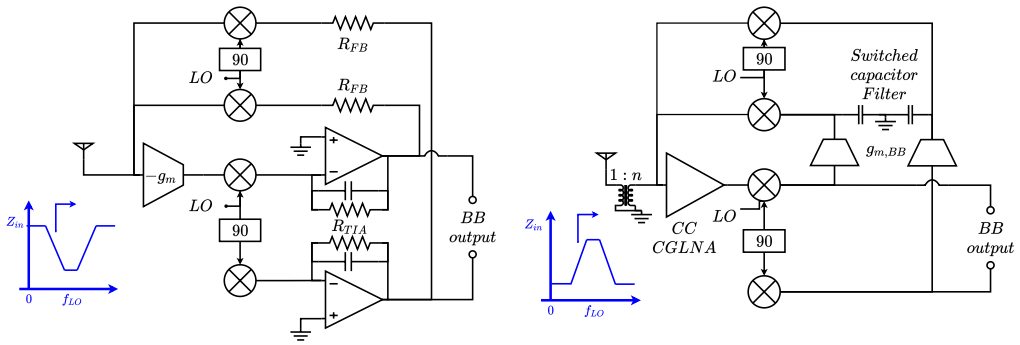


Figure 3.1.1: Negative (a) and positive (b) translational feedback loop proposed respectively in [45, 46]

On the right side, the schematic presented in [46] (Figure 3.1.1b) adopts a positive translational feedback loop, resulting in an increase in input impedance. This configuration is advantageous for enhancing OOB linearity, although at the expense of reduced baseband gain. Additionally, an enhanced filtering effect is achieved through a switched capacitor filter of higher order.

Figure 3.1.2 shows the block diagram of the proposed Main receiver, where the output current of a Low Noise Transconductance Amplifier (LNTA) is down-converted to the baseband (BB) transimpedance amplifier (TIA), which provides a low impedance termination of the mixer, I-V conversion of the RF current and pseudo-second order filtering. The output voltage is then converted into current by the complex feedback impedance Z_{FB}, which also provides the translational feedback loop gain. The feedback current is then

up-converted and fed into the input of the LNTA.

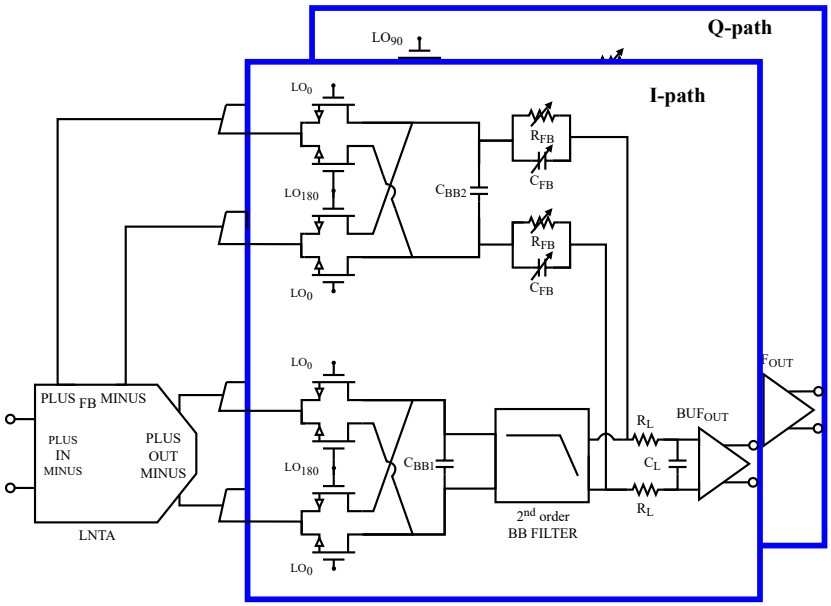


Figure 3.1.2: Block schematic of the proposed feedback front-end receiver

3.2 Circuit Analysis

Positive feedback mechanisms, as discussed in [45], significantly affect system performance, particularly in terms of input impedance. A comprehensive analysis of noise and linearity in relation to feedback parameters is provided in [46]. This analysis not only discusses theory but also explores the practical implications of varying feedback parameters on system metrics.

To streamline the analysis of input matching, noise characteristics and receiver linearity, it is introduced a simplified and more intuitive approach, providing a step-by-step breakdown of the methodology employed. Practical examples and plots will be used to explain key concepts, ensuring a clear understanding of the proposed architecture.

3.2.1 Input Impedance

It is now considered the basic case shown in Figure 3.2.1, where the transconductance load current I_{RF} results from the sum of an input current I_S and

a feedback current I_{FB}, all assumed to be in phase. Assuming $I_{FB} = \beta H(s) \cdot I_{RF}$, the input impedance Z_{IN} is given by

$$Z_{IN} = \frac{1}{gm \cdot (1 - \beta H(s))} \tag{3.2.1}$$

For simplicity, $H(s)$ is modeled as a first-order low-pass filter with a cutoff frequency of ω_p. This allows expressing the feedback current as

$$I_{FB} = \frac{\beta I_{RF}}{1 + s/\omega_p} \tag{3.2.2}$$

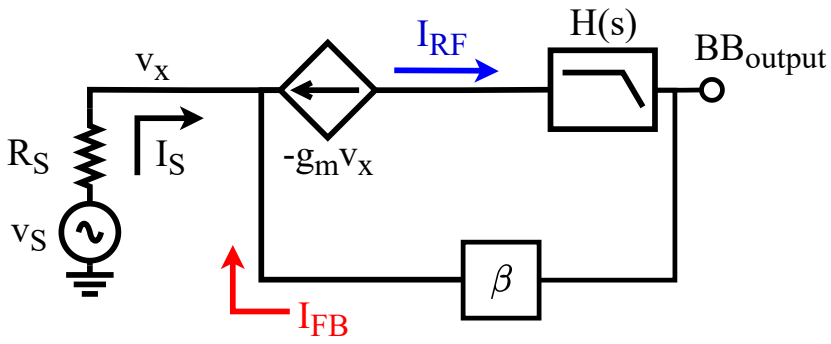


Figure 3.2.1: Simplified translational loop LTI model

The resulting input impedance and admittance are

$$Z_{IN} = \frac{1}{(1-\beta)g_m}\frac{1 + s/\omega_p}{1 + s/\omega_z} \quad Y_{IN} = (1-\beta)g_m\frac{1 + s/\omega_z}{1 + s/\omega_p} \tag{3.2.3}$$

where $\omega_z = (1 - \beta)\omega_p$.

Considering that the matching condition requires

$$Y_s = \frac{1}{R_S} = g_m\,(1 - \beta) \tag{3.2.4}$$

the reflection coefficient Γ can be express as

$$\Gamma = \frac{Y_{IN} - Y_s}{Y_{IN} + Y_s} = \frac{\beta/2}{1 - \beta/2} \cdot \frac{s}{\omega_{LP}} \cdot \frac{1}{\frac{s}{\omega_{LP}} + 1}, \tag{3.2.5}$$

where

$$\omega_{LP} = \frac{2\omega_p\omega_z}{\omega_p + \omega_z} = \omega_p\frac{1 - \beta}{1 - \beta/2}. \tag{3.2.6}$$

From Equation 3.2.5 is obtained the Out-Of-Band reflection coefficient Γ_{HF} as

$$\Gamma_{HF} = \frac{\omega_p - \omega_z}{\omega_p + \omega_z} = \frac{\beta/2}{1 - \beta/2}. \tag{3.2.7}$$

The best baseband bandwidth and Out-Of-Band (OOB) mismatch requirements can be determined as a function of the input transconductance and the width of the input impedance matching by exploiting Equations 3.2.5 and 3.2.6.

A noteworthy finding that emerged from Equation 3.2.7 is that a perfect broadband matching can be obtain imposing $\Gamma_{HF} = 1/3$ by fixing the ratio between ω_{LP} and ω_p as

$$\frac{\omega_{LP}}{\omega_p} = \sqrt{9\left(\frac{\beta/2}{1 - \beta/2}\right)^2 - 1}. \tag{3.2.8}$$

The analysis progresses to the scenario where $H(s)$ represents a second-order low-pass filter with a cutoff frequency of ω_p and a quality factor Q. In this context, the expression for the feedback current becomes

$$I_{FB} = \frac{\beta I_{RF}}{s^2/\omega_p^2 + s/(Q\omega_p) + 1}. \tag{3.2.9}$$

The reflection coefficient, as derived in Equation 3.2.10, includes the increased complexity of a second-order filter. The parameters ω_{LP} and Q_{LP} are defined in Equation 3.2.11.

$$\begin{aligned} \Gamma = \frac{Y_{IN} - Y_s}{Y_{IN} + Y_s} &= \frac{\beta/2}{1 - \beta/2} \cdot \frac{s}{\omega_p} \frac{\frac{s}{\omega_p} + \frac{1}{Q}}{\frac{s^2}{{\omega_p}^2} + \frac{s}{\omega_p Q} + \frac{1-\beta}{1-\beta/2}} \\ &= \frac{\beta/2}{1 - \beta} \cdot \frac{s}{\omega_p Q} \cdot \frac{s\frac{Q}{\omega_p} + 1}{\frac{s^2}{{\omega_{LP}}^2} + \frac{s}{\omega_{LP} Q_{LP}} + 1} \end{aligned} \tag{3.2.10}$$

$$\omega_{LP} = \omega_p \sqrt{\frac{1 - \beta}{1 - \beta/2}} \qquad Q_{LP} = Q \sqrt{\frac{1 - \beta}{1 - \beta/2}} \tag{3.2.11}$$

From Equation 3.2.10, the OOB reflection coefficient with a second-order feedback loop is expressed as

$$\Gamma_{HF} = \frac{\beta/2}{1 - \beta} \cdot \frac{\omega_{LP}^2}{\omega_p^2} = \frac{\beta}{1 + \beta/2}. \tag{3.2.12}$$

In Figure 3.2.2, an ideal simulation using Cadence Virtuoso® is compared with an analytical calculation in MATLAB®. The comparison considers $\beta = 0.7$ and a closed-loop cutoff frequency of $\omega_{LP} = 10\,MHz$ with $Q_{LP} = 1/\sqrt{2}$. The results reveal that utilizing a second-order filter leads to increased mismatch in the specified frequency band.

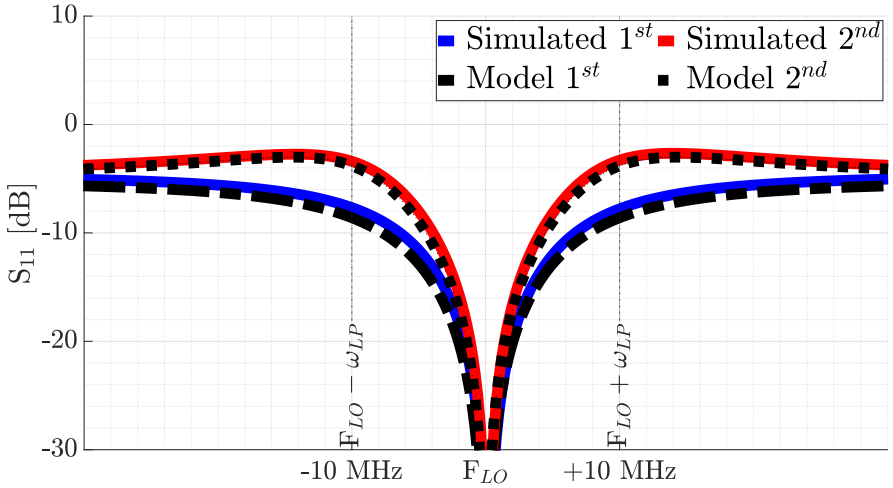


Figure 3.2.2: Representation of an ideal S_{11} with a 1st order filter (blue) and a 2nd order filter (red)

3.2.2 Transfer Function

The LTI equivalent schematic is derived from the block diagram presented in Figure 3.2.3, exploiting the mixer model proposed in [47]. For the sake of simplicity, the resistances of the mixer and the capacitors C_1 and C_2 are assumed to be negligible within the frequency band of interest.

Considering a low-pass BB filter described by the transfer function

$$H(s) = \frac{R_{BB}}{s/\omega_p + 1} \tag{3.2.13}$$

it is possible to derive the analytical expression of the transfer function from v_s to v_{out} as follows

$$\frac{v_{out}}{v_s}(s) = \frac{\gamma R_{BB}}{2R_S(1-\beta)} \frac{1}{s/\omega_{LP} + 1} \tag{3.2.14}$$

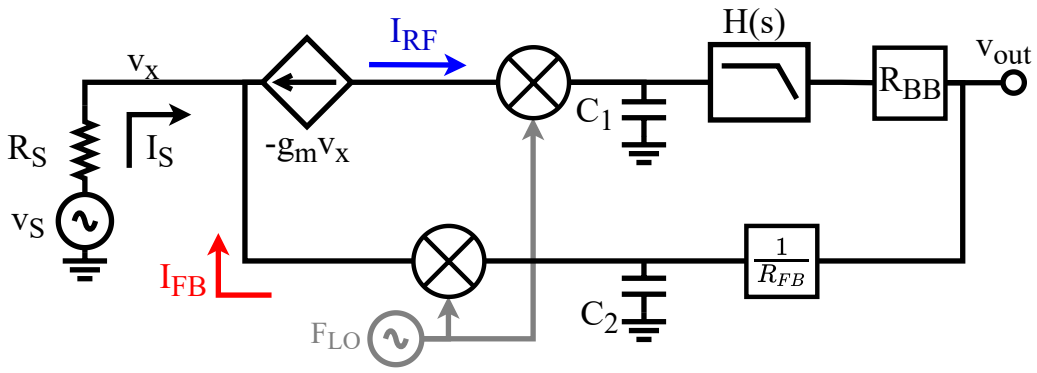


Figure 3.2.3: Simplified schematic of the proposed positive feedback receiver

For a second-order filter, the expression is given by

$$\frac{v_{out}}{v_s}(s) = \frac{\gamma R_{BB}}{2R_S(1-\beta)} \frac{1}{\frac{s^2}{\omega_{LP}{}^2} + \frac{s}{\omega_{LP}Q_{LP}} + 1} \tag{3.2.15}$$

with $\gamma = 4/\pi^2$ and ω_{LP} and Q are defined in Equations 3.2.6 and 3.2.11.

In the initial approximation, β can be estimated as R_{BB}/R_{FB}. However, the actual equation is more complex. A detailed differential mixer model is available in Appendix A and a comprehensive calculation is provided in Appendix B.

A comparison is illustrated in Figure 3.2.4 between the simulated and calculated v_{out} considering Equation 3.2.14 and Equation 3.2.15 with $\omega_{LP} = 10\,MHz$ and $Q_{LP} = 1/\sqrt{2}$.

3.2.3 Frequency dependent feedback

The comparison between a first-order baseband filter and a second-order filter highlights the trade-off between achieving linearity performance and input matching impedance. The question arises: can this compromise be avoided?

Considering the frequency-dependent parameter $\beta(s) = \beta_0(1 + s/\omega_p)$ shown in Figure 3.2.1, Equation 3.2.5 and Equation 3.2.14 are transformed as follows:

$$\Gamma = \frac{Y_{IN} - Y_s}{Y_{IN} + Y_s} = \frac{g_m(1-\beta_0) - g_m(1-\beta_0)}{2g_m(1-\beta_0)} = 0 \tag{3.2.16}$$

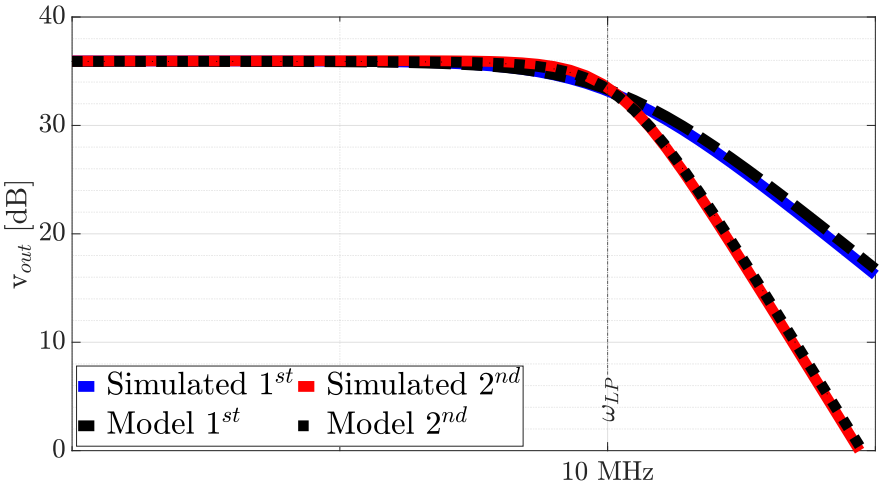


Figure 3.2.4: Comparison between the simulated and calculated v_{out} with a 1^{st} order filter (blue) and a 2^{nd} order filter (red)

and

$$\frac{v_{out}}{v_s}(s) = \frac{\gamma R_{BB}}{2R_S(1-\beta_0)} \frac{1}{s/\omega_p + 1} \tag{3.2.17}$$

This configuration achieves broadband matching while maintaining the same closed-loop bandwidth.

Advancing the analysis, as done in the previous section, it is considered $H(s)$ as second-order low-pass filter with a cutoff frequency of ω_p and a quality factor Q described by the equation

$$H(s) = \frac{1}{s^2/\omega_p^2 + s/(Q\omega_p) + 1} \tag{3.2.18}$$

with frequency-dependent $\beta(s) = \beta_0(1 + s/\omega_p)$.

The Equation 3.2.10 and Equation 3.2.15 become now

$$\Gamma = \frac{\beta_0/2}{1-\beta_0} \cdot \frac{s(1-Q)}{\omega_p Q} \cdot \frac{s\frac{Q}{\omega_p(1-Q)} + 1}{\frac{s^2}{{\omega_{LP}}^2} + \frac{s}{\omega_{LP}Q_{LP}} + 1} \tag{3.2.19}$$

and

$$\frac{v_{out}}{v_s}(s) = \frac{\gamma R_{BB}}{2R_S(1-\beta_0)} \frac{1}{\frac{s^2}{{\omega_{LP}}^2} + \frac{s}{\omega_{LP}Q_{LP}} + 1} \tag{3.2.20}$$

where

$$\omega_{LP} = \omega_p \sqrt{\frac{1-\beta_0}{1-\beta_0/2}} \qquad Q_{LP} = \frac{Q}{1+Q\beta_0/(2\beta_0-1)} \sqrt{\frac{1-\beta_0}{1-\beta_0/2}} \tag{3.2.21}$$

Figure 3.2.5 presents a comparison between simulated and calculated S_{11}, considering Equation 3.2.19 with $\omega_{LP} = 10\,MHz$ and $Q_{LP} = 1/\sqrt{(2)}$.

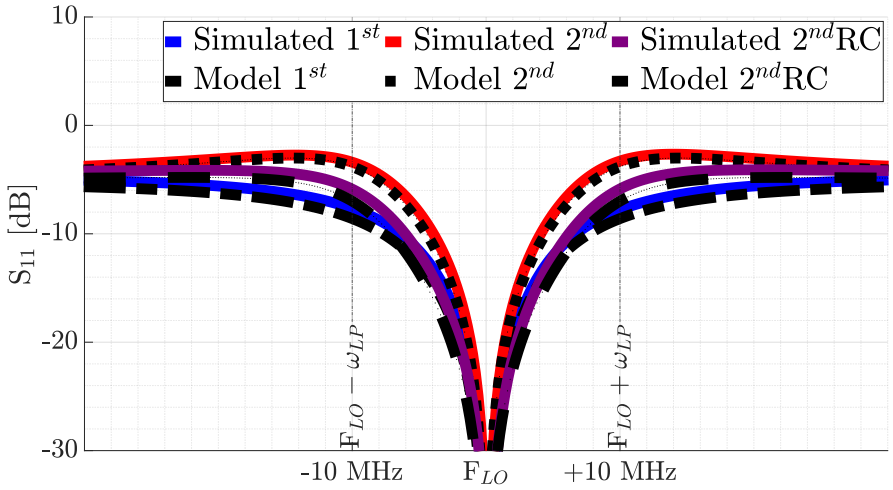


Figure 3.2.5: Ideal S_{11} with a 1st order filter (blue), 2nd order filter (red) and 2nd order filter with a zero added in the feedback (purple)

It is important to note that, by appropriately selecting values for ω_p and Q, the transfer function doesn't change. The S_{11} plot exhibits characteristics between those of a first-order and second-order shaping, allowing the achievement of a second-order filtering effect. Consequently, the desired input impedance can be obtained by carefully choosing the appropriate values of ω_p, Q and β_0.

Figure 3.2.6a and 3.2.6b show the root locus of Equation 3.2.15 and 3.2.20 respectively, as a function of the factor β.

3.2.4 Noise analysis

In this section, the noise model for the translational positive receiver is presented. The schematic shown in Figure 3.2.7 illustrates the primary contri-

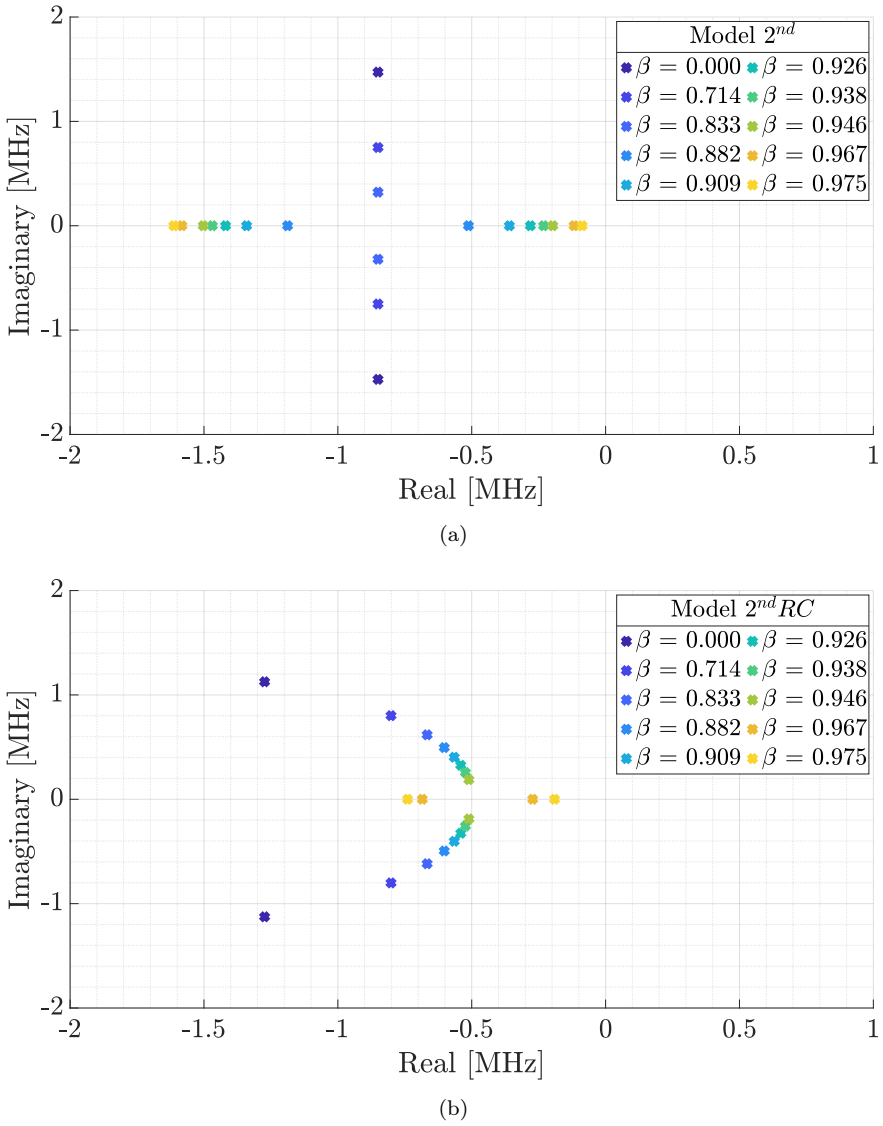


Figure 3.2.6: Root locus foi 2nd order filter (a) and 2nd order filter with a zero added in the feedback (b)

butions, with the noise factor F calculated by considering all noise sources as white noise.

The transfer function of the system from v_s to v_{out} is given by

$$\frac{v_{out}}{v_s} = \frac{R_{BB}}{2R_s\,(1-\beta)} = A_v \tag{3.2.22}$$

This analysis assumes negligible the noise contribution from harmonic mixing caused by mixers. Additionally, it is assumed that noisy devices

exhibit no frequency dependency.

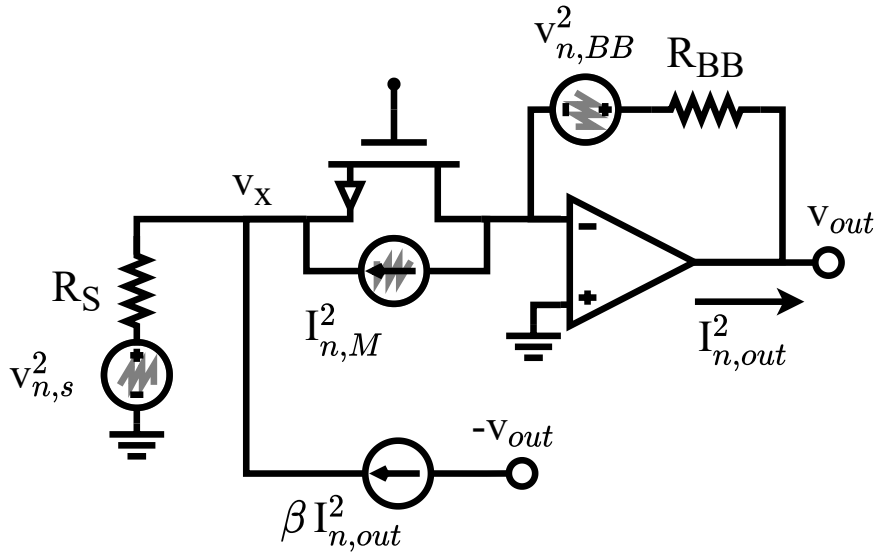


Figure 3.2.7: Simplified noise schematic of the proposed positive feedback receiver

The noise factor is defined as

$$F = \frac{v^2_{n,out,R_s} + v^2_{n,out,MOS} + v^2_{n,out,R_{BB}}}{v^2_{n,out,R_s}} \tag{3.2.23}$$

From the schematic shown in Figure 3.2.7, three primary contributors are considered: the contribution from the source resistance v_{n,out,R_s}, the noise contribution from the LNA $v_{n,out,MOS}$, modeled as a common-gate MOSFET and the one originating from the baseband $v_{n,out,R_{BB}}$, as described in the following equation

$$\begin{aligned} v^2_{n,out,R_s} &= 4kTR_SA^2_v \\ v^2_{n,out,MOS} &= \frac{4kT\gamma g_m R^2_{BB}}{(g_m R_S(1-\beta)+1)^2} \\ v^2_{n,out,R_{BB}} &= 4kTR_{BB} \end{aligned} \tag{3.2.24}$$

where $k = 1.38 \cdot 10^{-23}\,\mathrm{J/K}$ represents the Boltzmann constant, T is the absolute temperature and γ is the MOSFET coefficient dependent on the basic transistor parameters and bias conditions.

Substituting the results from Equation 3.2.24 into Equation 3.2.23, the noise factor becomes

$$F = 1 + \frac{4\gamma g_m R_S \left(1-\beta\right)^2}{\left(g_m R_S(1-\beta)+1\right)^2} + \frac{4R_s}{R_{BB}}\left(1-\beta\right)^2 \tag{3.2.25}$$

Applying the matching condition from Equation 3.2.4 ($g_m R_S = 1/(1-\beta)$), the expression of the noise factor results in

$$F = 1 + \frac{\gamma}{2}\left(1-\beta\right) + \frac{4R_s}{R_{BB}}\left(1-\beta\right)^2 \tag{3.2.26}$$

As shown in Equation 3.2.26, a higher loop gain results in lower receiver noise. While reducing the Noise Figure is desirable, it's crucial to assess the system's stability margins. Balancing noise reduction with stability forms a critical aspect of receiver design, requiring an in-depth analysis to find an optimal solution.

3.2.5 Third-order intercept point

In order to evaluate the linearity of the receiver, it is considered the Linear Time-Invariant (LTI) model of the receiver shown in Figure 3.2.8, 3.2.9 and 3.2.10. The in-band nonlinearity is examined under the assumption that the linearity limit is determined only by the Low Noise Amplifier (LNA). Additionally, it is assumed that the transistor exhibits only third-order nonlinearity.

The coefficient α_1 is determined considering the schematic in Figure 3.2.8. Under the matching condition $R_S \cdot g_m = 1/(1-\beta)$ (Equation 3.2.4), the value of α_1 is calculated as

$$\alpha_1 = \frac{H(s)}{2R_S(\beta-1)} \tag{3.2.27}$$

A third-order nonlinearity ($g_{m3}(v_s)^3$) is injected, as illustrated in Figure 3.2.9. Assuming two in-band tones at frequencies f_1 and f_2 with $2f_1 - f_2$ also falling in-band, the inter-modulation tone experiences input matching. The value of α_{3IB} is derived as

$$\alpha_{3IB} = \frac{g_{m3}H(s)}{2} \tag{3.2.28}$$

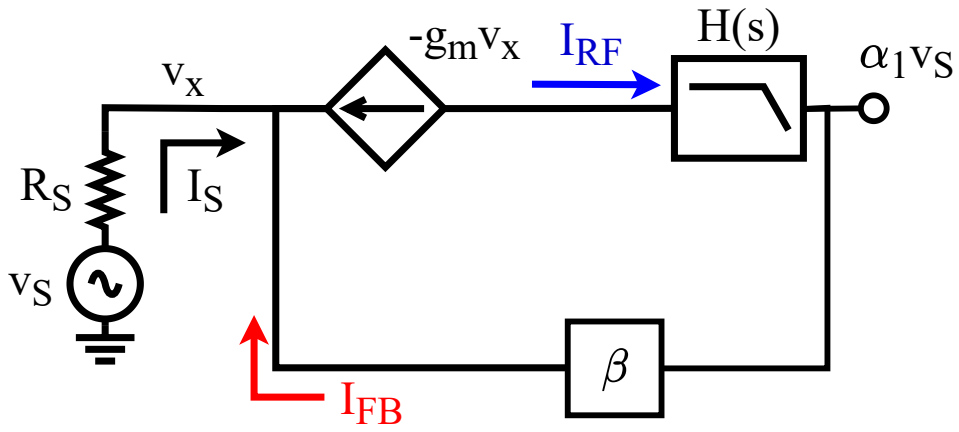


Figure 3.2.8: Simplified translational loop LTI model to compute third-order nonlinearity

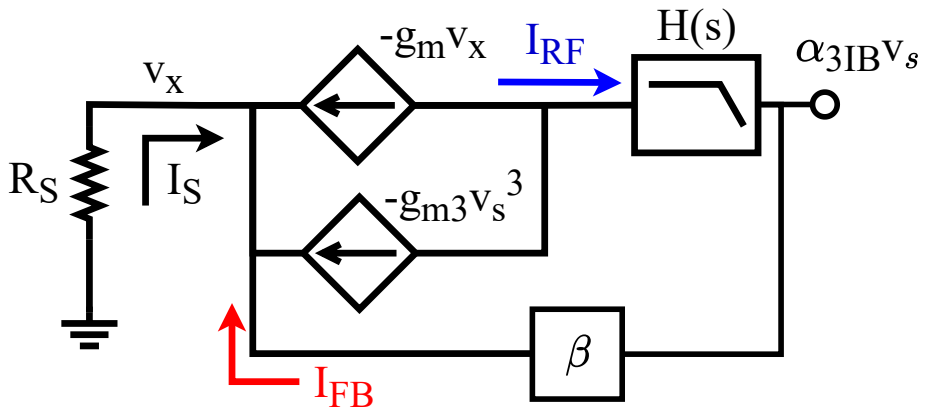


Figure 3.2.9: Simplified translational loop LTI model to compute the in-band third-order nonlinearity

To determine the IIP_3 the Equation 3.2.29 [1] to the results shown in Equation 3.2.27 and 3.2.28

$$|\alpha_1 A_{IIP3}| = \left|\frac{3}{4}\alpha_3 A_{IIP3}^3\right| \tag{3.2.29}$$

obtaining in-band IIP3 as

$$A_{IB-IIP3} = \sqrt{\frac{4}{3}\frac{g_m}{g_{m3}}} = \sqrt{\frac{4}{3}\frac{1}{g_{m3}R_S(1-\beta)}} \tag{3.2.30}$$

For the out-of-band IIP3 calculation, it is considered the two tones f_1 and f_2 to be outside the band and the third-order intermodulation $(2f_1 - f_2)$ falls

in-band. Assuming that at the frequencies f_1 and f_2 the positive feedback is inactive due to being far from the cut-off frequency of the baseband filter, the coefficient α_3 is calculated in Equation 3.2.31 with $I_{FB} = 0$:

$$\alpha_3 = g_{m3}\frac{1-\beta}{2-\beta}H(s)A^3_{OOB-IIP3} \tag{3.2.31}$$

The out-of-band IIP3 is then obtain from Equation 3.2.29 as

$$A_{OOB-IIP3} = \sqrt{\frac{4}{3}\frac{g_m}{g_{m3}}\frac{1-\beta/2}{1-\beta}} = \sqrt{\frac{4}{3}\frac{1}{g_{m3}R_s}\frac{1-\beta/2}{(1-\beta)^2}} \tag{3.2.32}$$

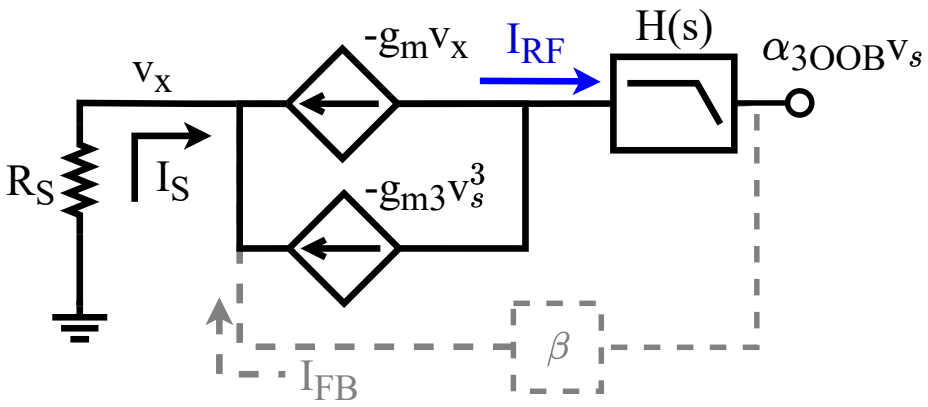


Figure 3.2.10: Simplified translational loop LTI model to compute the out-of-band third-order nonlinearity

3.3 Low Noise Transconductance Amplifier

Figure 3.3.1 illustrates the schematic of the cross-coupled common gate LNTA. The input signal, differentially applied to IN_{PLUS} and IN_{MINUS}, is directly fed into the sources of the NMOS transistors and it is capacitively coupled to the sources of the PMOS transistors and to the gates of the four input transistors through capacitors C_P and C_C, respectively.

The feedforward capacitance managed to obtain roughly two-fold reduction in transconductance (g_m) while also reducing noise by a comparable amount [1].

The differential feedback signal from the up-conversion mixers (FB_{PLUS} and FB_{MINUS}) is capacitively coupled to the sources of both NMOS and

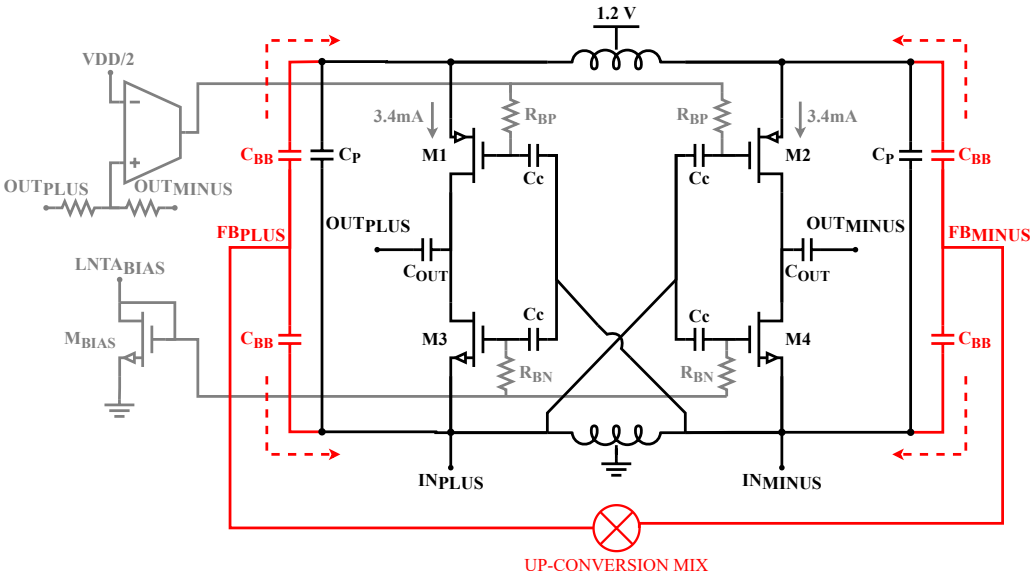


Figure 3.3.1: Detailed LNTA schematic

PMOS transistors through C_{BB}. In particular, large tail inductors (7.5 nH) are employed to resonate the input impedance around 2 GHz. The use of inductor degeneration facilitates voltage swings both above and below the supply, enabling class AB operation and low-noise biasing.

The selection of a low-quality factor for the matching network, achieved through the use of large inductors and small capacitors, is crucial for optimal noise performance, as extensively analyzed in [46].

The output nodes OUT_{PLUS} and OUT_{MINUS} receive the sum of the input signal current and the feedback current. These nodes are AC-coupled with the down-conversion mixer.

To strike a balance between parasitic capacitance and output conductance, a non-minimum gate length of 60 nm is chosen. Both factors significantly influence noise and distortion attributable to the transimpedance amplifiers (TIAs). DC biasing is achieved through a common-mode feedback circuit implemented using a single-stage self-biased Operational Transconductance Amplifier (OTA). The overall current consumption of the LNTA stage is 7.2 mA from a 1.2 V voltage supply. The biasing is adjustable through the current mirror M_{BIAS}. In order to evaluate the performance advantage given by the positive feedback architecture, the receiver is simulated, assum-

Instance	Value	Unit
M1/2	115.2/0.06	$\mu m/\mu m$
M3/4	115.2/0.06	$\mu m/\mu m$
C_P	4	pF
C_C	655	fF
C_{BB}	200	fF
C_{OUT}	3.2	pF
L_{choke} (diff)	15	nH
$R_{BP/N}$	100	$k\Omega$

Table 3.3.1: Design parameters for the LNTA

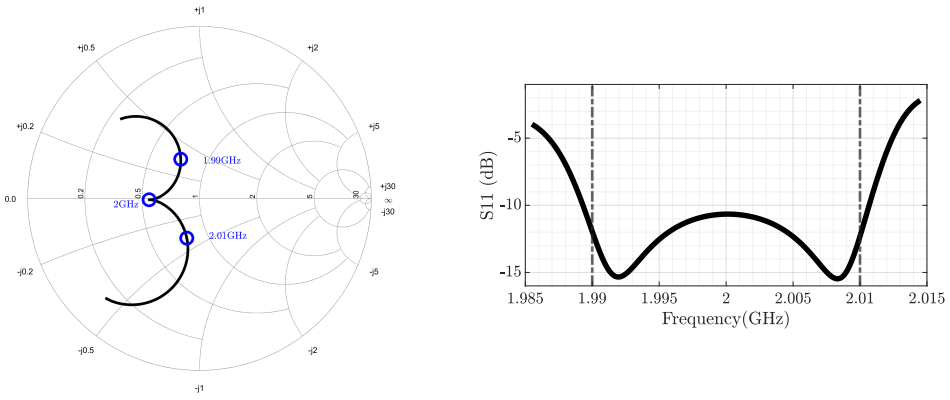
ing ideal blocks for all components except the LNTA.

As previously discussed, the use of inductor degeneration enables the achievement of a 10 dBm compression point. This point is reached when the output nodes, OUT_{PLUS} and OUT_{MINUS}, approach the rail-to-rail voltage. The LNTA emerges as the primary bottleneck affecting the out-of-band third-order intercept point (OOB IIP3) of the receiver, achieving a value of 20 dBm.

Following the considerations presented in Section 3.2.3, the decision is made to intentionally deviate from a perfect 50 Ω differential impedance match for the input impedance. As depicted in Figure 3.3.2, when all receiver components are assumed ideal except the LNTA, the S_{11} parameter exhibits two notches. These notches are a consequence of the Q factor of the baseband filter being higher than $1/\sqrt{2}$. This compromise results in a reduction in inband matching, but it yields advantages in terms of out-of-band linearity and matching bandwidth, as described in Section 3.2.5.

3.4 Down/up-conversion passive mixers

The I and Q down-conversion and up-conversion mixers are implemented as passive switches. This architecture is chosen for his low complexity design and zero bias current which provides a low flicker noise because there is no DC current in switch-pair [48]. Passive switches give a conversion current effi-



(a) (b)

Figure 3.3.2: Simulated LNTA S_{11} considering ideal receiver exept for the LNTA. The implementation of the notches helps to keep a matching bandwidth over 20 MHz

ciency equal to $2/\pi$ [49], while a detailed differential mixer model is available in Appendix A.

This architecture enhances the mixer's linearity. The absence of any voltage swing across the switching transistors indicates the absence of any signal across the nonlinear capacitors at the switching pairs' input. In reality, charging and discharging nonlinear capacitances can have a significant influence on the linearity of the receiver, which, ideally, should depend only on the LNTA [50]. Larger MOS transistors in the mixer can achieve a better linearity as shown in Figure 3.4.2 resulting in larger overlap capacitances and hence larger RF drain currents which could lead to an increasing in its noise contribution [51].

The I and Q down-conversion and up-conversion mixer switches are biased with a V_{GS}=0.75 V and driven by a single frequency divider working off a 1 V supply. The down-conversion mixer switches are low threshold voltage NMOS in order to reduce the resistance R_{swdc}=25 Ω, while the up-conversion mixer switches have a resistance of $R_{swuc} = 140\,\Omega$. The shunt capacitor C_{BB1} is implemented as 14 pF single-ended and 6 pF differential while C_{BB2} is 1 pF.

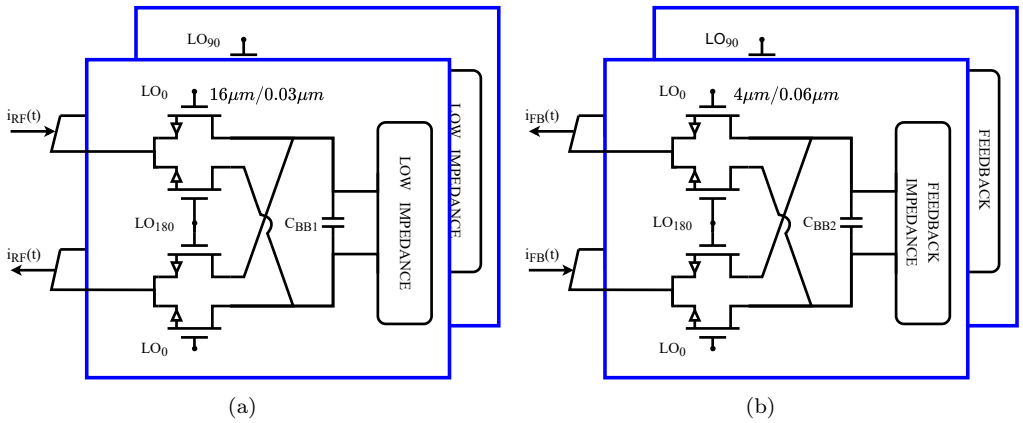


Figure 3.4.1: Main receiver down-conversion (a) and up-conversion (b) mixers schematic.

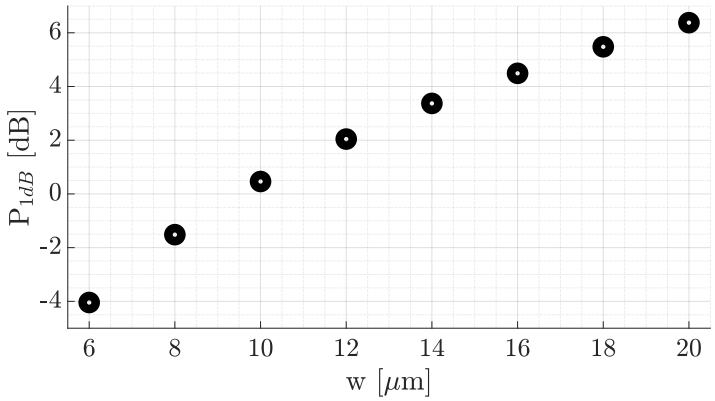


Figure 3.4.2: P_{1dB} of the down-conversion mixer as a function of mixer's switches

3.5 Base-Band Filter

In the current-mode receiver architecture, the first block after the passive mixer is either a filtering trans-impedance amplifier (TIA) or a higher order filter [52–54]. This stage must have a good OOB linearity not to limit the receiver IIP3 and also it has to show low input impedence not to degrade linearity of the LNTA. To achieve these targets, an also a good input referred noise, the architecture shown in Figure 3.5.1 is proposed.

The base-band filtering TIA is implemented with three CMOS inverter-based integrators with multi-loop feedback. A virtual ground is created at the TIA input, making the TIA bandwidth, gain and poles quality factor independent of the LO frequency. The first stage, which is an integrator,

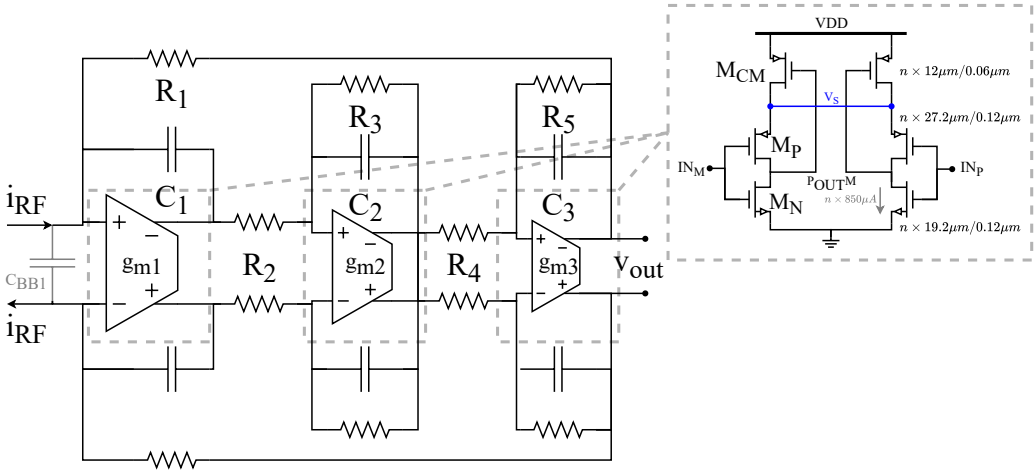


Figure 3.5.1: Main receiver baseband filter schematic

should have a high gain (small C_1) in order to make the noise contribution of the following stages negligible. However, the first stage absorbs most of the down-converted OOB blockers current through capacitor C_1. A large C_1 is therefore desirable to reduce the voltage swing and the distortion introduced by the first stage due to large OOB blockers. Hence, the value of C_1 was chosen as a compromise between noise and linearity.

The input impedance of the TIA increase as the frequencies does because of the decreasing of the stages' gain. This effect could be mitigated with the shunt capacitor C_{BB1} which provides low impedance path for high frequency components. Besides shunting the signal at the clock harmonics, C_{BB1} maintains low input impedance across frequency to preserve both mixer IIP2 and IIP3 with strong OOB interferers [55] and it filters the higher frequency down converted interferers, improving TIA OOB IIP3 [56].

The feedback resistor R_1 can be chosen once defined the desired gain. The time constants of the second and third stages (τ_2 and τ_3) allow to set the poles at the desired frequency, while resistors R_4 and R_5 control the quality factor of the complex poles. The DC gain and unity-gain frequencies of the second and third stages were set to 4 and 100 MHz and 2 and 160 MHz respectively. This ensures that in-band distortion is limited by the third stage, which sees the largest voltage swing.

As the interferers frequency increase, IIP3 improves quickly thanks to

the second-order frequency response. A further improvement is introduced above 80 MHz by the real pole. Assuming perfectly linear components in the LNTA and mixers, the receiver OOB IIP3 reaches a value of 31 dBm at 80 MHz offset frequency, limited by the TIA. The power consumption ratio of the three stages is n = 4 : 2 : 1, resulting in a total power consumption of 28.6 mW I and Q.

Instance	Value	Unit
R_1	3.45	$k\Omega$
R_2	1	$k\Omega$
R_3	4	$k\Omega$
R_4	2	$k\Omega$
R_5	4	$k\Omega$
C_1	12	pF
C_2	1.7	pF
C_3	0.5	pF

Table 3.5.1: Design parameters for the Main receiver baseband filter

The structure of each inverter stage is the same presented in [2, 35]. The inverter-based BB TIA architecture is chosen because it offers low noise with good power efficiency [57] and also doesn't require any extra common-mode feedback (CMFB), avoiding any extra noise or power consumption.

This circuit shows a differential gain of $(g_{mN}+g_{mP})\cdot(r_{oN}//r_{oP})$ and a common mode gain of g_{mN}/g_{mCM}, where $g_{m\_}$ and $r_{o\_}$ are the transcondactance and the output impedance of the mosfets M_{CM}, M_P and M_N [2].

It has been shown that by sizing the PMOS and NMOS devices such that their transconductances are equal, IIP2 is improved through push-pull drive and IIP3 through local distortion cancellation [58, 59].

The transfer function of the third order filter is:

$$\frac{v_{out}}{i_{in}} = \frac{R_1}{s^3\tau_1\tau_2\tau_3 + s^2\tau_1\left(\tau_2/A_3 + \tau_3/A_2\right) + s\tau_1/(A_2A_3) + 1} \tag{3.5.1}$$

$$\tau_1 = R_1 \cdot C_1 \quad \tau_2 = R_2 \cdot C_2 \quad \tau_3 = R_4 \cdot C_3$$

$$A_2 = R_3/R_2 \quad A_3 = R_5/R_4$$

3.6 Measurement Results

The proposed Main receiver prototype was fabricated in a TSMC 28 nm CMOS process and the chip photograph is reported in Figure 3.6.1. The area is 0.360 mm^2 and it is mostly occupied by the two choke inductors of the LNTA.

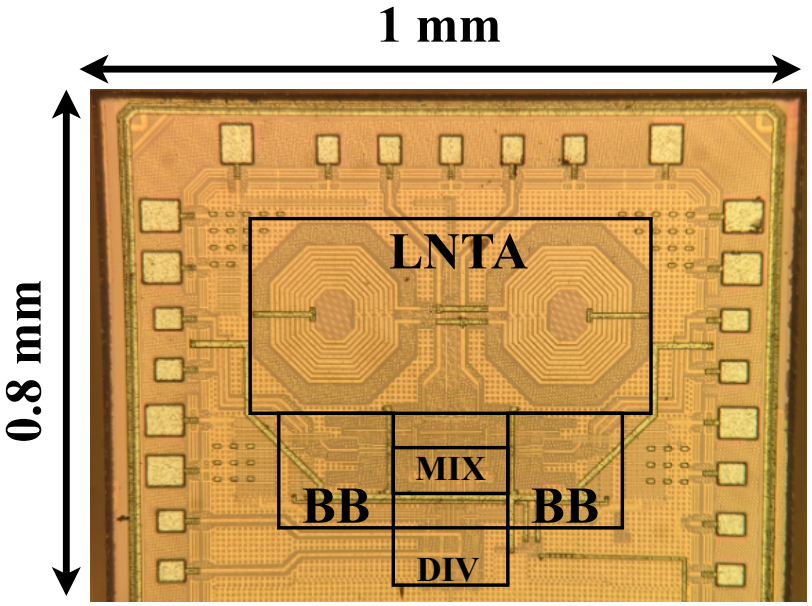


Figure 3.6.1: Main receiver chip photograph [60]

Figure 3.6.2 shows the measured and simulated S_{11} at 2 GHz. The plot is obtained probing directly the pad of the chip. The plot shows a S_{11} slightly below −10 dB over a RF bandwidth of 17 MHz also resulting in an S_{11} that is unbalance between frequencies on the left and on the right of the carrier. This issue can be fixed mixing the I and Q path with a crossing resistance [61].

Figure 3.6.3 shows the measurement setup. The chip is bonded on PCB and two on-board baluns are mounted to convert the signal from single-ended to differential. The output is detected with a *LeCroy AP033* active differential probe which is connected to the onboard pinhead. The losses of the measurement setup including 1:1 off chip balun, PCB traces and cables are de-embadded from the plot presented in this section.

The Main receiver frequency response is shown in Figure 3.6.4. It shows

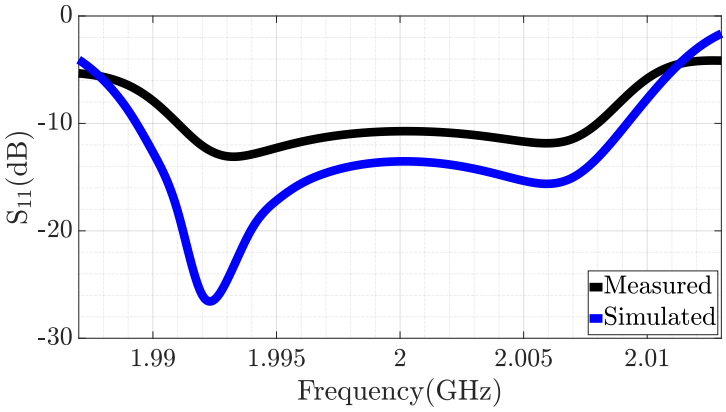


Figure 3.6.2: Main receiver measured and simulated S_{11}

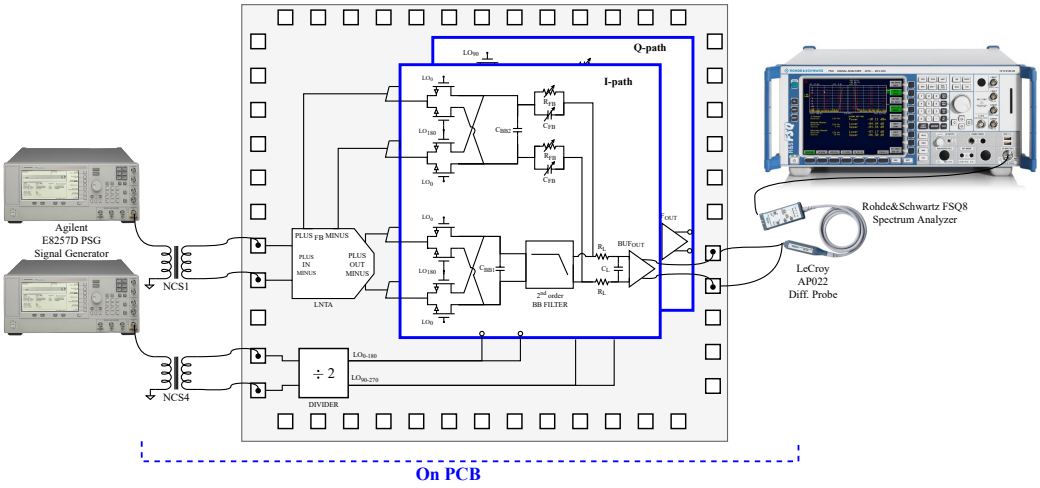


Figure 3.6.3: Main receiver simplified measurement setup. Where needed (compression measurement, NF expansion measurement...) the input signal is first combined and then sent to the PCB

14 MHz cut of frequency and more than 40 dB gain. The high filtering order is due to the third pole in the third stage of the baseband filter and the RC low-pass filter at the input of the output buffer which also help at reducing the picking of the transfer function.

The integreted Double Side-Band Nose Figure (NF_{dsb}) (Figure 3.6.5) over 10 MHz bandwidth is 3.3 dB. It is measured with 20 dB probe gain to overcome the spectrum analyzer's noise and reduce the loading parasitic capacitance of the probe. Table 3.6.1 shows the simulated noise breakdown. Considering the noise contribution from the port, the excess of noise is due to the

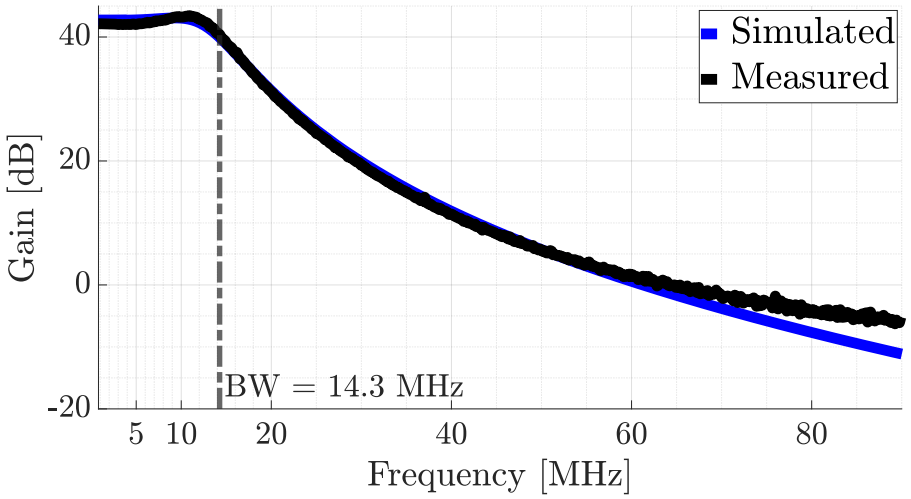


Figure 3.6.4: Main receiver transfer function with 2 GHz frequency carrier

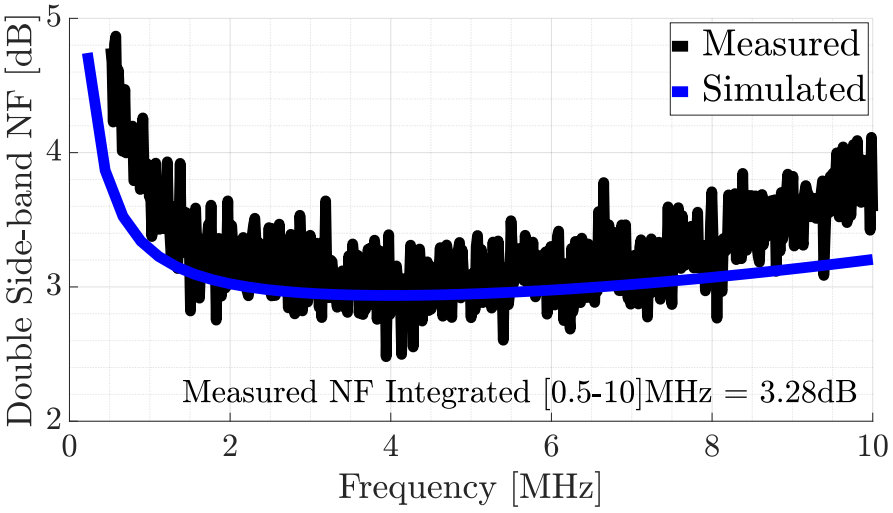


Figure 3.6.5: Main receiver Noise Figure with 2 GHz frequency carrier

folding effect. At the band-edge the gain of the first stage of the baseband filter start to decreased and so the noise of the following stages start to ramp up, increasing the overall noise figure, as shown in Figure 3.6.5.

The In-Band (IB) small-signal gain compression is measured combining an interferer at 2.085 GHz ($\Delta f/\omega_{\text{3-dB}} = 6$ respect to LO) through *Suhner 4901 19.a* power combiner with a small IB signal. Figure 3.6.6 shows the 1 dB compression point (P1dB) of the Main receiver. From the reported plot

Block	Noise Factor @2 MHz	Noise Factor @5 MHz	Noise Factor @10 MHz
PORT	68%	69%	66%
LNTA	15%	15%	14%
BB-FILT	6%	6%	10%
MIXERs	7%	7%	7%
OTHERS	4%	3%	3%

Table 3.6.1: Main receiver noise breakdown

it is visible that P1dB = −2 dBm is achieved, which is 5 dB higher than the target TX leagage interferer plus 6 dB peak-to-average power ratio (PAPR). The gain compression is mainly due to the baseband filter, as discussed in Section 3.5

As discussed in Section 1.1.4, reciprocal mixing effect increases the noise spectrum at the IF frequency when a strong unwanted signal is present. The Noise Figure expansion is tested measuring the output noise spectrum with a OOB blocker at 85 MHz ($\Delta f/\omega_{3\text{-dB}} = 6$) offset frequencies (with respect to LO). In order to decouple the phase noise of the instruments from the one of the on-chip divider, the input LO signal and the blocker are filtered with a Cavity Band Pass Filter. In detail *ZVBP-4000-S+* [62] cavity bandpass filter is connected after the $2F_{LO} = 4$ GHz signal generator and a *ZVBP-2100-S+* [63] cavity bandpass filter is used to attenuate phase noise around blocker's frequency.

Figure 3.6.6 shows Noise Figure expansion as a function of blocker power. 1 dB noise figure expansion is observed for $P_{blocker} = -4$ dBm, increasing to 6.5dB when a 0 dBm blocker is introduced.

The OOB IIP3 is measured through a two-tone intermodulation test two tones at $F_{LO} + \Delta f$ and $F_{LO} + 2\Delta f + 2$ MHz with $F_{LO} = 2$ GHz. OOB IIP3 is tested for different offset frequencies shown in Figure 3.6.7. The OOB IIP3 increases very steeply reaching the maximum around $\Delta f = 40$ MHz offset.

Comparing the measurement results of 1 dB compression point, 1 dB noise figure expansion and IIP3 targeted performances (Equations 3.1.2 and 3.1.4),

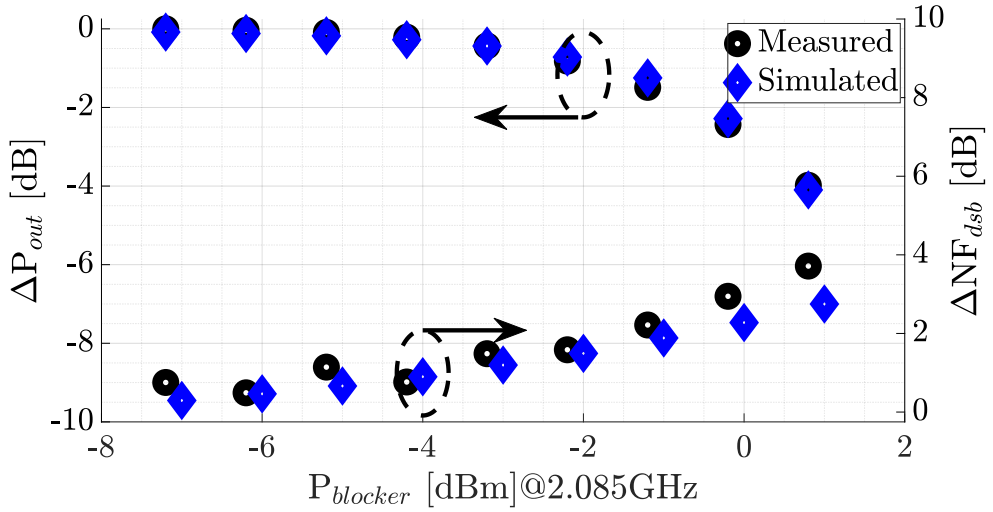


Figure 3.6.6: Measured Main receiver compression gain (left) and NF expansion (right) due to a blocker located at 85 MHz from F_{LO}

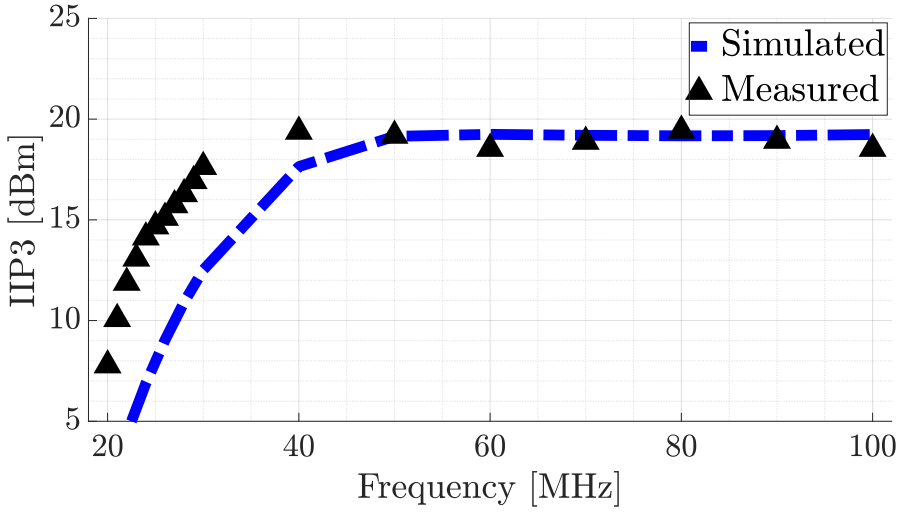


Figure 3.6.7: Measured Main receiver OOB-IIP3 due to two interferences at $F_{LO} + \Delta f$ and $F_{LO} = 2\Delta f + 2$ MHz

it is derived that this receiver could tolerate an OOB insertion loss of 35 dB, which is 5 dB lower than the targeted value.

The receiver's transfer function is also measured as a function of different carrier frequencies. The results from $F_{LO} = 2$ GHz up to $F_{LO} = 2.8$ GHz is reported in Figure 3.6.8. The average gain remains above 40 dB, with

good agreement with the simulations. The OOB IIP3 is also measured as function of the of the LO frequency F_{LO} and reported in red 3.6.8. The OOB IIP3 is obtain using the same measurement setup with the first tone at $\Delta f/\omega_{3\text{-dB}} = 2.8$, where $\omega_{3-dB} = 14.3\,\text{MHz}$ is the $-3\,\text{dB}$ bandwidth of the receiver.

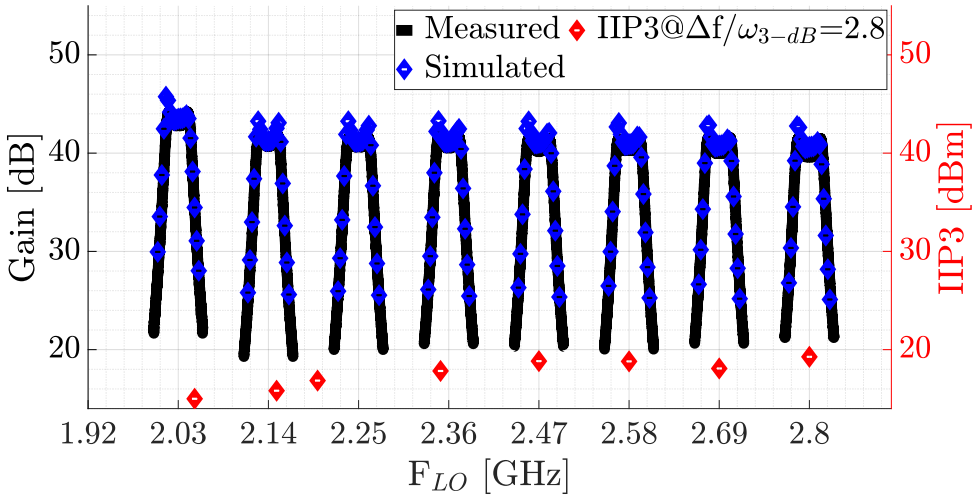


Figure 3.6.8: Measured Main receiver transfer function as frequency of F_{LO}

The NF_{dsb} is measured as a function of the F_{LO} as well. Figure 3.6.9 reports less than 3.5 dB NF_{dsb} integrated over 10 MHz bandwidth from 2 to 3 GHz of frequency's carrier.

The achieved results are compared with other State-of-the-Art receiver in Table 3.6.2. In comparison with solutions [45, 64–67] the proposed receiver achieves higher gain and comparable Noise Figure and it exhibits the lowest NF expansion in the presence of a 0 dBm an interferer, except for [64] which places the blocker at relative greater distance ($\Delta f/\omega_{3\text{-dB}} = 8$) respect to this solution ($\Delta f/\omega_{3\text{-dB}} = 6$) and consuming over twice the power at 2 GHz compared to this design.

The traslational positive feedback architecture effect is enlightened by the linearity result. This solution achieves the higher OOB IIP3 with a blocker placed at only $\Delta f/\omega_{3\text{-dB}} = 2.8$ distance respect to the LO. This result is exceeded only by [64] due to its significantly lower gain (20 dB). The blocker tolerance measured thought 1 dB gain compression shows a very

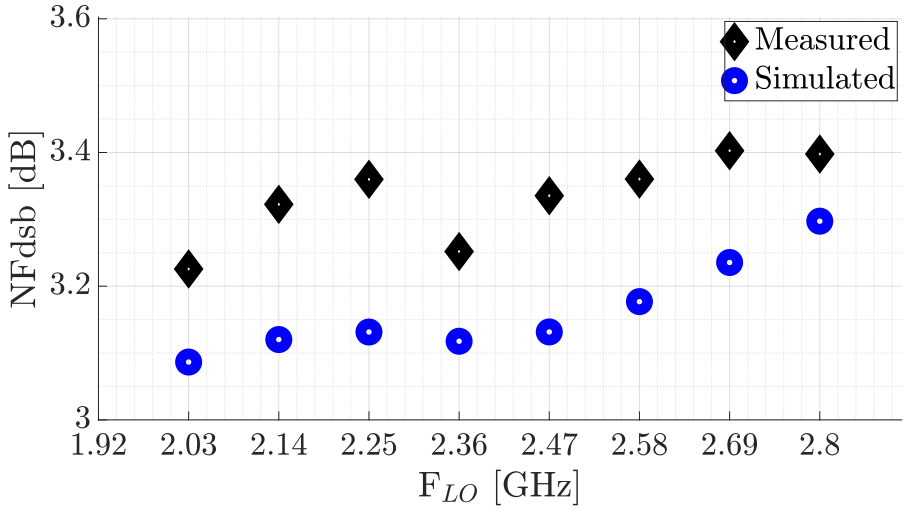


Figure 3.6.9: Measured Main receiver noise figure as frequency of F_{LO}

good tolerance to the interferes.

The area occupied by this design is the second smallest, while in terms of power consumption, it is the lowest among the designs presented at 2 GHz. Compared to other works with similar RF bandwidth reported in Table 3.6.2, the solution presented in this work provides the largest S_{11} bandwidth below -10 dB.

Reference	[45] RFIC 2015 Nejdel	[64] JSSC 2018 Lien	[65] JSSC 2021 Wang	[66] ISSCC 2023 Montazerolghaem	[67] ISSCC 2023 Araei	[60] **This Work**
Architecture	Mixer First Trasl.Pos. FB	Mixer first	BPCG Noise Canceling	LNTA first Double Trasl. FB	Mixer first Harmonic-Rejecting	LNTA first Trasl.Pos. FB
Technology	65nm CMOS	45 nm SOI	45nm SOI	40nm CMOS	45nm SOI	28nm CMOS
f_{RF} [GHz]	$0.7-3.8$	$0.2-6$	$0.02-2$	$0.4-7.3$	$0.25-2.5$	$2-2.8$
Gain [dB]	40	21	40	42	35	43
BB BW [MHz]	15	10	-	150	15	14
NF [dB]	$2.5-4.5$	$2.3-5.4$	$2.1-2.5$	$3.2-5.8$	$3.5-5.5*$	$3.2-3.4$
0 dBm Blocker NF [dB]	-	4.7 $\Delta f/\omega_{3\text{-dB}}=8$	6.7 $\Delta f=80$ MHz	9.65 $\Delta f/\omega_{3\text{-dB}}=10$	7.8 $\Delta f/\omega_{3\text{-dB}}=12$	6.2 $\Delta f/\omega_{3\text{-dB}}=6$
OOB IIP3 [dBm]	+8 $\Delta f/\omega_{3\text{-dB}}=2.8$	+22 $\Delta f/\omega_{3\text{-dB}}=2.8$	+14 $\Delta f=100$ MHz	+7 $\Delta f/\omega_{3\text{-dB}}=3$	+8 $\Delta f/\omega_{3\text{-dB}}=2.8$	+18 $\Delta f/\omega_{3\text{-dB}}=2.8$
P1dB [dBm]	+1 $\Delta f/\omega_{3\text{-dB}}=6$	+10 $\Delta f/\omega_{3\text{-dB}}=6$	-	-4.8 $\Delta f/\omega_{3\text{-dB}}=6$	-2 $\Delta f/\omega_{3\text{-dB}}=6$	-1.9 $\Delta f/\omega_{3\text{-dB}}=6$
LO leakage [dBm]	<-70	<-65	<-80	-	-	<-70
Supply [V]	1.2	1.2	1.2-1.6	1.3	1-1.2	1.2
Active Area (mm^2)	0.23	0.8	1.05	0.42	0.65	0.36
Power [mW]	8.16 27 [mW/GHz]	50 30 [mW/GHz]	68-95	100 13 [mW/GHz]	32.4-54	37 7 [mW/GHz]

*Minimum spotted Noise Figure.

Table 3.6.2: Performance comparison with state-of-art receivers

Chapter 4

Auxiliary Receiver validation

In this chapter the Auxiliary receiver is presented. In the first Section 4.1, the target performances and the receiver's architecture will be briefly introduced and in the end the results obtained from the measurements will be presented in Section 4.2.

4.1 Circuit implementation

The design of the Auxiliary receiver was not addressed in this activity and its design approach is detailed in [68]. Figure 4.1.1 illustrates the schematic of the Auxiliary receiver.

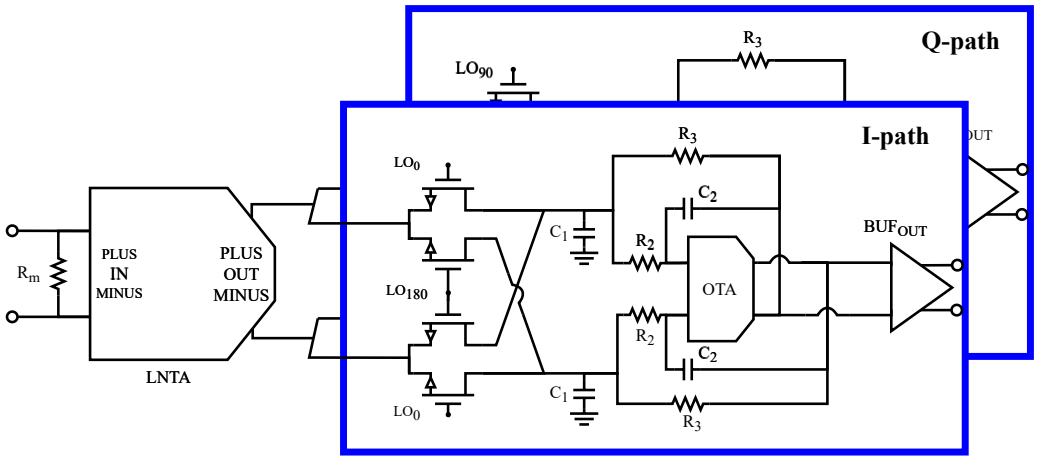


Figure 4.1.1: Block schematic of the proposed Auxiliary receiver

The LNTA employs a two-stage topology. The first stage adopts a Source Degenerated (SD) topology, as depicted in Figure 4.1.2, with a single degeneration inductor L_D. At lower frequencies, capacitor C_D decoupled the center-tap of the inductor.

The drain current of the P and N input MOSFETs is routed to the second stage via a transformer. A transformer with a 5 : 3 turn ratio is utilized to implement an LC filter while providing current gain. The second stage functions as a current buffer utilizing Cross-Coupled Common Gate (CCCG) transistors.

The output current from the LNTA is down-converted by a 4-phase 25% duty-cycle passive mixer. Rauch TIAs complete the chain, converting the signal current to voltage and performing second-order filtering.

The total bias current of the LNTA is 9.5 mA, with 8 mA allocated to the SD-LNTA stage and the remainder to the second stage. The transconductance (g_m) of each transistor in the first and second stage is 90 mS and 14.4 mS respectively. The center-tapped inductor L_D has an inductance of 4.9 nH, while the capacitor C_D is 4.1 pF.

To match the input impedance with the instrument's output impedance, an on-chip resistance $R_m = 1.2\,\text{k}\Omega$ is implemented.

4.2 Measurement Results

The proposed Auxiliary receiver prototype was fabricated in a TSMC 28 nm CMOS process. Figure 4.2.1 displays the chip photograph. The total area occupies 0.5 mm^2, mainly comprising two transformers and the L_D inductor.

Figure 4.2.2 shows the measurement setup. The chip is wire-bonded to a 4-layer PCB with FR-4 substrate and the input signal is converted from single-ended to differential by a *NCS2-33+* [69] on-board balun. The 4 GHz input signal used to drive the on-chip divider is converted from single-ended to differential by a *NCS4-442+* [70] on-board balun. The output is sensed with a *LeCroy AP033* active differential probe which is connected to the onboard pinhead. The losses of the measurement setup including 1:2 off chip balun, PCB traces and cables are de-embadded from the plot presented in this section since they will not be present when the circuit is integrated with

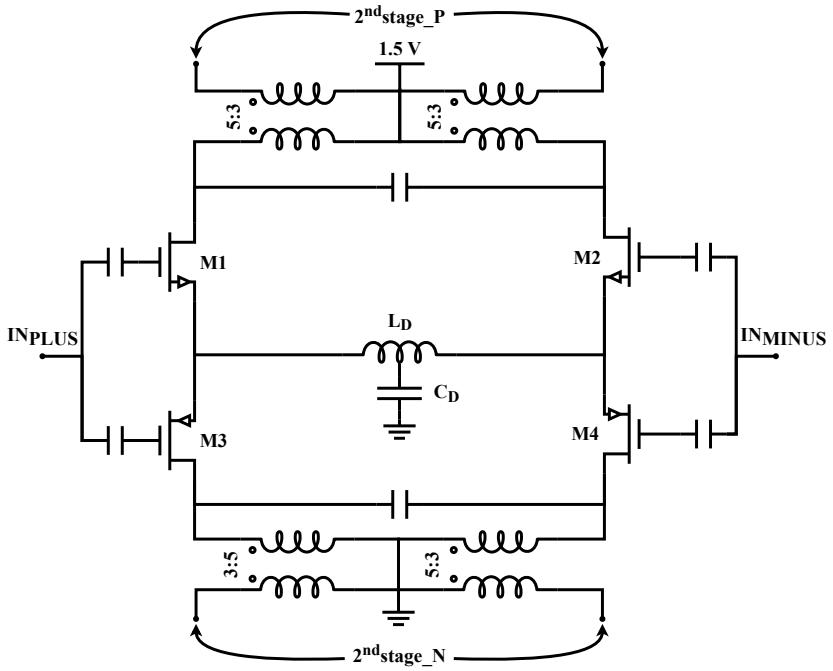


Figure 4.1.2: Schematic of the first stage of the Auxiliary LNTA

the TX.

Figure 4.2.2 illustrates the measurement setup. The chip is bonded to a 4-layer PCB with an FR-4 substrate and the single-ended input signal is converted to differential using an *NCS2-33+* [69] on-board balun. The 4 GHz input signal driving the on-chip divider is converted from single-ended to differential with an *NCS4-442+* [70] on-board balun. The output is probed with a *LeCroy AP033* active differential probe connected to the onboard pinhead. Measurement setup losses, including the 1:2 off-chip balun, PCB traces and cables, are de-embadded from the presented plots in this section. In the final FDD chip, these losses won't be present when the circuit integrates with the TX.

During the chip validation phase, an oscillation was observed at the receiver input. Figure 4.2.3 displays the resulting measurement using the *Rohde&Schwartz FSQ8* Spectrum Analyzer connected via the PCB connector. This oscillation is common-mode and can be simulated by considering the S-parameters of the balun or by applying a common-mode stimulus at the input of the LNTA.

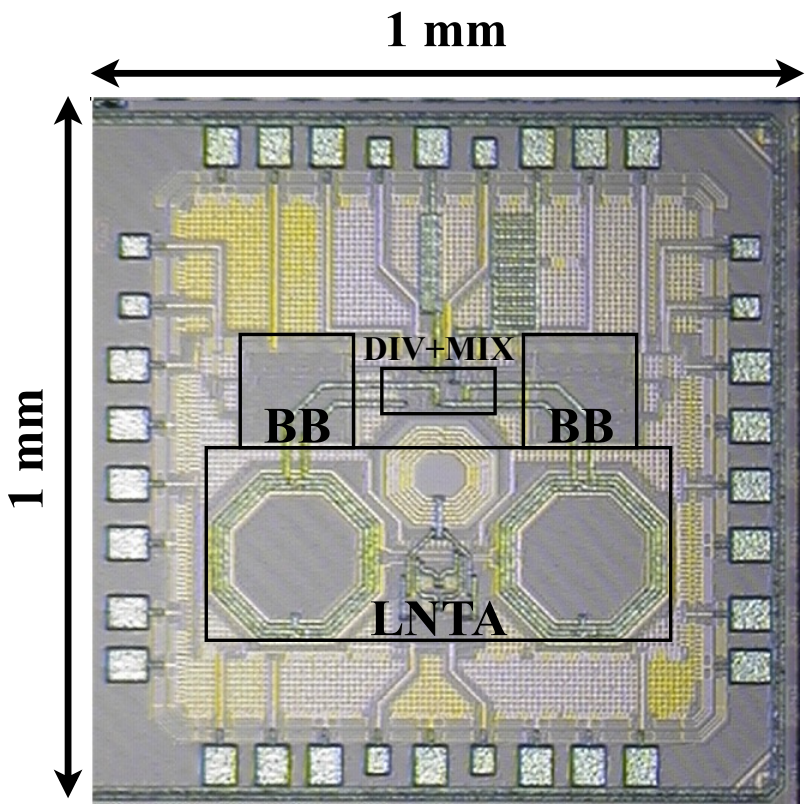


Figure 4.2.1: Auxiliary receiver chip photograph [68]

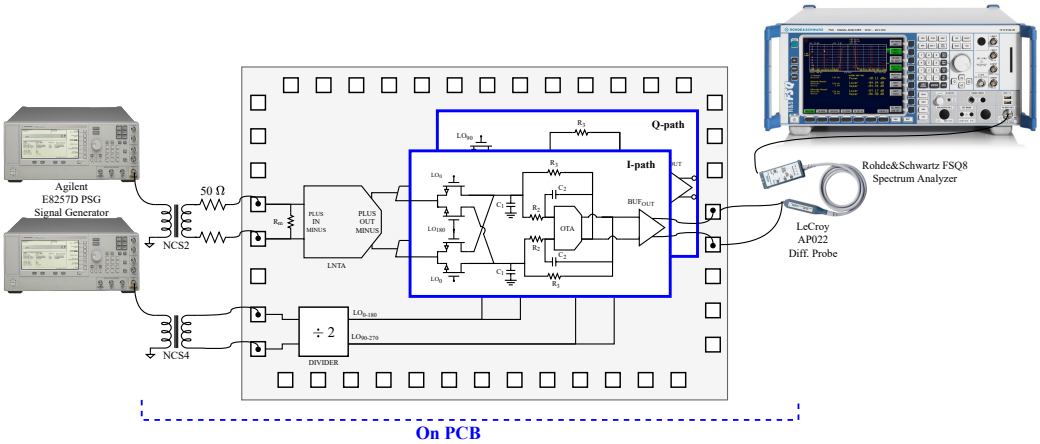


Figure 4.2.2: Auxiliary receiver simplified measurement setup. Where needed (compression measurement, NF expansion measurement...) the input signal is first combined and then sent to the PCB

In Figure 4.2.4 can be observed the simulated voltage at the input node

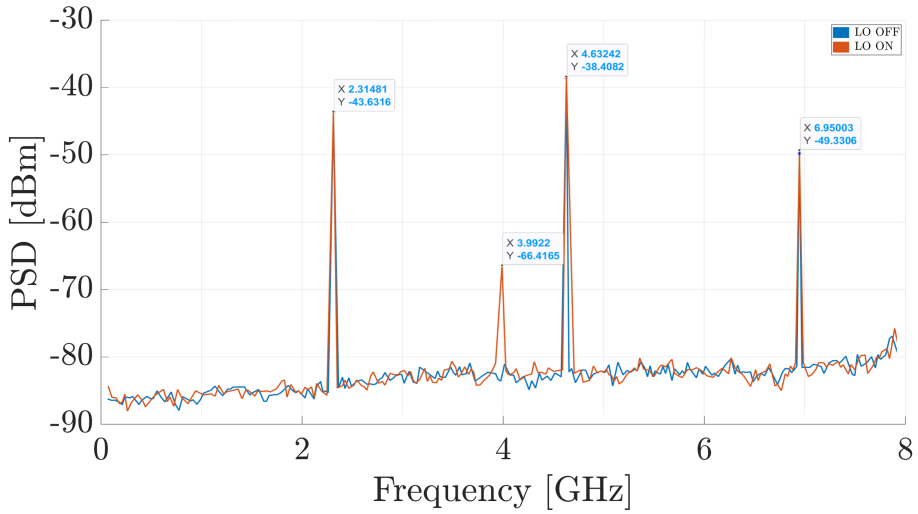


Figure 4.2.3: Power spectral Density of the oscillation observed at the input of the auxiliary receiver

of the receiver considering PCB trace parasitic extraction and the balun's S-parameters. From the simulation results can be observed that the oscillation can be avoid with the introduction of two 50 Ω resistors in series at the output of the balun, as shown in Figure 4.2.2. This result is validate with the measurement.

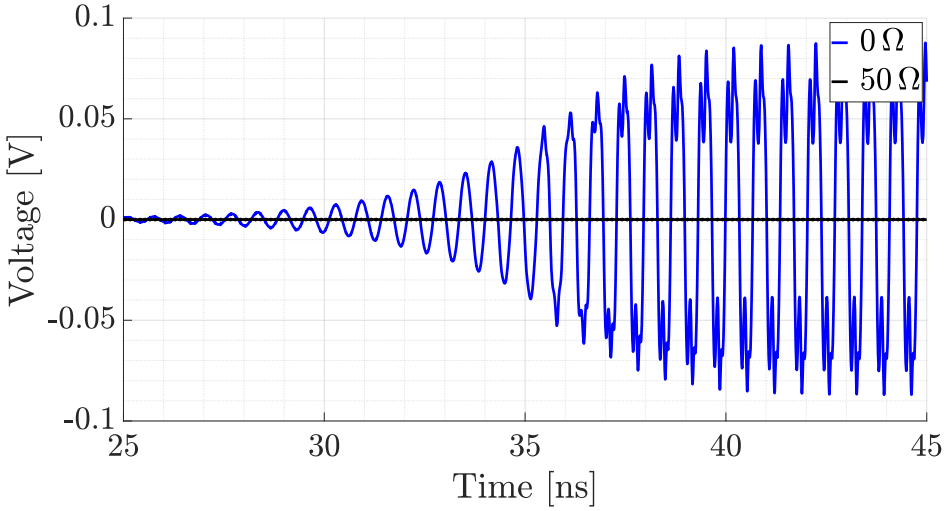


Figure 4.2.4: Transient simulation of the input voltage of the LNTA with and without resistors

The frequency response of the Auxiliary receiver is measured using the

setup depicted in Figure 4.2.2 and the gain versus IF frequency is presented in Figure 4.2.5 for a 2 GHz LO. The in-band down-conversion gain is 25.2 dB, achieving 35 dB filtering thanks to the Rauch filter at the 80 MHz offset frequency from the RX band.

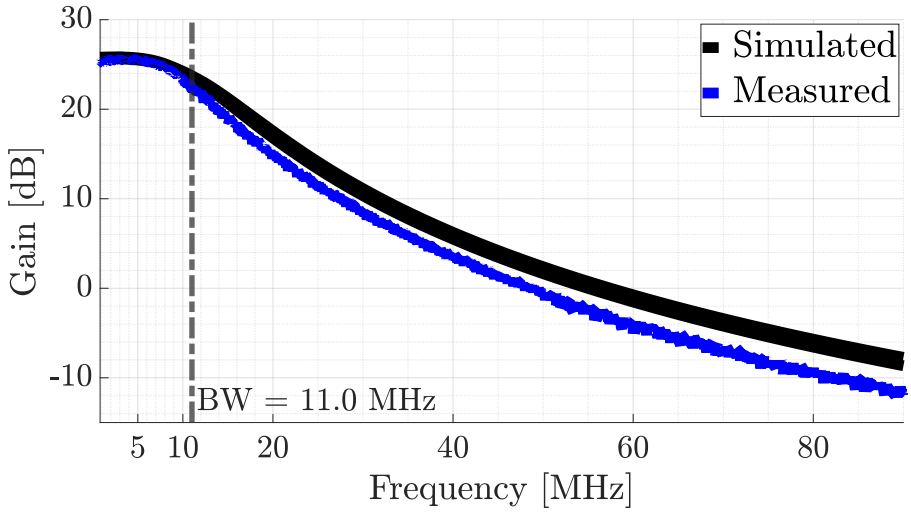


Figure 4.2.5: Auxiliary receiver transfer function with 2 GHz frequency carrier

Figure 4.2.6 illustrates the integrated Double Side-Band Noise Figure (NF_{dsb}) over a 10 MHz bandwidth, which is 6 dB. Similar to the Main RX, the NF_{dsb} is measured with a 20 dB probe gain to overcome the spectrum analyzer's noise and reduce the loading parasitic capacitance of the probe.

The large signal tolerance of the Auxiliary receiver is demonstrated in Figure 4.2.7. The measurement combines an interferer at 2.080 GHz ($\Delta f/\omega_{3\text{-dB}} = 7$ with respect to LO) through a *Suhner 4901 19.a* power combiner with a small IB signal. The 1 dB compression point (P1dB) occurs at 7 dBm, 4 dB earlier than in pre-tapeout simulations.

This discrepancy is due to the interconnect parasitic resistance (about 25 Ω) between the mixer and the baseband filter, that was not correctly extracted. [68]

Figure 4.2.8 shows the Noise Figure expansion in the presence of an Out-of-Band (OOB) blocker at 80 MHz and 160 MHz. The system is affected by the phase noise of the instrumentation, as the phase noise of the divider at 80 MHz and 160 MHz frequency offsets is almost equal.

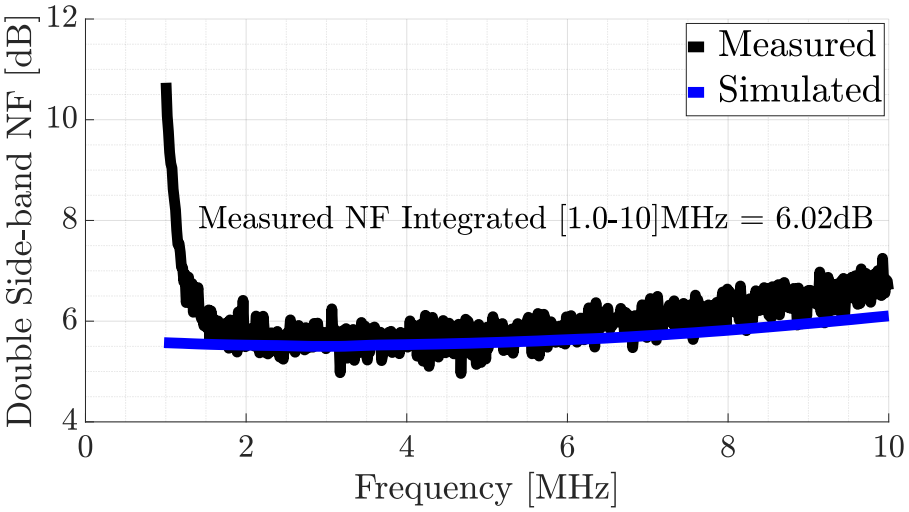


Figure 4.2.6: Auxiliary receiver Noise Figure with 2 GHz frequency carrier

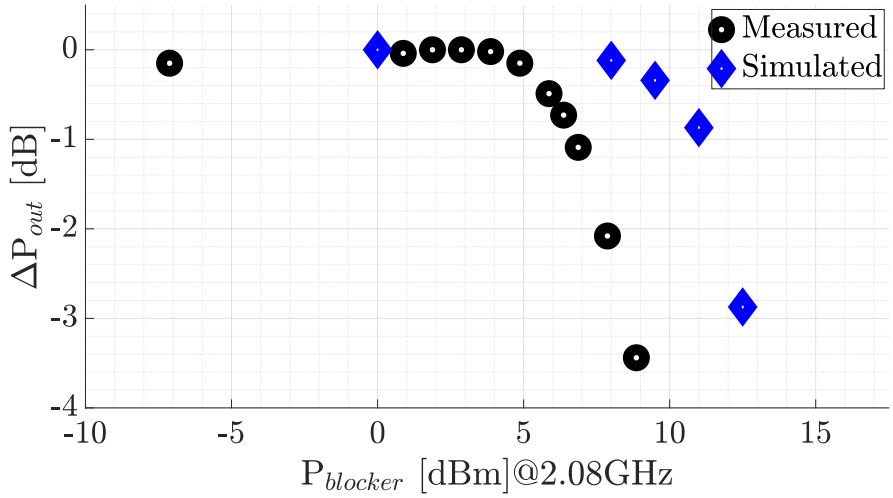


Figure 4.2.7: Measured Auxiliary receiver compression gain due to a blocker located at 80 MHz from F_{LO}

The performance of the Auxiliary receiver is compared with the state-of-the-art in Table 4.2.1. In [71], a filter Figure of Merit (FOM) is proposed, which is independent of the integrated bandwidth and considers power consumption. It is defined as

$$\mathrm{FOM} = \mathrm{P1dB}_{dBm} - \mathrm{P}_{n1Hz} - 10\log_{10}(\mathrm{Pwr}_{FLO}) \tag{4.2.1}$$

where P1db is the 1 dB compression point, P_{n1Hz} is obtained from the thermal

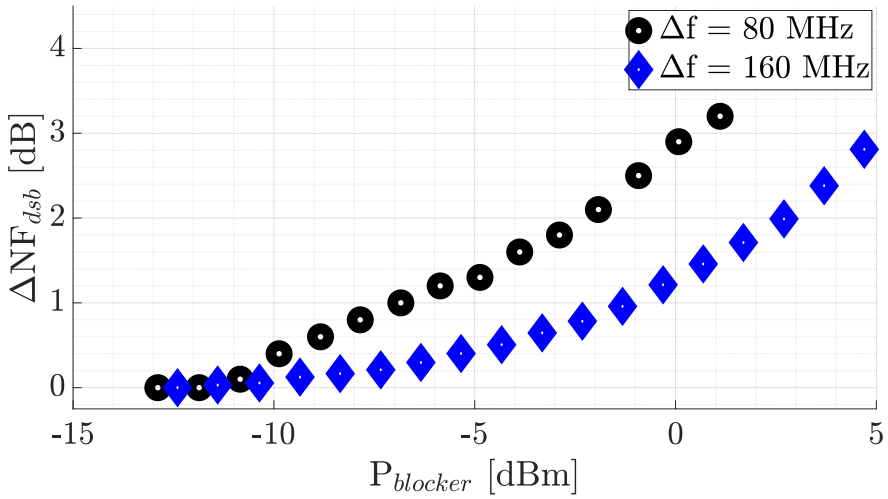


Figure 4.2.8: Measured Auxiliary receiver NF expansion due to a blocker located at 80 MHz and 160 MHz from F_{LO}

noise floor (-174 dBm/Hz) increased by the noise figure and Pwr_{FLO} is the total power consumption at the working frequency.

Reference	[72] ESSCIRC 2017 Montanari	[73] TMTT 2016 Hasan	[2] ISSCC 2017 Lien	[64] JSSC 2018 Lien	[74] JSSC 2019 Musayev	[75] ISSCC 2021 Montazerolghaem	[68] **This Work**
Architecture	LNTA first	N-Path filter	N-Path RX	Mixer first	Quantized RX	N-Path LNA RX	LNTA first
Technology	28 nm CMOS	65 nm CMOS	28 nm CMOS	48 nm SOI	65 nm CMOS	40 nm CMOS	28 nm CMOS
f_{RF} [GHz]	0.7 – 2	0.1 – 1.4	0.1 – 2	0.2 – 8	0.7 – 1.4	0.4 – 3.2	1.9 – 2.1
Gain [dB]	27 – 30	23	18-12	21	20.8-36.8	36	25.3
BB BW [MHz]	30	10	13	10	10	80	10
NF [dB]	6.2 – 9.6	3 – 4.2	4 – 10	2.3 – 5.4	14.6 – 1.9	2.7 – 3.6	6
0 dBm Blocker NF [dB]	6.2 $\Delta f/\omega_{3\text{-dB}} = 3$	6 $\Delta f/\omega_{3\text{-dB}} = 4$	8 (1.3 GHz) $\Delta f/\omega_{3\text{-dB}} = 6$	4.7 (1.4 GHz) $\Delta f/\omega_{3\text{-dB}} = 8$	7.9 at B1dB	8.3 $\Delta f/\omega_{3\text{-dB}} = 6.25$	7.1 $\Delta f/\omega_{3\text{-dB}} = 16$
P1dB [dBm]	5 $\Delta f/\omega_{3\text{-dB}} = 1.7$	8 $\Delta f/\omega_{3\text{-dB}} = 4$	13 $\Delta f/\omega_{3\text{-dB}} = 6$	12 $\Delta f/\omega_{3\text{-dB}} = 8$	10.5, -8.5 $\Delta f/\omega_{3\text{-dB}} = 10$	-5 $\Delta f/\omega_{3\text{-dB}} = 5$	7 $\Delta f/\omega_{3\text{-dB}} = 8$
Active Area (mm^2)	0.12	2.4 (w/ pads)	0.49	0.8	0.25	0.6	0.5
Power [mW]	16.2 24 [mW/GHz]	48 17.7 [mW/GHz]	30 36 [mW/GHz]	50 30 [mW/GHz]	13.7, 14 37.2 [mW/GHz]	58.5 17.6 [mW/GHz]	27 10 [mW/GHz]
FOM [dBm/Hz]	151.3 2 GHz	160.1 1 GHz	156.9 2 GHz	162.8 2 GHz	153 – 146.8 0.9 GHz	146.3 2 GHz	158.3 2 GHz

Table 4.2.1: Performance comparison with state-of-art receivers

Compared to other receivers consuming almost twice [73–75] or more [2, 64] power at 2 GHz, this solution exhibits an FOM close to N-path based and mixer-first receivers with impedance-matched input and it demonstrates a 7 dB improved FOM compared with the input unmatched auxiliary receiver [72].

Considering the post-layout simulation shown in Figure 4.2.7, a lower resistance mixer interconnect provides over 5 dB improvement in the 1 dB compression point, resulting in a FOM of 163.3 dBm/Hz, which would be the best among those listed in Table 4.2.1.

Chapter 5

Digital Signal Processing

In this chapter, the FPGA design, which includes a Clock and Data Recovery (CDR) module, a storage memory and a UART interface for signal transmission, is presented in Section 5.1. Subsequently, the design is validated, demonstrating initial signal cancellation through the utilization of an adaptive digital filter employing the Least Mean Squares (LMS) algorithm.

5.1 FPGA Design

In order to validate the effectiveness of the Frequency Division Duplex (FDD) proposed and the capability of the digital cancellation of the leakage noise, a Digital Signal Processing (DSP) block has to be design, where the Self-Interference Cancellation will be executed.

In this first step of the project it was not possible to implement a DSP on-chip, so the design of an FPGA coupled with a post-processing signal with the software MATLAB® is considered.

Figure 5.1.1 illustrates the design implemented in the FPGA. The data path is shown in purple, while the clock signals are highlighted in blue. It is important to note that the input RF signal, the clock signal and the internal clock of the FPGA must have the same phase reference. This can be achieved by implementing a Clock and Data Recovery (CDR) which selects

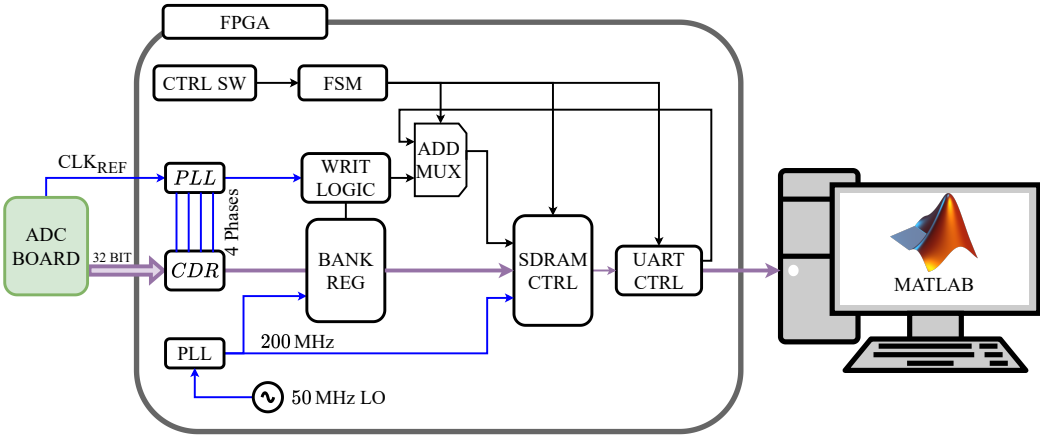


Figure 5.1.1: Block diagram of the implemented FPGA design

one of the four phases generated by a Phase-Locked Loop (PLL) that takes the reference from the same signal that clocks the ADCs. Once the 4 bytes are sampled, they are stored in a bank register to be sent to the on-board Dynamic Random Access Memory (DRAM). An Finite State Machine (FSM) controlled by on-board switches determines the state of the DRAM through writing, reading, or resetting states.

5.1.1 Clock and Data Recovery

In serial data communication, there could be a situation in which the clock phase at the opposite end of the communication is relatively different, resulting in the data receiver being unable to sample correctly. In this situation a CDR must be implemented.

Figure 5.1.2a illustrates the first stage of the Clock and Data Recovery (CDR) proposed in [76]. The received data is sampled by four clock phases generated by a PLL whose reference is the same clock as that of the ADCs.

The Least Significant Bit (LSB) is taken as the reference signal because it has the highest switching frequency. The four paths are four delay lines with different delays to obtain a coherent signal at the end of the chain. The third (XZ(2)) and the fourth (XZ(3)) delayed bits are fed into logic gates, as shown in Figure 5.1.2b, whose result determines if the sampled signal has changed or not. If so, this path provides valuable information, as shown in Figure 5.1.3a.

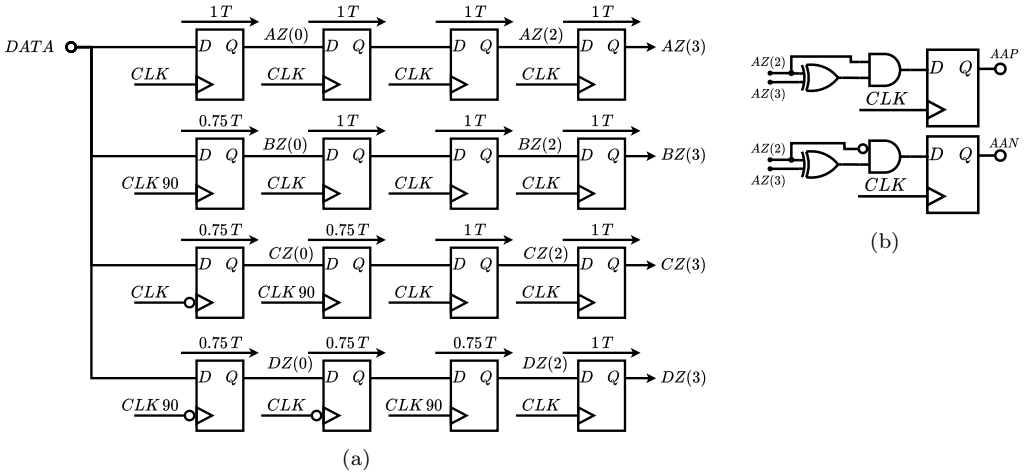


Figure 5.1.2: Block diagram of the 4 triggers of the CDR (a). Logic gates XOR and AND of the path A (b)

In Case 1, clock domain A is the first to detect that the LSB has changed, so path C will be used because in its domain the data will be stable. In Case 2, clock domain B recognizes the transition first, so the data clocked in during time domain D is forwarded into the system. Similarly, the correct front is determined in Cases 3 and 4, where the signal switches just before the clock edges C and D.

The results of the logic gates XORs and ANDs are used as a control signal for a multiplexer, whose truth table is shown in Table 5.1.1. This multiplexer selects which signal $XZ_{n\text{-}5}(0)$ is led to the output, where X is a row A, B, C, or D. The output signal is delayed by five clock cycles relative to the input signal. The default starting path selected is C, deemed optimal when the signal synchronizes with the input clock reference (A).

Table 5.1.2 shows all the possible states of 4 triggers of the CDR with the correspondent path selected as a function of the input signal.

Figure 5.1.3b shows the time diagram of the behaviour of the CDR block simulated through ModelSim environment when a phase variable signal is applied at the input.

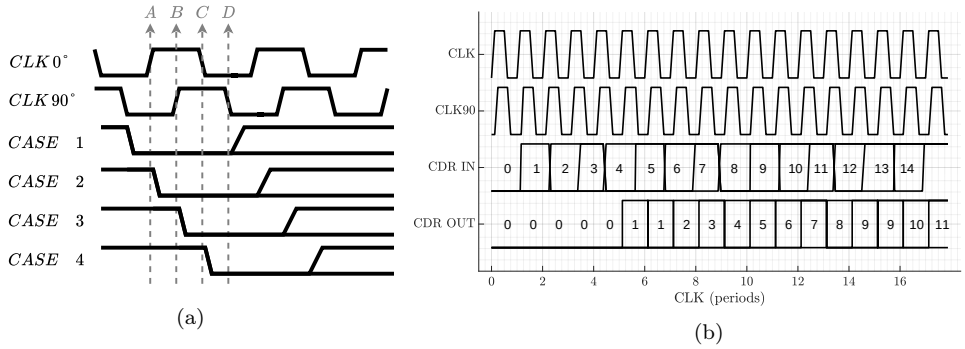


Figure 5.1.3: Time diagram example of the possible input signal timing (a). Output behaviour of the CDR simulated with ModelSim (b)

AAP/N	BBP/N	CCP/N	DDP/N	Chosen Path
1	1	1	1	C
1	0	0	0	D
1	1	0	0	A
1	1	1	0	B
others				LAST

Table 5.1.1: Truth table of Multiplexer implemented in the CDR

5.1.2 SDRAM controller and FSM

The SDRAM Controller serves as an interface to the 128 MB Synchronous Dynamic Random Access Memory (SDRAM) incorporated in the DE2-115 board, implemented through two 64 MB SDRAM devices [77]. Each device features separate 16-bit data lines interfaced with the FPGA, alongside shared control and address lines.

The on-board SDRAMs execute an auto-refresh routine a minimum of 8192 times per clock period. Throughout this auto-refresh command, address bits remain in an idle state. To prevent any data loss during this period, a bank register is employed, as shown in Figure 5.1.1.

Given the absence of a feedback control flag in the devices, the designed SDRAM controller must align with the latency of every command [78]. Figure 5.1.4 illustrates the controller implemented with a (FSM).

Following the power-up and initialization of the SDRAMs, the sampled

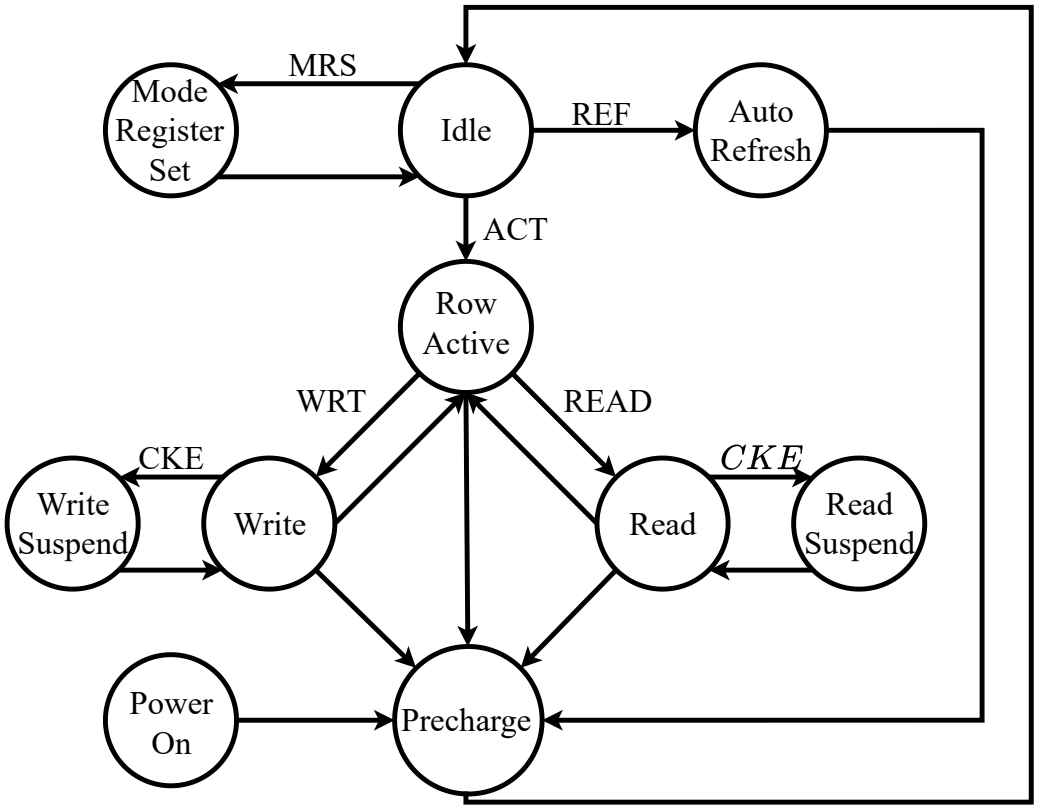


Figure 5.1.4: State diagram of the SDRAM controller FSM

signals are stored in the memories until they reach full capacity. Subsequently the state changes from *Write* to *Read* and the stored signals are transmitted through the UART interface.

5.2 First prototype results

The initial prototype encounters limitations when measuring a modulated signal. To evaluate the design's robustness, two sinusoidal signals, each with a power of $-3\,\mathrm{dBm}$ at $2.7\,\mathrm{MHz}$, are inputted into a fourth-order low-pass filter with a cutoff frequency of $15\,\mathrm{MHz}$. The filtered signals are then sampled at $50\,\mathrm{MHz}$ by the 8-bits ADCs. The FPGA utilized is a Cyclone® IV FPGA chip on the DE2-115 [77] development and education board. It is designed to sample and store $1.5\,\mathrm{ms}$ of signal in the on-board SDRAM, serialize it (as detailed in Section 5.1) and then transmit the bit stream through

UART communication to MATLAB® for further processing, as illustrated in Figure 5.2.1.

The Adaptive Filter employed is a linear equalizer from the comm.LinearEqualizer System object™ [32], as depicted in Figure 2.2.5 in Section 2.2.2.

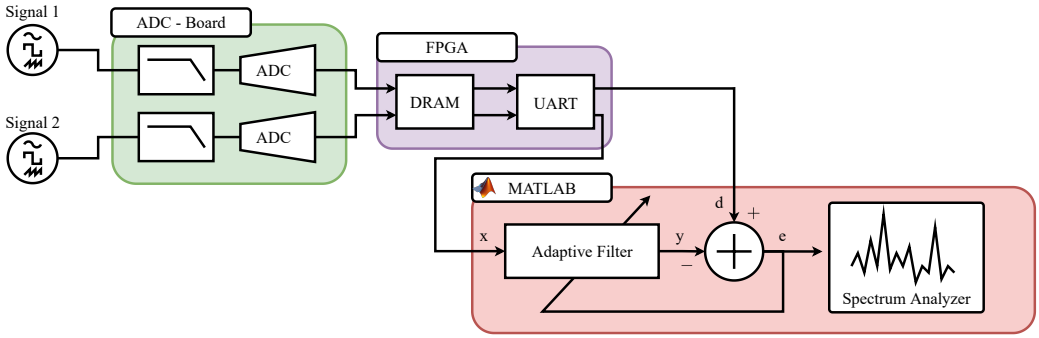


Figure 5.2.1: Block diagram of the measurement setup. Transmission of serialized signals from FPGA to MATLAB® for processing

In this application, the condition in which the two input signals cancel out is examined, focusing on the output e of the equalizer. Once implemented, the equalizer adaptively adjusts tap weights to minimize the difference between the desired signal d (Signal 1) and the filter output y.

Figure 5.2.2 illustrates three metrics useful for choosing the length of the adaptive digital filter and so its complexity. The root mean square (rms) is calculated for each period of the signal as

$$rms_k = \sqrt{\frac{1}{T} \sum_{i=(k-1)T}^{kT} \left(\overline{e_k} - e_i\right)^2} \quad \text{with } k = 1, 2 \ldots \tag{5.2.1}$$

where e_i and $\overline{e_k}$ are the signal error at the filter output and its mean in the period k, T is the period of the input signal and k is the period index. In the top plot of Figure 5.2.2, the minimum achieved rms is shown as a function of the number of taps. As expected [31], the error decreases as the filter complexity increases.

The convergence time of the filter is defined as the time at which the rms_k is less than two times the amplitude of the signal reduced by 35 ($2A \cdot 0.0178$) or 40 dB ($2A \cdot 0.01$). As depicted in the middle plot of Figure 5.2.2, the convergence time increases with the number of taps, reaching its maximum around 4 μs for the 35 dB condition, corresponding to 180 samples.

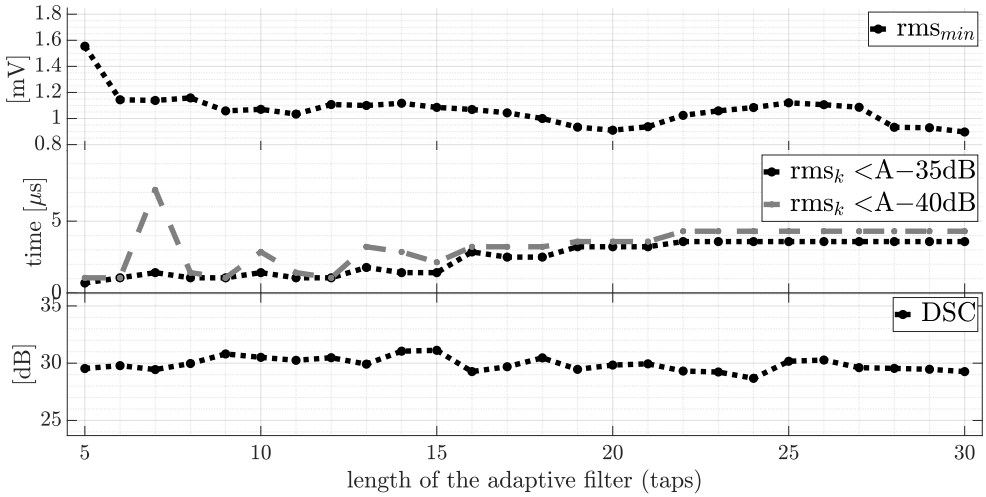


Figure 5.2.2: Resulting rms of the e LMS output for 1 ms sampled input signals (top), time required to the filter to reach convergence level (middle) and, DNR as function of number of taps (bottom)

The last plot in Figure 5.2.2 displays the Digital Signal Cancellation (DSC) calculated as

$$DSC|_{dB} = P_{signal}|_{dB} - P_{e-LMS}|_{dB} \tag{5.2.2}$$

where P_{signal} is the Power Spectral Density (PSD) of Signal 1 and P_{e-LMS} is the integrated PSD of the output e of the equalizer. The spectrum of the signal is obtained through a custom MATLAB® function where the spectrum can be derived from a waveform. A Hanning window can be applied to the signal and the noise can be integrated up to 10 MHz, as depicted in Figure 5.2.4.

As illustrated in the third plot of Figure 5.2.2, after convergence, the filter successfully reduces the signal level by up to 30 dB regardless of the number of taps.

Figure 5.2.3 portrays the waveform of Signal 1 and 2 along with the respective output error e and rms_k value for an LMS filter with 9 taps. In the time domain, the applicability of the adaptive digital filter is even more evident, as it achieves convergence in just a few periods, compensating for the delay of the two signals.

The respective PSD is shown in Figure 5.2.4. Here, the sampled signal and its noise are visually represented in black and red, respectively. The resulting

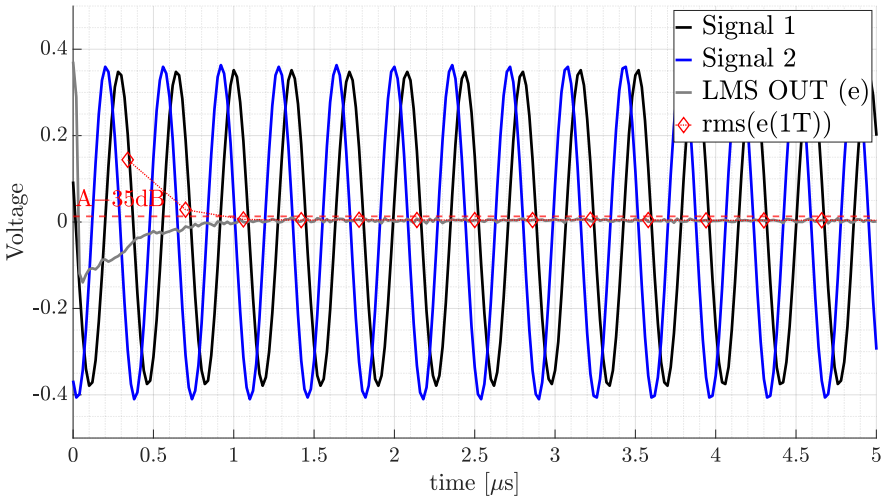


Figure 5.2.3: Wave plot of the sampled signals (black and blue) with the resulting e LMS output

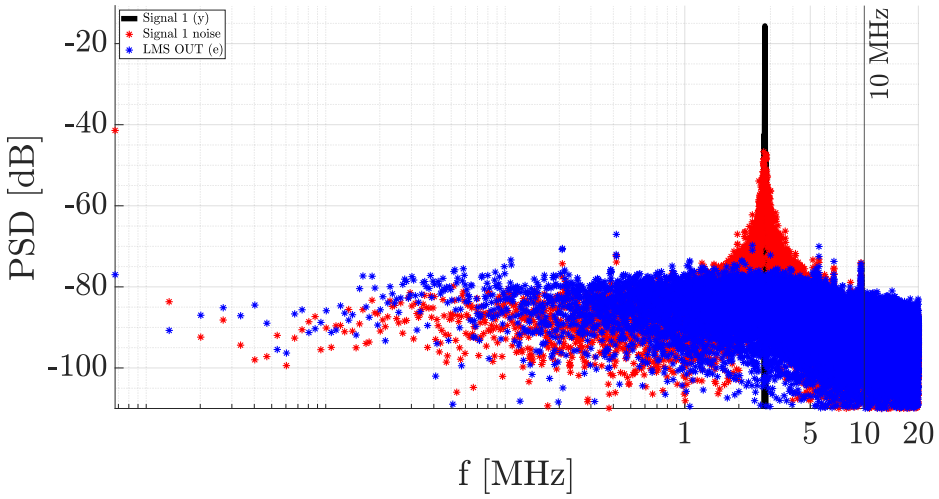


Figure 5.2.4: Signal and noise representation with resulting power spectral density after Adaptive Digital Filter processing

power spectral density of the output signal of the filter e is depicted in blue. This comprehensive visualization provides insights into the efficacy of the applied Adaptive Digital Filter using the LMS algorithm.

The plot in Figure 5.2.4 demonstrates that the filter successfully cancels out the $-3\,\mathrm{dBm}$ signal, resulting in an integrated noise power of $-33.5\,\mathrm{dBm}$.

The current prototype lays the foundation for future enhancements, envi-

sioning the integration of both main and auxiliary receivers. This evolution will enable measurement of the cancellation efficacy when a modulated signal is introduced at the receiver's input as simulated in Section 2.2. The successful cancellation of modulated signals presents an exciting avenue for further exploration and application in scenarios

CLK	Path	DATA	Z(0)	Z(1)	Z(2)	Z(3)	P	N	Chosen Path
1	A	0	X	X	X	X	X	X	C
	B	0	X	X	X	X	X	X	
	C	0	X	X	X	X	X	X	
	D	0	X	X	X	X	X	X	
2	A	1	0	X	X	X	X	X	C
	B	1	0	X	X	X	X	X	
	C	1	0	X	X	X	X	X	
	D	1	0	X	X	X	X	X	
3	A	1	1	0	X	X	X	X	C
	B	0	1	0	X	X	X	X	
	C	0	1	0	X	X	X	X	
	D	0	1	0	X	X	X	X	
4	A	0	1	1	0	X	X	X	C
	B	0	0	1	0	X	X	X	
	C	1	0	1	0	X	X	X	
	D	1	0	1	0	X	X	X	
5	A	1	0	1	1	0	1	0	C
	B	1	0	0	1	0	1	0	
	C	1	1	0	1	0	1	0	
	D	0	1	0	1	0	1	0	
6	A	0	1	0	1	1	0	0	C
	B	0	1	0	0	1	0	1	
	C	0	1	1	0	1	0	1	
	D	0	0	1	0	1	0	1	
7	A	1	0	1	0	1	0	1	D
	B	1	0	1	0	0	0	0	
	C	1	0	1	1	0	1	0	
	D	1	0	0	1	0	1	0	
8	A	1	1	0	1	0	1	0	A
	B	0	1	0	1	0	1	0	
	C	0	1	0	1	1	0	0	
	D	0	1	0	0	1	0	1	

Table 5.1.2: Possible states of the CDR output as a function of the input DATA (LSB)

Conclusions

Confronting the new challenges posed by the 5G communications era, this thesis proposes a SAW-Less FDD Receiver that uses SIC architecture in order to achieve strong OOB interferer tollerance while providing the necessary tunability required by modern mobile communication standards.

The receiver prototype architecture consists of three main components: the Main receiver, the Auxiliary receiver and the Digital Signal Processing (DSP) block. The design is first verified through MATLAB® simulations. The SIC is applied by employing an Adaptive Digital Equalizer within both the Main and Auxiliary loops. As a result, the desired standards requirements can be met while significantly reducing the front-end SAW filter's level to less than 40 dB.

The Main and Auxiliary receivers are validated on silicon. For the Main receiver is chosen a translational positive feedback loop architecture. This design achieves a balance between IB and OOB selectivity, thereby improving both linearity and noise performance, as described in the dedicated chapter. The selectivity is a function of the local oscillator (LO) frequency and can be tuned over a wide range, which can be extended paying more attention to parassitic effects.

A more traditional approach is considered for the Auxiliary receiver. The primary focus of this block's design is to minimize the noise-to-compression point ratio. This optimization ensures robustness against high transmitter output levels while avoiding the introduction of undesirable noise into the system.

Additionally, the feasibility of the DSP implementation is demonstrated through the coupling of an FPGA design with a software-based adaptive digital filter.

Overall, this work lays the foundation for future advancements in RF communication. It underscores not only the importance of adopting SIC techniques but also the necessity of exploring new design strategies and architectures. Combining these two targets can bring in a new era of faster and more efficient communication devices.

Appendix A

Differential Passive Mixer Model

All the considerations, steps and models outlined in this appendix are credited to [47]. Following the same approach, here is presented the differential a passive mixer model.

As shown in Figure A.1a, the analysis begins with a simplified model of a 4-phase passive mixer with non overlapping, 25% duty cycle quadrature LO pulses. Except for a small series resistance that represents the on-resistance of the switching MOSFET, the model treats the switches as ideal. Because the LO pulses are completely nonoverlapping and only one is active at a time, the series resistance of all the switches can be combined and treated as a single resistor of the same value, as shown in Figure A.1b.

The entire RF portion of the circuit can be modelled as R_a and R_{sw} in series with a parallel array of four ideal switches if we treat the antenna impedance as a resistor R_a (ignoring its reactive components for the time being). An effective antenna resistance can be defined as

$$R'_a = R_{sw} + R_a \tag{A.1}$$

Now we define a virtual voltage V_x at the node between R_{sw} and the ideal switches. The parallel combination of a filtering capacitor C_B and the amplifier input resistance R_B loads the switches' baseband port. We can approximate these capacitors as holding their voltage constant over a given LO cycle if the time constants $R_B C_B$ and $R'_A C_B$ are significantly larger than the LO period T_{LO}.

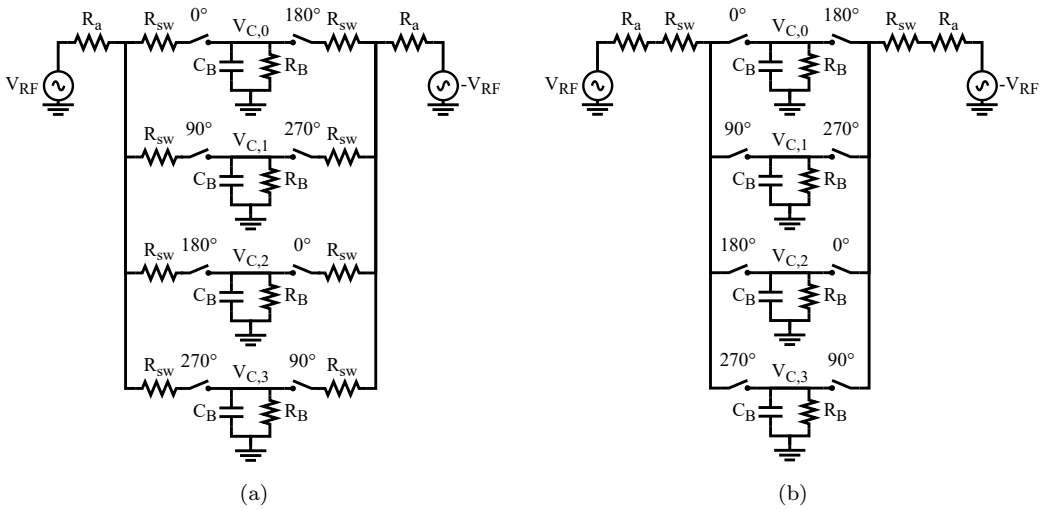


Figure A.1: Simplified circuit model of 4-phase differential passive mixer (a) and equivalent circuit based on non-overlapping LO driving waveforms

For in-band signals, the antenna input can be approximated as a sinusoid with fundamental frequency $\omega_{LO} = 2\pi/T_{LO}$ and time varying phase $\phi(t)$ and amplitude $A(t)$, which captures both modulation and offset frequency. If the amplitude and phase offset change slowly relative to T_{LO}, they can be approximated as constant over a given LO period and the input as

$$V_{RF}(t) = A\cos(\omega_{LO}t + \phi) \tag{A.2}$$

To calculate the input impedance provided by the mixer to the antenna, first compute the voltage across each output capacitor in response to the input. Each capacitor C_m ($m = 0, 1, 2, 3$) will continually dissipate a current equal to $I_{C,m} = V_{C,m}/R_B$ through its resistive load, R_B, that correspond to a total charge of $Q_m = T_{LO}V_{C,m}/R_B$ with $R_BC_B \gg T_{LO}$.

Meanwhile, for each LO cylce, this charge is recharged two times when the switches are closed. Assuming that the voltage across the mth capacitor, $V_{C,m}$, is stable (that is, that $\phi(t)$ and $A(t)$ change slowly relative to the time constants R_BC_B and R'_aC_B), conservation of charge implies that charge dissipated by R_B is balanced by the integral of the input current during the two given quarter-LO cycles. We also incorporate a temporal shift in the

integration limits of $-T_{LO}/8$ to simplify this and subsequent integrals

$$\begin{aligned} Q_m &= T_{LO}\frac{V_{C,m}}{R_B} \\ &= \int_{m\frac{T_{LO}}{4}-\frac{T_{LO}}{8}}^{(m+1)\frac{T_{LO}}{4}-\frac{T_{LO}}{8}} \frac{V_{RF}-V_{C,m}}{R'_a}\,dt - \int_{(m+2)\frac{T_{LO}}{4}-\frac{T_{LO}}{8}}^{(m+3)\frac{T_{LO}}{4}-\frac{T_{LO}}{8}} \frac{V_{RF}+V_{C,m}}{R'_a}\,dt \\ &= \frac{T_{LO}}{2R'_a}\left(\frac{2\sqrt{2}}{\pi}A\cos\left(\phi+\frac{m\pi}{2}\right)-V_{C,m}\right) \end{aligned} \tag{A.3}$$

Solving for $V_{C,m}$ results in the expression

$$V_{C,m} = \frac{2\sqrt{2}R_B}{\pi(R_B+2R'_a)}A\cos\left(\phi+\frac{m\pi}{2}\right) \tag{A.4}$$

This means that the mixer's output is affected not only by the intensity of the RF input, but also by the antenna's relative impedance R'_a to the baseband R_B. In this scenario, a reradiation current arises as a consequence of voltage disparities between the mixer filter capacitors and the antenna input. The voltage V_x shown in Figure A.1b is consistently linked to one of the output capacitors, giving rise to a stair-step waveform, featuring four phases aligned with the LO phases. To assess the effective impedance experienced by the antenna, it becomes necessary to compute the current flowing from the antenna into the receiver within the time domain.

$$I_A(t) = \frac{V_{RF}(t)-V_x(t)}{R'_a} \tag{A.5}$$

To obtain $I_A(t)$, a Fourier series representation of the signal within the time interval $\mathrm{T_{LO}}$ is employed to isolate the component of V_x corresponding to this frequency. Subsequently, the fundamental term is extracted. Upon substituting Equation A.4 into the waveform, a term for the fundamental frequency at ω_{LO} is derived

$$\begin{aligned} V_{x,fund}(t) &= \frac{8}{\pi^2}\frac{R_B}{R_B+2R'_a}A\cos\left(\phi+\omega_{LO}t\right) \\ &= V_{RF}(\omega_{LO})\frac{8}{\pi^2}\frac{R_B}{R_B+2R'_a} \end{aligned} \tag{A.6}$$

from which

$$\begin{aligned} I_{A,fund}(t) &= \frac{V_{RF}(t) - V_{x,fund}(t)}{R'_a} \\ &= V_{RF}\frac{2R'_a + R_B\left(1 - \frac{8}{\pi^2}\right)}{R'_a(2R'_a + R_B)} \end{aligned} \tag{A.7}$$

Consequently, the original time-varying circuit in Figure A.1a is represented by the linear time-invariant (LTI) model in Figure A.2. This circuit incorporates an impedance transform term and an additional shunt resistance to account for the linear time-varying (LTV) effects caused by the switches. It's important to note that this model reflects power wastage resulting from LO harmonic upconversion through the switches to the antenna. Given the schematic in Figure A.2, the expression of the current I_A is

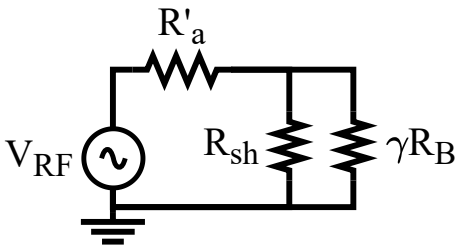


Figure A.2: LTI equivalent circuit for passive mixer with R_{sh} due to harmonics and impedance-transformed R_B.

$$I_A(\omega_{LO}) = V_{RF}(\omega_{LO})\frac{\gamma R_B + R_{sh}}{R'_a\gamma R_B + R'_a R_{sh} + R_{sh}\gamma R_B} \tag{A.8}$$

The equivalent relationship between Equation A.7 and Equation A.8 is imposed to determine the values of the scaling factor γ and the virtual shunt resistance R_{sh}

$$\gamma = \frac{4}{\pi^2} \qquad R_{sh} = R'_a\frac{2\gamma}{1 - 2\gamma} \tag{A.9}$$

It's important to note that the analysis and the model depicted in Figure A.2 remain valid even when R_B exhibits frequency dependence.

Appendix B

LTI equivalent receiver model

Following the methodology outlined in [46], a Linear Time-Invariant (LTI) model for the translational positive feedback receiver is proposed, leveraging the feedback loop gain β.

The receiver depicted in Figure B.1 constitutes a Linear Periodic Time-Varying (LPTV) system, where all components are assumed to be ideal. Similar to the receiver described in 3, a passive down-conversion mixer directs the output current of the LNTA to a baseband filter, with its input node held at a virtual ground. The resistance R_{FB} serves as a Voltage-to-Current converter, and the resulting positive feedback current I_{FB} is fed back to the input node of the LNTA (v_x).

While a first-order filter is depicted in Figure B.1, the analysis remains applicable to filters of any order, characterized by a DC gain R_{BB} and a transfer function of $R_{BB} \cdot H(s)$.

The output voltage $v_{out-I/Q}$ is defined as

$$v_{out} = -i_{BB} R_{BB} H(s) \tag{B.1}$$

where i_{BB} is the down-converted current.

Applying similar assumptions as presented in [47] and in Appendix A, the circuit in Figure B.1 can be approximated by an LTI half-circuit equivalent, particularly for frequencies close to the local oscillator frequency, as depicted in Figure B.2.

Assuming a virtual ground at the input of the baseband filter and considering the resistances of the Up-Conversion (UC) and Down-Conversion (DC)

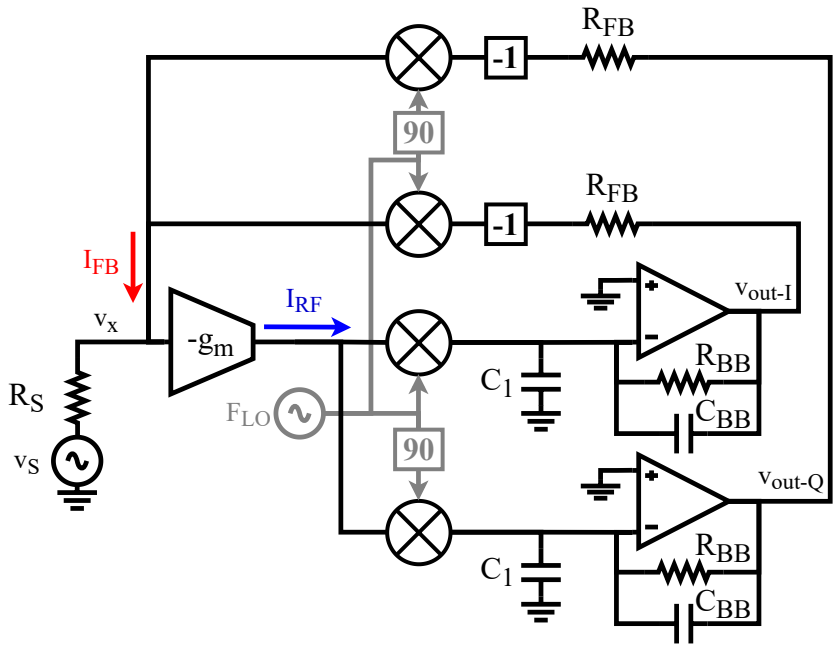


Figure B.1: Schematic of a positive feedback receiver

mixers as

$$r_{sw} = r_{sw-UC} \gg r_{sw-DC} \sim 0 \tag{B.2}$$

the formulations for R'_a and R_{sh} can be derived from Equation A.9 as follows

$$R'_a = r_{sw} + R_s \parallel \frac{1}{g_m} \sim r_{sw} \qquad R_{sh} = R'_a \frac{2\gamma}{1-2\gamma} \sim 4.3 \cdot R'_a \tag{B.3}$$

where the shunt resistance R_{sh} represents the harmonic up-conversion losses occurring in the baseband output.

The loop gain β of the receiver, with $I_{FB} = \beta I_{RF}$ as the feedback current, can be determined by applying Kirchhoff's law at node v_x. This leads to the matching condition

$$\frac{v_x}{v_S} = \frac{1}{g_m R_S(1-\beta)+1} = r_{match} \tag{B.4}$$

from which, once defined the transconductance g_m and the desired matching ratio r_{match}, the value of β is given by

$$\beta = \frac{g_m R_S - 1/r_{match} + 1}{g_m R_S} \xrightarrow{r_{match}=1/2} \frac{g_m R_S - 1}{g_m R_S} \tag{B.5}$$

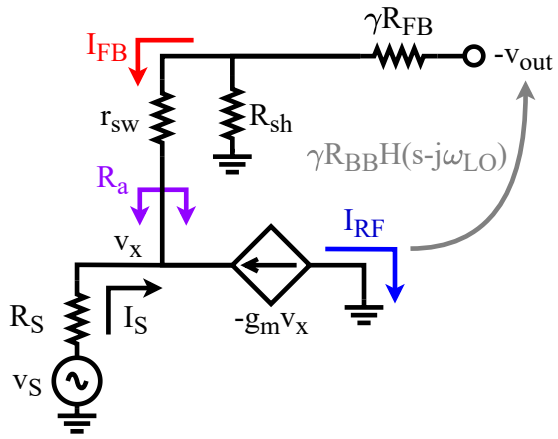


Figure B.2: Equivalent LTI model for the positive feedback receiver

The desired loop gain can be achieved by appropriately selecting the feedback resistance R_{FB}, as defined by

$$R_{FB} = \frac{R_{sh}(\gamma R_{BB} g_m - (\beta g_m r_{sw} + 1))}{\gamma(\beta g_m r_{sw} + \beta g_m R_{sh} + 1)} \tag{B.6}$$

From Equation B.6, another expression for β as a function of the ratio between R_{BB} and R_{FB} can be derived as

$$\beta = \frac{\gamma R_{BB} g_m R_{sh} - (R_{sh} + \gamma R_{FB})}{g_m(r_{sw} R_{sh} + \gamma R_{FB} r_{sw} + \gamma R_{FB} R_{sh})} \sim \frac{R_{BB}}{R_{FB}} \cdot \frac{R_{sh}}{r_{sw} + R_{sh}} \tag{B.7}$$

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