University of Pavia

Ph.D. Dissertation

Modeling and Design of High-Performance DC-DC Converters

Author:
Thomas Eleftherios Dimitrios Kizas

Supervisor:
Prof. Piero Malcovati

Co-Supervisor:
Prof. Andrea Baschirotto

A dissertation submitted in partial fulfillment of the requirements for the degree of

Doctor of Philosophy in Microelectronics

to the

University of Pavia
Faculty of Engineering
Department of Electrical, Computer and Biomedical Engineering
Ph.D. school in Microelectronics

May, 2023

Acknowledgements

Before proceeding with the content of this thesis, I would like to express my gratitude to those who either supported or contributed to the research activity that lead to it.

First of all I would like to thank my supervisors Prof. Piero Malcovati and Prof. Andrea Baschirotto for their invaluable support and guidance throughout this PhD program. I would also like to thank two companies for their collaboration. Synaptics and specifically the group of Lorenzo Crespi in Irvine CA for their support during the first modeling activity. Infineon Technologies and its teams in Padua for their support during the second modeling activity as well as the design, fabrication and evaluation of the current sensor. In particular, I want to thank Giovanni Capodivacca, Luca Scandola and Michele Bergo for their aid during every stage of the above activities, Luca Marini and Marco Flaibani for the training related to the evaluation of the the prototype as well as everyone else who was involved in the integration of the design in a test chip. I also want to thank the Integrated Microsystems and Sensors laboratory of the Department of Electrical, Computer, and Biomedical Engineering of the University of Pavia for providing the equipment and infrastructure that was used to perform the necessary measurements as well as its members for their help in the preparation and troubleshooting of the test setup.

In addition, I want to thank the colleagues from the University of Pavia and the University of Milano-Bicocca that I had the pleasure to meet during this PhD. The interaction with them has been a source of both knowledge and good memories for me.

Last but not least, I would like to thank my parents for instilling me with the love for continuous learning and for supporting me throughout my life and studies.

Abstract

The goal of the research that was pursued during this PhD is to eventually facilitate the development of high-performance, fast-switching DC-DC converters. High switching frequency in switching mode power supplies (SMPS) can be exploited by reducing the output voltage ripple for the same size of passives (mainly inductors and capacitors) and improve overall system performance by providing a voltage supply with less unwanted harmonics to the subsystems that they support. The opposite side of the trade-off is also attractive for designers as the same amount of ripple can be achieved with smaller values of inductance and/or capacitance which can result in a physically smaller and potentially cheaper end product. Another benefit is that the spectrum of the resulting switching noise is shifted to higher frequencies which in turn allows designers to push the corner frequency of the control loop of the system higher without the switching noise affecting the behavior of the system. This in turn, is translated to a system capable of responding faster to strong transients that are common in modern systems that may contain microprocessors or other electronics that tend to consume power in bursts and may even require the use of features like dynamic voltage scaling to minimize the overall consumption of the system.

This work is further focused on the application of automotive buck converters. These converters have wide input voltage range and need to be able to operate with input voltages as high as 40 V and provide a lower (down to 3.3 V) regulated output voltage that their load requires. In a step-down buck converter, the low conversion ratio results in small duty cycle values which when combined with the high switching frequency of the converter results into a strict requirement for the time that the converter has to decide whether it needs to turn off its high-side switch. Lastly, they have to provide power for the significant amount of electronics that are present in a car and therefore, the specification for their load current is also wide and with a maximum in the order of magnitude of several Amperes. These demanding system-level specifications are reflected to the specifications of the analog and digital signal processing blocks that allow the system to monitor its inputs and outputs and properly control its switching behavior to provide a well regulated voltage at its output. Meeting any of the above specifications can be a challenge by itself and achieving them all at the same time is a non-trivial task as some specifications (like the requirement to handle high input voltages) impose design and implementation constraints that negatively impact its performance with respect to the rest.

While the analysis of the open loop behavior of a DC-DC converter is relatively straightforward, it is of limited usefulness as they almost always operate in closed loop and therefore can suffer from degraded stability. Therefore, it is important to have a

way to simulate their closed loop behavior in the most efficient manner possible. The first chapter is dedicated to a library of technology-agnostic high-level models that can be used to improve the efficiency of transient simulations without sacrificing the ability to model and localize the different losses.

This work also focuses further in fixed-frequency converters that employ Peak Current Mode Control (PCM) schemes. PCM schemes are frequently used due to their simple implementation and their ability to respond quickly to line transients since any change of the battery voltage is reflected in the slope of the rising inductor current which in turn is monitored by a fast internal control loop that is closed with the help of a current sensor.

Most existing models for current sensors assume that they behave in an ideal manner with infinite bandwidth and ideal constant gain. These assumptions tend to be in significant error as the maximum response time of the sensor and therefore its settling time requirements are reduced. Some sensing architectures, like the ones that approximate the inductor current with the high-side switch current, can be even more complex to analyze as they require the use of extended masking time to prevent spike currents caused by the switch commutation to be injected to the output of the sensor and therefore the signal processing blocks of the control loop. In order to solve this issue, this work also proposes a current sensor model that is compatible with time averaged models of DC-DC converters and is able to predict the effects of static and transient non-idealities of the block on the behavior of a PCM DC-DC converter.

Lastly, this work proposes a new 40 V, 6 A, fully-integrated, high-side current sensing circuit with a response time of 51 ns. The proposed sensor is able to achieve this performance with the help of a feedback resistance emulation technique that prevents the sensor from debiasing during its masking phase which tends to extend the response time of similar fully integrated sensors.

Contents

List of Figures

List of Tables

Part I

Modeling of the Transient Behavior of DC-DC Converters

1 High-Performance Modeling of Transient Behavior and Losses in DC-DC Converters

Chapter Contents

The first contribution of this work in the field of modeling for high-performance converters is the creation of a library of high-level models for the transient simulation of DC-DC converters that allow the designers to simulate the key current and voltage quantities of a closed loop DC-DC converter as well as the evolution of the different types of losses present in the circuit [1]. Typically, such transient simulations are only possible towards the end of a design iteration after the schematics of the different building blocks have been designed. Therefore, any mistakes in the initial block-level specifications are caught after the design process has progressed and this can result in delays due to the need for additional design iterations. This work gives designers a library of building blocks that allow them to do this even at the stage of the feasibility study while also reducing the required simulation time.

1.1 Previous Work

The speed at which an analog simulator can perform a transient analysis of a switching DC-DC converter is in general slow due to the switching nature of the circuit. As a result, several tools have been developed to provide some speed improvement. Some of them use event-based evaluation and transfer functions [2], others use interpolated component models [3], others focus solely on the frequency response of the converters [4] and there are also tools able to generate models automatically from transistor-level schematics [5]. While some of them achieve a remarkable speedup, they are either unable to estimate losses, require significant user input (derivation of transfer functions)

or they are unsuitable for early-stage designs where transistor-level schematics are unavailable. However, the most interesting category of tools are those which use analog but highly parametrizable macro-models that can be included and simulated directly in a circuit schematic [6], [7]. Such tools allow the designer to use a mix of transistor-level cells and behavioral models in the same circuit and choose different levels of abstraction for each component, while also improving the simulation time. The presented library follows this strategy and is implemented with a combination of standard analog library and custom Verilog-A cells, which can be simulated with an analog simulator.

1.2 Target Specifications for the Library

The models of the proposed library have the following improvements: speed improvement, robustness in terms of convergence, hardware abstraction, ability to model common non-idealities, modularity, interchangeability with transistor-based blocks and possibility to use an analog simulator.

Simulation speed is crucial for high-level models. The time spent to simulate a circuit in an analog simulator depends on two factors. The first factor is obviously the amount and complexity of the calculations that the simulator has to do. The second factor is the time-step used by the analog simulator, which can be affected by the models that are used. The existence of high Q factor, high-frequency parasitic components can force the simulator to reduce the time-step, in the order of magnitude of the period of their resonance frequency. The existence of steep transitions in the functions implemented by the models is another factor that can lead to significant reduction of the minimum time-step used by the simulator. The time to simulate also increases with switching frequency as more cycles and therefore more timesteps have to be processed to simulate the operation of the converter for the same amount of time.

The effect of the models on simulation convergence is also critical. A frequent cause of such issues is the existence of discontinuities in them that can lead to oscillations of the Newton-Raphson method around the discontinuity which forces the time-step to become very small and makes the simulator abort the simulation due to convergence failure. Typical high-level models of switches have such discontinuous behavior, and the current flowing through them changes by several orders of magnitude between their on and off state. Including such a model in the testbench of a DC-DC converter operating in closed loop would cause the simulation to fail.

Hardware abstraction is another useful feature of high-level models. This feature allows the designers to include functional blocks with desirable high-level properties in their schematics without bothering about their implementation-specific parameters

and as a result allows them to have some results before every single block is implemented.

High-level models should also include the most common non-idealities of every block. It is also desirable for such models to be compatible with Monte Carlo and corner simulations. Both goals can be achieved in Verilog-A. The first thanks to the ability to define inherited parameters and define their statistical distribution in additional model files, and the second one by passing the values of the corners as parameters.

Modularity allows the designer to swap behavioral blocks with their transistor-level versions without making significant changes. In the proposed model library the behavioral blocks have the same input and output ports as their transistor implementations to ensure the compatibility.

1.3 Implementation

The library is implemented as a set of macro-models formed by combining Verilog-A modules and standard analog library components. This choice ensures that the cells can be used with any analog simulator that can make use of a Verilog-A compiler that supports a good portion of the functionality specified in the Verilog-AMS Language Reference published by Accellera Systems Initiative [8]. The cells were tested via simulations with the base analog simulator of the Spectre Simulation Platform[9]

1.3.1 Modeling of Switches

The models for the switches are perhaps the most important blocks. Their characteristics (on/off resistance, gate and parasitic capacitances, body diodes) determine the shape of the the inductor current waveforms and also the distribution of losses in the converter. The macro-model of a switch, shown in Fig. 1.1, consists of the model of a semi-ideal switch, a diode and, depending on the amount of required accuracy, blocks which emulate the behavior of the capacitors.

The body diode of the switch, is an ideal block with exponential I_D-V_D characteristic. This component is needed for correctly modeling bulk CMOS switches, since their body diodes are actually forced to turn on if the voltage on node X falls outside the range between ground and the battery voltage. This simple model was proven to be adequate for the designs that were investigated.

The capacitors model the parasitic capacitances seen on each side of the switch transistor. If the effect of ringing on the parasitic RLC circuits present in the power train of the converter is considered negligible, then a model without these capacitors can be

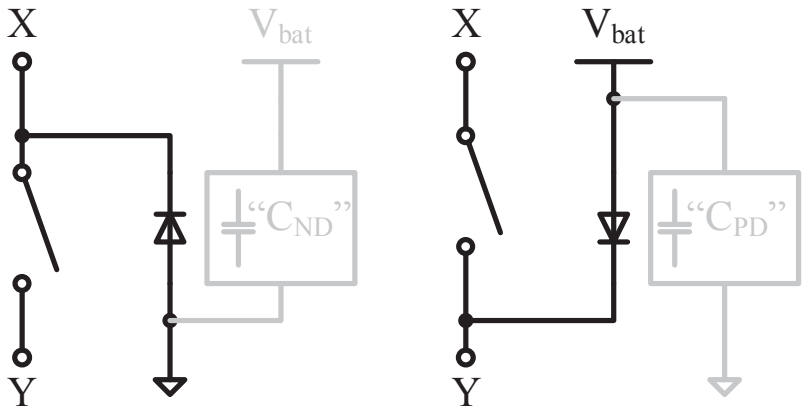


Figure 1.1: NMOS and PMOS switch macro-models

used to increase the speed of the simulation. However, the lack of parasitic capacitances at node X can lead to convergence difficulties. In such case a small capacitance has to be considered.

The semi-ideal switch has been implemented in two different ways. The models can replace a switch which is connected to one of the power supply rails, like any of the two PWM switches in a buck converter. All the model versions are based on continuous functions with continuous derivatives to ensure good convergence. The high-level blocks model the transistors as ideal voltage-controlled switches with a finite on and off resistance. The first parameter contributes to the ohmic losses and inductor current non-linearity while the second contributes to the leakage losses. Accurate modelling of the resistance between the two states was not considered a target as transition losses can be estimated without knowing its exact value.

The first version of the model is the most adaptable. It is based on the smootherstep function given by

$$f(x) = \begin{cases} 0 & x \leq 0 \\ 6x^5 - 15x^4 + 10x^3 & 0 \leq x \leq 1 \\ 1 & x \geq 1 \end{cases} \tag{1.1}$$

The smootherstep function Eq. 1.1 is polynomial, connects the x,y pairs (0,0) and (1,1) in a smooth way and has found application as an interpolation function in computer graphics applications [10], [11]. This function is also monotonic within the boundaries of the transition window and its first and second derivatives reach 0 at the edges of the window $f'(0) = f'(1) = f''(0) = f''(1) = 0$, which ensures that the function is smooth

even at the edges of every segment of its definition. The function was adapted as

$$R_{sw}(V_c) = \begin{cases} R_{off} & V_c \leq V_l \\ R_{on} + (R_{off} - R_{on}) \cdot y & V_l \leq V_c \leq V_r \\ R_{on} & V_r \leq V_c \end{cases} \tag{1.2}$$
$$y = 6{V_c}^5 - 15{V_c}^4 + 10{V_c}^3$$
$$V_c = 1 - (V_{sw\_c} - V_l)/(V_r - V_l)$$

The adaptations are required to adjust the minimum and maximum values of the y axis and the width and the center of the transition window, while still retaining the desirable properties of the original function. The adapted smootherstep function uses the on and off resistance of the switch, R_{on} and R_{off}, the threshold of the control voltage for state change V_{trans} and the width of the transition window $2 \cdot \Delta_X$ as parameters. The voltage of the control node V_{sw_c} is used as an input. Based on these parameters the left and right edges of the transition window V_l and V_r are given by

$$V_r = V_{trans} + \Delta_X, \qquad V_l = V_{trans} - \Delta_X \tag{1.3}$$

One weakness of the smootherstep-based model is the use of flat tails of its $R_{sw}(V_c)$ characteristic. In general, this is considered a risky modeling strategy as it can lead to an element that allows the simulator to accept multiple solutions of the same circuit which may not be really close to each other. For example, the simulator can accept for the same timestep solutions that assume $R_{sw} = R_{on}$ that have completely different values of V_c as long as they are above the threshold V_{trans}. In theory, this can lead to odd behavior or extended simulation time as the solver is searching between radically different solutions for the circuit between Newton-Raphson iterations. While no convergence issues had been encountered with the smootherstep-based switch while using it, it was decided to introduce a second version of the high-level switch with the same features but no flat tails. The resulting model allows for fast simulation time, without creating convergence difficulties.

The second version of the model is based on a logistic sigmoid function, given by

$$f(x) = 1/(1 + e^{-x}) \tag{1.4}$$

This function is exponential, connects the x,y pairs (0,0) and (1,1) in a smooth way and is frequently used as an activation function in artificial neural networks [12]. The function

is monotonic everywhere and has continuous derivatives. Its adapted version

$$R_{sw}(V_{sw\_c}) = R_{on} + \frac{R_{off} - R_{on}}{1 + e^{SF_{both}\left(V_{sw\_c} - \frac{V_r + V_l}{2}\right)}} \tag{1.5}$$

$$\begin{aligned} SF_{top} &= 2 \cdot ln\left(\frac{R_{off} - R_{on}}{R_{tol}} - 1\right) /(V_r - V_l) \\ SF_{bot} &= -2 \cdot ln\left(\frac{R_{off} - R_{on}}{R_{off} - R_{on} - R_{tol}} - 1\right) /(V_r - V_l) \\ SF_{both} &= max(SF_{bot}, SF_{top}) \end{aligned} \tag{1.6}$$

has adjustable minimum and maximum values of the y axis, as well as width and center of the transition window, while still retaining the desirable properties of the original function. The parameters given to this model set the on and off resistance, R_{on} and R_{off}, the voltage threshold for the state transition V_{trans}, the width of the transition window $2 \cdot \Delta_X$ and an "absolute tolerance" value R_{tol}. Since the function is purely exponential it can only asymptotically approach the values of R_{on} and R_{off}. Therefore, the parameter for absolute tolerance is used to set the maximum distance from their ideal values. This model is more computationally efficient than the smootherstep-based and is preferable as long as the designer considers its asymptotic behavior acceptable.

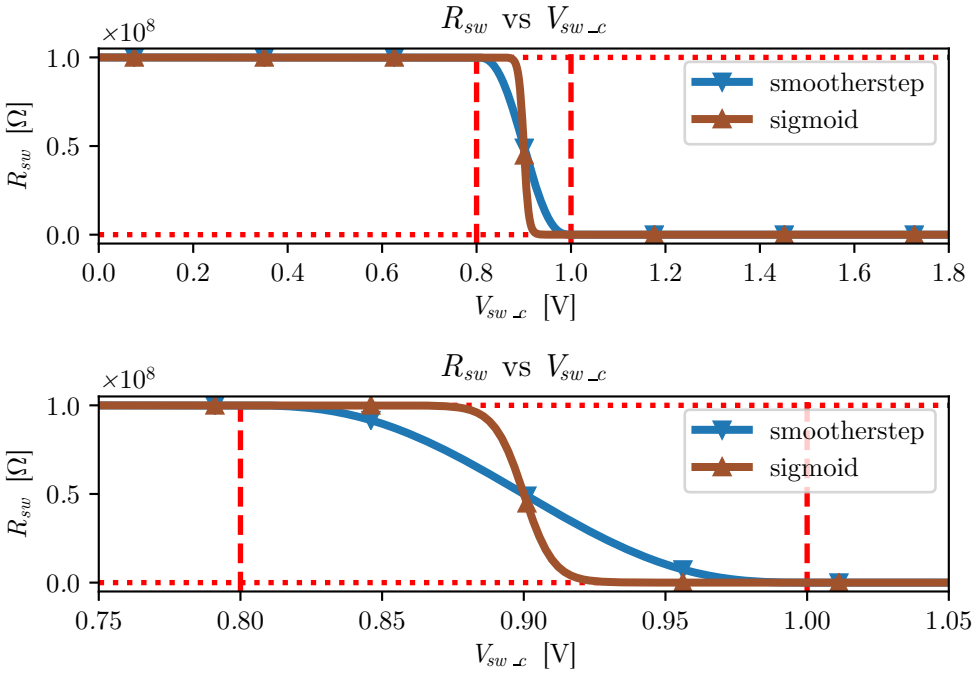


Figure 1.2: Adapted smootherstep and adapted sigmoid for a transition window of 0.2 V, $R_{tol} = 0.5\ \Omega$, $R_{on} = 0.5\ \Omega$, $R_{off} = 100\ M\Omega$.

A plot of the two functions is shown in Fig. 1.2. Both versions allow the designer to perform parametric sweeps as well as Monte Carlo simulations targeted to the values of their on and off resistance.

1.3.1.1 Limitations of the Model

While easy to handle by the simulator and abstract enough to be useful to designers these models have limitations that prevent them from being used as a universal replacement of the power transistors in testbenches that support transient analysis. The first limitation is imposed by the design choice to implement the switch models as a voltage controlled resistors that mainly switch between two different values of resistance (R_{on} and R_{off}). This choice reduces the importance of modeling the resistance between R_{on} and R_{off} with high accuracy as these transitions last for a negligible part of a switching period and even then they do not affect the overall switching losses significantly as slow-switching capacitive losses depend only on the size of the load capacitance and the change of voltage across it between the different switching phases. Furthermore, this simplification makes it easier to keep R_{on}, R_{off}, Δ_x and V_{trans} parametrizable at the same time while ensuring that there is no loss of continuity in the model equations. The drawback from this is that the switch models cannot substitute the models of transistors that are supposed to work as linear pass elements like the main switch of an LDO and they may lose accuracy when included in a converter architecture that employs very weak driving of the power switches (a non-standard practice). Lastly, they are less useful for AC analysis as the $R_{sw}(V_c)$ curves are not fitted to the $R_{ds}(V_{gs})$ curves of a transistor..

Another limitation is the fact that the control voltage of the switches is defined as the voltage between the gate and a fixed terminal that is considered the source of the transistor. While intuitive, this choice leads to error when trying to model the operation of load-side switches in a SIMO converter where the high/low voltage terminal (and therefore the electrical source/drain) of the PMOS/NMOS switch changes during operation and this can lead to the switch opening or closing when it should not.

1.3.1.2 Proposed Solution for Load-Side Switches

The problem of modeling the load-side switches while retaining all the features of the cells that are currently present in the library is not trivial. The straightforward solution to decide on the fly which terminal of the model is going to be considered as the source of the transistor does not work well due to the fact that the conditional statement can effectively change the terminal that it considers as a source between timesteps, and this

change can also happen during a switch transition which can make the solver bounce between solutions where the switch takes significantly different values of resistance. The safest alternative is to use a model that does not contain any conditional statements, takes into account the voltages of both switch terminals at the same time and "selects" the relevant one arithmetically through clever use of logarithmic and exponential functions as in the compact transistor models of EKV [13]. The main challenge of this approach is the difficulty in introducing the abstract parameters of on/off switch resistance and the transition window into a model that has been built to work with transistor-level parameters in mind.

1.3.2 Modeling of Gate Drivers

The switch drivers are inserted between the control circuit and the gates of the switches and have a dual role. Firstly, they ensure that switches change state sufficiently fast despite the large size of their gate capacitance. Secondly, their power supply pin acts as a port through which the designer can measure the power spent to turn on and off the switches.

The first goal is very easy to achieve in a behavioral model by representing the driver as a digital buffer with a specific propagation delay. The second goal is slightly harder to achieve since the ability to estimate the gate driving losses requires the knowledge of the total load capacitance as well as a structure which allows a straightforward way to access the quantities needed to estimate the power. As a result, the proposed model library also contains driver-switch bundle cells (Fig. 1.3), which can be used for simulations targeted to estimating the efficiency of the converter. The bundles contain capacitors to model the gate capacitance of the switch and the self-loading capacitance of the drivers, as well as the switch and driver models. The driver model is implemented with switch models whose on-resistance is adjusted based on the capacitor value to ensure sufficiently fast charging. Also in this case parametric and Monte Carlo simulations can be performed provided that the user includes a file that describes the deviation of switch resistance with process variations.

1.3.3 Eliminating Speed Degradation in DCM

Simulating DCM operation of an inductive DC-DC converter in the presence of parasitic capacitors on the side of the switches can lead to an extension of simulation time due to parasitic ringing. This is due to the existence of a high quality parasitic RLC circuit formed by the combination of the inductor and capacitor of the output filter and the parasitic capacitances of the switches. The resonant frequency can be in the order of

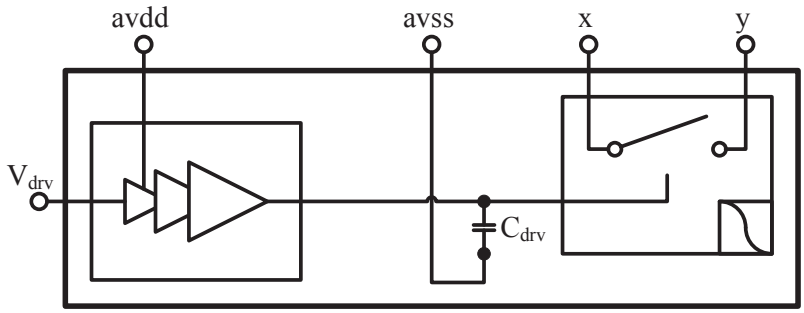


Figure 1.3: An example of a switch-driver bundle.

magnitude of 10s of MHz to a few GHz for fully integrated converters that use small inductors and this forces the calculation of a lot of additional timesteps towards the end of every switching cycle. Since the dead-time of a DCM cycle starts with approximately 0 inductor current it is safe to assume that the energy stored in the parasitic circuit is negligible when estimating the losses of the converter. In order to eliminate this form of inefficiency this work also proposes the use of an additional block that places a resistor in parallel of the inductor to dissipate the energy stored in the parasitic circuit once the dead time starts and removes it before a new cycle is about to start.

1.3.4 Control Blocks

The models for the control sub-system of a DC-DC converter include a number of commonly used analog blocks and logic, like comparators, zero-current detectors, delay generators, non-overlapping signal generators and analog filters. The models also provide parameters for common non-idealities like offset and delay, and allow parametric and Monte Carlo simulations.

1.4 Performance of the model library

To evaluate the performance of the model library the schematic of a Single Inductor Multiple Output converter shown in Fig. 1.4 was assembled. Two versions of the above schematic were used, one using the high-level models of the switches and one with the SPICE models of the actual transistors. Tab. 1.1 summarizes the model used for each block shown in the scheme. The circuit was simulated with a SPICE-like simulator and the following results were acquired.

The accuracy of the models can be appreciated in the results of the transient simulation shown in Fig. 1.5. The waveforms produced by the models are almost identical to the ones generated by the simulation with transistor-level models. The most observable

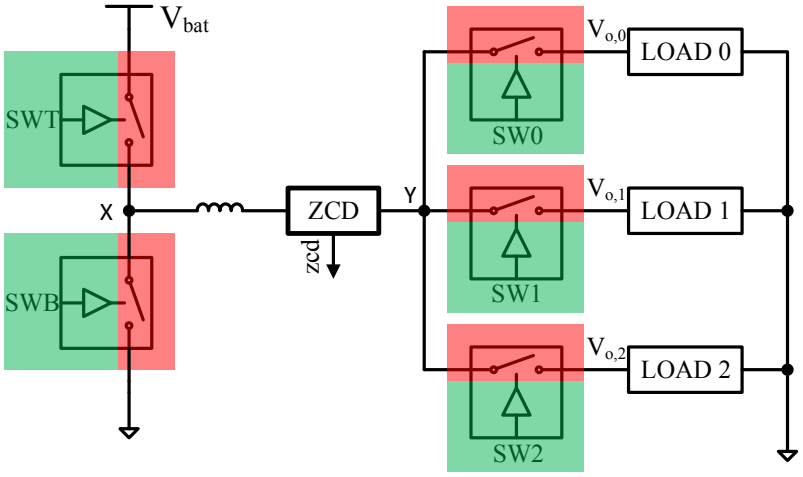


Figure 1.4: Example of a SIMO buck converter used as an example in this paper. The control logic is not shown. The drivers and switches were implemented as single blocks.

Table 1.1: Testbench implementation

Block name	Implementation	
	SPICE testbench	***HLM testbench***
SWT	driver-transistor bundle inverter-chain driver PMOS switch	driver-transistor bundle HLM driver HLM switch
SWB	driver-transistor bundle inverter-chain driver NMOS switch	driver-transistor bundle HLM driver HLM switch
SW0	driver-transistor bundle HLM driver NMOS switch	driver-transistor bundle HLM driver NMOS switch
SW1	driver-transistor bundle HLM driver NMOS switch	driver-transistor bundle HLM driver NMOS switch
SW2	driver-transistor bundle HLM driver NMOS switch	driver-transistor bundle HLM driver NMOS switch
ZCD and other control blocks	HLM cells	HLM cells

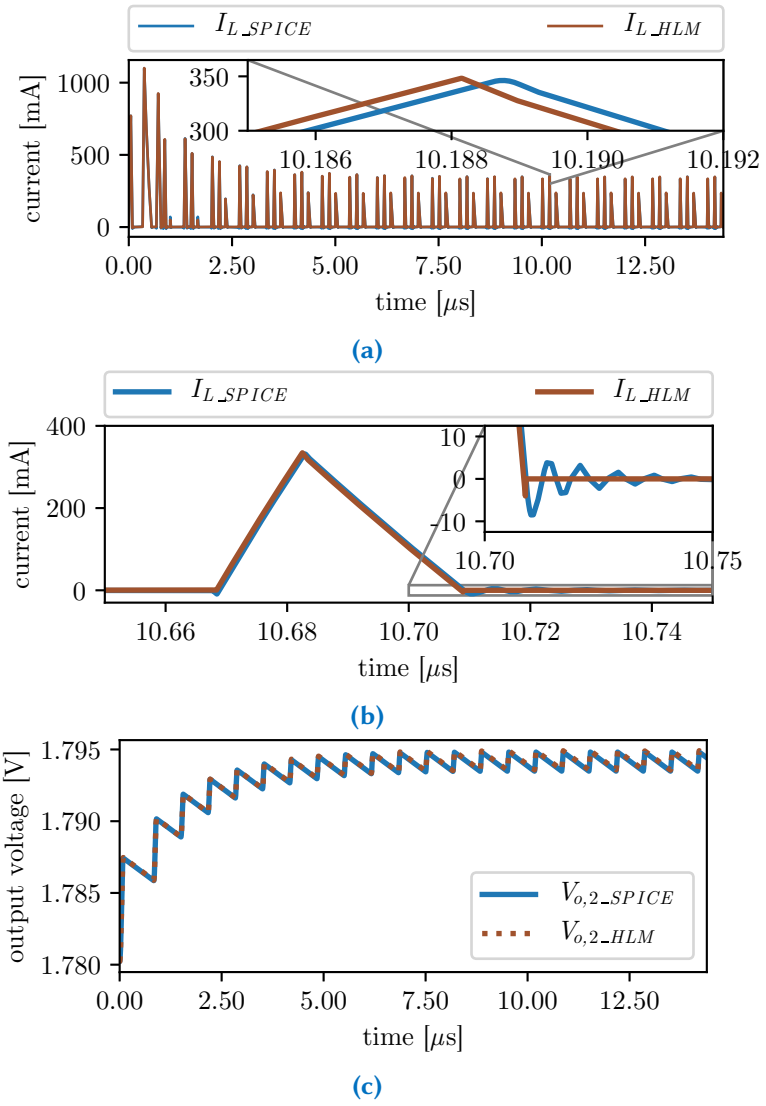


Figure 1.5: Comparison of transient simulation results for (a) inductor current, (b) inductor current (zoomed), (c) output voltage.

difference is a time-offset due to the delay between the application of a voltage on the gate of the transistor and its actual change of state. However, even this type of error can be compensated by introducing a matching delay in the model of the driver. The waveforms generated with the sigmoid and the smootherstep switch are identical.

Thanks to their simplicity the models can be simulated in just a fraction of the time required for the simulation with transistor-level models, as shown in Tab. 1.2. The observed speed improvement for a testbench with no inductive elements which can cause ringing is between 3 and 5 times.

Simulations of testbenches implementing the whole SIMO converter of Fig. 1.4 with the implementation given in Tab. 1.1 show that using the driver and switch cells of the

library allows for a speedup of approximately 2× as shown in Tab. 1.3.

Table 1.2: Transient simulation time for single switch (10^5 on-off cycles)

Type of switch	Simulation time
NMOS	491 s
PMOS	458 s
smootherstep-based	127 s
sigmoid-based	90 s

Table 1.3: Relative performance of mixed testbench and HLM testbench

Testbench	Simulation time
Mixed	78 s
HLM sigmoid	38 s
HLM smootherstep	38 s

1.5 Summary

A library of high-level macro-models of blocks (switches, drivers and control blocks) which are frequently used in the design of DC-DC converters has been presented. The models are parametrizable, take into account common non-idealities of the blocks and can be simulated with an analog simulator. The cells of the library allow for the simulation of mixed circuits containing instances of high-level library cells and cells based on SPICE models, also performing parametric and Monte Carlo simulations. The cells used for the drivers and switches can provide a speedup of at least 2× in the simulation of a triple output SIMO converter compared to a schematic with SPICE-level transistor models and drivers while retaining the error in the estimation of losses below 20% and the efficiency below 1%.

Part II

Modeling and Design of Fast-Response Current Sensors for Current-Mode DC-DC converters

2 High-Performance Modeling of Current-Sensor non-Idealities

Chapter Contents

2.1 Introduction

One of the early goals during the design of a custom DC-DC converter is to assess the ability to meet the specifications with a specific architecture and determine suitable preliminary values for the corresponding design parameters. The parameters that affect the efficiency and output power of the converter, can usually be estimated with the help of easy to derive hand calculations and validated through short transient simulations of the circuit operating in its steady-state. However, a DC-DC converter usually operates as a closed-loop system and, its stability has to be ensured for the nominal case as well as in the presence of non-idealities. Nonetheless, the switching nature of a DC-DC converter does not allow the direct application of simple analog control techniques. Nevertheless, it is possible to find models for Current-Mode (CM) DC-DC converters in literature [14]–[19] which allow the description of the system in a form that enables the use of the above techniques to design the required loop compensation without having to run time-consuming simulations. While easy to use, and able to provide the designer with acceptable ranges of design parameters, the above models do not take into account circuit non-idealities that can still compromise the stability of the system. The influence of static component non-idealities on CM or similar control schemes is taken into account by some tools based on state-space models [20], [21]. Still, non-idealities related to the current sensing of DC-DC converters tend to be ignored by most known models even though they can visibly affect stability. Two notable exceptions are [22] and [23]. In [22], the authors investigated the effect of time constant mismatch in DCR-based current sensing and extended a typical model for a Peak Current-Mode (PCM) converter by introducing an additional scaling factor for

the slope of the sensed current. [23] deals with the effect of the finite bandwidth of the current sensor on sub-harmonic oscillations by introducing the sensor bandwidth in the state-space equations and then calculating the minimum required compensation slope to define the boundary for sub-harmonic oscillations. However, these are not the only sensor non-idealities that can affect the behavior of the converter. Two of them are the non-linear sensor gain and the transient (time-varying) errors that occur due the appearance of additional parasitic currents when the high-side switch closes. This chapter proposes a computer-aided model architecture that allows large-signal averaged models of DC-DC converters to predict the effects of finite sensor bandwidth, non-linear sensor gain and parasitic current transients on stability. The new model is verified in a testbench focused on a converter operating in PCM while using a high-side current sensor.

2.2 Purpose of the work

As mentioned above, the typical implementations of averaged DC-DC models are rather ideal and cannot be used to predict the consequences of non-idealities like the non-linear current-sensor gain and the effect of transient phenomena like finite bandwidth or the current spikes that appear when the high-side switch closes. These phenomena can directly affect the duty cycle of converters employing CM control schemes and can change the effective gain of the current sensor and, as a consequence, the dynamic behavior of the control loop. The goal of this work is to provide a tool with the following features:

- It can model the impact of the above phenomena on stability which is a feature that commonly used models lack.
- It is compatible with analog simulators and does not require the use of dedicated simulation tools.
- It is compatible with AC/stability/loop-gain analysis. Thanks to this feature, it is possible to extract the value of the phase margin and use it to evaluate the stability of the converter around an operating point.
- It can find operating points of the converter quickly through efficient transient simulations. Small-signal analysis requires the calculation of an operating point which cannot be estimated via DC analysis in a switching testbench. Transient analysis can deal with switching circuits but is slow so a model capable of speeding

up this process is useful. Additionally, the resulting operating point should be in a form directly usable by the small-signal model.

- If possible, it accepts different parametrizable shapes for the transient errors. Their exact shape can vary significantly based on the design parameters and this shape determines how much these errors can affect the stability of the converter. Therefore, it is necessary to have a way to adjust the behavior of the model in an easy and clean way if the shape of the error changes.

A tool with the above features can be of significant help in the design of high-frequency and high-conversion-ratio CM converters that can be significantly affected by the above mentioned current sensor non-idealities.

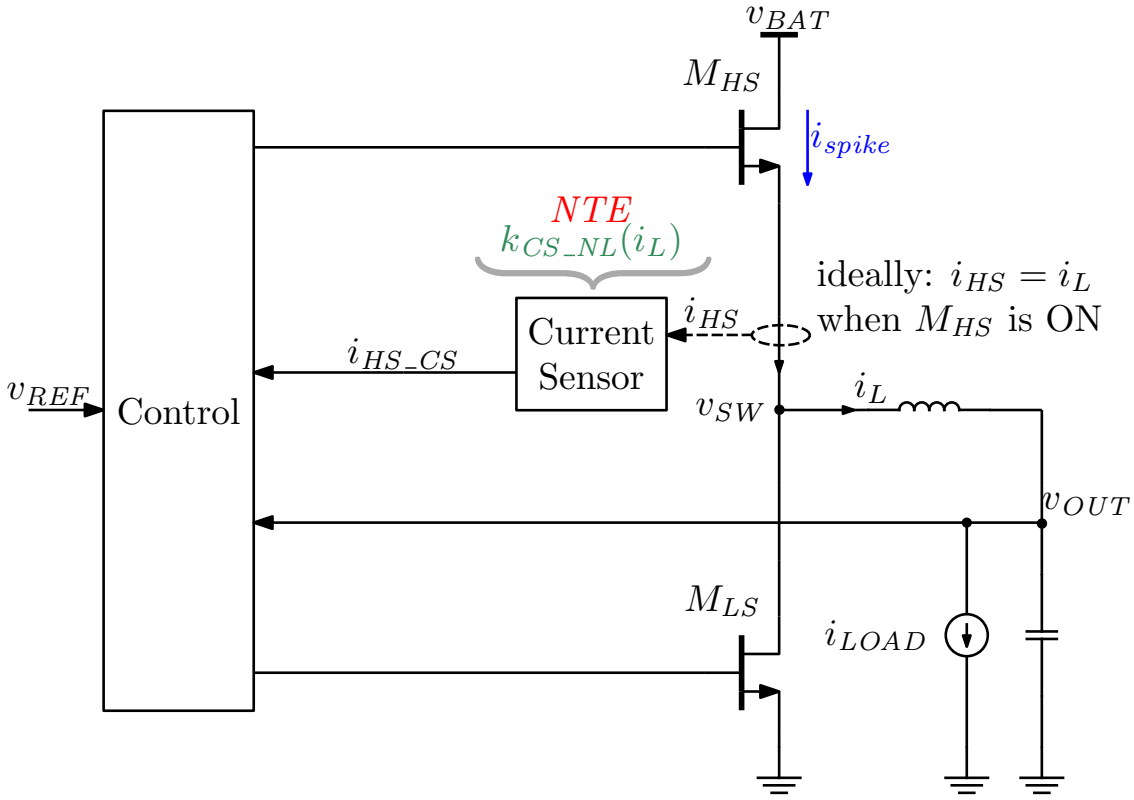


Figure 2.1: A buck converter, key quantities and the physical locations of Negative Transient Error (NTE), non-linear static gain (kcs_{NL}) and the spike current i_{spike} flowing through the high-side switch.

2.3 Proposed model

First of all, it is important to see how current sensing and the related errors work in the context of CM control. The current sensor is the block that is used to close the current

loop by providing a scaled version of the inductor current to the PWM generator of the modulator. If the gain of the current loop is sufficient, the double pole of the output filter of the converter is split into two real poles and leads to a system that is easier to stabilize. The simple schematic of Fig. 2.2 can be used to describe the behavior of the internal (current) loop of a typical current mode control system and the concept of filter pole splitting. K_m is the modulator gain, R_s is the sensing resistance, G_i is the gain of the current sense amplifier, C_O and R_O the output capacitance and equivalent load resistance, V_{SW} and V_O the voltage of the switching node and the output, and lastly V_C is the control voltage of the modulator, which is going to be generated by the voltage error amplifier that forms the external (and much slower in general) voltage loop. If the initial conditions are ignored for simplicity it is possible to derive the following equations in s-domain: Eq. 2.1 describes the behavior of the modulator, Eq. 2.2 the behavior of the inductor current and Eq. 2.3 the behavior of the voltage at the output. Then the control to output transfer function $\frac{V_O}{V_C}$ of this loop needs to be calculated so that it can later be combined with that of the external voltage control loop to model the behavior of the full system. The final transfer function is Eq. 2.4 and has one interesting feature: Its poles, given in Eq. 2.5, can become real and far enough from each other to make the transfer function of the current loop stable. If the product $K_m \cdot G_i$ is large enough, the sum under the square root can become positive and then we have the two poles of Eq. 2.6 and Eq. 2.7. The first depends on the load and the output capacitance, is slow, and is usually named as the "capacitor pole" as it depends on C_O. The second one becomes faster the higher $K_m \cdot G_i$ is, depends on L which leads to it being referred to as the "inductor pole". This pole splitting means that the designer does not have to deal with the typical double complex pole of the L-C filter anymore by implementing extra zeros in the voltage control loop to make the overall loop stable and can still use the ability to read the inductor current to implement necessary protection mechanisms (like overcurrent and load-short protection) without the requirement to add extra sensors. Instead, the gain of the current sensor ($G_i \cdot R_s$) can be used as an extra design variable that has the ability to affect the dynamic behavior of the converter.

$$V_{SW}(s) = K_m \cdot (V_c(s) - i_L(s) \cdot R_s \cdot G_i) \tag{2.1}$$

$$i_L(s) = \frac{V_{SW}(s) - V_O(s)}{L \cdot s + R_S} \tag{2.2}$$

$$V_O(s) = i_L(s) \cdot \frac{R_O \frac{1}{C_o \cdot s}}{R_O + \frac{1}{C_o \cdot s}} \tag{2.3}$$

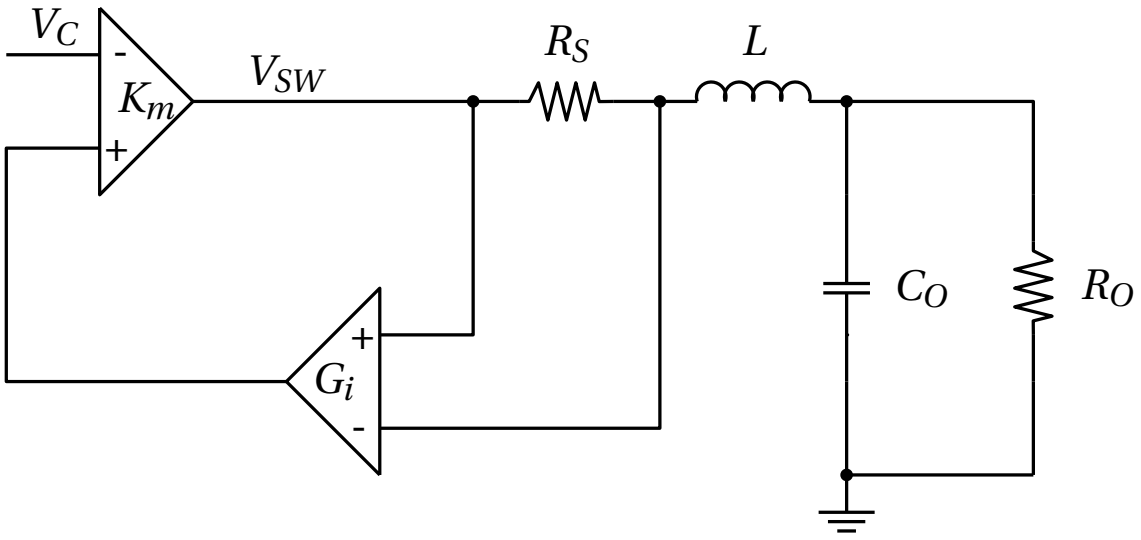


Figure 2.2: A very simplified version of a current mode control scheme

$$\frac{V_O}{V_C}(s) = \frac{K_m \cdot R_O}{C_O \cdot G_i \cdot K_m \cdot R_O \cdot R_S \cdot s + C_O \cdot L \cdot R_O \cdot s^2 + C_O \cdot R_O \cdot R_S \cdot s + G_i \cdot K_m \cdot R_S + L \cdot s + R_O + R_S} \tag{2.4}$$

$$\begin{aligned} p_{0,1} = &-\frac{G_i \cdot K_m \cdot R_S \cdot C_O \cdot R_O + R_S \cdot C_O \cdot R_O + L}{2 \cdot C_O \cdot R_O \cdot L} \\ &\pm \frac{\sqrt{(G_i \cdot K_m \cdot R_S \cdot C_O \cdot R_O + R_S \cdot C_O \cdot R_O - L)^2 + 4 \cdot R_S \cdot C_O \cdot R_O \cdot L}}{2 \cdot C_O \cdot R_O \cdot L} \end{aligned} \tag{2.5}$$

$$p_0 = -\frac{2 \cdot L}{2 \cdot C_O \cdot R_O \cdot L} = -\frac{1}{C_O \cdot R_O} \tag{2.6}$$

$$p_1 = -\frac{2 \cdot C_O \cdot R_O \cdot (G_i \cdot K_m \cdot R_S + R_S)}{2 \cdot C_O \cdot R_O \cdot L} = -\frac{G_i \cdot K_m \cdot R_S + R_S}{L} \approx -\frac{K_m \cdot G_i \cdot R_S}{L} \tag{2.7}$$

However, this simplified model does not capture the full behavior of an ideal implementation of CM DC-DC converter. The current loop also introduces additional terms to the transfer function of the system due to the implicit sampling that is applied on the current the moment that the sensed current triggers a change in the output of the PWM generator, and this can lead to undesirable sub-harmonic oscillations if the sensor gain pushes the inductor pole too far. The above dynamic behavior is modeled by the popular model of [15] which is the primary reference of this chapter. The effective large-signal value of the sensor gain plays a role in determining the state of the control

loop and lead it to an operating point where the system dynamics are different. Eq. 2.8 is derived by substituting $S_f = R_i \cdot V_O/L$ and $D' = 1 - D$ in Eq. 12 of [15] and gives an idea of how a change in the gain of the current sensor R_i (k_{CS} in this work) alters the steady-state behavior of the current loop and forces a change in the duty cycle for a given value of V_c (treated as a current i_{GM_C} in this work). It also becomes obvious that any significant dependence of the sensor gain on either $< i_L >$ or the duty cycle needs to be predicted by a model to avoid high error in the calculation of the steady-state of the control loop.

$$R_i \cdot \langle i_L \rangle = V_c - D \cdot T_s \cdot S_e - \frac{V_O \cdot R_i \cdot (1 - D) \cdot T_s}{2 \cdot L} \tag{2.8}$$

Another consequence of varying large-signal gain is that the values of important small-signal parameters (like the slope of the sensed current) can change as well. The effect of this change on the behavior of the converter around an operating point can be explained with the help of a formal analysis of the dynamics of the current loop in CM control with the help of an averaged small-signal model like the one given in [15] and [16]. In [15] the current sensor is considered ideal and is modeled after a constant gain that is included in S_n (the slope of the sensed current when the inductor current i_L is rising) and is proportional to the current sensor gain k_{cs}. The effect of this gain on the stability of the current loop can be deduced by observing the behavior of the control to output transfer function as the value of this term changes. The low-frequency characteristics of the transfer function (given by $F_p(s)$) as well as the dynamics that are caused by the current sampling behavior of the converter (given by $F_h(s)$) are affected by parameter m_c. Its value is given by $m_c = 1 + \frac{S_e}{S_n}$ where S_e is the slope of the compensation ramp which is used to prevent sub-harmonic oscillations for duty cycles above 50%. Based on this analysis and the assumption of a fixed slope S_e, any increase in small-signal gain due to current sensing non-idealities reduces m_c and in turn slows down the pole of $F_p(s)$ while increasing the quality of the complex conjugate poles of $F_h(s)$ and increasing the likelihood of sub-harmonic oscillations. Similarly, any decrease of the sensor gain speeds up the $F_p(s)$ pole while splitting the 2^{nd} order pole of $F_h(s)$ further with the side-effect of pushing the slower one to lower frequencies. The above analysis shows that averaged models for CM buck converters can predict the effect of current sensor gain in the stability of the converter. Furthermore, previous work [22] has shown that the effect of systematic current sensing errors caused by sensor dynamics, like the time-constant mismatch within the sensing structure of a DCR-based current sensor, can be boiled down into a modified gain value that can in turn be used with typical DC-DC models. This work, focuses on errors that have a behavior that is less linear and this

prevents the derivation of a similarly simple model without introducing significant error. Instead, it presents a model structure that enables the the input-output relationship of the sensor in a form that is compatible with a large-signal averaged model of a PCM DC-DC converter and uses the analog simulator to implicitly estimate the correct large and small-signal gain values at any meaningful transient or steady-state operating point and predicts the behavior of the converter by exploiting its ability to solve systems of non-linear equations.

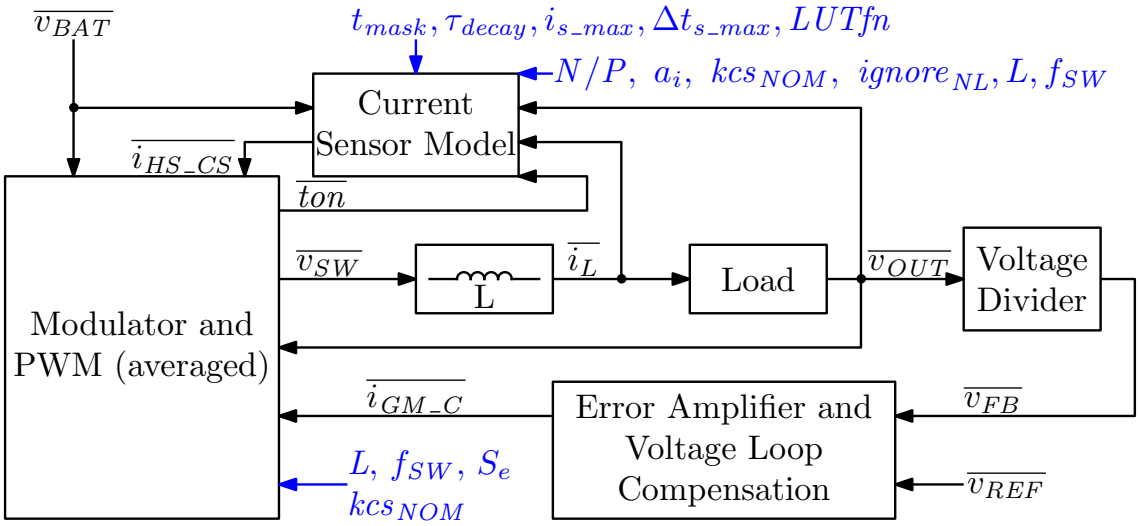


Figure 2.3: The current sensor model in the averaged testbench. The quantities in blue font are parameters.

The proposed model takes into account 3 types of errors related to current sensing that can be detected in a typical buck setup like the one shown in Fig. 2.1. The first two errors, the error due to the static non-linearity of the current sensor kcs_{NL} and the Negative Transient Error (NTE), are caused by inherent non-idealities of the current sensor and affect most CM converters. Non-linear gain is a common non-ideality of sensing circuits while NTE is the error caused by the finite bandwidth of the sensor and the masking of its output due to the use of blanking. This setup also assumes that the converter employs high-side current sensing and is susceptible to an additional parasitic current i_{spike} which appears when the high-side switch turns on and it is injected as a Positive Transient Error (PTE) into the sensed current. The new current sensor model is designed to complement the functionality of the averaged model of the DC-DC converter in a setup as the one shown in Fig. 2.3 that maps the behavior of the buck of Fig. 2.1. The two switches of the original scheme are eliminated and their behavior is represented by the modulator of the averaged model. The functionality of the control block is provided by the combination of the voltage divider, the error amplifier, the volt-

age loop compensation and the part of the averaged model block that calculates the duty cycle. The implementation of this block is based on Eq. 12 of [15] and the large-signal $\frac{V_{sw}}{D}$ gain for buck converters with V_g and V_o (v_{BAT} and v_{OUT} in this work) accessed directly through the corresponding inputs of the module. Lastly, the current sensor is replaced in Fig. 2.3 by the proposed model.

The functionality of this model setup can be summarized as follows. All the quantities that exist in the context of the averaged model are marked with an overbar in equations, text or figures to differentiate them from the corresponding quantities that belong to the normal switching testbench. The averaged dc-dc block uses the output of the voltage loop compensation $\overline{i_{GM\_C}}$, the sensed current of the high-side switch $\overline{i_{HS\_CS}}$, the battery and output voltages $\overline{v_{BAT}}$ and $\overline{v_{OUT}}$, and produces the analog outputs of the switching node voltage $\overline{v_{SW}}$ and the estimated length of the on-time of the high-side switch $\overline{ton}$. The model of the current sensor uses 4 analog inputs, the inductor current $\overline{i_L}$, the value of $\overline{ton}$ that is produced by the averaged block and the battery and output voltages $\overline{v_{BAT}}$ and $\overline{v_{OUT}}$ and generates the analog output $\overline{i_{HS\_CS}}$ that represents the read-out current. The inputs in blue font are the parameters of the model and are detailed below along with the structure of the model. The structure of the current sensor model is shown in Fig. 2.4. The model is comprised by 3 sub-blocks (shown as rectangles with dashed outline in the figure), one for every type of error being modeled. Every block is also implemented as an analog function and this allows the user to swap the model of an error by simply replacing an existing analog function with a new one. The inner workings of every one of these blocks is being detailed in their dedicated subsection.

The first sub-block on the bottom side is used for the modeling of the non-linearity of the static gain of the sensor and requires the analog input of the inductor current $\overline{i_L}$ and the parameters a_i to produce the value of the corresponding non-linear gain $kcs_{NL}(\overline{i_L})$. If the binary parameter $ignore_{NL}$ is 1 the above calculated value will be used in any calculations that require the value of the gain. If it is 0 the nominal gain given by parameter kcs_{NOM} will be used instead.

The second sub-block on the top left is used to model the NTE. It uses 4 analog inputs, the inductor current $\overline{i_L}$, the on-time $\overline{ton}$ and the voltages $\overline{v_{BAT}}$ and $\overline{v_{OUT}}$ and 4 parameters, the self-inductance of the power inductor L, the switching frequency f_{SW}, the decay time constant of the error τ_{decay} and the masking time t_{mask}. The sub-block produces a value of the NTE $i_{NTE}(\overline{ton})$ in the form of an additive error.

The third sub-block on the top right is used to model the PTE and is more relevant in architectures that employ high-side current sensing. It requires $\overline{ton}$ as its single analog input and the parameter of masking time t_{mask} and 3 or 1 additional parameters depending on whether the user opts to use a LUT-based or a fitted model. In the first case, a

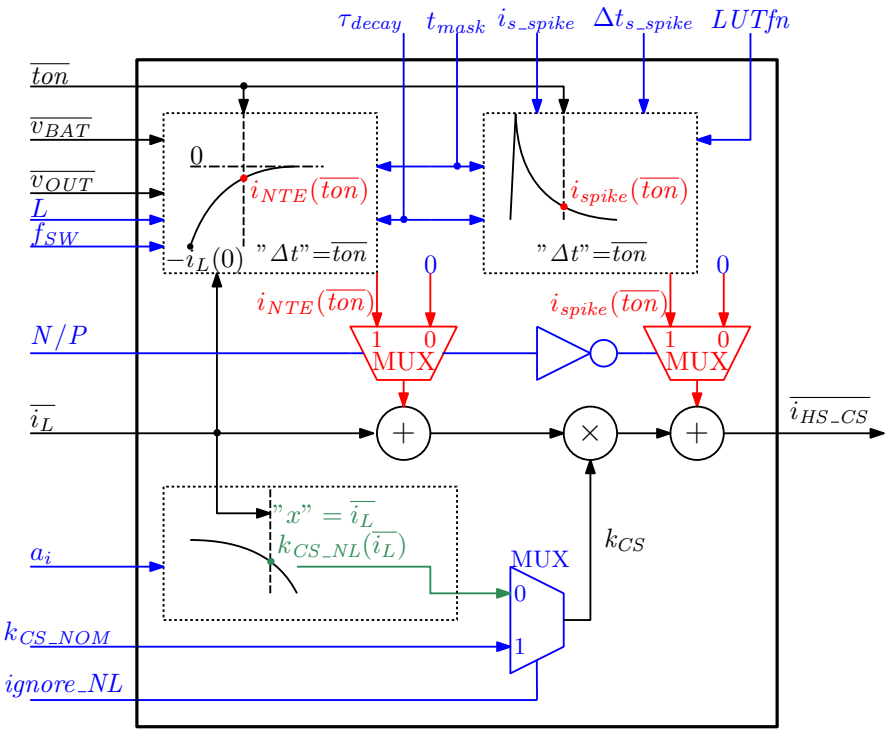


Figure 2.4: Current sensor model structure. The parameters of the model and all internal constants are shown in blue and the transient error contributions with their paths are in red.

valid filename to a LUT is given in $LUTfn$. If $LUTfn$ is blank then the parameters of the error τ_{decay}, i_{s_spike} and Δt_{s_spike} are being used to calculate the value for the additive PTE error $i_{spike}(\overline{ton})$.

The last binary parameter N/P is used to select whether the NTE or PTE is going to be used by the model. The reason behind the two being mutually exclusive is related to the fact that modeling the effect of finite bandwidth on PTE requires the convolution of the spike-current with the impulse response of the sensor. This implies that an analytical model for the transient behavior of the spike current is necessary. The relevant literature offers some models for its different components separately but no unified model for the spike current. Furthermore, the validation of such a model would be very hard in an experimental setting as the spike has high amplitude while also being very short lived and a sensor with very high dynamic range ($10^{-3} - 10^{+1}$ A) and bandwidth ($>$ 5 GHz) would be required to measure it without distorting it. To bypass this limitation, PTE is modeled with the help of fitted and interpolated models generated from testbenches that take into account all 3 errors together. Due to this choice it makes no sense to have both NTE and PTE active at the same time.

2.3.1 Non-linear current sensor gain

Static non-linear sensor gain can be intuitively modeled as an input-dependent gain. The proposed model implements this functionality as a combination of analog expressions in a Verilog-A module and is compatible with analog simulators. The input-dependent static gain of a properly biased current sensor can be modeled with a polynomial equation Eq. 2.9 implemented as a user-defined Verilog-A analog function. In this implementation the order of the polynomial was chosen to be $N = 5$. The input x of model of the non-linear gain takes the value of the inductor current $\overline{i_L}$, which is treated as the average i_L of a switching period by our implementation of the averaged DC-DC model. The parameters a_i can be estimated by applying the curve fitting methods of MATLAB or SciPy (Python) on the inputs and output of the current sensor in a DC sweep.

$$k_{CS\_NL}(x) = \frac{i_{OUT\_static}}{i_{IN\_static}} = \sum_{i=0}^{N} a_i \cdot x^i \tag{2.9}$$

2.3.2 Effects of transient errors

The transfer function of the current sensor of a CM buck affects its dynamic behavior. Ideally, the bandwidth of these sensors is high enough to properly track the inductor current and low enough to prevent high-frequency switching noise from reaching its output. In such a scenario, modeling the sensor after its static gain is sufficient and errors of transient and dynamic nature can be ignored. In reality, meeting both requirements at the same time is not easy for architectures operating at high frequency and low conversion ratios as they force the designer to raise the bandwidth to a level where the high-frequency "noise" cannot be sufficiently attenuated. These errors have significant effect in the operation of converters employing PCM and other versions of CM that do not explicitly filter the readout current before using it to determine the duty cycle. The amount of noise is also worse in converters that employ on-chip high-side current sensing as switching noise has high peak amplitude, it is relatively wide-band and most of its power flows through the sensing element of the current sensor right after the start of a switching cycle. As a result, the use of a model that takes into account transient errors is necessary for the evaluation of stability of designs with the above features.

Modeling the effect of current sensing errors of dynamic nature in the context of an averaged model is not straightforward but has been done successfully in the past. In [22] the effect of time constant mismatch between different parts of the sensing structure of a DCR-based current sensor is modeled as an additional factor that is multiplied with the ideal current sensor gain. The time constant mismatch is expressed in the time

domain and then a linearized model is derived based on the assumption that all the time constants of the involved quantities are much larger than the switching period. In this work, the transient errors modeled are non-linear, appear for a short time after the start of every new PWM cycle, follow the same trend in every switching period and their instantaneous value depends on how much time has passed after the high-side switch turns on. They are characterized by much shorter time constants compared to the ones involved in DCR sensing and prevent approximations that would lead to a simplified linear model. Instead, the model structure proposed by this work requires an analytical or at least a numerical model for the readout current error and the solution is calculated by the analog simulator for every operating point. In order to achieve this, both the positive and negative transient error (PTE, NTE) are represented as currents i_{spike} and i_{NTE} and are modeled with the help of Eq. 2.12 and Eq. 2.10, 2.11 where t is the time in the transient analysis, Δt is the time after the high-side switch turns on, Δt_{s_max} the value of Δt at which the spike error reaches its peak value i_{s_spike}, and τ_{decay} the time constant of the exponential decay of the transient errors. An example of their shape is given in Fig. 2.5. As mentioned above, the latter tends to affect only converters that employ high-side current sensing and this work assumes this type of sensing to properly showcase its effects.

Eq. 2.10 is derived by solving the differential equation that describes the transient response of a low pass filter that is driven by a ramp signal after introducing the design parameters of the buck into the equation. In cases where both the product $\frac{\overline{v_{BAT}}-\overline{v_{OUT}}}{L}\cdot\tau_{decay}$ and the current ripple $\frac{\overline{v_{BAT}}-\overline{v_{OUT}}}{L}\cdot\Delta t$ are small relative to the averaged inductor current the equation can be simplified to Eq. 2.11 as both the steady-state tracking error of the sensor and the error due to current ripple are negligible. The simulation results shown in this work have been generated with the help of the simplified model.

$$\begin{aligned} i_{NTE}(\Delta t) = {} & i_L(0)\left(1-e^{-\frac{\Delta t}{\tau_{decay}}}\right) - \overline{i_L(t)} + \\ & + \frac{\overline{v_{BAT}}-\overline{v_{OUT}}}{L}\cdot\tau_{decay}\left(e^{-\frac{\Delta t}{\tau_{decay}}}-1\right) \\ & + \frac{\overline{v_{BAT}}-\overline{v_{OUT}}}{L}\cdot\Delta t \\ for\ i_L(0) = {} & \overline{i_L(t)} - 0.5\frac{\overline{v_{BAT}}-\overline{v_{OUT}}}{L}\cdot\Delta t \end{aligned} \tag{2.10}$$

$$i_{NTE}(\Delta t) = -\overline{i_L(t)}\cdot e^{-\frac{\Delta t}{\tau_{decay}}} \tag{2.11}$$

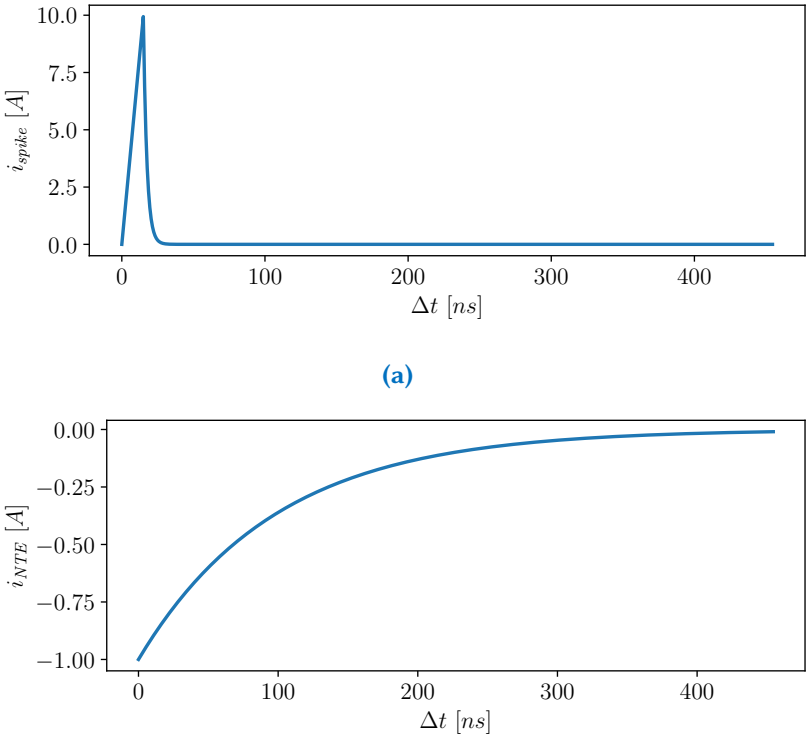


Figure 2.5: Example shapes of waveforms used to model the two transient errors. 2.5a is PTE with $i_{s\_max} = 10\ A$, $\tau_{decay} = 2.5\ ns$, $\Delta t_{s\_max} = 10\ ns$ and 2.5b is $\tau_{decay} = 100\ ns$, and NTE with $\tau_{decay} = 96\ ns$ and $i_L \approx 1\ A$.

$$i_{spike}(\Delta t) = \begin{cases} 0 & \Delta t \leq 0 \\ \Delta t \cdot \frac{i_{s\_max}}{\Delta t_{s\_max}} & 0 < \Delta t \leq \Delta t_{s\_max} \\ i_{s\_max} \cdot e^{-\frac{\Delta t - \Delta t_{s\_max}}{\tau_{decay}}} & \Delta t > \Delta t_{s\_max} \end{cases} \tag{2.12}$$

On the other hand, Eq. 2.12 is based on the equation that describes the current that charges the parasitic capacitances at the output of the half-bridge. This work uses a rough approximation of this model and assumes a fast linear rise to $i_{s\ max}$ with a duration close to the rise time of the gate driving signal and an exponential decay of this current with a non-varying time constant. The transitions between the branches are also smoothened with the help of a quadratic spline to prevent convergence difficulties due to the discontinuity of the first order derivative at these points and to enable the model to catch smoother transitions that happen when the spike is being filtered. The choice for the linear rise is based on the frequent assumption that drain current rises linearly until the gate-source voltage of the switch hits the miller plateau. The exponential decay is based on the assumption of constant switch resistance and capacitance

connected to the switching node. The derivation of a precise analytical model for this error would require the addition of the contributions of the reverse-recovery current of the body diode [24], [25] of the low-side switch combined with the effect of the miller plateau in the switching current [26] and is beyond the scope of this work that mainly focuses on providing a fast tool that can simulate the effects of such errors on control instead of providing a perfectly accurate model of each individual phenomenon. To mitigate the impact of the lack of a precise analytical model for PTE this work allows the use of models based on lookup tables (LUTs) that can be implemented with the help of the $table_model() function. In such a case, the user can deactivate all the other blocks of the model and force the PTE block to use a LUT-based model in the place of the analytical model for the error. The generation of the necessary look-up tables can be done with a few very short transient simulations of a simple testbench like the one shown in Fig. 2.6 and can be fully automated. The same LUTs can then be used to fit the parameters of the model for i_{spike} if the user prefers to avoid using them directly.

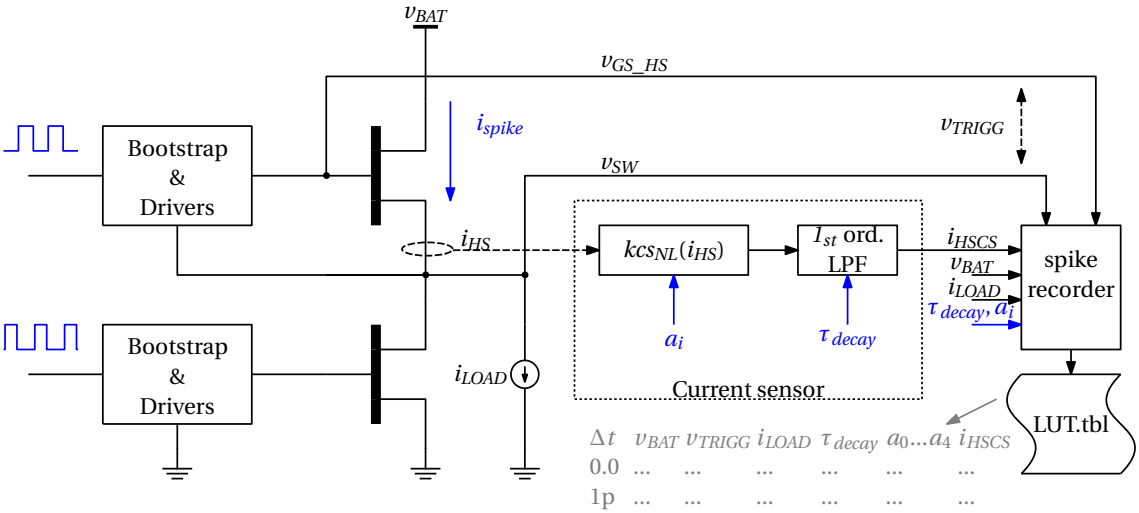


Figure 2.6: Testbench architecture used for the creation of LUT files and characterization of the spike.

The instantaneous value of each of the above mentioned errors depends on Δt. The contribution of each error at the moment of the peak detection and the resulting peak sensed current can be found by setting $\Delta t = ton$ with the latter being directly provided by the averaged model of the modulator and the PWM generator in the form of the average on-time $\overline{ton}$. The peak current is then translated back to the equivalent averaged value $\overline{i_{HS\_CS}}$ (which is done by removing 50% of the current ripple for the estimated ton in this work based on the steady-state approximation). This yields a significant amount of performance increase compared to a normal transistor-level transient simulation as the simulator can estimate values for $\overline{ton}$, $\overline{i_{HS\_CS}}$ and the respective peak values that solve

the resulting system of equations in a single timestep instead of multiple times around every switching event.

2.4 Performance of the model

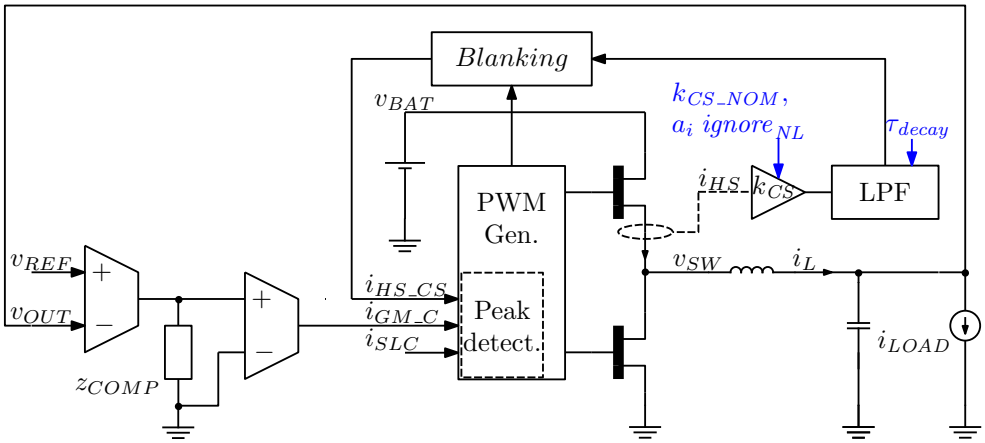


Figure 2.7: Testbench architecture used to investigate the effect of PTE and NTE on transient stability. PTE is introduced by the transistor switches.

In addition to the testbench of Fig. 2.7 a specialized testbench for NTE as well as an averaged testbench sharing the same main structure is created to evaluate the performance of the models. The testbenches use a PCM control scheme which is quite sensitive to transient errors. The first one is a representation of a (PCM) buck implemented with standard library components with the exception of the switches that are implemented as transistors and driven by bootstrapped inverter chains. The SPICE models representing the power transistors of the switches in the testbench can generate the spike currents that are picked up by the semi-ideal model of the sensor and can be used to simulate the effect of PTE with or without the presence of the other errors. The second one in Fig. 2.8 is the same as the first one with the exception that the switches and drivers have been implemented with standard library components and is used for the verification of the NTE model since the ideal switches do not introduce any PTE. Both testbenches are useful only for transient simulations. Both use block k_{CS} which is an instance of the module that allows the use of constant or non-linear static gain in the full-model structure and an RC filter that uses τ_{decay} to set its bandwidth in the place of the LPF. The last testbench, shown in Fig. 2.9, uses a lot of the circuit structure of the first one with the exception that the switches and the PWM generation parts are replaced by a block based on the averaged approximation and is suitable for both transient and AC analysis. The use of PCM requires the introduction of an additional compensation slope

current that is marked as i_{SLC} on the figures and is represented by the slope S_e in the averaged model. The parameter t_{mask}, also shown in Fig. 2.3 and Fig. 2.4 is introduced to emulate the effect of blanking time by preventing the current sensor from giving values corresponding to $\overline{ton} < t_{mask}$. Furthermore, the lack of switching parts in the testbench allows the simulator to use longer timesteps and as a result the transient simulations are sped up considerably.

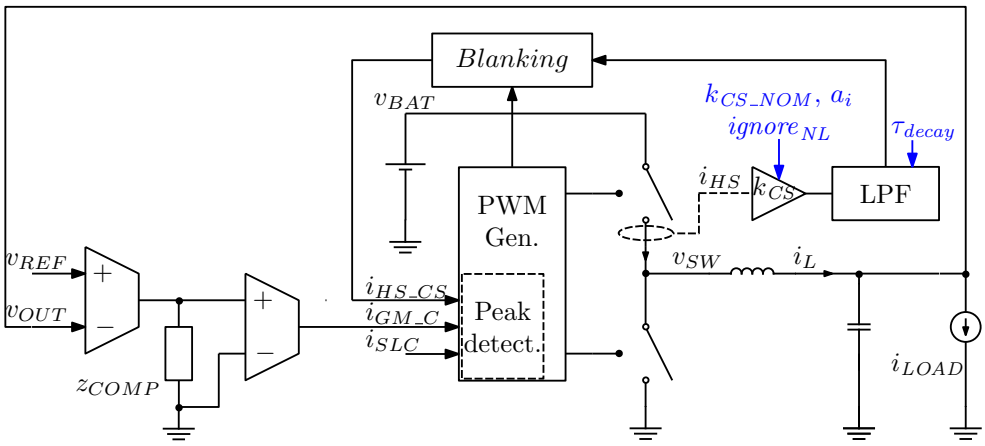


Figure 2.8: Testbench architecture used to investigate the effect of NTE on transient stability.

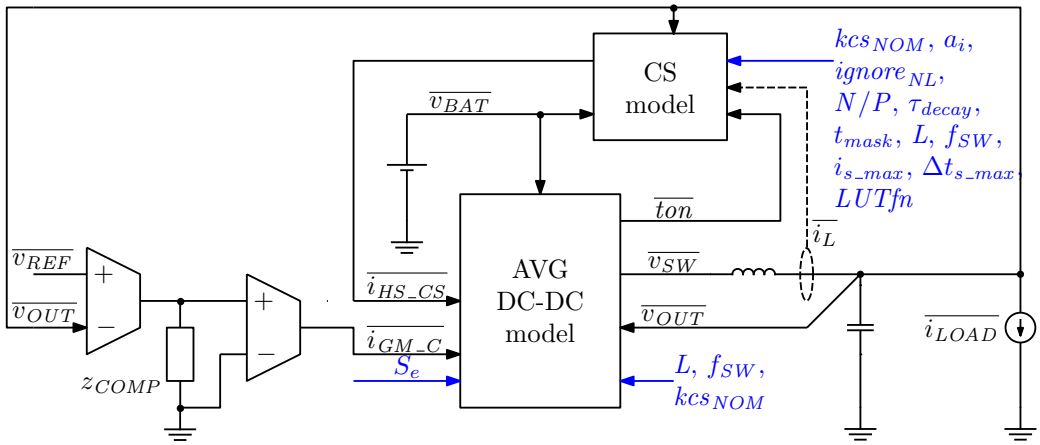
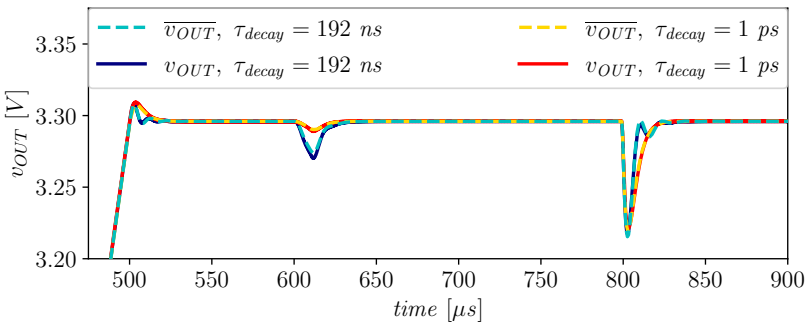
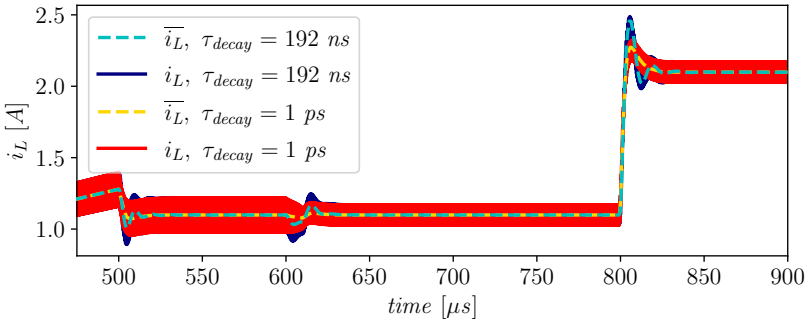


Figure 2.9: High-level representation of the averaged testbench used to evaluate the current sensor model. The quantities in blue font are parameters.

In Fig. 2.10 the results of transient simulations are shown with and without the effects of the negative transient error as estimated by the above mentioned testbenches. The traces for $\tau_{decay} = 1\ ps$ are identical with the ones produced by Fig. 2.7 and Fig. 2.9 where the LPF of the switching testbench is replaced by a short and the NTE block of the averaged is deactivated. During the time range shown in the plot there is a time interval during which both the reference and battery voltages are rising (up to 500 μs),



(a)



(b)

Figure 2.10: Results of transient simulations of the averaged and switching testbench. Output voltage (2.10a) and inductor current (2.10b) for negative transient error of $\tau_{decay} = 192\ ns$ (829 kHz sensor BW) and $t_{mask} = 60\ ns$. The dashed lines are generated by the new model.

another one when the battery voltage is halved (600-610 μs) and a last one during which the load current is increased from 1.1 A to 2.1 A (799-800 μs). The model follows the trend of the inductor current and output voltage of the switching testbench well enough as seen in Fig. 2.10 under the presence of negative transient errors in a fraction of the original simulation time as seen in Tab. 2.1. As a result, the model can be used to quickly find steady-state operating points of the DC-DC converter, which can then be used to study the stability or the efficiency of the converter. The speedup is up to 3 orders of magnitude even though the maximum timestep was limited to the size of one switching period to further improve the accuracy.

The accuracy of the model was also evaluated through the use of a metric. This work uses the Root-Mean-Squared-Error (RMSE) metric of the output of a transient simulation of the model versus a corresponding reference waveform. RMSE is an attractive choice as it inherits the properties that make its parent metric, the Mean-Squared-Error (MSE), a popular choice for comparing signals [27] and the application of the square root makes the resulting value easily comparable to the amplitude of the measured quantity.

Table 2.1: Simulation time for 1ms of operation with startup, battery voltage changes and load step

Testbench	Sim. time, NTE	Sim. time, Spike
Averaged	<1 s	
Averaged + CS model	<1 s	1.5 s
Switching semi-ideal	<1 s	
Switching semi-ideal+ error-emul.	1113 s	1153 s

However, the use of the averaged model leads to v_{OUT} wavefroms with no ripple and as a result any estimation of RMSE between the output of the switching and the averaged testbench would lead to an error value which is dominated by the ripple of the converter. To tackle this issue the waveform of v_{OUT} of the switching testbench is substituted with a non-rippling sampled version of it. Each sample is the average between the value of v_{OUT} when i_L becomes equal to i_{LOAD} while rising and its value when i_L becomes equal to i_{LOAD} while falling. This metric effectively removes the ripple and works well as both crossings happen within a switching period. As in Tab. 2.2, the accuracy of the model is very good in steady-state with the RMSE of less than $10 \cdot 10^{-6}$. The accuracy degrades during battery voltage transients but the RMSE stays below $3 \cdot 10^{-3}$. The RMSE with the model in the case of battery voltage halving is also inflated due to a bump caused by the existence of cycles with less than two crossings of i_L with i_{LOAD}. Excluding this part, the RMSE values become $11.23 \cdot 10^{-3}$ and $1.614 \cdot 10^{-3}$ respectively.

Table 2.2: RMSE of model output vs sampled averaged v_{OUT} under NTE of $\tau_{decay} = 192\ ns$ and $t_{mask} = 60\ ns$

Case	RMSE vs averaged	RMSE vs averaged+model
Steady state	$8.748 \cdot 10^{-6}$	$8.748 \cdot 10^{-6}$
v_{BAT} halving	$10.13 \cdot 10^{-3}$	$2.622 \cdot 10^{-3}$
v_{BAT} doubling	$3.677 \cdot 10^{-3}$	$309.6 \cdot 10^{-6}$

The most important advantage provided by the proposed model is its ability to also be used in AC/Loop-Gain/stability analysis and extract metrics like the phase margin of the system to evaluate its stability under the presence of non-linear gain and transient errors. Fig. 2.11 is generated with the help of the testbench of Fig. 2.9 and a reference testbench with a simple gain in the place of the sensor model and shows the noticeable

change of phase margin due to NTE. The resulting phase margin values also match the transient behavior of the converter as shown in Fig. 2.12. The model produces similar results under the presence of PTE as shown in Fig. 2.13. Lastly the effect of the NTE and PTE on the UGB of the sensor is shown in Fig. 2.14 and Fig. 2.15 respectively.

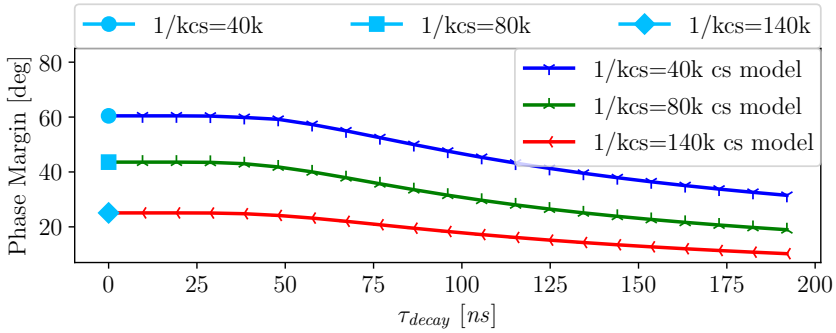


Figure 2.11: Effect of negative transient error on Phase Margin with increasing error decay time constant. Curves for $t_{mask} = 60\ ns$. The points using square, diamond and disc markers have been generated by a reference averaged testbench with constant current sensor gain.

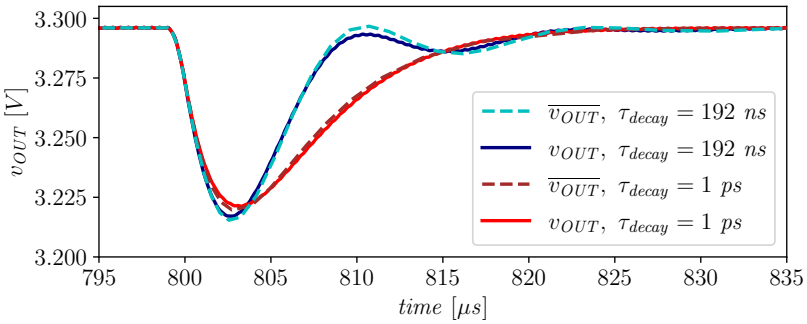


Figure 2.12: Transient behavior of output voltage under the effects of negative transient error and the estimated Phase Margin. Results for $t_{mask} = 60\ ns$. The dashed lines are generated by the model.

2.5 Summary

An improved model of a current sensor for use with the averaged model DC-DC converters is presented and evaluated in a PCM setup. It is implemented as a Verilog-A module and can be used in testbenches designed for transient and stability analysis while also being compatible with analog simulators. It can model the effects of non-linear current-sensor gain as well as positive and negative transient errors which can also lead to overestimation of the stability of a converter if ignored. Furthermore, the

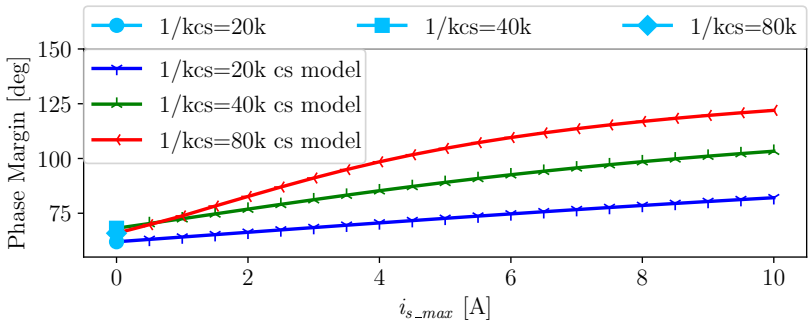


Figure 2.13: Effect of PTE on Phase Margin with increasing spike height. Results for $\tau_{decay} = 2.5\ ns$, $t_{s\_max} = 10\ ns$, $v_{bat} = 74.9\ V$ and $t_{mask} = 15\ ns$. The points using square, diamond and disc markers have been generated by the reference averaged testbench with constant current sensor gain.

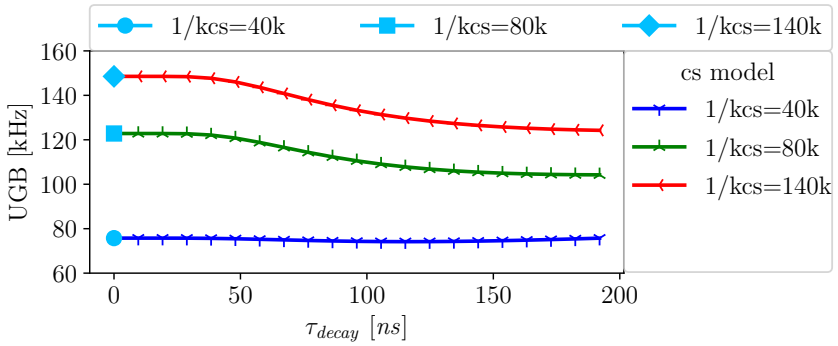


Figure 2.14: Effect of NTE on Unity Gain Bandwidth with increasing τ_{decay}. Curves for $t_{mask} = 60\ ns$. The points using square, diamond and disc markers have been generated by the reference averaged testbench with constant current sensor gain.

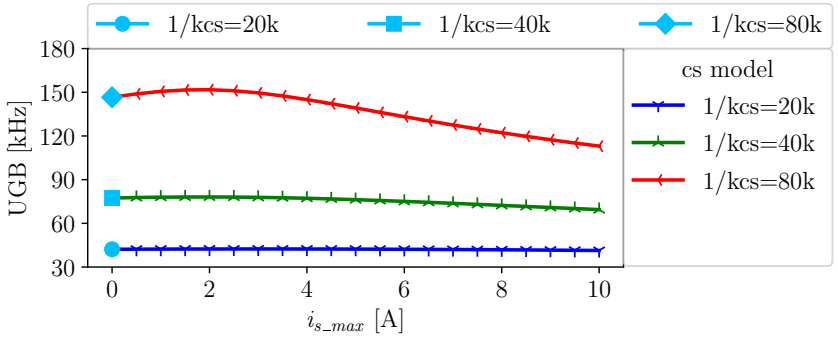


Figure 2.15: Effect of PTE on Unity Gain Bandwidth with increasing spike height. Results for $\tau_{decay} = 2.5\ ns$, $t_{s\_max} = 10\ ns$ and $t_{mask} = 15\ ns$. The points using square, diamond and disc markers have been generated by the reference averaged testbench.

enhanced model can reduce simulation time significantly as it can achieve a speedup of up to 1000× compared to normal transient simulations.

Acknowledgment

This research was supported by the EU project iDev40. The project iDev40 has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No 783163. The JU receives support from the European Union's Horizon 2020 research and innovation programme. It is co-funded by the consortium members, grants from Austria, Germany, Belgium, Italy, Spain and Romania.

The content of this presentation does not reflect the official opinion of the Joint Undertaking ECSEL. Responsibility for the information and views expressed in the presentation lies entirely with the author(s).

3 Design of a 40-V, Fast-Response, High-Side Current Sensor for Current-Mode DC-DC Converters

Chapter Contents

3.1 Fast-Response Current Sensors in Literature

3.1.1 Current sensor taxonomy

Integrated current sensors typically exploit one of the following sensing elements: sense-resistor [28], inductor DCR [29], or a sense-FET [30]–[35]. The first two are usually hard to fully integrate, due to the physical size of the additional components required (low-tolerance, high-power shunts in the first case and relatively high-value capacitors in the second case). The last category of sensor relies on sense-FETs, small replicas of the main power-FET. The sensors of this category can be fully integrated, allowing for the smallest possible bill of materials and as a result are less affected by board-level parasitics that degrade the performance of the converter. Sense-FET-based current sensors monitor

the switch current as an approximation of i_L and are typically half-wave sensors, that only track the current of the switch that is on during a single PWM phase, while they are reset during the opposite phase. A consequence of the reset is a higher slew-rate requirement, due to the fact that the expected change of their output at minimum t_{on} is proportional to the value of the inductor current instead of its ripple. Full-wave [32] as well as some hybrid [30] architectures sense the current of both switches to avoid this issue, but high-voltage implementations are rare and may require high-voltage devices [32] which are not available in most technology nodes and anyway achieve worse performance for the same area, compared to devices that support standard v_{gs} values.

3.2 High-Voltage High-Side Current Sensors in Literature

One inherent disadvantage of high-side current sensors is that their input (or at least its common-mode value) has to be close to the input rail voltage of the converter which can vary significantly. If the sensor is integrated in a high-voltage buck converter, this value can become several times higher than the maximum (input) voltage that can be handled by typical implementations of the signal processing blocks that are connected to its output. Thus, the sensor has to be able to perform well for the full range of the input voltage of the converter while providing its output at low voltage. There are technology-based, as well as topology-based solutions to this design problem.

3.2.1 High-voltage Technology Options

A straightforward implementation would be to make use of devices that can withstand the full voltage of the input of the converter. Such devices generally rely on thick gate oxide to keep the electric field at the gate of the transistor below the breakdown level of the dielectric. However, they are not generally available in standard modern CMOS processes and, if they are, they come at bad performance-area cost. Still, there are designs like [32] that make use of such devices for the part of the sensor that is expected to face the highest voltages while using lower-voltage devices elsewhere.

3.2.2 Level Shifting

The most direct way of dealing with the high common-mode input voltage of the sensor is by performing some form of dynamic level shifting in the circuit capable of removing the significant but relatively slowly changing high common-mode voltage while propagating the small differential-mode signal that is generated across the high-side sensing element to the low-voltage domain in voltage or current form.

3.2.2.1 Capacitive

A rather straightforward implementation of level shifting involves the use of capacitors that are charged close to the common-mode voltage of the input (ideally equal to v_{bat}) and then use them to connect each of the terminals of the sensing element to the high-impedance inputs of a low-voltage amplifier. The level shifting capacitors can be charged every cycle during the time that the sensor output is not needed. This technique has been successfully used in the past in lower voltage ($\leq 5\ V$) applications [36] and enables the use of high-performance low-voltage devices for the amplifier which in turn resulted in the design of a faster sensor. Capacitors can also be made to withstand a significant amount of voltage and they can also be matched well to reduce the amount of possible offset due to the capacitors discharging on the finite input impedance of the amplifier. However, this solution can be susceptible to high-amplitude, high-frequency noise in v_{bat} as it can end up pushing the level shifted voltage at the input of the amplifier to values that are outside its supported input range. Such type of noise can appear in high-voltage, high-current, high switching frequency converters like the ones used for automotive purposes as the voltage at the input of the amplifier is not constant but is contains the ringing of the parasitic RLC circuit that is formed between the high-side switch is on and the packaging and board parasitics are taken into account. As a result, this solution is not suitable for our application.

3.2.2.2 Amplifier-Based

Another way to get rid of the high common-mode voltage is by using suitable amplifier architectures that convert the input signal into a differential current in the high-voltage domain, let the current cross into the low-voltage domain and amplify it there. In terms of implementation, common-gate input structures like the ones used in [35], [37] are suitable for high common-mode voltage applications as the signal passes through the drain-source path of the input devices, which can be made less susceptible to the high voltage without the use of expensive technologies. Sophisticated gain-boosted topologies like [35] can achieve high gain and significant accuracy against mismatch with good bandwidth. However, the low differential input resistance of common-gate input stages and the fact that a significant part of the bias current of the structure flows through the inputs of the structure is still a source of input-dependent gain-error for the sensor. This can introduce a bad trade-off between the response-time of the sensor (typically decreasing with rising bias current) and its low-current accuracy and requires the use of a bias compensation circuit like the one proposed in [37] for structures that are based on the matched current source principle. On the other hand, common-source

Table 3.1: Target specifications for the sensor.

Parameter	Target Value
Input Voltage (v_{bat}) [V]	6–40
Load Current (i_{load}) [A]	0.2–5.5
KILIS (inverse of gain) [-]	$\approx$ 40k
ton_{min_buck} [ns]	$\leq$ 55
Settling time [ns]	$\leq$ 30–45
GBW [MHz]	$\geq$ 19.5[a]
PM [deg]	$\geq$ 70
I_q [µA]	as small as possible

[a] Step response at 5% settling error after 27 ns.

input structures present a high input resistance to the sensing structure which prevents such errors. Unfortunately, their implementation is not that trivial as the common-mode signal appears directly at the gate of the input transistors. This either limits the number of suitable architectures or imposes the requirement to use thick oxide transistors that come at extra cost and with worse performance/area trade-off density which is not optimal when the goal is the design of a fast-response sensor. This work, uses a common-source input amplifier architecture without requiring thick oxide devices.

3.3 Sensor Design and Implementation

The target specifications for the sensor are given in Tab. 3.1. The ultimate goal is to create a fast-response sensor that supports the operation of an automotive buck pre-regulator that uses Peak Current Mode (PCM). This means that it has to be able to regulate with a v_{bat} in the 6-40 V range to ensure a regulated output voltage even under warm-crank and (clamped) load-dump scenarios. The expected load current of the buck is 0.2-5.5 A.

The sensor was implemented on a 130-nm automotive CMOS node. The technology offers both low and high voltage devices including LDMOSFETs that can handle high drain-source voltages equal to the full maximum expected battery voltage[38].

3.3.1 Sensing Structure and Operation Principle

The chosen architecture is based on a modified sense-FET-based architecture that can be fully integrated. The block diagram of the sensor when it is tracking the current of the

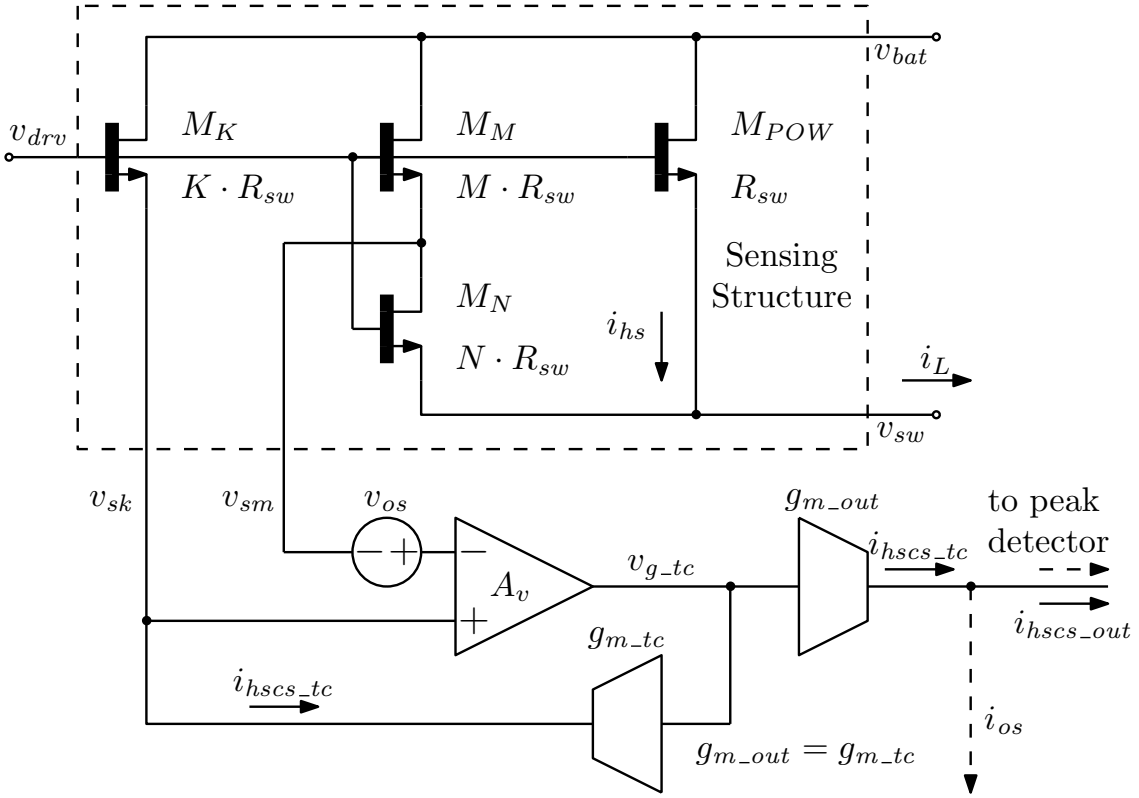


Figure 3.1: Sensing structure, and concept diagram of the sensor.

high-side switch is shown in Fig. 3.1. The voltage v_{bat} represents the input voltage of the converter, v_{sw} the voltage of its switching node (the output of the half-bridge) and i_L the inductor current. The input of the current sensor (CS) is the voltage drop on the high-side switch M_{POW}, that is approximately $v_{ds\_pow} = R_{sw} \cdot i_{hs}$, where R_{sw} is the on-resistance of M_{POW} and i_{hs} the part of i_L that flows through it. The sensing structure is formed by M_{POW} and its scaled-down versions M_M, M_N and M_K. The latter, are scaled in such a manner that their with on-resistances that are equal to M, N and K times R_{sw}. All the transistors of the sensing structure are driven by v_{drv} which is supplied by a bootstrap capacitor when the high-side switch is expected to be on. The above sensing structure has been inspired by [39]. The original structure can be used for current threshold detection by turning currents into voltages with a ratio-dependent gain and shifting them to the threshold of a comparator with the help of resistive device 133 and current source I_{THRESH}. The shift allows for easy tuning of the current threshold by adjusting the value of I_{THRESH}. The original structure has been adapted for closed-loop operation by moving device 133 (M_K in our case) and current source I_{THRESH} to the other input of the comparator, turning the comparator into an amplifier and the current source into the transconductor g_{m_tc}.

Transistors M_M and M_N form a voltage divider that is connected in parallel to M_{POW} and produces $v_{sm} = v_{bat} - \frac{M}{N+M} v_{ds\_pow}$ at the source of M_M. Transistor M_K, on the other hand, acts as a sense-FET and provides $v_{sk} = v_{bat} - K \cdot R_{sw} \cdot i_{hscs\_tc}$ at its source. Thanks to the voltage division done by M_M and M_N it is possible to achieve lower sensor gain k_{CS} with the same size of M_K compared to the sensor gain offered by a typical replica-based architecture. The main benefit from achieving lower gain with similarly sized devices is the improvement of light-load efficiency in high-voltage and high-load-current converters. This is possible due to the influence of the maximum readout current and sensor gain on the required specifications of several blocks of the control loop of a PCM DC-DC converter that tend to consume power regardless of the load.

Voltage v_{sm}, then, drives an amplifier that generates v_{g_tc}, which in turn is converted into the current domain by two matched transconductors. The output of the first transconductor produces the sensor output current, i_{hscs_out} after the offset i_{os} is removed, while the output of the other transconductor, i_{hscs_tc}, is sent back to the sensing structure. Then, i_{hscs_tc} produces v_{sk} at the source of the sense-FET M_K and closes the feedback loop, by reaching the positive input of the amplifier. The current at the output of the transconductor is given by

$$i_{hscs\_tc} = \frac{A_v g_{m\_tc} M R_{sw}}{(A_v g_{m\_tc} K R_{sw} + 1)(M + N + 1)} i_L - \frac{A_v g_{m\_tc}}{(A_v g_{m\_tc} K R_{sw} + 1)} v_{os} \tag{3.1}$$

The above equation consists of two terms. The first is the sensed current and is equal to the inductor current i_L scaled by the sensor gain. The second one is simply the offset current of the sensor i_{os} and is proportional to the input-referred offset voltage of the amplifier v_{os}. The latter is removed from i_{hscs_tc} to create the readout current i_{hscs_out} which is then sent directly into the peak detector of the converter. The term $A_v g_{m\_tc} K R_{sw}$ is much higher than 1 so Eq. 3.1 can be simplified to

$$i_{hscs\_tc} \approx \frac{M}{K(M + N + 1)} i_L - \frac{1}{K R_{sw}} v_{os} \tag{3.2}$$

At this point, it is possible to observe the two main advantages from the use of this sensing structure. The first one, is the fact that the sensor gain depends on transistor ratios and therefore can be controlled relatively well in modern planar CMOS processes. Furthermore, this gain can be made smaller for the same minimum acceptable size of M_K (maximum value of K) compared to a typical replica architecture by adjusting M and N. The second one is the fact that the offset term is not significantly affected by g_{m_tc}. This means that the value of i_{os} remains relatively constant despite the change of g_{m_tc} when i_L (and therefore i_{hscs_tc}) changes and this keeps the non-linearity of input-output

characteristic of the sensor low.

3.3.2 Optimization Versus Input Disturbances

The gain of the sensor $k_{CS} \approx \frac{M}{K(M+N+1)}$ can be achieved with several different combinations of K, M and N values. The relative values of these parameters affect the matching (and therefore the accuracy of the k_{CS}) and also the sensitivity of the sensor to supply disturbances from v_{bat}. The latter, is a result of the asymmetry of the sensing structure which creates a medium-frequency zero, followed by high-frequency poles in the noise transfer function and leads to a degraded CMRR at high frequencies. Due to the proximity of the high-frequency poles to the resonant frequency of the switch, bondwire and PCB parasitics, it is beneficial to minimize the height of the resulting peak. Early AC simulations with transistor-level and semi-ideal models of the switches that contained the C_{gs}, C_{gd}, C_{sb}, C_{db} and C_{ds} parasitics have shown that neither C_{ds} nor the bootstrap capacitance C_{bst} can be neglected and therefore the derivation of a simple analytical expression for the high-frequency CMRR behavior is not possible. In order to bypass this limitation, the optimization was performed with the help of a testbench and a support script written in Python. A flowchart describing the optimization process is shown in Fig. 3.2.

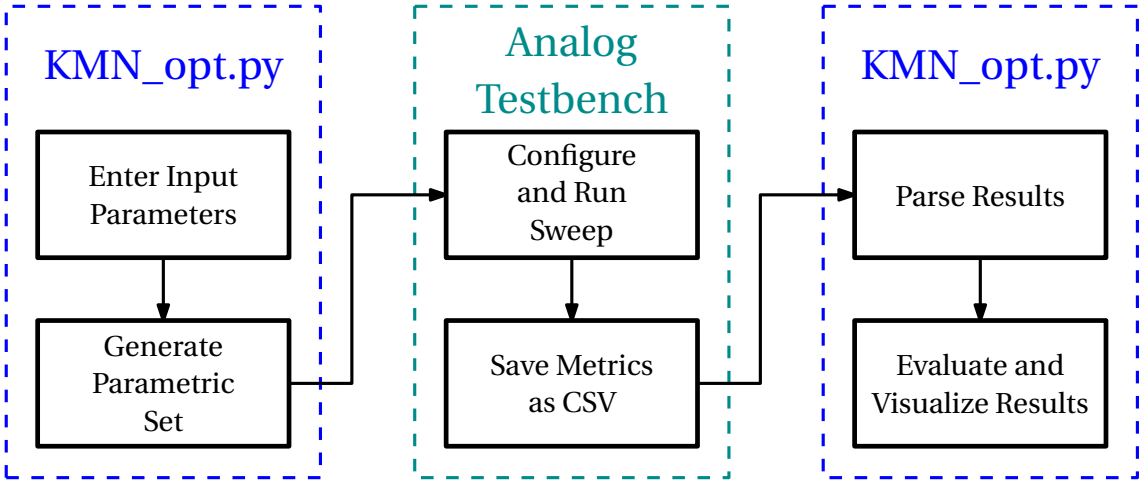


Figure 3.2: Flowchart of the procedure used for the optimization of the sensing structure against supply disturbances

The testbench itself is an analog testbench like the one shown in Fig. 3.3 and consists of a semi-ideal representation of the sensor that uses ideal blocks to emulate the amplifier and the transconductor and a transistor-level cell of the sensing structure that uses the values of K, M and N as parameters to change the sizes of the M_K, M_M and M_N. In this example, the parameters W_{POW}, W_M, W_N and W_K are the widths of M_{POW}, M_M,

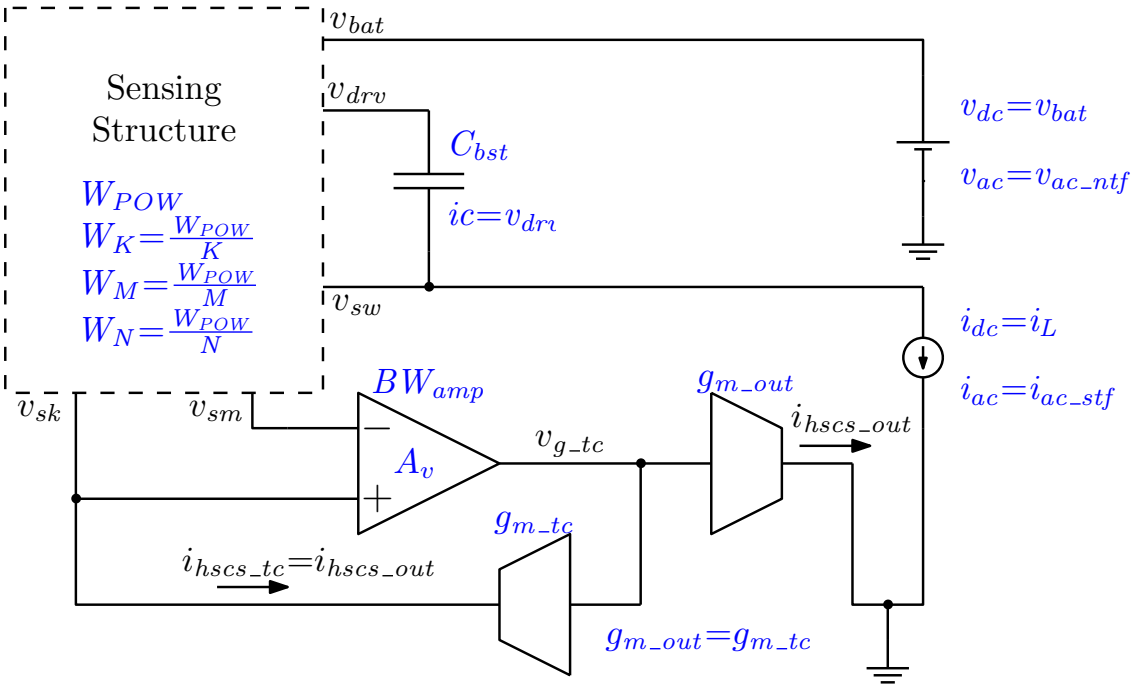


Figure 3.3: High-level representation of the testbench used for the optimization of the sensing structure

M_N and M_K respectively. Additional parameters are the DC gain (A_v) and bandwidth of the amplifier (BW_{amp}), the transconductance of the transconductor (g_{m_tc}) and the value of the bootstrap capacitance C_{bst}. A few more parameters can be passed to ensure that the DC operating point can be properly calculated like and the voltage across C_{bst} when the switches are on (v_{drv}) which is passed as an initial condition of the capacitor, the inductor current that is flowing through the high-side switch (i_L) and the battery voltage v_{bat} as a dc current and a DC voltage.

Two tests are run for every datapoint, one is focused on a "noise" transfer function (NTF) and is implemented through an AC analysis with a voltage source at v_{bat} and a current output at i_{hscs_tc}. The second test is focused on estimating the signal transfer function (STF) and is implemented through an AC analysis with a current source at i_L and a current output at i_{hscs_tc}. In this work, a third expression is generated by dividing the magnitudes of the STF with the NTF to create an SNR-like metric that allows the designer to see which frequency ranges are mostly affected by supply disturbance. To allow for the use of a single schematic for the estimation of both the signal and "noise" transfer functions the parameters v_{ac_ntf} and i_{ac_stf} can be used to turn on the respective ac source. For the "noise" transfer function, $v_{ac\_ntf} = 1$ and $i_{ac\_stf} = 0$ and the opposite for the signal transfer function. Lastly, the values of the SNR-like function at low, medium and high-frequencies can be sampled with the value() function of the calcula-

tor of Virtuoso to generate scalar values that can be used to compare the behavior of the sensor across the different datapoints with a single look. Another useful expression, is the static gain at the DC-operating point of the sensor which can be used as a sanity check to ensure that the input parameters can indeed yield the required value for k_{CS}. Finally, the effective widths of every switch can be exported with the help of expressions for every datapoint and make it easier for the designer to double-check that the provided parameters have actually reached the netlist. The script plays a dual role. Firstly, it is used to generate the parameter values that are going to be used for the parameteric sweep. Secondly, it is used for the visualization of the outputs as a 3-D surface in order to allow the designer to judge at a glance which is the optimal combination and how sensitive it is to the changes of the values of K, M, N. The script relies only on standard libraries of python [40] in addition to numpy [41] for processing and plotly [42] for the visualization. In order to function it requires the following parameters:

1. The required sensor gain k_{CS}
2. The acceptable gain error
3. Ranges for two out of 3 of the parameters (K, M, N)
4. The number of values for each variable
5. The width of the high-side switch W_{POW} and the maximum and minimum values of W_M, W_N and W_K (to ensure that all the estimated widths are acceptable)
6. The names of the output expressions of ADE XL that the designer wants to visualize.

When run, the script generates the values for the remaining parameter and gives the values of K, M and N as well as W_M, W_N and W_K in text format so that they can be directly copied to ADE XL and create a parametric set. Optionally, additional parameters are the gain (A_v) and bandwidth of the amplifier, $g_{m\perp tc}$ and the on-resistance (R_{sw}) of the power switch and W_{POW} can be provided to use the accurate equation instead of the simplified equation for the gain. Then, the designer runs the sweep, exports the results as a csv and the script reads the metrics that are specified by the last parameter of the script to generate a 3-D plot with the specified metric in its z-axis like the one shown in Fig. 3.4. If multiple metrics are specified the target 3-D plot (view) can be specified with the help of a slider. The script also generates an additional output (flag_valid) that confirms if the simulation results confirm that the target sensor gain could be achieved. To improve readability, the exact values of every datapoint can be shown by hovering over the

sphere that represents the datapoint. Lastly, the plot can be exported as a standalone html file containing all the necessary data. The final conclusions from this optimization

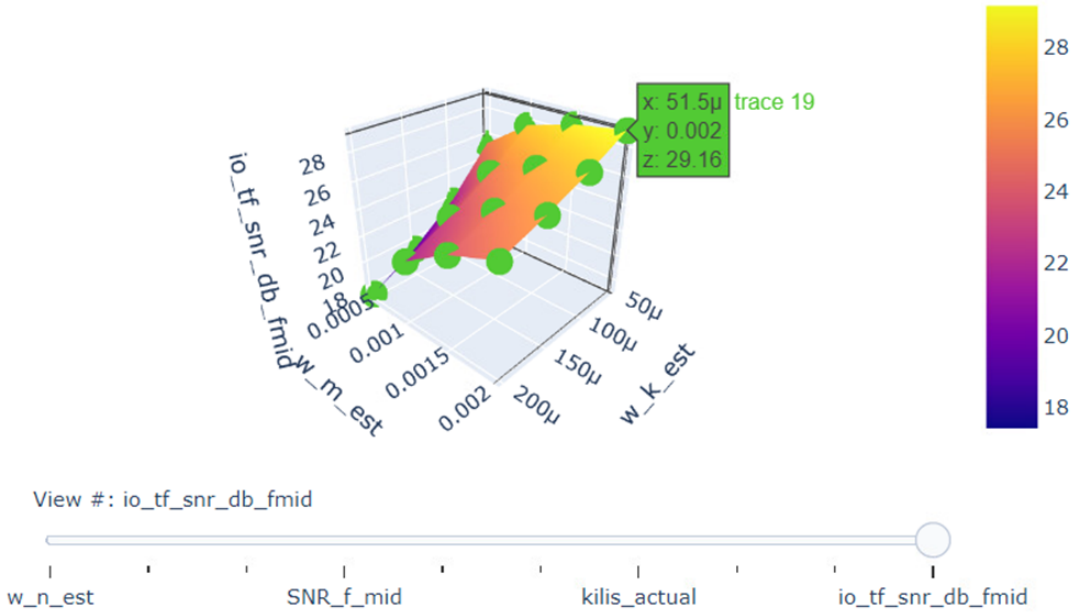


Figure 3.4: Example of the 3-D surface plot that is produced by the script that supports the optimization of the sensing structure

is that, in general, the sensitivity of the structure to medium/high-frequency noise from v_{bat} increases as W_K increases (K decreases) and the voltage division ratio performed by M_M and M_N decreases (smaller M and larger N). The final sizing of the sensing structure is chosen to be the one that yields the required sensor gain with the minimum acceptable (for reasons of matching) size of M_K. The chosen relative sizes of M_M and M_N are the ones that make it possible to achieve the required gain with the specified size of M_K and their absolute widths are chosen to be wider than W_K to improve the ratio of the signal to noise transfer functions for medium and high frequencies.

3.3.3 Overall Architecture

The complete current sensor architecture is shown in more detail in Fig. 3.5. The sensor uses 4 digital signals, the enable bit *en*, a pulse that is high during the time in which the high-side switch is on (hs_{on}), the masking pulse (*blank*), that is high when the output of the sensor needs to be masked through the *Blanker* block, and 2 trimming bits $trim_{tc}$. Voltages v_{2p5} and v_{1p5} are externally generated 2.5-V and 1.5-V power supplies.

One of the main challenges in the design of high-side current sensors is that they

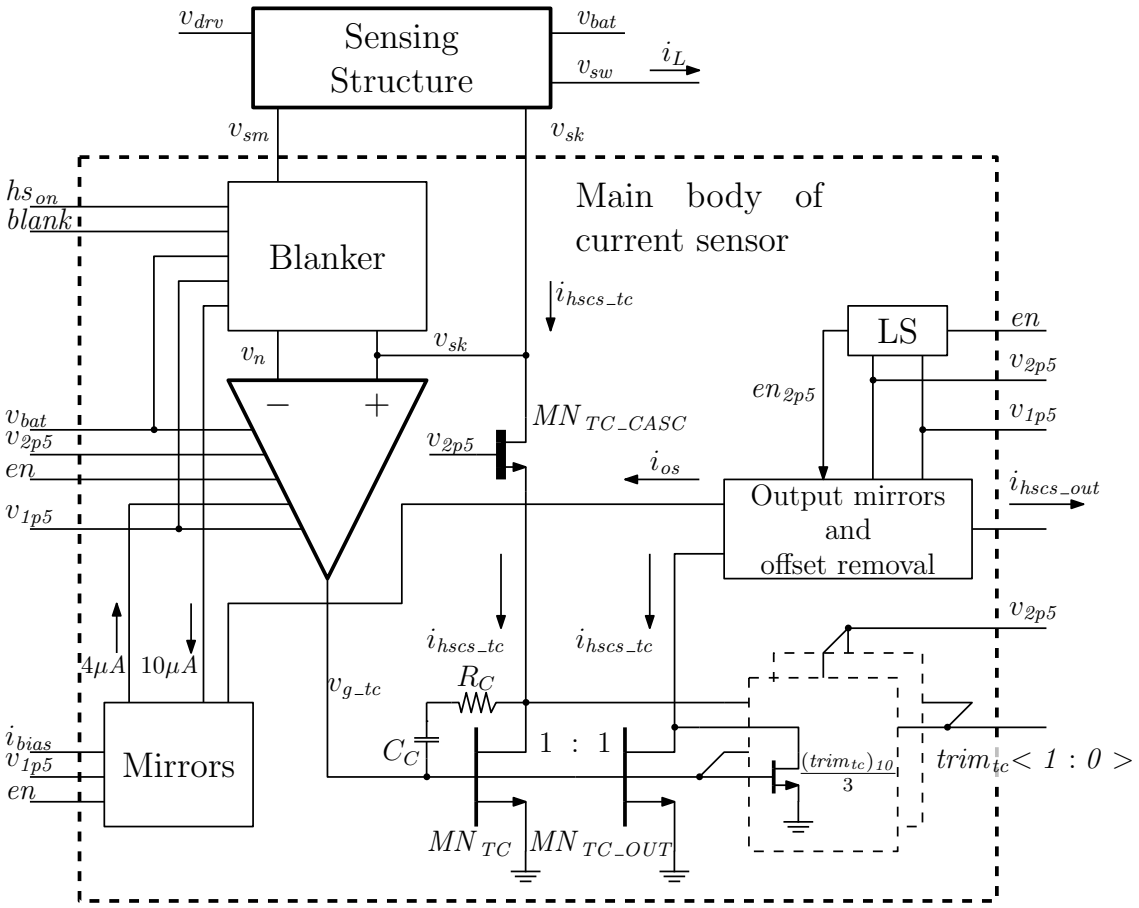


Figure 3.5: Detailed block diagram of the proposed current sensor

have to deal with a large common-mode voltage at their input, which is typically much higher than the maximum allowed common-mode input range of all the signal processing blocks. This problem is solved by exploiting signals in the current domain to cross between different voltage domains and by extensive use of cascode structures, as MN_{TC_CASC}, to separate the voltage domains. The sensing structure is designed to work in a voltage domain floating with the input voltage of the DC-DC converter v_{bat}, while the transconductors, the trimming block, the biasing block and the output current mirrors operate in a 2.5-V voltage domain referred to ground. The only blocks that are operating across both voltage domains are the amplifier and the blanker block.

The main issue in this architecture is that the transconductor (MN_{TC}) is biased with a current that is proportional to the sensor input. As a result, if the inductor current has a wide dynamic range, then MN_{TC} will behave non-linearly, with a transconductance g_{m_tc} that changes with the level of the input current. This has the additional consequence that the gain-bandwidth product (GBW) of the feedback loop changes with g_{m_tc} and can lead to degraded performance when the input current is low or if it hits zero during blanking. In the second case, g_{m_tc} becomes negligible and effectively cuts the loop open. In such a case, the response time of the sensor is extended by the amount of time needed by the amplifier to bring the v_{gs} of MN_{TC} back above its threshold voltage before the loop behavior can be approximated again with that of a linear system. Full-wave sensors can prevent this from happening by holding the value of the current that is forced through the sense-FET at the end of the off-time until the sensor is ready to sense the high-side current during the on-time [32]. However, this is not possible in half-wave sensors as the information about the valley current and the corresponding input of the transconductor is not known to the sensor.

Instead, this work relies on a combination of built-in offset and the use of a blanker block, in order to ensure that the loop remains closed during blanking and that g_{m_tc} is sufficient to achieve the response time requirements. The added offset i_{os} is then subtracted in the output current mirror before sensing the readout current with the peak detector of the control loop of the DC-DC converter.

The feedback loop requires the use of some form of frequency compensation. The dominant pole is at the output of the amplifier, but two non-dominant poles exist in the loop that can compromise the stability. The first one is inside the amplifier (f_{nd_oa}) and the second one is at the drain of MN_{TC} (f_{nd_dtc}). The latter is heavily affected by the large C_{gs} of the cascode transistor as well as any other parasitics. In this work, C_C is used to implement Miller compensation, to move the second pole far from the non-dominant pole, ensuring a phase margin above 65° without degrading the GBW of the loop. The resistor R_C is added in series with C_C to cancel the right half-plane zero. Lastly, the

built-in offset ensures that the distance between these poles is sufficient even for low values of the input current.

Last but not least, the sensor has a trimming functionality that works by adjusting g_{m_tc} by adding binary weighted matched transistors in parallel to MN_{TC} and MN_{TC_OUT}, doubling their aspect ratio to increase the effective g_{m_tc} by $\sqrt{2}$ with steps of 33%. This allows choosing between higher open loop gain or lower parasitic capacitances at the gate and drain of the transconductor to deal with the effect of the spread of g_{m_tc} due to process variations.

3.3.4 Keeping the Loop Biased

The proposed architecture has two disadvantages that cannot be directly observed in Fig. 3.1 but can severely degrade the performance of a straightforward implementation. Both of them can cut the loop open and significantly disturb the biasing of its building blocks. In such a scenario, the sensor needs to spend time rebiasing its blocks back to their expected operating points before its behavior can be sufficiently approximated by typical linear system models.

The first disadvantage is that a half-wave, high-side current sensor has to assume that the high-side switch current is at zero right before it starts tracking it. Simple implementations of the transconductor g_{m_tc} (like transistor MN_{TC} of Fig. 3.5) are highly non-linear for very low values of i_{hscs_tc} (operation in deep subtreshold). Furthermore, a very low value of v_{g_tc} can bring the output transistors of the amplifier into triode and severely reduce its gain. Forcing the input of the sensor during reset to a value equivalent to a current higher than the minimum expected switch current (i_{hs_min}) would not be an acceptable solution as it could potentially lead to false peak detection right after the end of the masking time if its value is higher than the expected peak value for that cycle ($i_{hscs\_out} > i_{L\_peak} \cdot k_{CS}$).

This disadvantage can be countered by introducing a minimum offset v_{os} (by design) as close as possible to the input of the loop. This offset voltage results in a minimum offset current i_{os} that flowing through g_{m_tc} which can be removed at the output of the sensor. This (approximately) known offset is responsible for keeping the loop biased to a known state that guarantees a minimum loop performance at the end of the masking time even when the expected readout current i_{hscs_out} is expected to be 0.

The acceptable range of i_{os} is chosen together with the size of the transconductor MN_{TC}. The first constraint is the need to keep MN_{TC}, as well as the output stage of the amplifier, in saturation across the full expected range of i_L in order to prevent significant loss of gain at low input current. The second one is the need to guarantee that at

minimum offset current i_{os_min} the value of g_{m_tc} is sufficient to allow the sensor to meet its performance specifications even when it starts from a reset state with a minimum transconductor current $i_{hscs\_tc\_min} = i_{os\_min}$). The last constraint is the SOA constraint for the v_{gs} of MN_{TC} which has to be respected when the sensor input is at the maximum possible value of i_L (i_{L_max}) and the transconductor current reaches its maximum value $i_{hscs\_tc\_max} = i_{os\_max} + k_{CS} \cdot i_{L\_max}$ and the offset has its maximum possible value i_{os_max}.

Additional constraints for i_{os} can be imposed by the minimum and maximum values of current that can be handled by the circuits of the node where the peak detection happens without causing any visible decrease in their performance. Additional limits are the absolute input and output limits of i_{gm_c} as well as the ones of the error amplifier before it as any offset in i_{hcscs_out} is eventually translated into an offset in i_{gm_c} once the loop settles in steady state.

The second disadvantage is the fact that the whole sensing structure turns off together with the high-side switch due to the fact that its transistors are biased by the voltage that drives the power switch. This design choice makes sense as it ensures that the ratio of the resistance of the sense-FET over the resistance of the power switch is as close to its designed value as possible and is good for accuracy but it can lead to speed degradation. When the sensing structure turns off, the node that provides v_{sm} is floating and $K \cdot R_{sw}$ becomes very high (M_K is off). The issue of the floating v_{sm} can be easily fixed by tying the node to v_{bat} (or a voltage at a constant offset from it) during blanking. However, the increase of $K \cdot R_{sw}$ eliminates almost all of the introduced offset i_{os} that is predicted by Eq. 3.2 and cuts the loop open and leads to the same performance issues that were described above.

The solution to the last performance bottleneck is to keep the loop closed by introducing a switch that emulates the sense-FET (M_K in our case) when the sensing structure turns off. Ideally, the resistance of such a switch (let's call it R_{K_EMU}) should be equal to $K \cdot R_{sw}$ but the sensor can be designed to have a significant amount of tolerance for this specification.

The maximum positive value for $\Delta R_{K\_EMU} = R_{K\_EMU} - K \cdot R_{sw}$ is of no importance as long as the gain-bandwidth product of the closed loop remains sufficiently high the moment that the masking time ends. This implies that the designer should care about the maximum possible absolute value of R_{K_EMU} ($R_{K\_EMU\_max}$) which has to be small enough to guarantee $i_{os} \geq i_{os\_gmtc\_min}$ and ensure that the sensor has the required minimum performance under the worst-case PVT variations. Therefore, the worst case value is given by

$$R_{K\_EMU\_max} = R_{K\_max} = \frac{v_{os\_min}}{i_{os\_gmtc\_min}} \tag{3.3}$$

where R_{K_max} is the maximum allowed value for the resistance of W_K and v_{os_min} the minimum possible offset current due to PVT. In contrast, the minimum acceptable value of ΔR_{K_EMU} is determined by the need to prevent false peak detection at the end of the masking time. The strictest possible limit is to go for $\Delta R_{K\_EMU} \geq 0$ which corresponds to an absolute minimum resistance value of $R_{K\_EMU\_min} \geq R_{K\_max}$ where R_{K_max} is the maximum possible resistance for switch M_K under the influence of PVT variations. This is also a very pessimistic limit as it assumes that the minimum possible resistance for MP_{EMU} can appear when M_K has its highest possible resistance which is usually not the case. Furthermore, such a limit would apply only when the converter operates with very low current ripple and at a very low peak current as in such a scenario its initial output due to feedback resistance emulation can end up being higher than the expected peak current value for that switching cycle. In conclusion, such a scenario is not realistically expected as the converter will have already switched into DCM operation before reaching the low-current, low ripple condition. Therefore, if the sensor is fast enough to converge from the high initial post-reset value to its actual value before the compensation ramp forces a peak detection (a realistic expectation for typical sensor designs due to the size of S_e) a more realistic negative limit for the error of the emulated resistance ΔR_{K_EMU} can be derived from

$$
\begin{aligned}
\Delta i_{os\_emu\_max} &= i_{L\_CCM\_min} \cdot k_{CS\_min} \\
\Delta i_{os\_emu\_max} &> v_{os\_max} \left(\frac{1}{R_{K\_EMU}} - \frac{1}{K \cdot R_{sw}} \right) \\
\Delta i_{os\_emu\_max} &> v_{os\_max} \left(\frac{K \cdot R_{sw} - R_{K\_EMU}}{R_{K\_EMU} \cdot K \cdot R_{sw}} \right) \\
\Delta i_{os\_emu\_max} &> v_{os\_max} \left(\frac{-\Delta R_{K\_EMU}}{(K \cdot R_{sw} + \Delta R_{K\_EMU}) \cdot K \cdot R_{sw}} \right) \\
\frac{v_{os\_max}}{\Delta i_{os\_emu\_max}} &< \frac{(K \cdot R_{sw} + \Delta R_{K\_EMU}) \cdot K \cdot R_{sw}}{-\Delta R_{K\_EMU}} \\
\Delta R_{K\_EMU} &> -\frac{(K \cdot R_{sw})^2}{\frac{v_{os\_max}}{\Delta i_{os\_emu\_max}} + K \cdot R_{sw}} \\
\frac{\Delta R_{K\_EMU}}{K \cdot R_{sw}} &> -\frac{K \cdot R_{sw}}{\frac{v_{os\_max}}{\Delta i_{os\_emu\_max}} + K \cdot R_{sw}}
\end{aligned}
\tag{3.4}
$$

where $\Delta i_{os\_emu\_max}$ is the maximum value of $\Delta i_{os\_emu} = i_{os\_emu} - i_{os}$, v_{os_max} is the maximum expected offset voltage of the amplifier, $i_{L\_CCM\_min}$ the minimum inductor current for CCM operation and k_{CS_min} the minimum expected value for the sensor gain. The worst case limit can be found by substituting $K \cdot R_{sw}$ with its minimum expected value. Another

advantage of this technique is that the generated offset current i_{os_emu} is affected by all the non-idealities of the sensor loop with the exception of the non-ideality of the resistance of W_K. If the matching between R_{K_EMU} and $K \cdot R_{sw}$ is good, then the voltage at the gate of M_{N_TC} and M_{N_OUT} v_{g_tc} can be sampled and held to be used to provide a non-constant but more accurate, dynamically generated value for i_{os} that is removed from i_{hscs_tc} to produce the readout current i_{hscs_out}.

3.3.5 Amplifier

The amplifier exists in both high and low voltage domains. Its output belongs to the low-voltage domain. However, it has to be able to handle the voltages produced at the output of the sensing structure which vary take values from v_{bat} to approximately $v_{bat} - v_{os} - i_L \cdot k_{CS} \cdot K \cdot R_{sw}$ which is just a few hundreds of mV below v_{bat}. v_{bat} itself takes values from 6 V to 40 V. All the above requirements are met by using a folded-cascode architecture with and NMOS input pair which is shown in Fig. 3.6. The separation of the voltage domains is done by implementing MP_{BL}, MP_{BR}, MP_{BC} and MN_{BC1-3} of the cascodic load of the amplifier as Lateral Drift MOSFETs (LDMOS). Such devices can withstand a v_{ds} equal to the full range of v_{bat}. The voltage at the output node is constrained in an active manner by the control loop but also with the help of a diode-connected PMOS transistor that is connected to the 1.5-V supply (not shown in schematic). The gate-source voltage of the input MOSFETs MN_{DR} and MN_{DL} is also clamped with the help of protection diodes connected between their gates and their common source node v_{com}.

The nodes $n2$ and $n3$, where the output of the differential input pair meets the cascodic load are the source of one of the lowest-frequency non-dominant poles of the sensor, because of the large parasitic capacitance due to the large minimum area of LDMOSFETs MP_{BL}, MP_{BR} and the large small-signal resistance seen at these nodes. The frequency of this pole (f_{nd_oa}) is made as high as possible by keeping MP_{BL} and MP_{BR} as small as possible and by properly sizing the bias currents of the input pair and of the cascode structure. The amplifier is designed with a built-in offset v_{os} that is responsible for the generation of the offset current i_{os} of the sensor. This offset is introduced by making MN_{DL} larger than MN_{DR}. The input pair is also implemented with high threshold transistors to ensure that none of its transistors fall into triode for the expected range of v_{os} and $v_{sm} = \frac{M}{M+N} R_{sw} \cdot i_L$. The achieved specifications were as follows: Nominal offset of 81 mV with a spread between 73-89 mV at nominal temperature. The amplifier also achieves a DC gain of $A_v = 74$ dB and a -3 dB bandwidth of $BW = 10.5$ MHz.

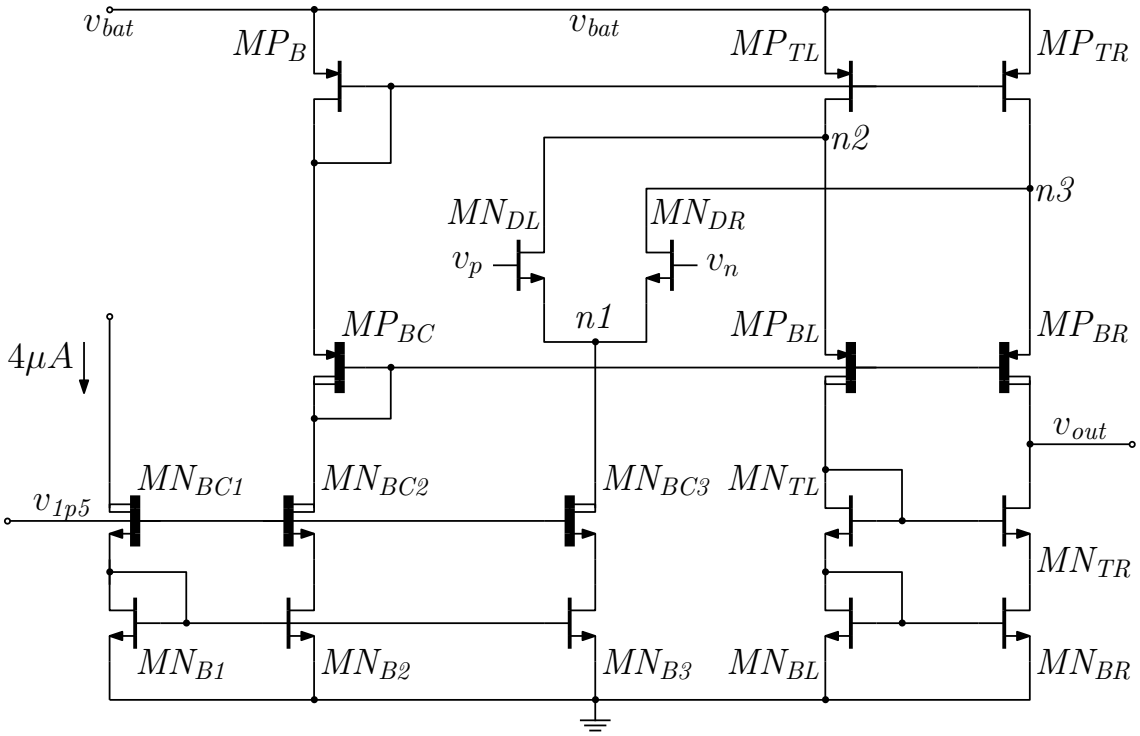


Figure 3.6: The schematic of the amplifier. Protection circuitry are not shown to improve readability.

3.3.6 Blanking Block

The blanking block has a dual role. Primarily, it is responsible for preventing voltage v_{sm} from reaching the inputs of the amplifier right after the high-side switch changes its state. During that time, the instantaneous value of the current that flows through the switch is close to an order of magnitude larger than the expected inductor current and as a result, it can cause an excessive drop of v_{sm} which can be caught by the sensor and lead to a false peak detection. Furthermore, such a fast and high voltage drop at the input of the sensor can affect the biasing of the cascodic load of the amplifier by momentarily pushing $M1P_{BR}$ and $M1P_{BL}$ into cutoff and $M1P_{TR}$ and $M1P_{TL}$ of Fig. 3.6 into triode. In such a case, the gain of the amplifier is effectively gone, the loop behaves as open and the re-biasing of the amplifier can take 100s of ns (at best) rendering the sensor useless for fast-response current tracking. Secondly, it is responsible for the application of a feedback resistance emulation technique that can be used to keep the sensor pre-biased at a state that ensures non-zero g_{m_tc} and therefore non-zero loop gain when the transistors of the sensing structure M_K, M_M and M_N turn off together with the high-side power switch M_{POW}. This anomaly is present in every cycle and is a side-effect of the design choice to drive every transistor of the sensing structure of Fig. 3.1 with the

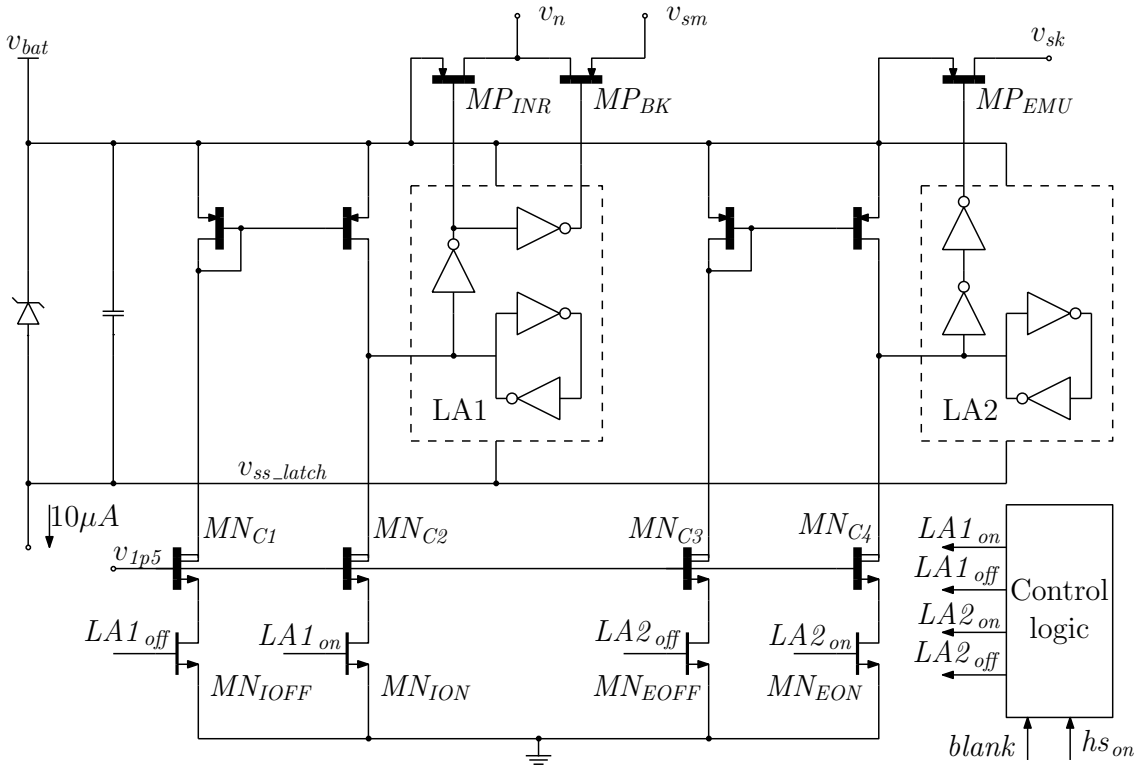


Figure 3.7: Simplified schematic of the blanker block.

same voltage signal that drives the power switch in order to ensure that the resistance ratios of the transistors of the structure are properly matched to the resistance of M_{POW}. Whenever the high-side switch turns off, the resistance of M_K rises to a very high value, the loop gain momentarily becomes very high, the offset current i_{os} is eliminated and the loop is cut open. During that time, the node v_{sk}, which is also one of the inputs of the amplifier, turns into a high-impedance node that is susceptible to any noise that can flow through the parasitic capacitances that are connected to it. The feedback resistance emulation technique solves this problem by keeping the loop closed when M_K is off with the help of switch MP_{EMU} that has approximately the same on-resistance as switch M_K ($K \cdot R_{sw}$) and can be seen in the implementation of the blanker in Fig. 3.7.

The first role of the blanker is performed with the help of switches MP_{BK} (blocking switch) and MP_{INR} (input reset switch). During blanking ($hs_{on} = 1$, $blank = 1$, Fig. 3.8c) and reset ($hs_{on} = 0$, Fig. 3.8b) MP_{BK} is off to prevent v_{sm} from reaching the input of the amplifier while MP_{INR} turns on, ties the input of the amplifier to v_{bat} (the voltage that is equivalent to $i_L = 0$). The reset phase differs from the blanking phase in the sense that MP_{EMU} is turned on to compensate for the fact that M_K (as well as the rest of the sensing structure) is off. Once the sensing structure is on and the blanking time of the sensor is over, the sensor enters in tracking mode, shown in Fig.3.8d and MP_{INR} turns

off while MP_{BK} turns on, allowing the output of the divider formed by M_M and M_N v_{sm} to reach the negative input of the amplifier.

In this work, a rather crude implementation is used to showcase the effectiveness of the concept of feedback resistance emulation. The switch is implemented as a PMOS switch that is turned on with a relatively constant v_{sg} and is sized so that its resistance is approximately $K \cdot R_{sw}$. This choice is sub-optimal as matching a PMOS device with an NMOS device under the presence of Process, Voltage and Temperature (PVT) variations is a non-trivial task but it imposed by the timing constraints of the project due to its simplicity.

Turning MP_{EMU}, MP_{BK} and MP_{INR} on and off is a challenge by itself as the control signals are generated in a low-voltage domain of the circuit but both the on and off gate voltages are close to the high-voltage v_{bat}. The most intuitive implementation involves separating the voltage domains through cascode transistors and using the control signals to turn on and off current sources, have the current cross the voltage domains and convert it on a resistor into the v_{sg} that turns the switch on, and properly size the resistor to discharge its gate in a reasonable amount of time with a scheme like that of Fig. 3.9. While intuitive, this strategy has two drawbacks. Firstly, since there will always be at least one switch that is on, the blanker is going to have some constant current consumption. Reducing this current can be done by increasing the value of the resistor but this has the side-effect of extending the time needed to discharge the gate of the switch through the resistor. Secondly, the gates of the switches have to be protected by individual clamping circuits that increase the parasitic capacitance connected in parallel of C_{gs} to account for the effect of PVT on the value of the resistor and the current provided by the current source. Lastly, the current produced by the current source cannot be very small as it needs to first charge the significant C_{gs} of the cascode transistor above it (an LDNMOS) and then both the capacitance that is connected to the gate of the switch.

Instead, this work uses a different implementation in order to achieve fast switching with no static power consumption. As seen in Fig. 3.7, the switches are driven with the help of two latches ($LA1$ and $LA2$) that force the gates of the switches to v_{bat} to turn them off and to v_{ss_latch} to turn them on. vss_{latch} is generated in a crude way with the help of a zener diode that acts both as a way to generate a voltage at a negative offset from v_{bat} and also as protection for the gates of all three switches.

The latches that control the switches change state by sending short pulses (< 5 ns) through lines $LA1_{on}$, $LA1_{off}$, $LA2_{on}$ and $LA2_{off}$ from the low-voltage domain to transistors MN_{ION} (input on), MN_{ION} (input off), MN_{EON} (feedback resistance emulation on) and MN_{EOFF} (feedback resistance emulation off). This leads to a short pulse of high current that turns on the cascode and changes the state of a latch in a very short amount

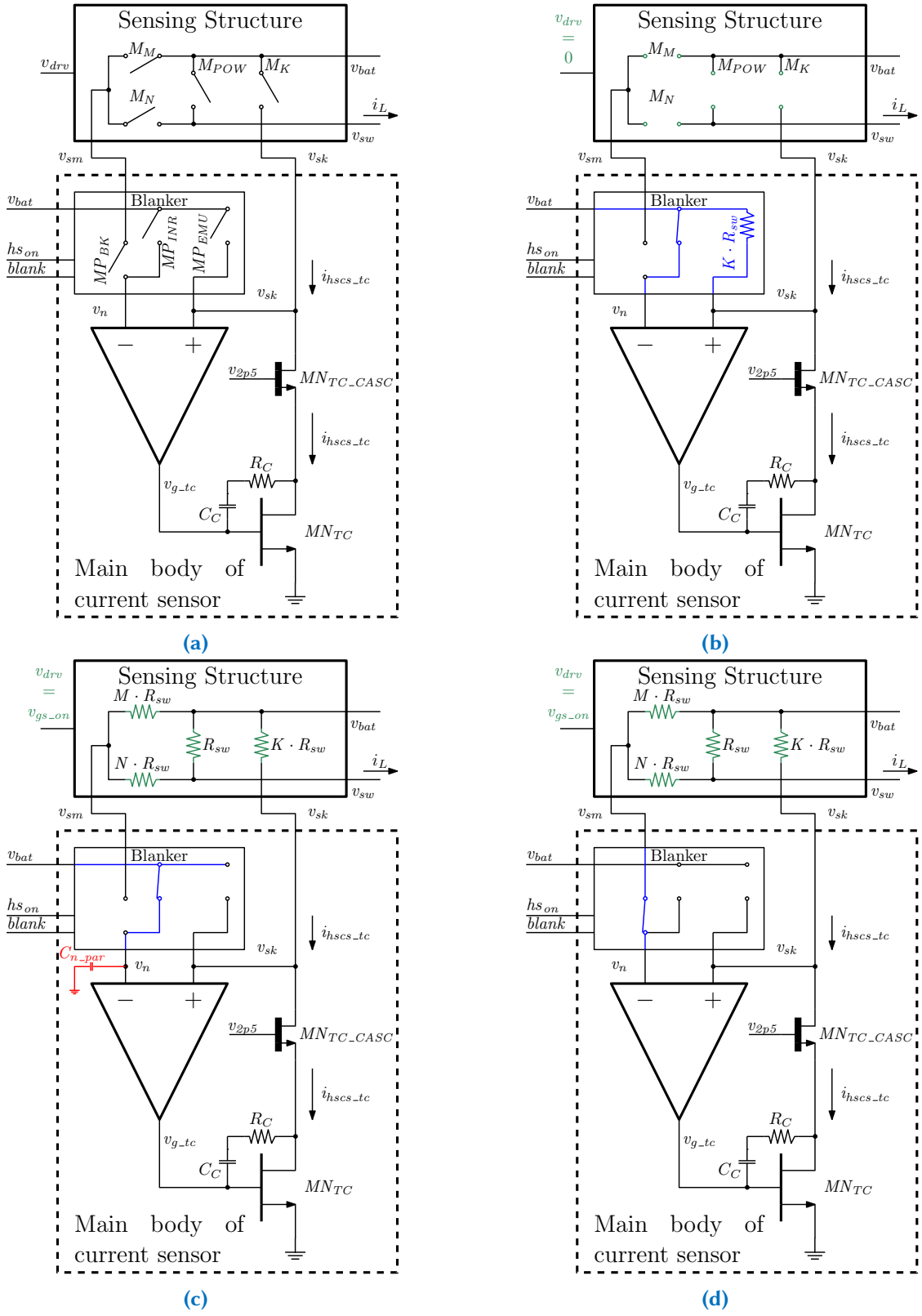


Figure 3.8: (a) Loop with blanker and sensing structure switches, (b) loop state during during reset phase ($hs_{on} = 0$), (c) during masking phase ($hs_{on} = 1$ AND $blank = 1$), (d) during tracking phase ($hs_{on} = 1$ AND $blank = 0$)

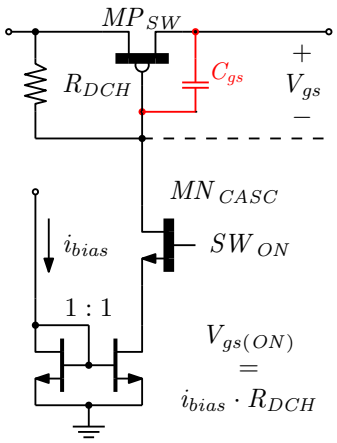


Figure 3.9: An intuitive implementation of cross-domain switch operation based on current sources and resistors

of time. Due to the short duration of the pulses, the average current consumption to turn on and off the switches remains low.

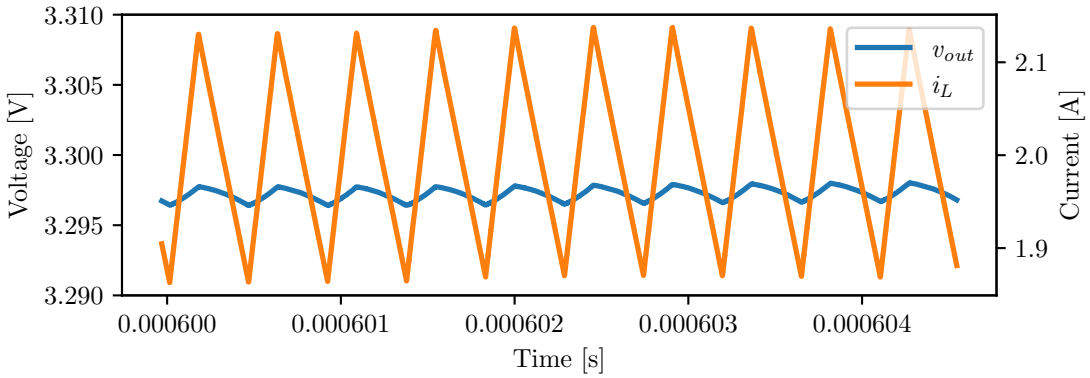
3.3.7 Simulation Results

A series of simulations with Safe Operating Area checks enabled has been performed to evaluate the ability of the sensor to meet the target specifications, the effectiveness of the new design concepts that the design incorporates as well as the limitations of its implementation. The simulations yielded no critical (Absolute Maximum Rating) SOA violations.

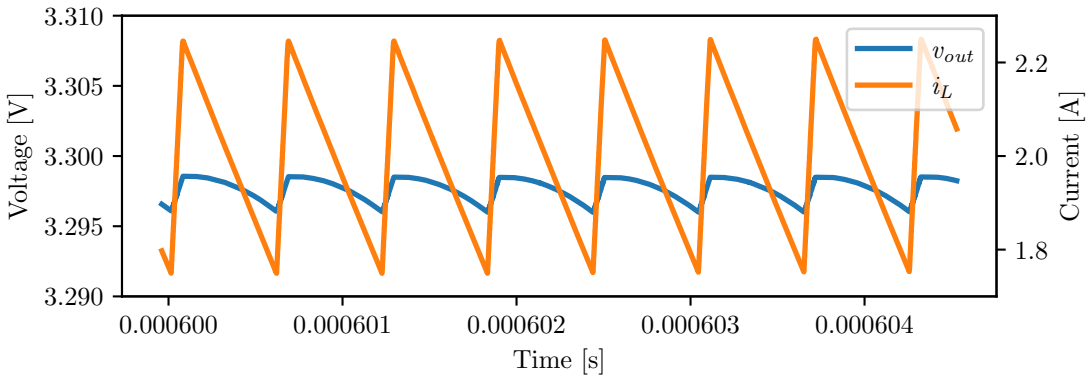
Fig. 3.11 shows what happens during a single cycle of the steady-state operation shown in Fig. 3.10a. As it is possible to see from the results, the sensed current stabilizes to its target value (minus the expected steady-state error) in less than 30 ns after the end of the blanking time.

The first specification to check is the static gain of the sensor across corners. Fig. 3.12 shows the static gain k_{CS} curves of the sensor for the full range of i_L for different corners. The gain is relatively stable with a peak-to-peak error of just 1.75% in the typical case and up to 9% across all corners despite the fact that the gate-source voltage of M_K differs by v_{os} from the gate-source voltages of M_M, M_N and M_{POW}. This is expected though as the value of $v_{gs} - v_{th}$ is significantly larger (> 1.5 V) than the offset itself.

The worst-case k_{CS} error is negative and appears at low i_L at high temperature. At such an operating point i_{hscs_out} gets close to zero and the current mirrors providing it operate at a low accuracy bias point which in turn introduces the error in the sensor gain. Fig. 3.16 further supports this argument by showing that i_{os} and $i_{hscs\_out}(i_L = 0)$ are shifted by approximately the same amount of current across corners. The low output current



(a)



(b)

Figure 3.10: Steady state for (a) $v_{bat} = 12\ V$, (b) $v_{bat} = 40\ V$.

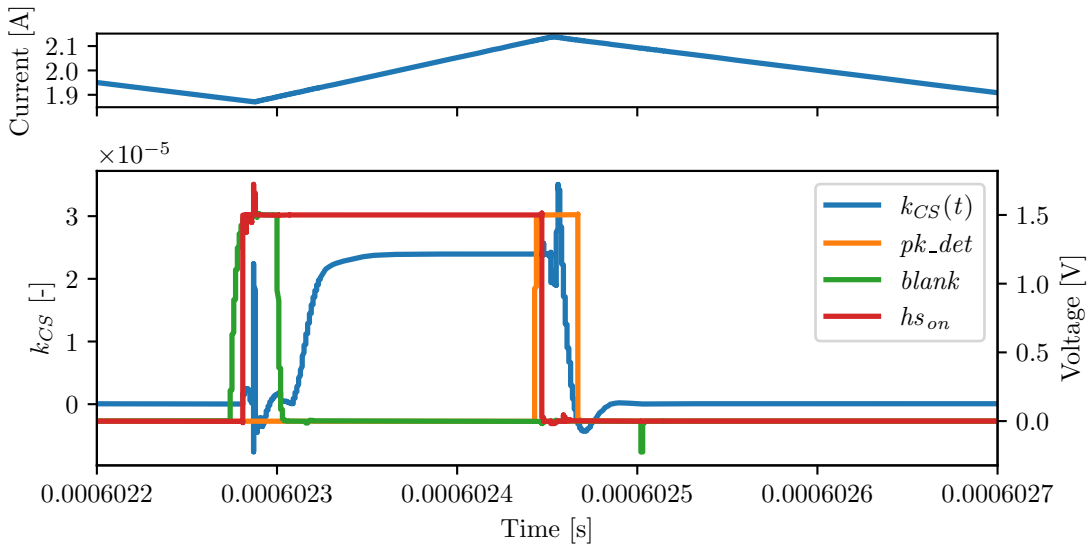
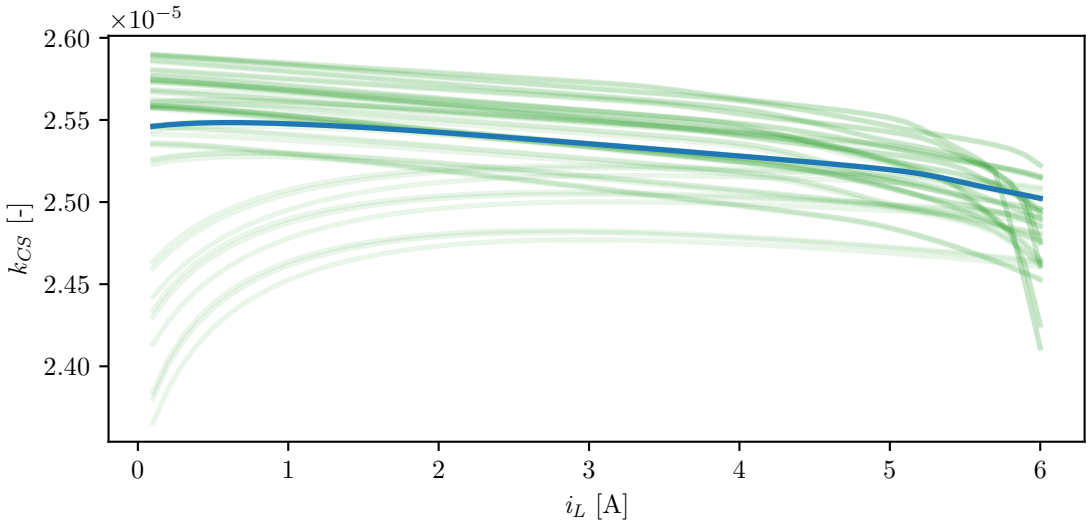
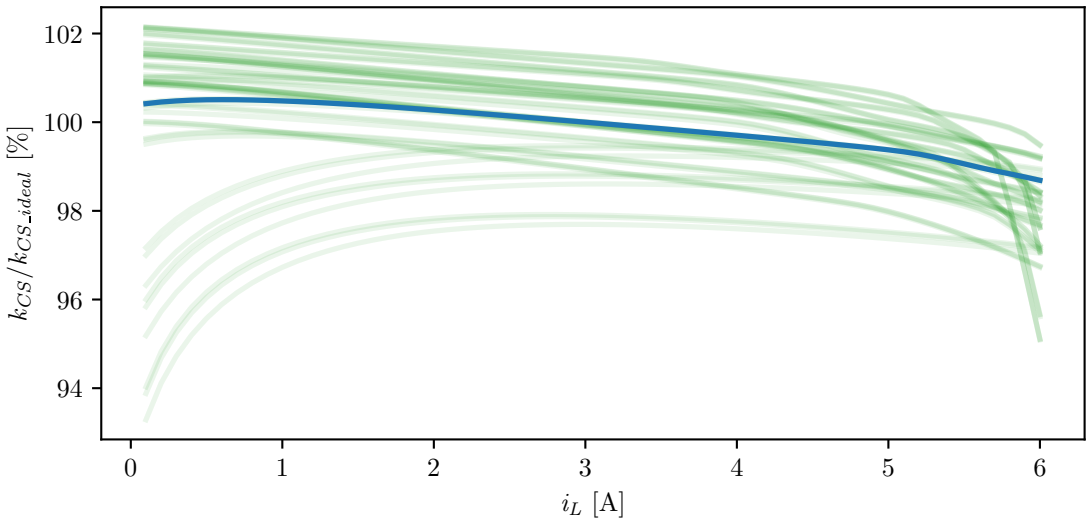


Figure 3.11: Key current sensor signals during steady-state operation



(a)



(b)

Figure 3.12: (a) k_{CS} and (b) k_{CS}/k_{CS_ideal}% curves across the full input range of the sensor and different PVT corners. Blue is typical corner.

behavior can appear at high-temperature corners due to the effect of temperature on switch resistance R_{sw} and its influence in i_{os} as seen in Eq. 3.1.

The second worst case of lost k_{CS} happens in the opposite scenario, near maximum i_L and corners that tend to increase the value of i_{os}. Here, the loss of gain is the result of the outputs of the mirrors of the output stage slowly leaving saturation and operating closer to triode.

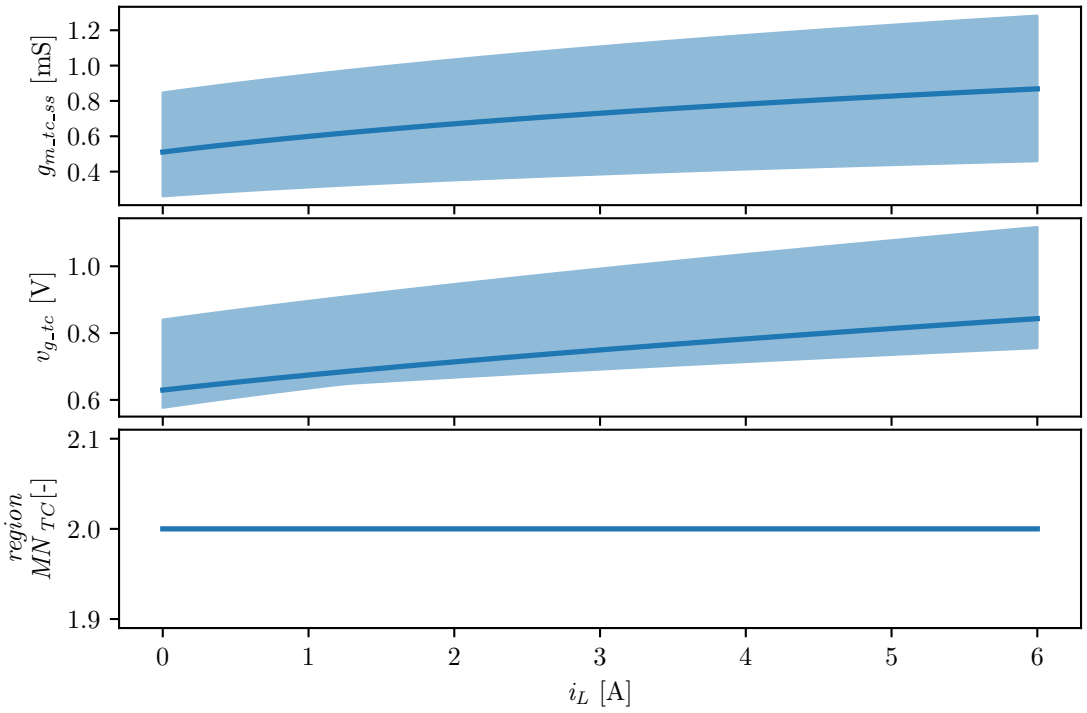


Figure 3.13: From top to bottom: Small signal transconductance of MN_{TCeff} ($g_{m\_tc\_ss}$), voltage at the input of the transconductor v_{g_tc}, and the region of operation of MN_{TC} (2= saturation) across corners. Solid line: typical value.

Another interesting plot is one showing the spread across PVT corners of quantities related to MN_{TCeff} which is the combination of MN_{TC} and the trimming transistors connected in parallel to it. The plot in Fig. 3.13 shows its small signal transconductance $g_{m\_tc\_ss}$, the gate voltage v_{g_tc} and the region of operation of MN_{TC} across all 4 process corners, the full temperature range for this chip (-40 to 100 °C), the full range of expected v_{bat} and i_L, ±10% variation of the v_{gs} of the power switches and trimming bit combinations. The plot confirms that MN_{TC} stays in saturation no matter the corner and the minimum $g_{m\_tc\_ss}$ remains above 500 µS while keeping the gate-source voltage of MN_{TC} within its safe operation limits. The proposed trimming scheme can also be used to extend the range of safe operation if there is the risk of exceeding a SOA limit.

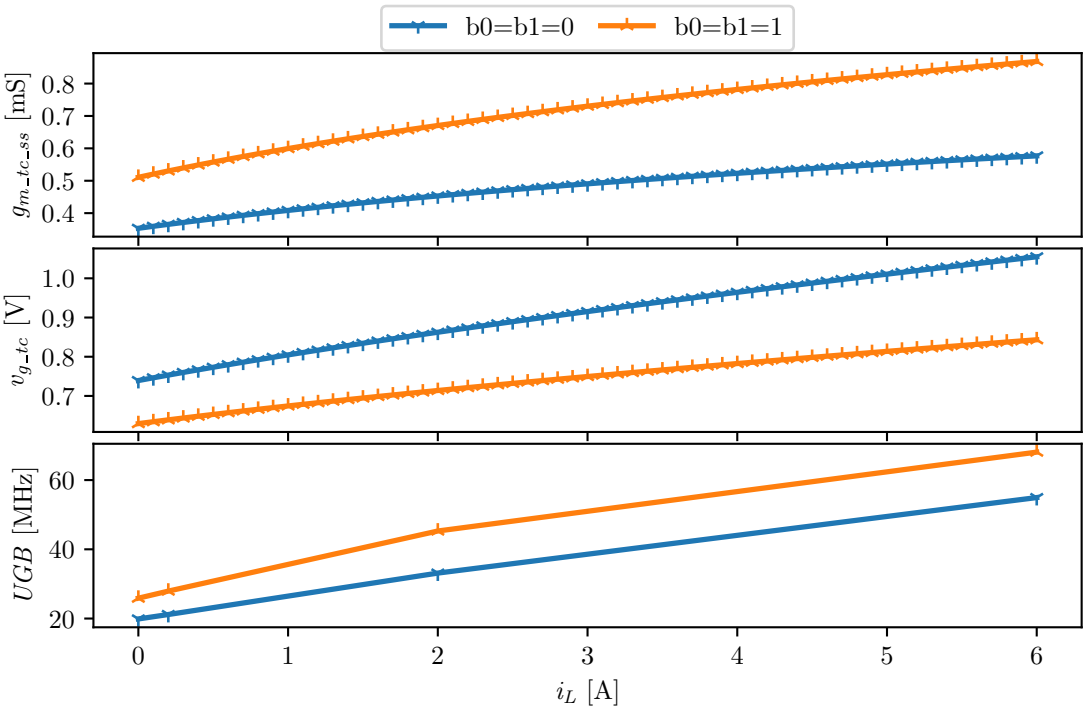
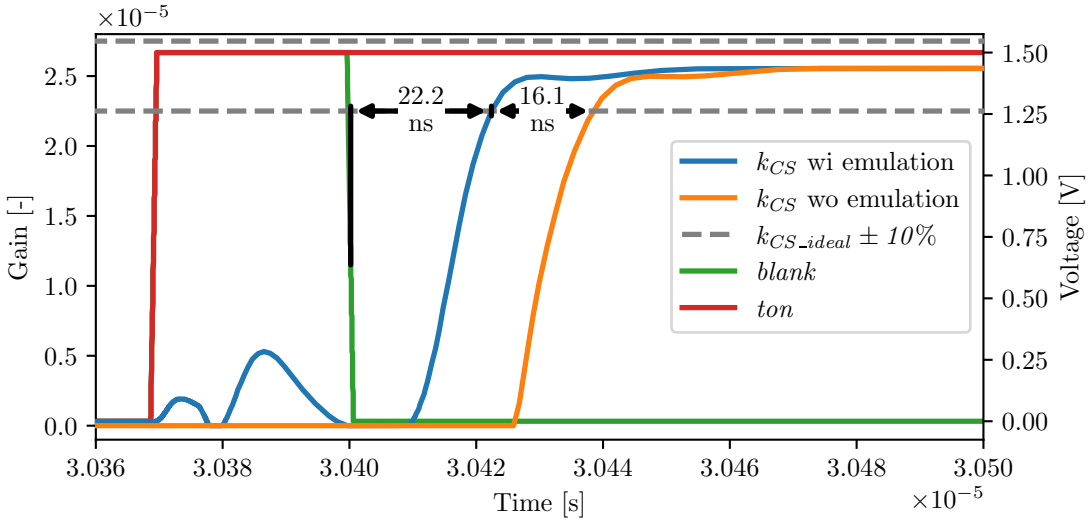


Figure 3.14: Effect of trimming on v_{g_tc}, $g_{m\_tc\_ss}$ and the UGB of the sensor

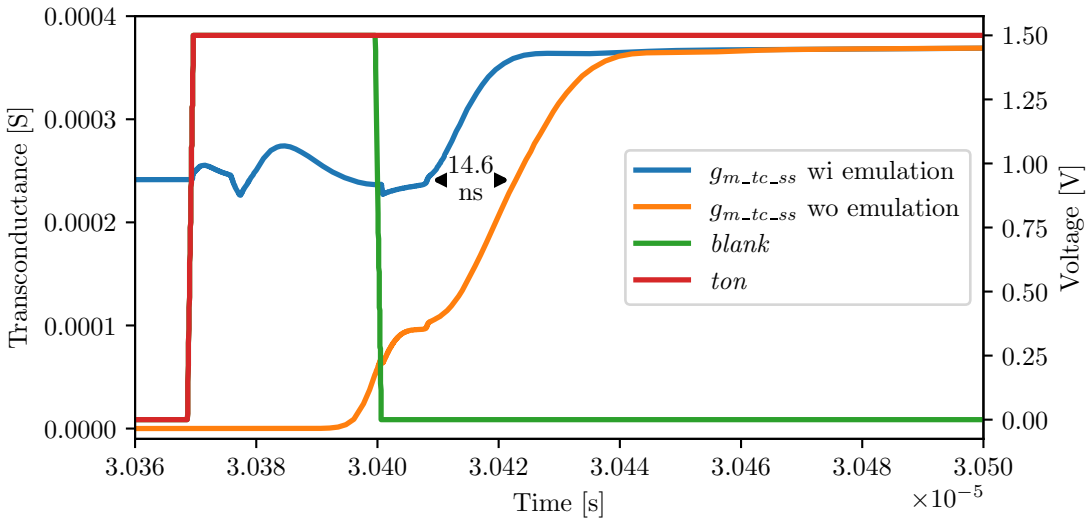
The effect of trimming on the equivalent $g_{m\_tc\_ss}$, v_{g_tc} and UGB in the nominal case can be seen in Fig. 3.14. Changing the trimming bits from setting 00 to 11 effectively doubles the W/L ratio of MN_{TCeff}, causes an approximate division of the overdrive voltage by $\sqrt{2}$ and an increase of the effective $g_{m\_tc\_ss}$ by approximately the same factor. This results to a slightly lower increase of the UGB of the loop due to an improvement of the ratio of $g_{m\_tc}/C_{gg\_m\_tc}$ (transconductance vs gate capacitance of the MN_{TCeff}) thanks to the use of small length trimming transistors and due to a change in the location of the zero of the nulling resistor that pushes UGB further up due to approaching the GBW.

The effectiveness of the operation of the block and the concept of feedback resistance emulation can be seen in Fig. 3.15. Even in this crude implementation, it enables the sensor to keep a non-zero loop gain by preventing $g_{m\_tc\_ss}$ from hitting zero and shortens its settling time by approximately 16 ns. This improvement is significant for high input voltage converters with a strict budget for sensor settling time as they have to employ a relatively long masking time to be safe from error due to switching current transients but have a very small *ton* due to the very low conversion ratio.

The short disturbance in i_{hscs_tc} is caused by charge injection from MP_{BK} and MP_{INR} on the small parasitic capacitance of node v_n (C_{n_par} of Fig. 3.8c) at the end of the blanking phase and causes a short dip of the voltage at the negative input of the amplifier. Since



(a)



(b)

Figure 3.15: (a) Example of performance improvement provided by the use of feedback resistance emulation. The emulation allows the sensor to reach 90% of the expected gain in 16.1 ns less. The dashed lines represent ±10% error from the nominal k_{cs}. (b) The behavior of the transconductance of MN_{TCeff}.

no identical dip appears at the same time on the other input of the amplifier this causes a disturbance in the output of the sensor after a while that can be caught by the peak detection circuitry if the dip is significantly larger than the dip of v_{sm} but this can be prevented through the use of techniques that mitigate the effects of charge injection like the use of dummy switches.

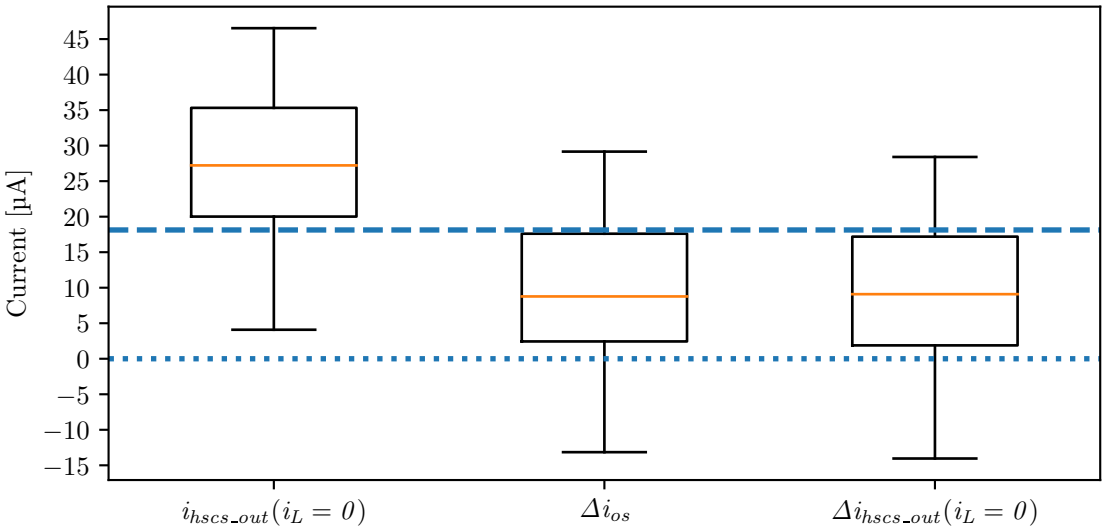


Figure 3.16: Value of $i_{hscs\_out}(i_L = 0)$ and its error vs its typical value and the same type of error for i_{os} across corners. The dashed blue line is the typical value for $i_{hscs\_out}(i_L = 0)$ and the dotted blue line the typical for the errors.

Lastly, Fig. 3.16 shows how the output offset current $i_{hscs\_out}(i_L = 0)$ varies across corners. Its variance follows that of i_{os} and is significant mainly due to its dependence to R_{sw} and also the v_{os} of the amplifier which are not easy to control. Since the offset-current removal mechanism relies on a stable current reference, this error is not mitigated in this design as seen in Fig. 3.16. However, as seen earlier in Fig. 3.13 the error of i_{os} cannot push MN_{TC} out of saturation even in the worst case and only seems to affect the output stage. Furthermore, the remaining offset error in i_{hscs_out} does not alter the small-signal gain of the sensor as long as it does not eliminate the readout current completely and as a result has no effect in the behavior of the PCM control loop. Lastly, the remaining error in the readout current can be minimized by providing a more accurate estimate of i_{os} as reference to the offset removal mirrors by using the technique described in the possible improvements section.

3.3.8 Test Setup

The schematic of the sensor was integrated in the design of an older test chip that was also provided by the company that contained the necessary blocks for operating and testing a Peak-Current-Mode Buck converter. The schematic was then given to a layout expert and the design process was concluded with a tapeout. The die can be seen in Fig. 3.17 and has an area of 5.472 mm^2 out of which the total sensor area is only 0.04529 mm^2 and out of which the 0.0085 mm^2 belong to the sensing structure. The die was finally bonded on a 24-pin PG-TSDSO-5 [43] (plastic TSDSO) package which was used during testing. The testing also required the use of a PCB capable of supporting the

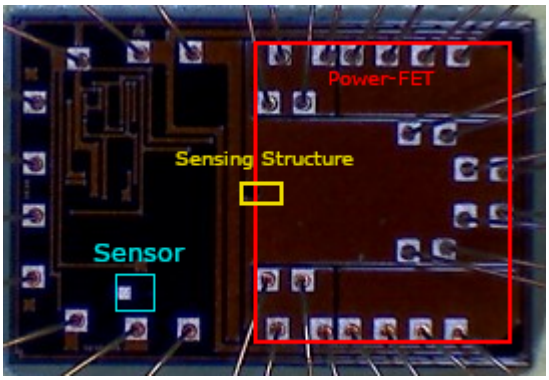
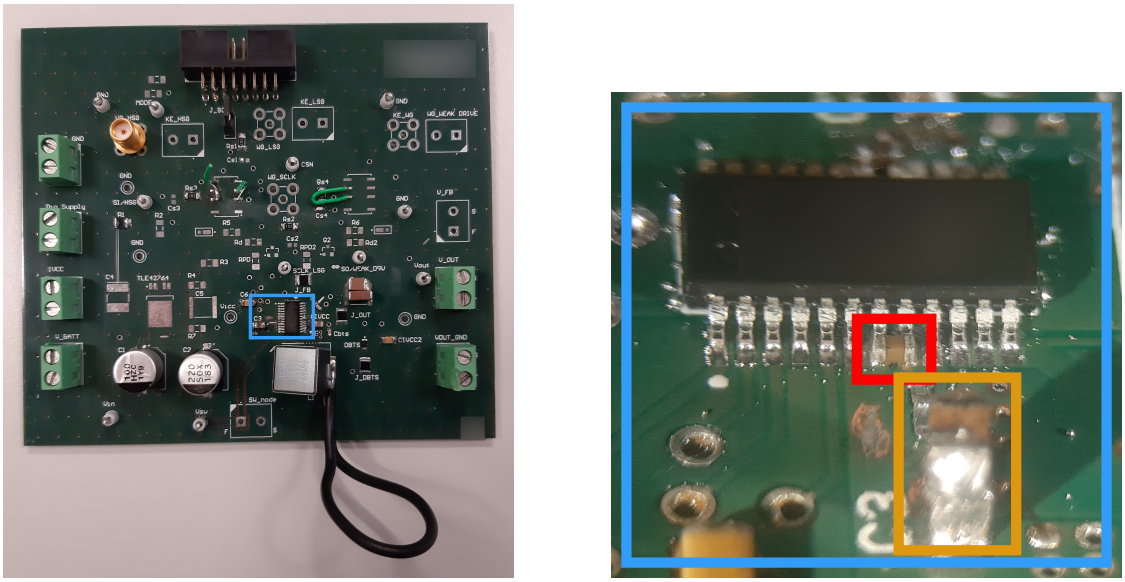


Figure 3.17: Micrograph of the die with the locations of the sensor and the sensing structure highlighted

operation of the buck as well as the communications with the digital part for the purpose of debugging. The design of the PCB had already been developed for the original design of test chip that the sensor was integrated into and supports communications with the chip through SPI by providing paths for the necessary control signals and additional test points for the outputs.

The assembled board is shown in Fig. 3.18a. Its assembly was done by hand and with the help of hot air in the case of the chip. Two inductors were used for the measurements. A shielded, composite, molded, 3.3 µH inductor by Coilcraft was used for the majority of the measurements that are included in the thesis. A high-current, shielded, ferrite core 4.7 µH inductor by Wurth (shown in the photo) was also used to ensure that the observed behavior was not affected by inductor saturation and/or coupled noise and for the high-f_{sw} transient measurements. For the transient measurements, one terminal of the inductor was connected to the PCB through a wire loop that was used as a connection point for the current probe as shown in 3.18a. The estimated additional inductance due to the wire loop was less than 100 nH and was considered to be negligible. To improve the quality of the input voltage v_{bat}, two sets of additional ceramic capaci-



(a) (b)

Figure 3.18: (a) Board photo and (b) additional capacitances.

tors were added on each side of the chip. The first set consisted of 9.4 µF capacitances that replaced the smaller ones that existed near the v_{bat} pins and was implemented as a combination of two stacked 4.7 µF capacitors. The second set consisted of 100 nF capacitors soldered directly between the pins for the v_{bat} and the power ground of the chip. Fig. 3.18b shows the added capacitors on the left side of the chip.

3.3.9 Measurements

The behavior of the DC-DC converter across different values of load current (i_{load}) and battery voltage (v_{bat}) was monitored. The line, load regulation and efficiency of the converter were measured with the help of digital and bench multimeters and its transient behavior with with the help of an 8-bit digital oscilloscope.

The measured transient voltage at the PCB pad connected to the switching node v_{sw} and its persistence plot are shown in Fig. 3.20 and Fig. 3.21. The converter operates with stable duty cycle with a minimum average on-time of 50.8 ns, out of which 22.5 ns are masking time, demonstrating that the current sensor works as expected. The measured standard deviation for ton is $\sigma(ton) = 0.87\ ns$ for $v_{bat} = 23\ V$, $v_{out} = 3.3\ V$, $f_{sw} = 3\ MHz$ and $i_{load} = 3\ A$. The output voltage v_{out} as a function of the load current i_{load}, obtained with $v_{bat} = 14$ V, and the output voltage v_{out} as a function of the input voltage v_{bat}, obtained with $i_{load} = 1.6$ A, are shown in Fig. 3.22. The achieved load and line regulation performance are 1 mV/A and 0.1 mV/V, respectively. The measured efficiency (η) as a

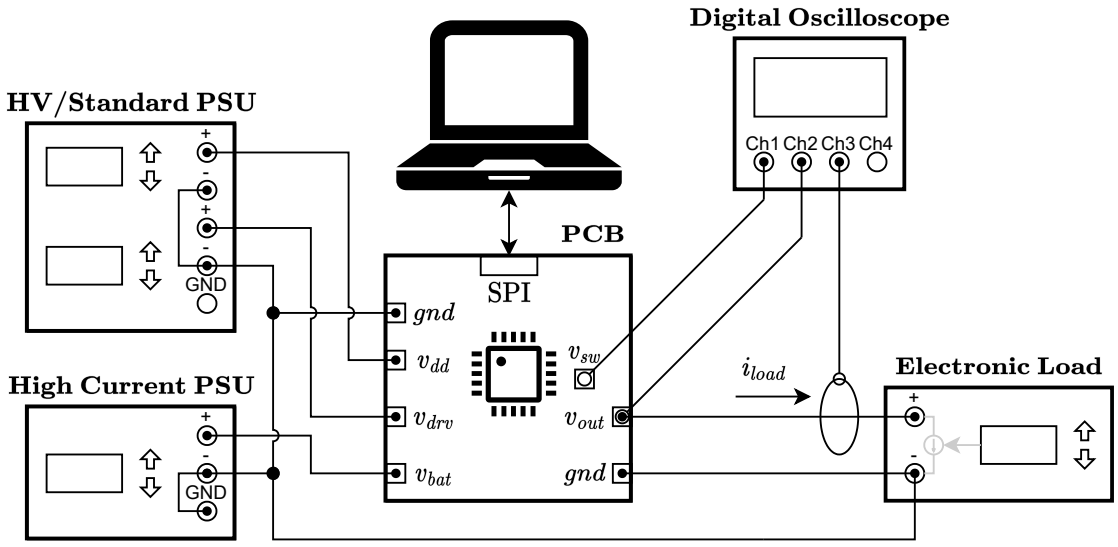


Figure 3.19: Measurement setup for load regulation setup. In the case of line regulation the high-current supply was replaced by a series combination of two HV supply channels

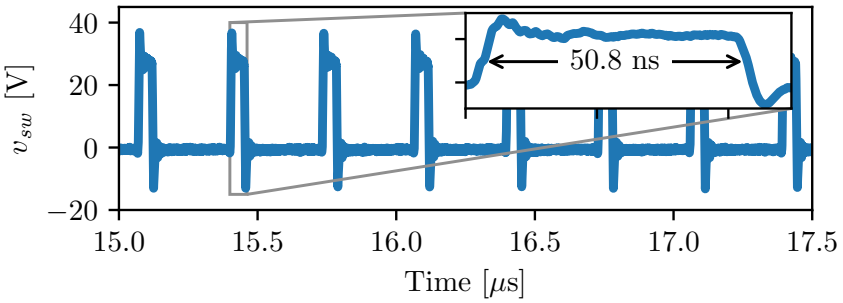


Figure 3.20: Measured v_{sw} during steady duty-cycle operation and measured *ton*.

function of v_{bat} and i_{load} is reported in Fig. 3.23, achieving a peak value of 92.5%. v_{bat} sweeps at max i_{load} were not technically possible due to the limitations of the available equipment. Finally, the performance of the sensor is summarized and compared with the state of the art in Tab. 3.3. The achieved specifications of the converter compared their initial values is given in Tab. 3.2 and the summary of the all the metrics that had been able to be produced through either measurements or simulations is given in Tab. 3.4.

The measured performance is lower than the one predicted by the simulations. The suspected cause is the underestimated inductive parasitics of the board. This theory can be hinted by Fig. 3.20 that shows ringing of significant amplitude on the voltage at the PCB pad of the switching node v_{sw}. The ringing seems to start from an amplitude of up to 10 V and decays down to approximately 1 V at 50 ns from the time that v_{sw}

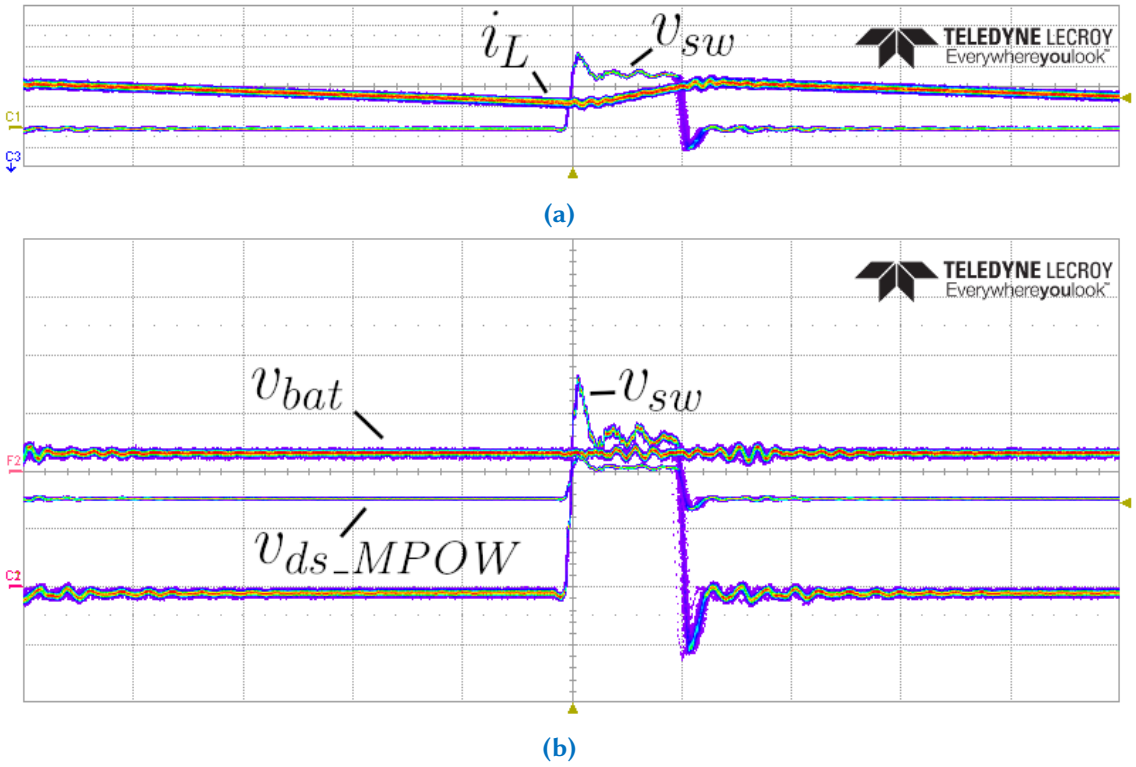


Figure 3.21: Persistence plots of the measured (a) v_{sw} and i_L, and (b) v_{sw}, v_{bat} and v_{ds_MPOW} with $v_{bat} = 23\ V$, $v_{out} = 3.3\ V$ and $i_L = 3\ A$. Vertical scales of 20 V/div -10 V offset for v_{sw}, v_{bat}, 50 V/div for v_{ds_MPOW}, 200 mA/div for i_L.

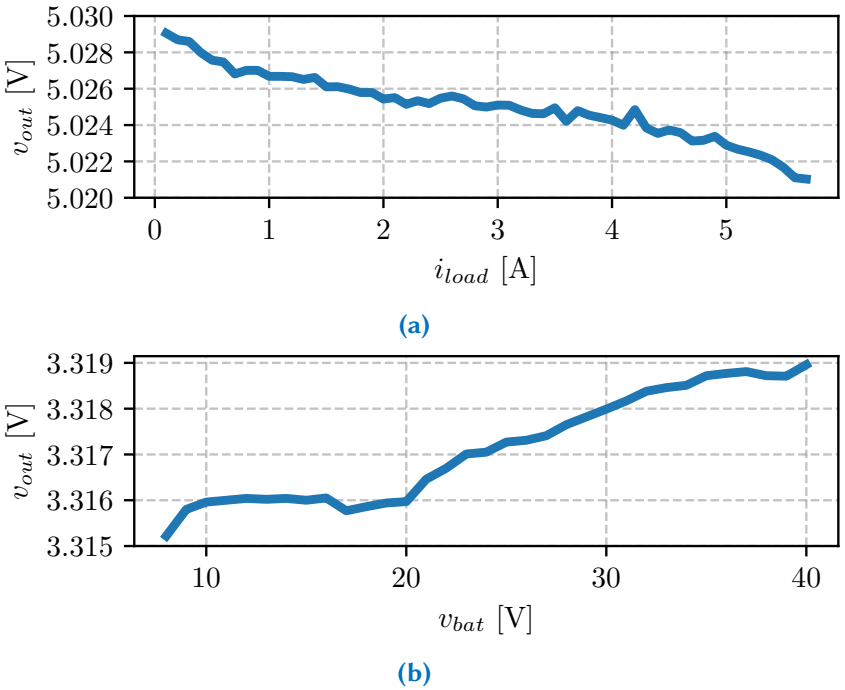


Figure 3.22: (a) Load regulation for $v_{bat} = 14\ V$, and (b) line regulation for $i_{load} = 3\ A$.

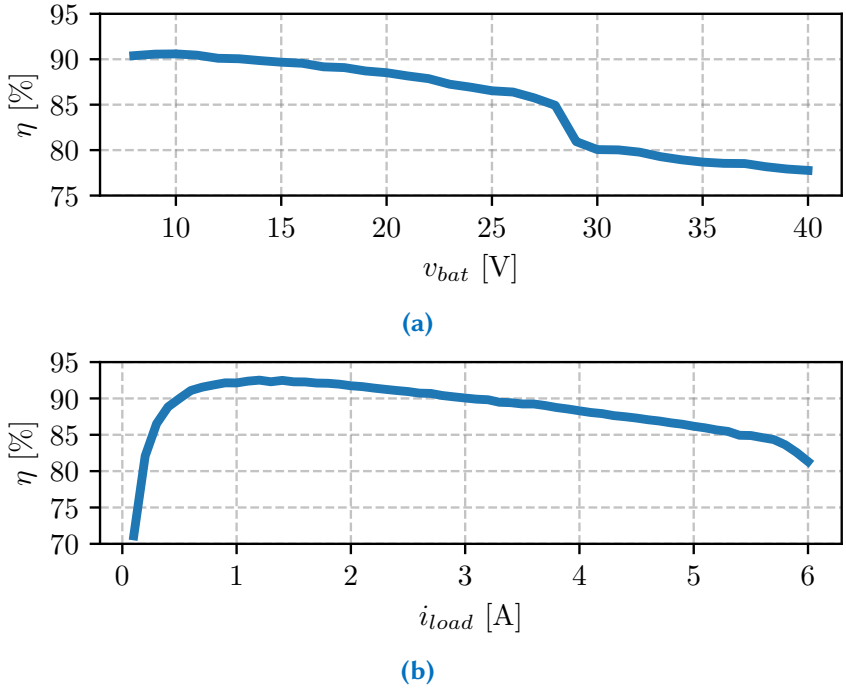


Figure 3.23: (a) Efficiency vs v_{bat} (at $i_{load} = 1.6\ A$), and (b) efficiency vs i_{load} (at $v_{bat} = 14\ V$).

Table 3.2: Target and achieved specifications for the sensor.

Parameter	Target Value	Achieved
Input Voltage (v_{bat}) [V]	6–40	6–40
Load Current (i_{load}) [A]	0.2–5.5	0.1–6.0
KILIS (inverse of gain) [-]	≈ 40k	39388
ton_{min_buck} [ns]	≤ 55	50.8
Settling time [ns]	≤ 30–45	28
GBW [MHz]	≥ 19.5	20.3
PM [deg]	≥ 70	74
I_q [µA]	As small as possible	0.0075 (off) 10 with v_{ss_latch} supply on[a]

[a] Recharging v_{ss_latch} from zero takes ≥ 10 µs and would slow down wake-up time.

Table 3.3: Performance summary and comparison of this work [38] with state of the art

Parameter	**[28]**	**[30]**	**[37]**	**This work**
Technology	180 nm BCD	350 nm BCD	180 nm	130 nm Automotive
Input Voltage (v_{bat}) [V]	4–60	2.5–4.2	5–40	6–40
Output Voltage (v_{out}) [V]	1.05–60	0.8	—	3.3, 5
Load Current (i_{load}) [A]	≤ 1.5	≤ 0.5	0.06–1.5	≤ 6
Switching Frequency [MHz]	1	2	0.5	≤ 3
Fully Integrated	No	Yes	Yes	Yes
Sensing Method	R_{sense} in L-Path	Sense-FET "Full"/Half-Wave[a]	Sense-FET Half-Wave	Sense-FET Half-Wave
Settling time [ns]	—	20	60	51
GBW [MHz]	—	—	7	20.3
Peak Efficiency [%]	96	83	—	92.5
Line Regulation [mV/V]	—	3	—	0.1
Load Regulation [mV/A]	—	46	—	1
Ripple [mV]	—	≤ 20	—	9
L_{buck} [μH]	4.7	2.2	—	3.3
$C_{out,buck}$ [μF]	10	4.7	—	69

[a] Only high-side current fully tracked. Momentarily tracks low-side current.

Table 3.4: Additional metrics.

Quantity	Source	Condition	Values
Static KILIS ($1/k_{CS}$) [-]	Simulation	T=27°C, $i_{load\_buck} = 3\ A$	39388
		full i_{load_buck} and v_{bat} range, T=-40–100°C, $v_{drv} \pm 10\%$	38986–40322
Settling time [ns]	Simulation	$i_{hscs\_out} = 90\% \cdot k_{CS} \cdot i_L + i_{ped}$[a]	28
i_{ped}[a][µA]	Simulation	$hs_{on} = 1, blank = 1$	≈ 15.5
		$hs_{on} = 1, blank = 0$	≈ 18.6
GBW [MHz]	Simulation	27°C, $i_{load} = 0.2\ A$, $trim_{tc} < 1:0 >= 00$	20.3
	Simulation	100°C, $i_{load} = 0.0\ A$, $trim_{tc} < 1:0 >= 11$	> 20.0
ton_{min_buck} [ns]	Measurement	min. avg(ton_{buck}) with $\frac{\sigma(ton_{buck})}{avg(ton_{buck})} < 2\%$	50.8
v_{bat} [V]	Measurement	Line-Regulation $\leq 0.1mV/A$ @ $v_{out} = 3.3\ V$	8–40[b]
	Simulation	Static KILIS -1.25% to +0.5% of nominal	6–40
i_{load_buck} [A]	Measurement	Load-Regulation $\leq 1mV/A$ @ $v_{out} = 3.3\ V$	0.1–5.7[c]
	Simulation	Static KILIS -7.5% to +2.5% of nominal	0.1–6
	Simulation	$PM > 70°$	0.1–6
	Simulation	Monotonic i_{hscs_out}[d]	0.56–6
Line Regulation (LiR) [mV/V]	Measurement	$v_{out} = 3.3\ V$, $i_{load} = 1.6\ A$	0.1
Load Regulation (LiR) [mV/A]	Measurement	$v_{out} = 5.0\ V$, $v_{bat} = 14\ V$	1
Expected V @ output [V]	Simulation	Output mirrors in saturation	< 1.1

[a] i_{ped}: Pedestal current. Offset current at the output of the sensor ($i_{hscs\_out}@i_L = 0$) that is left on purpose to keep the blocks connected to the peak detection node biased. In this work, it was chosen to be lower in reset phase than in the tracking phase to provide extra margin against the observed charge injection.

[b] Slope of LiR worsened between 8 and 6 V but v_{out} still above 3.3 V.

[c] Slope of LoR worsened between 5.7 and 6 A but v_{out} still above 3.3 V.

[d] Low-current non-monotonicity appears in extracted due to charge injection into C_{n_par} when the blanker is switching.

starts rising. This amplitude is far larger and slower decaying than what was observed during the simulation of the extracted view in a testbench with estimated bondwire and board parasitics which predicted that the amplitude would be one order of magnitude lower and it would have almost completely decayed within 30 ns from the moment of switching. This ringing has almost the same pattern during every switching cycle as it can be seen from the persistence plot of Fig. 3.21 so it can be safely assumed that it is not caused by some form of random noise but the result of the same circuit receiving the same stimulus in every cycle from the same initial state. The amplitude of the ringing was found to be rising with v_{bat} and i_{load} and therefore the high-voltage, high-current measurements were impossible with the same board design due to the noise caused by the ringing and the fact that the voltage across the drain and source terminals of the power transistors would exceed their maximum voltage rating and would significantly reduce the lifetime of the samples.

3.3.10 Possible Improvements

The design can receive further improvements aimed at improving its robustness against process, voltage and temperature variation and allow the sensor to have the required performance across the full temperature range required by AEC-Q100 for up to Grade-0 devices (-40°C to +150°C) [44]. Most of them are related to the implementation of the blanker and its digital control.

The proposed changes are the following:

- Optimization of the layout to reduce the parasitic capacitance at the drain of M_{TC}. The capacitance of this node had negligible effect during the first design iteration due to the the use of Miller compensation with a larger value of C_c. However, the post-layout simulations of the (faster) final design showed that the loss of g_{m_tc} above 100°C is enough to cause a visible degradation of the phase margin due to the loss of effective compensation capacitance and led to a slight non-monotonicity of the readout current. Alternatively, the size of MN_{TC} can be adjusted to increase the minimum possible g_{m_tc} and therefore the effective compensation capacitance.

- Switch from constant-current to temperature-dependent biasing for the amplifier and the offset removal blocks. This can be used to minimize the effect of temperature on the UGB and phase margin of the sensor by ensuring that any changes in R_{sw}, g_{m_tc}, A_v and v_{os} with temperature cancel each other. This is perhaps the change that would have the most impact in mitigating the sensitivity of the sensor to temperature variations.

- Investigate the possibility of turning the sensor into a "full"/half-wave hybrid like [30]. Such an architecture can eliminate the need for an offset as it can allow the sensor to sample the voltage v_{g_tc} right before the low-side switch turns off and keep the transconductor pre-biased to the state where it gives the readout current that is equivalent to the valley current. The main issue with this strategy is that the steady-state tracking error will have to kept low as a high error during the tracking of the low-side current can lead to an overestimation of the valley current and can cause false peak detection. To the above error, we also have to add the settling error during low-side sensing. However, this error is not necessarily significant as high settling error for low-side sensing happens at high duty cycle which means that the expected on-time is relatively long and the changes of the battery voltage are not that abrupt to cause a dramatic of duty cycle from high to low values between two cycles. Another way to introduce an offset would be by storing a constant offset voltage in a capacitor and connecting it at the input of the amplifier. However, this strategy is hard to implement as the designer would have to deal with charge injection, the need to operate switches at a voltage close to rail and the implementation of the circuit responsible for recharging the capacitor.

- Improve the generation of the signals that control the blanker to synchronize the transitions of MP_{EMU} and M_K and prevent momentary opening of the loop and/or having closed loop with halved gain (due to MP_{EMU} and M_K being on at the same time). This can be done by using feedback from the gates of the power switches to trigger the control signals for MP_{EMU} and current-starved inverters with controlled driving current to generate delays.

- Investigate the possibility of replacing MP_{EMU} with an LDNMOS (MN_{EMU}) and adapt the blanker accordingly. Such a change would simplify the matching of the resistances of M_K and the emulating switch across temperatures thanks to the use of the same type of channel and oxide thickness. While the feedback resistance emulation technique does not require accurate emulation of resistance, a design can still profit from minimizing this error as it relaxes the design constraint of Eq. 3.4. A possible implementation would be to use a sampled version of the bootstrap voltage to keep MN_{EMU} on when the drivers keep the power switch in off state. The transistor can also be placed physically close to M_K to further improve matching if the additional parasitic capacitance of the traces is not too high.

- Another possible improvement is to improve the accuracy of the offset removal mechanism. Currently, the mirrors that are responsible for the removal of the

offset are set to remove a constant current. However, the offset present in i_{hscs_tc} varies with the absolute value of the resistance of M_K and therefore it is relatively sensitive to variations of temperature as well as the v_{gs} of the transistors of the sensing structure. After swapping MP_{EMU} for MN_{EMU}, it is possible to exploit the feedback resistance emulation technique to further improve the accuracy of offset removal. In theory, it is possible to do so by creating a replica of MN_{TC} in the place of the transistor that sinks the offset current i_{os}, copying v_{g_tc} during when the circuit is operating in feedback resistance emulation mode and holding it on the gate of the replica. This way, it is possible to effectively copy the value of the offset current (whatever its value is after PVT) and remove it in an accurate way. The main challenge with such a strategy is the effect of mismatch between MN_{TC} and the new FET as well as any errors and performance overhead related to the mechanism used for copying and holding the voltage (extra capacitance at the output of the amplifier, recovery from charge injection, capacitors being discharged etc).

- Mitigate the bumps seen in seen in Fig. 3.15 caused by charge injection into C_{n_par} during the masking phase of the blanker (Fig. 3.8c). In this case, the bump is caused due to the fact that the turn on of MP_{BR} and the turn off of MP_{INR} are not perfectly synchronized due to the delay of the latches. This can be fixed by either making the last inverter of $LA1$ faster to sychronize the signals as much as possible or by adding properly-sized complementary NMOS switches that are driven by the same signal.

- The design can be further optimized by replacing MN_{TC} and MN_{OUT} with lower voltage devices. The current implementation uses 2.5-V devices but the range of v_{g_tc} is kept well below the limits of the faster, available lower voltage devices. This means that the same minimum value of g_{m_tc} can be achieved with lower drain current (and therefore lower i_{os}) without exceeding its SOA limit for its v_{gs}. However, such a change will require adaptations in the amplifier (offset generation and output clamping) and the biasing of the cascodes that protect MN_{TC} and MN_{OUT} to support transconductor transistors with lower voltage rating. Designing the transconductor for the same g_{m_tc} at a higher overdrive voltage also has the added benefit of decreasing its sensitivity to temperature variations.

There are also improvements that can be made to the supporting test chip and the PCB to allow for more measurements focused to the operation of the sensor.

- The easiest change would be to use a PCB with a layout optimized for low inductive parasitics in the loop that contains the current sensor. Such a change could

push the fundamental frequency of the parasitic ringing of v_{sw} further above the sensor bandwidth to ensure that it is attenuated to the point that its contribution to the output is not enough to lead to false peak detection even at when v_{bat} is at its maximum value of 40 V.

- It would be a good idea to have the ability to measure the transient response of the sensor. In order to do so, a copy of i_{hscs_out} can be converted into a voltage and then brought outside the chip with the help of a fast voltage buffer with an output stage that can drive the relatively high capacitive parasitics (both internal and external) that are connected to the test pin.

- The blocks that dictate the minimum supported on-time of the buck can be adapted to reduce that time and provide a wider margin between its value and the value of the minimum stable on-time that we want to measure. However, the verification of the ability of every other block of the chip to operate with the lowered minimum on-time would be necessary to make this possible.

3.4 Summary

A fully integrated, wide common-mode range, sense-FET based, fast response, high-side current sensor was designed. The sensor, designed in a 130-nm automotive CMOS technology, is integrated in a 40-V, peak-current Buck converter. Thanks to the proposed current sensor, the DC-DC converter is able to operate well with a minimum on-time down to 51 ns at $v_{bat} = 24$ V, $v_{out} = 3.3$ V and $f_{sw} = 3$ MHz. The DC-DC converter features a peak efficiency of 92.5% when regulating from 14 V down to 5 V with $i_{load} = 1.2$ A. A series of simple improvements have also been proposed to extend the operating temperature range of the sensor to the one required for Grade-0 automotive devices.

Conclusions

In this thesis, two new modeling tools for DC-DC converter design, as well as a design of a current sensor for CM buck converters has been presented.

The first modeling tool is a library of building blocks that are commonly used in DC-DC converter design like switches, gate drivers as well as cells that can be used for the generation of the required control signals. The blocks are in the form of technology-agnostic, high-level, parametrizable macro-models implemented as a mix of custom Verilog-A modules and standard analog library components. The parameters are design-oriented to allow the user to verify the suitability of the specifications of each block by letting them emulate their behavior under the influence of common non-idealities like offset, finite bandwidth and even support to make these parameters be affected by statistical variations in Monte-Carlo simulations. The cells do not require the use of specialized simulators and can be inserted in schematics along with other high-level or transistor-level cells and be simulated with a typical analog simulators. The blocks that represent switches and drivers make use of two new high-level switch primitives that do not introduce discontinuous behavior in the schematic in order to prevent the convergence issues that are observed when using typical switch models and also help with speeding up the simulation. Lastly, the switch and driver models can be parametrized to emulate capacitive losses in addition to resistive ones. The switch and driver cells can provide a speedup of at least 2× in the simulation of a triple output SIMO converter compared to a schematic with SPICE-level transistor models and drivers while providing nearly identical waveforms for the output voltage and inductor current, while keeping the error in estimated losses below 20% and the efficiency below 1%.

The second modeling tool is an enhanced current sensor model which is compatible with averaged models of DC-DC converters. This model is implemented in Verilog-A and is evaluated as part of a Peak Current Mode setup. In contrast to the typical modeling approach used for current sensors as a constant gain, this model takes into account the errors due to static gain non-linearity and the transient errors due to finite bandwidth and parasitic transient currents due to switching. Such errors tend to be ignored in typical DC-DC converters but they cannot be ignored in high-voltage, high switching-frequency converters as the decay time of both transient errors can become comparable to the very short on-time that they have to achieve. This can distort the shape of the sensed current and by extension the behavior of the current loop leading to instability. This model, makes use of the ability of analog simulators to solve systems of non-linear equations by introducing the non-linear equations describing these errors in the circuit. This model is suitable for both AC and (averaged-time) transient analysis.

In transient analysis, the model can provide accurate estimates of the behavior of the inductor current and output voltage of the converter with a speedup of up to 1000x compared to normal transient simulations.

The research activity was concluded with the design and testing of a fully integrated, wide common-mode range, sense-FET based, fast response, high-side current sensor. The sensor, designed in a 130-nm automotive CMOS technology, was integrated in a 40-V, Peak-Current mode Buck converter. The current sensor employs a 3-transistor sensing structure, originally used for open loop current threshold detection, as part of its closed loop architecture and retains its ability to achieve a high current division factor without excessively reducing the size of the sense-FET. The closed loop architecture relies on a folded cascode amplifier with LDMOSFET devices as cascodes to handle the large common mode input voltage and transport the signal from the high to the low voltage domain while an offset is introduced to guarantee the minimum acceptable loop bandwidth. The design implements a feedback-resistance emulation technique to prevent the debiasing of the closed loop due to the transistors of the sensing structure being turned off when the high-side power switch is switched off by turning on a switch that emulates its on-resistance. The commands to turn on or of that switch are passed from the low to the high voltage domain in ≈ 5 ns with the help of a current-pulse triggered latch-based structure without significantly increasing static power consumption. During the last part of the PhD, a set of measurements was performed to evaluate the performance of the design. Thanks to the proposed sensor, the DC-DC converter is able to achieve a stable minimum on-time of 51 ns at $v_{bat} = 24$ V, $v_{out} = 3.3$ V and $f_{sw} = 3$ MHz. The converter features a peak efficiency of 92.5% when regulating from 14 V down to 5 V with $i_{load} = 1.2$ A. A series of simple improvements have also been proposed to extend the operating temperature range of the sensor to the one required for Grade-0 automotive devices.

Bibliography

[1] T. E. D. Kizas, L. Crespi, P. Malcovati, and A. Baschirotto, "A library of high-level models for the simulation of DC-DC converters," in *2021 IEEE 12th Latin America Symposium on Circuits and System (LASCAS)*, ISSN: 2473-4667, Feb. 2021, pp. 1–4. DOI: 10.1109/LASCAS51355.2021.9459163.

[2] J. E. Jang, M. Park, and J. Kim, "An event-driven simulation methodology for integrated switching power supplies in SystemVerilog," in *2013 50th ACM/EDAC/IEEE Design Automation Conference (DAC)*, May 2013, pp. 1–7. DOI: 10.1145/2463209.2488903.

[3] M. Chen, W. Zhao, F. Liu, and Y. Cao, "Finite-point-based transistor model: A new approach to fast circuit simulation," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 17, no. 10, pp. 1470–1480, Oct. 2009, ISSN: 1063-8210, 1557-9999. DOI: 10.1109/TVLSI.2008.2005061.

[4] S. Samanta, S. Pam, H. M. Geddada, and S. Mukhopadhyay, "An improved algorithm for frequency response analysis of switching convertes and its implementation in verilog-a," in *2008 IEEE Region 10 and the Third international Conference on Industrial and Information Systems*, Dec. 2008, pp. 1–6. DOI: 10.1109/ICIINFS.2008.4798398.

[5] A. Tarraf and L. Hedrich, "Behavioral modeling of transistor-level circuits using automatic abstraction to hybrid automata," in *2019 Design, Automation Test in Europe Conference Exhibition (DATE)*, Mar. 2019, pp. 1451–1456. DOI: 10.23919/DATE.2019.8715184.

[6] K. Watanabe, M. Abe, T. Sai, and Y. Sugimoto, "A fast and precise circuit simulation method for switching power converters using a mixture of circuits and behavioral models," in *2014 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, Nov. 2014, pp. 579–582. DOI: 10.1109/APCCAS.2014.7032848.

[7] B. C. Lim and M. Horowitz, "An analog model template library: Simplifying chip-level, mixed-signal design verification," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 27, no. 1, pp. 193–204, Jan. 2019, ISSN: 1063-8210, 1557-9999. DOI: 10.1109/TVLSI.2018.2873387.

[8] A. S. Initiative. "Verilog-AMS language reference manual v.2.4.0." (May 30, 2014), [Online]. Available: https://www.accellera.org/images/downloads/standards/v-ams/VAMS-LRM-2-4.pdf (visited on 06/03/2023).

[9] "Spectre simulation platform." (), [Online]. Available: https://www.cadence.com/en_US/home/tools/custom-ic-analog-rf-design/circuit-simulation/spectre-simulation-platform.html (visited on 05/01/2023).

[10] K. Perlin, "Improving noise," in *Proceedings of the 29th annual conference on Computer graphics and interactive techniques*, ser. SIGGRAPH '02, New York, NY, USA: Association for Computing Machinery, Jul. 1, 2002, pp. 681–682, ISBN: 978-1-58113-521-3. DOI: 10.1145/566570.566636. [Online]. Available: https://doi.org/10.1145/566570.566636 (visited on 08/10/2023).

[11] *NVIDIA/MDL-SDK*. [Online]. Available: https://github.com/NVIDIA/MDL-SDK (visited on 11/22/2019).

[12] K. Hara and K. Nakayamma, "Comparison of activation functions in multilayer neural network for pattern classification," in *Proceedings of 1994 IEEE International Conference on Neural Networks (ICNN'94)*, vol. 5, Jun. 1994, 2997–3002 vol.5. DOI: 10.1109/ICNN.1994.374710.

[13] M. Bucher, C. Lallement, C. Enz, F. Théodoloz, and F. Krummenacher, "The EPFL-EKV MOSFET model equations for simulation," *EKV 2.6 Documentation*, Jul. 1998.

[14] V. Vorperian, "Simplified analysis of PWM converters using model of PWM switch. continuous conduction mode," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 26, no. 3, pp. 490–496, May 1990, ISSN: 1557-9603. DOI: 10.1109/7.106126.

[15] R. Ridley, "A new, continuous-time model for current-mode control (power convertors)," *IEEE Transactions on Power Electronics*, vol. 6, no. 2, pp. 271–280, Apr. 1991, ISSN: 1941-0107. DOI: 10.1109/63.76813.

[16] F. D. Tan and R. D. Middlebrook, "A unified model for current-programmed converters," *IEEE Transactions on Power Electronics*, vol. 10, no. 4, pp. 397–408, Jul. 1995, ISSN: 1941-0107. DOI: 10.1109/63.391937.

[17] J. Li and F. C. Lee, "New modeling approach and equivalent circuit representation for current-mode control," *IEEE Transactions on Power Electronics*, vol. 25, no. 5, pp. 1218–1230, May 2010, ISSN: 1941-0107. DOI: 10.1109/TPEL.2010.2040123.

[18] A. J. Forsyth and S. V. Mollov, "Modelling and control of DC-DC converters," *Power Engineering Journal*, vol. 12, no. 5, pp. 229–236, Oct. 1998, ISSN: 0950-3366. DOI: 10.1049/pe:19980507.

[19] S. Kapat and P. T. Krein, "A tutorial and review discussion of modulation, control and tuning of high-performance DC-DC converters based on small-signal and large-signal approaches," *IEEE Open Journal of Power Electronics*, vol. 1, pp. 339–371, 2020, ISSN: 2644-1314. DOI: 10.1109/OJPEL.2020.3018311.

[20] J. Cortés, V. Šviković, P. Alou, J. A. Oliver, and J. A. Cobos, "An optimization algorithm to design fast and robust analog controls for buck converters," in *2014 IEEE 15th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Jun. 2014, pp. 1–10. DOI: 10.1109/COMPEL.2014.6877166.

[21] A. Davoudi, J. Jatskevich, and P. L. Chapman, "Computer-aided average-value modeling of peak current-mode controlled dc-dc converters considering parasitics," in *2007 IEEE Power Electronics Specialists Conference*, Jun. 2007, pp. 2135–2139. DOI: 10.1109/PESC.2007.4342337.

[22] L. Hua and S. Luo, "Design considerations for small signal modeling of DC-DC converters using inductor DCR current sensing under time constants mismatch conditions," in *2007 IEEE Power Electronics Specialists Conference*, Jun. 2007, pp. 2182–2188. DOI: 10.1109/PESC.2007.4342346.

[23] A. E. Aroudi, "A new approach for accurate prediction of subharmonic oscillation in switching regulators—part i: Mathematical derivations," *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5651–5665, Jul. 2017, ISSN: 1941-0107. DOI: 10.1109/TPEL.2016.2606418.

[24] P. Lauritzen and C. Ma, "A simple diode model with reverse recovery," *IEEE Transactions on Power Electronics*, vol. 6, no. 2, pp. 188–191, Apr. 1991, ISSN: 1941-0107. DOI: 10.1109/63.76804.

[25] C. Ma, P. Lauritzen, and J. Sigg, "Modeling of power diodes with the lumped-charge modeling technique," *IEEE Transactions on Power Electronics*, vol. 12, no. 3, pp. 398–405, May 1997, ISSN: 1941-0107. DOI: 10.1109/63.575666.

[26] D. P. Nayak, R. K. Yakala, M. Kumar, and S. K. Pramanick, "Temperature-dependent reverse recovery characterization of SiC MOSFETs body diode for switching loss estimation in a half-bridge," *IEEE Transactions on Power Electronics*, vol. 37, no. 5, pp. 5574–5582, May 2022, ISSN: 1941-0107. DOI: 10.1109/TPEL.2021.3128947.

[27] Z. Wang and A. C. Bovik, "Mean squared error: Love it or leave it? a new look at signal fidelity measures," *IEEE Signal Processing Magazine*, vol. 26, no. 1, pp. 98–117, Jan. 2009, ISSN: 1558-0792. DOI: 10.1109/MSP.2008.930649.

[28] J. Moon, J. Lee, S. Kim, *et al.*, "60-v non-inverting four-mode buck–boost converter with bootstrap sharing for non-switching power transistors," *IEEE Access*, vol. 8, pp. 208 221–208 231, 2020, ISSN: 2169-3536. DOI: 10.1109/ACCESS.2020.3038444.

[29] S. Herzer, S. Kulkarni, M. Jankowski, J. Neidhardt, and B. Wicht, "Capacitive-coupled current sensing and auto-ranging slope compensation for current mode SMPS with wide supply and frequency range," in *2009 Proceedings of ESSCIRC*, ISSN: 1930-8833, Sep. 2009, pp. 140–143. DOI: 10.1109/ESSCIRC.2009.5326034.

[30] J.-W. Ha, B.-S. Kong, J.-H. Chun, and B.-H. Park, "A fast response integrated current-sensing circuit for peak-current-mode buck regulator," in *ESSCIRC 2014 - 40th European Solid State Circuits Conference (ESSCIRC)*, ISSN: 1930-8833, Sep. 2014, pp. 155–158. DOI: 10.1109/ESSCIRC.2014.6942045.

[31] J.-W. Ha, B.-H. Park, and J.-H. Chun, "A 7-MHz integrated peak-current-mode buck regulator with a charge-recycling technique," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, no. 7, pp. 797–801, Jul. 2017, ISSN: 1558-3791. DOI: 10.1109/TCSII.2016.2608833.

[32] G. Petrasuc, P. Miresan, M. Neag, and A. Stiglet, "Full-wave current sensor for automotive synchronous buck converter," in *2020 International Semiconductor Conference (CAS)*, ISSN: 2377-0678, Oct. 2020, pp. 249–252. DOI: 10.1109/CAS50358.2020.9267988.

[33] Z.-k. Zhou, H. Xie, Y. Shi, *et al.*, "A high-performance current sensing circuit with full-phase sampling capability," in *2013 IEEE 10th International Conference on ASIC*, ISSN: 2162-755X, Oct. 2013, pp. 1–4. DOI: 10.1109/ASICON.2013.6812050.

[34] Y. Zhou, Y. Zheng, and K. N. Leung, "Fast-response full-wave inductor current sensor for 10 MHz buck converter," *Electronics Letters*, vol. 54, no. 6, pp. 379–381, 2018, ISSN: 1350-911X. DOI: 10.1049/el.2017.4492. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1049/el.2017.4492 (visited on 06/14/2022).

[35] T. Dake and E. Ozalevli, "A precision high-voltage current sensing circuit," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 5, pp. 1197–1202, Jun. 2008, ISSN: 1558-0806. DOI: 10.1109/TCSI.2008.916452.

[36] S. Herzer, S. Kulkarni, M. Jankowski, J. Neidhardt, and B. Wicht, "Capacitive-coupled current sensing and auto-ranging slope compensation for current mode SMPS with wide supply and frequency range," in *2009 Proceedings of ESSCIRC*, ISSN: 1930-8833, Sep. 2009, pp. 140–143. DOI: 10.1109/ESSCIRC.2009.5326034.

[37] P. Renz, P. Lamprecht, D. Teufel, and B. Wicht, "A 40v current sensing circuit with fast on/off transition for high-voltage power management," in *2016 IEEE 59th International Midwest Symposium on Circuits and Systems (MWSCAS)*, ISSN: 1558-3899, Oct. 2016, pp. 1–4. DOI: 10.1109/MWSCAS.2016.7870011.

[38] T. E. D. Kizas, M. Bergo, G. Capodivacca, L. Scandola, P. Malcovati, and A. Baschirotto, "A 51-ns response-time, fully integrated, high-side current sensor for a 40-v 6-a dc–dc converter," *IEEE Solid-State Circuits Letters*, vol. 5, pp. 300–303, 2022, ISSN: 2573-9603. DOI: 10.1109/LSSC.2022.3227980.

[39] D. V. Cavalotto and E. Orietti, "Current threshold detection in synchronous regulation," U.S. Patent 9948183B2, Apr. 17, 2018. [Online]. Available: https://patents.google.com/patent/US9948183B2/en (visited on 05/11/2022).

[40] "The python language reference — python 3.7.16 documentation." (), [Online]. Available: https://docs.python.org/3.7/reference/ (visited on 05/28/2023).

[41] C. R. Harris, K. J. Millman, S. J. van der Walt, *et al.*, "Array programming with NumPy," *Nature*, vol. 585, no. 7825, pp. 357–362, Sep. 2020, ISSN: 1476-4687. DOI: 10.1038/s41586-020-2649-2. [Online]. Available: https://www.nature.com/articles/s41586-020-2649-2 (visited on 10/17/2022).

[42] P. T. Inc. "Collaborative data science." (2015), [Online]. Available: https://plot.ly.

[43] I. T. AG. "PG-TSDSO-24-5 - infineon technologies." (), [Online]. Available: https://www.infineon.com/cms/en/product/packages/PG-TSDSO/PG-TSDSO-24-5/ (visited on 10/12/2022).

[44] C. T. C. Automotive Electronics Council, *AEC-q100 -rev-h, FAILURE MECHANISM BASED STRESS TEST QUALIFICATION FOR INTEGRATED CIRCUITS*, Sep. 11, 2014. [Online]. Available: http://www.aecouncil.com/Documents/AEC_Q100_Rev_H_Base_Document.pdf (visited on 01/29/2023).