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In-Probe Front-End ASIC for MUT-Based 3-D Biomedical Ultrasound Imaging

Ph.D. Thesis of:

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To the

People Without a Country

To the

Country Without a Boundary

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List of Abbreviations

3-D	Three-Dimensional
ADC	Analog-to-Digital Converter
AFE	Analog Front-End
AGC	Automatic Gain Control
ASIC	Application-Specific Integrated Circuit
BCD	Bipolar CMOS DMOS
BJT	Bipolar Junction Transistor
BoM	Bill of Materials
BVD	Butterworth–Van Dyke model
CBF	Conventional Beamforming
CD	Cable Driver
CE	Charge Efficiency
CFA	Charge-Feedback Amplifier
CG	Current Generator

CK	Clock
CMOS	Complementary Metal–Oxide–Semiconductor
CMUT	Capacitive Micromachined Ultrasonic Transducer
CONUS	Conic Open scaNner for Ultra-Sound
CP	Co-Processing
CT	Computed Tomography
DAC	Digital-to-Analog Converter
DC	Direct Current
DMOS	Double-Diffused MOS
ECM	Equivalent Circuit Model
EMCC	Electromechanical Coupling Coefficient
EMI	Electromagnetic Interference
FE	Front-End
FEM	Finite Element Method
FGMOS	Floating-Gate MOSFET
FoM	Figure of Merit
FPGA	Field Programmable Gate Array
HD2	Second Harmonic Distortion
HV	High Voltage

IC	Integrated Circuit
IVUS	Intravascular Ultrasound
KLM	Krimholtz–Leedom–Matthei model
LDO	Low-Dropout Regulator
LNA	Low-Noise Amplifier
LV	Low Voltage
MC	Master Control
MEMS	Micro-Electro-Mechanical Systems
MIM	Metal–Insulator–Metal
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
MRI	Magnetic Resonance Imaging
MUT	Micromachined Ultrasonic Transducer
NEF	Noise Efficiency Factor
Op-Amp	Operational Amplifier
PCB	Printed Circuit Board
PGA	Programmable Gain Amplifier
PMUT	Piezoelectric Micromachined Ultrasonic Transducer
PRIN	Progetti di Ricerca di Interesse Nazionale
PSRR	Power Supply Rejection Ratio

PVT	Process, Voltage, Temperature
PZT	Lead Zirconate Titanate
QFG	Quasi-Floating Gate
RC	Resistor–Capacitor
RX	Receive
SAR	Successive Approximation Register
SNR	Signal-to-Noise Ratio
TD	Transducer
TGC	Time Gain Compensation
THI	Tissue Harmonic Imaging
TIA	Trans-Impedance Amplifier
TX	Transmit
TX/RX	Transmit/Receive
UoC	Ultrasound-on-Chip
US	Ultrasound
USB	Universal Serial Bus
VGA	Variable Gain Amplifier
R_{on}	On-State Resistance
R_{s}	Series Resistance

Introduction

Medical ultrasound has become an essential diagnostic and therapeutic tool in modern healthcare, offering real-time, non-invasive imaging with high resolution and minimal risk to patients. Its evolution over recent decades has been driven by advancements in microelectronics, transducer technology, and signal processing algorithms. Despite these developments, ultrasound systems continue to face key challenges, including power-efficient transducer driving, low-noise echo reception, effective beamforming in nonlinear and attenuative media (such as human tissue), and overall miniaturization.

Recent progress in semiconductor technologies has enabled the integration of high-voltage (HV) transmit/receive (TX/RX) switches, low-noise amplifiers (LNAs), and front-end application-specific integrated circuits (ASICs), leading to highly compact and power-efficient ultrasound probes. A particularly promising innovation is the adoption of Capacitive Micromachined Ultrasonic Transducers (CMUTs), which offer superior bandwidth, scalability, and compatibility with standard CMOS processes. Compared to traditional piezoelectric transducers, CMUTs enable lower power consumption, improved sensitivity, and seamless integration with on-chip electronics.

However, these benefits introduce new design constraints. Developing optimized front-end circuits that meet stringent requirements for power efficiency, noise performance, and miniaturization remains a significant challenge. This thesis addresses these issues by exploring the design and implementation of high-performance analog front-end solutions for CMUT-based 3-D ultrasound imaging systems.

The primary objective of this research is to design, implement, and evaluate a four-channel CMUT-based analog front-end ASIC for 3-D ultrasound imaging. The work focuses on optimizing critical performance metrics such as power consumption, noise, off-isolation, and overall system efficiency. The resulting chip is highly adaptable and applicable to various ultrasound imaging applications. The research spans the entire development cycle, covering study, design, simulation, layout, fabrication, PCB integration, and final validation.

Key Contributions

This dissertation presents several significant contributions to ultrasound imaging system design:

- **Four-Channel CMUT-Based Analog Front-End ASIC:** A fully integrated and optimized solution tailored for 3-D ultrasound imaging.
- **Power and Noise Optimization:** The proposed design significantly reduces power consumption and noise, carefully balancing efficiency and imaging performance.
- **Comprehensive Design and Implementation:** The research covers the entire ASIC development process, including schematic design, simulation, layout, PCB integration, and experimental characterization.
- **Versatile Application Scope:** Although designed for 3-D imaging, the proposed ASIC is suitable for a variety of ultrasound applications, such as portable diagnostics, Doppler imaging, and elastography.

Thesis Organization

- **Chapter 1** introduces the fundamentals of ultrasound imaging systems, ultrasound integrated circuits,and the motivation behind this research.
- **Chapter 2** provides an overview of the entire project framework and introduces the various components that constitute the overall system.
- **Chapter 3** outlines the design considerations and architecture of the proposed four-channel CMUT-based front-end ASIC, including the circuit-level design, including TX/RX switching, low-noise amplification, and the other blocks.
- **Chapter 4** describes the implementation process, including layout design, fabrication, and PCB integration, and experimental validation, presenting measurement results and comparisons with state-of-the-art solutions.
- **Chapter 5** concludes the thesis with a summary of contributions and suggestions for future research directions.

By addressing critical challenges in power efficiency, noise reduction, and integration, this research contributes to the advancement of next-generation ultrasound imaging technologies, enabling more compact, energy-efficient, and high-performance diagnostic systems.

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Chapter 1

Medical Ultrasound Integrated Circuits

Ultrasound refers to acoustic waves with frequencies above 20 kHz, placing them beyond the upper threshold of human hearing [1]. Due to its favorable characteristics—such as safety, non-invasiveness, and real-time imaging—ultrasound has become a vital tool in medical diagnostics and therapy. To appreciate its current relevance and anticipate future developments, it is important to reflect on its historical evolution.

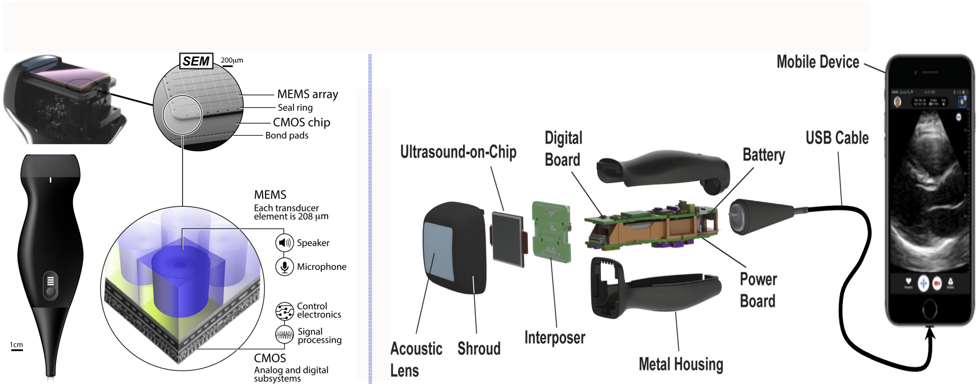
The origins of ultrasound date back to the late 1800s, a period marked by foundational theoretical and experimental contributions. Among the most influential figures was John William Strutt, better known as Lord Rayleigh, whose seminal work *"The Theory of Sound"* laid the groundwork for understanding acoustic phenomena [2]. Around the same time, the Curie brothers, Pierre and Jacques, discovered the piezoelectric effect in 1880—a principle later critical to ultrasound transducer development. While much of the early work in ultrasound was directed toward sonar applications, this thesis focuses on advances in medical ultrasound from the 1950s onward. For a more comprehensive historical perspective, readers are referred to [3, 4].

The 1950s marked a transformative era in medical ultrasound. In 1953, Inge Edler and Carl Hellmuth Hertz conducted the first echocardiographic examination, a major advancement in cardiac diagnostics. Later in the decade, in 1958, the groundbreaking study *Investigation of Abdominal Masses by Pulsed Ultrasound* by Ian Donald, John Macvicar, and Tom Brown revolutionized the use of ultrasound in obstetrics and gynecology [5]. These pioneering achievements firmly established imaging as the central focus of ultrasound research.

Despite early successes, ultrasound systems of that time were hindered by various limitations, such as large equipment size, suboptimal image quality, and high operator dependency. To address these shortcomings, research in the following decades pursued improvements along three key avenues: (i) the development of smaller and more efficient ultrasound transducers, (ii) the design of specialized integrated circuits (ICs) to enhance system integration and portability, and (iii) the creation of advanced signal processing techniques to improve image clarity. In particular, the work in [6, 7] initiated the design of imaging ICs capable of processing data from phased-array transducers in real time—a milestone that leveraged the rapid evolution of CMOS technology and helped drive miniaturization.

Equally transformative was the introduction of Capacitive Micromachined Ultrasonic Transducers (CMUTs), which emerged as a promising alternative to traditional piezoelectric transducers [8–10]. CMUTs offer several advantages, including wider bandwidth, easier fabrication of large arrays, and superior compatibility with CMOS electronics [11], positioning them as a key enabler for next-generation ultrasound systems.

For example, in the work by Rothberg *et al.* [9], a complete Ultrasound-on-Chip (UoC) device utilizing CMUTs for medical imaging is developed. As illustrated in Fig. 1.1(a), the system is built around a 140×64 CMUT array monolithically integrated with CMOS circuitry for control and signal processing, enabling the realization of a cost-effective full-body ultrasound imaging probe. The integrated CMOS layer includes thousands of transmitters, amplifiers, and analog-to-digital converters (ADC), achieving more than a trillion operations per second while consuming only 3 W of power. Fig. 1.1(b) presents a detailed view of the probe's structure.



(a) (b)

Figure 1.1: (a) CMUT-based UoC probe, (b) UoC probe breakdown [9].

The CMUT-CMOS chip is enclosed by an acoustic lens and wire-bonded to a PCB interposer. This interposer connects to a secondary board equipped with a Field Programmable Gate Array (FPGA) and a USB interface for communication with a mobile device. This compact and handheld scanner represents a new generation of ultrasound imaging tools, characterized by ease of use and accessibility. Unlike traditional ultrasound systems, this device does not require specialist training, making it suitable for use by general clinicians or even the general public [9].

Reflecting on the trajectory of medical ultrasound, it is evident that the field remains vibrant and innovative. This sustained interest stems from two primary factors. First, unlike modalities that involve ionizing radiation—such as X-rays and CT scans—ultrasound is inherently safer for patients [12]. Second, the synergy between CMOS technology and CMUT development has accelerated the trend toward compact, integrated systems. Miniaturization not only enhances device portability and reliability but also reduces overall system costs. The impact of this shift is exemplified by companies like Butterfly Network, Inc., which is pioneering handheld, smartphone-connected ultrasound devices designed to replace bulky, traditional systems [13].

A high-level overview of a typical ultrasound imaging system architecture is illustrated in Figure 1.2. Understanding the system at this level provides crucial insight into how individual hardware modules interact to achieve efficient imaging performance.

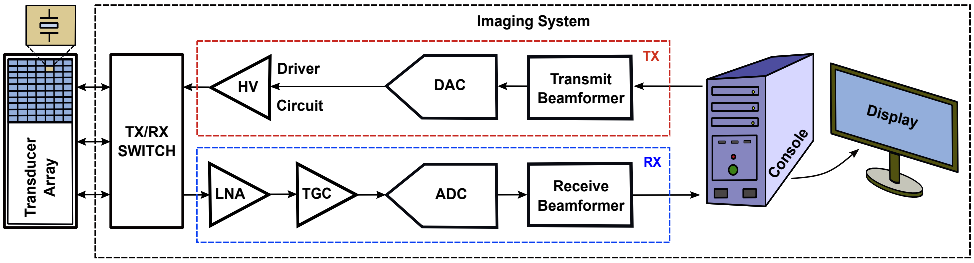


Figure 1.2: General block diagram of a typical ultrasound imaging system.

On the transmit (TX) side, the beamformer plays a key role by generating appropriate delay patterns (in the time domain) and amplitude weights (in the amplitude domain) to shape the outgoing ultrasound beam according to imaging requirements. The signals produced by the TX beamformer are then amplified by the transmitter driving circuitry, boosting them to high-voltage levels—often several tens of volts—to excite the transducer elements.

These excitation signals may vary in waveform shape, ranging from square and sine waves to Gaussian pulses, depending on application-specific constraints. In certain scenarios—such as intravascular or implantable imaging—the transducer driver circuitry may be replaced by high-voltage (HV) switches. These switches route pre-generated HV pulses from an external imaging system to the transducer, significantly reducing the on-chip power consumption [14]. This approach is particularly critical for power-sensitive, implantable designs. In contrast, for non-implantable or portable ultrasound devices, such as those described in [13], power constraints are generally less stringent. However, even in these cases, efficiency remains important due to the limitations imposed by battery operation.

On the receive (RX) path, the system first employs a transmit/receive (TX/RX) switch. This component isolates the sensitive, low-voltage (LV) RX circuitry from the potentially damaging HV TX pulses, protecting downstream components. Once the echoes from the tissue return, a low-noise amplifier (LNA) amplifies the weak signals. Ideally, the LNA also incorporates time-gain compensation (TGC) functionality, which helps to counteract the natural attenuation of the ultrasound signal as it penetrates deeper into tissue.

Following amplification, the RX beamformer applies appropriate delay and amplitude adjustments to the received echoes—effectively performing a time-reversed complement of the transmit beamforming process. Lastly, the analog signals are digitized by an ADC, enabling further processing and image reconstruction in the digital domain.

1.1 Basics of Medical Ultrasound

1.1.1 A Brief Description of Waves

Ultrasound, a subset of acoustic waves, belongs to the category of mechanical waves, which facilitate the transmission of energy without transporting mass from one point to another [15]. In medical applications, ultrasound waves are predominantly considered longitudinal. This assumption is based on the nature of soft biological tissues, which can be approximated as fluid-like media that inherently do not support the propagation of shear (or transverse) waves. Nevertheless, under certain conditions—particularly at low frequencies—shear waves can still propagate through soft tissues [1]. This phenomenon forms the foundation of a specialized imaging modality known as elastography, which exploits these shear waves to evaluate tissue stiffness [16, 17]. For the purpose of this thesis, however, all ultrasound waves will be treated as longitudinal in nature.

Ultrasound waves can further be categorized based on their spatial propagation characteristics, typically as either *plane* or *circular* waves. Plane waves exhibit uniform amplitude with surfaces of constant phase orthogonal to the direction of travel. In contrast, circular waves radiate symmetrically from a point or line source [1]. The geometry of the emitted wavefront is primarily influenced by the transducer's shape and dimensions. For example, when the diameter of a circular transducer is small relative to the wavelength of the emitted ultrasound wave, the wavefront tends to adopt a more spherical profile [1].

The behavior of ultrasound waves can be rigorously described by the wave equation in three dimensions, which governs the dynamics of wave propagation. The general form is expressed as:

$$\frac{1}{c^2}\frac{\partial^2 u}{\partial t^2} = \frac{\partial^2 u}{\partial x^2} + \frac{\partial^2 u}{\partial y^2} + \frac{\partial^2 u}{\partial z^2} = \nabla^2 u \tag{1.1}$$

where u represents the wave function, t denotes time, x, y, and z are spatial coordinates, and c is the speed of sound in the medium.

1.1.2 Transmission and Reflection

Consider an acoustic wave propagating through a material medium, where the pressure gradient generated by the wave induces motion and strain on the particles of the medium [1]. The pressure gradient, denoted as P, and the particle velocity, U, in this context are analogous to the voltage and current in electrical systems, respectively. Acoustic impedance, which characterizes the resistance of the medium to wave propagation, is defined as:

$$Z_{\text{acoustic}} = \frac{P}{U} \tag{1.2}$$

It is important to note that acoustic impedance depends on the pressure, which is directly related to the amplitude, power, and intensity of the acoustic wave. As a result, it is useful to employ acoustic impedance to derive analogs to the Fresnel coefficients commonly used in optics. The coefficients for pressure reflection, transmission, intensity reflection, and intensity transmission are defined in Equations (1.3)-(1.6), where θ_I and θ_T represent the angles of incidence and transmission, respectively, and Z_1 and Z_2 are the acoustic impedances of the two media. These equations describe the propagation of the acoustic wave from medium 1 to medium 2.

$$R = \frac{Z_2 \cos\theta_I - Z_1 \cos\theta_T}{Z_2 \cos\theta_I + Z_1 \cos\theta_T} \tag{1.3}$$

$$T = \frac{2Z_2 \cos\theta_I}{Z_2 \cos\theta_I + Z_1 \cos\theta_T} \tag{1.4}$$

$$I_R = \frac{P_2 R^2 Z_1^2}{Z_1 P_2 I} \tag{1.5}$$

$$I_T = \frac{P_2 T^2 Z_2^2}{Z_1 P_2 I} = \frac{Z_1}{Z_2} T^2 \tag{1.6}$$

Two extreme cases of acoustic wave interaction with materials are particularly noteworthy. First, if the acoustic impedance of the second medium (Z_2) is much greater than that of the first medium (Z_1), the reflection coefficient (R) and the transmission coefficient (T) both approach unity. In this scenario, the reflected wave experiences almost no decrease in amplitude. Second, when Z_1 is much larger than Z_2, the reflection coefficient approaches -1, indicating a complete phase shift of π radians relative to the incident wave, but with negligible loss in amplitude. A typical case of this phenomenon occurs when air bubbles are present between the skin and the ultrasound transducer (e.g., when no coupling gel is applied), leading to strong reflections and degraded imaging quality.

To mitigate poor imaging caused by significant impedance mismatches between the transducer and the medium, an impedance matching layer is often incorporated. This layer serves as an intermediary between the ultrasound transducer and the target medium (e.g., human tissue), facilitating better transmission of the ultrasound waves and improving image quality.

1.1.3 Attenuation

As an acoustic wave propagates through a medium, it inevitably undergoes attenuation. This attenuation follows an exponential decay, which can be expressed mathematically as:

$$A(x) = A_0 \exp(-\alpha x) \tag{1.7}$$

where $A(x)$ represents the amplitude of the wave at a distance x, A_0 is the initial amplitude at $x = 0$, and α is the attenuation coefficient.

In the context of medical ultrasound, the attenuation coefficient α depends on the frequency of the wave. Higher frequencies result in greater attenuation as they propagate through tissues [1]. This means that ultrasound waves with higher frequencies (which correspond to shorter wavelengths) offer higher resolution but experience more significant attenuation, limiting their penetration depth into tissues. Conversely, lower-frequency waves, with longer wavelengths, suffer from less attenuation but provide lower resolution.

For instance, the attenuation coefficient for soft tissues is typically around 0.5 dB/cm/MHz, while for bone tissue it ranges from 10 to 20 dB/cm/MHz [1]. Therefore, there is an inherent trade-off between penetration depth and resolution in ultrasound systems, with higher frequencies achieving better resolution but having shallower penetration capabilities.

For this reason, typically high frequency ultrasound (above 20 MHz) is mainly used in dermatology for the detection of various skin pathologies, while low frequency ultrasound (below 5 MHz) has medical applications for deep abdomen, obstetric and gynaecological imaging. In the range between 5 MHz and 15 MHz, ultrasound probes are successfully used for many clinical diagnostics including vascular, breast, thyroid and pelvic imaging.

1.2 Ultrasound Transducers

In ultrasound imaging systems, the transducer serves a dual purpose: it generates acoustic waves that propagate through the body (actuator) and captures the reflected echoes (sensor) that carry diagnostic information [18]. The time it takes for these echoes to return provides data about the depth of internal structures. However, to accurately distinguish between objects or scatterers that lie side by side (lateral resolution), beamforming techniques are employed.

To facilitate beamforming, transducers are typically structured as arrays composed of multiple discrete elements. For conventional two-dimensional (2-D) imaging, one-dimensional (1-D) arrays—such as linear or phased arrays—are commonly used and may include up to 256 individual elements. In contrast, three-dimensional (3-D) imaging systems, which do not rely on mechanical scanning, require 2-D arrays (often called matrix transducers), which may comprise thousands of elements.

The physical size, or aperture, of the transducer array influences both the field of view and the achievable spatial resolution. Additionally, the spacing between elements (pitch) is a critical design factor dictated by beamforming constraints—especially the necessity to suppress grating lobes. For phased-array configurations, maintaining an element pitch of approximately half the wavelength is typically required to achieve optimal performance [18].

There are three primary types of ultrasound transducers: (i) piezoelectric materials, (ii) capacitive micromachined ultrasound transducers (CMUTs), and (iii) piezoelectric micromachined ultrasound transducers (PMUTs). PMUTs offer several advantages over CMUTs, such as not requiring a high voltage bias, which makes integration with low-voltage CMOS electronics easier [19]. Examples of research utilizing PMUTs can be found in [20, 21]. However, despite these benefits, PMUTs have not been widely adopted when compared to piezoelectric materials and CMUTs, largely due to fabrication difficulties, performance issues, and the lack of accurate design and modeling tools [19]. A comparison of ultrasound transducers is presented in Table I.

Table 1.1: Comparison of Ultrasound Transducers

Transducer Type	Advantages	Disadvantages
PZT	Established technology.	No CMOS integration. No volume production.
PMUT	CMOS integration. High volume production. No need for large DC bias.	Theoretical and engineering problems remain.
CMUT	CMOS integration. High volume production. High bandwidth.	Needs large DC bias.

1.2.1 Piezoelectric Ultrasonic Transducer

Piezoelectric transducers, commonly referred to as PZTs, represent the most established class of ultrasonic transducers, with their origins tracing back to the late 1800s. Their operation relies on the *piezoelectric effect*—a property of certain materials to generate an electric field when subjected to mechanical stress [1]. Conversely, these materials also deform when an electric field is applied, producing mechanical strain. Materials frequently used in PZT devices include quartz, Rochelle salt, polyvinylidene difluoride, and most prominently, lead zirconate titanate, which was formulated in the 1950s by Jaffe [22] and remains the material of choice today.

Figure 1.3 illustrates the layered architecture of a typical PZT device. The impedance matching layer plays a critical role in optimizing energy transmission into biological tissues [23, 24], while the backing layer helps suppress prolonged vibrations by introducing damping—essential for improving axial resolution, especially in high-quality transducers [25]. In certain configurations, external impedance matching networks may be required to further enhance performance [26, 27].

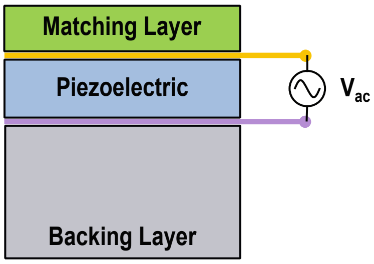


Figure 1.3: Structure of a typical PZT transducer [1].

1.2.1.1 Modelling of PZT Transducers

Over time, significant effort has been devoted to modeling and characterizing the behavior of PZTs. Early models, such as those proposed by Mason, the Krimholtz–Leedom–Matthei (KLM) model, and the Butterworth–Van Dyke (BVD) model [28–30], were circuit-based and intended to translate electromechanical phenomena into formats familiar to electrical engineers. These approaches often leverage analogies between electrical and mechanical domains—e.g., voltage-current pairs analogized with force-velocity, and RLC circuits with friction-spring-mass systems. Software-based models that use finite element methods (FEM) have also been developed [31, 32].

The operational characteristics of PZTs are determined by the nature of the applied vibrations—typically compressional or shear [33]. Assuming a transducer operates in compressional thickness mode (i.e., modeled as a thin plate), the KLM model (Figure 1.4) is frequently used due to its improved physical realism compared to Mason's original model. For example, the KLM model avoids the unphysical negative capacitance present in Mason's approach and uses a transformer to represent electromechanical coupling.

The KLM model parameters are defined as:

$$\begin{aligned} C_0 &= \frac{lw}{\beta_{33}^S t}, \quad v = v_{Dt} = \sqrt{\frac{c_{33}^D}{\rho}}, \quad Z_0 = \frac{\rho l w}{v_{Dt}}, \\ M &= \frac{h_{33}}{\omega Z_0}, \quad \phi = \frac{1}{2M} \csc\left(\frac{t\omega}{2v_{Dt}}\right), \quad X_1 = \frac{Z_0 M^2}{\sin(t\omega / v_{Dt})} \end{aligned} \tag{1.8}$$

Here, ρ denotes density, ω is angular frequency, β_{33}^S is the dielectric impermeability, c_{33}^D is elastic stiffness, and h_{33} is the piezoelectric constant. The transducer's physical dimensions—length l, width w, and thickness t—are also depicted in Fig. 1.4. The electrical port, with clamped capacitance C_0, is con-

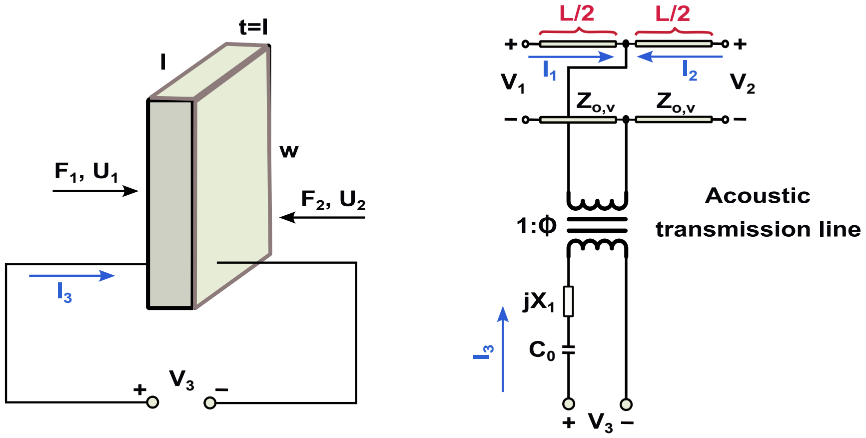


Figure 1.4: KLM model of a PZT transducer in thickness mode [28].

nected to the acoustic domain via a transformer. The acoustic domain is modeled as a transmission line with characteristic impedance Z_0 and velocity v, capturing the propagation delay of acoustic waves.

For initial approximations or simplified analysis, the Butterworth–Van Dyke (BVD) model (Figure 1.5) is often used. It models the resonant behavior of PZTs as an RLC bandpass circuit. The capacitance C_0 represents the static (clamped) capacitance of the transducer. The mechanical response is represented by R_1, L_1, and C_1, with R_1 accounting for losses, and L_1, C_1 modeling resonance.

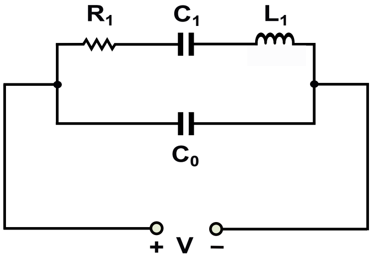


Figure 1.5: BVD equivalent circuit of a PZT [30].

The frequency-dependent admittance of the BVD circuit is given by:

$$Y(\omega) = \frac{j\omega^2 C_1 R_1 C_0 - \omega C_0(\omega^2 L_1 C_1 - 1) + \omega C_1 R_1 \omega C_1 + j(\omega^2 L_1 C_1 - 1)}{(R_1^2 + (\omega L_1 - \frac{1}{\omega C_1})^2) C_0} \tag{1.9}$$

The resonance frequencies occur where the magnitude of $Y(\omega)$ reaches extrema. At **series resonance** (ω_s), the imaginary part of the denominator becomes zero, giving:

$$\omega_s = \frac{1}{\sqrt{L_1 C_1}}, \qquad L_1 = \frac{1}{\omega_s^2 C_1} \tag{1.10}$$

At $\omega = \omega_s$, admittance simplifies to:

$$Y(\omega_s) = \frac{1}{R_1} + j\omega_s C_0 \tag{1.11}$$

From this, R_1 and C_0 can be determined using the real and imaginary parts respectively.

For **parallel resonance** ($\omega = \omega_p$), admittance is minimized, and we find:

$$C_1 = C_0 \left(\omega_p^2 L_1 C_1 - 1\right) = C_0 \left(\frac{\omega_p^2}{\omega_s^2} - 1\right) \tag{1.12}$$

It's important to note that these equivalent circuit parameters are frequency-dependent and only valid near resonance. Thus, the BVD model is most effective for initial design iterations or as part of an iterative optimization process.

1.2.2 Piezoelectric Micromachined Ultrasonic Transducer

Ultrasound signal generation can be achieved through several physical effects, with the piezoelectric effect being the most common in PMUTs and bulk PZT transducers [34]. This effect describes the bidirectional relationship between mechanical deformation and electric field in certain materials [35].

The behavior of piezoelectric materials is governed by the canonical equations:

$$S = [s^E]T + [d^T]E, \quad D = [d]T + [\varepsilon^T]E, \tag{1.13}$$

where S and T denote strain and stress tensors, E and D the electric field and displacement, and $[s^E], [\varepsilon^T], [d]$ represent compliance, permittivity, and piezoelectric coefficients.

PMUTs typically operate in the d_{31} or d_{33} modes, generating ultrasonic waves via membrane flexural motion. The electromechanical coupling coefficient (EMCC) is used to assess transducer efficiency [36, 37].

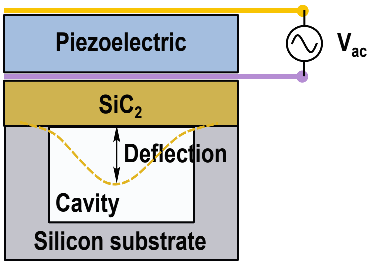


Figure 1.6: Cross-section of a PMUT structure.

A typical PMUT consists of a piezoelectric layer sandwiched between electrodes and supported by a SiO_2 layer. A cavity beneath the membrane enables resonance.

The fundamental resonant frequency of a circular clamped membrane is:

$$f_r = \frac{\alpha^2}{2\pi r^2}\sqrt{\frac{D_E}{\rho h}}, \tag{1.14}$$

with r being the radius, D_E the flexural rigidity, ρ the density, and h the membrane thickness [38].

Recent advancements in PMUT design have introduced unconventional membrane geometries aimed at enhancing device performance. Among these, piston-like membranes incorporate sealed peripheral openings that form a tent-shaped structure, allowing greater displacement and enabling operation in liquid environments. Island-shaped membranes improve mechanical resilience and flexibility through the use of a central island and a polyimide ring, resulting in enhanced diaphragm motion. I-shaped diaphragms are designed to offer improved sensitivity and higher resonant frequencies compared to traditional square or circular configurations of equivalent area. The bimorph structure, featuring two active piezoelectric layers with opposing electric fields, significantly increases the bending moment, leading to larger displacements, higher sensitivity, and better energy efficiency. Lastly, pre-concaved membranes improve piezoelectric coupling and deliver low impedance, high quality factors, and large displacements, making them suitable for high-frequency air-coupled applications, particularly in medical ultrasound imaging [35–38].

1.2.3 Capacitive Micromachined Ultrasonic Transducer

CMUT technology was introduced to overcome several limitations associated with traditional PZTs. Compared to PZT-based devices, CMUTs offer notable benefits such as broader operational bandwidth, simpler fabrication of large-scale arrays, lower sensitivity to temperature fluctuations, and improved integration with CMOS electronics—either through through-wafer interconnects [39–41] or monolithic CMUT-CMOS integration techniques [42, 43]. Although the concept of capacitive acoustic transducers dates back to the 1940s [29], significant progress in CMUT fabrication using micromachining techniques began in the late 20th century [44–46].

1.2.3.1 CMUT Operating Principle

The fundamental working mechanism of a CMUT is conceptually straightforward and derives from its physical structure, illustrated in Fig. 1.7. A CMUT cell consists of a movable membrane suspended above a vacuum gap (cavity), forming a capacitor. The top electrode is typically a metal layer on the membrane, while the bottom electrode resides in the silicon substrate. An insulating layer prevents electrical shorting.

When a DC bias voltage is applied, the membrane is electrostatically attracted toward the bottom electrode, creating a static force counteracted by the membrane's mechanical stiffness. Superimposing a smaller AC signal causes the membrane to oscillate, thus emitting ultrasonic waves. The vacuum gap minimizes mechanical loading on the underside of the membrane [8].

Conversely, in receiving mode, incoming acoustic pressure displaces the membrane, resulting in a capacitance change under constant DC bias. This variation produces a current signal that can be amplified and measured. The output current amplitude depends on the bias voltage, CMUT capacitance, and input frequency [47].

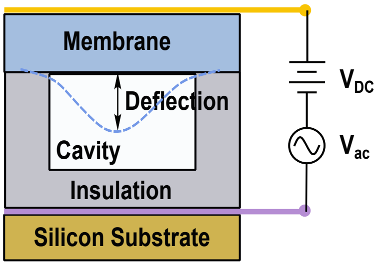


Figure 1.7: Cross-sectional structure of a CMUT device [11].

1.2.3.2 CMUT Modeling and Equivalent Circuits

Early CMUT models were developed from fundamental electromechanical principles, inspired by Mason's theory on transducers [29]. These models treated the CMUT as a two-port network—one electrical and one acoustic—linked via a transformer representing electromechanical coupling [8, 46]. Figure 1.8 presents this equivalent circuit.

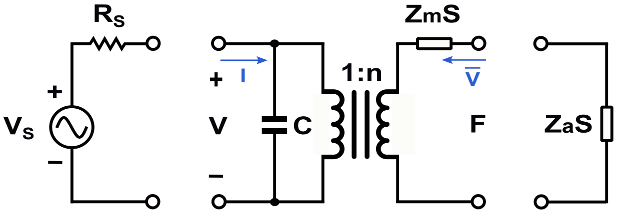


Figure 1.8: Electromechanical equivalent circuit model of a CMUT [8].

In this model, the total current I includes two components: an electrical part from the voltage source, and a mechanical part associated with membrane motion. The transformer ratio n links mechanical and electrical domains. The membrane's mechanical impedance is represented by Z_m, and the acoustic impedance of the surrounding medium is denoted Z_a. This small-signal model is valid for both transmit and receive modes as long as the membrane does not reach its collapse point and spring softening remains negligible.

For most immersion applications, the acoustic impedance Z_a is significantly larger than Z_m, allowing further simplification of the model into a parallel RC circuit, shown in Fig. 1.9.

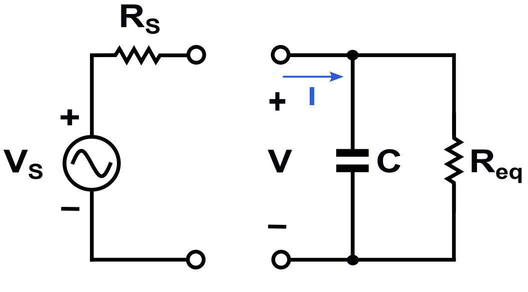


Figure 1.9: Simplified RC-parallel equivalent circuit of a CMUT [8].

In this simplified form, the equivalent resistance R_{eq} and capacitance C are defined as:

$$R_{eq} = \frac{Z_a \left(\varepsilon_0 l_t + \varepsilon l_a\right)^4 V_{DC}^2}{4\varepsilon_0^2 \varepsilon^4 S}, \tag{1.15}$$

$$C = \frac{\varepsilon_0 \varepsilon S}{\varepsilon_0 l_t + \varepsilon l_a}, \tag{1.16}$$

where:

- l_t: membrane thickness,
- l_a: electrode-to-membrane gap,
- ε: relative permittivity of the membrane material,
- V_{DC}: applied bias voltage,
- ε_0: vacuum permittivity,
- S: membrane area.

As simulation tools advanced, modern CMUT models have become more comprehensive, incorporating parasitic elements and nonlinear effects using finite element methods (FEM) [48, 49].

1.3 Transducer Driver Circuit

Transducer driver circuits are generally categorized into two main types: continuous-wave (CW) and pulsed-wave (PW) systems. CW ultrasound systems are typically used in specific medical contexts, such as continuous-wave Doppler imaging and certain therapeutic applications. Although several commercial integrated circuits (ICs) for CW systems are available [50, 51], the majority of microelectronics research focuses on pulsed-wave systems due to their broader applicability. As a result, this thesis emphasizes transducer driver circuits tailored for pulsed-wave applications, commonly referred to as *pulsers*.

Pulsers generate brief, high-voltage electrical signals to excite ultrasound transducers. To achieve deeper tissue penetration, these voltage pulses often need to reach amplitudes ranging from several tens of volts up to over 100 V. This high-voltage requirement typically necessitates the use of specialized high-voltage transistors. However, such components increase both the cost and silicon area, presenting challenges in space-constrained scenarios such as intravascular ultrasound imaging.

Among the front-end electronics in ultrasound systems, the pulser is usually the most power-intensive component. Whether for implantable or portable/wearable devices, optimizing the energy efficiency of the pulser is essential. The energy efficiency is closely linked to the shape of the generated pulse, which affects the spectral characteristics of the transmitted ultrasound, the efficiency of acoustic energy conversion, and the dynamic power consumption within the pulser [52].

Ideally, the pulse's energy spectrum should align with the effective bandwidth of the transducer's transfer function to ensure optimal performance. While conventional square waveforms are widely used, alternative shapes—such as continuous sine waves or Gaussian-modulated sinusoids—can offer advantages in specific contexts.

This section explores the two primary categories of pulser circuits: arbitrary waveform pulsers and square-wave pulsers.

1.3.1 Arbitrary Waveform Pulsers

Linear amplifiers are designed to faithfully reproduce the shape of an input waveform at a higher power level. Unlike square-wave pulsers, linear amplifiers can handle a wide range of input waveforms and are primarily used to generate arbitrary excitation signals for ultrasound transducers [53–56]. While they generally exhibit lower power efficiency and greater complexity than square-wave pulsers [57], their ability to produce complex waveforms with minimal harmonic distortion makes them particularly attractive for high-performance imaging systems [56].

A key benefit of low second-order harmonic distortion (HD_2) is its relevance to tissue harmonic imaging (THI), a technique that emerged serendipitously in 1997. THI offers significant advantages, including reduced reverberation noise, enhanced boundary clarity, and improved contrast resolution [58]. To support THI effectively, transmitters typically must achieve HD_2 levels below –40 dB [55]. Designing a linear amplifier that simultaneously provides large voltage swings, low HD_2, and wide bandwidth is particularly challenging, especially when using high-voltage transistors, which tend to have slower switching speeds [54]. As such, while discrete implementations on printed circuit boards (PCBs) are relatively straightforward [59, 60], integrating these amplifiers into ICs remains difficult.

Most linear amplifiers used in medical ultrasound systems are implemented in class AB or class B topologies, often using a multi-stage design. A common architecture separates the low- and high-voltage stages. The low-voltage gain stage typically employs standard MOSFETs and may take the form of a two-stage Miller operational amplifier [55], a transconductance amplifier [53], or a current amplifier [56]. For example, the transconductance amplifier described in [53] uses a bipolar input stage for high transconductance-to-bias current ratio (g_m/I_b), along with cascoded MOSFETs to improve output impedance and drive capability. It achieves a transconductance of 60 mS with a quiescent current of 4.5 mA.

While the amplifiers in [53, 55] use voltage feedback, the design in [56] employs current feedback, allowing for high bandwidth operation across various gain levels. This technique bypasses the gain-bandwidth limitations inherent in voltage feedback configurations. As a result, the current-feedback amplifier achieves a bandwidth exceeding 20 MHz and a slew rate of 12 V/ns, with distortion levels as low as –43 dBc at a power consumption of just 20 mW.

The high-voltage gain stage's primary goal is to maximize output signal swing. An example of such a stage is the transimpedance amplifier depicted in Fig. 1.10, which uses high-voltage DMOS transistors (except for the input, which uses thin-oxide transistors to minimize input impedance). The amplifier is designed with a balanced architecture to support both positive and negative current signals at the output node. To ensure proper signal delivery to the transducer, an output buffer is often added. This buffer can be implemented in class B [53] or class AB configurations [54–56].

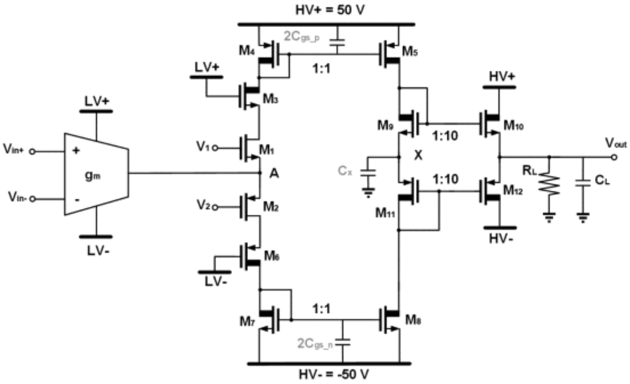


Figure 1.10: Transimpedance amplifier with class B output buffer [53].

An alternative linear amplifier design is shown in Fig. 1.11, featuring a differential architecture that inherently suppresses even-order harmonics. This results in improved HD_2 performance (up to –56 dBc) and a higher output swing of 180 V_{pp}. However, it requires an off-chip transformer to convert the differential output to a single-ended signal, which increases the bulk and complexity of the system.

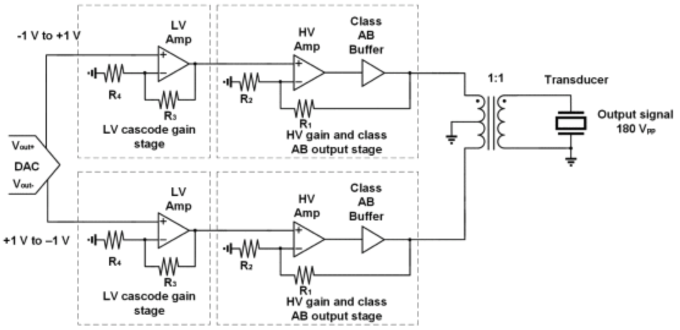


Figure 1.11: Differential linear amplifier architecture [55].

1.3.2 Square Wave Pulsers

1.3.2.1 Level Shifter

To generate large-amplitude square wave signals from logic-level control inputs, one of the most common and intuitive techniques is the use of a level shifter, often combined with an output stage—typically configured in Class D for enhanced power efficiency. This approach is prominently featured in a variety of prior works [27, 39–41, 61, 63–70].

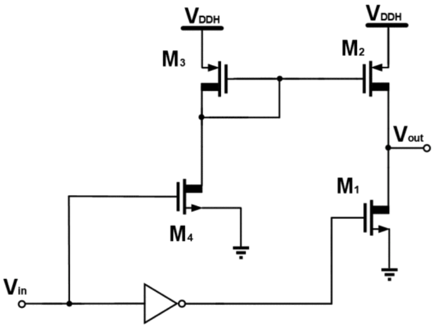


Figure 1.12: Conventional high-voltage level shifter using minimal transistors [27, 61].

A minimal transistor-level high-voltage level shifter implementation is illustrated in Fig. 1.12. This design is compact and thus suitable for space-limited applications. However, it suffers from imperfect gate control—especially for the PMOS output (M_2) and transistor M_3—leading to incomplete turn-off during a logic high-to-low input transition. Consequently, the output may exhibit a non-zero DC offset rather than returning to 0 V [71].

To address this limitation, the improved architecture shown in Fig. 1.13 was proposed in [62] and has become widely adopted in ultrasound ICs [39–41, 64, 65]. This configuration employs two cross-coupled branches. Each branch consists of a high-voltage NMOS in a common-source setup (M_1, M_2), a diode-connected PMOS (M_4, M_5), and a pull-up PMOS (M_3, M_6). These PMOS devices ensure full turn-off capability of the output transistors. The gate of transistor M_8 toggles between $V_{DDH} - V_{DD}$ and V_{DDH} to improve switching efficiency. The M_1-M_4 and M_2-M_5 branches form what is known as a voltage mirror [62].

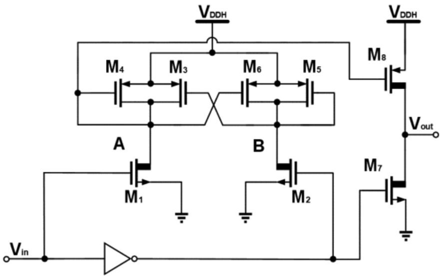


Figure 1.13: Enhanced level shifter with output buffer for improved switching [62].

Despite its effectiveness, this design comes with challenges. First, it relies on high-voltage transistors that are expensive, occupy larger die areas, and exhibit higher parasitics and on-resistance. To address this, alternatives such as those in [66, 72] utilize stacked standard CMOS transistors (1.8 V or 5 V) to emulate high-voltage operation. These designs replace the traditional two-transistor output stage with a multi-transistor stack, often integrated with a dynamic gate biasing technique adapted from [73] for smooth push-pull behavior.

The use of stacked low-voltage transistors introduces stress on the reverse diodes between n-well and p-substrate regions, which can compromise long-term reliability. Therefore, careful design across process corners and operating voltages is crucial. One such implementation occupies just 0.022 mm^2 but delivers a limited output swing of 9.8–12.8 V—significantly lower than the tens of volts achievable with true high-voltage devices [66].

Another key drawback of the architecture in Fig. 1.13 is its constant static power consumption. Voltage mirror branches dissipate power irrespective of the input state. Power-optimized variants, such as the pulse-triggered level shifter in [75], minimize energy usage by confining power consumption to short trigger periods. Originally based on a level-triggered design from [76], this pulse-driven variant offers reduced average power and improved propagation delay—ideal for portable medical applications.

Moreover, the unipolar nature of the output waveforms limits applicability in ultrasound systems that require bipolar pulses. To achieve bipolar return-to-zero operation, several level shifters and complementary output stages can be arranged in tandem, as demonstrated in [68, 77–81]. An illustrative design from [68] is shown in Fig. 1.14, where M_2 acts as a floating gate driver for M_1, enabling transitions between high (V_{DDH}) and zero outputs using parasitic capacitances.

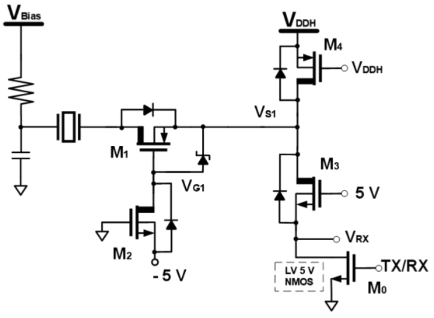


Figure 1.14: High-voltage positive output stage with embedded T/R switch for bipolar operation [68].

To summarize, the use of level shifters with output stages is a prevailing strategy for driving ultrasound transducers with square waveforms. Continuous innovation has improved their area efficiency, power performance, and output flexibility. Nevertheless, a major limitation remains: substantial capacitive power loss (fCV^2) at the transducer load, which is particularly problematic in capacitive systems. The subsequent section discusses pulser topologies designed to mitigate this inefficiency.

1.3.2.2 Multi-Level Pulse-Shaping

Due to the considerably higher capacitive load presented by PMUTs and CMUTs, efficient pulser designs must address the significant power loss caused by conventional fC_LV^2 dissipation. One promising method is stepwise charging, also known as adiabatic switching [82, 83], which has been effectively implemented in multiple designs [21, 84–88].

The principle of stepwise charging involves reducing the average voltage drop $\bar{V}$ across the load capacitance C_L, assuming constant switching frequency, load capacitance, and voltage swing [82]. By doing so, energy dissipation is minimized.

Fig. 1.15(a) illustrates the concept, where C_L is charged using N discrete voltage levels (V_1 to V_N) applied sequentially: connect V_1, disconnect V_1, connect V_2, and so forth, until V_N is reached. Discharging occurs in reverse order from V_{N-1} to V_1, followed by grounding the output. The energy dissipated in each step is:

$$E_{\text{step}} = Q\bar{V} = C_L V_N \cdot \frac{V_N}{2N} = \frac{1}{2N} C_L V_N^2. \tag{1.17}$$

For N steps, the total energy dissipation becomes:

$$E_{N\ \text{steps}} = N \cdot E_{\text{step}} = \frac{1}{2} C_L V_N^2 = E_{\text{conventional}}, \tag{1.18}$$

which is equal to the conventional single-step energy. However, since charging and discharging both benefit from this technique, the total power loss is halved and effectively reduced by a factor of N, due to the N-times lower voltage drop across each switch.

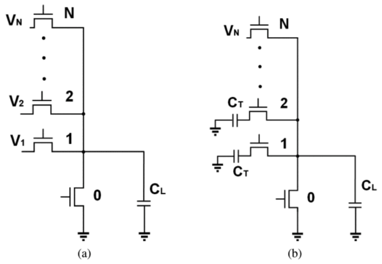


Figure 1.15: (a) Stepwise charging using multiple supply voltages [83]. (b) Alternative with large tank capacitors C_T [83].

One of the early implementations is shown in Fig. 1.16, employing a three-level pulser with a DC-DC converter generating 0 V, 15 V, and 30 V ($N = 2$). High-voltage transistors manage the voltage transitions. Though a 50% theoretical improvement is expected, only a 38% reduction was measured, largely due to parasitic losses in the large, capacitive HV switches. This self-loading effect reduces the benefit of additional voltage steps, making three-level pulsing the most power-efficient configuration in this case.

Despite these gains, this design relies on off-chip capacitors and achieves only moderate power savings. More recent work addresses these limitations [21, 86, 88]. In [88], a 7-level ultrasound pulser was developed using a modular supply multiplying strategy. Each module resembles a switched-capacitor cell operating in either a charge or transfer mode. When cascaded with proper timing, the modules generate a high-voltage, multi-level waveform, where each step equals the supply voltage (5 V).

Compared to the design in Fig. 1.16, this modular architecture can support more output levels before the self-loading penalty dominates. Two prototypes were fabricated for 55 pF and 1 nF loads. The 55 pF prototype included on-chip 3 nF MIM capacitors and achieved a 58% power reduction relative to fC_LV^2. The 1 nF version used external 60 nF capacitors, attaining a peak power reduction of 75.4%—one of the best reported.

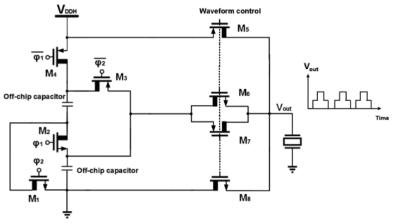


Figure 1.16: Three-level pulser design and output waveform [87].

Another novel approach was proposed in [21, 86], targeting bimorph PMUTs. As shown in Fig. 1.17, the PMUT is modeled as a capacitor with top (outer) and bottom (inner) electrodes. Initially, the top plate is charged to V_{DDH} and the bottom is grounded, causing membrane deformation. During the redistribution phase, the supply and ground are disconnected, and the plates are shorted together, returning the membrane to its flat state. With negligible leakage and equal electrode area, the final potential on both plates becomes $V_{\mathrm{DDH}}/2$.

This means subsequent charging/discharging involves only half the voltage swing, potentially cutting power usage. Measured reductions of 32.8% and 42.6% relative to fC_LV^2 were achieved in two variants of this design.

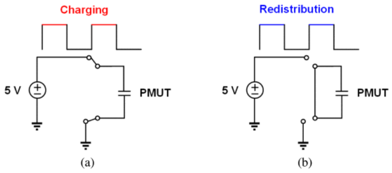


Figure 1.17: Operation of a PMUT-specific pulser: (a) Charging phase, (b) Redistribution phase [21, 86].

1.4 Ultrasound Receiver Circuit

The performance of an ultrasound system is heavily influenced by the design of its receiver circuit, which often serves as a critical bottleneck in the overall signal processing chain. Typically, a complete ultrasound receiver comprises three primary components:

- **Low-Noise Amplifier (LNA)**: Responsible for amplifying weak echo signals, the LNA prepares the input for subsequent beamforming and analog-to-digital conversion stages.
- **Time Gain Compensation (TGC) Circuit**: This block manages a wide dynamic range of input signals to maintain consistent signal levels across varying depths.
- **Transmit/Receive (TX/RX) Switch**: This circuit safeguards the sensitive, low-voltage receiver components from potentially damaging high-voltage transmit pulses.

The LNA and TGC may be implemented as separate entities or integrated into a single module. Designers must navigate several trade-offs when developing receiver circuits, including bandwidth, linearity, noise performance, power consumption, and silicon area. Achieving both ultra-low noise and a wide dynamic range remains a significant challenge in ultrasound receiver design [25].

This section offers a comprehensive analysis of the ultrasound receiver circuitry, organized around its three primary functional blocks. First, it explores low-noise amplification, discussing various circuit topologies that achieve minimal signal distortion and noise. Next, the concept of TGC is introduced, along with different circuit-level implementations designed to manage the wide dynamic range of input signals. Finally, the design and operation of TX/RX switches are reviewed, focusing on protecting sensitive receiver components from high-voltage transmit pulses while ensuring minimal signal loss during reception. The section concludes with a discussion on figure-of-merit (FoM) metrics used to evaluate receiver performance.

1.4.1 Low-Noise Amplifier (LNA)

In ultrasound systems, the LNA plays a crucial role in determining the overall signal integrity and system performance. Various LNA architectures have been developed to support different transducer types and application requirements. Common LNA implementations include charge amplifiers [90], transconductance amplifiers [91], and current amplifiers [14, 92], with some designs being adapted from transimpedance amplifier (TIA) architectures, such as the one reported in [93].

For example, the charge amplifier presented in [90] employs a floating node charge adaptation technique, achieving high signal-to-noise ratio (SNR) and low power consumption, particularly for CMUTs. However, its limited bandwidth—only in the kilohertz range—renders it unsuitable for typical MHz-range medical ultrasound imaging.

In contrast, current and transconductance amplifiers are more architecture-specific. In [92], a current amplifier was used to maintain compatibility with a current-mode beamforming back-end. Similarly, the design in [14] utilized a current output to accommodate the constraints of an intravascular ultrasound (IVUS) probe, which was limited to a single transmission line.

Given that ultrasound transducers inherently generate current signals in response to acoustic waves, transimpedance amplifiers (TIAs), which convert current to voltage, are often the preferred LNA topology in ultrasound front-ends. TIAs are also widely used in other biomedical systems such as biosensors and photoplethysmography-based blood pressure monitors [94, 95].

Figure 1.18a illustrates the basic closed-loop TIA architecture, which employs shunt-shunt negative feedback. This feedback configuration senses the output voltage and feeds a proportional current back to the input, thereby lowering both the input and output impedances for improved performance. A practical single-ended implementation, shown in Figure 1.18b, consists of a common-source amplifier, a source follower stage, and a resistive feedback path.

The closed-loop transimpedance gain, R_T, and the input-referred current noise are given by:

$$R_T = \frac{g_{m1}R_D}{1 + g_{m1}R_D} R_F \tag{1.19}$$

$$\overline{I_{n,\text{in}}^2} = 4kTR_F + \frac{4kTR_F^2}{g_{m1}^2 R_D^2}(\gamma g_{m1} + \frac{1}{g_{m1}^2 R_D} + \gamma g_{m2}) \tag{1.20}$$

where k is Boltzmann's constant, T is absolute temperature, and γ is the excess noise factor.

The topology shown in Figure 1.18b is widely adopted due to its simplicity and compactness. Variations have been proposed to improve performance and reduce area. For instance, several designs [39–41, 43, 63] replace the resistive load R_D with an active load, while [43, 72] substitute the feedback resistor R_F with a pseudo-MOS device to save chip area. The work in [72] also introduces a resistor network to apply forward body biasing to transistor M_1, which lowers threshold voltage and supply requirements, leading to reduced power consumption.

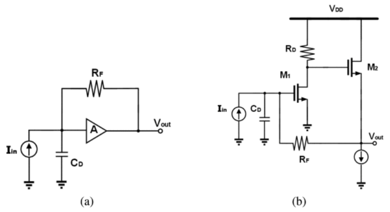


Figure 1.18: Closed-loop TIA employing negative feedback [96] (a) General architecture. (b) Typical single-ended implementation.

Although single-ended TIAs offer advantages in terms of area and power—ideal for probe-based ultrasound systems—they suffer from limitations such as poor power supply rejection and susceptibility to supply-dependent bias variations [96].

To mitigate these drawbacks, differential TIA architectures have been proposed. Differential implementations provide superior common-mode noise suppression, improved power supply rejection, and reduced even-order distortion. A differential-input, single-ended-output TIA was presented in [87], where a two-stage Miller op-amp was followed by a source follower. The design was optimized by carefully sizing transistors to balance bandwidth, noise, and power consumption, ensuring that dominant poles aligned with the desired frequency response.

Another approach is the single-ended input, differential output TIA illustrated in Figure 1.19, based on the design in [97]. This circuit includes a common-gate stage in combination with a common-source amplifier and leverages negative feedback for power efficiency. Additionally, the feedback resistor R_F contributes to noise cancellation at the differential outputs, enhancing overall signal fidelity.

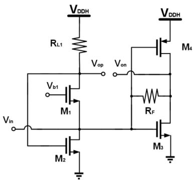
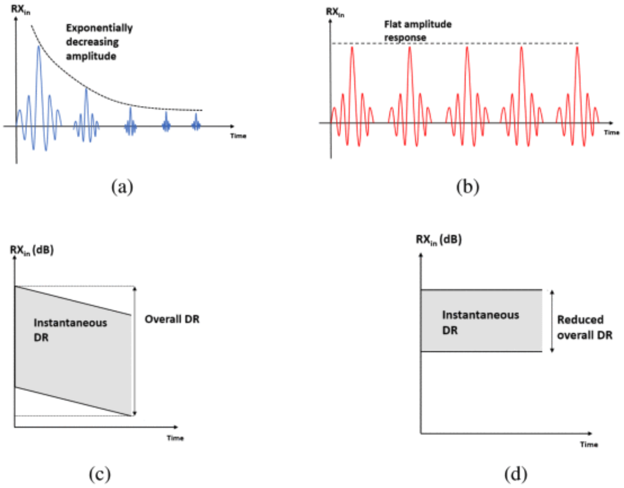


Figure 1.19: Low power, low noise single-ended to differential TIA [97].

1.4.2 LNA with Time-Gain Compensation

For ultrasound receiver systems, employing a single LNA with fixed gain is inadequate when dealing with signals that span a wide dynamic range. Echoes originating from deeper tissues undergo more attenuation and arrive at the receiver with lower amplitudes compared to echoes from tissues that are closer to the transducer. A fixed-gain LNA may lead to signal distortion: strong echoes could cause saturation, while weak echoes may remain under-amplified. In ultrasound imaging, saturation typically results in bright spots, whereas under-amplification can obscure important image features.

To address this issue, LNAs are often coupled with an automatic gain control (AGC) mechanism that adjusts amplification based on signal arrival time. Signals that arrive later—typically from greater depths—are amplified more, while earlier, stronger signals receive less gain. This time-dependent gain adjustment ensures a more uniform signal amplitude across depths and is referred to as TGC in ultrasound systems. Ideally, TGC should also reduce the overall input signal dynamic range (see Fig. 1.20), thereby easing the design constraints of downstream circuitry, particularly ADCs.



(a) (b) (c) (d)

Figure 1.20: Illustration of TGC effect [98]. (a) RX output without TGC. (b) RX output with TGC. (c) Wide dynamic range without TGC. (d) Reduced dynamic range with TGC.

Since ultrasonic waves attenuate exponentially as they propagate through tissue, the gain of the TGC circuit should ideally increase linearly in decibels over time to effectively compensate for this loss. However, implementing such dB-linear gain control in CMOS technology is challenging due to the inherent square-law behavior of MOSFETs. In contrast, bipolar junction transistors (BJTs) are more naturally suited for dB-linear gain control. As a result, CMOS-based TGC circuits often use approximations to achieve this behavior. These implementations typically fall into two main categories: (1) programmable gain amplifiers (PGAs), which provide discrete gain steps, and (2) variable gain amplifiers (VGAs), which allow for continuous gain variation [98].

1.4.2.1 Programmable Gain Amplifier

A widely adopted and relatively straightforward method for implementing TGC in ultrasound systems involves using a digitally programmable feedback network. These feedback networks are typically resistive [99–105] or capacitive [106–108], and are designed to approximate an exponentially increasing gain response through discrete gain steps. A common configuration for such TGC networks is illustrated in Fig. 1.21(a).

To enhance gain control resolution, these discrete steps can be distributed across multiple amplification stages. For instance, the LNA can handle coarse gain adjustments, while a subsequent PGA performs fine gain tuning [106,109]. Typical PGA implementations include inverter-based amplifiers, current-reuse operational transconductance amplifiers (OTAs), and cascoded flipped-voltage followers. Additionally, Kelvin switch configurations have been employed to minimize gain errors caused by switch on-resistance within the feedback path [99, 101, 109].

Among the key advantages of the PGA topology are its ease of digital control and its precise gain definition. The gain steps are determined by the ratios of feedback resistors or capacitors, which are relatively immune to variations in process, voltage, and temperature (PVT) [110]. However, this approach comes with notable limitations. Firstly, achieving a finer approximation of the ideal exponential gain response necessitates the inclusion of additional resistors or capacitors, which significantly increases chip area and reduces scalability. Secondly, the input and output impedance of the PGA can vary across gain settings, complicating the design of subsequent circuit stages. Thirdly, the closed-loop nature of this topology often limits the bandwidth. Lastly, image artifacts can arise due to abrupt transitions between discrete gain levels, impacting ultrasound image quality [98].

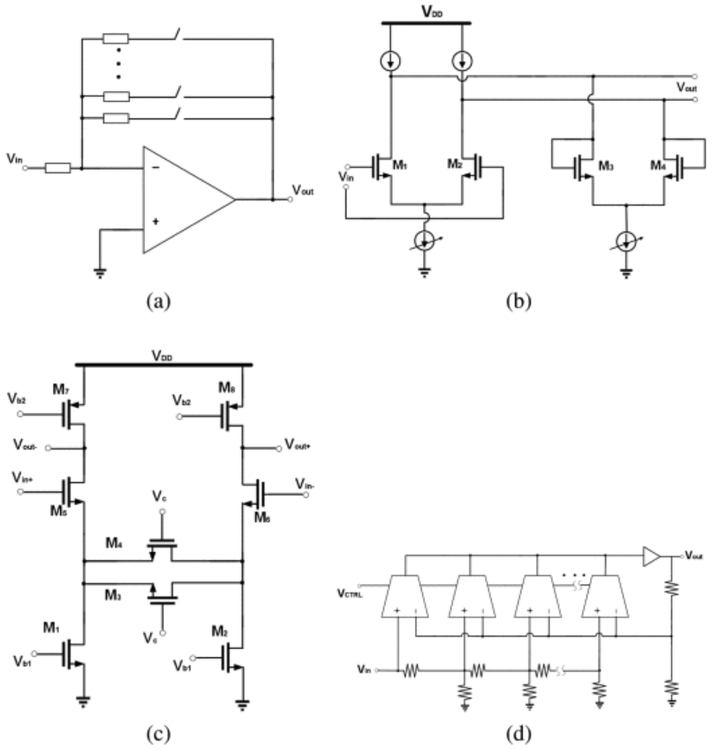


Figure 1.21: Examples of TGC circuit implementations [98]. (a) PGA using resistive or capacitive feedback. (b) VGA with variable transconductance [111]. (c) VGA based on linear signal terms [112]. (d) VGA with interpolated ladder attenuator [113].

1.4.2.2 Variable Gain Amplifier

The inherent limitations of PGAs have motivated the adoption of VGAs in scenarios where smooth, continuous gain variation is critical. Unlike PGAs, VGAs typically offer a gain response that is linear in decibels (dB), controllable via an analog signal such as a bias voltage. Although designing VGAs for ultrasound applications is generally more complex than designing PGAs, communication system VGAs provide a strong theoretical basis for this effort. As a result, this section briefly explores VGAs used in communication circuits to inform the design of ultrasound VGAs.

To realize dB-linear gain characteristics, VGAs can be broadly categorized into two types: (i) those utilizing exponential function approximations, and (ii) those that interpolate between discrete gain levels [98].

1) Exponential Function-Based VGAs:
VGAs in this category exploit the intrinsic nonlinearities of MOSFETs—specifically, their linear and quadratic regions—to approximate exponential functions. Popular approaches include the Padé approximation and the second-order Taylor series expansion.

The Padé approximation for e^{2x} is expressed as:

$$f(x) = e^{2x} \approx \frac{1+x}{1-x} \tag{1.21}$$

which achieves a relative error below 5% within the range $-0.32 \le x \le 0.32$ [114]. Due to this limited linearity range, several VGA stages often need to be cascaded to extend the operating region, which increases power consumption, silicon area, and potentially reduces bandwidth.

Alternatively, the Taylor series expansion is given by:

$$f(x) = e^{x} \approx 1 + x + \frac{1}{2}x^2 \tag{1.22}$$

This provides a slightly improved valid range ($-0.575 \le x \le 0.815$) while maintaining a similar accuracy level [114]. However, realizing these terms in practice requires additional circuit blocks—such as a linear voltage-to-current (V–I) converter and a squaring circuit—which increases design complexity [112].

Due to the constraints of the above approximations, alternative functional models have been proposed [111, 112, 115, 116]. One such example, given by:

$$f(x) = e^{2ax} \approx \frac{k + (1+ax)^2}{k + (1-ax)^2} \tag{1.23}$$

offers a significantly extended dB-linear range when the constant k is set to 0.12 [111]. The circuit realization involves adjusting the bias currents of a differential pair and its diode-connected load in response to a control voltage, achieving a variable transconductance and a nonlinear response aligned with the above expression. An improved VGA design for ultrasound based on this concept has also been proposed [117]. The corresponding implementation is depicted in Fig. 1.21(b).

2) Interpolation-Based VGAs:
This second class of VGAs strikes a compromise between PGAs and exponential approximation-based VGAs. Instead of fixed gain steps, the amplifier interpolates between them to achieve smoother transitions [98, 113, 118]. A representative example, introduced in [113] and illustrated in Fig. 1.21(d),

employs an R–2R resistor ladder for discrete input attenuation. This attenuated signal is then fed into multiple amplifier input stages whose bias currents are gradually varied using current steering techniques. This strategy allows for seamless interpolation between the discrete gain levels set by the resistor ladder.

More recently, this concept has evolved with the introduction of a current-interpolated transimpedance amplifier (TIA) that uses a capacitive ladder instead of resistors to minimize additional thermal noise [98]. However, a key drawback of this interpolation approach is the significant chip area required to accommodate the passive feedback network, particularly the resistor or capacitor arrays [117].

1.4.2.3 Transmit/Receive (TX/RX) Switch

The TX/RX switch is a critical component in ultrasound systems, tasked with safeguarding the sensitive receiver front-end from the high-voltage pulses generated during transmission. Several TX/RX switch implementations with varying degrees of complexity have been proposed, each aiming to balance protection, signal integrity, and integration ease.

The most straightforward TX/RX switch design in integrated ultrasound electronics employs a single high-voltage NMOS transistor [38,66]. With careful device sizing, both the on-resistance and parasitic capacitance of this MOSFET can be managed within acceptable limits. However, due to the inherent body diodes present in high-voltage MOSFETs, a single device is inadequate when the TX waveform includes both positive and negative voltages. To ensure bidirectional signal blocking and enhanced isolation, two high-voltage transistors are typically connected in a back-to-back configuration, as illustrated in Fig. 1.22.

The effectiveness of a TX/RX switch is mainly evaluated based on two performance metrics: (i) high isolation to protect the receiver and prevent TX leakage, and (ii) low on-resistance to preserve SNR and enhance power efficiency. To address these requirements, a variety of sophisticated TX/RX switch topologies have been developed, which can be broadly classified into the following four categories:

- **Zener Diode Biasing:** This method utilizes Zener diodes to establish bias voltages across the gates of the switching transistors, facilitating safe operation under high-voltage conditions [119,120].

- **Floating Latch Circuits:** Floating latches provide control logic that can float with the high-voltage signal, thus enabling precise gate drive

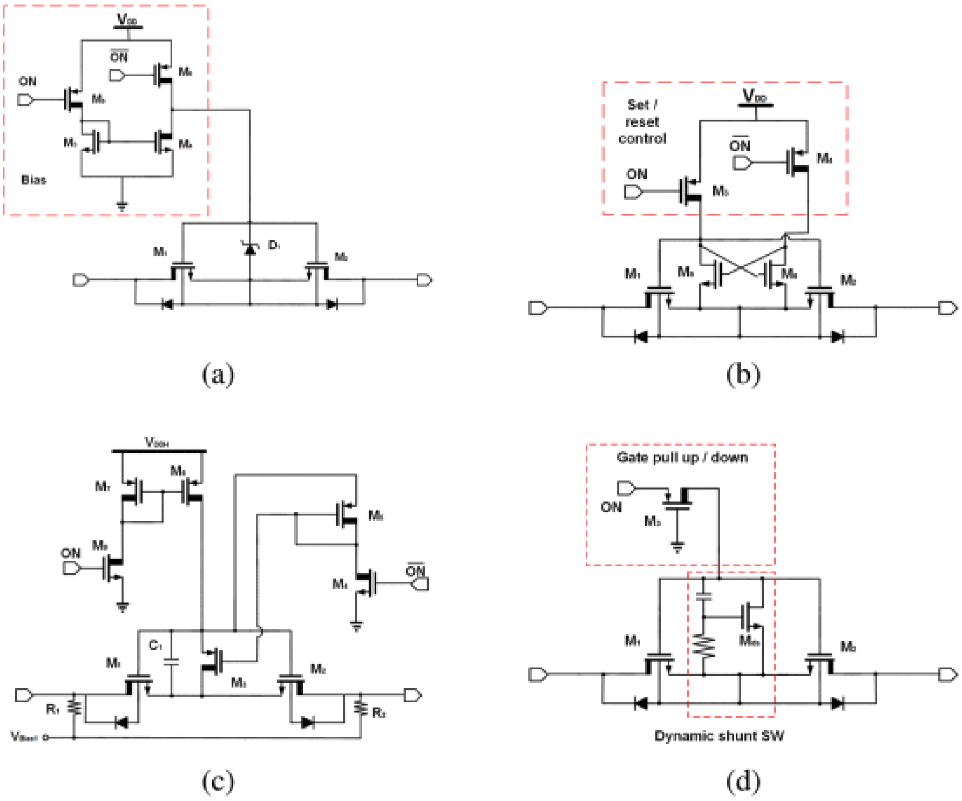


Figure 1.22: Various TX/RX switch architectures [127]. (a) Zener diode bias [119, 120], (b) Floating latch [121, 122], (c) Level shifter [123], and (d) Dynamic gate-source shunt [127].

control even during voltage transients [121, 122].

- **Level Shifter-Based Designs:** These circuits translate low-voltage control signals to high-voltage domains to properly drive the gates of high-voltage transistors, ensuring safe and effective switching [123–126].
- **Dynamic Gate-Source Shunt:** In this technique, the gate-source voltage is dynamically shunted to regulate transistor conduction and suppress leakage currents, providing fast switching and robust isolation [127].

1.5 Beamformer

The beamformer's core purpose in an ultrasound system is to control the spatial characteristics of the acoustic field, effectively shaping the transmitted or received beam to enhance directionality and focus [128]. This is accomplished by precisely manipulating the phase and amplitude across multiple transducer elements, thereby tailoring the pressure distribution within the target region.

On the transmit (TX) side, the beamformer coordinates the activation of multiple pulsers such that the emitted ultrasound waves constructively interfere along a desired direction or converge at a specific focal point. This directional steering or focusing of the ultrasound beam improves energy delivery and resolution at the region of interest.

Conversely, on the receive (RX) side, the beamformer processes incoming echo signals in a complementary manner. It selectively amplifies and combines echoes originating from a targeted direction or depth, while attenuating signals from undesired locations. This spatial filtering enhances image clarity by emphasizing relevant reflections and suppressing noise and clutter.

Fundamentally, beamforming operates on the principle of constructive and destructive interference of wavefronts to manipulate the beam's shape and direction. By introducing precise timing delays or phase shifts across transducer channels, the system can dynamically adjust the effective aperture and focal point of the ultrasound beam.

This section begins with an overview of beamforming theory to establish a foundation for understanding its operation. Following that, a detailed discussion of both analog and digital beamforming architectures in ultrasound IC design is presented.

1.5.1 Beamforming Overview

While the mathematical derivation of beamforming can be quite intricate (refer to [129] for a comprehensive treatment), this section offers a simplified and intuitive explanation to build foundational understanding.

Consider a phased array consisting of multiple ultrasound transducer elements, each independently addressable for transmission and reception. In the transmit (TX) mode, if all elements are excited simultaneously with identical electrical pulses, each acts as a point source emitting spherical wavefronts. These wavefronts constructively interfere and propagate in a direction normal to the array surface, producing a non-steered beam [Fig. 1.23(a)].

However, by introducing relative time delays to the drive signals of individual elements, the transmitted ultrasound beam can be electronically steered to a desired angle [Fig. 1.23(b)]. Furthermore, more sophisticated delay profiles allow for beam focusing at a particular depth in addition to steering [Fig. 1.23(c)]. Another technique known as *apodization* involves assigning amplitude weights to the excitation pulses of each element, which helps reduce sidelobes and improve image quality [Fig. 1.23(d)] [129].

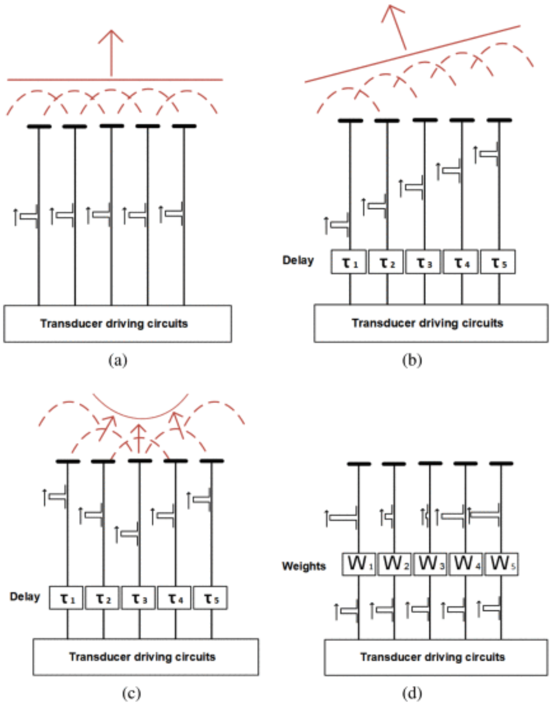
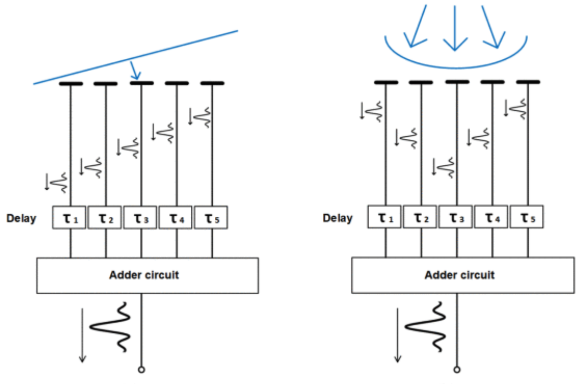


Figure 1.23: Transmit beamforming concept [129]. (a) No beamforming. (b) Beam steering. (c) Beam focusing. (d) Apodization.

The same concept of introducing time delays can be applied during the receive (RX) phase. By applying appropriate delays to the received echo signals before summing them, the signals are time-aligned to reinforce those from a specific direction or focal point. This technique makes the array behave as a large aperture transducer aligned orthogonally to the incoming wave [129]. RX beamforming is visualized in Fig. 1.24 for both angled and curved wavefronts.

Ultrasound beamforming circuits are typically categorized as either analog or digital. In both architectures, two fundamental building blocks are essential: the variable delay cell and the signal summation unit.

In analog beamformers, delays can be implemented using cascaded analog delay elements or analog memory cells [130]. Signal summation is often per-



(a) (b)

Figure 1.24: Receive beamforming concept [129]. (a) Delays for angled wavefronts. (b) Delays for curved wavefronts.

formed using operational amplifiers configured as summers. A major advantage of analog beamformers is that they require only a single high-resolution, high-speed ADC following the summation stage, leading to lower power consumption and smaller chip area (see Fig. 1.25). However, challenges such as mismatches between analog channels limit their accuracy and performance [25].

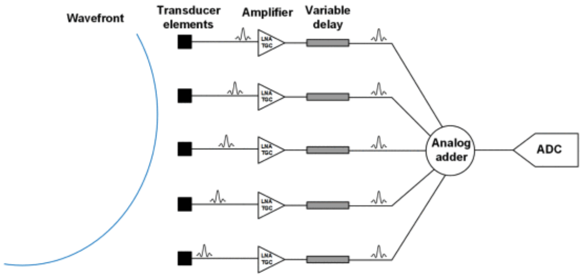


Figure 1.25: Analog beamformer [25].

In contrast, digital beamformers digitize each channel output individually using an ADC. Beamforming operations, including delay and summation, are then performed entirely in the digital domain using FIFO buffers and adders. Although this architecture consumes more power and silicon area due to the large number of ADCs required, it offers superior robustness, flexibility, and immunity to analog noise and mismatches (illustrated in Fig. 1.26).

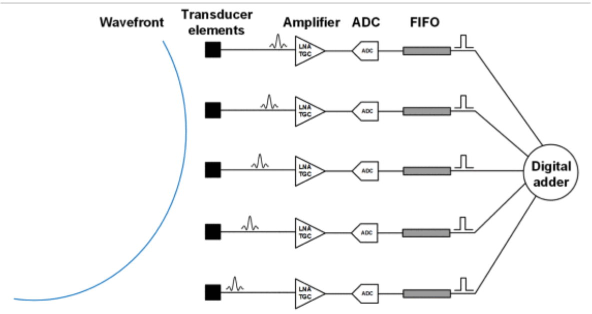


Figure 1.26: Digital beamformer.

1.5.2 Analog Beamformer

This section focuses on one of the most critical components of analog beamformers: the delay element, particularly within RX beamforming systems. According to the current state of research, all existing TX ultrasound beamformers are realized using digital architectures and will be discussed separately.

Analog RX beamformers utilize delay elements, which can be broadly categorized into two main types, as illustrated in Fig. 1.27: (a) cascaded delay cells and (b) analog memory cells [130].

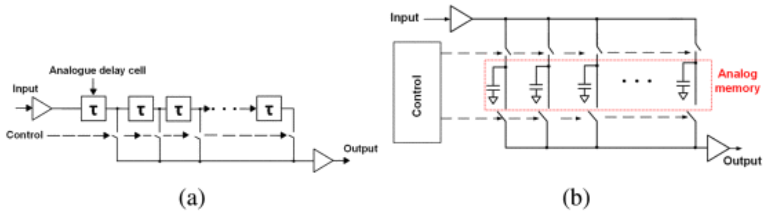


Figure 1.27: Analog delay elements [130]: (a) Cascaded delay cell. (b) Analog memory cell.

In the cascaded delay cell architecture, the input signal propagates through a sequence of delay stages (or taps), and the delayed output is retrieved from a tap selected based on an external control signal. The total delay imparted is proportional to the number of taps traversed [132, 134].

Various implementations of cascaded delay cells exist, such as:

- LC delay lines [133, 134],
- First-order fully differential RC all-pass filters [135],

- Log-domain BiCMOS all-pass filters [136],
- Current mirror all-pass filters [92].

An example of a current mirror all-pass filter used for delay is shown in Fig. 1.28. This circuit approximates an ideal delay element by cascading two biquad current mirrors to form a broadband all-pass filter. Its transfer function is given in Equation (1.24), which corresponds to a second-order low-pass filter. This configuration helps achieve a flatter amplitude response across a broader frequency range, thereby extending bandwidth [92].

$$H(s) = \frac{I_{\text{out}}}{I_{\text{in}}} = e^{-sT_d} \approx \frac{1 - sT_d}{1 + sT_d} \cdot \frac{g_{m1}C_{A-I} - I}{g_{m4}C_{A-II} - I} \cdot \frac{s^2 + s(g_{m4}C_{A-II} + g_{m1}C_{A-I}) + g_{m1}C_{A-I}g_{m4}C_{A-II}}{1 - \frac{sC_{B-I}}{g_{m6}} + \frac{sC_{B-I}}{g_{m6}}} \tag{1.24}$$

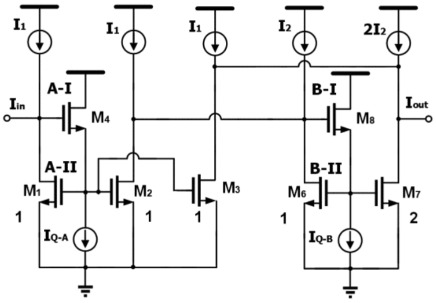


Figure 1.28: Current mirror all-pass filter for delay implementation [92].

The second type of analog delay element employs analog memory cells to introduce delays by controlling the timing between sampling and read-out operations [130–132]. Various types of memory-based delay implementations include:

- Switched-current memory cells [138],
- Bucket-brigade devices (BBDs) [139],
- Analog RAM architectures [131],
- Sample-and-hold circuits (switch-capacitors) [140].

Each approach has unique advantages in terms of resolution, area efficiency, power consumption, and suitability for integration in ultrasound imaging systems.

1.5.3 Digital Beamformer

Digital control logic is commonly employed in the implementation of TX beamformers. For example, the design presented in [58] utilizes shift registers combined with a global counter for timing control. Meanwhile, delay-locked loop (DLL) architectures are employed in [60, 70] to generate precisely timed and phase-aligned TX pulses. Notably, the digital TX beamformer in [60] is among the few that offer programmable phase and amplitude control. In this design, sixteen distinct phase delays enable beam steering and focusing, while four discrete amplitude levels provide apodization for side lobe suppression.

The design considerations for digital receive (RX) beamformers differ significantly from their analog counterparts. A majority of digital RX beamforming approaches are not tailored for implantable systems, and instead rely on field-programmable gate arrays (FPGAs) or commercial digital signal processors (DSPs) [141–144]. These implementations often focus on executing complex beamforming algorithms efficiently, rather than implementing variable delay lines directly. As such, FPGA-based and commercial solutions fall outside the scope of this chapter.

This section focuses on a subset of notable custom IC implementations of digital RX beamformers that are suitable for miniaturized systems [145–148].

In [146], a 64-channel digital RX beamformer was introduced, which employs non-uniform sampling at each channel. This technique samples only the most relevant portions of the received signal, reducing the memory footprint required for data buffering. A look-up table is used to store the timing information for these non-uniform ADC samples, resulting in a FIFO memory reduction of up to 75% compared to conventional uniformly sampled architectures. This method is a promising advancement for reducing area and power in digital ultrasound systems.

An analog-digital hybrid RX beamformer was presented in [145] to address the interfacing challenge of a large 2D CMUT array with dimensions 64×128. With 8192 transducer elements, direct wiring to dedicated beamforming circuits is impractical. To overcome this, a sub-array beamforming approach [149] was employed. The array is divided into smaller 8×8 sub-arrays, reducing the number of output channels to 128. The first stage of beamforming is performed using analog circuits within each sub-array, while the second stage is executed digitally. This hybrid method reduces the number of ADCs required and maintains the precision of digital beamforming.

In [147], a fully digital 3D beamformer capable of handling 10,000 channels was implemented using a VLSI architecture. The complete delay-and-sum beamforming process is performed on-chip without relying on external memory. This system achieves a throughput of 298.1 million focal points per second, enabling the generation of high-resolution volumetric images. Although this represents a significant advancement over analog and earlier digital systems—especially in terms of resolution and computational integration—the power consumption of this design makes it unsuitable for implantable or wearable use cases.

1.6 Analog to Digital Converter (ADC)

ADCs used in medical ultrasound applications are typically optimized for minimal power consumption and compact die area. These constraints are particularly critical in the design of ultrasound imaging probes, where physical size limitations must be considered. Ideally, the size of the ADC chip should be smaller than the transducer's half-wavelength pitch to minimize grating lobes and enhance image resolution.

Unlike other high-speed ADC applications, the stringent requirements for resolution and sampling speed in ultrasound can be somewhat relaxed. Instead, emphasis is placed on achieving sufficient performance within the tight power and area budgets dictated by probe and system integration.

Among the various ADC topologies, SAR, pipeline, and delta-sigma ($\Delta\Sigma$) architectures are the most widely adopted in ultrasound systems due to their balanced trade-offs in power, speed, and area efficiency. This section reviews several notable ADC designs developed specifically for ultrasound applications.

1.6.1 Successive-approximation register (SAR) ADC

SAR ADCs are widely recognized for their suitability in medium-to-high resolution applications, particularly those requiring sampling rates on the order of a few mega-samples per second. Their inherently low power consumption and compact layout make them highly attractive for integration in ultrasound imaging systems [107, 108, 146].

A noteworthy example is the SAR ADC developed in [107], tailored specifically for use in miniature 3D ultrasound probes. This architecture performs digitization in the charge domain, departing from the traditional voltage-domain approach. The conversion process involves comparing the input signal charge against binary-weighted charge references, which are generated using a pre-charged capacitor DAC array within the SAR algorithm. This method enables the removal of intermediate ADC buffer stages, thereby reducing both power consumption and silicon area—two critical design parameters in miniaturized ultrasound systems.

1.6.2 Pipeline ADC

Pipeline ADCs have become increasingly prominent in applications requiring moderate to high sampling speeds. Their balanced performance in terms of power efficiency and silicon area makes them an appealing option for medical ultrasound systems. Despite their practical benefits, only a limited number of pipeline ADCs specifically designed for ultrasound imaging have been documented in the literature [150, 151].

One notable example is presented in [151], where a 10-bit pipeline ADC was fabricated using a 250 nm CMOS process. This design incorporates two parallel sample-and-hold multiplexers to sequentially process signals from eight ultrasound channels, addressing the challenge of handling an increasing number of inputs. Although pipeline ADCs are widely adopted in commercial ultrasound integrated circuits, academic research into their application in medical ultrasound systems remains relatively sparse.

1.6.3 Delta-Sigma ADC

Delta-sigma ADCs are commonly employed in scenarios where low noise and high precision are critical. These characteristics make them a strong candidate for use in medical ultrasound applications. Several implementations of delta-sigma ADCs tailored for ultrasound systems have been reported in the literature [106, 152, 153].

A notable example is described in [153], where an element-matched delta-sigma ADC was developed. The unique aspect of this design lies in leveraging the inherent band-pass filtering properties of PZT materials. By taking advantage of this characteristic, the architecture eliminates the need for additional analog filtering stages, thereby reducing overall hardware complexity. This approach enables the entire delta-sigma ADC to be compact enough to fit directly beneath a transducer element, making it highly suitable for dense ultrasound arrays.

This chapter provided an in-depth overview of IC design for ultrasound systems, covering both medical and emerging non-medical applications (most of the context were based on [153]). Several of the circuits reviewed play a vital role in complete ultrasound platforms, such as those used in intracardiac and transesophageal echocardiography. Future work should focus on enhancing integration, minimizing power consumption, and enabling further miniaturization for next-generation imaging technologies.

Chapter 2

CONUS PRIN Project

2.1 Introduction to the CONUS Project

2.1.1 Overview and Motivation

In recent years, medical ultrasound echography has undergone significant advancements, particularly with the emergence of open ultrasound platforms. These systems enable researchers to develop, test, and validate innovative signal processing techniques and imaging strategies directly on hardware—free from proprietary restrictions. Despite these advances, a major bottleneck remains: the limited number of independently controllable channels, typically capped at 256 on most open scanners. This constraint has restricted research mainly to two-dimensional (2-D) imaging.

The shift toward three-dimensional (3-D) ultrasound imaging—offering immense clinical and research potential—requires simultaneous control of thousands of transducer elements and corresponding electronic channels. Realizing such complexity demands significant innovation in hardware architecture, data handling, and signal processing.

2.1.2 The Vision of CONUS

The conic open scanner for ultrasound (CONUS) project seeks to overcome these limitations by developing an open, modular ultrasound scanner capable of managing thousands of independent channels. It is paired with a cutting-edge 2-D matrix array transducer, enabling true volumetric (3-D) imaging capabilities in an open research framework.

The CONUS platform is:

- **Programmable**: Allowing implementation of custom beamforming and reconstruction algorithms.
- **Reconfigurable**: Supporting various experimental needs through adaptable architecture.
- **Scalable**: Modular design enables growth from small to large imaging arrays.

This architecture facilitates real-time experimentation with modern techniques, including AI and machine learning—paving the way for a new generation of advanced ultrasound imaging.

2.1.3 Consortium and Collaborative Expertise

The CONUS project is a collaboration among four leading Italian universities:

- **University of Florence** – Expertise in ultrasound physics, signal modeling, and biomedical instrumentation.
- **Roma Tre University** – Specialization in MEMS fabrication, modeling, and acoustic packaging.
- **University of Pavia** – Focused on analog and digital microelectronics, including ASIC design and AFE development.
- **University of Basilicata** – Responsible for embedded systems, software engineering, and AI-driven image analysis.

2.1.4 Project Scope and National Relevance

Launched in June 2022, CONUS is supported by the Italian Ministry of Education, University and Research (MIUR) through the PRIN initiative (Progetti di Ricerca di Rilevante Interesse Nazionale) under grant number 20205HFXE7.

PRIN promotes cooperation across academic and public/private research institutions. As such, CONUS not only advances ultrasound research in Italy but also contributes to broader European and global medical imaging initiatives.

2.1.5 System Architecture Overview

The system adopts a novel conical architecture that scales from the compact probe tip, through intermediate acquisition electronics, to a GPU-based mainframe mounted on a mobile cart. Signal conditioning and digitization occur close to the probe to reduce analog degradation, while computational tasks are handled further downstream.

The CONUS system comprises three major subsystems (probe head, front-end acquisition bloc, and mainframe) as illustrated in Fig 2.1:

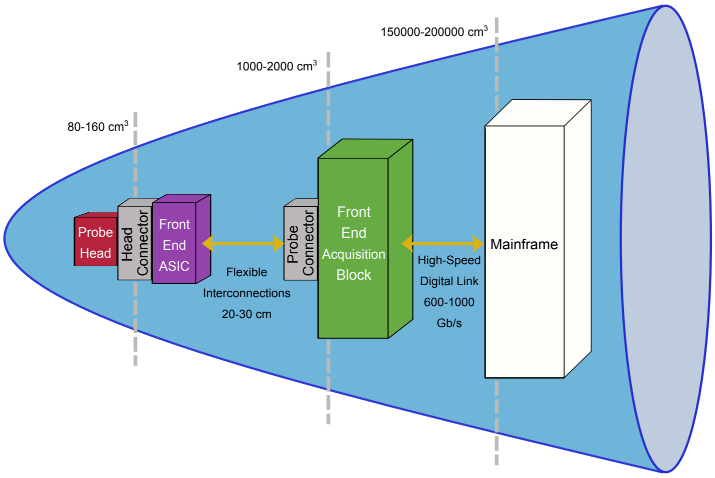


Figure 2.1: Block diagram of the conical architecture illustrating the three core components of the system.

- **Probe Head:** Integrates 2048 CMUT elements and custom ASIC preamplifiers to amplify received echo signals and optimize SNR.
- **Front-End (FE) Acquisition Block:** Performs analog signal conditioning, A/D conversion, and includes transmission circuitry.
- **Mainframe:** The system's backend contains GPU processing units and a workstation for image formation, real-time display, and overall system control.

The mainframe represents the back-end (BE) component of the system. It comprises a series of GPU-based processing units along with a workstation-class PC responsible for managing data processing, real-time imaging, and overall system operations. This distributed system architecture enables the FE module to be integrated into a mechanical support arm, while the mainframe electronics are housed in a mobile cart positioned at the base of the arm (see Fig. 2.2). A flexible connection between the cart and the support arm ensures ergonomic placement of the probe on the patient for optimal usability.

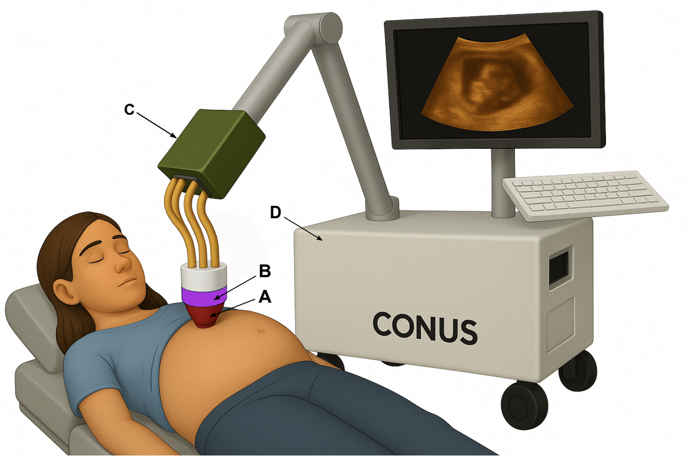


Figure 2.2: Conceptual rendering of the CONUS system: A) probe head, B) FE ASIC, C) FE acquisition Block, D) mainframe (GPU workstation).

2.2 Research Activities and Objectives

The CONUS project integrates multiple R&D activities across several domains. Key components are outlined below:

2.2.1 Ultrasonic Probe Development

A high-channel-count, two-dimensional ultrasonic array will be developed to support both planar and volumetric imaging. The transducer microstructure and acoustic stack are optimized via numerical modeling and fabricated using MEMS technology. Integration into the probe head will rely on a 3-D acoustically optimized packaging strategy to preserve signal fidelity.

2.2.2 Analog Front-End ASIC Development

To overcome the high-impedance nature of MEMS transducers, CMOS-based LNAs will be developed and integrated. After evaluating various design approaches, the selected architecture will optimize noise, linearity, and power consumption for both research and clinical usage.

2.2.3 Ultrasound Open Scanner Development

The system architecture follows a modular, scalable layout—designed as a conical structure. It scales from the probe interface to mid-size acquisition electronics, up to a GPU-powered mainframe. This structure ensures efficient signal flow, bandwidth management, and supports thousands of channels for 3D imaging.

2.2.4 Applications and AI Integration

Key application areas include:

- Resolution enhancement and speed optimization for 3D imaging
- Biometric recognition and medical diagnostics
- AI-based data rate reduction and complexity minimization
- Real-time segmentation and interpretation

Two public datasets will be released to facilitate AI development in ultrasound imaging and biometric identification.

2.3 Probe Design

The probe will incorporate a 2-D ultrasound transducer array, which is connected to custom-designed preamplifiers (Front-End ASIC) and interfaced with the FE acquisition system. The transducer elements, electronic circuitry, and probe casing will be co-developed with the goal of optimizing electroacoustic performance while maintaining a high level of user maneuverability.

2.3.1 CMUT

As illustrated in Figure 2.3, the probe will consist of two primary components: the *probe head*, which integrates the transducer array with appropriate acoustic materials and is mounted onto an electrical substrate, and the *flexible front-end* (flexible FE), which contains front-end ASICs and flexible interconnects. This modular design will allow users to replace either the entire probe or just the probe head via appropriate connectors.

The probe head will house a 2-D transducer array based on MEMS technology, utilizing flip-chip bonding to a substrate that provides both electrical redistribution and acoustic backing. The array will be encapsulated with materials for acoustic matching and protection. Both sparse and dense array configurations (1.5-D and 2-D), with up to 2048 elements, will be analyzed through simulation to optimize key performance parameters such as frequency response, beam steering, focusing capabilities, and overall imaging quality in terms of resolution, contrast, and field of view.

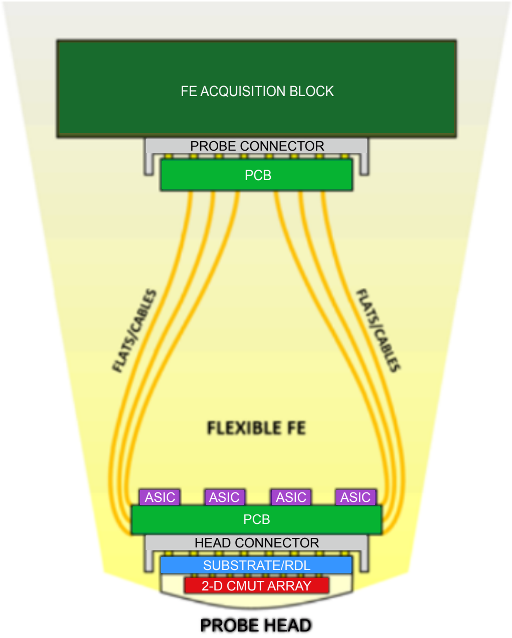


Figure 2.3: Schematic diagram of the probe and its interconnections.

2.3.1.1 CMUT Technology and Packaging

The 2-D transducer array will be fabricated using CMUT technology, chosen for its broad bandwidth, high electromechanical coupling efficiency (resulting in improved two-way sensitivity), and the availability of a microfabrication process well-suited for 2-D array implementation.

The array specifications are as follows:

- **Element count:** 2048 (32 × 64)
- **Footprint:** 16.2 × 27.8 mm
- **Center frequency (%BW):** ∼3 MHz (> 80% bandwidth)

Generally, CMUTs have higher impedance compared to PMUTs. Therefore, especially in the case of small 2-D array elements, placing an LNA nearby is mandatory to preserve the SNR, which would otherwise be severely impacted by the parasitic capacitance of the interconnections.

The CMUTs will be fabricated using the Reverse Fabrication Process [154], which has been successfully employed by Roma Tre University in the development of several medical imaging probes.

To ensure optimal CMUT performance, Finite Element Modeling (FEM) will be employed to evaluate the vibroacoustic interactions between the transducer elements and the surrounding packaging materials. The electrode layout of the CMUT will be carefully designed to accommodate the electrical interconnects to the underlying interposer or substrate, which interfaces with the flexible FE.

The bonding approach will leverage copper (Cu) pillar technology combined with a pre-applied benzocyclobutene (BCB) underfill. This vertical interconnection method enables efficient electrical contact between the CMUT array and substrate while preserving the full active area of the array.

2.3.1.2 Equivalent Circuit Model (ECM) and its parameters

To obtain the model of the CONUS transducer array element consisting of 18 CMUT cells in parallel, the value of N to be used for scaling is exactly 18. Therefore, each CMUT element comprises 18 membranes operating in non-collapse mode. Table 2.1 presents the electroacoustic parameters of the ECM (shown in Fig. 2.4) for a single CMUT membrane.

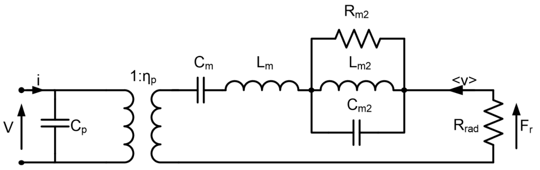


Figure 2.4: Equivalent circuit model of the CONUS single CMUT membrane.

Table 2.1: Numerical parameters for the ECM of a single CMUT membrane

Parameter	Value	Unit
$Area \times N$	10.961	nm^2
$\eta_p \times N$	0.22653	mN/V
$C_p \times N$	0.28168	pF
C_m/N	2.2623	μm/N
$L_m \times N$	0.44159	ng
C_{m2}/N	0.91236	μm/N
$L_{m2} \times N$	0.13389	ng
$R_{m2} \times N$	10.9606	kg/s
$R_{rad} \times N$	0.016222	kg/s

It should also be noted that the model parameters do not include any parasitic elements. With reference to the equivalent circuit below (Fig. 2.5), the most relevant parameter will be the interconnect capacitance (introduced by the cable/flex/PCB) between the CMUT and the AFE, C_{p-par}, which can be in the order of tens of pF. Given the high impedance of the CMUT array element, the other parameters probably won't have a relevant impact on the RX performance.

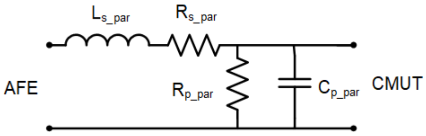


Figure 2.5: Schematic diagram showing the parasitic elements in ECM.

- Total series resistance of CMUT electrodes: $R_{\text{s-par}} = 11.5\ \Omega$
- Series inductance of the rigid-flex PCB: $L_{\text{s-par}} = 254$ nH
- Leakage resistance: $R_{\text{p-par}} = 3.6\ \text{G}\Omega$

2.3.2 In-probe FE ASIC

The FE ASIC architecture must be specifically tailored to the unique electrical and acoustic properties of the CMUTs developed for this project. Furthermore, the LNA designs undergo detailed transistor-level simulations to validate CMOS implementation feasibility.

Initially, single-channel LNA prototypes will be fabricated and tested to fine-tune the design. A multi-channel ASIC will later be developed for full integration into the probe system. The final ASIC's channel count and physical arrangement on the flexible FE PCB will be optimized based on area constraints and performance targets. Connection between the flexible FE and the probe head will leverage advanced high-density connectors, such as Land Grid Arrays (LGA), often used in desktop CPU packages. To maintain mechanical flexibility between the probe and system electronics, options such as micro-coaxial cables and Rigid-Flex PCBs will be explored.

2.3.2.1 Commercial in-probe FE ASIC

The commercial FE ASIC, MAX14822, a 16-channel low-noise operational amplifier with integrated high-voltage protection, was initially investigated for the CONUS project. Its compact design makes it well-suited for direct integration into ultrasound probes. The key circuit parameters, as listed in the MAX14822 datasheet, are summarized in Table 2.2 and its functional diagram is depicted in Fig. 2.6.

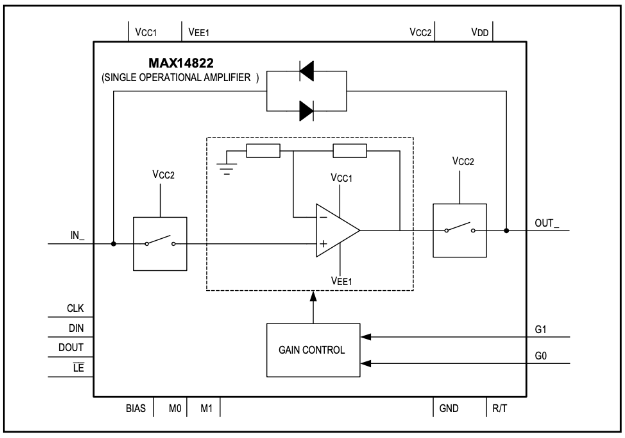


Figure 2.6: Schematic diagram of the MAX14822 ASIC.

Table 2.2: MAX14822: Key Performance Parameters

Parameter	**Value**
Power dissipation per channel	8.6 mW
Voltage noise @ 5 MHz	$1.3\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$
Current noise @ 5 MHz	$1.7\ \mathrm{pA}/\sqrt{\mathrm{Hz}}$
Output impedance	20 Ω
Input resistance	24 kΩ
Input capacitance	3 pF
C_{pai}	3 pF
R_{lna}	24 kΩ
R_{en}	106.44 Ω
R_{in}	9.8 mΩ

Taking all factors into account, the primary objective of my work in this project was to enhance the performance of the mentioned commercial FE ASIC, with a particular focus on reducing power consumption and minimizing input-referred noise.

The detailed design and implementation process of the proposed in-probe front-end ASIC will be thoroughly presented in the following chapters.

2.3.3 AFE Acquisition Block

The AFE acquisition subsystem manages all 2048 TX and RX channels. It is composed of modular units, each responsible for 64 channels, enabling scalable system integration. A standard interchangeable connector interface ensures compatibility with different probe types, both custom-designed and commercial. Adapter boards will be developed to facilitate this probe diversity.

Open ultrasound scanners have recently accelerated the development of innovative imaging methods. These platforms are generally categorized into hardware-oriented systems—utilizing embedded FPGAs and DSPs—and software-oriented systems—relying on GPU-based processing on host PCs.

In this project a high-performance, heterogeneous open scanner that combines the strengths of both approaches was developed by the University of Florence. The 256-channel *Ultrasound Advanced Open Platform* (ULA-OP 256) was enhanced through the integration of a compact co-processing GPU system-on-module (SoM).

A key contribution was the implementation of an efficient, low-latency PCIe communication interface between the GPU and onboard processing units, achieved through low-level optimizations.

As a proof of concept, high frame rate (HFR) color flow mapping (CFM) was implemented on the GPU SoM. Compared to a previous DSP-only implementation, the GPU-based solution demonstrated superior real-time frame rates and increased flexibility in configuring parameters such as ensemble length (EL).

For instance, with an ensemble length of 64 and a continuous-time high-pass filter (HPF), flow patterns were examined with high spatial and temporal resolution in the femoral vein bifurcation at 1.1 kHz frame rate, and the carotid artery bulb at 4.3 kHz frame rate.

These results revealed complex flow dynamics such as valve-induced disturbances and secondary velocity components. The success of this implementation suggests promising potential for real-time deployment of other computationally intensive ultrasound processing techniques and informs future developments in heterogeneous ultrasound scanner design.

The ULA-OP 256 ultrasound system, as depicted in Fig. 2.7, is composed of three main functional blocks: FE, Master Control (MC), and Co-Processing (CP) [155].

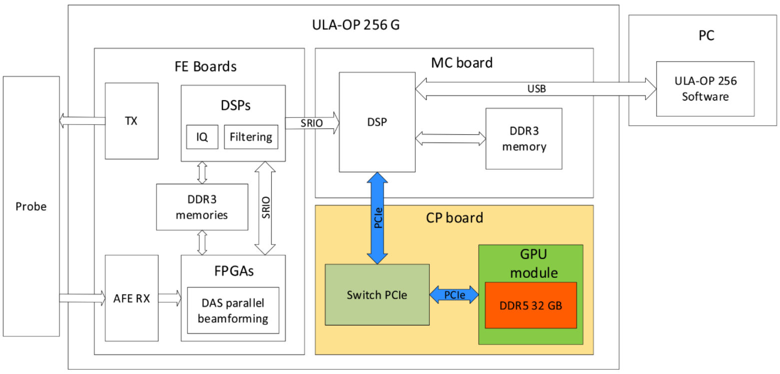


Figure 2.7: Block diagram of ULA-OP 256G with, highlighted, the novel CP board. [155]

2.3.3.1 FE Boards

The FE architecture consists of eight boards, each managing 32 channels and probe elements. Each board includes:

- An FPGA (ARRIA V GX, Altera) that generates sigma-delta modulated TX waveforms, which are low-pass filtered and fed to high-voltage amplifiers.
- An analog front-end chip (AFE5807, Texas Instruments) for RX echo signals, performing low-noise amplification, bandpass filtering, time gain compensation, and digitization at 78.125 MHz (or integer submultiples).
- An on-board DAS beamformer in the FPGA, supporting parallel mode for high frame rate (HFR) imaging.
- Two 8-core DSPs (TMS320C6678, Texas Instruments) for I/Q demodulation, filtering, and downsampling, with support for coherent compounding in HFR imaging.

Inter-board communication is handled by a SerialRapidIO (SRIO) bus with 10 GB/s full-duplex bandwidth in a ring topology. Beamformed baseband data is coherently accumulated across FE boards.

Each FE board includes 18 GB DDR3 SDRAM: 2 GB for the FPGA and 8 GB for each DSP, used for beamforming delay LUTs, apodization, real-time buffers, and data storage [155].

2.3.3.2 Master Control (MC)

The MC board features one DSP (same model as FE DSPs) which:

- Coordinates and sequences TX/RX phases and scan configurations across FE boards.
- Performs high-level baseband signal processing as needed.

2.3.3.3 Co-Processing (CP)

To enhance processing power, a CP expansion board integrates an Nvidia Jetson AGX Orin GPU module. Key specifications:

- 2048 CUDA cores, Arm Cortex-A78AE CPU, 32 GB LPDDR5 RAM
- Connected to the MC DSP via a PCIe switch (PEX8796) supporting up to 96 PCIe 3.0 lanes
- Data transfer over Gen 2 (DSP) and Gen 4 ×8 lanes (GPU)

The GPU acts as a co-processor: post-beamforming I/Q data from the MC DSP is sent to the GPU via PCIe, processed, and returned for visualization or forwarded to a PC via USB 3.1 SuperSpeed [155].

In summary, the CMUT equivalent circuit is the input and the entire AFE acquisition block, connected via cables, acts as the load for the in-probe FE ASIC, which is the central focus of this thesis. As a result, the output is modeled by taking into account the equivalent impedance and capacitance of the connecting cables, represented by a 160 pF capacitor.

Chapter 3

Front-End ASIC Design

This chapter presents the design of CMUT-based front-end (FE) receiver application-specific integrated circuit (ASIC) blocks, including TX/RX switches, LNA, low-dropout regulator (LDO), cable driver or buffer, current generator, delay cell, and operational amplifier (Op-Amp), all designed and described at the transistor level.

Initially, the key design requirements and candidate topologies for each block are introduced. This is followed by detailed circuit implementations, performance characterization, and a comparison with state-of-the-art solutions.

The chapter concludes with a discussion, while experimental measurements and overall conclusions are provided in Chapters 4 and 5, respectively.

3.1 Front-End ASIC Block Diagram

Ultrasound (US) imaging systems are extensively employed in medical applications and have emerged as a favorable choice for healthcare practitioners compared to other diagnostic imaging techniques like radiography, X-ray computerized tomography (CT), and magnetic resonance imaging (MRI), thanks to their inherent safety and noninvasive nature. Nowadays, relying on micro electro-mechanical systems (MEMS) technologies, the manufacturing process of US transducers is steering towards the so-called micro-machined ultrasound transducers (MUTs), at the expense of traditional bulk transducers.

A typical US imaging setup consists of a main unit and a probe, housing many electro-acoustic transducer (TD) elements, even thousands, arranged in a 2-D array matrix, thus enabling 3-D imaging capabilities. Each TD requires its own FE transceiver, in order to achieve a multi-channel system. Since HV transmission and LV reception circuits are linked to the TD arrays via micro-coaxial cables, in order to minimize the number of wires, and therefore cost and volume, the FE ASICs should allow both TX and RX operations using a single wire. Among MUT devices, the CMUT is particularly promising due to its wide bandwidth, high resolution, straightforward fabrication process, and ease of integration with ASICs. However, CMUTs necessitate high-voltage pulses, in the order of 100-V, when actuated as transmitters.

Therefore, appropriate circuitry, particularly TX/RX switches, is required to protect the LV part of the FE circuit from the HV pulses when a single cable is shared between TX and RX modes. The block diagram of the FE ASIC for a CMUT-based US system channel is shown in Fig. 3.1 (based on the commercial product MAX14822 frame).

The block diagram of the customized in-probe FE ASIC for a CMUT-based US system channel is shown in Fig. 3.1. To minimize cable count and reduce overall system complexity, both the HV TX and LV RX circuits within the AFE block interface with the CMUT through a single micro-coaxial cable. The ASIC integrates four channels arranged in a square matrix, each incorporating RX electronics interfacing with four CMUTs as a preliminary design specification.

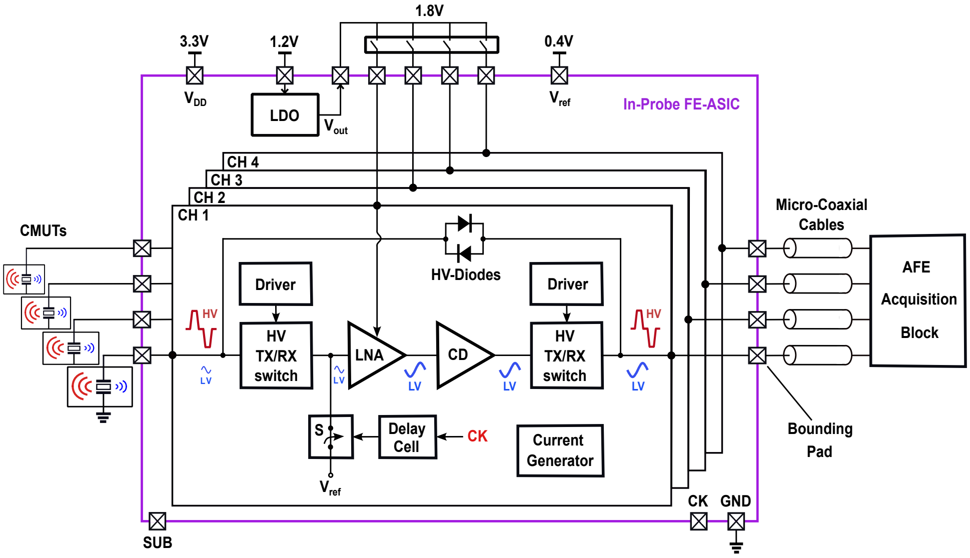


Figure 3.1: Block diagram of the proposed in-probe front-end ASIC, highlighting its main sub-blocks: TX/RX switches, LNA, LDO, buffer, current generator, delay cell, and two high-voltage diodes. The chip interfaces with the CMUT at the input and the micro-coaxial cable at the output.

Each channel includes a shared current reference, a low-noise amplifier (LNA), a reference switch (Vref = 400 mV) with an associated delay cell, two HV protection diodes, a cable driver (CD) stage, and a pair of HV TX/RX switches with dedicated driver circuits to protect the LV components from the bipolar HV excitation pulses used to drive the CMUT. In this prototype implementation, the four LNAs across all channels provisionally share a single LDO regulator.

As shown in Fig. 3.1, the ASIC comprises 19 pins in total: four inputs from the CMUTs and four outputs to the micro-coaxial cables, corresponding to the four RX channels, one main supply pin (3.3 V), a reference voltage pin (0.4 V), and an LDO reference voltage pin (1.2 V). These supply and reference voltages are provided off-chip in the open scanner system. Additional pins include one for the clock (CK) signal from the AFE block, a ground (GND) pin (0 V), and a substrate pin (SUB). As a single LDO is shared among the four channels, its output is routed off-chip through a dedicated pin and then returned to each channel via four separate input pins, utilizing pin headers and jumpers on the printed circuit board (PCB) to enable channel selectivity.

The design of FE-ASICs, and particularly in-probe implementations, must be closely tailored to the characteristics of the target transducer. Since the ASIC architecture, biasing conditions, and interface circuitry are highly dependent on transducer parameters such as impedance, operating voltage, and bandwidth, it is essential to first outline the transducer specifications and key performance features. This foundation enables a more precise understanding of the design considerations and constraints that shape the architecture of the subsequent ASIC blocks.

In this work, CMUTs were selected for two main reasons: firstly because of higher electromechanical coupling efficiency, leading to improved two-way sensitivity. Secondly because of availability of a microfabrication process particularly suited for 2-D array fabrication. Since CMUTs typically exhibit higher impedance than piezoelectric micromachined ultrasonic transducers (PMUTs), especially for small 2-D array elements, placing a preamplifier in close proximity to the elements is essential to preserve the signal-to-noise ratio (SNR) and to minimize the effects of interconnect parasitic capacitance.

As discussed in the previous chapter, this project utilized a CMUT model provided by our collaborator, the University of Roma Tre. To simplify the simulation environment, the physical cable was substituted with an equivalent capacitance of 160 pF, replicating its electrical characteristics. The cable specifications and parameters used for this substitution were supplied by another project partner, the University of Florence.

3.2 High-Voltage TX/RX Switches

For implementing HV TX/RX switches HV transistors have to be used, thus requiring a HV Bipolar-CMOS-DMOS (BCD) technology. As HV transistors typically occupy larger area with respect to LV transistors, it is desired to minimize the number of HV transistors in order to minimize the overall chip area. Furthermore, in the considered FE circuit, since the RX and TX chains share the same frame, the high-voltage power supply is not available in the FE ASIC and, therefore, it is necessary to use the only available low-voltage power supply.

In order to address the mentioned design considerations, this work proposes a HV TX/RX switch with a LV power supply driver and minimum number of HV transistors. Moreover, using a DC control loop, the proposed switch structure benefits from highly-matched current sources, to eliminate the leakage current and consequently achieve zero static power consumption in the TX phase.

3.2.1 TX/RX Switch Implementation

The TX/RX switch needs to provide bidirectional HV isolation, meaning that, when the switch is off, it must be able to maintain the off state while dealing with both positive and negative HV pulses. Therefore, the TX/RX switch must be configured with a back-to-back connection of two HV transistors sharing a common gate and a common source. Typically, NMOS transistors are preferred mainly because of their area efficiency, as illustrated in Fig. 3.2(a).

The fundamental operational mechanisms of the TX/RX switch during the RX and TX phases are illustrated in Fig. 3.2(b) and Fig. 3.2(c), respectively. In the RX phase, as depicted in Fig. 3.2(b), S_1 is on and S_2 is off and the gate-source voltage (V_{gs}) of the main switch (comprising M_1 and M_2) is between the HV transistor threshold voltage V_{th} and the LV supply voltage $LV\text{-}V_{DD}$, turning the main switch on to allow signal transfer. In the TX phase, Fig. 3.2(c), S_1 is off and S_2 is on, the V_{gs} of the main switch is 0 V, rendering the main switch off, and preventing HV signals from reaching the output.

In order to turn the TX/RX switch on and off, the required V_{gs} should be provided using a driver circuit, as shown in Fig. 3.2(d), where an N network is responsible for transforming the current provided by the current source I, into the V_{gs} voltage required to turn the switch on. Various components including resistors [162, 163], Zener diodes [164], or diode-connected MOSFETs [165] have been used to construct the network N. The main downside of this arrangement is the unavoidable leakage current from the positive supply voltage

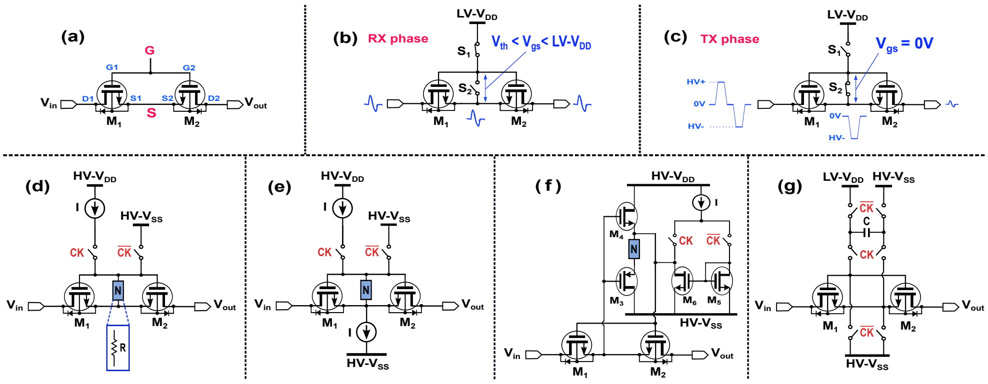


Figure 3.2: Implementation of HV TX/RX switch: a) basic configuration, b) operation in RX phase, c) operation in TX phase, d) structure of required driver presented in [163], e) two current source driver presented in [167], f) bootstrap method presented in [168], g) bootstrap technique presented in [169]

$HV - V_{DD}$ (for example +25 V) towards the negative supply $HV - V_{SS}$ (for example -25 V) through the switch terminal ports. To address this problem, several techniques have been reported [166]. For instance, incorporating an additional current source to sink the driver current, as shown in Fig. 3.2(e) [167], while, the mismatch between the current sources makes the complete cancellation of the leakage current still unattainable.

Alternatively, a bootstrapped technique is reported in [168], where the driver current path is isolated from the switch current path, as illustrated in Fig. 3.2(f). This can minimize the leakage current, but increasing the transition speed requires a higher current and consequently higher power.

A bootstrap technique using a pre-charged flying capacitor, presented in [169] and shown in Fig. 3.2(g), allows the use of a low-voltage power supply instead of the HV power supplies $HV - V_{DD}$ and $HV - V_{SS}$ (tens of volts) required by earlier methods [163, 167, 168]. This approach reduces the power consumption, though leakage current remains a concern.

3.2.2 Proposed TX/RX Switch Structure

As discussed in previous section, a channel of the FE ASIC for US transducers consists of an LNA, two HV switches and two diodes. The proposed HV TX/RX switch implementation, including the main switch, its driver circuit and the DC loop, is illustrated in detail in Fig. 3.3. The key role of the TX/RX switch is to protect the low-voltage LNA from high-voltage bipolar pulses up

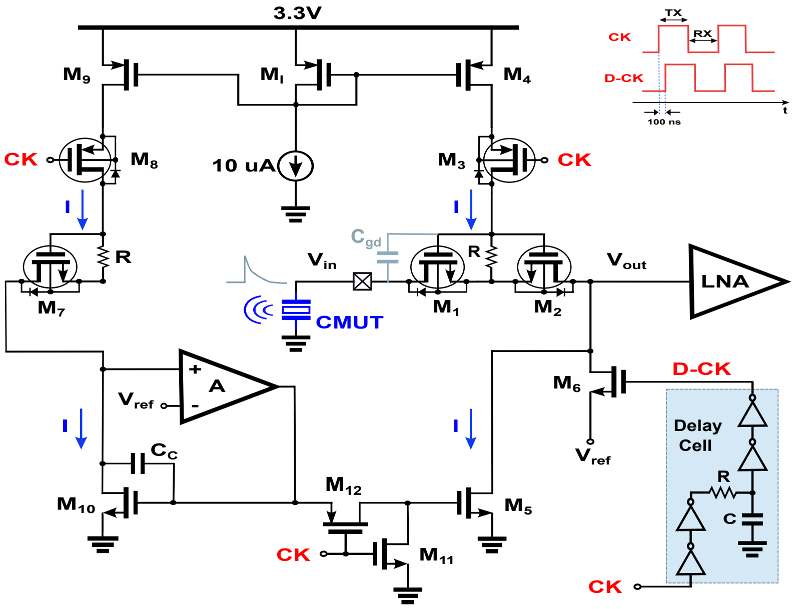


Figure 3.3: Architecture of the proposed HV TX/RX switch

to 200 Vpp during TX periods and to transfer small echo signals with a low on-resistance (R_{on}) during RX periods. It is therefore fundamental to guarantee that the TX/RX switch remains off during TX periods, as well as ensure proper switching between TX and RX operating phases. This can be easily achieved by using the proposed driver structure.

The main HV TX/RX switch is formed by two NMOS transistors, M_1 and M_2, featuring 100 V voltage rating. The sizes of M_1 and M_2 are defined based on their noise contribution, meaning that their noise should be significantly lower than the LNA input referred noise (at least by 10 dB).

The driver circuit of the main TX/RX switch consists of a HV PMOS transistor M_3 used as a switch, two current sources (implemented through M_4 and M_5) and a resistor R located between the common gate and common source terminals of the main switch. The PMOS HV switch M_3 and NMOS LV transistors M_6 and M_{11} are responsible for controlling the state of the main switch and isolating the low voltage current mirror devices from high voltages.

In the RX phase, the current I provided by current source M_4 flows through resistor R to turn the switch on and then is sunk by transistor M_5. The resistor R is set to 28 kΩ, while the current I is adjusted to 90 μA to provide 2.5 V between the gate and source of the main switch, ensuring it is turned on.

For ensuring matching between the two current sources (M_4 and M_5), a

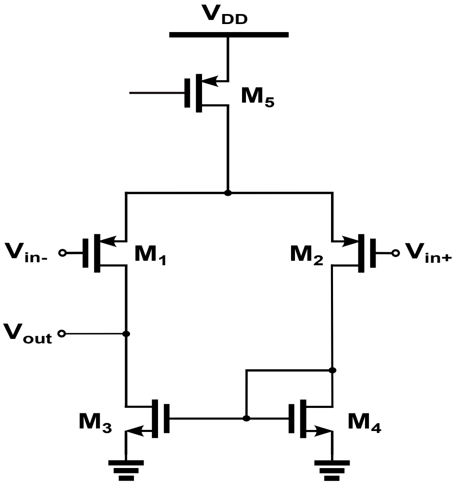


Figure 3.4: Schematic of the op-amp circuit used in the DC control loop

replica branch consisting of two HV MOS devices (M_7 and M_8, matching M_1 and M_3, respectively), two LV MOS devices (M_9 and M_{10}, matching M_4 and M_5, respectively), and a resistor R (matching the one used for the main switch), has been used. In this way, current I is effectively monitored in the replica branch. In addition, a DC control loop, by means of an operational amplifier, forces the DC voltage at the drain of M_{10} to be equal to the reference voltage V_{ref}, set to 400 mV, i.e., the desired common-mode voltage at the LNA input. As a result, the two current sources (M_4 and M_5) will be highly matched, and the 90 μA current I will be sunk entirely by current source M_5.

As depicted in Fig. 3.4, the operational amplifier is implemented with a simple differential pair with active load structure, featuring a 62 dB open-loop gain and 74° phase margin. Transistor M_{10} and the replica branch operate as a two-stage operational amplifier, with C_C, equal to 0.5 pF, acting as a Miller compensation capacitor to ensure the stability of the circuit.

In the TX phase, M_3 is off, no current flows through R and the main switch is off. Two additional switches M_{11} and M_{12} are used to guarantee that current source M_5 is also completely off and that there is no static current path from the 3.3 V supply to ground. Switch M_6 provides the required DC level ($V_{\text{ref}} =$ 400 mV) at the input of the LNA. A second TX/RX switch, connected after the LNA, is implemented with the same structure, using another replica branch, with just three HV MOS devices (M_{13}, M_{14} and M_{15}), two LV MOS devices (M_{16} and M_{17}) and a resistor R. During the transition from TX to RX, due to the coupling determined by the parasitic gate-to-drain capacitance (C_{gd}) of

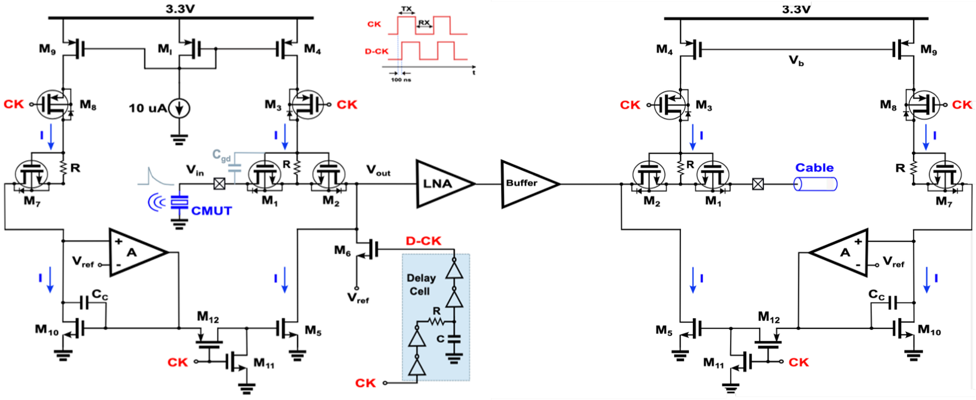


Figure 3.5: Schematic of the HV TX/RX switches

M_1, as illustrated in Fig. 3.5, a spike is generated at the CMUT input node. By opening the LV switch M_6 with a delay relative to the main clock signal CK controlling the other switches, this spike can be minimized. Specifically, M_6 is switched off by the delayed clock signal D-CK once the transition from TX to RX mode is completed and the V_{gs} of the main switch has settled. The delay cell is simply implemented using four inverters, a resistor, and a capacitor, as shown in Fig. 3.5. A delay time of 100 ns is selected to effectively suppress the spike.

The control signals *CK* and *D-CK* operate between ground and the 3.3 V supply. As a result, the proposed architecture can effectively drive the TX/RX switch without requiring a high-voltage supply, thereby fulfilling the requirements of the CMUT-based ultrasound system channel. The second switch can be implemented similarly to the first, with two main differences: first, the transistor sizes in the main switch must be selected based on the specific cable specifications; second, there is no need to include a switch connected to V_{ref} or a delay cell. The proposed TX/RX switches were designed using a 160 nm BCD8-SOI technology.

3.2.3 Simulation Results of the TX/RX Switch Block

The proposed TX/RX switch was implemented in a 160 nm BCD-SOI technology. Figure 3.6 illustrates the simulated waveforms of the input signals to the TX/RX switch in both RX and TX modes—specifically, the low-voltage sinusoidal echo signal received from the CMUT and the high-voltage pulses used for transmission—alongside the control clock and the switch output. During

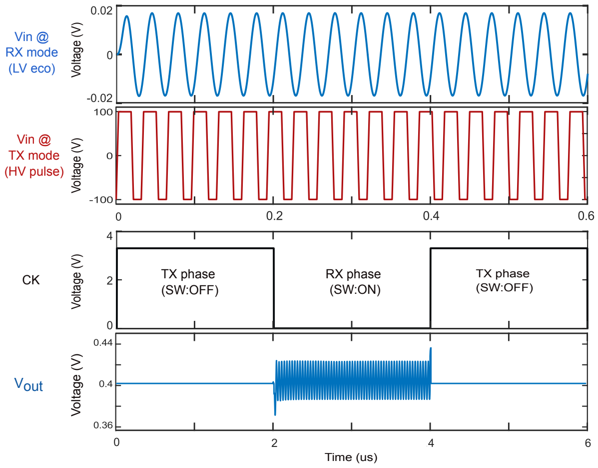


Figure 3.6: Simulated waveforms of the proposed TX/RX switch

the TX period, the output voltage is equal to $V_{\text{ref}} = 400\,\text{mV}$, while during RX, it tracks the input from the CMUT as expected. The CMUT signal is a sinusoid with a 34 mV peak-to-peak amplitude.

Figure 3.7 presents the open-loop gain and phase of the operational amplifier employed in the DC control loop. Under typical process conditions, the amplifier achieves a gain of 62 dB and a phase margin of 74°.

Simulation results demonstrating the suppression of the TX-to-RX transition spike are shown in Fig. 3.8. Without delay, the spike reaches approximately 150 mV, whereas applying a 100 ns delay nearly eliminates it. Figure 3.9 displays the off-isolation performance of the switch as a function of frequency, calculated as $20\log(V_{\text{out}}/V_{\text{in}})$ when the main switch is off. For a 100 V sinusoidal input, the off-isolation at the nominal frequency of 3 MHz is approximately $-42\,\text{dB}$.

Figure 3.10 shows the output voltage V_{out} across different process corners, where the maximum variation remains within 3 mV. Additionally, Monte Carlo simulations (500 samples) accounting for both process and mismatch variations were performed to evaluate the gate-source voltage V_{gs} of the main switch. The results indicate a mean value of 2.43 V with a standard deviation of 250 mV, ensuring reliable switch operation under all conditions.

The estimated area of a single TX/RX switch is approximately 25,600 μm^2, assuming 60% layout efficiency.

Table 3.1 compares the proposed HV TX/RX switch with prior designs, emphasizing its reduced supply voltage and lower number of HV transistors, while maintaining solid performance in other important parameters.

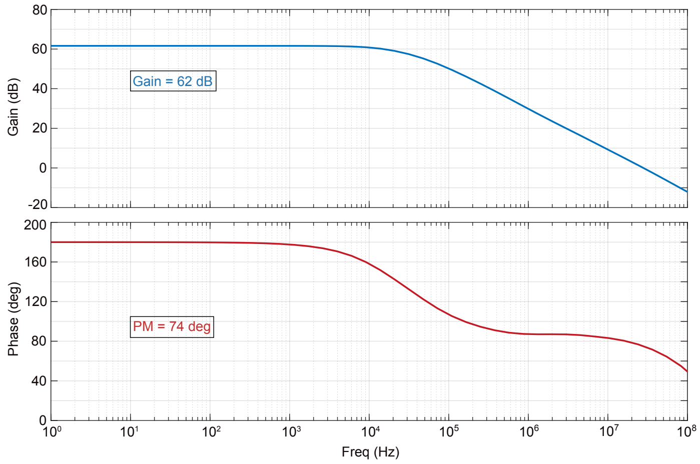


Figure 3.7: Open-loop gain and phase of the operational amplifier used in the DC control loop of the switch

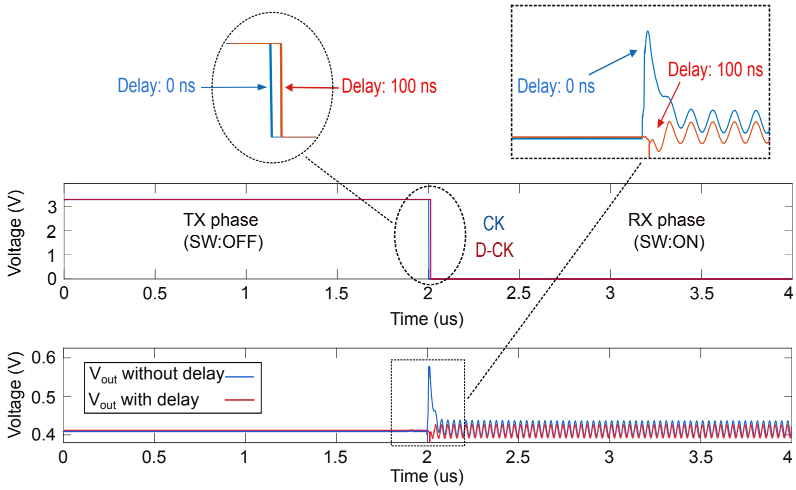


Figure 3.8: The proposed delayed-clock control for suppressing the TX to RX transition spike

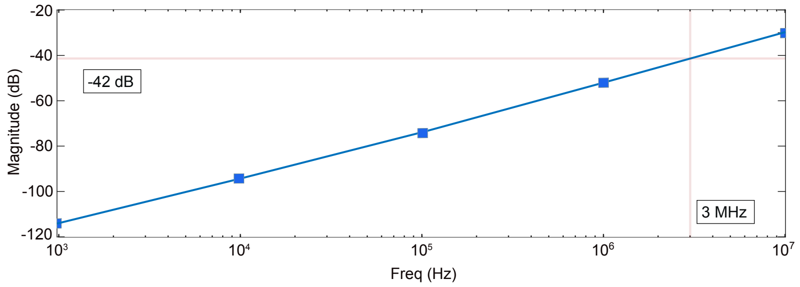


Figure 3.9: Off-isolation of the proposed switch as a function of frequency

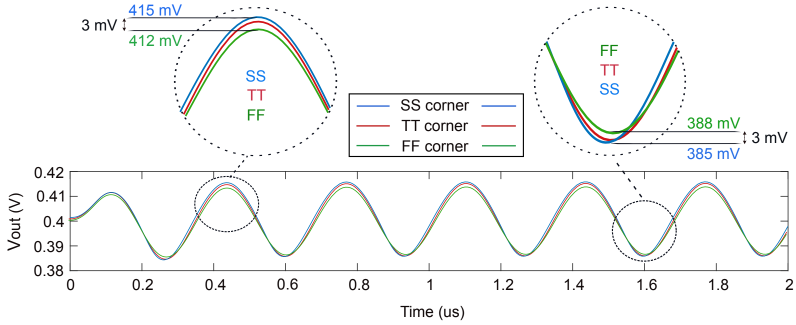


Figure 3.10: The output voltage (V_{out}) of the proposed switch in process corners

Table 3.1: Comparison with other works

Ref.@Year	**[171]@2016**	**[170]@2018**	**[166]@2022**	**This Work**
Technology	350 nm CMOS	350 nm CMOS	180 nm CMOS	160 nm BCD-SOI
SW Supply	120 V	40 V	25 V	3.3 V
Number of HV MOSs	9	>5	10	5
Static Power	N.A.	N.A.	7.5 μW	660 μW
R_{on}	700 Ω	180 Ω	100 Ω	190 Ω
Off-Isolation	-34 dB @10 MHz	-35 dB @10 kHz	-92 dB @10 kHz	-42 dB @3 MHz

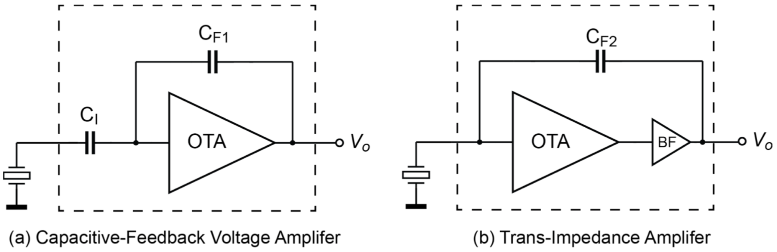


Figure 3.11: Architecture of (a) capacitive-feedback voltage amplifier (CFA) and (b)trans- impedance amplifiers (TIA).

3.3 LNA

3.3.1 Architecture Considerations

In most ultrasound receiver designs, the LNA is the critical first-stage component that directly interfaces with the transducer, typically through a TX/RX switch or limiter. By providing initial linear amplification of weak echo signals, the LNA plays a crucial role in minimizing noise contributions from the subsequent circuitry, thereby optimizing the overall noise-power trade-off of the receiver system.

The form of amplification, whether as a voltage gain, current gain, transimpedance gain, or transconductance gain, depends on both the characteristics of the transducer and the desired output signal format. Consequently, a transducer-oriented design approach is essential for selecting and optimizing LNAs in ultrasound applications.

Among the available topologies, capacitive-feedback voltage amplifiers (CFAs) and transimpedance amplifiers (TIAs) are the most widely used architectures in ultrasound front ends (see Fig. 3.11). This section compares their noise-efficiency, providing insight to select the suitable architecture [172].

3.3.1.1 Assumptions for Fair Comparison

- **Capacitive feedback** is applied in both architectures to achieve optimal noise and power performance, since capacitive networks are noise-free.

- In TIAs, the received echo current undergoes a **90-degree Phase shift** due to the capacitive feedback, and the resonance frequency may shift slightly. These effects must be accounted for in the system-level design.

- A **buffer stage** (commonly a source follower) is added after the OTA in the TIA to ensure accurate feedback by lowering the output impedance. The power required by this buffer and any frequency compensation circuitry should be included in power-efficiency evaluations.
- CFAs do not need an in-loop buffer. However, if the LNA drives a low-impedance load (e.g., a coaxial cable), an **out-of-loop buffer** is still necessary. Buffers inside a feedback loop typically require more power to preserve loop stability across wide bandwidths.
- In cases where the LNA is followed by an ADC sampler or micro-beamformer, the **power demands of buffer stages** (whether inside or outside the loop) must be carefully assessed.
- For simplicity, **large DC bias resistors** often used in both architectures are not shown in the referenced figures but are assumed to be part of the practical design.

3.3.1.2 Key Architectural Differences

The CFAs sense the voltage from the transducer and therefore present a high input impedance. Conversely, TIAs sense current by maintaining a low input impedance through a virtual ground. This fundamental distinction makes it non-trivial to directly compare their noise performance.

As discussed in earlier sections, the selection of an appropriate LNA topology in ultrasound front-end design is largely influenced by the electrical impedance characteristics of the target transducer. For CMUT-based systems, which typically exhibit relatively high output impedance, TIAs are commonly employed in readout ICs [172].

To reduce power consumption, it is essential to maximize the current efficiency of the OTA. This makes the CMOS inverter an appealing option. A basic implementation of an inverter-based OTA is illustrated in Figure 3.12. Here, the input signal is AC-coupled to the gates of the NMOS and PMOS transistors, while a DC feedback loop regulates the output voltage to the mid-supply level, ensuring both transistors operate in their optimal regions.

When used in the target ultrasound application, the circuit shown in Figure 3.12 presents several drawbacks. Firstly, the AC-coupling capacitors, together with the parasitic capacitance at the input gates, form a capacitive divider that reduces the input signal amplitude. This, in turn, increases the input-referred noise of the LNA. Increasing the size of these AC-coupling capacitors to mitigate the attenuation requires considerable silicon area [173].

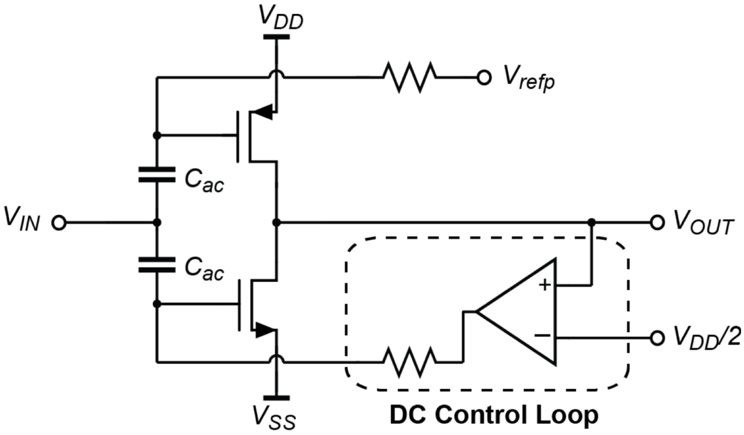


Figure 3.12: Simplified schematic of the inverter-based OTA in [173].

Secondly, the circuit exhibits limited power-supply rejection, which is a significant concern in ultrasound probes where the power lines may carry noise, even within the signal frequency band, due to nearby integrated digital signal processing units.

Lastly, the feedback amplifier used in the DC control loop is directly connected to one of the inverter inputs, contributing additional noise and parasitic capacitance.

In this work, these limitations are addressed through a set of dedicated circuit techniques, as detailed in the following.

3.3.1.3 Proposed LNA structure

To achieve an optimal balance between noise performance and power consumption, a noise analysis must first be carried out for the basic CMOS inverter configuration. The input-referred noise voltage is then derived as:

$$\overline{v_{n,\text{in}}^2} \approx \frac{4kT\gamma}{g_{m1} + g_{m2}} \approx \frac{2kT\gamma}{g_{m1}} \tag{3.1}$$

where g_{m1} and g_{m2} denote the transconductance of the transistors M_1 and M_2, respectively, k is the Boltzmann constant, T is the absolute temperature in Kelvin, and γ is the MOSFET noise coefficient.

Equation (3.1) indicates that the input-referred noise decreases with increasing transconductance of the input devices. This insight directly informs the sizing and biasing strategy used in the circuit design to achieve noise-power optimization.

On the other hand, the conventional CMOS inverter topology suffers from several limitations, most notably its significant sensitivity to process, voltage, and temperature (PVT) variations. The voltage gain is determined by the ratio of the combined transconductance of transistors M_1 and M_2 to the output resistance:

$$A_v = \frac{g_{m1} + g_{m2}}{R_{\text{out}}} \tag{3.2}$$

Moreover, M_1 and M_2 tend to compete in establishing the circuit's bias point, which can lead to instability. Therefore, appropriate modifications to this basic configuration are required to enhance its performance and reliability.

As illustrated in Fig. 3.13(a), the finalized LNA block diagram is presented. Transistors M_1 and M_2 function as the primary input devices, while M_3 and M_4, originally implemented as diode-connected MOSFETs, were designed to determine the voltage gain according to:

$$A_v = \frac{g_{m1} + g_{m2}}{g_{m3} + g_{m4}} \tag{3.3}$$

However, in the final implementation (see Fig. 3.13(b)), M_3 is replaced with a current source to allow sufficient headroom at the output node V_{out}.

A DC control loop is employed to define the bias point of the LNA. This loop includes transistors M_7 and M_8, which set the DC current for M_1 and M_2. To suppress thier noise contribution to the input-referred noise, RC filters composed of (R_1, C_1) and (R_2, C_2) are used. A differential pair consisting of M_5 and M_6 is included to apply an external reference voltage V_{ref} (400 mV) to the output node V_{out}. Transistors M_{R1} and M_{R2} implement local current mirroring, combined with RC filtering (R, C), to further reduce noise. The complete DC control loop comprises transistors M_5 through M_{11}.

The LNA topology operates in a closed-loop configuration for DC, while it remains open-loop with respect to the AC input signal. Input capacitors C_{in1} and C_{in2} are utilized for AC coupling of the signal V_{in} and their size chosen to set the RX bandwidth from 60 kHz to 8 MHz, aligning with the CMUT's frequency response, which peaks around 3 MHz.

To appropriately size the transconductance $(g_{m1} + g_{m2})$, the SNR requirements of the entire receive signal chain must be considered. A minimum SNR of 0 dB is imposed under the weakest mechanical input signals generated by the CMUT. The total input-referred noise of the LNA is integrated over the sensor's -3 dB bandwidth, ensuring it remains below the CMUT's minimum expected signal output.

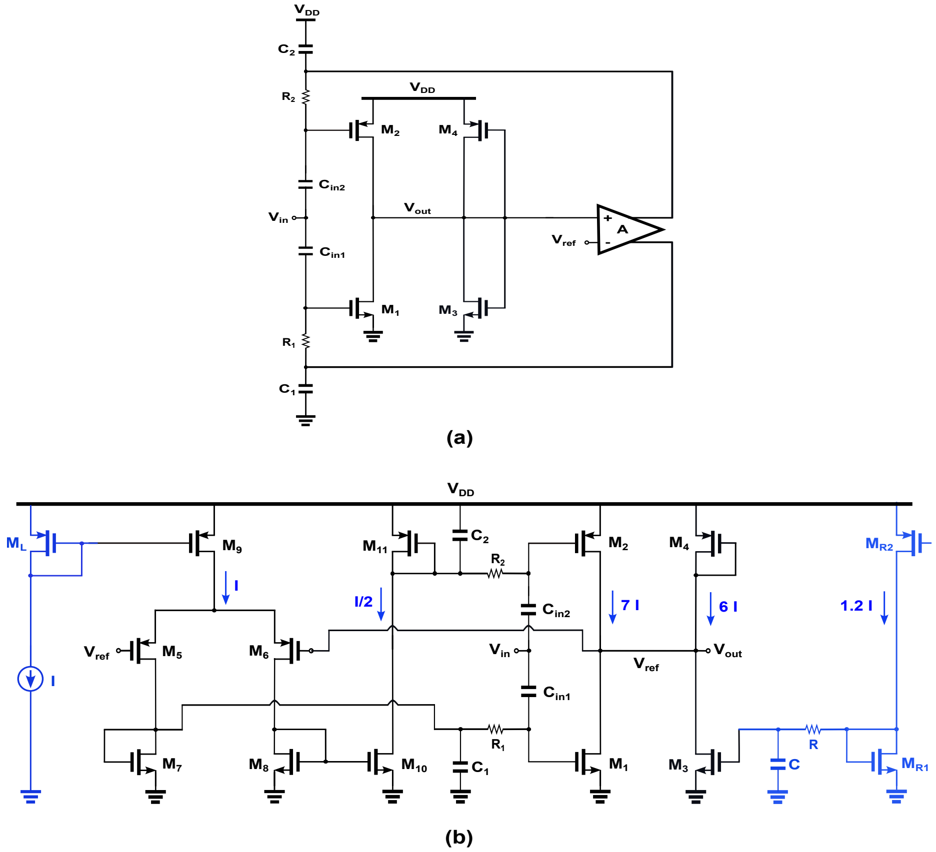


Figure 3.13: Transistor-level schematic of the proposed Low Noise Amplifier (LNA).

The voltage gain A_v is configured at 18 dB to accommodate the maximum expected input amplitude from the transducer.

Thanks to the relatively small input signal, the LNA maintains high linearity. Specifically, the second harmonic distortion (HD2) must remain below −30 dB in the worst-case scenario to ensure high-quality digital imaging. During the TX phase, most RX channels are powered down to conserve energy, so the LNA must be capable of powering up quickly. As the first echoes return approximately 500 ns after the TX pulse ends, the RX chain—including the LNA—must become fully operational within this brief interval. A buffer stage follows the LNA.

A known limitation of inverter-based single-ended OTAs is their low power supply rejection ratio (PSRR). Given the LNA's proximity to high-frequency digital blocks, such as those used for beamforming, significant supply noise may couple through power and ground lines. To address this issue, an on-chip LDO is included to improve PSRR.

In this implementation, the LNA achieves a PSRR of approximately 2. To stabilize the 1.8-V RX supply rail, the LDO derives its input from two sources: a 1.2 V and a 3.3 V off-chip power supplies.

3.3.2 Simulation Results of the LNA Block

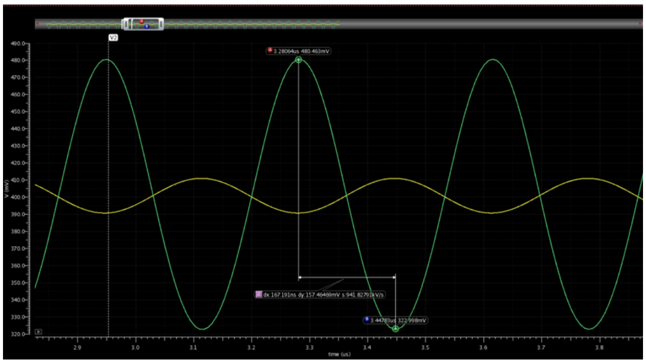


Figure 3.14: Input voltage (yellow) and output voltage (green) of the LNA.

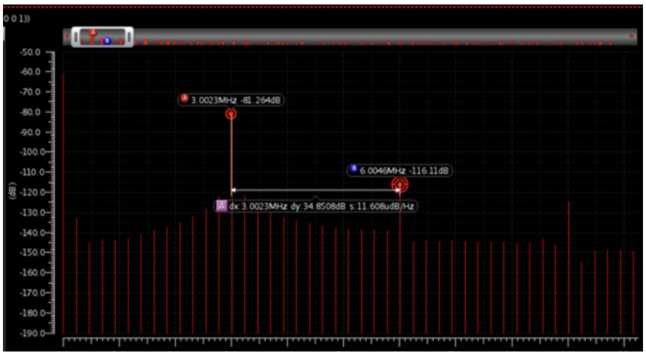


Figure 3.15: Obtained HD2 equal to −34 dB for 20 mV$_{\text{pp}}$ input signal.

This section discusses the simulation results pertaining to the LNA block. Figure 3. 14 depicts the LNA input voltage (yellow) and output voltage (green). The LNA demonstrates second harmonic distortion levels of −34 dB (see Fig. 3. 15) and −40 dB (see Fig. 3. 16) when driven with input signal

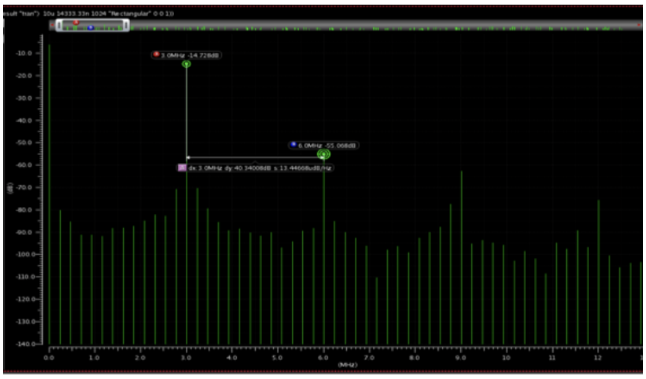


Figure 3.16: Obtained HD2 equal to −40 dB for 10 $\mathrm{mV_{pp}}$ input signal.

amplitudes of 20 $\mathrm{mV_{pp}}$ and 10 $\mathrm{mV_{pp}}$, respectively. These values indicate satisfactory linearity performance under varying input conditions.

The amplifier achieves a voltage gain of 18 dB, which is appropriate for amplifying low-level signals in the target application. Furthermore, the input-referred noise is measured at 7.7 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$, confirming the LNA's capability to maintain low noise performance as depicted in Fig. 3.17.

The circuit operates from a 1.8 V power supply, which is regulated and delivered by the integrated LDO. The design and performance analysis of the LDO block are presented in the following section.

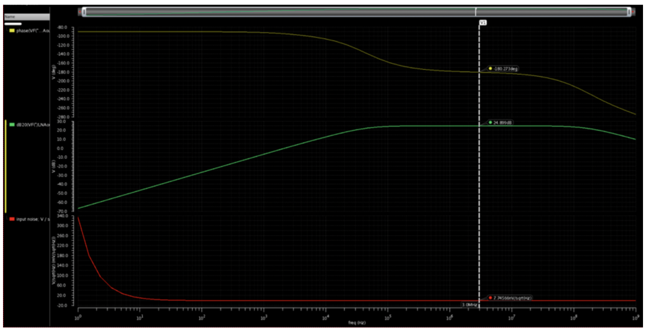


Figure 3.17: Obtained LNA gain, phase, and the input referred noise.

3.4 LDO

Linear voltage regulators can be broadly classified into two main categories: reference regulators and LDO regulators. Both types operate by allowing continuous power transfer from the input supply to the load, with the pass element functioning within its linear region to regulate current flow.

Additionally, linear regulators can be divided into series and shunt configurations. A series regulator employs an active device—most commonly a transistor—placed in series between the input supply and the load. When appropriately controlled, the transistor acts as a variable resistor, dynamically adjusting its resistance to maintain a stable output voltage. On the other hand, shunt regulators utilize a regulating component, such as a Zener diode or a transistor, connected in parallel with the load. In these configurations, the Zener diode helps to stabilize the voltage across the load by shunting excess current. However, significant power dissipation can occur in the series resistor (R_s), particularly at high load currents, reducing overall efficiency.

In most linear regulators, the fundamental architecture includes a pass transistor—which may be of NMOS, PMOS, or bipolar (NPN or PNP) type—integrated into a negative feedback loop. The output voltage is continuously monitored through a voltage divider network and compared against a stable reference voltage (V_{REF}) using an error amplifier. The amplifier then adjusts the control signal (either the gate or base voltage) of the pass element to ensure that the output remains at the desired level. This feedback mechanism enables the regulator to respond effectively to changes in input voltage or load conditions.

The majority of power loss in a linear regulator occurs across the pass element due to its operation in the linear region. In contrast, the current consumed by auxiliary components such as the error amplifier and the resistive feedback network is typically negligible. The total power dissipated can be approximated using the following relation:

$$P_{\text{diss,linear}} = I_{\text{load}} \cdot (V_{\text{in}} - V_{\text{out}}) \tag{3.4}$$

This expression highlights that power loss scales linearly with both the load current and the voltage differential between the input and output.

LDO regulators are particularly advantageous in light-load scenarios due to their inherently low quiescent current, which is usually much lower than that of switching regulators. They are also suitable for low dropout applications, where the input voltage is only slightly higher than the desired output voltage. Regulators designed to operate with a voltage differential of less than 1,V between input and output are classified as LDO regulators.

When compared to DC-DC switching regulators, LDOs offer several key benefits. First, they require fewer external components, resulting in a lower bill of materials (BoM) and reduced overall circuit footprint. For applications involving very light loads and minimal input-output voltage differences, LDOs can achieve efficiencies comparable to or exceeding those of their switching counterparts. Furthermore, LDOs generate minimal electrical noise, as they lack the high-frequency switching associated with DC-DC converters, thereby providing a clean, ripple-free output voltage. From a design perspective, many commercial LDOs come in compact, low-pin-count packages—often with only three pins—simplifying their integration into electronic systems.

In essence, the operation of an LDO relies on a pass element that behaves as a controlled resistor. The input voltage is dropped across this element to produce the desired output voltage. A control loop monitors the output and adjusts the pass element's resistance in real-time via the error amplifier, ensuring tight regulation even as supply voltage or load demand fluctuates. This approach allows LDOs to deliver consistent performance in a wide range of applications requiring stable, low-noise voltage regulation.

The LDO is depicted in Figure 3.14: it represents the most compact circuit capable of providing a clean supply to the RX chain, using a simple single-stage operational amplifier as an error amplifier. It is optimized for size and power consumption, featuring a PMOS transistor as the pass element for stability reasons. The LDO can either be shared among a group of AFEs or dedicated to each individual channel. In the first demonstrator, we chose to share a single regulator among 32 channels, which required scaling the pass transistor size by a factor of eight. The compensation capacitor of the regulator, equal to 20 nF, is placed off-chip. Consequently, using a single LDO for 32 channels (i.e., 32 LNAs) results in an output voltage of 1.778 V and an output current of 816 μA. In this project, since the designed chip includes four channels, a single LDO serving these four channels delivers an output voltage of 1.796 V and an output current of 334 μA, thereby significantly reducing power consumption.

3.5 Cable Driver (CD)

Voltage followers are essential building blocks in analog circuit design, used to replicate a voltage from a high-impedance input to a low-impedance output. Key design goals include low-voltage operation, power efficiency, and fast settling performance. However, traditional class A followers suffer from a trade-off between slew rate and power consumption due to limitations imposed by fixed bias currents.

To address these limitations, class AB followers are employed. These provide low quiescent currents for reduced static power consumption and dynamically increase current during large signal transitions, enhancing slew rate. This

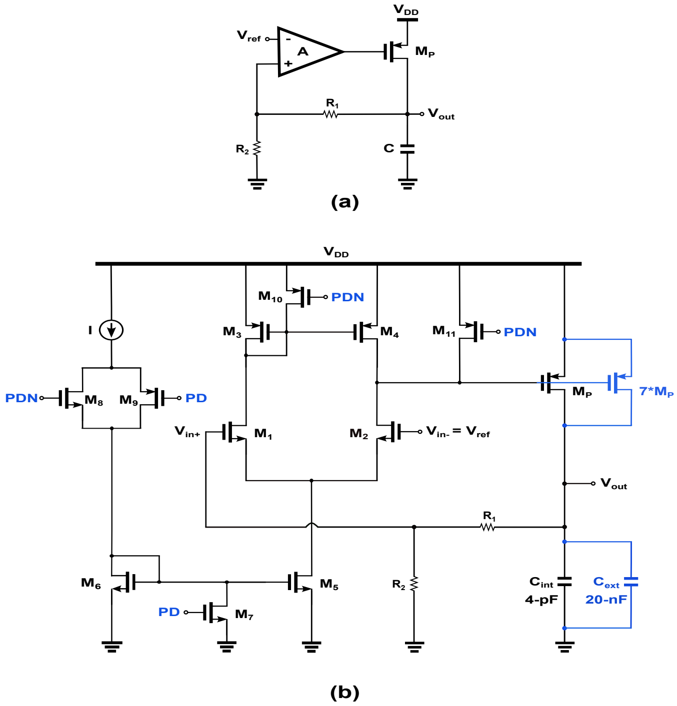


Figure 3.18: (a) Block diagram and (b) transistor level structure of the LDO

behavior is characterized by the *Current Boosting Factor (CBF)*, defined as $CBF = I_{\text{out,MAX}}/I_{\text{BIAS}}$.

Despite improvements, many class AB designs face challenges such as sensitivity of quiescent current to supply voltage and process variations, increased area and power from additional circuitry, and degraded settling due to added parasitic capacitances.

Another crucial metric is *Current Efficiency (CE)*, defined as $CE = I_{\text{out,MAX}}/I_{\text{supply}}$, which ensures effective power usage during both static and dynamic operation. High CE values (ideally close to 1) are achievable when large output currents are generated directly at the output stage.

This thesis presents five class AB voltage followers, derived from the well-known Super Source Follower (SSF), combining high accuracy, low output impedance, high CBF and CE, low-voltage operation, minimal quiescent power, and wide input range, along with precise quiescent current control [174].

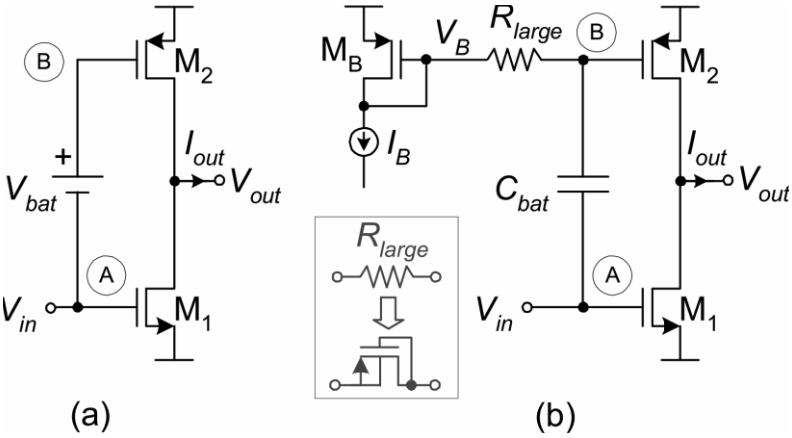


Figure 3.19: (a) Basic class AB stage using floating battery (b) Implementation of battery using QFG transistor [174].

3.5.1 Quasi-Floating Gate Transistors for Class AB Operation

An efficient approach for achieving class AB behavior with low power consumption is the use of *Quasi-Floating Gate (QFG)* transistors (Fig. 3.15). Traditional class AB output stages employ a floating battery or DC level shift (e.g., using diode-connected transistors or resistor-biased currents) to transfer signal variations from node A to node B with a DC offset V_{bat} (Fig. 3.15(a)). However, these implementations often suffer from extra quiescent power consumption, increased supply voltage requirements, poor accuracy due to process and temperature variations, and added parasitic capacitances which degrade speed.

The QFG-based solution (Fig. 3.15(b)) avoids these drawbacks by weakly connecting the gate of the output transistor (node B) to a DC bias voltage V_B through a very large resistance R_{large}, forming a high-pass filter with cutoff frequency:

$$f_c = \frac{1}{2\pi R_{\text{large}} C_{\text{bat}}} \tag{3.5}$$

This filter ensures that only AC (dynamic) variations at node A are passed to node B, while DC components are blocked, enabling high dynamic current capabilities with minimal static power draw.

Key advantages of this implementation include:

- **Accurate Quiescent Current**: Set precisely by a bias current I_B

through a current mirror, independent of process, temperature, and supply variations.

- **Low Cutoff Frequency**: Achieved by employing R_{large} in the GΩ range, resulting in $f_c < 1$ Hz.
- **Compact Implementation**: R_{large} can be realized using a minimum-size diode-connected MOSFET in cutoff, while C_{bat} can be small due to parasitic capacitance at node B.
- **No Extra Power or Voltage Requirements**: Unlike other level shifters, the QFG stage consumes no additional quiescent power and does not increase supply demands.

Thus, QFG transistors offer a compact, robust, and power-efficient means to implement class AB voltage followers or output stages [174].

3.5.2 Class AB Super Source Followers

Conventional MOS source followers (Fig. 3.16(a)) suffer from poor voltage transfer accuracy, limited by the dependency of transistor current on the input voltage. Their small-signal voltage gain is less than unity and output resistance is typically in the kΩ range. These limitations worsen if higher transconductance (g_m) is required, which demands larger bias currents and wider transistors. Moreover, conventional followers are class A circuits, with the maximum sourcing current limited to the bias current I_B, thus restricting the positive slew rate to:

$$SR_+ = \frac{I_B}{C_L} \tag{3.6}$$

where C_L is the load capacitance.

An improved version, known as the *super source follower* (Fig. 3.16(b)), introduces negative feedback through an additional transistor. This design maintains a constant bias current in the main transistor, achieving near-unity gain and significantly reduced output resistance. However, it still operates in class A and cannot deliver currents beyond I_B.

To overcome these limitations, a Class AB variant (Fig. 3.16(c)) incorporates a QFG) technique. A large positive swing at the input leads to a negative swing on the gate of the feedback transistor, translated via a coupling capacitor C_{bat} to increase current in the output stage beyond the quiescent level. This allows the follower to operate in class AB while maintaining the same

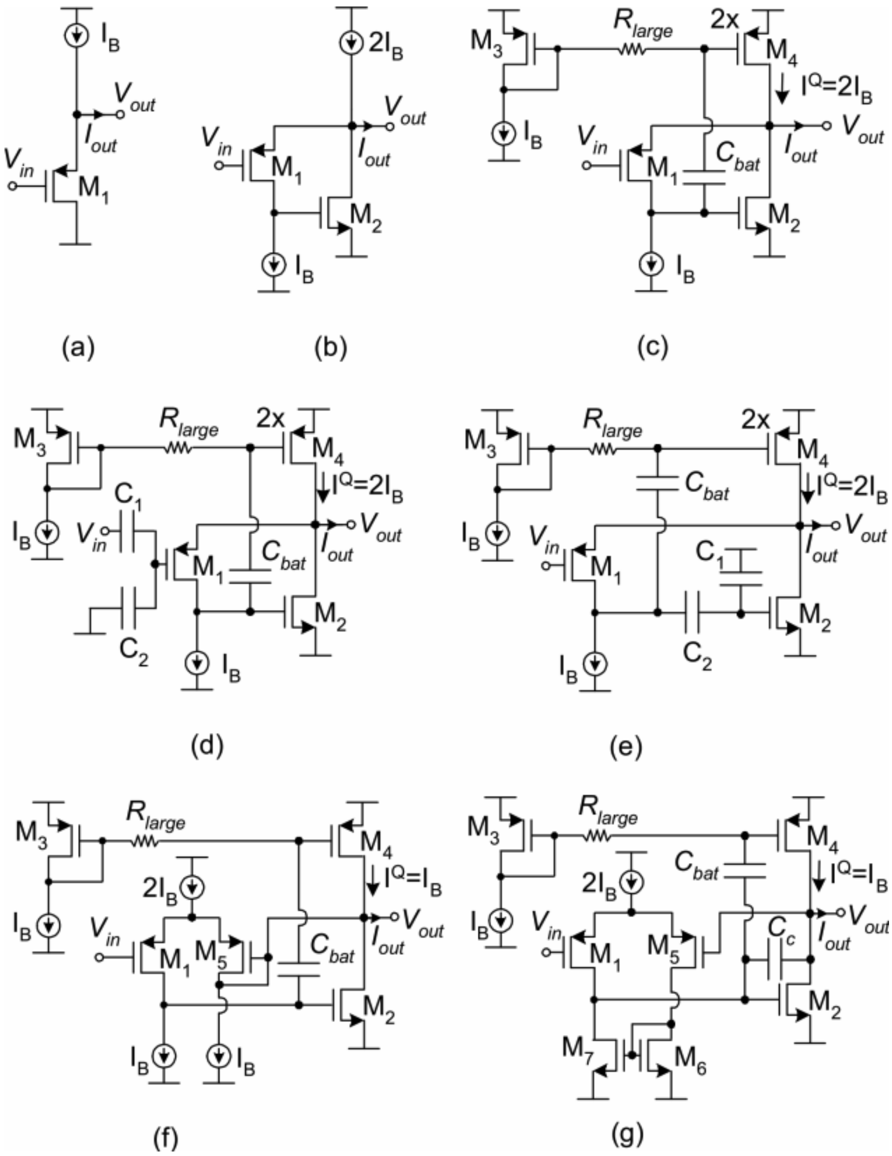


Figure 3.20: (a) Class A source follower (b) Class A super follower (c) Class AB super follower (d) Rail-to-rail class AB super follower (e) Modified class AB super follower (f) with DC compensation (g) Alternative DC compensation [174].

quiescent power and supply voltage requirements as class A designs. Moreover, this configuration also improves current sinking capability during large-signal operation [174].

To expand the input range and enable rail-to-rail operation, a floating-gate MOS (FGMOS) transistor with capacitive voltage division (Fig. 3.16(d)) is used. The input voltage is attenuated and DC-shifted, enabling proper biasing over the entire input swing. The voltage at the gate of the input transistor is given by:

$$V_G = \frac{C_1 V_{\text{in}} + C_2 V_{SS}}{C_1 + C_2} \tag{3.7}$$

Here, the attenuation improves linearity but also increases input-referred noise. this current source voltage in (Figs. 3.16(e)) is:

$$V_{IB} = \left(1 + \frac{C_1}{C_2}\right) V_{GS2} - \frac{C_1}{C_2}(V_{DD} - V_{SS}) \tag{3.8}$$

Several advanced variations of the class AB source follower architecture have been proposed to enhance voltage swing capability and mitigate input-output DC level mismatches. In particular, the configurations illustrated in Figures 3.16(e) through 3.16(g) address these challenges with increasing sophistication. For example, the circuit in Figure 3.16(f) introduces a diode-connected transistor to cancel the DC offset between the input and output, thus improving the accuracy of voltage tracking. Further refinement is achieved in Figure 3.16(g), where the conventional input transistor is replaced with a differential pair. This modification not only enhances matching and symmetry but also eliminates the DC level shift, making it especially beneficial for low-voltage operation and applications involving significant capacitive loading.

Owing to these advantages, the topology shown in Figure 3.16(g) has been selected as the basis for the cable driver architecture in this thesis. This choice is driven by its superior performance in terms of linearity, voltage swing, and signal integrity. Furthermore, the design has been tailored to meet the specific requirements of the custom ASIC developed herein. Notably, each sub-array in the system must drive a micro-coaxial cable with a load capacitance of up to 160 pF, necessitating a driver that can deliver large dynamic currents while maintaining power efficiency.

To fulfill this requirement, a class AB super source follower topology, depicted in Figure 3.17, has been adopted. This configuration is well-suited for driving large capacitive loads due to its ability to both source and sink current levels significantly beyond its quiescent bias, thanks to its intrinsic current-boosting mechanism. As a result, it enables fast signal transitions and high slew rates without incurring the high static power consumption typical of class A designs. To further optimize power efficiency and ensure thermal and process stability, a DC feedback loop is incorporated to precisely control the output quiescent current.

Importantly, the noise contribution of the cable driver, when referred back to the input of the analog signal chain, remains negligible. This is because the driver stage follows the LNA, and its noise is effectively suppressed by the gain of the preceding stages. Consequently, the chosen architecture provides a power-efficient, low-noise, and high-performance solution for cable driving in high-capacitance, mixed-signal ASIC applications.

Figure 3.17(a) illustrates the general block diagram of the proposed buffer architecture. The topology is based on a class AB super source follower structure, enhanced through the integration of Quasi-Floating Gate (QFG) elements—specifically, the capacitor C_{bat} and the large resistor R_{large}. Additionally, an op-amp is employed as a DC control loop, ensuring that the output quiescent current remains well-regulated across the variations.

The final implementation of the cable driver circuit is shown in Figure 3.17(b). In this design, local current mirroring is utilized to replicate and distribute the bias current efficiently throughout the circuit. A Miller compensation capacitor C_c is introduced to enhance frequency stability and ensure robust phase margin in the presence of large capacitive loads. Moreover, the high-value resistor R_{large}—critical for QFG operation—is realized using a minimum-size MOS transistor (denoted as M_9) operating in the subthreshold cutoff region. This approach not only achieves the desired gigaohm-range resistance but also contributes to a compact layout.

3.5.3 Evaluated Specifications of the Cable Driver

The performance of the cable driver was assessed by analyzing its input and output voltage waveforms. The results depicted in Fig. 3. 22 show a strong correspondence between the input and output, demonstrating effective voltage buffering and minimal signal distortion. This indicates that the buffer is capable of preserving signal integrity during transmission.

To further evaluate the robustness of the buffer design under process variations, a set of Monte Carlo simulations was performed, focusing on the output quiescent current. As illustrated in Fig. 3. 23, the statistical outcomes revealed a mean current of 37.59 μA, with the current values ranging from a minimum of 24 μA to a maximum of 46 μA. The standard deviation was found to be 3.28 μA, highlighting consistent performance and limited sensitivity to manufacturing variability.

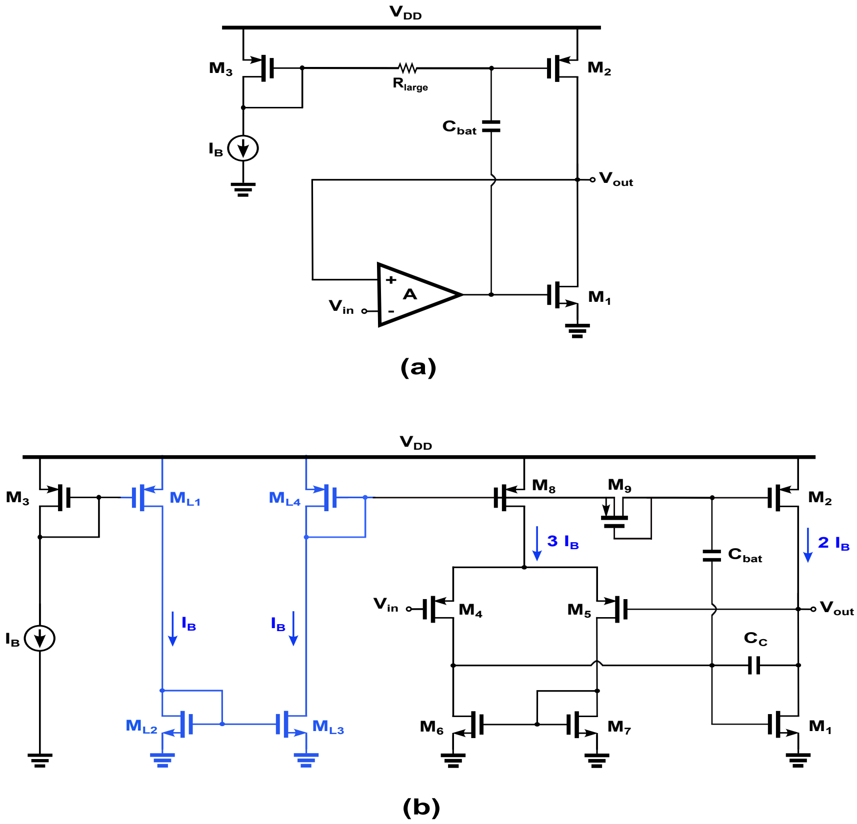


Figure 3.21: (a) Block diagram and (b) transistor level structure of the buffer.

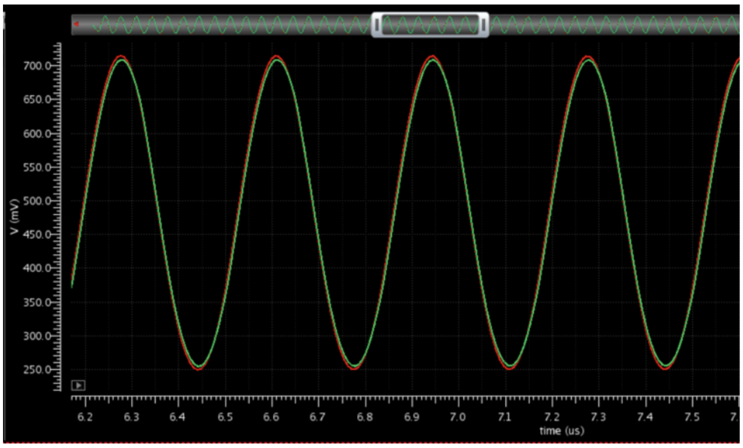


Figure 3.22: Input (red) and output (green) voltages of the Cable Driver.

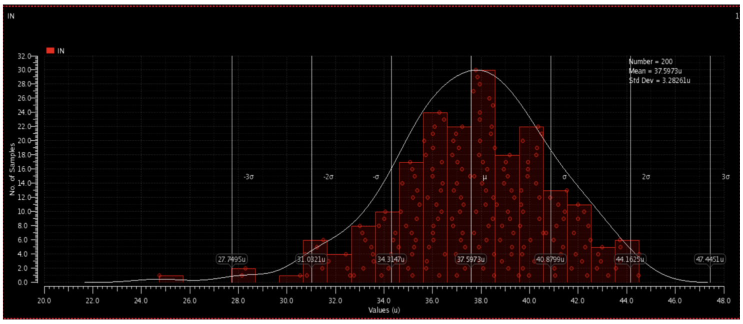


Figure 3.23: Monte Carlo simulation results for the buffer's output quiescent current.

3.6 Current Generator (CG)

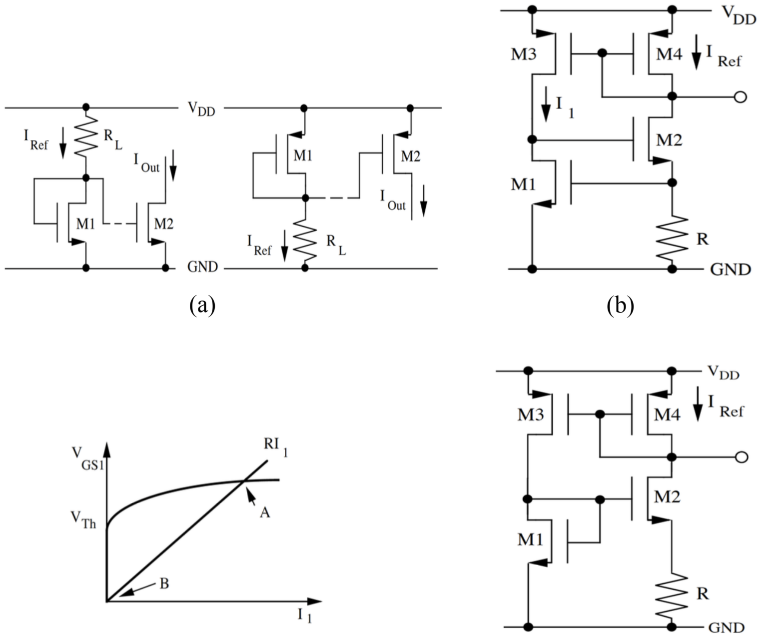
A fundamental requirement in most analog and mixed-signal integrated circuits is the availability of a stable and accurate reference current, which can be mirrored and distributed to various functional blocks within the system. The simplest and most intuitive method to generate such a reference current, as shown in Fig. 3.20(a), is to apply Ohm's Law, using a resistor to define the current as:

$$I_{\mathrm{ref}} = \frac{V_{\mathrm{DD}} - V_{\mathrm{GS1}}}{R_L} \tag{3.9}$$

However, this approach suffers from significant limitations in terms of accuracy and robustness. The output current is highly sensitive to both process variations in the resistor value and fluctuations in the supply voltage V_{DD}. In practice, this leads to a typical inaccuracy in the range of 30%, which is unacceptable for precision analog applications. Moreover, supply ripple and spur interference can further degrade the reliability of such a current source, making it unsuitable for noise-sensitive designs.

To achieve more precise and predictable current references, a variety of improved circuit topologies have been developed. These include: Self-biased current references, Self-biased micro-current generators, V_{BE}-based current references, and V_T-based current references.

Each of these techniques offers enhanced control over temperature dependence, supply insensitivity, and matching behavior. In particular, self-biased current references are notable for their ability to establish a stable operating point autonomously, often requiring an auxiliary start-up circuit to ensure that the circuit does not remain in a trivial (zero-current) state [175].



(a) (b) (c) (d)

Figure 3.24: Schematics showing: (a) a basic current source, (b) a self-biased current reference, (c) its two possible DC operating points, and (d) a self-biased μ-current generator [175].

For instance, in self-biased current generators employing matched transistor pairs (M_3 and M_4 in Fig. 3.20(b)), a stable current can be maintained by ensuring that the two devices share identical aspect ratios and thermal environments. The current mirror configuration guarantees equal current flow through both branches, assuming ideal matching.

These circuits typically exhibit two possible DC operating points—one corresponding to the desired bias current, and the other to a zero-current state (Fig. 3.20(c)). To enforce the correct bias point, a start-up mechanism is required. This auxiliary circuit injects a small perturbation during power-up to drive the system into the intended state.

When designing for current levels in the range of 100 µA, a supply voltage on the order of 1 V combined with a resistance of approximately 10 kΩ can achieve the desired current. Such resistor values are easily implementable in modern CMOS processes without excessive area consumption.

However, for ultra-low-power applications requiring currents in the microampere range, the above approach would necessitate extremely large resistors, leading to prohibitive silicon area usage. To mitigate this, an alternative method is to reduce the voltage drop across the resistor by leveraging the difference in overdrive voltages between two transistors (see Fig. 3.20(d)). Specifically, the resistor voltage is expressed as:

$$V_R = V_{\mathrm{OV1}} - V_{\mathrm{OV2}} = (V_{\mathrm{GS1}} - V_{\mathrm{th1}}) - (V_{\mathrm{GS2}} - V_{\mathrm{th2}}) \tag{3.10}$$

This leads to a system of two equations with two unknowns, which can be solved either algebraically or graphically to determine the stable bias point. In these designs, the aspect ratio of the transistors is carefully selected to ensure a suitable voltage difference across the resistor, facilitating accurate current definition even at low voltage drops [175].

For instance, the condition:

$$\left(\frac{W}{L}\right)_2 = k\left(\frac{W}{L}\right)_1 \tag{3.11}$$

ensures that the overdrive voltage of M_1 remains sufficiently higher than that of M_2, allowing a non-zero current to develop across the resistor. As always, a start-up circuit remains essential to initiate proper circuit operation, preventing the system from stabilizing at the zero-current solution.

In conclusion, while simple resistive biasing methods may suffice for non-critical applications, advanced current reference schemes provide the necessary performance and stability for high-precision, low-power, and temperature-resilient analog circuit designs.

Figure 3.21 presents the schematic of a designed 10-µA self-biased micro-current generator. The fundamental principle behind this circuit lies in the voltage developed across the resistor R_1, which is not simply a single (V_{gs}), but rather the difference between the V_{gs} values—or, more precisely, the overdrive voltages—of transistors M_1 and M_2. This differential voltage enables accurate current definition without dependency on absolute threshold voltage values.

The transistors M_3 and M_4 are designed to be perfectly matched and are arranged to carry identical currents, thereby ensuring a symmetrical and stable biasing condition. This symmetry plays a crucial role in the self-biasing mechanism, allowing the circuit to stabilize to a desired operating point.

However, self-biased current generators often exhibit two possible DC operating states: one being the correct biased condition and the other being a zero-current or "off" state. To guarantee that the circuit does not remain in this undesirable zero-current condition, a start-up circuit is essential. The start-up mechanism actively monitors the circuit during power-up and, if necessary, injects a small current at a suitable node to push the system out of the

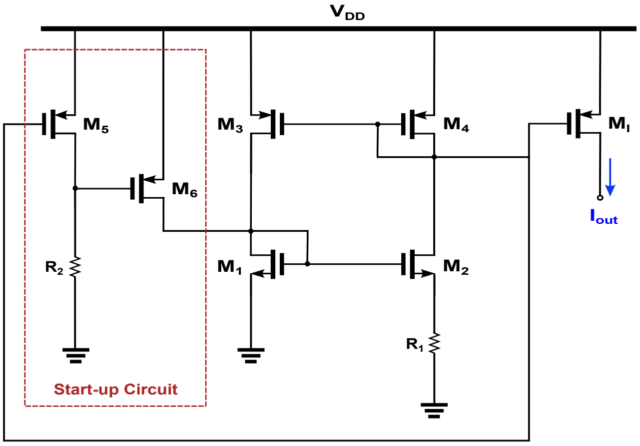


Figure 3.25: Schematic of the current generator and it's start-up circuits

zero-current state and into its intended operating region.

In the implemented design, the start-up functionality is realized through the inclusion of components R_2, M_5, and M_6. These elements form a robust start-up network that ensures reliable initialization across process, voltage, and temperature variations.

For the architecture developed in this project, a dedicated self-biased current generator is implemented for each individual channel. This approach ensures localized biasing and greater immunity to cross-channel interference, thereby contributing to improved performance consistency and noise isolation across the multi-channel analog front-end system.

3.7 Evaluated features of the complete RX chain

This section presents a comprehensive evaluation of the complete RX chain based on simulation results. Figures 3.26 and 3.27 illustrate voltage waveforms at various key nodes in the circuit, including the clock signal (CK), the input from the CMUT, gate and source voltages (V_g and V_s) of the main TX/RX switch, the input and output of the LNA, the output of the cable driver (V_{out}), the LDO output, the main supply voltage ($V_{DD} = 3.3$ V), and the reference voltage ($V_{ref} = 400$ mV). These results confirm the circuit's functional correctness and stable operation across all critical points.

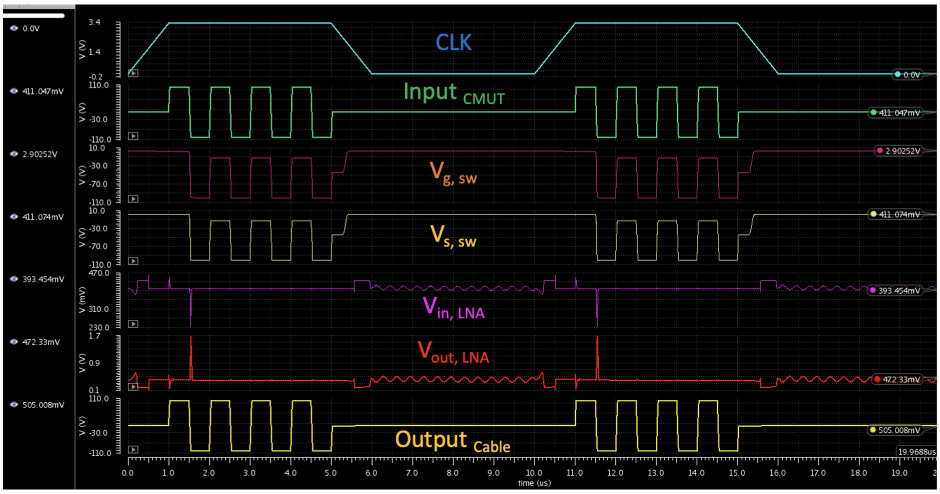


Figure 3.26: Simulated voltage waveforms of the clock signal (CLK), input signal from the CMUT, the gate and source voltages (V_g and V_s) of the main TX/RX switch, the input and output of the LNA, and the cable driver output.

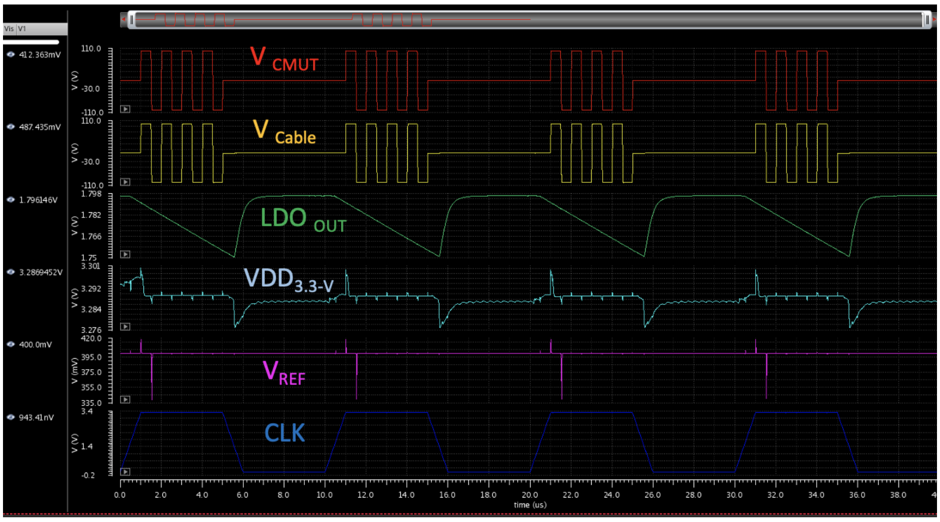


Figure 3.27: Simulated voltage waveforms of the input and output of the chain, LDO output voltage, supply voltage (V_DD = 3.3 V), and reference voltage (V_ref = 400 mV).

In terms of noise analysis, Figure 3.28 breaks down the input-referred noise contributions from individual blocks: the first TX/RX switch contributes

6.86 nV/$\sqrt{\text{Hz}}$, the LNA contributes 7.7 nV/$\sqrt{\text{Hz}}$, the cable driver contributes 14.4 nV/$\sqrt{\text{Hz}}$, and the second TX/RX switch contributes 1.3 nV/$\sqrt{\text{Hz}}$. As shown in Figure 3.29, the combined input-referred noise of the RX chain at the CMUT input is 12.27 nV/$\sqrt{\text{Hz}}$.

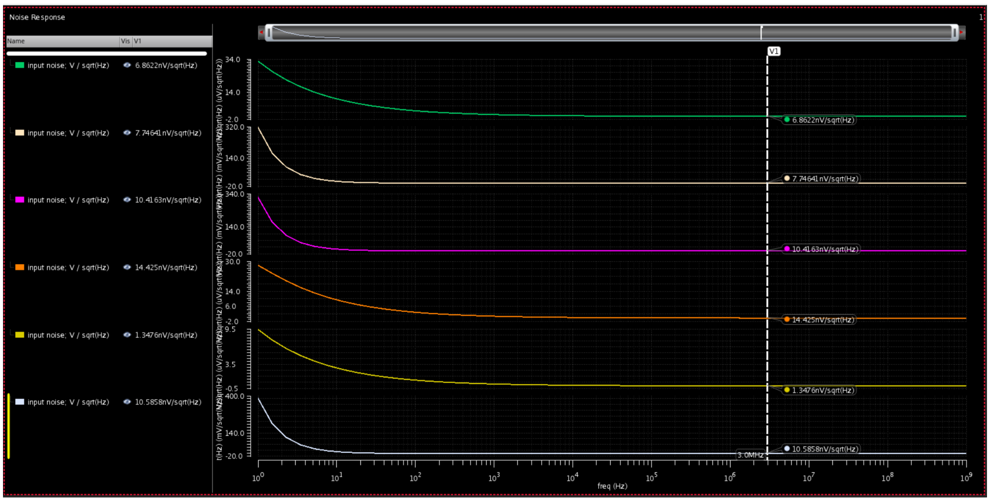


Figure 3.28: Input-referred noise of individual circuit blocks in the RX chain.

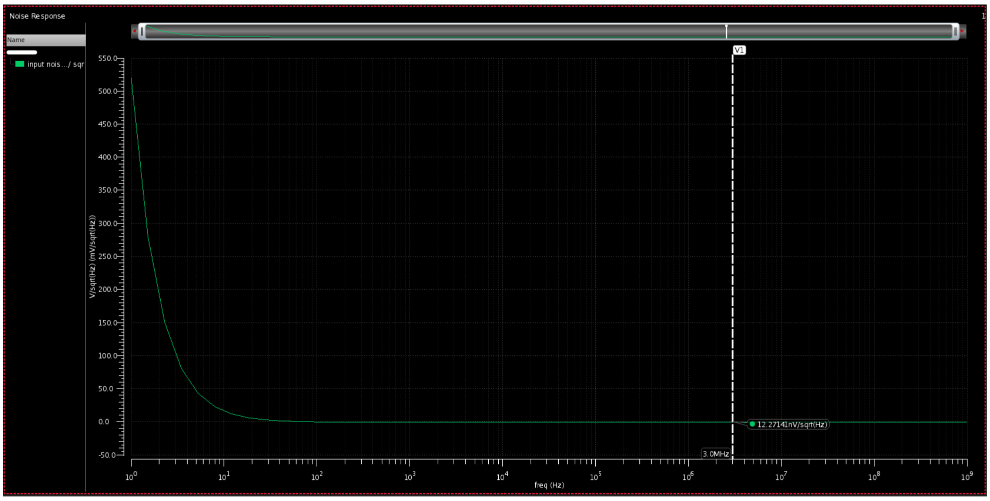


Figure 3.29: Overall input-referred noise of the complete RX chain.

The system's power consumption is distributed across the individual circuit blocks, with a detailed breakdown provided in Figure 3.30, enabling an assessment of power efficiency. Finally, Table 3.2 summarizes all the critical design specifications and key performance parameters of the complete RX chain.

As shown in Table 3.2, the LNA provides a voltage gain of 18,dB and exhibits an input-referred noise of $7.7\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$, playing a key role in determining the overall noise performance of the RX chain. The total input-referred noise of the RX chain, measured at the CMUT interface, is $12.27\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$, which includes contributions from the TX/RX switches, LNA, and buffer stages. The HD2 of the LNA is measured to be $-34\,\mathrm{dB}$, and improves to $-40\,\mathrm{dB}$ when driven with a 10 mV peak-to-peak input signal, demonstrating its linearity for small-signal operation. Furthermore, the system exhibits low inter-channel interference, with crosstalk levels measured at $-38\,\mathrm{dB}$. This indicates effective isolation between adjacent receive paths, which is critical in multi-channel ultrasound systems to ensure signal integrity and prevent degradation of image quality due to leakage or coupling effects.

The reference voltage (V_{ref}) used across analog blocks such as bias generators is set to 400 mV. The LDO provides a stable 1.796 V output, which is shared among four parallel RX channels, optimizing power efficiency. The TX/RX switch exhibits excellent isolation in the receive mode, with an off-isolation of $-42\,\mathrm{dB}$ at 3 MHz operation frequency. It also supports fast mode transition, with a TX-to-RX switching time of $1\,\mu\mathrm{s}$, ensuring minimal signal loss during duplexing.

The total power consumption of the RX chain is 20.13 mW, corresponding to less than 5 mW per channel. This power budget includes all signal-conditioning blocks from the front-end switch to the cable driver. The overall chip area dedicated to the RX chain is approximately $1.4 \times 1.4\,\mathrm{mm}$, yielding a total footprint of $2\,\mathrm{mm}^2$, which aligns with the area constraints of multichannel ultrasound systems.

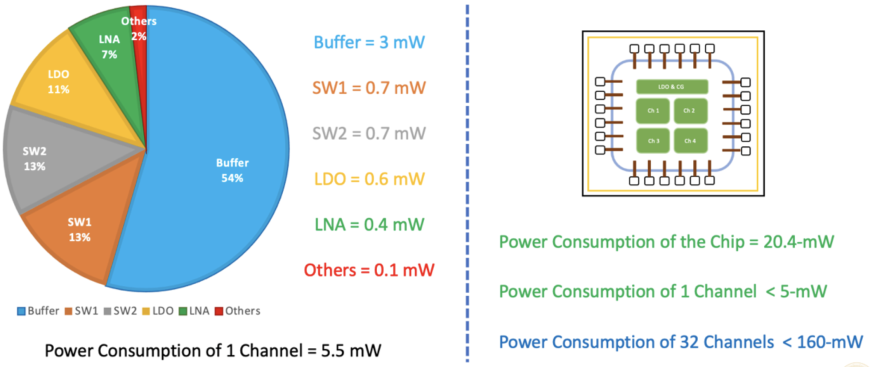


Figure 3.30: Comprehensive breakdown of power consumption across individual circuit blocks, highlighting the power efficiency of the RX chain, the 4-channel test chip, and the final 32-channel version.

Table 3.2: RX-chain performance specifications

Parameter	**Value**
Technology	160 nm BCD8-SOI
Power Supply	3.3 V
LNA Gain	18 dB
LNA Input-Referred Noise	$7.7\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$
LNA Supply Voltage	1.8 V
RX Chain Input-Referred Noise	$12.27\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$
Second Harmonic Distortion (HD2)	−34 dB (−40 dB @ 10 mV input)
Crosstalk	−38 dB
Reference Voltage (V_{ref} / V_{cm})	400 mV
LDO Output Voltage	1.796 V (shared across 4 channels)
TX/RX Switch Off-Isolation	−42 dB @ 3 MHz
TX-to-RX Switching Time	1 μs
Power Consumption	20.13 mW (<5 mW/channel)
Chip Area	1.4 mm × 1.4 mm (Total = 2 mm^2)

Chapter 4

Layout, PCB, and Experimental Characterization

4.1 Layout Implementation

The custom ASIC was implemented in a 160-nm BCD-SOI technology node, featuring both LV and HV devices to support the full functionality of the integrated circuit. The final layout was optimized for parasitic minimization and channel symmetry, ensuring matched performance among the four front-end channels. Each channel includes the TX/RX switch, an LNA, a shared LDO regulator, and the output CD which also operates as a buffer.

Special care was taken to separate the analog and digital domains through guard rings and dedicated supply routing to mitigate substrate noise coupling. The on-chip LDO and its CG provide a stable bias network for all analog blocks. The resulting layout area for one channel is 375 μm $\times$ 365 μm, while the LDO and CG occupy 105 μm $\times$ 290 μm, leading to a total die area of 2 mm^2. The complete layout and annotated die micrograph are illustrated in Fig. 4.1.

4.2 PCB Design for Testing

To validate the ASIC functionality, a two-layer PCB test board was designed to provide appropriate signal interfacing, power regulation, and impedance-matched connections for both electrical and acoustic measurements. The top layer accommodates the ASIC die, wire-bonded to a custom QFN package,

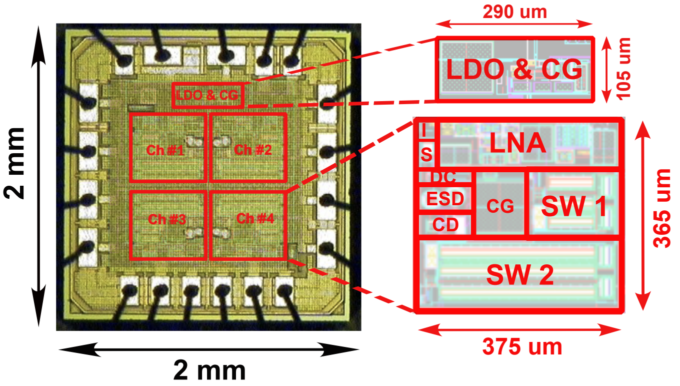


Figure 4.1: (a) Micrograph of the fabricated die in 160-nm BCD-SOI technology showing the four independent channels and the integrated LDO with its current generator. and, (b) Annotated layout of the circuits in one channel and a shared LDO with its current generator .

with local decoupling capacitors placed within 1 cm of each supply pad to minimize supply noise. The total size of the PCB is 11.5 cm × 15.5 cm.

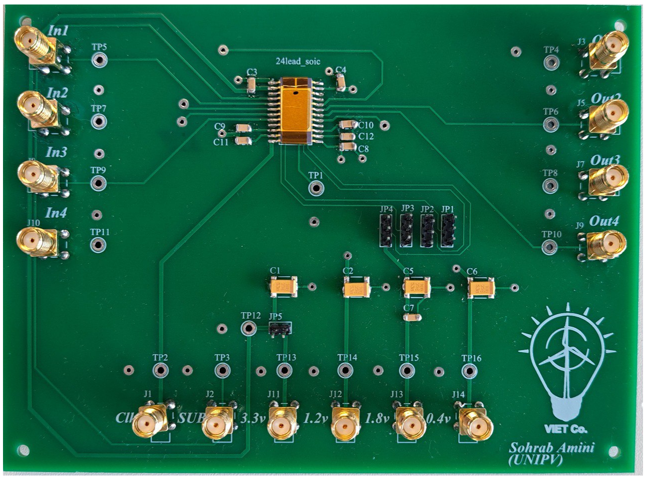


Figure 4.2: Photograph of the custom two-layer PCB designed for ASIC testing.

The inner layers carry ground and supply planes, designed to reduce electromagnetic interference (EMI) and crosstalk between channels. The bottom layer hosts the interface connectors to the external AFE block, and the CMUT array. Careful attention was paid to differential routing, high-voltage trace spacing, and probe pad accessibility to ensure reliable high-voltage operation during testing. The assembled PCB used for the experimental evaluation is shown in Fig. 4.2.

4.3 Measurement Results

The performance of the in-probe ASIC was characterized in both the electrical and acoustic domains.

Fig. 4.3 illustrates the acoustic experimental setup adopted to validate the proposed ASIC in conjunction with a commercial ultrasonic transducer. A single-element SonoMed ultrasonic transducer was employed for the measurements. The transducer was immersed in a water tank and positioned at a short distance from a planar metallic reflector placed at the bottom of the tank, enabling pulse–echo characterization under controlled laboratory conditions. The use of a water tank ensured a homogeneous propagation medium and repeatable acoustic conditions.

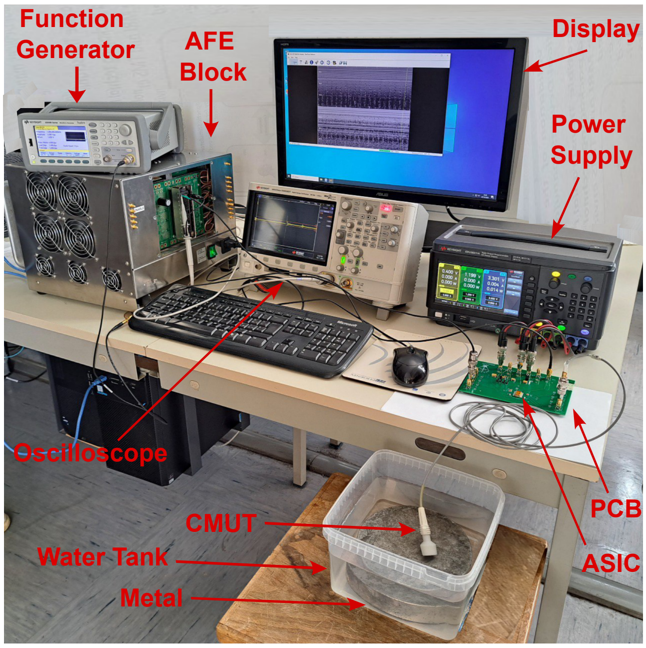


Figure 4.3: Acoustic measurement setup used for CMUT-ASIC characterization in a water tank environment with a single-element SonoMed ultrasonic transducer.

The SonoMed transducer used in this work is specified for operation around a center frequency of approximately 3 MHz, with a nominal fractional bandwidth corresponding to an effective bandwidth of about 2 MHz. Only one transducer element was connected at a time, and each ASIC channel was characterized individually in order to isolate channel-level performance and avoid array-related coupling effects.

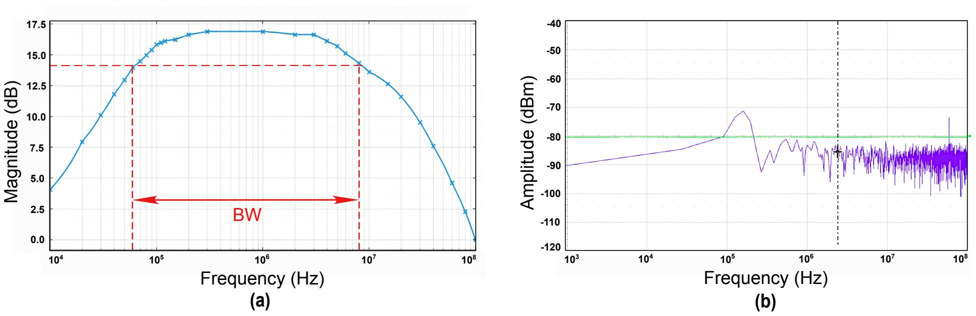
Although the ASIC circuits were designed and simulated to support high-voltage excitation pulses up to 200 $V_{p\text{–}p}$, the experimental measurements were performed using a reduced excitation amplitude of 90 $V_{p\text{–}p}$. This limitation was imposed by the maximum output voltage of the available external analog front-end (AFE) block used to generate the excitation pulses. As a consequence, the transducer was not driven at its maximum acoustic output capability during the experiments, and the reported results should be interpreted accordingly.

In the pulse–echo configuration, the reflected acoustic signal was received by the same transducer element, amplified by the proposed ASIC front-end, and routed back through the same cable to the external AFE for digitization, post-processing, and visualization. This configuration closely resembles a practical single-channel ultrasound front-end and allows evaluation of both electrical and acoustic signal integrity.

The electrical characterization results are reported in Fig. 4.4. The measured small-signal voltage gain is 17 dB, with a –3 dB bandwidth extending from 60 kHz to 8 MHz. While this bandwidth exceeds the nominal bandwidth of the SonoMed transducer (approximately 2 MHz), it demonstrates that the proposed ASIC does not represent a bandwidth bottleneck and is compatible with a wide range of ultrasonic transducers operating in the low- to mid-MHz frequency range. In the present measurements, the effective acoustic bandwidth is primarily limited by the transducer characteristics rather than by the ASIC front-end.

The measured output noise spectrum of a single channel yields an input-referred noise density of 12.2 $\text{nV}/\sqrt{Hz}$ at the transducer resonance frequency of 3 MHz, confirming the low-noise performance of the proposed design when interfaced with a practical ultrasonic load.

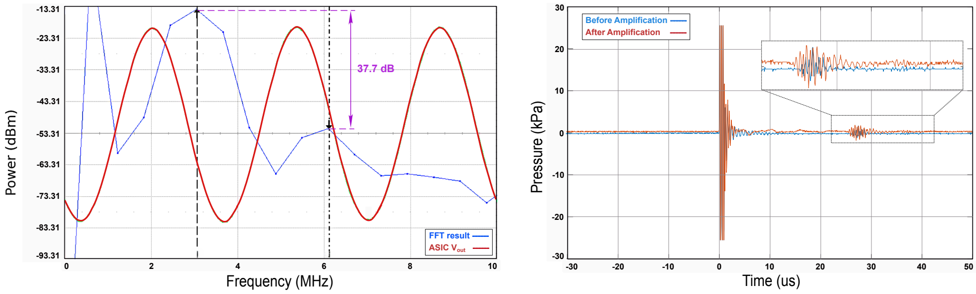
Furthermore, harmonic distortion was evaluated by measuring the second harmonic distortion (HD2), which resulted in a value of –37.7 dB for an input signal amplitude of 20 $mV_{p\text{–}p}$, as shown in Fig. 4.5. The corresponding time-domain waveforms display the excitation signal applied to the transducer and the received echo signal, together with its amplified version at the ASIC output. These results confirm correct acoustic transmission and reception as well as the linear operation of the proposed front-end under the adopted test



(a) **(b)**

Figure 4.4: (a) Measured voltage gain and bandwidth of the proposed ASIC front-end. (b) Measured output noise spectrum showing an input-referred noise density of 12.2 nV/$\sqrt{Hz}$ at 3 MHz.

conditions.



(a) **(b)**

Figure 4.5: (a) Measured HD2 for a 20 mV_{p-p} input signal. (b) Time-domain waveform of the excitation and received echo signals, confirming acoustic functionality.

The measured inter-channel crosstalk was –36 dB, indicating good channel isolation and validating the effectiveness of the layout strategy and power distribution network. It should be noted that the acoustic experiments were conducted using a single-element transducer and a limited excitation voltage. Consequently, array-level effects, such as beamforming performance and imaging depth, were not evaluated in this work. Nevertheless, the reported results demonstrate the suitability of the proposed ASIC architecture for ultrasound front-end applications and provide a solid basis for future system-level integration with multi-element transducer arrays.

Table 3.2 summarizes the performance comparison between the proposed front-end ASIC and state-of-the-art implementations reported in [176–178]. The presented design, fabricated in a 160-nm BCD-SOI process, targets CMUT-based 2-D arrays operating around 3 MHz. The Noise-Efficiency Factor (NEF) is used as a comparative figure of merit, defined as:

$$\mathrm{NEF} = V_{n,\mathrm{in}}\sqrt{P} \tag{4.1}$$

where $V_{n,\mathrm{in}}$ is the input-referred noise density and P is the per-channel power consumption.

In comparison with recent JSSC and ESSCIRC designs implemented in similar HV technologies, this work achieves a superior balance between noise, power, and area. Specifically, the proposed ASIC exhibits an input-referred noise density of 12.2 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at 3 MHz while consuming only 4.9 mW per channel, resulting in the lowest reported NEF of 0.854 $\mathrm{nV}\sqrt{\mathrm{W}}/\sqrt{\mathrm{Hz}}$ among comparable works. Furthermore, the effective receive bandwidth of 8 MHz ensures broad coverage around the CMUT resonance, while maintaining compact integration with a per-channel area of 0.13 mm^2, much smaller than prior designs (0.75–0.9 mm^2).

Table 4.1: Performance Comparison with State-of-the-Art

Parameter (Units)	**JSSC'2020 [176]**	**JSSC'2021 [177]**	**ESSCIRC'2022 [178]**	**This Work**
Technology	180 nm HV-CMOS	180 nm HV-CMOS	165 nm BCD-SOI	**160 nm BCD-SOI**
Transducer Type	CMUT	PZT	PMUT	**CMUT**
Fin [MHz]	40	13	2.5	**3**
RX Bandwidth [MHz]	37.7	20	2-4	**8**
Power/Channel [mW]	25.2	6	5.4	**4.9**
IRN Density [$\mathrm{nV}/\sqrt{\mathrm{Hz}}$]	9.66 @ 40 MHz	14 @ 15 MHz	13 @ 3 MHz	**12.2 @ 3 MHz**
NEF [$\mathrm{nV}\sqrt{\mathrm{W}}/\sqrt{\mathrm{Hz}}$]	1.533	1.084	0.955	**0.854**
Area/Channel [mm^2]	0.75	0.75	0.90	**0.13**

Chapter 5

Conclusions

This work presented the design, implementation, and experimental validation of a custom four-channel front-end ASIC for CMUT-based in-probe imaging systems, fabricated in a 160-nm BCD-SOI technology. The primary objective was to achieve a compact, low-noise, and power-efficient mixed-signal interface capable of operating under the demanding requirements of high-voltage CMUT excitation and broadband acoustic signal reception.

The proposed ASIC integrates four independent receive channels, each comprising two HV TX/RX switches, an LNA, and a class-AB cable driver. A shared on-chip LDO regulator provides a clean 1.8-V supply rail, enabling robust analog performance while maintaining channel-to-channel isolation. The TX/RX switches were designed to handle bipolar excitation pulses up to 200 $V_{p\text{–}p}$ using only a 3.3 V supply, thereby ensuring reliable protection and low leakage in receive mode without the need for external HV biasing.

Electrical characterization confirmed a measured gain of 17 dB and a –3 dB bandwidth from 60 kHz to 8 MHz, demonstrating a wide dynamic range suitable for CMUT arrays operating around 3 MHz. The input-referred noise density was measured at 12.2 $\text{nV}/\sqrt{\text{Hz}}$, resulting in an NEF of 0.854 $\text{nV}\sqrt{\text{W}}/\sqrt{\text{Hz}}$, representing state-of-the-art noise–power performance in this technology class. The HD2 was measured at –37.7 dB for a 20 $\text{m}V_{p\text{–}p}$ input, validating the linearity of the LNA and driver stages. The measured inter-channel crosstalk of –36 dB further confirmed the robustness of the layout, power routing, and isolation strategy.

Acoustic measurements verified the correct operation of each receive path in an experimental water-tank setup, where the CMUT element transmitted and received echo signals from a metallic reflector. The ASIC successfully amplified the weak received echo, maintaining signal fidelity and confirming full acoustic functionality. These results demonstrate that the proposed front-end ASIC can reliably support both transmission and reception phases in CMUT-based imaging systems.

From a system integration standpoint, the chip achieves a total active area of 2 mm^2, corresponding to only 0.13 mm^2 per channel—representing a substantial reduction compared to prior state-of-the-art designs occupying 0.75–0.9 mm^2 per channel. The total power consumption of 20.1 mW (4.9 mW per channel) ensures compatibility with compact probe implementations, where power efficiency and thermal management are critical.

When compared to recent JSSC'21 and ESSCIRC'22 designs, the proposed ASIC demonstrates a superior trade-off among noise, power, and area, validating the effectiveness of the adopted circuit topologies and layout methodologies. The 160-nm BCD-SOI process enabled the integration of high-voltage devices, precision analog components, and on-chip power regulation within a unified die, illustrating the potential of this technology for future scalable ultrasound front-end systems.

In conclusion, this research contributes a fully integrated, low-noise, and area-efficient ASIC solution optimized for CMUT-based imaging applications. The presented architecture establishes a foundation for next-generation miniaturized ultrasound probes and intravascular imaging catheters, where high channel density, low power, and broadband operation are essential. Future work may focus on extending the design toward multi-frequency operation, on-chip digital beamforming, and advanced calibration techniques to further enhance image quality and integration at the probe level.

List of Publications

1. A. Amini, G. Ricotti, P. Malcovati, and E. Bonizzoni, “High-Voltage TX/RX Switches for Efficient Sensor Interfaces Across Various Technologies in Ultrasound Imaging and Beyond: A Review,” *IEEE Access*, vol. 13, pp. 138776–138794, 2025.

2. A. Amini, E. Moisello, P. Malcovati, and E. Bonizzoni, “A High-Voltage TX/RX Switch with 3.3-V Supply for Ultrasound Imaging Front-End ASICs,” in *Proc. IEEE 31st International Conference on Electronics Circuits and Systems (ICECS)*, Nancy, France, 2024.

3. A. Amini and H. N. Kalehsar, “High-Accuracy ECG Signal Acquisition Using a Power-Efficient 6-bit Level-Crossing ADC,” in *Proc. IEEE 32nd International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES)*, Szczecin, Poland, 2025.

4. A. Amini, H. N. Kalehsar, E. Zehtabchi, and K. Javanmardi, “Improving Accuracy of the Current Mirrors for High-Resolution Applications,” in *Proc. IEEE 31st International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES)*, Gdansk, Poland, 2024.

5. K. Javanmardi, A. Amini, and A. Cabrini, “Ultra Low-Power, Area-Efficient Multiplier Based on Shift-and-Add Architecture,” in *Proc. IEEE 29th International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES)*, Wroclaw, Poland, 2022.

Bibliography

[1] H. Azhari, *Basics of Biomedical Ultrasound for Engineers.* Hoboken, NJ, USA: Wiley, 2010.

[2] J. W. Strutt (Lord Rayleigh), *The Theory of Sound*, vol. 1. Cambridge, U.K.: Cambridge University Press, 2011.

[3] P. G. Newman and G. S. Rozycki, "The history of ultrasound," *Surgical Clinics of North America*, vol. 78, no. 2, pp. 179–195, 1998.

[4] J. Woo, "A short history of the development of ultrasound in obstetrics and gynecology," *Ultrasound in Obstetrics & Gynecology*, vol. 3, pp. 1–25, 2002.

[5] I. Donald, J. Macvicar, and T. Brown, "Investigation of abdominal masses by pulsed ultrasound," *The Lancet*, vol. 271, no. 7032, pp. 1188–1195, 1958.

[6] O. Ramm and J. Castellucci, "Real-time 3D ultrasonic data acquisition NSF/ERC unit 2.1 A," in *Proc. 12th Annu. Int. Conf. IEEE Eng. Med. Biol. Soc.*, 1990, pp. 668–669.

[7] J. Poulton, O. Von Ramm, and S. Smith, "Integrated circuits for 3-D medical ultrasound imaging," *MCNC Technical Bulletin*, vol. 3, no. 4, 1987.

[8] I. Ladabaum, X. Jin, H. Soh, A. Atalar, and B. Khuri-Yakub, "Surface micromachined capacitive ultrasonic transducers," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 45, no. 3, pp. 678–690, May 1998.

[9] Jonathan M. Rothberg, *et al.*, "Ultrasound- on-chip platform for medical imaging, analysis, and collective intelligence," *In: Proc. Natl. Acad. Sci. U. S. A.* 118.27, 2021.

[10] Y. Huang, A. Ergun, E. Haeggstrom, M. Badi, and B. Khuri-Yakub, "Fabricating capacitive micromachined ultrasonic transducers with wafer-bonding technology," *J. Microelectromech. Syst.*, vol. 12, no. 2, pp. 128–137, 2003.

[11] O. Oralkan *et al.*, "Capacitive micromachined ultrasonic transducers: Next-generation arrays for acoustic imaging," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 49, no. 11, pp. 1596–1610, Nov. 2002.

[12] M. G. Andreassi, "The biological effects of diagnostic cardiac imaging on chronically exposed physicians: The importance of being non-ionizing," *Cardiovasc. Ultrasound*, vol. 2, no. 1, p. 25, 2004.

[13] N. Sanchez *et al.*, "An 8960-element ultrasound-on-chip for point-of-care ultrasound," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, vol. 64, pp. 480–482, 2021.

[14] D. M. van Willigen *et al.*, "A transceiver ASIC for a single-cable 64-element intra-vascular ultrasound probe," *IEEE J. Solid-State Circuits*, vol. 56, no. 10, pp. 3157–3166, Oct. 2021.

[15] D. C. Giancoli, *Physics for Scientists and Engineers with Modern Physics*, London, U.K.: Pearson Education, 2008.

[16] J. Ophir *et al.*, "Elastography: Ultrasonic estimation and imaging of the elastic properties of tissues," *Proc. Inst. Mech. Eng. Part H: J. Eng. Med.*, vol. 213, no. 3, pp. 203-233, 1999.

[17] K. J. Parker, L. S. Taylor, S. Gracewski, and D. J. Rubens, "A unified view of imaging the elastic properties of tissue," *J. Acoustical Soc. Amer.*, vol. 117, no. 5, pp. 2705-2712, 2005.

[18] T. L. Szabo, "Diagnostic Ultrasound Imaging: Inside Out.," *Boston, MA, USA: Academic*, 2004.

[19] Y. Qiu *et al.*, "Piezoelectric micromachined ultrasound transducer (PMUT) arrays for integrated sensing, actuation and imaging," *Sensors*, vol. 15, no. 4, pp. 8020–8041, 2015.

[20] D. E. Dausch, K. H. Gilchrist, J. B. Carlson, S. D. Hall, J. B. Castellucci, and O. T. von Ramm, "In vivo real-time 3-D intracardiac echo using PMUT arrays," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 61, no. 10, pp. 1754–1764, Oct. 2014.

[21] X. Jiang *et al.*, "Monolithic ultrasound fingerprint sensor," *Microsyst. Nanoeng.*, vol. 3, no. 1, pp. 1–8, 2017.

[22] H. Jaffe, "Piezoelectric ceramics," *J. Am. Ceram. Soc.*, vol. 41, no. 11, pp. 494–498, 1958.

[23] T. E. G. Alvarez-Arenas, "Acoustic impedance matching of piezoelectric transducers to the air," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 51, no. 5, pp. 624–633, May 2004.

[24] M. Toda and M. Thompson, "Novel multi-layer polymer-metal structures for use in ultrasonic transducer impedance matching and backing absorber applications," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 57, no. 12, pp. 2818–2827, Dec. 2010.

[25] E. Brunner, "Ultrasound system considerations and their impact on front-end components," *Analog Devices*, vol. 36, pp. 1–19, 2002.

[26] H. Huang and D. Paramo, "Broadband electrical impedance matching for piezoelectric ultrasound transducers," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 58, no. 12, pp. 2699–2707, Dec. 2011.

[27] W. T. Ang, C. Scurtescu, W. Hoy, T. El-Bialy, Y. Y. Tsui, and J. Chen, "Design and implementation of therapeutic ultrasound generating circuit for dental tissue formation and tooth-root healing," *IEEE Trans. Biomed. Circuits Syst.*, vol. 4, no. 1, pp. 49–61, Feb. 2010.

[28] R. Krimholtz, D. A. Leedom, and G. L. Matthaei, "New equivalent circuits for elementary piezoelectric transducers," *Electron. Lett.*, vol. 6, no. 13, pp. 398–399, 1970.

[29] W. P. Mason, *Electromechanical Transducers and Wave Filters.* New York, NY, USA: Van Nostrand, 1942.

[30] K. Van Dyke, "The piezo-electric resonator and its equivalent network," *Proc. Inst. Radio Eng.*, vol. 16, no. 6, pp. 742–764, 1928.

[31] R. Lerch, "Finite element analysis of piezoelectric transducers," in *Proc. IEEE Ultrason. Symp.*, 1988, pp. 643–654.

[32] R. Lerch, H. Landes, and H. T. Kaarmann, "Finite element modeling of the pulse-echo behavior of ultrasound transducers," in *Proc. IEEE Ultrason. Symp.*, vol. 2, 1994, pp. 1021–1025.

[33] M. Redwood, "Transient performance of a piezoelectric transducer," *J. Acoust. Soc. Am.*, vol. 33, no. 4, pp. 527–536, 1961.

[34] J. E. Aldrich, "Basic physics of ultrasound imaging," *Crit. Care Med.*, vol. 35, pp. S131–S137, May 2007.

[35] Y. Birjis, S. Swaminathan, H. Nazemi, G. C. A. Raj, P. Munirathinam, A. Abu-Libdeh *et al.*, "Piezoelectric micromachined ultrasonic transducers (PMUTs): Performance metrics advancements and applications," *Sensors*, vol. 22, no. 23, p. 9151, Nov. 2022.

[36] M. Trindade and A. Benjeddou, "Effective electromechanical coupling coefficients of piezoelectric adaptive structures: Critical evaluation and optimization," *Mech. Adv. Mater. Struct.*, vol. 16, no. 3, pp. 210–223, Apr. 2009.

[37] K. Roy, J. E.-Y. Lee, and C. Lee, "Thin-film PMUTs: A review of over 40 years of research," *Microsyst. Nanoeng.*, vol. 9, no. 1, pp. 1–15, Jul. 2023.

[38] L. Jia, L. Shi, C. Liu, C. Sun, and G. Wu, "Enhancement of transmitting sensitivity of piezoelectric micromachined ultrasonic transducers by electrode design," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 68, no. 11, pp. 3371–3377, Nov. 2021.

[39] I. O. Wygant *et al.*, "Integration of 2D CMUT arrays with front-end electronics for volumetric ultrasound imaging," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 55, no. 2, pp. 327–342, Feb. 2008.

[40] I. O. Wygant *et al.*, "An integrated circuit with transmit beamforming flip-chip bonded to a 2-D CMUT array for 3-D ultrasound imaging," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 56, no. 10, pp. 2145–2156, Oct. 2009.

[41] A. Bhuyan *et al.*, "Integrated circuits for volumetric ultrasound imaging with 2-D CMUT arrays," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 6, pp. 796–804, Dec. 2013.

[42] J. Zahorian *et al.*, "Monolithic CMUT-on-CMOS integration for intravascular ultrasound applications," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 58, no. 12, pp. 2659–2667, Dec. 2011.

[43] G. Gurun, P. Hasler, and F. L. Degertekin, "Front-end receiver electronics for high-frequency monolithic CMUT-on-CMOS imaging arrays," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 58, no. 8, pp. 1658–1668, Aug. 2011.

[44] D. Hohm and G. Hess, "A subminiature condenser microphone with silicon nitride membrane and silicon back plate," *J. Acoust. Soc. Amer.*, vol. 85, no. 1, pp. 476–480, 1989.

[45] D. Schindel, D. Hutchins, L. Zou, and M. Sayer, "The design and characterization of micromachined air-coupled capacitance transducers," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 42, no. 1, pp. 42–50, Jan. 1995.

[46] M. Haller and B. Khuri-Yakub, "A surface micromachined electrostatic ultrasonic air transducer," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 43, no. 1, pp. 1–6, Jan. 1996.

[47] B. T. Khuri-Yakub and Ö. Oralkan, "Capacitive micromachined ultrasonic transducers for medical imaging and therapy," *J. Micromech. Microeng.*, vol. 21, no. 5, p. 054004, Apr. 2011.

[48] A. Caronti, G. Caliano, A. Iula, and M. Pappalardo, "An accurate model for capacitive micromachined ultrasonic transducers," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 49, no. 2, pp. 159–168, Feb. 2002.

[49] A. Lohfink and P. Eccardt, "Linear and nonlinear equivalent circuit modeling of CMUTs," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 52, no. 12, pp. 2163–2172, Dec. 2005.

[50] Microchip, *8-Channel Ultra-Low-Phase-Noise Low-Power Continuous Wave Transmitter With Beamformer*, Chandler, AZ, USA, 2016.

[51] Microchip, *4-Channel Low-Phase-Noise Low-Power Continuous Wave Transmitter*, Chandler, AZ, USA, 2017.

[52] J. Choi, S. Youn, J. Y. Hwang, S. Ha, C. Kim, and M. Je, "Energy-efficient high-voltage pulsers for ultrasound transducers," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 1, pp. 19–23, Jan. 2021.

[53] D. Bianchi, F. Quaglia, A. Mazzanti, and F. Svelto, "Analysis and design of a high voltage integrated class-B amplifier for ultrasound transducers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 7, pp. 1942–1951, Jul. 2014.

[54] Z. Gao, P. Gui, and R. Jordanger, “An integrated high-voltage low-distortion current-feedback linear power amplifier for ultrasound transmitters using digital predistortion and dynamic current biasing techniques,” *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 6, pp. 373–377, Jun. 2014.

[55] K. Sun *et al.*, “A 180-Vpp integrated linear amplifier for ultrasonic imaging applications in a high-voltage CMOS SOI technology,” *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 2, pp. 149–153, Feb. 2015.

[56] D. Ghisu, A. Gambero, M. Terenzi, G. Ricotti, A. Moroni, and S. Rossi, “180Vpp output voltage 24MHz bandwidth low power class AB current-feedback high voltage amplifier for ultrasound transmitters,” in *Proc. IEEE Custom Integr. Circuits Conf.*, 2018, pp. 1–4.

[57] B. Haider, “Power drive circuits for diagnostic medical ultrasound,” in *Proc. IEEE Int. Symp. Power Semicond. Devices*, 2006, pp. 1–8.

[58] M. Averkiou, D. Roundhill, and J. Powers, “A new imaging technique based on the nonlinear properties of tissues,” in *Proc. IEEE Ultrason. Symp.*, vol. 2, 1997, pp. 1561–1566.

[59] J.-Y. Lu and J. L. Waugaman, “Development of a linear power amplifier for high frame rate imaging system,” *Biomed. Ultrasound Imaging Appl.*, vol. 2, pp. 1413–1416, 2004.

[60] J. Park, C. Hu, and K. K. Shung, “Linear power amplifier for high frequency ultrasound coded excitation imaging,” in *Proc. IEEE Int. Ultrason. Symp.*, 2010, pp. 1809–1812.

[61] P. Behnamfar, R. Molavi and S. Mirabbasi, ”Transceiver design for CMUT-based super-resolution ultrasound imaging,” *IEEE Trans. Biomed. Circuits Syst.*, vol. 10, no. 2, pp. 383–393, Apr. 2016.

[62] M. Declerq, M. Schubert and F. Clement, ”5 V-to-75 V CMOS output interface circuits,” in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 1993, pp. 162–163.

[63] A. Nikoozadeh *et al.*, ”Forward-looking intracardiac ultrasound imaging using a 1-D CMUT array integrated with custom front-end electronics,” *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 55, no. 12, pp. 2651–2660, Dec. 2008.

[64] R. Chebli and M. Sawan, "Fully integrated high-voltage front-end interface for ultrasonic sensing applications," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 54, no. 1, pp. 179–190, Jan. 2007.

[65] D. Zhao *et al.*, "High-voltage pulser for ultrasound medical imaging applications," in *Proc. Int. Symp. Integr. Circuits*, 2011, pp. 408–411.

[66] H.-K. Cha *et al.*, "A CMOS high-voltage transmitter IC for ultrasound medical imaging applications," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 60, no. 6, pp. 316–320, Jun. 2013.

[67] H.-Y. Tang *et al.*, "Miniaturizing ultrasonic system for portable health care and fitness," *IEEE Trans. Biomed. Circuits Syst.*, vol. 9, no. 6, pp. 767–776, 2015.

[68] M. Tan *et al.*, "An integrated programmable high-voltage bipolar pulser with embedded transmit/receive switch for miniature ultrasound probes," *IEEE Solid-State Circuits Lett.*, vol. 2, no. 9, pp. 79–82, Sep. 2019.

[69] G. Jung *et al.*, "A reduced-wire ICE catheter ASIC with Tx beamforming and Rx time-division multiplexing," *IEEE Trans. Biomed. Circuits Syst.*, vol. 12, no. 6, pp. 1246–1255, Dec. 2018.

[70] T. Costa *et al.*, "An integrated 2D ultrasound phased array transmitter in CMOS with pixel pitch-matched beamforming," *IEEE Trans. Biomed. Circuits Syst.*, vol. 15, no. 4, pp. 731–742, Aug. 2021.

[71] J. Doutreloigne, H. De Smet, J. Van den Steen and G. Van Doorselaer, "Low-power high-voltage CMOS level-shifters for liquid crystal display drivers," in *Proc. 11th Int. Conf. Microelectron.*, 1999, pp. 213–216.

[72] A. Banuaji and H. Cha, "A 15-V bidirectional ultrasound interface analog front-end IC for medical imaging using standard CMOS technology," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 61, no. 8, pp. 604–608, Aug. 2014.

[73] B. Serneels, T. Piessens, M. Steyaert and W. Dehaene, "A high-voltage output driver in a 2.5-V 0.25-μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp. 576–583, Mar. 2005.

[74] M. Khorasani *et al.*, "Low-power static and dynamic high-voltage CMOS level-shifter circuits," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2008, pp. 1946–1949.

[75] X. Jiang, W. T. Ng and J. Chen, "A miniaturized low-intensity ultrasound device for wearable medical therapeutic applications," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 6, pp. 1372–1382, Dec. 2019.

[76] Y. Moghe, T. Lehmann and T. Piessens, "Nanosecond delay floating high voltage level shifters in a 0.35-μm HV-CMOS technology," *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp. 485–497, Feb. 2011.

[77] Y. Igarashi *et al.*, "Single-chip 3072-element-channel transceiver/128-subarray-channel 2-D array IC with analog RX and all-digital TX beamformer for echocardiography," *IEEE J. Solid-State Circuits*, vol. 54, no. 9, pp. 2555–2567, 2019.

[78] C. Hsia, Y.-C. Huang and C.-W. Lu, "Single-chip ultra high slew-rate pulse generator for ultrasound scanner applications," in *Proc. IEEE Int. Ultrason. Symp.*, 2013, pp. 1556–1559.

[79] Y. Huang, C. Hsia and G. Wu, "A high-voltage integrated bipolar pulser for medical ultrasound scanner applications," in *Proc. IEEE Int. Conf. Consum. Electron.*, 2017, pp. 33–34.

[80] Y. Huang *et al.*, "A high-speed high-voltage bipolar pulser for medical ultrasonic imaging applications," in *Proc. IEEE Int. Conf. Consum. Electron.*, 2018, pp. 1–2.

[81] A. L. Holen and T., "A high-voltage cascode-connected three-level pulse-generator for bio-medical ultrasound applications," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2019, pp. 1–5.

[82] L. Svensson *et al.*, "Adiabatic charging without inductors," Tech. Rep. ACMOS-TR-3, 1993.

[83] L. J. Svensson and J. G. Koller, "Driving a capacitive load without dissipating fCV^2," in *Proc. IEEE Symp. Low Power Electron.*, 1994, pp. 100–101.

[84] G. Jung *et al.*, "Supply-doubled pulse-shaping high voltage pulser for CMUT arrays," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 65, no. 3, pp. 306–310, Mar. 2018.

[85] K.-J. Choi and D.-W. Jee, "High-efficiency 6.6-29 V pulse driver using charge redistribution," *Electron. Lett.*, vol. 54, no. 12, pp. 746–748, 2018.

[86] J. Tillak *et al.*, "A 2.34-μJ/scan acoustic power scalable charge-redistribution pMUT interface system with on-chip aberration compensation for portable ultrasonic applications," in *Proc. IEEE Asian Solid-State Circuits Conf.*, 2016, pp. 189–192.

[87] K. Chen *et al.*, "Ultrasonic imaging transceiver design for CMUT: A three-level 30-Vpp pulse-shaping pulser with improved efficiency and a noise-optimized receiver," *IEEE J. Solid-State Circuits*, vol. 48, no. 11, pp. 2734–2745, Nov. 2013.

[88] K.-J. Choi *et al.*, "A 28.7 V modular supply multiplying pulser with 75.4% power reduction relative to CV^2f," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 68, no. 3, pp. 858–862, Mar. 2021.

[89] R. C. Levine, "Apparent nonconservation of energy in the discharge of an ideal capacitor," *IEEE Trans. Educ.*, vol. 10, no. 4, pp. 197–202, 1967.

[90] S. Y. Peng *et al.*, "A charge-based low-power high-SNR capacitive sensing interface circuit," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 55, no. 7, pp. 1863–1872, Aug. 2008.

[91] M. Sautto *et al.*, "A CMUT transceiver front-end with 100-V TX driver and 1-mW low-noise capacitive feedback RX amplifier in BCD-SOI technology," *Proc. 40th Eur. Solid State Circuits Conf.*, pp. 407–410, 2014.

[92] G. Gurun *et al.*, "An analog integrated circuit beamformer for high-frequency medical ultrasound imaging," *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, no. 5, pp. 454–467, 2012.

[93] B. Razavi, "A 622 Mb/s 4.5 pA per sqrt(Hz) CMOS transimpedance amplifier," in *Proc. IEEE Int. Solid-State Circuits Conf.*, pp. 162–163, 2000.

[94] M. Crescentini *et al.*, "Noise limits of CMOS current interfaces for biosensors: A review," *IEEE Trans. Biomed. Circuits Syst.*, vol. 8, no. 2, pp. 278–292, Apr. 2014.

[95] G. Wang, M. Atef and Y. Lian, "Towards a continuous non-invasive cuffless blood pressure monitoring system using PPG: Systems and circuits review," *IEEE Circuits Syst. Mag.*, vol. 18, no. 3, pp. 6–26, Jul.–Sep. 2018.

[96] B. Razavi, *Design of Integrated Circuits for Optical Communications*, Hoboken, NJ, USA: Wiley, 2012.

[97] S. Firouz, E. N. Aghdam and R. Jafarnejad, "A low power low noise single-ended to differential TIA for ultrasound imaging probes," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 68, no. 2, pp. 607–611, Feb. 2021.

[98] E. Kang *et al.*, "A variable-gain low-noise transimpedance amplifier for miniature ultrasound probes," *IEEE J. Solid-State Circuits*, vol. 55, no. 12, pp. 3157–3168, 2020.

[99] J. Yao *et al.*, "Design of a low power time-gain-compensation amplifier for a 2D piezoelectric ultrasound transducer," *Proc. IEEE Int. Ultrason. Symp.*, pp. 841–844, 2010.

[100] Y. Wang, M. Koen and D. Ma, "Low-noise CMOS TGC amplifier with adaptive gain control for ultrasound imaging receivers," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 58, no. 1, pp. 26–30, Jan. 2011.

[101] Z. Yu *et al.*, "Front-end receiver electronics for a matrix transducer for 3-D transesophageal echocardiography," *IEEE Trans. Ultrason., Ferroelect., Freq. Control*, vol. 59, no. 7, pp. 1500–1512, Jul. 2012.

[102] C. Chen *et al.*, "A prototype PZT matrix transducer with low-power integrated receive ASIC for 3-D transesophageal echocardiography," *IEEE Trans. Ultrason., Ferroelect., Freq. Control*, vol. 63, no. 1, pp. 47–59, Jan. 2016.

[103] P. Wang and T. Ytterdal, "A 54-µW inverter-based low-noise single-ended to differential VGA for second harmonic ultrasound probes in 65-nm CMOS," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 63, no. 7, pp. 623–627, Jul. 2016.

[104] H. Attarzadeh, Y. Xu, and T. Ytterdal, "A low-power high-dynamic-range receiver system for in-probe 3-D ultrasonic imaging," *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 5, pp. 1053–1064, Oct. 2017.

[105] T. Kim, S. Shin, and S. Kim, "An 80.2 dB DR 23.25 mW/channel 8-channel ultrasound receiver with a beamforming embedded SAR ADC," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 66, no. 9, pp. 1487–1491, Sep. 2019.

[106] M. C. Chen *et al.*, "A pixel pitch-matched ultrasound receiver for 3-D photoacoustic imaging with integrated delta-sigma beamformer in 28-nm UTBB FD-SOI," *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 2843–2856, Nov. 2017.

[107] C. Chen *et al.*, “A pitch-matched front-end ASIC with integrated subarray beamforming ADC for miniature 3-D ultrasound probes,” *IEEE J. Solid-State Circuits*, vol. 53, no. 11, pp. 3050–3064, Nov. 2018.

[108] M. Tan *et al.*, “A front-end ASIC with high-voltage transmit switching and receive digitization for 3-D forward-looking intravascular ultrasound imaging,” *IEEE J. Solid-State Circuits*, vol. 53, no. 8, pp. 2284–2297, Aug. 2018.

[109] C. Chen *et al.*, “A front-end ASIC with receive sub-array beamforming integrated with a 32 × 32 PZT matrix transducer for 3-D transesophageal echocardiography,” *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 994–1006, Apr. 2017.

[110] H. Nguyen *et al.*, “A binary-weighted switching and reconfiguration-based programmable gain amplifier,” *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 56, no. 9, pp. 699–703, Sep. 2009.

[111] Q.-H. Duong *et al.*, “A 95-dB linear low-power variable gain amplifier,” *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 53, no. 8, pp. 1648–1657, Aug. 2006.

[112] I. Choi, H. Seo, and B. Kim, “Accurate dB-linear variable gain amplifier with gain error compensation,” *IEEE J. Solid-State Circuits*, vol. 48, no. 2, pp. 456–464, Feb. 2013.

[113] B. Gilbert, “A low-noise wideband variable-gain amplifier using an interpolated ladder attenuator,” in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 1991, pp. 280–281.

[114] C.-C. Chang and S.-I. Liu, “Pseudo-exponential function for MOSFETs in saturation,” *IEEE Trans. Circuits Syst. II: Analog Digit. Signal Process.*, vol. 47, no. 11, pp. 1318–1321, Nov. 2000.

[115] Q.-H. Duong, Le-Quan, and S.-G. Lee, “An all CMOS 84dB-linear low-power variable gain amplifier,” in *Proc. Dig. Tech. Papers 2005 Symp. VLSI Circuits*, 2005, pp. 114–117.

[116] Q.-H. Duong and S.-G. Lee, “86 dB 1.4 mW 1.8 V 0.07 mm^2 single-stage variable gain amplifier in 0.18 µm CMOS,” *Electron. Lett.*, vol. 43, no. 1, pp. 19–20, 2007.

[117] J.-Y. Um, “A compact variable gain amplifier with continuous time-gain compensation using systematic predistorted gain control,” *IEEE Trans. Circuits Syst. II: Exp. Briefs*, to be published, doi: 10.1109/TCSII.2021.3090424.

[118] E. Brunner, “An ultra-low noise linear-in-dB variable gain amplifier for medical ultrasound applications,” in *Proc. WESCON*, 1995, p. 650, doi: 10.1109/WESCON.1995.485477.

[119] L. Dufort and Mukherjee, “Digitally controlled high-voltage analog switch array for medical ultrasound applications in thin-layer silicon-on-insulator process,” in *Proc. IEEE Int. SOI Conf.*, 2002, pp. 78–79.

[120] F. Yamashita, J. Aizawa, and H. Honda, “A new compact, low on resistance and high off isolation high voltage analog switch IC without using high voltage power supplies for ultrasound imaging system,” in *Proc. 28th Int. Symp. Power Semicond. Devices ICs*, 2016, pp. 415–418.

[121] K. Hara *et al.*, “A new 80V 32×32ch low loss multiplexer LSI for a 3D ultrasound imaging system,” in *Proc. 17th Int. Symp. Power Semicond. Devices ICs*, 2005, pp. 359–362.

[122] G. Ricotti and V. Bottarel, “HV floating switch matrix with parachute safety driving for 3D echography systems,” in *Proc. IEEE 44th Eur. Solid State Circuits Conf.*, 2018, pp. 271–273.

[123] Y. Li *et al.*, “An integrated 90V switch array for medical ultrasound applications,” in *Proc. IEEE Custom Integr. Circuits Conf.*, 2006, pp. 269–272.

[124] S.-J. Jung, S.-K. Hong, and O.-K. Kwon, “Area-efficient high-voltage switch using floating control circuit for 3D ultrasound imaging systems,” *Electron. Lett.*, vol. 50, no. 25, pp. 1900–1902, 2014.

[125] S. Dai, R. W. Knepper, and M. N. Horenstein, “A 300-V LDMOS analog-multiplexed driver for MEMS devices,” *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 62, no. 12, pp. 2806–2816, Dec. 2015.

[126] H. Jung *et al.*, “CMOS high-voltage analog 1-64 multiplexer/demultiplexer for integrated ultrasound guided breast needle biopsy,” *IEEE Trans. Ultrason., Ferroelect., Freq. Control*, vol. 65, no. 8, pp. 1334–1345, Aug. 2018.

[127] S. Kajiyama *et al.*, “T/R-switch composed of 3 high-voltage MOSFETs with 12.1 µW consumption that can perform per-channel TX to RX self-loopback AC tests for 3D ultrasound imaging with 3072-channel transceiver,” in *Proc. IEEE Asian Solid-State Circuits Conf.*, 2019, pp. 305–308.

[128] L. Demi, “Practical guide to ultrasound beam forming: Beam pattern and image reconstruction analysis,” *Appl. Sci.*, vol. 8, no. 9, p. 1544, 2018.

[129] L. W. Schmerr Jr., *Fundamentals of Ultrasonic Phased Arrays.* Berlin, Germany: Springer, 2014, vol. 215.

[130] J. Um *et al.*, “A single-chip 32-channel analog beamformer with 4-ns delay resolution and 768-ns maximum delay range for ultrasound medical imaging with a linear array transducer,” *IEEE Trans. Biomed. Circuits Syst.*, vol. 9, no. 1, pp. 138–151, Feb. 2015.

[131] S. Sharma and T. Ytterdal, “In-probe ultrasound beamformer utilizing switched-current analog RAM,” *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 62, no. 6, pp. 517–521, Jun. 2015.

[132] J. Jeong *et al.*, “A low-power analog delay line using a current-splitting method for 3-D ultrasound imaging systems,” *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 65, no. 7, pp. 829–833, Jul. 2018.

[133] C. Maslak and H. Samuel, “Acoustic imaging apparatus,” U.S. Patent 4140022, Palo Alto, CA, Feb. 1979. [Online]. Available: `https://www.freepatentsonline.com/4140022.html`

[134] L. Zhang, C. Hu, J. T. Yen, and K. K. Shung, “Design of a 64 channel analog receive beamformer for high frequency linear arrays,” in *Proc. IEEE Int. Ultrason. Symp.*, 2010, pp. 1968–1971.

[135] J. R. Talman, S. L. Garverick, and G. R. Lockwood, “Integrated circuit for high-frequency ultrasound annular array,” in *Proc. IEEE Custom Integr. Circuits Conf.*, 2003, pp. 477–480.

[136] T. Halvorsrod, W. Luzi, and T. S. Lande, “A log-domain μbeamformer for medical ultrasound imaging systems,” *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 52, no. 12, pp. 2563–2575, Dec. 2005.

[137] T. K. Song and J. F. Greenleaf, “Ultrasonic dynamic focusing using an analog FIFO and asynchronous sampling,” *IEEE Trans. Ultrason., Ferroelect., Freq. Control*, vol. 41, no. 3, pp. 326–332, May 1994.

[138] B. Stefanelli *et al.*, "An analog beam-forming circuit for ultrasound imaging using switched-current delay lines," *IEEE J. Solid-State Circuits*, vol. 35, no. 2, pp. 202–211, Feb. 2000.

[139] Y. Mo *et al.*, "Pipelined delay-sum architecture based on bucket-brigade devices for on-chip ultrasound beamforming," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1754–1757, Oct. 2003.

[140] Z. Yu, M. Pertijs, and G. Meijer, "Ultrasound beamformer using pipeline-operated S/H delay stages and charge-mode summation," *Electron. Lett.*, vol. 47, no. 18, pp. 1011–1012, 2011.

[141] J. A. Brown and G. R. Lockwood, "A digital beamformer for high-frequency annular arrays," *IEEE Trans. Ultrason., Ferroelect., Freq. Control*, vol. 52, no. 8, pp. 1262–1269, Aug. 2005.

[142] C.-H. Hu *et al.*, "High-frequency ultrasound annular array imaging. Part II: Digital beamformer design and imaging," *IEEE Trans. Ultrason., Ferroelect., Freq. Control*, vol. 53, no. 2, pp. 309–316, Feb. 2006.

[143] C.-H. Hu *et al.*, "Development of a real-time, high-frequency ultrasound digital beamformer for high-frequency linear array transducers," *IEEE Trans. Ultrason., Ferroelect., Freq. Control*, vol. 53, no. 2, pp. 317–323, Feb. 2006.

[144] G. Peyton *et al.*, "Quadrature synthetic aperture beamforming front-end for miniaturized ultrasound imaging," *IEEE Trans. Biomed. Circuits Syst.*, vol. 12, no. 4, pp. 871–883, Aug. 2018.

[145] J. Y. Um *et al.*, "An analog-digital hybrid RX beamformer chip with non-uniform sampling for ultrasound medical imaging with 2D CMUT array," *IEEE Trans. Biomed. Circuits Syst.*, vol. 8, no. 6, pp. 799–809, Dec. 2014.

[146] Y. J. Kim *et al.*, "A single-chip 64-channel ultrasound RX-beamformer including analog front-end and an LUT for non-uniform ADC-sample-clock generation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 1, pp. 87–97, Feb. 2017.

[147] P. A. Hager, A. Bartolini, and L. Benini, "Ekho: A 30.3 W, 10k-channel fully digital integrated 3-D beamformer for medical ultrasound imaging achieving 298 M focal points per second," *IEEE Trans. VLSI Syst.*, vol. 24, no. 5, pp. 1936–1949, May 2016.

[148] J. Kang *et al.*, “A system-on-chip solution for point-of-care ultrasound imaging systems: Architecture and ASIC implementation,” *IEEE Trans. Biomed. Circuits Syst.*, vol. 10, no. 2, pp. 412–423, Apr. 2016.

[149] B. Savord and R. Solomon, “Fully sampled matrix transducer for real-time 3D ultrasonic imaging,” in *Proc. IEEE Symp. Ultrason.*, 2003, vol. 1, pp. 945–953.

[150] K. Nakamura *et al.*, “An 85 mW, 10 b, 40 Msample/s CMOS parallel-pipelined ADC,” *IEEE J. Solid-State Circuits*, vol. 30, no. 3, pp. 173–183, Mar. 1995.

[151] K. Kaviani *et al.*, “A multichannel pipeline analog-to-digital converter for an integrated 3-D ultrasound imaging system,” *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1266–1270, Jul. 2003.

[152] Y. Zhang *et al.*, “A continuous-time delta-sigma modulator for biomedical ultrasound beamformer using digital ELD compensation and FIR feedback,” *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 62, no. 7, pp. 1689–1698, Jul. 2015.

[153] Y. Zhang and A. Demosthenous, “Integrated Circuits for Medical Ultrasound Applications: Imaging and Beyond,” in*IEEE Transactions on Biomedical Circuits and Systems*, vol. 15, no. 5, pp. 838–858, Oct. 2021.

[154] G. Caliano, A. Caronti, A. Savoia, C. Longo, M. Pappalardo, E. Cianci, and V. Foglietti, “Capacitive micromachined ultrasonic transducer (CMUT) made by a novel reverse fabrication process,” in *Proc. IEEE Ultrasonics Symp.*, vol. 1, pp. 479–482, 2005.

[155] G. Bonciani *et al.*, “A heterogeneous ultrasound open scanner for the real-time implementation of computationally demanding imaging methods,” *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 72, no. 1, pp. 100–108, Jan. 2025.

[156] A. J. Lopez-Martin *et al.*, “Micropower class AB voltage followers with simple quiescent current control,” *IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Boise, ID, USA, pp. 218-221, 2012.

[157] S. Kajiyama et al., “T/R Switch Composed of Three HV-MOSFETs With 12.1 uW Consumption That Enables Per-Channel Self-Loopback AC Tests and 18.1 dB Switching Noise Suppression for 3-D Ultrasound

Imaging With 3072-Ch Transceiver," *IEEE Trans. on VLSI Systems.*, vol. 30, no. 2, pp. 153-165, Feb. 2022.

[158] C. Chen and M. A. P. Pertijs, "Integrated Transceivers for Emerging Medical Ultrasound Imaging Devices: A Review," *IEEE Open J. Solid-State Circuit Society*, pp. 104-114, Oct. 2021.

[159] M. Tan et al., "A 64-channel transmit beamformer with ±30-V bipolar high-voltage pulsers for catheter-based ultrasound probes," *IEEE J. Solid-State Circuits*, vol. 55, no. 7, pp. 1796–1806, Jul. 2020.

[160] K. Brenner et al., "Advances in capacitive micromachined ultrasonic transducers," *Micromachines*, vol. 10, no. 2, p. 152, Feb. 2019.

[161] Datasheet of MAX14822.online: https://www.mouser.it/datasheet/2/609/Maxim_4_19_22_MAX14822_FDS-3114393.pdf

[162] A. Amini et al., "On improving accuracy of the resistor strings based on a new design technique," *Iran J Sci Technol Trans Electr Eng Springer*, vol. 45, no. 1, pp. 221–227, Mar. 2021.

[163] J. Borg and J. Johansson, "An ultrasonic transducer interface IC with integrated push-pull 40 Vpp, 400 mA current output, 8-bit DAC and integrated HV multiplexer," *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp. 475–484, Feb. 2011.

[164] D. Dufort, T. Letavic, and S. Mukherjee, "Digitally controlled high-voltage analog switch array for medical ultrasound applications in thin-layer silicon-on-insulator process," *in Proc. IEEE Int. SOI Conf.*, Oct. 2002, pp. 78–79.

[165] H. Shafir, C. M. Daft, and P. M. Wagner, "Switch for aperture control in medical diagnostic ultrasound imaging," U.S. Patent 0021920 A1, 2011.

[166] A. Safarpour et al., "speed-power improvement in high-voltage switches employed in multielectrode arrays," *IEEE Transactions on circuits and Systems-II:Express Briefs*, vol. 69, no. 7, pp. 3139–3143, Jul. 2022.

[167] G. Diaz, "Wide common mode range transmission gate," U.S. Patent 0 132 331 A1, 2014.

[168] C. S. Birk and G. M. Puchalt, "Four-quadrant bootstrapped switch circuit," U.S. Patent 0 009 623 A1, Jan. 10, 2013.

[169] D. Y. Aksin and I. Ozkaya, “25V sampling switch for power management data converters in 0.35μm CMOS with DNMOS,” *in Proc. Eur. Solid-State Circuits Conf. (ESSCIRC)*, 2009, pp. 136–139.

[170] H. Jung et al., “CMOS High-Voltage Analog 1–64 Multiplexer/ Demultiplexer for Integrated Ultrasound Guided Breast Needle Biopsy,” *IEEE Trans. Ultrasonic, Ferroelectrics, and Frequency Control*, vol. 65, no. 8, pp. 1334-1345, Aug. 2018.

[171] D. Osipov et al., “Current driver with read-out HV protection for neural stimulation,” *IEEE Nordic Circuits Syst. Conf. (NORCAS)*, 2016, pp. 1–4.

[172] C. Chen., ”Front-End ASICs for 3-D Ultrasound: From Beamforming to Digitization,” *Dissertation (TU Delft), Delft University of Technology*, 2018. https://doi.org/10.4233/uuid:a5002bb0-4701-4e33-aef6-3c78d0c9fd70

[173] S. Robert, O. Abed-Meraim, and L. L. Coco, ”Wide-band variable-gain LNA in 65nm CMOS with inverter based amplifier for multi-tuners cable TV reception,” *in European Solid-State Circuits Conference (ESSCIRC)*, pp. 104 - 107, 2009.

[174] A. J. Lopez-Martin et al., ”Micropower class AB voltage followers with simple quiescent current control,” *2012 IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Boise, ID, USA, pp. 218-221, 2012.

[175] F. Maloberti, “Analog Design for CMOS VLSI Systems,” Boston, MA, USA:Kluwer, vol. 646, 2003.

[176] J. Lim, C. Tekes, E. F. Arkan, A. Rezvanitabar, F. L. Degertekin, and M. Ghovanloo, “Highly integrated guidewire ultrasound imaging system-on-a-chip,” *IEEE Journal of Solid-State Circuits*, vol. 55, no. 5, pp. 1310–1323, May 2020.

[177] D. M. van Willigen *et al.*, “A transceiver ASIC for a single-cable 64-element intra-vascular ultrasound probe,” *IEEE Journal of Solid-State Circuits*, vol. 56, no. 10, pp. 3157–3166, 2021.

[178] L. Novaresi *et al.*, “A PMUT transceiver front-end with 100-V TX driver and low-noise voltage amplifier in BCD-SOI technology,” in *Proc. ESSCIRC 2022 - IEEE 48th European Solid-State Circuits Conference*, 2022, pp. 221–224.