A CMOS Current-Mode Magnetic Hall Sensor With Integrated Front-End

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***Abstract*—A Hall magnetic sensor working in the current domain and its electronic interface are presented. The paper describes the physical sensor design and implementation in a standard CMOS technology, the transistor level design of its high sensitive front-end together with the sensor experimental characterization. The current-mode Hall sensor and the analog readout circuit have been fabricated using a 0.18-μm CMOS technology. The sensor uses the current spinning technique to compensate for the offset and provides a differential current as an output signal. The measured sensor power consumption and residual offset are 120 μW and 50 μT, respectively.**

***Index Terms*—CMOS Hall sensors, current spinning, magnetic sensor.**

I. Introduction

In RECENT years, Hall sensors became widely used because of their compatibility with modern semiconductor technologies. In particular, there are on the market applications for proximity switching, positioning, speed detection, and current sensing that use integrated Hall sensors fabricated in low-cost complementary metal-oxide-semiconductor (CMOS) technologies.

Since the Hall sensors convert a magnetic field into an electrical signal, either voltage or current, we distinguish between operation in voltage or current mode. For both modes, the biasing is a constant voltage or a constant current. In the voltage mode, the magnetic field (orthogonal to the Hall plate) is converted into an output voltage, as shown in Fig. 1(a). The layout permits current spinning, a technique used to compensate for the offset. The output voltage is typically in the order of micro- to millivolt and, therefore, it must be amplified before being transmitted to the outside world. A chain of amplifiers, often directly integrated on the same silicon chip, amplifies the signal by factors that can go up to 1000. Important features for qualifying Hall sensors are signal-to-noise ratio (SNR), residual offset, and sensitivity and offset temperature dependent drifts. Several techniques have been developed for improving these characteristics, [1]–[6]. In particular, works reported in [3] and in [4] present Hall sensor microsystems operating in the voltage mode achieving a temperature sensitivity lower than 100 ppm/°C. The result is made possible by continuous time measurement and calibration of the device sensitivity. The same techniques are effective to compensate for drifts due to mechanical stresses and ageing. The work described in [6] focuses on the reduction of input referred noise and power consumption. The Hall microsystem uses current spinning and a delta-sigma modulator employing a switched biasing amplifier. The measured input referred noise is reduced down to 25 $\mu\mathrm{T}/\sqrt{\mathrm{Hz}}$, a remarkable value, but the power consumption is 4.5 mW.

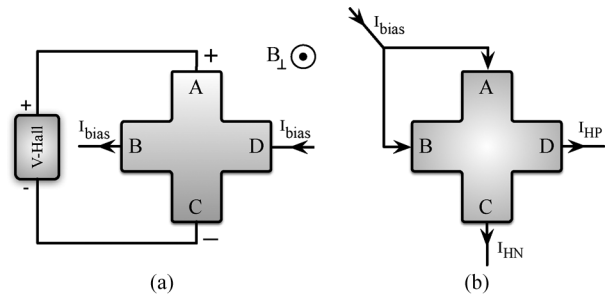

Fig. 1. (a) Hall plate operating in the voltage mode. (b) Proposed Hall plate working in the current mode.

The current mode is an alternative to the widely used voltage mode. The output is a current and the configuration is like the one of Fig. 1(b). Even in this case, the shape of the sensor allows current spinning. The bias current, I_{bias}, enters into two consecutive arms (A and B in the figure); for zero magnetic field, it is split in two equal parts, assuming that the voltages of terminals C and D are equal. A magnetic field orthogonal to the Hall plate unbalances the sensor giving rise to different output currents, I_{HP} and I_{HN}, equal to $I_{bias}/2 \pm I_{Hall}/2$. The difference of these two currents can be represented by an equivalent current source of a Hall current, I_{Hall}, which is proportional to the applied magnetic field.

The effectiveness of Hall devices is measured by the sensitivity. It corresponds to the output quantity for unity supply quantity and magnetic field. Table I gives the sensitivity definitions for the two types of Hall devices.

This paper describes the design of a current mode Hall microsystem and its electronic interface. The prototype has been fabricated in a standard 0.18-μm CMOS technology. The system consists of two Hall plates driven in the current mode able to provide a differential output current proportional to the applied magnetic field. The offset caused by possible mismatch in Hall plates dimensions is canceled out by means of current spinning. A fully differential chopper stabilized current integrator cascaded to the sensor determines the output voltage. Experimental results are reported.

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TABLE I
SENSITIVITY OF HALL DEVICES IN VOLTAGE AND CURRENT MODE

Mode	Sensitivity	Unit
Current biased voltage mode	$S_{V_I} = \left\lvert \frac{V_{Hall}}{I_{bias} \times B} \right\rvert$	$[V/AT]$
Voltage biased voltage mode	$S_{V_V} = \left\lvert \frac{V_{Hall}}{V_{bias} \times B} \right\rvert$	$[V/VT] = T^{-1}$
Current Mode	$S_I = \left\lvert \frac{I_{Hall}}{I_{bias} \times B} \right\rvert$	$[A/AT] = T^{-1}$

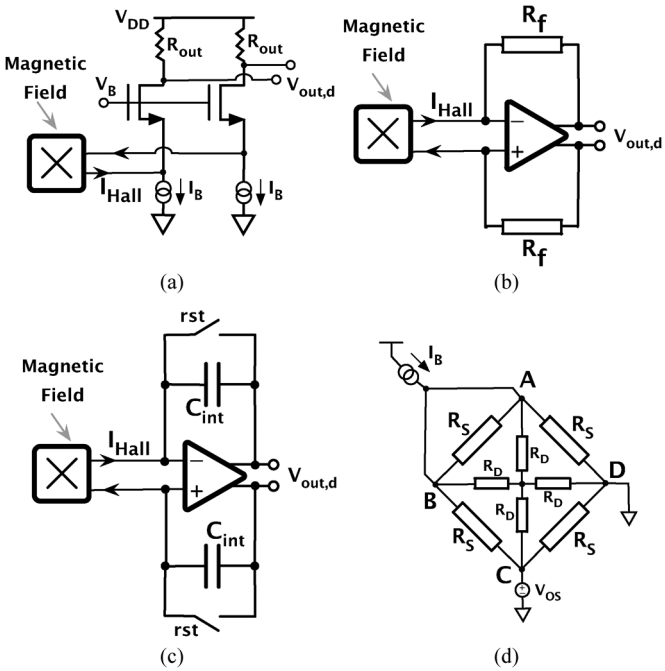

Fig. 2. Three I/V configurations: (a) common-gate detection, (b) resistive detection, and (c) integrator capacitive detection. (d) 8-resistors Hall plate equivalent model.

The paper is organized as follows. Section II provides the sensor and the readout circuit implementation details while Section III discusses the simulation results achieved in COMSOL Multiphysics environment of the designed Hall plate. Section IV presents the experimental verification of both the sensor and the entire microsystem while Section V draws the conclusions.

II. SYSTEM DESIGN

A current-mode Hall device typically generates small output currents, in the nano- to microampere range for very small bias currents. Fig. 2 shows three possible non-sampled techniques for the I/V conversion: the common-gate detection, the resistive detection, and the integrating detection, [7]. For the solution of Fig. 2(a), the Hall currents, $\pm \mathrm{I}_{Hall}$, flow into the sources of a common-gate stage (N-channel input). The input resistances and the thermal noise currents depend on the transconductance of the input transistors. Therefore, in order to have a good SNR, a relatively large bias current, I_B, is required. The resistive detection of Fig. 2(b) uses a resistance, R_f, to convert the sensor current into voltage. In this case, the resistance R_f itself is the main noise source. This limits the maximum transresistance gain of the sensor interface. The third method, shown in Fig. 2(c), integrates the currents $\pm \mathrm{I}_{Hall}$ over the capacitor C_{int} for a given period of time after a reset. The method grants better noise performances, [7], [8], and provides a transresistance gain proportional to the integration time.

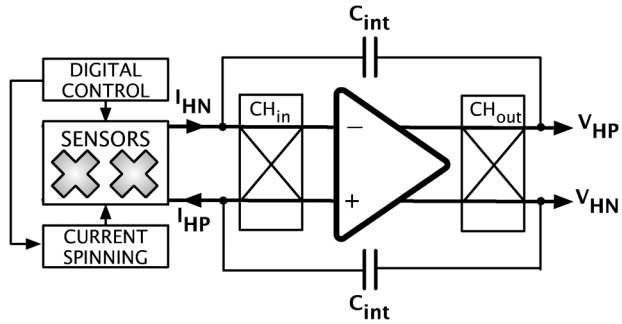

Fig. 3. Block diagram of the proposed magnetic current-mode Hall sensor microsystem.

The first scheme is pseudo-differential, the other fully differential. For all of them, the equivalent offset of the measure circuit causes an offset in the differential current. If significant, it is necessary to compensate for the limit. In order to quantify the consequence of the offset, we can use the equivalent circuit of the sensor depicted in Fig. 2(d), [9]. Simple calculations show that an offset V_{os} unbalancing nodes C and D causes a current difference, ΔI, equal to

$$\Delta I = V_{os} \frac{R_S + 3R_D}{R_S R_D} \tag{1}$$

It is proportional to the offset voltage and is independent on the bias current. A fitting of the designed Hall sensor with the electrical model of Fig. 2(d) provides $\mathrm{R}_S = 18$ kΩ and $\mathrm{R}_D = 8$ kΩ. With these values, an offset of 4 mV causes a current imbalance $\Delta \mathrm{I} = 1.67$ μA. If the current sensitivity is 3%/T, it is required to use $\mathrm{I}_B = 55.67$ mA for generating equal signal current with a 1-mT magnetic field.

This project avoids the limit by using a chopper stabilized op-amp [10]. Fig. 3 shows the block diagram of the architecture. It uses two current-driven Hall plates to form a twin horizontal Hall sensor. They provide two differential output currents, I_{HN} and I_{HP}, which are integrated for a given time-slot. The digital unit controls the circuit and generates the phases necessary for chopper and current spinning operations.

A. Horizontal Current Mode Twin Hall Sensor

For an optimal design of the Hall structures, it is necessary to account for noise, offset, and sensitivity. This has been done using the software COMSOL Multiphysics. Reference [9] shows that the cross-shaped layout is a good choice for a minimum noise, residual offset and good sensitivity. In addition, the symmetry of the cross-shaped layout enables current spinning [11].

Fig. 4 shows the four configurations for each 90° rotation. The graph at the bottom of the figure conceptually shows the output offset during the four states. Every fourth phase, the average of the offset is zero.

Since simulations show that the optimal sensitivity is for relatively low doping, an N-well layer makes the Hall plate. A shallow highly doped P^+ top layer that covers the surface of the active area significantly reduces the 1/f noise. The four contact

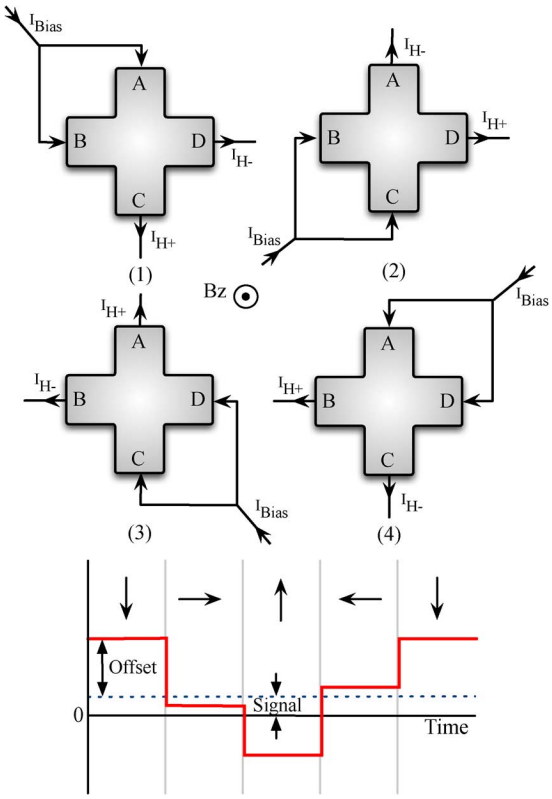

Fig. 4. Current spinning technique and output offset of a single cross-shaped Hall plate during the four possible states.

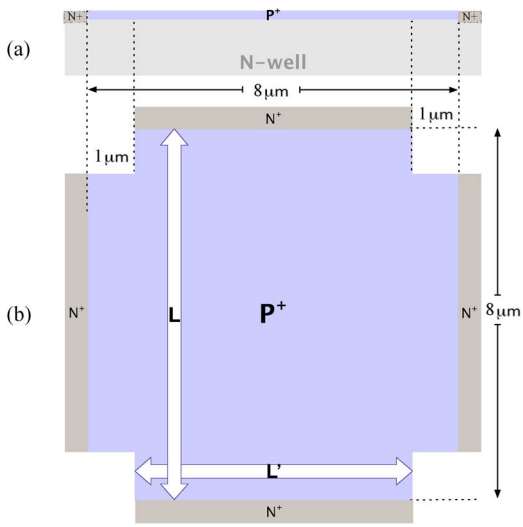

Fig. 5. Model geometry of a cross-shaped Hall plate in a CMOS technology: (a) cross view and (b) top view.

regions in the N-well diffusion are N^+. Fig. 5 shows the geometry of the Hall plate; Fig. 5(a) shows the cross section while Fig. 5(b) shows the top view. The device is 8 μm $\times$ 8 μm and the four contacts are 0.5-μm wide.

Since the output currents are the signal plus half of the bias current, $I_{bias}/2$, it is necessary to subtract this term from the two outputs. This is done by using a twin cross-shaped Hall sensor, as shown in Fig. 6. The bias current, I_{bias}, is injected into two shorted terminals of the cross shaped plate A and the same amount of current is drained from two shorted terminals of the Hall plate B. With no magnetic field, the sensor structure is balanced, thus making null the output currents, I_{HN} and I_{HP}.

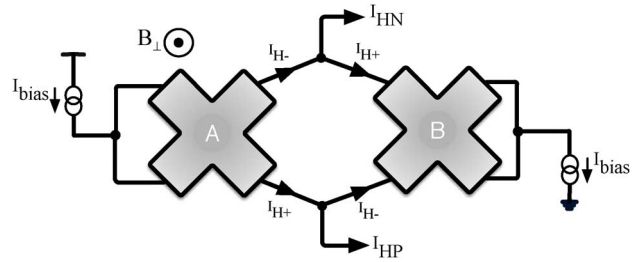

Fig. 6. Twin current mode Hall sensor structure.

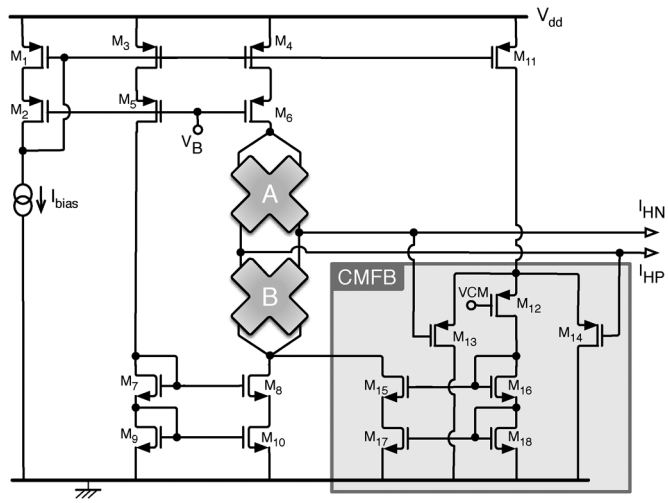

Fig. 7. Schematic diagram of the twin sensor with biasing and common mode feedback circuits.

When an external magnetic field orthogonal to the sensor plane, $B_\perp$, is applied, the sensor is unbalanced and, as mentioned, the output currents become

$$I_{H+} = \frac{I_{bias}}{2} + \frac{I_{Hall}}{2} \tag{2}$$

$$I_{H-} = \frac{I_{bias}}{2} - \frac{I_{Hall}}{2} \tag{3}$$

where the currents, I_{Hall}, proportional to the current mode sensitivity, depend on the sensor geometry, physical parameters, and temperature.

As evident from Fig. 6, the differential output current is twice the Hall current. The solution is also suitable for the current spinning technique.

B. Twin Sensor Current Bias

The schematic of Fig. 6 uses two nominally equal current generators. A possible mismatch between them causes an unwanted common mode current at the outputs. The limit is avoided by the feedback control shown in Fig. 7. The high compliance cascode P-channel current mirror replicates and injects the bias current, I_{bias}, into the Hall sensor A. The N-channel cascode current mirror sinks a current lower than the nominal value, thus leaving room for the common mode control. The missing current is determined by the common mode feedback (CMFB) made by the P-channel differential pair $M_{13} - M_{14}$, sensitive to the common mode voltage of the output terminals.

C. Current Spinning

The current spinning technique, [12], periodically interchanges output and supply terminals of Hall plates so that the bias current enters in each pair of terminals whereas a

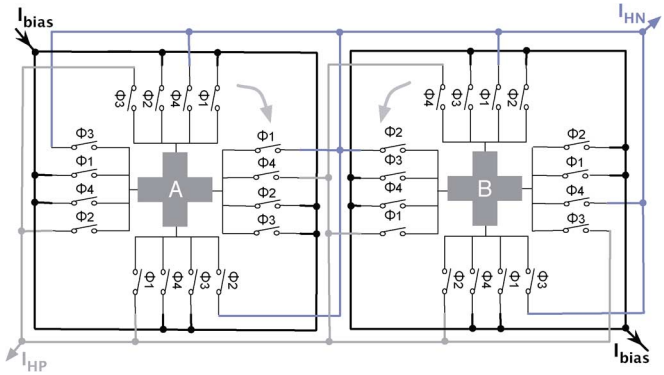

Fig. 8. Hall plates with switches configuration for current spinning.

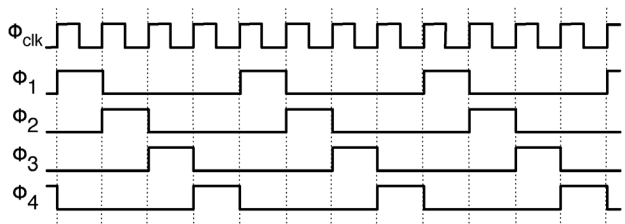

Fig. 9. Phases timing diagram for current spinning operation.

corresponding offset appears at the output. For the twin structure, the sensor A rotates clockwise while the sensor B rotates anti-clockwise, as shown in Fig. 8. At the end of a full spinning cycle, the average of the offset becomes zero. The spinning can be realized with a clockwise or an anti-clockwise rotation. Since there is the possibility of second order asymmetry, the direction of the spinning rotation is programmable by changing the clock phase generator. Fig. 8 shows the two sensors and related switches. Phases Φ_1, Φ_2, Φ_3, and Φ_4 (given in Fig. 9) drive them so that during each phase two sensor terminals are connected to the bias generators and the other two to the outputs. The switches are complementary CMOS pairs.

D. Readout Circuit

The block diagram of Fig. 3 includes an op-amp. Its integration of the signal current over the capacitances C_{int} gives rise to complementary voltage ramps at the output. However, its finite gain, A_0, affects the accuracy of the measure because of the voltage at the input terminals $(-\mathrm{V}_{out}/\mathrm{A}_0)$ which unbalances the magnetic sensors. If the maximum swing of the complementary ramps is ± 0.4 V, a DC gain higher than 100 dB unbalances the input by ∓ 4 μV. This high gain is obtained with the fully differential scheme of Fig. 10. It is a two stages amplifier. Each stage is a cascode. The coupling between the two stages uses source followers to accommodate the voltage room necessary for the current chopping of the first stage. The common mode feedback uses a resistors averaging network. The value of R_{CM} is large (1 MΩ) and does not affect the gain of the second stage. The simulated DC gain is 109 dB and the GBW is 11 MHz. The chopping frequency used in the chopper is such that an integer number of spinning periods is performed within each chopping phase. Therefore, the offset affects an integer number of spinning cycles with positive sign and the same number of spinning periods with the negative sign. Moreover, the integration of the signal lasts for an integer number of chopping periods.

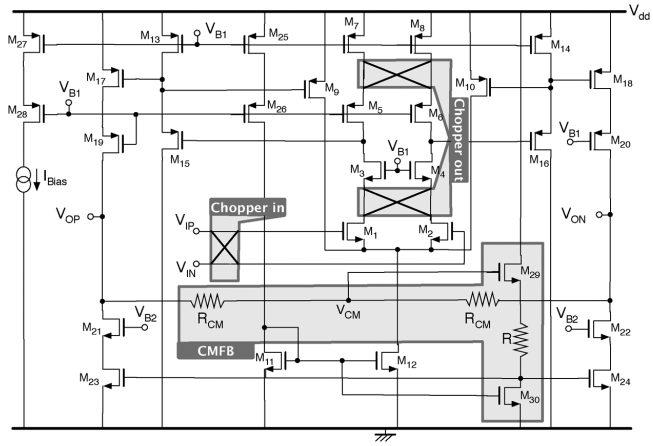

Fig. 10. Schematic diagram of the two stage fully differential amplifier.

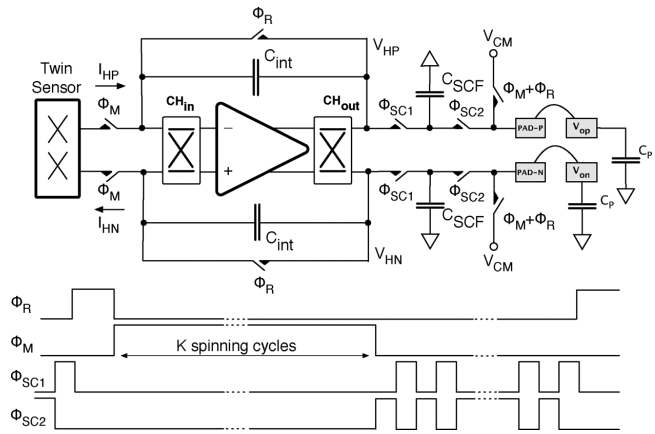

Fig. 11. Simplified block diagram of the proposed microsystem with output SC filter and control signals of a complete read-out operation.

E. Digital Control Unit, Output SC Filter, and Read-Out Operation

A digital control unit generates all the signals necessary for current spinning, reset, integration cycles, chopper and output switched-capacitor filter (Fig. 11). It uses an external master clock of $f_{clk} = 1$ MHz.

The read-out operation starts with a reset (phase Φ_R shown in Fig. 11) of the integrating capacitors, C_{int}. The measure (phase Φ_M) lasts for an integer number, K, of current spinning cycles, digitally controlled. The amplifier differential output voltage becomes

$$V_{out,\pm} = \pm \frac{|I_{HP}|8K}{C_{int} f_{clk}} \tag{4}$$

At the end of the integration period, the twin sensor output currents I_{HP} and I_{HN} are disconnected from the readout circuit and the output voltages V_{HP} and V_{HN} are available for further processing or for output sampling.

A typical processing chain moves the signal generated by the front end into the digital domain by means of a suitable A/D converter. This design does not include the conversion on chip and provides at the output the analog differential signal. In order to avoid output buffers, two switched-capacitor RC networks drive the output pins as shown in Fig. 11. During the integration phase (Φ_M), the op-amp is load-free and the output pins are pre-charged to the common mode voltage, V_{CM}. At the end of the integration phase, the small switched capacitors C_{SCF}

TABLE II
MODEL PARAMETERS

Symbol	Value	Parameter
n [cm^{-3}]	7.38*e*16	Carrier Concentration
μ [cm^2/Vsec]	1058	Mobility
sigma0 [S/m]	$qn\mu$	Silicon Conductivity
r_H [m^3/C]	$-1/(qn)$	Hall Coefficient
B_z [mT]	0 ~ 20	Magnetic Field
V_0 [V]	0.02	Applied Voltage
t_si [m]	0.5*e* − 6	Silicon Thickness
I_0 [μA]	12	Input Current

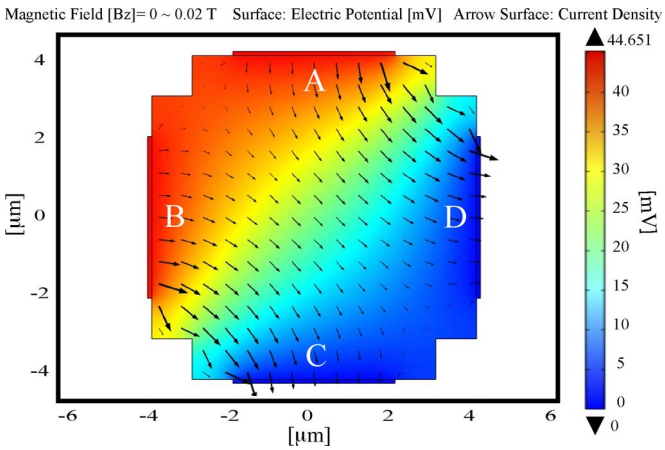

Fig. 12. COMSOL Multiphysics simulation results of a single current mode cross-shaped Hall sensor.

exponentially charge the output pins under the control of signals Φ_{SC1} and Φ_{SC2} (easily achievable by masking the master clock with the signal Φ_M).

III. SIMULATION RESULTS

The study, design and performance optimization of the single Hall plate and the twin sensor have been carried out with the software COMSOL Multiphysics. It is used to estimate the currents distribution in the Hall devices with and without magnetic field and to account for possible geometrical mismatches. Table II summarizes the parameters used in the simulations. They correspond to the available technology.

A. Single Horizontal Cross-Shaped Hall Plate

Fig. 12 shows the geometry of a single Hall plate with width and length of 8 μm. The figure also shows the surface electrical distribution when a magnetic field of 20 mT is applied and the arising current density distribution (indicated by the arrows). The simulation uses the nominal bias current of 12 μA injected in terminals A and B. The voltage drop across the device is 44.6 mV. The surface electric potential distribution seems symmetrical, but the small asymmetry caused by the magnetic field determines a difference in the output currents, as Fig. 13 shows. A swing of the magnetic field from 0 to 20 mT gives rise to a linear response with maximum differential output current of 3.4 nA. The resulting sensitivity is 1.42%/T. The value can be increased by using a well with lower doping and lower thickness.

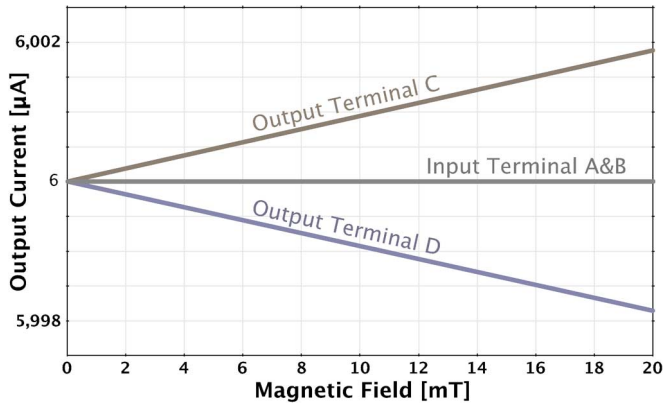

Fig. 13. Simulated input and output currents of the current-mode Hall plate without any mismatch.

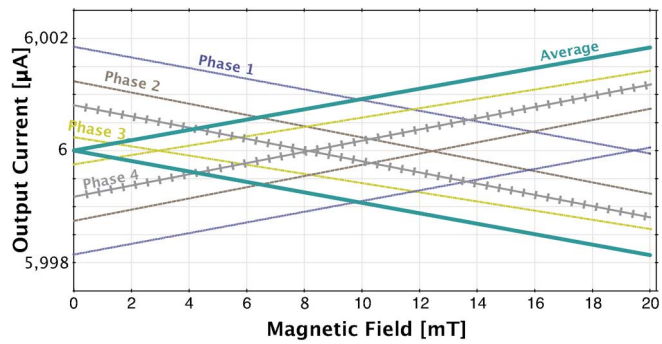

Fig. 14. Simulated average output currents (I_{H+} and I_{H-}) of current mode Hall sensor plate with mismatch and current spinning.

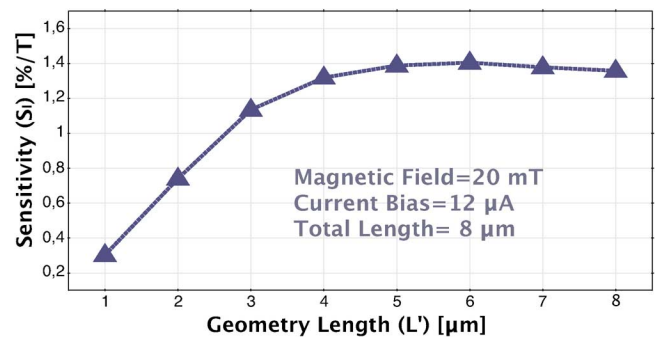

Fig. 15. Simulated sensitivity as a function of the Hall plate width.

Fig. 14 shows the sensor responses in the four spinning connections with the arm B 0.01-μm longer than the others. The current mismatch with zero magnetic field is, in the worst case, equivalent to the full scale signal. However, the spinning makes the average equal to zero, as indicated by Fig. 14.

The Hall current and, hence, the sensitivity depends on the geometry of the device and on physical parameters. It is given by

$$S_I = G\frac{r_H}{qnt} \tag{5}$$

where G is the geometry parameter, r_H the Hall factor, t the thickness of the sensor, and n the carrier concentration, [1].

COMSOL Multiphysics simulations determine the optimal dimensions of the cross-shaped sensor. This study uses a total length of 8 μm and the inner square varying from 1 to 8 μm. Fig. 15 shows the results for a constant bias current of 12 μA and 20-mT magnetic field. The sensitivity goes from a minimum of 0.37%T^{-1} to an optimum value (1.42%T^{-1}) for L′ = 6 μm.

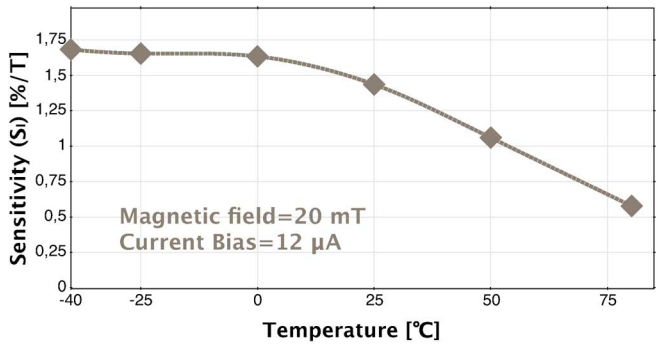

Fig. 16. Simulated sensitivity as a function of the temperature.

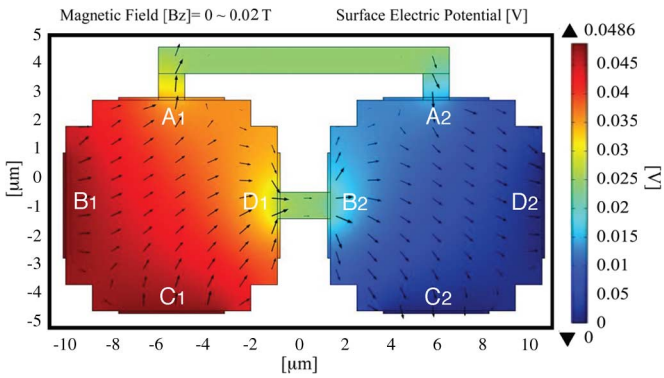

Fig. 17. COMSOL Multiphysics simulation results of a twin current mode cross-shaped Hall sensor.

The sensitivity depends on temperature because the Hall factor r_H depends on temperature. This because of the variation of carriers concentration, n, and carriers mobility, μ, [13]. COMSOL Multiphysics simulations verify the expected behavior, as Fig. 16 shows. The figure considers the relatively low temperature range, from -40 °C to $+85$ °C. Even for this simulation the bias current is 12 μA and the applied magnetic field is 20 mT. Since the sensitivity significantly changes above the room temperature, as it happens for all the Hall sensors, suitable correcting methods will be necessary.

B. Twin Horizontal Cross-Shaped Hall Plate

Fig. 17 shows the model geometry of the simulated twin Hall sensor. The figure shows the simulated surface electrical distribution and the current distribution when a perpendicular magnetic field of 20 mT is applied. The plot is for a bias current of 12 μA injected in terminals B_1 and C_1 of the first plate and drained from terminals C_2 and D_2 of the second plate. In the same conditions, Fig. 18 plots the two output currents, I_{HP} and I_{HN}, as a function of the magnetic field applied in the range from 0 to 20 mT. The result confirms the expectations.

IV. Measurement Results

The proposed sensor microsystem has been fabricated in a standard 0.18-μm TSMC CMOS process with 6 metal and 2 poly layers. The chip microphotograph including the 24 pins is shown in Fig. 19(a). The chip area is 1.08×1.08 mm^2. Fig. 19(b) shows a detail of the microphotograph with back-annotated layout of the sensor plates and relevant switches: they occupy an active area of 80×50 μm^2. The readout circuit area is 300×200 μm^2. The supply voltage of the entire chip is

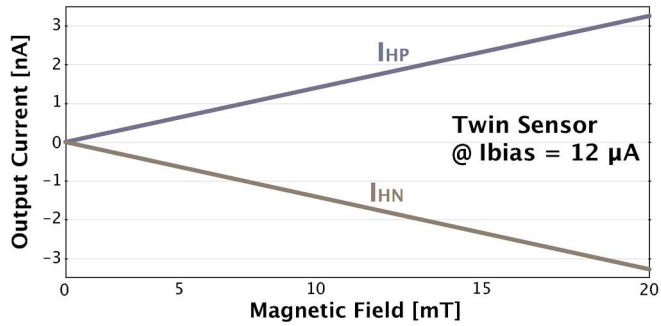

Fig. 18. Simulated output currents (I_{HP} and I_{HN}) of the twin Hall sensor as a function of the magnetic field.

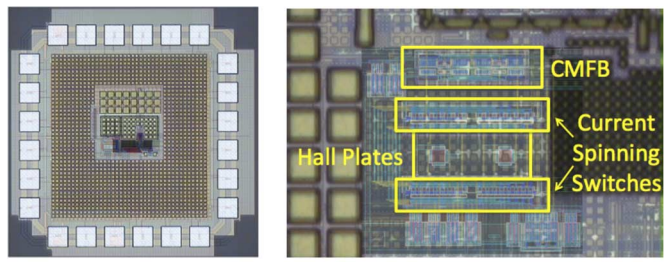

Fig. 19. Hall sensor microphotograph: (a) whole chip including pads and (b) detail of the sensor plates area (with back-annotated layout).

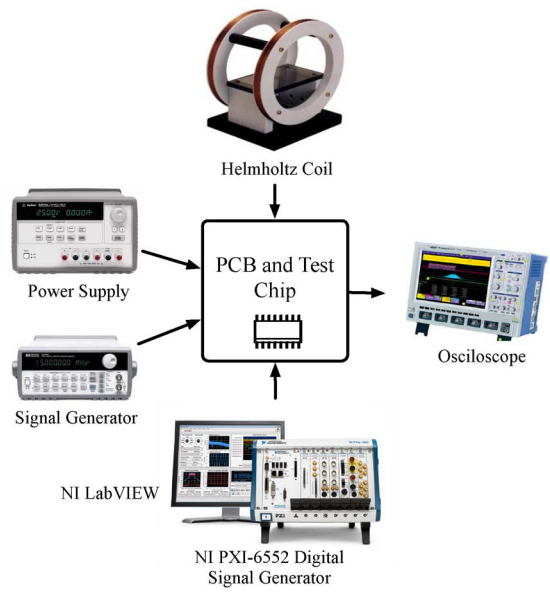

Fig. 20. Used measurement setup.

1.8 V and the master clock is at 1 MHz. The test chip permits to measure the sensor performance with [14] and without [11] the readout circuit.

Fig. 20 shows the measurement setup. A digital signal generator/analyzer (NI PXI-6552) provides the master clock. Two Helmholtz coils connected in series produce a nearly uniform magnetic field in middle of the two coils, [15]. The applied magnetic field ranges from 0 to 10 mT.

Fig. 21 plots the measured differential sensor output current, I_{Hall}, before the sensor interface as a function of the bias current for three different magnetic fields, 5 mT, 7.5 mT, and 10 mT. I_{bias} ranges from 0 to 48 μA. The figure shows that within the measure accuracy the sensor is linear with respect to the applied magnetic field.

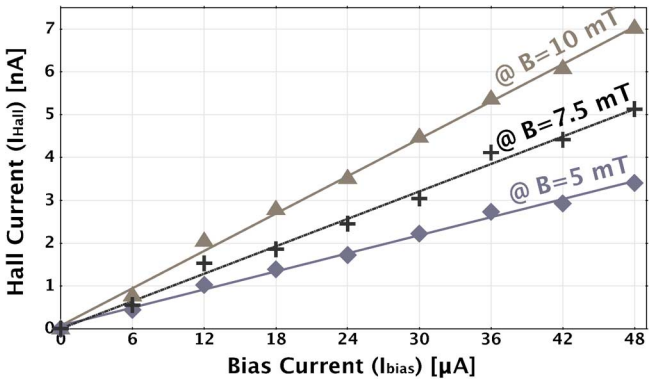

Fig. 21. Measured sensor output current before interface as a function of the biasing current at different magnetic fields.

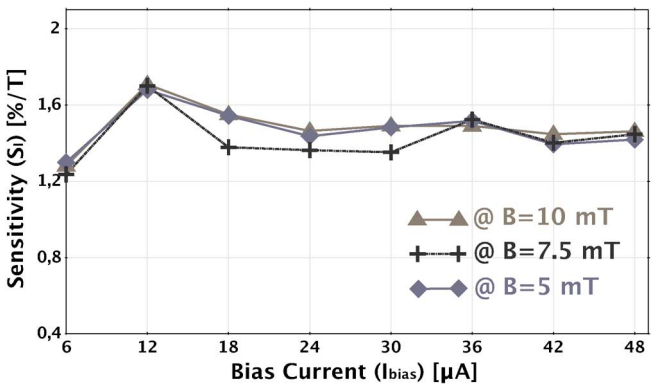

Fig. 22. Measured sensor sensitivity without interface as a function of the biasing current at different magnetic fields.

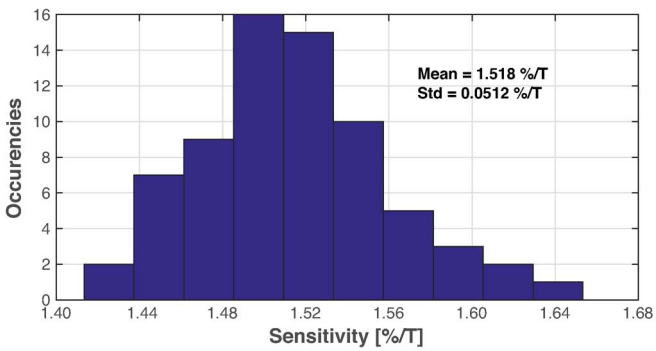

Fig. 23. Distribution of the sensitivity after 70 repeated measurements for a bias current of 30 μA and a magnetic field of 5 mT.

Fig. 22 gives the sensitivity (measured before the sensor interface), S_I, as a function of the sensor bias current (ranging from 6 to 48 μA) for the above external magnetic fields.

Fig. 23 plots the distribution of the sensitivity (measured before the sensor interface), S_I, obtained after 70 measurements repeated on the same sample in the same conditions (sensor bias current and magnetic field equal to 30 μA and 5 mT, respectively). The achieved average value is 1.518%T^{-1} while the standard deviation is 0.0512%T^{-1}, equivalent to 11 bit.

Fig. 24 shows the differential output voltage of the whole microsystem (twin sensor with readout circuit) as a function of the applied magnetic field. It ranges from 0 to 10 mT. The bias current is 36 μA. The sensors offset is less than 50 μT and the differential signal has a slope of about 8 mV/mT. The nonlinearity error, as Fig. 24 shows, is always lower than $\pm 0.2\%_{FS}$ ($\pm 20\,\mu$T). The used integrating capacitor is 4 pF and the integration is for 64 clock periods, with a conversion rate of 15.625 kS/s.

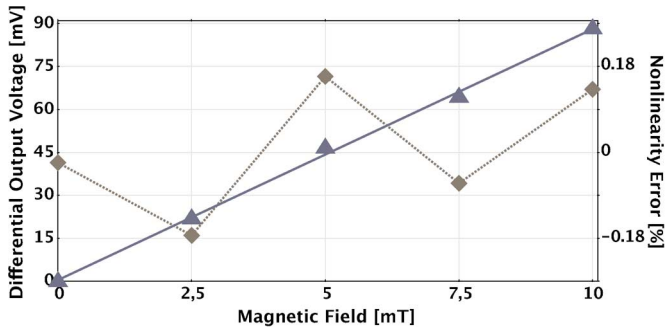

Fig. 24. Measured sensor differential output voltages as function of the magnetic field and its nonlinearity error.

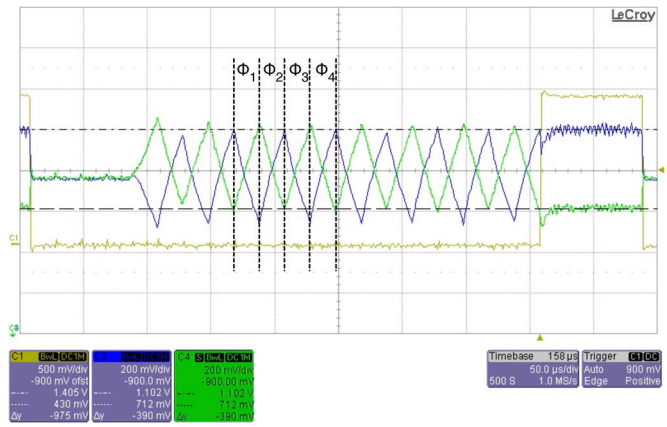

Fig. 25. Output voltages transient response measured with active probes.

TABLE III
PERFORMANCE SUMMARY AND COMPARISON TABLE OF THIS WORK WITH RECENTLY PUBLISHED CMOS HALL SENSORS

	[4]	[16]	This Work
Year of Publication	2013	2014	2015
CMOS Technology	0.35 µm	0.18 µm	0.18 µm
Hall Plate Shape	Square	Cross	Cross
Plates Number	4	4	2
Mode of Operation	Voltage	Voltage	Current
Spinning Frequency	20 kHz	1 kHz	250 kHz
Supply Voltage	3.3 V	5 V	1.8 V
Max Sensitivity	50 mA/T	50 mV/T	1660 V/A/mT
Residual Offset	40 µT	25 µT	< 50 µT
Sensor Bias Current	1 mA	350 µA	12 µA
Power Consumption	6.6 mW	N/A	120 µW
Non-linearity	< 0.08%	N/A	< 0.2%
Chip Area	11.55 mm^2	N/A	1.16 mm^2
Active Area	N/A	N/A	0.06 mm^2

Fig. 25 shows the integrator output voltages measured with low capacitive active probes. The master clock frequency has been reduced to 50 kHz to emphasize the integration of the offset each spinning period. It results spur signals as large as few hundreds of millivolt cancelled out at the end of the spinning cycle. For a bias current equal to 48 μA and an applied magnetic field of 7.5 mT, the final differential output voltage is the expected 390 mV.

Table III summarizes the microsystem performance for a bias current of 12 μA and provides a comparison of this work with other two recently published CMOS Hall sensors. The overall

measured power consumption is about 120 μW. The readout section consumes 54 μW. The sensor and the relevant switches for current spinning measured power consumption is 65 μW.

V. Conclusion

This paper described a magnetic current-mode Hall microsystem. Two Hall plates operating in the current mode and able to provide differential currents at the output nodes have been fabricated in a standard 0.18-μm CMOS process. The use of a low-noise chopper stabilized operational amplifier enables the integration of the signal current and ensures good voltage sensitivity. The measurement cycle starts with a reset phase followed by the integration of a multiple of full current spinning cycles. Measurement results show that the Hall sensor can achieve a sensitivity after the sensor interface better than 1660 V/A/mT when the magnetic field is in the range from 0 to 7 mT ($I_{bias} = 36$ μA, 512 T_{CK}). The use of the crossed-shaped Hall plates and a current-mode approach enables current spinning technique for offset cancellation. The overall measured offset, power consumption and the achieved voltage sensor sensitivity after the sensor interface are remarkable.

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