UNIVERSITÀ DEGLI STUDI DI PAVIA

FACULTY OF ENGINEERING

Department of Electrical, Computer and Biomedical Engineering

Ph.D school in Electronics, Computer Science
and Electrical Engineering
XXIX Cycle

Design and automated characterization of a 10 bit SAR ADC for diffraction imaging at X-ray FELs

Advisor:
Prof. Carla Vacchi
Prof. Lodovico Ratti

Ph.D Coordinator:
Prof. Paolo Di Barba

Ph.D thesis of
Luca Lodola

Academic year 2015/2016

Contents

Introduction

This thesis work presents the design and the characterization of an interleaved Successive Approximation Register (SAR) Analog to Digital Converter (ADC), part of the readout channel for the PixFEL detector. The PixFEL project aims at substantially advancing the state-of-the-art in the field of 2D X-ray imaging for applications at the next generation Free Electron Laser (FEL) facilities, through the adoption of cutting-edge microelectronic technologies and innovative design and architectural solutions. The unprecedented features of X-ray free electron lasers, capable of producing photon pulses with outstanding brightness and ultra-short duration, promise to revolutionize a number of research fields, including structural biology and chemistry, material science and nuclear and molecular physics. To take full advantage of the potential of X-ray FELs, suitable electronic instrumentation, compliant with the X-ray beam properties and with the experiment specifications, needs to be designed. The new instrumentation has to satisfy severe requirements in terms of space and amplitude resolution, frame rate, input dynamic range and frame storage capability. The PixFEL project is pursuing the development of a 110 μm pitch, four side buttable tile for a large area X-ray imager. For this purpose, the PixFEL collaboration is developing the fundamental building blocks of the front-end readout channel covering the 1 to 10^4 photons input dynamic range at both 1 keV and 10 keV of energy with the capability to be operated at the high (1 MHz or larger) rates foreseen for the future X-FEL machines.

The first chapter begins with a brief description of the operating principle at FELs and their main applications to the scientific research. An overview of the state-of-the-art in FEL instrumentation is presented, paying particular attention to the PixFEL project, described from its goals to the details about the sensor and the analog front-end channel, already designed, fabricated and tested.

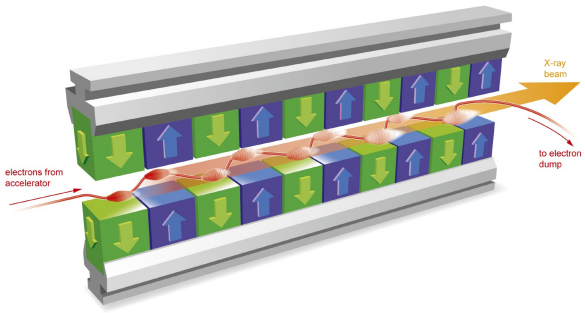
The second chapter deals with the main topic of this thesis work: the design of the 10 bit analog to digital converter, which digitizes the signal processed

by the PixFEL analog channel. After an introduction on the motivation for in-pixel A-to-D converters, the interleaved SAR architecture used for the ADC is discussed. Its design is then described in detail starting from the split capacitor DAC (Digital to Analog Converter) based on the charge redistribution technique, to the bootstrap switches, the dynamic latched comparator and the SAR logic. The simulation results are presented, together with the layouts of single blocks and of the overall ADC.
Eventually, the third chapter presents results from the ADC characterization. At first the test chip is described, than the automated measurement setup is discussed from the test board to the instrumentation used for chip characterization. Test results of ADCs with different layout options are reported, from static measurements, such as offset, gain error or non-linearities, to noise performance and dynamic measurements (Signal to Noise and Distortion Ratio and Equivalent Number of Bits).

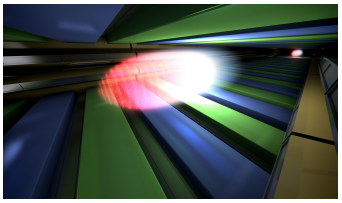
Chapter 1

X-ray Free Electron Lasers

One of the main trends of modern scientific and technological research is investigating the very small, the extremely fast phenomena occurring at the nanometer scale and the complex structure of organic and inorganic materials. Nanotechnologies require the capability to perform measurements on and manipulate objects such as biological macromolecules or viruses. The time scale of the dynamic processes at such dimensions is defined by the femtosecond vibration of an atom in a chemical bond. Understanding the states of matter is of fundamental importance for the development of advanced materials with innovative functionalities. Free electron lasers (FEL) are bound to become the predominant tool for the investigation of natural phenomena in this research topic. A number of research centers, in Europe, the United States and Japan, have started studying, designing and building free electron laser facilities. A wide set of research programs is being outlined. Some of these facilities, like the SLAC Linear Coherent Light Source (LCLS), in Stanford [1], or the SPring-8 Compact SASE Source (SCSS), in Japan [2], are already operational. Other facilities, such as the European-XFEL [3], are currently under construction or, like in the case of the SwissFEL [4], the upgrade of the LCLS (LCLSII) [5], or Iride [6], are finalizing their proposed design.
In this chapter the operating principle of FELs is described, together with their main applications to research. An overview of the FEL imagers requirements is also presented. Then, an overview of the state of the art in the FEL instrumentation area is given. The last part of the chapter is dedicated to the PixFEL project.



(a)



(b)

Figure 1.1: Principle of free electron lasers: electron bunches, first brought to high energies in a superconducting accelerator, then fly on a slalom course through a special arrangement of magnets (the "undulator" (a)), in which they emit laserlike flashes of radiation, organizing themselves into a multitude of thin disks (b) [3].

1.1 Operating principle of FELs

The FEL functioning is based on the acceleration of a bunch of electrons by means of a linear accelerator. The electron bunches are generated by knocking the particles out of a piece of metal, by photoelectric effect, using a conventional laser. The electron source has to meet very challenging specifications, as even the smallest irregularities at the beginning would amplify in the course of the acceleration process and result in an electron beam of insufficient quality. The electrons are accelerated at nearly the speed of light in special cavities some kilometers long, the so-called resonators. In these resonators, an oscillating microwave transfers its energy to the electron bunches, which are brought up to several GeV, sometimes in excess of 10 GeV. The resonators are made of a superconducting metal: when they are cooled to a temperature near to absolute zero, they lose their electrical resistance. Electrical current then flows through the resonators with no losses whatsoever and nearly the entire electrical power is transferred to the particles. The accelerated electrons then race through so-called undulators, periodic arrangements of magnets that force the electrons onto a tight slalom course (Fig. 1.1). In the process, each individual electron emits X-ray radiation. The wavelength of the emitted radiation, λ_r is proportional to the spatial period of the magnetic field in the undulator, λ_u,

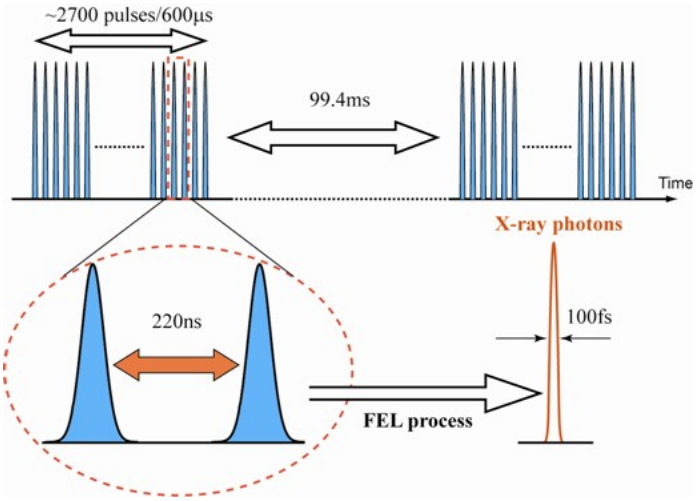


Figure 1.2: European XFEL bunch structure.

in particular

$$\lambda_r \propto \frac{\lambda_u}{2\gamma^2}, \tag{1.1}$$

where γ is the relativistic Lorentz factor [7]. The amplification process, called SASE (Self-Amplified Spontaneous Emission) is induced by the interaction of the X-ray radiation with the electrons: because the radiation is faster than the electrons speeding along their slalom path, the radiation overtakes the electrons flying ahead and interacts with them along the way, accelerating some of them and slowing others down. As a result, the electrons gradually organize themselves into a multitude of thin disks, spaced by one wavelength (Fig. 1.1(b)). The key property of this process is the fact that all of the electrons in a given disk emit their light in phase and every disk emits light in phase with the others. This produces extremely short and intense X-ray flashes with the properties of laser light. As an example, Figure 1.2 shows the X-ray bunch structure at the European XFEL: the XFEL machine generates macro-bunches with a repetition rate of 10 Hz; every macro-bunch is composed of a train of about 2700 X-ray pulses with a time distance of about 220 ns.
Starting from the same linear accelerator, FEL facilities can have several undulators, i.e. different light sources providing X-ray flashes with different properties, suitable for disparate types of experiments. Also, FEL operation may change significantly from one facility to the other. For example while the European XFEL is operated in a burst mode (see Fig. 1.2), on the other hand,

Project	Start of operation	Beam energy [GeV]	Photon energy [keV]	Burst repetition rate [Hz]	Number of X-ray pulses/burst @inter-bunch period
FLASH	2005	1.25	0.03-0.3	5	800@1 μs
LCLS	2009	14.5	0.3-10	120	1
SCSS	2010	8	4.5-15	60	1
Fermi	2010	2.4	0.01-0.06	10	1
SwissFEL	2016	5.8	12	100	2@50 ns
Eu-XFEL	2017	17.5	0.4-20	10	2700@220 ns
LCLSII	$>$ 2020	4-14.5	0.2-25	120-10^6	1

Table 1.1: Main features of some existing and future FEL facilities.

the LCLS facility in Stanford is operated at a constant pulse rate of 120 Hz. Table 1.1 shows the main features of some FEL, some already operational, some others still under construction.

1.2 Research base with FELs

FEL facilities can provide high intensity beams of ultrafast X-rays, whose energies range from tens of eV to tens of keV and wavelengths between 10 nm and 0.1 nm. A quite broad science base is accessible at FELs [8, 9, 10]. A non exhausting list of research areas is reported:

- **Comprehending the structure of biomolecules**. Already, the structure of biomolecules can be investigated in detail. However the X-ray radiation sources used for these analysis are too weak to allow the study of single molecules, so crystals in which the molecules are aligned in regular order have to be grown. These crystals are used for a group picture such that the individual images reinforce one another enough to create a serviceable result through the so called Bragg peak effect. Nevertheless for many biological substances that crystallization is not feasible. The X-ray FELs introduces new opportunities in this respect. The intensities of

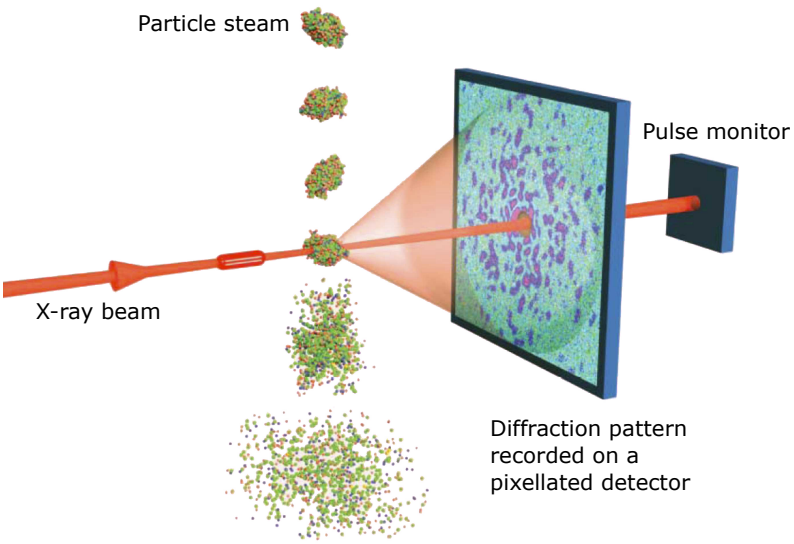


Figure 1.3: The very short X-ray flashes of FELs enable to collect scattering image before Coulomb explosion destroys the molecule [4].

their X-ray flashes are so high that small crystals of bad quality can also be used or even do away with crystallization altogether. Furthermore the duration of the flashes is sufficiently short that the molecule hardly changes during the exposure (Fig. 1.3). The large forces generated by the strong incident light brings the molecule to decay only after the X-ray flash has passed the sample and the picture of the atomic structure has been taken. In addition, the ultrashort X-ray flashes allow to follow from instant to instant the motion of molecules.

- **3D exploration of the nanoworld**. The progression in the miniaturization of technology demands an ever better understanding of the nanoworld. Computer chips and optical, magnetic, and biological sensors are approaching dimensions of just a few nanometres. At this scale, materials exhibit surprising new properties: copper becomes transparent, aluminum inflammable, gold liquid, silicon conductive. X-ray flashes of the X-ray FELs enable to find the properties of such small systems. For instance, they can study the relationship between the form and behavior of different materials at the nanoscale.

- **Filming chemical reactions**. Many chemical reactions are very rapid:

durations of the order of a hundred of femtosecond are not unusual. Changes occur at the atomic level on this time scale in some bio-chemical processes. X-ray flashes at FELs will enable to film this fast processes with unprecedented accuracy. Since the duration of the flashes can be as short as 100 fs, snapshots can be captured without moving details appearing blurred. Atomic details can be perceptible thanks to the short wavelengths. These outstanding properties of the beam available at FEL facilities will thus enable to examine and understand the exact mechanisms of a chemical reaction on the atomic and molecular level. In those experiments a time-dependent process is reconstructed by using the pump-probe technique [11]: the process is initiated and after a time delay, a synchronized X-ray pulse probes the excited sample. The measurement is then replicated with different delay times.

- **Reversing magnetization**. When materials reverse their magnetization, this is caused by a complex interaction between the electrons in the materials. By the use of X-ray FEL flashes, these very fast phenomena can be studied with very high resolution in terms of time and space. A better understanding of how magnetization is created and how it can be reversed is of interest for the miniaturization of electronic devices. Technology is now reaching limits set by physical boundary conditions, with respect to the size of memory devices and the time needed to write or read data.

- **Observing small objects in strong fields**. New experiments with atoms, molecules, ions or clusters became feasible thanks to X-ray flashes of FELs. Taking advantage of the high intensity of the flashes, previously unknown states of particles can be explored. Hence X-ray FELs create an unequaled environment for basic research, allowing new profound perception into processes which could not be investigated so far. Beside the progress in basic research, these insights can lead also to new products, for instance novel catalysts or electronic devices controlled by X-ray radiation.

- **Investigating extreme state of matter**. In physics knowledge about matter in extreme states is quite poor, i.e. at a pressure of a billion atmospheres and temperatures up to 10^4 Celsius degrees. Theoretical models are no longer valid in that conditions and cannot be used any more. That high pressures and temperatures can be found inside large planets like Jupiter, or throughout igniting the so-called inertial confinement fusion using laser light. The very little experimental data about these states

imply an extreme difficulty in theoretically describing them. The possibilities introduced by X-ray FELs consists in both creating and studying matter in that extreme states. The benefits from these new experiments can be used in very different scientific fields, for example planetary science and the development of new technologies about energy generation.

1.3 FEL imagers requirements

Specific instrumentation needs to be designed and fabricated to comply with the demanding specifications of the most challenging experiments at FELs, which depends on the beam characteristics and may vary from one facility to the other, or from one beam line to the other within the same facility. The main FEL application of interest for this thesis project is the two-dimensional X-ray diffraction imaging. Taking advantage of measurements with ultrashort pulses, crystallographic techniques can be applied to non-repetitive structures (including cells, viruses, and single macromolecules). With respect the diffraction from a crystal, there are not coherent addition of scattering from many identical unit cells, but the proposed XFELs are able to provide enough photons per pulse to give a measurable atomic-resolution signal. A diffraction pattern is recorded by the imager and a computer reconstruction algorithm can replace the role of a lens. Although the phase of the diffraction pattern is not detected, the reconstruction of the complex-valued image of a finite object is still possible from the far-field diffracted intensity [12].
In this section, the main specifications leading to the design and the development of a specific detector to be used at next generation FEL facilities are summarized.

1.3.1 Photon energy range

The very large energy range covered by FEL facilities cannot be dealt with a single detector or detector technology: the input signal can range from an energy of 250 eV to 90 keV. This means that rather than developing one detector per scientific application, different systems need to be developed, each one optimized for a circumscribed energy range. With direct detection in silicon, a 0.25 keV photon will only generate $250/3.62 = 70$ electron hole pairs (where 3.62 eV is the electron-hole pair creation energy in silicon). Therefore, to be able to detect single photons, both detection and amplification need to meet a noise performance well below 25 electrons (for a minimum 3σ separation between signal and noise). At the same time, a dynamic range of 10^3 or even 10^4 photons in each pixel would be desirable. Using this same system at

12 keV generating 3315 electron-hole pairs per absorbed photon implies that the available dynamic range is reduced by a factor of 50 [13]. This leads to a significant challenge for the electronic design, that has to match single photon sensitivity at 0.25 keV with a large dynamic range at 12 keV.

1.3.2 Single shot imaging

Single shot experiments are in many cases imposed and not only allowed by the very high peak brilliance of X-ray FELs. Indeed the focused beam will have a photon density so high that the sample under study will no longer be usable after a single shot. This means that every single shot will have to be handled as a different experiment and, in a single pulse, a complete X-ray scattering image has to be recorded. More than one photon has to be recorded by many pixels, in order to have an image of statistical relevance. Hence photon counting is excluded, although it is normally used to achieve desirable signal to noise ratios. Therefore X-ray detectors based on integration techniques will have to be used for single shot experiments. Concurrently, many imaging experiments require single photon sensitivity and this, once again, means that the detector specifications are closely related to the experiment.

1.3.3 Frame storage

As already mentioned before, the specific time structure in particular of the European XFEL has up to 2700 X-ray pulses, separated by 220 ns, per pulse train and with 10 pulse trains per second. This implies that, to perform single shot imaging, a complete image needs to be recorded every 220 ns (4.5 MHz) during a time period of 0.6 ms. Since up to now, current technology cannot allow to transmit a full megapixel image in 220 ns, a storage of the recorded images inside the front-end of the detector will be needed, and subsequently it will be possible to read out them during the inter train period of 99.4 ms. Hence a compromise, based on the scientific application, is needed between maximizing the number of images storable inside a pixel, and keeping as small as possible the size of the pixel.

1.3.4 Central hole

Since the focused primary X-ray beam has sufficient energy to ablate most materials, the use of small primary beam stops is not possible in front of the detectors. Hence, the need of a central hole in the X-ray imaging detectors in the forward scattering direction, which lets the direct beam pass through. The size of this hole has to be as moderate as possible in order to contain the loss

of small-angle data, of crucially importance in image reconstruction, while at the same time it has to be large enough to be compliant with occasional small fluctuations in the direct beam position.

1.3.5 Radiation tolerance

The radiation tolerance of the detectors is another issue of concern, in particular when used at the harder X-ray energies of 12 keV. In [13] a calculation of the total dose absorbed by the detector over one year in the case of the European XFEL for 12 keV photons and a 500 μm thick silicon sensor with an area of $(200 \times 200)\mu m^2$ is reported. It results to a total absorbed dose of 1 Giga Gray. For the front end electronic a tolerance to a total dose of the order od 10 MGy has to be guarantee. It has to be noticed that the radiation at which the sensor and the electronics are exposed is not uniform: it is higher around the central hole and it diminishes moving away from it.

1.3.6 Angular coverage and size of the detector

The angular resolution is another parameter that is directly determined by the experiment and that has a large dispersion among different applications. It is determined by the pixel size and the sample-to-detector distance. The highest required angular resolution of all applications is the one needed by X-ray Photon Correlation Spectroscopy experiments (XPCS). In such experiments, for practical choices of the beam size and of the photon wavelength, it can be shown that pixels not larger than 160 μm are required even if a relatively large sample-to-detector distance of 40 m is selected [13].

1.4 State of the art in the FEL instrumentation area

Instruments for experiments at FEL facilities are, at present, in different stages of development, depending, among other factors, on the expected start of operation date of the machine they are being built for. X-ray imagers features are adjusted to the specific qualities of the FEL beam line they will be working on. In the following paragraph, a short overview on the state of the art in the area of instrumentation for bi-dimensional X-ray imaging is given.

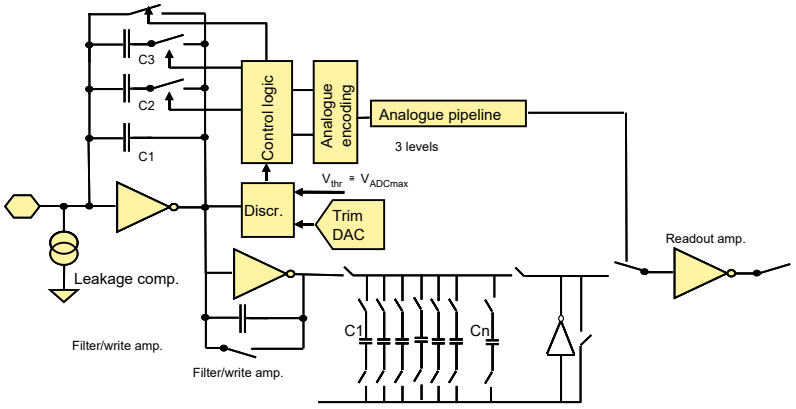


Figure 1.4: Schematic view of the pixel cell for the AGIPD detector [14].

1.4.1 Detectors for the European XFEL

The European XFEL consortium is funding the development of three different detector projects. Each of the three projects is proposing a different solution to the challenges posed by the characteristics of the X-ray beams at the EU-XFEL, in particular the wide signal dynamic range (from 1 to 10^4 photons @12 keV) and the high frame rate foreseen for the burst mode of operation, where each burst includes about 3000 bunches with an inter-bunch interval of about 200 ns.

The **Adaptive Gain Integrating Pixel Detector (AGIPD)** [14] consists of a hybrid pixel array, with readout ASICs bump-bonded to a silicon sensor. For the ASIC design a 130 nm CMOS technology is used and it takes advantage of a dynamic gain switching amplifier to cover the large dynamic range (from single photon sensitivity to 10^4 coincident photons) by selecting feedback capacitors with different size. The readout channel features an analog pipeline capable of storing the pictures at the desired 4.5 MHz speed during the 600 μs bunch train, as it is shown in Fig. 1.4. The large storage depth per pixel ($\geq$ 200 images) calls for small storage capacitors because of the limited pixel size (200×200 μm^2). While, because of the leakage current of the switches and the capacitor itself, to guarantee the long hold time (up to 99 ms) and high analog resolution large storage capacitors are required. An array of 2×8 ASICs, with 64×64 pixels per chip, are bump bonded to a

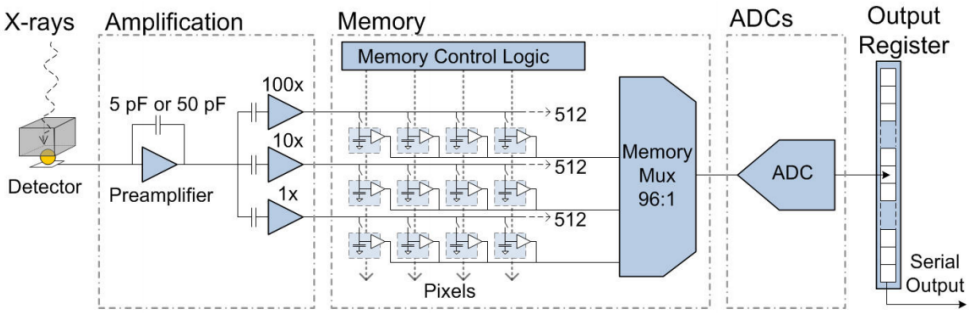


Figure 1.5: Schematic view of the pixel cell for the LPD detector [15].

monolithic pixelated silicon sensor. The detector will consist of four quadrants and a central hole for the direct beam.

In the **Large Pixel Detector (LPD)** [15] there are 8 ASICs bonded to each sensor with 512 pixelated readout channels on each ASIC. The ASIC takes advantage of the bunch structure of the European XFEL machine. The images are saved onto the ASIC in analog form at the foreseen frame rate of 4.5 MHz during the burst of pulses. During image capture, the charge readout from the sensor is input into a preamplifier with 50 pF capacitive feedback. This is a relatively large feedback capacitance and gives a high dynamic range of 10^5 photons at 12 keV. Following the preamplifier there is a series of parallel gain stages. For the smallest signals, an amplifier with a gain of 100 is used to boost the signal. An intermediate gain of 10 is used for mid-range signals and a unity gain amplifier is used for the largest signal levels. There is also an option to switch the preamplifier feedback to a 5 pF capacitor, giving a boost to the signal to noise ratio of the system at the expense of dynamic range. The output from the gain stages is saved to 512 channels of analog memory. During the readout phase, 16 on chip SAR ADCs convert the data in the analog memory and stream it off the ASIC at 100 MHz via an LVDS output. The pixel pitch is 500 μm, relatively large for some applications in the photon science field, and hence its name. Each chip will integrate 16×32 pixels, 8×1 chips are bump-bonded to a monolithic silicon sensor, obtaining 128×32 pixels tiles. Super modules will be built with 2×8 of these tiles, which are the building blocks for larger systems, with 256×256 pixels. The gap between active areas is 4 pixels on each side of tile. This is equivalent to 13.8% dead area.

The **DEPFET Sensor with Signal Compression (DSSC)** [16] takes advantage of a nonlinear response in the sensing element of the pixel to cover

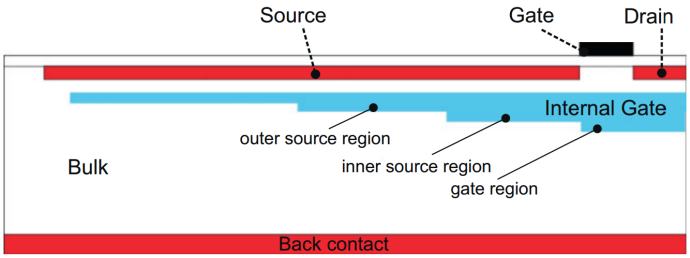


Figure 1.6: Cross-section of the DEPFET with non-linear signal response [16].

the wide dynamic range and it stores images inside the pixel through a digital memory. Although it is one of the original aspect of the project, the realization of the non linear characteristic in the DEPFET sensor demands quite a complex fabrication process, resulting in long turnaround times. Nevertheless, the DEPFET is an optimum candidate for experiments with low energy X-ray (1 Kev or smaller), thanks to its very low noise performance. The DSSC detector is constituted by hexagonal pixels with a 136 μm side, to guarantee a bump bond pitch of 200 μm. The absorbed photons generate electrons which are stored in the internal gate beneath the gate of the FET, like in a standard DEPFET. In the DSSC DEPFET design, however, the internal gate spreads beyond the gate region into the source region (Figure 1.6). As a result the first electrons generated will be stored straight under the gate, producing a large effect on the source drain current, while, subsequent electrons will be stored only in part under the gate and more and more under the source region, causing a reduced effect on the source drain current and resulting in the non-linear gain response. The front-end chip, designed in a 130 nm CMOS process, includes 64×64 elements. 8 ASICs will be bump-bonded to a monolithic DEPFET sensor. Unlike the previous two solutions, DSSC detector performs data digitization directly in-pixel through a high speed, 8-bit, single-ramp (Wilkinson) analog to digital converter. The memory counts about 600 cells per pixel. 2×8 ASICs are bump-bonded to a monolithic DSSC giving 128×512 pixels ladders. 16 ladders are finally used to achieve a 1024×1024 pixels (1 Mpixel) imager.

1.4.2 The PERCIVAL project

Actually the Pixelated Energy Resolving CMOS Imager, Versatile and Large (PERCIVAL) [17] is a monolithic pixel sensor, but it is not based on a fully

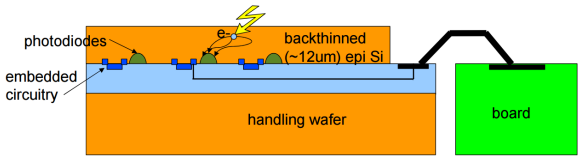


Figure 1.7: Schematic of a back-thinned MAPS sensor for the PERCIVAL project, wire-bonded to the periphery electronics board [17].

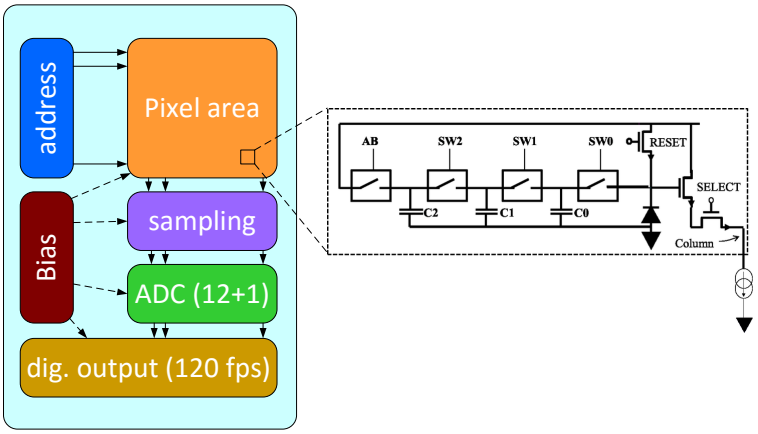


Figure 1.8: The PERCIVAL full sensor block diagram.

depleted detector, as the previous three projects for the European XFEL. The technology used is a quadruple well 180 nm CMOS process, which provides a high resistivity epitaxial layer with a thickness of 12 μm, representing the sensitive volume of the detector (Figure 1.7). From this, the maximum detectable photon energy is limited to a few keV. Besides, the equivalent noise charge is sufficiently small (about 15 electrons) that enables to detect photons with energy down to few hundreds of eV. The PERCIVAL sensor takes advantage of a multi-gain setting approach, similar to the one of the LPD, to embrace the broad input dynamic range. The ambitious goal of the project is to produce a 4000×4000 pixel detector with a 25 μm pitch, readable at a rate of 120 Hz or lower (Figure 1.8). This characteristics matches with the operation at the LCLS.

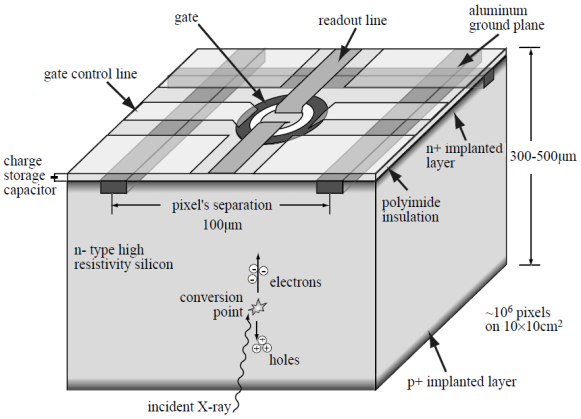


Figure 1.9: XAMPS pixel structure [18].

1.4.3 The XAMPS detector

XAMPS (X-ray Active Matrix Pixel Sensor) [18] is a 90 μm pitch monolithic pixel detector, fabricated in a high resistivity substrate (400 μm thick) (Figure 1.9). The read out is performed by a multichannel ASIC . The sensing layer integrates JFET switches, which serve the purpose to set the system in an accumulation or a data readout mode. In the accumulation phase, the switches are open and a capacitor, which occupies most of the pixel area, collects the charge released by a photon in the substrate of the sensor. The read out of the 3.5 pC charge corresponding to the full well capacitance needs a few microseconds. Hence, during the readout phase, the switches are closed and the charge is sent to the readout lines. Amplitude measurements are carried out in two stages, in order to cover the large input dynamic range. At first, the signal is digitized coarsely on-chip. Then, the digitization of the residuals from the conversion is performed by an external 14-bit ADC (Figure 1.10). In order to readout the entire detector, a few milliseconds are needed. Hence the XAMPS detector is suitable for applications at FELs like the LCLS, which is continuously operated at rates in the 100 Hz range.

1.4.4 The SOPHIAS detector

The Silicon-On-Insulator PHoton Imaging Array Sensor (SOPHIAS) [19] is an X-ray pixel detector for diffraction imaging experiments, designed with a silicon-on-insulator CMOS technology. The detector, with a 300 μm pitch, is sensitive to single photons in the 5.5-7 keV energy range. It performs frame

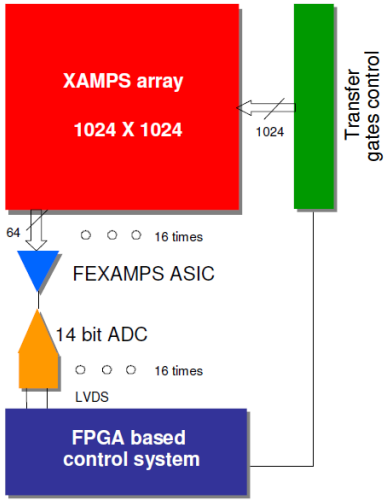


Figure 1.10: XAMPS detector system block diagram [18].

readout at a 60 Hz rate, appropriate speed for operation at the SCSS. The processing of the charge is the typical one of a CMOS MAPS scheme. The radiation hardness of this technology is usually low, but the 500 μm thick handle wafer, which is also the sensitive volume of the detector, acts as a shield, strongly mitigating that intrinsic negative characteristic. Similarly to the case of the Percival detector, a dual-gain approach is used in the SOPHIAS detector in order to cope with the wide input dynamic range. The basic chip integrates about 1.9 Mpixels.

1.4.5 CCD based detectors

Normally, CCDs are one of the first choice for imaging applications. Despite this, FEL applications needs suitable architectures to be investigated, in order to go beyond the limited readout rates (of the order of a few frames per second) of sequentially read out structures. For this purpose, for applications at the LCLS FEL experiments, almost-fully or fully-column-parallel architectures have been submitted. Front-end chips are required to amplify, sample and digitize the charge collected by the detector. An exemple, designed in a 65 nm CMOS technology, is the High-speed Image Preprocessor with Oversampling (HIPPO), which is a column-parallel CCD readout ASIC [20]. This ASIC integrates 16 channels organized in four modules of four channels each. The channel integrates an analog front-end block and a sample-and-hold circuit. A

Name	**Technology**	**Pitch** [μ**m**]	**Number of pixels**	**Input range** [**ph**]	**Energy** [**kev**]	**Noise** [e^-_{RMS}]	**Facility**
AGIPD	130 nm	200	1 M	10^4	12	300	Eu-XFEL
LPD	130 nm	500	1 M	$10^4 \div 10^5$	$5 \div 20$	1000	Eu-XFEL
DSSC	130 nm	200	1 M	6×10^3	$0.5 \div 20$	70	Eu-XFEL
Percival	180 nm	27	$10 \div 16$ M	10^5	$0.25 \div 1$	15	LCLS
XAMPS	250 nm	90	1 M	10^4	up to 8	650	LCLS
SOPHIAS	200 nm	30	1.9 M	3.6×10^3	$5.5 \div 7$	150	SCSS

Table 1.2: State-of-the-art in FEL instrumentation.

pipeline ADC shared among the four channels performs the signal digitization. Digital data are sent off chip at a rate of 480 Mb/s.

1.4.6 Summary of the state-of-the-art FEL instrumentation

Table 1.2 summarizes the main specification of the FEL instrumentation described in the previous sections.

1.5 The PixFEL project

The PixFEL project (advanced X-ray PIXel cameras at FELs) aims at substantially advancing the state-of-the-art in the field of 2D X-ray imaging by furthering the understanding of FEL experiments requirements and exploring cutting-edge solutions for fabrication technologies and for the design of detector readout architectures. The project, funded by Istituto Nazionale di Fisica Nucleare (INFN) and started in 2014, is a three year collaboration activity between University of Pavia, University of Bergamo, University of Pisa, University of Trento, Trento Institute for Fundamental Physics and Applications (TIFPA) and INFN. The long term goal of the research activity starting with the three year PixFEL project is the fabrication of a 2D X-ray camera, complying with the specifications of the experiments at the European XFEL, under

construction at DESY, Hamburg. The Eu-XFEL, with its 4.5 MHz maximum pulse rate and burst operation mode, currently represents the most challenging machine among the ones already operational, or being built or proposed around the world. While being designed with the Eu-XFEL in mind, the final instrument will retain the necessary flexibility to be compatible with the continuous operation mode typical of other FEL facilities (like the LCLS, in Stanford, US, and its foreseen upgrade). A list of the main system requirements includes:

- extremely wide dynamic range, from 1 to 10^4 photons at fixed energy, which may change between 1 keV and 12 keV according to the specific experiment;
- single photon resolution capability at small signals ($\leq$ 20 input photons) and, for a larger number of photons, a resolution much better than the limit imposed by the Poisson noise;
- a square pixel with a pitch of 110 μm, which can be reasonably assumed to satisfy the spatial resolution specifications for a wide range of experiments at FELs [13];
- capability of recording one image at rates up to 4.5 MHz and to store on chip as many images as possible, since no direct readout can be performed at event rates in the MHz range; the goal is a front-end full capacity of 10^3 images;
- the need of an in-pixel analog to digital conversion to store the data collected in each pixel, with 10 bit resolution ($\geq$ 9 bit effective resolution) to guarantee single photon resolution at small signals;
- minimum dead area, less than 5% to significantly improve on the present implementations of sensors for coherent X-ray diffraction imaging (CXDI) applications;
- tolerance to very high ionizing radiation doses, in the order of 1 GGy for the sensor and of 10 MGy for the readout electronics.

In order to satisfy the above specifications, cutting-edge microelectronic fabrication technologies will have to be fully exploited. Fig. 1.11 gives an overview of such technologies, showing a matrix (part of a more complex and larger area detection system) of 9 four-side buttable blocks. Each block consists of a multilayer device, obtained with the vertical interconnection of the sensor to a dual-tier front-end chip. High density through silicon vias (TSV) in the upper

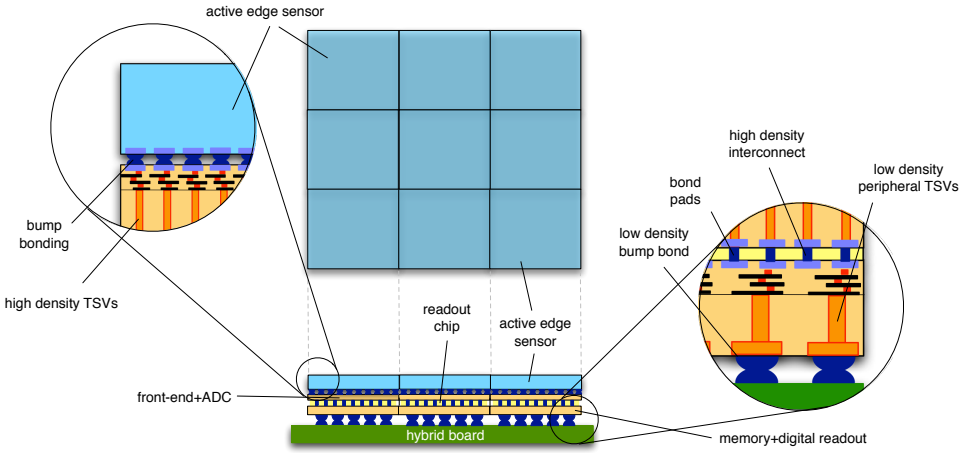


Figure 1.11: Conceptual view of a 3×3 detector matrix made of 9 four-side buttable elementary blocks.

layer of the front-end chip, with a diameter in the order of 1 μm, which also implies aggressive thinning of the substrate, are necessary to enable inter-layer communication through high density interconnects. A process with these characteristics is available from Tezzaron Semiconductor [21]. Low density TSVs, on the other side of the vertically integrated structure, represent another important ingredient of a four-side buttable chip: the access to the input-output pads through the substrate enables to avoid the use of wire bonds and makes possible the placement of the elementary tiles tight side-by-side. Since the TSV diameter can be of the order of a few tens of micrometers, the thinning step required may be less aggressive here with respect of the previous case. Facilities which offer a low density TSV service are for instance CEA-LETI in Europe [22] and by Tohoku-MicroTec in Japan [23]. The chip, in turn, is bump bonded to a hybrid board. Interconnection between the sensing layer and the front-end chip, since the pitch is relatively large (110 μm), can be accomplished with bump-bonding techniques (for instance the Fraunhofer Institute for Electronic Packaging and System Integration (IZM) provides a chip-to-chip bump bonding process).
With this ambitious goal in mind, in its 3-year time span, the PixFEL project aims to lay the groundwork for an advanced pixel detector by:

- investigating the enabling technologies which can lead to a four-side buttable elementary chip and to a detector with zero or almost zero

dead-area;

- designing, testing and optimizing the microelectronic building blocks required for the front-end chip of a 2D X-ray camera;
- investigating the solutions suitable for high performance in-pixel storage and readout of the data.

So far, a slim edge sensor with minimum dead area has been developed, fabricated and tested, together with an analog front-end with an ADC compatible with the specifications discussed above.

1.6 Active edge pixel sensors

To minimize the dead area in the sensor layer, a planar pixel sensor fabricated with an active edge technology is used, which has been already applied successfully in silicon pixel sensors by many foundries, like SINTEF (Norway) [24], VTT (Finland) [25], and FBK (Italy) [26]. This technology was proposed as a possible solution to minimize the gap between the active area and the edge of the detector. The active edges are obtained by etching deep trenches around the pixel sensors using Deep Reactive Ion Etching (DRIE) process and doping the trenches walls to shield the leakage current from defects located at the edge. One of the most important aspects of the technology is in the capability of achieving, in the excavation step, a trench with a high aspect ratio ($\geq$ 20:1). Trench depth is typically around 200 μm. While the current trend is towards thinner substrates in pixel sensors for High Energy Physics applications, relatively thick sensors are necessary for FEL applications to obtain a detection efficiency in the order of 90% at the maximum X-ray energies of interest, even greater than 10 keV (see Fig. 1.12). The figure shows that a thickness of 450 μm would allow for a $\sim$87% efficiency at 12 keV. On the other hand, thicker sensors require larger depletion voltages with respect to thinner ones. Moreover, for FEL applications the most important aspect to be considered is the consequences of plasma effects in case a large number of photons hit one pixel at a time, implying a high charge carrier densities. This could affect the charge collection properties, such as linearity, point spread function and response time of the detector. A solution to this is to apply a high bias voltage: as an example, a bias voltage of larger than 500 V is recommended in [27]. Such high values can be achieved by the use of multiple guard-ring terminations, even in the worst-case conditions represented by the extremely high ionization doses foreseen at FELs, but this costs a wide dead area at

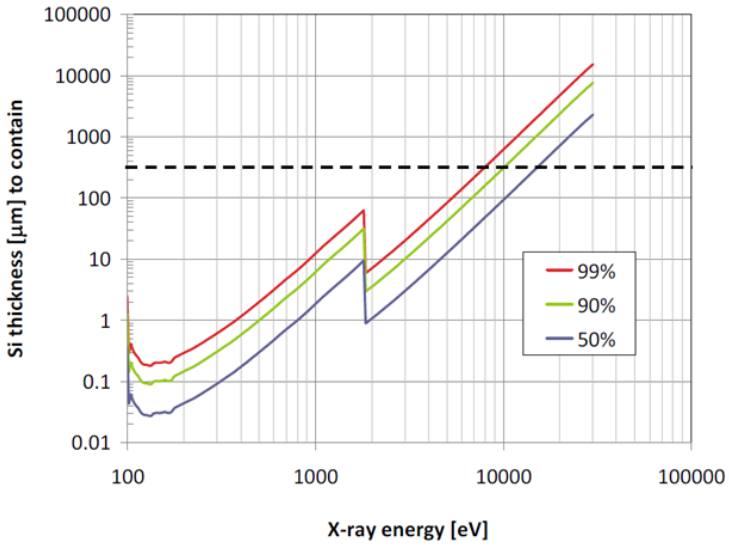


Figure 1.12: Plot of the required sensor thickness as a function of the energy for different efficiencies.

the edge (>1 mm [28]). On the contrary, the goal of active edge sensors is to minimize the size of the edge region, but this implies early breakdown voltage which represents a limiting factor and inhibits the sensors from being properly biased. Therefore, a TCAD simulation campaign was set up and performed in order to find the best trade-off among edge region size, breakdown voltage and charge collection properties of the sensor. Using 4 floating guard rings with external plate, a 2.4 μm deep junction for the collecting diffusion and a 300 nm thick oxide, a breakdown voltage larger than 400 V can be maintained over the entire lifetime of the detector, which involve the absorption of a 1 GGy total ionizing dose and an accumulated surface oxide charge density of 3×10^{12} cm^{-2}. Furthermore, the accumulated surface oxide charge density is minimized by the use of p-on-n sensors, for which the reverse bias voltage causes the electric field to point in the opposite direction with respect to the Si-SiO_2 interface. Figure 1.13 shows a cross section of the active-edge planar sensor and a top view of the four guard-ring border termination. The sensors have already been fabricated and tested [29].

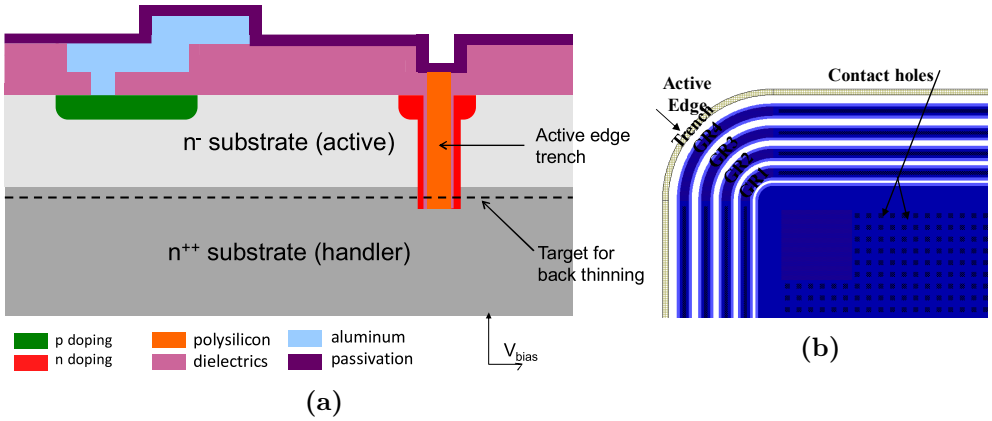


Figure 1.13: Schematic cross-section of planar active-edge sensors using Si-Si Direct Wafer Bonded substrate (a) and layout of the corner of a planar active-edge sensor with a four guard-ring border termination (b).

1.7 PixFEL analog front-end channel

The pixel sensors are to be connected to a readout chip. The block diagram of the front-end circuit is shown in Figure 1.14. The choice of a nanoscale CMOS technology for the front-end chip fabrication is important, in order to integrate in the target pitch of 110 μm the necessary amount of on-board intelligence. Also, synergy with the large number of activities about to start in the particle physics community and focused on microelectronic developments provides a persuasive motivation to opt for the 65 nm node. In Figure 1.14, the signal from the detector is processed by a charge sensitive amplifier (CSA) with a dynamic compression feature based on the non linear behavior of the MOS capacitor in the feedback network. The integrated charge is reset through the switch SR. The voltage at the preamplifier output is converted to a current by means of a transconductor with enhanced linearity properties. Trapezoidal, time-variant shaping of the signal is performed through a so called flip-capacitor filter [30], whose operation is based on the appropriate timing of switches S0 to S4. The sample at the channel output is converted to a 10 bit word by means of a SAR (Successive Approximation Register) ADC with time-interleaved architecture, which is the main subject of this thesis work.

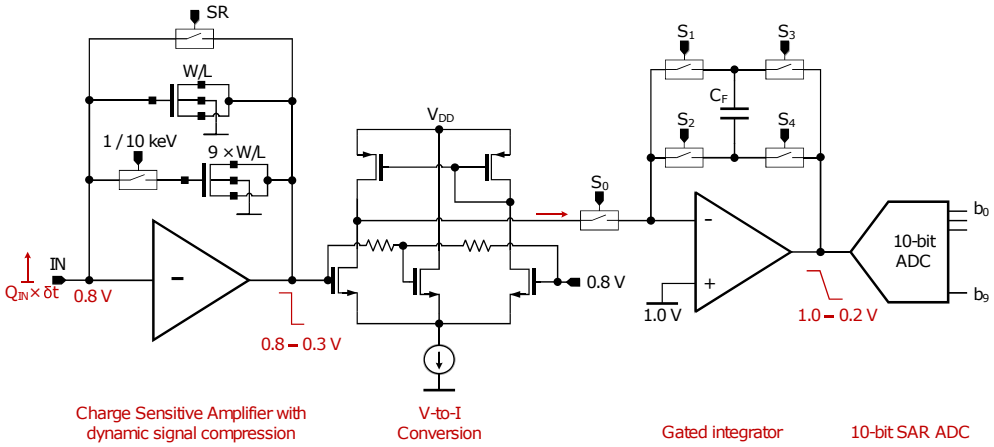


Figure 1.14: Readout channel for the PixFEL imaging detector.

1.7.1 CSA with dinamic signal compression

The readout channel designed for the PixFEL project is required to cover a 10^4 photons input dynamic range at both 1 keV and 10 keV energies, while preserving at the same time a single photon resolution for input signal up to 100 photons. In order to fit the wide input dynamic range into a reasonable output signal swing (in the order of a few hundreds of mV in this technology), a strongly nonlinear characteristic is required. This can be achieved at either sensor level, as in the case of the DSSC device [31], or at front-end level, like in the LPD detector [15]. In the case of the PixFEL front-end channel, a novel front-end level solution to dynamically change the feedback capacitance of the CSA according to the intensity of the input signal has been devised [32]. The stage has been optimized for an output signal with negative polarity, as the detector, based on a p-on-n structure, will collect holes and deliver a current pulse flowing into the CSA input terminal. The feedback capacitance consists of a MOSFET transistor, with the gate terminal connected to the preamplifier input and the source and drain terminals shorted together and connected to the output. The device is kept far from the accumulation region by attaching its bulk to ground (inversion-mode configuration) [33]. When operated in this fashion, the MOS transistor behaves as a strongly non-linear capacitor, with a capacitance monotonically increasing with increasing V_{GS}. A selection bit (1 keV/10 keV in Fig. 1.14) is used to change the charge sensitivity of the preamplifier, that can be switched between a 1 keV and a 10 keV gain mode, according to the expected photon energy, by correspondingly switching the

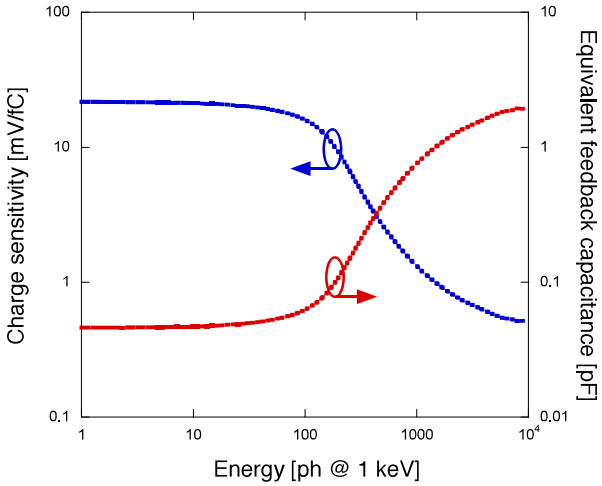


Figure 1.15: Charge sensitivity and equivalent feedback capacitance as a function of the input signal.

channel width W of the feedback MOS capacitor between 40 μm and 400 μm (the channel length L being 4 μm). The smallest capacitance value C_{min}, with the predominant contribution coming from the overlap region between the gate and the source and drain diffusions, is achieved for V_{GS} much smaller than the threshold voltage, i.e., close to zero in the case considered here. As V_{GS} increases and exceeds the threshold voltage, carrier type inversion takes place under the gate and the channel is formed. C_{MOS} consistently increases in a strongly non-linear fashion, peaking at a C_{max} value corresponding to the gate-to-channel capacitance of the device. C_{min} and C_{max} can be expressed at first order as:

$$C_{min} \approx 2W\Delta LC_{ox}, \tag{1.2}$$

$$C_{max} \approx WLC_{ox}, \tag{1.3}$$

where ΔL is the extension of the gate-to-source (or gate-to-drain) overlap region along the direction of L and C_{ox} is the gate oxide capacitance per unit area. Fig. 1.15 shows the charge sensitivity G_Q (blue curve) as a function of the input signal (i.e., the number of 1 keV photons). This result was obtained in the case of an aspect ratio $W/L = 40\ \mu m/4\mu m$ for the NMOS capacitor in the preamplifier feedback network. The charge sensitivity varies from about 20 mV/fC for small input signals to about 0.5 mV/fC for large signals.

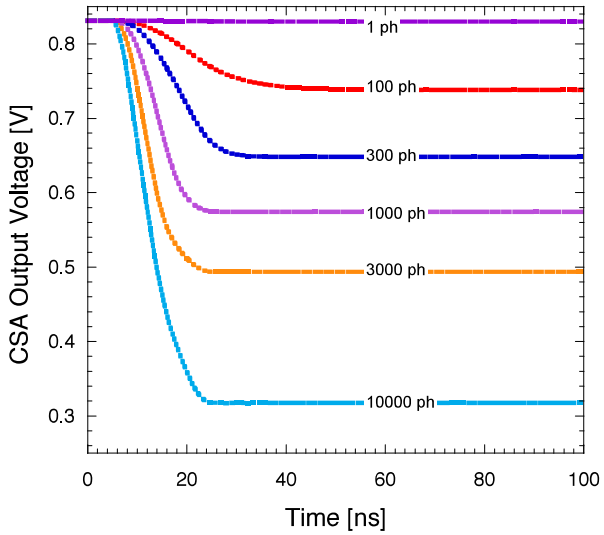


Figure 1.16: Simulated transient response of the charge preamplifier to different input signals for a photon energy of 1 keV.

Correspondingly, the equivalent feedback capacitance C_{eq}, defined as

$$C_{eq} = \frac{1}{G_Q} = \left(\frac{dV_{out}}{dQ}\right)^{-1} \tag{1.4}$$

and represented by the red curve in Fig. 1.15, changes from around 30 fF to about 2 pF. The simulated transient response of the charge preamplifier for different values of the number of input photons is shown in Fig. 1.16 for a photon energy of 1 keV. The strong non-linearity of the circuit can be easily detected for instance by observing that the response amplitude for an input signal of 10^4 photons is just twice the amplitude for an input signal of 10^3 photons. The equivalent noise charge (ENC) contributed by the charge sensitive amplifier, about 50 electrons, is compatible with single photon resolution at 1 keV. The dissipated power is 90 μW. For more details about this stage, see [34], where its design and test are deeply discussed.

1.7.2 Shaping stage

In the PixFEL readout channel, a time variant shaper (including a transconductor to perform a voltage-to-current conversion) is used to process the signal at the preamplifier output, taking advantage of the known repetition rate of

the X-ray pulses to precisely set the processing time and the duration of the individual processing phases. A further benefit of using a time-variant shaper is that the circuit may be designed to provide the sample to convert directly at the ADC input. The proposed architecture is based on the Flip Capacitor Filter (FCF) idea, performing a Correlated Double Sampling (CDS) technique to achieve, with a single integrator stage and a flipped feedback capacitor, a trapezoidal weighting function [30]. A Voltage-to-Current converter based on a transconductance stage, with an additional linearization network, has been introduced to convert the voltage at the output of the CSA into a current. The input reference voltage of the stage is close to the DC output voltage of the CSA (about 800 mV), in order to minimize the output current when no signal is applied at the input. The gain of the transconductance stange is about 30 $\mu A/V$ for the expected input voltage range of 500 mV. The forward stage of the flip capacitor filter (FCF) consists of a classic Miller-OTA (Operational Transconductance Amplifier) with an AB class output stage, able to charge the 2.5 pF capacitance of the SAR ADC. The feedback capacitance has been set in such a way to match one photon to 1 ADC bins for low input signals at a 5 MHz burst mode operation. Since 1 ADC bin is expected to be about 800 μV, the FCF feedback capacitance is given by the following equation:

$$C_F = \frac{70e \cdot G_m \cdot \tau}{C_f \cdot LSB}, \tag{1.5}$$

where 70 is the number of the electrons generated by one impinging photon at low energy, G_m is the transconductance of the Voltage-to-Current converter and τ is the integration time of the flip capacitor filter. For a 5 MHz burst mode operation, $\tau = 50\ ns$, leading to a feedback capacitance of about 700 fF. Figure 1.17 shows the simulated transient response of the FCF for different input signals at 1 keV, with a conversion rate of 5 MHz. Figure 1.18a shows the relationship between the input of the CSA and the FCF output and Fig. 1.18b the sensitivity of the channel as a function of the input signal amplitude, for both the energy configurations. As it can be seen from Figure 1.18, for small input signals, the channel features a sensitivity (G_{ph}) of 1.5 mV/ph and 1.65 mV/ph, respectively for the 1 keV and the 10 keV configuration, and a non-linearity lower than 0.08 ph [34].

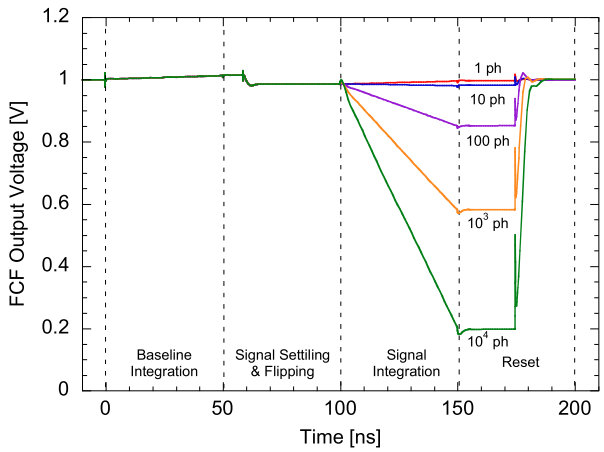
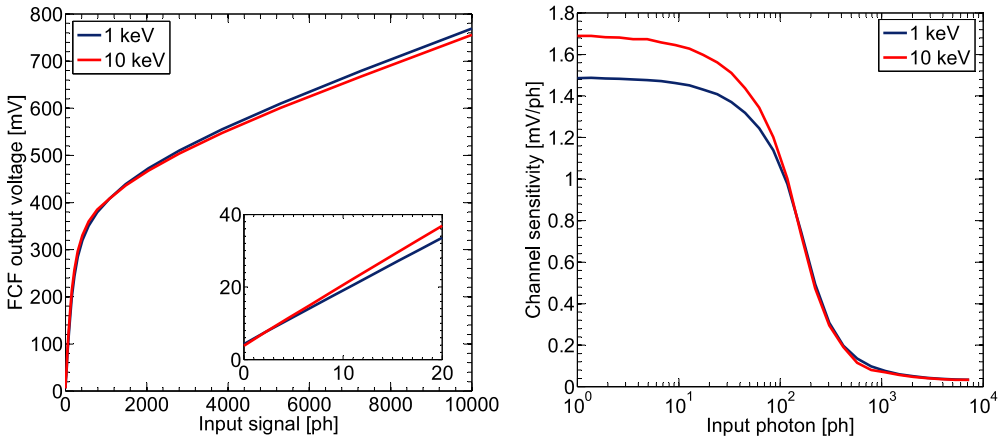


Figure 1.17: Transient response at the 5 MHz conversion rate of the flipped capacitor filter for different input signals at 1 keV.



(a) **(b)**

Figure 1.18: Transcharacteristic (a) and sensitivity (b) of the analog front-end.

Chapter 2

A-to-D converter for the PixFEL project

This chapter will be devoted to the description of the Analog to Digital Converter (ADC), which is part of the front-end channel developed in the PixFEL project. In the first part of the chapter, the ADC specifications in terms of area, bit resolution and sampling frequency are discussed. The choice of a SAR ADC architecture is explained and the architecture is described. The charge redistribution technique is discussed, focusing on the split capacitor array DAC designed and on its dimensioning. The use of bootstrap switches is justified and their circuit is described. The dynamic latched comparator and the SAR logic are illustrated. Together with a circuital level description, the layouts of each block and of the whole ADC are reported.

2.1 In-pixel ADC

As already said in the previous chapter, the readout channel for the PixFEL detector has been designed with keeping in mind the specifications set by the Eu-XFEL. The specific time structure of the beam line at this facility, featuring 10 trains of 2700 X-ray 100 fs pulses per second, the pulses being generated at a rate of 4.5 MHz, implies that, for single shot imaging, a complete image has to be recorded every 220 ns during a time interval of 0.6 ms, while data readout form the chip can be perfomed during the inter-train period, lasting 99.4 ms. The detectors described in the previous chapter use different approaches for in-pixel storage: storage of analog samples as in AGIPD [14] and LPD [15], or in-pixel digitization as in the DSSC [16]. Beside that, they implement different solutions for signal digitization. AGPID and LPD projects use ADCs in the

chip periphery. PERCIVAL [17] project uses seven 12-bit ADC per column (with a total column number of 4000) to be shared between the 4000 pixels of that column. XAMPS [18] project uses a 3-bit coarse conversion on chip and the residual are converted by discrete 12-bit ADC out of the chip. HIPPO [20] project has a 12-bit pipeline ADC shared between 4 channels. Only the DSSC project uses an in-pixel conversion, with a selectable 8 or 9 bit, single ramp ADC. For the PixFEL project an approach with in-pixel digitization has been preferred, since it guarantees a higher storage capability than the analog approach. Moreover, off-chip transmission of analog data, or analog samples transfer from the pixel to the chip periphery, where they would be digitized before data output, is more exposed to corruption with respect to the adoption of an in-pixel digitization.

2.2 ADC specifications

The disadvantage of immediate digitization of amplitude information is the requirement of an ADC into each pixel. This means that the ADC needs to fit in the 110 μm pixel pitch together with the analog front-end and that fast clock signals have to run close to the most sensitive points of the front-end circuit. Furthermore the converter power consumption has to be limited in view of its integration in a large (64×64) pixel matrix. However, in continuously operated FELs, the conversion rate is typically quite low, slightly exceeding 100 Hz in the worst case. In the case of burst mode operation, as in the European XFEL, during the pulse train period the event frequency and the required conversion rate could be as high as 4.5 MHz, but the average frequency, and consequently the average dissipated power, becomes relatively low taking into account the large inter-train period (99.4 ms), when the converter is idle. For the design of the ADC, a target sampling and conversion frequency of 5 MHz was pursued, in order to be compliant with the experiments at the Eu-XFEL, setting the most challenging specifications.
The choice of the ADC resolution relies upon some inherent properties of light in diffraction experiments and on the features of the dynamic compression characteristic of the channel. Single photon resolution over the entire input dynamic range of 10^4 photons would require an ADC with an effective resolution of 14 bit. This specification, beside exacerbating the noise performance requirements for the analog front-end, would be very hard to satisfy with an in-pixel converter, given the area and speed constraints. Actually, the number of photons n_{ph} hitting a pixel during diffraction imaging experiments is sub-

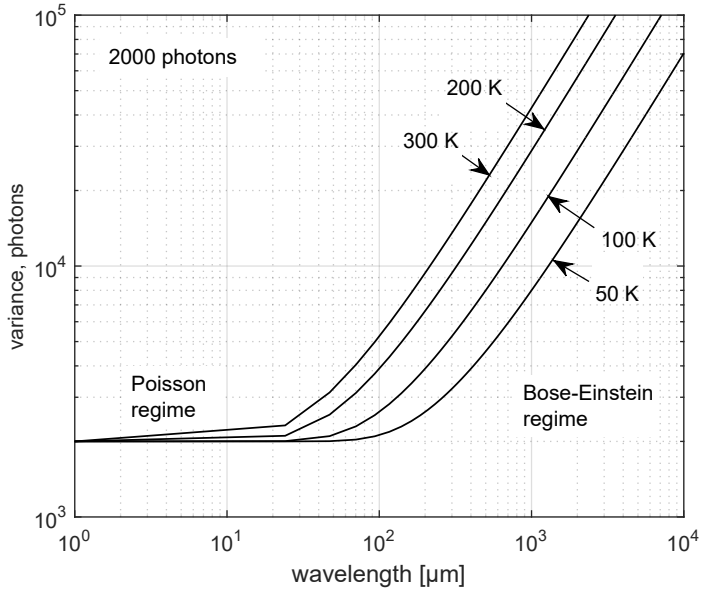


Figure 2.1: Photon shot noise variance as a function of wavelength.

ject to fluctuations according to a random process, also known as shot noise, described by Bose-Einstein statistics [35]:

$$\sigma^2_{shot}(n_{ph}) = n_{ph}\frac{e^{hc/\lambda kT}}{e^{hc/\lambda kT}-1}, \tag{2.1}$$

where h is Planck's constant ($6.626 \times 10^{-34} J \cdot s$), λ is the photon wavelength, k is Boltzmann's constant ($1.38 \times 10^{-23} J/K$), c is the speed of light and T is the temperature (K). Figure 2.1 plots Eq. 2.1 as a function of the wavelength (μm) and the absolute temperature of the semiconductor. In the case of wavelengths greater than 10 μm, photons couple with photons, hence the shot noise increases. Reducing the operating temperature, the plot shows a decrease of the semiconductor production of coupling action and variance. However, since the photoelectric effect for wavelengths >1 μm cannot occur, this phenomenon does not affect silicon detectors. Assuming that $hc/\lambda \gg kT$, Poisson statistic is a good approximation of Bose-Einstain statistic. Eq. 2.2 represents the Poisson probability distribution:

$$p_i = \frac{n^i_{ph}}{i!}e^{-n_{ph}}, \tag{2.2}$$

where p_i is the probability of the occurring of i interactions per pixel. From the previous equation, Eq. 2.3 can be reduced to the well-known shot noise relation characteristic of visible imagers:

$$\sigma^2_{shot}(n_{ph}) = n_{ph}. \tag{2.3}$$

The latter is the case for X-ray photons. This result indicates that there would be no use for the ADC to provide single photon resolution when n_{ph} grows, as the Poisson noise at some point would be so large that some degree of quantization noise might be accommodated with no significant performance degradation. In fact, the dynamic compression features of the readout channel make it possible to preserve single photon resolution at small signals using an ADC with $n < 14$ bit, at the cost of some increase in quantization noise at large signals, where it is largely exceeded by Poisson noise. Once the number of bits and the input dynamic range ΔV_{ADC} of the ADC have been set (equal to 800 mV), the number of photons per ADC bin n_{bin} can be defined as

$$n_{bin} = \frac{LSB}{G_{ph}}, \tag{2.4}$$

where $LSB = \frac{\Delta V_{ADC}}{2^n}$ is the least significant bit and $G_{ph} = \frac{dV_{FCF}}{dn_{ph}}$ is the gain of the analog readout channel. If the analog channel gain for small numbers of photons is chosen in such a way that $G_{ph,high} = 1\ LSB/photon$, then one ADC bin will correspond to one photon. In this situation, the quantization noise is zero, as, for a given ADC output, the number of detected photons is known with no uncertainty. As the number of input photons increases, the gain decreases due to the dynamic compression feature of the system, so that n_{bin} increases. In this case, the ADC will provide information about the number of impinging photons with some uncertainty due to quantization. In the case of a discrete variable, like the number of detected photons, quantization noise $\sigma_{q,ph}$ may be expressed as:

$$\sigma^2_{q,ph} = \frac{1}{n_{bin}} \sum_{i=1}^{n_{bin}} (i - x)^2, \tag{2.5}$$

where the sum is calculated for each value of the variable i in the bin interval. The photon number which minimize the error $\sigma^2_{q,ph}$ can be found as x_{opt}:

$$\frac{d\sigma^2_{q,ph}}{dx} = 2x_{opt} - (n_{bin} + 1) = 0 \ \Rightarrow \ x_{opt} = \frac{n_{bin} + 1}{2}. \tag{2.6}$$

Hence the quantization error is going to be:

$$\sigma_{q,ph}^2 = \frac{1}{n_{bin}} \sum_{i=1}^{n_{bin}} \left(i - \frac{n_{bin}+1}{2} \right)^2 = \frac{n_{bin}^2 - 1}{12} \tag{2.7}$$

Note that $\sigma_{q,ph}^2$ is zero for $n_{bin} = 1$ and tends to the well known expression for quantization noise for large values of n_{bin}. The ADC resolution and the compression characteristic should be chosen in such a way that

$$\sigma_{q,ph}^2 \ll \sigma_{shot}^2(n_{ph}) \tag{2.8}$$

for any value of n_{ph}. If n_{bin} is replaced in (2.7) with its expression in (2.4), then a lower limit can be obtained for the gain at large input signal $G_{ph,low}$ as:

$$G_{ph,low}(n_{ph}) \gg \frac{\Delta V_{ADC}}{2^n \sqrt{1 + 12 n_{ph}}}. \tag{2.9}$$

In the case of a bilinear characteristic, which is very close to the one of the PixFEL readout channel, given the input signal range n_H in which single photon resolution is implemented and where the gain is $G_{ph,high} = 1\ LSB/photon$, the number of photons per LSB in the low gain region can be expressed as

$$n_{bin} = \left[\frac{n_{ph,max} - n_H}{2^n - G_{ph,high} \cdot n_H} \right], \tag{2.10}$$

with $n_{ph,max}$ the maximum number of input photons (here assumed to be 10^4). Fig. 2.2 shows the quantization noise and the smallest Poisson noise in the low gain region of a bilinear compression characteristic as a function of n_H, if the gain in the high gain region is $G_{ph,high} = 1\ LSB/photon$. Being closer to the quantization error, the smallest Poisson noise in the low gain region represents the worst case and is equal to $\sigma_{shot}^2(n_{ph}) = n_H$. An 8 bit resolution is not sufficient to satisfy the condition on the quantization noise in 2.8. The same holds for $n = 9$, although $\sigma_{q,ph}^2 < \sigma_{shot}^2(n_{ph})$ ($\sigma_{q,ph}^2$ only smaller, not much smaller than $\sigma_{shot}^2(n_{ph})$) for some values of n_H. The condition $\sigma_{q,ph}^2 \ll \sigma_{shot}^2(n_{ph})$ is satisfied instead in the case $n = 10$ for $94 \leq n_H \leq 704$, where $\sigma_{q,ph}^2 < \sigma_{shot}^2(n_{ph})/10 \Rightarrow \sigma_{q,ph} < \sqrt{n_H/10}$. Hence, the choice of an ADC with a resolution of $n = 10$ bit. From the inequality in (2.9) and considering $n_{ph} = n_H = 94$, G_{ph} has to be much grater than 23.25 $\mu V/ph$ in the low gain region. Note that an increase in $G_{ph,high}$ can be used to relax the noise requirements for the analog front-end. However, this choice affects the quantization noise in the low gain region. As a result, if $G_{ph,high} = 2\ LSB/photon$, for $n = 10$ bits, no range can be found for n_H where σ_{shot}^2 is at least one order of magnitude

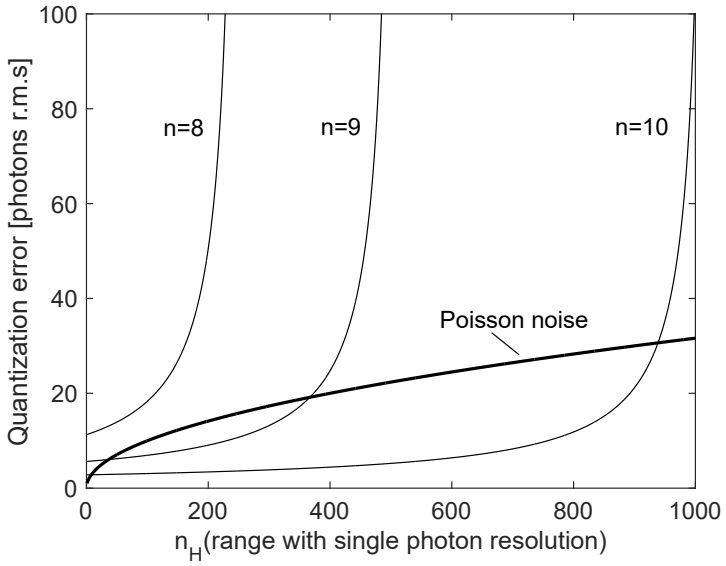


Figure 2.2: Quantization noise in the low gain region of a bilinear compression characteristic as a function of the single photon resolution range. The quantization noise for three different ADC resolutions is compared to the lowest Poisson noise in that region.

larger than $\sigma^2_{q,ph}$ (i.e., 2.8 cannot be fully satisfied). On the other hand, under the same conditions for $G_{ph,high}$ and the ADC resolution, $\sigma^2_{q,ph} < \sigma^2_{shot}(n_{ph})/9$ for $117 < n_H < 239$, still acceptable for low noise operation of the ADC.
The choice of a 10-bit resolution might seem in disagreement with the ADC design choice in the DSSC project [16], where a resolution of 8 bit is considered sufficient, even if the DSSC project has similar specifications to the ones of PixFEL, e.g. single photon resolution for small signals and about 8000 photons range. However the compression feature achieved through the DSSC sensor can not be approximated with a bilinear function as the compression feature achieved with the PixFEL CSA. In particular the PixFEL project has a wider high gain region than the DSSC. Hence, the considerations about the ADC resolution proposed in this section can not be readily applied to the DSSC readout channel.
Summarizing, the ADC specifications for the PixFEL projects are:

- 10 bit resolution;

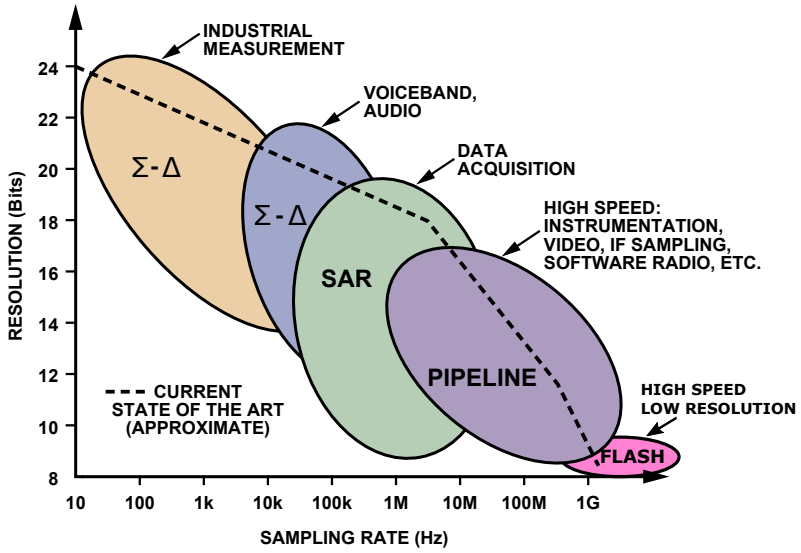


Figure 2.3: ADC architectures comparison as regards to sampling frequency and bit resolution.

- sampling frequency up to 4.5 MHz to be compliant with the operation rate of the Eu-XFEL, up to 1 MHz for the LCLSII;
- area of a square pixel with a pitch of 110 μm to be shared with the analog front-end and the readout logic; 65% of the area available for the ADC;
- a total power budget for the pixel of 350 μW, with 25% of the power available for the ADC.

2.3 Choice of ADC architecture

The performance and energy efficiency of analog-to-digital converters (ADCs) have improved steadily over the past two decades. No specific ADC architecture dominates the entire application space, the choice actually depending on the required performance. As indicated by Fig. 2.3, four main types of ADC cover most of the application needs: $\Sigma\Delta$, SAR, pipeline and flash ADC. Below a brief comparison between the four ADC architectures is provided [36].
Oversampling/sigma-delta converters can achieve high resolution, but they have limited bandwidth: high-bandwidth sigma-delta converters with 12 to 16

bits of resolution can reach bandwidths up to 1 MHz to 2 MHz. These are the cases of very high order sigma-delta modulators (4th-order or higher), integrating a multibit ADC and a feedback with a multibit DAC. Sigma-delta ADCs have a natural advantage over SAR A-to-D converters: even to accomplish 16 bits of resolution or more, they does not need trimming or calibration. This type of converter privileges resolution over speed. Since it needs to sample many times (often more than 16 times) to obtain one final sample, the analog blocks of the sigma-delta converter need to work much faster than the output data rate.
A pipelined ADC is made up of several stages, each one working on 1 to a few bits (of subsequent samples) simultaneously. This parallelism enables to increase the throughput, but at the expense of more power consumption, silicon area and latency than a SAR ADC with an equivalent bit resolution.
A flash ADC is made up of a large number of comparators, each one generally consisting of a wide-band, low-gain preamplifier followed by a latch. Hence, a flash ADC is the fastest ADC architecture available. While a flash ADC offers the best performance in terms of speed, the SAR ADC boasts smaller silicon area occupation and significantly lower power consumption. For every extra bit of resolution, in a flash ADC the number of comparators increases by a factor of two, while each comparator accuracy must be doubled. Also in a SAR ADC, however, an increased resolution needs more accurate components, but without an exponential increase of the complexity.
Therefore, while noise shaping ADCs ($\Sigma\Delta$) satisfy high resolution low-bandwidth applications, higher sampling speeds and higher resolution require pipelining. On the other hand, if very-high-speed, low resolution ADCs can be implemented with a flash architecture, SAR ADC is very effective for medium resolution and low-to-medium sampling speeds. Given the specification for the PixFEL front-end channel, a SAR ADC architecture is the most suitable choice among the solutions explored in this section, even if the available area and the power budget still represent challenging requirements.

2.4 Interleaved SAR ADC architecture

The successive approximation algorithm performs the analog to digital conversion over multiple clock periods by exploiting the knowledge of previously determined bits to fix the next significant bit. The algorithm is based on a feedback loop around a DAC (Digital to Analog Converter) as represented by the flow chart of Fig. 2.4. The converter starts by initializing the successive approximation register (SAR) to a value where all bits are set to '0', except the

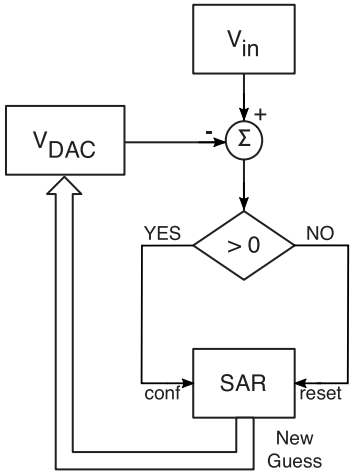


Figure 2.4: Flowchart of the successive approximation algorithm.

MSB (Most Significant Bit) which is set to '1'. This represents the mid-level code. The analog signal is applied to a sample-and-hold (S/H) circuit, and, on the first clock cycle after the sampling, the DAC converts the digital code stored in the SAR into an analog signal, generating a voltage level equal to half the analog input range. The sampled input analog sample V_{in} is compared to the DAC output to establish if it is greater or less than it. The control logic in the SAR leaves the MSB set to '1' if the sampled signal is larger than the DAC output, or changes it back to '0' if it is smaller. The process is repeated during the next clock cycle on the next significant bit: the sampled signal is compared to 1/4 or 3/4 of the input dynamic range depending on the decision taken at the end of the previous clock cycle. The algorithm continues until the least significant bit is determined. For an n-bit converter, besides a clock cycle needed to sample the input signal, n clock cycles are required to fully quantize each sample, yelding a total of at least n+1 clock periods per conversion. Fig. 2.5 represents the block diagram of a SAR ADC: it includes a sample-and-hold block, a D-to-A converter, the SAR logic and a discriminator, comparing the DAC output to the sample value and providing the comparison result to the SAR logic. Fig. 2.6 shows an example of the time evolution of some internal signals of a 3 bit SAR ADC. In particular the diagram shows how the decision taken on the bits, at first inizialized to '1', lets the DAC output voltage V_{DAC} get closer and closer to the sampled input.
The purpose of speeding up the ADC operation [37], while avoiding large cur-

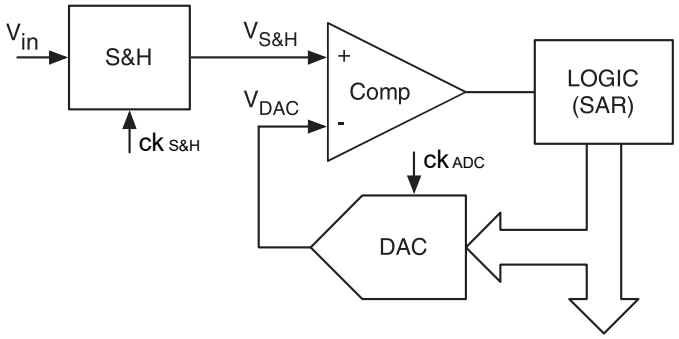


Figure 2.5: Block diagram of a SAR ADC.

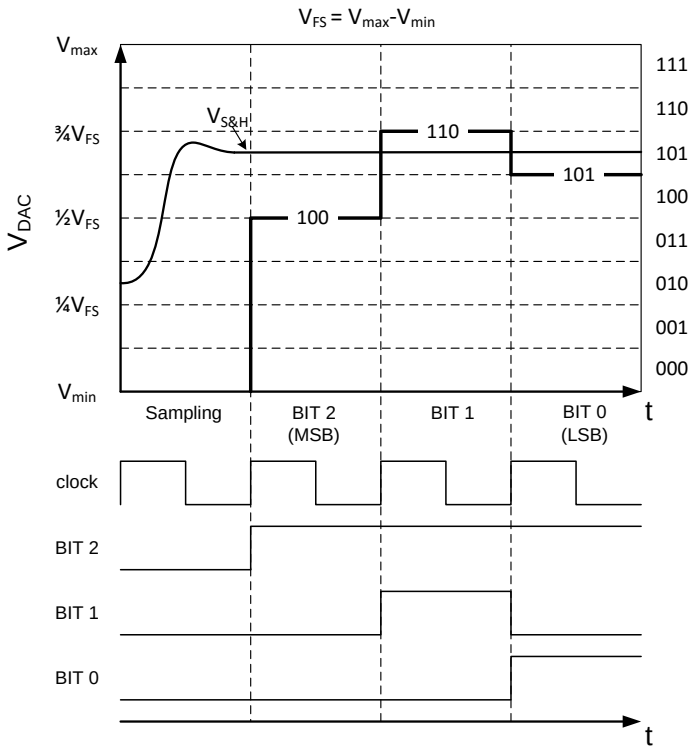


Figure 2.6: Timing of a 3 bit SAR ADC.

rent peaks during the sampling phase, leads to the use of a time-interleaved structure. Indeed, the amplitude of the current needed to charge the sampling capacitance can be reduced by a factor equal to the number of clock per sample if the pre-charge period is increased from one clock period, as in Fig. 2.6, to the whole sampling period. As a further benefit, the driving capability requirements of the stage coming before the ADC (the shaping stage) can be accordingly relaxed, but the drawback of this solution is the doubling of part of the ADC area. Actually, during each sampling period, half of the circuit is involved in sampling the input voltage directly from the previous stage of the readout channel, while the sample stored in the other half of the circuit during the previous sampling period is being converted. This leaves one entire sampling period available for A-to-D conversion of each sample. Since in FEL experiments the `clock` signal and a `trigger` signal, which informs on the moment on which the conversion has to start, are available as input, the ADC is designed to start the conversion every `clock` rising edge after the `trigger` goes high (the `trigger` signal is internally synchronized with the `clock`). The block diagram of the time-interleaved SAR ADC designed is represented in Fig. 2.7, where the two blocks performing the sampling and D-to-A conversion are alternatively connected to the comparator thought the $\texttt{CONV}_{1,2}$ signal generated by the SAR logic. The timing is shown in Fig. 2.8. As it can be noticed from this figures, the ADC inputs are the `clock` and `trigger` signals from the extern of the chip and V_{in} from the previous stage of the readout channel, while the outputs are the ten bits and the `EoC` (End of Conversion) signals, which goes to '1' every time the conversion process ends and remains high for one clock period.

2.5 Charge redistribution technique

One of the most important advantages of the SAR ADC architecture is its low power consumption, which is guaranteed in particular by the use of the charge redistribution technique. The name comes from the fact that the charge sampled at the beginning of the conversion cycle is properly redistributed on a capacitive array during the conversion. This technique can be implemented using a capacitive DAC with binary weighted capacitors, which also performs the sample and hold function. Fig. 2.9 shows an example of a 10-bit capacitive DAC in a SAR ADC scheme. All the capacitances in the array are obtained as a multiple by a power of 2 of the elementary capacitance C_u. During the acquisition phase, the array common terminal (the terminal shared by all the capacitors in the array) is connected to V_{REF1} and all free terminals are

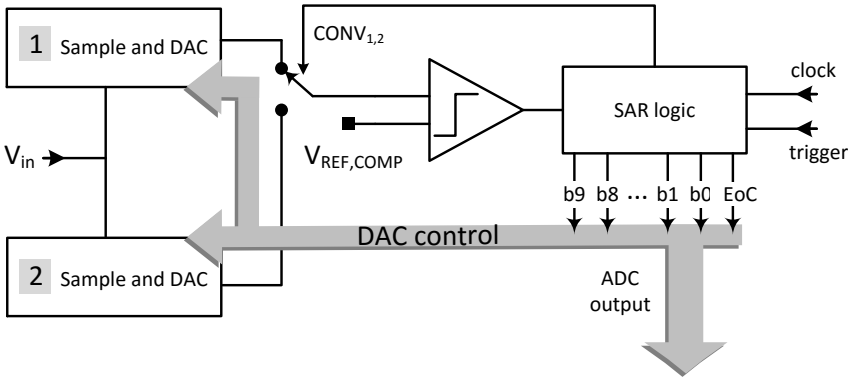


Figure 2.7: Block diagram of the designed time-interleaved SAR ADC.

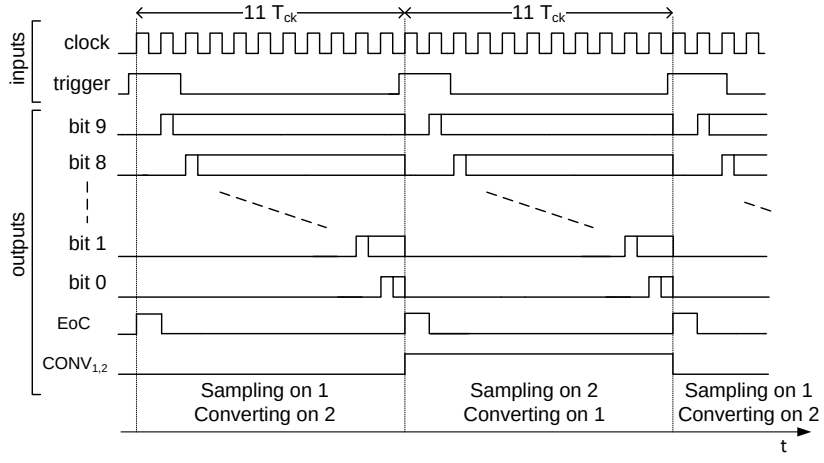


Figure 2.8: Timing of the designed time-interleaved SAR ADC.

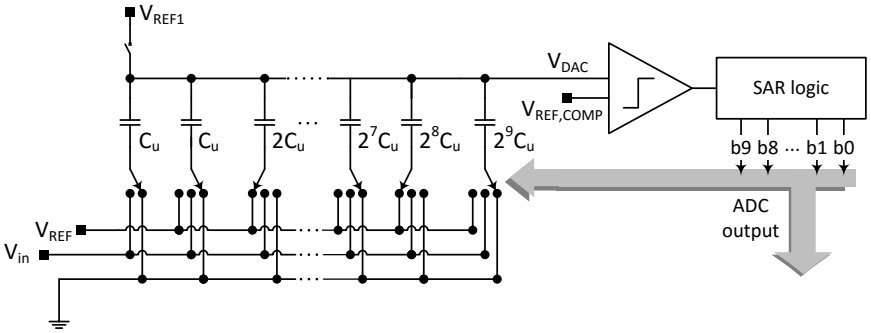


Figure 2.9: Charge redistribution implementation.

connected to the input signal (V_{IN}). After acquisition, the common terminal is disconnected from V_{REF1} and the free terminals are disconnected from V_{IN}, thus holding a charge Q_{TOT}, which depends on the input voltage according to Eq. 2.11,

$$Q_{TOT} = 2^{10} C_u (V_{REF1} - V_{IN}). \tag{2.11}$$

After the sampling phase, at the next rising clock edge, the SAR ADC begins the conversion by first connecting the bottom plate of the biggest capacitance ($2^9 C_u$) to V_{REF} and the bottom plate of the remaining part of the array ($2^9 C_u$) to ground. The charges redistribute and, according to the charge conservation principle, we have:

$$Q_{TOT} = 2^9 C_u (V_{DAC}(1^{st}\, ck) - V_{REF}) + 2^9 C_u V_{DAC}(1^{st}\, ck). \tag{2.12}$$

Hence, substituting (2.11) in (2.12), the voltage on the top plate at the first clock period after the sampling ($V_{DAC}(1^{st} ck)$), applied to the comparator, can be calculated as

$$V_{DAC}(1^{st}\, ck) = V_{REF1} - V_{IN} + \frac{V_{REF}}{2}. \tag{2.13}$$

This voltage is compared to $V_{REF,COMP}$. If $V_{DAC}(1^{st} ck)$ from (2.13) is smaller than $V_{REF,COMP}$, then V_{IN} is larger than half the input dynamic range, hence the MSB is confirmed to be '1', otherwise it has to be changed to '0' (i.e., connected to ground). This works properly, considering that the input range is $[0.2; 1]\, V$, $V_{REF1} = 1\, V$, $V_{REF} = V_{REF,COMP} = 0.8\, V$, and it brings to the use of a comparator with an inverted output, which can be directly used

as the settled logic level for the involved bit. For example, if V_{in} is equal to 0.3 V (an input voltage in the first half of the input dynamic range), from 2.13 $V_{DAC}(1^{st}ck)$ results equal to 1.1 V, larger than $V_{REF,COMP}$, hence the comparator output has to be '0'. Otherwise, if V_{in} is equal to 0.8 V (an input voltage in the second half of the input dynamic range) $V_{DAC}(1^{st}ck)$ results equal to 0.6 V, smaller than $V_{REF,COMP}$, hence the comparator output has to be '1'. At the beginning of the second clock period, the capacitance 2^8C_u is tentatively connected to V_{REF}, yielding:

$$\begin{gathered} V_{DAC}(2^{nd}\,ck) = V_{REF1} - V_{IN} + \frac{3V_{REF}}{4} \\ \text{or} \\ V_{DAC}(2^{nd}\,ck) = V_{REF1} - V_{IN} + \frac{V_{REF}}{4} \end{gathered} \tag{2.14}$$

for MSB = '1' or MSB = '0' respectively. $V_{DAC}(2^{nd}\,ck)$ is compared to $V_{REF,COMP}$ and the result is used to establish the value of the second MSB. The algorithm continues until all 10 bits are determined.
From the description of the charge redistribution technique, it is apparent that the power consumption in the DAC is determined by the power dissipated in charging and discharging the capacitive array.

2.6 SAR ADC with split capacitor DAC

The main drawbacks of the charge redistribution architecture with binary weighted capacitors are the large area occupation and the input capacitance: the total capacitance needed for a 10 bit resolution is equal to $2^{10}C_u$ and provides the main contribution to the area occupation in the SAR ADC.
One possible solution to this problem is to divide the capacitor array in two blocks, representing the MSBs array and the LSBs array, with a bridge capacitance between the two blocks [38], as shown in Fig. 2.10. The value of the bridge capacitance is such that the capacitance seen from the MSB array is equal to the unit capacitance C_u:

$$C_{eq(1)} = C_u \;\Rightarrow\; \frac{C_{bridge}\cdot 2^5C_u}{C_{bridge}+2^5C_u} = C_u \;\Rightarrow\; C_{bridge} = \frac{32}{31}C_u. \tag{2.15}$$

With this approach, the total capacitance used is 2^6C_u, a significant reduction with respect to the classical capacitive DAC of Fig. 2.9. The drawback of this solution is the fractional value of the bridge capacitance. This may be responsible for a poor matching of the bridge capacitance with the other

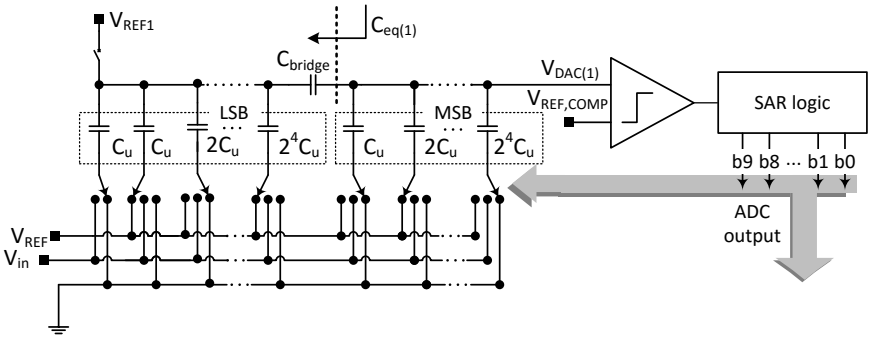


Figure 2.10: Charge redistribution implementation with fractional bridge capacitance ($C_{bridge} = \frac{32}{31}C$).

capacitances of the DAC. To address this problem, a unit bridge capacitance is used and the unit dummy capacitance in the LSB block is removed (the leftmost one in Fig. 2.10), as shown in Fig. 2.11. This solves the matching problem, because every capacitance in the DAC is now an integer multiple of the unit capacitance C_u. However in this case, the equivalent capacitance $C_{eq(2)}$ seen from the MSB array is not C_u, but:

$$C_{eq(2)} = \frac{C_u \cdot (2^5 - 1)C_u}{C_u + (2^5 - 1)C_u} = \frac{31}{32}C_u. \tag{2.16}$$

Actually, this scheme introduces a gain error. For example, when the MSB is initialized to '1', the DAC scheme can be reduced to the one in Fig. 2.12. Hence, the variation of the DAC analog output V_{DAC} is:

$$\Delta V_{DAC(2)} = \frac{(2^4 - 1)C_u + C_{eq(2)}}{2^4 C_u + (2^4 - 1)C_u + C_{eq(2)}} V_{REF} = \frac{512}{1023} V_{REF} \tag{2.17}$$

The same calculation done for the case of a fractional bridge capacitance of Fig. 2.10, would yield $\Delta V_{DAC(1)} = V_{REF}/2$ (that is the same variation of the DAC output in the fully binary weighted SAR ADC). It can be shown that, at the full scale for the DAC output,

$$V_{DAC(1)} = \sum_{i=1}^{10} \frac{1}{2^i} V_{REF} = \frac{1023}{1024} V_{REF}, \tag{2.18}$$

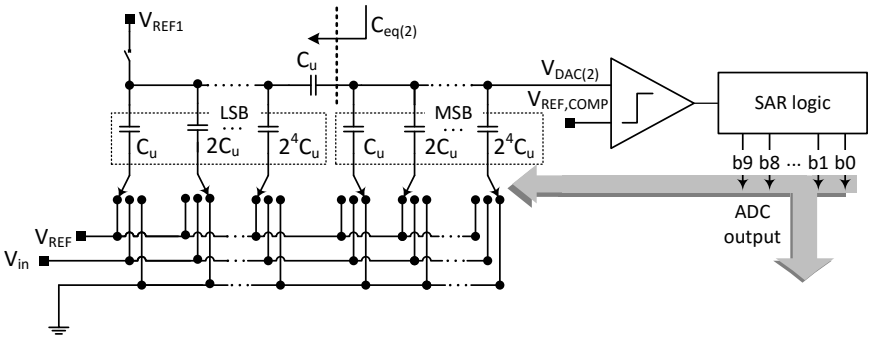


Figure 2.11: Charge redistribution implementation with unit bridge capacitance.

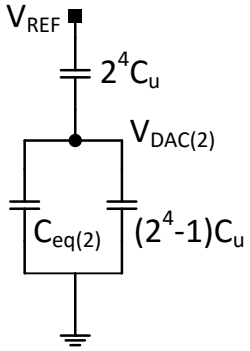


Figure 2.12: Equivalent DAC circuit at the initialization of the MSB at '1' for the unit bridge capacitance scheme.

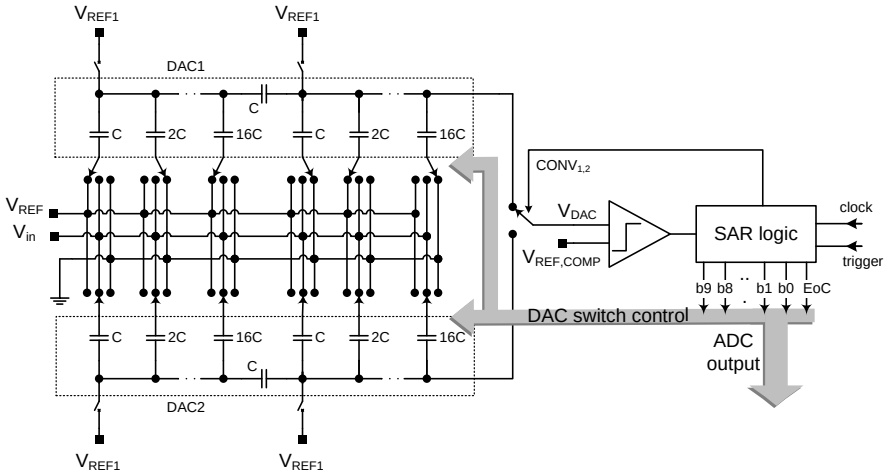


Figure 2.13: Simplified scheme of the complete interleaved SAR ADC.

$$V_{DAC(2)} = \sum_{i=0}^{9} \frac{2^i}{2^{10}-1} V_{REF} = V_{REF}. \tag{2.19}$$

It is worth noticing that the error introduced by the unit bridge capacitance scheme is equally distributed between the quantization intervals of the DAC and, instead of causing INL, the error leads to 1 LSB gain error that can be easily taken into account.The last solution has been adopted for the design of the ADC in the PixFEL readout channel: it makes it possible to reduce the area and the input capacitance by a factor 2^4 with respect to the fully binary weighted capacitor DAC, at the cost of 1 LSB gain error.
The time interleaved structure (see section 2.4) asks for the presence of two split capacitor DACs alternatively connected to the comparator or to V_{REF1} and V_{in} to perform the conversion or the sampling respectively. That is controlled through the `CONV`$_{1,2}$ signal generated by the SAR logic from the `clock` and `trigger` signals (see section 2.11). Fig. 2.13 shows the time-interleaved ADC scheme with split capacitor DACs.

2.7 DAC capacitors sizing

In a SAR ADC based on the charge redistribution technique, the size of the DAC capacitors has to be chosen based on considerations on the thermal noise associated with the sampling switch (see section 2.9) and on the mismatch between the capacitors [39].
The thermal switching noise power, $\frac{kT}{C_s}$ (where C_s is the sampling capacitance, k is the Boltzmann's constant and T the absolute temperature), has to be lower than the quantization noise, which, for a 10 bit ADC with an input range of V_{REF}, is equal to:

$$P_Q = \frac{LSB^2}{12} = \frac{1}{12}\left(\frac{V_{REF}}{2^{10}}\right)^2. \tag{2.20}$$

Therefore, the condition on the sampling capacitance C_s is:

$$\frac{kT}{C_s} < P_Q \;\Rightarrow\; \frac{kT}{C_s} < \frac{1}{12}\left(\frac{V_{REF}}{2^{10}}\right)^2 \;\Rightarrow\; C_s > 12kT\left(\frac{2^{10}}{V_{REF}}\right)^2. \tag{2.21}$$

Since $V_{REF} = 0.8\,V$, then $C_s > 81.43\,fF$. This means that since the equivalent sampling capacitance of the DAC scheme used is equal to $62C_u$, as it can be calculated from Fig. 2.11, the unit capacitance has to be:

$$C_u > 1.31\ fF. \tag{2.22}$$

A second constraint on the choice of the capacitance value in the DAC is set by the mismatch between DAC capacitors. Assuming random capacitance values with normal distribution and a standard deviation inversely proportional to the square root of the area, the mismatch of the capacitors is given by

$$\sigma\left(\frac{\Delta C}{C}\right) = \frac{A_C}{\sqrt{W_C L_C}}, \tag{2.23}$$

where W_C and L_C define the geometric dimensions of the capacitor and the factor A_C depends on the technology and on the capacitor type. For the 65 nm CMOS technology used in this work and for MIM (Metal-Insulator-Metal) capacitors (which were used for the design of the DAC as they have the lowest mismatch factor among the available capacitor types), A_C is equal to $0.86\% \cdot \mu m$. The standard deviation of a single capacitor is by a factor $\sqrt{2}$ smaller than the standard deviation of the difference of two capacitors, hence

$$\sigma(C) = \frac{C \cdot A_C}{\sqrt{2W_C L_C}} = \sqrt{\frac{c_A \cdot C}{2}} A_C, \tag{2.24}$$

where the factor c_A is the capacitance per unit area $\left[c_A = \frac{C}{W_C L_C}\right]$, which, for the used technology, is equal to $2\frac{fF}{\mu m^2}$. The goal in dimensioning the capacitance is to guarantee a probability grater than 99.73% (3σ) that the error of the DAC output voltage V_{DAC} due to capacitance mismatch is smaller than half LSB:

$$3\sigma(V_{DAC}) < \frac{1}{2}LSB = \frac{V_{REF}}{2 \cdot 2^n}. \tag{2.25}$$

The worst case for capacitor matching happens halfway through the dynamic range, where all the bits change value (the MSB switches from '0' to '1' and all the other bits from '1' to '0'). At this point of the ADC input-output characteristic, the DAC output voltage is

$$V_{DAC} = V_{REF1} - V_{IN} + \frac{\sum_{to\ REF} C_i}{\sum_{to\ REF} C_i + \sum_{to\ GND} C_i} V_{REF} \tag{2.26}$$

where the capacitor connected to V_{REF} ($\sum_{to\ REF} C_i$) is only the one associated to the MSB ($2^{\frac{n}{2}-1}C_u$) and the capacitors connected to ground ($\sum_{to\ GND} C_i$) are the rest of the capacitors in the MSB array in parallel with the equivalent capacitance C_{eq} seen from the MSB array. Equation 2.26 can be written as:

$$V_{DAC} = V_{REF1} - V_{IN} + \frac{X_1}{X_1 + X_2} V_{REF}, \tag{2.27}$$

where

$$\begin{aligned} X_1 &= 2^{\frac{n}{2}-1}C_u \\ X_2 &= \left(2^{\frac{n}{2}-1} - 1\right) C_u + C_{eq} \approx 2^{\frac{n}{2}-1}C_u. \end{aligned} \tag{2.28}$$

So, an expression for the uncertainty in the DAC output voltage can be found as a function of the uncertainty in the unit capacitance value of Eq. 2.24, using the error propagation theory. If $f(x_1, x_2, \ldots, x_n)$ is a function of n variables $(x_1, x_2, \ldots, x_n)$ affected by some known uncertainty $(\sigma(x_1), \sigma(x_2), \ldots, \sigma(x_n))$, then the uncertainty in f can be calculated as:

$$\sigma^2(f) = \left(\frac{\partial f}{\partial x_1}\right)^2 \sigma^2(x_1) + \left(\frac{\partial f}{\partial x_2}\right)^2 \sigma^2(x_2) + \cdots + \left(\frac{\partial f}{\partial x_n}\right)^2 \sigma^2(x_n). \tag{2.29}$$

By applying the previous equation to V_{DAC} in (2.27), we get:

$$\begin{aligned} \sigma^2(V_{DAC}) &= \left[\left(\frac{\partial V_{DAC}}{\partial X_1}\right)^2 \cdot \sigma^2(X_1) + \left(\frac{\partial V_{DAC}}{\partial X_2}\right)^2 \cdot \sigma^2(X_2)\right] V_{REF}^2 = \\ &= \left[\frac{X_2^2}{(X_1 + X_2)^4}\sigma^2(X_1) + \frac{X_1^2}{(X_1 + X_2)^4}\sigma^2(X_2)\right] V_{REF}^2, \end{aligned} \tag{2.30}$$

where

$$\sigma^2(X_1) = \sigma^2(2^{\frac{n}{2}-1}C_u) = 2^{\frac{n}{2}-1}\sigma^2(C_u) \tag{2.31}$$

$$\sigma^2(X_2) = \sigma^2\left(\left(2^{\frac{n}{2}-1}-1\right)C_u + C_{eq}\right) = \left(2^{\frac{n}{2}-1}-1\right)\sigma^2(C_u) + \sigma^2(C_{eq}). \tag{2.32}$$

C_{eq} is the series of the bridge capacitor (equal to C_u) and the LSB array (rounded to $C_{LSB} = 2^{\frac{N}{2}}C_u$):

$$C_{eq} = \frac{C_u \cdot C_{LSB}}{C_u + C_{LSB}}. \tag{2.33}$$

Since $\sigma^2(C_{LSB}) = 2^{\frac{N}{2}}\sigma^2(C_u)$, applying again the error propagation theory, $\sigma^2(C_{eq})$ can be found as a function of $\sigma^2(C_u)$:

$$\sigma^2(C_{eq}) = \frac{2^{2n} + 2^{\frac{n}{2}}}{(2^{\frac{n}{2}}+1)^4}\sigma^2(C_u). \tag{2.34}$$

Substituting (2.34) in (2.32), it results:

$$\sigma^2(X_2) = \left[2^{\frac{n}{2}-1} - 1 + \frac{2^{2n} + 2^{\frac{n}{2}}}{(2^{\frac{n}{2}}+1)^4}\right]\sigma^2(C_u). \tag{2.35}$$

Eventually, substituting (2.28), (2.31), (2.35) in (2.30), an expression of $\sigma^2(V_{DAC})$ as a function of $\sigma(C_u)$ can be found and, using Eq. 2.24, it can be expressed as a function of the unit capacitance C_u:

$$\sigma^2(V_{DAC}) \approx \frac{(2^{\frac{n}{2}-1}C_u)^2}{(2^{\frac{n}{2}}C_u)^4}\left(2^{\frac{n}{2}} - 1 + \frac{2^{2n} + 2^{\frac{n}{2}}}{2^{2n}}\right)\frac{c_A C_u}{2}A_C^2 V_{REF}^2. \tag{2.36}$$

In order for (2.25) to be satisfied, we get:

$$C_u > 9\frac{2^{\frac{n}{2}}(2^{2n}+1)}{2^{n+1}}c_A A_C^2. \tag{2.37}$$

In Fig. 2.14 the minimum value of C_u is plotted as a function of the number of bit: it can be seen that C_u has to be larger than around 22 fF for $n = 10$, which is a more stringent constraint than (2.22).

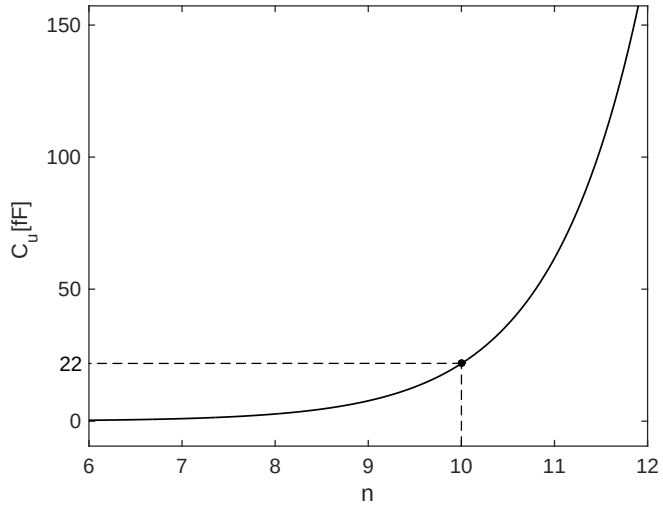


Figure 2.14: Minimum of C_u to guarantee $3\sigma(V_{DAC}) < \frac{1}{2}LSB$ as a function of the number of bit.

2.8 Capacitor DAC layout

When capacitors are fabricated, etching beneath the borders of the mask causes an error in the capacitance ratio between capacitors, creating potentially large non-linearities errors as resolution increases [40]. Fig. 2.15 shows the designed area $A = W_C L_C$ and the achieved one $A_C^* = W_C^* L_C^*$: the second can be written as $A^* = W_C L_C - 2(L_C + W_C)\Delta x$, where Δx is the undercut length. Therefore:

$$A^* \approx A - P\Delta x, \tag{2.38}$$

where P is the designed perimeter. The solution adopted for this problem is not to use one MIM capacitor for each capacitance value needed, but different numbers of unit capacitors connected in parallel, because undercut effect gives the same proportional reduction if the perimeter-to-area ratio for each capacitance value is kept constant, as Eq. 2.38 shows. Beside this, a non-uniformity in the fabrication process can cause gradients in the oxide growth, the consequences of which can been limited by the use of a layout with a common centroid structure, so that the first-order gradient related errors average out

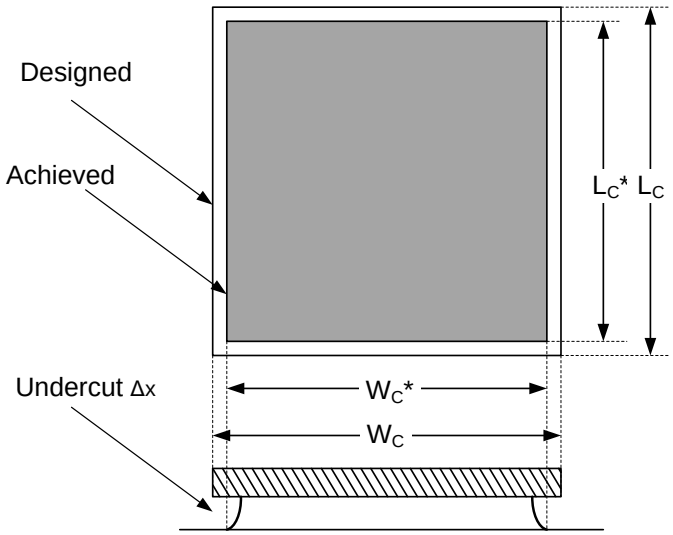


Figure 2.15: Undercut effect on MIM capacitors (top view and cross section).

and are the same for every capacitor. To comply with all the constraints, in the design of the split capacitor DAC a unit capacitance of 35 fF was used (MIM capacitor of an area 4 $\mu m \times 4$ μm). The designed layout of the DAC is shown in Fig. 2.16. In the figure, the unit capacitance can be easily detected as it is replicated in two 4×8 matrices (one for the MSB array and the other for the LSB one). Each matrix includes a unit capacitor by itself, two unit capacitors connected together representing $2C_u$ and so on up to sixteen unit capacitors connected together representing 2^4C_u. A common bottom plate is used for the capacitors of the MSB array and a separate one is used for the LSB array in a dedicated metal level just above metal 7: they represent the nodes on the bridge capacitor plates, as it can be seen in figure 2.11. The top plates, fabricated in a dedicated metal just below metal 8, are connected together for capacitances multiple of the unit capacitance and are brought out of the DAC layout to be connected to V_{REF} or ground by means of switches. Another delicate issue in the design of the split capacitor DAC architecture, that arises in particular for small capacitance values, is represented by parasitic capacitances, which can alter the binary weighted structure and be responsible for non-linearities. Parasitics due to metal lines were accounted for by adding suitably designed metal strip to the layout of the metal interconnec-

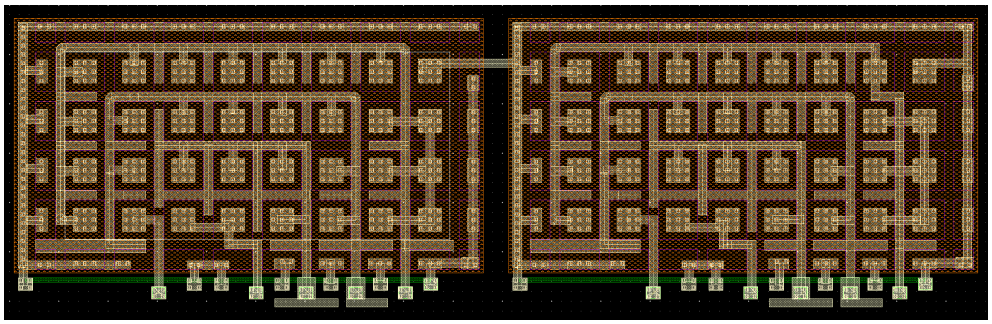


Figure 2.16: Split capacitor DAC layout.

tions. Actually, parasitic capacitances shunting the bridge capacitor terminals to ground can lead to linearity degradation. Charge cancellation techniques have been proposed in the literature to minimize the effects of this kind of parasitics on the DAC linearity performance [41]. However, a purely layout solution, like the one briefly mentioned above, was used in this case, to keep the area as small as possible.
Eventually, in order to have the same boundary condition on each unit MIM capacitor, all around the capacitor matrices, dummy MIM capacitors are designed with their top plates connected to the common bottom plate.
The total area occupied by the DAC capacitor is 97.73 $\mu m \times 29.22\ \mu m$. Since the interleaved architecture requires the presence of two DACs, the area occupied by them is the 47% of the total pixel area.

2.9 Bootstrap switch

In a switched capacitor circuit as the capacitive DAC described in the previous section, the input switch, the one involved in the DAC pre-charge phase, is required to work properly over the whole input signal range [0.2; 1] V. At low supply voltages (in this case 1.2 V), complementary CMOS switches are not the best solution for switching rail-to-rail analog signals. This is due to a region which appears in the middle of the input voltage range, where both transistors are close to the weak-inversion region. This results in different switch on-resistance with respect to the input voltage as it is shown in Fig. 2.17, where dimensions of the MOSFET transistors are $W_{NMOS} = W_{PMOS} = 2\ \mu m$ and $L_{NMOS} = L_{PMOS} = 60\ nm$ and their threshold voltages are the minimum available in the used technology

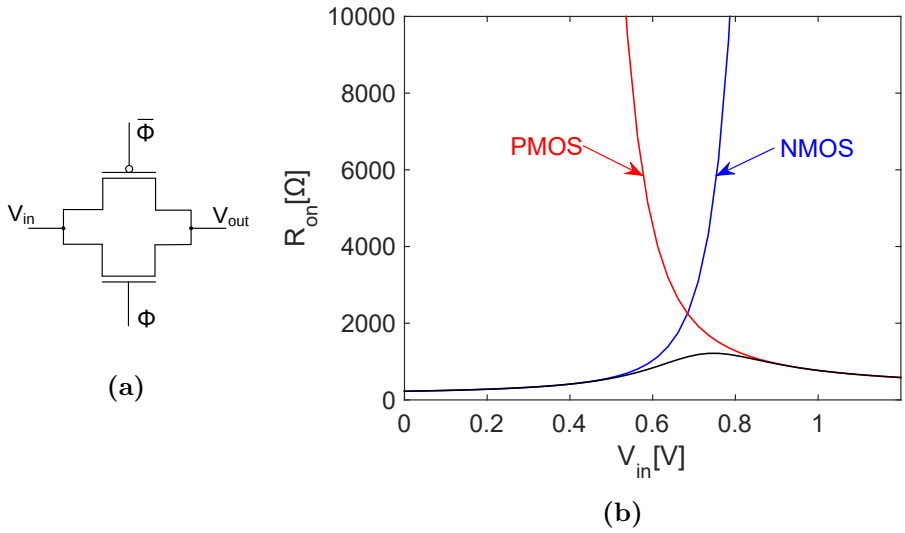


Figure 2.17: CMOS switch scheme (a) and its simulated on resistance as a function of the input voltage (b).

($V_{th,NMOS} = 462\ mV$ and $V_{th,PMOS} = 498\ mV$). This causes a worsening of the ADC linearity performance. Hence for the two switches involved in the pre-charge phase, the one which connects the top plates of the DAC MIM capacitance to V_{in} and the one which connects the common bottom plate on the DAC MIM capacitance to V_{REF1}, a gate-source bootstrap technique is used [42]. In Fig. 2.18 a simple scheme of the bootstrap switch used is represented. The figure shows the signal switch MN_{SW} together with five additional switches (S1-S5) and an additional capacitor C_{offset}. Switches S3 and S4 charge the capacitor during Φ1 to VDD. During Φ2 switches S1 and S2 add the pre-charged capacitor in series with the input voltage V_{IN}, such that the gate-source voltage of transistor MN_{SW} is equal to the voltage V_{DD} across the capacitor. This guarantees maximum switch conductance independently of the input voltage. Switch S5 sets the gate voltage of MN_{SW} to ground during Φ1 to make sure that the transistor is in the OFF state.
Another advantage of the bootstrap technique is the minimization of the charge injection effects. Indeed, since the bootstrap technique enables to keep the ON gate-source voltage of MN_{SW} equal to VDD over the whole input range, the charge injected is at first approximation always the same, hence its effects on the switch performance are minimized.
The transistor level implementation is shown in Fig. 2.19. Transistors MN1,

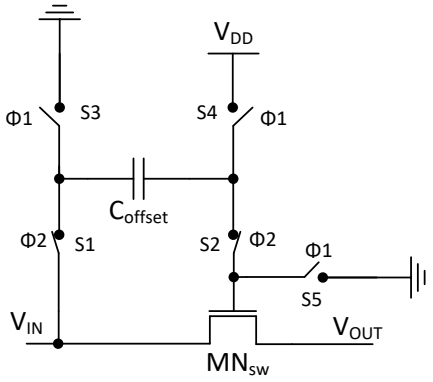


Figure 2.18: Basic bootstrap switch circuit.

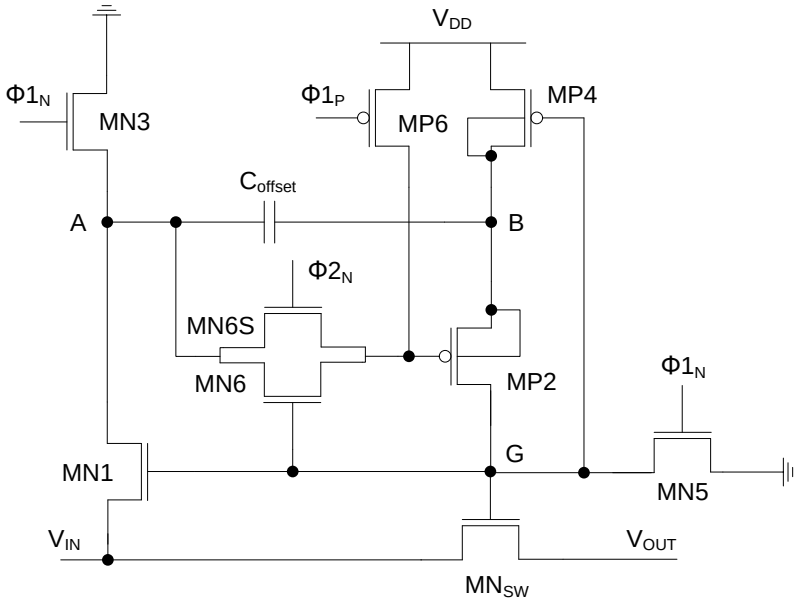


Figure 2.19: Bootstrap switch circuit at transistor level.

MP2, MN3, MP4 and MN5 correspond to the five ideal switches S1-S5 shown in Fig. 2.18 respectively. Additional transistors and modified connectivity shown in Fig. 2.19 were introduced to extend all switch operation from rail to rail, while limiting all gate-source voltages to VDD. The worst case input signal (with respect to switch operation), since the signal switch MN_{SW} is a NMOS transistor, is $V_{IN} = V_{DD}$, which is the value attributed to V_{IN} in the discussion hereafter. An apparent problem is that of the n-transistor MN1, which has to switch V_{DD}, but as it is the same problem as that of MN_{SW}, its gate is tied to that of MN_{SW}, where a gate-source potential of V_{DD} assures its high conductivity during $\Phi 2$. The gate potential then drops to zero during $\Phi 1$, to cutoff both transistors. Furthermore, the voltages at nodes B and G reach 2 V_{DD}, but transistor MP4 must remain OFF during $\Phi 2$, in order not to lose the charge stored on C_{offset} during $\Phi 1$. If the clock is used to drive it as shown in Fig. 2.18, its gate-source voltage would be $-V_{DD}$ and the transistor would not be able to be turned OFF. Hence its gate is connected to node G, which provides a voltage of 2 V_{DD} during $\Phi 2$, cutting-off the transistor, and it is connected to ground, during $\Phi 1$ which ensures its high conductivity. Besides, transistor MP2 gate-source voltage, using the clock as shown in Fig. 2.18, would be -2 V_{DD} during $\Phi 2$. In Fig. 2.19 transistor MN6 is used to connect the gate of MP2 to node A, keeping its gate-source voltage equal to $-V_{DD}$ (the voltage across C_{offset}) during $\Phi 2$. During $\Phi 1$, transistor MP6 connects it to V_{DD} turning it OFF. The gate of MN6 is tied to node G to keep it conducting as the voltage on node A rises to V_{DD} during $\Phi 2$. Therefore a dependency loop is present: in order that MN6 conducts, it must have a sufficient gate-source voltage, i.e. MP2 must then be conducting. Transistor MN6S is then necessary as a startup to force transistor MP2 to conduct and it is assumed to conduct only when the voltage of node A is close to zero (which is the case at the beginning of $\Phi 2$). When MP2 conducts, the voltage on node G rises to 2 V_{DD}, while node A rises to V_{DD}, thus MN6S turns OFF while MN6 remains ON. At last, the bulk of transistors MP2 and MP4 is tied to the highest potential, i.e. node B, and not to V_{DD}.

The two phases $\Phi 1$ and $\Phi 2$ are generated from the `Start` signal, obtained as the synchronization of the external `trigger` signal with the external `clock` and indicating the beginning of the ADC operation. They have to be two non-overlapping signals, in order to avoid the leakage of the charge storage in C_{offset} at the moment of the switch. The two complementary non-overlapping phases are generated with the logic circuit in Fig. 2.20. If the `Start` signal is at low level, $\Phi 2_N$ ='0' and $\Phi 1_N$ ='1'. When `Start` goes high, the top NOR switches, but there is a delay of three logic ports (3τ) before the output $\Phi 1_N$

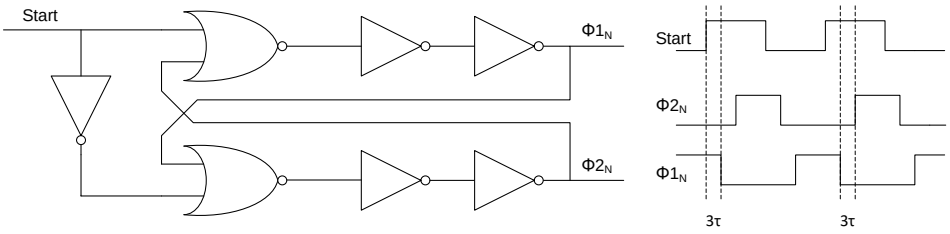


Figure 2.20: Logic circuit used to generate two non-overlapping phases.

goes low. Following this transition both inputs of the bottom NOR become zero and after a further 3τ delay, $\Phi 2_N$ becomes '1'. Therefore, the non-overlapping time is equal to three logic ports delays. The $\Phi 1_P$ signal is generated from $\Phi 1_N$ simply with an inversion.
The period of both the signals $\Phi 1$ and $\Phi 2$ is twice the sampling period: the `Start` signal is generated by a divide-by-2 counter from the `trigger` signal synchronized with the `clock`. The reason for this is the interleaved architecture described in section 2.4.

2.10 Dynamic latched comparator

Beside the DAC, the other most critical component of a SAR ADC is the comparator. The most important features of the comparator are listed in the following:

- Sensitivity: a 10-bit ADC requires a sensitivity of at least 1/2 LSB, that corresponds to $V_{REF}/(2 \cdot 1024) \approx 390\ \mu V$, since $V_{REF} = 800\ mV$.

- Amplifier response time: it is the minimum time required to achieve the proper logic output as a response to the minimum input step. It cannot exceed the minimum clock period, where the minimum clock period is the minimum sampling period divided by eleven (ten bits decisions, plus one extra period for sampling).

- Overdrive recovery time: it is the extra time the gain stage takes to react and generate the voltage required to produce the output logic, when the previous input signal is large enough to saturate it to the positive or negative rails.

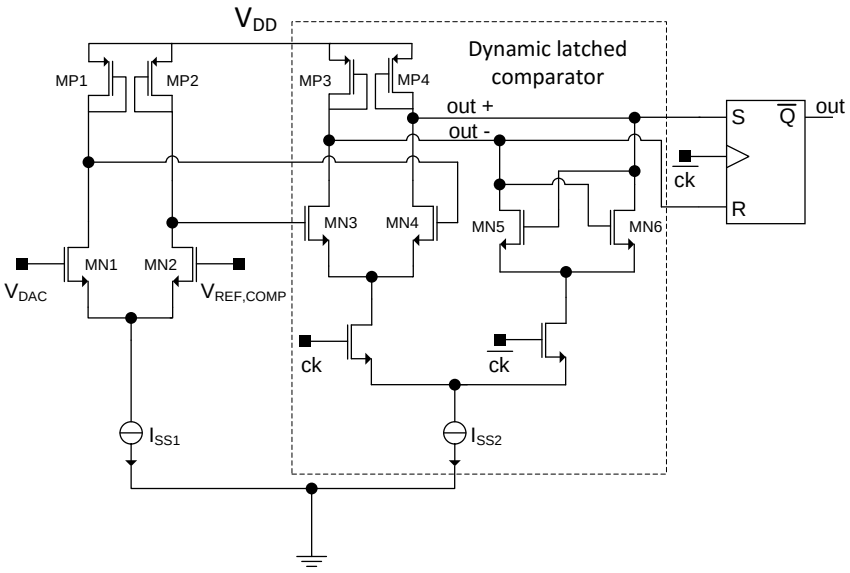


Figure 2.21: MOS level schematic of the designed comparator.

- Input offset: it has to be as low as possible, even if it can be taken into account with a calibration step at the beginning of the operation.

- Power consumption: it must be limited, in order to integrate the ADC in a 64×64 matrix. The maximum power consumption was set to 70 μW.

The designed comparator is a dynamic latched comparator. It consists of the cascade of an amplifier and a latch, working in two separate phases: for each decision of the comparator one clock period is allocated, half of which (clock signal high level) is dedicated to the amplification of the DAC output, and the other half (clock signal low level) to the final decision taken by the latch, taking advantage of its positive feedback mechanism to regenerate the amplifier output into a large signal. The MOS level schematic of the designed comparator is represented in Fig. 2.21. The amplification stage and the latch are powered alternatively, half clock period each. A linear pre-amplification stage is also introduced in the comparator design, for two main reasons:

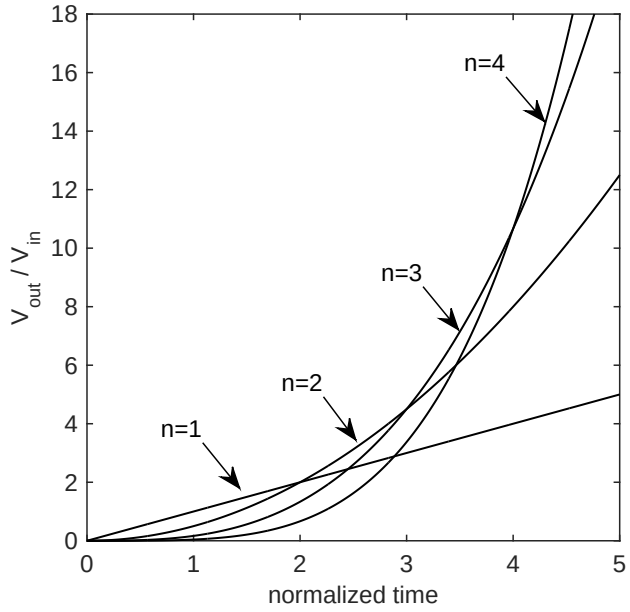


Figure 2.22: The beginning of the ideal step response of the cascade of n equal gain stages, each modeled by a single pole transfer function. The time on X-axes is normalized to the time constant of each stage.

- to split the needed amplification in two stages in order to increase the bandwidth and reduce the response time;
- to decouple the dynamic latched comparator, suffering from kickback noise problems, from the previous capacitive DAC [43].

The gain provided by the amplification stage has to be sufficiently high to produce a proper output to drive the latch in the available time. For high frequency applications the static gain is not the key parameter. The time required to obtain a proper output level is normally much less than the time constant of the gain stage. Therefore, just the initial part of the step response is effective. What is important is not the asymptotic value but the voltage amplitude that the output reaches in the time-slot available. In Fig. 2.22 the initial part of the step response of a different number (n) of equal gain stages is represented (for each gain stage a single pole model is used) [44]. For a single stage the output is a ramp, in the case of two stages it is the convolution of a ramp with a ramp, so a quadratic curve, for three stages it is a cubic curve

Name	**Size [μm/μm]**
$MN1, MN2$	12/0.5
$MP1, MP2$	4/1
$MN3, MN4$	6.8/0.45
$MP3, MP4$	1/1
$MN5, MN6$	4/0.3

Table 2.1: Comparator's MOSFETs sizes.

and so on. For a specified gain, an optimum number of stages can be found. The amplification needed to properly drive the latch with the minimum input (1/2 LSB) at the minimum clock period ($T_{ck,min} = 200/11\ ns$) is around 8. Simulations show that two amplification stages, each providing a gain of $\sqrt{8}$), are sufficient to satisfy the dynamic gain requirements.
As previously mentioned, the dynamic latched comparator suffers from kick-back noise problems. It means that the large voltage variations on the regeneration nodes of the latch output (in Fig. 2.21 nodes $out+$ and $out-$) are coupled, through the gate-drain parasitic capacitances of the input transistors ($MN3$ and $MN4$), to the input of the dynamic latched comparator. If the comparator is directly connected to the capacitive DAC output, since the DAC does not have zero output impedance, a disturbance with peak values in the order of several mV can be observed at the comparator input, degrading the accuracy of the converter. The insertion of a preamplification stage solves the problem, decoupling the capacitive DAC output from the dynamic latched capacitor input.
The available power budget for the comparator is split between the preamplification stage and the dynamic latched comparator as follows: 35 μA for the preamplifier and 20 μA for the dynamic latched comparator. Indeed, even if the two amplification stages provide almost the same gain, they are not identical, as it can be seen in Table 2.1, showing the dimensions used for the comparator transistors. The different design of the two stages is related to their different contribution to the input offset due to mismatch. In the first approximation, each differential stage input offset is proportional to:

$$V_{os} \approx \sigma_{V_{th}} = \frac{A}{\sqrt{WL}}, \tag{2.39}$$

where A is a technological parameter expressed in $[mV \times \mu m]$ and $W$and L are the MOSFET sizes (width and length). Since there are two gain stages, the input offset is obtained as:

$$V_{os}^2 = \sigma_1^2 + \frac{\sigma_2^2}{G^2} \approx A^2 \left(\frac{1}{(WL)_1} + \frac{1}{8} \frac{1}{(WL)_2} \right), \tag{2.40}$$

where $(WL)_1$ and $(WL)_2$ are the area of the input MOSFET respectively of the first and the second gain stage and $G = \sqrt{8}$ is the gain of the first stage. Indicating with m the $(WL)_2/(WL_1)$ ratio, such that $(WL)_2 = m(WL)_1$, from 2.40:

$$V_{os}^2 \approx A^2 \left[\frac{8m+1}{8m(WL)_1} \right]. \tag{2.41}$$

From the previous equation, the sum of the areas occupied by the input MOSFETs of the two gain stages can be calculated as a function of m:

$$area_{sum} = (WL)_1 + m(WL)_1 \approx (1+m) \frac{8m+1}{8m} \frac{A^2}{V_{os}^2}. \tag{2.42}$$

To obtain a specified V_{os}, for a given parameter A, the factor m can be calculated in order to minimize the area occupation, finding the minimum of the following function:

$$f(m) = (1+m) \frac{8m+1}{8m}. \tag{2.43}$$

In Fig. 2.23 the trend of the function $f(m)$ is represented. The minimum is obtained for m almost equal to 0.35. From simulations, as it can be noticed from the values of Table 2.1, the optimum value for m is about 0.5. The achieved input offset voltage is about 1.94 mV, as it can be seen in Fig. 2.24, where an histogram, with a superimposed gaussian curve, shows the Monte-Carlo simulation results on the dispersion of the offset in the designed comparator. The comparator offset results in an offset on the whole input-output characteristic of the ADC, without degrading the linearity performance. Hence an offset larger than the LSB is not critical and it can be taken into account with a post-elaboration of the ADC outputs.

Fig. 2.21 shows also the presence of a clocked SR flip-flop after the dynamic latch comparator. The stage is included to generate, a full scale digital signal from the large output signal produced by the latch. The flip-flop is sensitive to the comparator output only during the latch phase, while during the amplification phase it maintains the previous state, as it is shown in the truth table 2.2.

Fig. 2.25 shows the simulated time evolution of the comparator signals. In par-

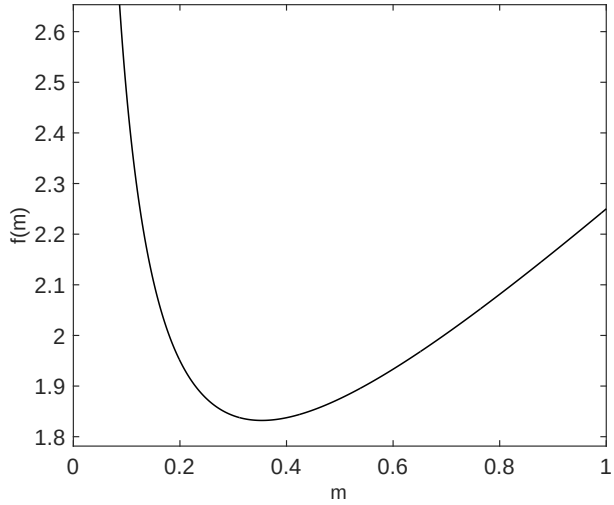


Figure 2.23: Plot of the function f(m) (Eq. 2.43). The ratio (m) between the areas of the input MOSFETs of the two comparator's stages which minimizes the area occupation, for a desired offset, is the one which minimizes f(m).

$\overline{ck}$	**S**	**R**	**Q**
0	×	×	latch
1	0	0	latch
1	0	1	0
1	1	0	1
1	1	1	×

Table 2.2: SR flip-flop truth table.

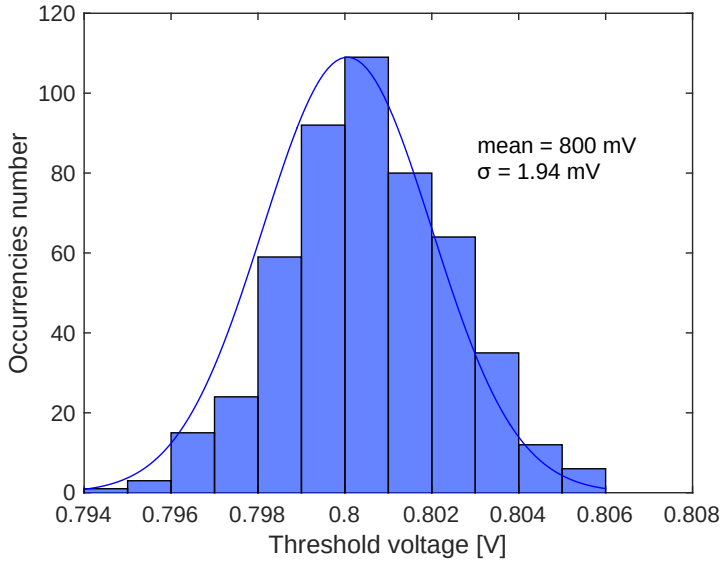


Figure 2.24: Monte-Carlo simulation results on the comparator input offset, shown as an histogram with a superimposed gaussian curve.

ticular the figure shows an example of the comparator response to an input signal (V_{in}) large enough to saturate the dynamic latch comparator output and to a small signal just above the comparator threshold (1 mV), to show its robustness with respect to the overdrive time recovery. When the clock signal is in its high logic level, the preamplification of the input signal takes place, while, when the clock logic level is low, the latch regenerates the amplification outputs into large signals. After the latch, the clocked SR flip-flop produces the final logic output of the comparator and, as it can be seen in figure, it is available after the clock falling edge.
Fig. 2.26 shows the comparator layout. To minimize the mismatch effects on the input offset, multi-finger transistors are used in common centroid structures, in particular for the current mirrors used for comparator biasing and for the differential input pairs of the amplification stages. In the periphery of the common centroid structures, dummy transistors are placed to guarantee the same boundary condition to each transistor. The total area occupied by the comparator is about 20.09 $\mu m \times 12.72\ \mu m$.

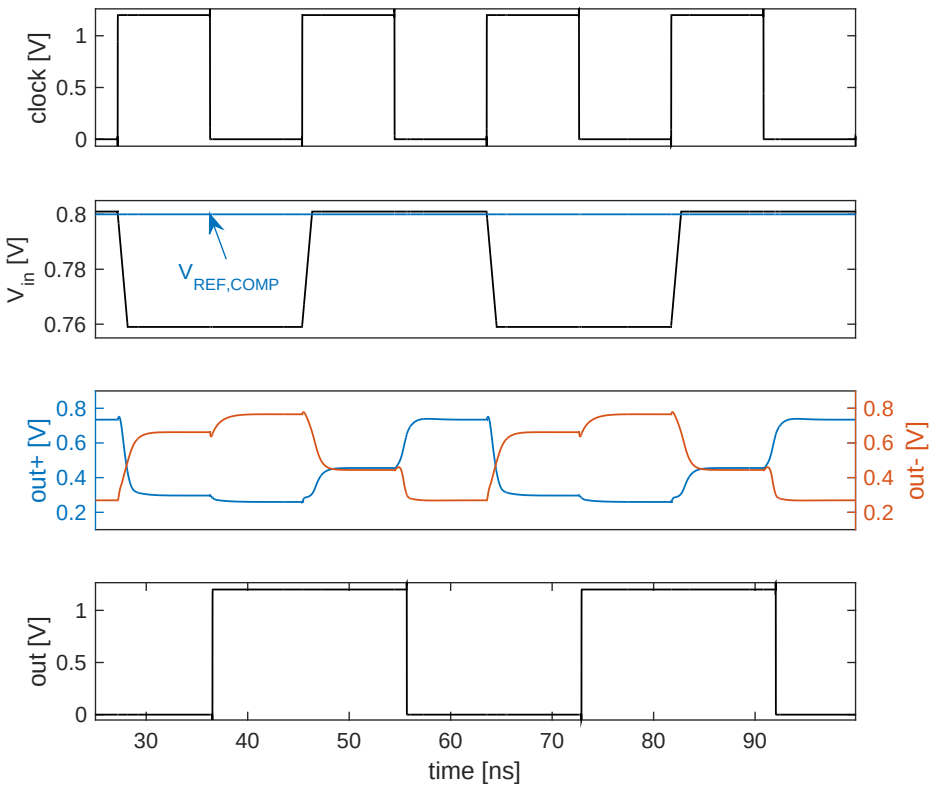


Figure 2.25: Time evolution of the comparator signals in response to an input signal (V_{in}) large enough to saturate the dynamic latch comparator output and to a small signal just above the comparator threshold (1 mV).

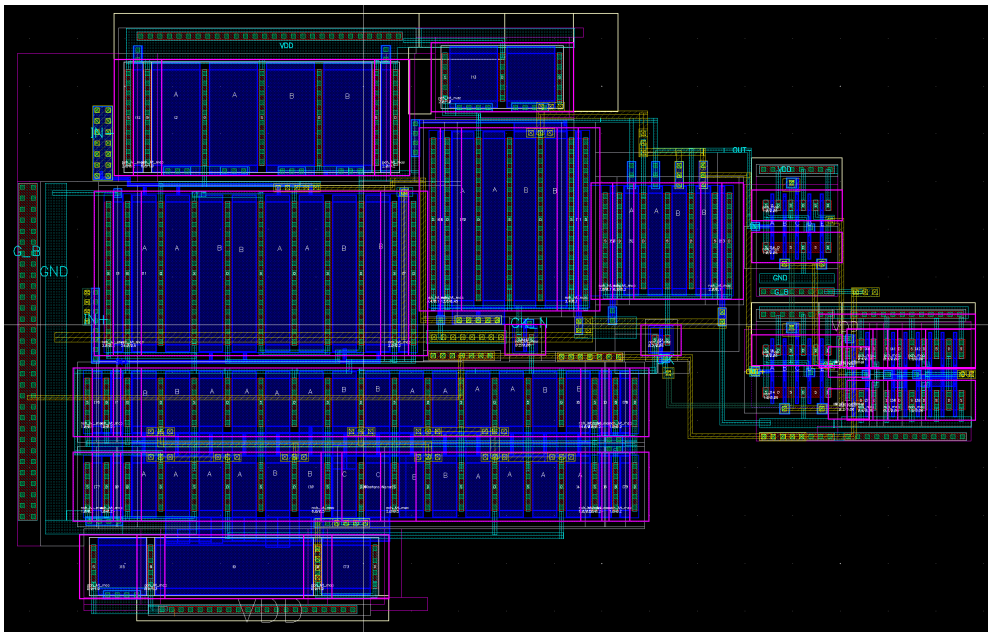


Figure 2.26: Comparator layout.

2.11 SAR logic

The successive approximation register logic is the block of a SAR ADC which controls the correct timing of the converter operations, beside storing bit after bit the conversion result. It has to initialize one bit after the other to '1', starting from the MSB, and to store the logic state set by the comparator, until the conversion on the next sample begins. In that moment the register is reset. This operation can be performed by the circuit of Fig. 2.27, including a shift register in the top line, consisting of a sequence of delay flip-flops, where the output of each flip-flop is the input of the subsequent one. The input of the first flip-flop of the shift register is the signal generated by the external `trigger` synchronized with the `clock` by means of the first two flip-flops on the top left of the figure. Indeed the conversion operation has to start upon arrival of the external `trigger`, which is internally synchronized with the `clock`. Hence, at the first rising `clock` edge after the `trigger` goes to '1', a '1' is presented at the input of the shift register (which is reset as all the SAR logic flip-flops at the beginning of the conversion operation) and clock after clock it shifted trough the whole register. Each time a logic '1' shifts in

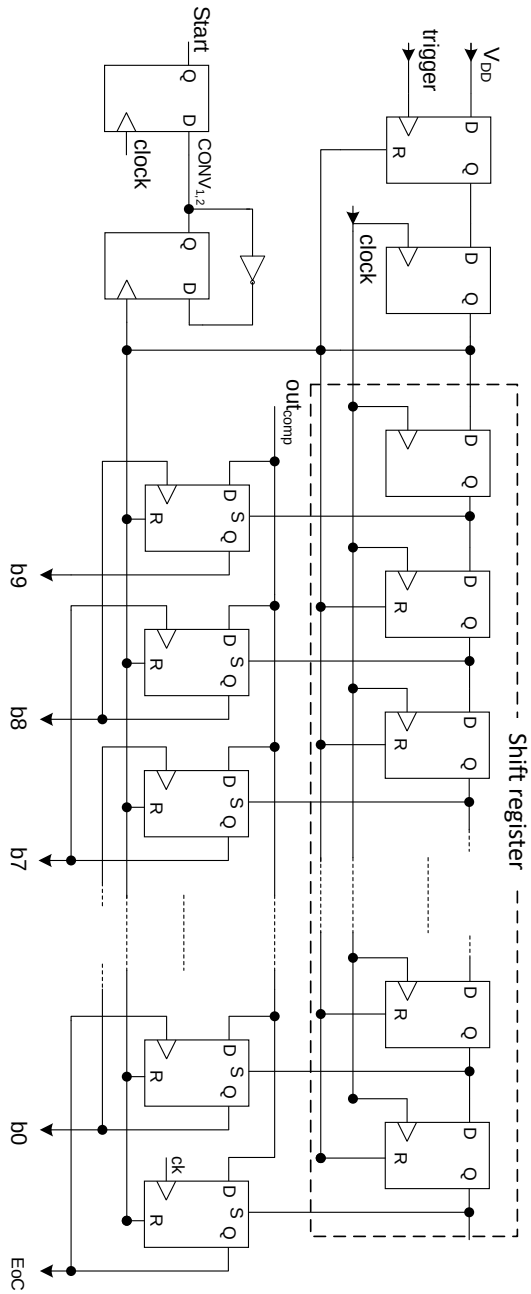


Figure 2.27: Schematic of the Successive Approximation Register logic.

a flip-flop of the shift register, it sets the output of the corresponding flip-flop on the line below to '1'. Then that flip-flop, after a clock period, when the subsequent flip-flop is set to one, stores the logic state of the comparator output, which is presented at its input. When the last flip-flop of the bottom line is set (10 clock periods after the beginning of the conversion), it generates the *end-of-conversion* (`EoC`) signal, whose high logic state indicates the end of the conversion operation. The outputs of the flip-flops in the bottom line of Fig. 2.27 control the DAC switches and represent the ADC digital output word.
Furthermore, the SAR logic generates the signals for the interleaving timing, $\texttt{CONV}_{1,2}$ and `Start`, from which the two phases for the bootsrap switches are generated. $\texttt{CONV}_{1,2}$ is obtained by a divider by two from the `trigger` signal syncronized with the `clock`, while `Start` is simply a version of $\texttt{CONV}_{1,2}$ shifted by one `clock` period. In the next session a time diagram showing the main ADC signals is shown.

2.12 Overall view of the ADC and its layout

After having described in detail each block of the ADC, Fig. 2.28 shows the principal simulated ADC signals during two consecutive conversions on an input voltage ramp, the first giving as result '`0011110101`' and the second '`0100101001`'. Since the ADC has a time-interleaved architecture (see Fig. 2.13), the first conversion is performed on one of the two DACs and the second conversion is performed on the other DAC. Each conversion lasts eleven clock periods, starts at the first rising edge clock after the trigger goes to '1' and ends with the rising edge of the `EoC` signal. The comparator output is available each falling edge clock. Between the commutation of $\texttt{CONV}_{1,2}$ (the signal which switches the DACs at the comparator input) and $\Phi 1$ or $\Phi 2$ (the two phases of the sampling bootstrap switches) there is a clock period: this is foreseen to guarantee that the sampled voltage could reach its regime, continuing the sampling of the input voltage on a DAC for a clock period after that DAC has been connected to the comparator input.
Fig. 2.29 shows the layout of the complete interleaved SAR ADC, where the main blocks are framed with different colors. The layout is designed to be as more symmetric as possible and its dimensions are $108 \times 74\ \mu m^2$. The ADC layout has been designed in order to fit the 110 μm pitch pixel, together with the rest of the analog channel and the digital logic, which manages the readout of the matrix and which is not discussed in this thesis. Fig. 2.30 shows the complete layout of the pixel, where the analog channel, the ADC and the logic

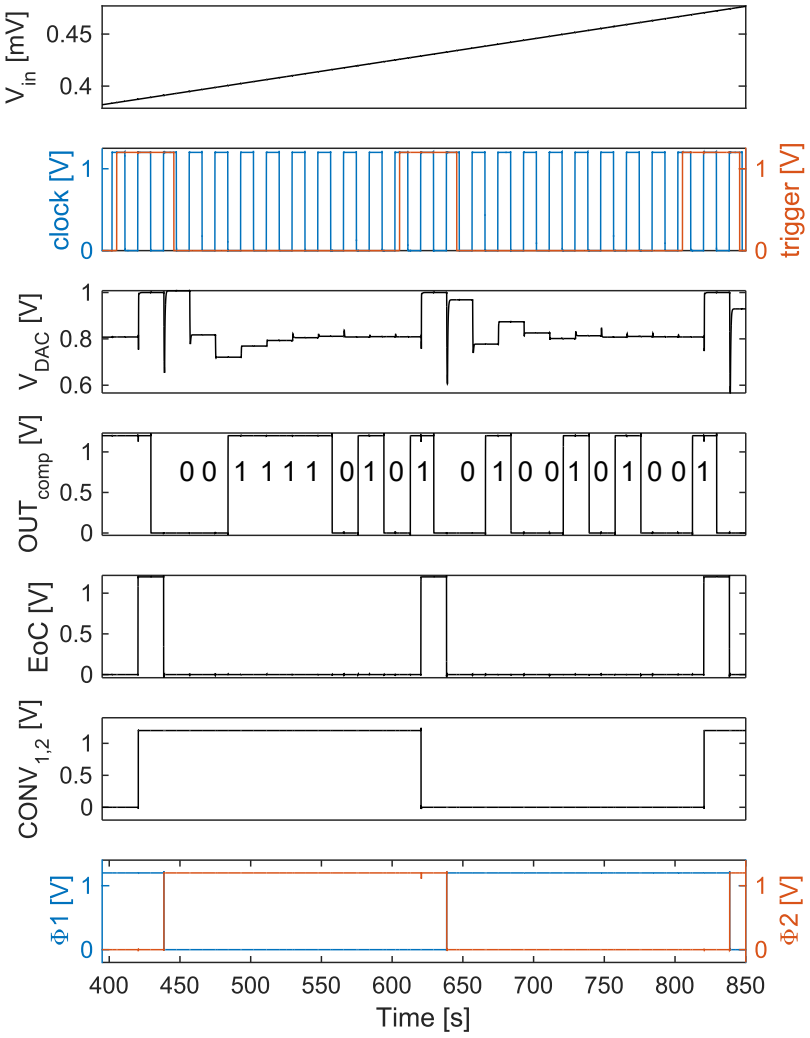


Figure 2.28: Simulated time diagram of the main ADC signals.

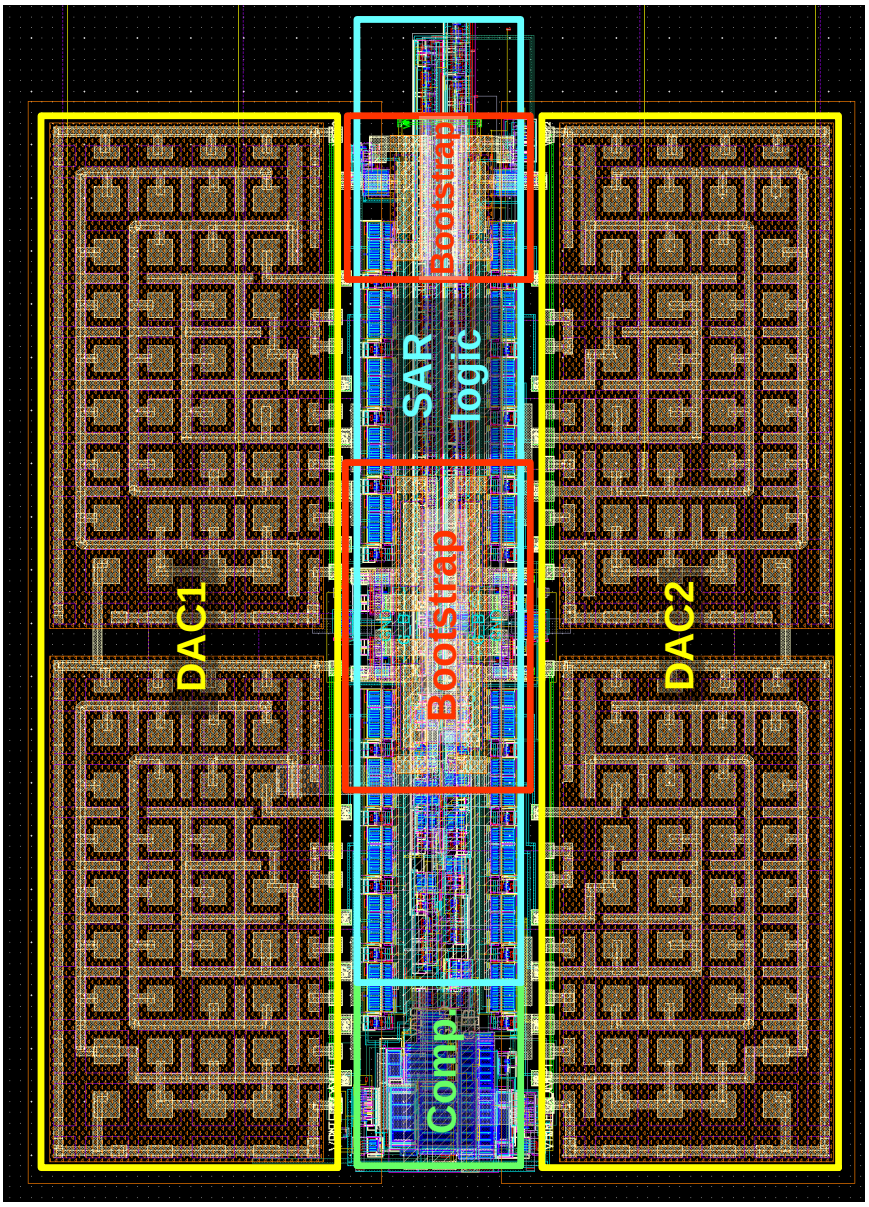


Figure 2.29: Layout of the interleaved SAR ADC [$108 \times 74\ \mu m^2$]. The two DACs in a yellow frame, the comparator in a green frame, the SAR logic in a cyan frame and the bootstrap switched in a red frame.

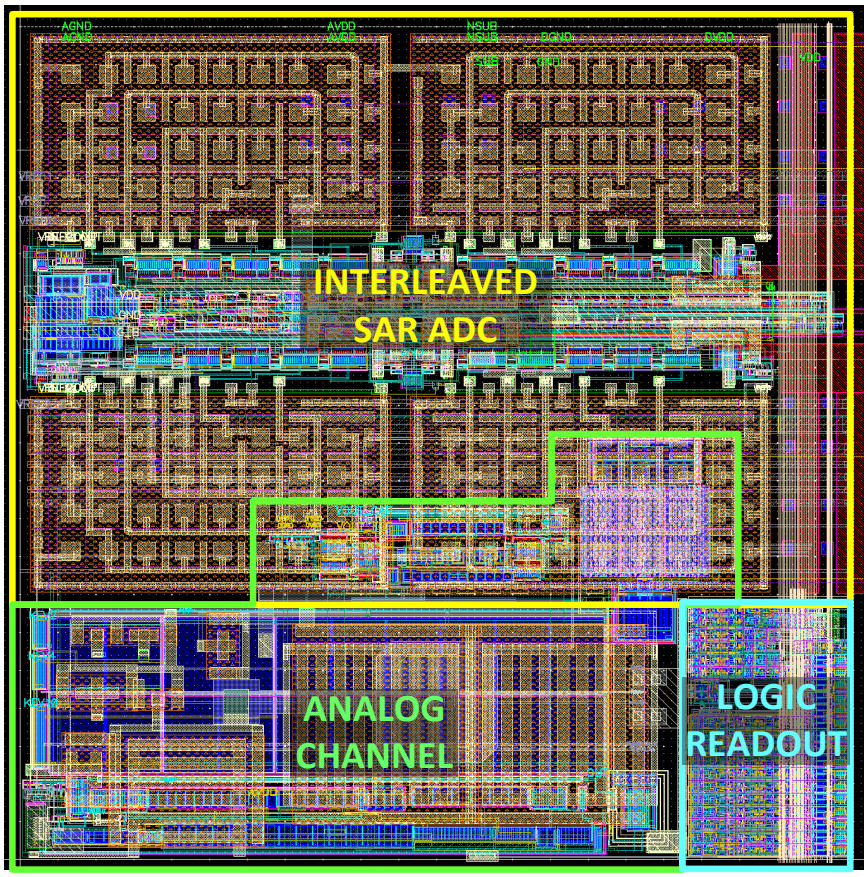


Figure 2.30: Layout of the pixel ($110 \times 110\ \mu m^2$), which includes the analog channel (in a green frame), the interleaved SAR ADC (in a yellow frame) and the readout logic (in a cyan frame).

for the readout are framed in different colors. The figure shows that part of the analog channel is placed beneath the MIM capacitors of the DAC which adjoins the analog channel itself.

Chapter 3

Test setup and measurement results

This chapter presents the test setup and the experimental results from the characterization of a test chip integrating different layout options for the time-interleaved SAR ADC discussed in this work. In the first part, the test chip and the different ADC layouts will be described. Then the measurement setup will be presented, from the test boards to the instrumentation used for the characterization. Eventually, after a description of the MATLAB programs for data post-processing, the main measurement results will be presented and discussed.

3.1 Test chips

A test chip has been submitted for fabrication, together with another chip integrating a 8×8 matrix of readout channels. The chip integrates different test structures of the analog front-end and includes four layout options for the time-interleaved SAR ADC. These different layouts were included in the test chip in order to evaluate their effect on the ADC performance and to choose, based on the measurement results, the best trade-off between linearity performance and area. The four layouts are:

1. ADC without either metal shield or digital electronics beneath the capacitive DAC,

2. ADC with digital electronics, but no metal shield, beneath the capacitive DAC,

3. ADC with a shield in metal 6 and digital electronics beneath the capacitive DAC,

4. ADC with a shield in metal 6, but no digital electronics, beneath the capacitive DAC.

The 1^{st} layout is the one which minimizes the parasitic capacitance between the bottom plates of the DAC MIM capacitors and ground, but is also the most expensive in terms of area occupation ($108 \times 74\ \mu m^2$), since the area beneath the capacitive DAC is not used (the layout is shown in Fig. 2.29 and 2.30). A metal shield connected to ground makes it possible to place part of the ADC electronics beneath the DAC MIM capacitors, minimizing crosstalk problems between the ADC electronics and the DAC and consequently minimizing ADC noise. This solution enables the reduction of the ADC area to $108 \times 58\ \mu m^2$. However, the metal layer used for the shield has to be high enough to fit the electronics and the metal interconnection beneath it, therefore approaching the MIM capacitor bottom plates and increasing the parasitic capacitance between them and ground. To evaluate the metal shield effects on linearity performance, also an option with only metal shield but not the electronics under the capacitive DAC was designed and tested. Likewise, to evaluate the contribution to the ADC noise performance due to digital signals coupling with the DAC MIM capacitors, an option without shield but with part of the ADC electronics beneath the DAC was included.
Beside the different versions of the ADC layout, the test chip integrates analog front-end blocks and an injection bus in order to test the charge sensitive amplifier, consisting of an injection capacitance. The analog blocks included in the test chip are:

- a charge sensitive amplifier with an NMOS feedback transistor to achieve the dynamic signal compression;

- a charge sensitive amplifier with a PMOS feedback transistor to achieve the dynamic signal compression;

- a charge sensitive amplifier with an NMOS feedback transistor to achieve the dynamic signal compression and without the injection bus;

- a shaping stage by itself, made up of the transconductance amplifier and the flip capacitor filter;

- a complete front-end analog channel (CSA with NMOS feedback transistor, tranconductance amplifier and FCF) not including the injection bus;

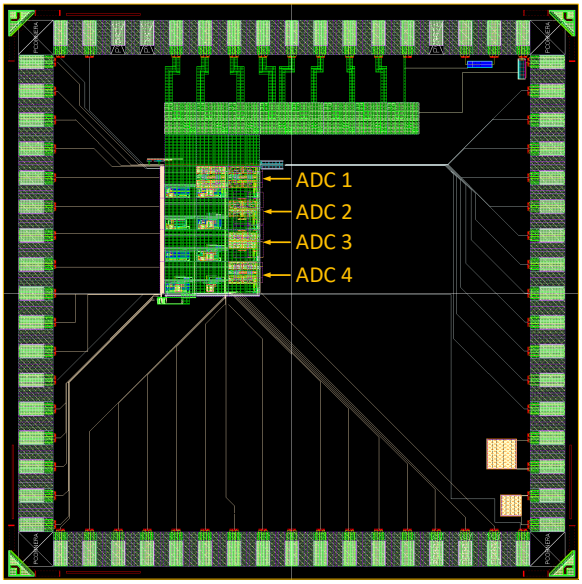


Figure 3.1: Layout of the test chip.

- a complete channel (CSA with NMOS feedback transistor, tranconductance amplifier, FCF and ADC);

- a complete front-end analog channel (CSA with NMOS feedback transistor, tranconductance amplifier and FCF);

- a complete front-end analog channel (CSA with PMOS feedback transistor, tranconductance amplifier and FCF);

A detailed report on the measurement results collected from the analog blocks can be found in [34].
In the test chip, the different blocks are organized in a 4×3 matrix. In the first two columns the analog blocks and the complete channels have been integrated, while in the third column the four ADC versions have been placed. Each cell can be selected through two input bits for the rows and two bits for the columns. The test chip layout is shown in Fig. 3.1.

3.2 Measurement setup

To perform an automated and systematic testing campaign on the ADCs, a proper measurement setup has been developed. Two testing PCBs (Printed Circuit Boards) have been designed: a main board and an ASIC carrier. The ASIC carrier hosts the test chip, which can be both soldered or wire bonded to the board, since part of the available chips are put in a package and part of them are available as bare dice. The ASIC carrier plugs into the main board through terminal sockets arranged on its periphery. All the bias and the digital control signals are brought to the ASIC carrier from the main board through those terminal sockets. The main board provides:

- the power supplies (analog and digital power supplies are separated on chip) through adjustable voltage regulators;
- an input voltage for the stand alone ADCs, through a commercial 16 bit DAC controlled via SPI (Serial Peripheral Interface);
- voltage references for both the analog front-end blocks and the ADCs through adjustable voltage regulators;
- current references for the analog front-end blocks;
- static digital inputs, such as configuration bits, through a DIP switch array with pull up resistors.

Figure 3.2 shows the measurement setup. A graphic rendering of the ASIC carrier and the main board, where its main features are pointed out, is shown. The figure represents also a block diagram showing the instrumentation used to perform automated tests on the ADC. The ADC digital inputs, the `clock` and the `trigger` signals, are provided through a pattern generator (Tecktronix TLA7PG2) by means of a LVCMOS probe, which is able to provide digital signals at 1.2 V. The ADC input voltage can be generated by means of a 16-bit commercial DAC with high linearity performance mounted on the main board. The DAC used is the MAX541 by Maxim Integrated. With a reference voltage of 2 V, wich implies an LSB_{DAC} equal to $2/2^{16} \approx 30.5\mu V$, it guarantees a typical integral non linearity of 0.5 LSB_{DAC}, a typical differential non linearity of 0.5 LSB_{DAC}, and a monotonic input/output characteristic. The reference voltage for the MAX541 DAC is provided by a commercial voltage reference, MAX6126 by Maxim Integrated, which complies with the specifications set by the DAC. Indeed, it has a typical load regulation from 1 to 1.8 $\mu V/mA$, when the required one is less than 7 $\mu V/mA$ for a maximum error of 0.1 LSB.

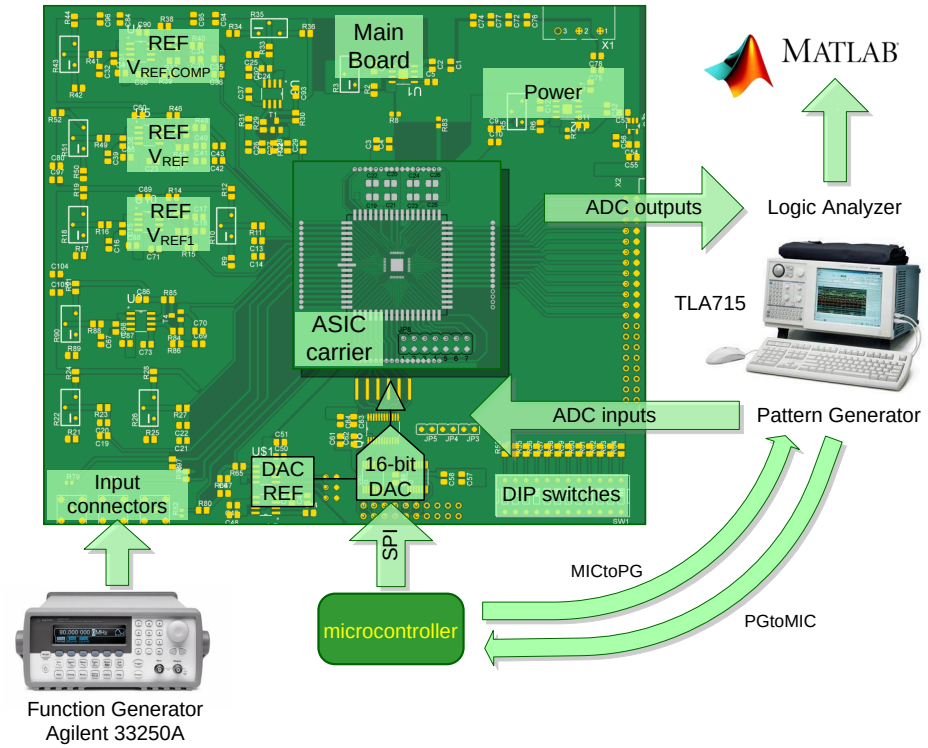


Figure 3.2: Measurement setup for ADC testing.

Morover the MAX6126 guarantees a very low output noise voltage equal to 1.45 μV_{pp}. In order to properly drive the capacitive load represented by the ADC under test, an external buffer (MAX4091) has been used after the DAC output.
The MAX541 DAC receives the digital inputs through SPI protocol. These digital signals are generated by means of a properly programmed microcontroller. The microcontroller, after having provided the digital inputs, forces a waiting time of around 26 μs to let the DAC output settle, and, driving an output bit at its high level (`MICtoPG` in Fig 3.2), tells the Pattern Generator that the conversion can start. The Pattern Generator is programmed in such a way to repeat a sequence of a `trigger` signal and 11 `clock` periods, necessary to perform a conversion, each time the `MICtoPG` bit from the microcontroller goes high. The Pattern Generator, in turn, generates another control bit `PGtoMIC`,

which goes high each time a conversion sequence ends. Hence the microcontroller is programmed to generate a new SPI chain, each time the control bit from the Pattern Generator goes high, to produce a new voltage input for the ADC. The use of both Pattern Generator and microcontroller is required by the need to read and/or provide digital signals with different logic levels to the ADC under test and to the external DAC: the first needs [0;1.2]V digital signals, available from the LVCMOS probe of the Pattern Generator, while the second requires [0;5]V levels, available from the microcontroller. This enables to avoid the use of level shifters, the presence of which was not foreseen in the main board.
Another way to provide the input voltage to the ADCs under test, is by disconnecting the ADC input from the MAX541 DAC in the main board and connecting it to an external function generator by means of one of the connectors placed in the periphery of the main board.
However the ADC input voltage is provided, the ADC digital output words are collected by the Logic Analyzer. The Logic Analyzer is programmed to sample the 10 ADC output bits at every rising edge of the `EoC` signal, which is the ADC signal going high at the end of a conversion.
The data collected by the Logic Analyzer are then post-processed by means of a MATLAB program.

3.3 Static measurements

In the first set of measurements performed on the ADCs, the input-output transfer characteristic is obtained and from it the static specifications of the converter can be extracted. These measurements are accomplished by feeding the sample to be converted to the ADCs through the MAX541 DAC programmed by the microcontroller. The DAC output has to cover the whole ADC dynamic input range from 0.2 V to 1 V. Hence the minimum DAC input digital word is 6500 (decimal), corresponding to a voltage of $6500 \cdot LSB_{DAC} \approx 198\ mV$, while the maximum DAC input digital word is 36000 (decimal), corresponding to a voltage of $36000 \cdot LSB_{DAC} \approx 1.098\ V$. The ADC dynamic input range was divided in such a way to have 4 points for ADC bin. This means that the input voltage step has to be around 195.3 μV, corresponding to a DAC digital input step of 6 (decimal). Hence the microcontroller is programmed to provide the input digital words to the DAC through the SPI protocol, starting from 6500 to 36000 with steps of 6 (all the values are in decimal code). For each input voltage (or DAC input word) the conversion on the ADC is repeated thirty times, in such a way to have 15 results from

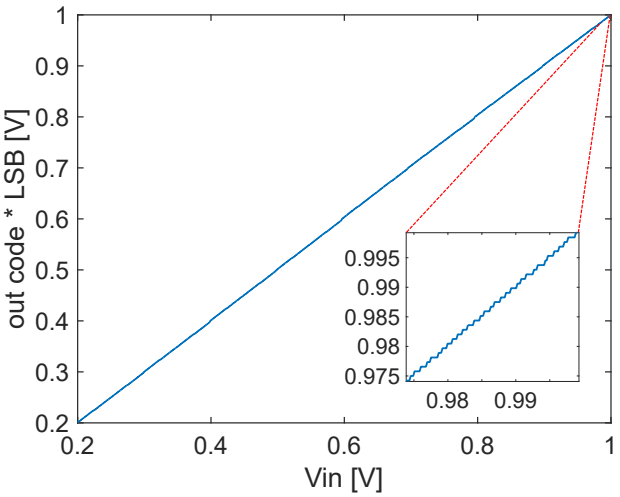


Figure 3.3: Example of a measured input-output characteristic, with an inset showing the single photon resolution part. Conversions were performed at a sampling period of 550 ns.

one half of the ADC interleaved structure and 15 results from the other half. The ADC output digital words resulting from the static measurements and collected by the Logic Analyzer are then post-processed by means of a MatLab program. The even digital words are separated from the odd ones, since the first ones come from the conversion performed on one of the two DACs of the interleaved ADC and the second ones result from the conversion on the other DAC. These measurements were repeated on 6 test chips.
Figure 3.3 shows an example of the input-output characteristic obtained from these measurements at a sampling period of 550 ns on one half of the ADC interleaved structure, where each point of the characteristic is the result of a mean of the 15 data acquired with that input voltage. The figure represents the results obtained from the ADC layout option without either a metal shield or the electronics beneath the DAC MIM capacitors. The inset shows a blow out of the final part of the characteristic, where the application for which the ADC has been designed requires single photon resolution: indeed, as it can be seen in Fig 1.17, the ADC input voltage, or the FCF output voltage, corresponding to 0 input photons is 1 V and the more photons are detected, the less the voltage is.
From these measurements the main ADC static parameters, listed below, can

be extrapolated.

- The offset between the results obtained from the two parts of the interleaved ADC architecture.
- The gain error, that is the deviation of the slope of the straight line interpolating the transfer curve from the ideal one.
- The non-linearity parameters.
  - The DNL (Differential Non-Linearity) is defined as the deviation of the measured step size in the transfer function from the ideal step equal to 1 LSB. If V_k is the input voltage corresponding to the transition point between successive codes $k-1$ and k, the width of the bin k is $\Delta(k) = V_{k+1} - V_k$ and the differential non-linearity, expressed in fraction of LSB, is defined as

    $$DNL(k) = \frac{\Delta(k) - LSB}{LSB}. \tag{3.1}$$

    DNL enables to verify the presence of missing codes, that are digital codes which are never generated at the ADC output, whatever the input voltage is. Indeed in the case of a missing code, the DNL is equal to -1.
  - The INL (Integral Non-Linearity) is defined as the deviation of the transfer function from the endpoint-fit line and is expressed in fractions of LSB.

The offset between the digital outputs measured from the two halves of the ADC interleaved structure is equal 9 LSB, averaging on all the collected data, with a standard deviation of 2.5 LSB. This is not classified as a critical problem for the application for which the ADC is designed, since the offset can be accounted for by suitably calibrating the channel response before starting the real experiment.
Instead, the gain error is found to be negligible in all the tested ADC.
In order to calculate the DNL as expressed in (3.1), the MatLab program used for data post-processing finds the transition points between successive codes. At the same time, in order to evaluate the INL, the MatLab program fits the input-output characteristic with a straight line and, for each point of the transfer function, calculates the deviation from it in terms of fractions of LSB. The results obtained from measurements on each of the ADC layout options for one of the six test chip, separately showing the two parts of the ADC interleaved

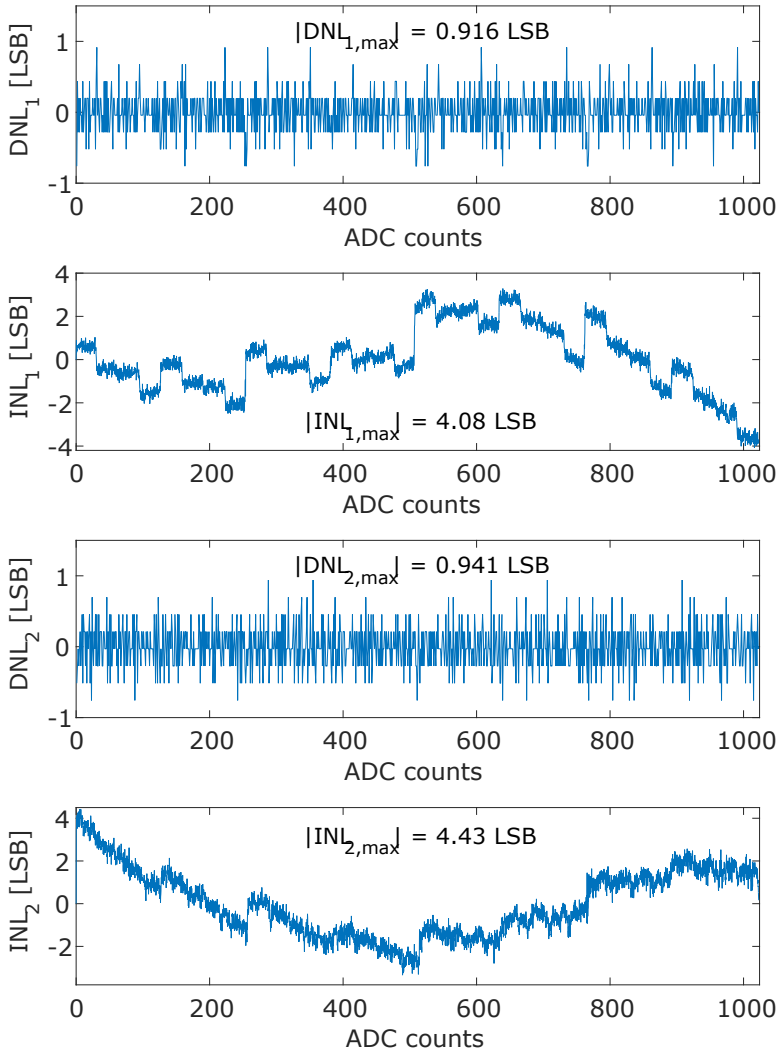


Figure 3.4: DNL and INL of the ADC without either metal shield or electronics beneath DAC MIM capacitors. (a) and (b) show the non-linearity results of one half of the ADC interleaved structure, (c) and (d) of the other half. The sampling period is 550 ns.

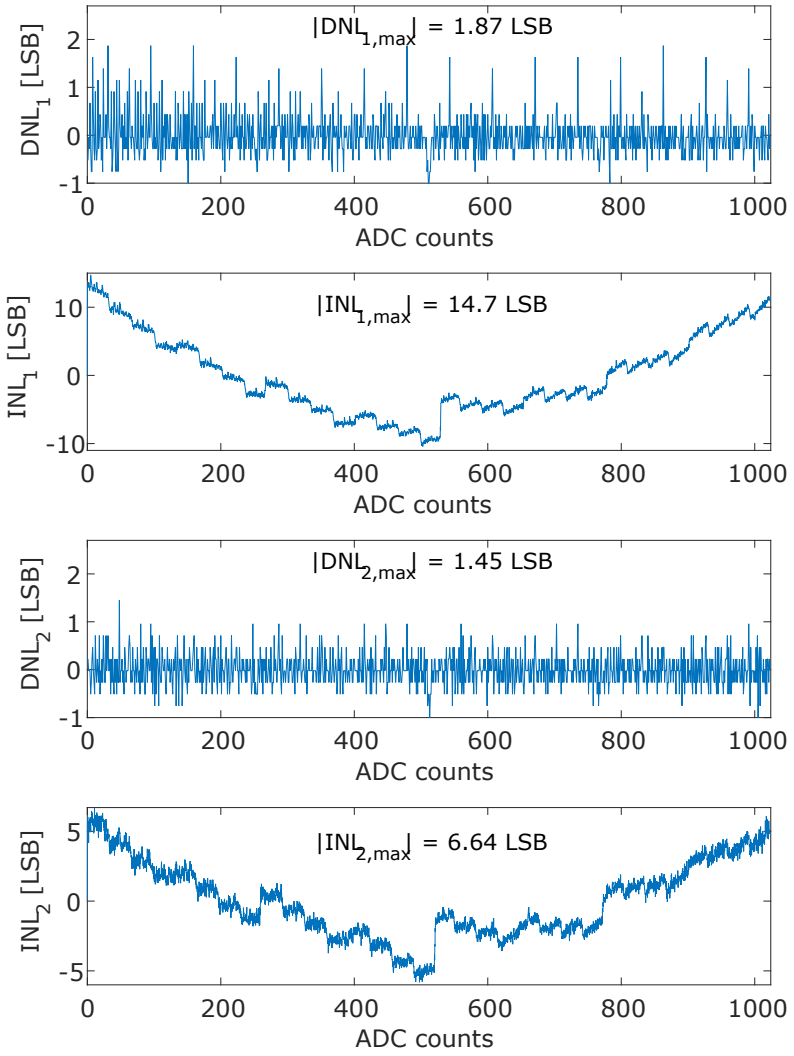


Figure 3.5: DNL and INL of the ADC with electronics, but not metal shield beneath DAC MIM capacitors. (a) and (b) show the non-linearity results of one half of the ADC interleaved structure, (c) and (d) of the other half. The sampling period is 550 ns.

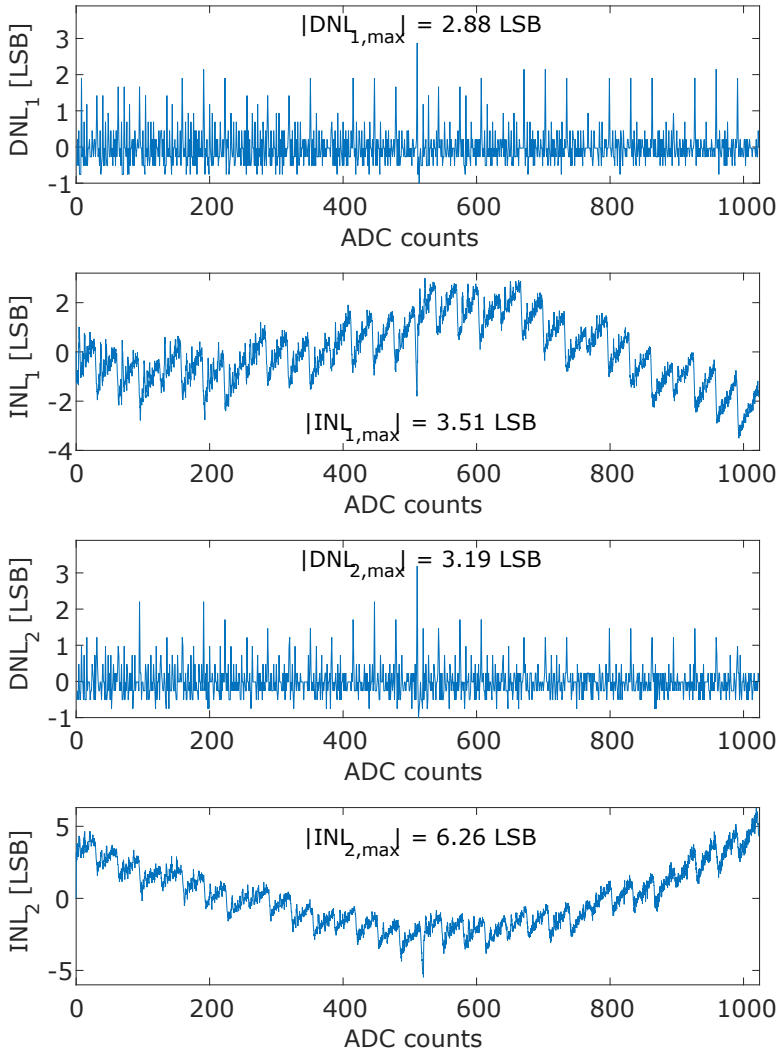


Figure 3.6: DNL of the ADC with both electronics and metal shield beneath DAC MIM capacitors. (a) and (b) show the non-linearity results of one half of the ADC interleaved structure, (c) and (d) of the other half. The sampling period is 550 ns.

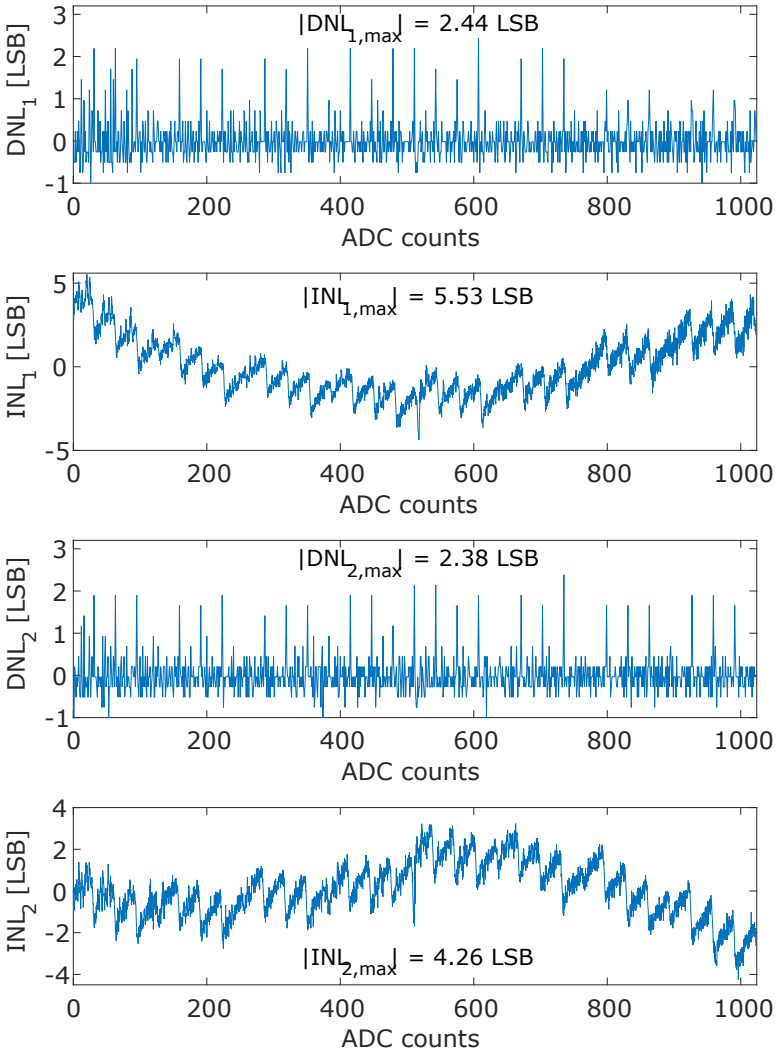


Figure 3.7: DNL and INL of the ADC with metal shield but not the electronics beneath DAC MIM capacitors. (a)and (b) shows the DNL results of one half of the ADC interleaved structure, (b) of the other half. The sampling period is 550 ns.

structure, are shown in Fig. 3.4, 3.5, 3.6, 3.7. The non-linearity parameters extracted from the data collected from the other five chips are in fair agreement with the ones shown above. As far as the DNL is concerned, different values are extracted from the different ADC layouts. The best performance in terms of differential non-linearity was found in the ADC with neither metal shield, nor electronics beneath the DAC MIM capacitors (DNL always smaller than 1 LSB and, hence, no missing codes). Then, considering the other layout options, it can be noticed that the more layers are placed beneath the DAC MIM capacitors and the closer they are to the MIM capacitor bottom plates, the worst the DNL performance are, as it could be expected because of the parasitic capacitance effects (see section 2.8). Indeed, from the ADC layout with part of the electronics beneath the MIM capacitors, but without metal shields, the maximum DNL is about one time and a half larger than the one with the best DNL performance, while for the ADC with only metal shields beneath the MIM capacitors, the maximum DNL is about two times and a half greater than it. Finally, the ADC with both metal shields and electronics beneath the MIM capacitors has a maximum DNL around three times larger than the ADC without any layer under the DACs capacitors.
On the contrary, the maximum INL of every ADC layout is greater than 1 LSB. Such a high value may degrade the ADC performance and results in increased harmonic distortion when the ADC is used for dynamic signal sampling and reconstruction. In applications like the one for which the ADC is designed and since the analog readout channel processing the signal before it has a strong non-linear behavior, the ADC INL can be accounted for by suitably calibrating the channel response at the beginning of the operation. Channel calibration, in general, will consist of reconstructing the input-output characteristic for each pixel. This can be achieved by measuring the response of each channel to an input charge pulse with varying but well known amplitude, as it is described in the literature, for example in [45]. In order to optimize the calibration procedure, the number of measurement points should be kept to the minimum required for correct input-output curve reconstruction. From this standpoint, the most critical part is represented by the transition region between the low and high gain portion of the gain curve.
The reason for the relatively high INL value could be found in the parasitic capacitances, which play an important role in split capacitor DAC architectures [46]. Actually, post-layout simulation results do not reveal such a high INL value. In simulation, the INL is always lower than 1 LSB, even if its maximum value approaches 1 LSB. This means that stray capacitance modeling in the foundry design kit is poor. Another INL source may lie in random mismatch

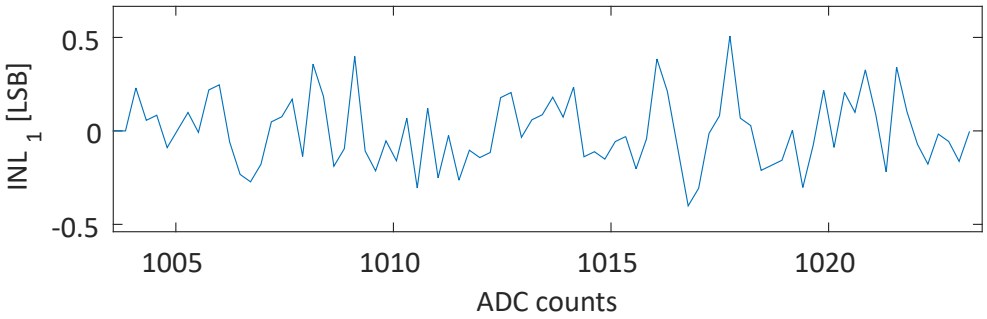


Figure 3.8: INL calculated on the last 20 bins of the characteristic, where single photon resolution is required.

between unit capacitors. Actually, a Monte Carlo simulation after parasitics extraction over the entire input-output characteristic of the ADC could never be performed, due to the very long simulation time.
However, if only the final part of the measured characteristic (the last 20 bin) is taken into consideration, the one where single photon resolution is required, there the INL is found to be smaller than 1 LSB, as shown in Fig. 3.8.

3.4 Equivalent input referred noise

Beside the static parameters, the electronic noise produced by the circuits of the ADC can be evaluated. In this case, the measurements performed on the ADCs are slightly different from the ones described in the previous section, even if the setup is the same. The microcontroller is programmed in such a way that the A-to-D conversion on the same input voltage generated by the MAX541 DAC is repeated 2000 times, 1000 conversions on each of the two ADC interleaved structures. After the 2000 conversions, the microcontroller increases the DAC input digital word by 1, in order to take advantage of the maximum MAX541 DAC resolution ($LSB_{DAC} \approx 30.5\mu V$). Fig. 3.9 shows an example of the results obtained from these measurement on one half of the ADC interleaved architecture, with a sampling period equal to 550 ns. In the figure, the ADC output codes collected by the Logic Analyzer are represented on the Y-axis, while the number of the sample being converted is on the X-axis. The transition from a code to the successive one is not sharp, due to noise. By processing the collected data by means of MatLab, the probability that the ADC output exceeds a certain code has been calculated [$P(ADC_{out} \geq k)$].

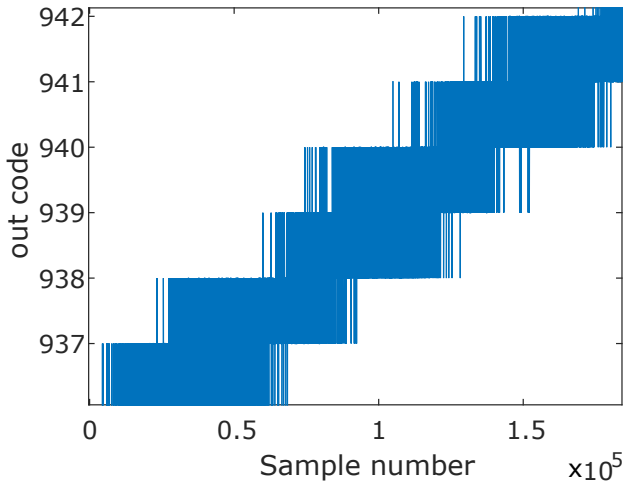
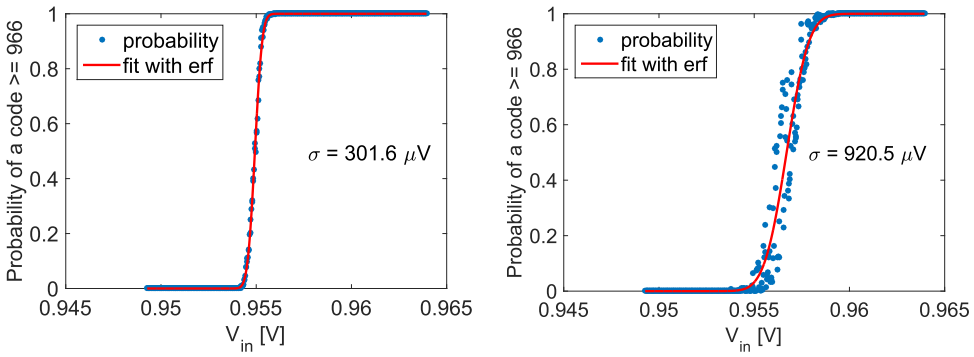


Figure 3.9: Example of the results obtained from input noise measurements: input voltage goes from 931.25 mV to 936.72 mV with step of 30.5 μV, each input voltage is converted 1000 times. The sampling period is 550 ns.

The results have been interpolated with the error function

$$P(ADC_{out} \geq k) = \frac{1}{2} + \frac{1}{2} \cdot erf\left(\frac{V_{in} - V_k}{\sqrt{2}\sigma}\right), \tag{3.2}$$

where V_k is the input voltage for which the transition from the output code k-1 to the code k takes place and σ defines the value of the ADC input referred noise. The results obtained from the interpolation of the data in the case of the ADC with neither metal shield nor electronics beneath the DAC MIM capacitors are shown in Fig. 3.10 (a) and (b), for each of the two parts of the ADC interleaved structure. Table 3.1 collects the values of the input noise obtained for each of the ADC layout options. Each reported value is the mean of 20 values of input referred noise calculated with the procedure described above, interpolating with 3.2 the probability that the ADC output exceeds 20 different codes in the last part of the input-output characteristic, where single photon resolution is required by the application. The standard deviation is reported together with the mean value. The table shows a significant difference between the two halves of the ADC interleaved architecture in terms of input noise. Since no information is available about which part of the interleaved structure is involved in the conversion, the smallest input referred



(a) **(b)**

Figure 3.10: Examples of interpolating the probability that the ADC output exceed a certain code with an error function. Figures (a) and (b) refer to the two parts of a time interleaved ADC with neither metal shield, nor electronics beneath DACs MIM capacitors.

	ADC (no metal shield, no electronics beneath MIM)	**ADC (electronics, but no shield beneath MIM)**	**ADC (electronics and shield beneath MIM)**	**ADC (metal shield, but no electronics beneath MIM)**
σ_1 $[\mu V]$	(313.9 ± 25.5)	(467.4 ± 31.1)	(305.1 ± 15.0)	(524.9 ± 53.1)
σ_2 $[\mu V]$	(950.1 ± 274.9)	(897.5 ± 167.4)	(611.2 ± 96.1)	(1300.0 ± 275.4)

Table 3.1: ADC input referred noise voltage (mean value and standard deviation) calculated as the σ of the error function interpolating the probability that the ADC output exceeds a given code. σ_1 refers to the data collected from one half of the ADC interleaved structure, σ_2 to the data of the other half.

noise between the two is indicated as σ_1 in the table, the other one is indicated as σ_2. The detected difference may be justified by an asymmetry in the ADC layout: indeed, beneath the MIM capacitors of one of the two DAC (DAC2 in Fig. 2.29), metal lines connecting the ADC outputs with the readout logic are placed. Coupling of that signals with the bottom plates of the DAC MIM capacitors mat be responsible for the noise degradation observed when one of the two DACs is used to sample the signal. For this reason the layout has been redesigned removing those lines from beneath the MIM capacitors and making the two DACs as symmetric as possible, in view of the next submission of the ADC. Moreover, comparing the input referred noise values indicated with σ_1 between the different ADC layout options, it can be noticed that the noise performance of the ADC with neither metal shields nor electronics beneath the DAC MIM capacitors is the best, together with the ADC with both electronics and metal shield under the MIM capacitor. In these cases the input noise is about 0.4 LSB. This means that the presence of the metal shield beneath the MIM capacitors is more damaging in terms of differential non-linearity than helpful in terms of noise.

The probability that a signal corresponding to 0 photons is misinterpreted as 1 photon ($P_{1|0}$) can be evaluated from the input noise previously calculated and equal to 0.4 LSB, which is the sigma of a Gaussian distribution, as shown in Fig. 3.11. Since the gain of the analog front-end in the single photon resolution region, in order to contain its input referred noise, is chosen in such a way that one photon count fits into two ADC bins in the single photon resolution region, the figure shows two x-axis: ADC bins and photon count. $P_{1|0}$ corresponds to the integral between 1 photon and 1.5 photons of the Gaussian curve centered in 0. $P_{1|0}$ is equal to 0.62%.

The noise at the ADC input can be referred to the input of the complete channel, in order to compare it with the ENC (Equivalent Noise Charge) of the analog front-end. The ADC contribution to the noise in terms of ENC is

$$ENC|_{ADC} = \frac{0.4\ LSB}{G_{ph,high}} \cdot \frac{1\ keV}{3.6\ eV} \approx 59\ e^{-}, \tag{3.3}$$

where 0.4 LSB is the noise referred to the ADC input, $G_{ph,high} = 1.5\ \frac{mV}{ph}$ is the gain of the analog front-end in the single photon resolution region for photons at 1 keV and 3.6 eV is the energy required to create an electron-hole pair in silicon. Fig. 3.12 shows a comparison between the measured ENC of the analog front-end and the measured ENC of the full channel, also including the ADC, as a function of the integration time τ of the shaper. As it can be seen, the main contribution to the noise comes from the analog front-end, in

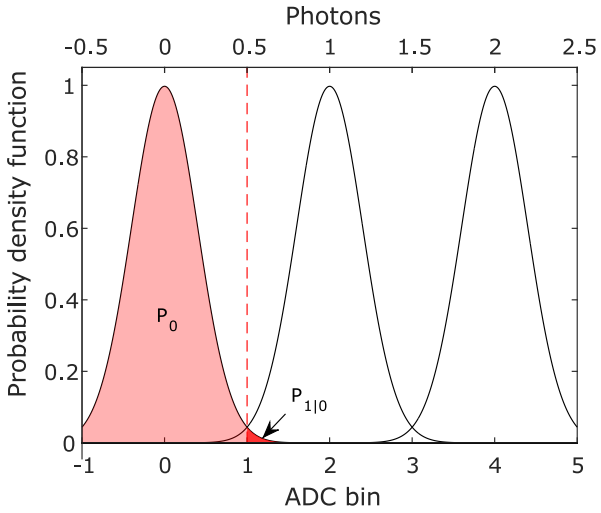


Figure 3.11: The ADC noise can be considered Gaussian. $P_{1|0}$ that a pixel erroneously detects one photon because of the electronics noise, even if no photon has been collected. $P_{1|0}$ is the integral of the Gaussian curve centered in zero between 0.5 and 1.5 photons.

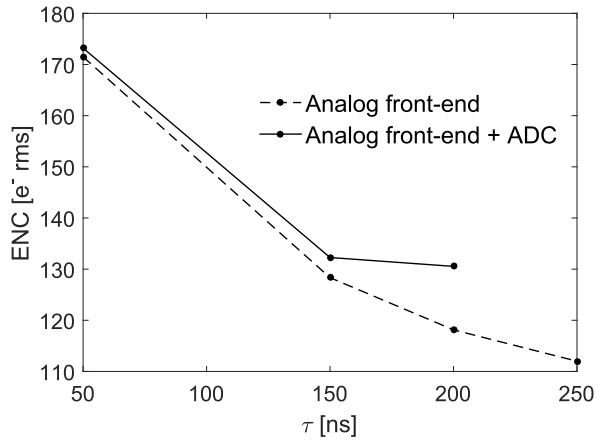


Figure 3.12: Comparison between the equivalent noise charge measured at the ADC output and the one measured at the shaper output as a function of the integration time τ.

particular at the target integration time of $\tau = 50\ ns$, compatible with operation at 4.5 MHz.

3.5 Dynamic measurement

Dynamic measurements have also been performed on the ADC under test. The test setup used for these measurements is different from the one used for the tests described in the previous sections. The ADC `clock` and `trigger` signals are still provided by the Pattern Generator and its outputs are still collected by the Logic Analyzer. Instead, the input voltage is no longer provided through the MAX451 DAC, but by means of a function generator through one of the connectors of the main board. In this way, a sinusoidal signal covering the whole ADC input dynamic range can be fed as an input to the ADC under test. With the data collected from these measurements, the SNDR (Signal to Noise and Distortion Ratio), and hence the ENOB (Equivalent Number of Bit), can be evaluated. The SNDR is calculated through MatLab as the ratio between the power of the signal and the power of the harmonic components plus noise

$$SNDR|_{db} = 10Log\left(\frac{P_{signal}}{P_{noise} + P_{distortion}}\right). \tag{3.4}$$

From the SNDR, the ENOB is calculated as

$$ENOB = \frac{SNDR|_{dB} - 1.76}{6.02}. \tag{3.5}$$

Fig. 3.13 shows an example of the power spectrum of the signal reconstructed from the output of the ADC with neither metal shield nor electronics beneath DAC MIM capacitors. The power spectrum, normalized to the maximum power, is obtained with an input sine wave covering the whole ADC input dynamic range at a frequency of around 4 kHz and with a sampling period of 550 ns. The figure also displays the calculated values of the SNDR and the ENOB. It also shows the presence of non negligible higher order harmonics, caused by the relatively high integral non-linearities. These higher order harmonics are also found for all the other ADC layout options, but, as mentioned before, this is not a problem for the application for which the ADC has been designed, since it is not used for dynamic signal sampling and reconstruction. If the higher order harmonics are removed from the spectrum, the resulting SNR (Signal to Noise Ratio) is in agreement with the one calculated from the

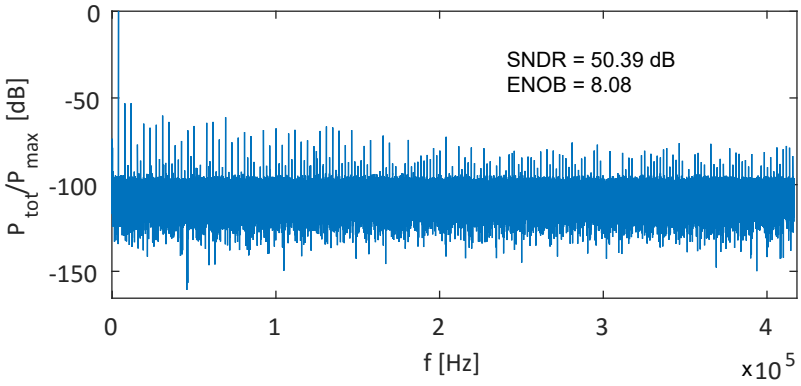


Figure 3.13: Example of the power spectrum of the signal reconstructed from the ADC output, obtained with an input 4 kHz sine wave and with a conversion period of 550 ns. The resulting SNDR and ENOB are also displayed.

input noise evaluated with the measurement described in section 3.4, as Table 3.2 shows. The SNR in this case is calculated as

$$SNR_{\sigma}|_{dB} = 10Log\frac{P_{sine}}{P_{noise}} = 10Log\frac{\frac{V_{REF}^2}{8}}{\frac{LSB^2}{12} + \sigma_{1,2}^2}, \tag{3.6}$$

where P_{sine} is the signal power and P_{noise} is the sum of the quantization noise power and the input referred noise power.

3.6 Summary of the measurements results and comparison with the state of the art

The measurement campaign on the different ADCs integrated in the test chip has brought to the choice of the ADC layout with neither metal shields nor electronics beneath the DAC MIM capacitors as the best solution. Indeed, this ADC layout option has the best performance in terms of differential non-linearity and noise: DNL always smaller than 1 LSB, no missing codes and input referred noise equal to 0.4 LSB. Even if it occupies a larger area than other layout solutions, it still fits the specified pixel pitch. A deterioration of the noise performance of one half of the ADC interleaved structure has been found, likely due to an asymmetry in the layout, redesigned to be more symmetric in view of the next submission. All the reported measurement results

		DAC1	DAC2
ADC (no metal shield, no electronics beneath MIM)	SNR_{sine} [dB]	55.81	53.19
	SNR_{σ} [dB]	57.29	49.24
ADC (no metal shield, no electronics beneath MIM)	SNR_{sine} [dB]	54.58	52.59
	SNR_{σ} [dB]	54.73	49.70
ADC (no metal shield, no electronics beneath MIM)	SNR_{sine} [dB]	56.78	53.28
	SNR_{σ} [dB]	57.45	52.75
ADC (no metal shield, no electronics beneath MIM)	SNR_{sine} [dB]	54.85	52.39
	SNR_{σ} [dB]	53.89	46.62

Table 3.2: SNR evaluated from measurement with a full range sinusoidal input (SNR_{sine}) and from the input referred noise calculated as explained in section 3.4 (SNR_{σ}). For each ADC layout, the results of both parts of the interleaved architecture (DAC1 and DAC2) are reported.

are obtained with a sampling period of 550 ns, higher than the target one for the Eu-XFEL of 220 ns, but short enough to be compliant with the LCLSII repetition period of 1 μs. Indeed, operation at sampling periods smaller than 550 ns deteriorate the ADC performance in terms of non-linearity and noise. For this reason the design of the comparator and especially its layout have been reviewed to improve its bandwidth for the next submission.
Considering the most promising ADC structure, to make a comparison with the state of the art, a Figure of Merit (FoM) has been evaluated as follows:

$$FoM = \frac{P_{tot}}{2^{ENOB} f_s}. \tag{3.7}$$

From measurement at the sampling frequency of $f_s = 1.82\ MHz$, the FoM has been found to be 172.82 $\frac{fJ}{conv\ step}$, since the dissipated power is $P_{tot} = 85\ \mu W$

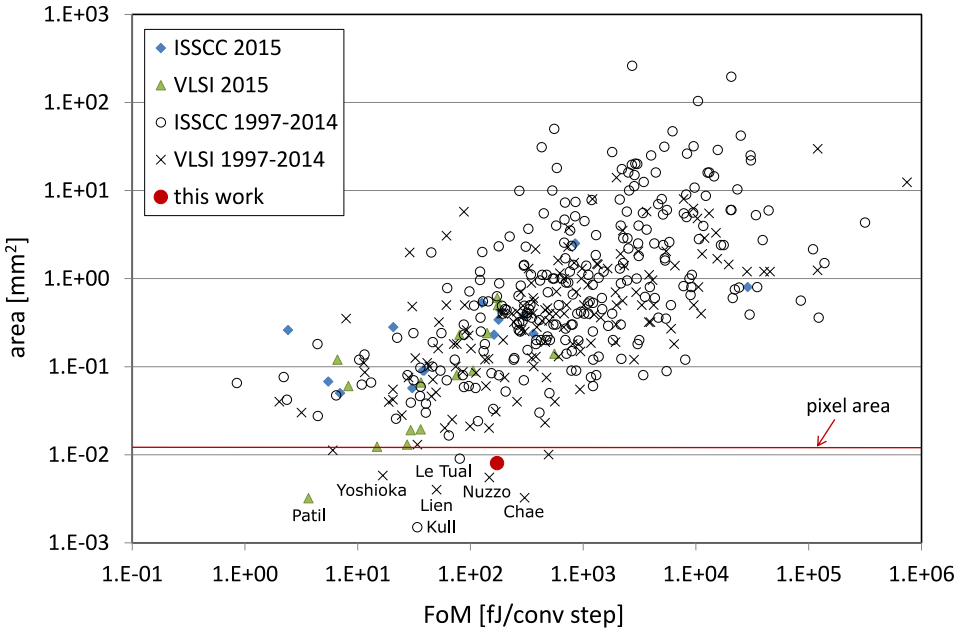


Figure 3.14: Comparison with the state of the art [47].

and the equivalent number of bits is $ENOB = 8.08$. In Fig. 3.14, the comparison with the state of the art [47] takes into account the FoM (power dissipation per conversion step) and the area occupation. Since the area is one of the main constraints for the ADC, a red line in Fig. 3.14 indicates the pixel area. In the figure can also be noticed the presence of ADCs with both smaller FoM and area than the ADC presented in this work. However they have a smaller ENOB, a smaller bandwidth or a higher power consumption. Table 3.3 shows a comparison between the performance of the ADC discussed in this thesis and the ones of Fig 3.14, with a smaller area than the pixel of the PixFEL front-end.

	architecture	**ENOB**	$f_{s,Nyq}$ **[MHz]**	**Power consumption** [μ**W**]	**Area** [μm^2]
this work	time-interleaved SAR ADC	8.08	1.82	85	8000
Patil [48]	error-shaping alias-free asynchronous ADC	6.86	80	24	3200
Yoshioka [49]	SAR ADC	7.06	24.6	54.6	5800
Kull [50]	asynchonous SAR ADC	6.24	1200	3060	1500
Lien [51]	asynchonous SAR ADC	6.91	750	4500	4000
Le Tual [52]	time-interleaved SAR ADC	5.32	10^4	32000	9000
Nuzzo [53]	SAR ADC	5.03	50	240	5500
Chae [54]	$\Sigma\Delta$ ADC	10.18	0.016	5.6	3240

Table 3.3: Performance summary and comparison with the ADCs of Fig 3.14 with an area smaller than the pixel of the PixFEL front-end. The parameter values are written in green or red depending on whether they satisfy or not the requirements for the PixFEL detector.

Conclusions

In this thesis work, the design and the characterization of a 10 bit analog to digital converter have been discussed. The ADC is part of the readout channel, developed in the framework of the PixFEL project, for a pixel detector to be used as an X-ray imager in experiments at FEL facilities. The converter is a SAR ADC, based on a charge redistribution architecture, implemented through a split capacitor DAC approach to reduce the circuit area. The discriminator includes a preamplification stage, also used to minimize kick-back noise effects, a second gain stage and a latch. The choice of a time-interleaved structure serves the purpose of speeding up the ADC operation, while avoiding large current peaks during the charging phase of the capacitive DAC. Four versions of the ADC layout have been designed for a test chip: with or without metal shields under the capacitive DAC and with or without electronics under the capacitive DAC. Depending on the adopted solution, the area of the converter can vary from $108 \times 74\ \mu m^2$ to $108 \times 58\ \mu m^2$, compatible with the target pitch of the pixel of 110 μm. Characterization of the ADC prototypes included in the test chips provided encouraging results. The static measurements showed that the parasitic capacitance introduced by the shield connected to ground or the electronics under capacitive DACs degrades the linearity performance. Therefore, the best layout solution chosen for the next submission to fabrication is the one without neither metal shield nor electronics beneath the DAC capacitors. The maximum DNL obtained from this structure is always smaller than 1 LSB, meaning that there are no missing codes, while the maximum INL is around 4.4 LSB, not a critical value for applications as the one considered here, since INL effects can be accounted by properly calibrating the channel response. The mean input noise for the most promising structure (without neither metal shield nor electronics under the capacitive DACs) turns out to be around 0.4 LSB. These results are obtained with the ADC operated at a clock frequency of 20 MHz, resulting in a sampling frequency of about 1.82 MHz, more than enough for experiments at some FEL facilities (e.g. LCLSII, SCSS, Fermi). Operation at the target

sampling frequency for the Eu-XFEL of 4.5 MHz are found to deteriorate the ADC performance in terms of non-linearity and noise. A slightly new design with a higher bandwidth comparator has been submitted to fabrication in order to improve the ADC performance at high frequency. The modifications introduced in the comparator design mainly affect the power consumption of the preamplification stage (increased from 35 μA to 50 μA) and its layout. In particular, more dummy transistors have been added in the periphery of the common centroid structure of the comparator current mirrors, in order to limit border effects. The new design includes also improvements in the symmetry of the interleaved structure layout. Actually, the test results underlined that one of the two parts of the interleaved ADC has worse performances in terms of noise than the other one. This is likely due to the coupling with the metal lines which are placed beneath one of the two capacitive DACs. Beside this, an output bit containing the information about which part of the ADC interleaved structure is involved in the conversion has been added in the new ADC version, together with the possibility to make the ADC work in a non-interleaved mode, in order to facilitate the debug. The improved ADC design has been integrated, together with the whole readout channel, in a 32×32 matrix suitable to be bump bonded to a sensor matrix.

Bibliography

[1] https://lcls.slac.stanford.edu/

[2] http://www.spring8.or.jp

[3] http://www.xfel.eu/

[4] https://www.psi.ch/swissfel/

[5] https://portal.slac.stanford.edu/sites/lcls_public/lcls_ii/Pages/default.aspx

[6] M. Ferrario et al., "IRIDE: Interdisciplinary research infrastructure based on dual electron linacs and lasers", Nucl. Instrum. Methods A, volume 740, 11 March 2014, Pages 138-146. [Online] http://dx.doi.org/10.1016/j.nima.2013.11.040

[7] G. R. Neil and L. Merminga, "Technical approaches for high-average-power free-electron lasers", Review of Modern Phisics, volume 74, July 2002, Pages 685-701. [Online] http://dx.doi.org/10.1103/RevModPhys.74.685

[8] LCLS-II, "LCLS-II new instruments workshops report." [Online] http://slac.stanford.edu/pubs/slacreports/reports19/slac-r-993.pdf.

[9] SwissFEL, "Ultrafast phenomena at the nanoscale: Science opportunities at the SwissFEL X-ray laser." [Online] http://www.psi.ch/swissfel/CurrentSwissFELPublicationsEN/SwissFELScienceCasesmall.pdf.

[10] European XFEL, "Research possibilities". [Online] https://www.xfel.eu/research/possibilities.

[11] B. D. Patterson and R. Abela, "Novel opportunities for time-resolved absorption spectroscopy at the X-ray free electron laser", Physical Chemistry Chemical Physics, issue 12, 2010, Pages 5647-5652. [Online] http://dx.doi.org/10.1039/C003406A

[12] H. N. Chapman, S. Bajt, A. Barty, W.H. Benner et al., "Ultrafast coherent diffraction imaging with X-ray Free-Electron Lasers", Proceedings of FEL 2006, BESSY, Berlin, Germany, 2006.

[13] H. Graafsma, "Requirements for and development of 2 dimensional X-ray detectors for the European X-ray Free Electron Laser in Hamburg," Journal of Instrumentation, volume 4, December 2009. [Online] http://dx.doi.org/10.1088/1748-0221/4/12/P12011

[14] B. Henrich, J. Becker, R. Dinapoli, P. Goettlicher, H. Graafsma et al., "The adaptive gain integrating pixel detector AGIPD a detector for the European XFEL", Nucl. Instrum. Methods A, volume 633, supplement 1, May 2011, pag. S11-S14. [Online] http://dx.doi.org/10.1016/j.nima.2010.06.107

[15] M. Hart, C. Angelsen, S. Burge, J. Coughlan et al. "Development of the LPD, a High Dynamic Range Pixel Detector for the European XFEL", Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), 2012 IEEE, Anaheim, California, October 29 - November 3 2012. [Online] http://dx.doi.org/10.1109/NSSMIC.2012.6551165

[16] M. Porro, L. Andricek, S. Aschauer, M. Bayer et al., "Development of the DEPFET Sensor With Signal Compression: A Large Format X-Ray Imager With Mega-Frame Readout Capability for the European XFEL", IEEE Transactions on Nuclear Science, volume 59, issue 6, December 2012. [Online] http://dx.doi.org/10.1109/TNS.2012.2217755

[17] C. B. Wunderera, A. Marrasa, M. Bayera, L. Glasera et al., "The PERCIVAL soft X-ray imager", Journal of Instrumentation, volume 9, March 2014. [Online] http://dx.doi.org/10.1088/1748-0221/9/03/C03056

[18] A. Dragone, J.F. Pratte, P. Rehak, G. A. Carini et al., "XAMPS Detector Readout ASIC for LCLS", Nuclear Science Symposium Conference Record, 2008. NSS '08 IEEE, 19-25 October 2008. [Online] http://dx.doi.org/10.1109/NSSMIC.2008.4774986

[19] T. Hatsui, M. Omodani, T. Kudo, K. Kobayashi et al., "A direct-detection X-ray CMOS image sensor with 500 μm thick high resistivity silicon",

Proceedings of the International Image Sensor Workshop (IISW), 1216 June 2013, Snowbird, Utah, USA.

[20] C. R. Grace, J.-P. Walder, P. Denes, H. von der Lippe, "Multiplexed Oversampling Digitizer in 65 nm CMOS for Column-Parallel CCD Readout", IEEE Transactions on Nuclear Science, volume 60, issue 1, February 2013. [Online] `http://dx.doi.org/10.1109/TNS.2012.2226604`

[21] `http://www.tezzaron.com/`

[22] T. Tick, M. Campbell, "TSV processing of Medipix3 wafers by CEA-LETI: a progress report", Journal of Instrumentation, volume 6, November 2011. [Online] `http://dx.doi.org/10.1088/1748-0221/6/11/C11018`

[23] `http://www.t-microtec.com/category/1426259.html`

[24] `http://www.sintef.no/`

[25] `http://www.vttresearch.com/`

[26] `http://www.fbk.eu/`

[27] J. Becker, D. Eckstein, R. Klanner, G. Steinbrck, "Impact of plasma effects on the performance of silicon sensors at an X-ray FEL", Nucl. Instr. Methods A, Volume 615, Issue 2, 1 April 2010, Pages 230-236. [Online] `http://dx.doi.org/10.1016/j.nima.2010.01.082`

[28] Joern Schwandt, Eckhart Fretwurst, Robert Klanner, Ioannis Kopsalis, Jiaguo Zhang, "Design and First Tests of a Radiation-Hard Pixel Sensor for the European X-Ray Free-Electron Laser", Radiation and Its Effects on Components and Systems (RADECS), 2013 14th European Conference on, 23-27 Sept. 2013, Oxford, UK. [Online] `http://dx.doi.org/10.1109/RADECS.2013.6937446`

[29] L. Pancheri, M. E. A. Benkechcache, G.-F. Dalla Betta, H. Xu et al., "First experimental results on active-edge silicon sensors for XFEL", International Workshops on Radiation Imaging Detectors (iWoRiD), 2016 18th Conference on, 3-7 July 2016, Barcellona, Spain.

[30] L. Bombelli, C. Fiorini, S. Facchinetti, M. Porro, G. De Vita, "A fast current readout strategy for the XFEL DePFET detector", Nucl. Instr. Methods A, Volume 624, Issue 2, 11 December 2010, Pages 360-366. [Online] `http://dx.doi.org/10.1016/j.nima.2010.03.123`

[31] M. Porro, L. Andricek, L. Bombelli, G. De Vita et al., "Expected performance of the DEPFET sensor with signal compression: A large format X-ray imager with mega-frame readout capability for the European XFEL", Nucl. Instr. Methods A, Volume 624, Issue 2, 11 December 2010, Pages 509-519. [Online] http://dx.doi.org/10.1016/j.nima.2010.02.254

[32] M. Manghisoni, D. Comotti, L. Gaioni, L. Ratti, Valerio Re, "Dynamic Compression of the Signal in a Charge Sensitive Amplifier: From Concept to Design", IEEE Transactions on Nuclear Science, Volume 62, Issue 5, October 2015, Pages 2318-2326. [Online] http://dx.doi.org/10.1109/TNS.2015.2477461

[33] M. Manghisoni, D. Comotti, L. Gaioni, L. Lodola et al., "Novel active signal compression in low-noise analog readout at future X-ray FEL facilities", Journal of Instrumentation, Volume 10, April 2015. [Online] http://dx.doi.org/10.1088/1748-0221/10/04/C04003

[34] D. Comotti, "High density microelectronic system for an intelligent readout of semiconductor pixel sensors", University of Pavia, academic year 2014/2015, Ph.D. paper.

[35] James R. Janesick, "Photon transfer", SPIE, 2007.

[36] J. Fredenburg and M. P. Flynn, "ADC Trends and Impact on SAR ADC Architecture and Analysis", Custom Integrated Circuits Conference (CICC), 28-30 September 2015, San Jose, California, USA. [Online] http://dx.doi.org/10.1109/CICC.2015.7338380

[37] B. Razavi, "Design Considerations for Interleaved ADCs", IEEE Journal of Solid-State Circuits, Volume 48, Issue 8, August 2013, Pages 1806-1817. [Online] http://dx.doi.org/10.1109/JSSC.2013.2258814

[38] Y. Chen, X. Zhu, H. Tamura, M. Kibune et al., "Split capacitor DAC mismatch calibration in successive approximation ADC", Custom Integrated Circuits Conference (CICC), 13-16 September 2009, San Jose, California, USA. [Online] http://dx.doi.org/10.1109/CICC.2009.5280859

[39] S. Haenzsche, S. Henker, R. Schffny, "Modelling of capacitor mismatch and non-linearity effects in charge redistribution SAR ADCs", Mixed Design of Integrated Circuits and Systems (MIXDES), 24-26 June 2010, Wroclaw, Poland. [Online] http://ieeexplore.ieee.org/document/5551648/

[40] R. J. Baker, "CMOS Circuit Design, Layout, and Simulation", IEEE Press Series on Microelectronic Systems.

[41] Y. Zhu, C. Chan, U. Chio, S. Sin, et al., "Parasitics nonlinearity cancellation technique for split DAC architecture by using capacitive charge-pump", Circuits and Systems (MWSCAS), 2010 53rd IEEE International Midwest Symposium on, 1-4 August 2010, Seattle, Washington, USA. [Online] http://dx.doi.org/10.1109/MWSCAS.2010.5548657

[42] M. Dessouky, A. Kaiser, "Input switch configuration suitable for rail-to-rail operation of switched op amp circuits", Electronics Letters, Volume 35, Issue 1, 7 January 1999. [Online] http://dx.doi.org/10.1049/el:19990028

[43] P.M. Figueiredo, J.C. Vital, "Kickback noise reduction techniques for CMOS latched comparators", IEEE Transactions on Circuits and Systems II, Volume 53, Issue 7, July 2006. [Online] http://dx.doi.org/10.1109/TCSII.2006.875308

[44] F. Maloberti, "Analog design for CMOS VLSI sysitems", Kluwer Academic Publishers, 2003.

[45] E. Quartieri and M. Manghisoni, "High precision injection circuit for in-pixel calibration of a large sensor matrix", Ph.D. Research in Microelectronics and Electronics (PRIME), 3-7 July 2011, Madonna di Campiglio, Trento, Italy. [Online] https://doi.org/10.1109/PRIME.2011.5966220

[46] Y. Zhu, U. Chio, H. Wei, S. Sin et al., "A power-efficient capacitor structure for high-speed charge recycling SAR ADCs", IEEE International Conference on Electronics, Circuits and Systems (ICECS), 31 August-3 September 2008, Malta. [Online] https://doi.org/10.1109/ICECS.2008.4674935

[47] B. Murmann, "ADC Performance Survey 1997-2015". [Online] http://web.stanford.edu/~murmann/adcsurvey.html

[48] S.harvil Patil, A. Ratiu, D. Morche, Y. Tsividis, "A 3-10 fJ/conv-step 0.0032 mm^2 error-shaping alias-free asynchronous ADC", Symposium on VLSI Circuits (VLSI Circuits), 17-19 June 2015, Honolulu, Hawaii. [Online] https://doi.org/10.1109/VLSIC.2015.7231249

[49] K. Yoshioka, A. Shikata, R. Sekimoto, T. Kuroda, and H. Ishikuro, "A 0.0058 mm^2 7.0 ENOB 24 MS/s 17 fJ/conv. threshold configuring SAR

ADC with source voltage shifting and interpolation technique", Symposium on VLSI Circuits (VLSI Circuits), 12-14 June 2013, Honolulu, Hawaii. [Online] http://ieeexplore.ieee.org/document/6578689/

[50] L. Kull, T. Toifl, M. Schmatz, P. A. Francese et al., "A 3.1 mW 8b 1.2 GS/s single-channel asynchronous SAR ADC with alternate comparators for enhanced speed in 32 nm digital SOI CMOS", Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 17-21 February 2013, San Francisco, CA, USA. [Online] https://doi.org/10.1109/ISSCC.2013.6487818

[51] Y.-C. Lien, "A 4.5-mW 8-b 750-MS/s 2-b/step asynchronous subranged SAR ADC in 28-nm CMOS technology", Symposium on VLSI Circuits (VLSI Circuits), 13-15 June 2012, Honolulu, Hawaii. [Online] https://doi.org/10.1109/VLSIC.2012.6243803

[52] S. Le Tual, P. N. Singh, C. Curis, P. Dautriche, " A 20 GHz-BW 6b 10 GS/s 32 mW time-interleaved SAR ADC with master T&H in 28 nm UTBB FDSOI technology", Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 9-13 Feb. 2014, San Francisco, CA, USA. [Online] https://doi.org/10.1109/ISSCC.2014.6757479

[53] P. Nuzzo, C. Nani, C. Armiento, A. Sangiovanni-Vincentelli, "A 6-Bit 50-MS/s threshold configuring SAR ADC in 90-nm digital CMOS", Symposium on VLSI Circuits (VLSI Circuits), 16-18 June 2009, Honolulu, Hawaii. [Online] http://ieeexplore.ieee.org/document/5205344/

[54] Y. Chae and G. Han, "A low power sigma-delta modulator using class-C inverter", Symposium on VLSI Circuits (VLSI Circuits), 14-16 June 2007, Honolulu, Hawaii. [Online] https://doi.org/10.1109/VLSIC.2007.4342734