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Design and Analysis of 2.4 GHz 30 µW CMOS LNAs for Wearable WSN Applications

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***Abstract*— To meet the requirements of wearable wireless sensor networks (W-WSN), the power dissipation of the RF transceiver has to be drastically reduced. This paper presents two ultra-low power Low Noise Amplifiers (LNAs) with RF performance exceeding the requirement of the intended application. In the first LNA, by reusing the current several times and employing passive gm boosting, the LNA input impedance is reduced by a factor of 24 compared to a single transistor using the same current. The feasibility of passive gm boosting for designing an ultra-low supply voltage LNA is also investigated. Limitations of both LNAs including NF, non-linearity and stability in a 40 nm CMOS technology are also investigated. The proposed LNAs consume only 30 µW of power, operate with 0.8 V and 0.18 V and show NF of 3.3 dB and 5.2 dB respectively. Using a widely accepted Figure-of-Merit for LNAs, the proposed circuit is almost three times better than the best previously reported sub-mW LNA.**

Keywords*— *ultra low power, low noise figure, current reuse, gm-boosting, ultra-low voltage, WSN.

I. Introduction

THE increasing demand for Wireless Sensor Networks (WSN) has recently motivated extensive research efforts on ultra-low power (ULP) transceivers. For WSNs it is especially critical to reduce receiver power dissipation since the sensor is mostly operating in the receive mode rather than in transmit mode. Moreover, some ULP applications, such as wireless medical telemetry and Wearable-WSN (W-WSN), require the portable devices to operate from a single Lithium Ion battery or to use energy harvested from the environment, calling for ultra-low voltage (ULV) designs. The use of a drastically reduced supply voltage makes designing ULP receivers even more challenging. It prevents stacking of devices, limiting the achievable reverse isolation and the maximum available gain in amplifiers.

Several low-power design techniques have been proposed to minimize the receiver power dissipation. The use of a low supply voltage (e.g. 300 mV in [1] and 180 mV in [2]) and the reuse of the same current in more than one block (e.g. [4,5,6]) are commonly adopted. The Bluetooth Low-Energy (BT-LE) receiver in [2] consumes as little as 382 µW. However, due to the extremely limited headroom, two stage inductive load LNA was used, leading to large chip area (1.65 mm^2). To reduce power and area, a mixer-first approach can be utilized. However, by removing the LNA, the noise contribution of the transimpedance amplifier (TIA) that typically follows the mixer increases due to the significantly reduced TIA driving impedance. As a result, a much larger power has to be consumed in the TIA, leading to larger overall power dissipation [3]. Stacking several circuit blocks that perform different functions on top of each other [4-6] poses several isolation issues that adversely affect the overall performance and prevent true ULP operation. For this reason, an ULP LNA that adopts current-reuse within the same block is proposed.

When the receiver noise requirements are relaxed, the main constraint on the LNA current consumption comes from the device g_m. This is due to the need to ensure impedance matching to the 50 Ω source and sufficient gain to make the noise contribution of the following stages negligible. In [6] the LNA, which performs also quadrature signal splitting, has a NF of 15.8 dB but still draws 530 µA. In [7] an ULP common-gate (CG) LNA operating at 2.4 GHz with a power consumption of only 30 µW was presented. The LNA operates from a 0.8 V supply voltage and, by reusing the current several times and employing transformer-based g_m boosting, it reduces the LNA input impedance by a factor of 24 compared to a single CG transistor using the same current. In this work an extended analysis of the LNA in [7] is presented, including transformer optimization, stability and linearity analyses and process and supply-voltage sensitivity analyses. Moreover, the design is compared with an ULV LNA based on the same transformer-based g_m boosting technique, operating from a 0.18 V supply and consuming only 30 µW. The comparison highlights the differences between a current-reuse design with a higher supply voltage and a ULV design with the same power dissipation. In section II, system overview of intended wireless standard is introduced. Fundamental limitations of popular LNA topologies and surveying recently published ULP LNAs are presented in section III. Analysis and design of the proposed LNAs are given in section IV. Simulation results and conclusion are provided in section V and VI respectively.

II. System Overview

The main communication standards for short range and low power applications are IEEE 802.15.4, IEEE 802.15.6, and Bluetooth Low Energy (BLE). Among them, BLE is dedicated to ultra-low power consumption systems and targets

applications for small and low-cost devices powered by small batteries, such as wireless sensors [8-9]. BLE operates in the 2.4 GHz ISM band ranges between 2400 to 2483.5 MHz and 40 channels with 1MHz bandwidth are spaced within 2 MHz [8]. BLE uses frequency hopping and GFSK modulation operating at symbol rate of 1 Msps and its modulation index is 0.5. It has data rate of 1 Mbit/s with an average throughput of 270 kbit/s. The main requirements of the BLE receiver are summarized in Table I [10]. The required 20 dB NF was determined based on the following considerations. For the optimum modulation scheme, the minimum SNR is 12 dB [10]. A 10 dB margin above the basic sensitivity level of -70 dBm is typically targeted to account for implementation non-idealities and 2 dB insertion loss (IL) is associated to the SAW filter placed in front of the receiver. As a result, the noise floor equals -94 dBm [11-12]. For the IIP3 requirement the standard specifies that the input signal should be 6 dB above the sensitivity level, i.e. -74 dBm. The third order intermodulation power (IM3) together with the integrated receiver input noise floor of -94 dBm, can be at most 6 dB above the noise floor, i.e. -88 dBm. Hence the maximum IM3 is -89.2 dBm. The largest in-band interferers have a minimum offset frequency from the desired channel of 3 MHz and have a power level of -50 dBm. As a result, an antenna-referred IIP3 requirement of -30.4 dBm is derived, corresponding to -32.4 dBm IIP3 for the receiver, considering the 2 dB IL of the SAW. Out-of-band interferers are larger than in-band interferers, up to -30 dBm, but are strongly attenuated by the input SAW filter and therefore are less of a concern. In the same way, a very relaxed receiver IIP2 requirement of -12.7 dBm can be derived.

According to the aforementioned discussion, BLE standards have very relaxed requirements in terms of noise, linearity and image rejection. In WSN applications, it is extremely important to take advantage of the relaxed specifications to reduce the receiver power dissipation. The LNA is generally considered as one of the most power hungry and challenging blocks and typically dominates both the NF and the out-of-band (OOB) IIP3. The most popular LNA topologies (e.g. inductive-degeneration, shunt-feedback, noise-canceling, etc.) were developed with the main goal of lowering the added noise. For WSN applications, instead, the main goal is to lower power dissipation. Hence, the noise-vs-power trade-off should be exploited to lower the power rather than to improve noise.

In the next section we will review the main LNA topologies that have been proposed to achieve this goal.

III. Review of Ultra-Low Power LNAs

Biasing transistors in the weak inversion region, where the maximum g_m/I_d can be achieved, is one of the most effective approaches to minimize the dissipated power in analog circuits [13]. However, weakly inverted transistors present very poor frequency response and, as a result, they cannot be widely used in RF circuit design. To optimize the ULP RF circuits, a figure of merit (FoM_{RF}), $g_m f_t/I_d$, was defined [13]. Maximizing FoM_{RF} corresponds to the maximization of the gain-bandwidth-product (GBW) represented by the $g_m f_t$ product for a given bias current. Maximum FoM_{RF} is achieved by biasing the transistors in moderate inversion region, which gives suitable compromise between current efficiency, i.e. g_m/I_d, and bandwidth (i.e. f_t). In this section, the fundamental limitations of popular Common Source (CS) and Common Gate (CG) LNA topologies for low power operation will be discussed. Then, the state-of-the-art LNA topologies for ULP will be investigated. In all topologies the noise contribution of the load will be neglected in order to emphasize the noise-power trade-off of the input devices.

Table. I. Summary of BLE Receiver Requirement

RX Sensitivity	-80 dBm
NF	20 dB
Maximum input power	-10 dBm
Adjacent interference, $C/I_{@\ 1,\ 2,\ >3\ MHz}$	15, -17, -27 dB
Image frequency interference, C/I_{Image}	-9 dB
Phase Noise @2.5 MHz	-102.5 dBc/Hz
IIP3	-30.4 dBm
IIP2	-12.7 dBm
Minimum Image rejection	26 dB

A. Resistively-terminated CS

The resistively-terminated CS amplifier shown in Fig. 1.a is the simplest configuration that allows to fulfill the input matching condition independently from the device transconductance. This allows to achieve impedance matching while dissipating very low power. However, other key RF metrics are seriously degraded. The noise factor (F) of this LNA is given by:

$$F \geq 2 + \frac{4\gamma}{g_m R_s} \quad (1)$$

where γ is the transistor thermal noise coefficient. To achieve a NF below 6 dB, the device g_m needs to be greater than 25 mS. The transconductance gain of the amplifier is simply given by the device g_m, hence if g_m is lower than 20 mS the LNA output current is lower than the input current and the LNA acts as a signal attenuator. Hence, lowering the bias current also leads to low gain and high noise from the following stages.

B. Shunt feedback CS

Shunt feedback CS amplifier is another popular topology and it can be relatively wideband (Fig. 1(b)). The noise factor (F), input impedance (Z_{in}) and the voltage gain (A_v) of the shunt

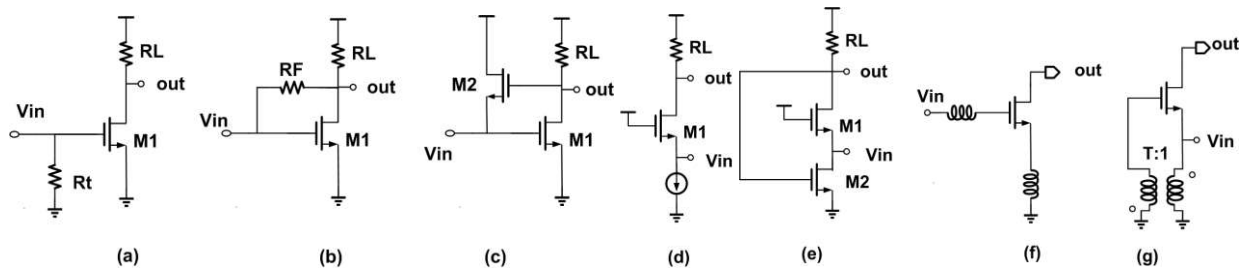


Fig. 1. Basic LNA topologies: (a) resistively-terminated CS; (b) shunt feedback CS; (c) active shunt feedback CS; (d) common-gate; (e) active shunt feedback CG; (f) inductive degeneration LNA; (g) transformer-based CG LNA (gate boosting for T>1).

feedback CS can be computed as follows:

$$F \geq 1 + \frac{\gamma}{g_m R_s} \tag{2}$$

$$Z_{in} = \frac{R_F + R_L}{1 + g_{m1} R_L} \tag{3}$$

$$A_V = \frac{g_{m1} + 1/R_F}{1/R_L + 1/R_F} \tag{4}$$

According to (2), to attain a NF lower than 6 dB, the device g_m only requires to be greater than 5 mS, which corresponds to a current of approximately 300 µA in moderate inversion. To perform the input impedance matching, however, the device g_m cannot be less than 20 mS, as given by (3) for $R_L >> R_F$. Hence, with this topology, the consumed power is limited by input matching more than by the noise or gain constraints.

C. Active shunt feedback CS

In contrast to the resistive shunt feedback, active feedback can be utilized to perform input matching while minimizing power consumption (see Fig. 1(c)). A buffer is placed around a CS amplifier to provide shunt feedback without loading the CS amplifier output, as shown in Fig.1(c). The input impedance of the amplifier can be computed as follows:

$$Z_{in} = \frac{1}{g_{m2}(1 + g_{m1} R_L)} \tag{5}$$

Both devices g_m can be easily less than 5 mS to provide input power matching (assuming resistive load of 1 kΩ), thus there is no significant power constrain from the input impedance matching condition. The NF of amplifier is given by:

$$F \geq 1 + \gamma . g_{m2} R_s + \frac{\gamma (1 + g_{m2} R_s)^2}{g_{m1} R_s} \tag{6}$$

It can be seen from (6) that, as the device g_m is reduced, the NF quickly degrades. To achieve a NF < 6 dB, $g_{m1} > 8$ mS and $g_{m2} > 1$ mS are required. This is better than with the resistive shunt feedback but still not quite ULP. In fact, the current of the core amplifier (M1) is constrained by noise considerations.

D. Common-Gate

The common-gate (CG) topology is well-known for its inherent wide bandwidth. In its basic configuration, as reported in Fig. 1(d), the input device g_m is limited by input power matching constrain ($Z_{in}=1/g_m$) and needs to be 20 mS, similar to that of resistive shunt feedback CS amplifier.

E. Active shunt feedback CG

One of the effective methods to reduce the required device g_m for input matching constrain is to employ active shunt feedback in CG amplifier [15]. As shown in Fig. 1(e), the circuit utilize the CG transistor (M1) as the core amplifier, with shunt feedback provided by a CS transistor (M2). The input impedance of the amplifier is given by:

$$Z_{in} = \frac{1}{g_{m1}(1 + g_{m2} R_L)} \tag{7}$$

According to (7), the feedback network boosts the effective g_m by loop gain, which facilitates good input matching with much less bias current. The required device g_m for CG is 20 mS divided by the loop gain ($g_{m2}R_L$). So it is reasonable to choose both device g_m to be less than 4 mS (assuming resistive load of 1 kΩ) to perform input matching, which allows to minimize power dissipation. The voltage gain and the noise factor are:

$$A_V = \frac{g_{m1} R_L}{R_S g_{m1}(1 + g_{m2} R_L) + 1} \tag{8}$$

$$F \geq 1 + \frac{\gamma}{g_{m1} R_S} + \gamma g_{m2} R_S \tag{9}$$

From (9), we can conclude that the main limitation of this configuration, with low device g_m, is higher NF. To attain NF<6 dB, g_{m1} has to be greater than g_{m2} by a factor of approximately 4 (e.g. g_{m1}=7 mS, g_{m2}=2 mS and R_L=1 kΩ).

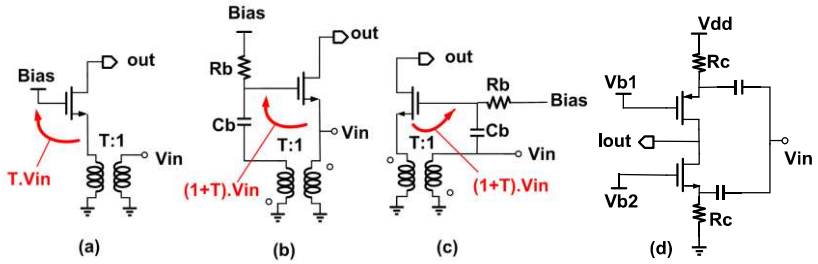


Fig. 2. Passive g_m boosting CG amplifiers (a-c) and current-reuse CG amplifier (d) [7].

F. Inductive degeneration LNA

So far the most popular inductor-less LNA topologies have been introduced. Now we can extend our exploration to magnetic devices based solutions. The inductive degeneration LNA is the most efficient method to perform low noise impedance matching (Fig. 1(f)). Assuming a loss-less inductor, input impedance matching can be achieved by resonating the reactive components (L_g+L_s with C_{gs}) and setting the real part g_mL_s/C_{gs} to R_s:

$$Z_{in} = \frac{g_m L_s}{C_{gs}} + s(Lg + Ls) + \frac{1}{sC_{gs}} \qquad (10)$$

where C_{gs} is gate-source capacitor and L_g and L_s are the gate and degeneration inductors respectively. In principle, it is possible to generate 50 Ω input impedance with a small g_m (e.g. 5 mS). However, to cancel the imaginary part of input impedance, it is required to employ very big series inductor at the gate to resonate it out. For large L_g and small L_s, the resonance condition can be written as $\omega_0 L_g = (\omega_t/\omega_0)(1/g_m)$, where $\omega_t = g_m/C_{gs}$ and ω_0 is the operating frequency. Assuming ω_t to be 4 times the operating frequency (e.g. 10 GHz for the 2.5 GHz band) a series inductor of more than 40 nH would be required, which can hardly be integrated on chip. The noise figure of this topology, assuming ideal inductors, is given by:

$$F \geq 1 + \gamma g_m R_s \left(\frac{\omega_0}{\omega_t}\right)^2 \qquad (11)$$

According to (11), NF can be well below 6 dB for a g_m of 5mS. The input device trans-conductance is enhanced by a factor Q, equal to the quality factor of the input resonant network, improving noise and gain. However, as the input device g_m scales down (when power dissipation is reduced), performance quickly degrades. In fact, the input Q must be increased so as to keep the transconductance gain (G_m) at an acceptable level. This quickly degrades the amplifier linearity since the signal between the gate and source of the transistor increases proportionally to the Q. Moreover, the use of the larger inductors increases chip size and degrades the noise due to increased series resistance of the inductor. In summary, the main limitation of this topology for low-power designs comes from technology limitations such as inductor area and losses.

G. Transformer-based gate-boosting CG LNA

As stated earlier, the power dissipation of CG LNAs is mainly limited by the input impedance matching requirement. Applying voltage gain through an on-chip transformer across the gate and source terminals of the input transistor (gate boosting) can effectively reduce the required device g_m to perform input impedance matching. Assuming ideal and noiseless transformer, input impedance and NF of transformer-based LNA in Fig. 1(g) can be computed as follows:

$$Z_{in} = \frac{1}{g_m (1+T)} \qquad (12)$$

$$F \geq 1 + \frac{\gamma}{(1+T)^2 g_m R_S} \qquad (13)$$

where T is the transformer turns ratio. However, it is difficult to achieve voltage gain of more than 3 with an on-chip transformer. Moreover, even though the device noise can be significantly reduced, the loss of the transformer can drastically degrade the overall NF.

From the above discussion, it is quite difficult, with popular and conventional LNA topologies, to achieve reasonably good performance with very low power consumption (e.g. 100 µW). Therefore, we need to explore more innovative topologies to drastically reduce power dissipation.

H. ULP LNA Topologies

In [16] a 100 µW LNA is presented. It is based on a complementary CS amplifier which is impedance matched to the source by the lossy LC resonant circuit at its input. This solution can be seen as an improved version of the resistively-terminated CS amplifier of Fig. 1(a). In fact, the inductor losses provide the resistive part of the input impedance, as required for power matching. Furthermore, the input resonator provides an effective passive voltage gain equal to its quality factor (~5), that boosts the LNA G_m. The main disadvantage is the degradation of the linearity but for ULP applications this may be acceptable. The complete receiver has a NF of 9 dB, an IIP3 of -21 dBm and consumes 400 µW from a 0.8 V supply. Another popular topology is shunt-feedback.

In [17] a complementary common-source amplifier with capacitive load and resistive shunt-feedback is presented. The resulting input impedance has a small resistive part and a large reactive part, which is resonated out using a large (10.2 nH) series inductor, leading to a large and resistive input impedance. Similar to [16], this passive impedance boosting scheme is used also to increase the gain. The resulting LNA has a NF of 5.3 dB at 2.4 GHz and draws only 150 μA from a 0.4 V supply. Even though the LNA performance and power are quite remarkable, the integration of the LNA in a complete receiver is not straightforward. In fact, the low supply voltage is hardly compatible with active mixers. On the other hand, the LNA would not work properly if a passive mixer was directly connected at its output since a capacitive LNA load impedance is required to achieve input impedance matching.

An improved active shunt feedback CG LNA is presented in [18]. Since reducing the bias current would severely degrade the NF, the power dissipation is reduced combining current reuse with a low voltage supply of 0.4 V. Operating with ultra-low supply voltage degrades the intrinsic gain of transistors due to short channel effects. In [18], forward body biasing (FBB) technique is employed to alleviate output conductance degradation without consuming extra power. The CG LNA along with a complementary current reuse active shunt feedback and inductive g_m-boosting is utilized to improve the overall performance and decreasing power consumption. The resulting LNA has a NF of 4.5 dB at 2.5 GHz and consumes 160 μW, however it requires 3 big inductors (30 nH total inductance), which significantly increase chip area.

In [13] a single-ended LNA using g_m-boosting inductive feedback is presented. A differential inductor with grounded center-tap is connected between source and gate of input device (in AC). The stage resembles the LNA in Fig. 1(g) but where the input is taken at the gate terminal and the transformer acts as an auto-transformer, with unitary turns ratio, effectively halving the input impedance and doubling the input device trans-conductance. To boost the source impedance above 50Ω and lower the g_m of the input transistor required for impedance matching, the inductor, together with a series capacitor, form a high-pass L-match network. The LNA draws 100 μA from a 1 V supply and achieves a NF of less than 4 dB at 1 GHz. Compared with the other ULP solutions, the latter LNA achieves lower noise and requires less current but it is hard to further lower its power dissipation without severely degrading its noise. In fact, to push further the impedance boosting factor, an even larger input inductor would be required, increasing the impact of its losses until, as in [16], they determine the real part of the input impedance, with a considerable NF degradation.

IV. Circuit Description

A. Gate-boosting and impedance boosting topology

Transformer feedback has been used extensively in the literature to improve LNA performance. Various configurations have been proposed: drain-source feedback achieves very low NF [26], gate-source feedback achieves low NF and wideband operation [27-28], drain-gate transformer feedback can be used to achieve gate-drain capacitance neutralization [29] improving the maximum gain at high frequencies. Transformer feedback can be used in combination with other techniques: in [30] gate-drain transformer feedback is used together with noise-cancellation to achieve lower noise [30] and dual-loop transformer feedback is used in [31] together with local positive feedback. Transformer feedback allows the LNA to operate at very low-voltage [1] and it has been employed also to achieve sub-1 mW power dissipation [13]. The proposed CG LNAs can be described conceptually starting from the simplified schematic reported in Fig. 2(a). A transformer with a 1:T turns ratio can be used to lower the power consumption of a CG amplifier in two ways: first, using a step-up transformer (T>1) as a wideband impedance converter by a factor T^2. Compared with an LC impedance transformation network, transformers have wider bandwidth and are less sensitive to inductor losses. Second, a 1:T transformer can be used to boost the gate-source voltage by a factor 1+T, without requiring extra power (Fig. 2(b)). In this work the basic idea is to combine impedance transformation and passive signal-boosting. As shown in Fig. 2(c), the LNA input is connected to the primary of the transformer and to the gate of the input device, while the source of the same device is connected to the transformer secondary. Assuming (ideally) a transformer with k=1, the source voltage is boosted by a factor of T while the gate-source voltage is boosted by a factor 1+T with respect to the input. The G_m is therefore:

$$G_m = (1+T)\, g_m \tag{14}$$

The input impedance is given by the impedance seen at the device source divided by T^2:

$$Z_{in} = \frac{1}{g_m T(1+T)} \tag{15}$$

To evaluate the required device g_m and the achievable NF versus the transformer turns ratio, the schematic in Fig.2(c) with lossless transformer was simulated and the results are reported in Fig. 3. A step-down transformer (T<1) can provide higher signal current and also improve NF but it significantly raises the power consumption. For instance, for T=0.25, NF can be as low as 0.8 dB and the required device g_m to perform input power matching is 64 mS, which is extremely power hungry for this application. With a 1:1 transformer (T=1) the device g_m required for impedance matching is $1/(2R_s)$ and G_m is the same as with a CG amplifier that carries twice as much current (i.e. doubling the G_m/I_d ratio). To save power, a step-up transformer should be used instead. Neglecting transformer loss, for T>>1, the required device g_m (and therefore power consumption) scales down as T^2 while F converges to 1+γ (i.e. typically below 3 dB). Hence, the noise-power trade-off is much better

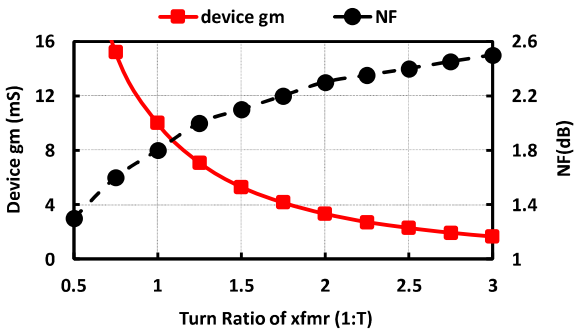


Fig. 3. Simulation of required device gm and NF vs T

compared to other ULP topologies such as the resistive-termination amplifier. With T=2, the device g_m required for impedance matching is $1/(6R_s)$ and G_m is one half that of a CG amplifier that carries six times the current (i.e. three times as efficient). When T becomes large transformer losses are no longer negligible. Modelling transformer losses as a resistance R_{loss} at its secondary, the LNA noise factor is:

$$F = 1 + \frac{\gamma T}{1+T} + \frac{T^2 R_S}{R_{loss}} \qquad (16)$$

where γ is the MOSFET noise parameter, the second term on the right-hand side accounts for the transistor thermal noise. For T=2 and a loss-less transformer $F=1+2/3\gamma$, which corresponds to a NF of 2.2 dB at the desired frequency. For large T the third term dominates since R_{loss} does not scale up as T^2. At the same time the G_m scales down as 1/T, making the noise of the following stages more important. An additional power saving technique is highly desirable to achieve ULP operation. Two options will be investigated: current-reuse and ultra-low supply.

B. Current-reuse LNA Design

Stacking more devices to re-use bias current can improve voltage efficiency, further reducing power consumption. A current reuse scheme for CG amplifiers is shown in Fig. 2(d): a PMOS is stacked on top of an NMOS and the signal is fed at both sources through capacitors, resulting in an equivalent $G_m = g_{m,NMOS} + g_{m,NMOS}$. For the same input impedance and NF, this enables to halve the DC current. A similar solution was adopted in [18] but using large inductors instead of resistors. Merging passive gain boosting in Fig.2(c) and current reuse scheme in Fig.2(d), results in the device g_m required for impedance matching to be $1/(12R_s)$. One of the issues to deal with is the minimum supply voltage required by the voltage-stacking scheme. When a low supply voltage is used the value of the bias resistors must be reduced, increasing the NF. In this work, we assume that only a supply voltage of 0.8 V is available and used for the entire design. Driving one of the two transistor sources with the secondary of the transformer eliminates one of the two bias resistors. This leaves plenty of voltage headroom that can

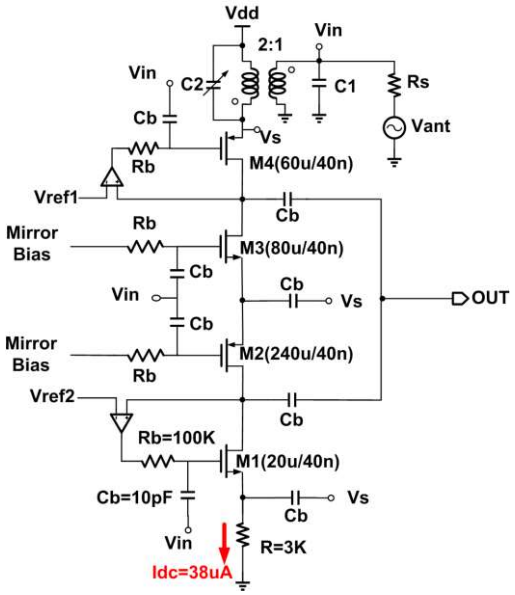


Fig. 4. Schematic of Proposed ULP LNA [7]

be used to further reduce the DC current by stacking more devices. The schematic of the actual ULP LNA proposed in this work is depicted in Fig.4. Two NMOS and two PMOS share the same bias current and have the same gate-source voltage signal. To have equal g_m for all devices, PMOS size is 3 times that of NMOS and all devices are biased in moderate inversion for optimum FoM_{RF}. Assuming all devices to have the same g_m, the total equivalent G_m is equal to four times the device g_m. Combining this current-reuse scheme with a 1:2 transformer, the device g_m required for impedance matching is only $1/(24R_s)$. As a result, the LNA bias current can be as low as 38μA. The voltage drop across the 3 kΩ bias resistor is less than 120mV, leaving on average more than 170 mV Vds across each MOS to ensure operation in saturation region. The gate-source voltage of each device is three times the LNA input voltage, resulting in a total G_m of $4x3/(24R_s)=10$ mS. This is one half that of a plain CG amplifier but with a current saving of 24x and a 12x G_m/I_d ratio. Including transformer losses, the noise factor of the proposed LNA is:

$$F = 1 + \frac{\gamma T}{1+T} + \frac{T^2 R_S}{R_{loss}} + \frac{T^2 R_S}{R} \qquad (17)$$

where R_{loss} is the equivalent parallel loss resistance of the transformer at secondary, and R is the biasing resistor. The bias current is set through a 1:20 current mirror using two diode-connected transistors in series, one NMOS and one PMOS, connecting to the gates of M2 and M3. The drain voltages of M4 and M1 are set to 0.65 V and 0.25 V respectively through two folded-cascode OPAMPs. Each OPAMP consumes 0.8 μA and its reference current (0.2 μA) is used also to generate Vref1 and Vref2. The total power dissipation of the references and bias circuits is 3.1 μW. In a complete receiver the proposed design can operate as low-noise transconductance amplifier

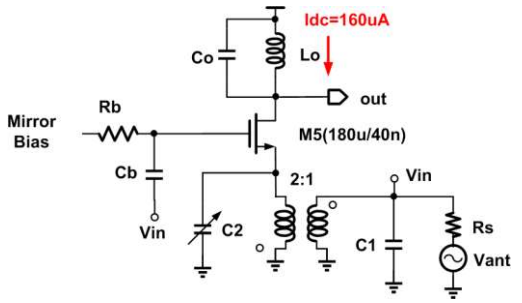


Fig.5. Schematic of ULV LNA

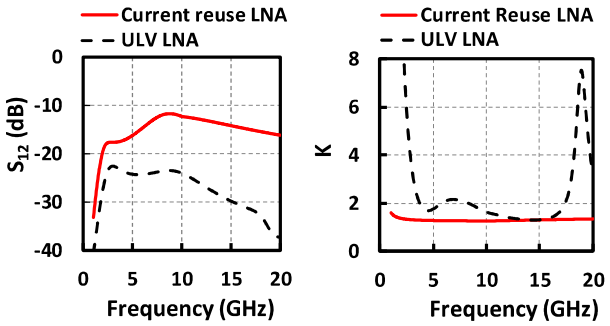
(LNTA) in front of passive mixer since it has sufficiently large transcondutance of 10 mS and a sufficiently high output impedance is 1.25 kΩ. Notice that, if a cascode had been used instead of M2 and M3 in Fig.4, ideally the required device gm to perform input matching would be 1/(12Rs) and the required current would be doubled. To preserve the same drop voltage across drain-source of all transistors, the bottom resistor would have to be halved, degrading the NF.

C. ULV LNA Design

In this section, we investigate feasibility of proposed impedance transformation and passive signal-boosting for ultra-low supply voltage LNA, as shown in Fig. 5. Instead of employing current reuse approach, we can drastically reduce supply voltage to minimize the power consumption. For fair comparison, the supply voltage is considered to be 0.18 V, similar to the average dropped voltage across drain-source of transistors in the current reuse LNA of Fig. 4. Additionally, for the same transformer turns ratio T=2, the required device g_m for impedance matching is $1/(6R_s)$. Using a four-times higher bias current compared to the current-reuse LNA of Fig. 4, the power consumption is nearly equal. Due to the extremely limited available voltage headroom, inductive load has to be used. Moreover, an ULP charge pump can be employed to boost the available supply voltage to the sufficient value to drive the gate of the transistor (e.g. in [2] the supply voltage of 0.18 V was boosted by factor of 3, reaching 0.54 V). Since a very small static current is required from the boosted voltage, the power dissipation and area occupation of the charge pump will be determined by other receiver building blocks and is not further investigated here. If we model the noise of the load inductor as a parallel resistor R_{load}, the equivalent noise factor can be computed as follows:

$$F = 1 + \frac{\gamma T}{1+T} + \frac{T^2 R_S}{R_{loss}} + \frac{4T^2 R_S}{R_{load}} \qquad (18)$$

where R_{load} is the equivalent loss of the load inductor. As can be clearly seen from (18), due to the limited Q of on-chip inductors, inductive load significantly contributes to the total noise factor. In fact, even assuming equal loss resistance for transformer and load inductor, the noise of the load directly goes to the output, while only half of the input transformer noise



(a) (b)

Fig.6. Stability simulations: (a) S_{12} and (b) K factor.

current goes to the output due to the input matching, as a result the input referred noise of the load counts 4 times more. As a consequence, the NF of the ULV is expected to be higher than for the current reuse LNA. For fair comparison, the load inductor is chosen such that the two LNAs have almost equal gain. The load inductor is chosen to be 3.5 nH and has a Q of 11.5. It is implemented in 4 turns, winding width of 6 µm, spacing of 2 µm and the occupied area is 0.048 mm^2. It is obvious that using inductive load leads to a narrow-band frequency response, as will be clearly shown in the simulation results (Fig.13).

D. Stability

In high frequency amplifier design, stability needs to be wisely taken into consideration. Even though standard CG LNAs are ideally very stable, it is interesting to investigate the stability of the proposed LNAs due to application of g_m boosting. The parasitic gate-drain capacitance introduces a high-frequency feedback path that reflects the load impedance at the input and can cause stability issues. This effect is more alarming for inductive loads. In fact, due to the Miller multiplication, inductive loads can create negative impedance at the input and potentially cause instability. The Rollett's stability factor (K factor), represents stability utilizing S-parameters and is expressed as follows [19]

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12}S_{21}|} \qquad (19)$$

When K>1 circuit is unconditionally stable. It can be observed from the simulation results in Fig. 6 that the ULV LNA is unconditionally stable at all frequencies. Initially the K factor of current reuse LNA was dangerously close to 1 at high frequencies. This is due to the fact that transistors M2 and M3 were oversized by factor of 4 with respect to M4 and M1 respectively in order to enable their biasing with gate voltages within the supply rails. Effectively M2 and M3 are biased in weak inversion, which strongly degrades their f_T. Using above-supply biasing as for the ULV LNA transistor would allow to reduce their size by 4x, significantly improving stability thanks to the lower S_{12}. As an alternative, in this work, a small 100 fF

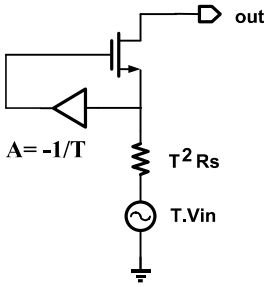


Fig.7. Simplified schematic for linearity analysis.

capacitor with 50 Ω series resistor is added to the output. This increases losses at high frequencies, well above the 2.5 GHz signal band, reducing S_{22} and ensures unconditional stability also for the current reuse LNA as can be clearly seen in Fig.6.

E. Linearity Analysis

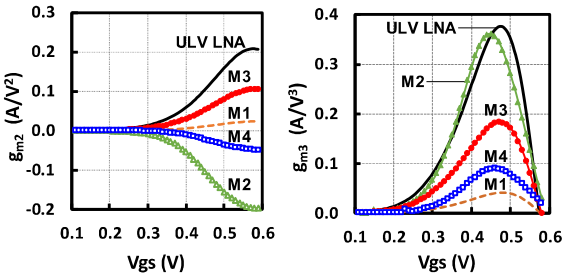
The dominant sources of nonlinearity in a MOS transistor are the nonlinear transconductance g_m, which converts the linear input voltage to nonlinear output drain current, and the output conductance [20]. When the voltage gain is sufficiently low, as in the present case, the drain conductance nonlinearity can be neglected to simplify further the analysis. Hence, in this section IIP3 will be evaluated assuming a grounded output. The weakly nonlinear MOS model for analysis of IIP3 is expressed as follows:

$$i_d \approx g_{m1}V_{gs} + g_{m2}V_{gs}^2 + g_{m3}V_{gs}^3 \quad (20)$$

To compute the IIP3 of the LNA, the simplified schematic of Fig. 7 can be used. The equivalent signal generator is represented at the source, scaled by the transformer by a factor T. The gate signal is therefore applied to an ideal amplifier that scales down the signal by 1/T. The complete derivation of the Volterra kernels is provided in Appendix I. The resulting IIP3 voltage A_{IP3} can be expressed as:

$$A_{IP3} \approx \sqrt{\frac{4}{3}\left|\frac{G_1}{G_3}\right|} \quad (21)$$

The nth-order transconductance nonlinearity coefficients of the transistors (g_{mx}) are derived from simulations and used in (21) to estimate the expected LNA IIP3. For the current reuse LNA, g_{mx} is the summation of nth-order nonlinearity of all NMOS and PMOS transistors. In Fig. 8 the second-order (g_{m2}) and third-order (g_{m3}) nonlinearity transcondutance coefficients of transistors versus V_{gs} is reported and each of them is separately extracted at its nominal Vds in the entire LNA. In principle, complementary derivative superposition could have been used as an effective linearization method to improve the stacked LNA IIP3 [21,22]. For instance, one NMOS transistor can be biased in strong inversion and the other one in weak inversion such that the nonlinearity of the two have the same magnitude but opposite polarity and cancel out each other. In this design, however, the main constraint is given by the NF vs power trade-off. Biasing the transistors in strong inversion to improve linearity would lower the overall transconductance due to the lower g_m/I_d and degrade the NF or require a higher bias current. Moreover, in order to ensure operation of all the transistors in saturation a higher supply voltage or fewer stacked devices should be used.



(a) (b)

Fig. 8. (a) Second-order (g_{m2}) and (b) third-order (g_{m3}) nonlinearity transcondutance coefficients of transistors versus Vgs.

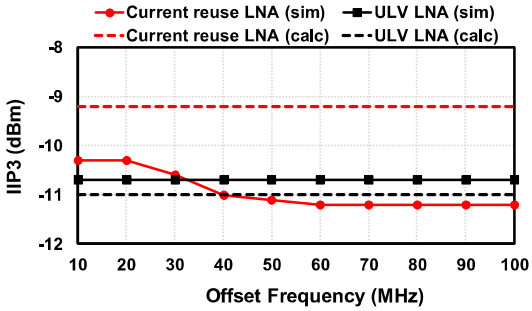


Fig. 9. Simulated and calculated IIP3 vs offset frequency from 2.4 GHz for current-reuse LNA (V_{gs}: $M_{1,4}$=0.4 V; $M_{2,3}$=0.3 V) and ULV LNA (Vgs=0.35 V).

Table II: extracted nonlinearity coefficients of transistors

	M1	M2	M3	M4	M5
g_{m1}(mA/V)	0.834	1.12	0.975	0.796	2.7
g_{m2}(mA/V²)	7.35	-9.1	9.5	-7.2	18
g_{m3}(mA/V³)	32.3	51.7	52	35.5	67.3

In this design the Vgs of all the devices are not equal: while M1 and M4 are biased in moderate inversion, the biasing of M2 and M3 was chosen to ensure that the gate of M2 stays above ground and the gate of M3 stays below the supply voltage. This avoids the use of a supplementary supply voltage but pushes M2 and M3 closer to weak inversion. The transistors small-signal nonlinear parameters at the nominal bias for the current reuse LNA (M1-4) and for the ULV LNA (M5) are reported in Table II. The IIP3 of the two LNAs is reported in Fig. 9 as a function of the two-tones frequency spacing. An IIP3 of -11.3 to -10.3 dBm for the current reuse LNA and -10.7 dBm for the ULV LNA are achieved. Based on the extracted nonlinearity coefficients and equation (21), the estimated IIP3 are -9.2 dBm and -11 dBm for current reuse LNA and ULV LNA respectively. The excellent agreement between calculations and this

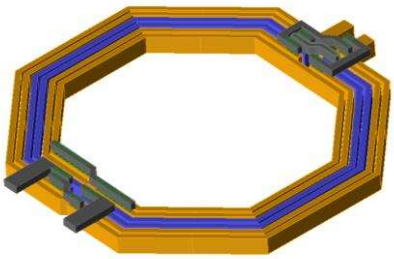


Fig.10. Layout of transformer

simulations confirms the validity of the nonlinearity analysis for the ULV LNA. For the current reuse LNA, the 1-2 dB error is likely due to the approximation taken when computing the combined distortion of the four transistors. In fact, the nonlinear voltages at gate and source of the four transistors are not exactly equal since some of them, being AC coupled, differ in the second-order intermodulation terms at f_1-f_2, that are not propagated by the AC-coupling capacitors. Nonetheless, the IIP3 is mostly determined by the third order nonlinearity coefficients and it is dominated by M2 and M3, that are biased closer to weak inversion and share the same source node, leading to an acceptable error.

F. Transformer Design and Optimization

The transformer is attached to the LNA input, hence its noise (loss) is directly added to the antenna noise source and degrades the NF. Moreover, the transformer offers ESD protection and it boosts the input transistors source voltage by a factor of 2. To design a transformer, self-inductance (L), quality factor (Q), coupling coefficient (k), and self-resonance (f_{SR}) are the main parameters to be considered. Self-resonance should be chosen such that Q is maximized at the operating frequency (f_0). As a rule of thumb, f_{SR} can be chosen to be twice f_0. The overall performance is highly dependent on the adopted technology back end of line (BEOL) and on the adopted transformer configuration. In the 40 nm CMOS technology used for this design only one ultra-thick metal with low sheet resistance (5 mΩ/sq) was available. A stacked transformer configuration has higher coupling factor but suffers from stronger capacitive coupling between primary and secondary. Moreover, the winding implemented in the high resistivity thin metal layer would lead to a lower Q. In contrast, coplanar configuration has less capacitive coupling resulting in high and more balanced Q on both primary and secondary but it has lower coupling factor. Since parasitic capacitive loading is present on both primary and secondary, both primary and secondary losses should be minimized. Hence, a coplanar configuration was selected.

The following aspects were considered to optimize the transformer. Transformer losses can be seen as a parallel loss resistance, which should be maximized. This calls for a high Q and high L. To maximize L, a large number of turns, large radius, and narrow spacing are required. Higher Q can be achieved by increasing the radius, winding width, and winding

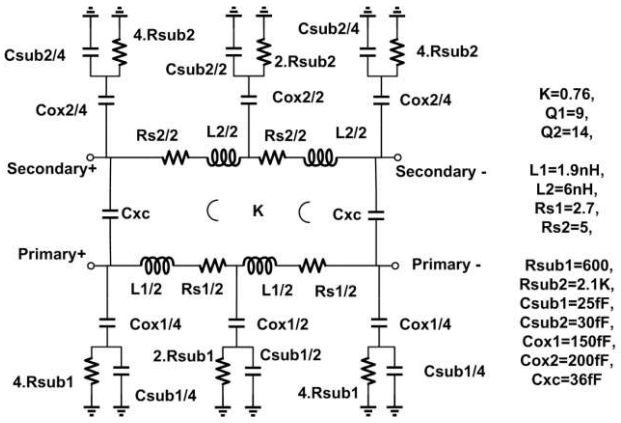


Fig.11. Lumped model of the transformer.

spacing. Finally, high k is achieved by increasing the number of turns and decreasing the inter-winding spacing. We are interested in designing a step up transformer (with turns ratio of 1 to 2), with highest Q and k. Two and four turns were considered for primary and secondary windings respectively. Even though increasing winding width can improve the Q (up to the point where parallel losses linked with the substrate become dominant [1], [19]), in a coplanar transformer, this would degrade k and hence the effective turns ratio. In a step-up transformer, parallel loss is more important, especially in the secondary and therefore a relatively small (4 μm) winding width was chosen. Choosing a large radius (90 μm in this design) results in high inductance. For a given winding inductance, a large radius allows reducing the number of windings, thus reducing the parasitic capacitance and improving the Q. Additionally, to maximize k, minimum winding spacing of 2 μm is chosen. The layout of the designed transformer, whose area occupancy is 0.065 mm^2, is shown in Fig. 10. The two middle windings make up the primary, which is inserted between the inner and outer winding of the secondary to maximize the coupling factor. EMX software was used to optimize and perform Electromagnetic (EM) simulation to precisely model transformer properties especially self-inductance (L), quality factor (Q), coupling coefficient (k). According to the EM simulation, a lumped model was derived to characterize the transformer. As can be seen in Fig. 12, there is a very good agreement between EM simulations and the extracted lumped model, which allows to examine the transformer design. A good compromise between reducing the losses, maximizing coupling factor and minimizing the area were achieved. The designed transformer has Q of 9 and 14 for primary and secondary respectively and the coupling factor is close to 0.8 at 2.4 GHz. The step-up coplanar configuration exhibits higher Q on the secondary due to the higher self-inductance. The self-resonance occurs above 9 GHz and the peaks of the Q are between 4 and 6 GHz, which shows that substrate losses were properly minimized and ensures that high Q is achieved even in worst-case corner with lowest f_{SR}.

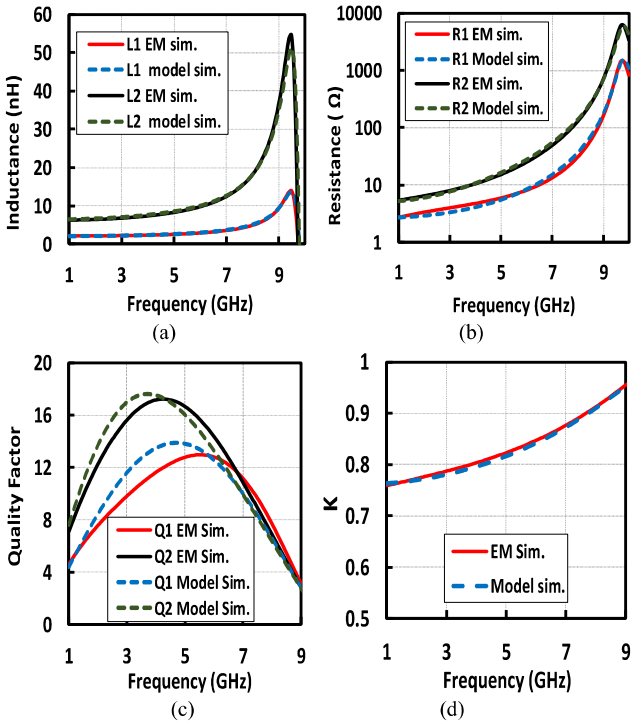


Fig.12. Simulation results of EM and lump model of transformer, (a) inductance, (b) loss, (c) Quality factor, (d) coupling factor

V. Simulation Results

The proposed LNA was designed in TSMC 40 nm CMOS technology using low threshold devices. The current-reuse LNA has a supply voltage of 0.8 V. The ULV LNA has a supply voltage of 0.18 V, which can be generated directly from energy harvested from environment [2]. The dissipated power in both LNAs is only 30 µW excluding the biasing network. The LNAs were designed and optimized to operate at 2.4 GHz. However, thanks to the use of a wideband transformer, the operating frequency band can be easily tuned though a variable capacitor (C_2) placed on the secondary of transformer between 1 GHz and 4 GHz. However, for the ULV LNA, an additional variable capacitor for load tuning is also required. Fig. 13(a) shows the performance of the proposed ULP LNA when tuned to operate at 2.4 GHz for WSN applications. As can be seen, it has a well-matched input impedance (S_{11} = -22 dB) at the desired frequency and it achieves a voltage gain of 14.2 dB while its 3-dB bandwidth is 2 GHz.

The minimum NF is 3.3 dB, including the transformer losses. The effectiveness of the passive g_m-boosting in a CG LNA can be seen considering that, for a lossless transformer, the NF is only 2.3 dB at the desired frequency, a remarkable result with a DC current of just 38 µA. The performance of the ULV LNA is plotted in Fig. 13(b). The input return loss is as low as -25 dB. Voltage gain and NF are 14 dB and 5.2 dB respectively at the desired frequency. The noise contributors of both LNAs are represented in Fig. 14. Simulations do not include the noise contribution from the voltage regulator that

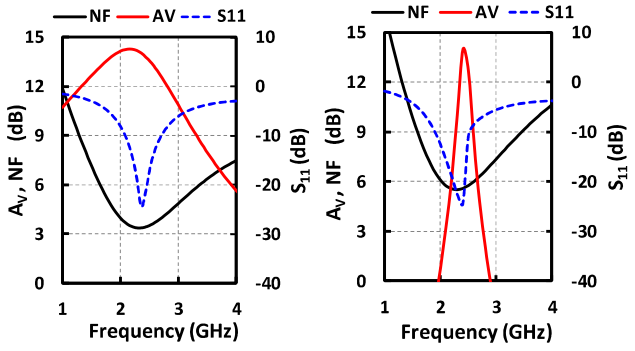


Fig. 13. Voltage gain, NF and S_{11} of (a) current-reuse LNA and (b) ULV LNA.

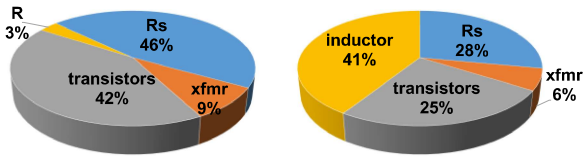


Fig.14. Noise contributors in % for (a) current-reuse LNA and (b) ULV LNA.

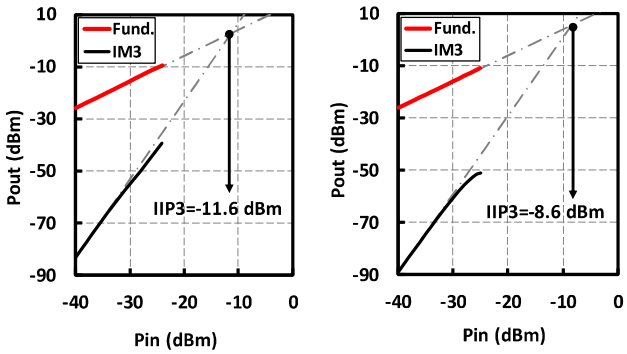


Fig.15. Simulated IIP3 of (a) current-reuse LNA and (b) ULV LNA.

would be required in real applications. As can be clearly seen, the noise contribution of transformer losses is less than 10% of the total noise in both cases, confirming the effectiveness of the transformer design optimization. Fig. 14(a) shows that for the current-reuse LNA the dominant noise contributor comes from the active devices, with a minimal contribution from the bias resistor. Fig. 14(b) shows that, for the ULV LNA, the losses of load inductor are dominant. This is due to the limited Q of the on-chip inductor but, more importantly, to the fact that the load inductor losses weigh 4 times more than for the input transformer, as indicated by (18). Unfortunately, it is unavoidable to use inductive loads at drastically reduced supply voltages. To simulate IIP3, two input tones are placed around 2.4 GHz with 20 MHz offset. Simulation results for current-reuse and ULV LNAs are -11.6 dBm and -8.6 dBm respectively, as reported in Fig. 15. A slight improvement/degradation is observed with respect to the IIP3

TABLE III: PERFORMANCES SUMMARY AND COMPARISON WITH STATE-OF-THE-ART LNAs

	Current-reuse	ULV LNA	[13]	[14]	[15]	[17]	[18]	[22]	[23]	[24]	[25]
Freq(GHz)	2.4	2.4	1	0.1-1	0.1-1.6	2.4	0.6-3.1	5	2.4	2.14	3.1-10
Tech (nm)	40	40	130	130	90	130	130	180	16	65	90
Vdd (V)	0.8	0.18	1	1.2	1	0.4	0.4	0.6	0.1	0.6	0.4
Pdc (µW)	**30**	30	100	720	425	60	160	1300	44	402	410
NF (dB)	**3.3**	5.2	3.9	4	5.5	5.3	4.5	3.5	3	2.8	4.5
Gain (dB)	14.2	14	16.9	10.2	10.5	13.1	13	12.5	10.8	9.2	15
IIP3 (dBm)	-11.6	-8.6	-11.2	-13	-4.5	-12.2	-12	-2	-18	NA	-7
FOM	**10.4**	10	3.65	0.39	1.1	1.9	0.97	2.11	1.58	NA	1.5
S/M	**S**	S	M	M	S	M	M	S	M	S	S

S/M: Simulation / Measurement

analysis carried out under low load impedance condition.

A. Process and Supply Voltage Variations

It is very important to investigate the sensitivity of the LNAs performance to the variations in process corners and supply voltage. The effect of a supply voltage variation of +/-10% on voltage gain (A_V) and NF for both LNAs are reported in Fig. 16. The current-reuse LNA is almost insensitive to the 10% variation of supply voltage. However, if supply voltage reduces below 0.68 V, the biasing mirror circuit does not work properly and the overall performance is degraded. The ULV LNA A_V is almost insensitive to variations in the low (0.18 V) supply since its gate bias voltage is generated from a separate (boosted) supply. The NF variation is less than 0.2dB. Gain, noise and input return loss simulations were performed in three different process corner cases (SS @+100ºC, TT @27 ºC, FF @-55ºC) and the results are reported in Fig. 16 (a) for the current-reuse LNA and in Fig. 16(b) for the ULV LNA. For the current-reuse LNA, A_V and NF variation in all corner cases are less than 1 dB and 1.4 dB respectively. ULV LNA performance is a bit more sensitive to the process corners and +/-1 dB and +/-2 dB peaking variation for NF and Av is shown respectively. In both LNAs, very good impedance matching is also preserved across process corners. The overall performance of both LNAs are acceptable with respect to the corner case variation.

The overall performance of the proposed LNAs is compared with that of recently published ULP LNAs in Table III. The proposed LNAs consume much less power compared to state-of-the-art LNAs and far exceed the requirements of WSN standards such as BT-LE [12]. The current-reuse LNA has also a very competitive NF, while the ULV LNA has a NF comparable to other ULV designs (with supply below 0.5 V), the only exception being the LNAs in [23,24]. Using very advanced technology of 16nm FinFET, the LNA in [23] is suppled at only 100 mV and shows NF of 3 dB and it consumes just 44 µW. Nonetheless, the dissipated power of the ULV LNA is 33% less and voltage gain and IIP3 are higher. Compared with [17], which is the second lowest power LNA reported, our designs exhibit equal or lower NF, better IIP3 and half the dissipated power. To evaluate the overall performance of the proposed LNAs we use a classic figure of merit (FOM), defined as:

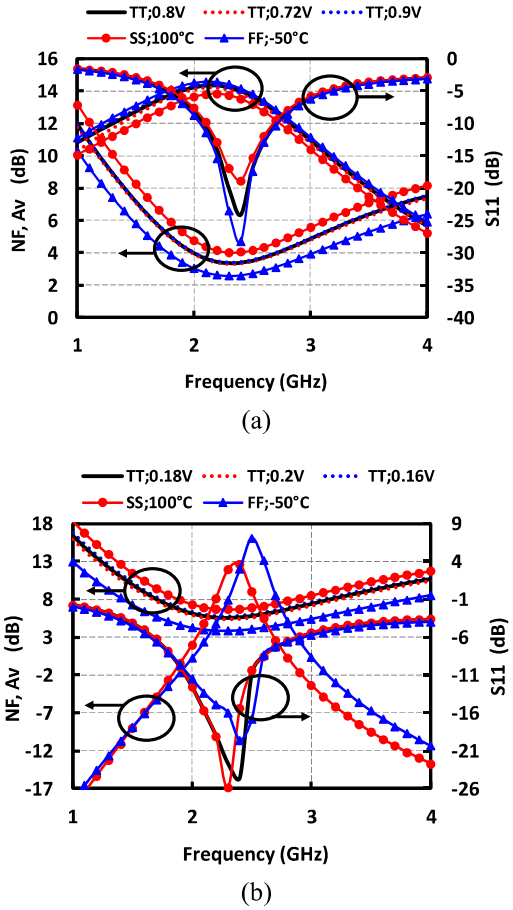


Fig.16. Corner simulations of (a) current-reuse LNA, (b) ULV LNA

$$FOM = \frac{IIP3(mW)\,Gain(lin)}{(F-1)\,Pdc(mW)} \qquad (22)$$

Due to the extremely low dissipated power and low NF, both

our designs have the highest FOM compared to the all previously published works reported in Table III. For fair comparison, it should be mentioned that while [13] [14] [17] [18] and [23] report measured results, this work, together with [15] [22] [24] and [25] only report simulation results. Furthermore, on given power consumption, the proposed current-reuse LNA represents the better NF, higher sensitivity and less estimated area compare to the ULV LNA. However, if an ultra-low supply voltage is required, the proposed ULV LNA demonstrates an overall competitive performance.

VI. Conclusion

A transformer-based passive g_m boosting technique for ultra-low power LNAs has been proposed. An ultra-low power ultra-low voltage LNA, powered from a 0.18 V supply, achieves in simulation 5.2 dB NF at 2.4 GHz and dissipates only 30 µW. Another design combines transformer-based passive g_m boosting with an efficient current-reuse topology. Powered from a 0.8 V supply the current-reuse LNA achieves in simulation 3.3 dB NF at 2.4 GHz and dissipates only 30 µW. Both LNAs demonstrate stable performance across +/-10% supply voltage variations. The proposed designs operate as low-noise transconductance amplifiers and are therefore suitable for integration in a passive-mixer based wireless receiver for wearable WSN applications with extend battery lifetime.

Appendix I

To start analysis of linearity using Volterra series, initially defining Vs, the voltage at the source node of transistor, as the intermediate variable, and express the relation between Vs and Vin up to 3rd-order as:

$$V_s \approx A_1(s_1)\circ V_{in} + A_2(s_1,s_2)\circ V_{in}^2 + A_3(s_1,s_2,s_3)\circ V_{in}^3 \quad (A.1)$$

Then by writing KCL equation for this circuit, we have:

$$i_d = \frac{V_S - TV_{in}}{T^2 R_s} \quad (A.2)$$

$$V_{gs} = -\frac{1+T}{T} V_S \quad (A.3)$$

To obtain the expressions for the 1st, 2nd-, and 3rd-order Volterra kernels $A_1(S_1)$, $A_2(S_1, S_2)$, $A_3(S_1, S_2, S_3)$, we substitute (21), (A.1) and (A.3) into (A.2) and cancel out Vs. To simplify calculation, it is assumed that passive components resonate at desired frequency and that the impact of parasitic capacitors is negligible, leading to frequency–independent intermodulation terms.

To get $A_1(S_1)$, we assume a single input tone and equating equations

$$-g_{m1}\frac{1+T}{T}A_1(s_1)\circ V_{in} = \frac{A_1(s_1)\circ V_{in} - TV_{in}}{T^2 R_S} \quad (A.4)$$

Therefore, the first order Volterra kernels can be easily obtained as follows:

$$A_1(s_1) = \frac{T}{1+(1+T)Tg_{m1}R_S} \quad (A.5)$$

Repeating previous procedure while applying two tone to the input results in,

$$-g_{m1}\frac{1+T}{T}A_2(s_1,s_2)\circ V_{in}^2 + g_{m2}\left(\frac{1+T}{T}\right)^2 A_1(s_1)A_1(s_2)\circ V_{in}^2 = \frac{A_2(s_1,s_2)\circ V_{in}^2}{T^2 R_S} \quad (A.6)$$

and after simplifying, the second order Volterra kernels can be achieved as follows:

$$A_2(s_1,s_2) = \frac{g_{m2}(1+T)^2 R_S A_1^2(s_1)}{1+(1+T)Tg_{m1}R_S} \quad (A.7)$$

For the third order coefficient, it is required to apply three tones to the input leading to,

$$-g_{m1}\left(\frac{1+T}{T}\right)A_3(s_1,s_2,s_3)\circ V_{in}^3 + 2g_{m2}\left(\frac{1+T}{T}\right)^2 \overline{A_1(s_1)A_2(s_1,s_2)}\circ V_{in}^3 - g_{m3}A_1(s_1)A_1(s_2)A_1(s_3)\circ V_{in}^3 = \frac{A_3(s_1,s_2,s_3)\circ V_{in}^3}{T^2 R_s} \quad (A.8)$$

Therefore,

$$A_3(s_1,s_2,s_3) = \frac{2g_{m2}\overline{A_1(s_1).A_2(s_1,s_2)}(1+T)^2 R_s - g_{m3}A_1^3(s_1)T^2 R_s}{1+(1+T)Tg_{m1}R_s} \quad (A.9)$$

Now, expressing output current with respect to the input voltage as follows,

$$i_d \approx G_1\circ V_{in} + G_2\circ V_{in}^2 + G_3\circ V_{in}^3 \quad (A.10)$$

By substituting (A.1) and (A.10) into (A.2), we have:

$$-g_{m1}\frac{1+T}{T}A_1(s_1)V_{in} = G_1 V_{in} \quad (A.11)$$

And the first order nonlinearity coefficient can be given as,

$$G_1 = -g_{m1}\frac{1+T}{T}A_1 \quad (A.12)$$

Applying similar procedure to obtain the second and third order nonlinear coefficients can be extracted as,

$$G_2 = -g_{m1}\frac{1+T}{T}A_2 + g_{m2}\left(\frac{1+T}{T}\right)^2 A_1^2 \quad (A.13)$$

$$G_3 = -g_{m1}\left(\frac{1+T}{T}\right)A_3 + 2g_{m2}\left(\frac{1+T}{T}\right)^2\overline{A_1A_2} - g_{m3}A_1^3 \quad \text{(A.14)}$$

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REFERENCES

[1] F. Zhang *et al*.," Design of a 300-mV 2.4-GHz Receiver Using Transformer-Coupled Techniques," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3190–3205, Dec. 2013.

[2] W. H. Yu *et al*., "A 0.18V 382µW Bluetooth Low-Energy (BLE) Receiver with 1.33nW Sleep Power for Energy-Harvesting Applications in 28nm CMOS," *in IEEE Internnational Solid-State Circuits Conference (ISSCC)*, pp. 414-415, 2017.

[3] H. Darabi *et al*.," Highly Integrated and Tunable RF Front Ends for Reconfigurable Multiband Transceivers: A Tutorial," *IEEE Transaction on Circuit and System-I: Regulare papers*, vol. 58, no. 9, Sep. 2011.

[4] Z. Lin *et al*, " A 2.4 GHz ZigBee Receiver Exploiting an RF-to-BB-Current-Reuse Blixer+Hybrid Filter Topology in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 49, no. 6, pp. 1333-1344, Jun. 2014.

[5] M. Ramella *et al*.," A 2.4GHz Low-Power SAW-less Receiver for SoC Coexistence," *in IEEE Asian Solid-State Circuits Conference (A-SSCC)*, Xiamen, Fujian, China, 2015.

[6] A. Selvakumar *et al*., " Sub-mW Current Re-Use Receiver Front-End for Wireless Sensor Network Applications", *IEEE* J. Solid-State Circuits, vol. 50, no. 12, pp. 2965–2974, Dec. 2015.

[7] E. Kargaran, D. Manstretta, and R. Castello," A 30µW, 3.3dB NF CMOS LNA for Wearable WSN Application," *in proceeding of IEEE International Symposium on Circuits and Systems (ISCAS)*, USA, 2017.

[8] B. S. I. Group, "Bluetooth core specification v4.0." https://www.bluetooth.org/en-us/specification/adopted-specifications, visited2013-09-15.

[9] R. Cavallari *et al*., "A Survey on Wireless Body Area Networks: Technologies and Design Challenges," *IEEE Commuications Surveys & Tutorials*, Vol.16, No.3, third quarter 2014.

[10] A. Pipino, A. Liscidini, K. Wan, A. Baschirotto," Bluetooth low energy reciever system desin," *in proceeding IEEE International Symposium on Circuits and Systems (ISCAS)* ,2015.

[11] H. Darabi *et al*. "A 2.4-GHz CMOS Transceiver for Bluetooth," *IEEE J. Solid-State Circuits*, vol.36, no.12, pp.2016-2024, Dec. 2001.

[12] J. Masuch, M. Delgado-Restituto, "A 1.1-mW-RX, -81.4dBm Sensitivity CMOS Transceiver for Bluetooth Low Energy", *IEEE Transaction on Microwave Theory and Technology.*," vol.61, no. 4, pp.1660-1673, Apr. 2013.

[13] A.Shameli, P.Heydari," A Novel Ultra-Low Power (ULP) Low Noise Amplifier using Differential Inductor Feedback," *in IEEE European Solid State Circuit Conference (ESSCIRC)* 2006.

[14] S.-T. Wang *et al*, "Design of a Sub-mW 960-MHz UWB CMOS LNA," *IEEE J. Solid-State Circuits*, vol. 41, no. 11, pp. 2449–2456, Nov. 2006.

[15] K. Allidina and M. El-Gamal, "A 1 V CMOS LNA for Low Power Ultra-Wideband Systems," *in proceeding of IEEE International Conference on Electronics, Circuits and Systems (*ICECS*)*, Aug. 2008, pp. 165–168.

[16] C. Bryant and H. Sjöland," A 2.45GHz Ultra-Low Power Quadrature Front-End in 65nm CMOS", *in proceeding of IEEE Radio Frequency Integrated Circuit (RFIC) Symposium* 2012.

[17] T. Taris, J.B. Begueret, Y. Deval," A 60µW LNA for 2.4 GHz Wireless Sensors Network Applications," *in proceeding of IEEE Radio Frequency Integrated Circuit (RFIC) symposium* 2011.

[18] M.Parvizi *et al*, "Short Channel Output Conductance Enhancement Through Forward Body Biasing to Realize a 0.5 V 250 µW 0.6–4.2 GHz Current-Reuse CMOS LNA," *IEEE J. Solid-State Circuits*, vol. 51, no. 3, Mar. 2016.

[19] B. Razavi, *RF Microelectronics*. Englewood Cliffs, NJ, USA: Prentice-Hall, 2012.

[20] Zhang Heng and E. Sanchez-Sinencio, "Linearization Techniques for CMOS Low Noise Amplifiers: A Tutorial," *IEEE Transaction on Circuit and System-I: Regulare papers*, vol. 58, no. 1, pp. 22–36, Jan. 2011.

[21] W. Chen, G. Liu, B. Zdravko, and A. M. Niknejad, "A Highly Linear Broadband CMOS LNA Employing Noise and Distortion Cancellation," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1164–1176, May 2008.

[22] E.Kargaran *et al*.," Highly Linear Low Voltage Low Power CMOS LNA," *in IEICE Electron. Express*, Oct. 2013.

[23] Ying-Ta Lu and Jun-De Jin," 100-mV 44-µW 2.4-GHz LNA in 16 nm FinFET Technology," *in proceeding of International Microwave Symposium (IMS)*, San Francisco, USA 2016.

[24] Vinaya M. M., Roy Paily, Anil Mahanta,," A New PVT Compensation Technique Based on Current Comparison for Low-Voltage, Near Sub-Threshold LNA," *IEEE Transaction on Circuit and System-I: Regulare papers*, vol 62, no.12, Dec. 2015.

[25] M. Parvizi *et al*, "A 0.4 V Ultra-Low-Power UWB CMOS LNA Employing Noise Cancellation", *in proceeding of* IEEE *International Symposium on Circuits and Systems (ISCAS),* 2013.

[26] D. J. Cassan and J. R. Long, "A 1-V Transformer-Feedback Low-Noise Amplifier for 5-GHz Wireless LAN in 0.18-µm CMOS," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 427-435, Mar. 2003.

[27] M. T. Reiha, J. R. Long, and J. J. Pekarik, "A 1.2 V Reactive Feedback 3.1–10.6 GHz Ultrawideband Low-Noise Amplifier in 0.13 µm CMOS," *in Proeeding of IEEE Radio Frequency Integrated Circuit (RFIC) Symposium*, Jun. 2006.

[28] P. Y. Chang, S. H. Su, S. S. H. Hsu, W. H. Cho and J. D. Jin, "An Ultra-Low-Power Transformer-Feedback 60 GHz Low-Noise Amplifier in 90 nm CMOS," *IEEE Microwave and Wireless Components Letters*, vol. 22, no. 4, pp. 197-199, Apr. 2012.

[29] G. Nikandish and A. Medi, "Transformer-Feedback Dual-Band Neutralization Technique *IEEE Transaction on Circuit and System-II: Express Briefs*, vol. 64, no. 5, pp. 495-499, May. 2017.

[30] L. Wu, H. F. Leung and H. C. Luong, "Design and Analysis of CMOS LNAs with Transformer Feedback for Wideband Input Matching and Noise Cancellation," *IEEE Transaction on Circuit and System-I: Regulare papers*, vol. 64, no. 6, pp. 1626-1635, Jun. 2017.

[31] S. Bagga, A. L. Mansano, W. A. Serdijn, J. R. Long, K. Van Hartingsveldt, and K. Philips, "A Frequency-Selective Broadband Low-Noise Amplifier With Double-Loop Transformer Feedback," *IEEE Transaction on Circuit and System-I: Regulare papers*, vol. 61, no. 6, pp. 1883–1891, Jun. 2014.

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