UNIVERSITÀ DEGLI STUDI DI PAVIA

CORSO DI DOTTORATO IN MICROELETTRONICA

DOTTORATO DI RICERCA

IN INGEGNERIA ELETTRONICA, INFORMATICA ED ELETTRICA

XXX CICLO

INTERFACE CIRCUITS FOR SENSORS AND ACTUATORS

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Tesi di Dottorato

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Anno Accademico 2017–2018

…إلى أمي و أبي

… to my parents.

Interface Circuits for Sensors and Actuators

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Abstract

Interface Circuits for Sensors and Actuators

The research activity described in this Thesis is the result of three different projects, all dealing with interface circuits for sensors and actuators.

1) Capacitive Humidity sensor with temperature controller and heater integrated in CMOS technology

The first project deals with the design of the integrated interface circuit for accurately controlling the temperature of a CMOS capacitive humidity sensor, with the final goal of allowing self-diagnostics and self-calibration of the sensor. The humidity sensor used is equipped with an integrated resistor and a temperature sensor which allow changing and measuring the actual sensor temperature.

This activity concentrated initially on the characterization of the humidity sensor provided by Texas Instruments, with the goal of determining the features and the behavior of the device and identifying the specifications of the integrated interface circuit. A measurement setup based on LabView has been developed to allow controlling the temperature of the sensor with an accuracy of 0.005˚C and measuring both the relative humidity and the temperature.

Based on the sensor measurement results we developed a model of the humidity sensor with built-in heater and thermometer in the Cadence framework, to allow the simulation of the complete system. In this sensor model, all the dynamic effects of the heater and relative humidity variation have been considered, to guarantee proper design of the temperature controller integrated circuit. The temperature controller is designed in CMOS technology; it allows a precise adjustment of the temperature with an accuracy better than 0.1˚C. The circuit is based on an analog control loop with PWM modulator.

The circuit has been fabricated using a 0.35μm CMOS technology.

2) Scaltech28 (test structures in CMOS 28nm)

The second project deals with the design of test structures in CMOS 28nm technology, to evaluate it potential for the implementation of sensor interface circuits in future high-energy physics experiments. This work has been carried out in the frame of project, SCALTECH28, which continues the tradition of other similar studies carried out in previous technology generations for achieving optimal results in IC design for various detectors.

This investigation within the selected 28nm technology had to address basic analysis on the single MOS devices (n-MOS and p-MOS), on passive elements like resistors and capacitors, and finally on basic circuits and system building blocks, among the most critical in the sensor interface circuits for different physics experiments.

The main purpose of the work is to investigate the performance of the 28nm technology in terms of signal processing quality, power consumption, and radiation hardness with respect to previous technological generations. An additional target is to experimentally evaluate radiation damage effects on single devices and on full circuits to develop rad-models for simulations. A test chip including elementary device arrays and dedicated read-out circuits has been developed and fully characterized. In particular, a capacitance to frequency converter has been integrated to measure the matching between different capacitors of a programmable array.

Experimental measurements showed that the worst-case measurement for the capacitor pair matching is around 0.98% error at 500fF. This value is compliant to the feasibility of A/D converters for sensor readout with resolution better than 10 bits. It is clear from the results that matching performance is comparable to previous technologies, making the 28nm technology eligible for analog signal processing in front-end circuits for physical experiments and related data converters. Samples have been sent to irradiation facility to be exposed to different radiation doses in order to be re-measured and compared in terms of matching and absolute capacitance values with respect to the measurements done before.

Based on the results obtained on the basic devices in 28nm technology, we designed a 14-bit 1MS/s extended range incremental A/D converter composed by the cascade of two resettable second-order sigma-delta modulators. The system is designed for reading out detector arrays in particle physics experiments. The two stages, ideally targeting 9 and 6 bits, respectively, are both based on a cascade of integrators with feed-forward (CIFF)

architecture to maximize linearity. If necessary, they can work in pipeline to minimize conversion time. When the conversion of each sample by the two stages is completed, a digital recombination filter produces the overall ADC output word with the required resolution (ENOB) of at least 13 bits and a throughput of 1MS/s at the very low over sampling ratio (OSR) of 16. Each stage, implemented with the switched capacitor technique, consists of two integrators followed by a multi-bit quantizer and a capacitive DAC for the feedback. At the start of each conversion cycle, both analog integrators and the digital filter memory elements are reset. The ADC has been sent for fabrication in 28nm technology.

3) Driving circuit for the piezoelectric actuators in ultrasonic washing machines

The third project deals with the design of the driving circuit for the piezoelectric actuators in ultrasonic washing machines.

The object of this project concerns the study and design of a driving and control system for an ultrasonic cleaning machine, or more commonly called ultrasonic washing machine. These devices are used in several industrial applications. Ultrasonic washing machines consist of a tank filled with a detergent solvent, an electronic interface circuit and one or more piezoelectric transducers, which are mechanically connected to the tank and electrically to the driving circuit.

The driving system is connected from the AC mains and consists of three cascaded stages: a rectifier followed by a boost converter, to regulate the power factor and produce an intermediate DC voltage; a buck converter, to adjust the amplitude of the supply voltage for the piezoelectric transducers; an inverter, to drive the actuators with a square wave at their resonance frequency between 30kHz and 40kHz. A flyback converter has also been designed for generating the auxiliary power supply voltage for all the integrated components in the system. A control system based on an Arduino microcontroller has been developed to adjust the frequency of the square wave to the resonance frequency of the transducer, control the output voltage of the buck converter and read data from a current sensor. The system is designed and implemented on a PCB board of 10cm$\times$ 15cm. The system has been tested on machined with two different tank sizes.

Part I

1.1 Introduction

1.2 Relative humidity and Absolute humidity

1.3 Operating principle of humidity sensor

1.4 Constructive typologies

1.5 Temperature control loop for capacitive humidity sensor

1.6 PID Controllers

1.7 Software implementation for temperature controlling

1.8 Overall system design for temperature controlling

1.9 Circuits design

1.10 Simulation results

1.11 Measurements results

1.12 State of Art

1.13 Conclusion

1.1 Introduction

The capacitive Humidity Sensor

Humidity sensors are very important and are widely used in many fields such as meteorology, agriculture, industrial control, medical instruments, etc. In the past two decades, there have been lots of researches on capacitive, resistive, piezo-resistive, optical, and microelectromechanical systems (MEMS) humidity sensors, which have got practical use in humidity measurement applications. [1] [2]. Humidity sensors have taken on a great deal of importance diffusion, in the electronic devices of consumption and in the field automotive, both in the industrial field.

Of all these types of sensors, capacitive humidity sensors are most commonly available in commercial field for their several advantages over other humidity sensors

- Linear sensitivity and high accuracy
- Low cost of manufacture
- Compatibility and ease of integration with CMOS technology

Humidity sensors main problems are

- Hysteresis
- Repeatability
- Stability
- Long term drift

In particular, capacitive moisture sensors have been established on the market thanks to the characteristics of response linearity and the possibility of integration with the CMOS and RFID technologies.

In these devices, long-term drift, the possibility of contamination and the combination of high levels of temperature and humidity can change the offset and sensitivity values obtained during initial calibration. This causes errors on moisture measurements.

A self-diagnostic and self-calibration system that updates periodically offset and sensitivity coefficients would increase the reliability and performance of the sensor in any situation.

Considering the relationship between relative humidity and temperature it is possible, at least in theory, change the relative humidity value in a predictable way at the level of the sensor only through controlled temperature variations, assuming that the absolute environmental humidity remains constant. Variations of temperatures can be obtained through a heater and a thermometer integrated in the humidity sensor itself.

The purpose of this discussion is to verify the practical applicability of the principle exposed on the sensor, comparing measure results with a suitable mathematical model, and propose

a system with self - diagnosis and autocalibration that uses only variations of temperature and capacity readings.

It is useful to analyze how the capacitive humidity sensor is working, also the parameters that characterized the sensor and the main constructive typologies which present now in market. But first we need to explain the basics concept about the relation between humidity and temperature.

1.2 Relative humidity and Absolute humidity

The absolute humidity of atmospheric air can be defined as the mass of water vapor present in the dry air mass per unit

$$X = \frac{m_w}{m_a} \left[\frac{Kg_{H_2O}}{Kg_{dry\ air}} \right] \qquad (1.1)$$

X is also referred to as the humid air. Another possible definition, referring to the unit of volume, is the following equation

$$AH = \frac{m_v}{V} \left[\frac{Kg_{H_2O}}{m^3} \right] \qquad (1.2)$$

The air is saturated when it is not able to contain any other water vapor, which, if added in more quantities, will condense.

Relative humidity is usually abbreviated “RH” and is expressed as a percentage between zero and 100%. RH indicates the amount of moisture in the air as a percentage of the maximum amount the air can hold (below 212°F). Unfortunately, the amount of moisture the air can hold depends on the temperature of the air. The higher the temperature (up to 212°F) the higher the amount of water vapor the air can hold. At 212°F and above it is possible for the air to be totally water vapor (steam) and the percent of moisture by volume can reach 100% [3].

The RH value (expressed as a percentage) indicates the amount of steam in the air (m_v).) in relation to the maximum value it can hold for a given maximum temperature (m_{max}). So, the definition is better to use (1.2) and expressing in percentage will give:

$$RH = 100 \frac{m_v}{m_{max}} = 100 \frac{\rho_v V/(R*T)}{\rho_{sat} V/ (R*T)} = 100 \frac{\rho_v}{\rho_{sat}} [\%]$$

Where ρ_v is the partial pressure of water vapor and ρ_{sat} is the saturation pressure.

The saturation pressure of water vapor is the partial pressure of water vapor at 100% humidity. 100% humidity is the point where liquid water and water vapor are in equilibrium, which means the water is evaporating into vapor and the vapor is condensing into liquid. Figure 1.1 shows the saturation pressure for water vs. temperature from 50°F to 550°F.

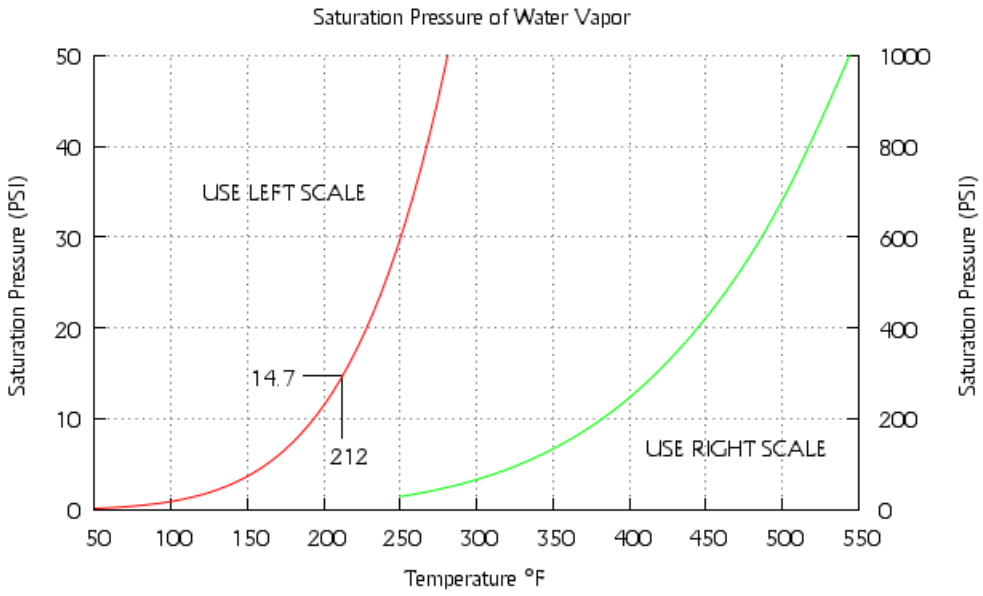

Figure 1.1: Saturation pressure for water vs. temperature.

From another physical point of view by inserting a liquid into a closed container. The evaporating water particles cannot therefore leave the container. There is also the reverse phenomenon or some molecules of water vapor condensing back to the liquid phase. The two processes occur simultaneously. Increasing the temperature (and thus the kinetic energy associated with the liquid molecules) will increase the number of particles changing to the vapor phase. This increase also influences the phenomenon of condensation. When the two processes are in balance, the saturation pressure for the chosen temperature is saturated. Saturation pressure therefore depends on the temperature (increases when the temperature rises) and of course the type of liquid.

In the following paragraphs, a few definitions are used frequently in humidity

Dew temperature is defined as the temperature at which the condensation begins if the air is cooled according to an isobaric process (constant steam pressure, constant atmospheric pressure). This is the saturation temperature corresponding to the partial steam pressure.

Wet-bulb temperature. When two thermometers are used to measure the relative humidity of the air: the first measures the dry bulb temperature. It is a normal thermometer that measures the air temperature. The bulb of the second thermometer is instead covered by a cotton soaked with water in contact with the air. The temperature thus measured is defined as wet bulb. It uses the principle that the air that passes through the cotton evaporates part of the water and its temperature decreases. When the temperature read on the thermometer is stabilized it is possible to calculate the RH of the air by knowing the difference in temperature between the two thermometers (dry bulb and wet bulb) [4].

1.2.1 Relative-temperature humidity relations

The relationships between the relative humidity and temperature required for the next explanation of the humidity sensors operation concept:

- AH = $\frac{m_{H_2O}}{V}$ Absolute Humidity

  Where m_{H_2O} is mass of water exist in air, while V is volume

- RH = 100 $\frac{\rho_v}{\rho_{sat}}$ Relative Humidity

Where $P_{H_2O} = \rho_v$ Partial pressure of water, $P_{SV} = \rho_{sat}$ is saturation vapor pressure

- μ_{H_2O} = $\frac{n_{H_2O}}{n_T}$ Mole of fraction of water

where n_{H_2O} is number of moles in water, n_T is total number of moles

the main used constant:

- μ_{H_2O} = 0.018 [kg.mol^{-1}] ➔ Molar mass of water
- R = 8.314 [J. mol^{-1}. K^{-1}] ➔ Universal gas constant

1.2.2 Dependence of temperature saturation pressure.

In order to express the relation between the relative humidity and the temperature, first, it is important to define the relation between the vapor saturation pressure and the temperature. As mentioned before, when saturation pressure increases, the temperature rises.

There are many formulas that link the relative humidity and the temperature. The most accurate is the Wexler formula that can be used as a reference. The expression binds the saturation pressure in Pa at the temperature expressed in °C through numerous coefficients,

$P_{SV} = e^{(\frac{a}{(273.15+T)^2}+\frac{b}{(273.15+\mathrm{T})}+c-d\,(273.15+T)+e(273.15+T)^2+f(273.15+T)^3+g(273.15+T)^4+hln(273.15+T)\,)}$

Where

- a = - 2991.2729;
- b = - 6017.0128;
- c = 18.87643854;
- d = - 0.028355721;
- e = 0.1783830 X 10^{-4};
- f = - 0.84150417 X 10^{-9};
- g = 0.44412543 X 10^{-12};
- h = 2.858487

For easier calculations, an approximate formula is used valid between -20◦C and 50◦C, the maximum error with respect to the Wexler formula is 0.2% of the value of RH, this simplified equation is:

$$P_{SV} = ae^{\frac{bT}{c+\mathrm{T}}} \qquad (1.3)$$

And it's called August-Roche-Magnus formula where the coefficients are:

- a = 6.11;
- b = -17.625;
- c = 243.04;

Now it is possible to define the relation between relative humidity and the temperature in open environment and closed environment.

1.2.3 Closed Environment

A closed sealed oven can be considered as sufficient closed environment where no air can escape. In this case V will depend on the geometry and constant coefficient. From eq. (1.2), it's clear that AH will remain constant while the temperature will be expressed as T[C] + 273.15 so now V is:

$$V = \frac{n_T\, R(T+273.15)}{P_T}$$

Substitute V in eq. (1.2):

$$AH = \frac{n_{H_2O}\, M_{H_2O}\, P_T}{n_T\, R(T+273.15)}$$

By substituting the partial pressure of water vapor

$$AH = \frac{M_{H_2O}\, P_{H_2O}}{R(T+273.15)}$$

By using RH definition stated before

$$RH = \frac{AH.\ R(T+273.15)}{M_{H_2O}\, P_{SV}} \qquad (1.4)$$

By substituting AH in previous equation and put all in equation 1.3

$$RH = \frac{1.36\, \mu_{H_2O}\, n_T\, (T+273.15) e^{\left(\frac{-17.625\, T}{243.04+T}\right)}}{V}\,[\%] \qquad (1.5)$$

It should be mentioned that with P_{SV} in RH is expressed in percentage.

1.2.4 Open Environment

In any open space or room can be considered open environment. In this case, P_T is constant (not depending on temperature) and the RH expression will be in f (T, μ_{H_2O}) and given by

$$RH = \frac{P_{H_2O}}{P_{sv}} = \frac{n_{H_2O}\, P_T}{n_T\, P_{sv}} = \frac{\mu_{H_2O}\, P_T}{P_{sv}}$$

By substituting in equation 1.3:

$$RH = \frac{P_T \mu_{H_2O}}{6.11} e^{\left(\frac{-17.625\, T}{243.04+T}\right)}[\%] \qquad (1.6)$$

In Figure 1.2, the RH relation with the temperature is shown. From equation (1.4), it is obtained AH so that RH is 80% at 10˚C. similarly from equation 1.6, the value of $\mu_{H_2O}$was obtained so that RH is 80% at 10˚C. In a closed environment RH changes with T less than in an open environment.

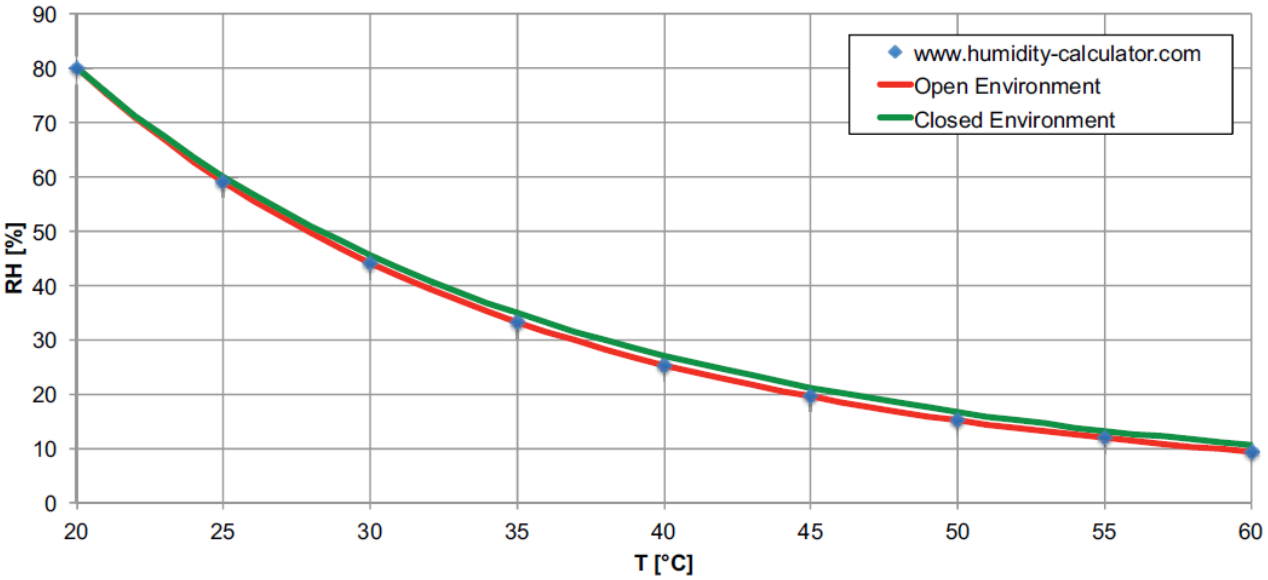

Figure 1.2: RH vs T in open environment and closed environment.

1.3 Operating principle of humidity sensor

The capacitive humidity sensor consists of a hygroscopic dielectric material placed between a pair of electrodes which forms a small capacitor. Most capacitive sensors use a plastic or polymer as the dielectric material [5], with a typical dielectric constant ranging from 2 to 15. When no moisture is present in the sensor, both this constant and the sensor geometry determine the value of capacitance.

At normal room temperature, the dielectric constant of water vapor has a value of about 80, a value much larger than the constant of the sensor dielectric material. Therefore, absorption of water vapor by the sensor results in an increase in sensor capacitance. At equilibrium conditions, the amount of moisture present in a hygroscopic material depends on both the ambient temperature and the ambient water vapor pressure. This is true also for the hygroscopic dielectric material used on the sensor. In our sensor, the polymer is used as dielectric material [6]. To explain the mathematical model, let's start with the formula used to measure the capacitance between two flat parallel planes.

$$C = \frac{\varepsilon_o \, \varepsilon_s \, A}{d} \qquad (1.7)$$

Where ε_o A and d are fixed constant depending on the geometry of the sensor.

Therefor the variation in capacity is related to the variation in dielectric permittivity ε_s. The dielectric permittivity of water ε_{H_2O} is of order 78.54 at 25◦C, while the dielectric permittivity

of the dry polyamide is of a lower value, so water absorption generates an appreciate variation of capacity. In conclusion, the variation in capacity value in equation (1.7) depends in the variation in relative humidity that as explained before, is related to the changes in absolute humidity and temperature.

1.3.1 Sensitivity and offset

Sensitivity refers to the ratio between the variation of the sensor response and the variation of the measurement of the object being measured. In the case of capacitive humidity sensors, it is therefore:

$$S = \frac{Variation\ in\ Capacity}{Variation\ in\ RH} \qquad (1.8)$$

S is defined as the derivative of the sensor response curve, mathematically it will be C=f(RH). In case of Polyamide, the response curve is a straight line and therefore " S " will be a roughly constant coefficient in the range [0%RH -100% RH]. Sensitivity value is a critical parameter for humidity sensors. At design level, it is requested to implement a constructive design such as to obtain the highest possible value of 'S', or maximize the percentage change in capacity relative to the total nominal capacity of the sensor derived from equation (1.7) by relative humidity variation.

Too low variations are difficult to measure and require tools that can measure small capacity which means high resolution. Typical capacities of humidity sensors are in the order of tenths of pF or hundreds of fF. The variation in capacitive is therefore of tenth of fF or hundreds of fF. Any effecting noise can disturb the measurements of the RH. With high sensitivity sensors, it is also possible to measure smaller RH variations in the sense that the sensors allow us to read such variations significantly. Larger 'S' allow to reduce the measurement error percentage (even in presence of any noises or insufficient accurate instruments) with respect to the RH variation with the same absolute error on the capacity variation measurements.

Offset means the zero value of the sensor measurement, in details what will be the capacitive value that is equal to 0% relative humidity RH. As discussed before, the capacitive value depends on the size of the sensor itself, but also there are some parasitic capacities that increase the capacitive value. These capacities (such as capacities from packaging or setup measurements components) can be behave as parallel capacitors to the main capacitors and thus have an effect which will increase the total capacity of the sensor and effect the measurements.

1.4 Constructive typologies

There are basically two elementary construction types for capacitive humidity sensor. Evolutions and modifications which can be found in industrial field, have on one hand the aim of reducing manufacturing costs and integration with technology CMOS, on the other hand, to increase sensor sensitivity as much as possible.

The primary capacitive sensors had a vertical structure. The polymer came inserted between the two electrodes (one above and the other under the polymer). This property has the advantage that all the electric field lines pass through the polymer. In this way, the sensitivity reaches the maximum possible value. It can be to consider that the sensitivity value obtained with this structure is theoretically maximum. It can be defined in terms of the vary of capacity per percentage unit has a change of RH percentage [7]. This type of construction has never been integrated with CMOS technology due to the difficulty of connecting to the electrode above the polymer.

The integrated sensors have instead a single layer of electrodes arranged in an interdigitated structure. The polymer is placed above this layer, as can be seen in Figure 1.3.

There are several variants of this basic scheme (for example, by removing part of the substrate or oxide) to increase the amount of polymer deposited between the spaces of the interdigitated structure, resulting in increased sensitivity up to values close to those of the vertical structure.

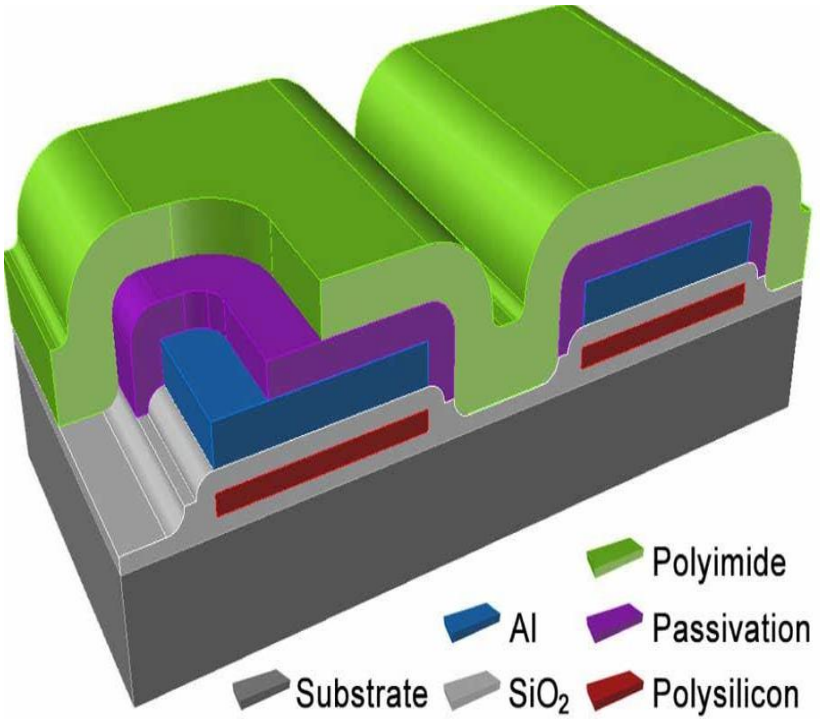

Figure 1.3: Humidity sensor with Polymer over interdigitated structure.

1.5 Temperature control loop for capacitive humidity sensor

The purpose of heating the sensor is to reduce the hysteresis phenomenon and the response time to changes in RH by increasing the kinetics of the system. The humidity sensor used in the studies, consists instead of the presence of a heater (a power-supplied resistor) and a thermometer (that is, a resistance whose read value can be suitably converted to temperature according to a known relationship), integrated for the purpose of performing a temperature control loop for the diagnostic and recalibration of the sensor.

Recalling the relationships (1.6) it is easy to guess the utility of a system like the one just described. Given the difficulty in performing controlled variations of μ_{H_2O} or equivalent of AH, it is necessary, for any self-diagnostic procedures and periodic autocalibration, to modify the relative humidity value read by the sensor through a known temperature ΔT as it is adjusted.

Indeed, a RH variation of 5% -10% obtained by variation of AH at a constant temperature requires a thermal chamber while an equivalent delta of RH obtained with temperature variation takes only a few minutes and can be realized with an integrated circuit.

The approach of the temperature control loop has some critical issues:

- In the construction phase, it is necessary to provide a uniform distribution of the temperature inside the sensor; the temperature read by the thermometer must, in fact, coincide with that actually present within the PI;
- The heater must be able to provide a useful temperature variation for the requested purposes with reasonable power consumption which is constrained by the voltages available for use in the integrated circuits; the reduction of the heat resistance value reduces the required voltage;
- it is only possible to heat the sensor and then decrease the value of RH according to (1.5) or (1.6) with equal of μ_{H_2O} ; the RH values read with such temperature variations are therefore less than or equal to the initial values (ambient values); however, sensitivity of the sensor can be reasonably assumed to vary in RH in the range [10% -90%] in most cases;
- In the humidity measurements with temperature variation without a reference sensor, it is necessary to consider the value of μ_{H_2O}during the measurement, i.e. assuming that the environmental conditions remain constant; it is necessary that the variations of RH are only induced by the ΔT imposed by the regulator; This hypothesis, though very strong, can be considered valid if the diagnostic and recalibration phases do not take too longtime.

1.5.1 Primary setup measurement

A preliminary measurement for setup was carried out prior to the temperature control loop achieved. An old sensor used for these tests is used with the presence of a higher resistance heater which request a higher voltage so more consumption of power. The heater also coincides with the thermometer (single resistance sensor).

The manufacturer provides a relationship between resistance and temperature according to the formula:

$$R(T) = R_0(1 + k_1 \Delta T + K_2 T^2) \qquad (1.9)$$

Where:

- $R_0$is the resistance value at a temperature R_0 [Ω];
- k_1 and k_2 are constant coefficients;
- ΔT is the temperature difference $T - T_0$ [K].

The coefficient values are k_1 = 3,6×10^{-3} $K^{-1}$and k_2 = -1,16×10^{-3} K^{-1}. The value of the coefficient k_2 makes the quadratic term negligible.

For example, if R_0 = 629Ω at temperature T_0= 297.25K, it is possible to obtain the value of T for each R value. Modifying the relationship (1.9) so it can be written

$$R - R_0 = R_0 k_1 (T - T_0)$$

It is convenient to introduce a C_{RT} coefficient that provides resistance variation for unit temperature variation. This coefficient is defined as

$$C_{RT} = \frac{R - R_0}{T - T_0} = R_0\, k_1\ [\Omega K^{-1}]$$

$$T = \frac{R - R_0}{C_{RT}} + T_0 \qquad (1.10)$$

The temperature value at instant time t where the resistance value read by the multimeter either (for example) 640 Ω will then be T = 302.11 K.

For the convenience of reading, in the rest of calculations that will follow, the temperature value will be converted to ° C according to the known relation T[°C] = T[K] – 273.15

The measurement set-ups done in open loop environment with 10 V power supply are represented in Figure 1.4.

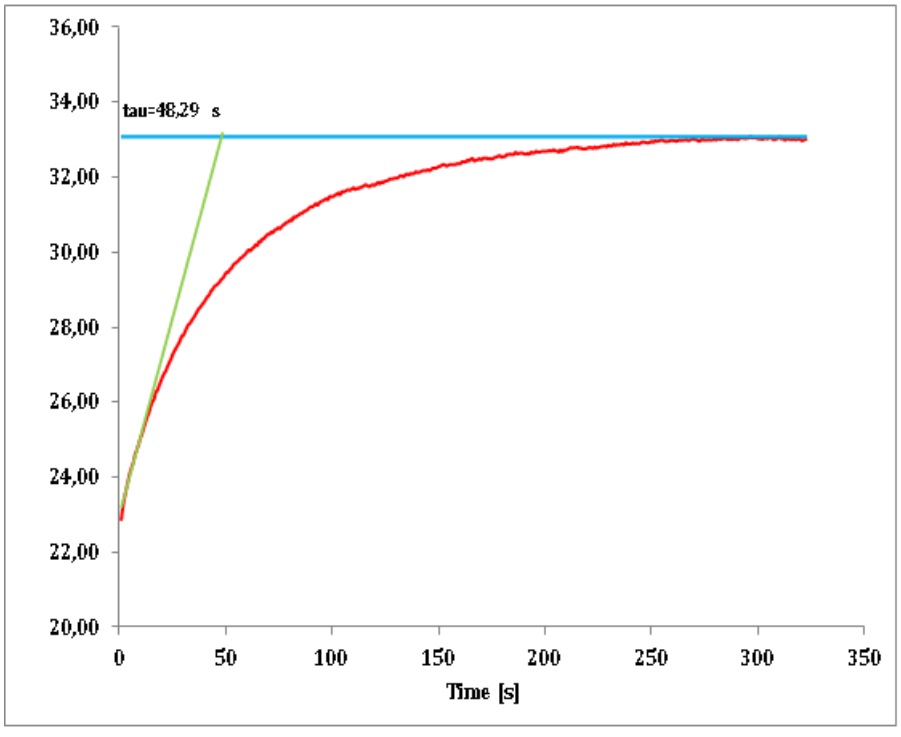

Figure 1.4: temperature response in the old sensor

From Figure 1.4, It is noticed that the temperature curve over time came from the voltage variation at the capacitor in a RC circuit of the first order for which:

$$V_c(t) = V_c(0)\, e^{-t/\tau} + V(1 - e^{-t/RC}) \qquad (1.11)$$

where

- V is the voltage from the power supply;
- τ = RC is the time constant of the circuit;
- $V_c(0)$ is the initial value of the voltage at the capacitors.

Note that for a RC circuit of the first order, the time constant is detected by the intersection between the tangent and the value of the voltage regime following the transient. In Figure 1.4, the time constant was calculated using the tangent method (finite differences). In Figure 1.5, the response of Figure 1.4 is compared to that of the exponential given by the equation (1.11) with a constant time of 48.29s, both normalized to the value of 1. The maximum error is -5% as shown in Figure 1.6 and therefore the approximation is only partially verified. But in fact, these considerations are acceptable, as it is limited to comparing the time constants between the different setup. After five-time constants which gives 241.45s, the temperature value in Figure 1.1a is 32.92 °C (99.5% of the value of the system). The percentage error after 5τ is therefore very low.

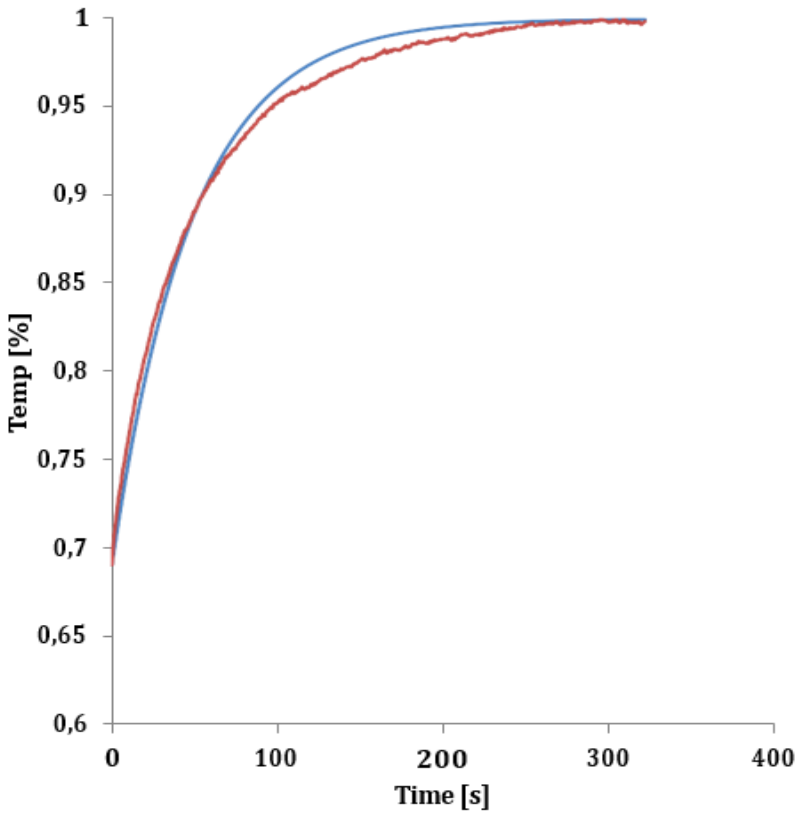

Figure 1.5: RC circuit first order in compare to normalized measurement (Red curve)

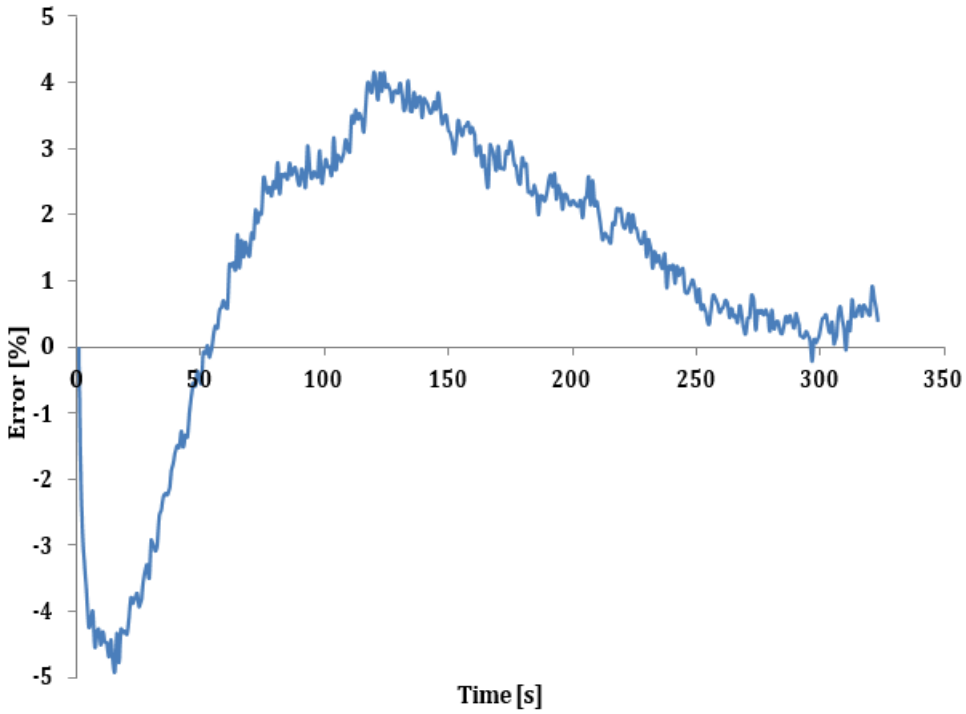

Figure 1.6: error in respect to the equivalent RC circuit

1.5.2 Equivalent Circuit of the Sensor

Based on the temperature responses obtained, it is possible to hypothesize an equivalent electrical circuit for the sensor including parameters of the chosen measurement setup. A possible equivalent circuit is shown in Figure 1.7 where the power supply is represented by a current generator. R_{tho} and C_{in} are considered the thermal resistance and thermal capacity of the sensor. R_{th1} is the thermal resistance between inside and outside the chip (thermal resistance of the package); R_{thset} and C_{set} are the two components that representing the thermal characteristics of the chosen setup. The circuit in Figure 1.7 is also valid for the sensor used in our measurement, taking into account that R_{tho} value is representing the physical separation between the heater and the thermometer. Regardless of the absolute values of the model parameters (which are not known) it can be stated that the choice of a different setup only varies with change in R_{thset} and C_{set}.

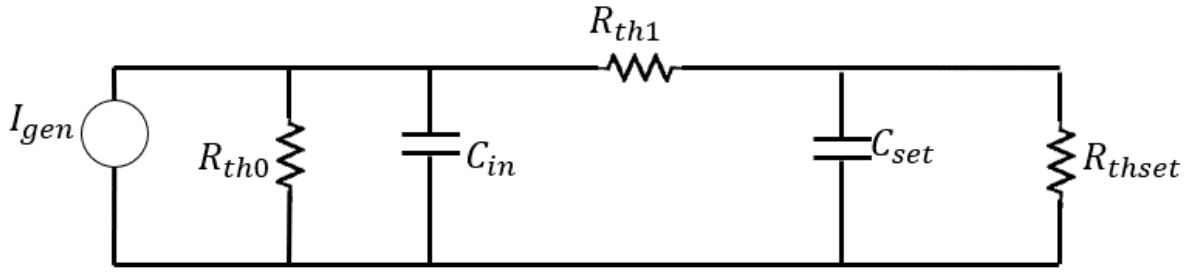

Figure1.7: Equivalent electrical circuit of the sensor used.

Another sensor from newer generation of humidity sensor is used for the primary measurements, it has parameters as follows:

- R_{heater} = 240Ω;
- R_{thermo}= 2.5KΩ

Figure 1.8 and Figure 1.9 show the results of the 5V and 7V power supply at the open loop environment. From the comparison with Figure 1.4 it can be noticed that the Δt obtainable by supplying 5V (11 °C) is slightly higher than that obtained with 10V (10 °C). The power provided in Figure1.4 is around 156mW, while Figure 1.8 is around 104mW. The higher ΔT (with lower power supplied) can be explained by the decrease happen in thermal resistance R_{tho} due to technology-size reductions (despite the increase due to the physical separation between heater and thermometer). The temperature curve in Figure 1.8 and Figure 1.9 is faster to reach the desired temperature because of the reduction in thermal capacity (again for the lower dimensions of the technology). The time constant is calculated by tracing the tangent after about 1s, so that after 5τ the temperature response is sufficiently close to the system. Therefore, in this case, the exponential approximation is worse. The difference between the two-time constants in the two figures is due to measurement error. The two values should obviously coincide in theory.

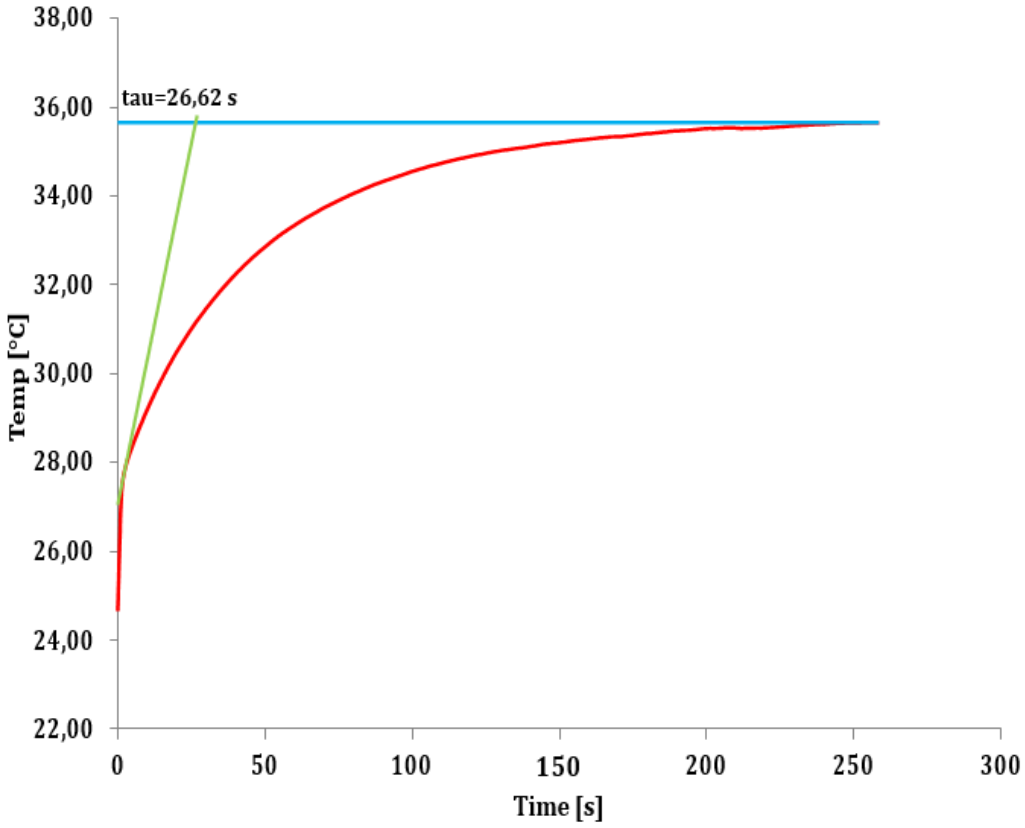

Figure1.8: temperature response of the sensor at 5V power supply

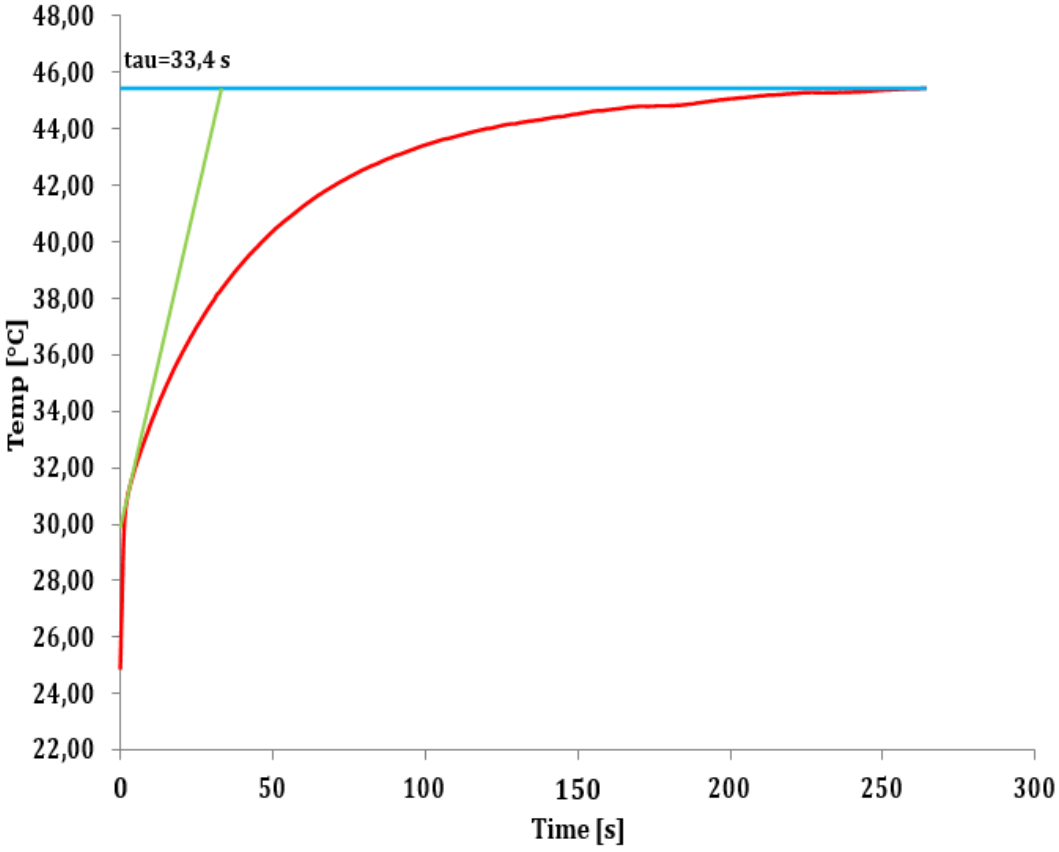

Figure 1.9: temperature response of the sensor at 7V power supply

1.5.3 Temperature control

The sensor temperature control involves selecting a temperature setpoint, where for measuring the temperature in the thermometer means a measurement of the resistance value depending on the relation stated in equation 1.9. The presence of a control loop which modulates the power supply to the heater in such a way as to add a value to the equality $T_{setpoint} = T_{measured}$. The control loop is presented in Figure 1.10, where $T_{setpoint}$ and $T_{measured}$ are respectively the setpoint temperature selected and the temperature read by the thermometer, R(s) is the temperature regulator, G(s) is the process object of adjustment where the transfer function of the equivalent circuit of the sensor is mentioned before. "e" is the instant error given by the difference between $T_{setpoint}$ and $T_{measured}$. "u" is the is the output signal from the controller; this is a voltage signal that forces the power supply to a value equal to the result of the controller calculation. Finally, there is a saturation block (SAT). In fact, a maximum limit on the power supply will be imposed which in fact simulates a saturation of the sensor. The block diagram has the following condition for working:

- m = u if $0 \leq u \leq L$
- m = L if $u \geq L$
- m = 0 if $u \leq 0$

In this first step, the control loop will be designed in a way as to have the maximum possible precision at the control system. At the end of the chapter, the necessary precision will be studied to have the regulator in the integrated circuit to limit the RH error within the prescribed limits.

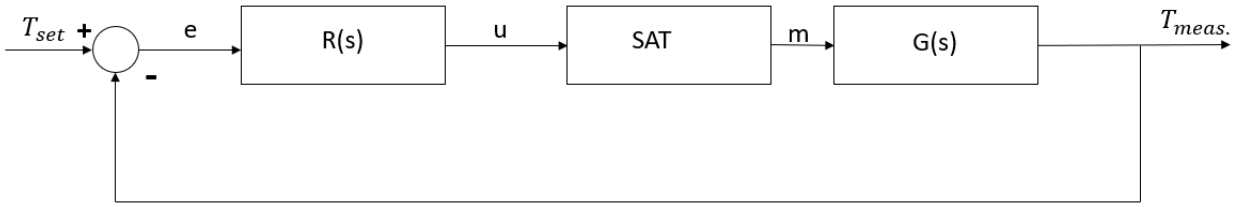

Figure 1.10: control loop

It's important to consider that the system require a high accuracy and high velocity time response. An accurate precision is critical requirement to guarantee an accurate RH measurement. The time response velocity is also important because, in the self-diagnostic and recalibration phase, the assumption is that the ambient conditions around the sensor (T and RH) do not change during the sweep temperature imposed by the heater.

It is worth considering that the search for a rapid response to the system will affect the precision of the system or even the stability of the system. So, the control of the system will nevertheless be that the preferred precision of the software controller.

Regarding the type of regulation, given the impossibility of knowing in detail the process transfer function (the values of the equivalent circuit components in Figure 1.7), the best choice is the PID regulator. This choice is also dictated by the simplicity of implementation at the integrated circuit level.

1.6 PID Controllers

PID controllers or proportional, integral and derivative regulators are widely used linear regulators that allow control many types of different processes [8]. The advantage they offer is the ability to control a system without having a precise mathematical model of the system itself or, without knowing its parameters. They can also be implemented through the most varied technologies:

• mechanics;

• pneumatic;

• hydraulic;

• digital and analog electronics.

The control law expressing the relation between error (e) and control variable (u) as the difference between a desired setpoint and a measured process variable and applies a correction during certain time is:

$$u(t) = K_p\, e(t) + K_I \int_{t_0}^{t} e(\tau)\, d\tau + k_D \frac{de(t)}{dt}$$

where k_p , $K_{I,}$, K_D are the coefficients of proportional, integral, and derivative respectively.

Applying the Laplace Transform at t_0= 0 you get the ideal shape of the PID controllers

$$R(s) = K_p + \frac{K_I}{S} + K_D s \qquad (1.12)$$

An alternative form is given by the introduction of integral time (T_I) and derivative time (T_D) will be defined as:

$$T_I = \frac{K_p}{K_I}, \qquad T_D = \frac{K_D}{K_P}$$

$$R(s) = K_p(1 + \frac{1}{T_I S} + T_D s) = K_p \frac{T_1 T_D s^2 + T_1 + 1}{T_1 s}$$

The ideal PID transfer function for an improper system should have number of zeros greater than the number of poles. For the applicability of the controller, in practice, a high-frequency pole is added. The derivative transaction transfer function becomes of the $R_D(s) = \frac{K_p T_p s}{1+\frac{T_p}{N}s}$.

The values of N are usually within a range 5-20.

1.6.1 Definition of the three terms of the controller

For the interpretation of the meaning of proportional, integral and derivative parameters, reference can be made to equation (1.12).

K_p proportional gain works on the actual value of the error. A low value slows down dynamics, while a high value increases, but it could put the system in non-stable case. In this case, the value of K_p will be chosen in such a way that it has a sufficiently high-speed response that does not create oscillations.

The only presence of K_p is not enough to ensure precision. In general, there will always be an offset that decreases by increasing the value of K_p but is eliminated only if K_p tends to infinity. However, as said before, increasing excessively K_p generates oscillations.

The integral term (K_I), which, as is often explained as working on the past history of the error, guarantees the cancellation of the setpoint error. K_I's value is once again works in determining the speed at which the system will run. A high value will increase the importance of integral action. By increasing K_I (or equivalently by reducing T), the error integral will increase faster by ensuring that the setpoint value is reached in less time. A too high value increases the oscillations again. The choice of the two K_P and K_I parameters should therefore be appropriately coordinated. The sum of the two proportional and integral actions must ensure a quick and precise response.

The derivative term (K_D) is proportional to the rate of variation in error. Therefore, it is possible to reduce the time response and eliminate any significant oscillations around the setpoint value. However, raising the value of K_D is likely to make the system unstable. It is also known that; the derivative term in the system is sensitive to the variations in the error

happen by the noise and therefore its introduction into the control should also be evaluated according to the measurement conditions.

Before introducing the derivative term in the control, it is necessary to evaluate the possibility of achieving the required performance with a PI (proportional-integral) controller. Most industrial controller are of this type. Based on the results obtained, decide whether or not to introduce TD.

1.6.2 Temperature implementation in PID controller

The operation of the temperature control has been explained before need to apply in PID controller used by the Lab-VIEW software to solve typical issues related to PID control. Reference is made to:

1. Mode of discrete of integral term;

2. Limitation of derivative term;

3. Non-saturation of integral term.

The discretization of integral term uses approximation according to this equation:

$$u_I(K) = u_I\ (K-1) + \frac{K_P}{T_I}\ \frac{e(K)+e(K-1)}{2}\Delta t$$

where:

- Δt is the sampling time;
- k is the sampling index that corresponds to time t = kΔT;
- $u_I(K)$, $u_I\ (K-1) +$ are the result of the calculation of the regulator for k and k - 1 indices
- e(k) and e (k - 1) are the error values for k and (k – 1).

The limitation of the derivative term follows the typical scheme used in the previous explanation that is intended to use as the input of the derivative the controlled variable rather than the error. This prevents the output of the derivative and therefore the overall control variables have an irregular trend in the case of a step change in the setpoint. The mathematical expression that defines the derivative action using the finite differences is as follows

$$u_D(K) = -K_P\ \frac{T_P}{\Delta t}\ \ (y(k) - y(K-1))$$

where y(k) and y (k - 1) are in this case the measured temperatures.

Lastly, the last point to be analyzed is the integral windup. When a substantial change in setpoint, the integral term can accumulate an error larger than the maximal value for the regulation variable (windup), thus the system overshoots and continues to increase until this accumulated error is unwound. If the error remains of the same sign for a certain time, the integral output of the controller increases in value (however, the saturation limit value is

supplied to the process). The solution adopted is a correction of the integral sum algorithm according to this relation:

$$\text{If } u_p(K) + u_I(K) > SAT \text{ then } u_I(K) = \text{SAT} - u_p(K)$$

1.6.3 Calibration and Adjustment of PID controller

Calibration of PID controllers is usually done by means of automatic methods that are valid for most processes, which provide for testing in open loop or closed loop directly on the system to be controlled. In this case, considering the possibility of rendering the system unstable for a short time without damaging it, the Ziegler and Nichols Methods were used in a closed loop.

This method expects to increase K_p gains to bring the system to the non-stability limit until permanent period $\overline{T}$ oscillations are generated. The K_p value for which permanent oscillation is created is called critical gain $\overline{K_p}$.

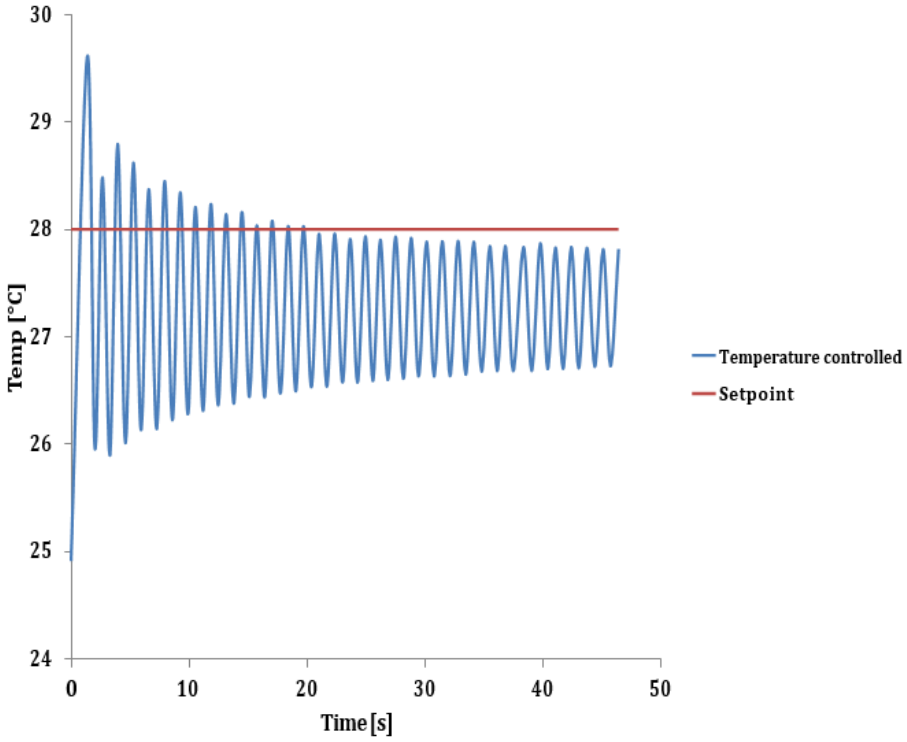

Figure 1.11: Permanent oscillation with $\overline{K_p} = 40$ and Temp. of 28°C

For the system to be controlled in this situation, the critical $\overline{K_p}$ value is 40, while $\overline{T}$ is 1.3s. Figure 1.11 shows the inserting of critical gain causing permanent oscillation.

Then to proceed by setting the other parameters according to the rules in Table 1.1 that assign different values to the gains depending on the type of adjustment.

	K_p	T_I	T_D
P	0.5 $\overline{K_p}$		
PI	0.45 $\overline{K_p}$	0.8 $\bar{T}$	
PID	0.6 $\overline{K_p}$	0.5 $\bar{T}$	0.125 $\bar{T}$

Table 1.1: Ziegler-Nichols step response factors

It is good to initially us a trial and error method to achieve the simplest possible regulator that guarantees the required requirements. for a PI, the results obtained with K_p = 18 and T_I = 1.04s as shown in figure 1.12, where a setpoint of 28 °C was set. It can be noticed that the introduction of integral action guarantees the precision of the system, but the response remains initially oscillating.

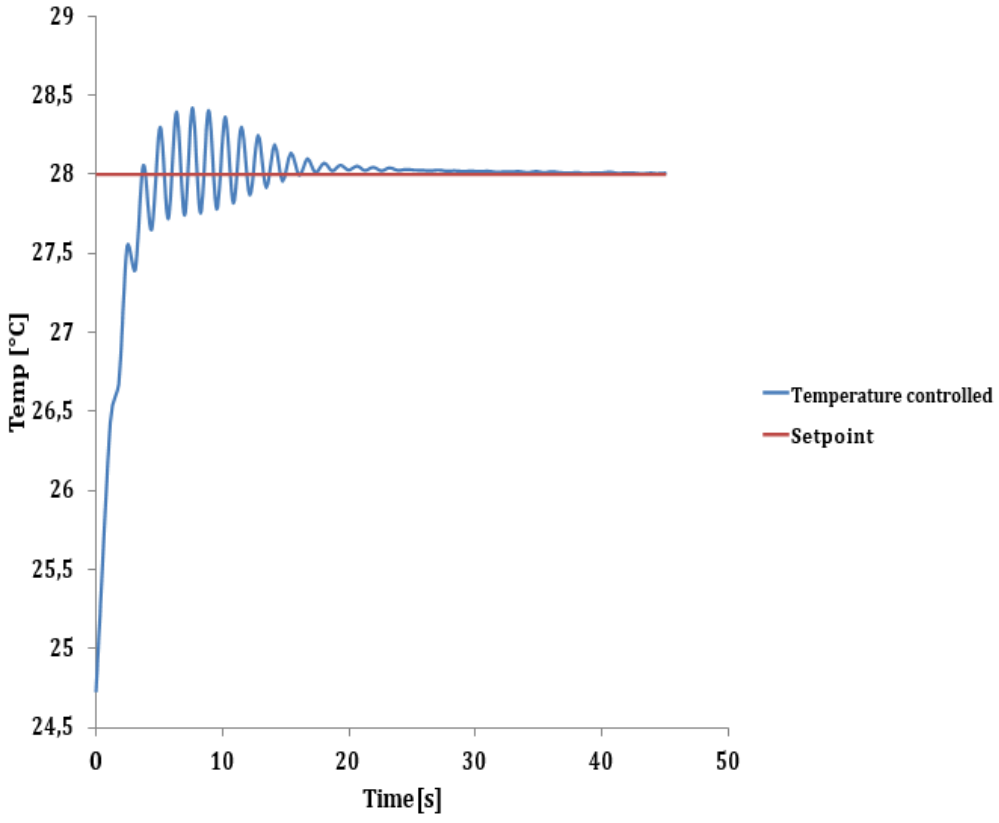

Figure 1.12: PI controller: step response. K_p=18,T_I=1.04s at T=28℃

By complicating the controller structure by adding derivative term according to the Ziegler and Nichols parameters, a worsening of the system response (Figure 1.13) returns to be strongly oscillating. In this case, it's better idea to return to the PI controller and improving the calibration manually. To reduce the oscillations of Figure 1.12, slow system response was required by decreasing proportional and integral gains (K_p and K_I).

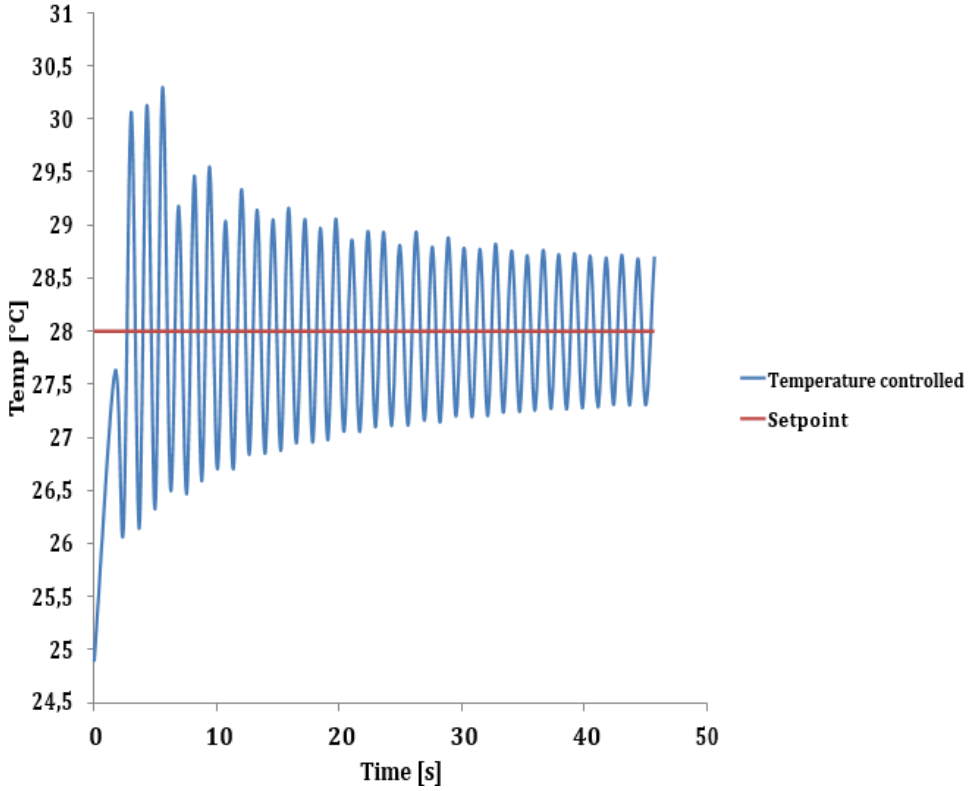

Figure 1.13: PID controller: step response. K_p=24,T_I=0.65s, T_D=0.1625s at T=28℃

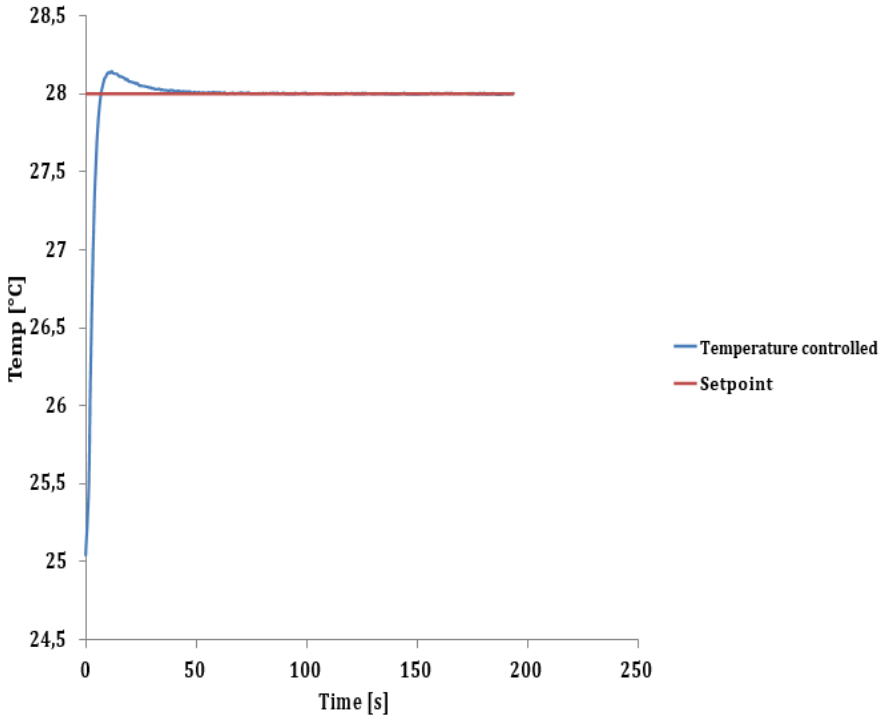

Figure 1.14: PI controller: step response. K_p=10,T_I=1.04s at T=28℃

The definitive PI parameters obtained manually are K_p = 10 and T_I = 1.04 s. Figure 1.14 and Figure 1.15 show the results of the PI control for ΔT of 3°C and 12 °C. The steady-state precision is ±0.005°C. Actually, after 25s in the case of ΔT of 3°C and 45s for the case of 12°C, the set temperature has an error with respect to the setpoint of +0.05°C.

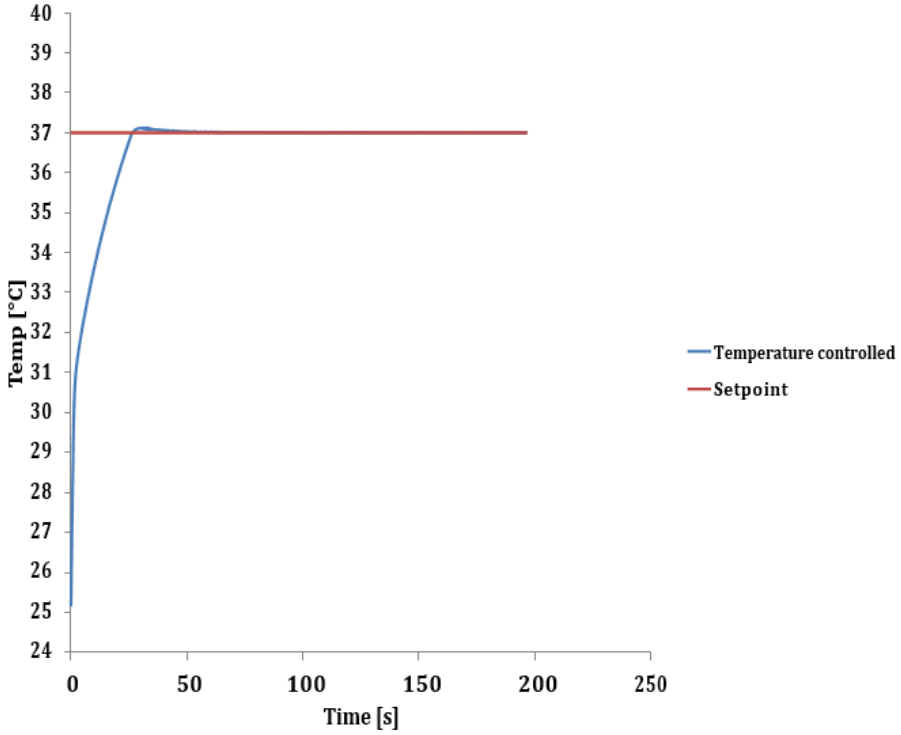

Figure 1.15: PI controller: step response. K_p=10,T_I=1.04s at T=37℃

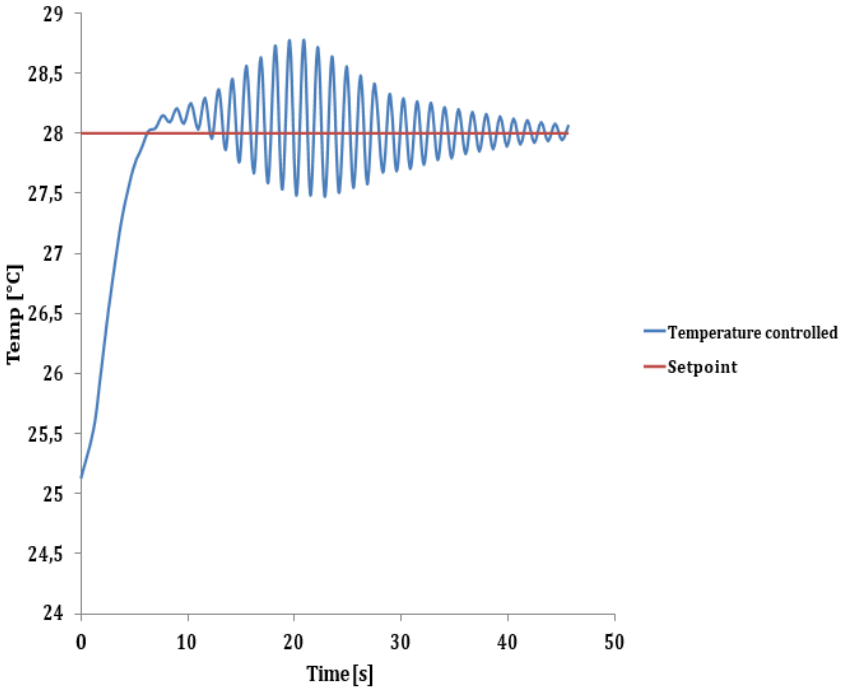

Figure 1.16: PID controller: step response. K_p=10,T_I=1,04s, T_D=0.5s at T=28℃

There is no need to complicate the control system by introducing the derivative term. For example, it is shown in Figure 1.16 when insert to the system T_D= 0.5s, it gives the worse system response.

1.6.4 Accuracy at regime required for the real controller

From the last explanation, the software controller's precision is ±0.005°C. In the electronic integrated circuit of the controller such a level of precision requires a resolution at least equal to the precision value. The difficulties in achieving so many levels are related to the noise (near-scaled noise ratio) and the linearity in the analog-to-digital conversion. The minimum accuracy required at the real controller is obtained for a relative humidity reading error within acceptable errors. It is assumed that you will not consider other measurement errors and accept a precision at ± 0.5°C. The absolute error on the measuring RH relative to the model given by (1.12) depends on two factors:

- Amplitude of ΔT setup; the absolute error decreases by increasing the temperature scale.
- Value of μ_{H_2O}; where it will depend on the relation between RH -T, therefore the higher the value of μ_{H_2O}, the greater the error in RH.

It is convenient to choose as a starting temperature of 24°C and it is assumed that ΔT is 3°C. In this case, the variation of the absolute error on the RH will then be represented in a graph as in Figure 1.17, where the error of μ_{H_2O} values is existing, so RH is between 10% and 90%. The maximum error reaches ± 2.3%RH. Considering that other types of measurement errors have not yet been considered, this value is not acceptable. While consider the precision of value ± 0.1°C, the results are reported in figure 1.18. In this case, the maximum error is ± 0.45% RH which is acceptable. The accuracy of the real controller must be at least ± 0,1°C. Better precisions will naturally release from self-diagnostic and autocalibration systems.

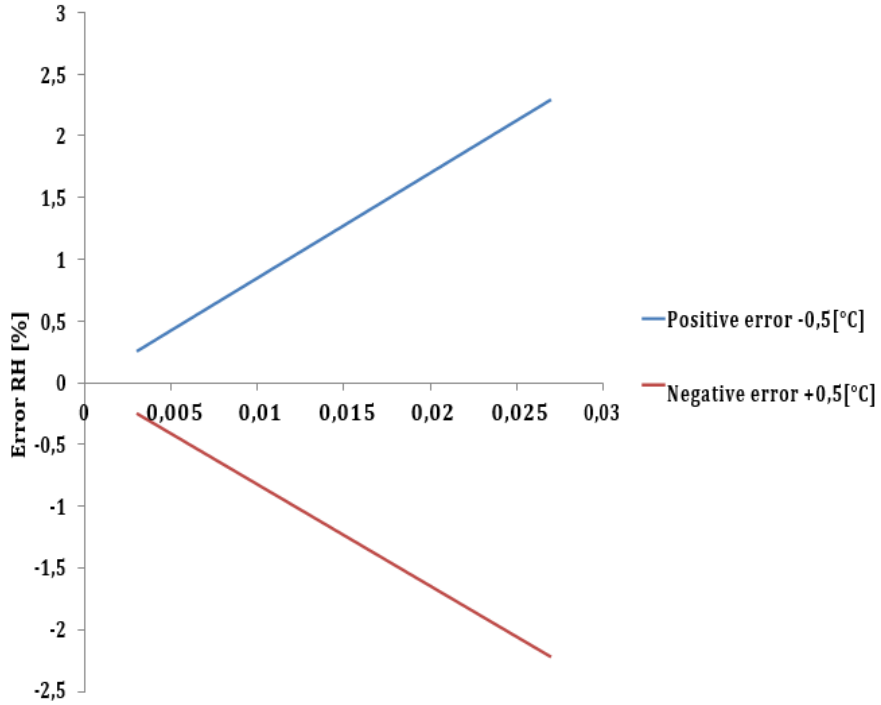

Figure 1.17: RH error with precision of ± 0.5°C in temperature control loop

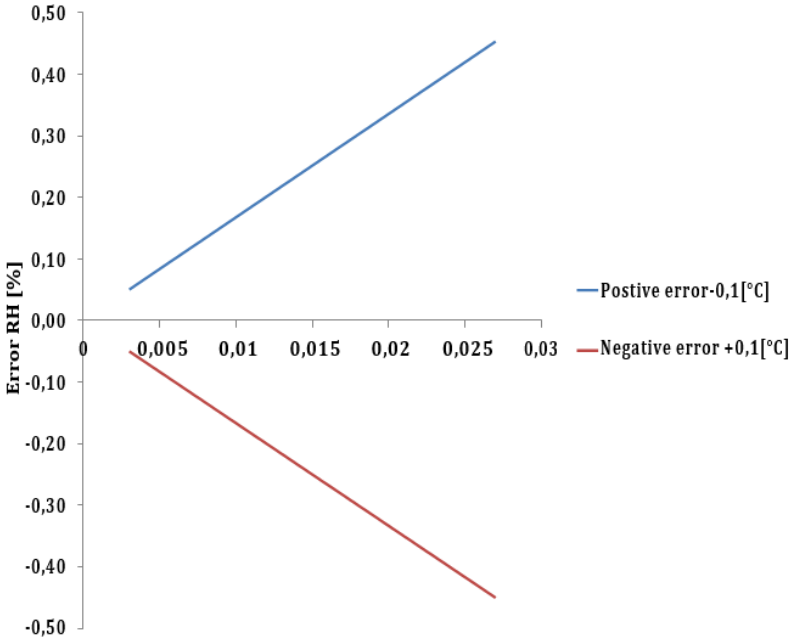

Figure 1.18: RH error with precision of ± 0.1°C in temperature control loop

1.7 Software implementation for temperature controlling

After last explanation of how to choose the best controller technique, the adjustment of the temperature values was produced by PI controller, calibrated according to an PI algorithm mentioned before (Ziegler-Nichols rules). A voltage source is connected to integrated heater (resistance) to provide a certain current, while a digital multi-meter used to read the instantaneous values of the resistor (and hence the temperature) of the sensor. The capacitive of the sensor has been approached through "capacitance-to-digital converter". The detected capacitor values are converted into the corresponding relative humidity values according to the graph of initial calibration of the sensor. The control loop, implemented in LabVIEW model. From Table 1.2, at 3V supply, R_{heater} is around 253Ω at ambient temperature T_0 = 23.1°C

V[V]	T [℃]	T_o [℃]	V^2	R*heater* [Ω]	Delta (T)	P [Watt]
1	23.765	23.306	1	250.4131	0.459	0.003993
2	25.107	23.196	4	251.7199	1.911	0.015891
3	27.336	23.145	9	253.7719	4.191	0.035465
4	30.44	23.193	16	256.5223	7.247	0.062373
5	34.76	23.312	25	260.3032	11.448	0.096042
6	40.041	23.492	36	264.8941	16.549	0.135903
7	45.696	23.679	42	269.8153	22.017	0.155662

Table 1.2: Response of the open loop system when the voltage supplied changes.

1.8 Overall system design for temperature controlling

The importance of controlling the temperature comes from the fact that the sensor response is strongly temperature dependent. A good stability would lead to higher sensor accuracy with strong reduction of drift effect. The design proposed has a self-calibration technique capable of periodically update the calibration coefficient to improve the performance and reliability of the sensor. Temperature control loop is required with embedded heater R_{heater} 250Ω (From primary measurements) and sensing resistance R_{thermo}= 2.5kΩ. Using 0.35µm CMOS technology, the temperature control loop shown in Figure 1.19 is implemented in the analogue domain, using a trans linear MOS geometric mean circuit, where the control loop is driven by a PI (proportional-Integral) controller with parameters K_p=10, T_I =1.04s. Gain and integrator op-amp are realized using switched-capacitor (SC) techniques, driven by two non-overlapped clock phases: ϕ1 and ϕ2 with a frequency of 100Hz. The integrator op-amp is followed by a comparator whose output is connected to a power n-MOS featuring W = 1000 µm and L = 0.4 µm which delivers the required current to R_{heater}.

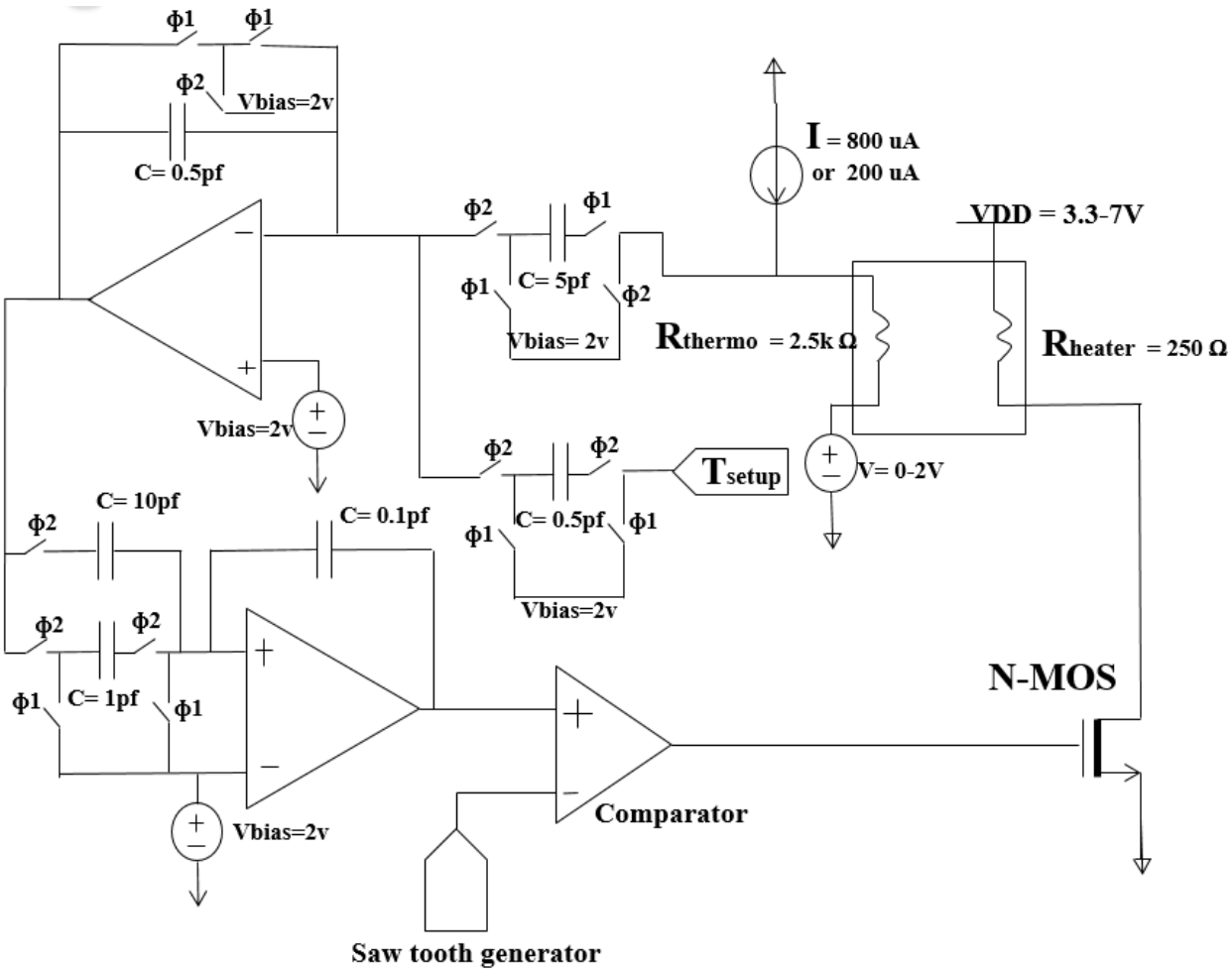

Figure 1.19: Temperature control system schematic architecture

The thermal coupling inside the sensor between R_{heater} and R_{thermo} resistors has been modeled in VerilogA for transistor level system simulations. The first one has a terminal

connected to the power n-MOS to regulate the temperature, while the other terminal is connected to an external voltage supply varies 3.3V to 7V depending on the range of temperature. The temperature signal from the second resistor (2.5kΩ) biased by a programmable current generator is converted into a voltage and amplified by a factor of 10 by a first SC stage.

In particular, the bias current 800 µA is used with the bias voltage of 0V in the range 24-27℃. The bias current of 200 µA is used with 2V bias volts in the range 27-34℃. For higher temperatures, the current will go further down (ex. 100 µA). The wavelength of the saw tooth to the inverting input of the comparator is 1 MHz and The loop gain is 1000.

The circuit exploits an operational amplifier in closed loop configuration which connected through the comparator directly to micro sensors having separated heater-thermometer. the source degenerated power transistor N-MOS delivers the demanded power to the heater (R_{heater}) which regulating its current. Temperature is again read-out through a resistance that operates as a thermometer. By operating the heater at constant power or by turning it off it is possible to control the sensor temperature without interferences. The current (or more generally) the power delivered to the heater resistance must be such that the temperature should remain constant at its desired value. The value of the thermometer resistance is calculated using the joule effect. The resistor- temperature relation is as follow:

$$R_{thermo} = R_{thermo_0}(1 + \propto \Delta T)$$

Where $R_{thermo_0} = 2.5K\Omega$, $\propto = 3.6 \times 10^{-3}$, ΔT = $T_{setup} - T_0$, $T_0 = 23.3$℃

The voltage across the R_{thermo} is calculated by $V_{thermo} = R_{thermo} \times I_{bias}$

Where I_{bias} has 2 different values, either 200µA or 800µA depends on the temperature range needed. The voltage will be amplified by 10 then passing by the integral op-amp to be compared to sawtooth wave by the comparator whose output supply the n-MOS which deliver current to the R_{heater} until reaching the desire setup value.

1.9 Circuit design

1.9.1 Operational amplifier

The implemented amplifier, shown in Figure 1.20, is a two-stage structure with Miller compensation. The current flowing through the second stage ensures a good driving capability and hence it is not necessary to implement a source follower output stage. In fact, the output impedance thanks also to the feedback is low enough. The gain of this amplifier is around 60dB, while the unity-gain bandwidth is of the order of 100kHz with 4.5pF compensation capacitance and up to 1pF output load.

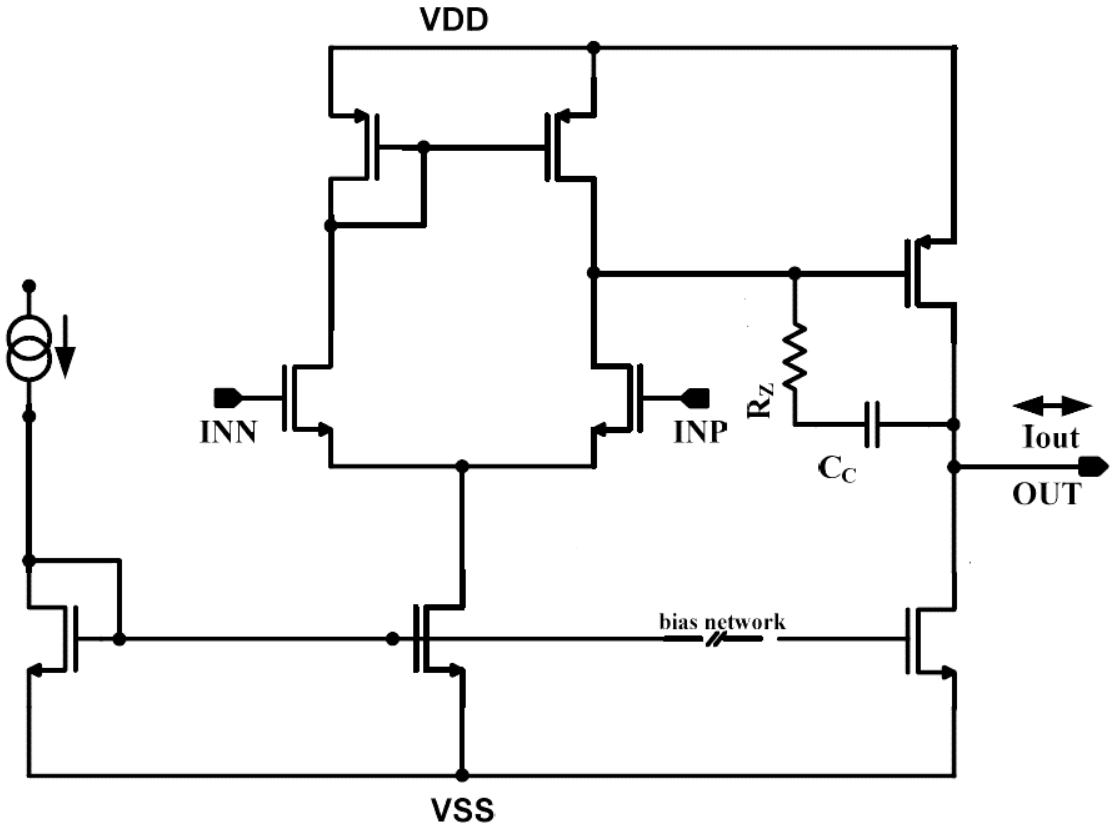

Figure 1.20: Operational amplifier schematic

1.9.2 Comparator

The schematic diagram of the voltage comparator used is shown in Figure 1.22. We added transistors M10 and M11 to obtain a positive feedback loop, which boosts the response time and avoid metastability. These two transistors are also used to introduce a small hysteresis. The output current of the comparator is given by:

$$I_{out} = \frac{g_{mM2}.(\frac{W_6}{L_6})}{V_{in}.(\frac{W_4}{L_4})}$$

The voltage gain is given by:

$$\frac{V_{out}}{V_{in}} = R_{out}.I_{out} = \frac{(r_{ds7} // r_{ds6}).g_{mM2}.(\frac{W_6}{L_6})}{(\frac{W_4}{L_4})}$$

By applying the voltage threshold V_{thr} at the gate of M1, and V_{in} at the gate of M2. When $V_{in} < V_{thr}$, M1 is ON while M2 is OFF. In this case, M3 and M10 are turned ON, While M4 and M11 are turned OFF.

The current of M5 flows through M1 and M3, and the drain voltage of M4 is close to V_{dd}, thus pushing V_{out} to be close to ground. When $V_{in} > V_{thr}$, the current of M5 starts to flow through M2 until it equalizes the current flowing in M10. At this moment, the output of the comparator changes. The current flows through M2 and M4, thus causing M11 to be turned ON while M3 and M11 are OFF.

To enhance the circuit performances, an output stage (M6 and M7) and two inverters have been added, obtaining sharp output transitions. The same architecture may also be thought as a composition of current mirrors, where the current drawn by M6 and/or M7 generates V_{out} by means of the output drain resistance of such transistors.

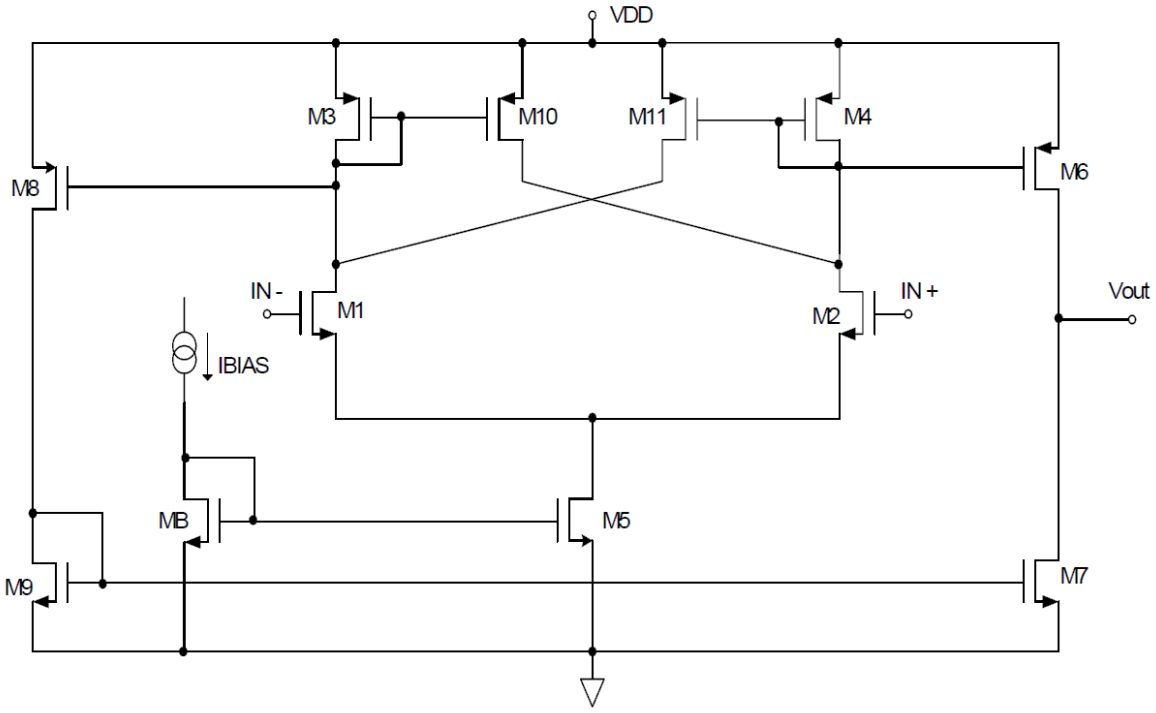

Figure 1.21: Comparator schematic diagram

1.10 Simulation results

The system was simulated in Cadence environment at transistor level. The achieved accuracy is in order of 0,005 ℃ in a temperature range of 50℃ as shown in Figure 1.22.

Figure 1.23 shows the layout of the core chip realized in 0,35µm CMOS technology with 24 pins. The chip area is 0.25 μm^2. 21 pins are used. The chip die microphotograph is shown in Figure 1.24

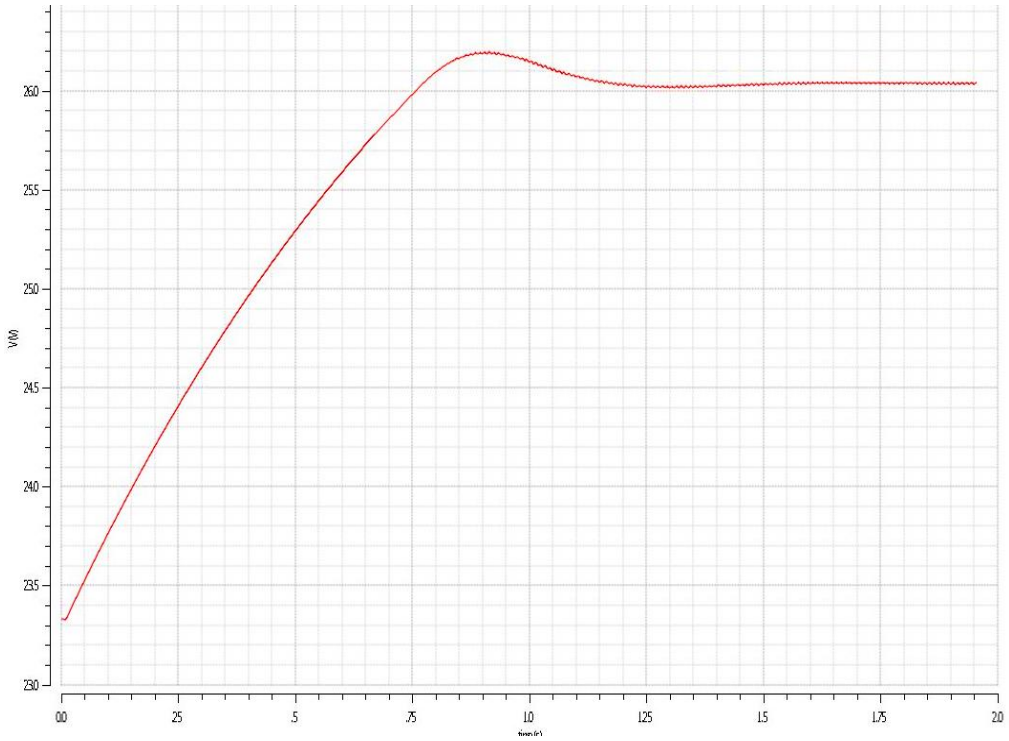

Figure 1.22: time response in cadence simulation at T = 26℃.

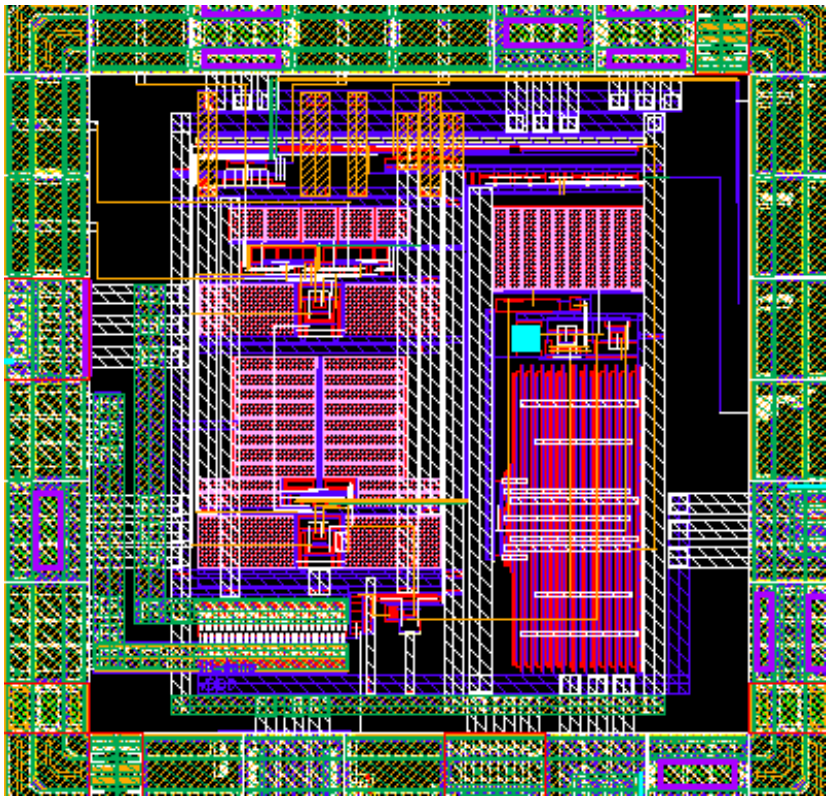

Figure 1.23: Temperature control system core layout

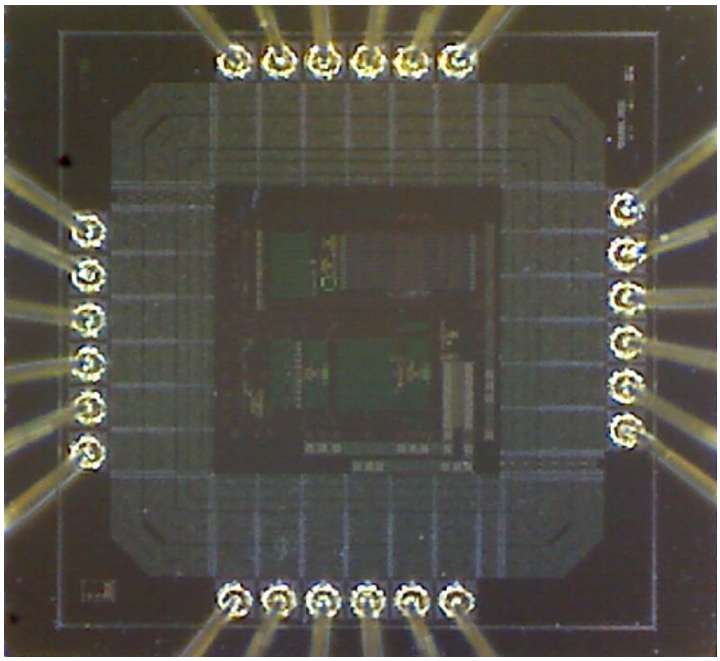

Figure 1.24: Chip die microphotograph.

1.11 Measurement Results

The read-out circuit has been fabricated in a 0.35µm, 3.3V supply CMOS technology. Figure 1.25 shows the photograph of the chip core with 24 I/O pins including auxiliary supplies for pad protections and buffers Due to typical platinum fabrication material of humidity sensors embedded heaters-thermometers, preliminary measurements may be carried out by using an equivalent PT2500 resistor, i.e. a platinum resistor (temperature coefficient $\alpha=3.927°mC^{-1}$) featuring 2.5kΩ at 0°C thermally insulated together with a 0.5W power transistor featuring 250Ω at ambient temperature (25°C). The measurements are divided into two set groups. The ones carried out with the internal NMOS supplied at 3.3V for a typical temperature range of [25°C – 30°C] and the ones performed using the external discrete power MOS to drive the sensor heater for a typical temperature range of [30°C – 50°C].

The measurement setup, shown in Figure 1.26, consists in a universal signals source, a clock generator, Two DC voltage generators, an oscilloscope, and digital multimeter. The universal source supplies the bias current, the clock generator gives the clock square wave of 100Hz. Two DC voltage supply generators provide the 3.3V for VDD and or 10Vor 3.3V (Depend on the range) for the heating resistance supply. Also, 2V for the bias reference voltage. The digital multimeter used to measure the thermometer resistor value which is proportional to the temperature value. The oscilloscope is used to display the output digital signal from the comparator. A breadboard is used to connect the chip to the lab instruments for implement the measurements. Figure 1.27, shows the test-bench used to test the chip including all the instruments mentioned before.

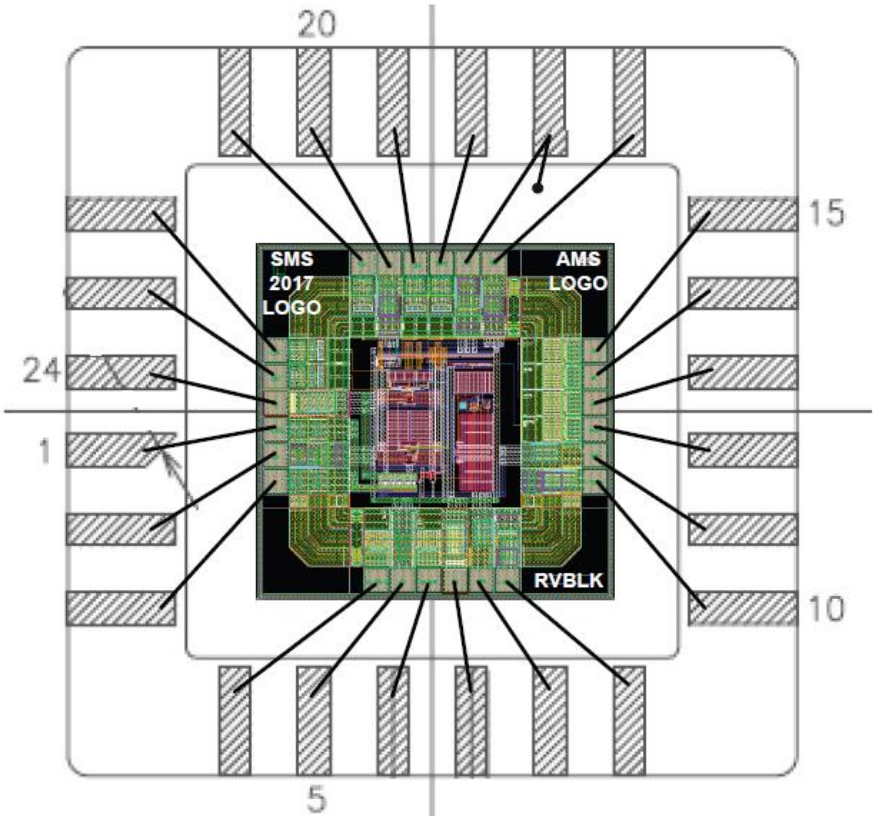

Figure 1.25: Temperature control system layout

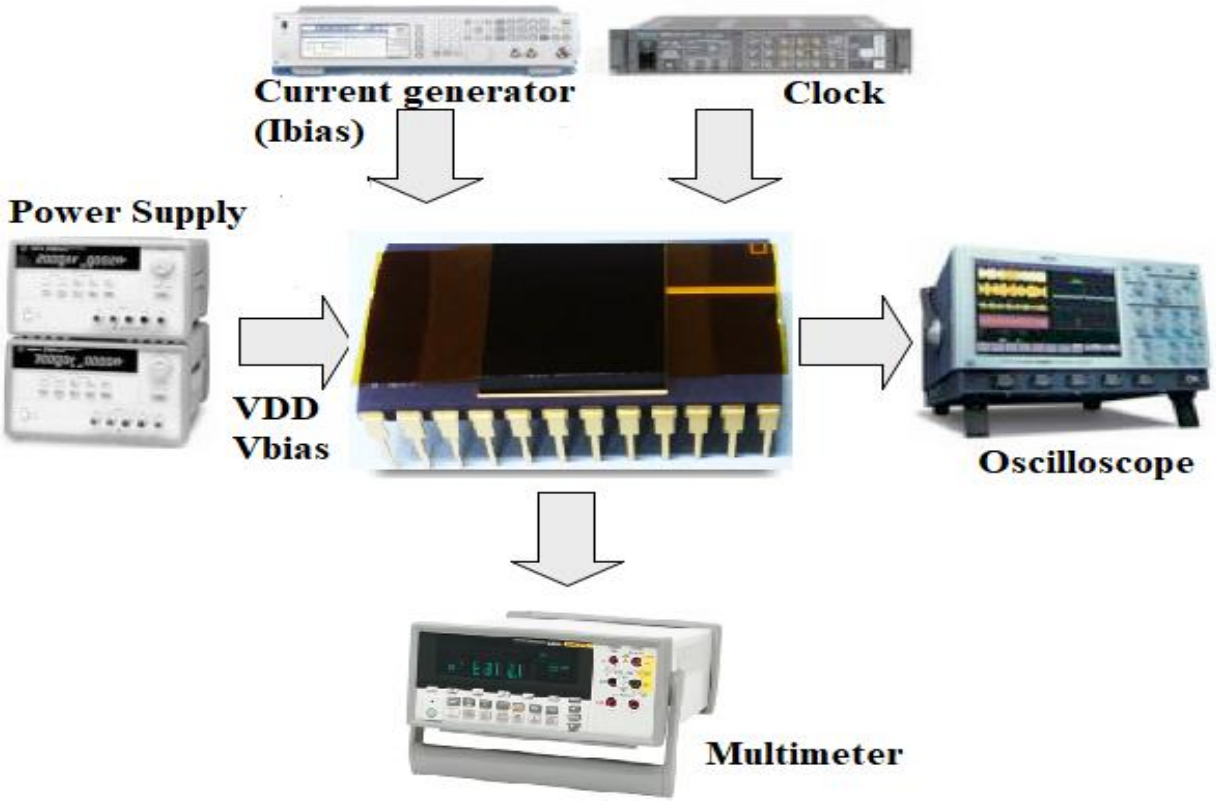

Figure 1.26: Measurements setup

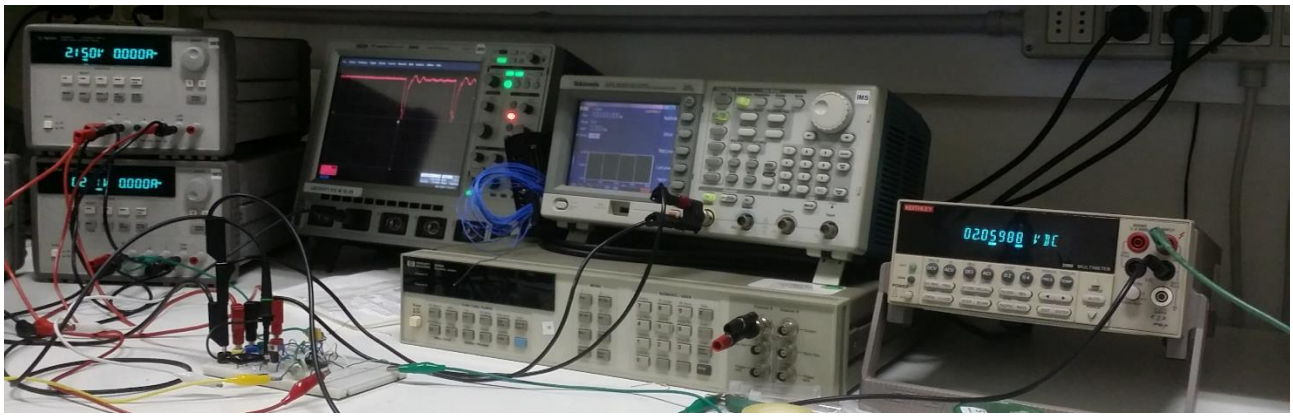

Figure 1.27: A Photograph of the test-bench measurements set-up.

The first measurement set is for the range of internal nMOS supplied with 3.3V, biased by 766.2µA using the current generator designed inside the chip and 2.15V voltage bias. A PT2500 resistor is used as thermometer and 250Ω resistor is connected to the internal nMOS for heating according to the set-point temperature. The measurements reported in Table1.3 have been carried-out by changing the setpoint and measure the PT2500 value which is equivalent to the desired temperature. Figure 1.28 shows a graph of the variation in measurement with different set-point.

Set Point (°C)	**Temp. Measured(°C)**
26.2383	*26,2025*
26.511	*26,4684*
26.7837	*26,7476*
27.0563	*27,0666*
27.329	*27,3591*
27.6017	*27,5851*
27.8744	*27,9041*
28.147	*28,2099*
28.4197	*28,4359*
28.6924	*28,7417*
28.965	*28,9943*
29.2377	*29,2735*
29.5104	*29,5127*
29.783	*29,7520*
30.0557	*29,9515*
48.4785	*48.4836*

Table 1.3: Measurements for the range from [27°C – 30°C]

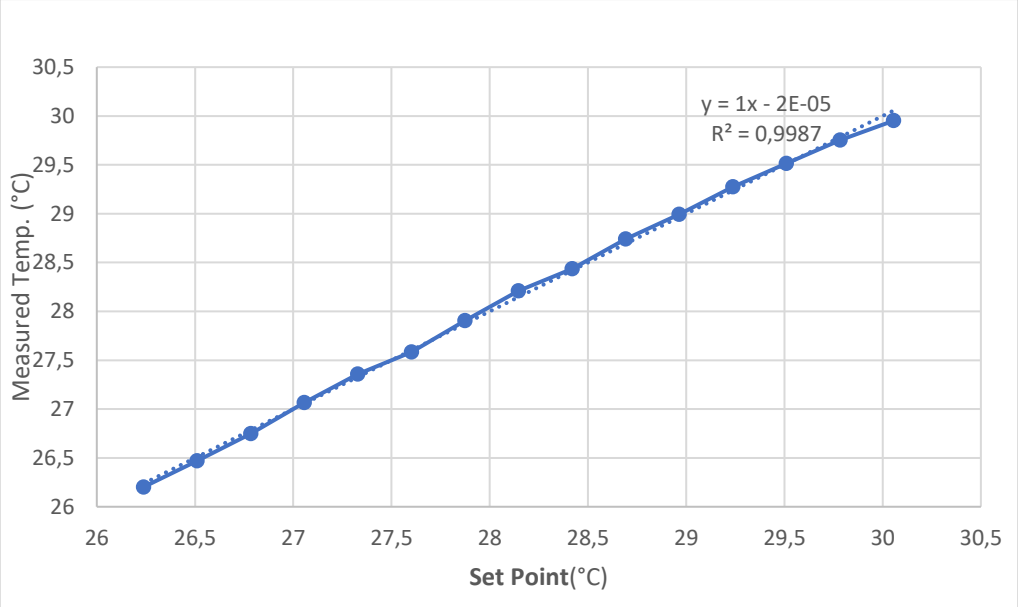

Figure 1.28: Measurements for the range from [27°C – 30°C]

The second set of measurements is performed using a high base input resistance NPN BDX53C Darlington BJT supplied at 10V to drive the sensor heater for a typical temperature range of [30°C – 50°C]. biased by 200μA and 2.11V voltage bias. A PT2500 resistor is used again as thermometer and 250Ω resistor is connected to the external Darlington BJT for heating according to the set-point temperature. The measurements reported in Table1.4 have been carried-out by changing the setpoint and measure the PT2500 value which is equivalent to the desired temperature. Figure 1.29 shows a graph of the variation in measurement with different set-point.

Set Point (°C)	**Temp. Measured(°C)**
32.8965	*33.1462*
34.0095	*33.8596*
35.1225	*35.0315*
36.2355	*36.1016*
37.3485	*37.2735*
38.4615	*38.4964*
39.5745	*39.6175*
40.6875	*40.6875*
41.8005	*41.8085*
42.9135	*43.0314*
44.0265	*44.1524*
45.1395	*45.1715*

46.2525	***46.2926***
47.3655	*47.1588*
48.4785	*48.4836*

Table 1.4: Measurements for the range from [30°C – 50°C]

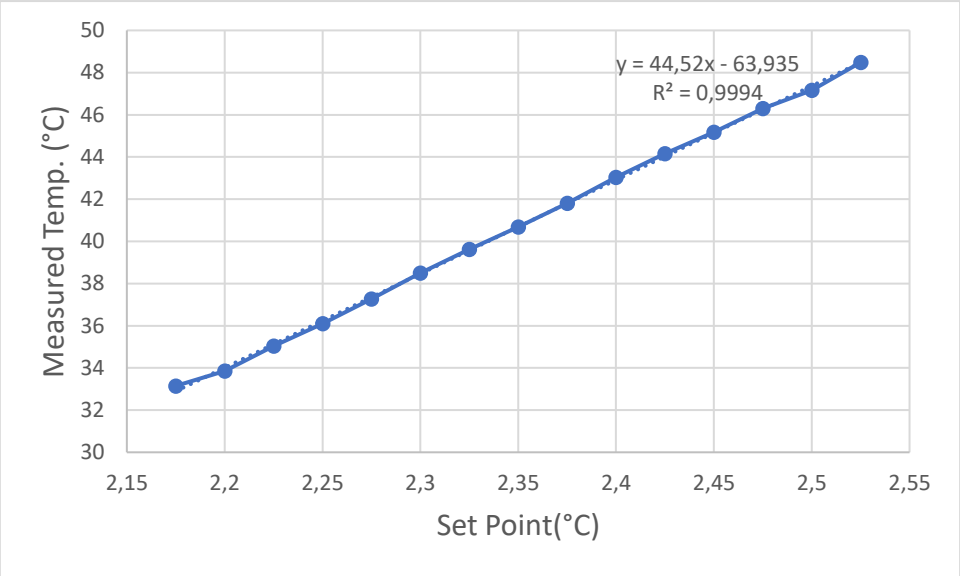

Figure 1.29: Measurements for the range from [30°C – 50°C]

The measurements that have been reported here have been carried out in MATLAB routine that calculate the temperature ripple accuracy for each set range of temperature according to the date set of measurements achieved. Figure 1.30 and Figure 1.31 show the system response from MATLAB code calculation where temperature ripple in measurements is <0.2°C peak, while closed loop system accuracy in temperature synthesis is 0.11°C while using 3.3V supplied heater power MOS and 0.25°C exploiting the external driver.

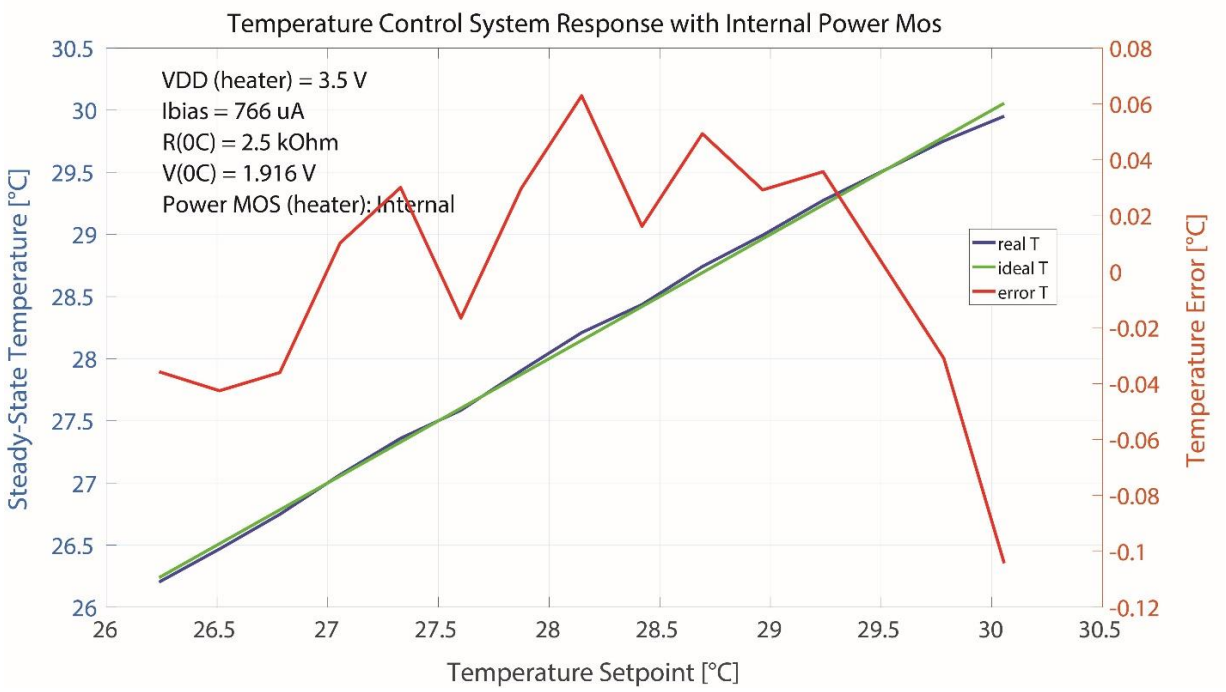

Figure 1.30: System response (internal 3.3V power MOS)

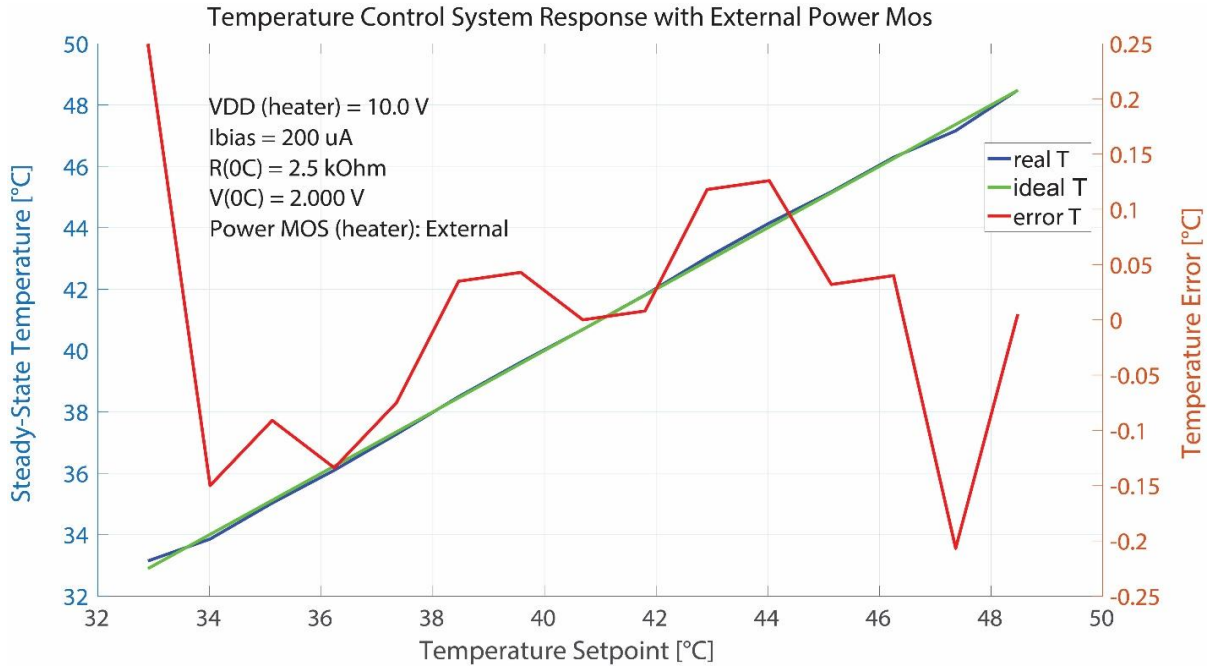

Figure 1.31: System response (external power device)

1.12 State of Art

In comparison with other temperature control systems for a same kind of sensors, Table 1.5 reports the achieved resolution presented in thesis and in other papers reported in literature.

	This work	[9]	[10]
Linearity	99.91%	99.6%	99.394%
Ripple Error	0.11˚C	0.75˚C	-

In [9], a temperature control interface with digital I/O for a gas sensing system is presented, where the temperature control system has heater and thermometer based on two platinum-titanium resistors embedded in the sensor. The power consumption of the control circuit is about 9.5mW at the steady state sensor temperature when the set-point is 264 °C in constant dry air flow, i.e. when the gas-sensor has reached the desired temperature and thus the temperature control circuit has only to deliver the average power necessary to keep sensor temperature constant. The ringing around the mean temperature value is about ±0.75 °C and is negligible, since it does not affect the gas-sensing operation. The linearity of the system is good, since the error is always lower than 1.5˚C, as shown in figure 1.32. The achieved precision is better than 1.50% over the entire range at low temperatures.

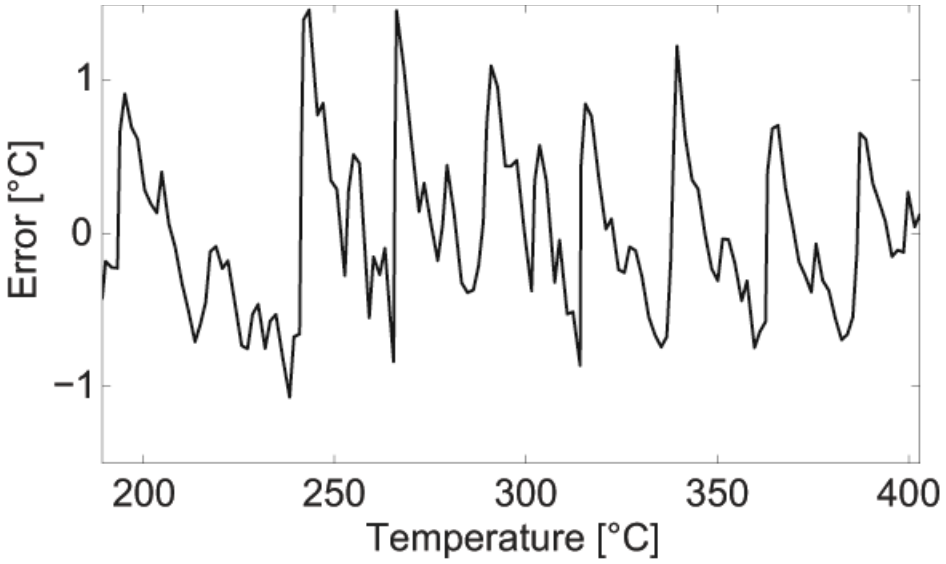

Figure 1.32: Synthesized temperature accuracy.

In [10], a low power capacitive humidity sensor readout IC with on-chip temperature sensor, which is manufactured using a 0.35μm CMOS technology is proposed, where the readout consists of a PTAT temperature sensing circuit. The average power dissipation is a low as about 150μW with one humidity measurement per one second. the minimum detectable

capacitance is as low as about 4.5fF. The total chip size is 1.8 mm by 1.9 mm, output resolution is 14bit for temperature sensor and 12bit for humidity sensor.

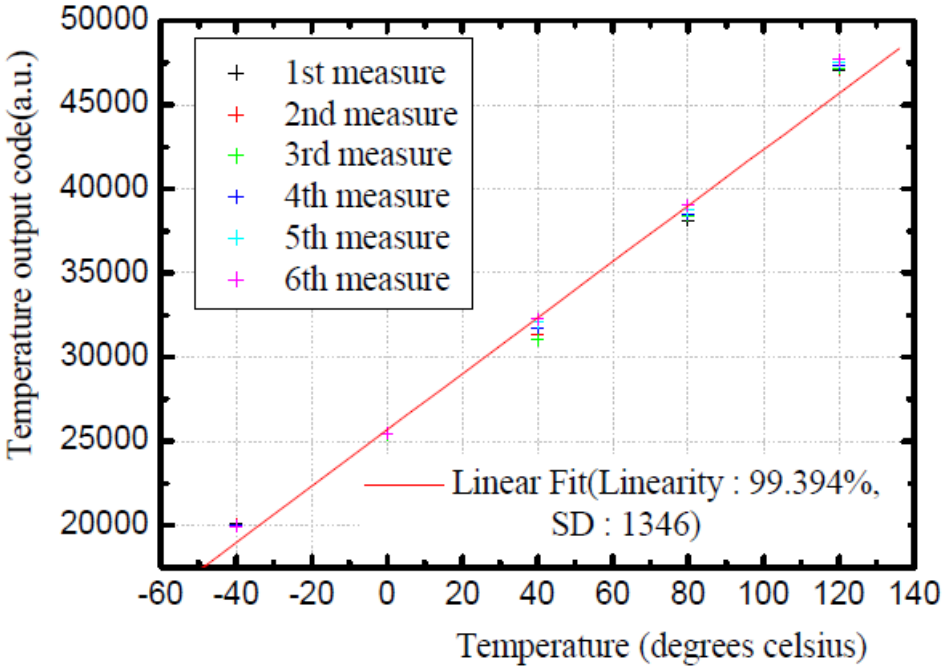

Figure 1.33: Readout of the IC at various temperature.

Figure 1.33 shows the experimental output digital code of the proposed circuit at various temperatures, from -40˚C to 120˚C. The linearity of the data is about 99.394%. In this case the temperature resolution is estimated as about 0.0058˚C at 25˚C.

1.13 Conclusion

The proposed temperature control circuit consists of a constant current thermometer read-out, a voltage amplifier, a PI analog controller and a PWM modulator for the temperature actuator driver. The control loop is implemented with the switched-capacitor technique. The supply voltage is 3.3V, while the maximum current consumption for the control part is 0.9mA, including external thermometer bias current, leading to an internal maximum power dissipation of about 1mW (the remaining 2mW are dissipated by the external thermometer). The maximum current drawn instead by the external heater actuator part is 13mA for maximum duty cycle, but this power contribution is almost all dissipated outside the chip, i.e. into the external connected resistive heater (43mW), whose temperature will range between 20°C and 45°C by regulation through a loop set-point. In fact, the resistance of the output power transistor is about 4Ω against 250Ω of the heater resistance. The heater will be connected to a 3.3V supply with common ground. The circuit is driven by two main clocks: one external and one internal. The external clock drives the switched capacitor architecture

for the control loop and is set at 100Hz, while the internal oscillator is set at 100kHz to generate a sawtooth for the PWM actuator driver.

Finally, it is possible to demonstrate a change in relative humidity controlled by temperature variation. The self-calibration enabled by temperature control strongly improves the performance and reliability of the sensors over time. The temperature control loop implementation in CMOS technology offers high accuracy (better than 0.1°C) and a strong reduction of drift effects. The temperature control of humidity sensors enables many applications, from the simple heating of the sensor in order to treat critical situations such as condensation or accumulation of water, to more complex sensor self-diagnostic systems that allows to figure out the malfunction in humidity reading and sensor self-calibration.

1.14 Bibliography

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Part II

2.1 Introduction

2.2 The Integrated Programmable Capacitor Array

2.3 Primary Experimental results

2.4 Introduction to ADC

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2.8 14-bit extended range incremental A/D

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2.1 Introduction

Microelectronics read-out IC design and advanced micro-systems are key parts for successful High-Energy Physics Experiments (HEPE) [1] [2] [3] and, at the present state-of-the-art, for many other scientific applications in different fields: including space, medical, and industrial applications. For this reason, optimum IC design is required for high-performance, low-power, and low system cost. These results can be achieved with a custom design and performance optimization since different experiments and applications require different specifications in terms, for instance, of radiation hardness, power supply, power consumption, accuracy, die size, and complexity.

In particular, the design of a complex HEPE instrument demands that microelectronics components are designed together with the overall system and in general that an overall global optimization of the full design is performed. This part of thesis thus deals with the optimization of the IC electronics read-out circuits for HEPE experiments in ultra-scaled technology, as they are at the forefront of the technological challenge and targets an optimization of all the possible aspects related to IC technologies.

This work, carried out in the frame of project, SCALTECH28, by investigating the potential useful features of the 28nm technology continues the tradition of other similar studies carried out at previous technology generations for achieving optimal results in IC design for various detectors. This advanced technology, widely used for massive digital consumer electronics, is not fully available yet for analog and mixed signal on-demand ASIC fabrication, but special access has been granted just for specific valued pilot sites. This investigation within the selected 28nm technology had to address basic analysis on the single MOS devices (n-MOS and p-MOS), on passive elements like resistors and capacitors, and finally on basic circuits and system building blocks, among the most critical in different physics experiments. Examples of significant complex circuits for the technology study are: very-low-noise charge amplifiers, ancillary ultra-low-power basic circuit blocks generally used in HEPE circuits, development of a high-accuracy mixed-signal circuit (14-bit A/D converter), and development of high-speed circuits for data transmission.

This activity is focused firstly on the study of matching of passive components in 28nm technology with particular emphasis on Metal-Oxide-Metal capacitors (MoM), by exploiting an integrated capacitance to frequency converter for experimental measurements. Secondly, the design of a low power 14-Bit 1MS/s Extended-Range Incremental ADC in 28nm technology is explained in detail considering the architecture study, the design, and the simulation validation.

Capacitor mismatches are due to variations in oxide thickness between the capacitor plates and variations at the edges of the capacitor plates, Thus, capacitors which have a large area to perimeter ratios will be desirable since they have better matching. Moreover, a better symmetrical layout can prevent the mismatch between the two paths in a fully differential

implementation. In circuits based on the switched-capacitor technique mismatch can cause gain errors and loss of resolution.

In the next section, we will show the results achieved in capacitor mismatch testing on the 28nm CMOS technology, which represent the starting point for the design of a low power Extended-Range Incremental ADC.

2.2 Integrated Programmable Capacitor Array

A typical mixed signal circuit for particle physics experiments is the successive approximation Analog-to-Digital converter (SAR ADC) due to its very low power consumption and robustness [4]. The SAR ADC architecture allows to fully exploit the potential in terms of integration density of scaled technologies, including passive devices, like arrays of Metal-Oxide-Metal (MOM) capacitors. Considering the latest studies by the physics community on the 65nm technology, a good compromise for the data converter would be a resolution of 10 bits with a sampling frequency of 5 MS/s, requiring around 1% matching performance with acceptable calibration complexity or 0.1% matching performance without any correction.

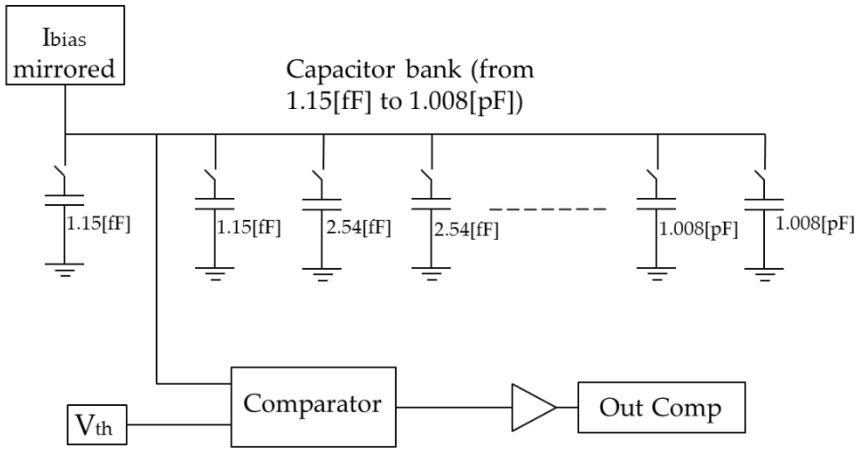

Figure 2.1: Test chip block diagram, including programmable bank capacitor

A specific test structure to emulate a SAR ADC capacitor bank has been integrated on the first test chip for characterizing the passive components before and after an induced radiation damage. Considering that small capacitance values (as low as 10fF) are typically required in a capacitive SAR ADC without range compression, additional embedded circuits must be included for internal probing of such small capacitance.

In the test circuit shown in Figure 2.1, each capacitor of the array may thus be enabled through an analog switch and connected to an oscillator for measuring its value. Furthermore, comparing measurements on large devices (where parasitic are not critical) with measurement of the parallel equivalent value of smaller devices, the effect of internal layout connections parasitics may be extrapolated and cancelled from the main measurements. The realized integrated capacitor bank consists of 10 couples of capacitors of different size, ranging from 1.15 fF to 1.008 pF.

2.3 Capacitance to Frequency Converter

In order to read-out the capacitance value and determine matching accuracy between different capacitors modules without affecting the measurement with external interconnection parasitic, an ad-hoc 1.8V supply analog measurement equipment has been embedded directly in the test chip. It consists of an analog switch in series to every capacitor module of the integrated array driven by a preloaded shift register, and of a constant-current integration-based oscillator [5] [6]. The core of the oscillator is actually made by the capacitor under test on which is conveyed a precise bias current from a high output impedance cascoded current mirror followed by a voltage comparator, which discriminates the voltage across the capacitor against an external voltage threshold V_{th}.

In order to maximize measurement flexibility, both reference bias current and voltage threshold are delivered from an external precision setup. Once the 20-bit shift register is loaded, the capacitors under test are charged by a constant current, which is a mirrored copy of the external reference I_{bias}. Once the comparator determines that the capacitor voltage has reached a value equal to V_{th}, a dedicated switch shorts the capacitor discharging it. Then the process starts over again, leading to a triangular waveform for the voltage across the capacitor and to a pulse waveform at the output of the oscillator core, which is followed by a toggle flip flop, as shown in Figure 2.2, to obtain a square waveform to be delivered off-chip for frequency measurement.

In first approximation, including discharge time (t_d) and comparator delay (t_c), the frequency as a function of the capacitance value under measurement C, including parasitic and toggling, is given by:

$$f_{osc} \frac{0.5}{((\frac{C}{I_{bias}})\cdot V_{th}+t_d+t_c).}$$

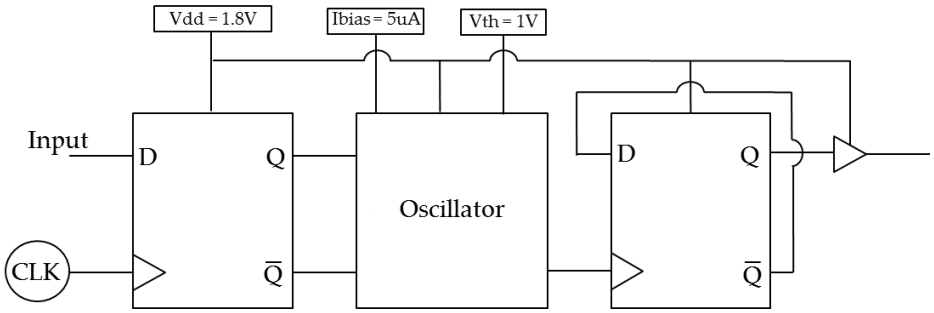

Figure 2.2: Block diagram of the frequency read-out setup (the D-flip-flop represents the shift register)

2.4 Experimental results

The proposed programmable capacitor array bank has been fully characterized in terms of specific capacitance value matching by exploiting the oscillator-based capacitance to frequency converter integrated on the same die in a 28nm silicon prototype occupying a core area of 180µm x 70µm. The microphotograph of the prototype core is shown in figure 2.3.

The worst-case measurement for the capacitor pair matching shows a 0.98% error around 500fF. Table 2.1 shows the detailed values for the capacitance pairs matching ratio in four different cases. The frequency measurements are done between each couple capacitor to get the matching error between them. Capacitance value matching ratio is obtained as an indirect measurement of the oscillator frequency by connecting different capacitors from the programmable array.

Figure 2.3: Silicon prototype (28nm) core photograph.

Mean capacitance pair value	Matching error
106.177 fF	0.71%
210.149 fF	0.72%
501.27 fF	0.98%
1.008 pF	0.57%

Table 2.1: Capacitor-pairs matching measurements

Oscillator output frequency was measured connecting capacitance values starting from 210 fF up to 2 pF. Fitting curves were obtained through at least quadratic polynomial interpolation of the oscillator measured period against the theoretical capacitance value and then compared to actual data to cancel systematic offset and gain error contributions due to constant parasitic layout connections in the chip and error in comparator threshold voltage (V_{th}) estimation. Some matching values were obtained by comparing couples of single capacitor modules in the array, while other values were obtained on groups of different capacitors modules connected together. For instance, a value of 170 fF has been obtained

by the sum of 64fF and 106fF capacitors, a value of 316fF by connecting together to the oscillator a 106fF and a 210fF capacitor, while 712fF by the parallel of 502fF and 210fF.

Measurements were repeated for different oscillator reference current values (I_{bias}): 4.6μA, 5μA, and 5.4μA. As expected by design, the oscillator Period-I_{bias} dependence is almost linear for a given capacitive module. Detailed measurement of the oscillator period versus connected capacitance value and the corresponding fit is reported in Figure 2.44 for all the different I_{bias} values. The described measurement has then been iterated over 15 different chips and 8 different capacitance values with a fixed setup of V_{dd}=1.8V, V_{th} = 1V and I_{bias} = 5μA.

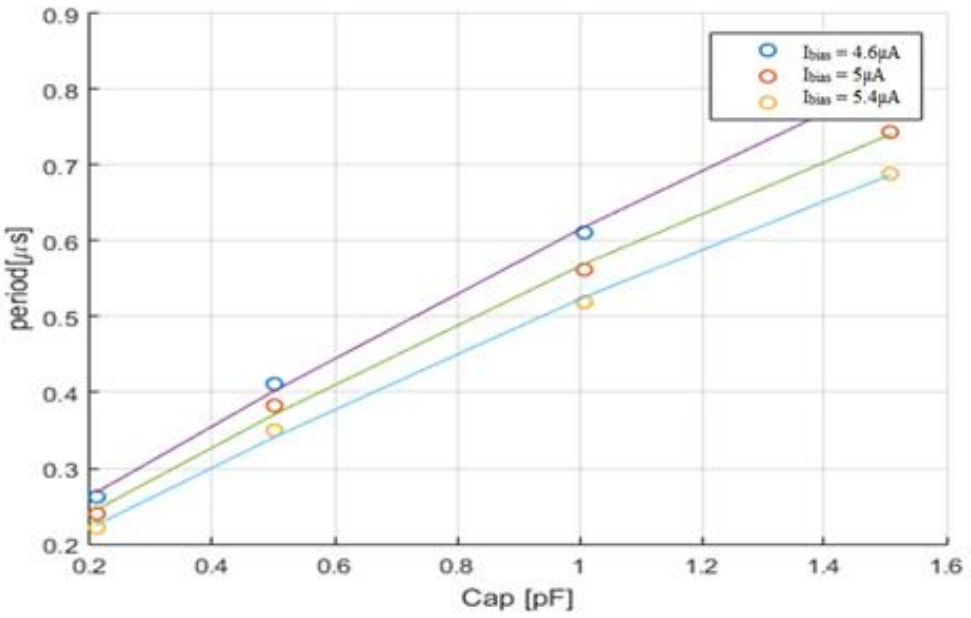

Figure 2.4: Measured oscillator period varying connected capacitance value, for different values of reference current (I_{bias})

In Figure 2.5 the probability density obtained based on the iterated measurements for the different expected frequency values, related to the corresponding connected capacitor modules in the array, is reported. It is clear that the oscillator frequency deviation is quite lower for higher capacitive values (as 2 pF), While for lower capacitance values like 100 fF,

the frequency deviation is greater where in the iterated measurement, sharper probability curves (even if normalized), means lower spread in value, were obtained for lower oscillator frequencies. Finally, in Figure 2.6, the normal Gaussian curve is plotted to better illustrate that the average value of the measurement for each capacitive module has a different normal distribution according to the frequency variation as expected.

A 28nm, 1.8V supply integrated capacitance measurement circuit has been developed and exploited to evaluate Metal-Oxide-Metal capacitors matching in ultra-scaled technology for high energy physical experiments applications. The capacitor array to be evaluated is integrated in the same chip with the measurement equipment and specific capacitor modules may be selected by means of a shift register.

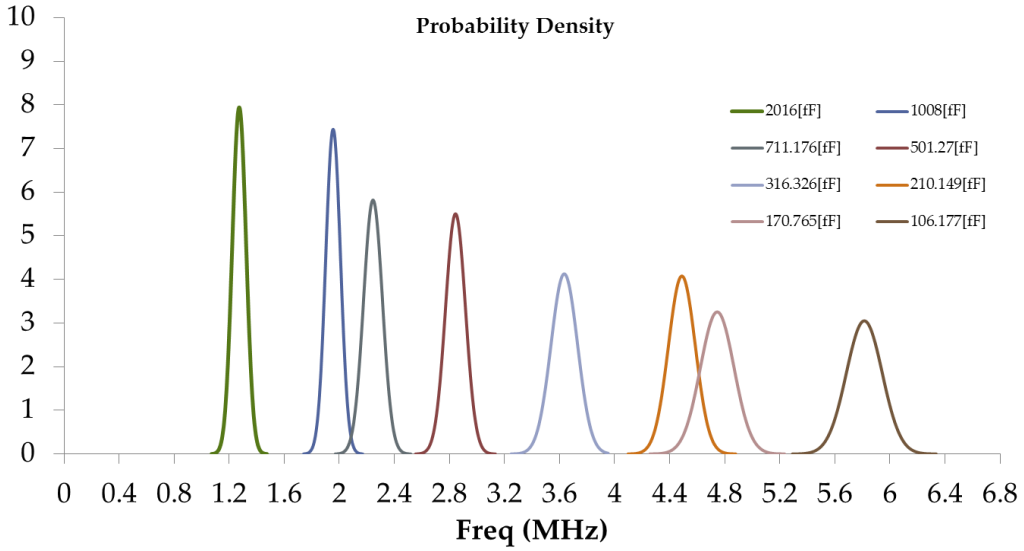

Figure 2.5: Probability density for the oscillator frequency measurement over 15 chips for 8 different capacitance values.

The worst-case matching is obtained for the capacitors values pair of about 500fF. This value is compliant to the feasibility of a 10-bit SAR A/D converter for low noise detectors charge amplifiers adding few additional fab calibration circuits. Furthermore, measurements over multiple capacitance values over different chips samples show that, as expected, larger capacitance values lead to higher matching accuracy. Finally, thanks to the embedded equipment, the capacitance measurement is not affected by large external interconnection parasitics. All the reported data refer to MoM capacitors before radiation exposure.

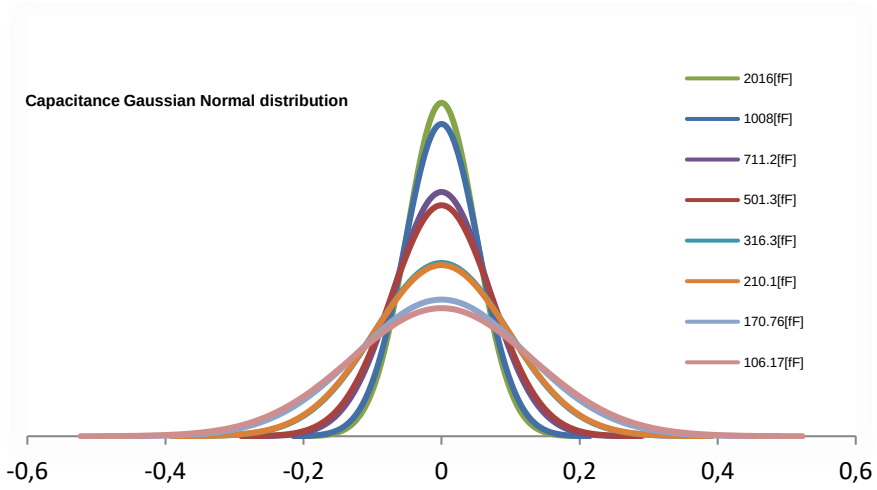

Figure 2.6: Normal Gaussian bell curve for the oscillator frequency measurement over 15 chips for 8 different capacitance values.

Experimental results show that matching performance is comparable to previous technologies, making the 28nm technology eligible for analog signal processing in front-end circuits for physical experiments and related data converters. This gives us a motivation to design a low power 14-Bit 1MS/s Extended-Range Incremental ADC in 28nm technology, but first we discus some important concepts about analog digital converters concepts and types.

2.5 Introduction to ADC

Analog to digital converters are important component in different electronic devices. ADC provide the critical translation of a measured analog signal into a digital form. In the digital domain, the data can be accurately processed to extract the desired information. Modern systems of conversion are trying to remove limits like speed, size, resolution and power consumption. The strategy is particularly important for portable communication system. Therefore, there is a big hunger to develop A/D converters that achieve both high speed and resolution using the lowest possible power consumption. The Flash A/D converter provides the highest conversion rate among all types of ADC architectures for a given technology, but, in the case of more than 8 bit of resolution, the required chip area becomes too expensive [12] [13].

There are more complex ADC architectures that allow obtaining the demanded high-speed conversion using less elementary devices. Sigma-Delta ADCs using oversampling technique provide high resolution with a reduced number of comparators. This kind of architectures do not require high precision analog components. Furthermore, the resolution of an n^{th}-order Sigma-Delta A/D converter increases by n+1/2 bit for each doubling in the oversampling ratio. Unfortunately, the needed high oversampling ratio in Sigma-Delta A/D converters has limited their use to primarily low-frequency applications.

In all those applications where a constant low noise floor is required on a large band of frequency, Sigma-Delta A/D converters can be replaced by other architectures like Pipeline ADC. This family of converters can provide an equal signal to noise ratio (SNR) over a range of frequency as large as Nyquist interval.

Pipeline architectures offer high flexibility of design and, after preliminary study, it is possible to choose an adequate structure for the target of project. Important aspects like the total power consumption, the number of bits and the basic building blocks performance depend on the considered application.

2.6 General ADC Specifications

This section describes the most common specifications of A/D converters.

Resolution: is the number of bits that an A/D converter uses to represent its analog input signal in the digital output format. The resolution together with the analog input range determines the minimum detectable voltage level [14].

Dynamic range: this parameter determines the maximum SNR and it is the ratio between the largest admitted input signal and the noise level expressed in dB.

Type of input-output analog signal: the input and the output signal can be single-ended, pseudo-differential or fully differential, respectively. The choice between these three various kinds of structure depends on the work conditions and applications. Single-ended

architecture presents analog signals referred to a common analog ground fixed value that is the same for the whole data converter. In a pseudo-differential structure, the analog signals are symmetrical with respect to a fixed reference voltage that can differ from the analog ground of the data converter. Finally, a fully differential structure uses analog signals that are not necessarily symmetrical with respect to a fixed level, but the information is expressed in terms of difference between a positive and a negative signal [15].

Analog resolution: is the smallest increment of the input signal corresponding to 1 LSB code change. For example, the analog resolution of a 10-bit converter with an analog input range of 1 V is 976.56 mV.

Offset error: is the difference between the ideal LSB transition to the actual transition point. The offset describes a shift for zero input as shown in Figure 2.7(a).

Input range: is the input voltage range over which the ADC is able to work and give back a correct digital code. The analog input range can be single ended or differential peak-to-peak and depends on the implemented structure.

Gain error: it defines the deviation of the real slope of the data converter characteristic from the ideal expected line. This parameter, shown in Figure 2.7(b), can also be expressed in term of difference between the input voltage just causing a transition to positive full scale and Vref - 1.5 LSB (full scale error) [16].

Common-mode error: it happens in the case of differential data converter structure and describes the common variation necessary on both input signals to cause a transition of one LSB of the output code.

Differential non-linearity (DNL): usually measured with a slow ramp input, it describes the maximum deviation from the ideal step size of 1 LSB. For a giver resolution, the value of the DNL measured in LSB must be within ±0.5 LSB as shown in Figure 2.8.

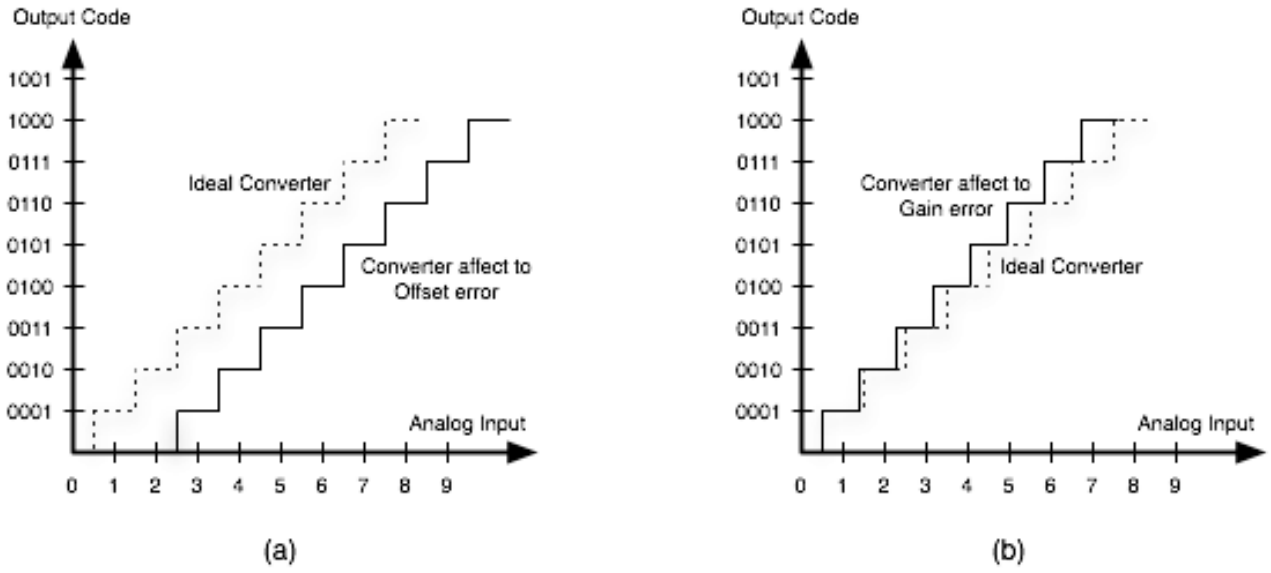

Figure 2.7: Offset error (a) and gain error (b)

Integral non-linearity (INL): usually measured with a slow ramp input, it describes the variation of each individual code from a line drawn from negative full scale through positive full scale. The deviation of any given code from this straight line is measured from the center of that code value. Also, this parameter must be within ±0.5 LSB to ensure the required resolution.

Power dissipation: is the value of the power used by the device during normal working conditions. Sometimes it can be also useful to know the required power consumption in stand-by (power-down) conditions.

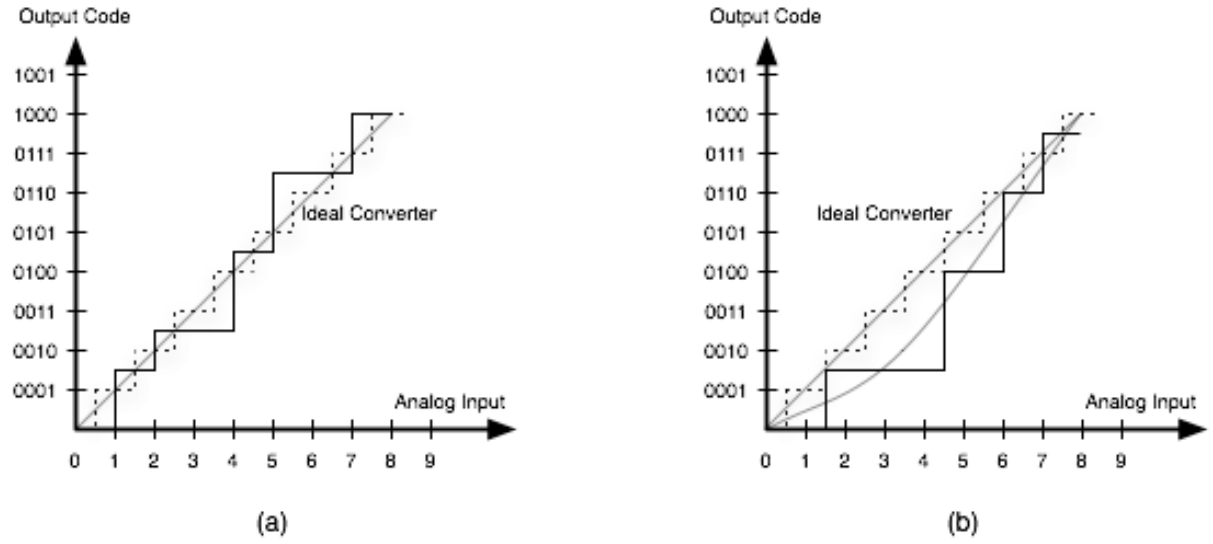

Figure 2.8: Differential non-linearity (a) and integral non-linearity (b)

Input impedance: is the value of the impedance seen between the input terminals. Ideally, in the case of a voltage input signal, this value is infinite while, for a current input signal, it is zero. This impedance is composed by a real part, a resistance, which dominates at low frequency, while at high frequency the input impedance is dominated by capacitiveelements. To ensure optimal working conditions for very high input frequency, the trend is adapting the input impedance with the load of the connection terminals [14].

Input bandwidth: is the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value, for a full-scale input signal.

Signal to noise ratio (SNR): is the ratio, expressed in dB, between the rms value of the input signal at the output and the rms value of the sum of all other spectral components below one-half of the sampling frequency.

Signal to noise plus distortion (SINAD): is the ratio between the rms value of the input signal at the output and the rms value of all the other spectral components below half the clock frequency, including harmonics but excluding dc. Figure 2.9 represents the value of the SINAD considering three different values of input amplitude. Also, this parameter is expressed in dB.

Effective number of bits (ENOB): is another method to specify SNR and SINAD. ENOB is defined as (SINAD - 1.76)/6.02 and it says that the converter is equivalent to a perfect ADC with ENOB number of bits.

Harmonic distortion (HD): is the ratio between the rms value of the input signal at the output and of all the other harmonics.

Spurious free dynamic range (SFDR): is the difference expressed in dB between the rms values of the input signal at the output and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present in the input.

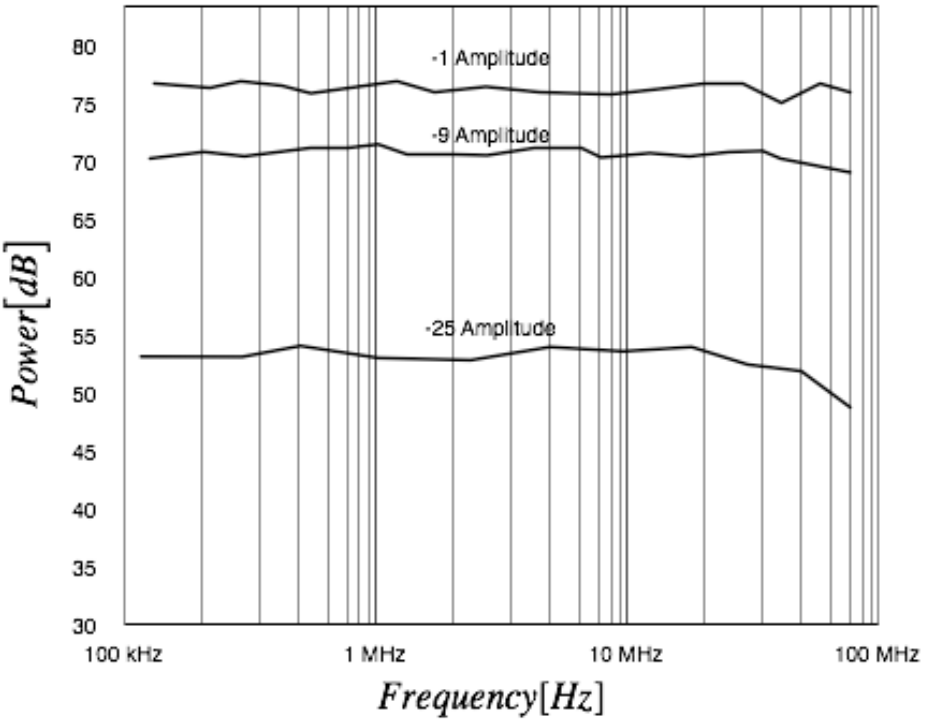

Figure 2.9: SINAD frequency representation.

Intermodulation distortion (IMD): is the spurious spectral component which appears when two sinusoidal signals are applied at the ADC input at the same time. It is defined as the ratio between the power of the intermodulation products and the total power of the original signals. IMD is usually expressed in dB.

2.7 Oversampling Techniques

Oversampling is a technique that improves the resolution obtained from a conventional converter by sampling the signal at a rate much faster (f_{os}= 2. OSR f_B , OSR > 1) than the minimum required Nyquist rate ($f_{sNyq.} = 2\ f_b$). Usually typical values for the oversampling ratio OSR=$f_s/2\ f_b$ are between 8 and 512 and usually it can be represented as a power of 2, i.e.$OSR = 2^r$, to facilitate the digital decimating filter [17].

By using oversampling technique, the power spectral density of the quantization error is stretched over the whole band [0, f_s], so its power in the signal band of interest [0, f_b] isreduced proportionally to OSR (Figure 2.10).

Therefore, the so-called in-band quantization noise power P_o is given by:

$$P_o = \int_0^{f_b} PSD_E(f)df = \frac{1}{OSR}\int_0^{f_b} PSD_E(f)df = \frac{{\sigma_e}^2}{OSR}$$

The power of the quantization noise is reduced significantly, provided that the out ouf band components are eliminated by a digital low-pass filter. The oversampled digital sequence is then processed by a decimator, which down-samples it to the Nyquist rate.

The signal-to-noise ratio with the oversampling technique is given by:

$$SNR_{os} = 10log_{10}\frac{P_x}{P_{oos}} = 20log_{10}\frac{A_x}{A_{max}} + 6.02N + 10log_{10}OSR + 1.76 \quad \text{[dB]}$$

If the over-sampling ratio is $OSR = 2^r$, then $10log_{10}OSR$= 3.01r[dB], so every doubling of the oversampling ratio, i.e. for every increment in r, the SNR_{os} improves by about 3dB, which means that the resolution improves by 0.5 bit. In other words, the oversampling converter has a 3dB/octave SNR or 0.5 bit/octave resolution improvement.

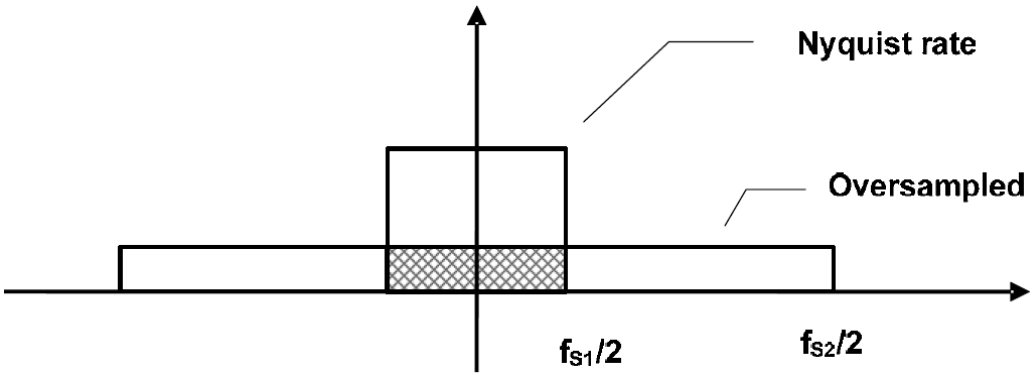

Figure 2.10: Quantization noise spectrum in Nyquist-rate and oversampled converters.

2.7.1 Sigma-delta modulators

The basic principle of operation of a sigma-delta modulator is shown in Figure 2.11. The circuit consists of a loop filter, which in its simplest form is an integrator, followed by an A/D converter which introduces a quantization error “E”. The digital output signal is subtracted from the analog input using a D/A converter in the feedback path. The error “E” due to the quantization process is the difference between the analog signal at the input of the quantizer and the output quantized digital signal. Suppression of the quantization error in a sigma-delta modulator is provided by two mechanisms: oversampling and noise shaping. As the reduction of the quantization error is quite effective, a high-resolution digital output is obtained using a low-resolution quantizer. In many cases, a one-bit quantizer with two output levels is sufficient.

The sigma-delta modulator architecture can be implemented with two different circuit techniques, either Discrete-Time (DT) or Continuous-Time (CT) circuits.

2.7.1.1 Continuous-time vs. discrete-time sigma-delta modulators

Figure 2.12 shows the block diagram of a sigma-delta modulator implemented using Continuous-Time (CT) techniques while Figure 2.13 shows its Discrete-Time (DT) counterpart. In a DT sigma-delta modulator a sample and hold stage is needed at the input to convert the CT analog signal into a discrete-time signal. This scheme can limit the linearity and noise of the sigma-delta modulator and, Also, an anti-aliasing filter is required in front of the sample and hold stage [18].

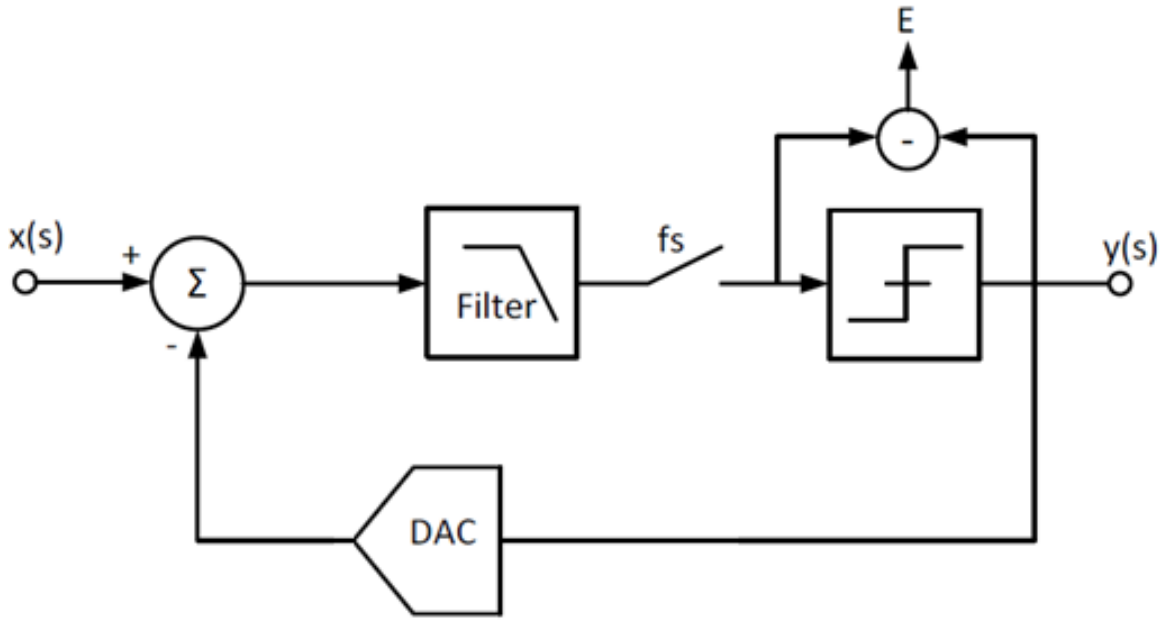

Figure 2.11: Basic principle of operation of a sigma-delta modulator.

In a CT sigma-delta modulator the sampling happens in the ADC only and eventual sampling errors are attenuated by the loop gain. The loop filter is working as an antialiasing filter; therefore, no filter is needed at the input.

The power consumption in CT sigma delta modulators is typically lower than in DT ones, thus making them suitable for high-speed and low-power applications. However, the linearity requirements are more difficult to achieve with CT than with DT circuits. CT circuits implemented with the active-RC techniques, feature worse linearity performance than DT circuits implemented with the switched capacitor (SC) technique.

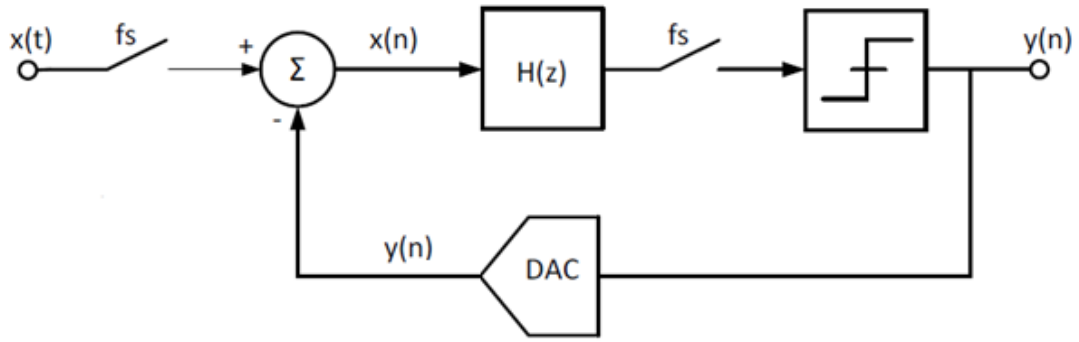

Figure 2.12: Block diagram of a discrete-time (DT) sigma-delta modulator

The main disadvantage of CT circuits is the clock jitter sensitivity in the feedback DAC where the DT feedback signal is added to the CT analog input signal. Time uncertainty in the feedback DAC raises the noise floor at the notch frequency, thus degrading the performance. The jitter effect can be reduced by using a return-to-zero DAC or by increasing the number of bits in the quantizer. A time-variant feedback waveform DAC, called an SCR-DAC, can also be used to reduce the effect of clock jitter, this can increase the power requirements for the operational amplifiers, leading to higher power consumption [14].

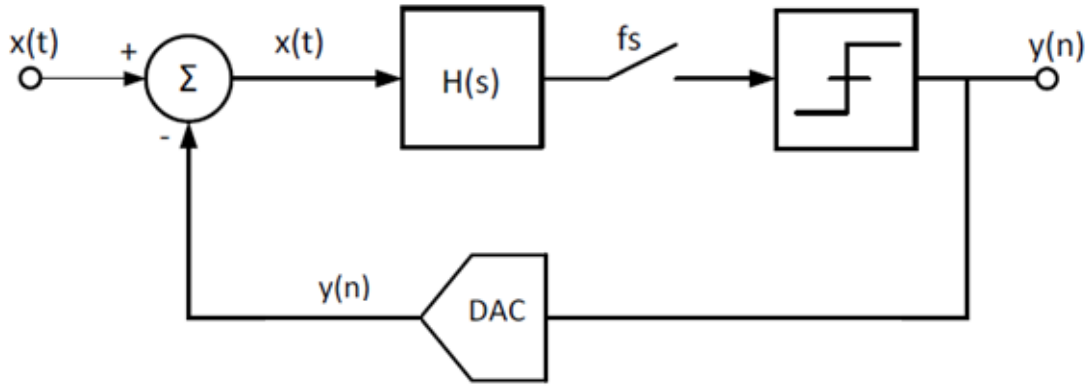

Figure 2.13: Block diagram of a continuous-time (CT) sigma-delta modulator.

2.7.1.2 Feedforward compensation

Increasing the order of the loop filter of a delta sigma modulator provides more tight quantization noise shaping and effectively improves the signal-to-quantization noise ratio. The general transfer function of a continuous time n^{th}-order loop filter consisting of "n" integrators is given by:

$$H(s) = \left(\frac{\omega_u}{s}\right)^n \qquad (2.1)$$

where ω_u is the unity-gain frequency of the integrators.

However, a sigma-delta modulator with the filter transfer given by (2.1) is not stable for n >1. An uncompensated second-order loop filter has a 180˚ phase shift at high frequencies. Feedforward and feedback compensation techniques are typically used for compensating the loop. Both compensation techniques can give similar noise transfer function, but have different signal transfer function characteristics.

To ensure stability in a second-order sigma delta modulator, a zero should be introduced in the loop-filter transfer function to reduce the high frequency phase shift. This can be done by adding a feedforward path in the loop filter, as shown in Figure 2.14. The choice for the ratio between c_1 and c_2 is determined by considering different parameters, as stability, maximum input level, signal-to-noise ratio and spread due to non-ideal processing. By increasing the coefficient ratio c_1/c_2, the zero in the loop filter transfer function is shifted to lower frequencies. An optimum option can be found, which provides both small phase shift at high frequencies and second-order noise shaping at low frequencies.

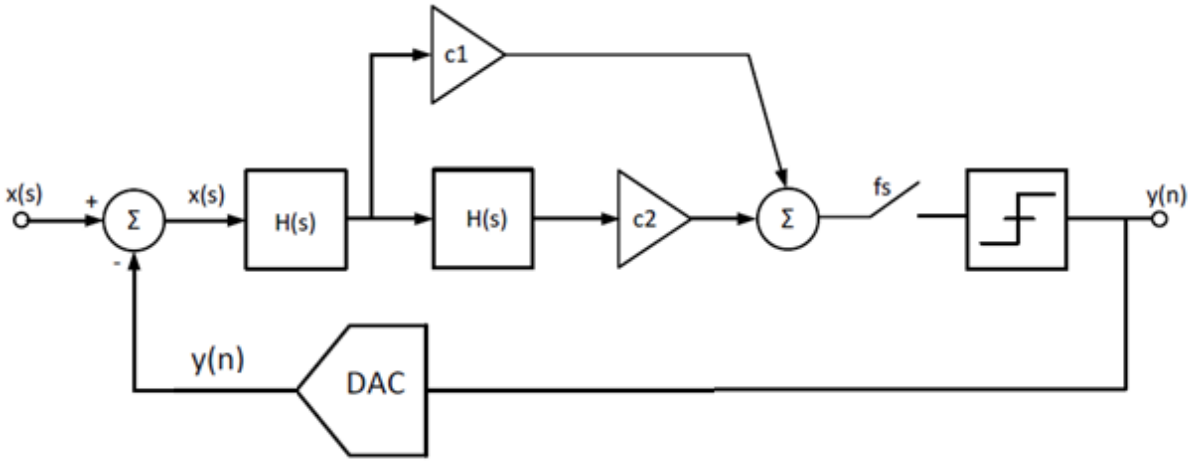

Figure 2.14: Second-order sigma-delta modulator with feedforward compensation

In general, filters of any order can be designed using this compensation technique. However, when increasing the filter order the zero position moves toward lower frequencies to achieve better stability. Therefore, increasing the filter order decreases the effective bandwidth where quantization noise is shaped. This will limit the maximum desired bandwidth. An effective way to maintain sufficient noise shaping while guaranteeing stability is to introduce local feedback paths in the loop-filter, thus creating resonator stages and providing extra notches at the edge of the signal band, which suppress the quantization noise.

2.7.1.3 Feedback compensation

Another way to stabilize the loop is to use feedback paths, as shown in Figure 2.15. for a second-order delta sigma modulator. In this case, a fraction of the output is fed back to the input of each integrator stage of the loop-filter. Generally, the signal transfer function (STF) of a n^{th}-order feedforward compensated filter has n poles and n-1 zeros, while in a feedback compensated filter, the STF has n poles only. Therefore, in the feedforward case, the STF is a first-order low-pass filter (first-order anti-aliasing filter), while in the feedback case, the STF

is an n^{th}-order low-pass filter (n^{th}-order anti-aliasing filter). Clearly, the STF in a feedback compensated sigma delta modulator provides much stronger filtering for high frequency signals than in the feedforward case. This is shown in Figure 2.16 for a high-order modulator.

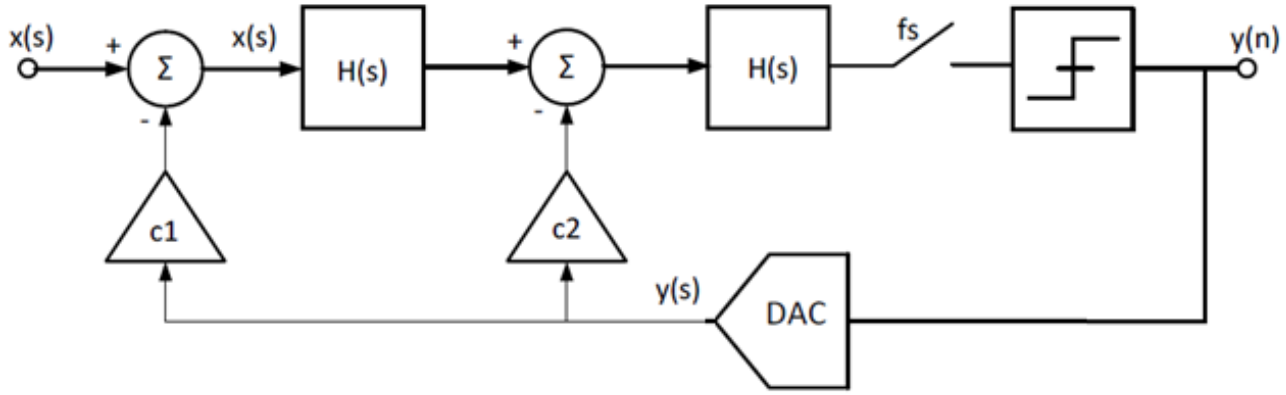

Figure 2.15: Second-order sigma-delta modulator with feedback compensation

Another difference between the two compensation techniques is that, due to the zeros in the transfer function, in the feedforward case the STF is not flat, but shows some peaking at a certain frequency. This means that at the peaking frequency, the maximum stable input level is reduced by the gain of the peaking. This is not the case with the feedback technique, since the STF has no zeros, and, hence, no peaking occurs.

A major drawback of the feedback filter architecture is that the outputs of the integrators contain, besides the quantization noise, a substantial part of the input signal. This implies that a larger output swing and a better linearity is requested in the operational amplifiers, thus leading in general to a higher power consumption [19].

Often, feedforward and feedback compensation techniques are implemented together in order to obtain an optimal filter design.

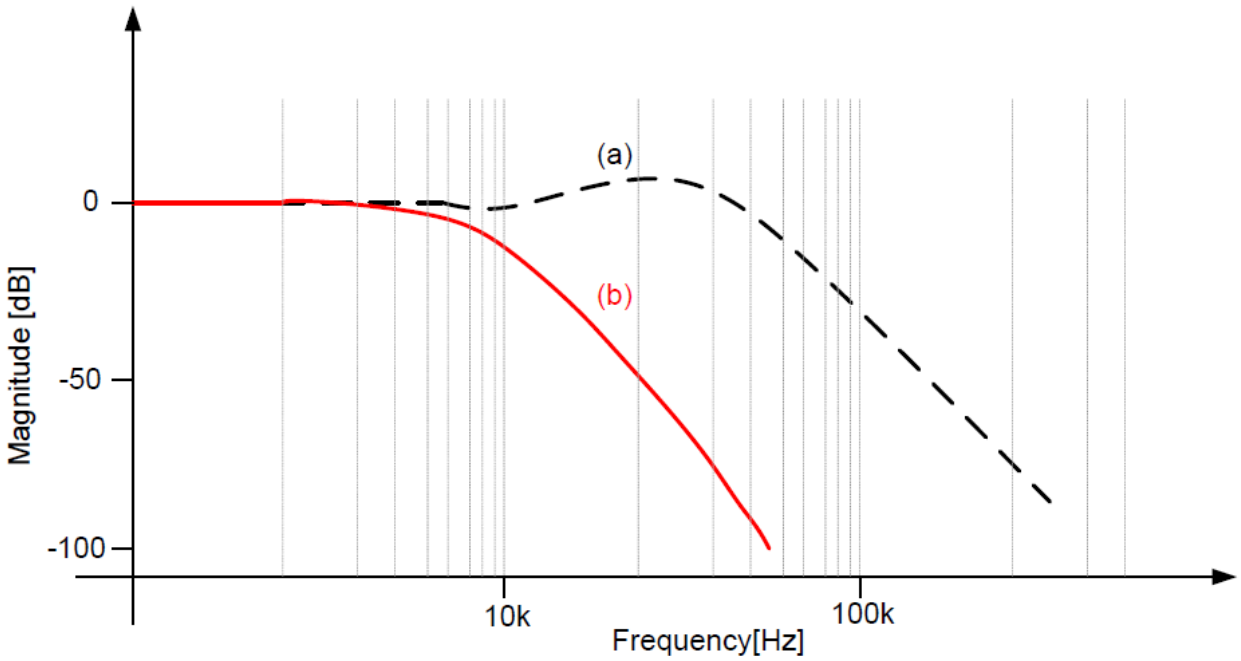

Figure 2.16: STF of a high-order sigma delta modulator with feedforward compensation (a) and feedback compensation (b).

2.7.1.4 Multi-bit vs. single-bit quantizer

The main motivation for adding more bits in the quantizer is the direct reduction of the quantization noise and of the jitter sensitivity. Furthermore, with more bits in the quantizer, the stability constraints are easier to achieve than with single-bit structures and the internal signal swing is lower, thus alleviating the operational amplifier requirements in terms of output swing and slew rate. On the other hand, a larger number of bits in the quantizer increases the capacitive load of the amplifiers, which is a problem especially in high-frequency applications [20]. Moreover, more analog circuit components are needed to implement the internal ADC and DACs. The possibility of using higher gain in the integrators with multi-bit quantizer than in a single-bit loop, can improve the SNR by even more than 6 dB per additional bit. Moreover, in multi-bit sigma delta modulators the out-of-band quantization noise is also decreased, which relieves the digital filtering required in the decimator.

Despite the advantages of multi-bit structures, single-bit sigma delta modulators are the most frequently used. The reason is the linearity requirement in multi-bit feedback DACs, which sets the upper limit for the sigma delta modulator performance. The distortion introduced in the first-stage DAC, indeed, is not shaped, but it is directly added to the input, as shown in Figure 2.17.

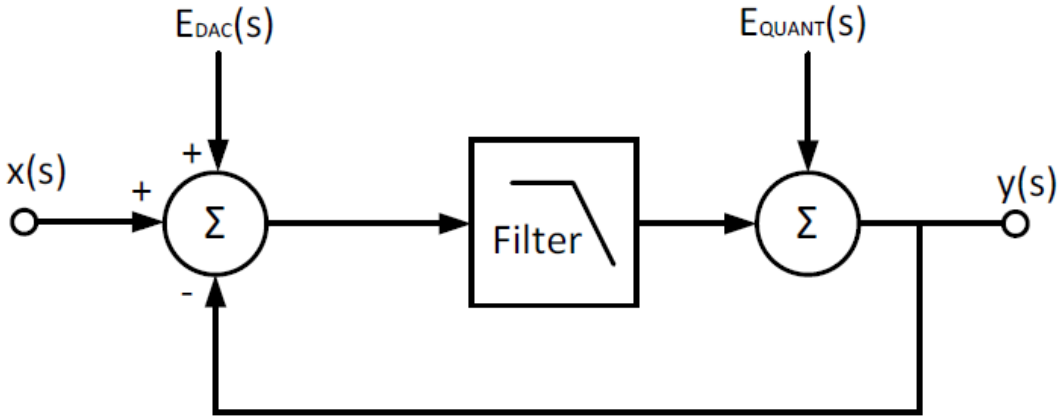

Figure 2.17: Sigma delta modulator with non-linear DAC error.

Therefore, the linearity of the whole sigma-delta modulator cannot be better than the linearity of the DAC. The DAC linearity can be improved by element trimming, but this is expensive, and it is not suitable for mass-produced products. Calibration techniques may also be utilized, but extra hardware and calibration time are needed [21]. Nowadays, different Dynamic Element Matching (DEM) techniques, which randomize and/or shape the distortion contribution of the DAC to improve the linearity over the signal band are widely used [22].

2.8 14-bit extended range incremental A/D

This work reports the architecture study, design, and simulation validation of a 14-bit extended range incremental A/D converter for high energy physics experiments in ultra-scaled technology (28nm) [23]. Traditional sigma-delta modulators are well suited for sensor read-out applications, like environmental and biomedical measurements, or even live audio recording from a microphone. On the other hand, these ADCs, which exhibit very high Dynamic Range (DR) thanks to oversampling and quantization noise shaping techniques, typically feature a narrower bandwidth with respect to Nyquist rate architectures. Moreover, because of their inherent memory effect (the digital value of each sample depends on the value of previous samples), they are not suitable for applications where single-shot events must be evaluated and measured with very high linearity, like for instance, particle energy in physics experiments.

For these kind of applications, time-count based ADCs are typically recommended. Most physical experiments applications exploit double ramp, Wilkinson, or time-Vernier converters. However, in the case of the combined requirement of defined start of conversion time (SoC), high linearity, oversampling, and noise shaping to boost the resolution, the best solution is to opt for incremental ADCs.

Incremental data converters (IDCs) can provide precise high-resolution single-shot conversion with accurate gain, low offset, no memory effects, and relatively short conversion time, leading to an adequate bandwidth even for high energy physics experiments [24].

The proposed extended-range IDC consists of the cascade of two second-order multi-bit incremental converters where the residual quantization error from the first stage is amplified and fine converted by a second incremental stage. The two stages, ideally targeting 9 and 6 bits, respectively, are both based on a cascade of integrators with feed-forward (CIFF) architecture to maximize linearity. If necessary, they can work in pipeline to minimize conversion time. When the conversion of each sample by the two stages is completed, a digital recombination filter produces the overall ADC output word with the required resolution (ENOB) of at least 14 bits and a throughput of 1MS/s at the very low oversampling ratio (OSR) of 16. Each stage consists of two integrators followed by a multi-bit quantizer and a capacitive DAC for the feedback. At the start of each conversion cycle, both analog integrators and the digital filter memory elements are reset.

The proposed ADC is implemented in a 28nm technology, which represents the new frontier for analog signal processing in front-end circuits and data converters for physics experiments, due to the intrinsic radiation hardness guaranteed by the thin gate oxide. Such rad-hard properties of the 28nm technology are being validated within Scaltech28 experiment, funded by Italian National Physics Institute (INFN). Basic structures of passive components and transistors have been already successfully tested after 1GRad irradiation. The aim of this new step of the experiment is to design and evaluate the performance of a complex mixed-signal circuit, such as a cutting-edge A/D converter, in 28nm technology before and after different doses of radiation exposure.

2.8.1 Second-order incremental A/D converter

Incremental ADCs may be considered as sigma-delta modulators which permanently operate in transient mode for each conversion. Reset operation is performed every time the sample being converted reaches the desired precision. This can be ideally guaranteed by the proper choice of oversampling ratio, modulator order, and number of bits of the internal quantizer circuit. IDCs, therefore, provide one-to-one correspondence between each sample of the input signal and the digital output after filtering and decimation. This feature is usually typical of Nyquist-rate converters and, in fact, an IDC may be considered a quasi-Nyquist-rate converter with respect to its effective data output rate $F_s=F_{s1}/OSR$, where F_{s1} is the master clock frequency, driving integrators and quantizer, and OSR is the oversampling ratio of the equivalent sigma-delta modulator.

Furthermore, in IDCs an input sample-and-hold buffer operating at F_s is often included in the design to fulfill all requirements for the IDC to be an effective Nyquist-Rate converter. Figure 2.18 shows the block diagram of a conventional CIFF multi-bit second order incremental A/D converter. The structure consists of two integrators followed by a multi-bit sub-ADC and a feedback DAC. It is important to underline that, exploiting feed-forward technique, we can use a single feedback path and thus a single DAC in the architecture. Again, at the beginning of each A/D conversion cycle, all the analog and digital memory elements are reset.

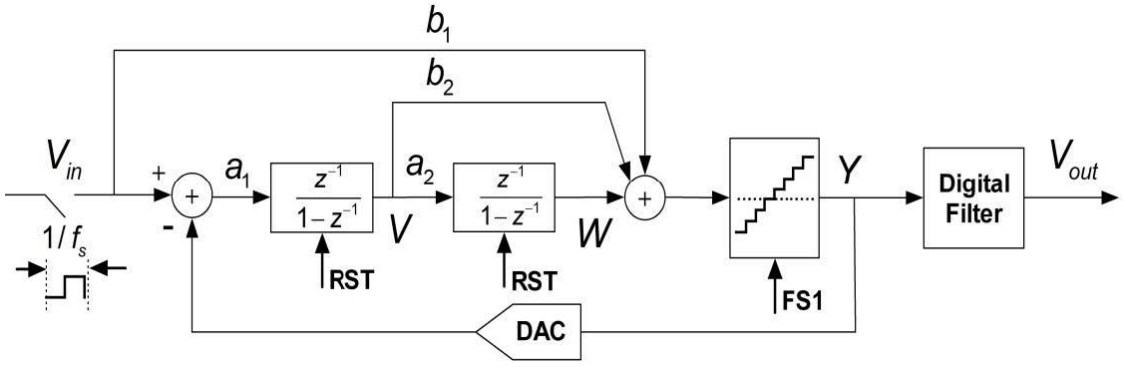

Figure 2.18: Block diagram of a conventional CIFF multi-bit second order incremental A/D converter with optional input sample-and-hold feature

If the S/H circuit is not present, the IDC will automatically perform averaging operation on the in-band input sampled signal. If the loop is stable for all possible amplitudes of the input signal in the operating range, which can be achieved by carefully designing the loop and limiting the maximum gain of the quantization Noise Transfer Function (NTF), the output of the two integrators can be bounded in a range compliant with the possible input range of the following multi-bit quantizer. This conventional solution features high linearity performance with moderate power consumption being furthermore inherently stable exploiting integrators with one-period delay and choosing a_1=1, a_2=2, b_1=1 and b_2=1 as architecture coefficients [25].

The drawback of this solution is that in the overall power consumption we must also consider an additional required block performing the analog adder function to implement the sum of the output of the second integrator with the two feed-forward paths in front the quantizer. To overcome this limitation, the two feed-forward signals can be added directly at the input of the second integrator instead of at its output. In order to compensate this topological variation, we must perform the discrete-time derivative of the two feed-forward signals, so that their branch transfer function will be "$b_1 \cdot (1-z^{-1})$" and "$b_2 \cdot (1-z^{-1})$", respectively, instead of simply "b_1" and "b_2".

In the circuit design this operation corresponds to the addition of two series capacitors in the feed-forward paths. The optimized architecture for the CIFF second order multi-bit IDC is then illustrated in Figure 22.19. This architecture has been chosen mainly for reducing the required integrator output voltage swing (thanks to the feed-forward paths) and hence the power consumption, while allowing an optimized op-amp design in scaled technology (28nm) as well as low voltage supply. In particular, the first integrator, which is the most critical in the design since its performance has a paramount impact on the digital output accuracy, needs only to process the quantization noise, thus allowing an optimal op-amp design, which increases the power efficiency. Furthermore, the N-bit quantizer allows higher system resolution for a given OSR and avoids undesired idle tones with respect to single-bit solutions.

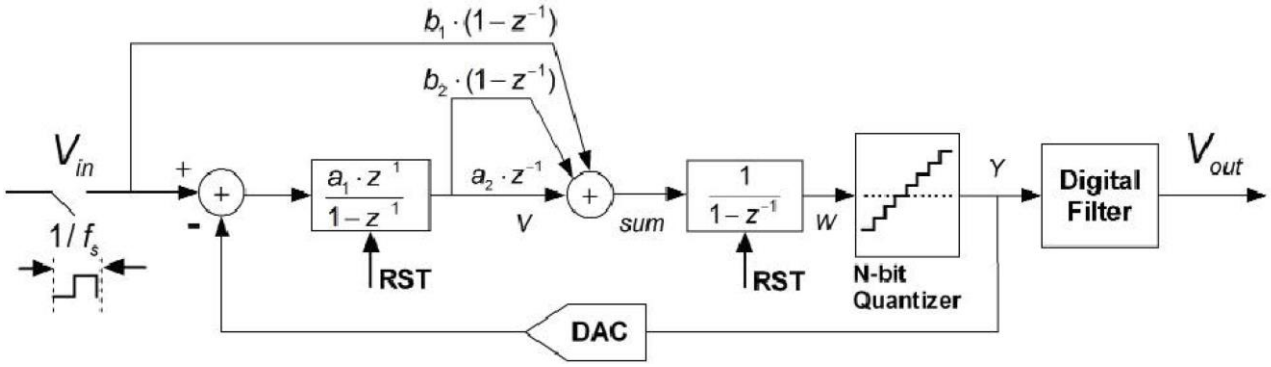

Figure 2.19: Improved adder-less CIFF multi-bit second-order incremental A/D converter block diagram

In order to guarantee stability for all input signal amplitudes, the coefficients of the architecture reported in Figure 22.19 should be set to a_1=1/2, a_2=1, b_1=1, and b_2=2 for the conventional implementation with one-period delay integrators. The same performance is also obtained by exploiting a second integrator without delay and setting the coefficients as: $a_1=a_2=b_1=b_2=1$.

The sampled output of the integrators v[i] and w[i] may be calculated for each cycle solving the equations defined by the block diagram. In particular, after OSR clock cycles, the output signal V_{out} is defined with a residual error $E_q=V_{in}-V_{out}$. The converted data is obtained thanks to a digital filter at the output of the quantizer which has also the function of decimator by a factor of OSR. Since in the IDC shown in Figure 22.19 the second integrator has also the function of adder, the residual error estimation is not simply proportional to the accumulated value in the second integrator at the end of the conversion, as in the conventional solution shown in Figure 2.18, but, in the particular case of unitary coefficients, it is directly proportional to the difference between w[OSR] and v[OSR]. We remind that the signal applied at the input of first integrator is V_{in} for all cycles except the last one, for which the input is zero. Non- iterative expressions for V_{out} and E_q after conversion are:

$$V_{out} = \frac{2}{a_1 \cdot a_2 \cdot OSR \cdot (OSR-1)} \cdot \sum_{i=1}^{OSR-1} i \cdot Y[OSR-i-1] \quad (2.2)$$

$$E_q = \frac{2}{a_1 \cdot a_2 \cdot OSR \cdot (OSR-1)} \cdot (w[OSR] - v[OSR]) \quad (2.3)$$

At its maximum value, E_q represents the LSB of the IDC, thus the ideal dynamic range DR of the IDC is given by:

$$DR = \frac{V_{in,FS}^2/2}{LSB/12} = \frac{3}{2} \cdot (a_1 \cdot a_2 \cdot OSR \cdot (OSR-1))^2 \quad (2.4)$$

The architecture, with unitary coefficients, has been implemented with switched capacitor circuits for an input signal bandwidth of 500kHz, setting by design OSR=16 and 3 bits (7 comparators) for the quantizer, leading to an ideal resolution of 9 bits and exploiting IDC residual error E_q for range extension.

2.8.2 Extended Range Incremental ADC

Most high-energy physics experiments require an ADC resolution of the order of 10 bits, so that the proposed CIFF second order multi-bit IDC architecture with OSR=16 may be directly used in many cases. However, the design is a pipelined range extension for the IDC which makes it also suitable for critical experiments requiring higher output rate and higher dynamic range.

In the conventional solution for achieving range extension, whose block diagram is shown in Figure 2.20 applied to a CIFF single loop second-order incremental converter, the residual value $E_q=V_{int,2}(OSR)$ is sampled, amplified by a factor A, and converted into the digital domain by a second M-bit ADC, for which usually full-flash or SAR architectures are used because of their low conversion time.

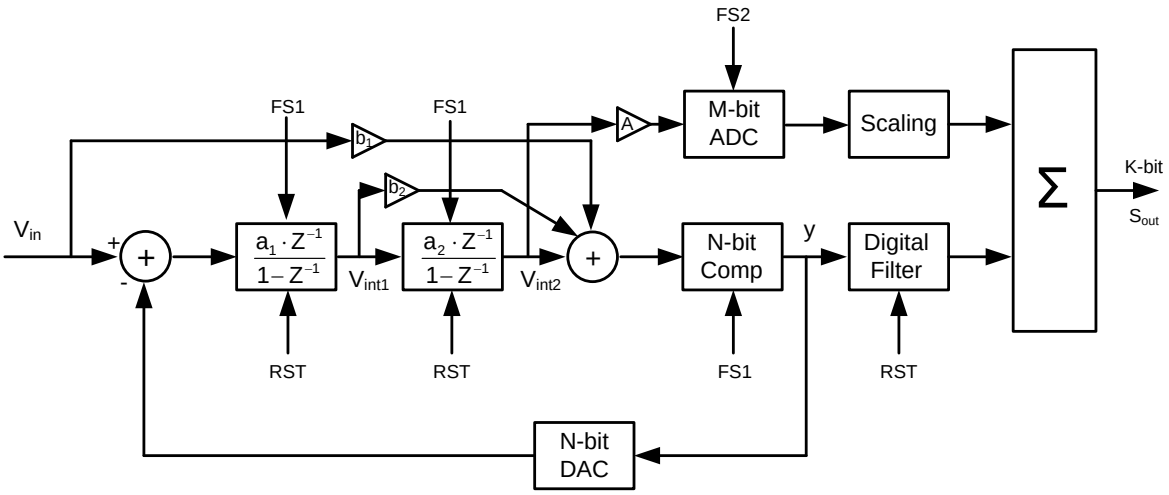

Figure 2.20: Block diagram of the conventional IDC range extension architecture

The M-bit sub-ADC must have the same output rate of the main IDC, which means that, in the case for instance of a full-flash ADC, its operating frequency is f_s/OSR where f_s is the master clock frequency of the IDC. After a digital scaling block with gain G, the output of the M-bit ADC can be directly added to the filtered output of the main IDC to get a digital output stream with extended range. For the conventional implementation, the digital scaling for range extension G_t is:

$$G_t = \frac{2}{a_1 \cdot a_2 \cdot A \cdot OSR \cdot (OSR-1)} \qquad (2.5)$$

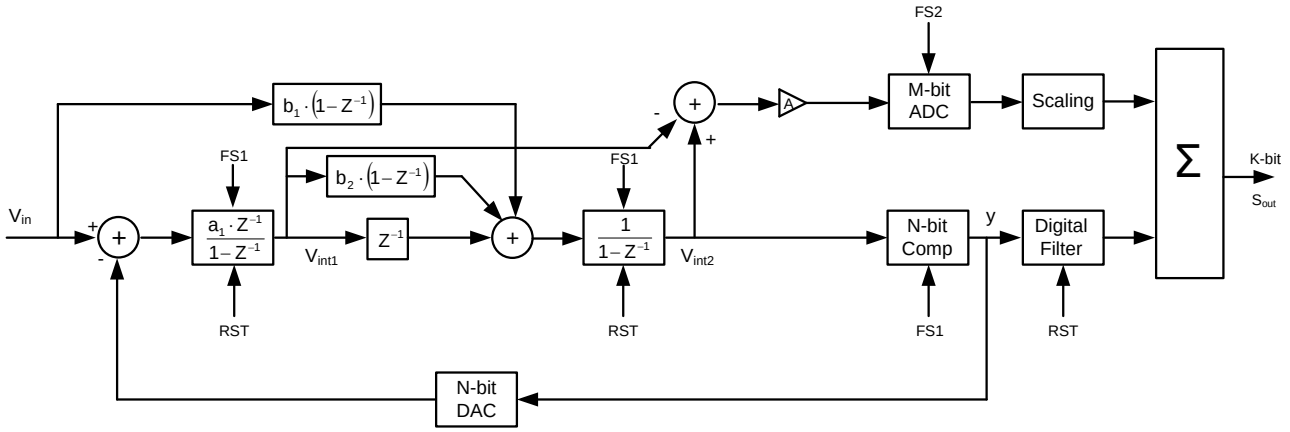

Figure 2.21: Block diagram of enhanced IDC range extension architecture

In this work, we report the implementation of a dynamic range extension solution specifically designed for the enhanced CIFF second order multi-bit IDC without additional adder. Since in this case, in order to extend the range, the feed-forward paths are connected directly to the input of the second integrator, we need to process with a sub-ADC, always operated at f_s/OSR, the residual difference between the two integrators outputs $E_q=V_{int,2}(OSR)-V_{int,1}(OSR)$ after amplification by a factor A. The scaling factor G_e in this case is, in first approximation, equal to the value of G_t as reported in (2.5) if V_{in} is masked to zero in the last cycle.

In the actual design, whose block diagram is illustrated in Figure 2.21, unitary coefficients have been set for loop stability, by exploiting a second integrator with no delay and removing the optional additional delay at the output of the first integrator. The residual amplification factor has been set to $A=2^{N-1}=4$ for ancillary ADC input dynamic range optimization.

A Matlab code model has been developed for the CIFF IDC, including the digital filtering and decimation block to get the final V_{out} value. The model has also the possibility to include thermal noise to define design constrains. A study on theoretical resolution limits for the extended range IDC, varying the resolution of the IDC quantizer and of the ancillary converter has then been carried out.

Since the overall resolution of the extended range converter will be mainly determined by the thermal noise and by the performance of the operational amplifier used in the first integrator stage, a reasonable target for the final resolution has been set to 14 bits with a power consumption lower than 1mW. This target could be safely fulfilled with some margin by the developed IDC running at 16 MHz with an oversampling ratio of 16, a 3-bit quantizer followed by a 6-bit extended range ADC operated at 1MHz.

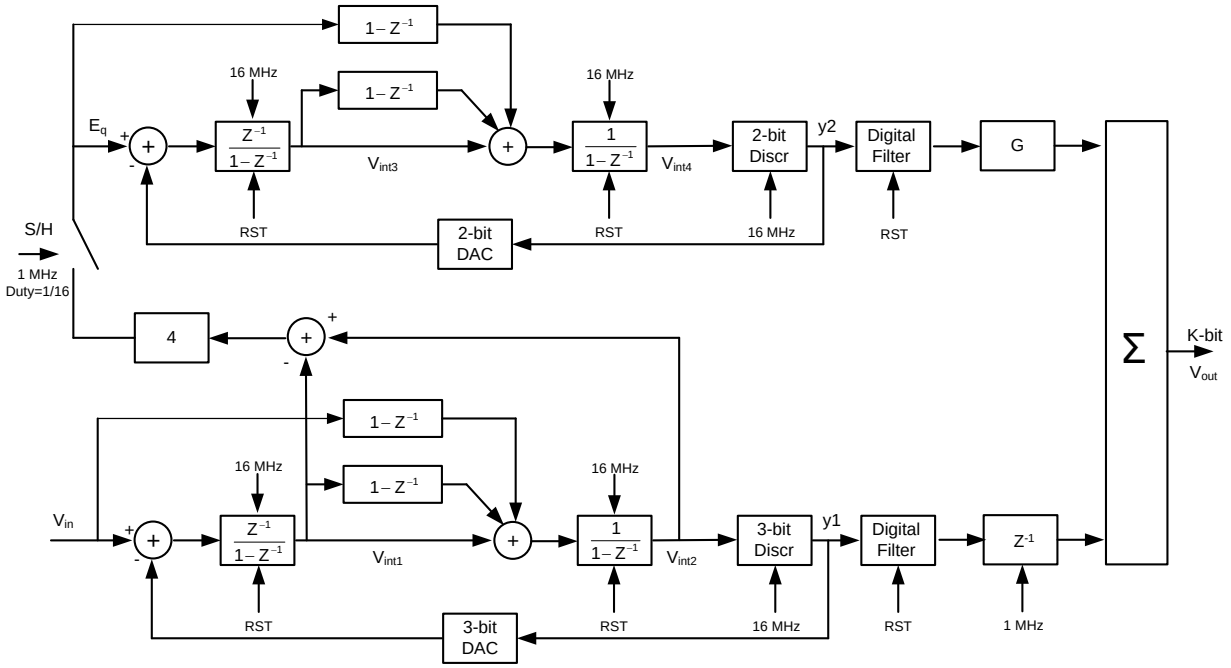

Figure 2.22: Block diagram of the proposed extended range IDC

After considering the use of a 6-bit SAR, an extended range ADC has been developed by exploiting a second incremental converter with the same output rate and OSR, to process the residual quantization error of the main IDC. The auxiliary IDC is less critical with respect to the main one, and thus the internal quantizer has been set to 2-bits by design (4 levels), while the requirements for thermal noise of the first integrator block are just 6 equivalent bits, which means very low power.

A significant improvement with respect to the architecture of Figure 2.21 is the possibility to run in pipeline this cascaded IDC for residual conversion and the main IDC, leading to a shorter overall conversion time, equal to the conversion time of a single IDC (1 μs), since the time for residual conversion may be considered pure latency. Figure 2.22 shows the detailed block diagram of the developed extended range IDC. A digital delay of 1μs must be added at the output of the first IDC to align the converted sub-samples and perform output recombination, while a sample-and-hold block (S/H) is required at the input of the second IDC. The role of the S/H is to maintain the residual value at the end of the conversion of the first IDC at the input of the second one for 16 cycles (sub-conversion). We can avoid the use of the additional S/H block if the pipeline feature is not required, saving further power at the cost of a reduction by a factor of two of the overall output data rate (500kHz instead of 1MHz). This solution can be implemented for instance in experiments where single pixels are read-out and the overall conversion time is considered (conversion period plus latency), while it is not convenient for a matrix scan in which the important parameter is only the conversion frequency, since the latency is negligible.

The proposed extended range IDC architecture, implemented with a differential switched-capacitor circuit, is shown in Figure 2.23. Both sub-IDCs are implemented using capacitive elements for the derivative feed-forward paths and thermometric flash ADC for the 3-bit and 2-bit quantizers. The quantization noise level has been set to 15 bits by design. The most critical block is the operational amplifier of the first integrator. For this op-amp, in order to guarantee a thermal-noise level at 14-bit resolution over 0.4Vpeak-differential range with 1V supply, a current consumption budget of 600μA has been allocated, while 300μA are used to fulfill the requirements of the rest of the system.

Due to low supply voltage, cascode topologies are not feasible, and, in order to overcome the limited transistor, gain in ultra-scaled technology, a two-stage op-amp choice is mandatory. On the other hand, a very low power budget has been allocated for the S/H block since it is operated with a duty cycle of 1/16 and the thermal noise requirement is only at 6-bit level. The complete IDC is reset once the residual is sampled and the digital output of the first IDC is stored in the delay element.

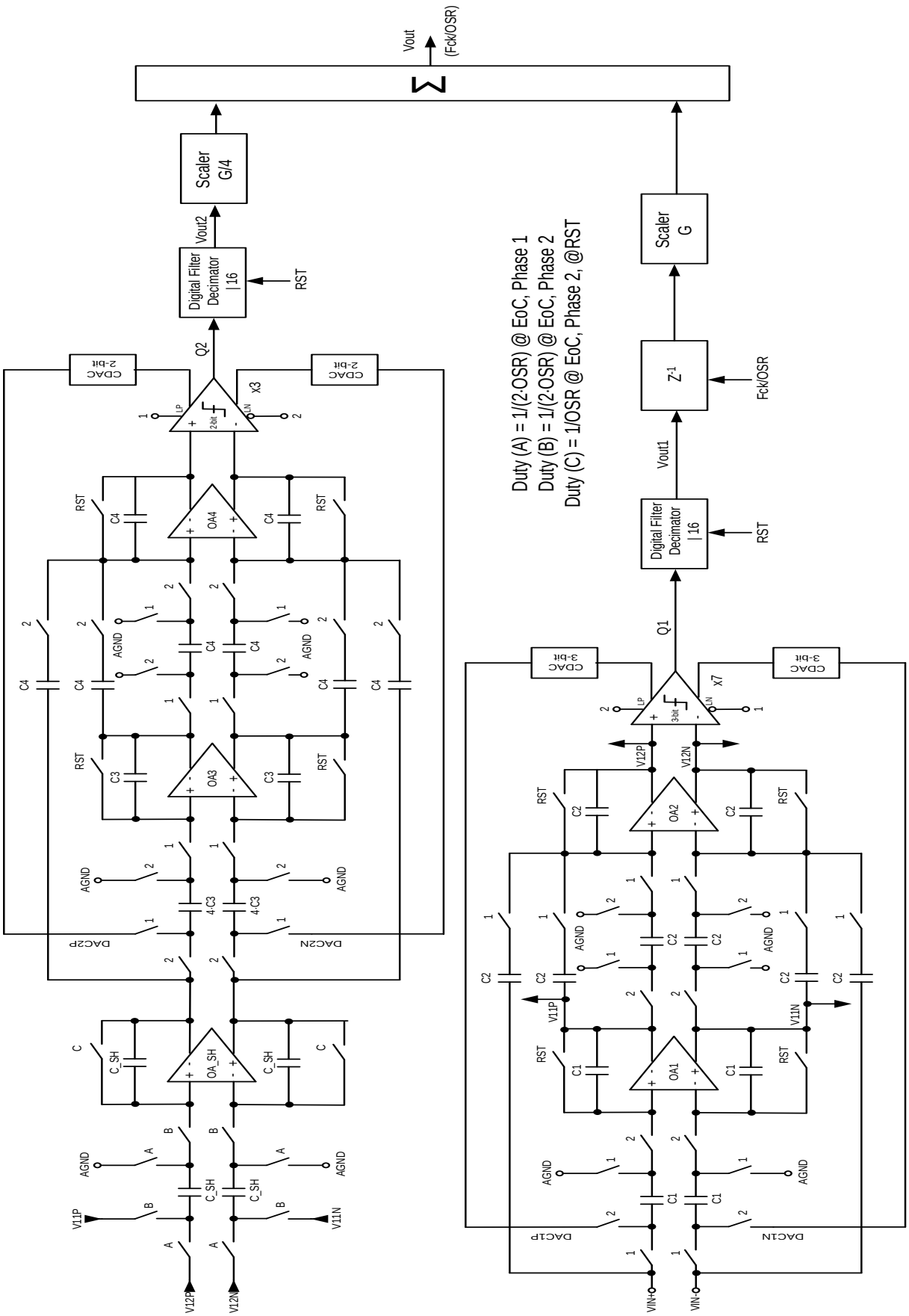

Figure 2.23: Switched capacitor differential implementation of the enhanced extended range IDC

2.9 Circuit design

2.9.1 Operational amplifier design

The main target in designing the operational amplifier is low power consumption and so we adopted a two-stage Miller compensated operational amplifier for the integrators as shown in Figure 2.24. Since the 1/f is not critical due to the input signal bandwidth, NMOS input devices operated in subthreshold are used to maximize the gm/I efficiency. The choice of multi-bit quantizer and feed-forward structure lowers the main operational amplifier output swing to ≃ 900mVpeak. The auxiliary operational amplifier implements integration and feedforward summation. Its output swing is as large as the quantizer full scale, i.e. the maximum signal.

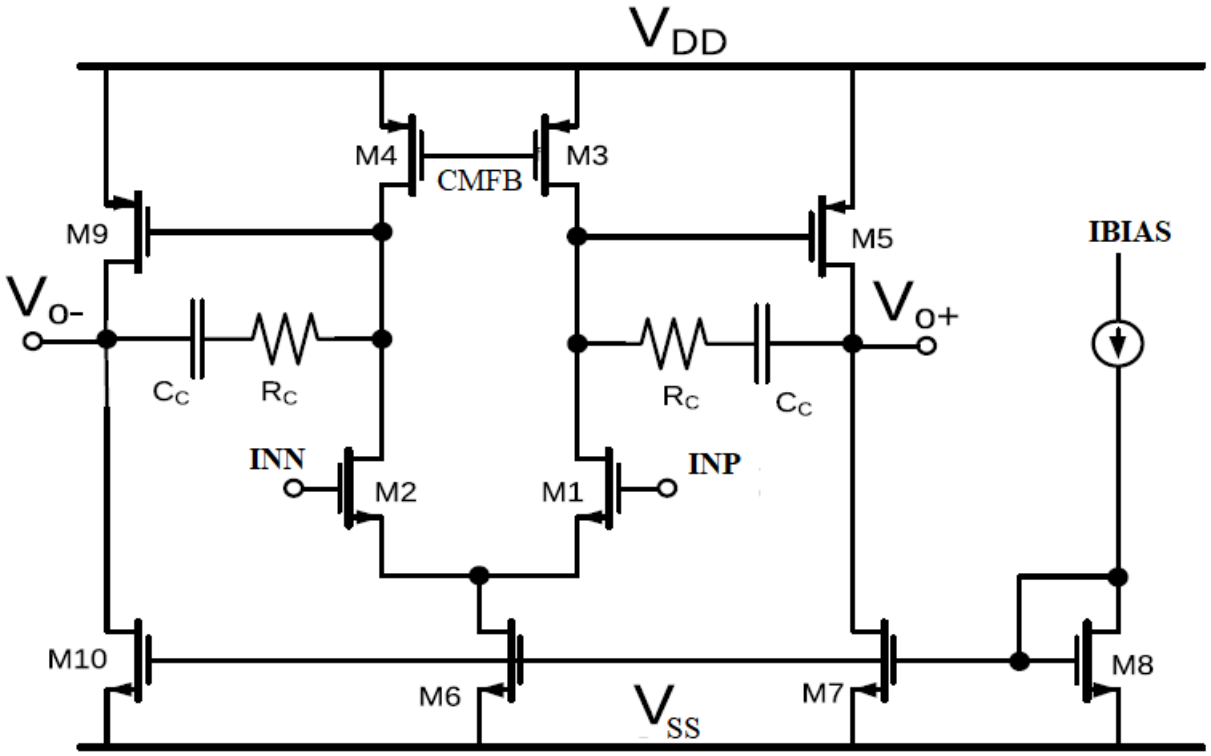

Figure 2.24: Two-stage operational amplifier with Miller compensation

2.9.2 Multibit quantizer design

The 3-bit quantizer utilities seven fully-differential comparators, and the threshold levels are generated by a passive capacitive partition as shown in Figure 2.25. This type of passive threshold generation reduces the power consumption of the overall quantizer.

The single threshold V_{thr} is realized following the relation

$$V_{thr} = (V_{R+} - V_{R-}).\ \frac{C_p - C_m}{C_p + C_m}$$

The comparators use a continuous-time PMOS input pair and a latched output stage to interface directly to the output digital filter and feedback DAC.

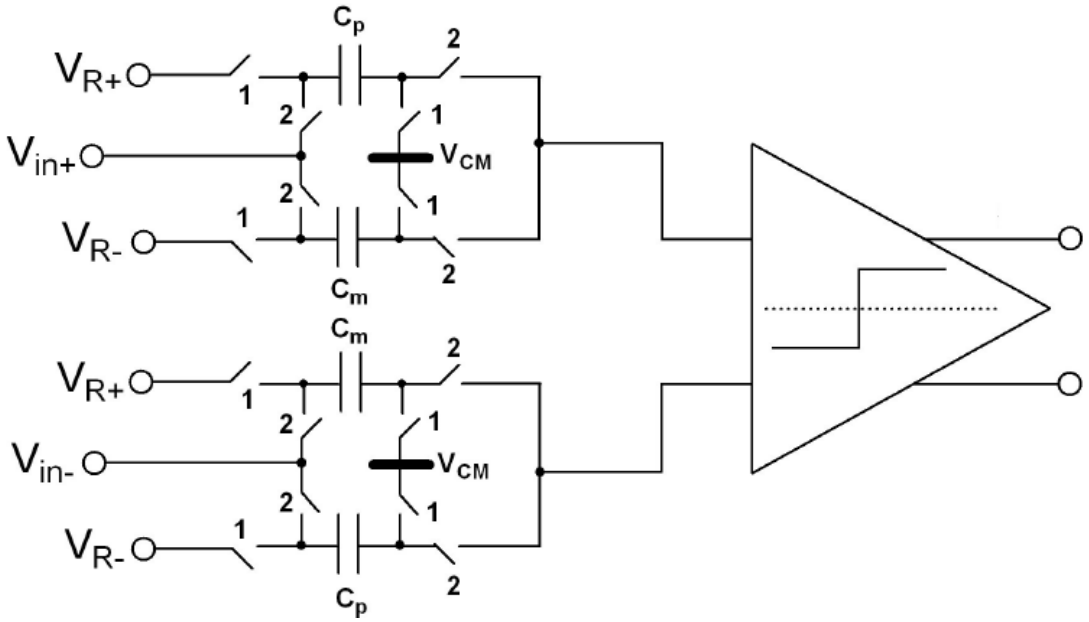

Figure 2.25: Passive threshold network of the quantizer structure.

2.10 Simulation Results and Conclusions

After a system study with ad-hoc MATLAB code including non-idealities as well as VerilogA top level simulations of the developed SC architecture, transistor level simulations have been carried out including the blocks designed fulfilling the specs given by the preliminary architectural study. The basic blocks have been developed at transistor level in 28nm technology and the estimated overall power consumption for 14-bit resolution is 900μA. Because of the noise requirements, the input sampling capacitor has been set to 5pF. A set of simulations with near-actual full scale (-7dBVref) sinusoidal signal of 300Hz, 0.4V peak differential amplitude have been carried out.

According to the above typical simulation setup, Figure 2.26 shows the digital output spectrum of the overall extended range IDC at transistor level without considering mismatch and thermal noise, which has been set to 15 bits by design and verified in simulation in a separate setup. Figure 2.27 illustrates the achieved SNDR as a function of the input amplitude, considering the extended-range IDC and the first-stage standalone IDC, respectively. These results are encouraging for the finalization of a first enhanced extended range double IDC in 28nm technology for high energy physics experiments. The prototype

will be also employed to investigate technology radiation hardness for mixed signal circuits. The chip has been sent out for fabrication. Figure 2.28 shows the design layout with area of $0.35mm^2$.

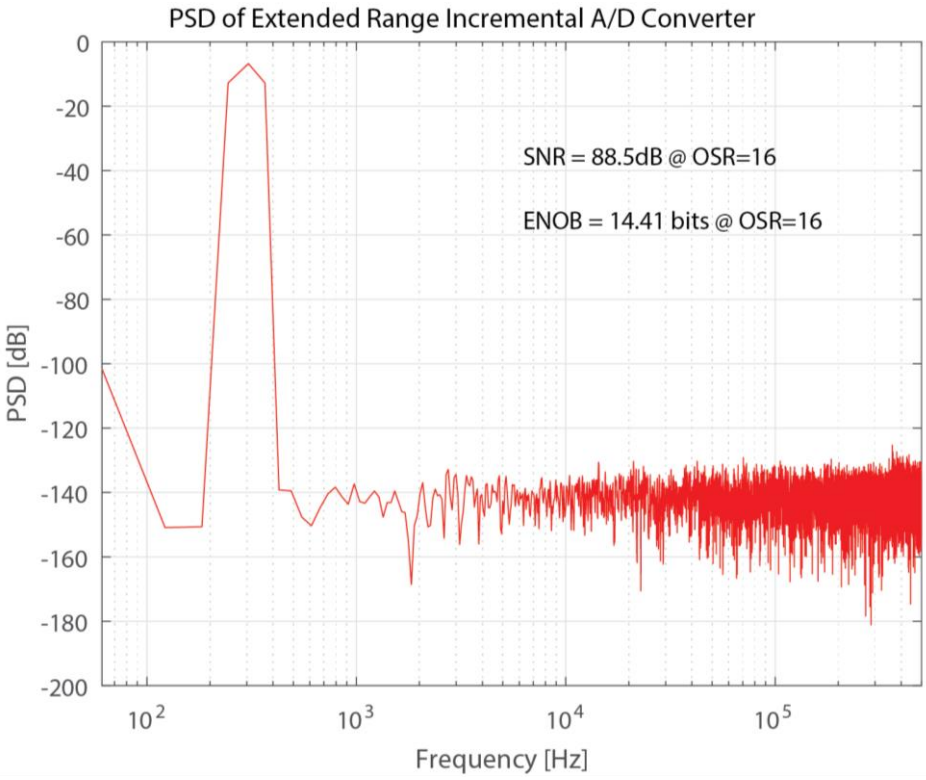

Figure 2.26: Digital output spectrum of the extended range IDC.

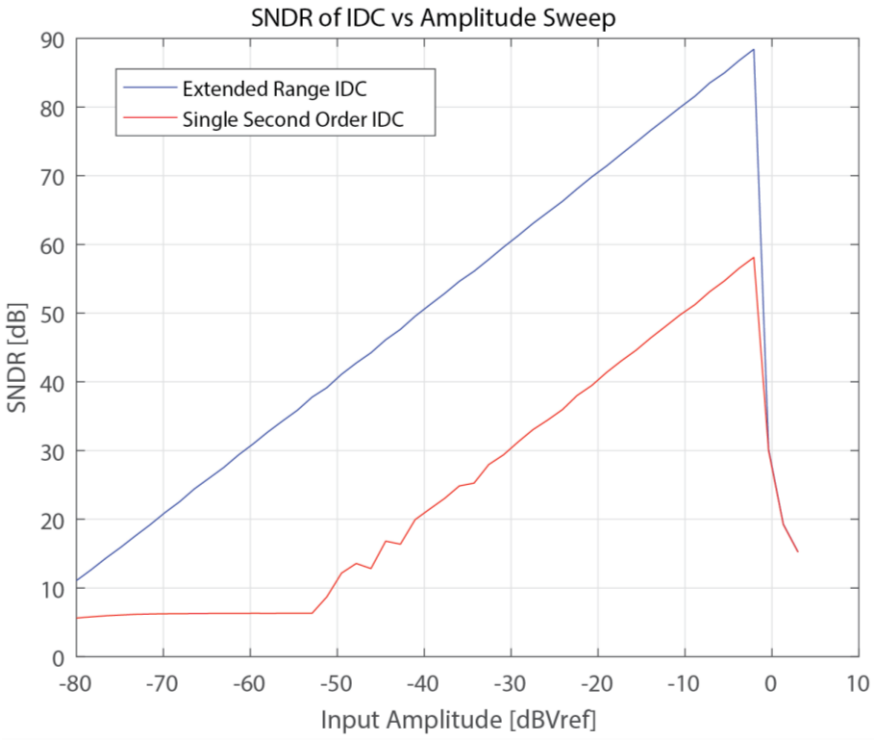

Figure 2.27: SNDR vs amplitude of the extended range and first-stage IDC.

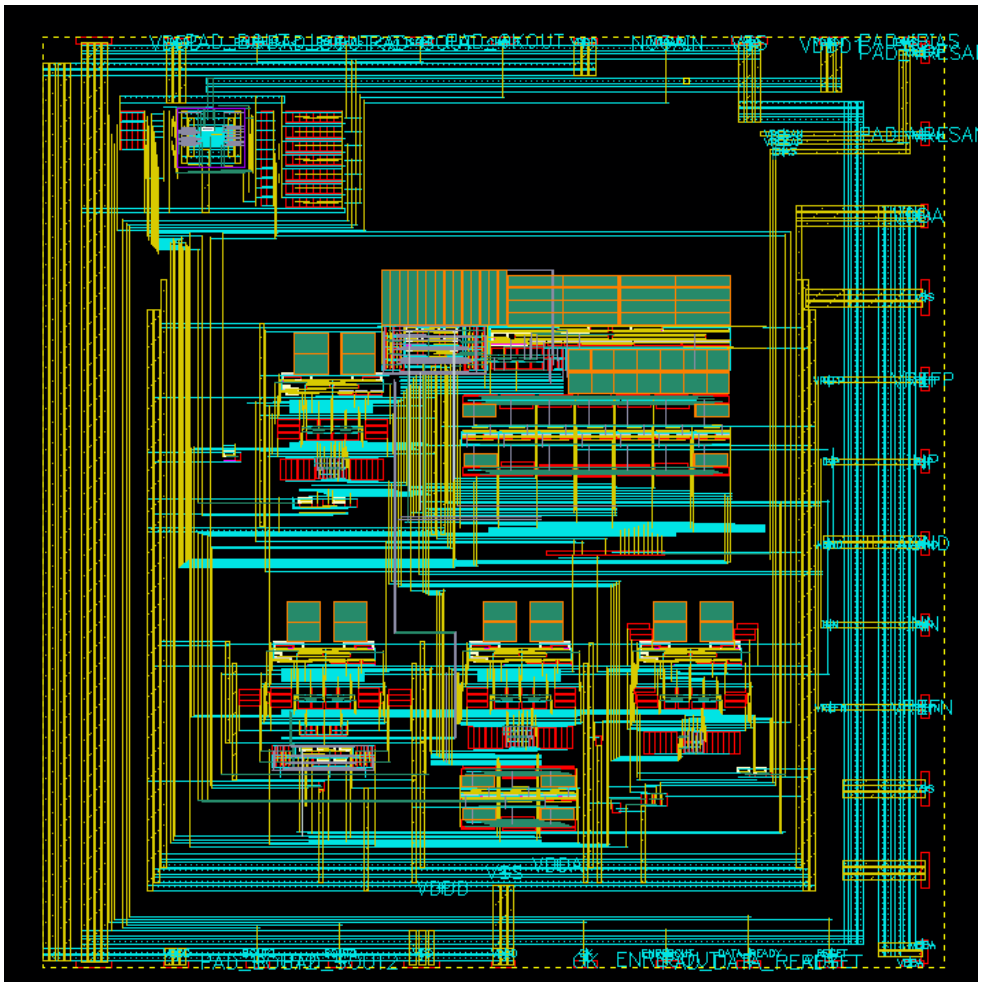

Figure 2.28: Design layout Core

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Part III

3.1 Introduction

3.2 DC/DC Converters

3.3 Description of the realized system

3.4 Arduino microcontroller

3.5 Circuit implementation

3.6 Measurements

3.7 Conclusion

3.1 Introduction

The object of this project concerns the study and design of a power-up and control system for an ultrasonic clean machine, or more commonly called ultrasonic washing machine. It is used in several industries, including medical, dental and optical operations tools. Solvents as water and many other types are used as cleaning media.

Ultrasonic washing machines are made up of a tank filled with a detergent solvent, an electronic generator and one or more piezoelectric transducers, which are mechanically connected to the tank and electrically to the generator.

In the basic operation of ultrasonic washing machines, high frequency signals are applied to the detergent solvent, so the waves applied generate different pressures effect which causes the cavitation phenomenon, or the formation of gaseous cavities called microbubbles. The energy generated by the imbalance of the microbubbles depends on the period by which the vibrating wave is repeated and then on the oscillation frequency of the piezoelectric transducers [1]. This energy decreases as frequency increases. Therefore, for coarse cleaning, a low frequency is better, while for fine and very accurate cleaning a higher frequency is preferable.

The ultrasonic washing mechanism requires applying a high frequency voltage to the electrical terminals of the transducers, which react by creating mechanical vibrations. These vibrations propagate inside the tank producing vibrating waves between the surface of the objects and the detergent solvent. The position of the transducer in the tank is a critical issue. It can be bonded to the tank or mounted in stainless steel housing for vibrating in the tank. The frequencies used in commercial ultrasonic washing machines are varying from 20 to 60 kHz, commonly 40 kHz. the power is commonly 200W, depending on the tank capacity.

Ultrasonic washing machines are used in many areas where precision is required in cleaning, it is the most effective way to remove impurities from solid complex objects. It can be used, for example, in:

- Mechanical workshops for degreasing frames, precision gears, bearings, steel ball wheels and mechanical parts of motors;
- Electronic laboratories for cleaning electronic cards;
- Biology laboratories to remove residues in glass tubes, graduated cylinders of different capacity;
- Medical studies to remove residues in medical irons and surgical scalpels.

3.1.1 Concept

The main block diagram of an ultrasonic washing machine, consisting of a tank and a power-up system, is shown in Figure 3.1. The piezoelectric transducers are mechanically connected to the bottom surface of the tank and are powered by a square wave voltage which is supplied by the power supply system. The amplitude and frequency of the square wave depend on the amount of solvent and the size of the inserted object inside the tank. The power up supply system is responsible to supply an output of square wave adjustable in amplitude and frequency.

In addition, the power needed by the piezo transducers is supplied by the power supply system, which should regulate the output voltage and frequency as well as limit the distortion of the waveform for current and input voltage.

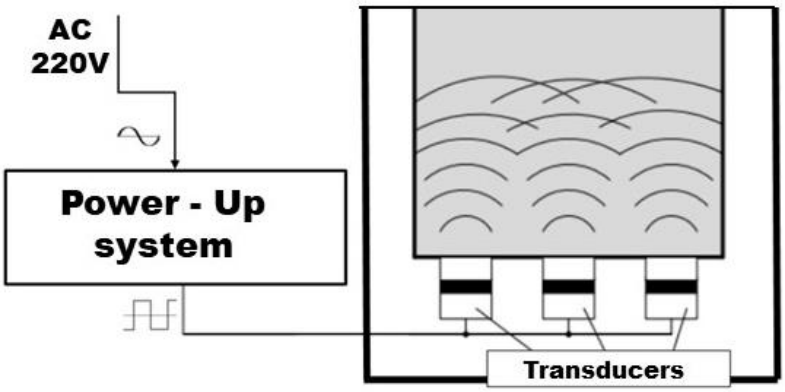


Figure 3.1: block diagram of the ultrasonic washing machine.

Figure 3.2, shows the power supply system block diagram. It consists of three different types of DC/DC converters and a half-bridge inverter providing voltage to the tank.

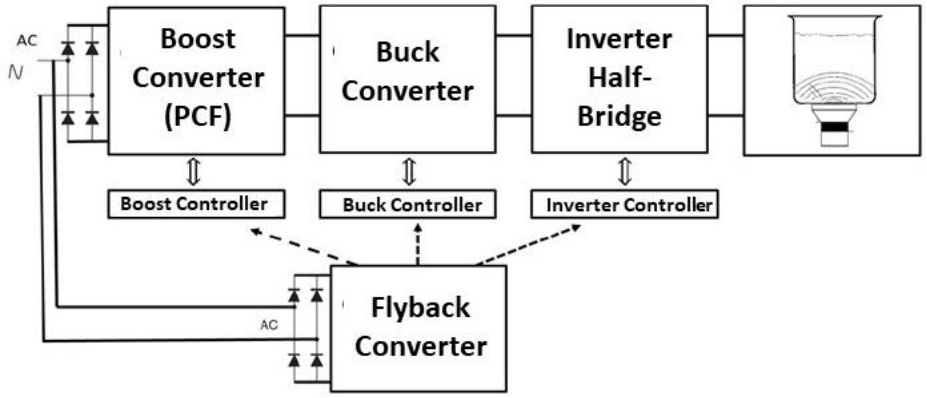


Figure 3.2: power supply system block diagram

3.2 DC/DC Converters

Huge amount of DC/DC converters are used daily in various electronic devices and systems, these converters are different in their operation and topologies. Despite the variation of the DC/DC converters operation, most of them are developed from three main basic topologies which are: Boost converter, buck converter and buck/boost converter. There are different ways to classify DC/DC converters. One of them is to classify PWM DC/DC converters into isolated converters and non-isolated converters. The buck converter is a typical example of non-isolated converter, while transformers are commonly used to provide the galvanic isolation, for example in flyback converters.

DC/DC converters are used to transfer power from the source to the transducers by converting current and voltages from one form to another. A control system has the role of managing the power transfer process with the goal of achieving maximal output power, power conversion efficiency, good power density and high energy efficiency for the power supply system [2]. An important consideration is the reduction of size, weight and cost. In high power supply applications, DC/DC converters are more efficient. The circuit typically performs the conversion by applying DC continuous voltage to an inductor for a certain period (normally with frequencies from 50kHz to 5MHz), where current flows to store magnetic energy. When the current is removed from the inductor, the stored energy is transferred to the output voltage. The ratio between the ON and OFF time in the conversion is used to regulate the output voltage. This conversion method is very efficient (between 80% and 95%), unlike the linear method that at the same power level has lower efficiency.

A main disadvantage of switching converters is electric noise generated at high frequencies, which can be limited by special filters.

3.2.1 Buck Converters

The buck converter is characterized by an output voltage lower than the input voltage, so it is also called step-down converter. The input source can be a DC or a rectified AC source. In addition, the load can be a device or any equipment or operating system with a constant supply voltage.

The buck conversion, ideally illustrated in figure 3.3, consists of single-pole double-throw (SPDT) switch and ideal low pass filter (LPF). The basic operation depends on closing the switch in one direction for period T_{on} and then close it in the other direction for T_{off} where $T_{off} = T_s - T_{on}$, T_s being the full switching period. The ratio between T_{on} and T_s is defined as the duty cycle D of the SPDT switch.

$$D = \frac{T_{on}}{T_s}$$

Similar is the ratio of T_{off} to T_s

$$D' = \frac{T_{off}}{T_s}$$

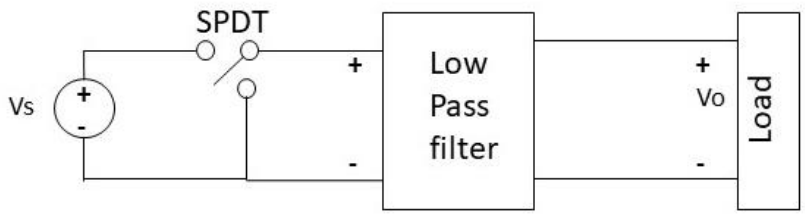


Figure 3.3: Step-down conversion block diagram

The switch transforms the input voltage V_s into a square waveform which is applied to an ideal low pass filter. Using Fourier series expansion, if the cut-off frequency of the ideal low pass filter is lower than the main frequency, the harmonic components are removed, and the dc voltage only appears at the output of the low pass filter:

$$V_o = D\,V_s$$

In the ideal DC-DC conversion, the circuit delivers a DC voltage to the load without any harmonics, due to the ideal characteristics of the low pass filter. The duty cycle is controlling the ratio between the output and the input voltages. Since the duty cycle is always D < 1, the conversion is step-down.

In a real buck converter, the SPDT switch can be replaced by semiconductor switch and an LC filter is used instead of the ideal low pass filter, as shown in figure 3.4. A MOSFET switch can be used for S1, which switches ON and OFF, while a diode is used for the other switch. When the MOSFET switch is ON, the diode is OFF, whereas, when the MOSFET is OFF, the diode turns ON. The LC structure provides filtering close to the ideal condition. The resistor is acting as load.

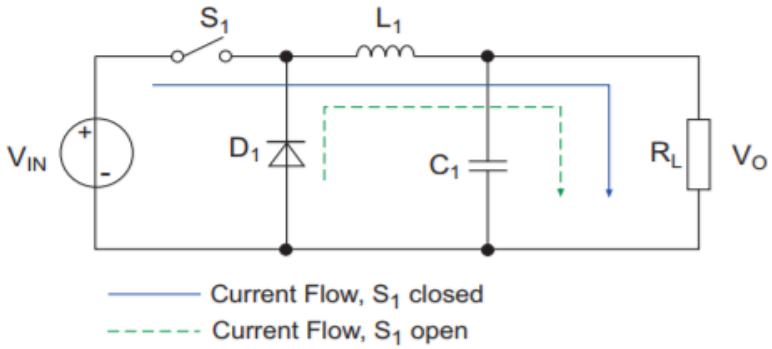


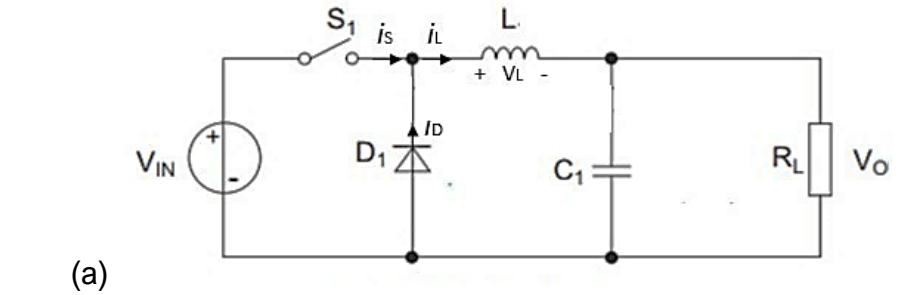
Figure 3.4: Buck converter operation circuit.

The LC filter cannot remove the high frequency components completely and the output voltage V_o contains an AC component which is called output voltage ripple. By a simple frequency domain analysis, it is easy to determine the output ripple which appear because of the non-ideal behavior of the LC filter. The transfer function of the LC filter is given by:

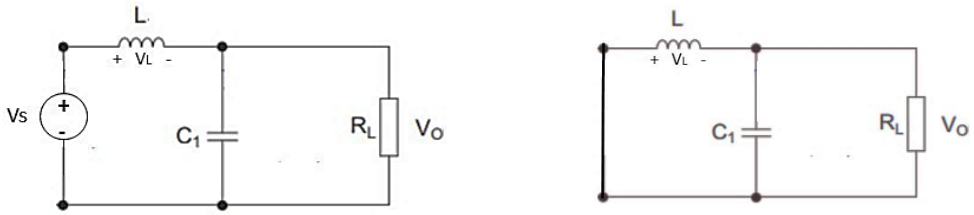
$$\mathrm{F}(s) = \frac{V_o(s)}{V_x(s)} = \frac{\frac{1}{sC} \parallel R}{sL + \frac{1}{sC} \parallel R} = \frac{1}{1 + \frac{s}{Qw_o} + \frac{s^2}{{w_o}^2}}$$

where $V_x(s)$ is the voltage difference over the diode and w_o is the pole frequency $w_o = \frac{1}{\sqrt{LC}}$.

In the steady-state analysis of the buck converter, the output voltage V_o of the converter is considered to be a constant during both ON/OFF time of the switch, Figure 3.5 and Figure 3.6 show the buck converter and both ON-time circuit and OFF-time circuit as well as the waveforms.



(a)



$D\ T_s$ $(1-D)\ T_s$

(b) ON-Time circuit OFF-time circuit

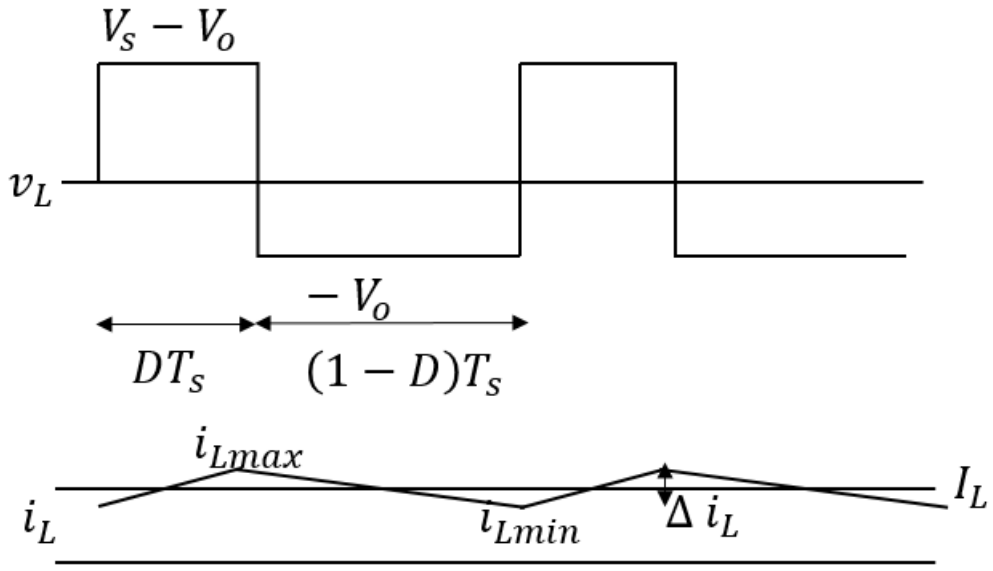
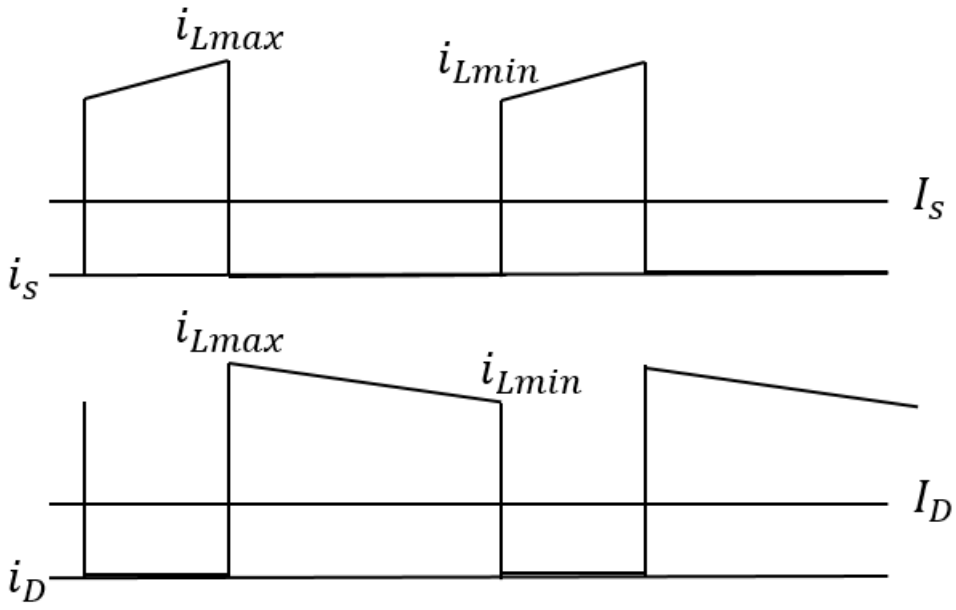


Figure 3.5: (a) Buck converter, (b) ON/OFF circuits.



(c)

Figure 3.6: Waveforms of buck converter.

3.2.1.1 Continuous conduction mode

In continuous conduction mode (CCM), the current is circulating through the inductor during both the ON and OFF periods. When the switch is closed for T_{on}, the current flow through the inductor results in a positive voltage, while when the switch is open the current flows through the diode leading to a negative voltage drop across the inductor. The voltage across the inductor can be determined by:

$$V_L(t) = V_s - V_o \qquad \text{at ON-time case}$$

$$V_L(t) = -V_o \qquad \text{at OFF-time case}$$

By applying a balance condition to get the relationship between the input voltage and the output voltage during both periods:

$$(V_s - V_o)\, DT_s = V_o(1-D)\, T_s$$

Simplifying we obtain:

$$V_o = D\, V_s$$

The equation gives the final voltage gain which guarantees that the current through the inductor is the same at the beginning and the end of the period.

The current which flows through the inductor can easily derived as:

$$i_L(t) = \frac{v_L(t)}{L}\, t = \frac{V_S - V_o}{\mathrm{L}}\, t \quad \text{For ON-time period}$$

$$i_L(t) = \frac{v_L(t)}{L}\, t = \frac{-V_o}{\mathrm{L}}\, t \qquad \text{For OFF-time period}$$

From both equations, the inductor current increases during the ON-time period and decreases during the OFF-time period leading to a triangular waveform, as shown in Figure 3.5 (c). The average value of the inductor current can be determined by considering the average value of current through capacitor as zero, so that the inductor current is equal to the current flowing in the resistor:

$$i_L(t) = I_L = \frac{V_o}{R}$$

The average value of the inductor current is the difference between the maximum and minimum values of the current flowing in the conductor.

$$\Delta i_L = \frac{v_L}{L}\Delta t = \frac{V_s - V_o}{\mathrm{L}} DT_s = \frac{V_o}{\mathrm{L}} (1-D)\, T_s$$

From this equation, the maximum inductor current value is:

$$i_{Lmax} = I_L + \frac{1}{2}\Delta I_L$$

while the minimum inductor current is:

$$i_{Lmin} = I_L - \frac{1}{2}\Delta I_L$$

The inductor current flows through the switch during the ON-time period, and through the diode in the OFF-time period. The average value of the switch current i_s and diode current i_D are given by:

$$i_S(t) = I_S = D\, I_L$$

$$i_D(t) = I_D = (1-D)\, I_L$$

The voltage ripple is influenced by the LC filter and, in particular, on the capacitor. As stated before, the inductor current has a triangular waveform, which consists of DC and AC components. The DC components flow through the load as the capacitor has a large impedance for the DC current. While the AC components flow mostly through the capacitor, a large capacitor value. is used, as shown in figure 3.7.

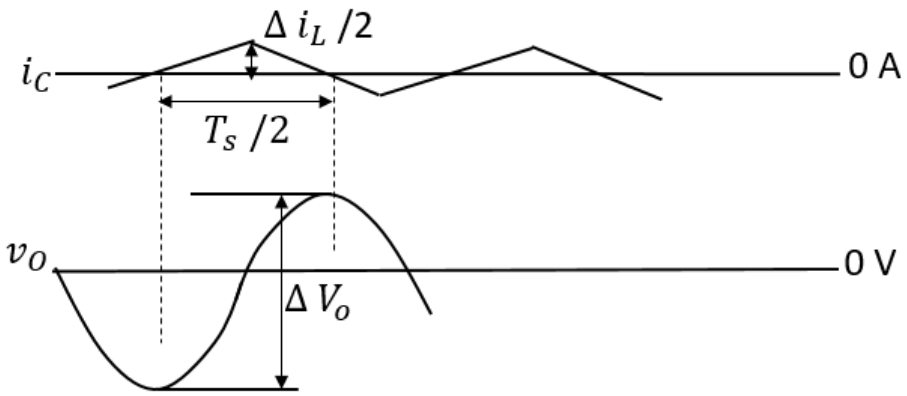


Figure 3.7: Output ripple in voltage and current.

The triangular current is flowing through the capacitor developing a ripple component over the DC output voltage. The AC voltage across the capacitor comes from:

$$v_{ac}(t) = \frac{1}{C}\int i_C(t)\, dt$$

where i_C is the current through the capacitor.

The voltage v_{ac} increases during the T_{on} period where the current through the capacitor is positive and it decreases during T_{off}. Therefore, by integrating i_C over the full switching period, the average voltage v_{ac} becomes:

$$\Delta v_{ac} = \frac{1}{C}\left(\frac{1}{2}\right)\left(\frac{1}{2}\Delta\, i_L\right)\left(\frac{1}{2}\, T_s\right)$$

By substituting Δi_L:

$$\Delta i_L = \frac{V_o}{\mathrm{L}}\,(1-D)\,T_s$$

we obtain:

$$\Delta v_{ac} = \frac{V_o}{8\mathrm{LC}}\,(1-D)\,{T_s}^2$$

The voltage swing Δv_{ac} is corresponding to the magnitude of the ripple component.

The operation of the buck converter in CCM is simple. However, it requires that the current in the inductor remains positive during the whole switching period. If this is not the case, the buck converter operates in discontinues conduction mode (DCM).

3.2.1.2 Discontinues conduction mode

If, during T_{off} the inductor current reaches zero the buck converter enters the so called discontinuous conduction mode (DCM). DCM operation depends on the duty cycle D and also on the load resistor, the DCM voltage gain is proportional to the load resistor and increases by the increasing the resistor value. As the load resistor is changing, the slope of the inductor current during the ON-time varies. During the OFF-time period, $I_L < \frac{1}{2}\Delta i_L$ and at a certain point the inductor current becomes zero, switching off the diode until the next ON-time period.

The operation mode of the buck converter can be determined as:

- $I_L < \frac{1}{2}\Delta i_L$: DCM
- $I_L > \frac{1}{2}\Delta i_L$: CCM
- $I_L = \frac{1}{2}\Delta i_L$: In between CCM and DCM

In most applications, the buck converter is used with constant input voltage while the output voltage varies according to the voltage requirement of the system. The borderline between CCM and DCM with constant V_s and variable V_O is obtained by imposing that the inductor current goes to zero at the end of each period, giving

$$I_L = \frac{1}{2}\,\Delta i_L \rightarrow I_L = \frac{DT_s}{2L}\,(V_s - V_o)$$

From $V_o = DV_s$ and $I_O = \frac{1}{2}\,I_L$:

$$I_O = \frac{V_O}{\mathrm{R}} = \frac{V_s T_s}{2\mathrm{L}}\,D(1-\mathrm{D})$$

From the last equation, the critical values of the load resistor or of the inductor can be determined to indicate the borderline between CCM and DCM:

$$R_{crit} = \frac{2L}{(1-\mathrm{D})\,T_s}$$

$$L_{crit} = \frac{(1-\mathrm{D})\,R\,T_s}{2}$$

R_{crit} and L_{crit} enable to determine the operation mode of the buck converter. When the load resistor is bigger than R_{crit} for a given value of inductance or when the inductor is less than L_{crit} for a given value of resistance, the converter enters the DCM operation.

3.2.1.3 Close loop control for buck converter

In real applications, DC/DC converters are powered by a non-ideal voltage source. In addition, converters are loaded with different electrical loads, not just a resistor. DC/DC converters can suffer different variations in the input source voltage and load current. The converter should maintain its output voltage at the desired value, whatever changes occur in the input voltage or load current. An output voltage regulation or simply DC regulation is needed to regulate the output voltage of a converter at a fixed DC value. A closed-loop feedback control must exist between the output and the active switch to do the DC regulation through the duty ratio of the converter [4].

Figure 3.8 shows a simplified diagram of the buck converter with a closed-loop feedback controller. The feedback controller consists of two functional blocks: the pulse width modulator (PWM) and the regulator. The PWM adjusts the duty-cycle of the active switch based on the output of the regulator depending on the feedback from the converter.

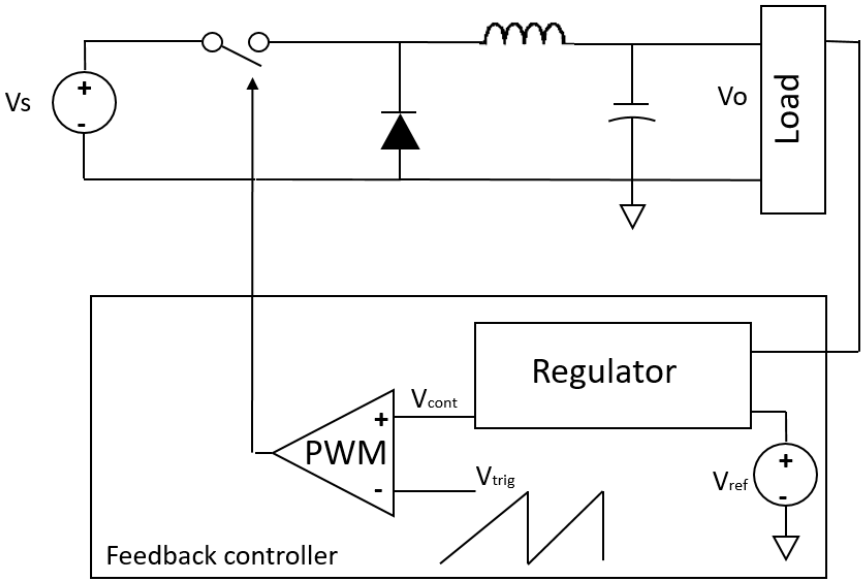


Figure 3.8: Block diagram of the closed loop feedback.

The output of the PWM is pulse-width-modulated to adjust the duty cycle of the switch as in figure 3.9. The timing diagram shows that a periodic triangular signal is used inside the feedback control loop where the period of the triangular signal is the switching period of the converter. The switch is ON when the signal is rising. When the value of the signal is larger than the control voltage, the switch is in OFF condition. In this case, the pulse width is modulated in proportion to the magnitude of the control voltage V_{cont}.

The analog implementation of the PWM modulator is basically a comparator, as shown in Figure 3.8, where the inverting input of the comparator is connected to sawtooth or a triangular wave carrier signal. while the control signal is applied at the non-inverting input. When the control signal is larger than the carrier signal, the output of the comparator switches to a high level, while when the signal drops below the carrier signal, the output of the comparator switches to a low level, producing a square wave. The carrier signal has a frequency equal to the switching frequency.

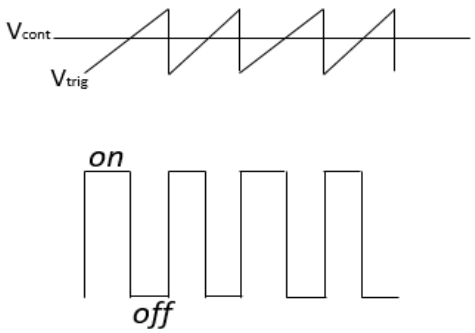


Figure 3.9: timing diagram

In a DC-DC converter the output voltage is not affected only by the duty cycle of the PWM modulator, but also by:

- Input voltage.
- Mode of operation of the converter (CCM or DCM).
- Output current in both modes CCM or DCM
  →In CCM, it depends on the voltage drop on semiconductor switch and the effect of the parasitic resistors in the circuit.
  →In DCM, the conversion ratio between input and output voltage depends on the load value.
- Other factors as ESL and ESR of the output capacitors.

A negative feedback closed loop control system is typically used, as shown in Figure 3.10, in which the output voltage is compared with reference voltage value. The error generated by the summing node enters a regulator, which provides the input modulating signal to the PWM. In turn, the PWM stage provides the switch control signal. This signal may have too low voltage value to directly control the opening and closing of the switch transistor. In these cases, a driver is interposed between the converter and the modulator.

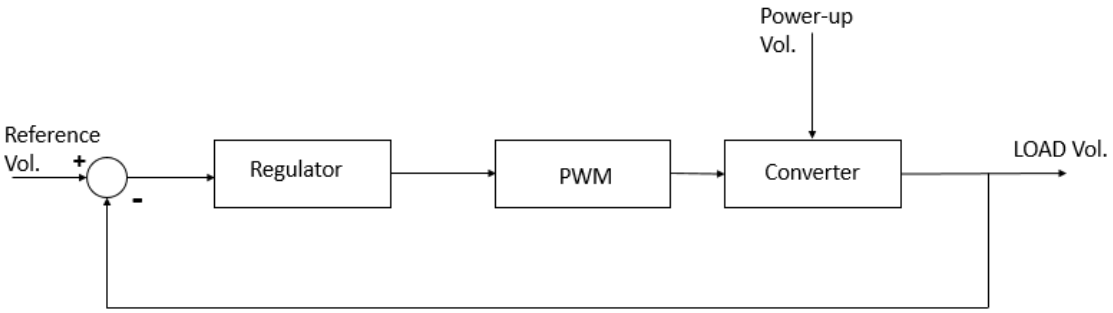


Figure3.10: control scheme of a DC/DC converter.

Figure 3.11 shows the block diagram of the closed loop control of the converter voltage. In a real regulator, the output signal U_o usually has is scaled down with a resistive divider before feeding it to the regulator, as shown in figure 3.12, while the reference signal U_0^* has a constant value. The desired output voltage is achieved by choosing proper values for R_1 and R_2 in the resistive divider [5].

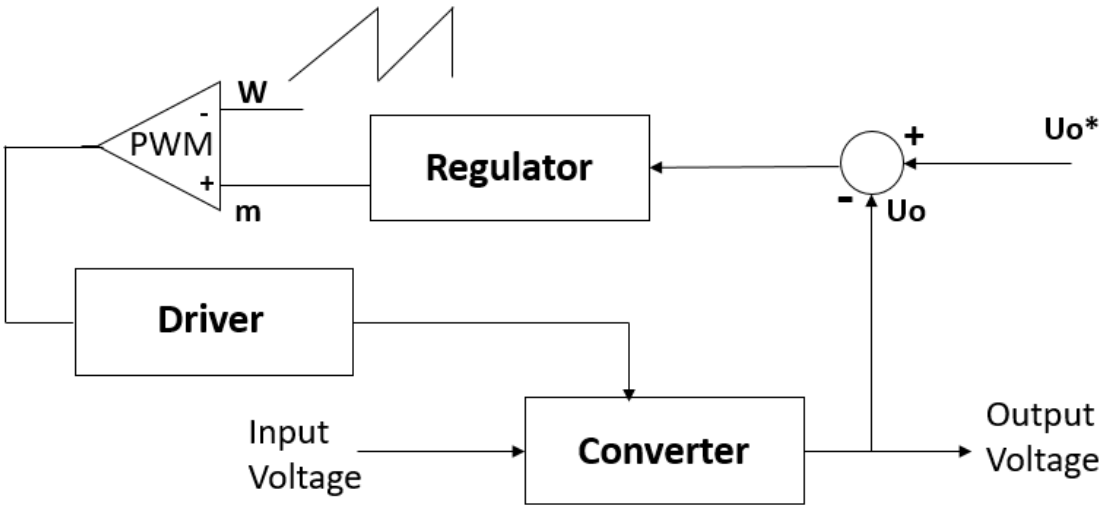


Figure 3.11: control loop of a DC/DC converter

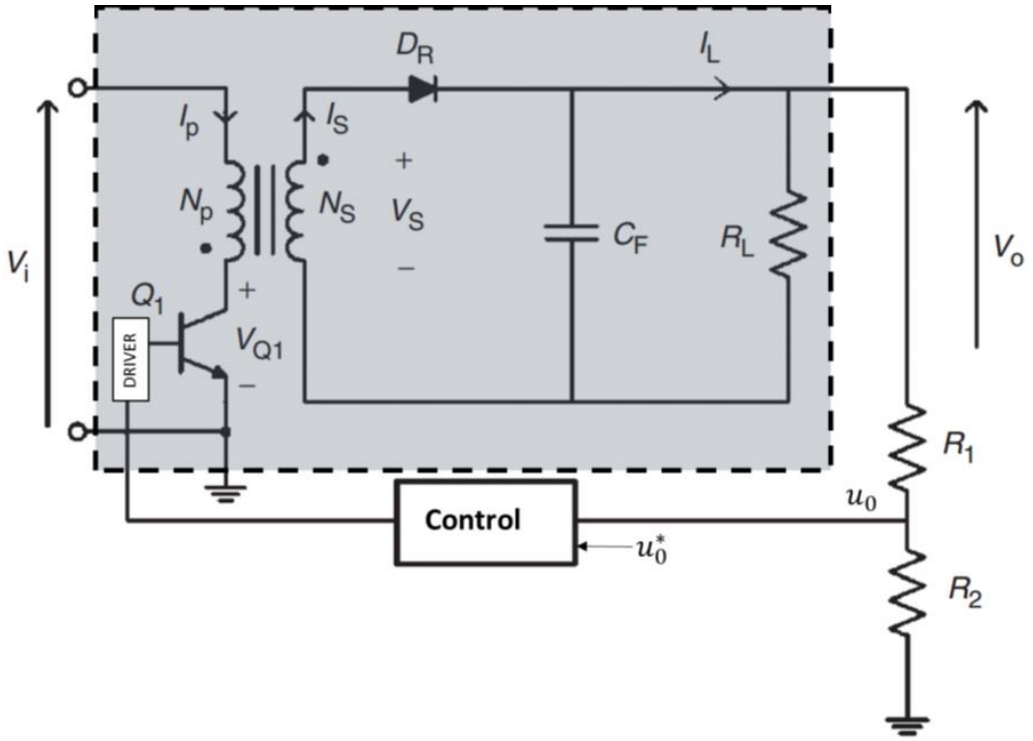


Figure 3.12: example of control the voltage in Flyback converter.

In conventional converter designs, the power stages are designed first, to determine the inductor and filtering capacitor parameters to achieve the desired static and dynamic ripples and then the analysis of the transfer function is performed to compensate the system.

The overall system should ensure good stability and high precision. Usually, the proportional controller is not used because it leads to instability, while the proportional-integral (PI) and the proportional-integral-derivative (PID) are typically used. The proportional-integral (PI) controller guarantees a good precision and stability, however the dynamics of system are slow, with a slow response time compared to the open loop system. The most used system is the PID controller, which has a good dynamic performance, but needs careful design to guarantee the stability of the system. A PID controller can be implemented using operational amplifiers as shown in figure 3.13.

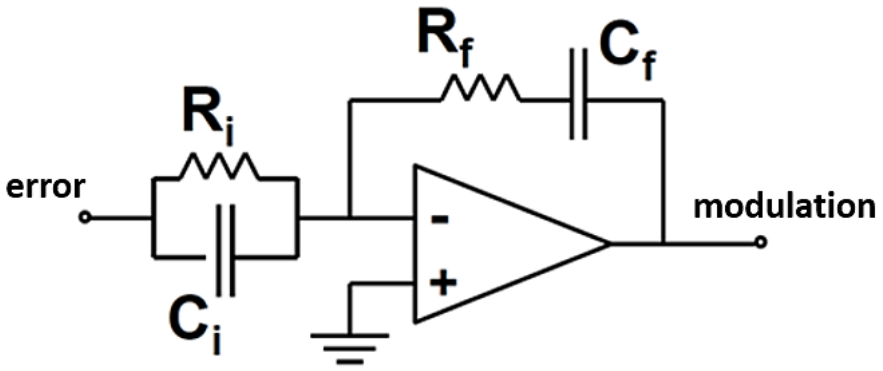


Figure 3.13: PID control loop

The transfer function of the PID control is given by:

$$G(s) = K_p + \frac{K_i}{s} + K_d = -\frac{R_f}{R_i}\,\frac{(1 + s\,R_f\,C_f)(1 + s\,R_i\,C_i)}{s\,R_f\,C_f}$$

in which

$$K_p = \frac{R_f}{R_i} + \frac{C_i}{C_f} \qquad K_i = \frac{1}{R_i\,C_f} \qquad K_d = R_f\,C_i$$

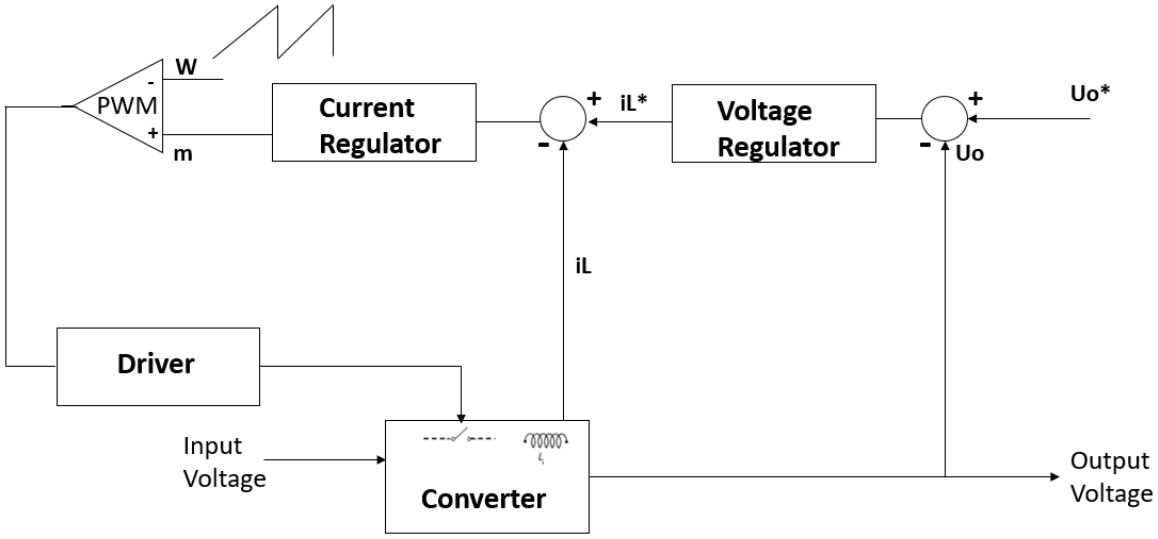


Figure3.14: block diagram of the converter with voltage and current control loop.

Another type of control method used in DC/DC converters is to simultaneously regulate the voltage and the current, as shown in figure 3.14. In this diagram, the voltage compensated error is used as reference to be compared with the current in the main inductor of the converter. In fact, as shown in the previous paragraphs, the current in the inductance plays

a fundamental role in determining the ratio between input voltage and output voltage. For this reason, adding a second feedback, the dynamic response is noticeably improved.

3.2.1.4 Power factor correction

The types of electrical loads are typically linear and nonlinear, the linear loads are divided into three categories:

- Resistive
- Inductive
- Capacitive

- **Resistive loads**: resist current flow linearly and cause heat.
- **Inductive loads**: resist changes in current and as such, when current is measured, it lags the voltage. Electromagnetic fields are the key to inductive loads, and as such all motors (fans, pumps, etc), solenoids, and relays are inductive in nature. The inductive loads lead to active power and reactive power. The active power is related to the work actually done by the device (for example by a motor). The reactive power is drawn from the source to produce magnetic fields. The total apparent power consumed (product between current and voltage) is the combination of active and reactive power and is measured in VA (volts-amperes).
- **Capacitive loads**: resist changes in voltage, and hence the voltage lags the current (or more commonly said "current leads voltage"). A capacitor consists of two conductive surfaces separated by an insulator, which store charge. When voltage is first applied, current is very high, but drops as the voltage increases. Like inductive loads, capacitive loads also introduce reactive power, but it has opposite the polarity with respect to an inductive load. Capacitive loads are not very common, but things like a flashbulb or a heart defibrillator might be considered a capacitive load.

In these linear elements, in sinusoidal regime, the absorbed current is a sine wave and has the same frequency as the voltage. The relationship between voltage and current is given by the Ohm's law. Depending on the reactive load component, there is a phase-shift φ between voltage and current.

Nonlinear loads consist of elements that exhibit nonlinear characteristics, such as semiconductor elements. In sinusoidal regime, these loads absorb a periodic current consisting of the sum of:

- a sinusoidal current called fundamental at the same frequency as the voltage;
- sinusoidal currents of lower amplitude and with integer multiple frequencies of the fundamental frequency, called harmonics.

Current harmonics create a disturbance to the power line, causing distortion of the waveform of the voltage, additional heating, and over-voltages (due to resonance situations) in electrical distribution and power systems.

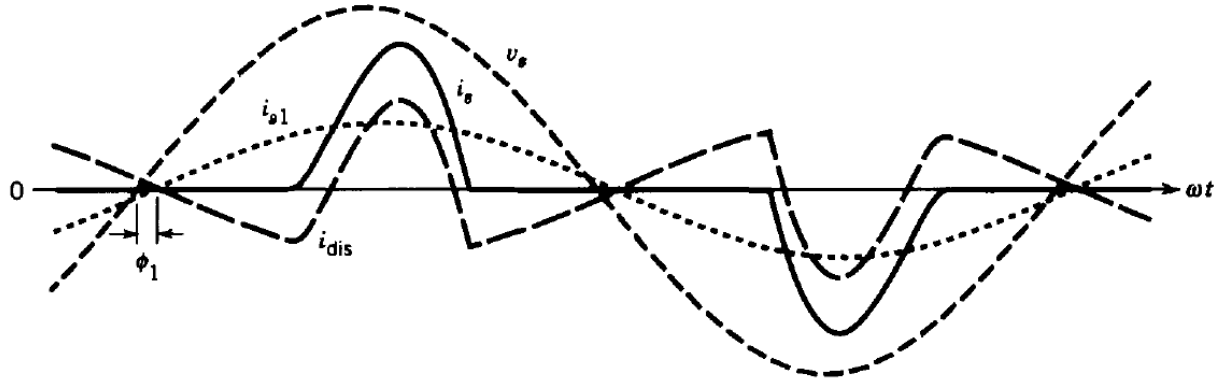


Figure 3.15: nonlinear load current and voltage distortion.

Figure 3.15 shows the input voltage and input current of a rectifier bridge (nonlinear). The voltage can be considered a sine wave because its distortion is small [6]. Current is the sum of its Fourier harmonics:

$$i_s = i_{g1}(t) + \sum_{h\neq 1} i_{sh}(t)$$

where i_{g1} is the fundamental component, i_{sh} is the harmonic component.

The magnitude of the distortion signal is identified as Total Harmonic Distortion(THD) which is given by:

$$THD = \frac{\sqrt{{I_s}^2 - {I_{g1}}^2}}{I_{g1}} = \sqrt{\sum_{h\neq 1} (\frac{I_{sh}}{I_{g1}})^2}$$

The average power is derived from the following equation:

$$P = \frac{1}{T}\int_0^t v_s(t)\ i_s(t)dt = V_s I_{s1}\cos\varphi_1$$

In case of the sinusoidal voltage signal, the average active power depends only on the effective voltage value and the effective value of the fundamental component of the current signal. The apparent power is the product of the effective voltage and effective current.

$$S = V_s I_s$$

The power factor is the ratio between the average active power and the apparent power, from last two equations mentioned before:

$$PF = \frac{I_{g1}}{I_s}\cos\varphi_1$$

From the equation, it is evident that a large distortion in the waveform of the current translates into a small value of $\frac{I_{g1}}{I_s}$, from which a low power factor.

Displacement power factor (DPF) is corresponding to the power factor in the linear circuit, with sinusoidal voltage and current signal is defined as the angle φ_1 of the cosine.

In recent years, various standards and regulations have imposed to limit the introduction of current harmonics to maintain decent quality of power. Diode rectifiers are used to interface the power electronics with the power supply. But diode rectifier introduces harmonics that can exceed the limits imposed by the regulations. This poses a problem when low voltages are required and has a detrimental effect, even on the electronic power equipment as:

- Reduce the power available at the wall outlet.
- The capacitor at the DC side is strongly affected by the current pluses.
- The losses in the rectifier bridge diodes are higher since the direct voltage drop on the diode depends on the current.

3.2.1.5 Power factor correction in power converters

The term PFC (Power Factor Correction) refers to an electronic DC/DC converter that performs the power factor correction. By applying a current control to the power converter, it is possible to make the input current absorbed by the rectifier bridge sinusoidal and in phase with the input voltage. A boost converter is used in this project which is suitable due to its ability to absorb less distorted current.

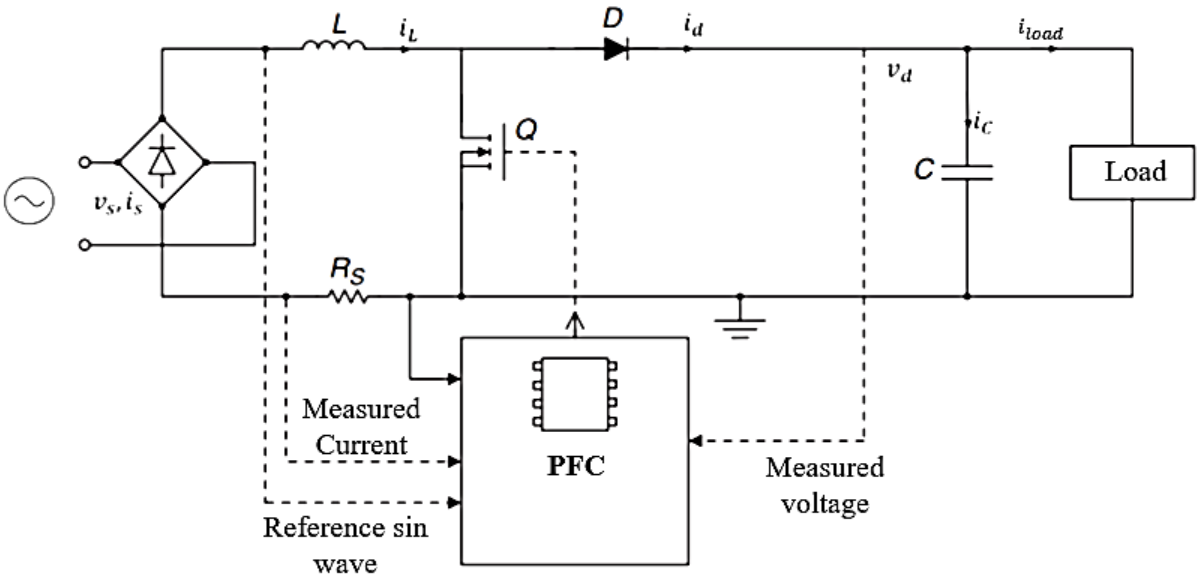


Figure 3.16: boost converter with PFC control

Figure 3.16 shows a boost converter with a PFC control. The capacitor C has the role of minimizing the voltage ripple vd and meeting the demand for power by the power electronics system. The current at the load i_{load} can be considered continuous, thanks to the large value of the capacitor C. It represents the current supplied to the rest of the system.

To achieve a high-power factor, the input current i_s at the rectifier bridge should have the same form as the voltage v_s, this means that at the output of the rectifier bridge, $\| v_s \|$ and i_L should feature the same waveform. The basic principle of operation can be derived from the block diagram shown in Figure 3.17.

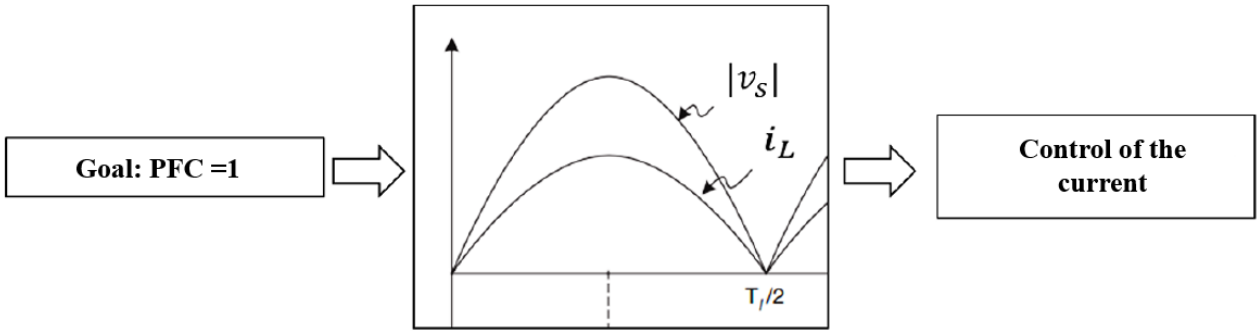


Figure 3.17: principle of PFC

As the input current is increasing and needs to be controlled, the converter itself is working in current mode control. Figure 3.18, shows the block diagram of a closed loop control in which i_L has the same waveform as $\| v_s \|$ and the reference sinusoidal wave or the desired current value i_L.

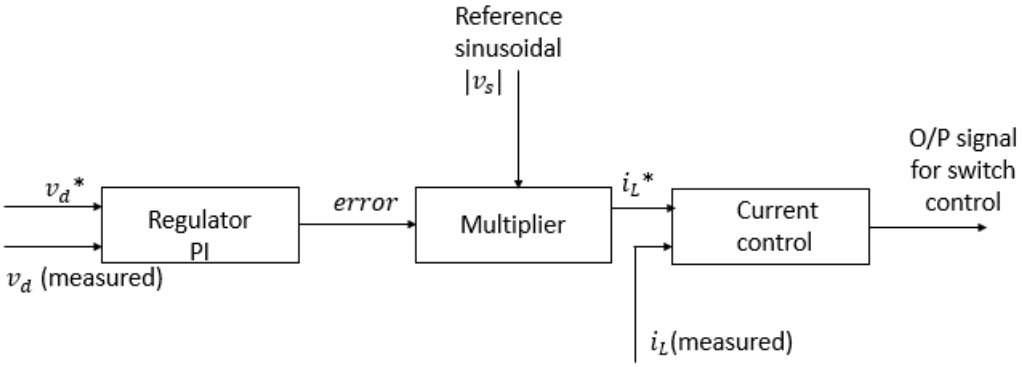


Figure3.18: block diagram of PFC control scheme.

The amplitude of the current i_L* must be such as to adjust the output voltage to the desired level and can be determined by PI control. The waveform of i_L* is obtained by measuring the voltage $|v_s|$ usually by a resistor divider and then multiplied by the error between the reference value v_d* and the actual measured value v_d. The real current i_L is obtained by measuring the voltage at the resistor R_s in Figure 3.16. The switch state in the converter is determined by comparing the real current i_L to i_L*. Once i_L and i_L* are known, there are several ways to implement the current control of the driver.

When i_L reaches i_L*, the converter switch is opened. The switch is closed by a clock signal that has a constant frequency. During a switching frequency period, it is assumed that the output voltage v_d is constant and that the input voltage of the converter is constant over that time interval. the peak-to-peak value of the current ripple within each switching frequency period can be obtained from the relation between t_{on} and t_{off}:

$$t_{on} = \frac{L_d I_{rip}}{|v_s|}$$

$$t_{off} = \frac{L_d I_{rip}}{v_d - |v_s|}$$

The switching frequency is given by:

$$f_s = \frac{1}{t_{off} + t_{on}} = \frac{(v_d - |v_s|)|v_s|}{v_d \; L_d I_{rip}}$$

As f_s has a constant value, the current ripple can be obtained in function of $|v_s|$:

$$I_{rip} = \frac{(v_d - |v_s|)|v_s|}{v_d \; L_d . \; f_s}$$

From this equation, it is obvious that the ripple current is inversely proportional to the switching frequency. For this reason, in practical application f_s value is chosen much higher than the network frequency.

Figure 3.19, shows the input current flow in the boost converter with a constant frequency. The maximum ripple value is at $|v_s| = \frac{1}{2} v_d$:

$$I_{rip,max} = \frac{v_d}{4\, L_d\, f_s}$$

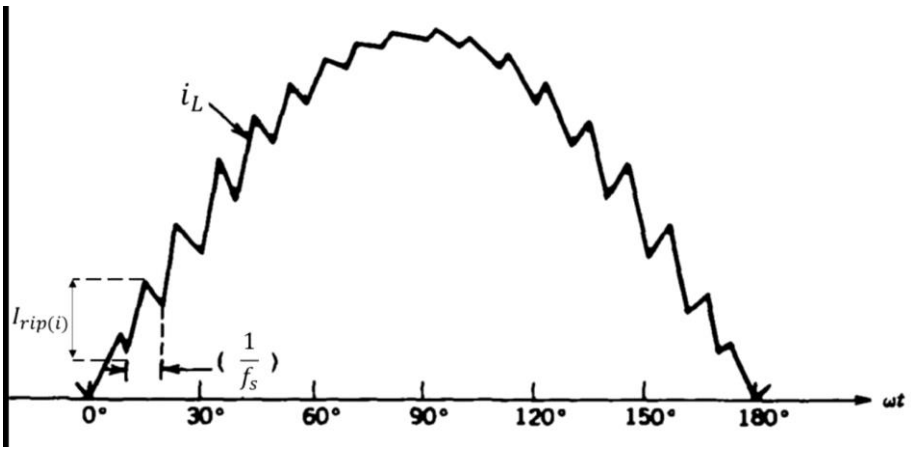


Figure 3.19: current control in PFC for boost converter at constant frequency.

Another control mode is Average Current Control, which is based on the control of the average value of the current. Figure 3.20 shows a boost converter with the PFC control scheme at medium average current. As shown in the diagram, in addition to the voltage regulator, there is a current regulator. With this solution, the control signal of the switch is obtained by means of a compensation network that causes the ripple to oscillate around the average current value. The current value is determined by the multiplier which has a set logic value. In this control mode, the frequency is adjusted to be constant by the PWM modulator. The input current flow in the boost converter is now as shown in figure 3.21.

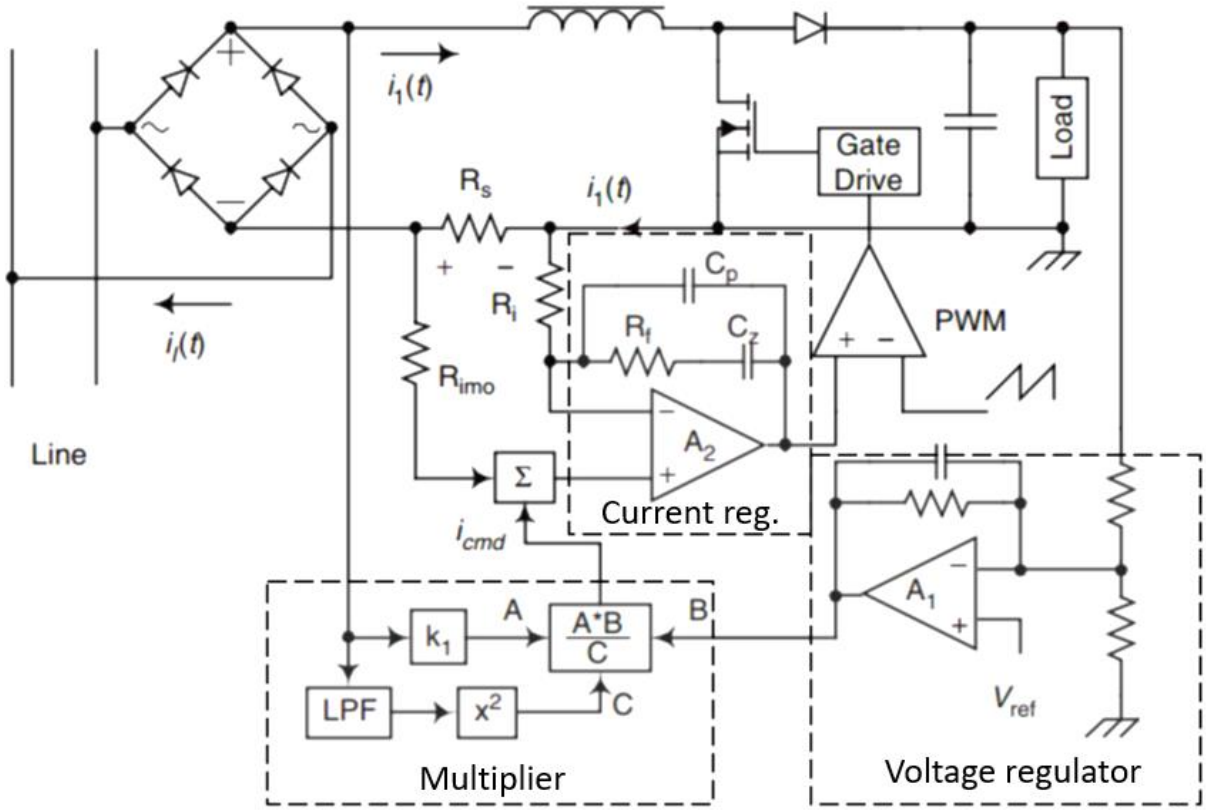


Figure3.20: average current control of PFC in boost converter

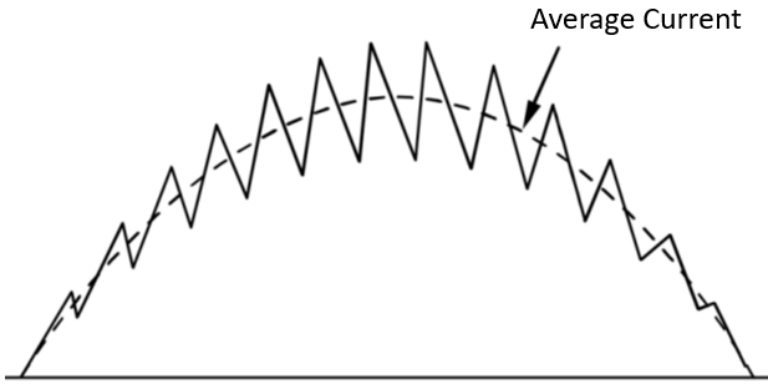


Figure 3.21: average current in boost PFC.

3.2.2 Boost converters

The boost converter main function is to step- up the input voltage to a higher value at the output. The boost converter is obtained from the buck converter by changing the switch location in the circuit diagram and rearranging the circuit to allow the charge flow from the source to the load branch.

In the CCM operation, the same techniques used in buck converter are used for circuit analysis. Figure 3.22 shows the boost converter and both ON-time circuit and OFF-time circuits as well as the waveforms shown in Figure 3.23. When the switch is closed for T_{on}, the current flows through the inductor, resulting in a positive voltage, while when the switch

is open the inductor current decreases with slope $(V_s - V_o)/L$. The voltage across the inductor can be determined by:

$$V_L(t) = -V_o \qquad \text{at ON-time case}$$

$$V_L(t) = V_s - V_o \qquad \text{at OFF-time case}$$

By applying a balance condition to get the relationship between the input voltage and the output voltage during both periods:

$$V_s \, . DT_s = (V_o - V_s)(1 - D) \, T_s$$

resulting in a voltage gain

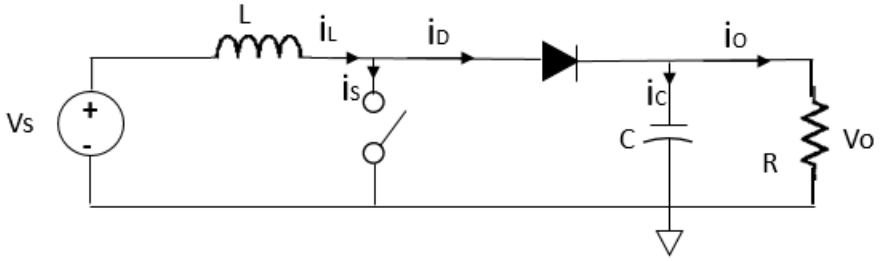
$$\frac{V_O}{V_s} = \frac{1}{1 - \mathrm{D}}$$

The expression of the gain is showing that the output voltage is always larger than the input voltage since the duty cycle D < 1. By applying the current analysis for the boost converter:

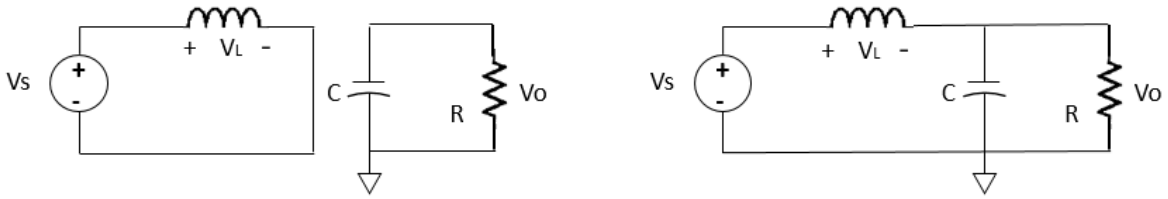
$$\Delta \, i_L = \frac{V_s}{\mathrm{L}} \, DT_s = \frac{V_o - V_s}{\mathrm{L}} \, (1 - D) \, T_s$$

$$I_S = D \, I_L$$

$$I_D = (1 - D) \, I_L$$



(a)



(b) $D \, T_s$ $(1 - D) \, T_s$

Figure 3.22: (a) the boost converter, (b) ON/OFF circuits

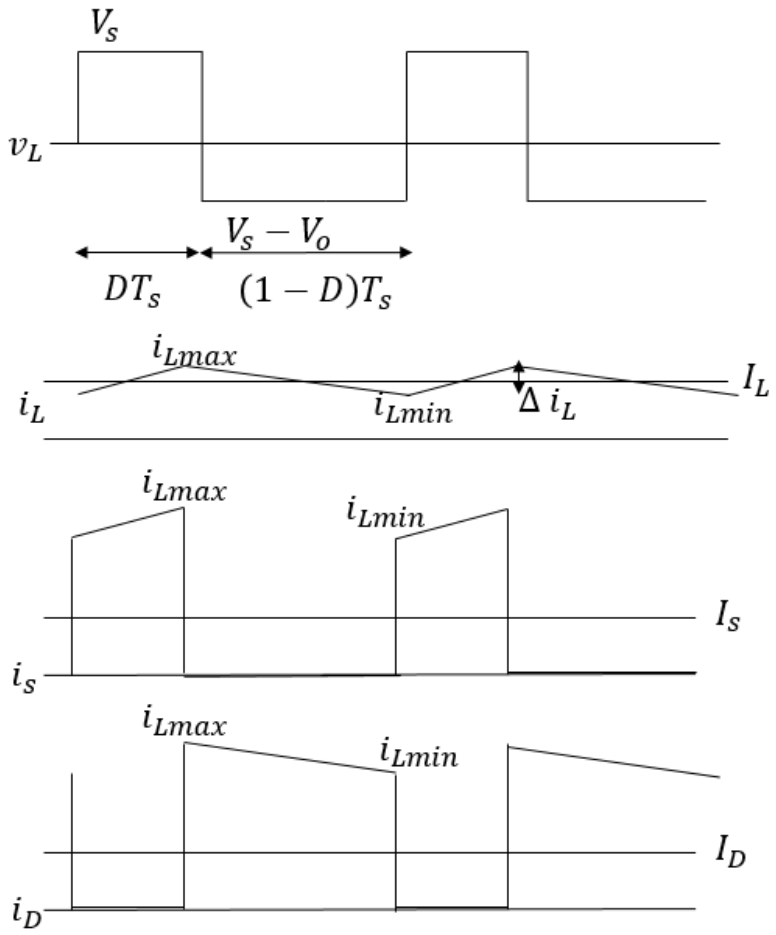


Figure 3.23: (c) Waveform analysis

In the boost converter, the inductor is at the source side and the diode is in series with the load. The average inductor current values are given by the charge balance where the average capacitor current value is zero and hence the load current is equal to the diode current.

$$I_D = I_O = \frac{V_O}{R}$$

By substituting $I_D = (1-D)\, I_L$:

$$I_L = \frac{1}{1-D}\, I_D = \frac{1}{1-D}\frac{V_O}{R}$$

The maximum value of the inductor current is given by:

$$i_{Lmax} = I_L + \frac{1}{2}\Delta\, I_L$$

while the minimum inductor current is:

$$i_{Lmin} = I_L - \frac{1}{2}\Delta\, I_L$$

The output voltage ripple can be estimated form the waveform in Figure 3.24. The diode current is the sum of the capacitor current and the load current as shown in Figure 3.23(a), where the AC components are filtered by the capacitor, while the DC components are delivered to the load resistor

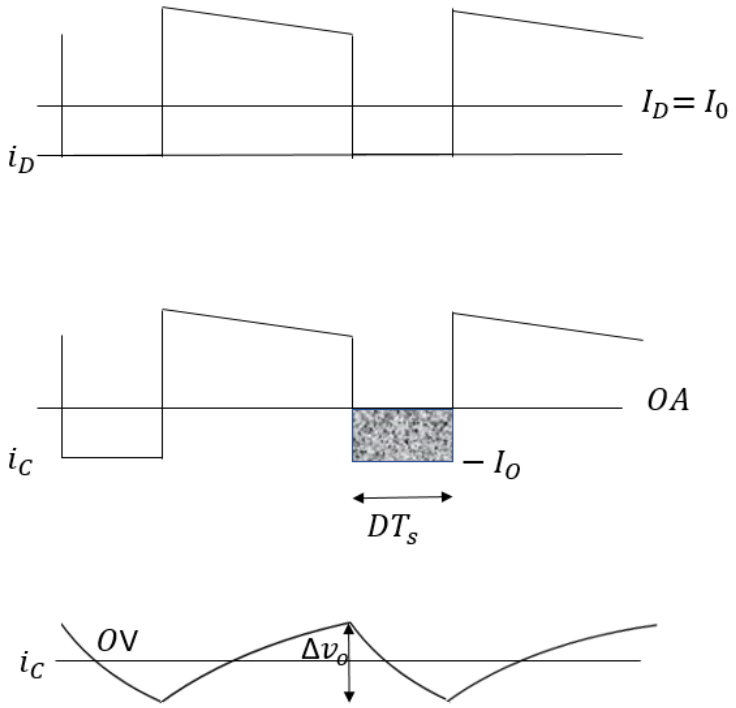


Figure 3.24: Waveform of both current and output voltage ripple

The magnitude of the output voltage ripple Δv_o is the integral of i_C over the negative semi period, which is equivalent to evaluate the negative rectangular area in Figure 3.24 and dividing the value by the capacitance.

$$\Delta v_o = \frac{1}{C}\int i_C(t)\,dt = \frac{1}{C} I_O\, D\, T_S = \frac{1}{C}\frac{V_O}{R} D\, T_S$$

This equation is valid in CCM operation case.

The boost converter switches from CCM to DCM operation when $I_L = \frac{\Delta i_L}{2}$ where

$$\frac{1}{1-D}\frac{V_O}{R} = \frac{1}{2}\frac{V_S}{L} D\, T_S = \frac{1}{2}\Delta i_L$$

As mentioned before, the boost converter gain is $\frac{V_O}{V_S} = \frac{1}{1-D}$ leading to

$$R_{crit} = \frac{2L}{\mathrm{D}(1-\mathrm{D})^2\, T_s}$$

Therefore, the boost converter enters DCM operation, when the load resistance value is larger than R_{crit}. The DCM operation waveform is shown in Figure 3.12, where

$$V_s \, . DT_s = \, (V_o \, - \, V_s) \, \, D_1 \, T_s$$

gives

$$\frac{V_O}{V_S} \, = \frac{D + \, \, D_1}{D_1}$$

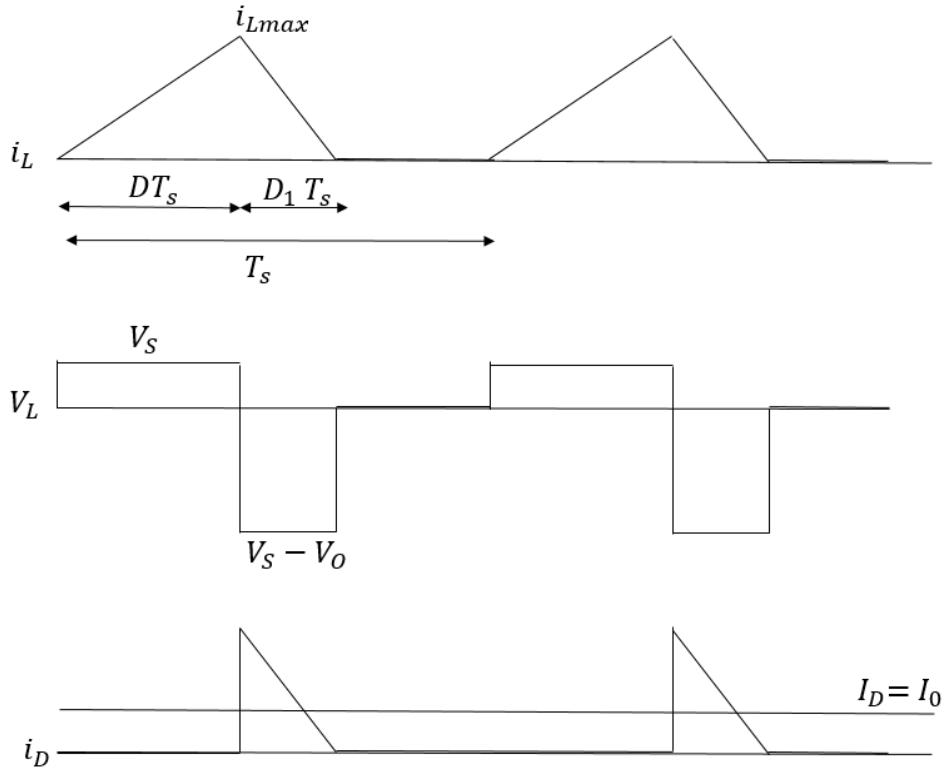


Figure 3.25: Current waveform of the DCM operation in Boost converter

To calculate the unknown variable D_1, the average value of the current through the diode should be equal to the current in the resistor. From the current waveform in Figure 3.25 we obtain:

$$I_D = I_O \, = \frac{i_{Lmax} \, D_1 \, T_s}{2 \, T_s}$$

By substituting

$$i_{Lmax} \, = \frac{V_S}{L} \, DT_s \quad \text{and} \quad I_O \, = \frac{V_O}{\mathrm{R}}$$

we obtain then

$$D_1 \, = \frac{V_O}{V_S} \frac{2\mathrm{L}}{RDT_s}$$

By applying D_1 in the DCM voltage gain equation, it turns out that

$$\frac{V_O}{V_s} = \frac{1}{2}\left(1+\sqrt{1+\frac{2D^2 \mathrm{R} T_s}{L}}\right)$$

It is clear that the voltage gain in the DCM operation has non-linear behavior: the voltage gain is getting larger as the resistance increases. Also, the DCM operation has a larger voltage gain comparing to CCM operation at equal duty ratio.

3.2.3 Flyback converters

The flyback converter is used when galvanic isolation between the input power source (typically from 90 to 260V at 50 to 60Hz) and the output. The isolation can be achieved by inserting an isolation transformer in any of the DC/DC conversion topologies considered above. In particular, the flyback is an evolution of the boost converter in which the inductance is replaced with a transformer. Figure 3.26 shows the main schematic of the flyback converter, where the transformer model consists of an ideal transformer with its magnetizing inductance L_m. The magnetizing inductance value can be controlled by introducing a gap in the magnetic path of the transformer, as for example an air gap in the magnetic core.

The operation of flyback converter can be divided into two phases: during the first phase, energy is accumulated in the magnetizing inductance of the transformer, while in the second phase the accumulated energy is transferred to the load. When the transistor Q is switched ON, the primary winding of the transformer is directly connected to the input voltage source. This means that energy is accumulating in the core of the transformer due to an increase in magnetic flux. The voltage at the secondary side is negative and the diode is inversely biased. Consequently, the output capacitor provides the energy required by the load. When the transistor is switched OFF, the polarity of the magnetization inductance is reversed. At this stage, the diode is directly biased, and the energy accumulated in the transformer is transferred to the load [7] [8].

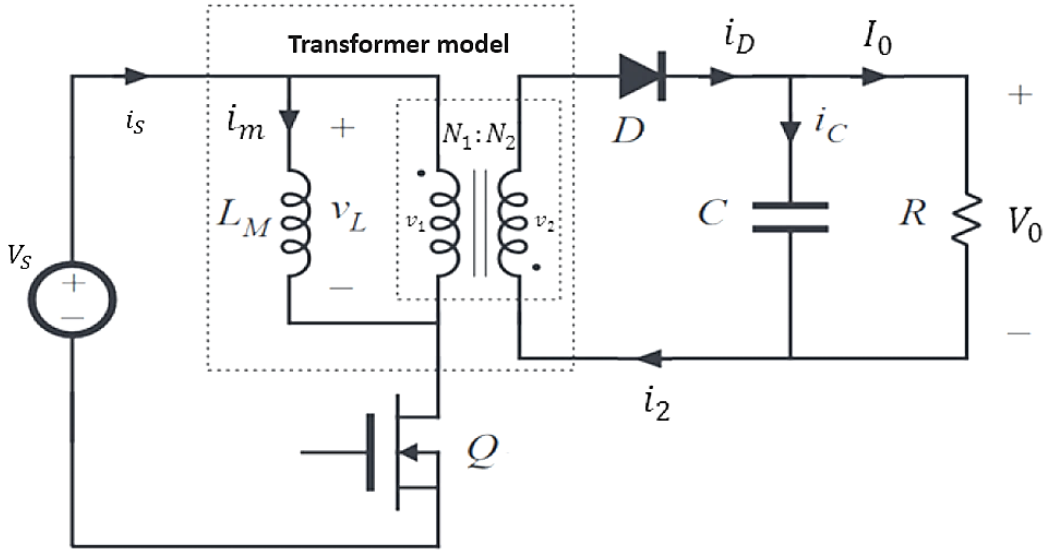


Figure 3.26: Basic schematic of the flyback convertor.

3.2.3.1 In Continuous Conduction Mode (CCM), since there is a transformer, in order to determine the relationship between input and output voltages, we have to consider the magnetic fluxes and the voltage at the primary, representing the only continuous quantities in the circuit. Figure 3.27 shows the waveforms in the flyback converter.

When the transistor is ON, the voltage across the magnetizing inductance V_L is the input voltage V_s. The current flowing through the magnetizing inductance ramps up with slope V_s/L_M. The current i_m is the same current that flows through the switch Q, while both primary and secondary currents are zero. During this period, energy is transferred to the magnetizing inductance from the input source. The energy is stored in the transformer linearly as the current in the magnetizing inductance also increase linearly and when current arrives to its maximum value, the energy stored is at its peak value.

When the transistor is OFF, the magnetizing current flows through the primary winding of the transformer and this pushes a positive current through the diode at the secondary side, turning it on. The current through the diode is given by: $i_D = i_m . (\frac{N_1}{N_2})$. The output voltage V_o is reflected through the $N_1 : N_2$ transformer and applied to the magnetizing inductance with negative polarity. The inductance current decreases linearly with a slope ($-V_o \frac{N_1}{N_2}$) / L_M, the accumulated energy in the transformer is delivered to the output capacitor and load resistance. By applying the balance condition, we obtain:

$$V_s\, DT_s = V_o\, \frac{N_1}{N_2}\, (1-D)T_s$$

leading to:

$$\frac{V_o}{V_s} = \frac{D}{1-\mathrm{D}}\,\frac{N_2}{N_1}$$

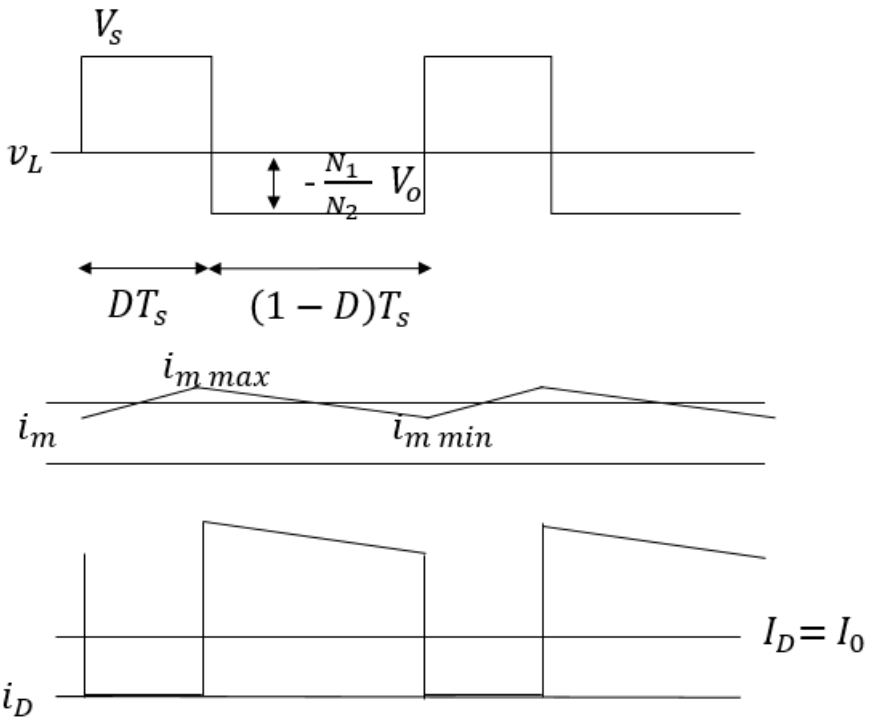


Figure 3.27: Waveform diagram of the flyback converter in CCM

3.2.3.2 In Discontinues Conduction Mode (DCM), when i_m current goes to zero, the flux is zero for a part of the period and also the diode at the secondary side of the transformer is turned off, as shown in figure 3.28. In this condition, the voltage across the switch Q is v_Q = V_s. By applying the voltage balance condition to the magnetizing inductance, we obtain:

$$V_s\, DT_s = V_o\, \frac{N_1}{N_2}\, D_1 T_s$$

leading to:

$$\frac{V_o}{V_s} = \frac{D}{D_1}\,\frac{N_2}{N_1}$$

where D_1 can be obtained from the calculating the average value of the diode current and the load current, according to:

$$D_1 = \frac{V_o}{V_s} \cdot \frac{2\,L_m}{RD\,T_s} \cdot \frac{N_2}{N_1}$$

By substituting D_1 in the voltage gain equation we obtain:

$$\frac{V_o}{V_s} = D\sqrt{\frac{RT_s}{2L_m}}$$

This equation shows that the gain is independent of the number of turns of the transformer.

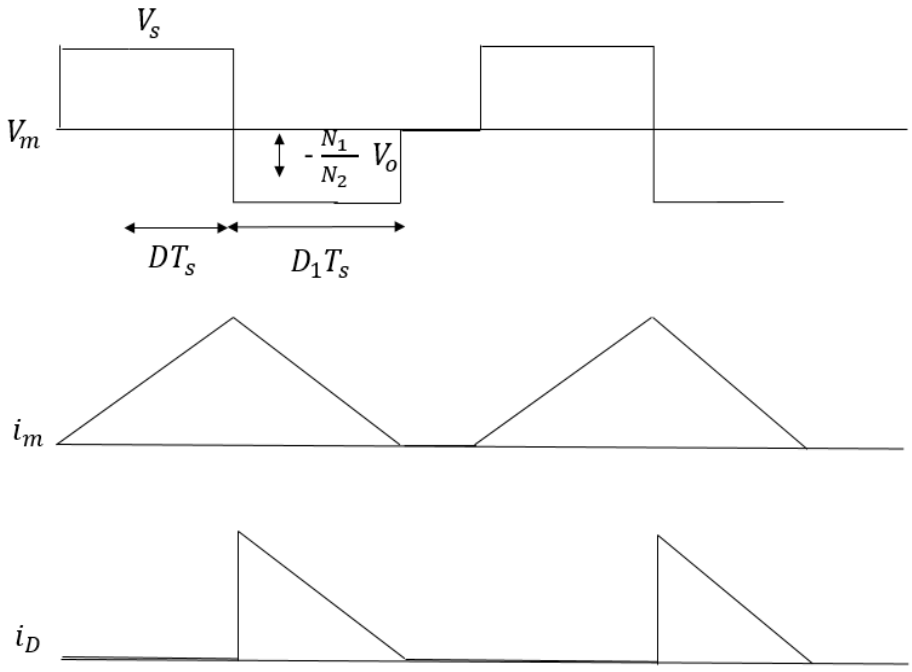


Figure 3.28: Waveform diagram of the flyback converter in DCM

3.3 Description of the realized system

In this section, the complete explanation of the circuit realized for the ultrasonic washing machine is reported. The system consists of various stages, where each stage has a different role to drive the machine and control the entire system. The first stage, is a boost converter which has mainly the role of regulating the power factor (PFC) and stabilizing the output voltage obtained from the rectifier. The second stage is a buck converter supplied with the output voltage of the boost stage. In the last stage, the half- bridge inverter receives the

regulated voltage by the buck converter and supplies a square-wave signal to the piezoelectric transduces of the ultrasonic washing machine. Another supplementary flyback converter is used to supply the drivers that control the MOSFET switches of the other stages. Altium and Multisim software have been used to implement the schematic and the also the layout PCB.

3.3.1 General scheme

3.3.1.1 Boost stage

The boost converter has been designed to stabilize the DC supply voltage of the system and to adjust the power factor (PFC) [9] [10]. The circuit is based on Infineon products as shown in figure 3.29. The PFC can be work at a minimum required input voltage $V_{in(\min)}$ = 90V RMS and maximum input voltage $V_{in(\max)}$ = 265V RMS with input frequency of 50/60 Hz, while the output voltage is V_{out}= 400V with a nominal power of 200W and estimated efficiency of η = 0.9 at full load. The switching frequency is 65kHz.

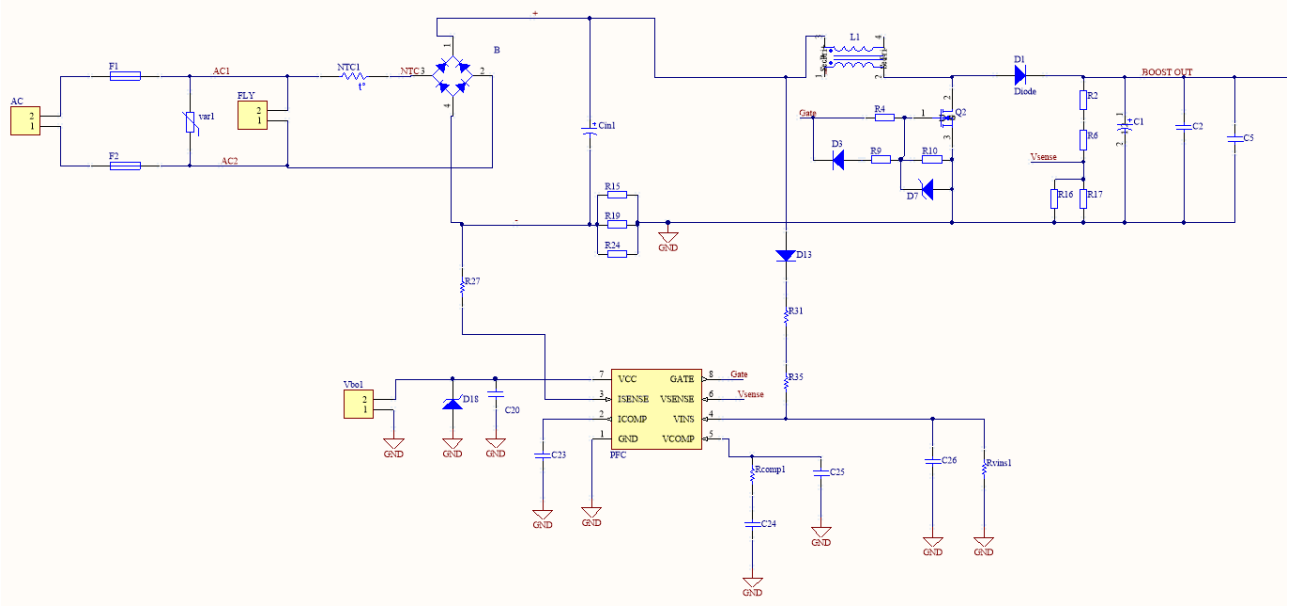


Figure 3.29: Circuit diagram designed in Altium of the boost stage

In order to obtain 200W output power at 90V minimum AC input voltage, the maximum input RMS current is

$$I_{in\_RMS} = \frac{P_{out}}{V_{in\_RMS}} = \frac{200}{90\ (0.9)} = 2.47\text{A}$$

And at the peak of the sinusoidal current is:

$$I_{in\_pk} = \sqrt{2}\,.\,\frac{P_{out}}{V_{in\_RMS}} = 3.5\text{A}$$

For these values, using a bridge rectifier with an average current capability of 6A is necessary and, due to power dissipation, a heat sink has to be connected to the bridge rectifier. A gate drive resistance is used to drive the power MOSFET as fast as possible. Another resistor is connected between the gate and the source of the power MOSFET to discharge the gate capacitance. The boost diode has an enormous influence on the performance, because of the reverse recovery behavior. Therefore, an ultra-fast diode is used to reduce the switching losses. The inductance L_1 is determined based on the maximum current value at the lowest input voltage multiplied by a coefficient k = 0.22 and also on the high frequency ripple peak to peak current I_{HF_pk}

$$I_{HF\_pk} = \text{k.}\ \sqrt{2}\ .\ \frac{P_{in\_max}}{V_{in\_min}} = 692\text{mA}$$

The peak current that flows through the inductor is then:

$$I_{L\_pk} = I_{in\_pk} + \frac{I_{HF\_pk}}{2} = 3.5 + 0.346 = 3.846\text{A}$$

The peak current has a maximum value when the duty cycle D = 0.5, so the minimum value for the inductance is:

$$L_1 > \frac{D(1-D)\,V_{out}}{I_{HF\_pk}\,.\,f_s} = 2.22\text{mH}$$

The output capacitors were chosen based on the output voltage ripple. The output voltage ripple must be less than 10% of the DC voltage V_{out} and hence

$$C_{out} > \frac{I_{out}}{2\,\pi\,f_s\,.\,V_{o(ripple)}} = 160\mu\text{F}$$

where I_{out} is the PFC output current, $V_{o(ripple)}$ is the output voltage ripple (peak to peak) and f_s is the switching frequency.

Another important design parameter is the holdup time, i. e. the stage needs to provide an isolated output even when the AC input voltage becomes zero for a short time (holdup time). This time is around 20ms. If the minimum output voltage is 360V, then the required capacitance value becomes:

$$C_{out} > \frac{2.\,P_{out}\,.\,t_{holdup}}{V^2{}_{out} - V_{out\_min)}} = 263\mu\text{F}$$

The final C_{out} capacitance has been implemented with an electrolytic capacitor and two ceramics capacitors connected in parallel C_1 =270 µF C_2 =C_3 = 1µF.

The input current is sensed using the resistance R_{sense} (R_{15}, R_{19}, R_{24}), which is calculated according to the threshold given in the PFC datasheet [10], which is 0.68V maximum. So R_{sense} is:

$$R_{sense} < \frac{0.68}{I_{L\_pk}} = 0.194\Omega$$

To reach this value, three parallel resistors R_{15}, R_{19}, R_{24} , all with same value of 0.33Ω are used, leading to $R_{\text{sense}} = 110m\Omega$.

Another issue is related to startup. When the AC input signals is powered up, a negative voltage-drop at R_{sense} will appear if 150A to 200A flow through the resistor. To limit this current, the value of R_{27} is chosen equal to 220Ω, limiting the current to 1mA.

A resistor divider is used to have the required feedback voltage:

$$R_a = \frac{V_{out} - V_{ref}}{V_{ref}} . R_b \Rightarrow R_{2+6} = \frac{V_{out} - V_{ref}}{V_{ref}} . R_{16\|17}$$

where V_{ref} = 3V.

leading to $R_2 = 330k\Omega, R_6 = 390k\Omega, R_{16} = 10k\Omega, R_{17} = 15k\Omega$.

The power supply for the control IC of the boost convertor is 15V and is provided by the flyback converter. A compensating capacitor is used for the current error in the closed loop feedback with value 10nF. Also, other capacitors and resistors are used to compensate the voltage error in closed loop, the values are C_{24} = 1μF, C_{25} = 100nF and R_{comps} = 33kΩ.

When the input voltage is below the minimum value, the PFC chip stops working properly. Therefore, a protection is needed to prevent the boost converter to draw a high current which would lead to overheat in the MOSFET and the diode. A sensing pin (VINS) of the input voltage is present in the IC, as shown in Figure 3.30. An external network, connected to the input voltage, turns the IC ON when the VINS voltage is more than 1.5V, while it turns off it is less than 0.7V.

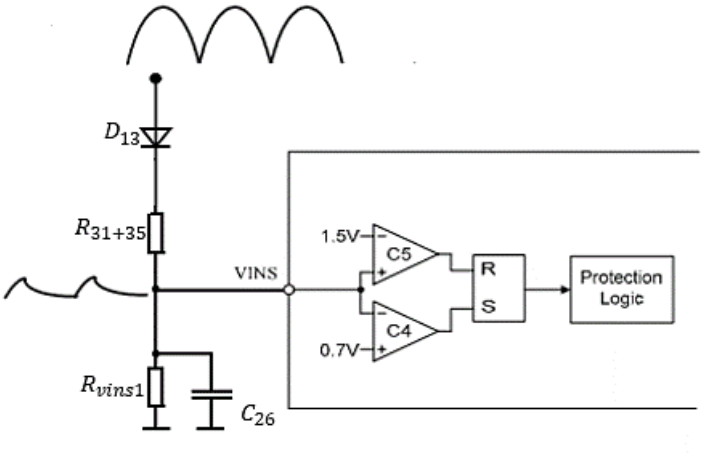


Figure 3.30: Block diagram of the network used for under voltage protection

From the block diagram in Figure 3.30, the resistor R_{31+35} has a large value to guarantee high input impedance and, due to voltage stress, it is divided in two parts R_{31} and R_{35} :

$$R_{31+35} = \frac{\sqrt{2} . V_{AC\_on} - 1.5}{1.5} . R_{\text{vins1}} = 7.8\text{MΩ}$$

where $V_{\mathrm{AC\_on}} = 70\mathrm{V}$ and $R_{\mathrm{vins1}} = 120\mathrm{k}\Omega$ to guarantee a current of more than 5µA which is much larger than the bias current on the VINS pin. A capacitor $C_{26} = 150\,nF$ is used to modulate the ripple at the VINS pin.

Pin GATE role is to provide a signal to open and close the MOSFET Q_2. The network of resistors R_9, R_4 and diode D_3 are used to define the MOSFET power-on and off times. Another protection circuit is the Zener diode D_7 and resistance R_{10} which represent a protection against over voltage between gate and source.

The measurement performed on the boost converter with PFC control on and off are shown in figures 3.31 and 3.32, where the output voltage is in blue and the input current in green.

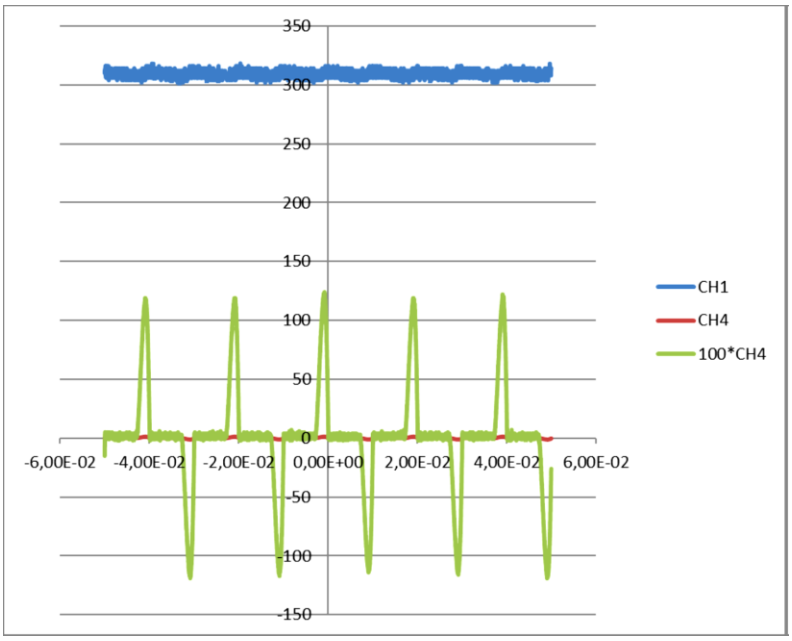


Figure 3.31: Measurement of the input current and the output voltage when PFC is OFF

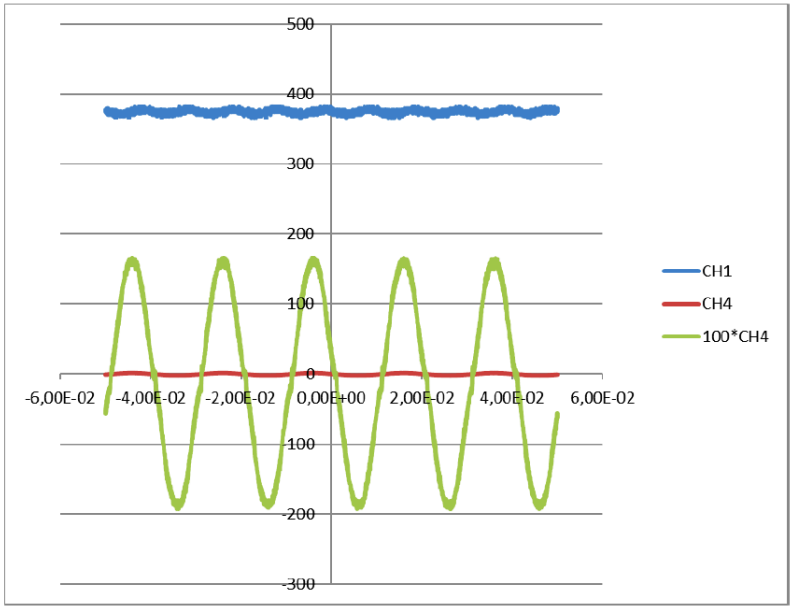


Figure 3.32: Measurement of the input current and the output voltage when PFC is ON

3.3.1.2 Buck stage

The buck converter receives a constant stable voltage from the boost converter. The amplitude of the output voltage of the buck is adjusted according to the load. The components in the buck converter are chosen according to the specification requested, as shown in figure 3.33. A high voltage driver is used to drive a high-speed power MOSFET switch with independent high-side output floating channels designed for the bootstrap operation. The buck converter features a 400V input voltage and from 100V to 300V regulated output voltage with nominal power of 200W. At the input side of the buck converter, an input filter capacitor C_{15} of 1µF is used to fit the current ripple that can be tolerated on the DC input line, also considering the capacitor already present at the output of the boost stage [11] [12].

The inductance is determined according to the output power, operating frequency, and efficiency. Low inductance values would cause a large ripple current, low efficiency, and high output noise. The value is calculated starting from the desired maximum ripple current in the inductor (Δi) which has to be between 20% to 50% of the output current. The inductor value is, therefore:

$$L_2 = (V_{\text{in}} - V_{\text{o}}).\frac{V_{\text{o}}}{V_{\text{in}}.\Delta i.f_s} = 4.7\text{mH}$$

where the ripple current is 30% of the output current (Δi = 0.2A), the switching frequency is 100kHz, and V_{o} is the average between maximum and minimum values of the output voltage.

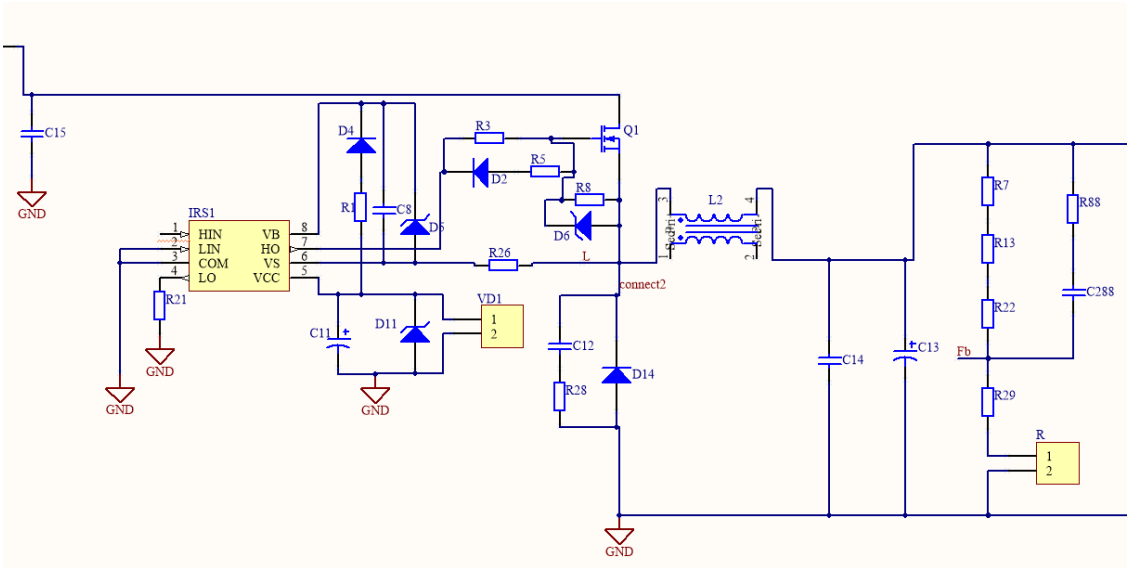


Figure 3.33: Circuit diagram of the buck stage

The output capacitor is selected according to the values of the voltage ripple at the output of the buck converter and the ripple current flowing through the inductance:

$$C = C_{13} + C_{14} = \frac{\Delta i_{\text{L}}}{8.\Delta v_{\text{o}}.f_s} = 22.27\mu\text{F}$$

$$C_{13} = 1\mu\text{F}, \qquad C_{14} = 22\mu\text{F}$$

The output capacitor indeed influences the overall performance of the converter and determines the transient behavior. Ceramic capacitor is an appropriate choice because of its low ESR.

The MOSFET Q_1 must have a maximum operating voltage (V_{DSS}) greater than the maximum input voltage to meet the power transfer requirements. Therefore, a MOSFET with $V_{\mathrm{DSS}} = 650V$ is chosen.

The output voltage is adjusted by a resistive voltage divider in which R is a variable resistance whose value determines the output voltage of the buck converter.

A high voltage PWM synchronous controller is used to control the high side driver which in turn drives the MOSFET switch. The output voltage is adjusted by a feedback pin (Fb) and the internal reference voltage (1.25V). These two signals are send to an error amplifier inside the controller IC where the error signal is compared to a fixed frequency linear saw-tooth ramp generating a pulse at fixed frequency with variable duty-cycle (D), as shown in Figure 3.34.

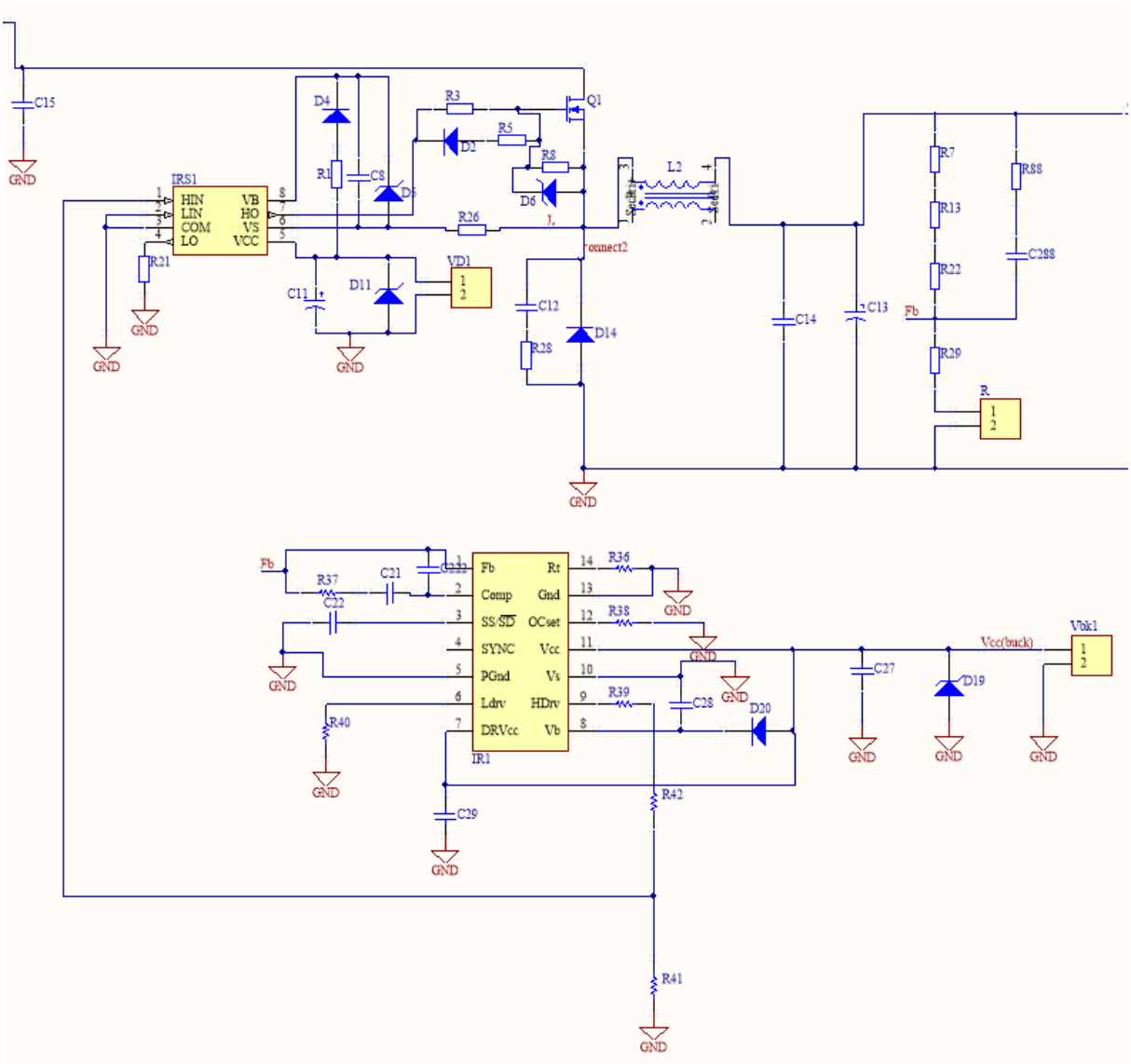


Figure 3.34: Control scheme of the buck converter

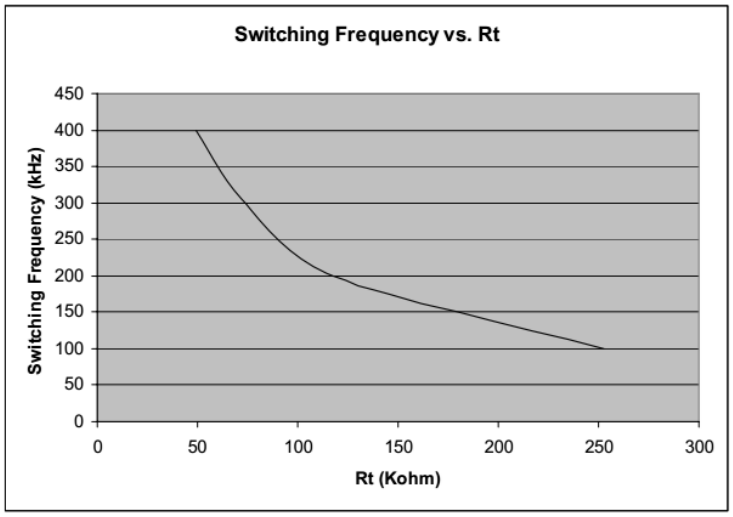


Figure 3.35: Switching frequency vs Rt.

The timing of the IC is controlled by an internal oscillator circuit that can be programmed externally up to 400kHz. The switching frequency is determined by an external resistance R_{36} connected between the Rt pin and ground. Figure 3.35 shows the oscillating frequencies versus Rt. R_{36} = 220kΩ is selected to achieve a switching frequency of around 120kHz [11].

Pin Vcc is the power supply of the chip, working at 15V, supplied by flyback converter.

Pin HDrv is connected to a resistor divider in order to limit the maximum input voltage to the driver for the MOSFET:

$$R_{39} = R_{41} = R_{42} = 10\text{k}\Omega$$

Pin SS/Sd function is to regulate the soft start, to control the output voltage rise and limit the inrush current during the start-up. The start-up time depends on the size of the external soft-start capacitor. The start-up time chosen is $T_{\text{start}} = 50\text{ms}$, which is corresponds to $C_{22} = 1\mu\text{F}$.

Pins (OCset, Ldv, Vb, DRVcc) have unneeded functions in this case, so they have been connected to ground with some resistors and capacitors for protection.

A compensation network is needed for the PID controller which has been mentioned in the previous section.

The data sheet of the PWM controller offers the equations needed to calculate the values of the components used for compensation. The goal of the compensation network is to provide a closed loop transfer function with the highest crossing frequency and adequate phase margin greater than 45°:

$$f_{z2} = 10.10^3 \sqrt{\frac{1-\sin(\frac{\pi}{3})}{1+\sin(\frac{\pi}{3})}} = 2.68\text{kHz} \qquad f_{p2} = 10.10^3 \sqrt{\frac{1+\sin(\frac{\pi}{3})}{1-\sin(\frac{\pi}{3})}} = 37.32\text{kHz}$$

$$f_{z1} = 0.5.\ f_{z2} = 1.34\text{kHz}$$

$$R_{37} > \frac{2}{1.5.10^{-3}} = 1.33\text{kΩ},$$ 10kΩ has been chosen

$$C_{21} = \frac{1}{2\,\pi\,.f_{z1}.R_{37}} = 11.88\text{nF},$$ 10nF has been chosen

$$C_{22} = \frac{1}{2\,\pi\,.f_{p3}.R_{37}} = 0.24\text{nF},$$ 0.33nF has been chosen

$$C_{288} = \frac{2\,\pi\,.L_2.C_0.1.25}{V_{in}.R_{37}} = 2.12\text{nF},$$ 1.8nF has been chosen

$$R_{88} = \frac{1}{2\,\pi\,.f_{p2}.C_{288}} = 2.37\text{kΩ}$$ 2.7kΩ has been chosen

$$R_7+R_{13}+R_{22}= \frac{1}{2\,\pi\,.f_{z2}.C_{288}} - R_{88}= 30.62\text{kΩ}$$ 3x8.2kΩ has been chosen

$$R_{88}+R_{29}= \frac{1.25}{V_{out}-1.25}(R_{7,13,22})= 103\Omega$$ 100 Ω has been chosen

The driver which controls the buck converter switch is powered with 15V provided by the flyback converter [13]. This driver can deliver up to 600V, working with a bootstrap technique. The gate drive voltage ranges from 10V to 20V. The bootstrap network has R_1= 10Ω, C_8= 0.22µF and R_{26}= 10Ω. Figure 3.36 and figure 3.37 show the measurements of the voltage at the diode D_{14} (in blue) and the buck output current (in green).

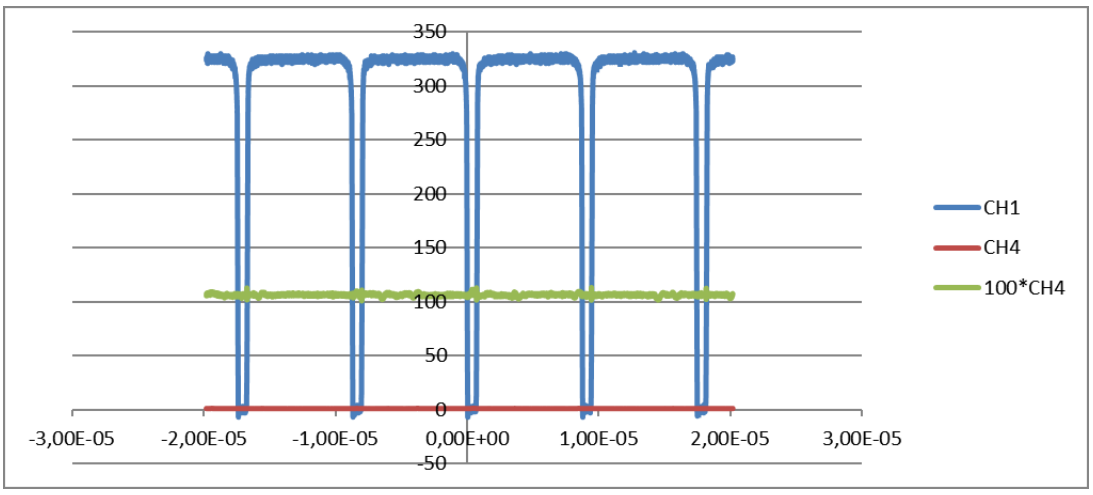


Figure 3.36: Measured voltage at D_{14} and output current of the buck converter up to 1A

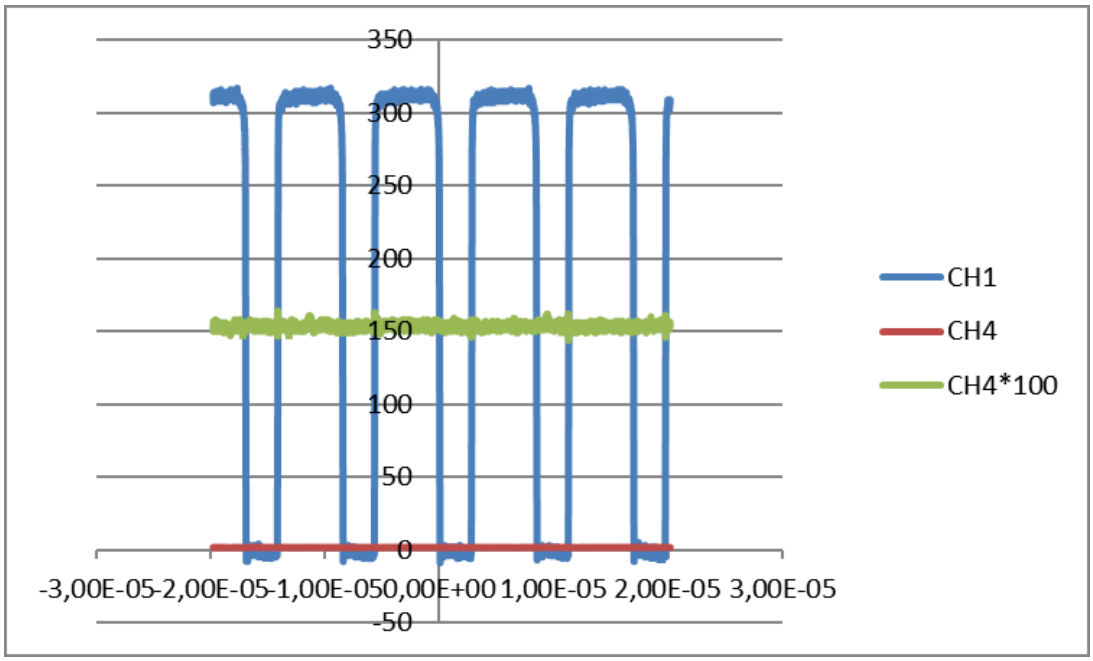


Figure 3.37: Measured voltage at D_{14} and output current of the buck converter up to 1.5A.

3.3.1.3 Inverter (Half Bridge)

The half-bridge inverter receives the buck-controlled continuous voltage as input and provides a square-wave voltage to piezoelectric transducers. Figure 3.38 shows the schematic of the inverter [14].

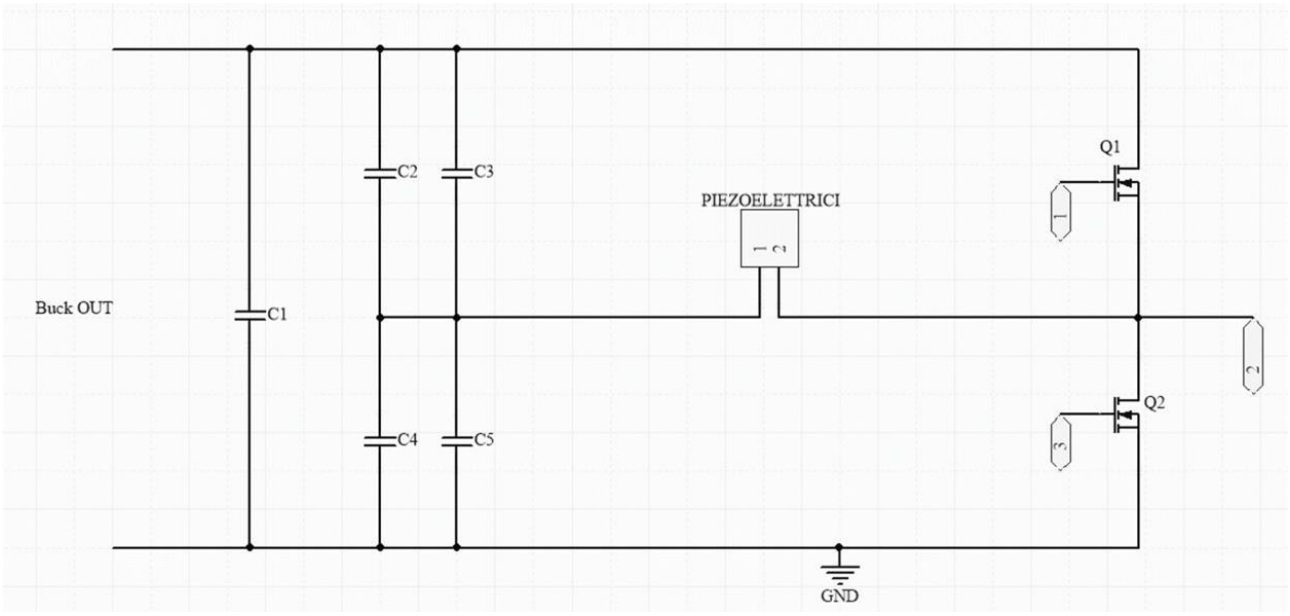


Figure3.38: Inverter half bridge

The input capacitor used to limit the ripple voltage at the output from the buck converter has value of 1μF. The inverter capacitor has been resized to limit the voltage drop ΔV to less than 10% during the switching period. It is calculated using this following equation:

$$C > \frac{I}{f_s \frac{V_{buck}}{2}.0.1} = 1.43\mu F.$$

f_s is chosen to be 40kHz so the piezoelectric transducer can absorb around 1.15A. Figure 3.39 shows the final schematic used including the driver of the MOSFET switch. The capacitors ($C_6, C_7, C_{17}, C_{18},$) used have a value of 1μF. To control the driver, a PWM signal is needed. An Arduino microcontroller is used to supply the PWM signal with switching frequency sweep ranging from 30kHz to 40kHz. By using a current Hall sensor, it is possible to detect the best frequency to be used for resonance and fix it during the machine operation period.

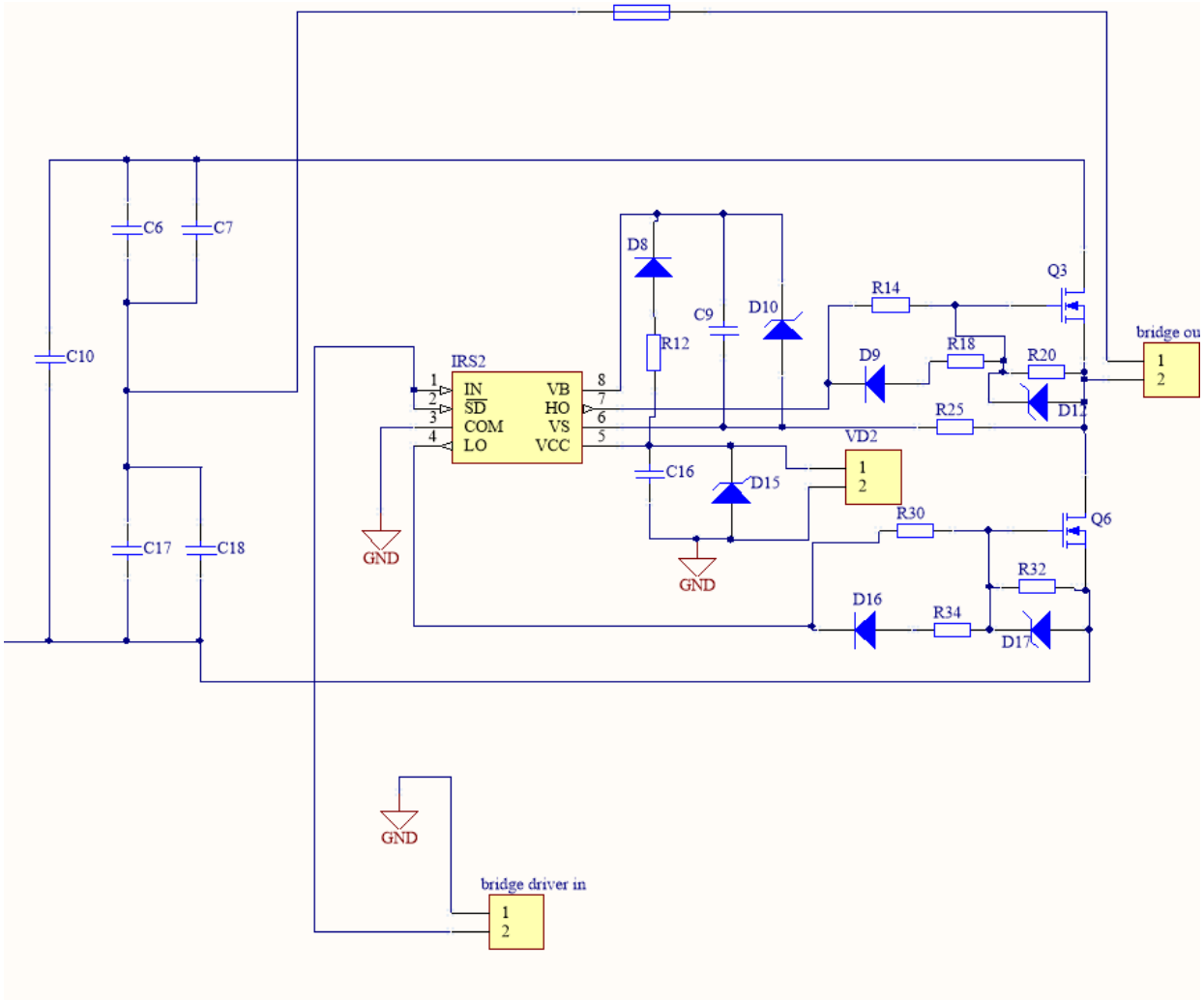


Figure 3.39: Final schematic with driver controlling the MOSFET switches.

3.4 Arduino microcontroller

The Arduino microcontroller board used is called Genuino Zero, shown in figure 3.40. It is a simple and powerful 32-bit microcontroller for different applications. Arduino applications span from smart IoT devices, wearable technology, high-tech automation, to robotics. The board is powered by Atmel SAMD21 MCU, which features a 32-bit ARM Cortex® M0+ core. One of its most key features is Atmel Embedded Debugger (EDBG), which provides a full debug interface without the need for additional hardware, significantly increasing the ease-of-use for software debugging. EDBG also supports a virtual COM port that can be used for device and bootloader programming.

The board contains everything needed to support the microcontroller; simply connect it to a computer with a micro-USB cable or power it with a AC-to-DC adapter or battery to get started. The board is compatible with all the shields that work at 3.3V.

Figure 3.40: Genuino zero Arduino microcontroller board.

The board major features are 20 digital input/output pins, 6 analog input pins (12-bit ADC channels), one analog output pin (10-bit DAC), current capability up to 7mA for each pin,

flash memory of 256KB, SRAM of 32KB and clock speed of 48MHz. The board can operate with an external supply of 6 to 20 volts. The power pins are as follows:

- VIN: The input voltage to the board when it is using an external power source (as opposed to 5V from the USB connection or other regulated power source). Supply voltage connected through this pin, or if supplying voltage via the power jack, access it through this pin.
- 5V: This pin outputs a regulated 5V from the regulator on the board. The board can be supplied with power either from the DC power jack (7 - 12V), the USB connector (5V), or the VIN pin of the board (7-12V). Supplying voltage via the 5V or 3.3V pins bypasses the regulator.
- 3.3V: A 3.3-volt supply generated by the built-in regulator. Maximum current draw is 800 mA.
- GND: Ground pins.
- IOREF. This pin on the board provides the voltage reference with which the microcontroller operates. A properly configured shield can read the IOREF pin voltage and select the appropriate power source or enable voltage translators on the outputs for working with the 5V or 3.3V.

Each of the 20 general purpose I/O pins on the board can be used for digital input or digital output using *pinMode(), digitalWrite()*, and *digitalRead()* functions. Pins that can be used for PWM output are: 3, 4, 5, 6, 8, 9, 10, 11, 12, 13 using 8-bit PWM output with the *analogWrite()* function. All pins operate at 3.3V. Each pin can source or sink a maximum of 7 mA and has an internal pull-up resistor (disconnected by default) of 20-50 kΩ.

The analog inputs are 6 of the 20-general purpose I/O pins on the board. These are labeled A0 through A5, and each provides up to 12bits of resolution (i.e. 4096 different values). By default, they measure from ground to 3.3 volts, though is it possible to change the upper end of the range using the AREF pin and the *analogReference()* function.

3.4.1 Code

the Arduino language is a set of C/C++ functions that can be called from the code. The code undergoes minor changes then is passed directly to a C/C++ compiler.

The code written for this application is used to send square-wave signals to the inverter with a sweep frequency range from 30kHz to 40kHz and to receive the measured current from the Hall current sensor. During the measurements of the current, Arduino measures in parallel the frequency of the square-wave and the current value, looking for the frequency value that features the maximum current level, i.e. the resonance frequency of the transducer. The current is measured by the Hall-effect current sensor. The current flows through a copper conduction path (electrically isolated from the sensor leads) that generates a magnetic field which is sensed by the Hall IC and converted to a proportional voltage. The voltage is amplified by a low-offset, chopper-stabilized operational amplifier and read by Arduino analog input A0. Arduino compares the variation in current value as a function of the frequency applied to the driver. Another role of the Arduino microcontroller is to power up and adjust the digital potentiometer from 0 to 1kΩ (“R” in figure 3.20). The value of R determines the output voltage of the buck converter.

```
// contol potentiometer resistor.

#define Cs 7
#define UD 2
#define INC 4

// current sensor measurments.
int mVperAmp = 610; // resolution of current sensor with 3.3 amplification
unsigned int RawValue = 0;
int ACSoffset = 2512; //offset of current sensor(theortical = 2500)
double Voltage = 0;
double Amps = 0;
```

```
// sweep from 30KHz to 40KHz
int Pin = 8;
double freqmax = 40000;
double freqmin = 30000;
int i = 0;
double frequency;
int number = 41 ;
const double step = (freqmax - freqmin) / (number - 1);
int analogPin = A5;
double freqused;
//maxiumim current from 100 samples
int size=100;
unsigned long time[100];
int rawdata;
int maxAmps = 0;
//measure freq. at maximum current.
int  frqpin = 8; // digital pin 8
int oneSecond = 100;
uint32_t timer = 0;
uint32_t sts = 0;
const uint32_t c = 100; // wait for pulses count
uint32_t ets = 0;
// final sweep frequency
double freqma;
double freqmi;
double freqfinal;
// time interval for final frequency
unsigned long starttime;
unsigned long endtime;
double loopcount;

void setup() {
pinMode(Pin, OUTPUT);
Serial.begin(9600);
pinMode (Cs, OUTPUT);
pinMode (UD, OUTPUT);
pinMode (INC, OUTPUT);

for ( int i= 0; i <100; i++)
 {
  Dec();
 }
for ( int i= 0; i <36; i++)
 {
  Inc();
 }

  maxAmps = analogRead(A5);
}
void sav ()
```

```
{
  digitalWrite (INC,HIGH);
  digitalWrite (Cs,HIGH);
delay(20);
  digitalWrite (INC,LOW);
}

void Inc ()
{
  digitalWrite (Cs,LOW);
  digitalWrite (INC,HIGH);
  digitalWrite (UD,HIGH);
delay(20);
  digitalWrite (INC,LOW);
  delay(20);
}

void Dec ()
{
  digitalWrite (Cs,LOW);
  digitalWrite (INC,HIGH);
  digitalWrite (UD,LOW);
delay(20);
  digitalWrite (INC,LOW);
  delay(20);
}
void loop() {
  sav();
  frequency = freqmin;
  for (i = 1; i <= number; i++) {
    tone(Pin, frequency);
   delay(500);
     frequency = frequency + step ;
    rawdata = analogRead(A5);

  for (int x = 0; x < 100; x++)
    {
    RawValue = RawValue + analogRead(A5);
    }

    Voltage = ((RawValue / 100) / 1023.0) * 3300; // calculation for voltage
    Amps = ((Voltage - ACSoffset) / mVperAmp); // calculation for current

//calculation for maximum current
if ( (RawValue /100) > maxAmps) maxAmps = (RawValue /100);

{
 pulseIn(Pin,LOW);
 sts = micros(); // start time stamp
  for (int i=c; i>0; i--)
   pulseIn(Pin,HIGH);
 ets = micros(); // end time stamp
 if ( (RawValue / 100) >= maxAmps) freqused =((c*2*1e6/(ets-sts)));
}
```

```
    Serial.print("\t maxAmps = "); // shows the voltage measured
    Serial.print(Amps,3);
    Serial.print(" , ");
    Serial.print(frequency);
    Serial.print(" , ");
    Serial.print(freqused);
    Serial.print(" , ");
    Serial.println(RawValue /100);
    RawValue = 0; // reset value
    delay(10);
  }
  starttime = millis();
endtime = starttime;

 delay (5000);

  for ( int i= 0; i <32; i++)
 {
  Dec();
 }

 sav();

while ((endtime - starttime) <=1500000) // time for main frequency
{

freqma = freqused + 400;
freqmi = freqused ;

const double step = (freqma - freqmi) / (6 - 1);
    freqfinal = freqmi;

  for (i = 1; i <= 5; i++) {
     tone(Pin, freqfinal);
    delay(2500);
     freqfinal = freqfinal + step ;
  }


  for (i = 5; i > 1; i--) {
    tone(Pin, freqfinal);
    delay(2500);
     freqfinal = freqfinal - step ;
  }
     loopcount = loopcount+1;
endtime = millis();
maxAmps = 0;// reset value
}
}
```

3.5 Circuit implementation

A printed circuit board PCB has been realized, including all the electronic components of the designed circuit diagram [15]. Altium software has been used to design the PCB on a double-sided board, following all the software rules to ensure safety and operation of the circuit. These rules are in accordance with electrical, physical and fabrication regulations. The board size is chosen in such manner that can be easily fixed in the ultrasound washing machine. Sufficient physical and electrical clearance should be provided for all mechanical hardware that requires electrical isolation. Particular attention is devoted to the physical design of the board, specifically the size, shape, type of components, components thickness, to mount the board in the tank easily and to reduce the effects of vibrations. The electrical considerations deal with power distribution, grounding scheme, lead length, and component polarity. Power traces are designed wide enough, while ground is realized in big planes. Spacing between lead traces on each layer is maximized enough to avoid any interference.

Components has a significant role in the design of the board. They can affect fabrication, routing, soldering and testing of the circuit. All components are selected to have the electrical performance and electrical clearance requirements of the circuit design. Heat sink is used also to minimize heat generation and heat dissipation problems. Through-hole parts and components are used in the board whenever possible.

In the ultrasonic washing machine, two separated PCBs are used. The first one (PCB1) includes the main power converters including the boost and buck converters and the inverter that supplies the transducer. The second one (PCB2) contains the auxiliary flyback converter. Terminals are provided for connecting the two PCBs together. The transformer and the matching inductance between power supply and piezoelectric devices are not included in these two PCBs, also the Arduino board is connected externally. The two PCBs are double-sided with the components mounted on the top layer with through holes. The top layer of PCB1 has the ground plan and the integrator feedback links. All the traces line and power lines are on the bottom layer. PCB2 has two separate ground planes on the top layer and the other lines for components connections are on the bottom layer.

Figure 3.41 shows the PCB1 in 3D view, while figure 3.42 shows the two layers, where top layer is in red color, while bottom layer in blue color. Figure 3.43, shows the top layer plane, while figure 3.44 shows the bottom layer plane.

PCB1 specifications:

- Dimensions: width 100mm, height 160mm.
- Number of components: 120
- Number of electrical connections: 89

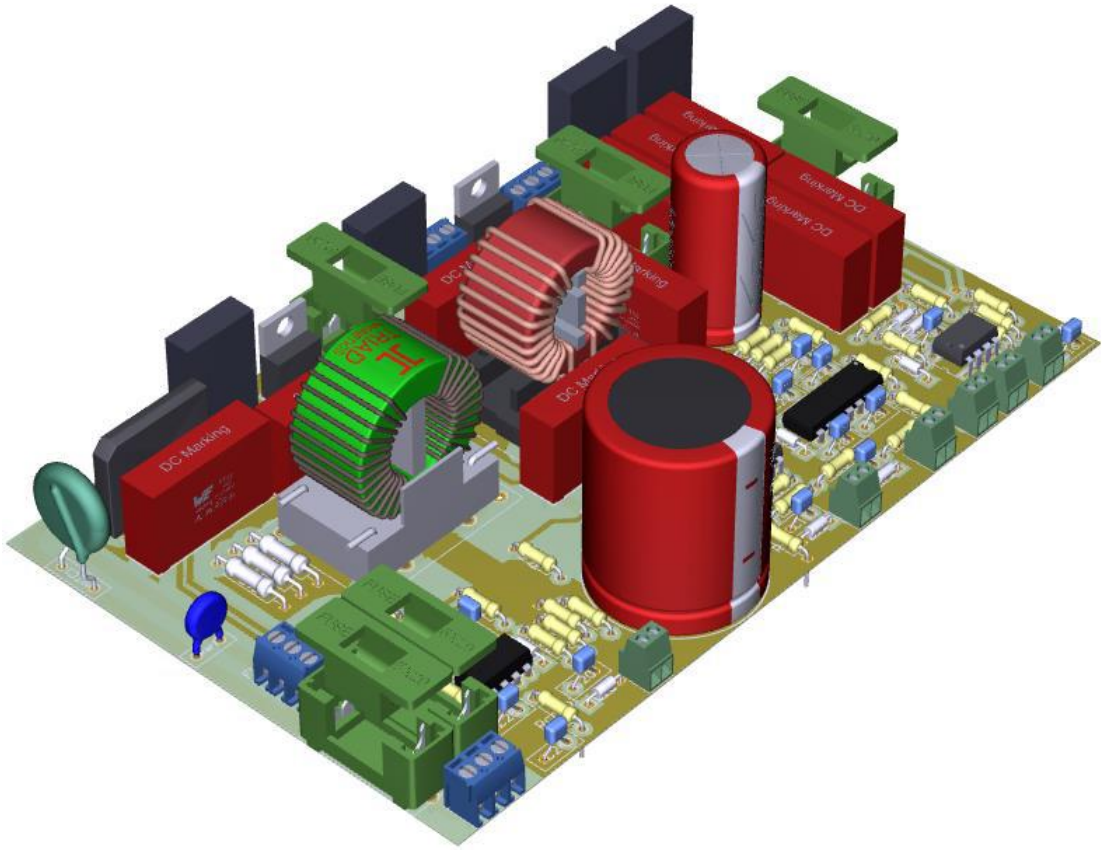


Figure 3.41: 3D view of PCB1 with components fixed

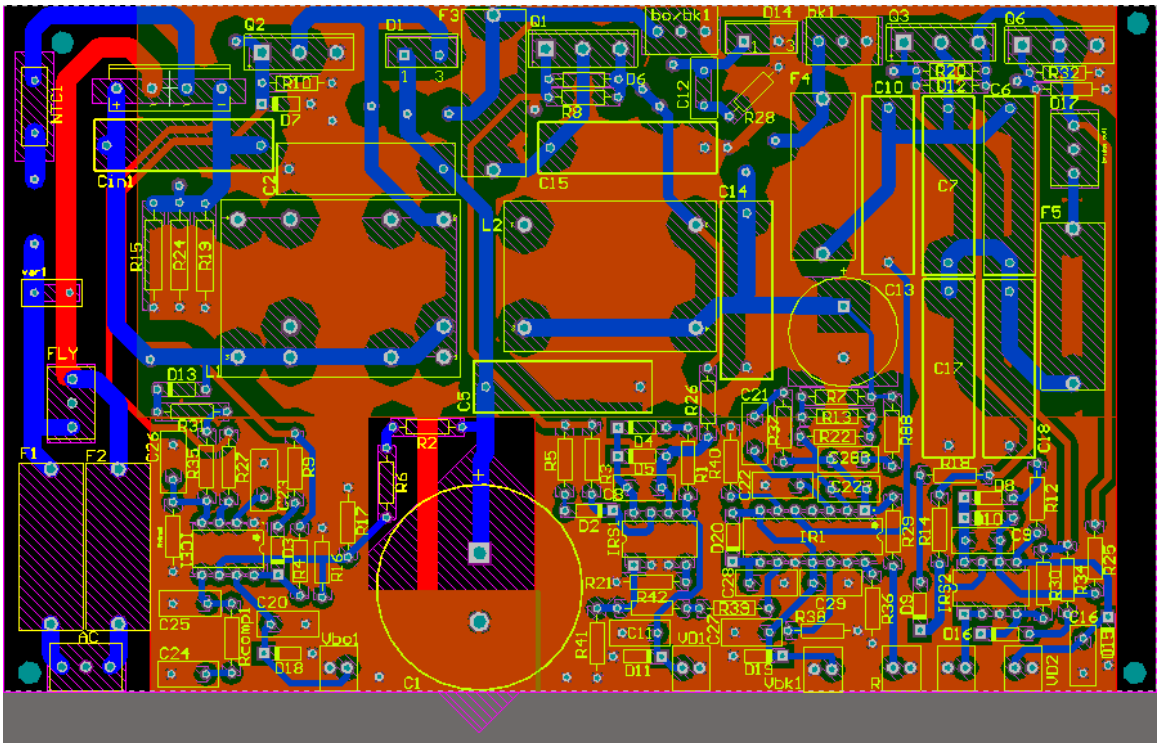


Figure 3.42: PBC1 layout with all components connections

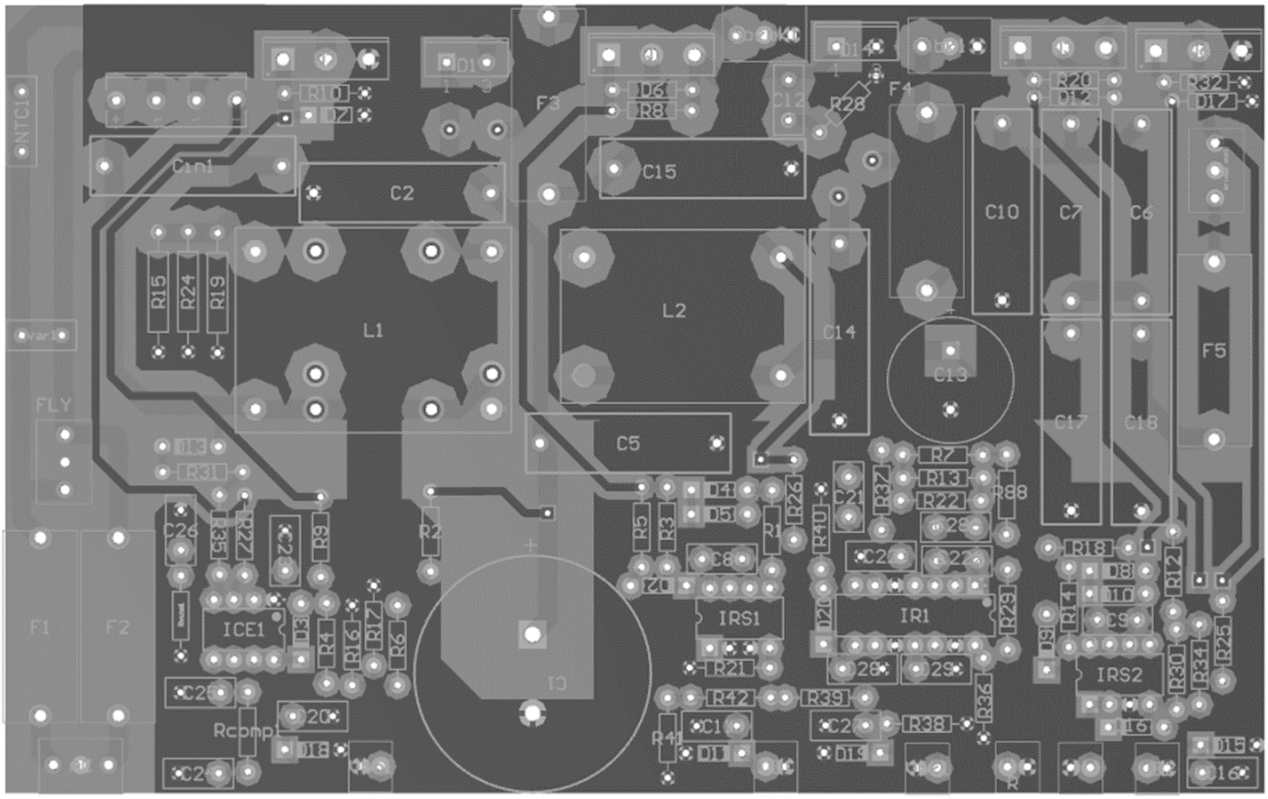


Figure 3.43: Top layer of PCB1

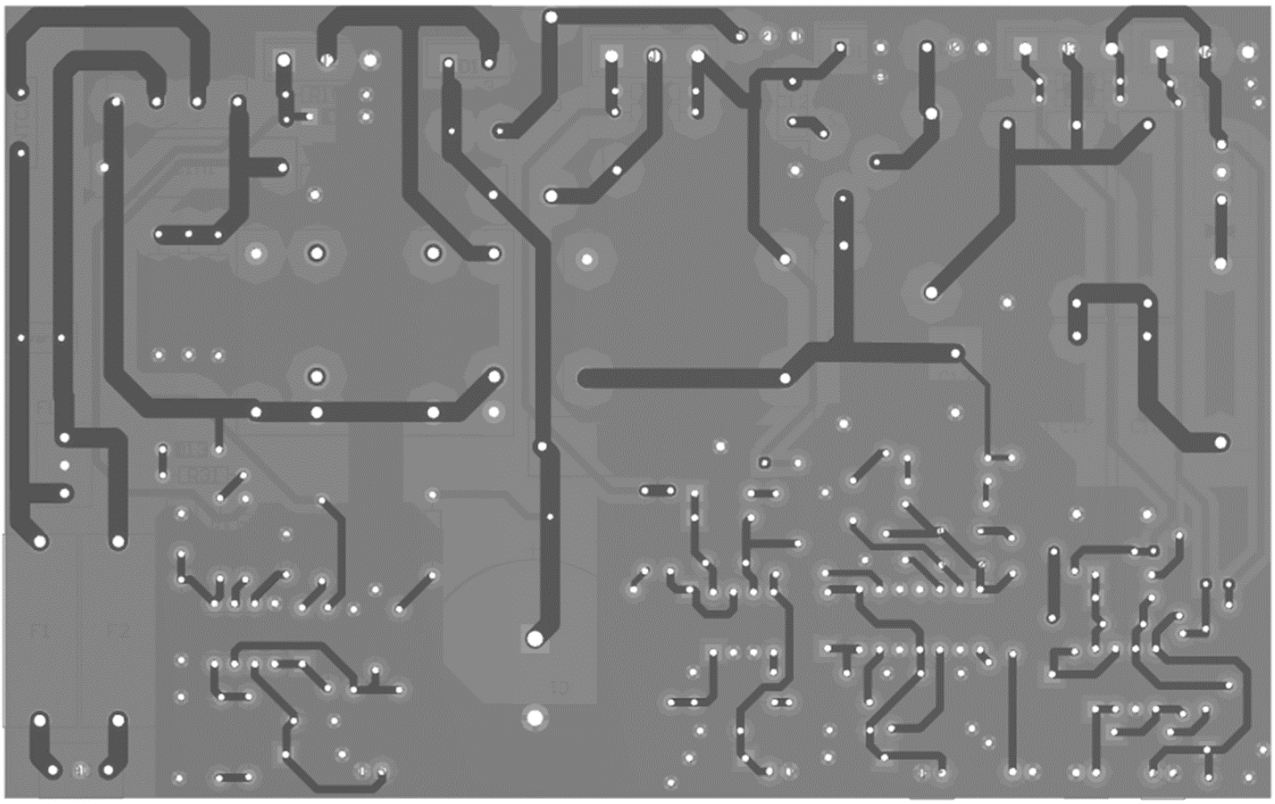


Figure 3.44: Bottom Layer of PCB1

PCB2 specifications:

- Dimensions: width 50mm, height 60mm.
- Number of components: 39
- Number of electrical connections: 23

Figure 3.45 shows the PCB2 in 3D view, while figure 3.46 shows the two layers and components connections. Figure 3.47 shows the top layer plane, while figure 3.48 shows the bottom layer plane.

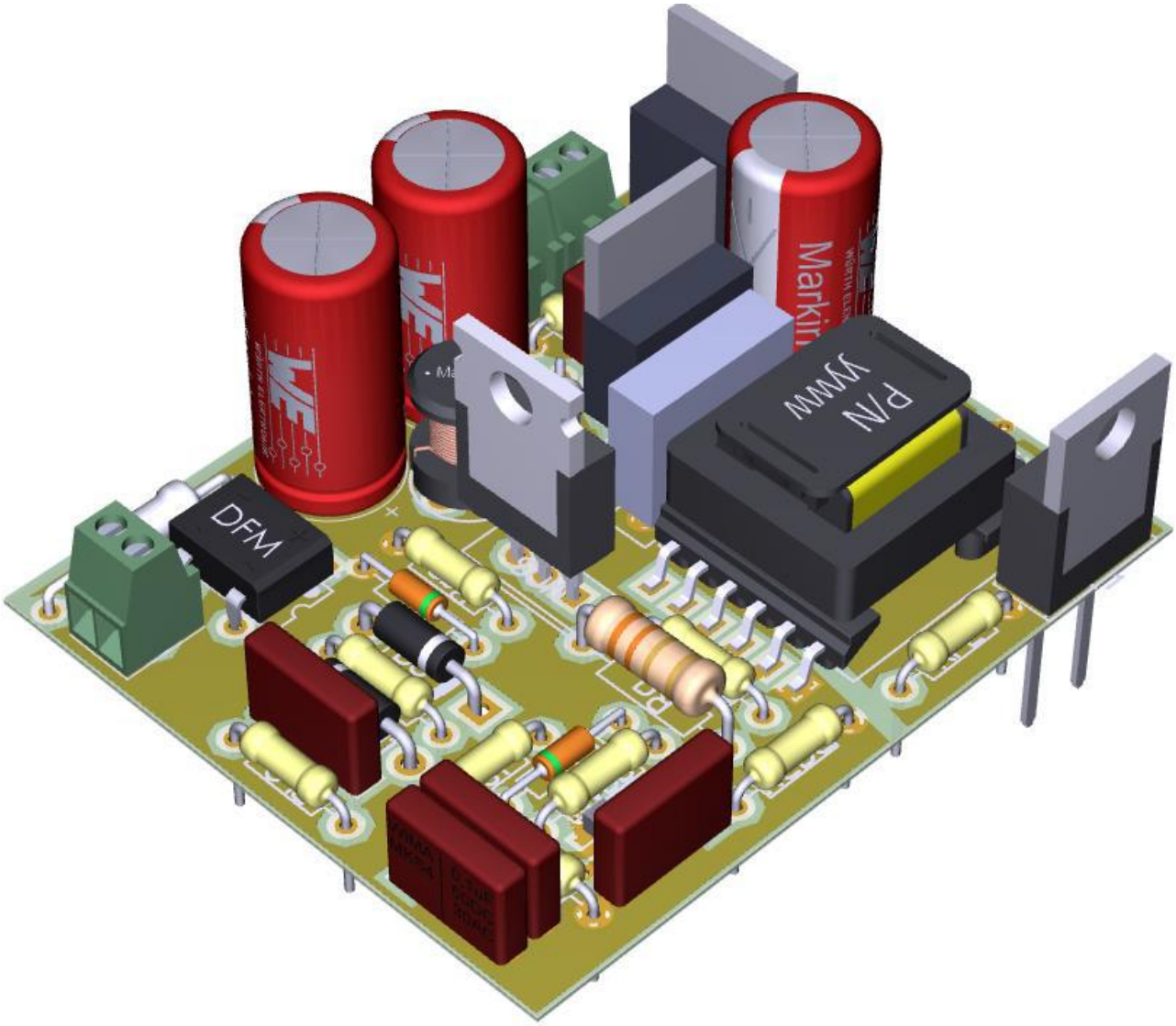


Figure 3.45: 3D view of PCB2 with components fixed

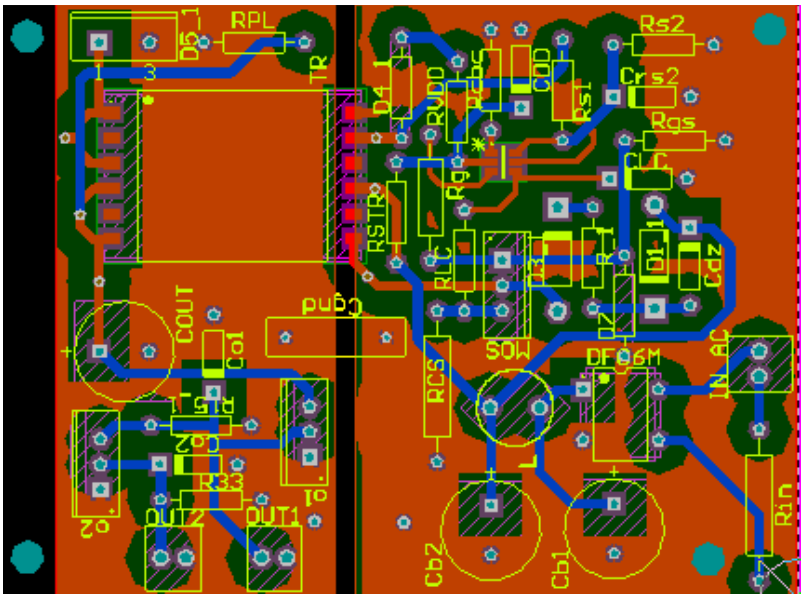


Figure 3.46: PBC2 layout with all components connections

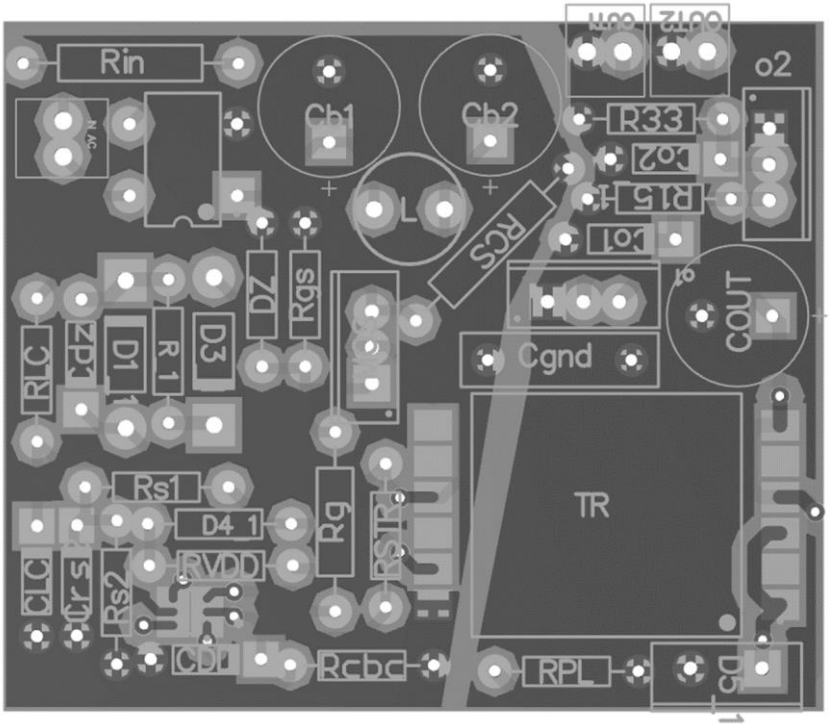


Figure 3.47: Top layer of PCB2

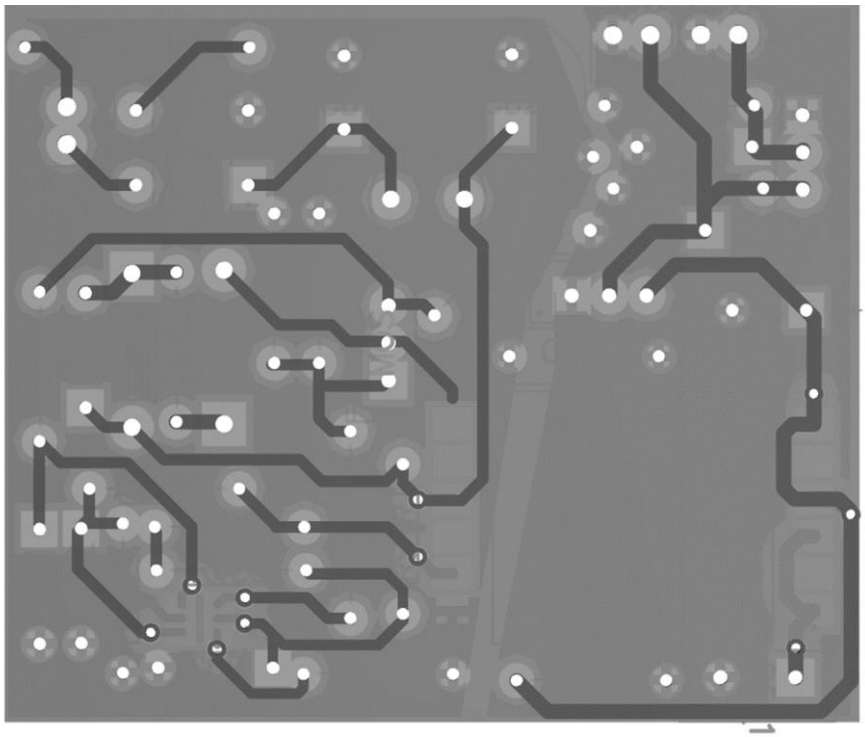


Figure 3.48: Bottom layer of PCB2

3.6 Measurements

Measurements have been performed to determine the output current for each stage and also to the power used in the system. Also, a validation test is done to evaluate the microcontroller orders to supply the square wave and fix the resonance frequency after comparing the sweep frequency to the current sensor measurements and, to validate the control of the digital potentiometer. As explained before, the system consists of 3 main stages as shown in the block diagram in figure 3.49. The first stage, is a boost converter which has mainly the role of regulating the power factor (PFC) and stabilizing the output voltage obtained from the rectifier. The second stage is a buck converter supplied with the output voltage of the boost stage. In the last stage, the half- bridge inverter receives the regulated voltage by the buck converter and supplies a square-wave signal to the piezoelectric transduces of the ultrasonic washing machine.

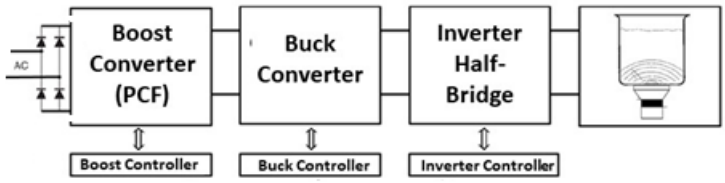


Figure 3.49: Bock diagram of the main driving system.

The real PCB after mounting all the components is shown in Figure 3.50, where the system is implement on PCB of 10*15cm designed using Altium for printed board.

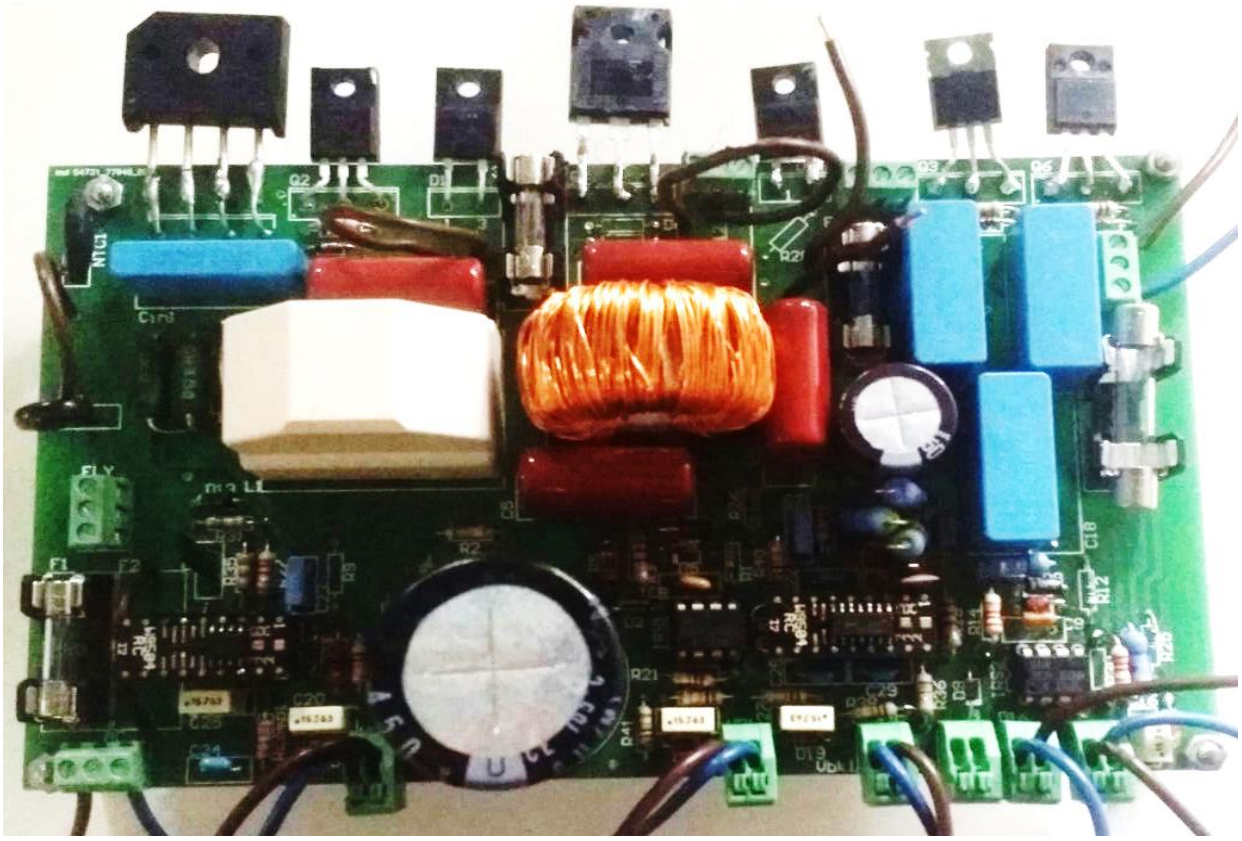


Figure 3.50: A photograph of the power-up PCB with components mounted.

The ultrasonic washing machine used is shown in figure 3.51 with details for each part of it. The tank with capacity for 15 liters of water and has 4 transducers are shown Figure 3.52. Figure 3.53 shows the measurement set-up for the power board and the Arduino board in connection to the tank and the lab instruments to analyze the performance of the circuit and validate the operation of the Arduino microcontroller to supply the square wave and read out the data from the current hall sensor.

Figure 3.51: Washing machine complete system

1) Piezoelectric Transducer
2) Power-up PCB
3) Arduino Microcontroller
4) Stainless steel TIG welded
5) Stainless steel surface
6) Keyboard with led display
7) Drain cock
8) Handles

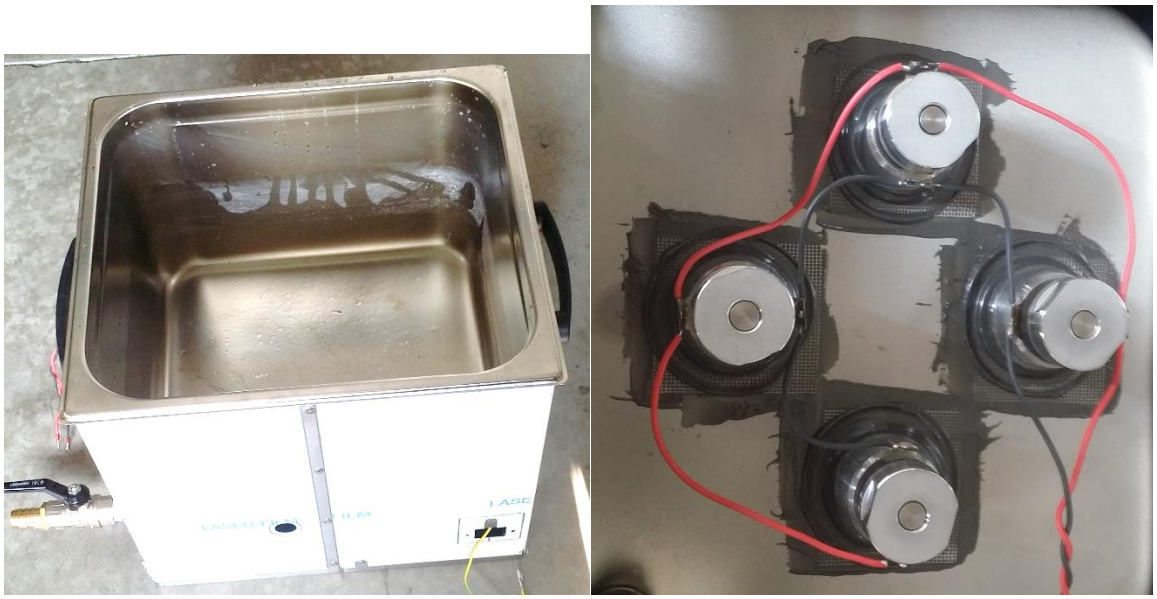


Figure 3.52: Photograph of the tank and the transducers in rear.

Figure 3.53: Photograph of the measurement setup in the Lab.

The system has been tested with two different tanks, a small one with 2 transducers and larger one with 4 transducers. The measurements show that the maximum nominal power is 80W for the small tank and 170W for the larger one. The electronic ultrasonic generator produces a continuous signal at a frequency of about 40 kHz and drives the piezoelectric transducers which transform the electrical signal into a mechanical vibration in the cleaning fluid in the tank.

The measurement performed on the boost converter with PFC control on and off are shown in Figures 3.54 and 3.55, where the output voltage is in blue and the input current in green.

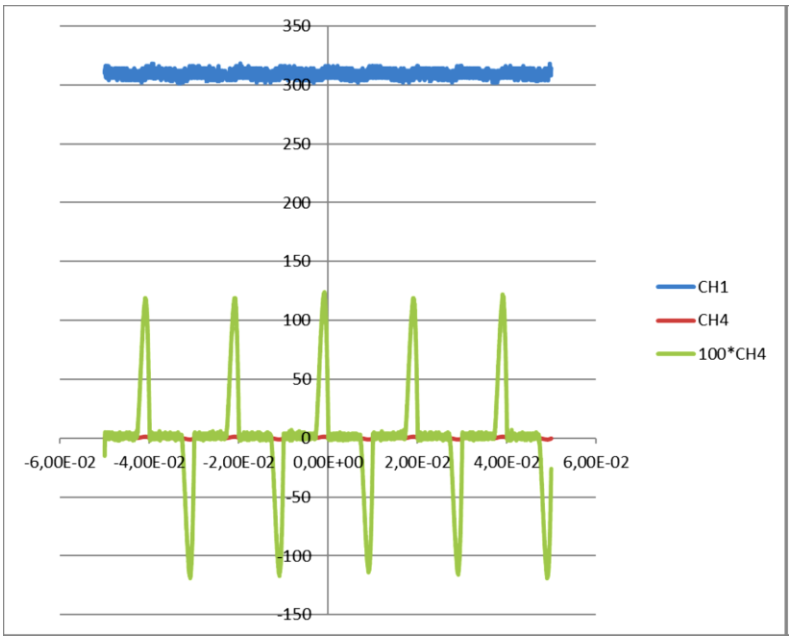


Figure 3.54: Measurement of the input current and the output voltage when PFC is OFF.

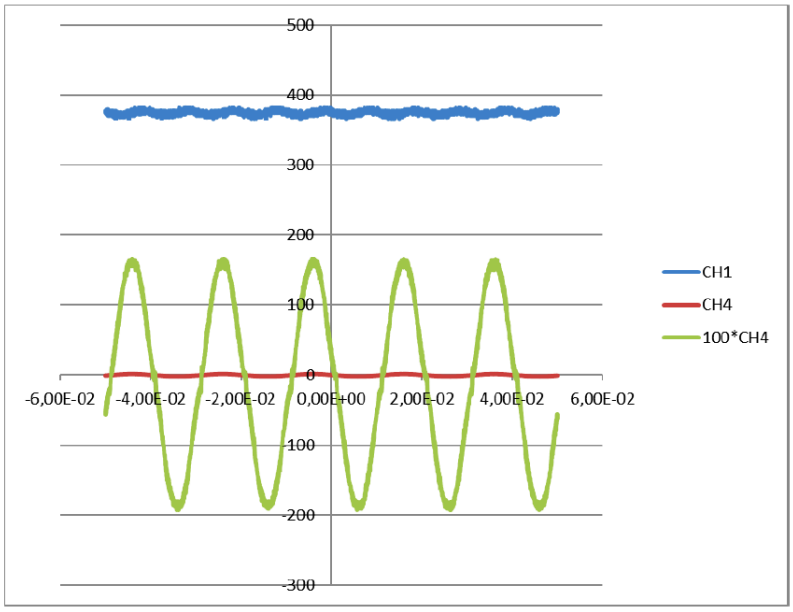


Figure 3.55: Measurement of the input current and the output voltage when PFC is ON

Figure 3.56 and figure 3.57 show the measurements of the buck converter output voltage (in blue) and the buck converter output current (in green).

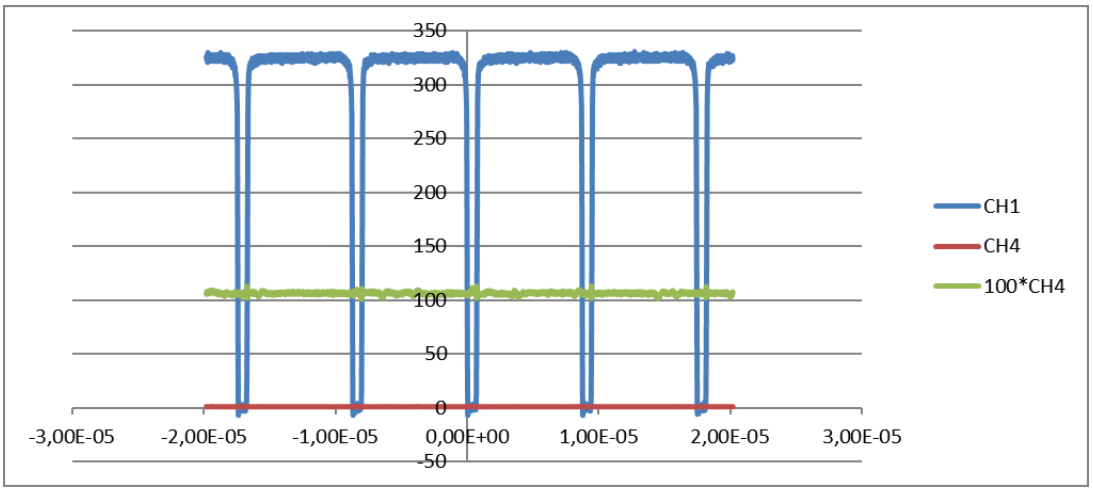


Figure 3.56: Measured voltage and current at the output of the buck converter up to 1A

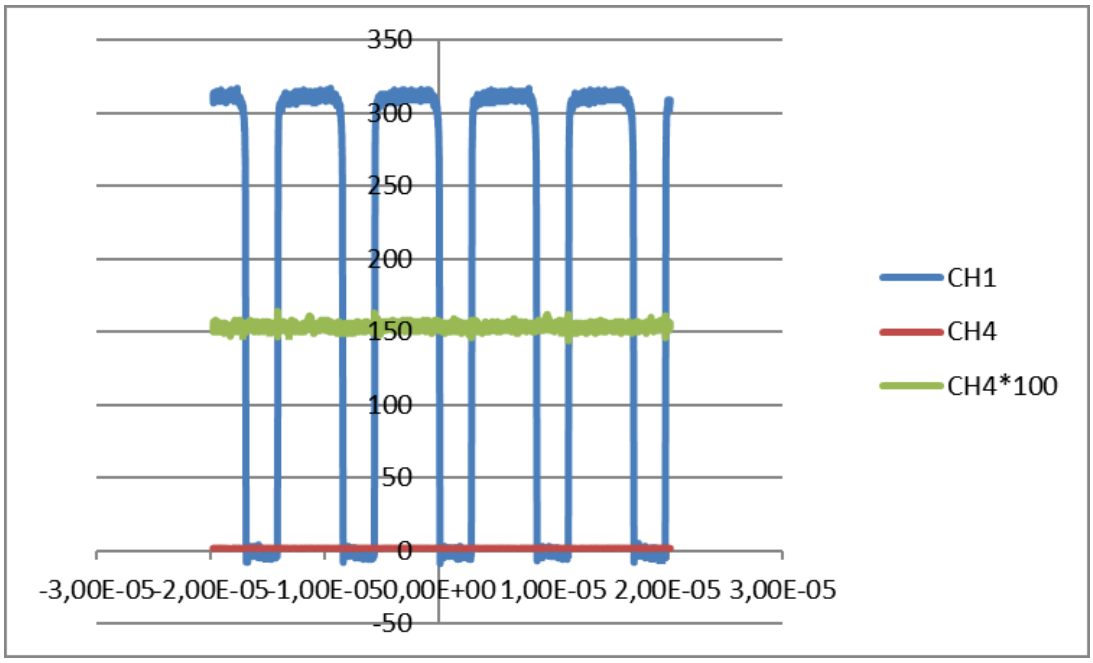


Figure 3.57: Measured voltage and current at the output of the buck converter up to 1.5A

For the Arduino Microcontroller, the board is powered by Atmel SAMD21 MCU, which features a 32-bit ARM, clock speed of 48MHz. Figure 3.58 shows the chart diagram of the software implementing the main function of sending a square-wave signal to the inverter with a sweep frequency range from 30kHz to 40kHz and receiving the measured current from the Hall current sensor. During operation, Arduino measures in parallel the frequency of the square-wave and the current value, looking for the frequency value that features the maximum current level, i.e. the resonance frequency of the transducer. The current is measured by the Hall-effect current sensor. The current flows through a copper conduction path (electrically isolated from the sensor leads) that generates a magnetic field which is

sensed by the Hall IC and converted to a proportional voltage. The voltage is amplified by a low-offset, chopper-stabilized operational amplifier and read by Arduino analog input A0. Arduino compares the variation in current value as a function of the frequency applied to the driver. Another role of the Arduino microcontroller is to adjust the digital potentiometer. At the end, the system is supposed to work for a certain specified time (for example: 1hour) then the cycle is repeated again.

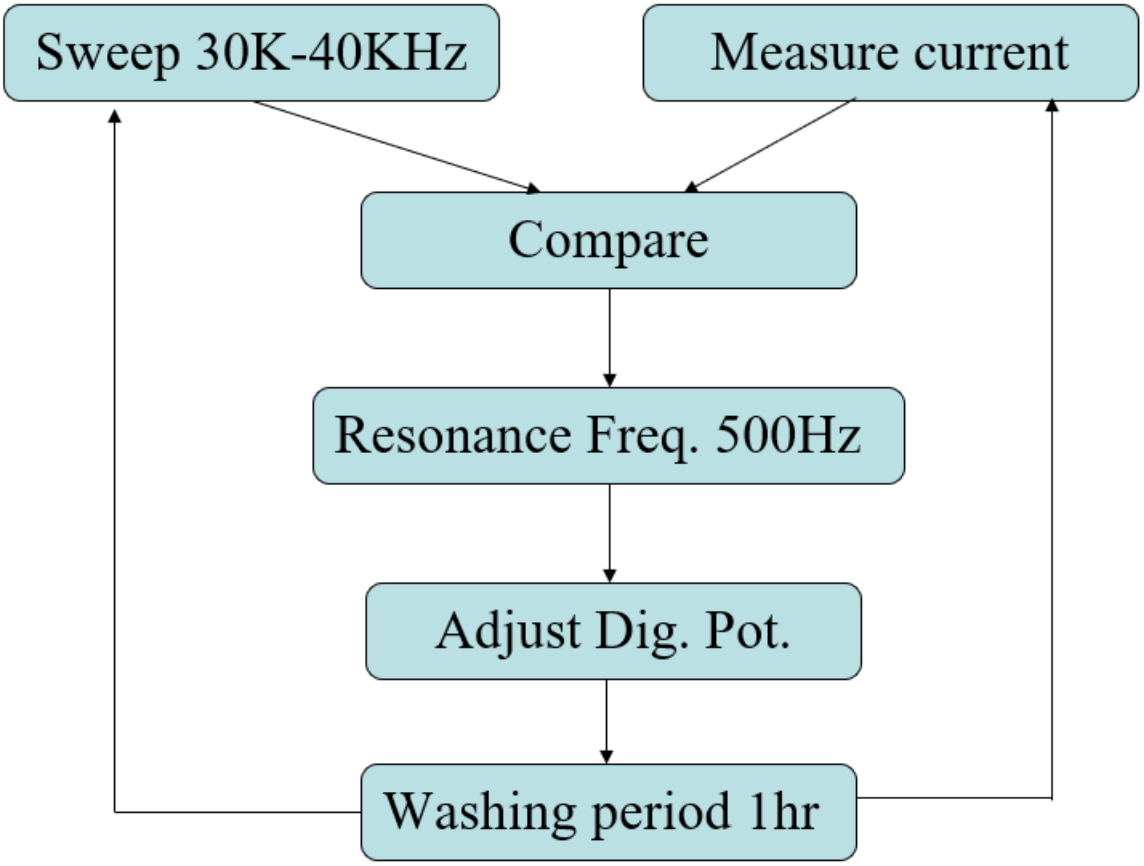


Figure 3.58: Software of the Arduino microcontroller.

3.7 Conclusion

Ultrasonic precision cleaning is a modern, safe, efficient, economical and fast way for effectively removing contaminants and tenacious deposits from objects with complex geometry. The ultrasonic cleaning benefits consist of a deep cleaning of the objects and the elimination of the risk of injury or infection with manual cleaning.

The ultrasonic cleaning mechanism consists of an electronic generator coupled to one or more piezoelectric transducers (according to the model) which are attached to the outside base of the tank in stainless steel containing the cleaning fluid. The electronic ultrasonic generator produces a continuous signal at a frequency of about 35 kHz, and controls the piezoelectric transducers which transform the electrical signal into a mechanical vibration in the cleaning fluid in the tank. With sweep system technology, the output frequency of the ultrasonic generator is modulated around a center frequency, so the ultrasonic transducer shifts between 33kHz and 40kHz. The sweep system technology offers the following advantages:

- Faster cleaning.
- Damage free cleaning.
- Increased distribution of ultrasound energy.
- Improved cavitation.
- Facilitate the ultrasonic wave crossing through the complicated objects to be cleaned.

These pressure and vacuum oscillations create a huge quantity of micro-bubbles in the cleaning liquid which, by imploding in extremely rapid succession, create enormous impact energies between the detergent liquid and the surface to be cleaned. This is known as "cavitation" and provides an efficient and safe cleaning method in less time. This high ultrasonic acoustic energy removes dirt, oil, grease, filings, small chips, surface dust, biofilm, organic matter and contamination of various kind from different shaped items like mechanical parts, gears, molds, surgical instruments, precision instruments.

3.8 Bibliography

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Part IV

4.1 Final Conclusion

Part IV

4.1 Final Conclusion

In this thesis, we presented three projects dealing with interface circuits for sensors and actuators in different application areas. In all the projects the main targets have been reaching good sensitivity, small size, and low power consumption.

The work described in this thesis stems from the consideration that the upcoming new frontier of electronics, the Internet of things (IoT), could not exist without sensors and the growing use of smart technology is indeed transforming the way in which manufacturers implement electronic devices. Sensors are indeed bringing more connectivity and analytics to the supply chain by being embedded in applications, which can help to improve the manufacturing process or the applications themselves. The lower cost, more advanced capabilities, and lower power consumption for the smart sensors will enable wider and more effective interface with IoT.

In particular, the first two projects described in this thesis deal with integrated interface circuits for microsensors, namely an integrated temperature control loop for capacitive humidity sensors in 0.35μm CMOS technology and a 14-bit extended range incremental A/D converter for high energy physics experiments in ultra-scaled technology (28nm CMOS). The main advantages of an integrated solution are essentially related to low power consumption and small area occupation, without significant losses in performances. The third project, on the other hand, deals with the driving circuit for the piezoelectric transducers used in ultrasonic washing machines.

The first part of the thesis describes a capacitive humidity sensor with integrated temperature control loop based on embedded heater and thermometer. The realized circuit enables the implementation of a self-calibration technique capable of periodically updating the calibration coefficients used to improve the performance and reliability of the humidity sensor over time. With the same technique also self-diagnostic functions are implemented, in order to determine whether the sensor is still operational.

The second part of the thesis deals with A/D converters, which are the bottleneck in the design of interface circuits for sensors in many applications. Basically, the ADC performance is often limiting the performance of the entire system and, hence, the ADC requirements are quite challenging. In addition, technology scaling does not bring that much benefit to analog circuit performance and introduces some hard challenges for achieving an acceptable dynamic range, due to the reduction of the supply voltage. At the same time, the threshold voltage is not scaling linearly with the supply voltage, thus leading to a further strong degradation of the useful dynamic range, making difficult to drive CMOS switches and use cascode configurations circuits. Despite these limitations, we designed a 14-bit incremental A/D converter, in 28-nm CMOS technology.

The third part of the thesis is discussing the driving circuit, based on AC-DC and DC-DC converters, for the piezoelectric actuators in an ultrasonic washing machine. The driving circuit implements an innovative digitally controlled frequency sweep system to track the

resonance frequency of the piezoelectric transducers and guarantee perfect cavitation in the detergent. The nominal operating frequency of the ultrasonic generator (38kHz) is swept between 35kHz and 40kHz giving faster cleaning, better distribution of the ultrasonic energy, better cleaning and improvement of cavitation.

Acknowledgment

Dear Prof. Piero Malcovati, I really learnt many things from you, not only concerning the scientific issues, but also you offered me your experience in practical life and you give me the perfect advice to move on in my career. I wanted to take a moment to say how much I appreciate the great insight you have offered me during this time.

To my college Marco Grassi, Warmest thanks for your hard work and outstanding contributions as a member of our sensor microsystem lab. I know how much time and energy you gave to help me, and I deeply appreciate all of your efforts to make it a great success. As always, it's great to know that we can count on you to go the extra mile. Thank you again for all you do.

At the end, after three years together, thanks to the one supported me always,

thanks to Magda.