UNIVERSITÀ DEGLI STUDI DI PAVIA

PH.D. COURSE IN MICROELECTRONICS

Resistive Memories for Space Applications

A Radiation-Hardening By Design Approach for Non-Volatile Memories

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Chapter 1

Radiations in Space Environments

OUR daily lives take place in an environment permeated by electromagnetic radiations. Even if our attention to this aspect has only quite recently arisen, the Earth, our atmosphere and the sun have always generated a natural electromagnetic background, beside which, as a consequence of the technological progress, the electromagnetic fields generated by all the sources related to the human activity have to be mentioned. Living beings and environment on Earth have lived and developed together with these phenomena, evolving and adapting themselves to the various radiation effects.

Ionizing radiations are characterized by very high frequencies and, high energies and high penetrating power, sufficient to induce deep interactions inside the matter. Within the Earth's atmosphere these radiations are mainly associated to the nuclear decay of particular chemical elements such as radionuclides or radioisotopes; their instability generates the emission of different high energy particles that can be characterized either by a large mass, (such as α-particles and β-particles) or low mass and higher frequency (such as X-rays and γ-rays) (see Tab. 1.1).

On the other hand, *non-ionizing* radiations are characterized by relatively low energy emissions, so that no interaction with matter arises and, hence, their main

Type	Charge	Mass [kg]	Energy [MeV]	Wavelength [nm]
α	$2e^{+}$	6.64×10^{-27}	5	7.15×10^{-23}
$\beta^{\pm}$	$1e^{\pm}$	9.11×10^{-31}	0.5	1.93×10^{-20}
γ	neutral	negligible	≈ 1	$\approx 1\times10^{-3}$
X	neutral	negligible	≈ 0.1	$\approx 1\times10^{-2}$

Table 1.1: Typical values referred to rad nuclear decay of radiative particles

effects are related to the propagation of electromagnetic waves.

In the last century electric and electronic devices as power machines, computing devices and radio-communications have acquired a central role in human everyday experience. The number of devices has impressively increased so that electronic designers had to face the issues related to both the contemporary operation of many electronic devices and the impact of their activity on the surrounding environment, such as electromagnetic interferences emissions. The study of the Electromagnetic Compatibility (EMC) has defined criteria and standards capable to ensure the desired level of reliability for the common terrestrial applications, making possible the designers to focus on continuous performance improvements and obtaining systems with an always higher number of operations per chip area.

At the beginning of the so called “satellite era” the number of space missions increased and the designers experienced a dramatic number of failures in electronic systems. What they soon realized is that outside our atmosphere, without its shielding effect, a very large variety and amount of ionizing radiations are present and the disruptive effects on electronics were their practical evidences. It has been evident since then the need to take into account the serious effects of high energy radiations on functionality and endurance of electronic circuits for space applications, including these aspects in the design flow of spacecraft systems. It is therefore clear that reliable and cost-effective designs needed a good understanding and accurate modeling of the radiation environment.

1.1 Radiations in the Near-Earth Space

High energy particles' activity outside Earth's atmosphere is due to many phenomena that can have origin inside and outside our solar system and are modulated by the complex interactions of sun, Earth's magnetic field and other planets' activities.

1.1.1 Cosmic Rays

The deep space, outside our solar system, is the scenario of many, and still not fully understood, cosmic events: planets, stars and matter masses evolve in their natural life cycles interacting with different substances. Many species of high energy particles are emitted as a product of these heterogeneous activities and are globally referred to as Cosmic Rays (CRs). CRs are originated either outside the galaxy or inside - GCRs. Little information about the direction of the source can be provided, as the complex galaxy magnetic field randomizes the trajectories of the particles.

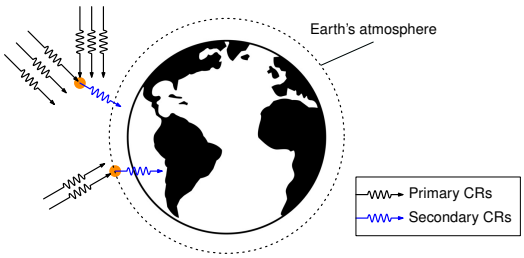


Figure 1.1: Typical interactions of primary and secondary cosmic rays.

Despite the use of the term "rays", CRs are highly energized massive particles. The *primary* CRs are the ones that reach directly the upper level of the Earth's atmosphere; here they can have further interactions and produce different emissions that are labeled *secondary* cosmic rays. Secondary cosmic rays can

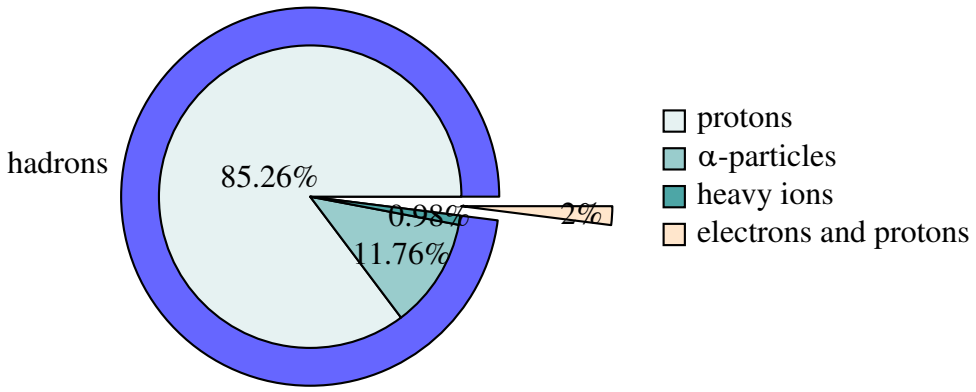


Figure 1.2: Common composition of cosmic rays.

also be produced by interactions in the interstellar medium, typically *spallation* products from cosmic ray collisions (See Fig.1.1).

The composition of CRs is mainly constituted by hadrons, but all Periodic Table elements can be found (See Fig.1.2). Their occurrence decreases with the atomic number Z, with a steep decrease for elements higher than iron. Fig.1.3 shows the relative abundances of GCRs [1.1] in both inside and outside our solar system. As it can be seen, the two chemical compositions of CRs are similar one to the other, indicating the stellar origin of cosmic rays. The differences that can be noticed can be due to some secondary nuclei produced in the spallation of heavier elements (i.e. Li, Be and B from C and O, or Mn, V, and Sc from the fragmentation of Fe).

Typically the energy distribution for the most common elements has a peak around 1GeV/amu. As it will be discussed later, the solar activity influences the measured fluence of the particles and, in particular, the higher solar activity acts as a shield for CRs. In Fig. 1.4 the energy spectra of some elements are shown, [1.2]. For higher energies no change in fluence is noticeable, while, for lower energies, fluences are strongly modulated by solar activity.

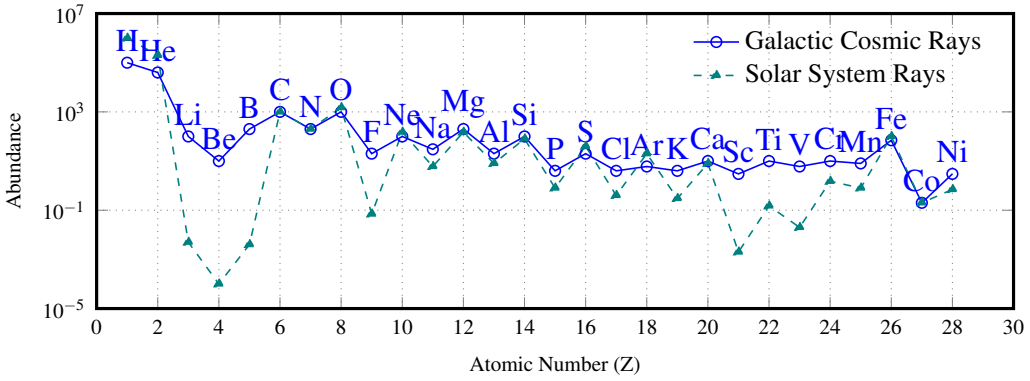


Figure 1.3: Abundances of GCRs.

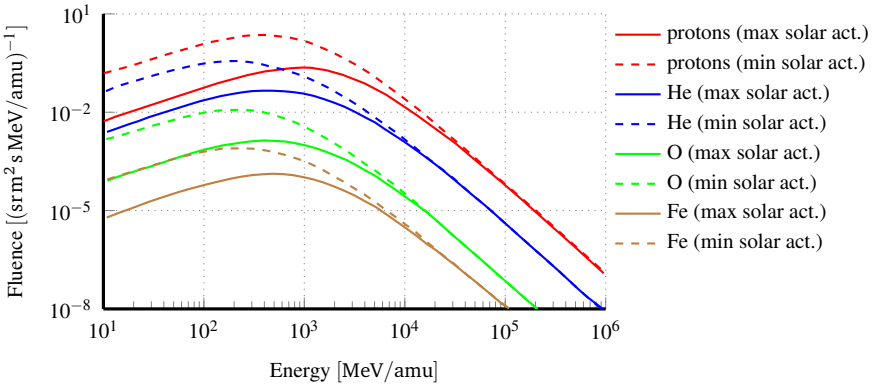


Figure 1.4: Energy spectra for hydrogen, helium, oxygen and iron.

1.1.2 Solar Activity

The sun is a very important source of radiations and, moreover, with its activity strongly modulates the exogenous radiation phenomena. In the first case, the particle events that take origin from the solar activity can be classified into two important categories: solar flares and Coronal Mass Ejection (CME).

The coronal magnetic field of the sun confines high energies. When the local energy becomes too high, it is released in peculiar explosions that cause the solar flares. This activity, having the duration of hours, arises electron reach ionic emissions.

Beside these short emissions, CMEs are the main cause of radiative disturbances in outer space; they consist in large plasma eruptions that accelerate particles with their shock waves. Their activity can last for days and produces emissions reach in protons (96.4%), α-particles (3.5%) and heavy ions (0.1%). Their energies can reach 1GeV.

Sun's activity, even if stochastic, shows a periodic behavior. A 11 years average activity period has been noticed (7 years of strong activity followed by 4 years of low activity), after which the sun's magnetic polarity switches (having a global average period of 22 years).

1.1.3 Earth's Magnetic Field and Radiation Belts

The Earth is surrounded by a strong magnetic field that surrounds and protects the planet against the actions of the cosmic radiations. The main contribution of the magnetic field is internal, probably originated by a fast spinning iron core.

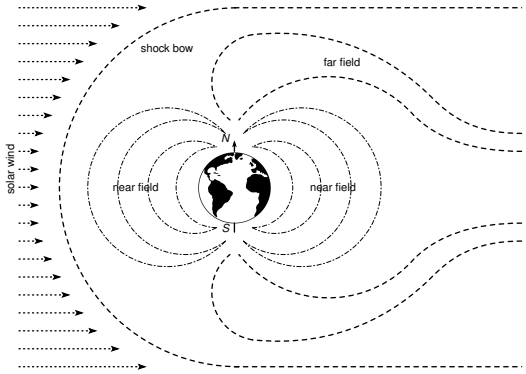
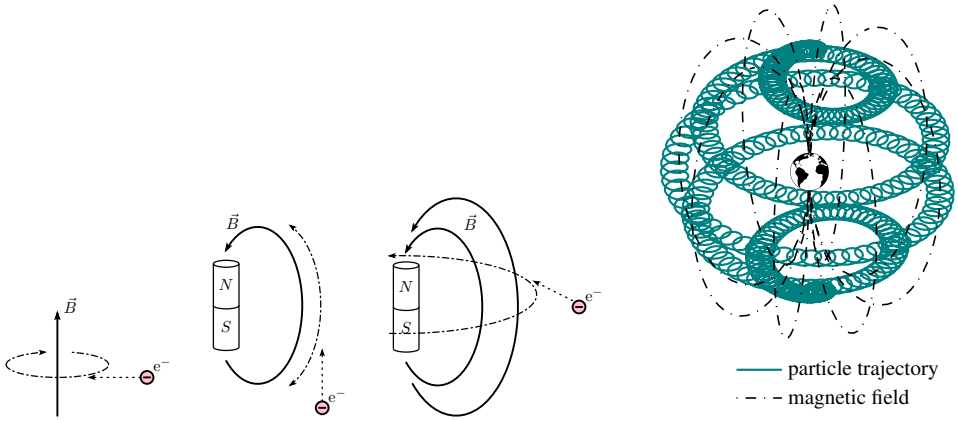


Figure 1.5: Scheme of the Earth's magnetosphere.

For this, the near magnetic field (at about 5 to 6 Earth radii) behaves approximately as a magnetic dipole, with the magnetic axis really close to the Earth's rotational axis and the magnetic north-pole as oriented as the geographic north. The near field lines move from the north pole, describing coils and closing inside



(a) Gyration **(b)** Bounce **(c)** Drift **(d)** Overall motion

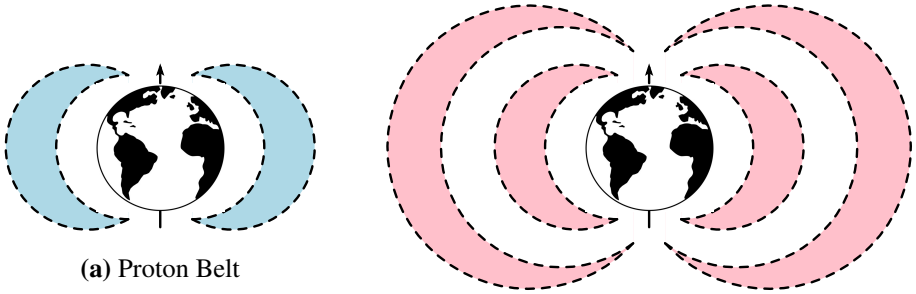
Figure 1.6: Fundamental periodic motions in (a), (b) and (c) of the charged particles under the influence of the Earth's magnetosphere. In (d) the scheme of the global motions is represented.

the south pole. On the other hand, the far field is quite different, as it is strongly influenced by the intense solar wind generated by the sun emissions. The ejected high energy ions that reach the Earth's magnetosphere, in fact, compress the field lines of the day-side and stretch the field lines of the other side until forming a bundle of aligned lines.

When a charged particle reaches the near magnetic field, its trajectory will be strongly influenced. In particular, as illustrated in Fig. 1.6, the dipolar magnetic field can bring to three kind of periodic movements of the particles:

Gyration: When a charge particle moves with a velocity component orthogonal to the field line, it will be accelerated by a Lorentz force, and it will rotate around the field line.

Bounce: This motion is due to the velocity component of the charge particle parallel to the field line. As the particle moves toward increasing magnetic field, its parallel speed component will decrease, till stopping and inverting



(a) Proton Belt

(b) Electron Belts

Figure 1.7: Van Allen Belts.

the direction of the parallel component.

Drift: The drift movement is due to the fact that particles approach Earth traveling toward increasing magnetic field. For this reason the gyration axis rotates in turn around the magnetic axis.

The composition of these quasi-periodic motions induces the accumulation of charged particles that get trapped in some regions of the near magnetosphere. These regions are named *Radiation Belts* or *Van Allen Belts*.

Proton Belt: The closer belt, extended from 1.5 to 4 Earth radii, is rich in protons and, hence, called *proton belt*. Protons energy can be from few MeV to hundreds of MeV.

Electron Belt: The *electron belt* is rich in electrons and has two maxima in electron flux, the inner at around 1.4 Earth radii and the outer at around 5 Earth radii. Maximum electron energies are around 10MeV.

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Chapter 2

Radiation Effects On Electronic Devices

THE high energy particles activity in the space has been discovered by reason of the damaging effects on electronic systems sent in the first missions outside the Earth's atmosphere. Since then, many studies have been carried on and the main phenomena involved have been characterized and modeled.

It has been suddenly clear that, according to the kind of failures occurring in systems, there was a strong dependance between the radiation effects and the exposure time. In particular, longer exposures caused a higher degradation and shorter lifetime of the devices. In this case devices were experiencing the so called *cumulative effects* of radiations.

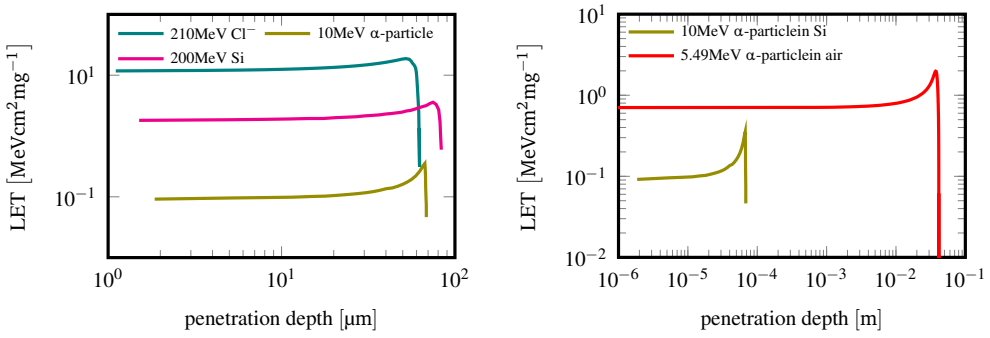
On the other hand, other failures were occurring in a total stochastic way, showing that energy particles could instantaneously lead to immediate functional failures or disruptions; this is the case of the *transient effects*.

In this chapter the main physical phenomena involved in the interactions between radiations and semiconductor devices will be discussed analyzing the specific cases for the memory devices.

2.1 Ionization Process

The most important interaction between a high energy particle and a target material is the *ionization*. As it travels in the target medium, it releases its energy to it, along its path. At a certain distance, defined as *range*, the particle has lost all its energy and stops.

The amount of energy transferred per length unit is defined as LET and it is measured in $\mathrm{MeV} \cdot \mathrm{cm}^2 \cdot \mathrm{mg}^{-1}$, as it is normalized by the density of the target material.



(a) LET in Silicon target

(b) LET in different targets

Figure 2.1: LET versus penetration depth for (a) different particles and (b) different targets.

The interaction between the particle and target material is usually represented by the relative LET as a function of the penetration depth. In Fig. 2.1 some examples are shown. As it can be seen, energy transfer has a peak, referred to as *Bragg peak*, after which all energy turns out to be transferred.

As electronic systems are constituted by semiconductor devices, almost entirely silicon, it is fundamental to understand the effects of this energy transfer inside the semiconductor lattice. In semiconductors, thanks to their energetic structure characterized by a band gap energy, the conductive process is determined by

bipolar charge carriers, electrons and holes. As introduced, high energy radiations transfer energy to the atoms in the semiconductor lattice, ionizing them and, consequently, generating electron-hole pairs (HEPs).

The generation rate is proportional to the LET and depends on band gap energy height of the target material. In an equilibrium condition HEPs would suddenly recombine for the charge neutrality, ideally completely, with a fast recombination rate f_y due to the high mobility of electrons.

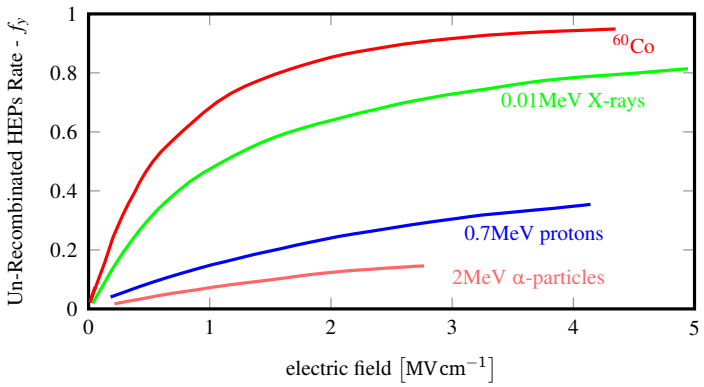


Figure 2.2: Recombination rates for different colliding particles. For larger electric fields the recombination decreases, as newly formed HEPs are suddenly split away.

On the other hand, in presence of an electric field, HEPs' recombination drastically decreases, inducing a certain amount of free net charge available. This radiation-induced charge is the responsible of the electrical effects in semiconductors. In Fig. 2.2 the recombination rate as a function of the applied electric field is represented. As said, the recombination decreases with larger electric fields and, for higher incident energies, the decrease of recombination rate saturates, as a the initial energy is high enough to separate the HEPs.

2.2 Cumulative Effects in Semiconductors

Cumulative radiation effects are related to the atomic damage induced by the high energy particles passing through the semiconductor lattice. The longer is exposure to radiations, the higher is the damage induced and, therefore, the entity of the effects depending on the Total Ionizing Dose (TID) of radiation.

As it will below explained, if a devices is exposed to a certain amount of radiation, it will exhibit a high parameter drift mainly through:

- intra-device leakage (2.2.2),
- inter-device leakage (2.2.3),
- transconductance degradation (2.2.4).

2.2.1 Radiation Effects Mechanisms in MOS Oxides

The almost whole amount of present integrated circuits are based on the CMOS technology and thus a Metal-Oxide-Semiconductor (MOS) structure will be considered. In such devices the SiO_2 layer plays an important role under radiation exposure, [2.1]. When a high energy particle crosses a MOS device, its energy is transferred along its path. If this energy is sufficiently higher than the SiO_2's energy band gap (and this is the case, as particles' energies are around MeVs, while $E_{gSiO_2} = 8\text{eV}$) its atoms are ionized and HEPs are generated. As long as the radiation induced HEPs's energies are higher than the oxide's band gap energy, more HEPs can be generated in turn. Thus, a single radiation event can raise to a big amount of free charge in the semiconductor.

As soon as these carriers are generated, many of them naturally recombine; the net remaining number of carriers drift under the action of the applied electric field. If a positive voltage is applied to the gate, electrons, faster carriers, will

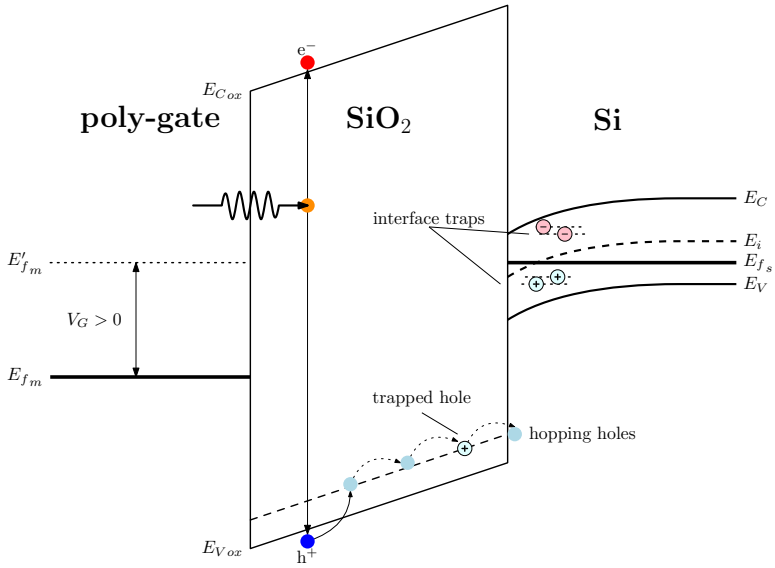
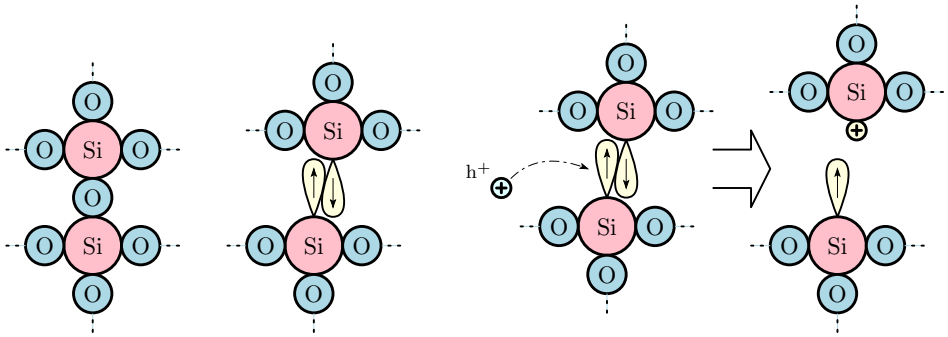


Figure 2.3: Band diagram of a MOS structure under the action of a direct gate voltage. The hopping movement of the holes is shown. During their drift holes are trapped by either oxide or interface traps.

move directly to it. On the other hand, holes drift toward the Si/SiO_2 interface is a bit more complex: because of their higher effective mass and the electrostatic interactions with the lattice, holes move through a *polaron* hopping, [2.2,3]. This mechanism is really dispersive and strongly dependent on the temperature and, important, on oxide thickness. A scheme of the generation and drift of the radiation-induced HEPs is shown in Fig.2.3.

The clumsy drift of holes is subjected to the presence of trapping centers that build up positive charges clusters. These traps are located either inside the oxide, close to the interface with Si (oxide traps) or at the Si/SiO_2 interface (interface traps).

Oxide Traps are the consequence of the large number of oxygen vacancies caused by the oxygen out-diffusion in the oxide [2.4] whose dependency is strictly correlated to the manufacturing process quality. In particular, in amorphous sili-



(a) Normal SiO_2 lattice structure

(b) Oxygen vacancy into the SiO_2 lattice

(c) Hole trapping mechanism in a oxygen vacancy

Figure 2.4: Oxide trapping mechanism. The radiation-generated hole accept an electron made disposable by an oxygen vacancy in the silicon oxide.

con oxide it is possible to find clusters of SiO_2 molecules in which the shared atom of oxygen is missing (the oxygen vacancy) and two valence electrons are shared. This structure, even if electrically neutral, is really easy to donate one electron to the radiation-generated hole and so it splits, remaining with an unbalanced positive charge. A scheme is represented in Fig. 2.4.

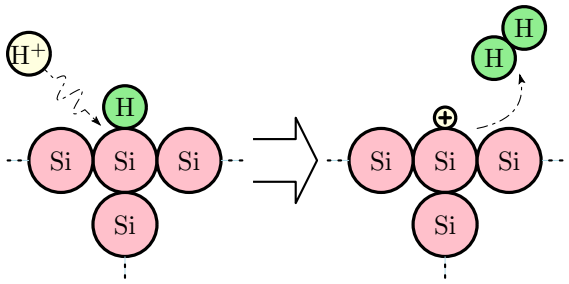


Figure 2.5: Interface trapping mechanism. Protons capture hydrogen electrons and form a new H_2 molecule.

Charge traps are also present in silicon at the oxide interface and they can occupy both donor or acceptor energy levels, [2.5]. Donor impurities behave as

positive charges, leading to a negative shift of the threshold, while acceptors build up negative charges, causing a positive threshold shift.

The most common mechanism, however, is originated by a defect generation due to hydrogen atoms. At the Si/SiO_2 interface the dangling silicon bond is passivated by an hydrogen atom, introduced inside the lattice during the manufacturing process. When a radiation-generated proton (H^+) passes by the lattice, it may happen that the hydrogen-silicon bond is broken and the electron is captured to neutralize the hydrogen ion, [2.6]. In Fig. 2.5 the hydrogen/proton interaction is shown.

Charge trap mechanisms are not only present at the gate silicon/oxide interface, but may arise at any depth of the bulk oxide layers, such as in the thick field oxide (FOX), Silicon On Insulator (SOI) buried layers and MIM capacitors.

The first consequence of the trapped charges is the MOS threshold voltage shift, due to the different flat-band condition. In particular, if N_{ot} and N_{it} are respectively the oxide and interface trap densities ($[\text{cm}^{-2}]$), the threshold voltage shift can be evaluated as:

$$\Delta V_{th} = -\frac{eN_{ot}}{c_{ox}} - \frac{eN_{it}}{c_{ox}} \tag{2.1}$$

where $c_{\text{ox}} = \frac{\varepsilon_{ox}\varepsilon_0}{t_o x}$ is the oxide capacitance per area unit ($[\text{Fm}^{-2}]$). A first consideration arising from 2.1 is that for a positive charge the voltage shift is negative: positive trapped charges recall for induction electrons at the silicon interface, and in this way the electric potential at the interface decreases, and so the flat-band voltage. An example of the threshold voltage shift is shown in the scheme of Fig.2.6.

An expression for N_{ot} as a function of the total dose D, the un-recombined HEPs rate f_y, and the HEPs generation rate per rad κ_g is given by [2.7, 8]:

$$N_{ot} = D\kappa_g f_y f_{ot} t_{ox} \tag{2.2}$$

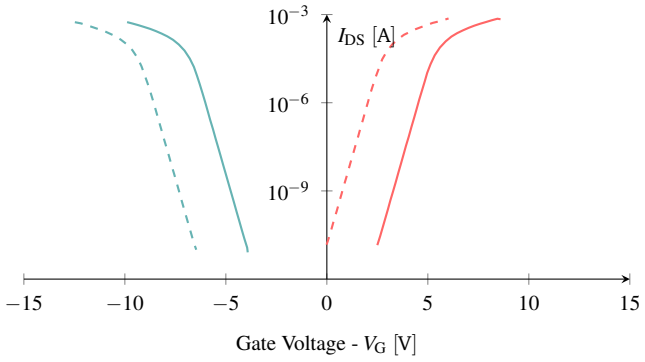


Figure 2.6: Representation of the threshold voltage shift for both a nMOS and a pMOS.

where f_{ot} is the hole trapping efficiency, depending on the electric field.

Thus, combining 2.1 and 2.2, the quadratic dependance of the threshold voltage shift due to oxide traps on the oxide thickness can be outlined:

$$\Delta V_{th,ot} = \frac{eD\kappa_g f_y f_{ot} t_{ox}^2}{\varepsilon_{ox}\varepsilon_0} \Rightarrow \Delta V_{th,ot} \propto D t_{ox}^2 \tag{2.3}$$

meaning that cumulative effects decrease with smaller oxide thicknesses. This was intuitively predictable, because, as the thickness decreases, same happens to the number of impurities, and hence to the total amount of build up charge; moreover, a smaller thickness means a higher electric field, thus a larger amount of charge recalled into the channel. Oxide thickness, together with its purity, becomes so a key feature for the radiation effect control, implying that cumulative effect radiation hardening of MOS devices increases with device scaling.

In Fig. 2.7 some experimental results emphasizing the threshold voltage shift dependence on the total dose is represented. Then, Fig. 2.8 shows the threshold voltage shift dependence on the oxide thickness.

It has also been noticed that these cumulative mechanisms are partially reversible. In fact, as soon as a certain amount of positive charge is trapped, electrons tend to neutralize it either thanks to either interface tunneling [2.9–13], or thermal emission of electrons from the oxide valence band [2.13]. For this reason,

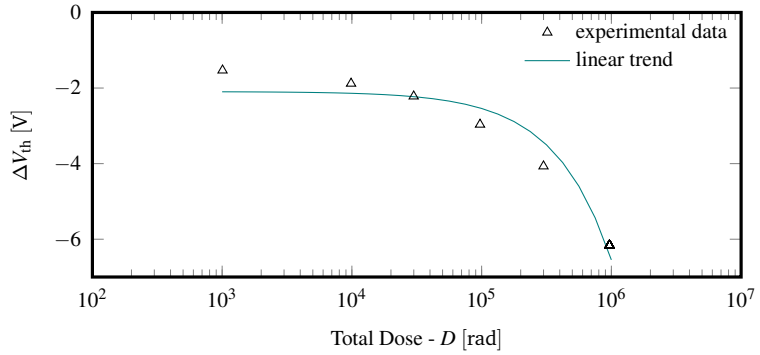
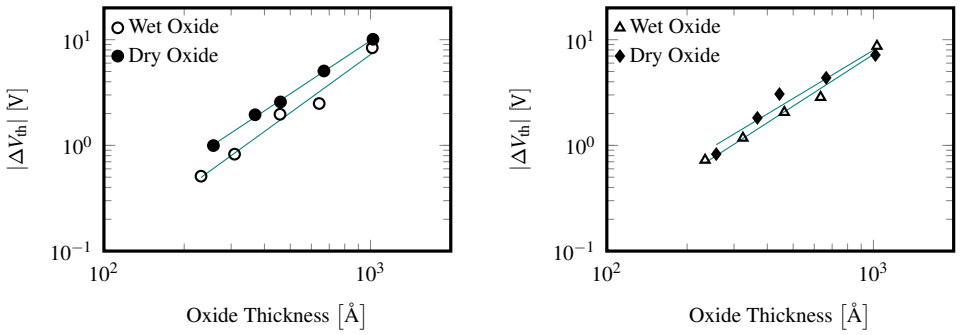


Figure 2.7: Threshold voltage shift versus total ionizing dose. The linear dependency on the total dose D can be recognized.



(a) Oxide Traps

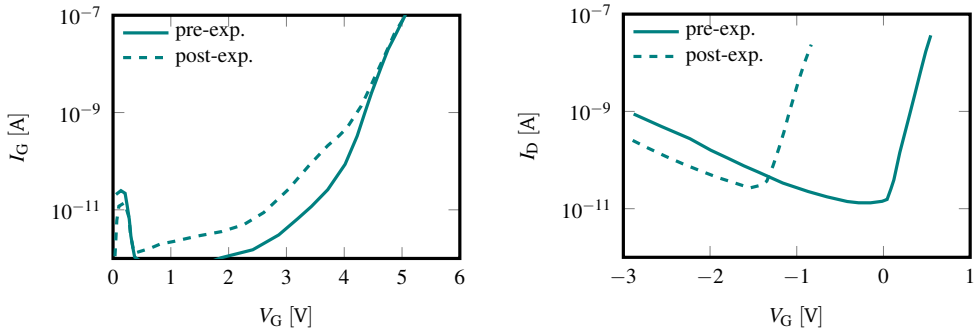
(b) Interface Traps

Figure 2.8: Dependency of radiation-induced threshold voltage shifts.

controlled annealing procedures can be useful to neutralize the trapped charges, [2.14].

2.2.2 Radiation-Induced Leakage

When the thin oxide of a MOS structure is exposed to radiations, radiation-induced leakage current (RILC) phenomena arise. If a positive gate voltage is applied to an irradiated MOS device, an increased gate leakage current will be measured. Fig.2.9(a) depicts some experimental results from [2.15]. As it can be noticed,



(a) Gate leakage

(b) Drain leakage

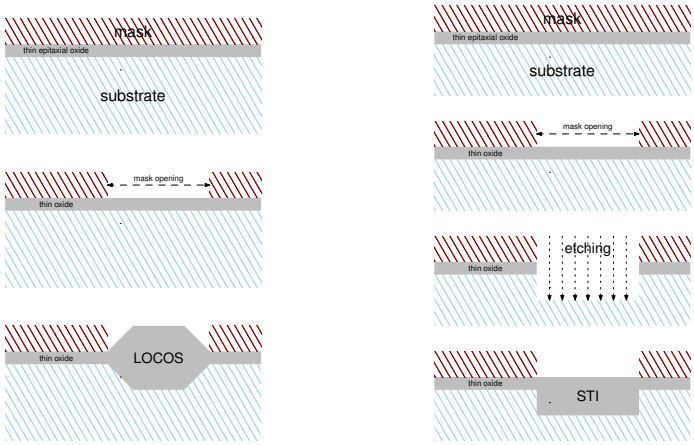
Figure 2.9: Radiation-induced leakage currents before and after irradiation of a n-channel MOS device. In (a) the gate current before and after irradiation of a n-channel MOS device exposed to 5.3Mrad of ^{60}Co γ-rays, while in (b) the drain current before and after irradiation of a n-channel MOS device exposed to 1Mrad of ^{60}Co γ-rays.

the two curves tend to coincide for higher voltages, as for low electric fields the radiation-induced aspect is predominant, while it becomes negligible for higher voltages with respect to the other leakage effects (stress induced leakage or hot-electrons tunneling). On the contrary, in p-type MOS transistors, accumulated charges induce an increase of the threshold voltage (in absolute value), degrading its conductive performance. The reasons behind this leakage current are due to the formation of electron traps inside the oxide layer that facilitate the tunneling of electrons from silicon to gate.

Moreover, as mentioned, a direct consequence of the charge trapping at the gate oxide is the threshold voltage shift in a MOS device. For a positive charge build up the threshold voltage shift is negative and in a n-channel MOS the sub-threshold Drain currents dramatically increase. Fig. 2.9b shows measured data taken from [2.16]. In the picture is shown the drain radiation-induced leakage current of a n-channel MOSFET for drain voltage.

2.2.3 Parasitic Field Oxide FET

In real CMOS integrated circuits the oxide layer covers all the substrate, except for the breaches created for the contacts for the electrical connections. The thin gate oxide layer covers the channel area between the source and drain diffusions, while the thick FOX lays elsewhere, eventually filling lower etched profiles created to insulate the different devices. First types of FOXs were fabricated with LOCOS, where the thick oxide's growth was obtained through a oxidation of the silicon bulk. Latest techniques has allowed the use of STIs in which oxide is deposited by mean of an epitaxial growth after a deep etching of the substrate. In Fig. 2.10 the technological manufacturing steps for LOCOS (Fig. 2.10a) and STI (Fig. 2.10b) are shown.



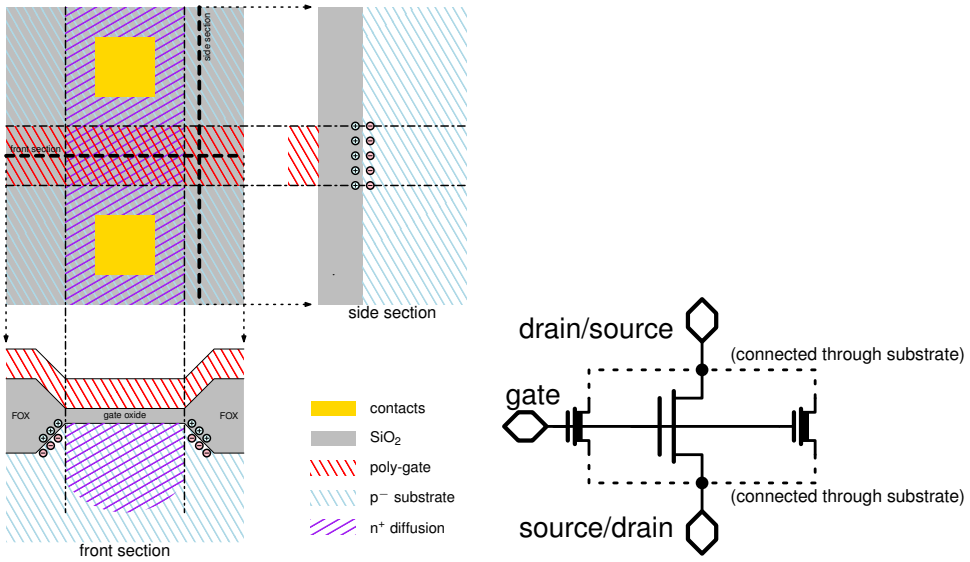
(a) LOCOS technological steps

(b) STI technological steps

Figure 2.10: Substantial technological steps of the LOCOS and STI manufacturing.

In both cases, at the silicon/oxide interface and inside the FOX, a large amount of positive charge traps build up. The poly-silicon gate edge, then, overruns the diffusion area of the mos, overlapping the FOX and creating a narrow parasitic FET with the source/drain areas corresponding to the undoped bulk. As previously

described in 2.2.2, under the parasitic gate regions the positive charges arise a negative threshold voltage shift, so that the parasitic FET is slightly on.



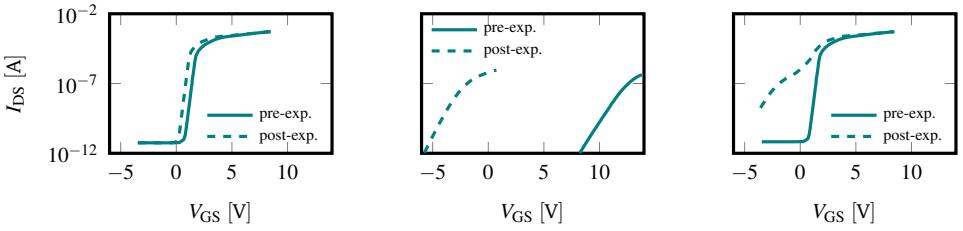
(a) Parasitic channel build up at gate edges. **(b)** Electrical scheme of the parasitic FET.

Figure 2.11: Description of the parasitic FET effect at the gate edges. The gate overlaps on the thin/thick interface create two built-in depleted field effect transistors (FETs).

As a result, at the edges of the poly-gate there are two parasitic n-channel FETs in conduction, electrically connected in parallel to the real n-channel MOSFET. As radiation exposure increases, the parasitic FETs become more and more conductive, and as a consequence the parasitic currents may lead to the total failure of the device.

In Fig. 2.12 experimental data are shown. The parasitic FETs before irradiation show a really high threshold voltage, because of the large thickness of the oxide. However, after irradiation, there is a consistent negative shift in their threshold, for the large number of oxide damages.

Summarizing, TID effects are strongly related to the quality of the crystalline substrate, as impurities collect the charges generated by the radiation particles



(a) MOSFET **(b)** Parasitic FET **(c)** Combined Effects

Figure 2.12: Measured data for leakage currents in the parasitic edge device.

striking the device, causing parameters drift and leakage. For this reason, high quality technology processes are mandatory for the global endurance of the system.

2.2.4 Transconductance Degradation

For a MOS transistor the transconductance is proportional to $\bar{\mu}$, the carrier mobility at the proximity of the oxide/silicon interface. Mobility is strongly influenced by the carrier scattering, as it depends on the average time between scattering collisions. Collisions in a perfect lattice would be almost absent, but, due to the real nature of matter, mobility is finite. As radiation dose increases, the lattice damage due to the oxide and interface traps increases as well, consisting in a degradation of the average collision time and, thus, of the mobility, [2.17–19]:

$$\bar{\mu} = \frac{\mu_0}{1 + \alpha_{ot} N_{ot} + \alpha_{it} N_{it}} \tag{2.4}$$

showing once again, according to 2.2, a strict dependance on total dose and oxide thickness.

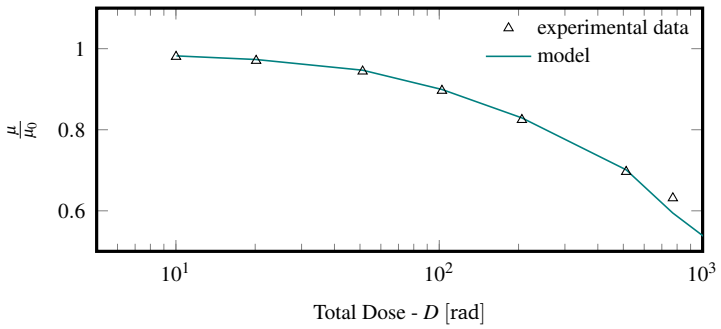


Figure 2.13: Experimental and modeled mobility damage versus the total ionizing dose D, [2.17].

2.3 Single Event Effects

The energy transferred by a radiation particle crossing a device can lead to instantaneous phenomena. If not properly managed, these effects can have a serious impact on the normal device operation, endurance and lifetime. In fact, even if the event times are in the range of thousands of picoseconds, consequences may lead from a single electrical transient to disruptive current streams. All these effects are referred to as Single Event Effects (SEEs) and, according to their impact on electronic systems, they are classified in *soft* or *hard errors*.

Soft Errors: they are reversible functional errors due to SEEs not affecting the physical integrity of the devices. They can arise from different electrical mechanisms and thus they are accordingly classified as follows:

- **Single Event Transient (SET):** spurious signal spikes instantaneously induced by the ionization;
- **Single Event Upset (SEU):** SETs of larger duration can lead to soft errors and bit flips in the digital memory elements;
- **Multiple Bit Upset (MBU):** high energy ions can interest more elements in their ionization path; if transients, and thus upsets, interest

multiple memory elements, multiple bits can erroneously flip.

- **Single Event Functional Interrupt (SEFI):** from a digital system aspect, SEUs can cause global system failures; in this case SEEs lead to serious SEFIs.

Hard Errors: are irreversible and destructive phenomena induced by instantaneous events. Most important are the following:

- **Single Event Latch-ups (SELs):** are latch-ups induced by radiation ionization, very important and harmful in CMOS technologies;
- **Single Event Hard Errors (SHEs):** some non-volatile memories (NVMs) such as erasable programmable read only memories (EPROMs) or other one time programmable (OTP) memories, can be subjected to such radiation-induced currents that some bits can erroneously flip, leading to a permanent storage of wrong data.
- **SEGRs:** as integration increases, electric fields induced by ionizations can be very high and, for this, brake the dielectric layers of the devices.

In Tab. 2.1 a summary of the most important SEEs has been depicted.

2.3.1 Physical Mechanism

Radiation induced errors had already been object of study in the "far" 1962, outside the space application field, as they were considered a possible consequence of the deep miniaturization and integration trend for terrestrial electronics, [2.20]. Proves linking radiations to errors arose in late 1970s, as integration, circuit memories' size and space missions significantly increased.

The growing experience with space activities showed the importance of the different ionization sources, bringing the attention on the proton and neutron ion-

Event			Description	Target
Soft Errors	SET	Single Event Transient	temporary variation of a node voltage or, eventually, of a bit	analog and digital circuits
	SEU	Single Event Upset	single erroneous bit change in a memory device	latches, FFs, registers, memories
	MBU	Multiple Bit Upset	multiple erroneous bit flips	latches, FFs, registers, memories
	SEFI	Single Event Functional Interrupt	corruption of the data path in state machines	Flash memories, µ/ Processors, FPGAs
Hard Errors	SHE	Single Event Hard Error	irreversible erroneous bit flip	Non-Volatile Memories
	SEL	Single Event Latch-up	self-sustaining disruptive current flow	CMOS, BiCMOS technologies
	SEGR	Single Event Gate Rupture	gate ruptures	Power devices, deep VLSI, Non-Volatile Memories

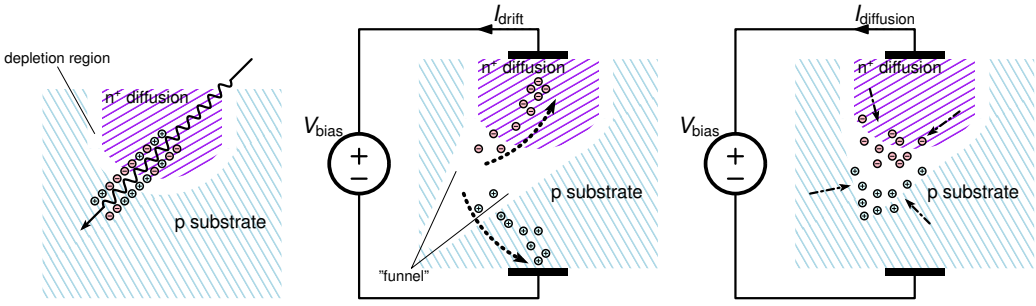
Table 2.1: Summary of the most common soft and hard errors induced by SEEs.

ization effects, initially neglected with respect to heavy cosmic rays ions. Since then, the instantaneous effects of radiation have been accurately studied and a physical model has been presented, [2.21].

When a high energy particle collides with a semiconductor device, there is a ionization mechanism. According to its LET, as the particle moves inside the semiconductor, releases energy creating HEPs, causing, hence, a *direct ionization*. If the ionization products, on turn, contribute to other HEP creations, we have an *indirect ionization*.

The availability of a great number of free charge carriers becomes a problem in CMOS circuits, because of the presence of reverse biased p-n junction, where *charge collection* mechanisms arise. Electrically, the final effect of this resulting charge movement is a current pulse characterized by two transport mechanisms, the electric *drift* and the *diffusion*.

Drift Current In p-n junction depletion regions the electric fields are very high, so, as soon as charges are made available by ionization, they are drifted



(a) Ionization **(b)** Drift **(c)** Diffusion

Figure 2.14: Charge collection mechanism in a single event. The radiation particle ionizes the substrate (a) generating free charge carriers that are drifted by the applied electric (b) and then neutralized by diffusion (c).

away from the electric field increasing the depletion. Here, electric field increases and carriers drift away in turn. As a result, the depleted volume increases at the junction proximity, arising to a *funnel* structure. The effect of the drift is a fast current increase that saturates with the exhaustion of the ionized charges.

Diffusion Current The intrinsic carriers inside the semiconductor, then, tend to restore the equilibrium filling the depleted funnel, arising a diffusion current that slowly decreases.

2.3.2 Electrical Model

A first order model, studied by [2.22], represents this current pulse as a sum of two exponential terms:

$$i(t) = I_0 \left(e^{-\frac{t}{\tau_{\text{coll}}}} - e^{-\frac{t}{\tau_{\text{tran}}}} \right) \tag{2.5}$$

where I_0 is the maximum current, τ_{tran} is the transit time of the drifting ions and τ_{coll} is the collection time of the junction.

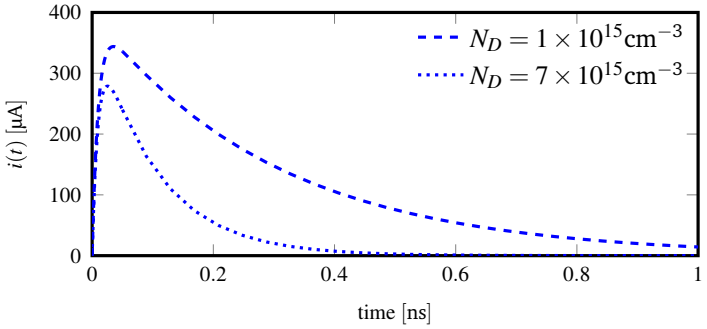


Figure 2.15: Transient response for a 5 MeV α-particle with different doping concentrations, [2.22].

The ionization time constant τ_{tran} is very small, in the order of tenth of picoseconds. This ionization creates in a really small time a very large amount of HEPs, some orders of magnitude larger than the bulk doping concentration, meaning that the resulting charge transport process is ambipolar (and not unipolar as in a doped semiconductor).

The collection process has a time constant of τ_{coll} much higher value, in the order of nanoseconds. Its expression, analytically estimated in [2.22], is:

$$\tau_{\text{coll}} = \frac{\varepsilon_{\text{Si}}}{q\bar{\mu}N_D} \tag{2.6}$$

where $\bar{\mu} = \frac{\mu_n(E)+\mu_p(E)}{2}$ is the average mobility of electrons and holes for high electric fields and N_D is the doping concentration.

From the 2.5 the total injected charge can be estimated as:

$$Q_{\text{tot}} = I_0\left(\tau_{\text{coll}} - \tau_{\text{tran}}\right) \tag{2.7}$$

A very important parameter expressing the robustness of a circuit against radiation-induced signal degradations is the *critical charge*, Q_{crit}, usually defined as the minimum amount of radiation-induced charge, collected in a node, necessary to deteriorate a stored data [2.23] or to induce a SEE.

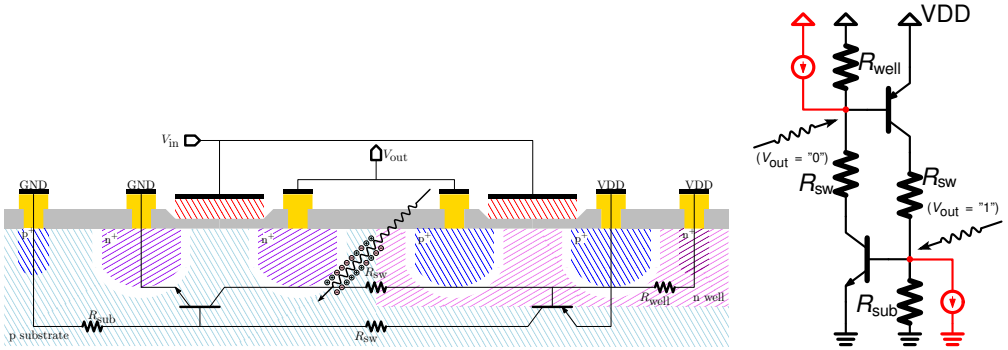


Figure 2.16: Scheme of a CMOS inverter implementation representing a scheme of the parasitic BJTs

2.3.3 Hard Errors

2.3.3.1 Single Event Latch-ups

Latch-up is a common problem of CMOS circuits, typically related to the CMOS inverter structure, intrinsically due to the proximity of different types of doped diffusion areas. As depicted in Fig. 2.16(a), in the semiconductor there are contiguous n-doped and p-doped areas, representing the terminals of two parasitic BJTs. In particular, the p-substrate and the n-well represent respectively the bases of a npn and pnp transistor, while the n^+ and p^+ contact diffusion represent their respective emitters and collectors. Because of the bulk biasing, the p-substrate and the n-well are connected respectively to ground and supply voltage.

As better schematized in Fig. 2.16(b), the two BJTs are cross-connected in positive feedback. In this configuration, as soon as one of them turns on, a self-increasing current loop will build up leading to an unavoidable rupture of the junction due to the unsustainable current density.

In case of ionizing radiations, the triggering event is represented by the current due to the charge injection. In particular, the charge is collected in correspondence

of the reversed biased junction, at the output node, either in the substrate, when the output voltage is high, or in the well, when the output voltage is low. As substrate and well are lightly doped, they have a consistent resistivity. For this reason, the eventual ion-induced currents are easy to generate a voltage drop across R_{sub} or R_{well} sufficiently high to overcome the threshold voltage V_γ of the BJTs' junctions and turn on the relative transistor.

2.3.3.2 Single Event Gate Ruptures

With the size shrinking carried out by technological progress, electrical field intensities have to be accurately controlled. In particular, in new technology nodes, in order to preserve the integrity of the thin gate oxides, very low voltages values are mandatory. Unfortunately, ionization can locally arise to high electric fields, seriously harmful for the thin gate oxides.

As described, ionization induces the creation of many HEPs and the presence of an electric field on the structure (for instance due to the supply voltage) inhibits their recombination. In turn, the funneling effect may locally increase the electric field intensity, exceeding the dielectric breakdown field strength of the thin gate oxide. As a result, the device can be permanently damaged. In Fig. 2.17 the electric field composition after a ionization funneling has been depicted.

The gate rupture is more likely for high power devices, where electric fields are usually high. However, even Non-Volatile memories can be affected, as in write or erase operations high electric fields are applied.

2.4 Basic Physical Definitions

The following are fundamental definitions useful to quantify the entity of the radiation-induced effects.

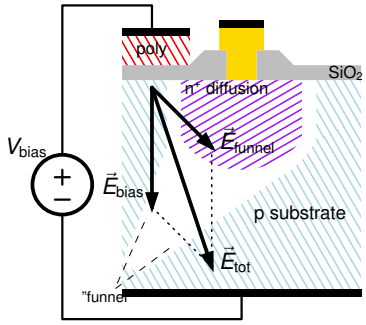


Figure 2.17: Scheme of a SEGR generation. The electric field across the funnel depletion volume E_{funnel} is added to the bias electric field E_{bias}, resulting in a higher electric E_{tot} across the gate oxide.

Radiation Flux: is the amount of radiation hitting the surface unit in a time unit. It can be measured in W cm^{-2} for a generic radiation or, for a given particle, in $\text{s}^{-1}\text{cm}^{-1}$.

Radiation Fluence: is the amount of radiation hitting the a certain surface. It can be measured in J cm^{-2} or, in analogy to the flux, in cm^{-2}.

Sensitive Volume (SV): is the volume involved in the charge collection during the ionization.

LET Threshold (LET_{th}): is the minimum LET necessary to induce a particular SEE. In particular:

- $LET_{th,\textbf{SEU}}$**:** is the minimum LET necessary to have a SEU;
- $LET_{th,\textbf{SEL}}$**:** is the minimum LET necessary to have a SEL;

Critical Charge (Q_{crit}): is the minimum amount of injected charge in correspondence of a SEE.

Cross Section (σ): measured in cm^2, represents the probability to have a SEE and it is related to the effective area of a target subject to a hitting particle.

In particular one can define:

Cross Section per bit (σ_{bit}): is the probability of a ionization event, normalized to the number of bits. This definition is convenient for devices having large arrays, such as memories.

Saturation Cross Section (σ_{sat}): is the (maximum) saturation value of the cross section for increasing LET values. Over a certain energy, in fact, and, consequently, over a certain penetration depth, the error probability remains constant.

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Chapter 3

Radiation Effects in Memory Devices

MEMORIES are complex integrated circuits made up many and different digital and analog blocks. They are large arrays of cells based on peculiar storage strategies, surrounded by a digital periphery needed to access the data. Then information stored is sensed through comparing circuits and routed through I/Os. A control logic, or even a micro-controller unit, is generally necessary to manage the timing phases for the operation flow.

volatile memories (VMs) are devices in which the stored information is kept as long as the circuits are supplied, while NVMs keep information for decades even without any provided supply.

The simplest memory element is the capacitor that stores information through a charge retention. Dynamic RAMs (DRAMs) are capacitor-based VMs, used for very large storage volumes and fast access times.

To follow, the latch is the fundamental digital memory device, which constitutes the basic element of more complex structures such as flip-flops and registers. In latches, information is stored thanks to the bistable bias condition that estab-

lishes between two cross-coupled inverter in positive feed-back. Static RAMs (SRAMs) are VMs based on latch elements, and are used for smaller storage volumes and high speed operations.

Cumulative and transient radiation effects so far discussed are always coexisting and interacting during normal device operation. However, because of their heterogeneous nature, memory devices manifest different sensitivity to the radiation effects.

3.1 Radiation Effects in Volatile Memories

Historically, first evidences of ionizing radiations in the outer space were noticed from SEUs in DRAMs. Then, a great part of single event have been found to cause soft errors VMs and in all memory circuits whose storage strategy relies on the charge retention.

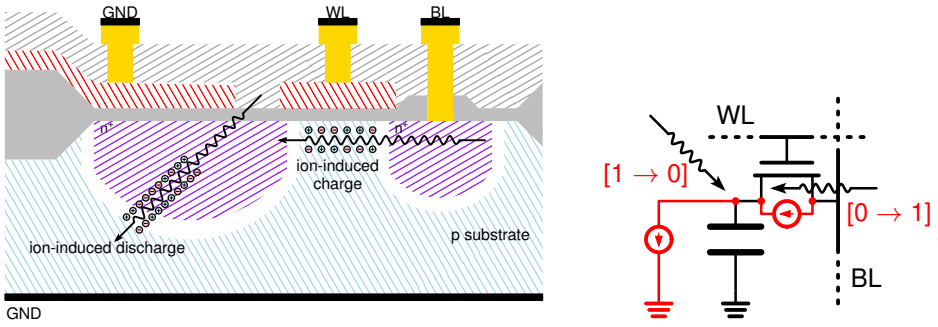
In fact, the physical phenomena of the ionization so far described can be seen as a charge injection resulting in a current pulse flowing through the hit junction node.

3.1.1 SEUs in DRAMs

As said, data in DRAMs are stored by mean of the charge collected inside the cell capacitor. As in this topology no positive feedback is present, if a single event hits the capacitor or the access transistor, the cell charge can change, resulting in a bit flip.

In the most of the cases, if the particle hits the storage node, a ion-induced current will neutralize the charge stored in the cell, resulting in a $1 \rightarrow 0$ flip. On the other hand, for sub-micron devices, further studies [3.1] have showed how, for grazing incident particles crossing both drain and source, a spurious “on” state in

access transistors can be determined, forcing a $0 \rightarrow 1$ transition. In Fig. 3.1 the DRAM SEU has been shown.



(a) Charge collection mechanism **(b)** Electric behavior

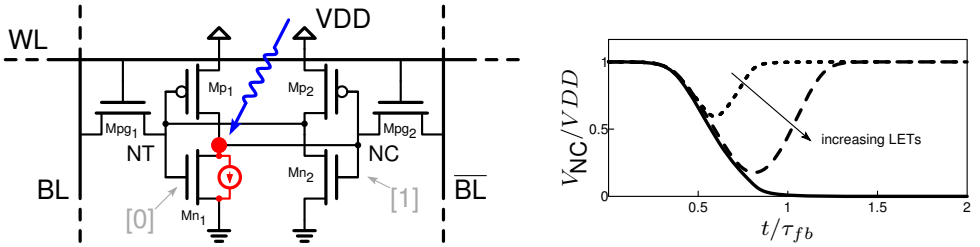
Figure 3.1: SEUs in a DRAM cell.

Beside these soft errors directly related to the cell charge, there is a failure behavior related to the injection of ion-induced charge from a floating bit-line during the sense operation. While cell upsets are frequency independent, bit-line error rates increase with higher clock frequency, [3.2].

3.1.2 SEUs in SRAMs

SRAMs cells are based on the simple structure of two cross-coupled inverters. The positive feedback that ensures the bi-stability of the cell determines also a drastically different behavior for soft errors. The bit flip is not induced by a charge leak from the memory node, as it happens in DRAMs, but it derives from a voltage spike acting as a spurious write of the cell. The sensitive nodes of the cell are the reversed biased junctions that can collect charge from an ion collision.

As an example, let's consider the SRAM cell in Fig. 3.2; supposing that a "0" is stored, the n^+ diffusion at the drain of the nMOS transistor M_{n1} is reverse biased ($V_{NT} = 0$, $V_{NC} = VDD$. If an ion strikes the junction, a certain current will be drained from the pMOS M_{p1}, inducing a voltage drop across its drain and



(a) SRAM cell schematic

(b) Voltage drop across the pull-up pMOS

Figure 3.2: SEU mechanism in a SRAM cell.

source, due to the finite pMOS on-resistance.

However, in order to establish a bit error, the voltage disturbance must last a time sufficiently long to sustain the feedback inside the cell. The collected charge, in fact, tend to be neutralized in a certain time, defined as *recovery time* τ_r. If the recovery time of the system is lower than the feedback time τ_{fb}, then no soft error will occur, while, with longer recovery times, the feedback loop closes, writing a wrong value.

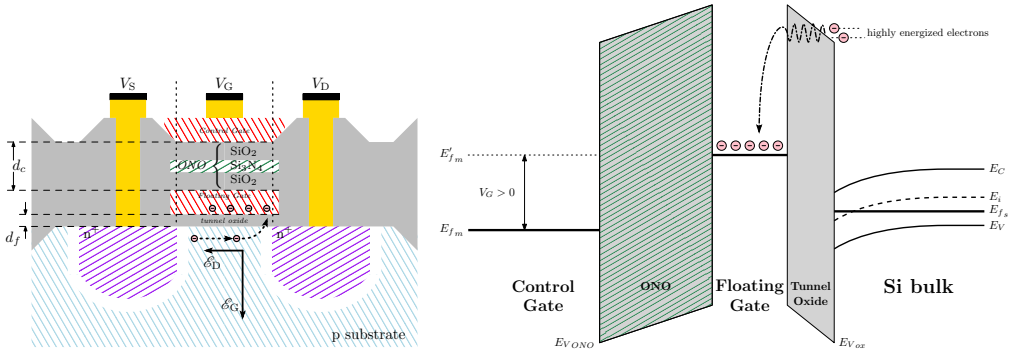
In case of soft error, the ion-induced collected charge equals the critical charge, meaning that the ionizing particle had sufficient penetration energy, represented by the threshold LET, LET_{th}.

3.2 Radiation Effects in Non-Volatile Memories

Flash memories represent the most significant part of non-volatile memories present in the almost totality of the nowadays' electronic applications. They appeared in the scenario in the 80s thanks to Toshiba industries and their success has rapidly grown, thanks to the always increasing progresses of integration technology.

3.2.1 Flash Memories Overview

Flash technology is based on the so called *FG device*, a nMOS with two separated gates, one accessible, defined as control gate (CG), and one fully embedded in the SiO_2 insulator and hence isolated. The insulator layer between the CG and the FG is generally manufactured by a stack of Oxide Nitride Oxide (ONO), tiling between two oxide layer a thin film of Si_3N_4.



(a) FG nMOS **(b)** Band diagram scheme in a FG device

Figure 3.3: FG device. Structure and band diagrams.

Their storage mechanism is based on the charge trapping phenomenon. If a high drain-source voltage is applied, some highly energized electrons, deflected by the CG potential, can eventually overcome the potential barrier of the thin oxide layer, pass inside the FG and there be trapped. The threshold voltage that arise to the n-channel is:

$$V_{th} = V_{FB} + 2\left|\Phi_p\right| + \frac{Q_d}{\varepsilon_{ox}}(d_f + d_c) - \frac{Q_{fg}}{\varepsilon_{ox}}d_c \tag{3.1}$$

where d_c and d_f are the control and FG oxide layer thickness, respectively, Q_d is the depletion charge, Q_{fg} is the negative charge stored in the FG, V_{FB} is the flat-band potential and Φ_p is the potential in the bulk silicon.

In a Single Level Cell (SLC), only two logic digital values are considered. The *program* operation, associated conventionally to a logic "0", consists in injecting electrons in the FG and increasing the threshold voltage. Complementary, the *erase* operation that writes a logic "1" defines the electron discharge that decrease the threshold voltage.

A FG cell behaves like a MOS transistor: if the voltage applied to the CG is higher than the threshold (with or without any charge stored in the FG), the cell is in conductive state. Otherwise, the cell is off. Two logic states are associated to two different threshold values:

- the first, lower, relative to the FG without any charge stored,
- the second, higher, relative to negative charge stored inside the FG.

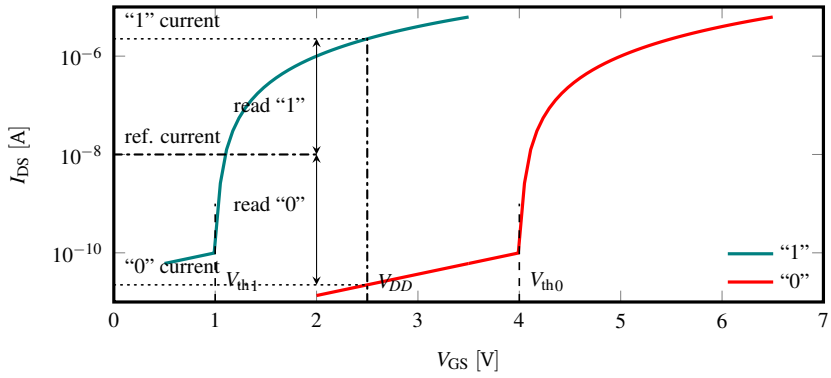


Figure 3.4: Currents in a FG device and reading principle. When a FG cell is selected, the relative current is compared with a reference and the digital value discriminated.

As illustrated in Fig. 3.4, if an intermediate voltage is applied to the CG, a current will flow through the FG according to the stored charge and comparing it with a reference value, the logic state can be read out.

During programming, a dedicated algorithm is used to set the threshold voltage of the FG cells to well defined values for program and erase, corresponding

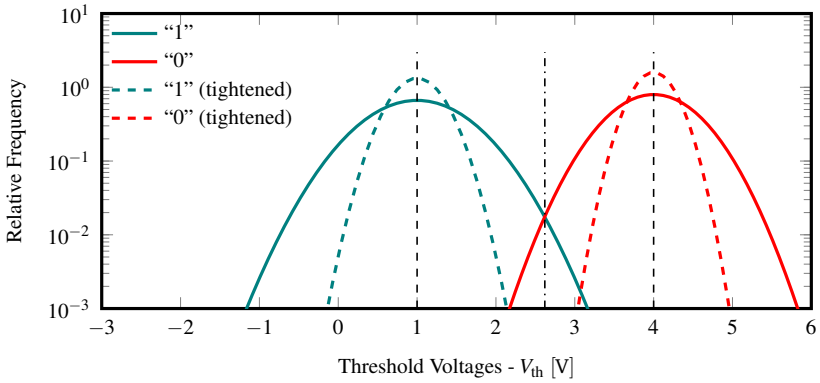


Figure 3.5: Threshold voltage distributions in a flash device.

to the two logic states of the cell. Unfortunately the algorithm cannot precisely place all the memory cells' thresholds at the desired target voltage. Instead, they are normally distributed around two average values, with a standard deviation that has to be minimized in order to reduce the overlap between the two distributions (i.e. minimize the error associated with a wrong value discrimination). An example is shown in Fig. 3.5.

For this reason *tightening* algorithms are used in writing operation, such as the write and verify (WaV) procedures. WaV algorithms consist in applying successive writing pulses to the cells and checking their state after each write attempt. When the target state is reached, the write procedure is considered successful and no more pulses are applied. Otherwise, if no writing is achieved after a fixed number of attempts, the writing operation is considered null and the relative cell is marked as defective.

3.2.2 Cumulative Effects in Flash Memories

When FG devices are exposed to radiations, cumulative and single events effects induce shifts of the V_{th} distributions. Errors occur because of these shifts that disturb the reading operation.

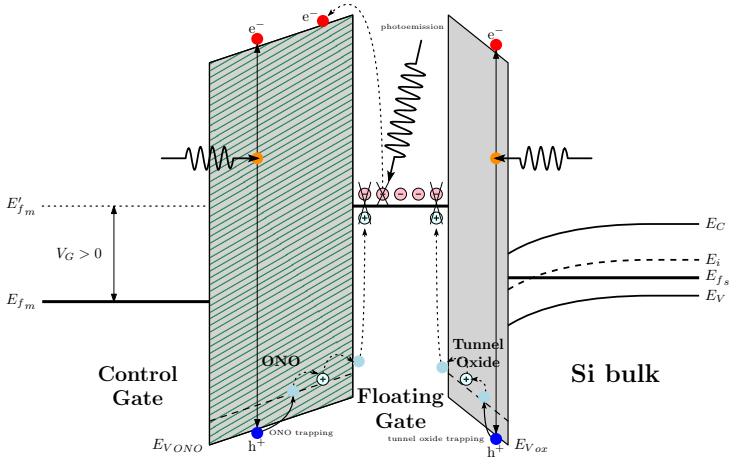


Figure 3.6: Scheme of the radiation-induced effects in a FG cell.

FG memories, despite their high penetration in the customer market and their proven reliability gained thanks to years of technological maturity, are quite susceptible to cumulative effects. Their full functionality, in fact, can not be granted for doses larger than 100 krad, [3.3, 4].

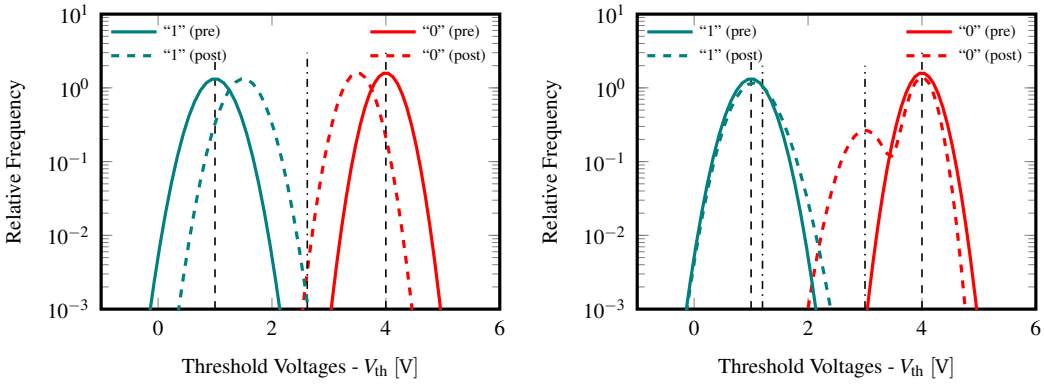
The main contributions to the TID-induced threshold voltage shifts are due to:

ONO Charge Trapping: the radiation-induced ionization creates HEPs; holes are then drifted by the electric field and trapped inside the FG.

Tunnel Oxide Charge Trapping: same as the previous, but the amount of the generated carriers is much lower because of the thinner oxide layer.

Photoemission: radiations can interact directly with the electrons trapped inside the FG, transferring to them a sufficient energy to escape from the potential well.

All of these mechanisms, depicted in Fig. 3.6 induce a negative voltage shift. In the first two cases holes neutralize stored electrons, while, in the third, electrons are forced out of the FG. A typical TID situation is shown in Fig. 3.7(a).



(a) Cumulative effects

(b) Single event effects

Figure 3.7: Radiation-induced threshold voltage shifts.

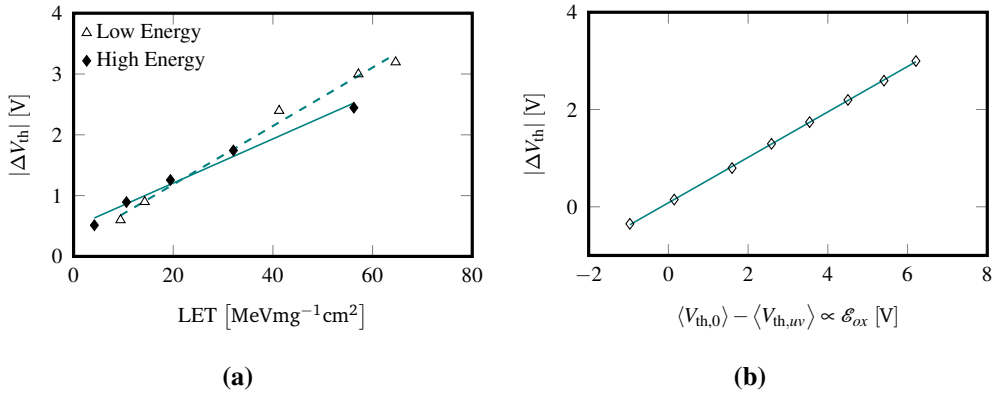
Flash memories sensitivity to TID effects is so high that FG cells are used as radiation dosimeters.

3.2.3 Single Event Effects in Flash Memories

Beside TID effects, when ions strike a FG device, their high energy amount can perturb the charge stored inside the FG, determining instantaneous bit flips. The physical mechanisms involved are the ones just listed above, but their effects will damage only the stroke cells, whose number will depend on the irradiation fluence, [3.5]. The statistical analysis of the SEUs in flash devices exhibits threshold distributions with two peaks. A composition of two categories of cells can be hypothesized, i.e. the undamaged cells and the affected ones. Fig. 3.7(b) shows the threshold voltage distributions in presence of SEEs. The distance between the two peaks, corresponding to the SEE-induced voltage shift, depends on many factors and their physical causes involved are still object of investigation.

3.2.3.1 Physical Mechanisms

First, it has been noticed that single events can induce threshold voltage shifts (and consequently SEUs) whose amount linearly depends on the LET of the incident ions, [3.6]. This phenomenon is illustrated in Fig. 3.8(a). A possible explanation of this linear dependency can be found in the fact that the mechanisms leading to the FG charge neutralization happen quite suddenly after the radiation-induced ionization, before any initial recombination.



(a) **(b)**

Figure 3.8: Threshold voltage dependence on LET incident energy (a) and electric field (b).

Fig. 3.8a also illustrates that for a given LET the single event damages depend on the energy of the incident ions. In fact, for smaller incident energies (smaller length tracks), higher leakage path in oxides are generated, arising to a more efficient availability of free charges, [3.7]. Then, in Fig. 3.8(b) is shown a linear dependence of the threshold voltage shift with the difference between the average threshold voltage before irradiation, $\langle V_{\mathrm{th},0}\rangle$, and the average "neutral" threshold voltage, $\langle V_{\mathrm{th},uv}\rangle$, quantity proportional to the electric field across the tunnel oxide and ONO multilayer, [3.8].

Scaling has clearly proved to be effective in increasing SEE damages from

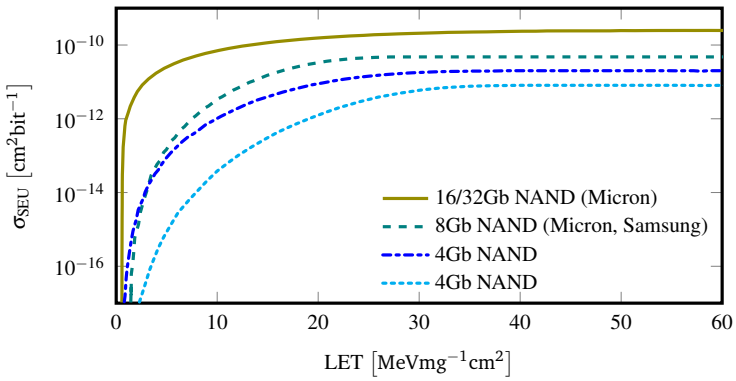


Figure 3.9: SEU dependance on integration node]

heavy ions. This was intuitively predictable, as smaller sizes correspond to smaller amount of charge stored in the FG and, thus, easier to be neutralized by radiation-induced single events. In other words, the same amount of charge in proximity of the FG determines a higher shift in the threshold voltage. In Fig. 3.9 the cross sections behavior of different technological nodes have been shown. As size features decrease, SEUs accordingly increase.

The missing element in the understanding of the SEU generation needs a focus on the reasons behind the FG charge neutralization. As discussed in the 3.2.2 for the cumulative effects, the threshold voltage shift can be either due to the oxide holes trapping or to the electrons leakage through the tunnel oxide. Even if earlier models attributed single event errors to the positive charge trapping, latest evidences deriving from experiments on device annealing, prove that the dominating aspect is the electron loss of the FG. In fact, as annealing has proved to restore the trapping damages, no effect in Flashes' SEUs is obtained by annealing after radiation exposure.

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Chapter 4

Memristors and Resistive Memories

4.1 Introduction

4.1.1 A Brief History

LEON Chua in 1971, in an article, that from then on would have become very famous, [4.1], theorized the existence of a new passive two-terminal circuital element, having as characteristic function the following:

$$M(\varphi, q) = 0 \tag{4.1}$$

where the "memristance" M is a function of the charge q and the *flux-linkage*, φ, defined as:

$$\varphi(t) = \int_{-\infty}^{t} v(\tau) d\tau \tag{4.2}$$

The existence of this novel element, named *memristor* (a syncretism between the words *memory* and *resistor*), was hypothesized on the base of the symmetry of the Maxwell's equations. In Fig. 4.1 a summary for the equations for condensed parameters is represented.

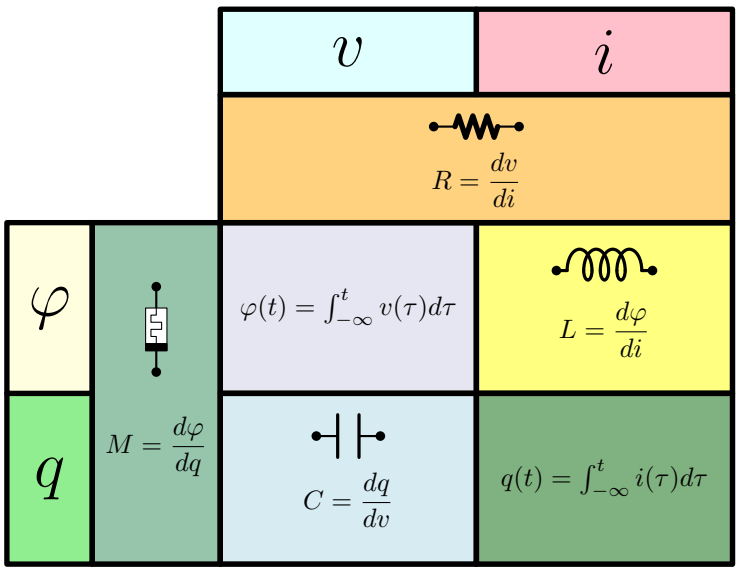


Figure 4.1: Scheme of the Maxwell's equations for condensed parameters.

Chua demonstrated in his paper that an element respecting the relation $f(\varphi, q) = 0$ could be implemented, but, at that time, no physical passive element with such a characteristic had been discovered yet.

A first physical memristor evidence was finally proved in 2008 by Hewlett Packard Labs, with the discovery of the non-volatile behavior of the TiO_2 films, [4.2]. In their work, Strukov and al. considered some already known electrical properties of thin-film materials (the apparent negative resistance, hysteresis and multiple resistive states, [4.3,4]) and formulated a simple physical model, associating these phenomena to the resistance switch of Titanium-Oxide thin-film materials.

After all, in these years, a big interest in the electrical switching of materials has arisen. The big family of the "emerging technologies" is considered an excellent opportunity to overcome the integration limits that the traditional CMOS technology begins to show, especially for memories.

A first attractive aspect of the thin-film-based solutions is the easy and imme-

diate integrability with the traditional CMOS processes. In fact, all these technologies are based on the deposition of different materials during the back-end phase, i.e. during the metal deposition steps, making really cost-effective the implementation of the necessary masks. Moreover, in the most of the cases, the switching devices are developed in height according to the minimum size features of the relative technological node, resulting in a big advantage in terms of size and density.

Resistive-switching-based devices are also interesting because of their higher power efficiency. For example, Flash memories waste a lot of power to increase the energy of the electrons to be used in the state switch (hot electron mechanisms). On the other hand, in memristive devices, almost the whole energy amount is used to induce the resistance switch,

4.1.2 Resistive Switching Memories

The memristor offers a new paradigm to memory designers to implement the memory devices. The logical state is no longer associated to the amount of charge stored in a capacitive node (the latch/SRAM's positive feedback, the DRAM's capacitor, the trapped charge in the Flash floating-gate), but bond to a physical state, i.e., the resistivity of a material.

Many materials have proven, so far, various resistance switching properties, each belonging to a different physical mechanism. Even if in this cluttered scenario a systematic classification of the resistance-switch-based devices is difficult, three main physical mechanisms can be identified.

Magnetic RAMs (MRAMs) are based on the giant magneto-resistance (GMR) effect, discovered by Grünberg's and Fert's groups, [4.5], according to which, the global resistance of a stack of different layers depends on the magnetic spin orientation of each layer. When the spin orientations are anti-parallel, the stack

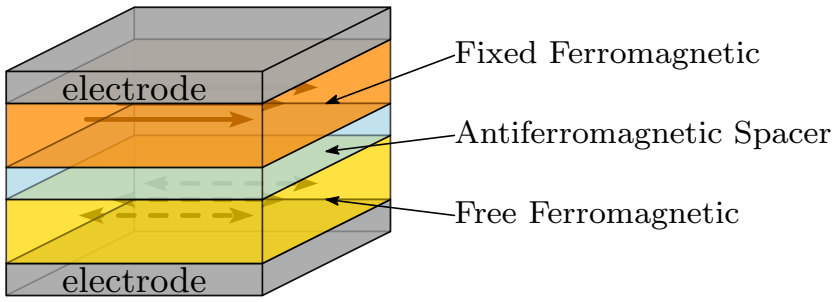


Figure 4.2: Scheme of a magnetoresistive device element.

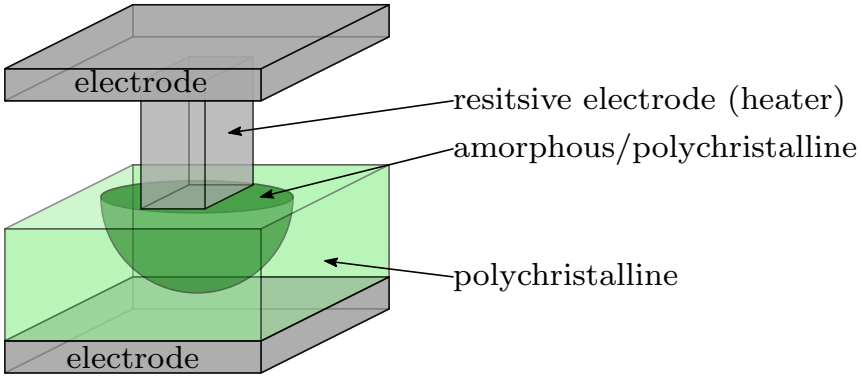


Figure 4.3: Scheme of a phase-change device element.

offers a high resistance; on the other hand, when the layers have the same spin orientation, the resistance decreases. Two resistance levels are, thus, obtainable, a parallel low resistive state and an anti-parallel high resistive state.

The basic structure of a MRAM element, represented in Fig. 4.2, is a stack of alternate ferromagnetic and antiferromagnetic spacer layers. One (or more) ferromagnetic layer has a fixed polarity, while the other (or others) need to have a free polarity that can be changed by the control circuitry.

According to the technique used to change the spin, i.e. the resistivity, a further classification can be reported: spin transfer torqe MRAMs (STT-MRAMs), thermal assisted switching MRAMs (TAS-MRAMs), vertical transport MRAMs (VMRAMs).

	Physical Mechanism	Switching Technique	Typical Materials
Resistive Switching Memories	Magnetoelectric	STT-MRAM	Fe/Cr, CoFeB/MgO
		TAS-MRAM	IrMnCr/AlO_x
		VMRAM	CoFe/Cu/NiFe
	Thermoassisted	PCM	GeSbTe (GST)
	Electrochemical	OxRAM	TiO_2, HfO_2
		Electro-metallization	NiO, CuO

Table 4.1

Another important group of resistive memories is based on thermal effects, whose most important category is represented by the phase change memories (PCMs). These devices are based on materials whose resistivity depends on the lattice structure. In particular, the amorphous state offers a higher resistivity with respect to the crystalline phase. The two phases are obtained by mean of different cooling profiles after a current-induced heating: a slower temperature decrease promotes a crystalline annealing, while a faster one induces an amorphous structure. In Fig. 4.3 an example of PCM device is shown. The active material of the element is generally a calcogenide compound.

The widest group of resistive memories, generally referred to as resistive RAMs (RRAMs or ReRAMs) or oxide resistive RAMs (OxRRAMs), is based on electrochemical and red-ox reactions involving ion migrations (cations or anions). For n-type transition metal oxide compounds, such as TiO_2 and HfO_2 among the most used, an anion migration of oxygen vacancies is observed (Red-Ox RAMs), while for p-type compounds, such as NiO, cations migrate (Electrometallization RAMs).

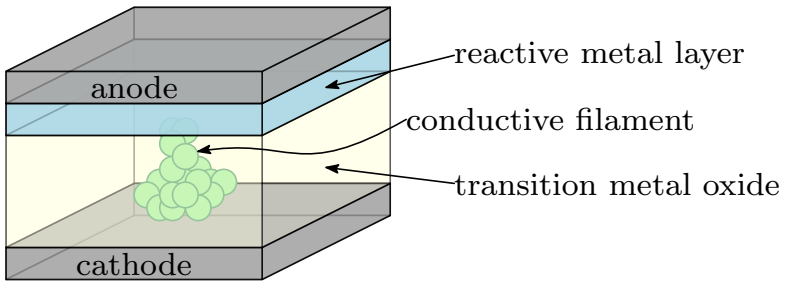


Figure 4.4: Scheme of the MIM stack of the resistive device.

4.2 Oxide Resistive RAMs

RRAMs, also referred to as Oxide RAMs, are MIM structures manufactured with a stack of a transition metal oxide layer sandwiched into two metal electrodes. Typically used oxides are TiO_2 or, more recently, HfO_2, while Platinum and Titanium are the most employed metals due to their chemical compatibility with the red-ox process involved. A sketch of the device stack is illustrated in Fig. 4.4.

In this kind of memories, the main physical mechanism leading to the resistance change is related to the formation and transport of oxygen vacancies inside the oxide: while the above mentioned oxides show an intrinsic insulator behavior, the defects introduced by oxygen vacancies create a conductive path in the compound.

At room temperature, the oxygen vacancies defects' number and the mobility are too small to possibly allow any charge transport. However, under the action of an electric field, oxygen atoms migrate inside the stack (ionic migration) drifting toward the anode, creating the vacancy defects. At this point, it is necessary to accumulate these oxygen ions so that the new crystalline structure modified by the defects has room and time to build up. For this reason, at the anode, a Ti layer between the HfO_2 and TiN is commonly used (Fig. 4.4), as titanium oxidation can accommodate oxygen ions without inhibiting the further vacancies motion.

4.2.1 Electroforming, Set and Reset

Oxygen vacancies are originally dislocated homogeneously into the device. This situation is quite inconvenient for the formation of adequate conductive paths. A first step, commonly defined as *electroforming* (or simply *forming*), is necessary to create the first CF and is quite critical, as it influences the dislocation of the vacancies defects inside the oxide. Many studies as [4.6] have been performed in order to understand how the voltage waveform applied in the forming steps can influence the CF evolution and the successive reliability.

After the constitution of the first CF, the successive conductive material buildups occur faster as the structure of the compound has been affected by the new location of the vacancies. The filament reconstitution is defined as *set* phase.

In bipolar resistive switching (BRS), when a reverse voltage is applied to the stack, it is possible to have the rupture of the CF. In the so called *reset* process, a reverse electric field moves the oxygen ions back to the filament where they oxidize back the conductive Hf in HfO_2 and disrupt the conductive path. However, the conductive behavior of the filament decreases the electric field intensity and, for such a reason, the reset process is slower.

4.2.2 Phases of the Conductive Filament Growth

As soon as a direct electric field is applied, oxygen ions are induced to migrate toward the anode with the vacancies moving toward the cathode. At the cathode interface, in some localized points where interface defects lower the Schottky barrier, electrons flow into the oxide facilitating in that region the red-ox, [4.7]. An initial cluster of vacancies starts to grow with a quasi-isotropic initial expansion, as depicted in Fig. 4.5(a).

With the growth of the first vacancies, the electric field concentrates around

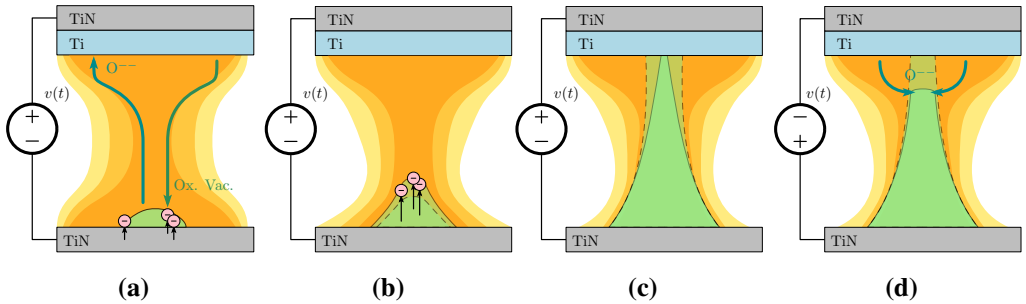


Figure 4.5: Evolution of the CF. The oxygen dislocation follows the intensity of the electric field (as schematized in the pictures). In some areas, the injection of electrons establishes an early CF (a). As it grows, the electric field localizes where there is a higher current density, promoting the filament growth along one direction (b), until reaching the anode (c). The electric field intensity curvature has been intentionally emphasized. When a reverse bias is applied, the CF is worn out and decreases (d).

the early-formed CF and the current density in that point increases, localizing in that region the red-ox reaction and forming a conductive wire as the process goes on – Fig. 4.5(b).

The filament grows along the device length until reaching the anode – Fig. 4.5(c). At this point, the red-ox reactions keep on going, widening the filament size and, consequently, decreasing its resistance value. The longer a direct voltage is applied, the lower is the final filament resistance value obtained, so that different Low Resistive States (LRSs) can be achieved.

In Fig. 4.5(d), the *reset* process is shown. Reciprocally to the *set* process, when an inverse electric field is applied, oxygen ions start to oxide the CF that wears thinner and thinner until reaching a rupture. After the first rupture the filament will be consumed along vertical direction, until reaching the High Resistive State (HRS) resistance.

4.3 The Memristor Model

4.3.1 Existing Memristor Models

When the first concrete memristor device was presented, a simple linear approach for the I-V model was proposed by Strukov, [4.2]. In this Section, a brief overview of that model is discussed.

The basic assumption of the Strukov model considers the oxide layer resistance as a series of two contributions: the first associated to the intrinsic insulator layer, characterized by a high resistivity; the second related to the oxygen-vacancies-doped layer, characterized by a low resistivity. Fig. 4.6 conceptually depicts model.

By defining R_{u} and R_{d} the resistances associated to the intrinsic part and to the doped one, respectively, the overall memristor resistance, R_M, is given by:

$$R_M(w) = R_{\mathrm{d}}(w) + R_{\mathrm{u}}(w) \tag{4.3}$$

where w is the thickness of the doped layer.

It is assumed that R_{off} is the value of the resistance associated to the pristine material ($w = 0$) and, reciprocally, R_{on} is the resistance of the device fully formed ($w = D$, where D is the thickness of the oxide layer).

The memristance, R_M, can be rewritten as:

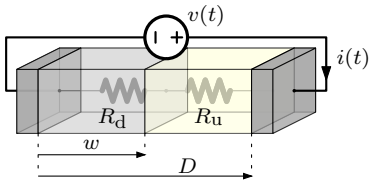


Figure 4.6: Representation of the model proposed by Strukov, [4.2]. The global resistance is the series of the doped and undoped layers' resistances.

$$R_M(w) = R_{\text{on}}\frac{w}{D} + R_{\text{off}}\frac{D-w}{D} = R_{\text{off}} - \frac{\Delta R}{D}w \tag{4.4}$$

where $\Delta R = R_{\text{off}} - R_{\text{on}}$.

In order to determine the voltage-time behavior of the device, the following fundamental relations describing the memristive device behavior have to be considered.

$$\begin{cases} v(t) = R_M(w,t)i(t) & \text{(4.5.a)} \\ \dot{w}(t) = f(w,i) & \text{(4.5.b)} \end{cases}$$

In (4.5), the length w is the state variable of the dynamic system representing the memristor, v and i are the voltage across the memristor and the current flowing through it, respectively, while $f(w,i)$ is a function describing the kinetic of the red-ox reaction leading to the filament growth.

4.3.1.1 The Linear Model

The basic assumption of the linear model is to consider the doped layer growth as directly proportional to the current flowing through the device. The $f(w,i)$ becomes, hence, a proportionality relation:

$$\dot{w}(t) = K_I i(t) \tag{4.6}$$

Such hypothesis basically states that the speed of the red-ox that generates the oxide vacancies is proportional to the carriers fed by the current flow. With this hypothesis, the system to be solved is the following:

$$\begin{cases} R_M(w,t) = R_{\text{off}} - \dfrac{\Delta R}{D} w(t) & \text{(4.7.a)} \\ v(t) = R_M(w,t) i(t) & \text{(4.7.b)} \\ \dot{w}(t) = K_I i(t) & \text{(4.7.c)} \end{cases}$$

where the constant K_I merges physical and technological aspects, such as the oxygen-vacancies mobility and the oxide resistivity.

A solution for (4.7), assuming $R_0 = R_M(0)$, is given by:

$$R_M(t) = \sqrt{R_0^2 - 2K_I \frac{\Delta R}{D} \Delta\varphi(t)} \tag{4.8}$$

with the flux-linkage $\Delta\varphi(t) = \int_0^t v(\tau) d\tau$, [4.8].

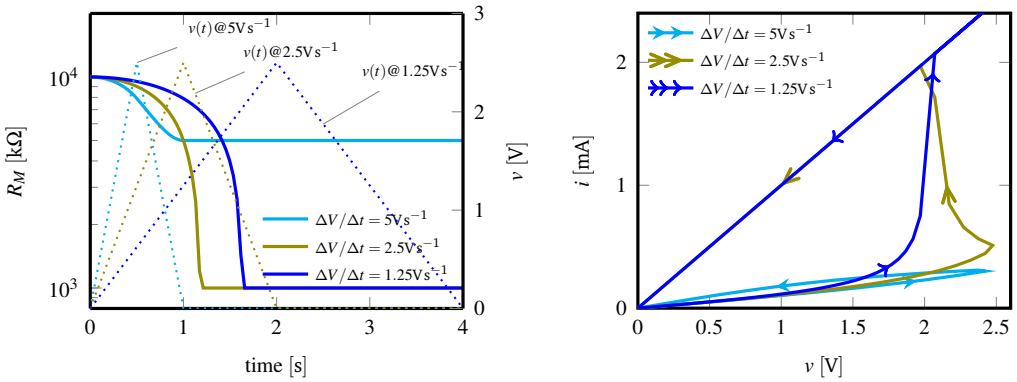
A further consideration, as it can be derived from (4.7.a) and (4.7.c), is that the resistance change for the linear model depends on the charge Q gathered (dispersed) during the *set* (*reset*) process:

$$R_M(Q) = R_0 + R(Q) = R_0 - K_q Q \tag{4.9}$$

where $K_q = -K_I \Delta R/D$ takes into account the technological aspects and $R_0 = R_{\text{off}} - w(0)\Delta R/D$.

Some examples of the memristor *set* have been plotted in Fig. 4.7. In particular, Fig. 4.7.(a) shows the time behavior of a memristor device driven with voltage ramp sweeps of different duration and slope, while in Fig. 4.7.(b) the respective I-V characteristics are depicted.

As it can bee seen, the resistance change depends on the area under the voltage curve. For a slope of $\Delta V/\Delta t = 5\,\text{V}\,\text{s}^{-1}$, the resistance change is minimal. For a lower slope (and larger duration), $\Delta V/\Delta t = 2.5\,\text{V}\,\text{s}^{-1}$, the LRS is achieved during the decreasing phase of the voltage sweep and this can be noticed by the jerk



(a) Memristance as a function of the time

(b) Memristor I-V characteristic

Figure 4.7: Examples of resistance-time behaviors (a) and I-V characteristics (b) for a linear memristor with $R_M(0) = R_{\text{off}} = 10\,\text{k}\Omega$, $R_{\text{on}} = 1\,\text{k}\Omega$ and $K_I = 3 \times 10^{16}\text{nm}\,\text{C}^{-1}$. The voltage is applied by mean of ramps with different slopes $\pm\Delta V/\Delta t$. The three situations depicted for decreasing slopes, correspond, respectively, to: incomplete resistance switch, resistance switch in the falling slope and resistance switch in the rising slope.

in the I-V characteristic at around 2.2 V. When $\Delta V/\Delta t = 1.25\,\text{Vs}^{-1}$, the resistance change saturates during the rising slope so that the relative I-V characteristic shows a sudden switch at around 2 V.

4.3.1.2 Non-Linear Models

Beside to the simple linear model, various alternatives have been so far presented, [4.8–11]. The open aspects in the linear model are basically two: the resistive mechanisms in the intrinsic insulator and the non linear kinetic of the impurities.

The non-ohmic behavior of the undoped part of the device can be taken into account. Pickett's analysis, [4.11], considers the series of an ohmic resistor for the doped region in series to an electron potential barrier and develops the Simmons' equations, [4.12], to achieve a solution for $f(w,i)$:

$$\dot{w} = \frac{f_{\text{on/off}} \sinh\left(\dfrac{i}{i_{\text{on/off}}}\right)}{\exp\left[\exp\left(\mp\dfrac{w - a_{\text{on/off}}}{w_c} - \dfrac{|i|}{b}\right) + \dfrac{w}{w_c}\right]} \tag{4.10}$$

with $f_{\text{on/off}}$, $i_{\text{on/off}}$, $a_{\text{on/off}}$, b and w_c fitting parameters to be used, respectively, for *reset* and *set*. Even if [4.11] ensures a good match with measured I-V curves, the achievable time behavior of R_M is not very accurate, as the Pickett's model is affected by serious computational issues and convergence problems depending on the choice of the input signal, [4.13, 14].

A second category of models, [4.8–10, 15], takes into account the non-linear nature of the dopant kinetic. The function $f(w,i)$ is weighted by a *window* function, $g(w)$, of the state variable w:

$$f(w,i) = K_I g(w) i(t) \tag{4.11}$$

4.3.1.3 Piece-Wise Linear Models

Another group of modeling solutions presented in literature gathers the so called piece-wise linear (PWL) models, [4.16–19]. PWL models are based on empirical window functions implemented by mean discretized algorithms. In particular, the time dependance of the memristance is evaluated at discrete times considering the approximated differential increment:

$$R_M(t) \approx R_M(t - \Delta t) + \frac{\Delta R_M}{\Delta t} \tag{4.12}$$

The model proposed in [4.17] introduces a threshold voltage $T_{h/l}$ and two fitting parameters K_{h/l_1} and K_{h/l_2}, having:

$$\frac{\Delta R_M}{\Delta t} = K_{h/l_1} e^{K_{h/l_2}\left[v(t) - T_{h/l}\right]} \tag{4.13}$$

where $v(t)$ is the voltage across the memristor at the time t and the indexes h and l refer to the parameters to be used in *set* or *reset*, respectively.

A more complex solution is proposed in [4.19], where a discrete windowing function $f(R_M,t)$ equal to:

$$f(R_M,t) = \frac{1}{1+e^{\mp\frac{R_M(t)-\Theta_x R_x}{\beta_x (R_{\text{off}}-R_{\text{on}})}}} \tag{4.14}$$

is introduced to evaluate the memristance discrete increment:

$$\frac{\Delta R_M}{\Delta t} = \mp C_x \left[\frac{v(t)-V_t}{V_t}\right]^{P_x} f(R_M,t) \tag{4.15}$$

The parameters C_x, P_x, Θ_x and β_x assume a different value for *set* or *reset* and R_x is respectively R_{off} or R_{on}.

4.3.1.4 Alternative Physical Modeling of the Conductive Filament

As it can be clear, the modeling of the memristor switching behavior of is strictly associated to the description of the CF growth. In [4.2, 8–10, 15–19] the CF stretching is evaluated and this leads to the series modeling of the memristor.

A different approach has been chosen in [4.20,21], where the resistive switching is described by the growth of the CF width due to a thermally activated ion migration. The solution for the CF diameter ϕ becomes:

$$\frac{d\phi}{dt} = Ae^{-\frac{E_{A0}-\alpha qV}{kT_0\left(1+\frac{V^2}{8T_0\rho k_{\text{th}}}\right)}} \tag{4.16}$$

where V is the voltage across the memristor, A is an integration constant, ρ is the electric resistivity, k_{th} is the thermal conductivity, E_{A0} is the ion energy barrier, α is a coefficient related to the barrier lowering, T_0 is the room temperature and k is the Boltzmann constant. According to this modeling, the LRS corresponds to a wide CF, while the the HRS coincides with a narrow one, eventually reduced till its rupture.

4.3.2 Approximated Verilog

-A Model The aim of the mentioned electrical models is to give an analytical description of the physical processes occurring inside the memristive device. From the designer point of view, an efficient model should give an accurate representation of the electrical variables of the device inside the full circuit, with a sufficient accuracy.

Even if in real writing operations the value of the resistive cell is verified by the mentioned incremental step pulses with verify algorithms (ISPVA) methods, simulations need a reliable description of the memristor devices. It is necessary, in fact, to investigate the effectiveness of the architectural solutions, estimate the currents and voltage drops due to parasitics and all the possible secondary effects involved in the interaction of the circuit periphery connected to the cells, in both read and write access.

Moreover, for a designer, the simulation speed is also important, as analog simulations in memories need to consider a huge number of devices. For these reasons, an approximated Verilog-A model has been implemented and used in the simulations. The model is based on the solution given by the linear model. If we reasonably suppose that our observation time is much shorter than the time constants involved in the resistance change process, then we can consider a linearized version of (4.8):

$$\begin{cases} R_M(0) = R_0 & \text{(4.17.a)} \\ \left.\dfrac{dR_M(t)}{dt}\right|_{t=0} = \dfrac{-\tilde{K}_I v(0)}{2\sqrt{R_0^2 - \tilde{K}_I \Delta\varphi(0)}} = -\dfrac{\tilde{K}_I}{2R_0} v(0) & \text{(4.17.b)} \end{cases}$$

where $\tilde{K}_I = 2K_I \dfrac{\Delta R}{D}$.

The approximated solution becomes:

$$R_M(t) \approx R_0 - \frac{\tilde{K}_I}{2R_0} v(0)t \tag{4.18}$$

Simulation engines evaluate at discrete times the state of the electrical variables of the circuit: the result at a certain time t_k is evaluated by mean of the state at the previous discrete time t_{k-1}. The (4.18) can be the rewritten considering the resistance value at the $k-$th integration step:

$$R_M[k] = R_M[k-1] - \frac{\tilde{K}_I}{2R_M[k-1]} v[k]\Delta T_k \tag{4.19}$$

being $\Delta T_k = t_k - t_{k-1}$ the discretization time at the $k-$th integration step.

The proposed model introduces a better accuracy of [4.16, 18] with a lower level of complexity with respect to [4.17, 19].

4.3.2.1 Parameters Estimation

In order to have an appropriate description of the device, model parameters need to be extracted from measured data. Experimental curves have been obtained by averaging the measured currents obtained by 100 consecutive *set* and *reset* cycles on a 1T-1R cell. Model parameters have been evaluated by fitting the measured data with the proposed model and with what reported in [4.17] and [4.19]. The device has been driven by stepped voltage sweeps (rising and falling in each cycle with voltage steps of 0.1 V). In Fig. 4.8 the experimental I-V characteristic is plotted, together with the results achieved from the considered models. As it can be seen the proposed model ensures a good fitting, comparable with what achieved with models reported in [4.17, 19].

4.3.2.2 Simulation Example

In Fig. 4.9 some simulation results are illustrated. The simulation implements the approximated model previously presented to evaluate the memristor resistance

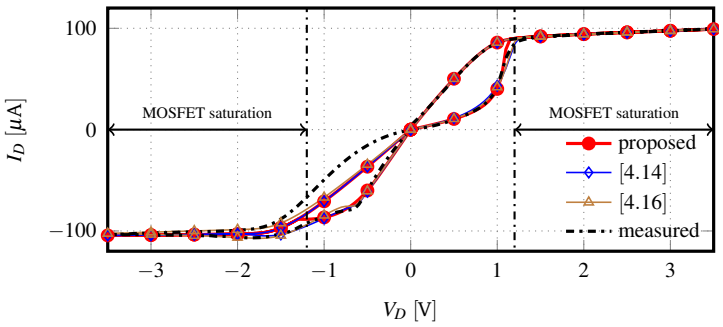
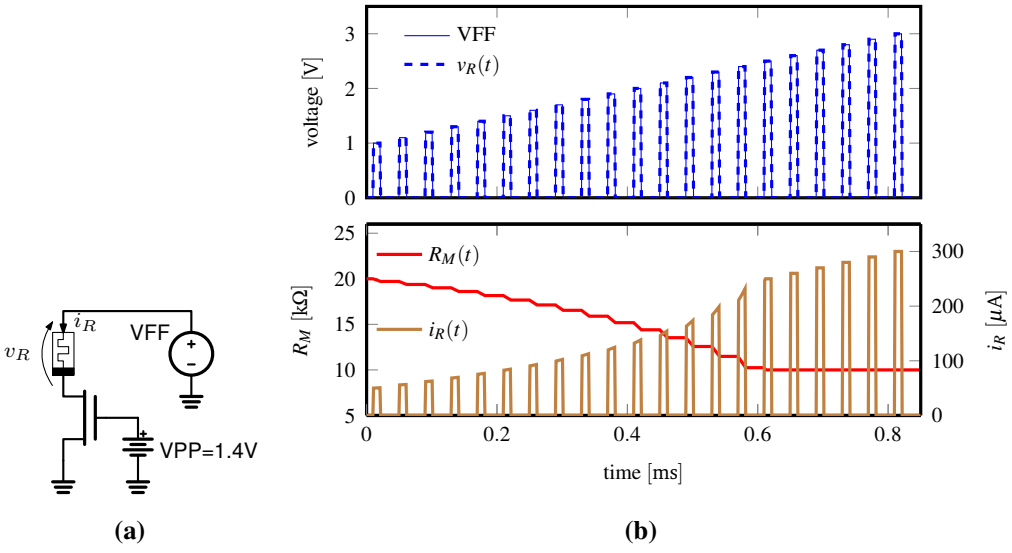


Figure 4.8: Measured I-V characteristics versus estimated values. The extracted parameters are: $R_{on} = 7\,k\Omega$, $R_{off} = 60\,k\Omega$, and $\tilde{K}_I = 4.50 \times 10^9\,\Omega/C$.

during a *set* operation. The schematic is depicted in Fig. 4.9(a).



(a) **(b)**

Figure 4.9: Simulation of a cell *set*. A pulse sequence is applied to the drain-line, while the transistor gate is driven with a DC voltage of 1.4 V. It is possible to notice the linear decrease of the resistance value when the voltage pulse is applied.

4.4 Memristive Memories Architectures

The most common array architectures for resistive memories are basically two: *crossbar* and 1T-1R.

The crossbar approach, schematized in Fig. 4.10.(a) is used when really high densities are needed. In a crossbar array, memristor devices are placed at the cross points of word-lines and bit-lines and the electrical access depends on the voltage applied across the row and the column of the selected cell. The selection mechanism is the following: all the un-selected devices are driven at an intermediate voltage, equal for both word-line and bit-line, so that a zero voltage drop across them is held, while, for the selected one, a full swing voltage drop is driven. An example is shown in Fig. 4.10.(b).

The main drawback of this approach is due to the parasitic currents (*sneak currents*) flowing through the unselected devices across which is applied a low, but non-zero, voltage. As depicted in Fig. 4.10.(b), the selected device is driven by a full range voltage (green highlight), while the sneak currents affect the de-

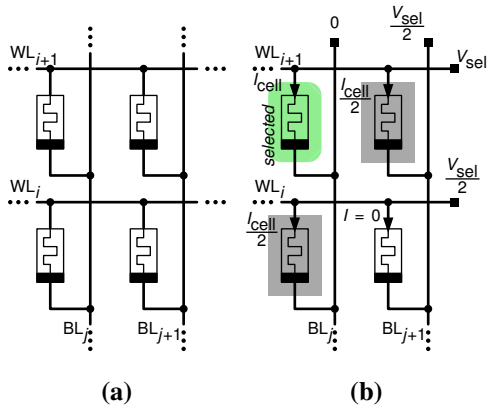


Figure 4.10: Sample of a crossbar array (a) and selection approach (b). Sneak current effects are also shown.

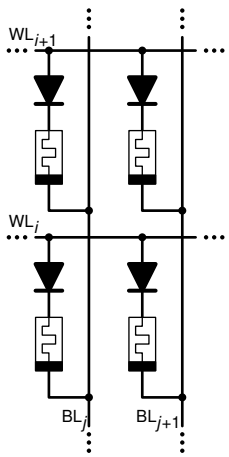


Figure 4.11: 1D-1R array.

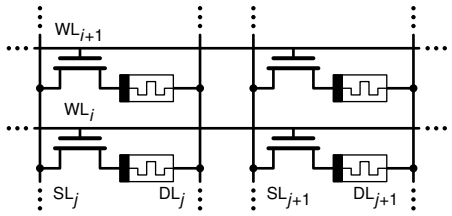


Figure 4.12: 1T-1R cell schematic.

vices connected either to the selected word-line or to the selected bit-line (gray highlighted). Others should be unaffected. This leakage is strongly dependent on the voltage amplitude used in the write/clear operations and on the number of unselected elements and thus, speed, power consumption and endurance degrade with increasing densities, [4.22, 23].

Sneak currents issues can be solved by improving the selectivity in the crossbar approach. An example is the 1-Diode/1-Resistor (1D-1R) element in which a diode is implemented in series to the resistive element (Fig. 4.11). The cost in terms of area of a 1D-1R device is not much higher than the simple crossbar, as diodes can be easily implemented just below the oxide area. However, this architecture is not efficient for BRS devices, as they need to be biased in both verses.

A more reliable architecture is based on the use of 1T-1R devices (Fig. 4.12). The basic cell is composed by a transistor (1T), used as a switch, to access the resistive element (1R). Each 1T-1R is connected to two separate bit-lines: one contacting the source terminal of the transistor (usually defined *source-line*) and the other contacting the anode of the memristive device (called *drain-line* or, more generally, bit-line). Provided the cost in terms of lower density, the use of a switch improves power, speed and endurance, as the only current flowing during an access phase is the one through the selected device. For this reason 1T-1R is considered a choice suitable for embedded applications.

4.5 Radiation Effects on Memristive Devices

Resistive memories have demonstrated a strong robustness against SEUs caused by high-energy particles. The reason is intrinsic, as ReRAMs do not store information by mean of charge retention, but in a resistive state whose change is regulated by process with a high inertia.

However, experiments carried on in [4.24] have proven the occurrence of SEUs in 1T-1R cells. Their origin has been demonstrated to be provoked by current transients in the memory cell transistors that represent the weak part of the ReRAM element against the radiation effects.

As discussed beforehand in previous chapters (2.3), SEEs are mainly due to charge collection phenomena occurring in p-n junctions; the generated currents, in fact, induce voltage drops across the resistive elements, increasing the probability to obtain an appreciable state change.

Actually, even if SEUs show up as instantaneous spurious state changes, each due to a single ion, in ReRAMs these events are somehow depending on the charge collected by subsequent ion strikes. In fact, in ReRAMs' resistance can change continuously in between the two limits and, for this reason, if no restore process is implemented, accumulated ion dose may slowly affect their resistive state, until reaching a threshold value, beyond which an error occurs.

The intrinsic asymmetry between the *set* (faster) and *reset* (slower) makes very difficult spurious transitions from the LRS to the HRS. Moreover, the lower impedance path of the LRS path makes inefficient the charge collection process induced by ion strikes. Beside this, charge collections at the source are not effective as no significant voltage drops establish across the memristor.

An important factor for SEUs occurrence in ReRAMs is the voltage applied at the memory cell. Resistance switching is a voltage controlled process and, for this reason, the probability of SEUs increases with drain-line voltages. Fig. 4.13 shows

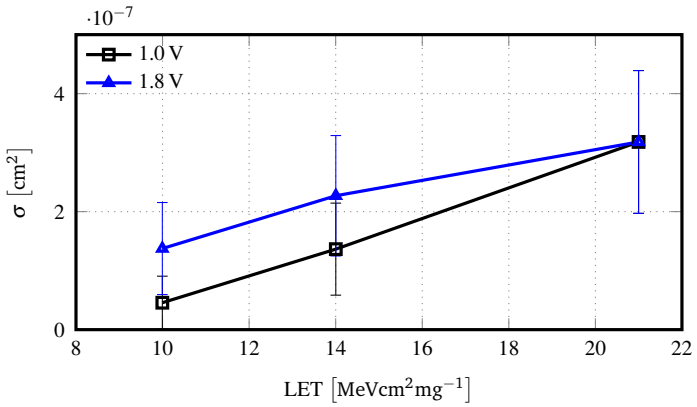


Figure 4.13: SEUs' occurrence versus LET for different bit-line voltages, [4.24].

as, for a certain LET value, the number of SEUs increases for higher voltages. SEUs' occurrence, then, saturates with high LETs as the ion energy starts to be sufficient to determine errors.

If cumulative effects are considered, the high robustness of single resistive oxide memory devices against TID and displacement damages (DDs) has been exhaustively demonstrated [4.25–28]. In particular, HfO_x/Hf devices have shown no remarkable effect to total doses up to several Mrad [4.29–31].

The most remarkable physical effect that occurs in memristive devices when a high energy particle hits the resistive oxide stack, is a displacement damage in the lattice. These damages lead to the creation of additional oxygen vacancies that slightly perturb the resistive state of device. As in the case of SEEs, it is crucial to understand the impact of the TID on the entire 1T-1R cell, considering how important is the contribution of the transistor in the degradation of the memory element. Interesting results have been shown in [4.32]. As depicted in Fig. 4.14, at very high fluence values (2×10^{14} cm^{-2} of 1.8 MeV protons) the HRS is compromised by the oxide vacancies degradation induced by the lattice damages. However these damages are not irreversible and (high) resistive states can be recovered with a certain number of writing cycles.

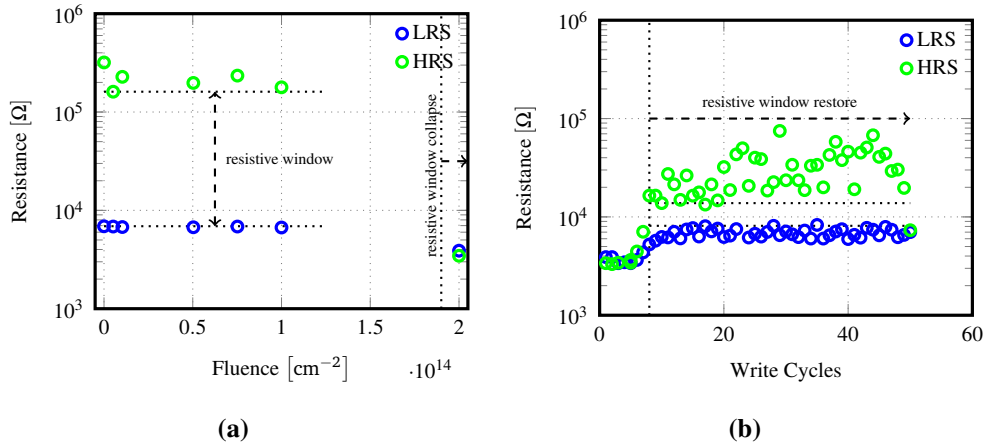


Figure 4.14: LRS/HRS state of a single 1T1R ReRAM cell for different 1.8 MeV proton fluences, [4.32]. The loss of the resistive windows occurs for fluences higher than 2×10^{14} cm^{-2}.

In this work some important results are presented: in Chapter 7 a full characterization and modeling of the displacing damages occurred on 1T-1R cells exposed to protons and heavy ions has been discussed. Also in this case, TID damages have been proved to be recoverable.

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Chapter 5

Radiation Hardening By Design

5.1 Introduction

AROUND forty years ago, as electronics for space applications were fast developing for the increasing needs of modern communications, it became necessary to find new solution for the implementation of circuit that could face the radiation effects.

Historically, the first approach that has been used to minimize the effects of high energy particles on electronic systems has consisted in implementing devices with dedicated technology processes (i.e. SOI, Silicon On Sapphire (SOS)) and heavy shielded packages, both causing higher costs, heavier pay-loads and lower performances (with respect to their traditional homologous). Initially these aspects had a negligible impact on space application design, because of the overall high costs and because of the not so demanding performances required from the electronic systems.

With the increasing interest in space missions for telecommunication and defense application, the effective impact of the electronic systems has grown, pushing the design effort toward more convenient and cost-affordable solutions. More-

over, in the last years electronic systems have been characterized by an always increasing level of integration due to the greedy demand of functions in electronic devices, while a niche area such as the space application one, have not completely exploited the performance advantages of the integration technology, preferring architectures and design strategies more focused on reliability and endurance.

From these needs a more effective trend to deal with the radiation effects in semiconductors has established: the Radiation Hardening By Design (RHBD). Thanks to it, common silicon technologies are used and the designer effort consists in minimizing the radiation effects at architecture, circuit and layout level. This approach is becoming more and more attractive because of its lower costs and higher performances and, moreover, it can be extended to those traditional applications that have to deal with harsh environment, like automotive systems. For this reason it is important to study architecture and design strategies for rad-hard complex systems and treat those aspects that are strictly connected with the sub-micron integration issues.

As spotted, the RHBD techniques cover the three fundamental levels of the typical design flow for integrated circuits, proposing diverse solutions and approaches such as:

Architectural Level: redundancy, error correction codes (ECCs), adequate floor-planning of the functional blocks can minimize the impact of the radiation effects on the functionality of the system.

Circuit Level: congruous digital design styles, proper transistor sizing, novel circuit solutions can minimize the impact of single event effects.

Layout Level: correct placements of devices, wells, bias contacts and so on minimize the effects of long term exposures and disruptive events.

In the present chapter we will introduce some fundamental RHBD techniques

according to the solution of the radiation effects described in the Chapters 2 and 3.

5.2 TID Effects Hardening

In the previous chapter it has been shown as the most important consequence of radiations in a semiconductor lattice is the ionization and the resulting free charge is responsible of the eventual degrading effects. From the physical analysis some remarks can be pointed out:

- Cumulative effects increase with larger oxide thickness, higher applied electric fields, insufficient purity of the oxide manufacturing process, meaning that TID effects become less important as miniaturization increases.
- Single event effects depend on doping concentrations, critical charge of the electric nodes, oxide thickness and, oppositely to cumulative effects, SEEs impact increases with smaller device sizes.

As it comes out, a technological compromise is necessary between cumulative and instantaneous effects and all the design choices have to deal with it. So, even if the manufacturing process is important in TID effects minimization, some harmful effects need to be treated with more complex design efforts, according to the RHBD purpose.

The most relevant degradation related to TID effects is the radiation-induced leakage due to the edge effect in MOS devices and the relative solution has to be implemented at layout level.

A smart way to get rid of the overlapping edge of the poly over the thin/thick oxide interface, is the use of enclosed gate geometries for transistors, defined as Edge-Less Transistors (ELTs). The first use of ELTs can be found in 1977 ,

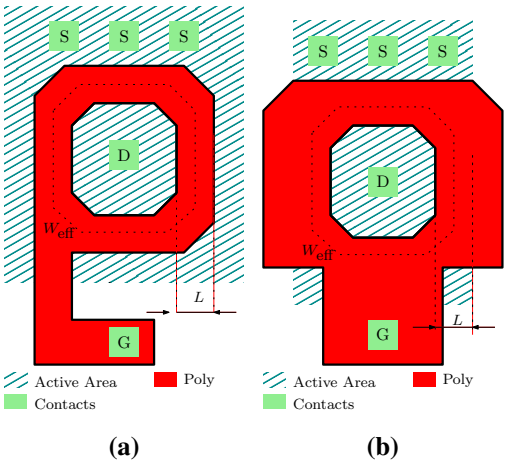


Figure 5.1: Examples of enclosed gate geometries. The geometry in (a) has a larger drain area, while the one in (b) offers a larger gate area and a smaller drain area.

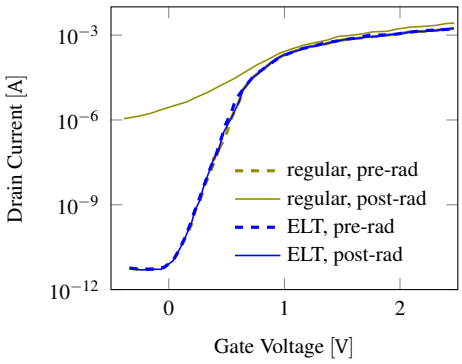


Figure 5.2: Pre- and post- irradiation experimental curves for edge-less and regular transistors.

where an enclosed poly-gate structure for the transistors, referred to as Closed complementary-symmetry MOS (COS/MOS) Logic (C^2L) was used for performance improvement, [5.1, 2]. Then, in 1999, Anelli et al. in [5.3] showed as annular gate geometries could be an effective solution to mitigate degrading TID effects.

An example of this geometries can be found in Fig. 5.1, where two different implementations of enclosed gates have been depicted.

The effectiveness of the ELTs has been extensively proven and represent the state of the art of the transistor implementation if a high level of radiation hardening has to be achieved. In Fig. 5.2 some experimental data have been shown. It is evident the huge degradation in terms of off current for the regular transistors with respect of the small shift of the ELTs.

Unfortunately, this geometry presents various drawbacks, mainly related to a lower area efficiency. As it can be seen, differently from regular transistors, source

and drain terminals in ELTs are not symmetrical and, thus, their areas are not equal. This asymmetry has to be taken into account in some analog application.

It is evident, then, that the minimum size transistor has a much larger area occupation with respect to the minimum regular transistor of the same technological node, as the minimum size depends on the smallest annular geometry that can be designed. The worse area performance is more evident if multi-finger structure are considered, whereas multiple fingers are substituted by multiple rings. Moreover, particular attention has to be paid in sizing ELTs. In fact, the geometric features of width and length have to be carefully estimated by evaluating the equivalent sizes through numerical estimations.

5.3 Single Events Hardening

5.3.1 Hard Errors Hardening

As discussed in Chapter 2, ionization induced latch-ups are extremely harmful. Their occurrence, however, can be significantly minimized by some layout precautions.

Now, let's consider the schemes reported in Fig. 2.16. A latch up is triggered by the current flowing through the bases of the parasitic BJTs and enhanced by the positive feedback through the well-substrate resistances. It follows that the well/substrate resistances have to be minimized, while the well and the substrate volumes have to be properly split.

For the first aspect it is necessary to provide a sufficient number of contacts for the substrate/well bias. Then, to proper insulate the well and the substrate, a very effective technique is the use of double guard rings. For CMOS circuits, it means to implement separately the n and p parts of the circuit, each in the proper well, and then surround each area with a congruous number of bias contacts. The

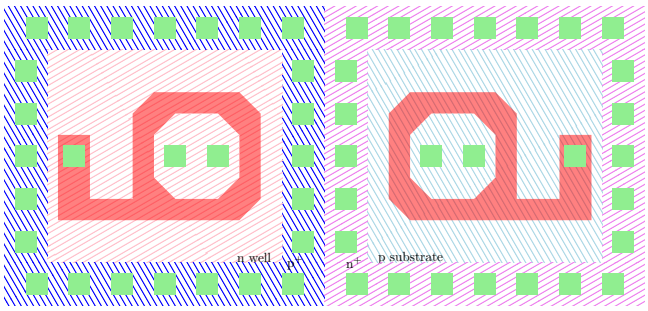


Figure 5.3: Example of layout implementing double guard rings.

good insulation is granted by the inverse voltage across the well and substrate that brings about a depletion volume.

An example of layout implementation with the use of ELTs and double guard rings is shown ing Fig. 5.3. The two transistors are confined in the respective area; the n-well and the p-substrate are, on their turn, surrounded by the bias diffusions that ensure a reciprocal insulation. It is evident how the increase of reliability is paid in term of lack of efficiency in area, as connections and placement are strongly affected by this approach.

5.3.2 Single Event Upsets Hardening

SEUs are peculiar problems for memory circuits exposed to radiations. For this we will refer to the simplest and most common memory cell configuration, i.e. the cross coupled inverter pair.

Going more in specific, it has been shown that the upset events are caused by a ionization-induced charge re-distributions through the nodes of the cells. A circuit solution that may increase the critical charge in the memory cell is the use of a capacitor across these nodes, as depicted in Fig. 5.4. The effectiveness of the solution takes advantage from the Miller effect across the nodes NT and NC, because of the high gain of the positive feedback. For this reason, even in SRAM

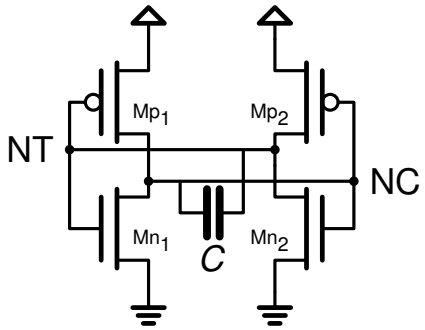


Figure 5.4: Cross coupled inverter pair with Miller Capacitor.

cells, where the high density forces small sized capacitors, a significant increase in critical charge can be obtained. Of course, this solution increases the electrical inertia of the cell as well, making slower the writing process.

5.3.3 Single Event Transient Hardening

The transient voltage fluctuations due to the ionization events are responsible of spikes and wrong evaluations in digital circuits. The most effective approach to mitigate these effects consists in using circuit design styles that allow a full control of the electric nodes of the network.

First, dynamic logic styles should be strictly avoided, because the retention of the data held by nodes cycle by cycle is very weak, being it based on parasitic capacitance, meaning a very small critical charge. For this reason, it is strictly recommended the use of a static combinatorial CMOS logic, [5.4].

As remarked, floating nodes should be avoided. For this reason, series of more than two transistors should be avoided. An example of possible dangerous situation is reported in Fig. 5.5. If transistor M_1 and M_3 are on, the middle transistor M_2 is susceptible by ionization induced charge sharing as its p-n junctions are inversely biased. For this reason, a single event is capable to switch the state of the middle transistor and, consequently, induce a wrong state.

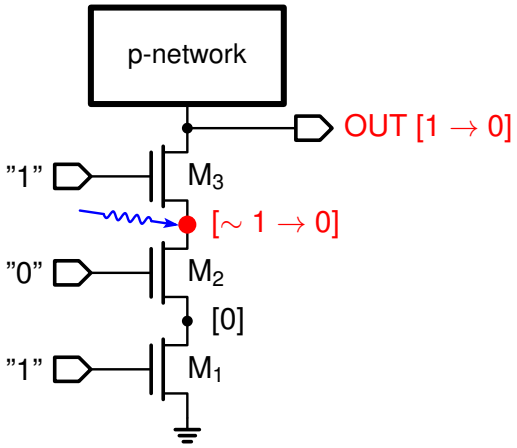


Figure 5.5: Example of erroneous switch due to a single event in a series connection of transistors.

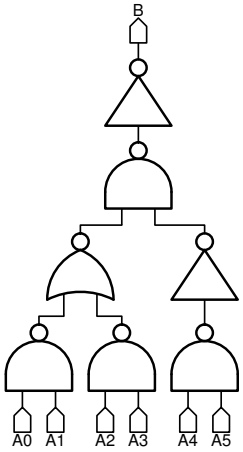


Figure 5.6: Example of a 6 input AND implementation by mean of two inputs basic gates.

5.4 Architectural Strategies for Single Events Minimization

Redundancy is a common architectural technique that can mitigate the impact of radiation induced errors in memories. The addition of some bits to the stored digital words, according to particular ECCs, can lead to the detection and, eventually, the correction, of single or multiple errors. ECCs can be then associated to other mechanisms such as majority voting or operation repetitions in order to complete the correction algorithm.

These solutions are well established practices, not taking into account the physics involved in the error generation, and eventually costly in terms of area and access time. As a general aspect, single events errors cannot be totally eliminated, and the approach of the above cited techniques is to ensure functionality in presence of events or even errors. Beside this, it is important to inhibit any propagation of the instantaneous effects.

5.4.1 Asynchronous Design

Due to the transient and stochastic nature of single event effects, the clock synchronization can be a vehicle of errors in digital circuits. Some transients on the clock nodes, in fact, can be seen as spurious clock transitions and may cause harmful functional errors. For this reason, asynchronous circuits are preferred, as this reduce the sensitivity window of the error to the only circuit blocks interested by the signal switching.

5.4.2 Floor-Planning

Asynchronous circuit somehow introduce a time independence between the various circuit blocks of a system. A spatial confinement of errors can be achieved by dividing the full system in smaller functionally independent sub-blocks. In the case of memories, for example, a whole array can be split among various sub-arrays. Consequently, the single functional blocks such as decoding and I/O, originally dedicated to whole array, need to be replicated for each sub-array, [5.5, 6].

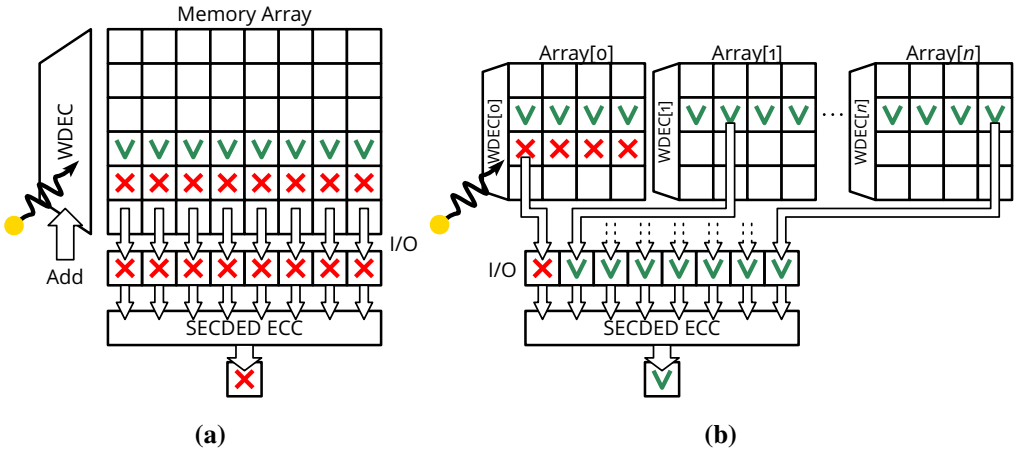


Figure 5.7: Single (a) and independent (b) memory array architectures.

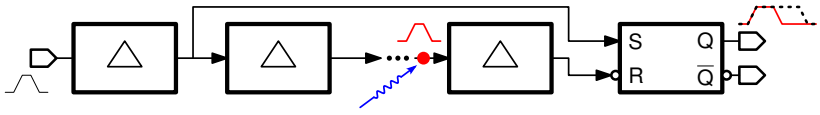
This approach is effective and extremely convenient in concurrence of ECCs

strategies, [5.7]. In fact, some single events can show up as multiple errors, as in the case of a word decoding malfunctioning. An example is shown in Fig. 5.7: a single event in a normal array causes a multiple error, while, in the sub-block configuration, the eventual multiple error shows up as a single one and eventually corrected by the correction algorithms.

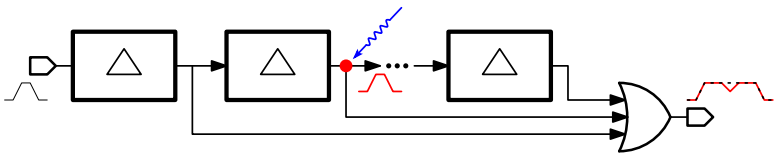
As in the other cases, architectural choices aimed to reliability are area (and consequently) power effective.

5.4.3 Latches Minimization

Transient effects can be somehow absorbed by the characteristic delays along the signal path: fast radiation-induced spikes are attenuated by the real raise and fall time of the gates. On the other hand, as discussed in Chapter 2, latches are extremely sensitive to voltage transients, because they can lead to complete state flips. For this reason the design of state machines should avoid, or at least minimize, the use of latches or Flip-Flops preferring, for example, asynchronous solutions as delay chain implementations. An example is reported in Fig. 5.8, where a digital phase is implemented by mean of latches and delay elements.



(a)



(b)

Figure 5.8: Different implementations of a digital phase.

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Chapter 6

Rad-Hard ReRAM Design

6.1 Introduction

EMERGING memories have been investigated for years, but, to date, they occupy a marginal place in the memory applications scenario. NAND Flash memories are still the undisputed winner in the market competition for their reliability (it is a mature technology) and, above all, for their low cost-per-bit. In fact, the recently developed stacking and piling techniques [6.1–5] overcame the density saturation due to the shrink limits, delaying their (many times) forecast decline.

However, in the scope of the space applications, the cost-per-bit is not a major requirement, as the storage capacity is not as high as the one required in consumer applications. On the other hand, the main requirement is the highest robustness against radiation effects and emerging memories gain an important position in that field. Memories are regular arrays of basic cells surrounded by a digital and analog periphery necessary to manage the data access and, for a full radiation hardening, both of these blocks need a particular consideration during the design development. In this scope, Flash memories present some criticalities for space

applications: beside to the charge retention issues related to single events and cumulative dose, as explained in Chapter 3, in their periphery, charge pumps are very susceptible to SELs, while the memory cells are not implementable by mean of ELTs in order to guarantee a reliable charge injection.

In the wide scenario of emerging memories, oxide resistive technology turn out to be really profitable for space applications. Their physical storage mechanism is intrinsic robust to radiations, while the periphery circuitry does not need charge pumping, so that normal RHBD techniques can be really effective. As it follows, it seems highly profitable for space application to consider a radiation-hardened design of an oxide memory.

However, oxide memories, like the rest of the other emerging technologies, still suffer a strong process variability. Because of this, in large arrays, cells placed in different and distant positions from each other, may present very different behavior. Because of the parasitic RC of the internal connections, this variability is much more difficult to manage when the memory is accessed. A technological characterization is, then, as much as necessary and, for this reason, a proper test device should be developed in order to collect all the basic data for a complete characterization of the technology. In this work, developed in the frame of the European project "R2RAM", a 1-Mbit ReRAM device has been designed in collaboration with RedCat Devices srl (Milan, Italy) and silicon prototypes were manufactured by IHP-Microelectronics (Frankfurt-Oder, Germany).

The test capabilities of the memory device described in this chapter are enhanced by the implementation of a double access strategy, providing a direct memory access (DMA) beside a standard read access: a dedicated supplementary access path allows test units to drive any single cell and measure the relative current, allowing a complete physical characterization.

The present chapter will introduce the technological requirements related to

Corner Name	Process (n-type/p-type)	Voltage [V]	Temperature [°C]
typ	nominal/nominal	2.5	27
nfc	fast/slow	2.5	27
pfc	slow/fast	2.5	27
bcc	fast/fast	2.75	-40
wcc	slow/slow	2.25	150

Table 6.1: Design Corners

the resistive cell, necessary to understand the adopted design choices. To follow, our discussion will focus on the architecture and floor-plan of the device, describing the main functional blocks, for each of whom, the circuit solutions will be presented.

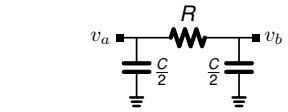
6.1.1 Simulation Settings and Modeling of Parasitics

The circuit solutions described in the present chapter will eventually be provided with computer simulations, in order to consolidate the implemented design choices. The design corners used in the simulations are summarized in Tab. 6.1.

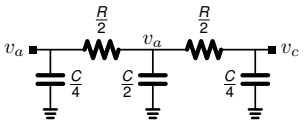
The simulation results presented refer to post-layout data, with parasitic resistance and capacitance extracted by the specific tool, from the layout database.

Memories, and in particular this device, are large structures, characterized by long interconnections that considerably affect the signal synchronization among the different blocks (for example word-lines) and may lead to excessive voltage drops (along bit-lines during read or write operations). For this reason long metal wires have been modeled by mean of double π transmission line, as schematized in Fig. 6.1(a), 6.1(b) and 6.1(c).

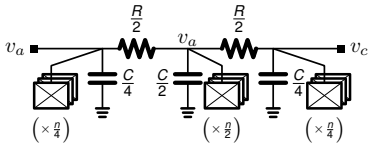
For the memory array, in addition to passive parasitics, the capacitive load of the memory cells has been considered, placing dummy devices at the terminal nodes of the π-lines. The equivalent array sub-block, shown in Fig. 6.1(d), allows



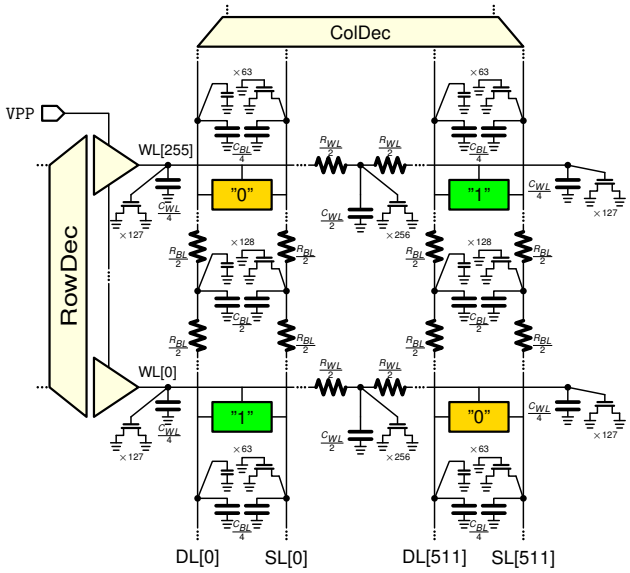
(a) π-line



(b) Double π-line



(c) Long interconnection modeling



(d) Simulation Critical Path

Figure 6.1: Simulation setup. (a) , (b) Modeling of a long metal interconnection having total resistance *R* and total capacitance *C* by mean of π transmission lines. (c) Long metal interconnection modeled by two π transmission lines with the contribution of *n* (capacitive) dummy loads. (d) Critical-Path circuit used for the simulations

faster analog simulations, maintaining a high level of numeric precision.

6.2 The RReRAM Cell

6.2.1 The 1T1R Cell Architecture

As mentioned in Chapter 4, the most common array architectures for resistive memories are basically based on two approaches: crossbars, with no selector element, and 1T1R-based arrays, with a selector device. The first approach is used when really high densities are needed, but the sneaky currents effects can dangerously affect the performances and the reliability of the devices, above all in the scope of space applications. The second kind of architecture relies on the use of a switch transistor (1T) to access the resistive element (1R) (Fig. 6.2).

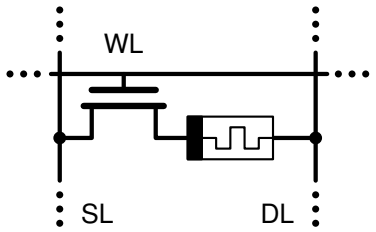


Figure 6.2: Schematic of the 1T1R cell.

Provided the cost in terms of lower density, the use of a switch improves power, speed and endurance, as the only current flowing during an access phase is the one through the selected device. For this reason 1T1R seems to be a necessary choice for reliable applications.

Oxide memristors are bipolar devices, since *set* and *reset* operations are carried out with opposite polarities voltages. It follows that both terminals of the memristors have to be accessed and, for this, each cell element is connected by mean of to two separate and accessible bit-lines (Fig. 6.2).

Of course, the choice of a transistor selector means to introduce an element that may affect TID leakage effects. So, the switch is implemented with an ELT. The technology used for the project is a 250-nm BiCMOS technology provided by IHP-Microelectronics. Fig. 6.3 depicts a rough scheme of layout of the single memory cell.

The basic cell technology steps are the following: first the selecting element,

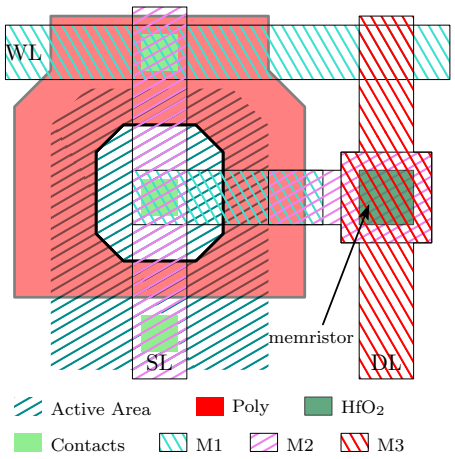


Figure 6.3: Scheme of 1T1R Cell layout implementation using a ELT. The memristive layer is sandwiched between metal2 and metal 3.

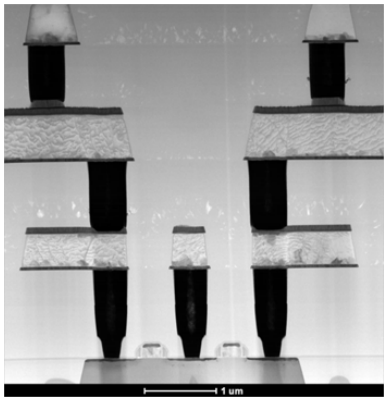
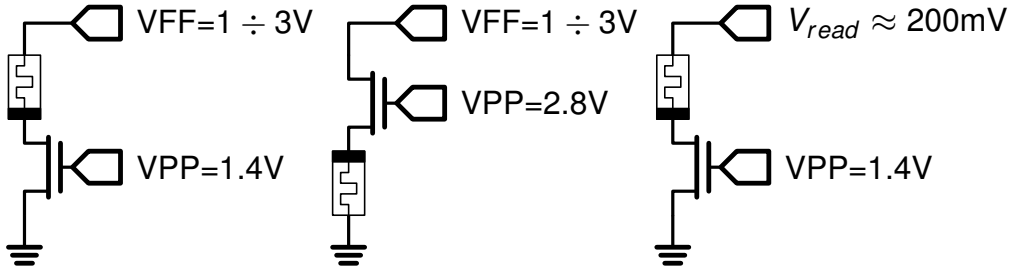


Figure 6.4: TEM image of two 1T-1R cells, sharing the source-contact. The resistive MIM cells are placed on metal 2.

the nMOS transistor, is fabricated. After that, featuring width (W) of 1.14 µm and length (L) of 0.24 µm, the resistive switching cell of MIM is placed between the metal levels 2 and 3. In order to study the impact of the bottom electrode deposition process, an additional AVD TiN with thickness of 20 nm is deposited on top of the metal 2 stack. In addition, in order to study thickness dependence, HfO2 films with thickness of 10nm are deposited at 400 °C by using AVD method. Finally, HfO_2 is capped by 7 nm ionized metal plasma (IMP) Ti and 20 nm PVD TiN. The devices is then induced by a 400 °C/30 min post-metallization annealing (PMA) step. A transmission electron microscopy (TEM) picture of the elements is shown in Fig. 6.4.

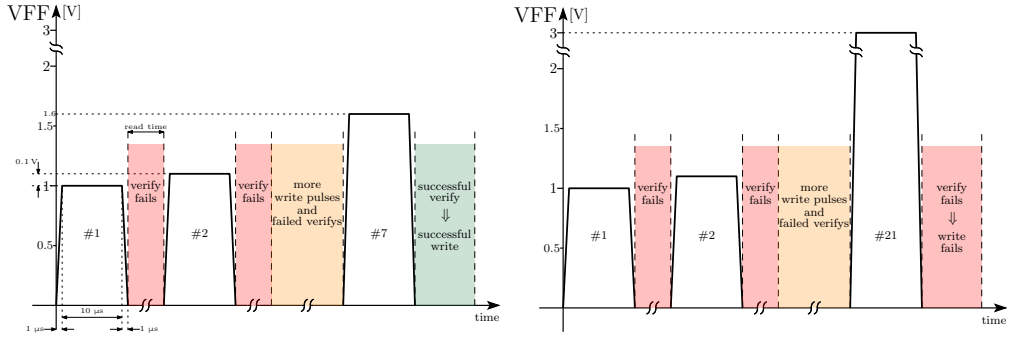
6.2.2 Requirements

The 250-nm BiCMOS technology provides a maximum supply voltage of 2.5 V (usually this voltage refers to the maximum voltage applicable to the transistor



(a) Set/Forming bias **(b)** Reset bias **(c)** Read bias

Figure 6.5: Biasing conditions for the bipolar cell operations. VFF is the Forming/Set/Reset voltage that has to applied to the memristor, while the voltage VPP controls the compliance current in the different operations.



(a) Write OK **(b)** Write KO

Figure 6.6: Time diagram of a *Write & Verify* operation.

gate, to avoid break-downs of the thin oxide). The *set/forming*, *reset* and *read* operative bias conditions have been schematized in Fig. 6.5.

The driving voltage VFF is provided through a dedicated pin and can vary in the range of $1\,\mathrm{V} \div 3\,\mathrm{volt}$, as a *Write & Verify* algorithm is used. *Write & Verify* algorithms, already used in other NVM technologies, such as Flash, are necessary to optimize the endurance of the memory cells, as they minimize their electrical stress.

Fig. 6.6 depicts a diagram of the *Write & Verify* time evolution. The writing

operations are performed by applying pulses of increasing amplitude (in this case the initial pulse amplitude is 1 V with an increase step of 100 mV) and after each write attempt, the resistive value of cell is checked; if it reaches the target value, then the write operation will stop and will be considered successful, otherwise the pulse amplitude is increased by a fixed step and another attempt is carried on [Fig. 6.6.(a)]. If no successful attempts occurs, the write operation will be considered unsuccessful and the cell will be marked as corrupted and unusable [Fig. 6.6.(b)].

For the gate voltage a devoted supply VPP is provided through a specific pin as well. Two voltage values are considered: a lower voltage of 1.4 V and a higher one of 2.8 V. The former value provides a current compliance for a better reliability during *set/forming* and *read* operations; the latter is necessary to keep the transistor in triode operating region when the *reset* inverse biasing is applied.

The *read* operation, then, present some critical aspects. In fact, excessively large voltages across of the memristor could trigger a reaction into the HfO_2 layer, corrupting the resistive state of the cell. For this reason the read voltage has to be kept as low as possible in order to minimize electrical stress. A read voltage of around 0.2 V is recommended.

Write voltages will be externally provided. A pulse duration of 10 µs would be enough for effective operations. Some requirements are provided for the rise/fall time too: as voltage overshoots can be disruptive for the cell, a 100 ns rise/fall time is suggested.

6.3 Memory Architecture

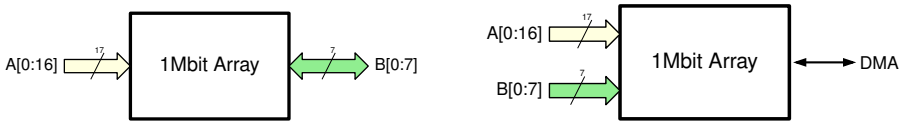
As mentioned, the main research goals of the implemented ReRAM are intended to verify the robustness against radiations of the emerging resistive oxide technology and, at the same time, obtain a cell characterization inside a whole device.

A storage size of 1 Mbit has been considered reasonably sufficient to gather the necessary information. The memory array can be accessed in two ways:

- byte access in standard mode (128 kB device);
- single bit access in DMA mode.

The device I/O consists in a 17 bit address bus, A[0:7], and in a 8 bit bidirectional bus, B[0:7], while for the DMA access a dedicated bidirectional pin is reserved.

A scheme is shown in Fig. 6.7. In particular, for DMA mode, as one out of eight bits has to be pointed, the B bus is used as extension of the address bus, using a 8 bit unary coding [1].



(a) Standard Access **(b)** DMA

Figure 6.7: Access modes of the 128 kB ReRAM test device. For standard access mode (a) the B bus is used for the I/O, while in DMA mode (b) the B bus addresses one selected bit out of eight.

[1] A *unary coding*, or *thermometer coding*, addresses $k = n$ digital levels by asserting only one out of n bits, whereas most common digital codes use n bits to address $k = 2^n$ levels.

6.3.1 Asynchronous Device

Clock trees are avoided in radiation hardened designs, as they may propagate voltage transients along the digital system and lead to wrong states by triggering spurious transients. For this reason, an asynchronous memory has been implemented. A time diagram that summarizes the evolution of the device is shown in Fig. 6.8.

As soon as a bit of the address word or a control input toggles, its transition is detected by an address transition detection (ATD) circuit that consequently drives a triggering signal toward the the control logic. The control circuits, then, internally generate the timings necessary for the operating phases.

A typical CMOS implementation for ATD circuits is shown in Fig. 6.9. The working principle of the circuit is straightforward. Initially the output B is stable at "0", as the same signal is applied at the XOR's inputs. Then, when an address toggles, the XOR gate will see at its inputs two different signals, for a time τ equal to the delay introduced by the digital delay line (a chain of an even number of slow inverters), so that a pulse of τ width is generated. The delay time has to be accordingly designed: conveniently large in order to be effective for the following functional blocks (interconnections offer large RC delays that may degrade the pulse) but not that wide to affect the cycle time.

6.3.2 Differential Reading

Logic states in resistive memories are associated to the resistance values of the memory cell. In principle, the cell resistance can continuously vary from its LRS to its HRS, giving the possibility of a multilevel storage, [6.6]. However, the present technological processes for resistive memories do not easily provide the necessary stability that may allow effective references. Moreover, the resistance

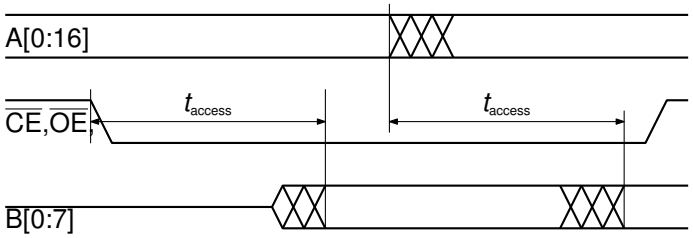


Figure 6.8: Simplified time diagram for an asynchronous read access. Data access is triggered by the transitions of control signals (OE and CE that are active low inputs) and addresses.

ratio further limits the availability of multiple references. So, storage will be based on the two fundamental states:

- LRS (R_{on}) for logic High state, "1";
- HRS (R_{off}) for logic Low state, "0".

With only two digital logic levels, the reading process reduces to a comparison of the resistive state of the cell with an accordingly chosen resistive reference. This comparison has to be carried out by mean of electrical variables, i.e. currents or voltages. Considering the electrical constraints related to the HfO_2 devices, a convenient implementation would be to apply a fixed and constant voltage to the resistive samples and compare the currents flowing through them.

Referring to the scheme of Fig. 6.10, if the series resistance of access transistor is neglected, with the two resistances R_{cell} and R_{ref} the sensed current difference will be:

$$\Delta I = V_{read}\left(\frac{1}{R_{cell}} - \frac{1}{R_{ref}}\right) = \frac{V_{read}}{R_{cell}R_{ref}}\left(R_{ref} - R_{cell}\right) \tag{6.1}$$

From (6.1) it is clear how the current comparison can be optimized by increasing the reading voltage and chosing a convenient value of R_{ref}.

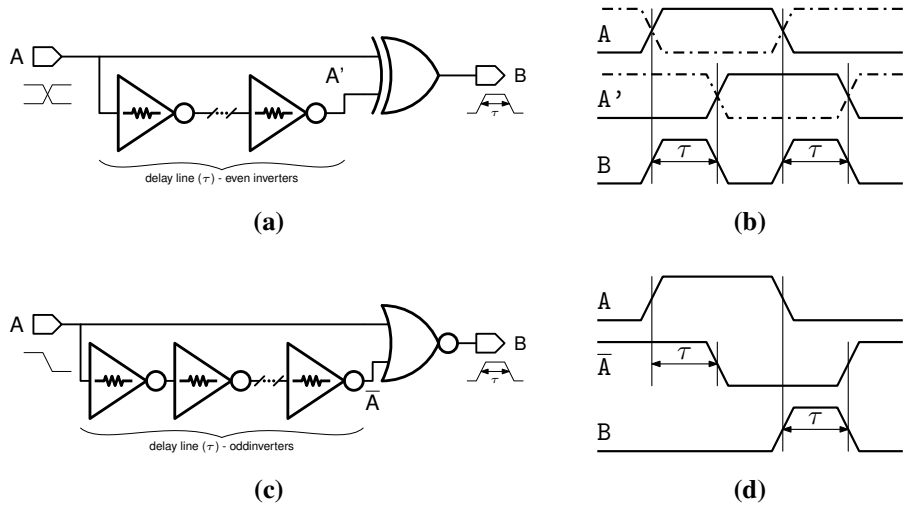


Figure 6.9: CMOS implementation for an ATD circuit (a) and a active-low control signal transition circuit (c). Respective time diagrams are (b) and (d).

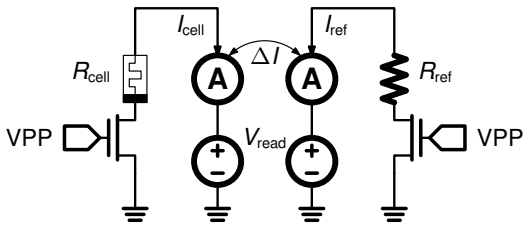


Figure 6.10: Digital read scheme for memristive memories. The resistance values are compared by mean of a current comparison.

As previously mentioned, the read voltage amplitude is limited, because of the reading disturbance to the cell. Hence, the choice of the reference value becomes crucial.

In Fig. 6.11 some resistance distributions are plotted, related to different wafers and runs. As it can be seen, resistances are characterized by a wide intra-wafer variability (wide variances σ), especially for the high resistive states and, also, by a inter-wafer variance (mean values μ change significantly).

For this reasons, a differential storage has been implemented in the memory:

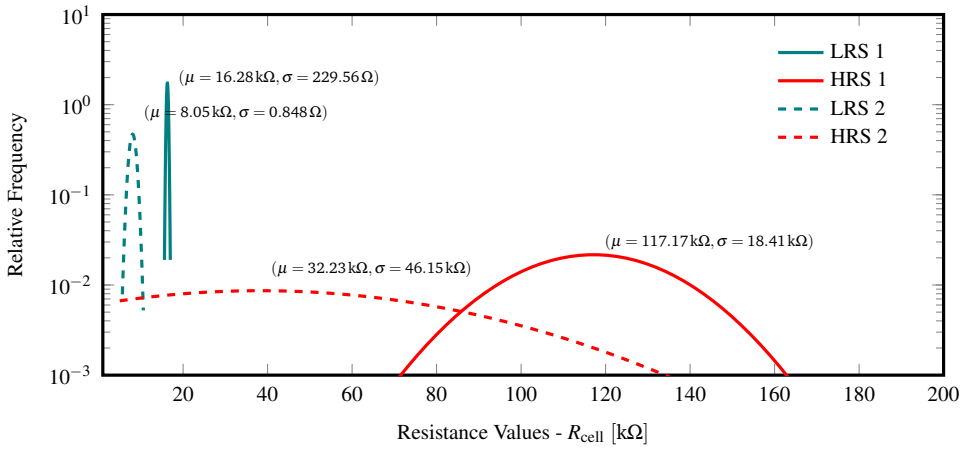


Figure 6.11: Cell resistance value distributions.

at the cost of a halved storage density, two resistive cells are used to store a single bit, [6.7]. The physical size of the device consists, hence, in 2 mega cells for 1 Mbit, [6.8]. The differential architecture is implemented as follows:

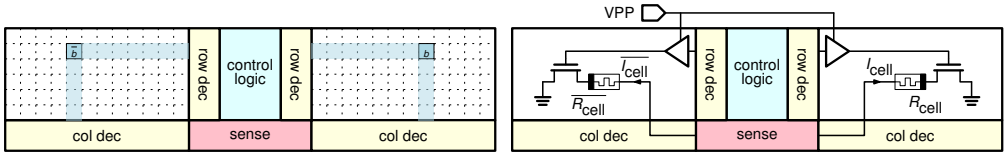
Write: at each write cycle, data are complementary written in two different phases, in symmetrical locations.

Read: for the reading phase, then, the two symmetrical locations are contemporary accessed and connected through their column decoders to the read out circuits that compares the currents and gives the corresponding digital output.

A scheme of the differential reading architecture is depicted in Fig. 6.12. As it can be seen, the decoding structures need to be replicated in both arrays. Then, symmetry has to be granted in order to equalize the parasitic effects of the interconnections for both the complementary cells.

In case of differential storage, the current difference becomes the maximum achievable:

$$\Delta I = \frac{\alpha V_{\text{read}} \Delta R}{{R_{\text{off}}}^2} \tag{6.2}$$



(a) **(b)**

Figure 6.12: Differential approach. The memory array is split in two parts, whereas one single bit b is stored complementary in two symmetrical locations (a). When a data is accessed, the resistance values of the two symmetrical locations are compared (b).

where $\alpha = \frac{R_{\text{off}}}{R_{\text{on}}}$ is the resistance ratio of the resistive cell and $\Delta R = R_{\text{off}} - R_{\text{on}}$ the difference between HRS and LRS. According to the (6.2), the reading process is enhanced with high resistive ratios and more conductive processes (lower resistances).

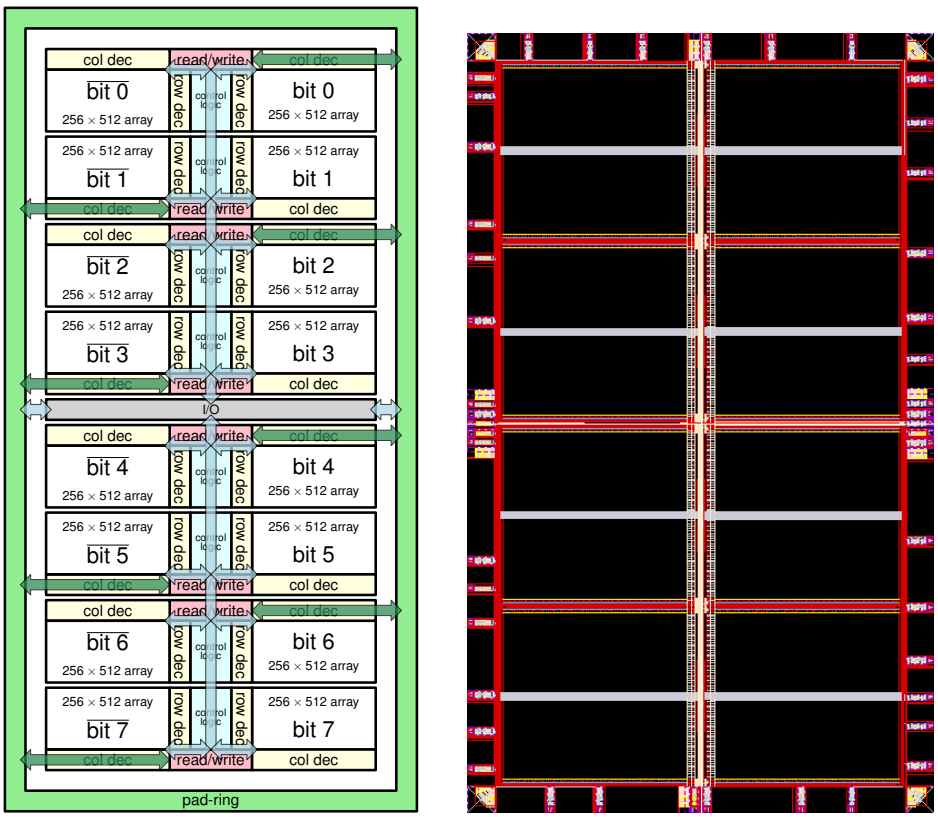
6.3.3 Floor-Plan

The 1 Mbit array is internally split in 8 independent sub-arrays of 128 kbit, each supplied with its own digital (i.e. decoding, control) and analog (sensing) periphery. A scheme of the memory floor-plan is shown in Fig. 6.13.

This floor-plan is compliant with the radiation hardening approach, as any possible transient is confined within the single block of origin and does not propagate to nearby circuits.

As explained in 6.3.2, the memory device provides a differential storage, so in each block a double 128 kbit array has been implemented.

The memory is a stand alone device implemented in a DIL48 package. The pad-ring, that connects externally to the device pins, exchanges data with the device through the I/O block, placed at the middle of the device, which contains also the ATD circuits (as seen in 6.3.1) producing the timing signals that are buffered and rerouted toward the decoders and the control logic blocks.



(a) Floor-Plan **(b)** Layout

Figure 6.13: Floor-plan (a) and layout (b) of the 1 Mbit memory device. The whole array is split among 8 independent blocks of 128 kbit each.

Then, the read-out circuits are directly connected to the pad-ring through bidirectional pads. This is possible as the memory device is asynchronous and data flow does not have to be synchronized through central I/O block.

Moreover, in an asynchronous device, time phases can be locally generated, minimizing the occurrence of multiple bit errors induced by single events.

Each 128 kbit half-array is arranged as a 256 rows $\times$ 512 columns array. The first 9 bits of the address bus, A[0:8]) decode the columns, while the remaining 8 bits (A[9:16]) decode the rows. The selected bit-line/source-line pair is then routed into the sensing circuits.

6.4 FunctionalBlocks

In this section the fundamental functional blocks of the memory device will be described, focusing the attention on the radiation hardening precautions that have been implemented. A functional scheme that summarizes the main functional blocks present in each 128 kbit part is depicted in Fig. 6.14.

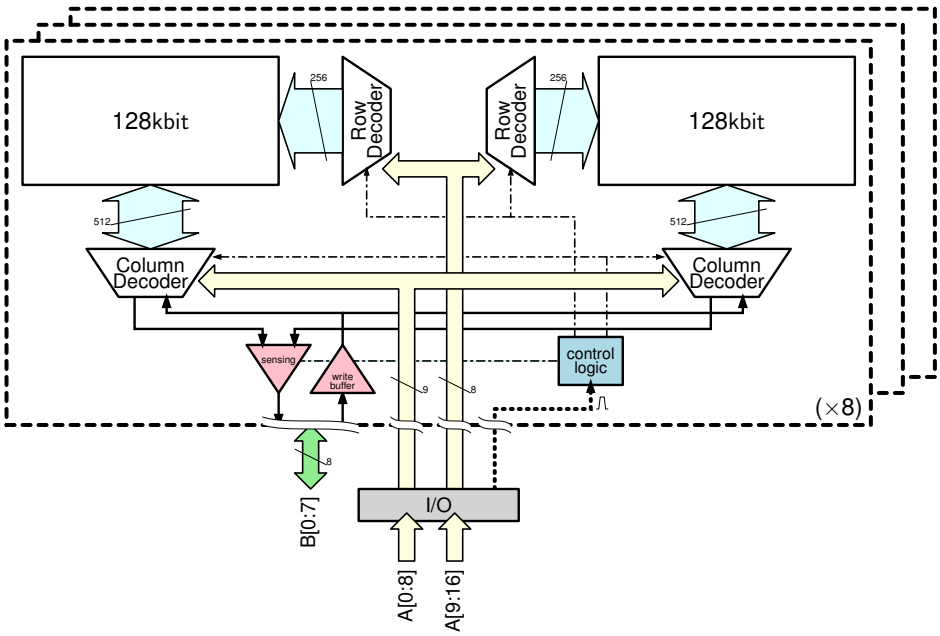


Figure 6.14: Functional scheme of the single block. The row decoder asserts the 512 memory cells; one of them, then, is connected by the column decoder, according to the operation to be carried out, either to the read-out circuits or to the write switches. Each block is also provided with its own control logic block.

6.4.1 Row Decoding

For the row selection a two-level decoding has been used: 4 bits of the address (A[13:16]) decode 16 blocks, each of which is composed by 16 word-lines. Then, the other 4 address bits (A[9:12]) decode, in each block, one of the 16 word-lines.

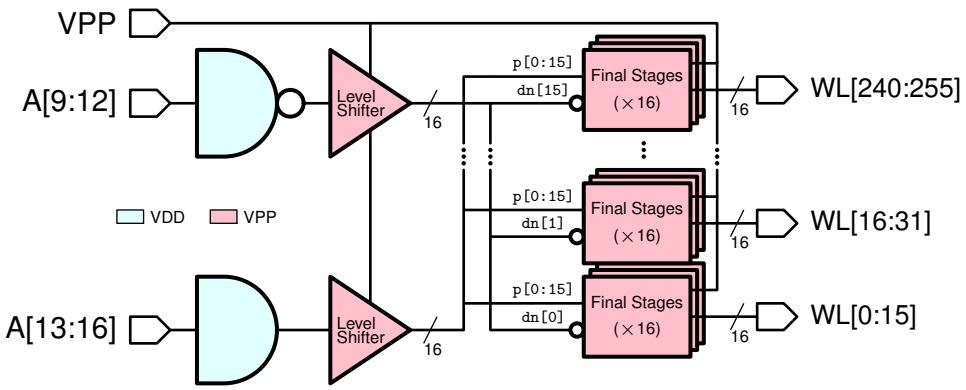
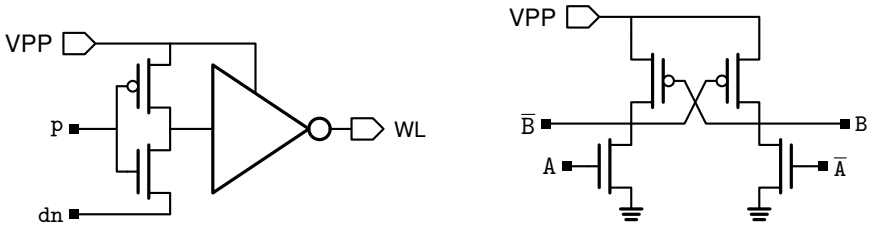


Figure 6.15: Row decoder scheme. A two level decoding has been implemented. Different colors have been used for different voltage domains.



(a) Final Stage **(b)** Level Shifter

Figure 6.16: Row decoder sub-blocks.

The row-decoding scheme is depicted in 6.15.

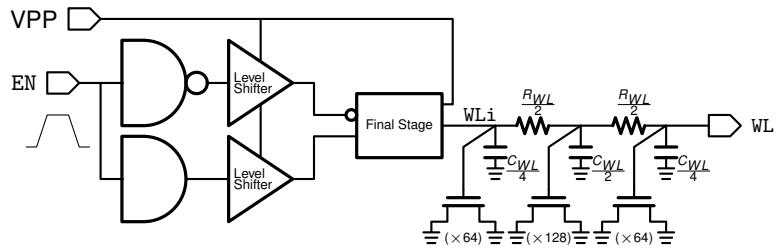
An important feature of the row decoder block is the possibility to drive the word-lines with different voltages, as this is necessary to create the different bias conditions for the resistive cell (1.4 V for forward bias and 2.8 V for reverse bias). The variable voltage supply VPP is driven through a dedicated pin of the device.

The row decoder asserts the relative row by mean of final stage buffers, directly connected to VPP, that provides the current necessary to drive the large capacitance of the word-line. On the other hand, the demuxing stages (AND or NAND arrays) must connect to the final stages through level-shifters.

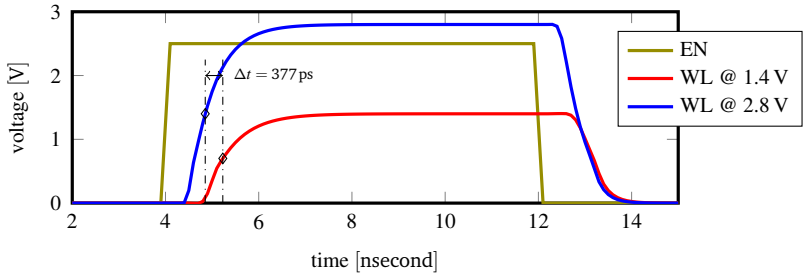
Fig. 6.16(a) shows a schematic of the final stage, while in Fig. 6.16(b) the

level-shifter schematic is depicted. For the level-shifter a traditional differential configuration has been considered.

The level-shifter stage, however, introduces some additional delay. Moreover, for low voltage values of VPP, the driving force of the driver is reduced and this further increases the delay of the word-line signal. A simulation in Fig. 6.17 shows how a lower value of VPP determines larger delays.



(a) simulated circuit



(b) simulated waveforms

Figure 6.17: Simulations of the word-line signal for two different values of VPP. The delay of the signal increases with lower voltages. The word-line metal wire has been modeled with a π transmission line (a). Simulations have been performed with typical process, room temperature (27°) and nominal voltage ($V_{DD} = 2.5\,\text{V}$). Wire parasitics (resistance and capacitance) have been evaluated by post-layout extractions tools to be $R_{WL} = 330\,\Omega$ and $C_{WL} = 550\,\text{fF}$.

6.4.2 Column Decoding

The column decoding architecture has to match the strict bias requirements necessary for the bipolar access to the resistive cell. Two switches for each column of the array is necessary so that, for each access operation, one out of two wires (either the drain-line, or the source-line) has to be selected. Moreover, read and write operations need to be biased with different voltage levels ($\sim 0.2\text{V}$ and $\sim 2.5\text{V}$, respectively). In principle, the use of a bipolar switch (for instance, a CMOS pass gate) would be necessary. However, the implementation of bipolar switches would arise to some critical drawbacks:

Area occupation: the ELTs implementation of bipolar switches, necessary for the space requirements, would be very space demanding and hard to fit with the memory cell pitch.

Parasitcs: strictly related to the area issues, the capacitive load represented by bipolar switches would be three times larger than the one of unipolar devices (p-type transistor are generally twice larger than n-type ones in order to compensate the reduced mobility), representing a clear problem for transient phases during switches.

Interconnections: bipolar switches require differential signals for the correct assertion and this leads to a critical interconnection pattern, as two metal wires per decoded bit should be used. In the considered two-level decoding implementation, with double connections for each cell, the use of bipolar switches would mean to implement 128 metal wires.

6.4.2.1 Architecture

According to these aspects, it looks more convenient to implement unipolar switches, eventually using n-type ELTs for an improved conductivity. The n-type transistors

are compatible with the read operation, as it is performed at low voltages (at least lower than $V_{DD} - V_{th}$). On the other hand, set/forming and reset operations need p-type transistors to drive higher voltages into the memory cell.

This issue is overcome by implementing the column management by mean of two blocks, as illustrated in Fig. 6.18. The first block is proper column decoder for the selection of the desired drain/source of the cell. A two level decoding has been used: the address bits A[4:8] select one out of 32 blocks, each composed by 16 column switches, while the remaining address bits A[0:3] decode one out of 16 columns in the selected block. The second block is constituted by an array of precharge/bias switches that connects the selected columns with the write voltage supply VFF, accordingly to the bias configuration, while un-selected columns are left floating. The control signals assert p-type switches connected to VFF for the write operations and n-type ones connected to ground for the read access.

The full working principle, hence, can be summarized as follows:

- **Write phase (forming/set/reset):**
  - the p-type switches connect VFF to every column;
  - only one column, the selected one, allows a path to ground through the column decoder and the control transistor M_W;
  - all the other un-selected columns are in high impedance.
- **Read phase:**
  - the column decoder connects the selected drain-line to the read-out circuits;
  - the n-type switches are connect to ground to close the read path.

Some read and write configurations are shown and commented in Fig. 6.19 and Fig. 6.20 for standard and direct memory access, respectively.

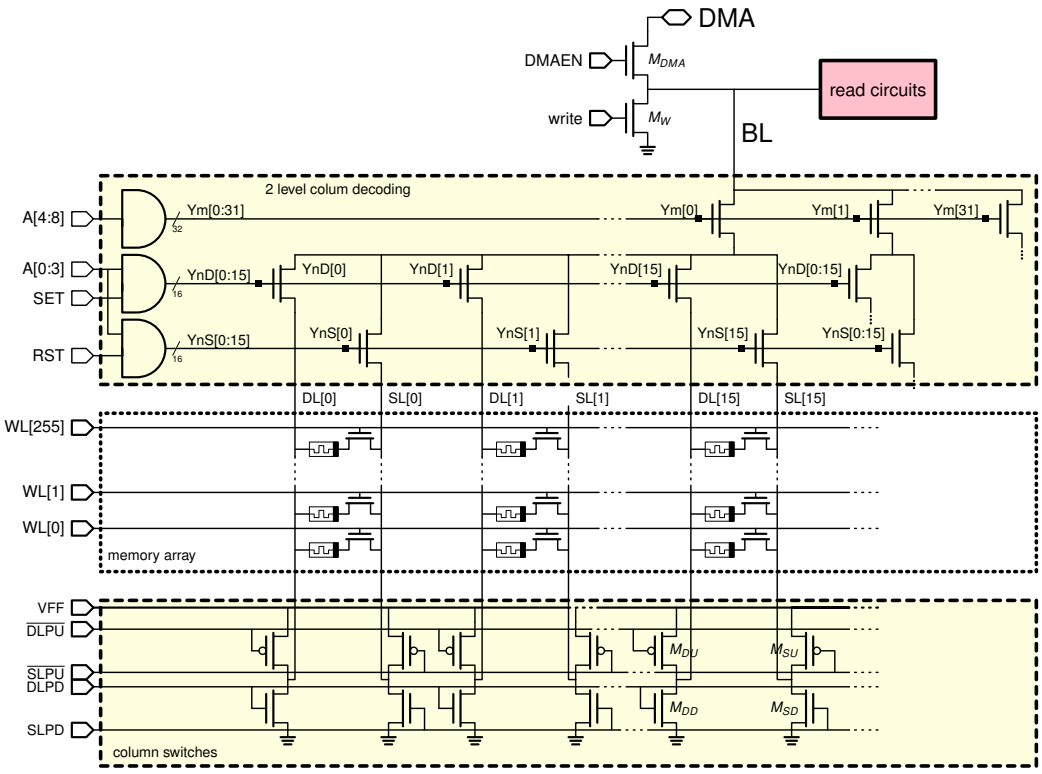
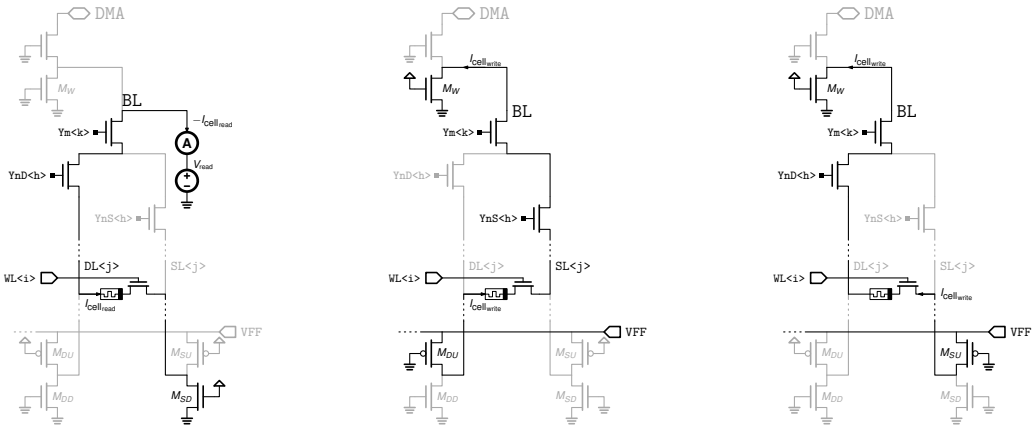


Figure 6.18: Column decoding scheme. Also in this case a two level decoding has been implemented: signals Ym[0:31] select the 32 blocks, while signals YnD[0:15] and YnS[0:15] select the specific drain-line or source-line, for *set* or *reset*, respectively. Then, global control signals activate/deactivate an array of switches for the bit-line bias, according to the data that have to be written: $\overline{\texttt{DLPU}}$ and $\overline{\texttt{SLPU}}$, active low, activate the *set* and *reset* connection to VFF, respectively, while DLPD and SLPU, active high, connect to ground the drain-line or the source-line, respectively.

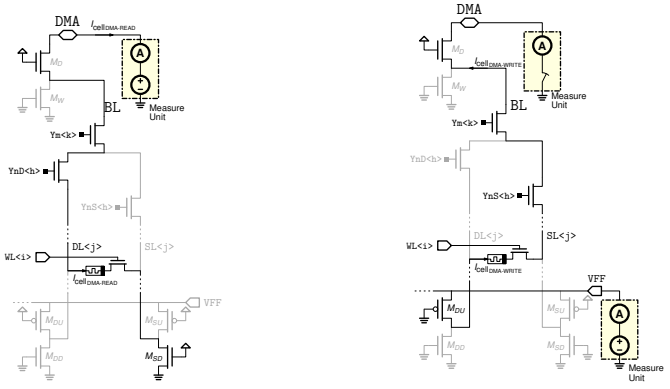
6.4.2.2 Precharge Phases

As previously discussed, a constant control of floating nodes is necessary for SEEs minimization. So, when the memory is in idle state, source-lines and drain-lines need to be held to a constant voltage and, in particular, since 1T-1R cells and column decoding use n-type transistors, driven to ground. This choice is in agreement with the read bias, as low read voltage are used.



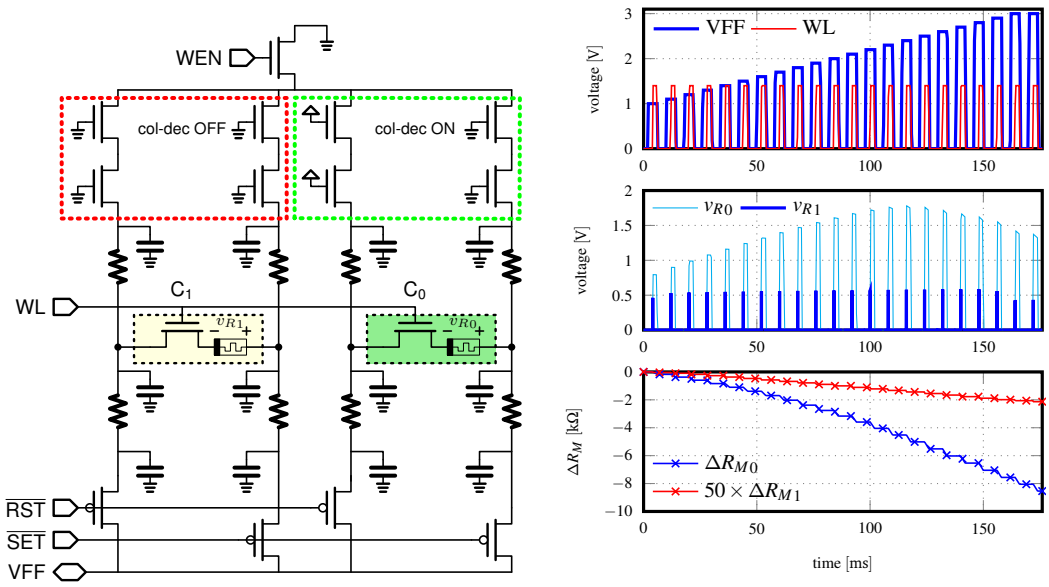
(a) Read **(b)** Set/Forming **(c)** Reset

Figure 6.19: Standard access examples for *read* (a), *set* (b) and *reset* (c) operations. In (a) the column decoder connects the selected cell to the read circuits and the read current has a path to ground thanks to the switch transistor M_{SD}. In (b) and (c), VFF drives all the columns through the switch transistors M_{DU} (M_{SU}), but only the selected one has a current path to ground through the final stage of the column decoder, thanks to the transistor M_W.



(a) DMA Read **(b)** DMA Set

Figure 6.20: DMA examples for *read* (a) and write (*set*) (b). While read mode the measure unit (MU) can directly force the read voltage to the DMA pin, analogously to the standard mode, in the write configuration the MU should connect the DMA pin to ground.



(a) schematic **(b)** simulations

Figure 6.21: Simulations of a *set* operation for two 1T-1R cells connected to the same word-line. Cell 0 is accessed and written. If source-lines are precharged to ground, cell 1 is affected by a spurious *set* due to source-line charge.

On the other hand, in the writing phase, precharging to ground the bit-lines can be critical, as the contribution of the parasitics should be considered. During a writing phase, the selected word-line is asserted and, according to the column decoding topology chosen, all source- and drain-lines are driven to VFF, while only the selected column has a path to ground. However, in case of ground precharge, across all cells of the active row would establish a non-zero voltage for a short time, just necessary to charge the parasitic capacitance of the bit-lines to VFF. As these voltage spikes across cells can lead to spurious writings, they need to be prevented, eventually beginning the writing phase with a precharge to VFF of both source- and drain-lines.

Fig. 6.21 shows some simulation results emphasizing a spurious write in case of a wrong precharge strategy for a *Write & Verify* operation. Two cells, on a

same word-line are considered. The cell 0 is the selected one: a full voltage v_{R0} establishes across it and a resistance change ΔR_{M0} is achieved. The cell 1 is spuriously written by small voltage spikes (v_{R1}) across it, and its resistive state is corrupted ($\Delta R_{M1} \neq 0$).

6.4.3 Reading Circuit

As anticipated in 6.3.2, the standard read access consists in sensing and comparing the currents flowing through two complementary memory cells. The cell currents are generated by applying an appropriate voltage at the selected bit-line and its value has to remain constant in the range of variability of the cell resistance ($R_{\text{cell}} \approx 10\,\text{k}\Omega \div 100\,\text{k}\Omega$).

6.4.3.1 Bit-line Voltage Regulator

A possible voltage regulation scheme is shown in Fig. 6.22: an operational amplifier forces the bit-line voltage to the desired value $V_{\text{BL}i} \approx V_{read}$ driving a nMOS that, at the same time, senses the cell current through its source terminal.

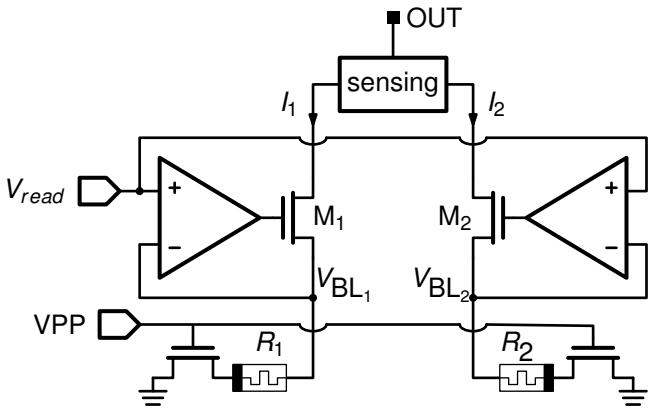


Figure 6.22: Reading principle scheme.

In the described configuration the access time is limited by the band of the op-

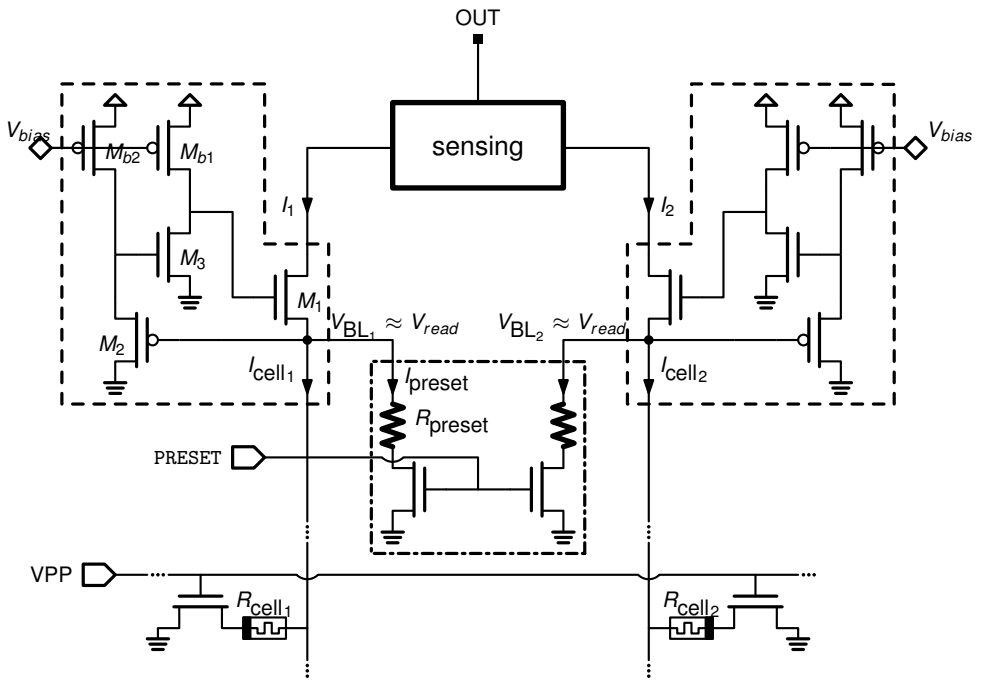


Figure 6.23: Schematic of the read circuit. The voltage regulators (in the dashed boxes) drive a voltage to the respective bit-lines, so that the cell currents $I_{\text{cell}1}$ and $I_{\text{cell}2}$ can be eventually amplified and compared by the sensing circuit. It is also present a preset circuit (in the dash-dotted box): the PRESET signal is complementary to the word-line assertion, so that the voltage regulator is ready to drive the bit-line voltage.

erational amplifier, which may also imply stability concerns. A different solution has been implemented in this work: a simple stage, shown in Fig. 6.23, has been implemented. In this way better speed and stability are expected, [6.8, 9].

The voltage V_{BL} is up-shifted by transistor M_2 (it is supposed to be $\approx 0.2\text{V}$) and applied to transistor M_3; hence, the common source stage together with the source follower provide a negative feedback to regulate the node. The transistor M_1 also behaves as a current follower and it starts to work as soon as the feedback loop turns on, taking some time; for this reason, in order to suppress this delay, when no cell is selected yet, a preset current, close to the average cell current

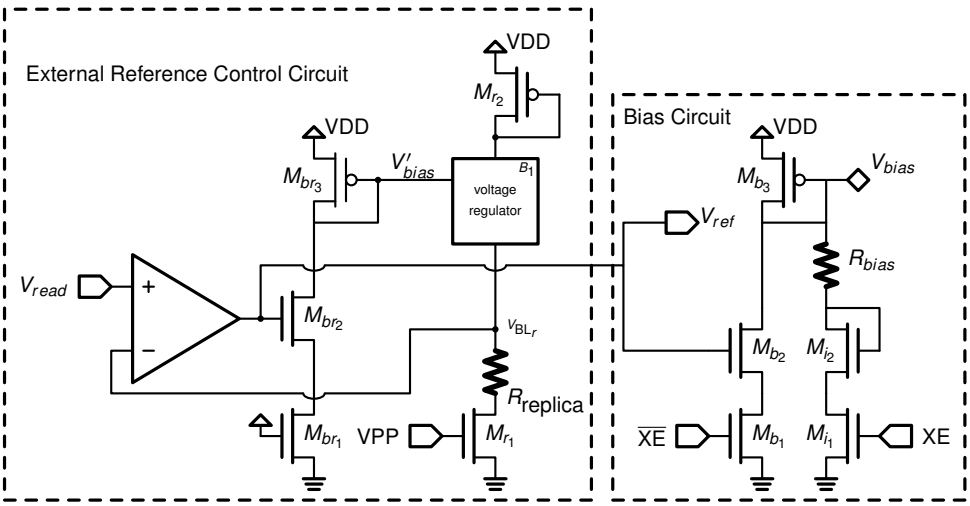


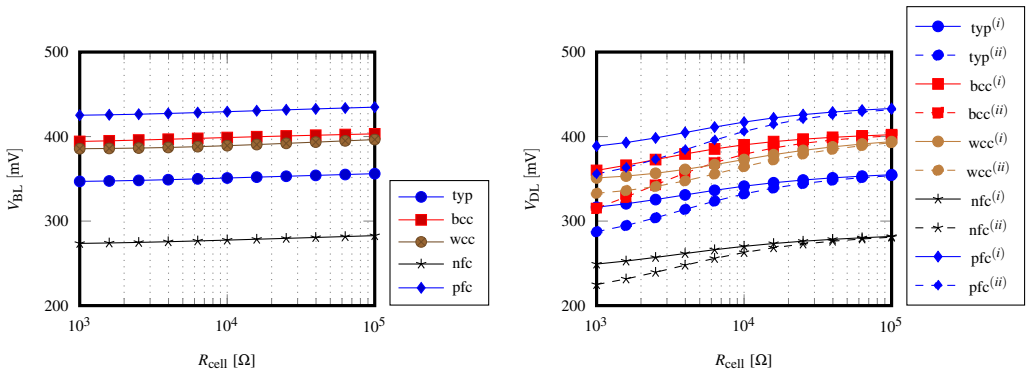
Figure 6.24: Schematic of the bias network for the voltage regulation. The bias can be either internally regulated (XE=1) or provided externally (XE=0). In the second case, the bias voltage V_{bias} is generated by a replica of the circuit that is fed by the external read voltage (V_{read})and supplies the correct reference to the bias circuit (V_{ref}).

value, is provided to the loop some time in advance.

The proposed architecture intends to be reusable for different memristor technologies, offering a fast implementation for the characterization of different processes. To achieve that some tuning features have to be added. A first aspect may concern the reading bit-line voltage; in order to minimize the reading stress for the cell, it must be kept as low as possible and this determines low currents to be sensed, i.e. a lower functional yield.

Nevertheless, it may be useful to inspect, in test mode, the behavior of the memristive cells and tht reading structure under the different read voltage values. This feature is implemented through the control of the bias of the sensing block: the bias circuit, shown in Fig. 6.24, can employ either an internal reference (XE=1), or an external one (XE=0).

As shown in Fig. 6.24, the external reference is obtained through a replica of



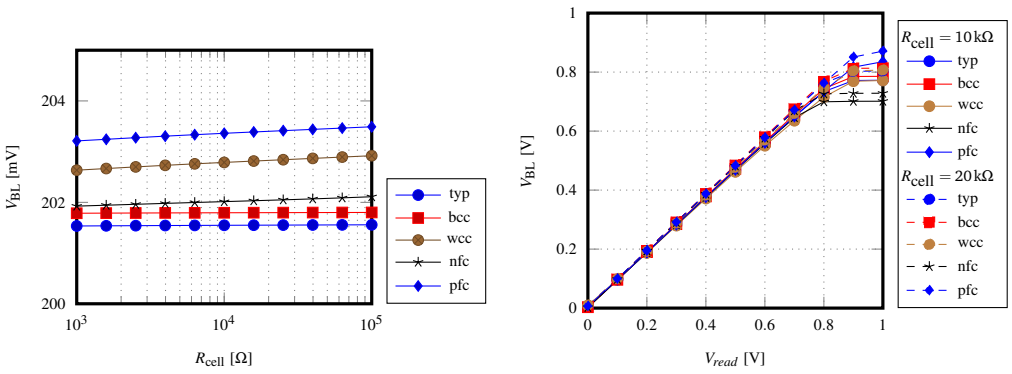
(a) V_{BL} **(b)** V_{DL}

Figure 6.25: DC simulations of the regulated voltage, sweeping the resistance value ($R_{\mathrm{cell}} = 1 \div 100\mathrm{k}\Omega$), over all the process corners. The bias used is the internal generated one. In (a) is plotted the voltage directly driven by the voltage regulator, while (b) are represented the voltage at the memory cell drain-line, for the near (i) and far (ii) cells.

the reading current path (transistors M_{r_1}, M_{r_2} and block B_1) and a replica of the bias circuit (transistors M_{br_1}, M_{br_2} and M_{br_3}): with a feedback loop the regulated voltage V_{BL_r} is read and an operational amplifier drives the bias branch, accordingly to the input reference voltage. The so obtained V_{ref}, then, is used in the reading blocks of the device. If the external read voltage is fixed for the various reading cycles, this will not influence the frequency of the device. Moreover, a single control block can feed more memory arrays, lending modularity to the architecture.

In Fig. 6.25 and Fig. 6.26 some DC simulation results are shown. Fig. 6.25 represents the bit-line (a) and drain-line (b) respective voltages relative to the internal bias, over a range of possible cell resistance values. It can be noticed the unavoidable voltage drop between the two nodes, due to the wire connections.

In Fig. 6.26(a) the externally-driven bit-line regulated voltage variation as a function of the cell resistance is represented. The overall variation of the regu-



(a) **(b)**

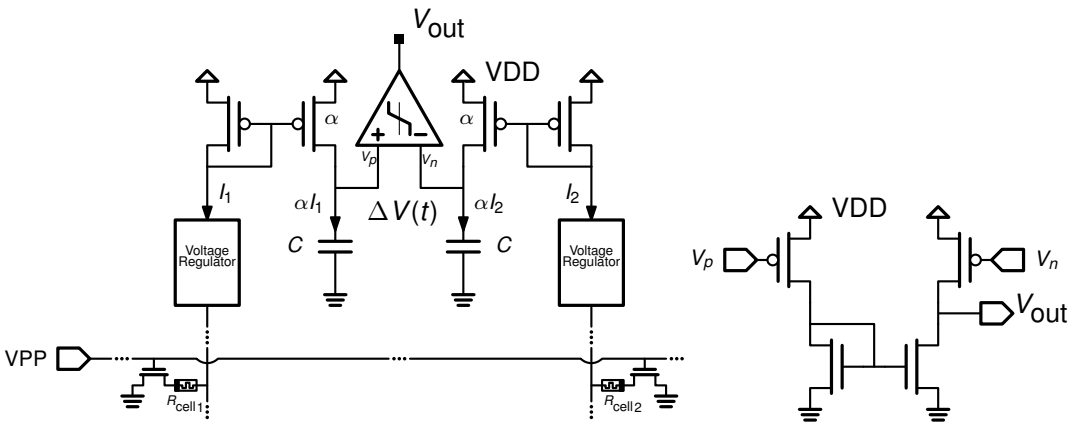
Figure 6.26: Simulation results of the regulated voltage V_{BL} over all the process corners, sweeping the resistance value R_{cell} for a $V_{read} = 200\,mV$ (a) and varying the external read voltage for $R_{cell} = 10\,k\Omega$ and $R_{cell} = 20\,k\Omega$ (b).

lated node is below 1% around a systematic error of 2.3 mV (1.15%). Beside, in Fig. 6.26(b) the possible range of read voltage is plotted.

6.4.3.2 Sensing Circuit

The current sensing and comparison, critical because of the small value of the currents, has to be converted in a digital voltage signal. Considered these aspects, the following solution has been chosen: two capacitors integrate the currents and the resulting voltage difference is sensed by a comparator. Beside, two current mirrors are used to amplify by a factor α the cell currents. In Fig. 6.27(a) a schematic of the sensing circuits is shown: the two current mirrors drain current from the voltage regulators and feed the capacitors, initially discharged; the voltages across the capacitors constantly increase in time so that a sufficient voltage difference can trigger the comparator.

For the complementary cells, the current difference is $|\Delta I| = |I_{on} - I_{off}|$ and the voltage input of the comparator is:



(a) Sensing **(b)** Comparator Schematic

Figure 6.27: Sense amplifier schematic. Cell currents sunk by the voltage regulators are amplified by a current mirror, converted into a voltage ramp by capacitors and then compared.

$$\Delta V(t) = \frac{\alpha \Delta I}{C} t \tag{6.3}$$

As it can be seen in the (6.3), small capacitance values would lead to a large gain in short integration times, hence better for shorter access times. However, a larger capacitance value would be advisable for the following reasons:

Mismatch: large capacitance values minimize the impact of the mismatch.

Saturation: fast common mode increase can saturate the output.

Critical charge: large capacitance can attenuate the impact of radiation-induced current spikes. These spikes can be eventually generated inside the n-type transistors used to precharge the capacitors.

Fig. 6.27(b) shows the comparator schematic. No latched structure has been used: the positive feedback can be triggered by spurious transitions, preventing the possibility to recover the correct value during the reading phase.

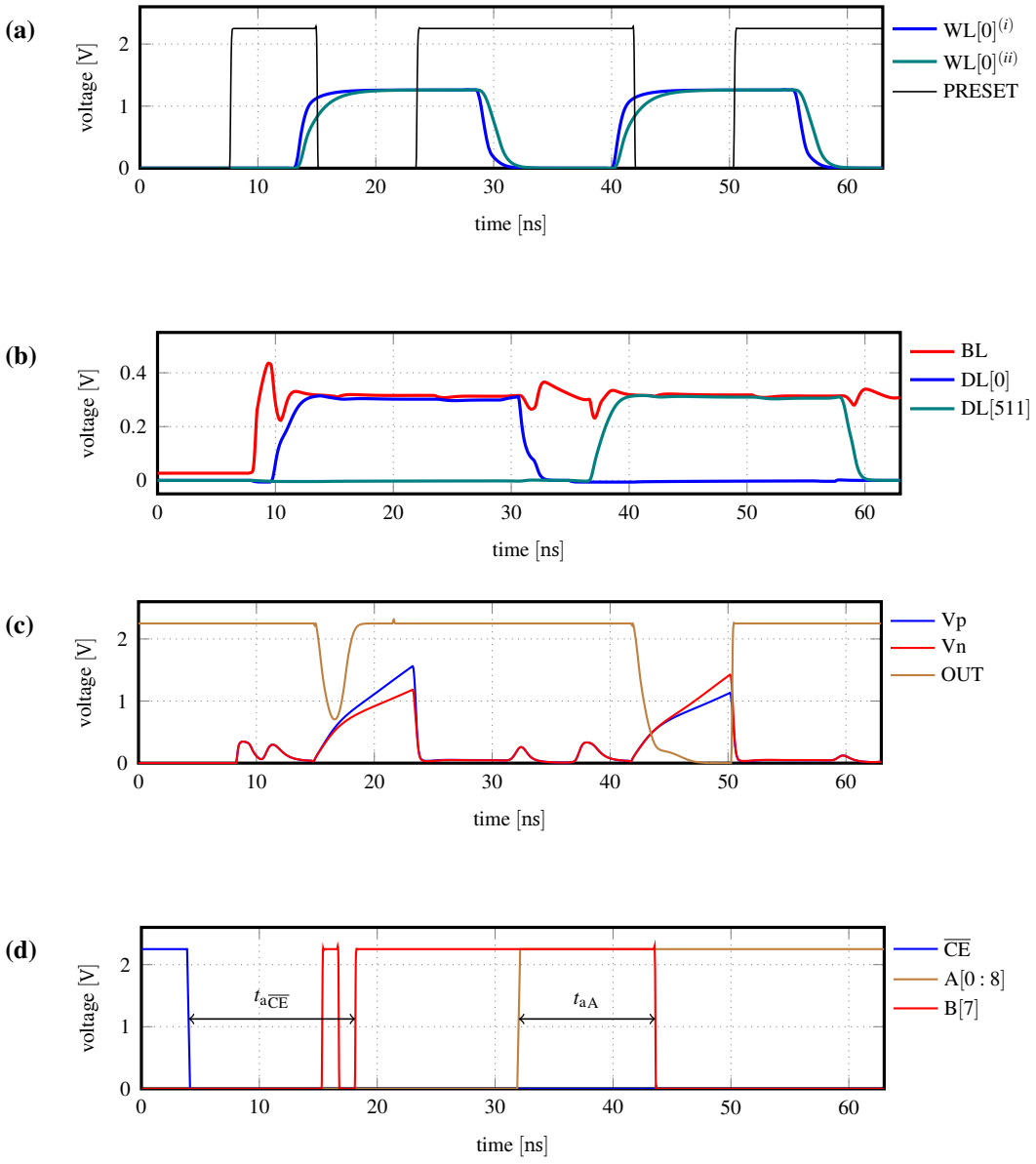
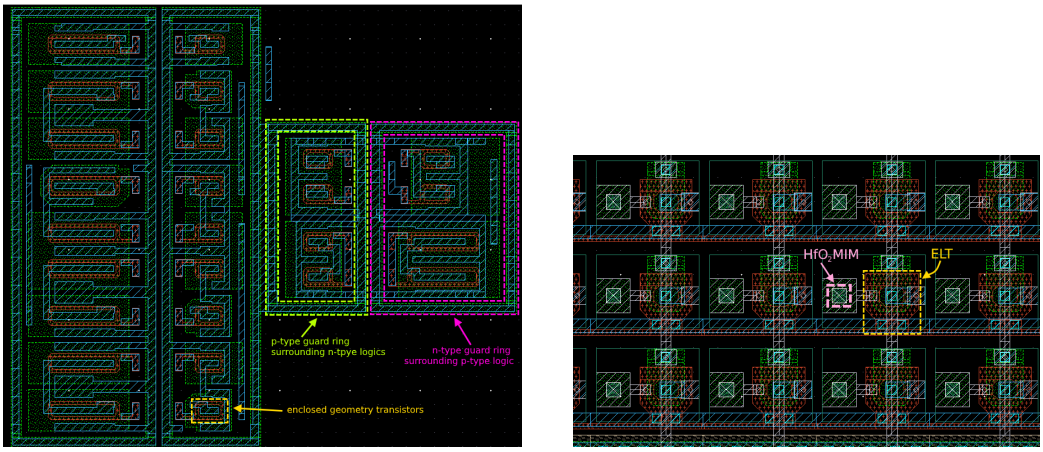


Figure 6.28: Simulation (worst case corner - wcc) of two read accesses. In the simulation two cells are accessed: first the cell at the beginning of the word-line is accessed (*i*), triggered by the *chip enable* signal ($\overline{\text{CE}}$) asserted low; then the cell at the end of the word-line (*ii*) is accessed as soon as the address input word toggles.

In Fig. 6.28 some simulated waveform for two consecutive read accesses are plotted. In particular, Fig. 6.28(a) shows the *preset* signal synchronized with the word-line assertion: the first signal turns on the regulator and preset the bit-line voltage to the target value; when the word-line is asserted, the regulator adjust the voltage according to the new load and the bit-line voltage is kept to its set-point [Fig. 6.28(b)]. Fig. 6.28(c) shows the sensing circuits capacitors that charges up, giving the peculiar ramp trend to the input voltages of the comparator. Finally, in Fig. 6.28(d), the output signal is represented: as soon as the read operation starts ($\overline{\text{CE}}$ asserted low) the output (on a bidirectional bus) dirves its formerly stored value (in the plot "0"). Then the output flips during the comparator evaluation until the final value sets to the correct output ("1").



(a) **(b)**

Figure 6.29: Layout examples. (a) Detail of the row-decoder: a 6-inputs NAND is shown. Guard rings and ELT are highlighted. (b) Detail of the memory array. ELT selectors and HfO_2 MIM are recognizable.

6.5 Radiation Hardening by Layout

The RHBD layout techniques implemented in the design layout are below summarized:

- annular transistor implementation (TID hardening);
- double guard rings (SEU hardening);

In Fig. 6.29 some layout examples are reported.

ELT geometries present some drawbacks. First of all, the annular geometry makes difficult to obtain any desired aspect ratio, as width and length size are mutually related and have also to match with the design-kit rules. For the digital blocks, for example, this means that the smallest transistor (ELT with one internal contact) that can be implemented has an effective aspect ratio of around $4.2\,\mu m/0.27\,\mu m$ with respect to the minimum size transistor provided by the 250-nm technology which has an aspect ratio of $0.33\,\mu m/0.24\,\mu m$. Actually, for a

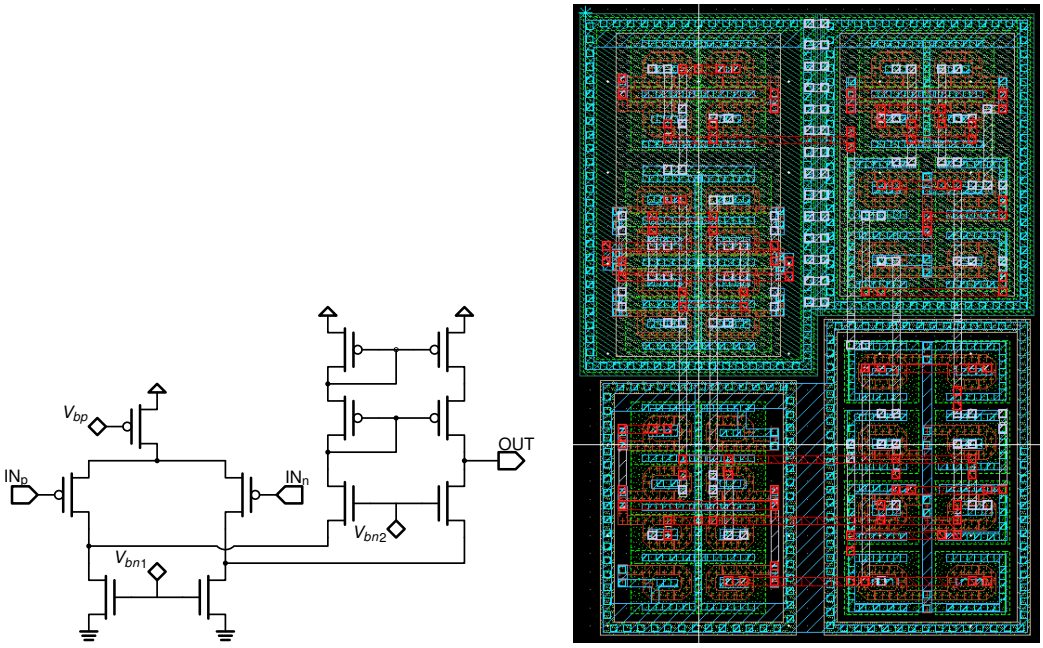


Figure 6.30: Schematic (a) and layout (b) of the folded cascode Operational Amplifier implemented with ELTs.

higher reliability, the smallest transistor used in this design is implemented with two internal contacts and has an aspect ratio of around $6.0\,\mu m/0.25\,\mu m$. It is worth to remark that the values provided for the ELT aspect ratio are not true values based on the geometrical sizes, but effective values, evaluated by the design kit tools. Many algorithms have been proposed to evaluate an effective aspect ratio whose value could provide accurate analog results. For the digital blocks, this aspect ratio issue determines higher delays and currents, as parasitics capacitance increase with the transistor sizes, while an accurate aspect ratio value is not necessary, as digital transistors work in on/off mode.

On the other hand, for analog applications, ELT geometries can arise two kind of problems. First, in analog circuits a good accuracy is necessary to determine the

correct operating point of the circuit and this can considerably affect the circuit performances. Then, with the annular geometry, a larger gate is not obtainable without increasing its width as well. In Fig. 6.30 the schematic and layout of an Operational Amplifier have been shown.

The chosen configuration is a folded cascode operational amplifier. Advisable transistor lengths should be larger to improve mismatch and output resistances (higher gain). In particular, for the output active load, a cascode configuration is necessary, because of the geometrical constraints discussed above.

For an optimal match, a common centroid configuration has been implemented, which presents a more complex connection also due to the use of the enclosed geometries.

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Chapter 7

Experimental Results

7.1 The Chip Implementation

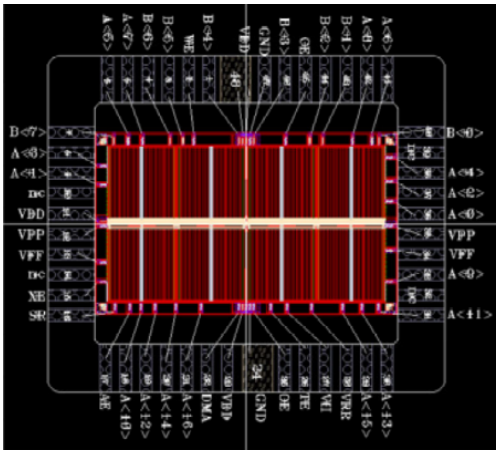


Figure 7.1: Bonding diagram of the 1 Mbit chip for a DIL 48 package.

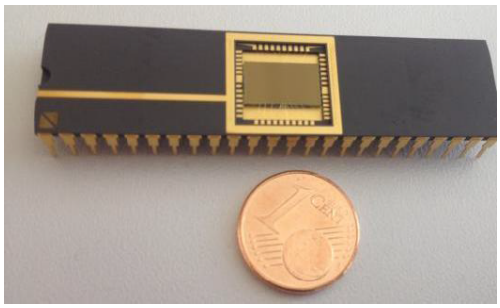
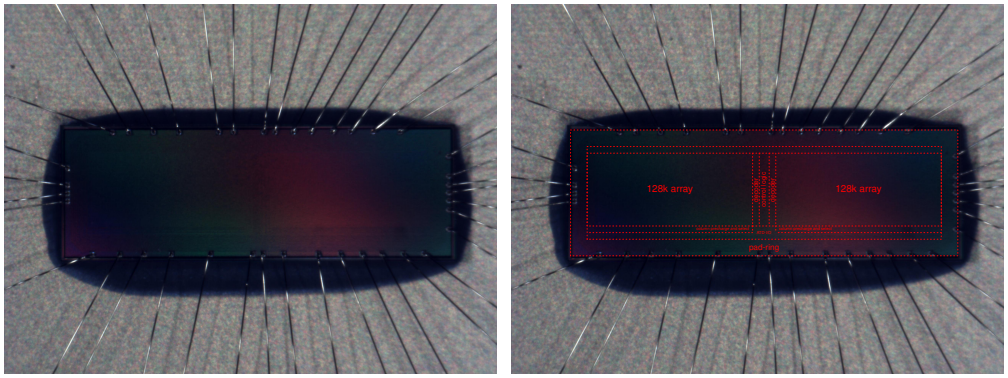


Figure 7.2: Demonstrator assembled into a DIL 48 package, [7.1].

THE 1-Mbit memory chip has been implemented as a stand alone device. The die has been assembled in a standard ceramic DIL48 package, according to the bonding diagram shown in Fig. 7.1. A picture of the assembled die is shown in Fig. 7.2, [7.1].



(a) **(b)**

Figure 7.3: Photography of the stand alone 128 kbit device (a) and highlighting of the functional blocks (a).

Fig. 7.3 shows a photography of a 128 kbit implementation of the device. Functional blocks, barely recognizable for the metal filler layers, are highlighted in Fig. 7.3(a).

7.2 Radiation Test Campaign Overview

An exhaustive test campaign has been carried out to investigate the impact of radiations on the functionality and reliability of the ReRAM 1-Mbit chips. The tests have been conducted thanks to the contribution of the RedCat Devices team and researchers from University of Calabria in the facilities of the Department of Physics of the University of Jyväskylä (Finland). The test station includes of a vacuum chamber and is provided with adequate equipments to control, during the irradiation, the beam quality and intensity by mean of physical parameters like flux, fluence, total dose and beam homogeneity.

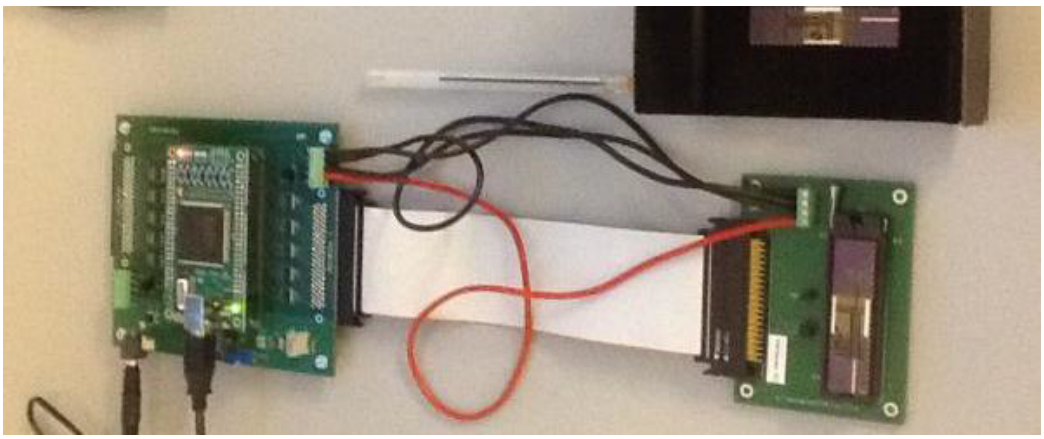


Figure 7.4: Setup board for the 1 Mbit test vehicle, [7.1].

7.2.1 Equipment Setup

The setup equipment, developed by RedCat Devices, is composed by a mother board hosting a Xilinx Spartan 3 FPGA, necessary to drive the control signals, and daughter boards connected via flat cable (Fig. 7.4). With this configuration the standard (non rad-hard) active components on the mother board can be properly shielded during the radiation exposure of the device under test (DUT), placed on the daughter board. A USB connection is used to connect the board equipment to a Personal Computer (PC) (Fig. 7.5).

7.2.2 Description of the Radiation Tests

In order to fully characterize the behavior of the device under radiation, two main kind of experiments have been carried out:

- test of single event failures under exposure to high energy radiations, in particular heavy ions and protons;
- test of cumulative effects under exposure to ^{60}Co.

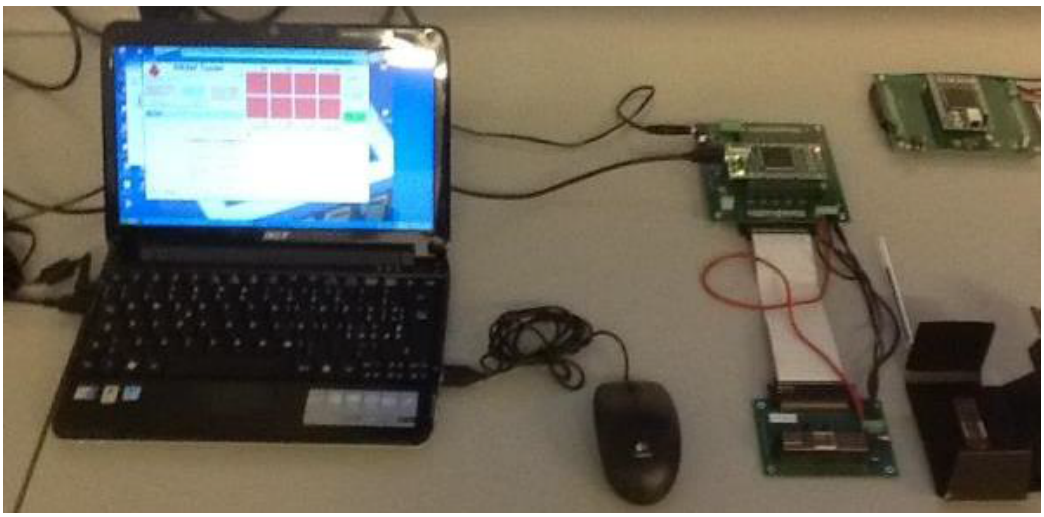


Figure 7.5: Setup board connection via USB to laptop PC, [7.1].

The electric and functional integrity of the DUTs have been preemptively validated in standard environment.

For the SEE investigation the devices have been exposed to high energy Xe ions and proton beams and their integrity under radiations has been checked before and after diverse write and erase cycles.

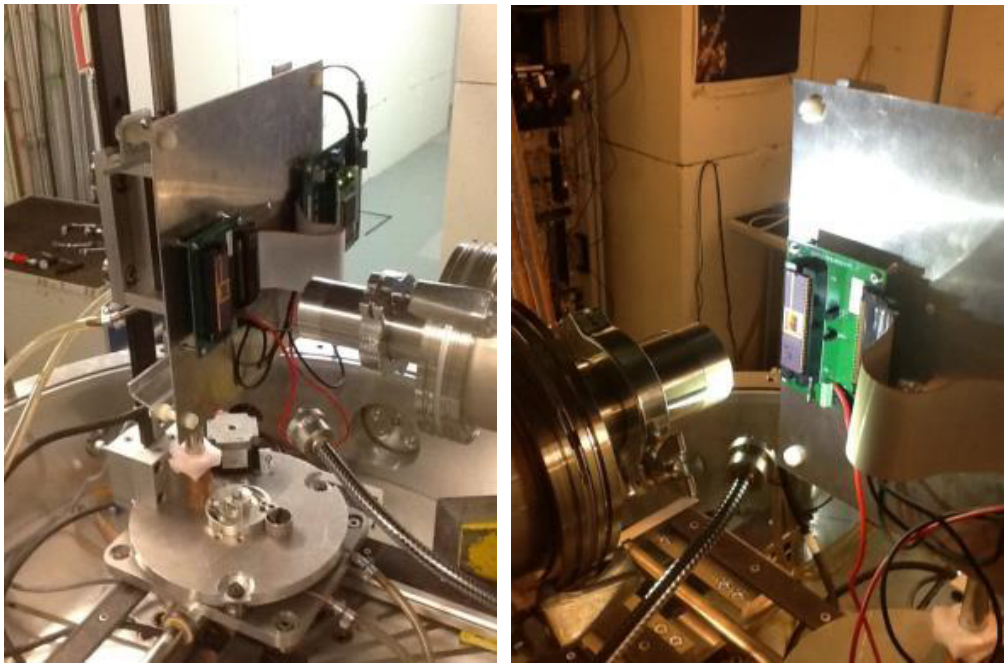
On the other hand, the effects of the TID have been analyzed by recursively checking the stored values of DUTs continuously exposed to ionizing radiations.

7.3 Single Event Tests

7.3.1 Heavy Ion Test

In Fig. 7.6 it is possible to see the test setup for DUT exposure to heavy ions and the list of the DUTs is presented in Tab. 7.1.

The characteristics of the ion beams are listed in Tab. 7.2, while in Tab. 7.3 are listed the different functional tests performed under exposure, with their relative duration and ion fluence.



(a) **(b)**

Figure 7.6: Board positioning for ion beam, [7.1].

Dev. Id.	DUT Description
V2#2	written with known pattern
V3#1	un-formed device
V3#2	un-formed device
V3#3	un-formed device

Table 7.1: DUT description.

Ion	Energy (E)	Beam Radius (R)	LET	Temperature
Xe	1217 MeV	89 µm	60 MeVmg^{-1} cm^{-2}	Room Temperature

Table 7.2: Heavy ion Characteristics

#	Average Flux [cts s^{-1} cm^{-2}]	Fluence [cm^{-2}]	DUT	Operative Condition
1	9848.8	1.00×10^6	V2#2	stand-by ($\overline{CE}$=H)
2	9887.2	1.01×10^6	V2#2	read cycles
3	9627.2	1.01×10^6	V2#2	write cycles
4	9527.9	1.01×10^6	V2#2	stand-by ($\overline{CE}$=L)
5	9364.5	7.38×10^6	V2#2	read cycles - complete scan
6	9161.5	9.00×10^6	V2#2	write cycles
7	9458.8	9.00×10^6	V3#1	stand-by ($\overline{CE}$=L)
8	10801.2	9.01×10^6	V3#2	read cycles
9	9437.8	9.01×10^6	V3#3	read cycles - complete scan

Table 7.3: Heavy ion test list.

In Fig. 7.7 is plotted an example of heavy ion flux monitoring.

7.3.2 Proton Test

The DUTs are listed in Tab. 7.4 have been exposed to proton beams according th the test setup of Fig. 7.8.

Analogously to the heavy ion case, we report the the proton beams' character-

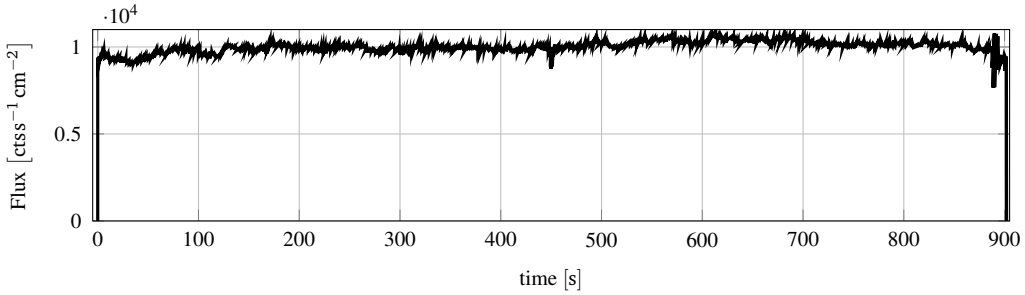


Figure 7.7: Example of heavy ion flux during a test cycle, [7.1].

(a) **(b)**

Figure 7.8: Board positioning for proton beam, [7.1].

Dev. Id.	DUT Description
V2#1	written with known pattern
V3#4	un-formed device
V3#5	un-formed device

Table 7.4: DUT description.

Energy (E)	Beam Radius (R)	LET	Temperature
52 MeV	0.0 µm	0.0 MeVmg^{-1} cm^{-2}	Room Temperature

Table 7.5: Proton Beam Characteristics.

#	Average Flux [cts s^{-1} cm^{-2}]	Fluence [cm^{-2}]	DUT	Operative Condition
1	1.8×10^8	1.01×10^{11}	V2#1	read cycles
2	1.8×10^8	1.01×10^{11}	V3#4	read cycles
3	1.8×10^8	1.00×10^{11}	V3#5	read cycles

Table 7.6: Proton test list.

istics in Tab. 7.5 and the functional test list in Tab. 7.6.

Fig. 7.9 plots a typical proton flux evolution in time.

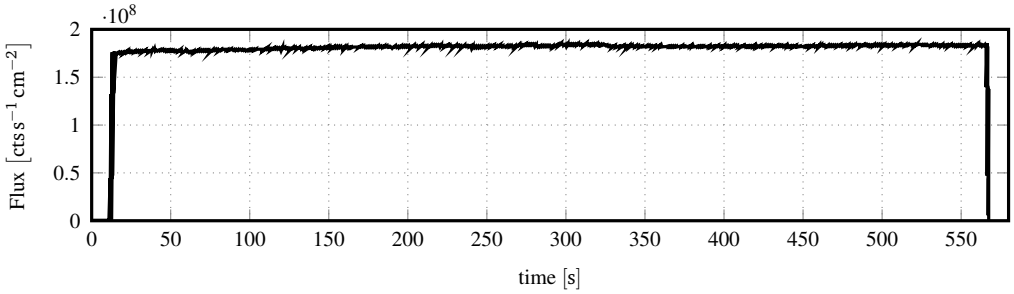
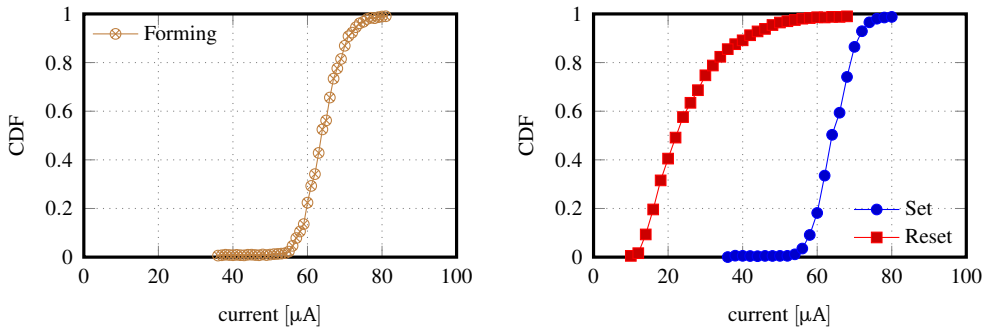


Figure 7.9: Example of proton flux during a test cycle, [7.1].

7.4 Heavy Ion and Proton Radiation Effects on the ReRAM Array

7.4.1 Radiation Effects on Memristive Cells

The CDF in Fig. 7.10.(a) demonstrates the forming process of the devices with a common compliance current I_{CC} of about 100 µA (corresponding to a gate voltage of 1.4 V). After the electroforming process step, all devices demonstrate resistive switching (RS) behaviors. As illustrated in Fig. 7.10(b), the un-irradiated RRAM array is characterized by HRS and LRS states.

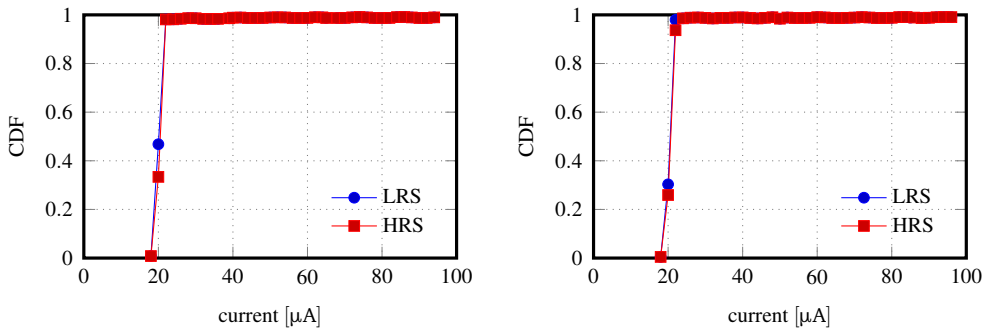


(a) electroforming **(b)** set/reset

Figure 7.10: CDF of forming and HRS/LRS currents (after the first set and reset process).

7.4.1.1 Ionization-Induced SEUs

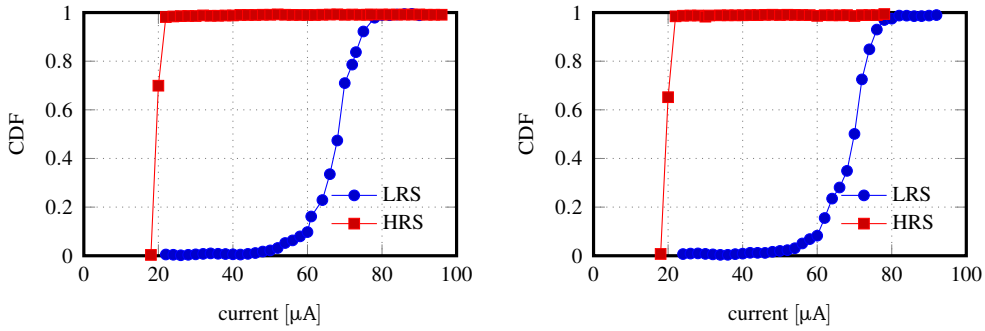
The 1Mbit chips were irradiated by Xenon ions and protons with all terminals left floating. After the exposure of a high fluence of 1011 cm^{-2} at 52 MeV (protons) and 106 cm^{-2} 1200 MeV (Xenon) for 9 and 15 min, respectively, the LRS states of all cells were switched to HRS, as illustrated in Fig. 7.11. Moreover, the distribution of the HRS states is strongly reduced.



(a) Xe ions **(b)** protons

Figure 7.11: CDFs of HRS and LRS states after irradiation with Xenon ions (a) and protons (b).

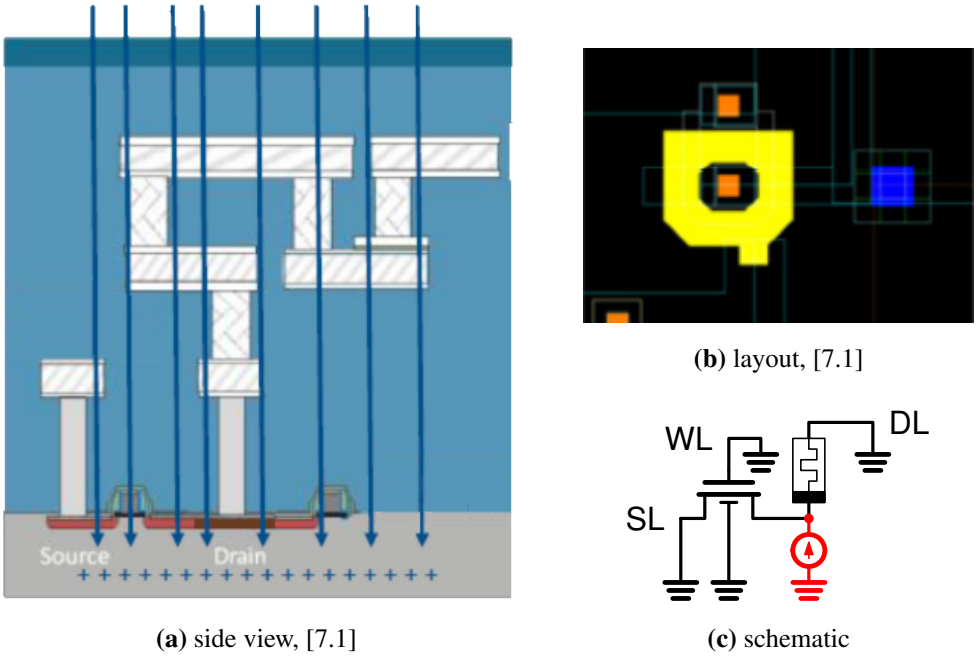
After the readout procedure, the LRS states could be recovered completely by a standard set process, as shown in Fig. 7.12.



(a) **(b)**

Figure 7.12: Post irradiation cycling: recovered CDFs of HRS and LRS states after irradiation with Xenon ions (a) and protons (b).

Caused by the high energies of the Xenon ions and protons, the species have stopped in the bulk silicon, generating free charge. A side-view scheme of the layers is represented in Fig. 7.13(a). At large proton and Xenon fluence, the generated charge below the ELT ring, marked in yellow in the layout scheme presented in



(a) side view, [7.1]

(b) layout, [7.1]

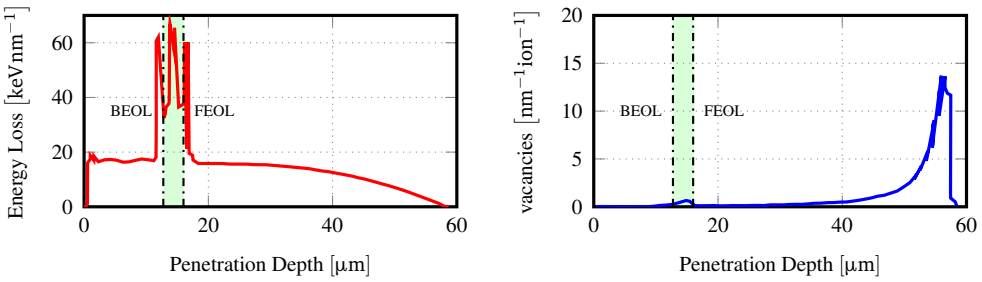
(c) schematic

Figure 7.13: Representation of the high energy particle damage induced in the device.

Fig. 7.13(b), has induced current spikes whose action could be comparable to the standard reset procedure, as schematized in Fig. 7.13(c). These spikes, applied for a sufficient time (minutes) destroyed the filament and switched the cells to the HRS state.

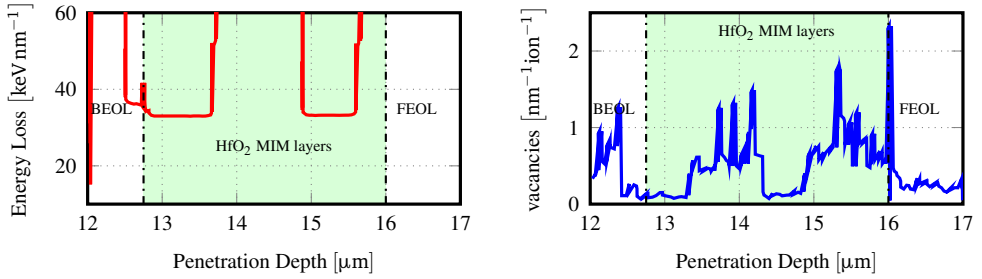
A quantitative estimation of the energy lost by the heavy ions and their penetration depth distributions after the stop within the memory chip can be simulated by the software STRIM, [7.2], using as input all the layer information related to the 250-nm technology used. Energy loss of Xenon ions and protons are illustrated in Fig. 7.14. As it can be noticed from the pictures, most of the ions are stopped deep in the silicon wafer, resulting in the highest number of atom displacements (or vacancies) by energetic collisions far away from the resistive MIM cell.

The induced damage in the back end of line (BEOL) area next to the resistive MIM cell is enlarged in Fig. 7.15. The energy loss peaks of the Xenon ions, illus-



(a) energy loss **(b)** recoiling vacancies

Figure 7.14: SRIM estimated energy loss and vacancies recoils for Xenon ions within the memory device.

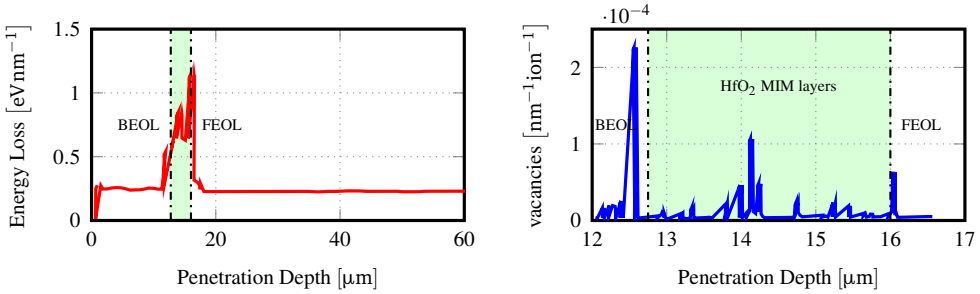


(a) energy loss **(b)** recoiling vacancies

Figure 7.15: SRIM estimations for Xenon ions. Zoom of the HfO_2 layer.

trated in Fig. 7.15(a), are mainly located in corrispondence of the Tungsten vias connected to the MIM cells. Therefore, as highlited in Fig. 7.15(b), the number of created vacancies is much larger in these via plugs. The number of created vacancies in the HfO_2 is about 0.25 $nm^{-1}ion^{-1}$. Taking into account the fluence of 107 cm^{-2} with HfO_2 thickness of 6 nm, the number of created vacancies by recoils is about 0.075 per MIM cell. That means, every 13th cell is damaged by Xenon ions.

Energy loss of proton ions after penetrating the memory chip is illustrated in Fig. 7.16. In contrast to the Xenon ions, the protons transit the memory chip with-



(a) energy loss

(b) recoiling vacancies (HfO_2 layers zoom).

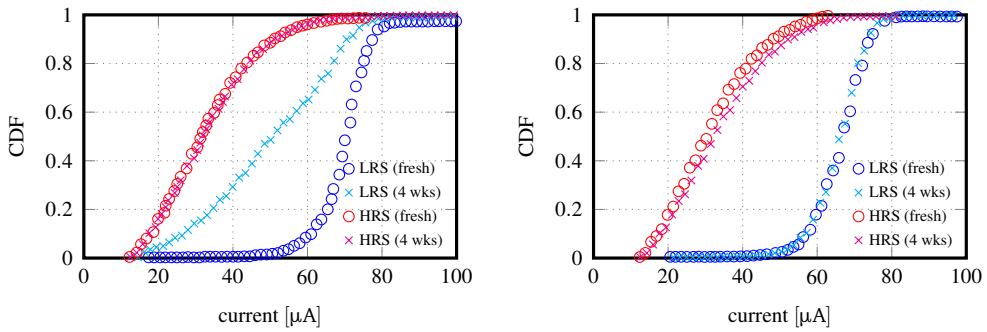
Figure 7.16: SRIM estimations for Protons. Vacancies have been zoomed in the HfO_2 layer.

out losing a huge amount of energy, as depicted in Fig. 7.16(a). Accordingly, the number of created defects is much smaller. Comparable to the impact of Xenon ions, the protons lost their energy mainly in the Tungsten vias. The number of created vacancies in the HfO_2 is about $0.000\,25\,\text{proton}^{-1}\text{nm}^{-1}$. Taking into account the fluence of $1011\,\text{cm}^{-2}$ and the HfO_2 thickness of 6 nm, the number of created vacancies by recoils is about 0.75 per MIM cell, meaning that almost every cell should be affected by protons.

7.4.1.2 Ionization-Induced Long-Term Damage

In order to evaluate the long term damage caused by high energy radiations, fresh unformed devices were irradiated, formed and successively switched to the HRS and LRS state . Then, their LRS and HRS distributions after 4 weeks of retention have been measured, as illustrated in Fig. 7.17.

As illustrated in Fig. 7.17(b), there is no long term effect of the proton irradiation. On the contrary, the high energy irradiation with Xenon ions leads to a long term degradation of the LRS. A possible reason of this degradation could be found in ionization-induced displacement damages of the HfO_2 film. These damages act



(a) Xe ions **(b)** protons

Figure 7.17: CDFs of devices soon after irradiation and after 4 weeks.

as attractive trap centers for oxygen vacancies that are subtracted to the filament.

7.5 TID Characterization

The measurement setup for the TID functional tests is shown in Fig. 7.18

(a) **(b)**

Figure 7.18: TID measurement setup, [7.1].

As it can be seen, the daughter-board hosting the device is placed close to the ^{60}Co source, with the rest of the connected measurement devices conveniently shielded.

7.5.1 TID Effects on ELT Selectors

The drain current versus gate voltage characteristics after irradiation of the ELT is illustrated in Fig. 7.19. The leakages are almost unaffected during the TID irradiation up to 750 krad.

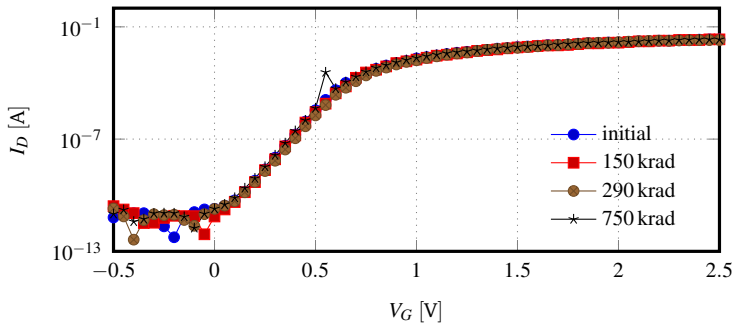


Figure 7.19: Before and after irradiation I-V characteristics of the 1T-1R cell ELTs, [7.1].

7.5.2 TID Functional Tests

In total, 2048 resistive 1T-1R cells were tested: arrays of 16x16 cells have been sequentially scanned by applying 100 ms read pulses. Fig. 7.20 illustrates measurements for all 8 blocks. In left arrays "ones" have been stored, while, complementary, right arrays store all "zeros".

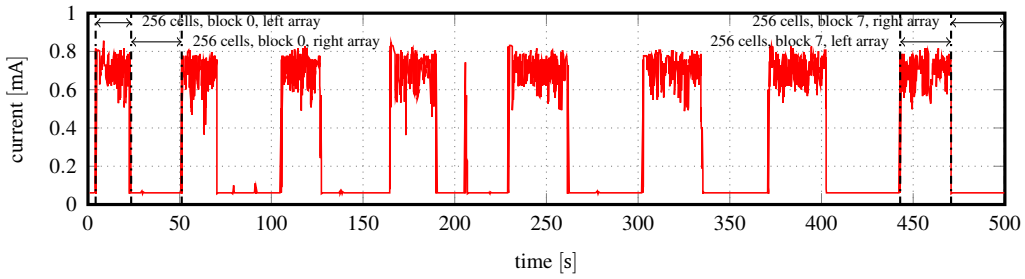
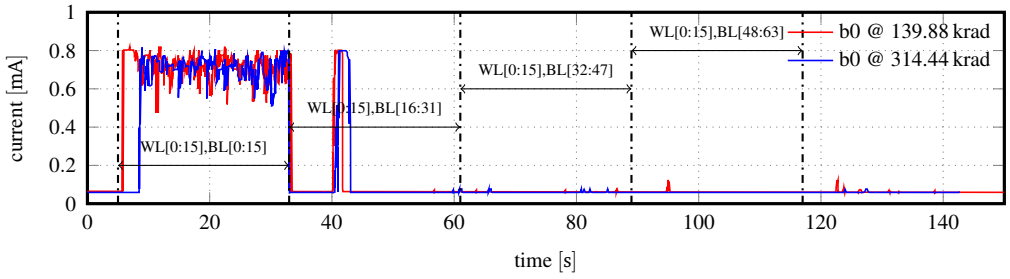
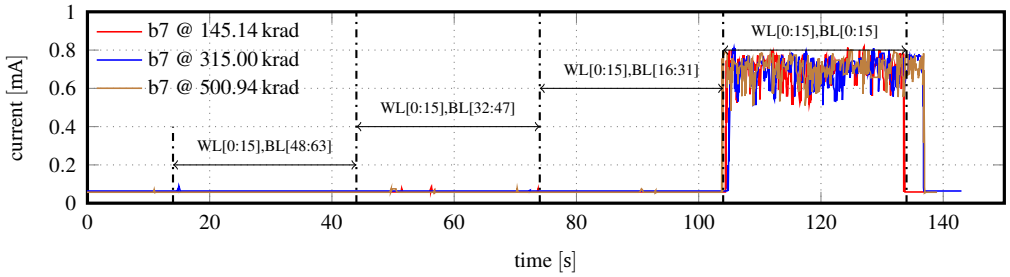


Figure 7.20: Example of a read scan of the resistive cells, [7.1]. All 8 blocks are scanned. Results refers to an exposure of 134.31 krad.

The TID absorbed can result in device failures. Satellites and space probes typically encounter TIDs between 10 and 100 krad. In this measurements, the dose has been ramped up to 500 krad, without any loss of data, as illustrated in the following figures. In Fig. 7.21 are illustrated the measured currents relative to the 2 kbit portions examined. As it can be noticed, data are retained without any kind of sensible degrade in the resistive state.



(a) Block 0



(b) Block 1

Figure 7.21: Read results relative to the block 0 (a) and block 1 (b), [7.1].

Bibliography

[7.1] C. Wenger, C. Calligaro, C. Zambelli, P. Olivo, C. Pace, F. Crupi, and A. Virtanen. R2RAM 640073 Project - Radiation Hard Resistive Random-Access Memory. Technical Report Ares(2017)907301, European Commission - Community Research and Development Information Service (CORDIS), 2017.

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Chapter 8

Conclusions

THIS work has demonstrated that resistive memories can be a valid candidate for space applications. Obviously, the effectiveness of this technological choice relies on a suitable radiation hardened design of the digital and analog periphery of the device. The critical point of the discussed design is the match of two peculiar technical areas, i.e., the radiation effect hardening on semiconductors and the emerging technologies for NVMs.

On one side, radiation hardening by design techniques, strong in the technological advances of the last decade, have consolidated as a reliable design paradigm for space applications, characterized by clear and precise design choices.

On the other side, emerging memories have only recently reached a engineering level suitable for market applications, mainly, by reason of a slow establishment of systematic design styles. Case- and technology-specific solutions have been so far preferred, indicating a lack of reliable and general electrical models for the memristor devices.

In our approach, as discussed in Section 4.3.2, a linear-based approximated model has been proposed, as simulation speed and numerical reliability were necessary to accomplish the full functional design of the device. Moreover, some of

the architectural solutions presented in Chapter 6, such as the column decoding management, arise from a compromise between radiation hardening and technological requirements. In particular, in Section 6.4.2.2 we have presented a case in which some area occupation issues, introduced by RHBD implementations had to be solved by a proper management of the operating phases (proper precharge and write approach).

Beside this, it has to be remarked the high complexity level of the read architecture, necessary to ensure to the device a confident degree of versatility, necessary to face the high variability of the oxide resistive technological process.

Nevertheless, as demonstrated in Chapter 7, the device has kept its full functional integrity under both the action of high energy particles and radiation total ionizing dose. With respect to Flash memories, that barely reach TID values under 100 krad, our implemented ReRAM device has proven TID robustness up to 750 krad and no irreversible damage after 1.2 GeV Xenon ions and 52 MeV protons exposure.

Overall, this project has shown the many possibilities in the frame of emerging memories for space applications, as much the many improvement margins necessary to gain a good technology maturity.

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List Of Acronyms

1D-1R 1-Diode/1-Resistor

1T-1R 1-Transistor/1-Resistor

ATD address transition detection

BEOL back end of line

BJT Bipolar Junction Transistor

BRS bipolar resistive switching

CDF cumulative distribution function

CF conductive filament

CG control gate

CME Coronal Mass Ejection

COS/MOS complementary-symmetry MOS

CR Cosmic Ray

DD displacement damage

DMA direct memory access

DRAM Dynamic RAM

DUT device under test

ECC error correction code

ELT Edge-Less Transistor

EMC Electromagnetic Compatibility

EPROM erasable programmable read only memory

FET field effect transistor

FG floating gate

FOX field oxide

GCR Galactic Cosmic Ray

GMR giant magneto-resistance

HEP electron-hole pair

HRS High Resistive State

IMP ionized metal plasma

ISPVA incremental step pulses with verify algorithms

LET Linear Energy Transfer

LOCOS local oxidation on silicon

LRS Low Resistive State

MBU Multiple Bit Upset

MIM metal-insulator-metal

MOS Metal-Oxide-Semiconductor

MRAM Magnetic RAM

MU measure unit

NVM non-volatile memory

ONO Oxide Nitride Oxide

OTP one time programmable

OxRRAM oxide resistive RAM

PC Personal Computer

PCM phase change memory

PMA post-metallization annealing

PWL piece-wise linear

ReRAM Resistive RAM

RHBD Radiation Hardening By Design

RILC radiation-induced leakage current

RRAM resistive RAM

RS resistive switching

SEE Single Event Effect

SEFI Single Event Functional Interrupt

SEGR Single Event Gate Rupture

SEL Single Event Latch-up

SET Single Event Transient

SEU Single Event Upset

SEU Single Event Upset

SHE Single Event Hard Error

SLC Single Level Cell

SOI Silicon On Insulator

SOS Silicon On Sapphire

SRAM Static RAM

STI shallow trench insulation

STT-MRAM spin transfer torqe MRAM

TAS-MRAM thermal assisted switching MRAM

TEM transmission electron microscopy

TID Total Ionizing Dose

VM volatile memory

VMRAM vertical transport MRAM

WaV write and verify