# SIMO DC-DC Converter for Automotive Audio Amplifier

A Ph.D. Thesis by
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*To*
*My Parents*

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# Abstract

Modern auto industry is ubiquitously deploying electronic systems for several applications like control, infotainment and security among others in the vehicles. Automotive infotainment is a key segment for the growth of automotive electronics as the vehicles, both light and heavy, require radio, video, navigation-assistance and telematics systems for both entertainment and networking.

Like any battery-operated systems, the automotive infotainment systems are required to provide high efficiency. One major constituent of in-vehicle infotainment being the radio, improving the overall efficiency of a car radio system is emphasized by the industry. In the state-of-the-art, the automotive audio amplifiers severely lack efficiency offering $< 40\%$ in the mute condition. This research targets to improve the overall efficiency of an audio amplifier in a car radio by power supplying efficiently.

A Single Inductor Multiple Output dc-dc converter is explored as a supply voltage generator for an automotive audio amplifier in a car radio. The presence of line and load fluctuations, together with wide range of operating temperatures, in the automotive environment pose major challenge to the voltage regulation. A systematic feasibility study and analysis of specifications brought out the equivalence between the target SIMO converter and a non-inverting buck-boost SISO converter. Based on the equivalence, equilibrium and small signal models for the SIMO converter

are developed. A voltage-mode, error-based controller is designed to control the dynamics of the converter. A novel power switching stage is conceived to generate the supplies required in a multi-channel class-D power amplifier. The switch configuration is critical due the absence of a well-defined reference to one of the regulated outputs and the effect of package parasitics at high switching frequencies. The converter is charged synchronously and discharged quasi-synchronously to the loads. The switches are configured and driven optimally based on extensive simulations in the presence of package models to suppress the switching noise. In order to reduce the EM interference in the AM band of interest, the SIMO converter is switched at permissible high frequencies based on the EMI mask.

The automotive-class SIMO dc-dc converter is designed and integrated with a state-of-the-art class-D audio amplifier using 110-nm BCD process technology offered by STMicroelectronics. The SIMO converter provides a battery tracking boost and a ground referred buck outputs for driving the class-D power stage. A unique feature of the converter is the generation of a floating voltage across half battery to supply the DSP core of the amplifier. The converter starts-up as boost converter alone followed entering boost-assisted SIMO converter mode. The active area occupied is 2.5 $mm^2$. The switching frequency is 2-2.4 MHz. The converter has a load capability to drive up to 4 channels of a class-D power stage with peak efficiency of 86% and peak output power of 2.8 W. The ripple voltage on the regulated outputs is below 25 mV. The SIMO converter is able to sustain the automotive battery crank and dump conditions across the battery variation range of 4.5-27 V. A line regulation of 6.3-16.2 mV/V and a load regulation of 0.16 mV/mA are provided by the SIMO converter. In the presence of wide range of battery variations, the SIMO converter incorporates all the necessary protections circuits and under/over voltage interrupts through $I^2C$ communication.

# Sommario

L'industria dell'auto sta evolvendo sempre più rapidamente nella direzione di avere a bordo dei veicoli sempre più sistemi elettronici per diverse applicazioni come il controllo del veicolo stesso, l'infotainment e la sicurezza. L'infotainment è un segmento chiave per la crescita dell'elettronica automobilistica in quanto i veicoli, sia leggeri che pesanti, richiedono sistemi radio, video, di assistenza alla navigazione e telematici per l'intrattenimento e il networking.

Come ogni sistema alimentato a batteria, i sistemi di infotainment automobilistici sono tenuti a fornire un'elevata efficienza di potenza. Uno dei principali componenti dell'infotainment a bordo del veicolo è la radio. Allo stato dell'arte, gli amplificatori audio per autoveicoli sono generalmente piuttosto inefficienti, riportando un'efficienza di potenza inferiore a 40% quando il volume viene messo in muto. Questo lavoro di ricerca mira a migliorare l'efficienza complessiva di un'autoradio, utilizzando un generatore di tensione di alimentazione efficiente in termini di potenza.

Questo lavoro di tesi si concentra sulla progettazione di un convertitore DC-DC a singolo induttore e uscita multipla (SIMO) da utilizzare come alimentatore per un amplificatore audio. La presenza di fluttuazioni della batteria e del carico, assieme ad un'ampia gamma di temperature di esercizio rappresentano una grande sfida per

la regolazione di tensione. Uno studio di fattibilità sistematico e l'analisi delle specifiche hanno evidenziato l'equivalenza tra il convertitore SIMO oggetto di questo progetto e un convertitore SISO (a singolo induttore e uscita singola) di tipo buck-boost non invertente. Sulla base di questa equivalenza, il convertitore SIMO è stato modellizzato sia per grandi che per piccoli segnali. Il loop di controllo del convertitore è stato implementato in tensione. Uno stadio di potenza non convenzionale è stato concepito per generare tutte le tensioni necessarie per il funzionamento di un amplificatore di potenza in classe D multicanale. La progettazione degli interruttori è critica a causa dell'assenza di un riferimento ben definito a una delle uscite regolate e a causa dell'effetto dei parassiti introdotti dal package ad alte frequenze di commutazione. L'induttore viene caricato in modo sincrono e scaricato in maniera quasi-sincrona verso i carichi. Al fine di ridurre le interferenze elettromagnetiche (EM) nella banda AM di interesse, il convertitore SIMO viene commutato ad una frequenza relativamente alta, compatibile con le maschere EM fornite.

Il convertitore DC-DC SIMO è progettato e integrato con un amplificatore audio in classe D all'avanguardia. Il dispositivo è stato fabbricato con una tecnologia BCD a 110-nm offerta da STMicroelectronics. Il convertitore SIMO fornisce una tensione di tipo boost capace di inseguire le fluttuazioni della batteria e un?uscita di tipo buck riferita a massa. Queste due uscite sono impiegate per il pilotaggio dello stadio di potenza in classe D. Inoltre, una caratteristica unica del convertitore è la generazione di una tensione floating a cavallo di metà della tensione di batteria per alimentare la parte digitale dell'amplificatore. L'area di silicio occupata dal dispositivo è di soli 2,5 $mm^2$. Il convertitore SIMO richiede un condensatore di filtro da 10 μF ad ogni uscita e un induttore esterno da 10 μH. La frequenza di commutazione è 2-2,4 MHz. Il convertitore può pilotare fino a 4 canali con un'efficienza di picco pari a 86% erogando una potenza di uscita di picco di 2,8 W. La tensione di ripple sulle uscite regolate è inferiore a 25 mV in tutti i casi. Il convertitore SIMO è in

grado di sostenere variazioni (anche brusche) del valore della batteria nel range 4,5-27 V. La line regulation misurata è di 6.3-16.2 mV/V, mentre la load regulation misurata è di 0.16 mV/mA. Il convertitore SIMO include tutti i circuiti di protezione da sovratensioni e sovracorrenti necessari e comunica attraverso il protocollo $I^2C$.

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# Chapter 1

# Introduction

The in-car electronics landscape is rapidly expanding as the electronically controlled subsystems are increasingly pervading the vehicles. Continued semiconductor demand is expected in each of the main areas of the vehicle such as powertrain, body electronics, comfort electronics and infotainment. The automotive semiconductor market value is projected to be at $ 43 billion in 2023 [1]. Experts see the in-car infotainment as a key growth driver, which includes audio, radio, navigation and telematics.

As the infotainment systems add more features, the audio power budgets are being pushed to the limit. Consequently, high performing, efficient audio solutions are sought. In high-end vehicles, multi-channel and multi-speaker systems require high audio amplification and low distortion. These requirements are conventionally met by (i) increasing channels driven by the audio amplifier, (ii) raising the supply voltage using DC-DC converters, (iii) lowering the output speaker impedance. However all these techniques result in increased power dissipation. Hence, efficient audio amplifiers are critical in the state-of-the-art car-radio systems.

Owing to their far superior efficiency, class-D audio amplifiers are the sought after solutions to maintain the power budget under control yet process high quality audio. Basically, class-Ds are switchers. They require special design considerations

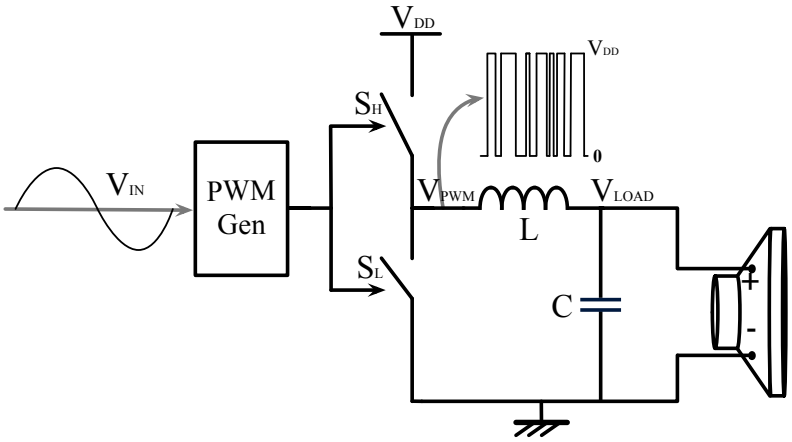


**Fig. 1.1** Principle of a Class-D Amplifier.

and consequently give rise to cost vs. performance trade-off in comparison with the conventional class-AB amplifiers. The following section overviews briefly the class- D audio amplifier system and highlights the application specific challenges and motivation for the thesis.

## 1.1 Overview of the application

The basic principle of class-D operation is shown in Fig. 1.1 [2, 3]. The audio signal in digital or analog format is modulated into a PWM signal, which drives the output power switches. The output of the power stage is low-pass filtered externally to retrieve the analog signal and feed the speaker load.

Fig. 1.2 shows a block level representation of a modern, automotive class-D audio amplifier system. The system consists of n-channels at the output power stage together with the corresponding drivers, the analog processor for pulse width modulation (PWM) of the audio signal, a digital core for digital signal processing (DSP)

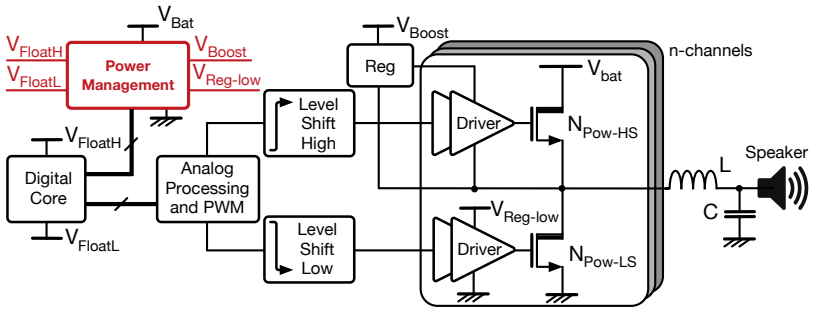


**Fig. 1.2** Automotive class-D audio amplifier system.

and the power management block to provide regulated supplies to each of these stages of audio signal processing. An automotive battery ($V_{Bat}$) powers the entire system. In order to improve the signal to noise ratio (SNR), the analog signal processing and the DSP operations are performed at $V_{Bat}/2$.

Each channel in the power stage is composed of two n-channel, drain- extended metal-oxide-semiconductor (N-DMOS) transistors. The choice of N-DMOS transistors is underscored by the reduced gate-capacitance ($C_G$) as well as on- resistance-area product ($R_{ON}$*A) of the device [4]. A regulated driver drives each switch. In order to drive the high-side switch $N_{P\text{-}HS}$, the driver requires a voltage $V_{Boost}$ that exceeds $V_{Bat}$ by the gate-source voltage ($V_{GS}$) of $N_{P\text{-}HS}$. Conventionally, $V_{Boost}$ is generated using a bootstrap capacitor. $V_{Reg\text{-}low}$ supplies the low side driver. The floating supplies, $V_{FloatH}$ and $V_{FloatL}$ across $V_{Bat}/2$, are required to supply the digital core in the class-D audio power amplifier system in Fig. 1.2.

The immediate challenge arising in a car radio system is the battery profile. The automotive batteries are plagued by sharp variations, both rise and dip. A typical automotive battery profile is shown in Fig. 2.1. The conditions known as cold- crank and load-dump may result in the nominal $V_{Bat}$ to vary by multiples. The car radio system is required to function immune to $V_{Bat}$ excursions and output audio without

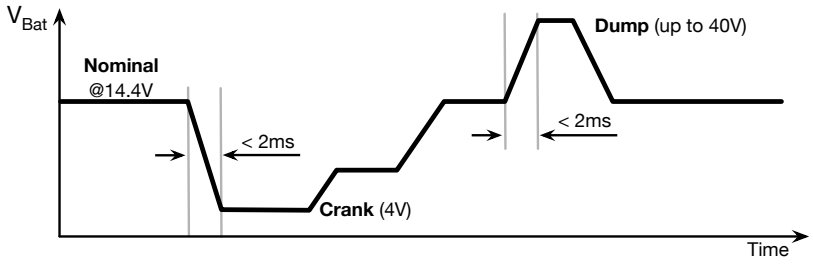


**Fig. 1.3** Profile of an automotive battery showing cold-crank and dump.

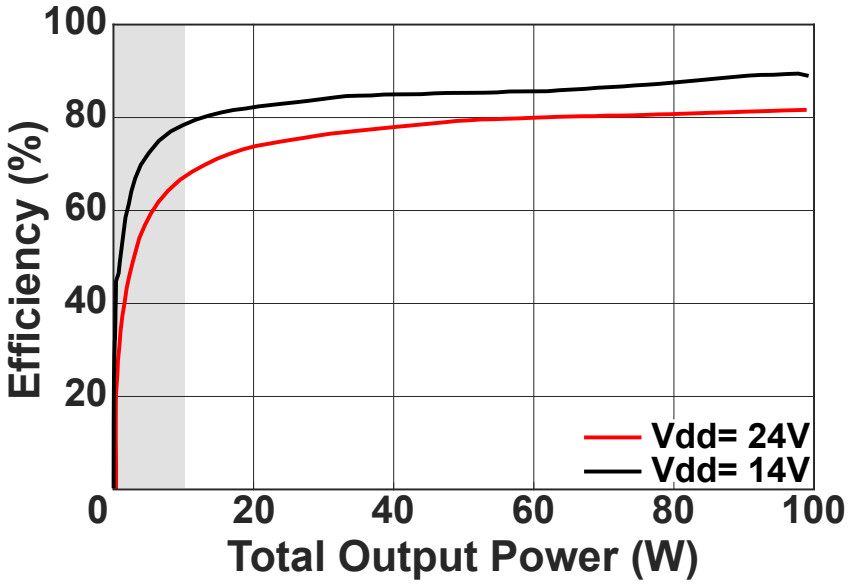


**Fig. 1.4** Efficiency plot of state-of-the-art class-D automotive audio amplifier.

any artifacts. As a result, the proper regulation of the supplies under all $V_{Bat}$ range of variations and protection clamps are vital for the audio fidelity of a car radio.

The efficiency is an important figure of merit (FOM) of an audio power amplifier among others that marks its advantages and qualifies it for specific applications. The efficiency is defined as the average power delivered to the load divided by the power drawn from $V_{Bat}$. Fig. 1.4 represents the efficiency curve of the state-of-

the-art class-D audio amplifier [5] for automotive applications. As highlighted with grey shade, the efficiency drops at low-load/quiescent condition. In the quiescent condition, there may be switching activity in the power stage without any power delivery to the load. All the circuit blocks in Fig. 1.2, except the power stage, load the supply voltages. Hence, in the quiescent condition, the efficiency of the power management block (supply voltage generator) determines the system efficiency. An efficient, automotive-grade supply voltage generator is required to be integrated with class-D audio amplifier for optimizing overall efficiency of car radio.

It is the goal of this thesis to investigate and design high efficiency, robust power management circuit to supply a class-D audio amplifier for car radio.

## 1.2 Comments on the suitability of different dc-dc converter techniques

In the state-of-the-art class-D audio power systems, all the supplies are generated linearly [6–8]. In addition to increased pin count of the integrated circuit (IC) and external component count, the efficiency of linear regulation is known to suffer. This gives scope for exploring the integrated, switching dc-dc converters as potential supply generators in a high voltage application like car radio. In the art, switching converters are implemented using an energy storage element periodically switched between battery and load. Using a capacitor or an inductor as the energy storage element, the switched capacitor and switched inductor power converters may be realized.

A straightforward approach to generate each supply required in the application is to use independent switched capacitor/inductor dc-dc converters. As the number of supplies increase, this approach would be prohibitively expensive in terms of the bill of materials (BoM) and board area. Reducing the number of external components,

especially inductors, is crucial in power management ICs (PMICs). Multiple output dc-dc converters support the regulation of two or more supply voltages while sharing some of the reactive components. In the switched capacitor multi-output regulators, the number of flying capacitors increases exponentially with the rise in number of outputs and conversion ratio. In addition, HV capacitors add severe cost constraints in the automotive applications. In contrast, a multiple output switched inductor dc-dc converter is the best suited solution as it requires a single inductor for energy acquisition and load capacitors, numbering equal to the outputs, for filtering. The single inductor multiple output (SIMO) dc-dc converter is studied extensively over the last decade and implemented effectively in several applications like portable systems, LED lighting among others. Owing to its suitability, a SIMO converter is explored as a solution to generate the supplies required in a car-radio.

## 1.3 Discussion of the general aspects of SIMO converter

As the battery operated applications proliferated, the importance of effective power management for improving the energy efficiency and longevity of the battery charge were understood. The advantages of having multiple supplies at different functional blocks, viz. memory, analog, digital, in a complex system are highlighted in many works [9–11]. Microprocessors, portable electronics gadgets, wireless transceivers are some of the systems where multiple supplies and dynamic voltage scaling (DVS) techniques are employed. On-chip supply generation using a SIMO converter is an attractive solution in all such applications due to the small form factor and high efficiency that SIMO converters offer [2, 3, 3, 5, 12–16, 18, 20, 21].

Fig. 1.5 shows the block diagram representation of a SIMO dc-dc converter. A switching power stage with its switching sequence controlled by a negative feedback implemented in the controller block mainly constitutes a SIMO converter. A SIMO

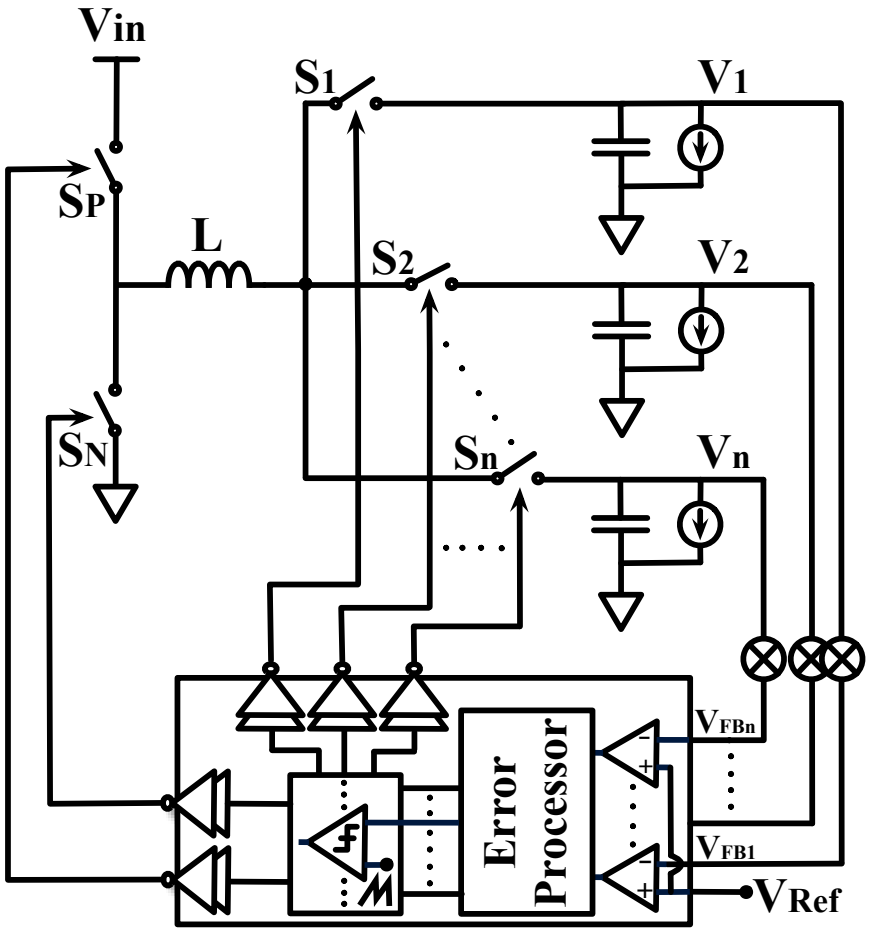


**Fig. 1.5** Block diagram representation of SIMO dc-dc converter.

converter topology is essentially a combination of several single inductor single output (SISO) switched converters. The outputs are sensed and collectively fed back into the controller that generates phases for energy acquisition from the battery and its distribution to the loads. The driver block drives the control signals to turn on/off the power switches in the SIMO converter.

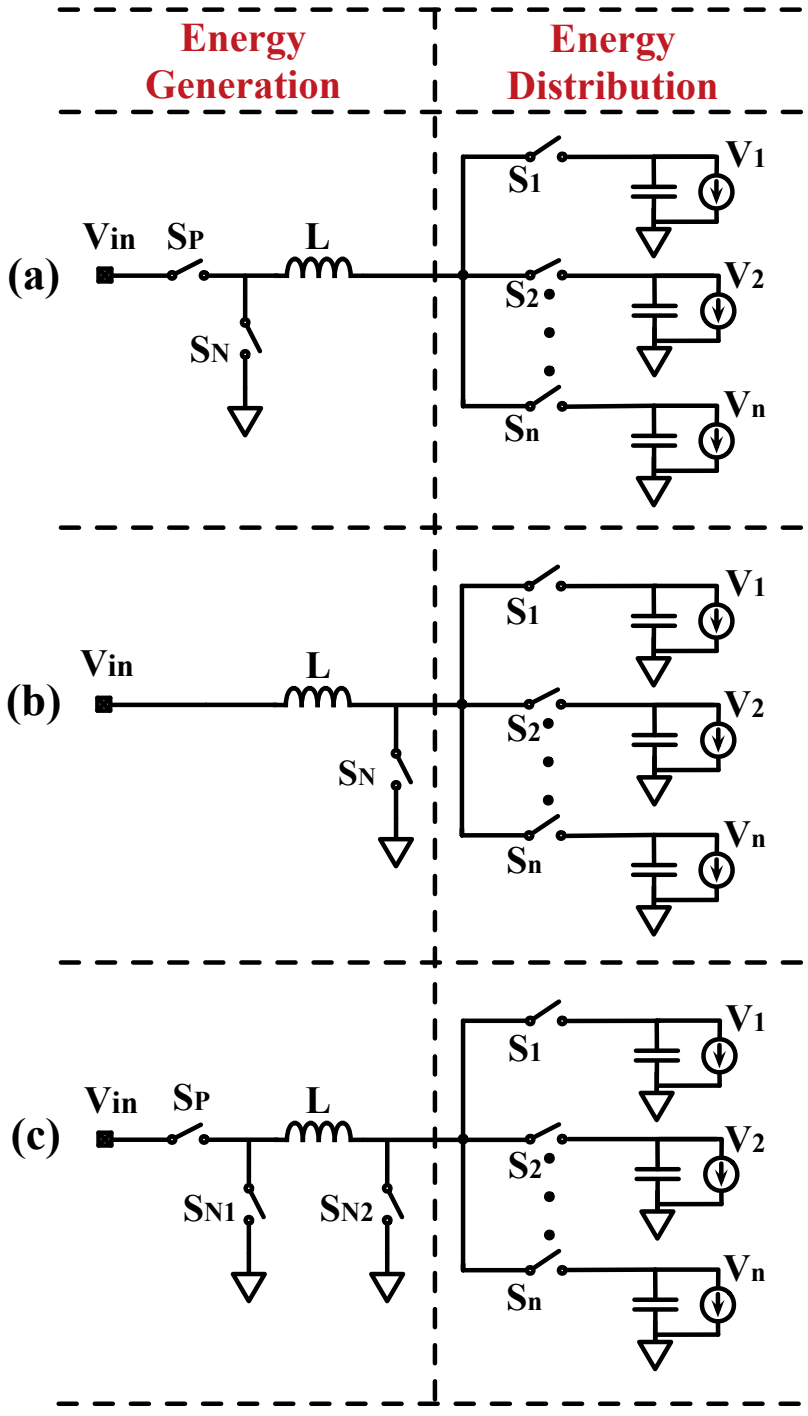


**Fig. 1.6** Power stage of SIMO dc-dc converter. (a) SIMO Buck, (b)SIMO Boost, (c) SIMO Buck-Boost.

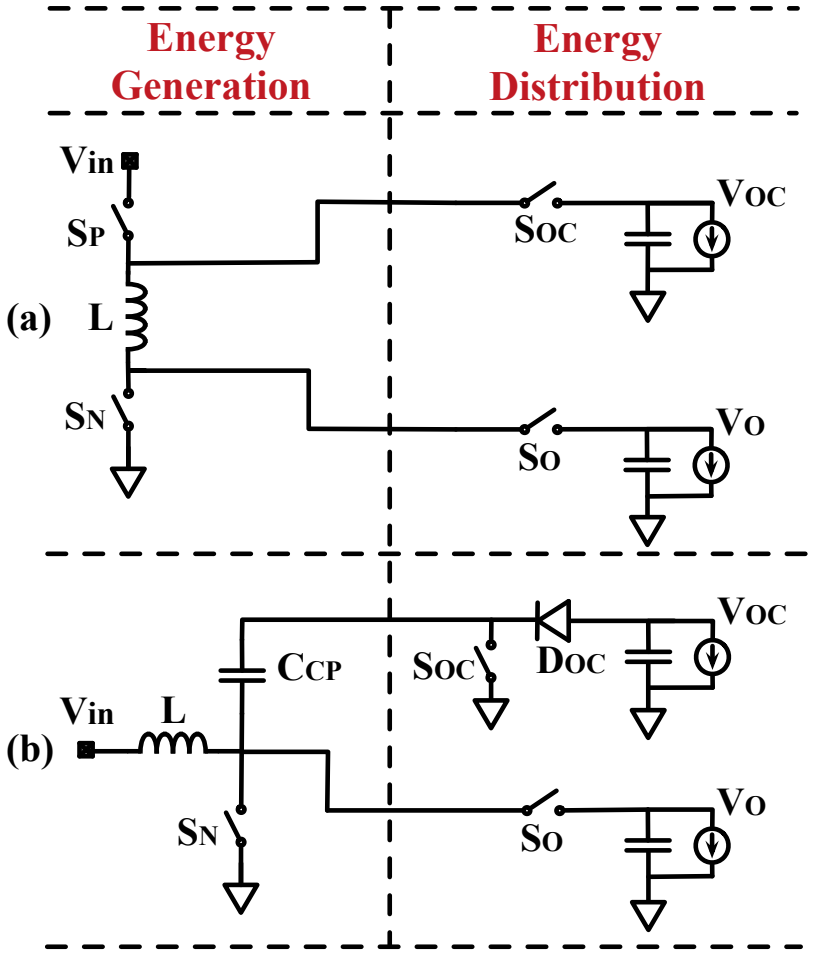


**Fig. 1.7** Complementary SIMO converter power stages. (a) SIMO Boost, (b) SIMO charge-pump complementary outputs.

In a SIMO converter, the topology of the power stage determines the buck/boost/buck-boost regulation of the outputs. As shown in Fig. 1.6, the power stages of SISO buck/boost/buck-boost converters may be used to regulate multiple outputs which are collectively equivalent to buck/boost/buck-boost voltages.

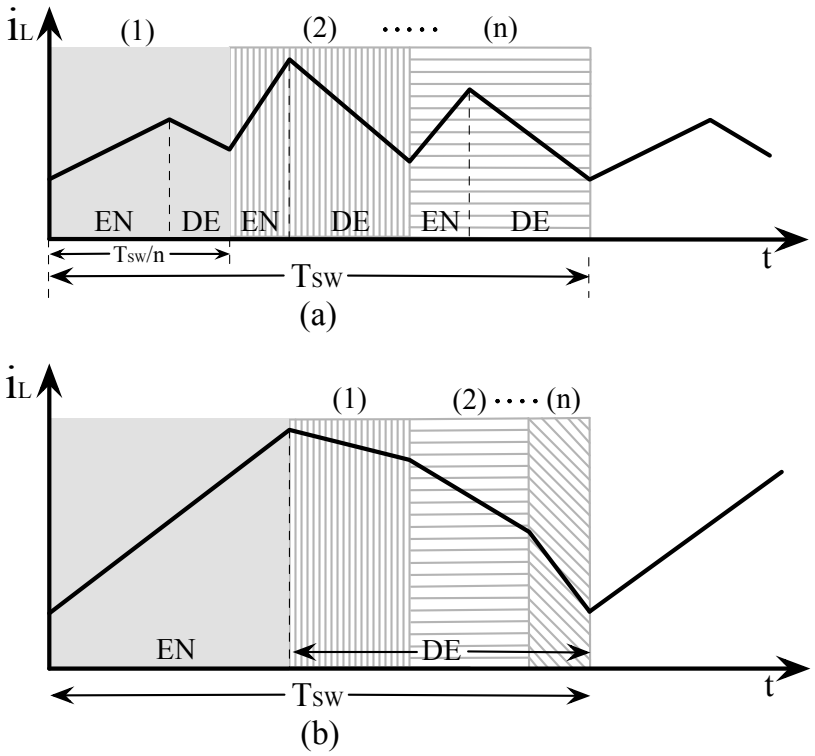


**Fig. 1.8** Inductor-current waveforms of SIMO in CCM. (a) Separate energizing/de- energizing inductor per load, (b) Single-step energizing inductor for all loads.

In addition, the power stages may be configured as shown in Fig. 1.7 to provide complementary and charge-pumped outputs. Hence, the SIMO converters may be adopted conveniently to regulate diverse types of load voltages.

The inductor current is time-multiplexed to supply multiple loads in a SIMO converter. The inductor may be energized in single step or multiple steps equal to number of outputs in each switching period. As shown in Fig. 1.8, by multi-step energizing the inductor, each load may be separately fed independent of the other load conditions. However, a single step, sufficient energizing of the inductor to supply all

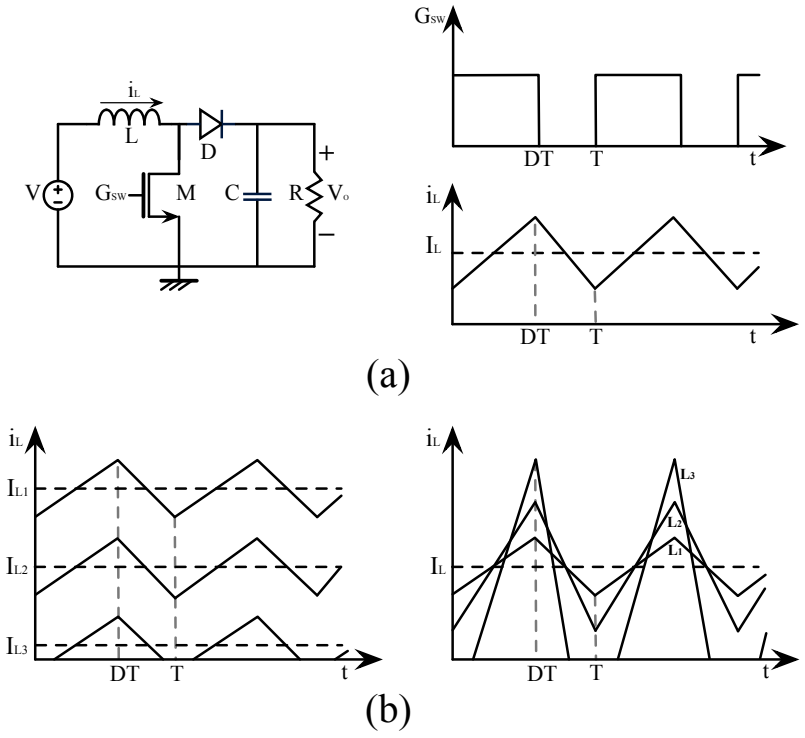


**Fig. 1.9** Comparison of CCM and DCM operation. (a) SISO boost converter in CCM, (b) Transition between CCM and DCM with the variation of inductor value.

the loads in each switching period reduces the output voltage ripples. As a result, high frequency switching may be employed [3].

Depending on the load current and the value of inductor, the dc-dc converters (SIMO/SISO) operate in continuous conduction mode (CCM) or discrete conduction mode (DCM). For a simplified explanation of the concept of CCM and DCM, a SISO boost converter may be considered [2]. The component values of the output LC filter determine the ripples in the inductor current ($i_L$) and the output voltage $V_O$. Fig. 1.9(a) shows the SISO boost converter together with the inductor current waveform in steady state. The peak-to-peak ripple in $i_L$ may be obtained as:

$$\Delta\, i_{L,pp} = \frac{VDT}{L} \tag{1.1}$$

Hence, for a specified $\Delta\, i_{L,pk}$:

$$L \geq \frac{VDT}{\Delta\, i_{L,pp}} \tag{1.2}$$

The percentage ripple ($X_{RPL}$) may be defined as:

$$X_{RPL} = \frac{Peak\ \ Ripple}{Average\ \ i_L} = \frac{\Delta\, i_{L,pp}}{2L} \tag{1.3}$$

Using (1.1), $X_{RPL}$ may be re-defined as:

$$X_{RPL} = \frac{D(1-D)^2 TR}{2L} \tag{1.4}$$

It is clear from (1.4) that the ripple percentage increases with smaller inductor and light load condition (larger R). The converter operates in CCM when the peak ripple ($i_{L,pk}$) is lower that the average inductor current $I_L$ (i.e. $X_{RPL}<1$). As shown in Fig. 1.9(b) , when $i_{L,pk}$ exceeds $I_L$, the diode turns off for a part of the switching period and the boost converter enters DCM. In case of synchronous switching in the converter, $i_L$ is monitored for zero current and the switches are turned off by the controller to set in DCM. When a converter enters DCM, its output impedance increases and the output voltage becomes load dependent. The small-ripple approximation is invalid in DCM.

Negative feedback is indispensible in SIMO converters to regulate the outputs against load and supply variations. The general aspects of the control techniques in SISO converters apply to SIMO converters with the additional challenge of mixing multiple feedback signals to generate the control phases required to regulate multiple outputs. The compensation of the feedback loop depends on (i) the type of converter *viz*. buck, boost or buck-boost, (ii) the mode of controller *viz*. hysteretic

mode (HM), voltage mode (VM) or current mode (CM) and (iii) the conduction mode of power stage *viz*. CCM or DCM conduction modes.

A buck/boost converter in CCM may be controlled with a hysteretic mode as shown in Fig. 1.10. The HM controller with adaptive, constant ON time employs a varying pulse frequency modulator (PFM) to regulate the output of a dc-dc converter. The controller reacts with an instant change in the pulse frequency in response to the inductor current variations due to the load or line changes. Such a transient triggered fluctuation of the switching frequency is a major constraint in EMI sensitive applications. The sever output ringing response of a HM converter, unless using a large filter capacitance, is an added drawback.

A VM dc-dc converter with buck/boost power stage may be represented as in Fig. 1.11. The feedback loop consists of a scaled output voltage feedback loop alone. Additionally, a VM dc-dc converter may incorporate the input (line) signal feed-forward by modulating the slope of ramp signal. In the input signal feed-forward VM converter, large signal transient response is independent of input voltage and output current fluctuations.

In the control to output transfer function, the buck converter introduces a fixed LC resonance (double pole) at the output. In a boost converter, a variable LC resonance

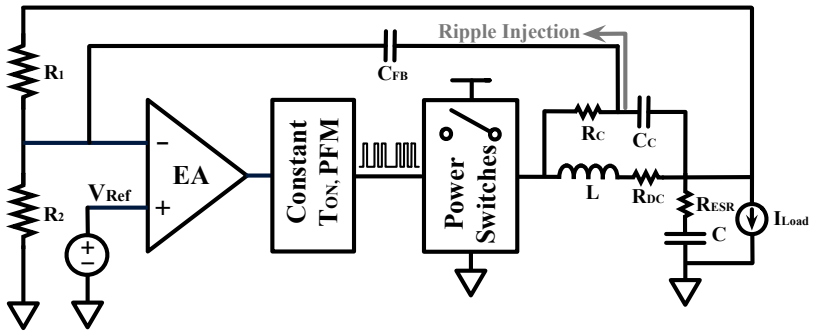


**Fig. 1.10** Controller of a dc-dc converter in hysteretic mode (HM).

and a right half place (RHP) zero appear in the transfer function. A zero due to the equivalent series resistance (ESR) of the output filter capacitor is ubiquitous in all the converters. In the presence of these dominant phase shifts along the voltage feedback path, a proportional-integral-derivative (PID) compensator is required to rewind the phase of the feedback loop and avoid positive feedback. Although, a PID compensator is complex to design, it provides unconditional stability to the VM dc-dc converters over wide range of line and load variations. A consistent performance over wide range of parameter changes and lower ringing response are the attractive features of VM dc-dc converters.

In the CM dc-dc converters, the controller consists of multi-loop feedback viz. an outer voltage feedback loop and an inner current feedback loop to respond to high frequency transients in the converter. The output voltage derived (scaled) signal and the inductor current derived signal are fed back into the two loops as shown in Fig. 1.12.

The current loop is unstable for the switching duty cycles above 50% and any perturbation to the inductor current sets in sub-harmonic oscillations. A compensating ramp of suitable slope, which depends on buck/boost conversion, is added/subtracted to the current feedback signal. The choice of slope involves a

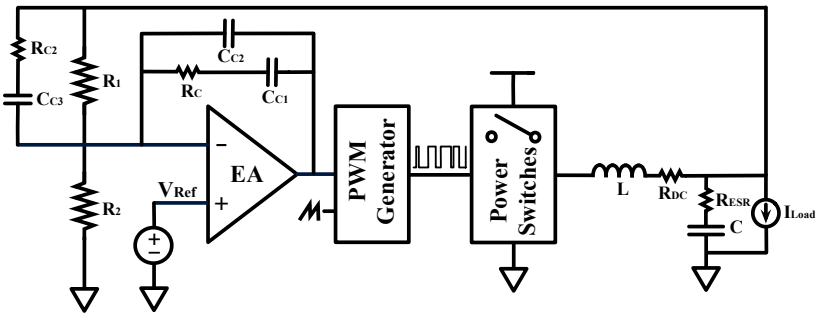


**Fig. 1.11** Controller of a dc-dc converter in voltage mode (VM).

trade-off among suppression of sub-harmonics, peak vs. average current sensing and the ripples on $i_L$.

The optimally compensated current feedback loop renders the inductor as a current source, eliminating its phase lag (-90°) contribution. Consequently, the output LC filter contributes a dominant single pole alone. The ESR-contributed zero and the RHP zero (in case of boost converter) are unperturbed by the current feedback loop. A simplified PI compensation ensures stability in a current mode controller. The CM controller offers a faster (high bandwidth) response than a VM controller. The main limitations of CM dc-dc converter are the ringing $i_L$ and residual sub-harmonic oscillations.

## 1.4 Important figures of merit (FoM) of SIMO converter

A SIMO dc-dc converter is required to offer strong output voltage regulation in the presence of varying supply and loads, that may impact the steady-state operating point. The regulation is characterized by some of the important figures-of- merit described here.

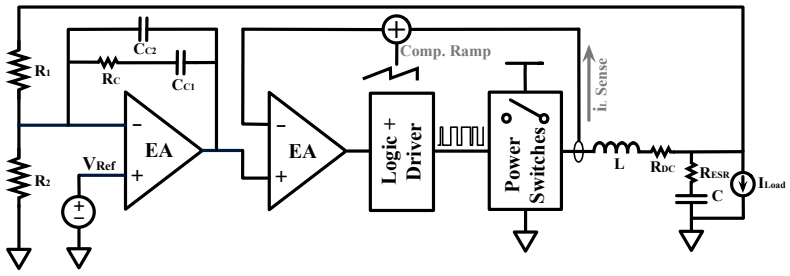


**Fig. 1.12** Controller of a dc-dc converter in voltage mode (CM).

1. Line Regulation: Line regulation of a SIMO dc-dc converter quantifies the fluctuation in regulated output voltage in response to a line voltage variation. Line Regulation in mV/V:

$$LineRegulation = \frac{\Delta\, V_{Out}}{\Delta\, V_{Line}} \tag{1.5}$$

2. Load Regulation and Cross Regulation: Load regulation of a SIMO dc-dc converter is its ability to maintain a regulated output constant in the presence of fluctuations in its load current. The load regulation is defined in mV/mA:

$$LoadRegulation = \frac{\Delta\, V_{Out_i}}{\Delta\, I_{Load_i}} \tag{1.6}$$

   As the SIMO converter time multiplexes the energy distribution to multiple outputs, the load transient in one of the outputs affects the regulation of the rest of the outputs. The variation in the regulated outputs of a SIMO converter, in response to the load transient in one of its outputs, is quantified by cross regulations in mV/mA.

3. Efficiency of a SIMO converter, like any other voltage regulator, is the measure of the fraction of power drawn from the battery ($P_{Battery}$) that is delivered to the load ($P_{Load}$). Efficiency in percentage:

$$Efficiency\ \ (\eta) = \frac{P_{Load}}{P_{Battery}} \tag{1.7}$$

   Using (1.7), the power loss in the SIMO converter may be obtained as:

$$P_{Loss} = P_{Out}\left(\frac{1}{\eta} - 1\right) \tag{1.8}$$

In addition to the above described FoMs, the active silicon and board area requirement, the external passive components, the bill-of-materials, the input voltage

range are the important specifications of an integrated SIMO dc-dc converter to be optimized.

In the following chapter, the automotive audio application is analyzed to define the architecture of a SIMO dc-dc converter to supply a car radio. The novel architecture is further modeled to study the steady state and dynamics of the converter.

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# Chapter 2

# Application specific analysis and topology selection of SIMO dc-dc converter

## 2.1 Introduction

In this chapter, a SIMO dc-dc converter is explored as a power supply generator required in a car-radio. Firstly, the requirements and limitations in the automotive audio application will be studied in detail to derive the system specifications. Based on the specifications, a suitable topology of the power stage in the SIMO dc-dc converter is introduced. The converter is modeled to study the steady state and the dynamic response. A controller together with the compensator is configured to control the multi-feedback loop of the SIMO converter. The system is split into multi blocks depending on the functionality and supply domains. System simulations are performed to derive block level specifications of the SIMO converter. Simulations results are provided wherever necessary.

## 2.2 Automotive audio specific system design constraints

The foremost constraint on the electronics systems targeting automotive application arises from the automotive battery profile. The cold-crank and load dump conditions result in large variations (> 25V) in the power rails. The automotive elec-

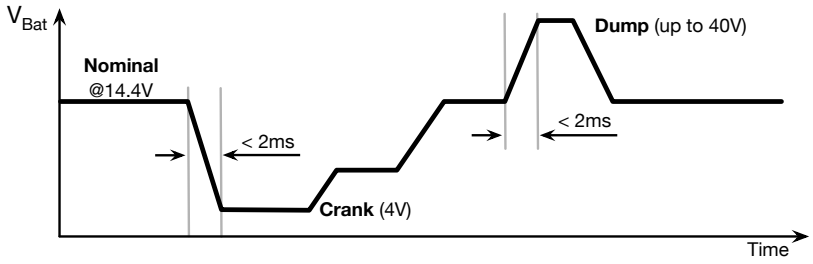


**Fig. 2.1** Automotive battery profile showing load dump and cold crank.

tronic systems are required to operate in the presence of such high voltage stress offering full functionality or tri-state. The automotive ICs are subjected to qualify AEC-Q100 to enter the market. The automotive battery profile may be recalled as shown in Fig. 2.1. The SIMO converter is required to power the class-D audio amplifier across the battery variation range of 4-40V. The output regulation in the presence of high frequency spikes and dips in the power rails demand a superior line regulation by the SIMO converter. In addition, all the integrated devices have to be protected against any violation of safe operating voltage rating. The SIMO converter, together with over-voltage/current protection circuits, has to implement soft-start/tri-state/shutdown to function in the safe operating area (SOA) of the system.

The other major constraint on the automotive electronic systems is the broad range of temperature over which the systems are required to function. The AEQ-100 specify an operating temperature range of -40° to +150° C for the packaged integrated electronic systems. Hence, the functionality over the specified temperature range is a key consideration in the design of SIMO dc-dc converter.

SIMO dc-dc converter being an inductor switching power converter, the high frequency switching current generates electromagnetic noise. The EM noise is susceptible to interfere with other electronics in the vehicle. The EMI related prob-

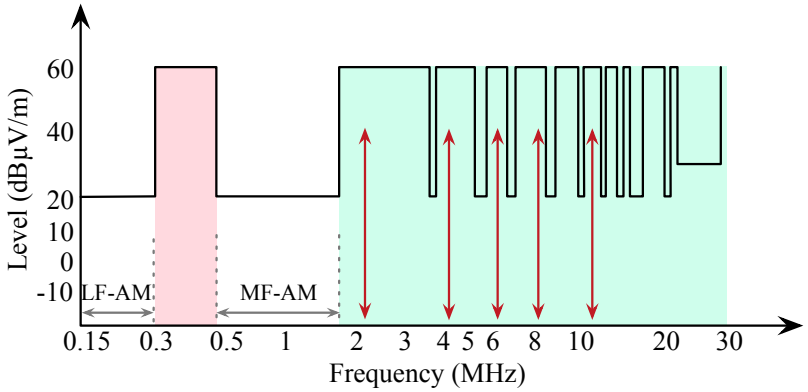


**Fig. 2.2** EMI mask used in class-D audio amplifier.

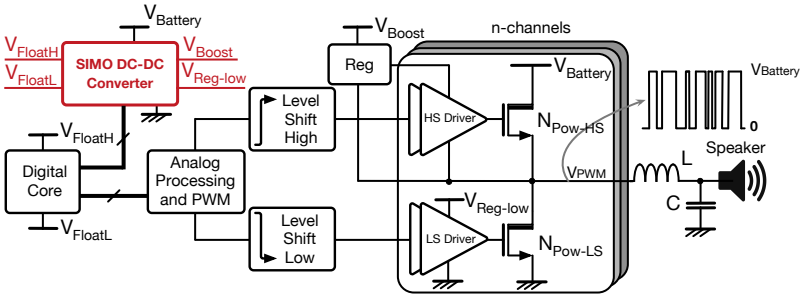


**Fig. 2.3** Automotive class-D audio amplifier with SIMO regulated supplies.

lems range from jamming the on-board radio to malfunctioning of the vehicle control systems. Consequently, immunity to EMI is critical in automotive environment. The sensitive automotive radio receivers are rendered immune to EMI by masking the EM noise in the AM/FM frequencies of interest. Fig. 2.2 shows a typical EMI mask to prevent any interference in the low and medium frequency AM broadcasting bands. EMI in the frequency bands 140kHz-300kHz and 500kHz- 1.8MHz must be strictly suppressed. By using a switching frequency in the range of 2-2.4MHz for the SIMO converter (i) avoids the EM interference in the AM frequency bands, (ii) significantly reduces the risk of interference at higher frequencies.

## 2.3 Modeling and analysis of SIMO dc-dc converter for car-radio

The power stage of a class-D audio amplifier drives the input audio PWM signal to the speaker load. The regulated floating/grounded drivers drive the power switches ($N_{Pow\text{-}HS,LS}$) as shown in Fig. 2.3. As the SIMO converter supplies both the high-side (HS) and low-side (LS) drivers, the gate charging currents of $N_{Pow\text{-}HS}$ and $N_{Pow\text{-}LS}$ load $V_{Boost}$ and $V_{Reg\text{-}low}$ respectively. The gate charging current of the power switches is a function of the switch dimension and the number of channels. Hence, the load currents of the driver supplies, *viz.* $V_{Boost}$ and $V_{Reg\text{-}low}$, scale directly with the switch dimension and the number of channels.

Fig. 2.4 shows the load profile of $V_{Boost}$ and $V_{Reg\text{-}low}$ specified for a class-D audio amplifier with maximum 4 channels switching at 2.4 MHz. The gate charging current drawn from the HS driver to turn on $N_{Pow\text{-}HS}$ in a single channel PWM switching is shown in Fig. 2.4(a). Similar current is drawn from the LS driver to turn on $N_{Pow\text{-}LS}$. High frequency switching of the power DMOSFETs results in large spikes (estimated $I_{Peak}$ =200 mA) in the gate-charging current. The average load current of the driver supplies scales with the number of channels enabled as shown in Fig. 2.4(b). The maximum average HS/LS diver current per channel is estimated at 20 mA. The SIMO converter is required to offer high load/cross regulation with respect to the average current variations during channel transitions. The load current spikes, due to gate charging, are filtered at the output capacitances of the SIMO converter.

SIMO converter also supplies the digital core in Fig. 2.3. The floating outputs, $V_{FloatH}$ and $V_{FloatL}$, are quasi-differentially regulated across half of $V_{Battery}$. The digital core that loads the floating outputs of the SIMO converter draws 30 mA of average current.

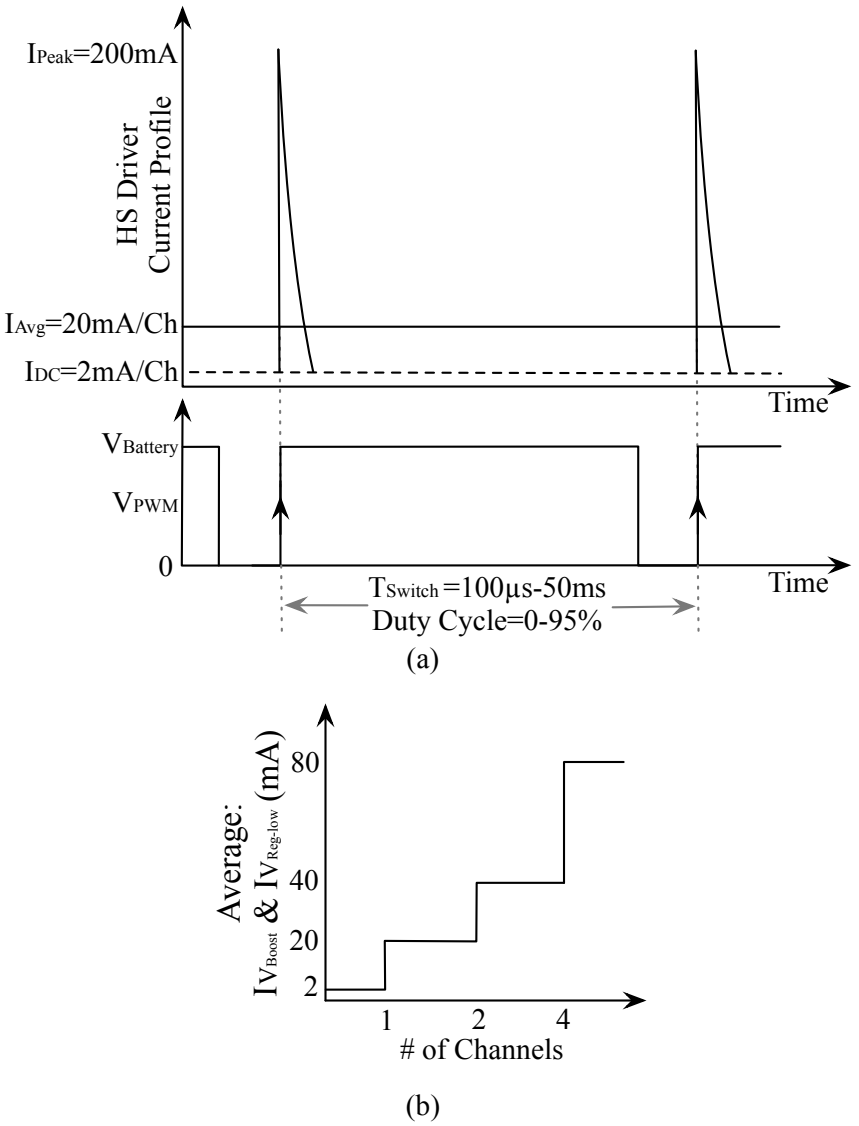


**Fig. 2.4** Load current profile of the driver supplies. (a) HS-Driver current profile for 1-channel PWM switching, (b) Average load current of the driver supplies scaling with number of channels.

Having understood the line (input) characteristics as well as the load and switching requirements, the initial specifications of the target SIMO converter are listed in Table 2.1.

**Table 2.1** Initial specifications of SIMO dc-dc converter.

| | | | |
|---|---|---|---|
| Input battery voltage ($V_{Battery}$) | 4-40V | | |
| Regulated output voltages | $V_{Boost}$ | $V_{Reg\text{-}low}$ | $V_{FloatH}$-$V_{FloatL}$ |
| | $V_{Battery}$ + 6.5 V | 4.5 V | 1.8 V |
| Load currents at regulated outputs | $I_{Boost}$ | $I_{Reg\text{-}low}$ | $I_{Float}$ |
| | 2-80 mA | 2-80 mA | 30 mA |
| Switching frequency ($F_{SW}$) | 2.1-2.4 MHz | | |
| Target Efficiency | > 80 % | | |

As noted in the introductory chapter, a multi-output dc-dc converter may be equivalently represented as a single output converter. By weighing average the output voltages of the SIMO converter, a direct correspondence may be obtained between the topologies of the SIMO and SISO converters. Such a representation would reduce the multi-feedback loops into a single feedback system and largely simplify the analysis of SIMO converter.

$$V_{Oi} = \frac{\Sigma\, V_{Ok} I_{Ok}}{\Sigma\, I_{Ok}} \tag{2.1}$$

$$V_{Od} = \frac{\Sigma\, V_{Ok} D_{Ok}}{\Sigma\, D_{Ok}} \tag{2.2}$$

The concept of weighing average of the outputs of a SIMO converter with k outputs converter is given by (2.5) and (2.2) [1]. $V_{Ok}$, $I_{Ok}$ and $D_{Ok}$ are the voltage, load current and duty cycle of the $k^{th}$ output. The outputs may be current or duty cycle weighted average. Both the weighted averages are equal when the multiple output powers are equal. In the present application, however, the output powers vary widely due to line and load current variations. Hence, the current weighted averaging is used to determine the topology of the SIMO converter.

Using (2.5), a current weighted average output for the SIMO converter may be evaluated across $V_{Battery}$ and the load current variations according to the specifica-

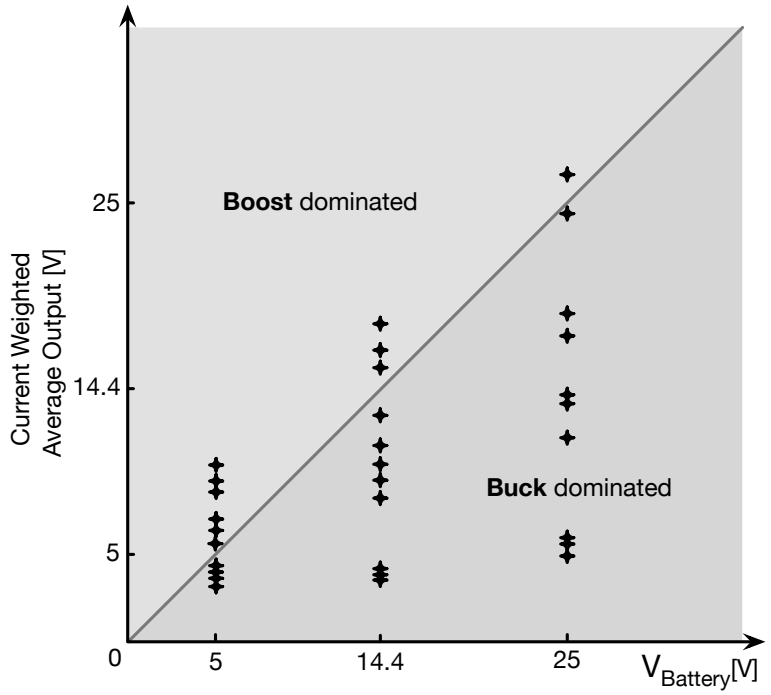


**Fig. 2.5** Current weighted average of the outputs of SIMO converter.

tions in Table 2.1. These calculations provide a ratio between the SIMO equivalent SISO output and $V_{Battery}$ in all the required operating conditions. Fig. 2.5 shows a plot of the current weighted average of the SIMO converter outputs with varying loads versus $V_{Battery}$. It is clear from Fig. 2.5 that the SIMO equivalent SISO converter is buck dominated in some of the load and line conditions and boost dominated in others. The buck-boost mode transitions are observed at a fixed $V_{Battery}$ as well due to load variations. As $V_{Battery}$ and the load current profiles in a car-radio consist of random, high frequency transients, the converter must offer a fast transition among buck and boost modes. Therefore, a non-inverting buck-boost converter with its seamless buck-boost output capabilities is best suited to supply a car-radio. The conversion factor of a non-inverting buck boost is given by (2.3) where D is the

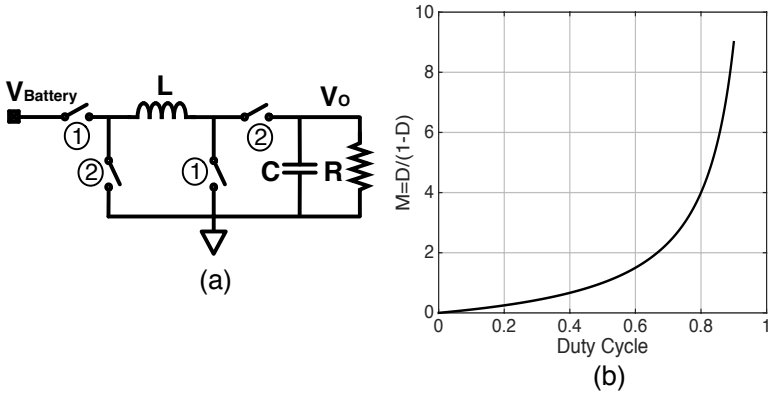


**Fig. 2.6** SISO non-inverting buck-boost converter. (a) Switching stage, (b) Conversion factor M versus duty cycle D.

duty cycle. Fig. 2.6(a) and Fig. 2.6(b) depict the power switching and the conversion factor of a non-inverting buck-boost converter in steady state [2].

$$M(D) = \frac{D}{(1-D)} \tag{2.3}$$

### 2.3.1 Modeling of the power stage of the SIMO converter

The car-radio sensitivity to EMI restricts the switching frequency of the SIMO converter to a higher value exceeding 2 MHz. At high switching frequencies, the output-voltage and inductor-current ripples may be reduced by a single step energy acquisition in the inductor and its time-shared distribution to all the loads in a switching period [3]. Hence, the SIMO converter employs a single inductor-charging event per switching cycle. Based on the analogy of the specified SIMO converter with a SISO non-inverting buck-boost converter explained in the previous sub-section, the power switching stage may be modeled as shown in Fig. 2.7. The power switches

$S_{P1}$ and $S_{P2}$ enable inductor charging. The switch $S_{P2}$ together with $S_{Boost}$ and $S_{Reg\text{-}low}$ distribute energy to the ground referred outputs $V_{Boost}$ and $V_{Reg\text{-}low}$. In the last phase, the inductor current circulates through $S_{FloatH,L}$ to energize the floating output ($V_{FloatH}$-$V_{FloatL}$).

As the regulated output $V_{Boost}$ is specified to exceed $V_{Battery}$ by 7V it has to track the battery profile earlier shown in Fig. 2.1. Therefore, with reference to ground, $V_{Boost}$ is not line regulated. Referred to $V_{Battery}$, however, $V_{Boost}$ (i.e $V_{Boost}$- $V_{Battery}$) requires both line and load regulation. $V_{Boost}$ filtering capacitor, $C_{Boost}$, rides over battery as shown in Fig. 2.7 to pump the event (crank, dump, step-up etc.) based variations in $V_{Battery}$ to $V_{Boost}$.

Similarly, the floating output requires difference regulation across half of the battery value. The regulated voltage, ($V_{FloatH}$- $V_{FloatL}$), must track the variations in $V_{Battery}$. In the power stage model, a balanced floating load is used. Therefore, the floating outputs, $V_{FloatH}$ and $V_{FloatL}$, are differential across the common mode voltage $V_{Battery}/2$. Resistive division of $V_{Battery}$, as shown in Fig. 2.7, provides the battery tracking common mode voltage.

The output $V_{Reg\text{-}low}$ in Fig. 2.7 needs both load and line regulation as it is regulated referred to ground. Among the non-idealities, the power stage models the on resistance ($R_{ON}$) of the power switches, DC resistance ($R_L$) of the inductor and equivalent series resistance ($R_C$) of the output filtering capacitors.

In the steady-state and CCM, using the power-stage in Fig. 2.7, the timing diagram and inductor-current waveform of the SIMO converter may be represented as shown in Fig. 2.8. Duty cycle $D_1$ accounts for the inductor-charging phase through $S_{P1}$ and $S_{P2}$. $D_2$ and $D_3$ account for the energy supply to $V_{Boost}$ and $V_{Reg\text{-}low}$ through $S_{P2}$, $S_{Boost}$ and $S_{Reg\text{-}low}$. During $D_4T_{SW}$, the remaining charge in the inductor is supplied to $V_{Float}$ by circulating $i_L$ through $S_{FloatH}$ and $S_{FloatL}$.

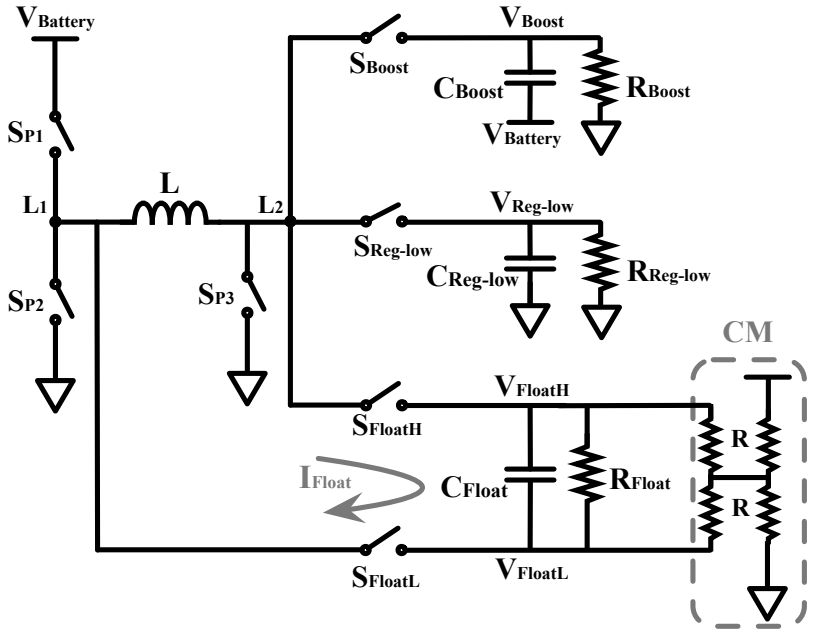


**Fig. 2.7** Switching power stage model of the SIMO dc-dc converter.

An equivalent synchronous SISO buck-boost converter, together with the non-idealities, to generate EN and DE phases in Fig. 2.8 is shown in Fig. 2.9 (a). $R_{ON}$, $R_L$ and $R_C$ model the ON resistance of the switches and the series resistance of the inductor and capacitor as modeled in the power stage of SIMO converter in Fig. 2.7. Asynchronous switching may be realized in the SISO buck-boost converter as shown in Fig. 2.9 (b). $V_D$ models the forward voltage drop of the diodes. The conversion factor of the synchronous and asynchronous SISO buck-boost converters in Fig. 2.9 is given by (2.4) and (2.5). In (2.4) and (2.5), $V_O$ is the current/duty-cycle weighted average of the outputs of the SIMO converter and $I_{Ok}$ is the load current of the $k^{th}$ output. Fig. 2.10 shows a comparison of the conversion factors of SIMO equivalent SISO buck-boost converters in Fig. 2.9 with $V_{Battery}$ at the nominal value of 14.4 V and crank value of 4.5 V loaded with 4-channel equivalent load current.

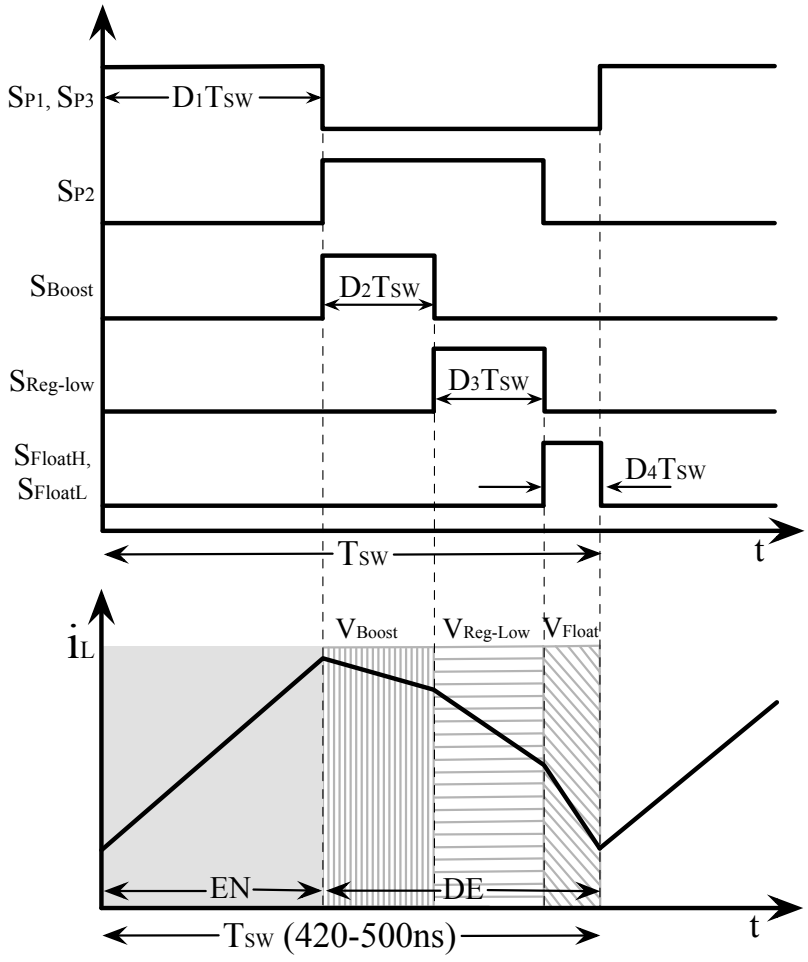


**Fig. 2.8** Timing diagram of the specified SIMO dc-dc converter in steady state and continuous conduction mode.

$$V_O = \frac{D_1}{1-D_1} V_{Battery} - \frac{\Sigma\, I_{Ok}(R_L + 2R_{ON})}{(1-D_1)^2} \tag{2.4}$$

$$V_O = \frac{D_1}{1-D_1} V_{Battery} - 2V_D - \frac{\Sigma\, I_{Ok} R_L}{1-D_1} - \frac{\Sigma\, I_{Ok}(R_L + 2R_{ON})}{(1-D_1)^2} \tag{2.5}$$

The wide range of $V_{Battery}$ results in similar, inversely proportional, range of variation in the average inductor current, $I_{LAvg}$, at a given load current. $I_{LAvg}$ is given by (2.6) [2,4]. From (2.4) and (2.5), the maximum value of duty cycle, $D_{1Max}$, occurs at the crank voltage of $V_{Battery}$= 4.5 V and the maximum load current (driving 4-channels of the class-D amplifier). Using the parameters $R_{ON}$= 0.5 Ω, $R_L$= 0.1 Ω and the maximum total load current $I_{OMax} = \Sigma I_{Ok}$ = 190 mA, the maximum duty cycle, $D_{1Max}$ = 0.8. Therefore, from (2.6), the maximum average inductor current $I_{LAvgMax}$ = 0.95 A. The peak current rating of the MOS switches limit the peak inductor current $I_{LPeak}$. $I_{LPeak}$ is given by (2.7), where $\Delta I_L$ is the ripple current.

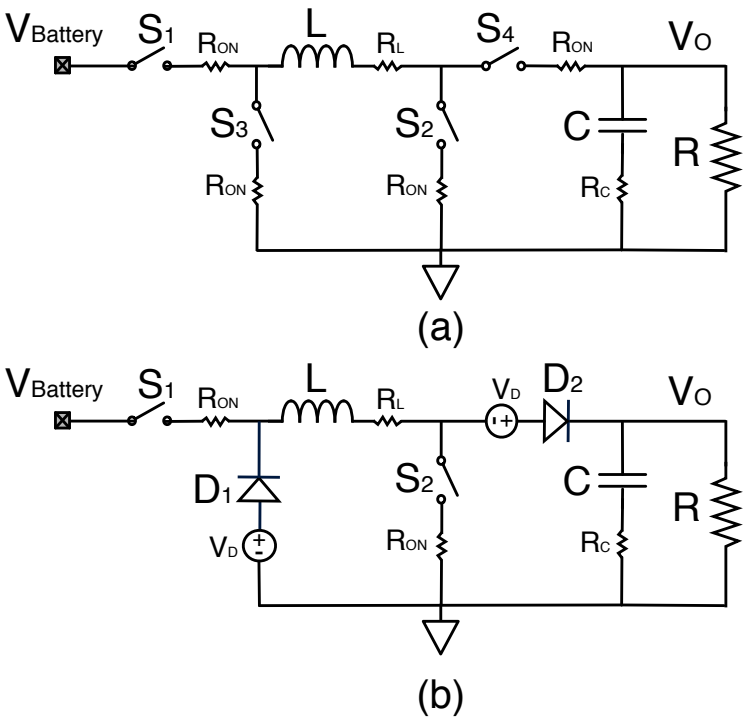


**Fig. 2.9** SIMO equivalent SISO buck-boost converter. (a) Synchronous switching, (b) Asynchronous switching.

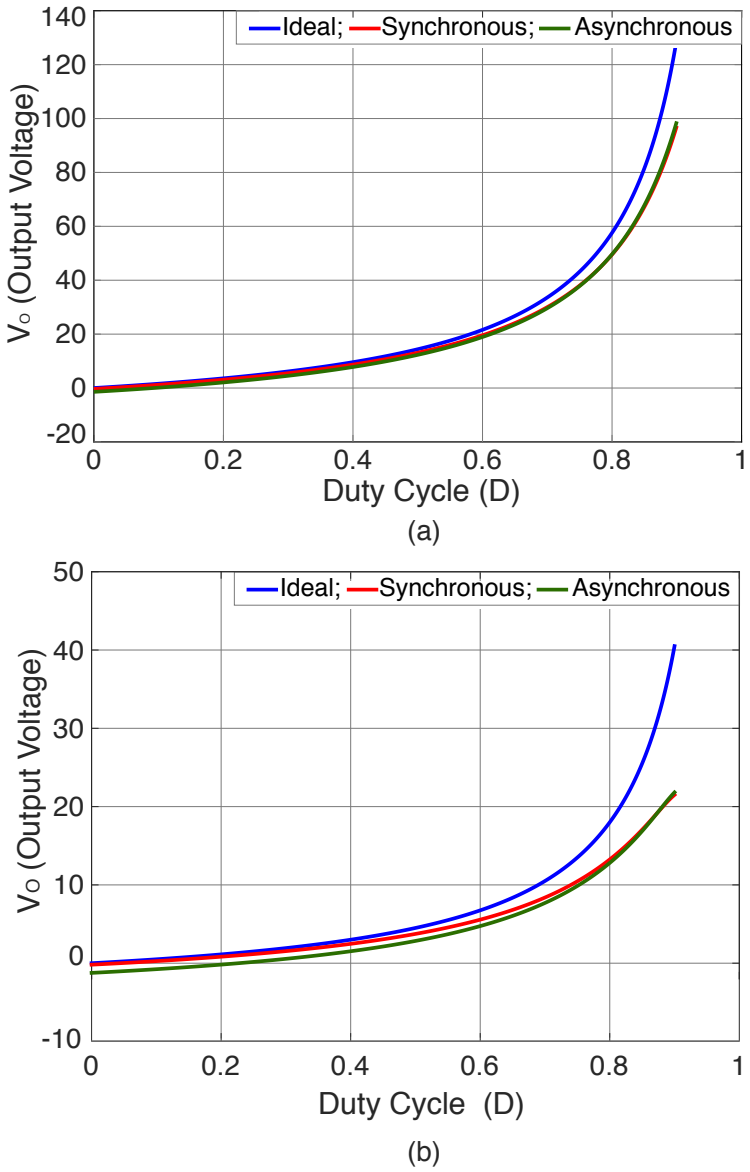


**Fig. 2.10** Conversion factor of SIMO equivalent SISO buck-boost converter with synchronous and asynchronous switching at (a) $V_{Battery}$= 14.4 V and (b) $V_{Battery}$= 4.5 V with $\Sigma I_{Ok}$= 190 mA, $R_L$= 0.1 Ω, $R_{ON}$= 0.5 Ω and $V_D$= 0.7 V.

Another objective to reduce $\Delta I_L$, in the present application, is to ensure CCM of the SIMO dc- dc converter at higher line voltages and lower load currents. Let $\Delta I_L$=

200 mA to limit $I_{LPeak} \leq 1.1$ A. The required inductance, using (2.8), is evaluated to be 8 μH. (2.9) yields the maximum RMS inductor current $I_{LRMSMax} = 0.952$ A. A commercial shielded power inductance, L= 10 μH with a saturating current $I_{LSat}$ = 3 A and $R_L = 0.1$ Ω is chosen for the SIMO converter.

$$I_{LAvg} = \frac{I_{OMax}}{1 - D_{1Max}} \tag{2.6}$$

$$I_{LPeak} = I_{LAvg} + \frac{\Delta I_L}{2} \tag{2.7}$$

$$L = \frac{(V_{Battery} - 2V_{ON} - V_L)D_{1Max}}{F_{SW} * \Delta I_L} \tag{2.8}$$

$$I_{LRMS\,Max} = \sqrt{I_{LAvg}^2 + \frac{\Delta I_L^2}{12}} \tag{2.9}$$

The output voltage ripple in the SIMO (equivalent SISO) converter is contributed by (i) the output capacitor discharge during inductor charging phase ($\Delta V_{OC}$) and (ii) the equivalent series resistance, $R_C$, due to instantaneous switch-on current flowing in the capacitor ($\Delta V_{ORC}$). Accordingly, the peak output ripple, $\Delta V_{OPeak}$, is given by (2.8) [2, 4]. The load-line combination that result in $I_{LPeak}$ and the corresponding $\Delta I_L$, also results in $\Delta V_{OPeak}$. Let the peak output ripple $\Delta V_{OPeak}$ = 30 mV. Typical ceramic capacitors used in power conversion offer $R_C \approx 20$ mΩ. At $I_{LPeak}$ = 1.1 A, as estimated previously, $\Delta V_{ORC} \approx 20$ mV. Therefore, to obtain $\Delta V_{OC}$ = 10 mV, an 8 μF capacitance is required. A multilayer ceramic chip capacitance, C = 10 μF with a parasitic $R_C$ = 20 mΩ is chosen for each output of the SIMO converter.

$$\begin{aligned} \Delta V_{OPeak} &= (\Delta V_{OC} + \Delta V_{ORC})_{Peak} \\ \Delta V_{OPeak} &= \frac{I_{OMax} D_{1Max}}{F_{SW} C} + I_{LPeak} R_C \end{aligned} \tag{2.10}$$

Table 2.2 enlists the component parameters of the switching power stage of the SIMO converter in Fig. 2.7.

**Table 2.2** Component parameter of the power stage of SIMO converter.

| Parameter | Value |
|---|---|
| $R_{ON}$ | 0.5 Ω |
| $V_D$ | 0.7 |
| L, $R_L$ | 10 μH, 100 mΩ |
| C, $R_C$ | 10 μF, 20 mΩ |

### 2.3.2 Modeling of the controller for the SIMO converter

In the SIMO converter the regulation of the outputs is established through multiple negative feedbacks. A controller is required to (i) compensate the feedback loops for stability and (ii) generate the switching phases to charge the inductor and discharge the energy into the loads.

With reference to the timing diagram of the SIMO converter in Fig. 2.8 , there are two distinct operations that determine the steady state energy input and output in the system. Several phases in the timing diagram may be expressed in terms of the switching period $T_{SW}$ as shown in the group of equations (2.11). The energizing (EN) and de-energizing (DE) phase balance the energy drawn from the battery and that delivered collectively to multiple outputs. The phase DE is further divided into sub-phases $D_2T_{SW}$, $D_3T_{SW}$ and $D_4T_{SW}$ to deliver energy to multiple outputs. Recalling the analogy between a SIMO converter and its equivalent SISO converter, EN and DE are synonymous with the charging and discharging phases of a SISO non-inverting buck-boost converter.

$$\begin{aligned} EN &= D_1 T_{SW} \\ DE &= D_2 T_{SW} + D_3 T_{SW} + D_4 T_{SW} \\ EN + DE &= T_{SW} \\ \sum_{i=1}^{4} D_i &= 1 \end{aligned} \tag{2.11}$$

Based on the above qualitative discussion, the control phase generation may be split into two parts. Firstly, the phases EN and DE may be generated taking into account the SIMO converter collectively. Hence, depending on the feedback gain, the collective system error may be processed to generate EN and DE. Further, DE may be divided into sub-phases to energize the outputs by relatively comparing the multiple output errors. The control phase generation may be mathematically formulated as follows.

Let the control phases in Fig. 2.8 be generated by processing the output errors $\varepsilon_i$ with i=1:3. Comparing the scaled outputs with a constant reference voltage may generate the errors as in (2.12).

$$\varepsilon_i = kV_i - V_{Ref} \tag{2.12}$$

Variable duty cycles $d_1$:$d_3$ may be represented by the linear combinations of the errors as in (2.13) [5]. Using a negative feedback with large dc loop gain and a proper compensation nullifies the linear combinations of errors $\varepsilon_i$ and the duty cycles settle at their steady state values $D_1$:$D_3$.

$$\begin{aligned} d_1 &= K_1(a_1\varepsilon_1 + a_2\varepsilon_2 + a_3\varepsilon_3) \\ d_2 &= K_2(b_1\varepsilon_1 + b_2\varepsilon_2 + b_3\varepsilon_3) \\ d_3 &= K_3(c_1\varepsilon_1 + c_2\varepsilon_2 + c_3\varepsilon_3) \end{aligned} \tag{2.13}$$

The set of equations in (2.13) form a linear non-homogenous system, which may be represented in a matrix form as in (2.14). The vectors A, ε and d are given by (2.15).

$$A\varepsilon = d \tag{2.14}$$

$$A = \begin{bmatrix} a_1 & a_2 & a_3 \\ b_1 & b_2 & b_3 \\ c_1 & c_2 & c_3 \end{bmatrix}; \quad \varepsilon = \begin{bmatrix} \varepsilon_1 \\ \varepsilon_2 \\ \varepsilon_3 \end{bmatrix}; \quad d = \begin{bmatrix} d_1/K_1 \\ d_2/K_2 \\ d_3/K_3 \end{bmatrix} \tag{2.15}$$

Recalling from linear algebra [6], a non-homogenous system of linear equations is consistent with a unique solution iff the corresponding homogenous system has a trivial solution only. Therefore, the linear system of (2.13) and (2.14) has a unique solution if matrix A is non-singular.

Mathematically several combinations of coefficients in matrix A yield unique solution to the system of (2.13). However, in the context of the error processing to generate the switching phases for the SIMO converter, the coefficients of matrix A are chosen to obtain summation and relative comparison of the errors [6]. Matrix A with the coefficients given by (2.16) is used for error processing in the controller.

$$A = \begin{bmatrix} +1 & +1 & +1 \\ +1 & -1 & -1 \\ +1 & +1 & -1 \end{bmatrix} \tag{2.16}$$

Using (2.16), the error combinations available for processing are given by (2.17). The sum of the errors $\varepsilon_i$ represents the total error in the outputs collectively. Hence it is used to generate the charging phase of the converter EN. The difference between $\varepsilon_1$ and ($\varepsilon_2$+ $\varepsilon_3$) compares the magnitude of error at the first output with the collective error of the remaining outputs. A positive value is an indication of a larger error

at the first output and the requirement of charge. Therefore the error combination of (2.17(b)) is used to generate the phase $D_2T_{SW}$. Similarly, the error combination in (2.17(c)) compares of the error in the third output with the sum of first and second output errors. After the phase $D_2T_{SW}$, however, the combination in (2.17(c)) is essentially a comparison of $\varepsilon_2$ and $\varepsilon_3$. A larger $\varepsilon_3$ in comparison with $(\varepsilon_1 + \varepsilon_2)$ determines the phase $D_4T_{SW}$.

$$\begin{aligned} d_1 &= K_1(\varepsilon_1 + \varepsilon_2 + \varepsilon_3) && (a) \\ d_2 &= K_2(\varepsilon_1 - \varepsilon_2 - \varepsilon_3) && (b) \\ d_3 &= K_3(\varepsilon_1 + \varepsilon_2 - \varepsilon_3) && (c) \end{aligned} \tag{2.17}$$

In (2.17) the gain coefficients of the error combinations $K_1$:$K_3$ determine the accuracy of regulation at the outputs. Higher value of $K_1$:$K_3$ reduces the magnitude of error combinations and thereby the errors $\varepsilon_1$:$\varepsilon_3$ themselves. However, the coefficient $K_1$ has an impact on the stability of the converter. This is because $K_1$ provides the feedback gain to the collective system error to determine EN and DE phases in Fig. 2.8. Hence, $K_1$ is determined considering the compensation and phase margin required to regulate the SIMO converter. The $K_2$ and $K_3$ in (2.17(b)) and (2.17(c)) provide gain to the error combinations that only divide the phase DE which is determined by (2.17(a)). Hence, $K_2$ and $K_3$ may be set equal to $K_1$.

The phases EN and DE of the SIMO converter being identical to the control phases of an equivalent SISO converter, both the converters may be similarly ac modeled for the small signal analysis to understand the dynamics and determine the compensation required. Hence, the small signal ac model of the SIMO equivalent SISO buck-boost converter with voltage mode controller is shown in Fig. 2.11. The non-idealities associated with the power switches and filtering passive components shown in Fig. 2.9 are included in the small signal analysis. In Fig. 2.11, d(t), $v_g$(t), v(t) represent the ac small signal values of the duty cycle (D), battery voltage

($V_{Battery}$) and output $V_O$. H(t) is the feedback factor. $V_M$ is the peak value of the sawtooth signal. $G_C$(t) models the transfer function of the compensator. Let A be the gain of the error amplifier EA.

The small signal control-to-output transfer function $G_{Vd}$((s) is given by (2.18). Similarly, the open-loop small signal line-to-output transfer function $G_{Vg}$(s) and the output impedance $Z_{Out}$(s) of the SISO buck-boost converter in Fig. 2.11 are given by (2.19) and (2.20) respectively. The weighted average output voltage of SIMO converter $V_O$ is characterized by large variations. Similarly, the load current is a function of the number of active channels of the class-D amplifier. Therefore, in (2.18)-(2.20), $V_O$ and load resistance R are characterized by large variations.

$$G_{Vd}(s) = \frac{D'R\left[\frac{V_O}{D} - \frac{V_O}{R}R'_{ON} - s\frac{V_O}{RD'^2}L\right](1+CR_C)}{s^2LC(R+R_C) + s[L + C(R+R_C)D'^2R'_{ON} + CR_CRD'^2] + D'^2(R+R'_{ON})} \tag{2.18}$$

where,

$$R = \frac{V_O}{I_{Load}}; \qquad R'_{ON} = \frac{R_L + R_{ON}}{D'^2}$$

$$G_{Vd}(s) = \frac{D}{D'}\frac{D'^2R(1+CR_C)}{s^2LC(R+R_C) + s[L + C(R+R_C)D'^2R'_{ON} + CR_CRD'^2] + D'^2(R+R'_{ON})} \tag{2.19}$$

$$G_{Vd}(s) = \frac{(s'^2LCR_C + s(L + CR'_{ON}R_CD'^2) + R'_{ON}D'^2)R}{s^2LC(R+R_C) + s[L + C(R+R_C)D'^2R'_{ON} + CR_CRD'^2] + D'^2(R+R'_{ON})} \tag{2.20}$$

The closed-loop gain of the control system in Fig. 2.11 may be obtained as in (2.21). The closed-loop, small signal output, line-to-output transfer function and output impedance are given by (2.22), (2.23) and (2.24) respectively.

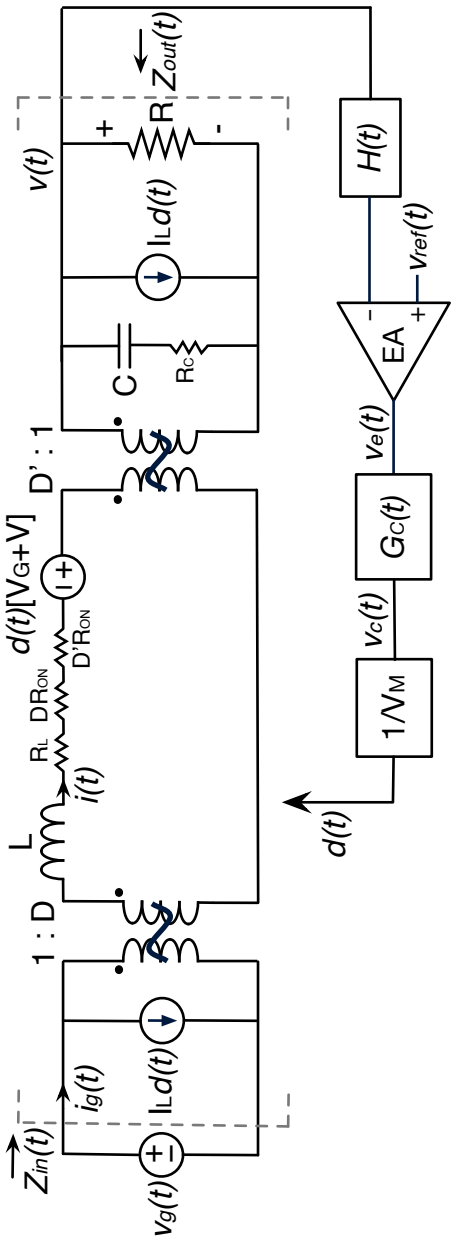


**Fig. 2.11** Controller with ac small signal model of SIMO equivalent SISO buck- boost converter.

$$LoopGain: \quad T(s) = G_{Vd}(s) * H(s) * A * G_C(s) * \frac{1}{V_M} \tag{2.21}$$

$$v(s) = v_{ref}(s)\frac{1}{H(s)}\frac{T(s)}{1+T(s)} + v_g(s)\frac{G_{Vg}(s)}{1+T(s)} - i_L(s)\frac{Z_{Out}(s)}{1+T(s)} \tag{2.22}$$

$$G'_{Vg}(s) = \frac{G_{Vg}(s)}{1+T(s)} \tag{2.23}$$

$$Z'_{Out}(s) = \frac{Z_{Out}(s)}{1+T(s)} \tag{2.24}$$

As the SISO buck-boost converter modeled in Fig. 2.11 is a negative feedback control system, the loop-gain, T(s), is required to maintain a phase margin before unity gain (0 dB) cross over to ensure stability of the system. Consider the loop gain without compensation, $T_{NC}(s)$, to determine the dominant poles and zeros contributing to the roll-off/on of the frequency response.

$$T_{NC}(s) = G_{Vd}(s) * H(s) * A * \frac{1}{V_M} \tag{2.25}$$

The SIMO converter being designed and the equivalent SISO converter are HV converters with input battery, $V_{Battery}$, varying between 4-40 V. However, the error processing may be performed at a lower voltage domain using the standard low-voltage CMOS devices. Therefore, the design parameters corresponding to 1.8-V domain are used here to model the error processor. Substituting the expression for $G_{Vd}(s)$ in (2.25), $T_{NC}(s)$ may be expanded as,

$$T_{NC}(s) = \frac{\left[D'R\left[\frac{V_O}{D} - \frac{V_O}{R}R'_{ON} - s\frac{V_O}{RD'^2}L\right](1+CR_C)\right] * H(s) * A * \left[\frac{1}{V_M}\right]}{s^2LC(R+R_C) + s[L + C(R+R_C)D'^2R'_{ON} + CR_CRD'^2] + D'^2(R+R'_{ON})} \tag{2.26}$$

In (2.26), a left half plane (LHP) zero $Z_1$, a right half plane (RHP) zero $Z_2$ and a pair of LHP real/complex-conjugate poles $P_1$ and $P_2$, are identified. $Z_1$ is fixed as ESR of the output filter capacitor contributes it. $Z_2$ is a function of equivalent output $V_O$, the load R and the resulting duty cycle D. As $V_O$, R and D vary over wide range, as explained previously, $Z_2$ is a moving RHP zero. Similarly, the poles $P_1$ and $P_2$ vary. In addition, the RHP zero contributes to degrading the phase margin as the phase drops while the magnitude of the frequency response increases.

Fig. 2.12 shows the pole-zero plot of the uncompensated loop gain $T_{NC}(s)$ for different input and load conditions. The peak amplitude of the sawtooth signal is set at $V_M$=1.8 V and the error amplifier gain, A=10 was used in the expression. The parasitic resistances of the off-chip the inductor and filtering capacitor were estimated from a commercial datasheet. The poles $P_1$, $P_2$ and the zeros $Z_1$ and $Z_2$ in (2.26) are plotted for $V_{Battery}$= 4.5, 14.4 and 25 V with a load current equal to 4-channels of the class-D amplifier. In Fig. 2.12 it is clear that $Z_1$ is a fixed LHP zero determined by the capacitor C and its ESR, $R_C$. The RHP zero $Z_2$ is a strong function of input battery voltage and load current. Consequently, $Z_2$ varies over a wide range of frequencies between 0.2M-30M rad/sec. Similarly, $P_1$ and $P_1$ are real/complex-conjugate pairs varying over the frequency range indicated by grey shaded region in Fig. 2.12.

In the presence of widely moving poles and zeros, the compensation is required to ensure system stability in the SIMO (or equivalent SISO) converter in all the line and load conditions. As the line and load variations are random, an adaptive compensator for every polo-zero location is unrealizable. Therefore, a compensator for the critical pole-zero location (nearest to the origin) may be realized to stabilize the system in the particular line-load condition. Although not optimal in terms of bandwidth, such a compensator would ensure stability of the system in non-critical pole-zero locations as well.

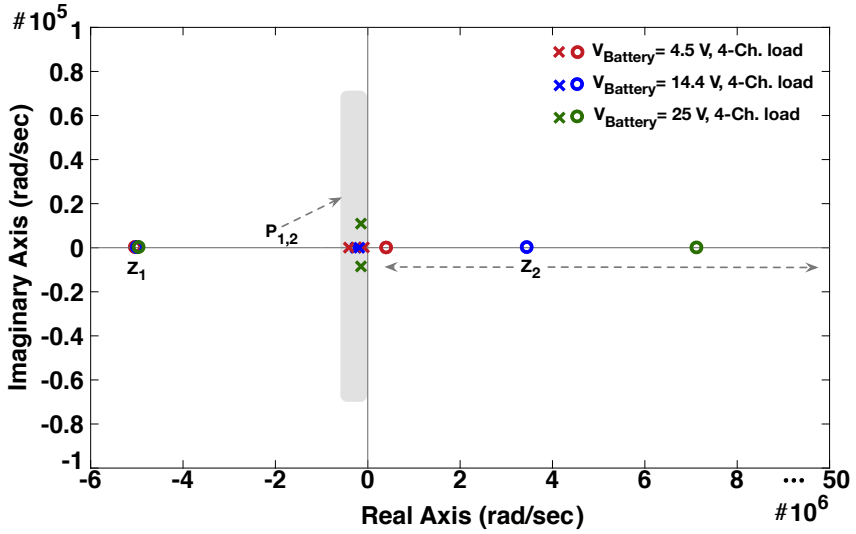


**Fig. 2.12** P-Z plots of $T_{NC}(s)$ for varying line-load conditions of the SIMO converter.

A multi-layer ceramic filter capacitor model yields $Z_1$, fixed at 5 Mrad/s (~800 kHz). To simplify the compensator, the maximum 0 dB cross over frequency of the compensated loop gain, T(s), may be targeted at 1 Mrad/s (~160 kHz) and $Z_1$ be left uncompensated. This avoids the requirement of a Type-3 compensator. The remaining pair of poles $P_{1,2}$ and the RHP zero $Z_2$ in (2.26) may be compensated by two approaches.

In the first method, $P_1$, $P_2$ and $Z_2$ may be cancelled by the compensator and 0 dB crossover of T(s) may be determined by a pole at origin. A lead-lag compensator, $G_{C1}(s)$, in (2.27) may be used to obtain the required compensation in T(s) with a low frequency of 0 dB crossover (1 kHz-10 kHz). $Z_{C1,2}$ compensate $P_{1,2}$ and $P_{C2}$ compensates $Z_2$ in T(s). To compensate the moving $P_{1,2}$ and $Z_2$ in Fig. 2.12, $Z_{C11,12}$ and $P_{C12}$ are placed at the frequencies lower than the critical locations (lowest frequency) of $P_{1,2}$ and $Z_2$. The critical locations of $P_{1,2}$ and $Z_2$ occur at $V_{Battery}$= 4.5 V and 4-channel equivalent load and correspond to: $P_1$= 8 krad/s, $P_2$= 100 krad/s and $Z_2$= 200 krad/s. The lower bandwidth of T(s) resulting from $G_{C1}(s)$ leads to a slug-

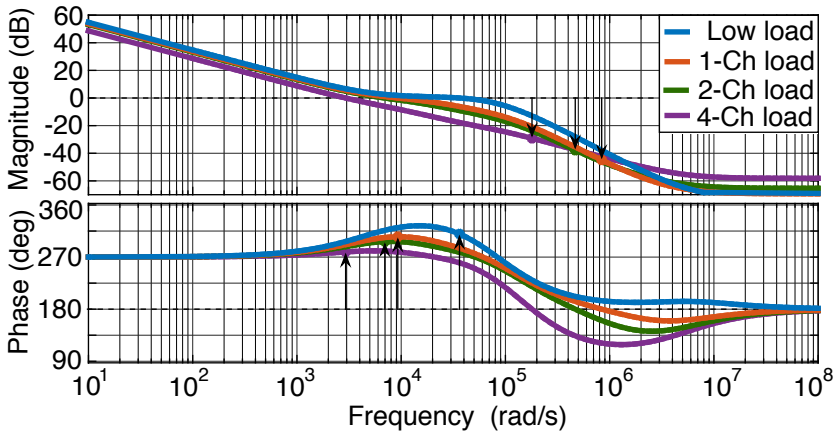


**Fig. 2.13** Frequency response of the loop gain T(s) compensated with a lead-lag compensator $G_{C1}(s)$ at the line voltage $V_{Battery}$= 4.5 V and varying load currents.

gish response to the line and load variations in the SIMO converter. Fig. 2.13 shows frequency response of T(s) compensated using $G_{C1}C_1(s)$ at $V_{Battery}$= 4.5 V and the load currents varying with the number of channels of the class-D amplifier.

$$G_{C1}(s) = \frac{(s+Z_{C11})(s+Z_{C12})}{s(s+P_{C12})} \tag{2.27}$$

In Fig. 2.13, T(s) is compensated with the pole and zeros of $G_{C1}(s)$ located at: $Z_{C11}$= 5 krad/s, $Z_{C12}$= 50 krad/s and $P_{C12}$= 100 krad/s. Clearly from Fig. 2.13, $G_{C1}(s)$ provides sufficient phase margin in all the load conditions at $V_{Battery}$= 4.5 V. In particular, at the critical pole-zero location corresponding to 4-channel load current, a low-frequency 0 dB crossover of T(s) at 3 krad/s (~ 0.5 kHz) is observed.

Loop gain, T(s), may be sufficiently compensated together with significant increase in 0 dB crossover frequency by using a lead compensator alone. Let $P_2$ be the non-dominant pole in $T_{NC}(s)$ when $P_{1,2}$ are real. A lead compensator, $G_{C2}(s)$ in (2.28), with the pole-zero pair $Z_{C21}$-$P_{C22}$ may compensate $P_2$ among the real poles $P_{1,2}$ and the RHP zero $Z_2$ in (2.26) respectively. In the load-line conditions where

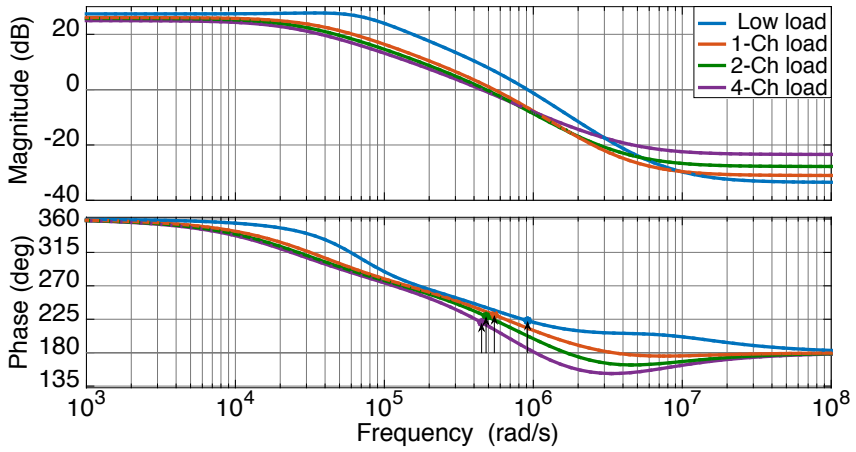


**Fig. 2.14** Frequency response of the loop gain T(s) compensated with a lead compensator $G_{C2}(s)$ at the line voltage $V_{Battery}$= 4.5 V and varying load currents.

$P_{1,2}$ are complex conjugates, $Z_{C21}$ compensates one of them ($P_2$). When $Z_{C22}$-$P_{C22}$ pair is positioned to compensate $P_2$-$Z_2$ at their critical locations and $Z_1$ fixed at 5 Mrad/s, $G_{C2}(s)$ compensates T(s) and $P_1$ determines the roll-off of the frequency response.

$$G_{C1}(s) = \frac{(s + Z_{C21})}{(s + P_{C22})} \tag{2.28}$$

As the critical locations of $P_{1,2}$ and $Z_2$ in Fig. 2.12 occur at $V_{Battery}$=4.5 V and 4-channel equivalent load, T(s) is compensated with $Z_{C21}$ and $P_{C22}$ located at: $Z_{C21}$ = 80 krad/s and $P_{C22}$= 600 krad/s. Fig. 2.14 shows the frequency response of the loop gain, T(s), compensated with $G_{C2}(s)$ at $V_{Battery}$= 4.5 V. A phase margin exceeding 40° is observed across all the loading conditions. The 0 dB crossover of T(s) occurs at 500 krad/s (~80 kHz) with minimum low frequency gain of 25 dB.

Similarly Fig. 2.15 and Fig. 2.16 show the frequency response of T(s) compensated with $G_{C2}(s)$ at the nominal battery voltages, $V_{Battery}$= 14.4 V and 25 V respectively. At both the battery voltages and across all the loading conditions, the phase

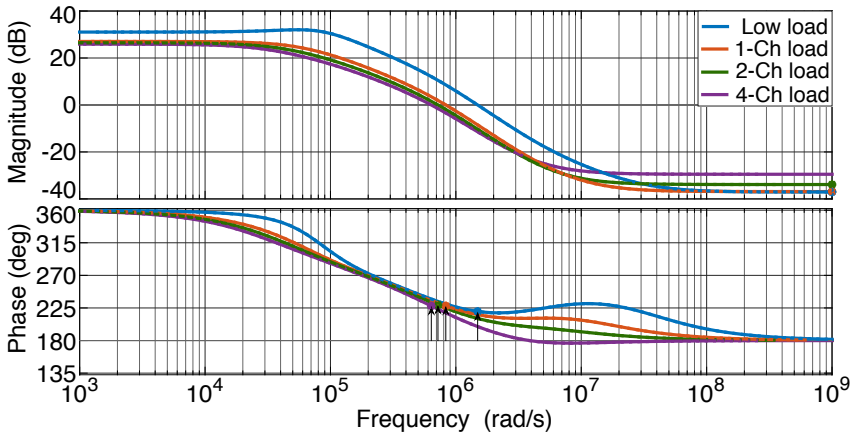


**Fig. 2.15** Frequency response of the loop gain T(s) compensated with a lead compensator $G_{C2}(s)$ at the line voltage $V_{Battery}$= 14.4 V and varying load currents.

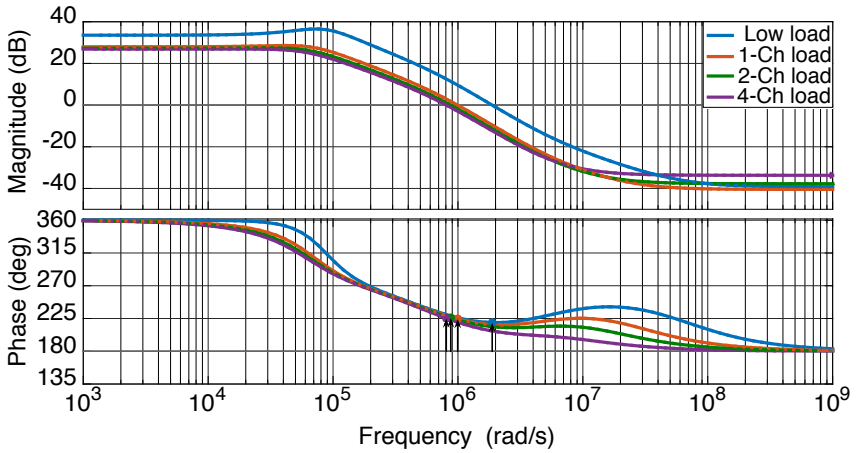


**Fig. 2.16** Frequency response of the loop gain T(s) compensated with a lead compensator $G_{C2}(s)$ at the line voltage $V_{Battery}$= 25 V and varying load currents.

margin of T(s) exceeds 40°. The 0 dB crossover of T(s) exceeding 100 kHz results in the required fast response to the load and line variations. A low frequency loop gain, |T(s)|, exceeding 25 dB is obtained in all the load-line combinations. The reduction in low frequency gain is the trade-off in order to simplify the compensation of T(s) using $G_{C2}(s)$ and obtain fast response.

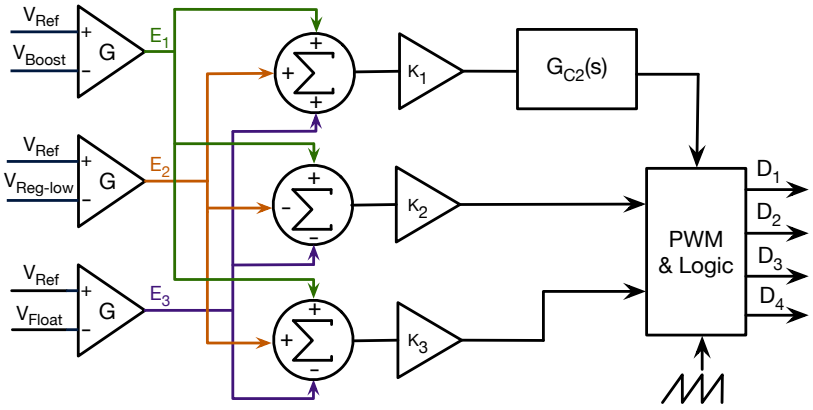


**Fig. 2.17** Functional block diagram of the error processor and switching phase generation in SIMO converter.

### 2.3.3 System simulation of the SIMO converter based on modeling

Based on the circuit parameters obtained from the steady state and small signal models described in the previous sections, the SIMO dc-dc converter was simulated at the system level targeting the specifications in Table 2.1. The main objective of system simulation was to verify the functionality of the SIMO converter with the available block level specifications.

Fig. 2.17 shows the functional block diagram of the error processor to generate the switching phases of the SIMO converter. The error processing operation follows (2.17). The previously analyzed lead compensator, $G_{C2}(s)$, is used to compensate the feedback loop. PWM of the error combinations followed by digital logic yields the switching phases, $D_1$-$D_4$, of the SIMO converter.

The power stage in Fig. 2.7 was implemented with the parameters in Table 2.2. The switches were modeled with $R_{ON}$, $R_{OFF}$ and the terminal capacitances. The tope level simulations confirmed (i) the steady state stability of the SIMO converter, (ii) the output response to the transients in $V_{Battery}$, (iii) line and load regulation. Fig. 2.18 shows the start-up of the SIMO dc-dc converter and the regulated outputs,

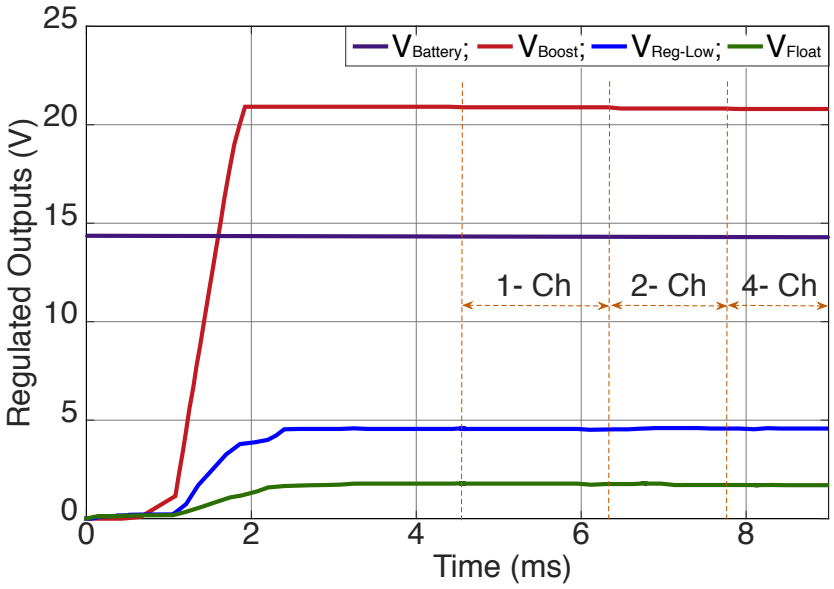


**Fig. 2.18** Start-up of the SIMO converter and output regulation with load current variations. $V_{Battery}$= 14.4V, $I_{Load}$ @ $V_{Boost}$ and $V_{Reg\text{-}Low}$= 5 mA- 80 mA.

$V_{Boost}$, $V_{Reg\text{-}Low}$ and $V_{Float}$= $V_{FloatH}$−$V_{FloatL}$, with varying load currents. The load current variation is equivalent to the varying number of output channels (up to 4) in the class-D amplifier. The simulations confirmed a load regulation of 0.1 mV/mA for 4-channel equivalent load current transient on $V_{Boost}$ and $V_{Reg\text{-}Low}$.

The output transient response of SIMO converter in the presence of crank and dump transient in $V_{Battery}$ is shown in Fig. 2.19. Clearly from the figure, SIMO converter provides $V_{Battery}$ tracking $V_{Boost}$ and $V_{Float}$ across $V_{Battery}/2$. $V_{Reg\text{-}Low}$ is regulated at 4.5 V across the crank and dump transients. The maximum line regulation at the crank and dump transients are 10 mV/V and 8 mV/V respectively.

The top-level simulation of the SIMO converter indicated a critical issue in the implementation of the floating outputs across $V_{Battery}/2$ and the common mode circuit in Fig. 2.7. In the presence of unbalanced charge on the terminals $L_1$ and $L_2$, the switching of $S_{FloatH}$ and $S_{FloatL}$ injects residual current into the common mode cir-

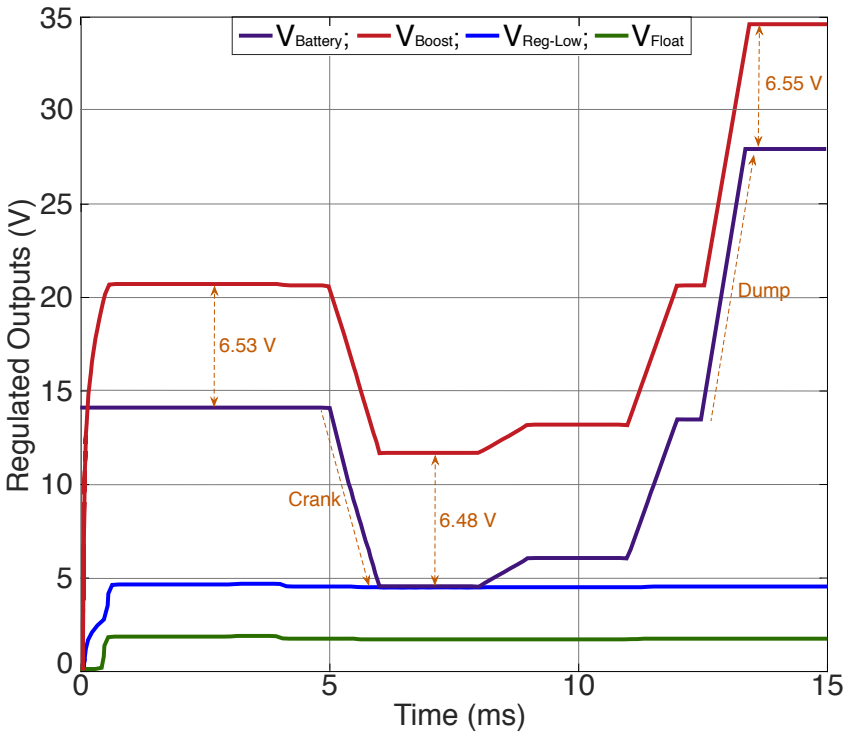


**Fig. 2.19** Regulated outputs of the SIMO converter during the crank and dump transient in $V_{Battery}$.

cuit (CM in Fig. 2.7). This results in glitches on $V_{FloatH}$ and $V_{FloatL}$ due to common mode variation as shown in Figure 2.20. A quasi-balanced injection of the charge while switching $S_{FloatH}$ and $S_{FloatL}$ is important to limit the glitches on the floating outputs $V_{FloatH}$ and $V_{FloatL}$.

## 2.4 Summary

A detailed, application specific analysis of the SIMO converter was performed in this chapter. Equivalence was brought out between the target SIMO converter and a non-inverting SISO buck-boost converter. The steady state and ac small-signal

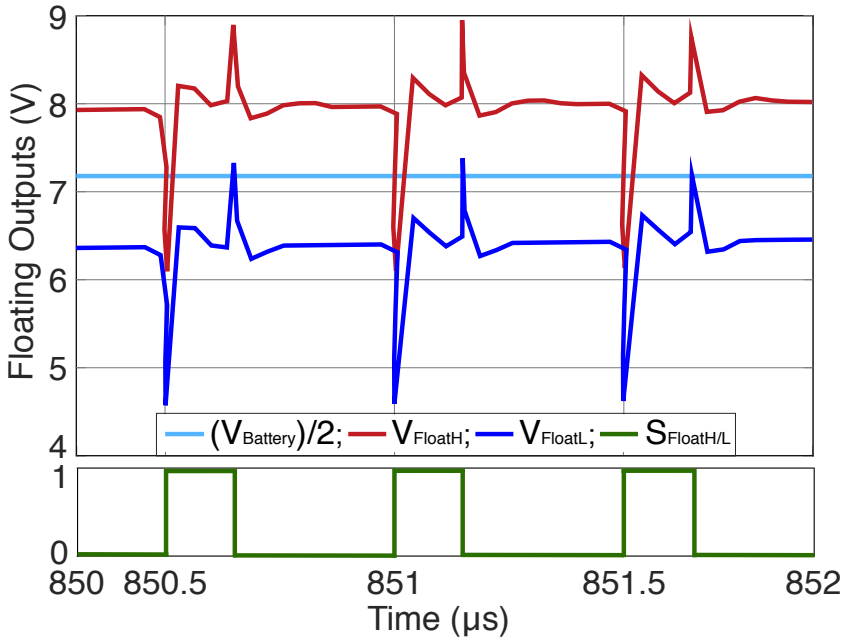


**Fig. 2.20** Glitches on $V_{FloatH}$ and $V_{FloatL}$ resulting from unbalanced charge injection through $S_{FloatH}$ and $S_{FloatL}$.

models of the SIMO equivalent SISO converter were developed. Based on the modeling, (i) the component parameters of the power stage were fixed and (ii) the error processing and controller network parameters were derived. System level simulations were performed with analysis-based parameters to verify the functionality of the SIMO converter. In the following chapter, the models are translated into transistor level physical design and the SIMO dc-dc converter is co-developed with an automotive class-D audio amplifier.

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# Chapter 3

# Design of SIMO dc-dc converter for automotive class-D audio amplifier

## 3.1 Introduction

In this chapter, the SIMO dc-dc converter is designed at the transistor level based on the system-specifications and model-parameters derived in the previous chapter. Firstly, the system is split into multiple blocks depending on the functionality and supply domains. The individual blocks are designed with the devices belonging to suitable voltage rating in the corresponding supply domain. The SIMO converter is co-designed and integrated with a class-D amplifier. Therefore, it is re-configurable and controlled using $I^2C$ communication. A 110-nm BCD process technology is used to implement the design.

## 3.2 Functionality-based block-level supply voltage assignment

SIMO converter is the power management block addressing a HV, automotive application with the battery profile as shown in Fig. 2.1 and described in the previous chapter. Therefore, HV transistors are required to withstand the voltage range of 4.5-40 V. However, the class-D amplifier system is a smart-power IC consisting of digital and analog processing circuits, power output stage, interfaces and pro-

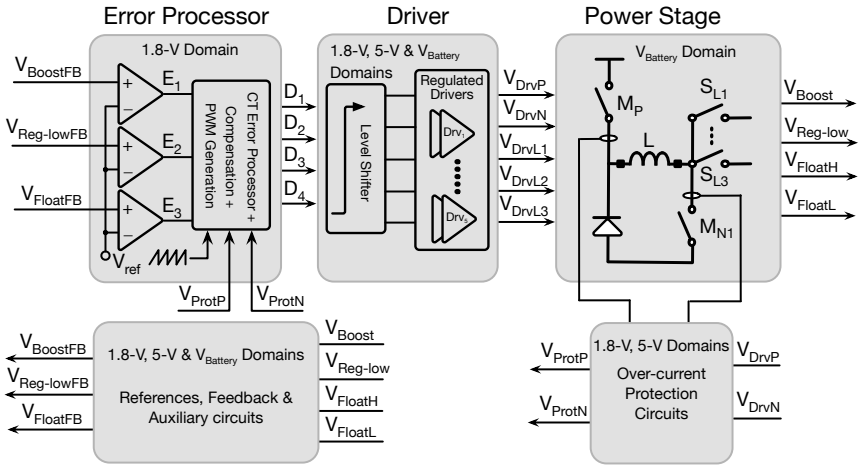


**Fig. 3.1** Block diagram of the SIMO converter indicating the functionality-based supply voltage domains of the blocks.

tection circuits with a combination of both LV and HV supply domains. A monolithic integration of the smart-power ICs is enabled by BCD technologies [1–4]. The state-of-the-art BCD technologies provide CMOS devices for LV supply domains in the system and DMOSFETs with varying voltage ratings for HV supply domains. Therefore the power management blocks in the smart-power ICs may leverage the voltage rating diversity of the devices in the BCD technologies by implementing the power switches with HV DMOSFETs and efficiently designing the feedback error processor using LV CMOS devices.

Fig. 3.1 shows the block diagram of the SIMO converter designed with each block in its functionality-based voltage domain. The Power Stage is supplied by $V_{Battery}$ and implemented using DMOSFETs with proper voltage rating thereof. The feedback Error Processor in designed with LV CMOS devices in 1.8-V domain. Driver block drives the power switches. It is also the interface between Error-Processor in 1.8-V domain and Power Stage in $V_{Battery}$ domain. Therefore, Driver block consists of circuits in 1.8-V, 5-V and HV domains. The auxiliary circuits, references and protection circuits are implemented in suitable voltage domains. Ta-

ble 3.1 provides the list of devices, used to design the SIMO converter, together with their corresponding voltage ratings.

**Table 3.1** List of devices used in the design.

| Device | Voltage Rating (V) |
|---|---|
| DPMOS | 32 |
| DNMOS | 27, 40, 48 |
| CMOS | 1.8, 5 |
| Capacitors (poly) | 1.8, 5 |

## 3.3 Design of the error processor

Based on the analysis and block specifications derived in Chapter 2, the error processor was designed in 1.8 V supply domain. The feedback error amplification and the processing of the errors $E_1$, $E_2$ and $E_3$ according to (2.17) were implemented in continuous-time (CT) using operational amplifiers. Fig.3.2 shows the op-amp based, CT error processor. A 2-stage op-amp with active-load and single ended output was used to implement the arithmetic operations. All the error processing operations are performed at a common mode voltage of $V_{Ref}$= 0.9 V. Fig.3.3 shows the pseudo schematic of the op-amp and Table 3.2 lists the characteristics.

**Table 3.2** Characteristics of the operational amplifier used in CT error-processor.

| Supply | 1.8 V |
|---|---|
| Quiescent Current | 0.2 mA |
| Gain | 90 dB |
| UGF | 40 MHz |
| Phase Margin | 58° |

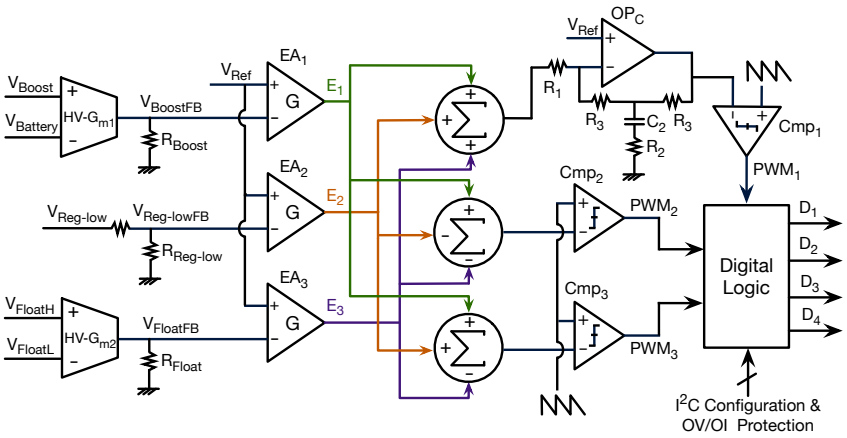


**Fig. 3.2** Op-amp based CT error processor.

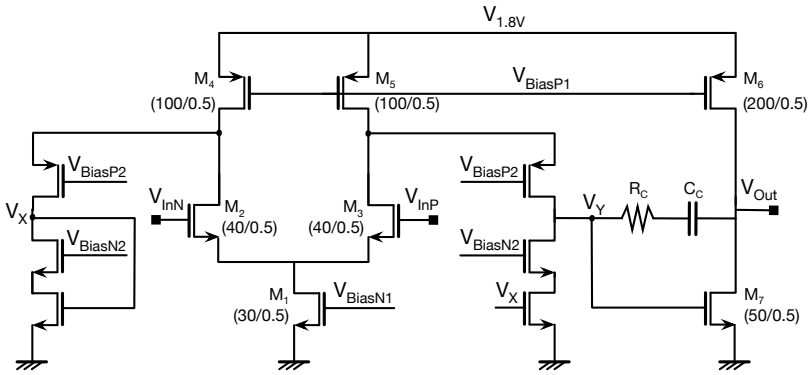


**Fig. 3.3** Schematic of the operational amplifier used in CT error-processor.

The error amplifiers $EA_1$:$EA_3$ provide a gain of G= 20 dB. In Chapter 2, a lead-compensator was proven sufficient to compensate, with 40◦ phase margin, the loop-gain of the SIMO converter across all the load-line variations. Accordingly, the lead-compensator is implemented with $OP_C$, $R_1$:$R_3$ and $C_2$. The passive component values used to realize the transfer function (2.28) are: $R_1$= 1 MΩ, $R_2$= 30 kΩ, $R_3$= 0.5 MΩ, and $C_2$= 50 pF. The PZ pair of the compensator is located at Z= 80 krad/s and P= 600 krad/s.

The feedback control in the error processor in Fig.3.2 is implemented in voltage mode. The sawtooth signal required for the pulse-width modulation (PWM) is generated as shown in Fig.3.4(a). The capacitors $C_1$ and $C_2$ are charged and discharged alternatively through the switches $S_1$:$S_4$. The inverted clock phases Clk and Clkb control the charging the discharging of $C_1$ and $C_2$. The switches $S_5$ and $S_6$ are synchronized with switching of $S_1$ and $S_2$ to alternatively select the discharging phase of the voltages $V_1$ and $V_2$ respectively to generate $V_{Sawtooth}$. Therefore, the frequency of the clock (Clk) required is half the frequency of $V_{Sawtooth}$. The main advantage of the sawtooth generating circuit in Fig.3.4(a) is that, the instantaneous charge/discharge of the capacitor and the resulting glitches on $V_{1.8V}$ (due to cur-

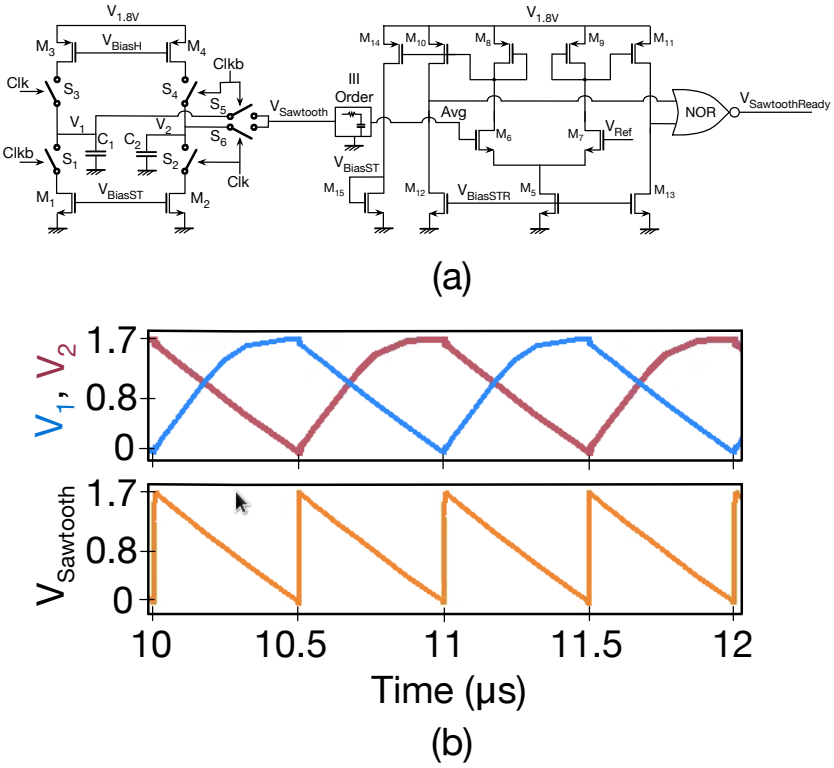


**Fig. 3.4** Sawtooth signal generator. (a) Schematic diagram, (b) Simulation results.

rent spikes) are prevented. $M_3(M_4)$ and $M_1(M_2)$ source and sink 60 μA current into the capacitor $C_1(C_2)$=6 pF, respectively, to generate $V_{Sawtooth}$ with a peak value of 1.7 V.

Fig.3.4(b) shows the simulation results of the sawtooth signal generator. A 1 MHz clock is used to generate $V_{Sawtooth}$ at 2 MHz. $V_{Sawtooth}$ is further averaged (Avg) and compared with $V_{Ref}$ to generate a sawtooth-ready signal, $V_{SawtoothReady}$, as shown in Fig.3.4(a). At turn-on, Avg < $V_{Ref}$ and $I_{M7,9} = I_{M5}$. In this condition, $M_{11}$ is in deep triode resulting in $V_{SawtoothReady}$= 0. The feedback bias signal $V_{BiasST}$ controls the average value of $V_{Sawtooth}$. When Avg ≈ $V_{Ref}$, $I_{M8,9} = I_{M5}/2$. In this condition, the transistors $M_{12}$ and $M_{13}$ are in deep-triode region and $I_{M10,11} = I_{M5}/2$. Therefore, $V_{SawtoothReady}$ is set logic "high". $V_{SawtoothReady}$, together with other control signals from $I^2C$ communication, is used to start-up the SIMO converter.

The error processor outputs are directly compared with $V_{Sawtooth}$ to generate PWM signals. A high-speed comparator, with rail-rail output swing, shown in Fig.3.5 is used for PWM. The comparator consumes a peak current of 100 μA and

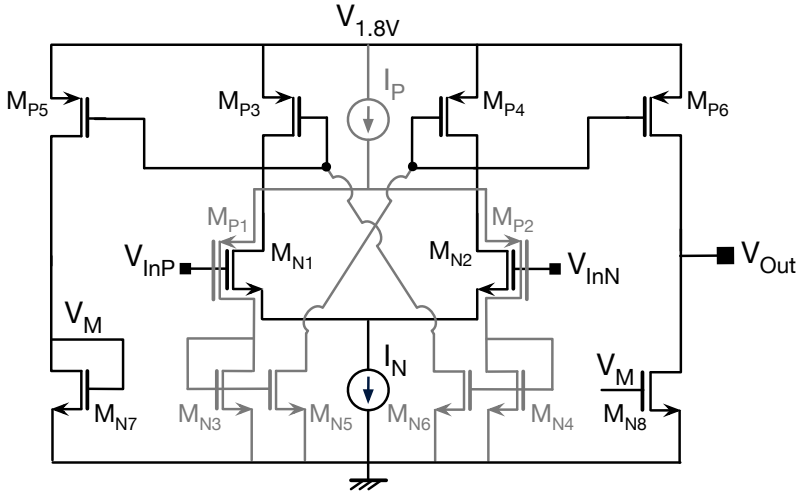


**Fig. 3.5** Schematic of the comparator for PWM.

operates up to a frequency of 100 MHz. The pulse width modulated error signals are combined with (i) configuration/control signals from $I^2C$ communication, (ii) over-voltage (OV) protection interrupts from system state-machine and (iii) over-current (OI) protection signals to generate the switching phases for the power stage in the SIMO converter.

High voltage trans-conductance circuits, HV-$Gm_1$ and HV-$Gm_2$, are used to feedback $V_{Boost}$ and $V_{Float}$ respectively with reference to ground as shown in Fig.3.2. $V_{Boost}$ is regulated with reference to $V_{Battery}$. Therefore, HV-$Gm_1$ generates an output current proportional to the difference $V_{Boost}-V_{Battery}$. Similarly, HV-$Gm_2$ gen-

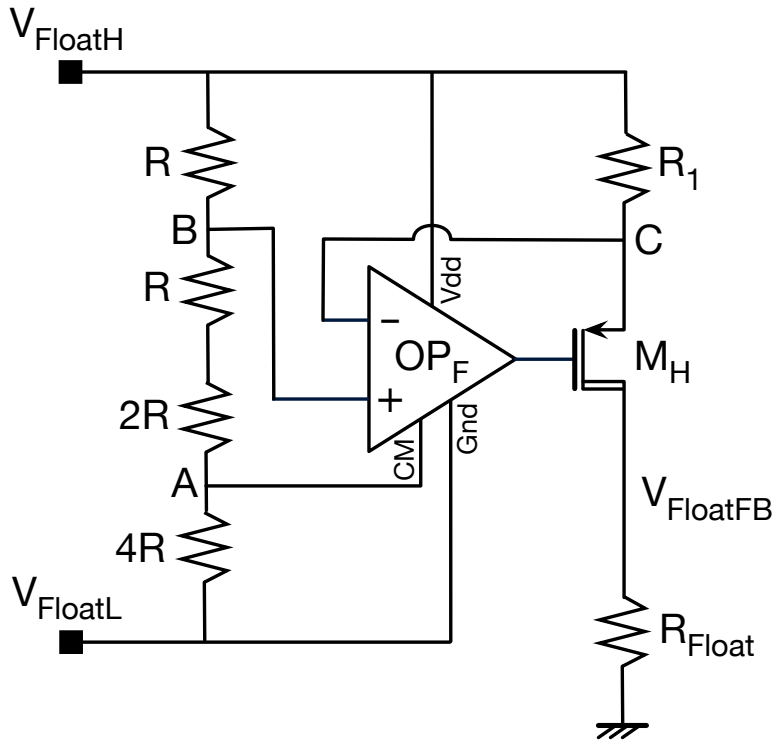


**Fig. 3.6** Schematic of HV-$Gm_2$.

erates an output current proportional to the floating output $V_{Float}t = V_{FloatH} - V_{FloatL}$. The feedback voltages $V_{BoostFB}$ and $V_{FloatFB}$ are regulated with reference to $V_{Ref}$.

Fig.3.6 shows the schematic of HV-$Gm_2$. The op-amp $OP_F$ is supplied between the floating outputs $V_{FloatH}$ and $V_{FloatL}$ with a common-mode at $V_{Float}/2$. For a given R, $R_1$ and $R_{Float}$, $V_{R1}$ determines the output current of HV-$Gm_2$, $I_{MH}$. $V_B$ and $V_C$ are held equal by $OP_F$. Hence, HV-$Gm_2$ transfers $V_{Float}$ to ground referred $V_{FloatFB}$. $V_{FloatFB}$ is regulated equal to $V_{Ref}$ by the SIMO converter. Therefore, in the steady state of the SIMO converter, $I_{MH}=V_{Ref}/R_{Float}$. By varying $R_{Float}$, say digitally, $V_{Float}$ may be programmed to different digital-supplies for the digital core in the class-D amplifier. A similar circuit technique is used for HV-$Gm_1$ to obtain $V_{BoostFB}$ and $V_{Boost}$ is made programmable.

## 3.4 Design of the power stage

Based on the configuration of the switches in the power-stage in Fig. 2.7 and the parameters derived thereof, the HV DMOSFETs with suitable voltage rating are used to realize the power-stage. With reference to Fig. 2.7, Table 3.3 shows the maximum voltages across the switches in the power-stage resulting at the dump condition of $V_{Battery}$=40 V. Realization of some of the switches, particularly P- DMOSFETs is found to be area expensive at $V_{Battery}$> 32 V. Therefore, a trade-off is reached and SIMO converter regulation is provided upto $V_{Battery}$ = 30 V. When $V_{Battery}$ exceeds 30 V, SIMO converter enters idle-state to protect the power switches.

An important issue highlighted in the system-model and simulation, in Chapter 2, is with respect to the common-mode fluctuation due to unbalanced charge injection into the switches $S_{FloatH}$ and $S_{FloatL}$ that feed the floating output. There are two main contributors to the common-mode fluctuations in $V_{Float}$. Firstly, the excess charge built-up on node $L_2$ (see Fig. 2.7) compared to the grounded node $L_1$ during $V_{Boost}$

**Table 3.3** Maximum voltages across switches in the power-stage.

| Switch | Max. Voltage @$V_{Battery}$ = 40 V | Max. Voltage @$V_{Battery}$ = 30 V |
|---|---|---|
| $S_{P1}$ | 40 | 40 |
| $S_{P2}$ | 40 | 30 |
| $S_{P3}$ | 47 | 37 |
| $S_{Boost}$ | 48 | 37 |
| $S_{Reg\text{-}low}$ | > 40 | 32 |
| $S_{FloatH/L}$ | > 30 | < 25 |

and $V_{Reg\text{-}low}$ phases result in current injection in the common-mode circuit when $S_{FloatH}$ and $S_{FloatL}$ turn on. The second contributor to the fluctuations in $V_{FloatH}$ and $V_{FloatL}$ is the mutual coupling of the bond-wire inductances that carry large di/dt when the power switches turn on/off.

Two techniques are adopted to minimize the common mode fluctuations due to unbalanced charge injection into the common-mode circuit. Firstly, during the load delivery phase of the SIMO converter, the switching sequence of the outputs follows the order (i) $V_{Boost}$, (ii) $V_{Reg\text{-}low}$ and (iii) $V_{Float}$. Secondly, the node $L_2$ is prevented from building up excess charge during the transition of load delivery from $V_{Reg\text{-}low}$ to $V_{Float}$. The switching phases $S_{Reg\text{-}low}$ and $S_{Float}$ are overlapped and the corresponding switches are switched quasi-asynchronously. This technique avoids the requirement of dead-time between the two phases $S_{Reg\text{-}low}$ and $S_{Float}$ and results in the transition of $V_{L2}$ from $V_{Reg\text{-}low}$ to $V_{FloatH}$, at the node $L_2$, without charging up to $V_{Boost}$ as shown in Fig. 3.7.

The fluctuations at the floating outputs, $V_{FloatH}$ and $V_{FloatL}$, due to bond-wire mutual coupling are reduced with the help of auxiliary linear regulators together with filtering and bond-wire separation. Recalling from the specifications, $V_{FloatH}$= ($V_{Battery}$)/2+0.9 V and $V_{FloatL}$= ($V_{Battery}$)/2−0.9 V. A pair of linear regulators are used to regulate/clamp $V_{FloatH}$ and $V_{FloatL}$ at ($V_{Battery}$/2)±0.8 V. As shown in Fig. 3.8, the pair of linear regulators $Reg_{High}$ and $Reg_{Low}$, (i) regulate $V_{Float}$=1.6 V before

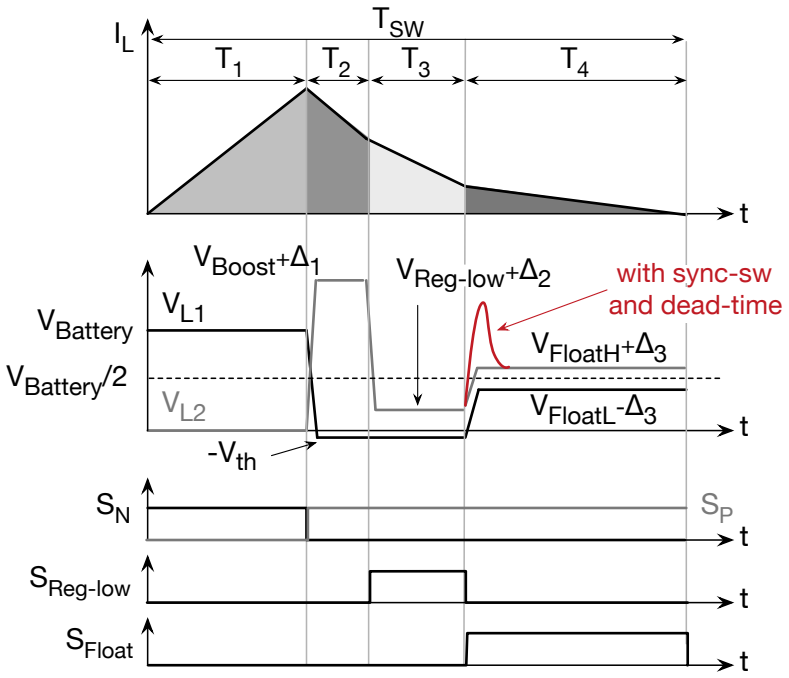


**Fig. 3.7** Quasi-asynchronous switching technique used in SIMO converter to mitigate the common mode fluctuations at the floating output.

the start-up of SIMO converter and (ii) clamp $V_{FloatH}$ and $V_{FloatL}$ at ($V_{Battery}$/2)±0.8 V during SIMO converter regulation of $V_{Float}$=1.8 V. A pair of filter capacitors $C_{Filter}$, connected as shown in Fig. 3.8, filter out the fluctuations at $V_{FloatH}$ and $V_{FloatL}$ due to bond- wire coupling and any residual unbalanced charge injection through $S_{FloatH}$ and $S_{FloatL}$. The mutual coupling at the nodes $A_1(A_2)$ and $B_1(B_2)$ in Fig. 3.8 are reduced by sufficient separation of the bond-wires.

Based on (i) the power-stage modeled in Fig. 2.7, (ii) the maximum voltage requirements of the switches, and (ii) the switching sequence and circuit techniques required to mitigate the common-mode variation of the floating output, the power-stage shown in Fig. 3.9 is configured for the SIMO converter. The switches are

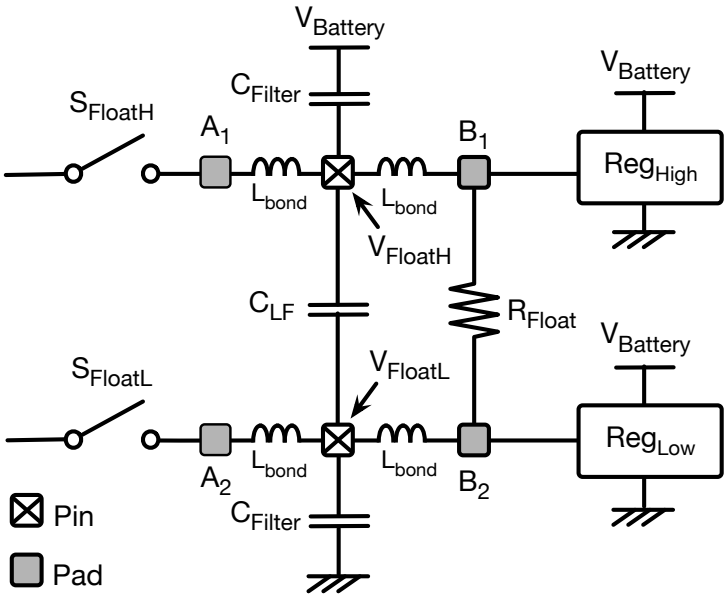


**Fig. 3.8** Circuit technique to mitigate the fluctuations at $V_{FloatH}$ and $V_{FloatL}$.

**Table 3.4** Voltage ratings of the switches used in the power-stage.

| Switch | Voltage rating (V) |
|---|---|
| $M_P$ | 32 |
| $M_N$ | 48 |
| HV-$D_N$ | 27 |
| HV-$D_B$ | 48 |
| $M_{N2}$ | 40 |
| $D_{RL}$ | 5 |
| $M_{N3,4}$ | 27 |
| HV-$D_{FH/L}$ | 27 |

configured and driven such that, the SIMO converter charges the inductor L synchronously and delivers the loads quasi-asynchronously. The switches used in the power-stage together with their voltage ratings are listed in Table 3.4. The component parameters of the power-stage derived in Table 2.2 are used to size the power

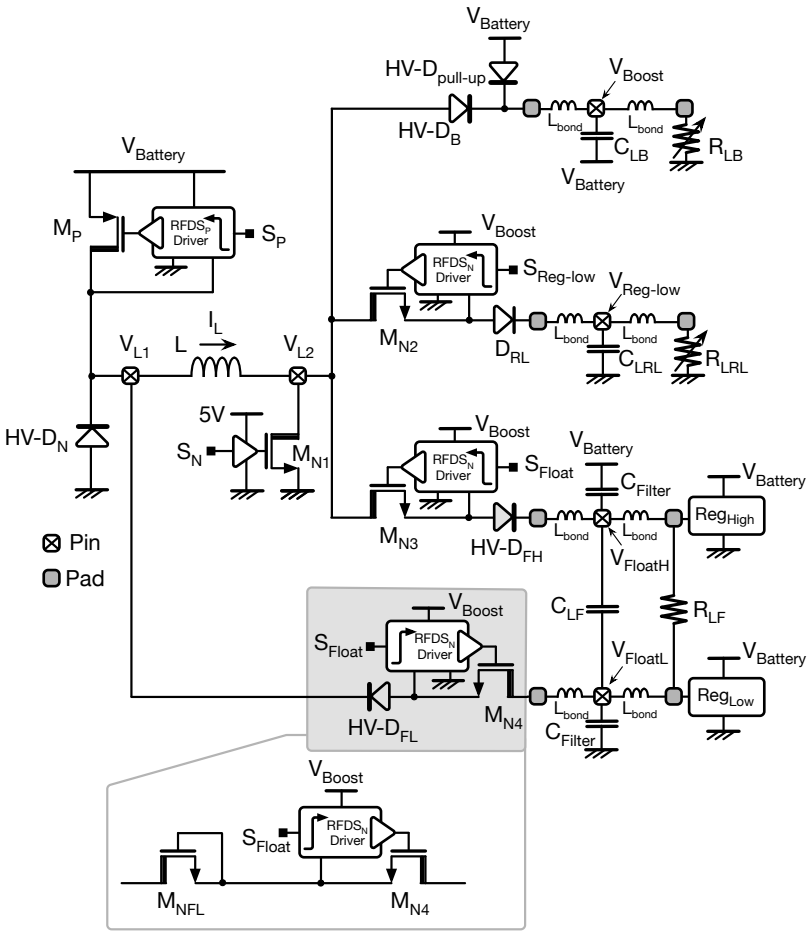


**Fig. 3.9** Schematic of the power-stage of the SIMO converter.

switches and select off chip passives components required. Small off-chip capacitors $C_{Filter}$ (10 nF) are used to filter common-mode ripples in $V_{Float}$.

The HV switches used for the load current delivery to $V_{Reg\text{-}low}$, $V_{FloatH}$ and $V_{FloatL}$ are unidirectional and implemented by series connected N-DMOSFETs, with suitable voltage rating, in switch and diode configuration. The use of quasi-asynchronous load delivery automatically handles the discontinuous conduction mode during low load condition. In addition, there is no requirement of non-

overlapped switching and dead-time control. Therefore, slight overlapping of $S_{Reg\text{-}low}$ and $S_{Float}$ is beneficially used to mitigate the fluctuations in the common-mode of $V_{Float}$.

Regulated Floating Dual Slope (RFDS) drivers are used to drive the HV, quasi-asynchronous switches across the gate and floating-source terminals, independently of the voltages at their i/o terminals. All the drivers provide a $V_{GS}$ of 5/0 V to turn on/off the power switches. RFDS drivers are supplied by $V_{Boost}$, which is one of the outputs of the SIMO converter. This is made possible by reconfiguration and programmable start-up sequence of the SIMO converter as explained in further sub-section.

## 3.5 Design of the drivers for the power switches

The power switches require the gate capacitance to be charged/discharged in order to turn on/off the switches. A driver circuit is used to provide the charge required to turn on/off the power switch. The speed of turning on/off the switch depends on the driver strength. In a DMOSFET switch, the gate-source voltage ($V_{GS}$) must be varied between 0 and $V_{GSMax}$ to modify its state of conduction. $V_{GSMax}$ is the rated maximum gate-source voltage of the switch. For $V_{GS} > V_{GSMax}$, the device suffers gate-oxide breakdown. Therefore, the driver is required to be regulated such that the power switch is driven safely with $V_{GS} < V_{GSMax}$.

In the SIMO converter, the turn on/off of the load-side power switches result in di/dt induced voltage fluctuations on the bond-wires of the package. The severity of the effect depends on the speed of switching. In addition, the bond-wires are mutually coupled with the adjacent ones. As noted in the design of power-stage, the mutually coupled bond-wires induce fluctuations on the floating outputs $V_{FloatH}$ and $V_{FloatL}$ which is a critical issue in the application. Therefore, the drivers must

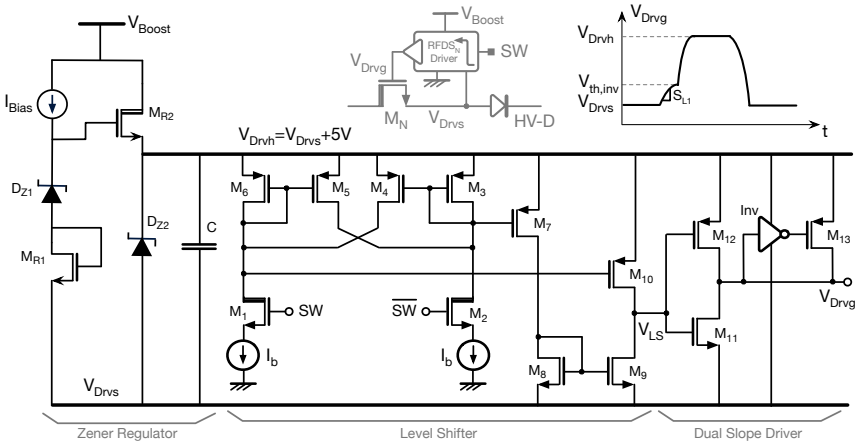


**Fig. 3.10** Schematic of the regulated floating dual-slope (RFDS) driver.

be optimized to drive the switches sufficiently, yet checking the di/dt on the bond-wires. As seen in Fig. 3.9, regulated floating and ground-referred drivers are required to drive various switches in the power-stage of the SIMO converter.

A regulated floating dual-slope (RFDS) driver is required to drive the power-switches with large voltage swings at the i/o terminals and to limit the di/dt as the switch turns on/off. The schematic of the RFDS driver used in the SIMO converter is shown in Fig. 3.10 together with a representative output. The driver consists of three sub-blocks namely (i) a regulator, (ii) a level-shifter and (iii) a dual-slope driver. A Zener voltage regulator is used to provide a regulated supply of $V_{Drvs}$+5 V to the driver and limit the maximum diving voltage within $V_{GSMax}$ of the power switch. A filter capacitor C= 20 pF is required to provide the filtering at $V_{Drvh}$.

A level-shifter, comprising of $M_1$:$M_6$ transistors, transfers the error processor generated switching phase SW in 1.8-V domain to the corresponding HV domain of the switch being driven. The positive feedback loop established by $M_4$ and $M_5$ speeds up the circuit to perform the level-shifting operation within 5 ns. A differential to single ended converter controls the dual slope buffer. A smaller transistor

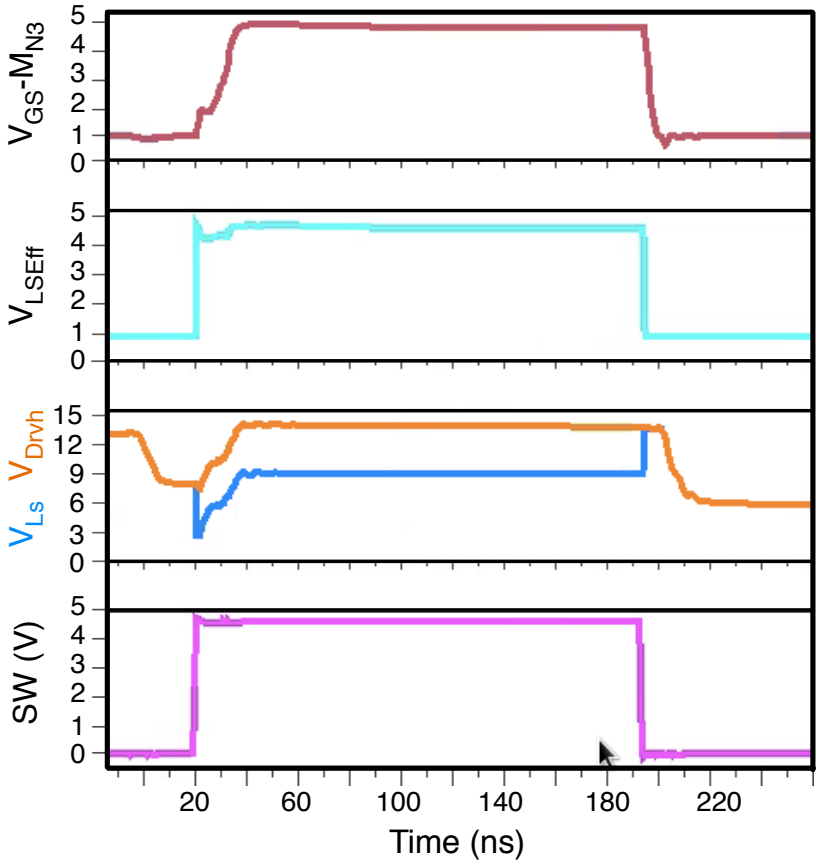


**Fig. 3.11** Schematic of the regulated floating dual-slope (RFDS) driver.

$M_{12}$ initiate the driving of the power switch with $S_{L1}$ until the inverter, Inv, turns on $M_{13}$ to augment the slope of driving to $S_{L2}$.

A complementary version of the driver in Fig. 3.10, $RFDS_P$, is used to drive the switch $M_P$ in the power-stage. Similarly, the power-switch $M_N$ in Fig. 3.9 is driven using a ground-referred dual-slope driver.

Fig. 3.11 shows the simulation results at of $RFDS_N$ driver, driving the switch $M_{N3}$ in the power-stage at the steady state of the SIMO converter. The figure clearly shows the ability of RFDS driver in driving the switch across its floating terminals

and independent of the voltages at its i/o terminals. SW signals of pulse width up to 5 ns are driven efficiently by RFDS driving technique in the SIMO converter.

## 3.6 Design of the protection circuits

The SIMO converter in the automobile application is a high voltage power converter with $V_{Battery}$ varying in the range 4-40 V. The integrated power switches and the off-chip passive components require a current protecting circuit to limit the currents below the maximum current ($I_{Max}$) rating. Any current in the devices, exceeding $I_{Max}$, may result in the breakdown of the device. Accordingly, over current protection (OCP) circuits are used in the SIMO converter to (i) limit the inrush currents in the power-stage below 1.5 A, (ii) enable soft-start of the SIMO converter and (iii) protect the power stage in case of a short on $V_{Battery}$-ground path through the power switches.

The current protection technique adopted to protect the power-stage in Fig. 3.9 is shown in Fig. 3.12(a). The inductor charging switches $M_P$ and $M_{N1}$ are the largest voltage and current handling switches in the SIMO converter. Hence, $M_P$ and $M_{N1}$ are protected using the over current protection circuits $OCP_P$ and $OCP_N$. This ensures limiting the inrush current during the start-up of the SIMO converter below the threshold of the protection circuits $OCP_P$ and $OCP_N$. In addition, the power stage is protected against any short-circuit current. The current limiting threshold, $I_{ThN}$ of $OCP_N$ is set larger than $I_{ThP}$ of $OCP_P$. As a result, $OCP_N$ offers primary protection to the SIMO converter. The presence of OCP circuits has, additionally, simplified the soft-start of the SIMO converter. As the inrush current is limited below $I_{ThN}$, additional reference voltage ($V_{Ref}$) ramping circuits with off-chip passive components, conventionally used, are not required [5,6]. OCP circuits provide a quasi soft-start to

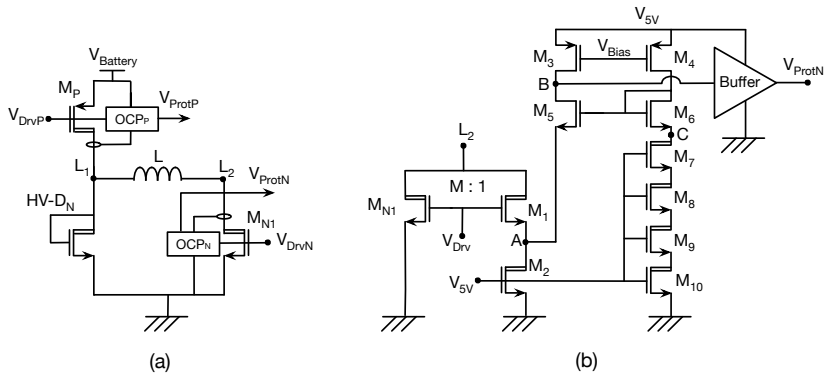


**Fig. 3.12** Over current protection. (a) OCP technique adopted in the power-stage, (b) Schematic of $OCP_N$ circuit.

the SIMO converter and self-adjust the start-up time depending on the load currents and output capacitors.

$OCP_P$ and $OCP_N$ are complementary circuits to protect n-channel and p- channel DMOSFETs respectively. The schematic of $OCP_N$ circuit is shown in Fig. 3.12(b). $M_1$ and $M_2$ are a matched pair that halve $V_{L2}$ at A. The threshold current is fixed by $I_{M4}$. The ON resistance of $M_7$-$M_{10}$ is set proportional ($\times$K) to $R_{ON}$ of the device being protected, $M_{N1}$. Therefore, a voltage proportional to $V_{L2}/2$ is generated at C. The matched pair $M_5$-$M_6$ and the current mirror pair $M_3$-$M_4$ form a current mode comparator. When $V_A<V_C$, $I_{MN1}$ is lower than $K\times I_{M4}$. At the limiting condition, $V_A=V_C$ and $I_{MN2} = I_{ThN} = K\times I_{M4}$. In the presence of inrush-current, $I_{MN1}>I_{ThN}$ and $V_A>V_C$. Therefore, the inrush-current detecting signal $V_{ProtN}$ sets high to turn-off $M_{N1}$. The protection signal $V_{ProtN}$ is programmable to different current level detections through $I_{M4}$. The effectiveness of the over current protection circuits in inrush current limiting and soft-starting the SIMO converter is shown in Fig. 3.13. The OCP circuits limit the inrush current to a maximum value of 1.5 A and soft-start the SIMO converter within 50 μs.

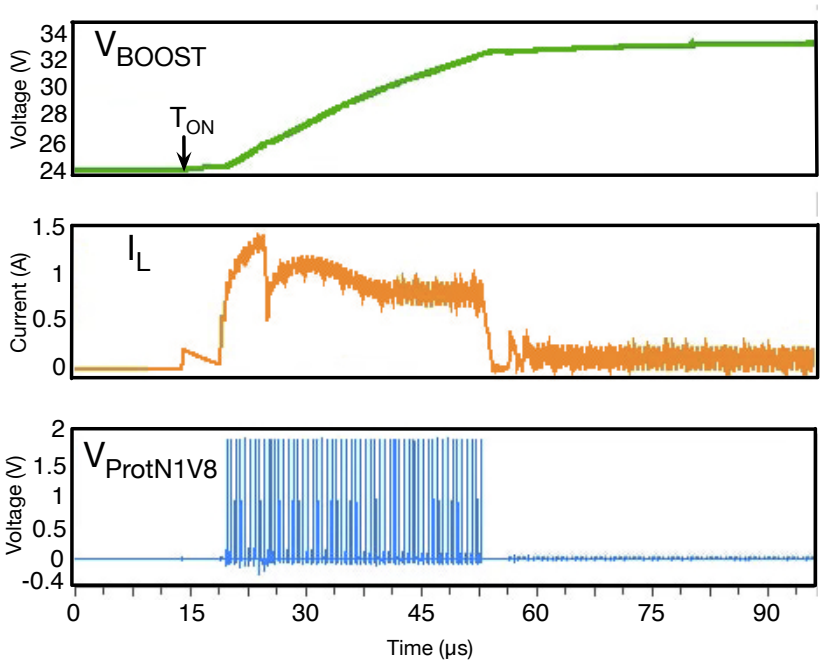


**Fig. 3.13** Inrush current limiting and soft-start of the SIMO converter.

## 3.7 Start-up sequence of the SIMO converter and the system state-machine

Depending on the system requirements and architecture of the SIMO converter, a unique start-up sequence is used. As observed previously, RFDS drivers are supplied by $V_{Boost}$. This requires the availability of $V_{Boost}$ during the start-up of SIMO converter. Therefore, the SIMO converter is configured to start-up in two phases. In the first phase, $V_{Boost}$ alone is regulated by configuring SIMO converter as a boost converter. Once $V_{Boost}$ is regulated, it is available to supply RFDS drivers. After a fixed start-up pulse, the converter is restarted in normal SIMO mode in the second phase. At the end of two-step start-up phase, the SIMO converter is ready to sup-

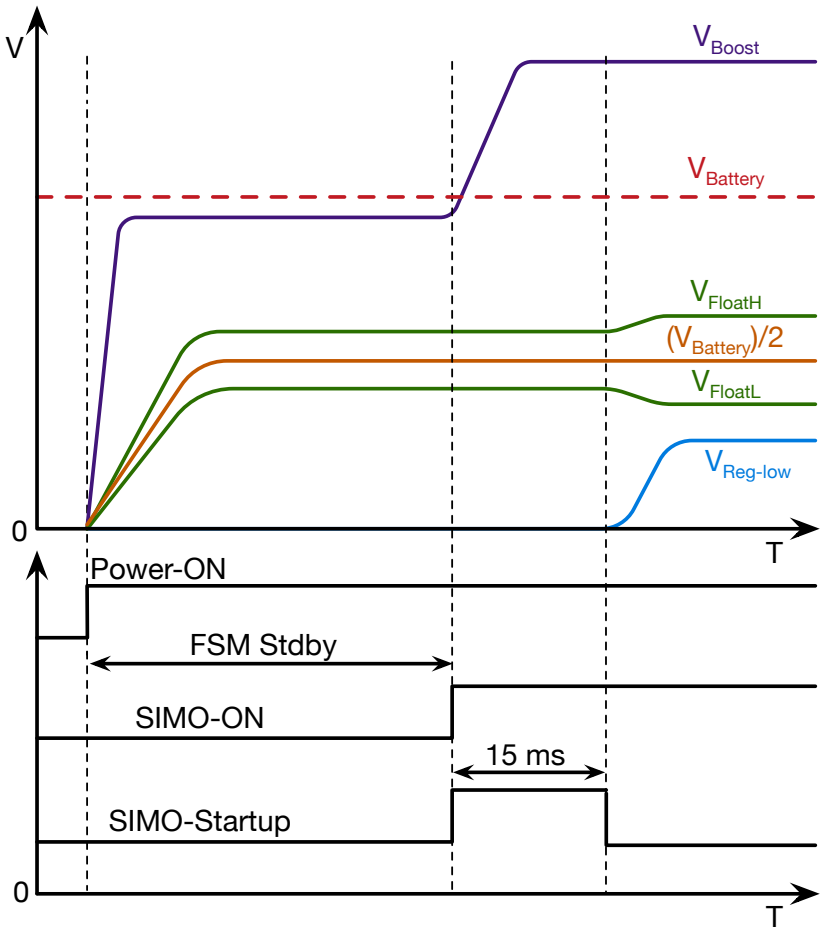


**Fig. 3.14** Start-up sequence of the SIMO converter.

ply the channels of class-D amplifier. Fig. 3.14 shows the start-up sequence of the SIMO converter.

The start-up of the SIMO converter, its configuration, over-voltage protection interrupts, output low-voltage monitoring and restart are all handled by a finite-state-machine (FSM) in the digital core of the class-D amplifier system. The auxiliary, linear regulators at the floating outputs supply the digital core during standby and start the FSM in Fig. 3.15. After start-up, SIMO converter supplies the digital core

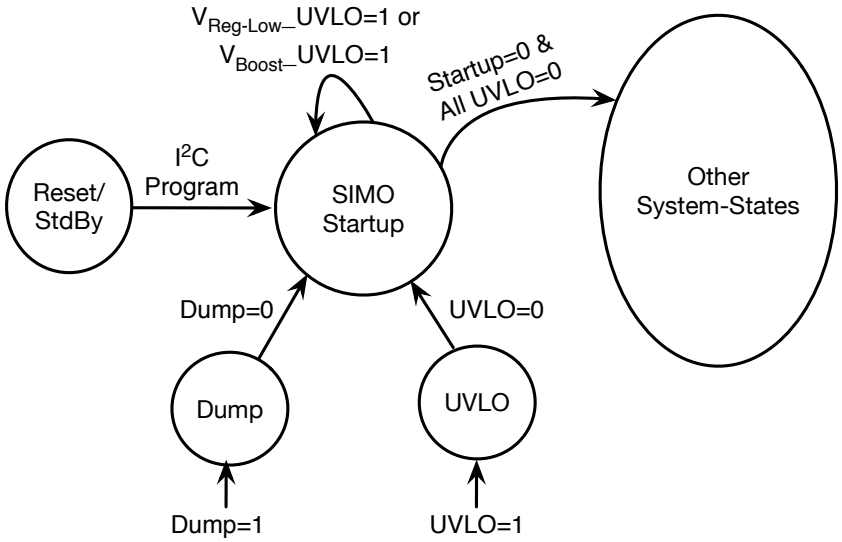


**Fig. 3.15** Finite state machine of the system.

and FSM monitors the system. The digital core, through $I^2C$ programming, has enabled the implementation of a re-configurable SIMO converter.

## 3.8 Power dissipation in the SIMO converter

As observed previously in Fig. 3.1, the SIMO converter system comprises of 4 major blocks operating in different voltage domains *viz.* 1.8 V, 5 V and $V_{Battery}$. The signal transition form one domain to another requires suitable level shifting operation among the voltage domains. The power dissipation $P_{Diss}$ in each of the blocks together with the signal transitions between different voltage domains in Fig. 3.1 contribute to the loss of efficiency. In order to relatively compare the contribution of power dissipation in each block, the block-wise evaluation of power dissipation was performed. Fig. 3.16 shows the block-wise distribution of power dissipation in the SIMO converter at peak efficiency and the nominal and step-up values of $V_{Battery}$.

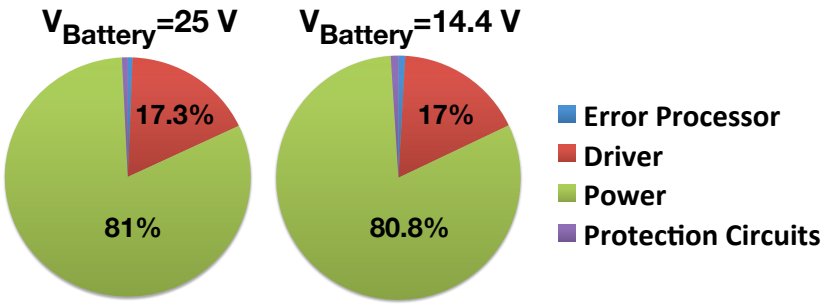


**Fig. 3.16** Block-wise power dissipation in SIMO converter.

At both the values of $V_{Battery}$ (14.4 V and 25 V), the power stage dissipates power exceeding 80% of the total power dissipation of the SIMO converter ($P_{DissTotal}$). The driver block which drives the power stage dissipates around 17% of $P_{DissTotal}$. The error processor and the protection circuits consume less than 1% of $P_{DissTotal}$ at both the values of $V_{Battery}$.

## 3.9 Layout of the SIMO converter

The SIMO converter is physically designed and integrated with a class-D amplifier for fabrication using a 110-nm BCD technology. The active area occupied is 2.5 $mm^2$. Fig. 3.17 shows the layout of the SIMO converter.

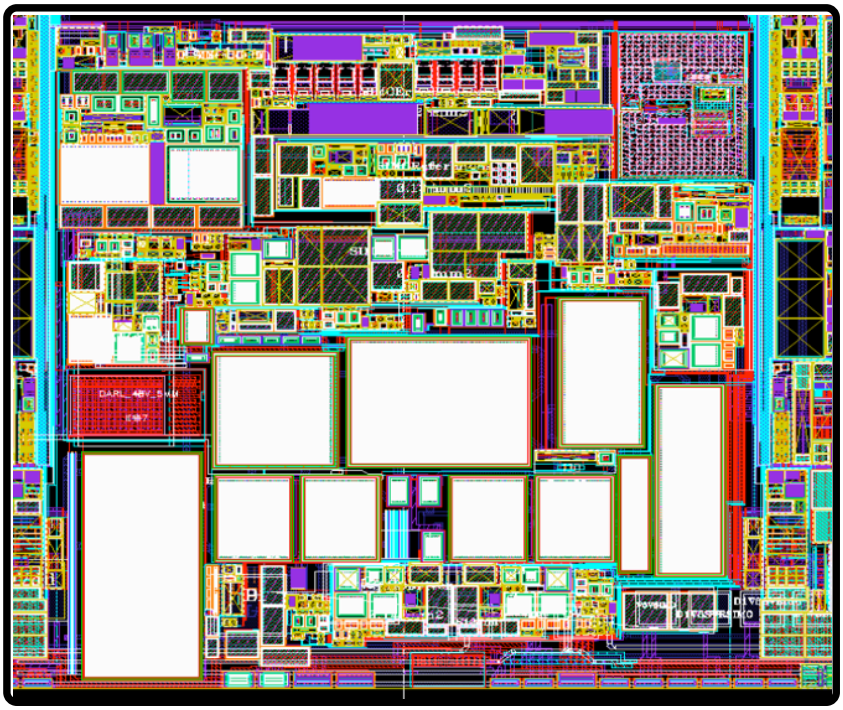

**Fig. 3.17** Layout of the SIMO converter.

## 3.10 Summary

This chapter presented the schematic design of the SIMO converter based on the modeling and analysis done previously. The system is divided into different voltage domains. All the major circuit blocks are described together with specifications. Important simulations results of the circuit blocks are presented. The circuit is physically designed and fabricated. In the following chapter, the detailed measurement results of the SIMO converter are provided.

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# Chapter 4

# Measurement results of SIMO dc-dc converter

## 4.1 Test-chip and board design

The SIMO dc-dc converter, modeled and designed in the previous chapters, was integrated with a class-D audio power amplifier for car-radio. The prototype was fabricated using an 110-nm BCD process offered by STMicroelectronics. The SIMO converter occupies a total active area of 2.5 $mm^2$. Fig. 4.1 shows the micrograph of the integrated circuit (IC) with annotated active area of the SIMO converter.

The die of the car-radio IC was packed in a QFN package with 64 pins. The SIMO converter requires 6 adjacent, dedicated pins only. 4 pins are used for the regulated outputs and 2 pins for switching the inductor. Separate battery and ground connections (with sufficient bond-wire separation) were provided to noise sensitive circuit blocks on the die. All the references and commands required for the SIMO converter were internally generated in the IC.

A 4 layered FR4 test PCB was used to evaluate the performance of the SIMO converter. The populated PCB with the car-radio IC bottom-side mounted is shown in Fig. 4.2.The loads of the SIMO converter were connected externally. A port was provided on the PCB for $I^2C$ communication with a computer. Ceramic capacitors

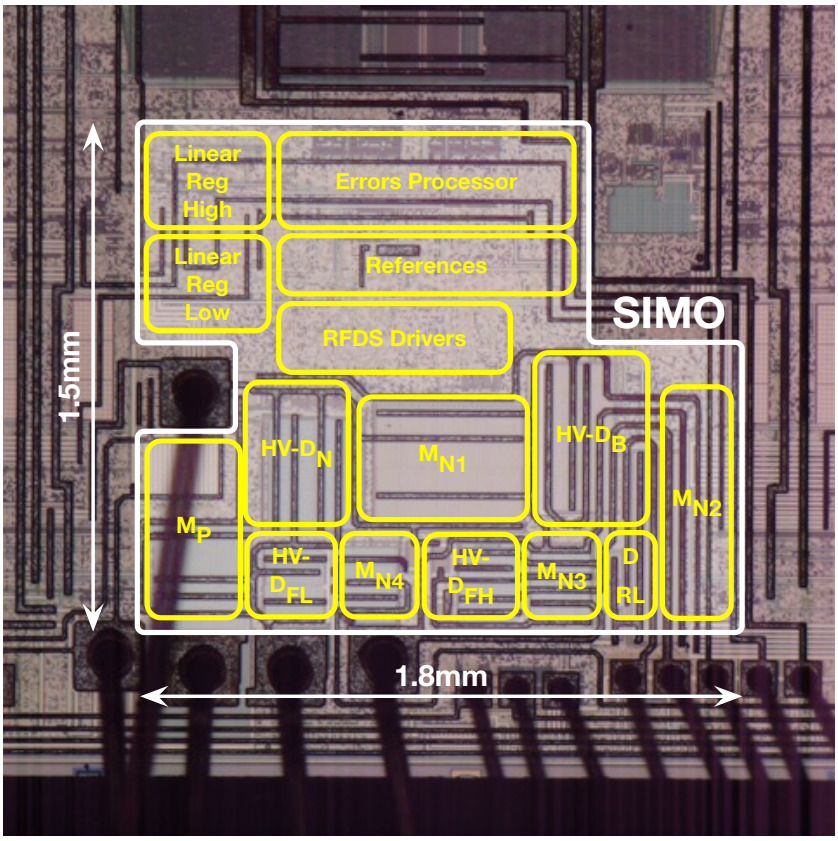


**Fig. 4.1** Micrograph of the chip showing the active area of SIMO converter.

from Murata were used for filtering the outputs. The switching inductor was a thin film inductor from Coilcraft.

## 4.2 Measurement Setup

The measurement set up used for the evaluation of the performance of SIMO converter is shown in Fig.4.3. The setup was in place to test the SIMO converter standalone. The power supply was provided using a programmable R&S supply. An ex-

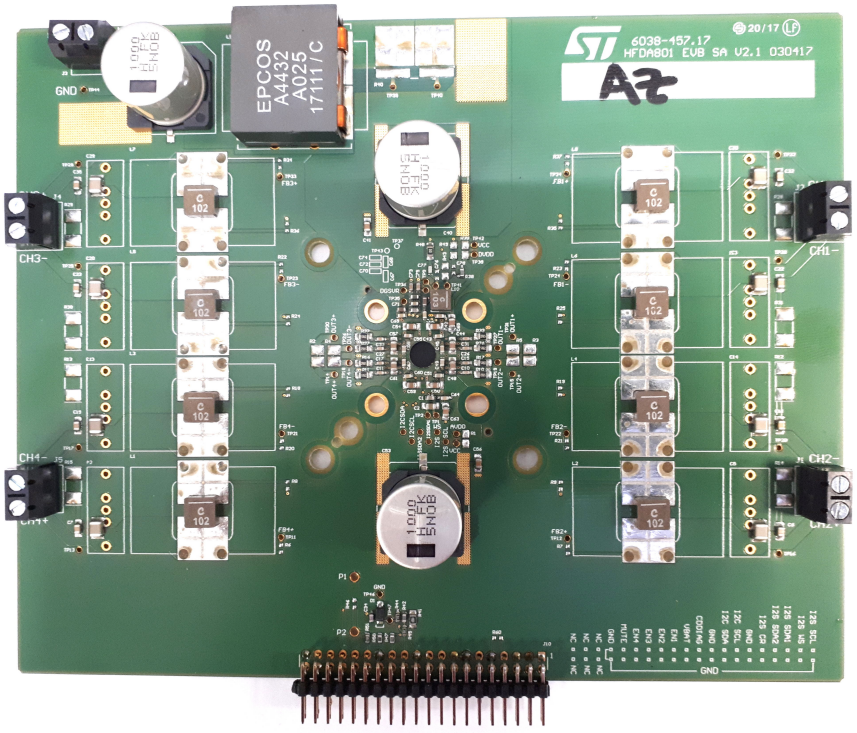


**Fig. 4.2** PCB used to evaluate the SIMO converter.

ternal function generator was used to feed the clock signal. Lecroy-WavePro high precision oscilloscope was used to measure the transient outputs of the SIMO converter. A PC was used to communicate $I^2C$ commands to the evaluation board. External resistors and potentiometers were used for load transient.

## 4.3 Start-up sequence and line-transient response of the SIMO converter

The startup sequence of the SIMO converter at $V_{Battery}$=14.4 V is shown in Fig. 4.4. At the "Turn ON" instant the converter is powered and the internal LDOs supply the digital core. $V_{Boost}$ is charged to one diode drop below $V_{Battery}$ by the pull-up

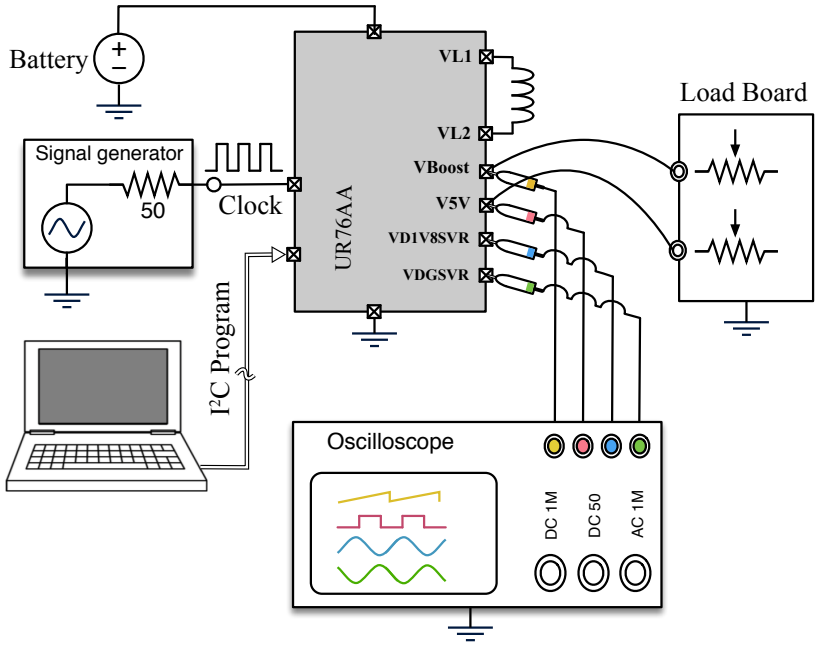


**Fig. 4.3** Test setup for the evaluation of the SIMO converter.

diode. On receiving the $I^2C$ command, the SIMO converter starts at "Boost Only ON" instant indicated in the figure. $V_{Boost}$ is regulated at 6.5 V above $V_{Battery}$ in 50 µs. After a 15-ms start-up pulse, the SIMO operation begins at the instant "SIMO ON". $V_{Reg\text{-}low}$ charges to its regulated value of 4.5 V. The SIMO converter regulates the floating outputs, $V_{FloatH}$ and $V_{FloatL}$. During SIMO operation, the LDOs clamp $V_{FloatH}$ and $V_{FloatL}$ at 100 mV around their regulated values. In the encircled zone of the Fig. 4.4, LDO-SIMO regulation transient of the floating outputs may be closely observed across the instant "SIMO ON". Difference floating output ($V_{FloatH}-V_{FloatL}$) changes from 1.6 V to 1.8 V at "SIMO ON". A non-differential regulation of $V_{FloatH}$ and $V_{FloatL}$ by the SIMO converter is attributed to the unbalanced floating load. The high-side regulator ($Reg_{High}$ in Fig. 3.9) supplies a small, grounded load current and fixes $V_{FloatH}$ during SIMO regulation. The SIMO con-

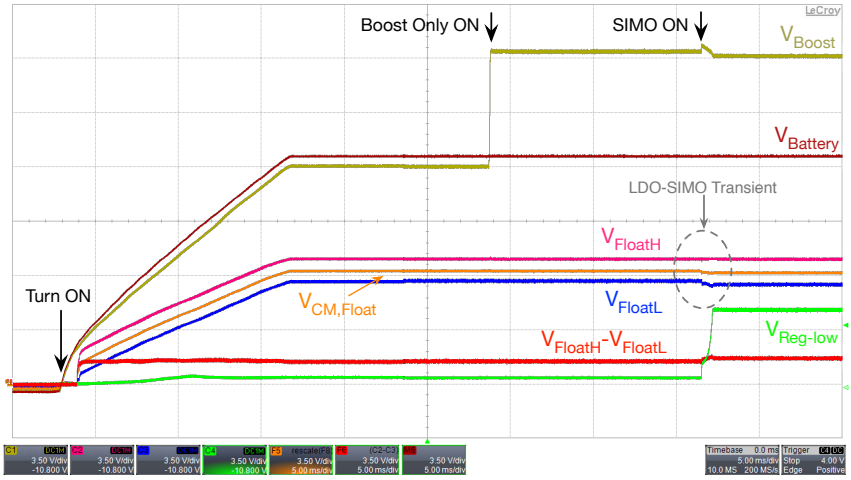


**Fig. 4.4** Start-up sequence of the SIMO converter.

verter supplies the the differential load between $V_{FloatH}$ and $V_{FloatL}$. As a result, $Reg_{Low}$ clamps $V_{FloatL}$ at 200mV below the pre-"SIMO ON" linear regulated value.

Output regulation together with battery tracking ability is one of the salient features required of the SIMO converter. Accordingly a dc supply, programmed to resemble the automotive battery profile of Fig. 2.1, was used to evaluate the battery tracking ability of the converter. The regulated outputs of the converter during $V_{Battery}$ transient are shown in Fig. 4.5. $V_{Battery}$ was varied between 4.5-27 V. The upper value of $V_{Battery}$ during load-dump is limited to 27 V by the voltage rating of the power switches used in the design. For $27<V_{Battery}<40$ V, the protection circuits disable the SIMO converter and it remains idle. The line regulation of the outputs at the crank and load-dump conditions of $V_{Battery}$ are annotated in Fig. 4.5. The maximum line regulation values of 16.2 mV/V and 10.1 mV/V are observed at $V_{Reg-low}$ and $V_{Boost}$ respectively during crank. During rest of the transients of $V_{Battery}$, line regulation at the converter outputs remain within 8 mV/V.

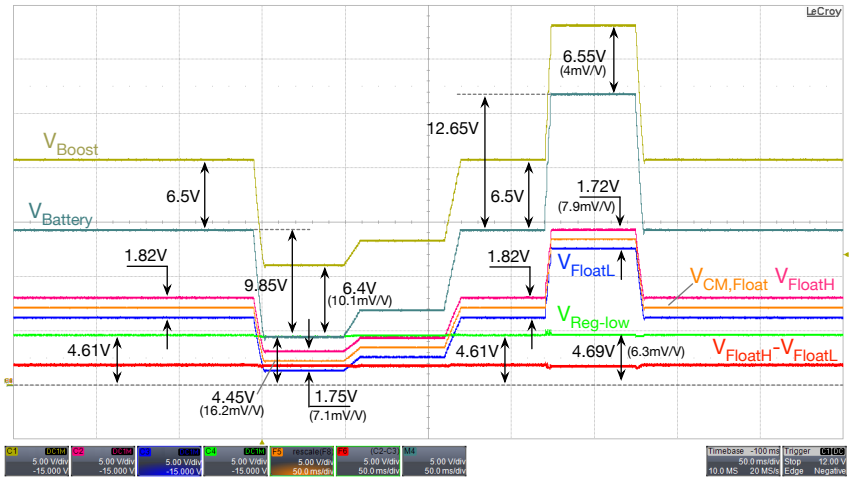


**Fig. 4.5** Output transient of the SIMO converter in response to automotive battery variations.

## 4.4 Steady state response of the SIMO converter

The steady state response of a SIMO dc-dc converter provides dual information on the stability of the converter and the output ripples. The steady state response of the converter in 2-channel equivalent load current on $V_{Boost}$ and $V_{Reg\text{-}low}$ is shown in Fig. 4.6 at the nominal value of $V_{Battery}$= 14.4 V. $V_{Boost}$, $V_{Reg\text{-}low}$ and the floating difference output $V_{FloatH}-V_{FloatL}$ are plotted ac coupled. Ripple values lower than 25 mV are observed on the outputs of the converter. The ripples caused by coupling of the switching noise dominate in the 2-channel load condition used. Fig. 4.6 also shows the switching voltage across the inductor in steady state. Periodic switching of the inductor indicates the stability of the SIMO converter.

A similar experiment was repeated at the stepped-up value of $V_{Battery}$= 25 V in 2-channel load condition on $V_{Boost}$ and $V_{Reg\text{-}low}$. Fig. 4.7 shows the steady state waveforms of the inductor current, $I_L$, and the switching voltages across the inductor, $V_{L1}$ and $V_{L2}$. A stable, periodic switching of $I_L$, $V_{L1}$ and $V_{L2}$ at 2.4 MHz is observed in the figure.

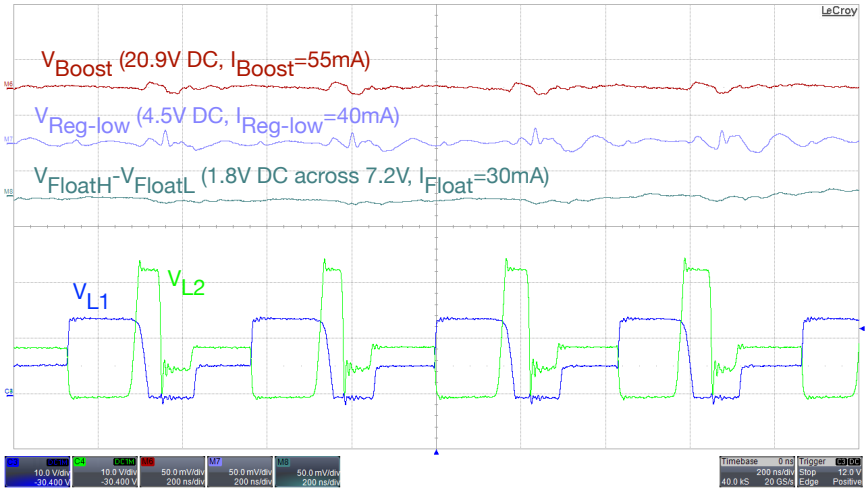


**Fig. 4.6** Steady state response of the SIMO converter at $V_{Battery}$= 14.4 V.

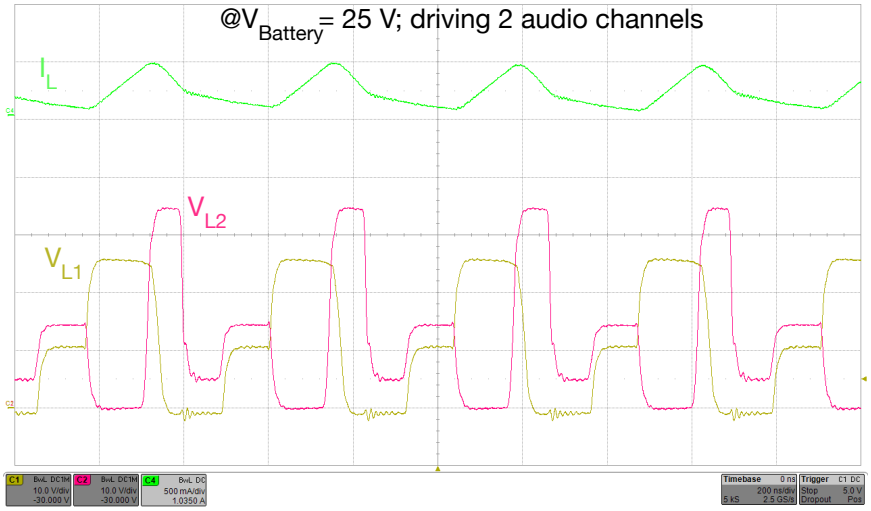


**Fig. 4.7** Steady state response of the SIMO converter at $V_{Battery}$= 25 V.

## 4.5 Load transient response of the SIMO converter

The load regulation performance of the SIMO converter was evaluated by varying the load current $V_{Reg\text{-}low}$ in the range 1-75 mA. This range corresponds to the equivalent condition of no switching to full load, 4-channel switching of the class D power amplifier. Fig. 4.8 shows the load transient performance of the SIMO con-

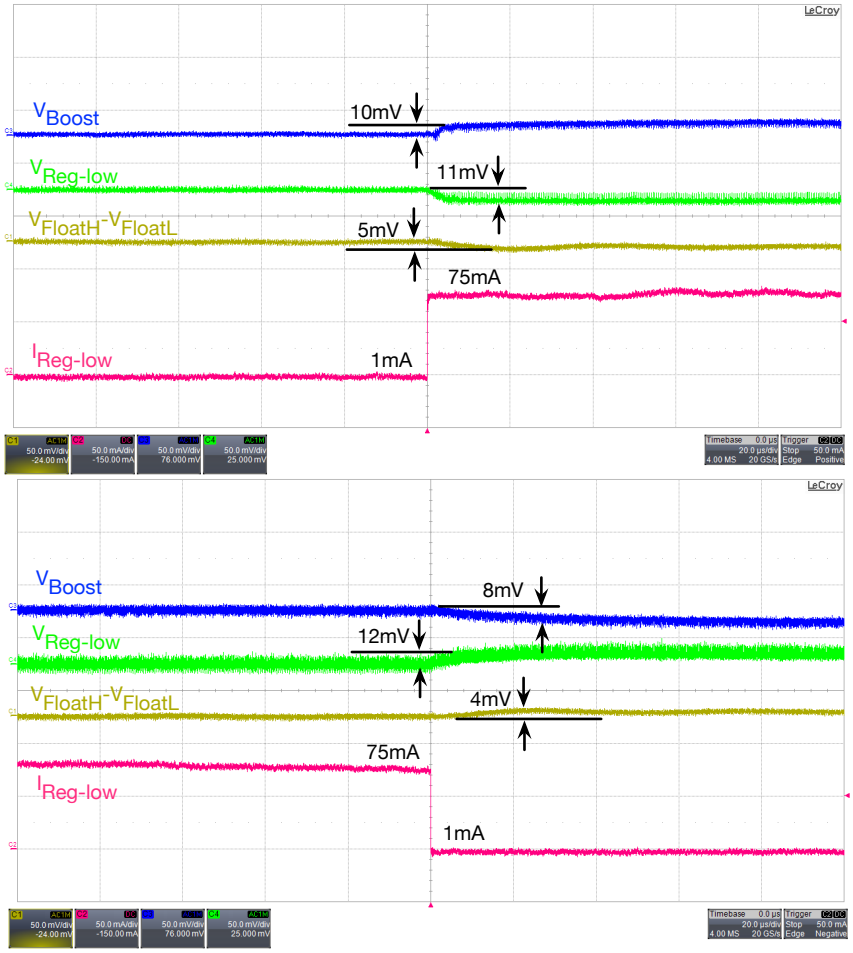


**Fig. 4.8** Load transient performance of the SIMO converter.

verter. A maximum load transient of 0.16 mV/mA at $V_{Reg\text{-}low}$ was observed. The corresponding cross-regulation on $V_{Boost}$ is 0.13 mV/mA.

## 4.6 Measurement of efficiency of the SIMO converter

Efficiency of a power converter is the most important figure of merit (FoM) of its performance. In the target application of car-radio, the efficiency of the SIMO converter is expected to reduce the quiescent power dissipation significantly increase the overall system efficiency as explained in the introduction. High efficiency of the SIMO converter at the nominal (14.4 V) and step- up (25 V) value of $V_{Battery}$ is crucial in the application. Fig. 4.9 shows the efficiency plots of the SIMO converter at different values of $V_{Battery}$. The load variation on the X-axis corresponds to the load currents required to drive the class-D power amplifier in 1-4 output channel conditions. At the nominal and step-up values of $V_{Battery}$, the SIMO converter provides efficiencies in the range of 80-86% to drive 2-4 channels.

The output power delivered by the SIMO converter in various load conditions during step-up operation with $V_{Battery}$=25 V is also annotated in Fig. 4.9. The converter delivers a peak output power of 2.8 W driving 4 channels of the power amplifier.

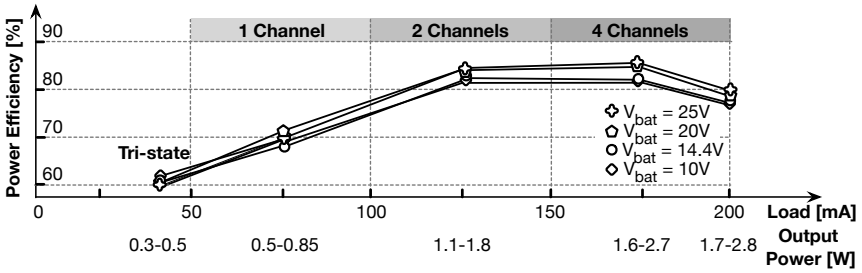


**Fig. 4.9** Output efficiency of the SIMO converter at different values of $V_{Battery}$ and across 4 audio channels.

## 4.7 Performance of the car-radio with the SIMO converter

After the performance of the SIMO converter is evaluated as described in the previous sections, it is used to supply a class-D audio amplifier. The target of the experiment is to determine the impact of the SIMO converter on the the car-radio. The SIMO converter being a switching regulator, the switching noise degrades the SNR of the car-radio. The degradation is quantified by comparing the SNR of the car-radio supplied using SIMO converter with that of the linear-regulator supplied car-radio. Fig. 4.10 shows the plots of the total-harmonic and noise distortion (THD+N) of the class-D amplifier supplied using SIMO and linear regulators at $V_{Battery}$= 14.4 V. SNR in both the cases, evaluated at -60 dBFS of input signal, is annotated in Fig. 4.10. SNR degradation of less-than 0.8% is observed by replacing linear regulators with the SIMO converter in the car-radio.

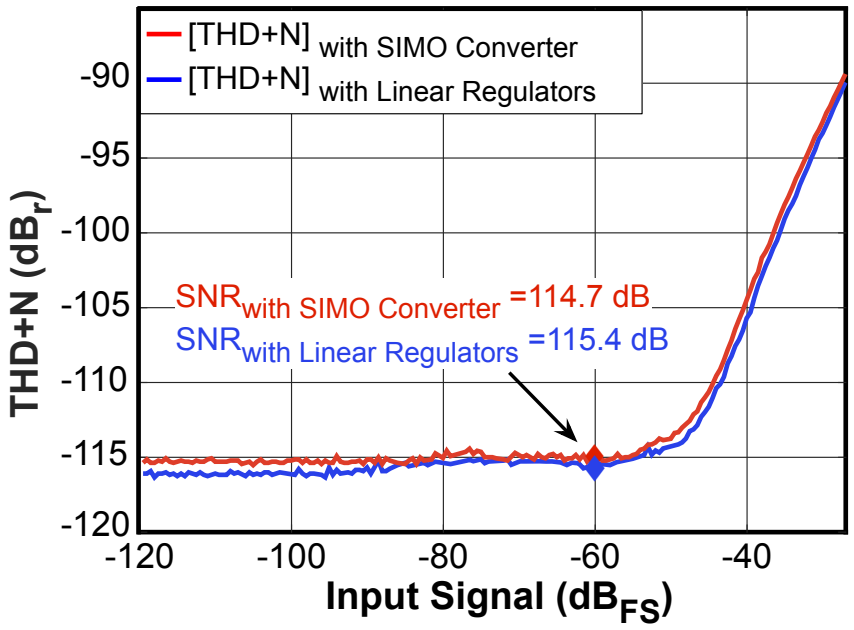


**Fig. 4.10** Comparison of SNR of the car-radio supplied using SIMO converter and linear-regulated power supplies.

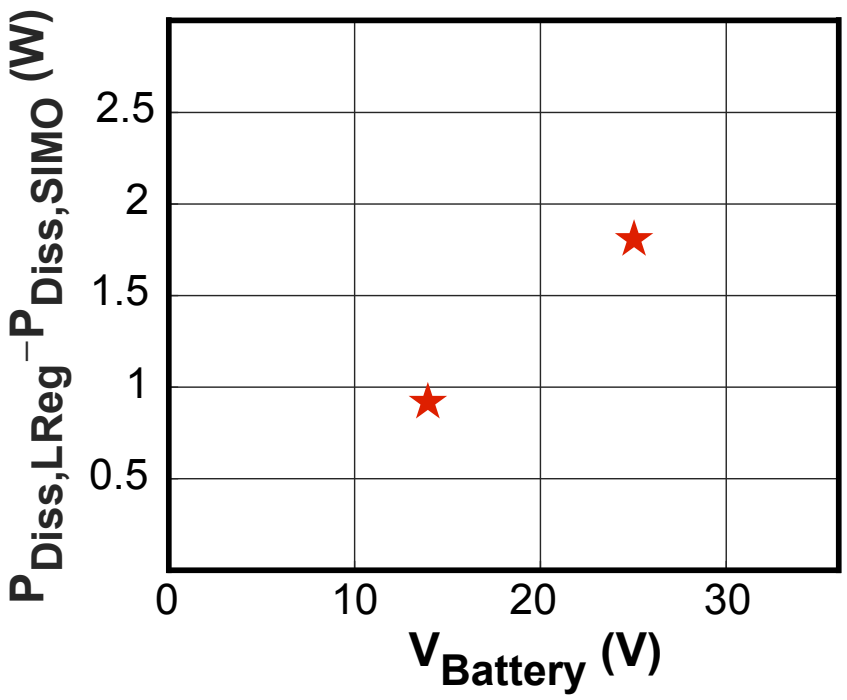


**Fig. 4.11** Power savings obtained using SIMO converter in comparison with the linear regulators in the car-radio system.

Reduction of the quiescent power dissipation ($P_{Diss}$) in the car-radio is the goal of project. Therefore, ($P_{Diss}$) at the mute condition of the car-radio is evaluated driving 4 audio channels at the nominal and stepped-up values of $V_{Battery}$. $P_{Diss,SIMO}$ corresponds to the system $P_{Diss}$ with SIMO converter. $P_{Diss,LReg}$ corresponds to the system $P_{Diss}$ using linear-regulators. $P_{Diss,LReg}-P_{Diss,SIMO}$ directly provides the power savings obtained using SIMO converter. As shown in Fig. 4.11, at the nominal value of $V_{Battery}$=14.4 V, 0.9 W of power is spared. At the stepped-up $V_{Battery}$=25 V, 1.7 W of power savings are obtained. Therefore, SIMO converter reduces $P_{Diss}$ significantly during the quiescent operating conditions of the car-radio.

## 4.8 Performance comparison of the proposed SIMO converter with the state-of-the-art

The performance of the proposed SIMO converter was compared with the state-of-the-art SIMO converters. There are no SIMO converters addressing high voltage (>10 V) applications in general and automotive applications in particular in the literature. The bases for comparison were the similar process technologies used and the maximum output power levels. A performance comparison of the proposed SIMO converter and the state-of-the-art is provided in Table 4.1.

The proposed SIMO converter provides efficiency exceeding 80%, driving upto 4 channels at nominal and stepped-up values of $V_{Battery}$. The line-regulation being an important FoM in the automotive application, a maximum value of 16.2 mV/V is obtained across 4.5-27 V of $V_{Battery}$ transients. Load transient and cross regulation performance of the proposed SIMO converter is on par with the state-of-art. The SIMO converter delivers 2.8 W of maximum output power and occupies a silicon active area of 2.5mm$^2$.

## 4.9 Summary

A detailed performance evaluation of the SIMO converter was carried out. The output regulating ability of the SIMO converter was verified in the presence of wide range of line and load variations as demanded by the automotive application. The converter offered overall efficiency exceeding 80% in all the nominal operating conditions. A comparison of performance with the state-of-the-art shows that the proposed SIMO converter excels in some of crucial figures of merit while performing on par in other aspects. The peak efficiency and output power are on par even with a significantly lower active area of 2.5mm$^2$. In terms of the topology, the buck, boost

**Table 4.1** Performance comparison of the SIMO dc-dc converters.

| Parameter | **This Work [1]** | Lu, [2] ISSCC'14 | Jung, [3] ISSCC'15 | Xu, [4] ISSCC'11 |
|---|---|---|---|---|
| Process | **110-nm BCD** | 0.35-µm CMOS | 0.35-µm BCD | 0.25-µm CMOS |
| Outputs/ Topology | **3 Outputs: Buck, Boost, Floating** | 4 Buck Outputs | 10 Buck Outputs | 1 Buck 1 Boost |
| Supply Voltage (V) | **4-40** | 2.7-5 | 5 | 2.5-5 |
| Inductors Capacitors | **L=10 µH C=10 µF** | L=4.7 µH C=10 µF | L=10 µH C=10 µF | L=2.2 µH C=20 µF |
| Switching Frequency | **2.4 MHz** | 1 MHz | 1.2 MHz | 2 MHz |
| Output Ripple (mV) | **<25** | <30 | <40 | <80 |
| Line Reg. (mV/V) | **4-16.2** | NA | NA | NA |
| Load Tran. (mV/mA) | **0.16** | 0.16 | 0.17 | 1.5 |
| Cross Reg. (mV/mA) | **0.13** | 0.04 | 0.1 | NA |
| Peak Efficiency | **86%** | 87% | 88.7% | 90% |
| Max. Output Power (W) | **2.8** | 2.16 | 2.5 (Estimated) | 2.5 |
| Active Area ($mm^2$) | **2.5** | 5.4 | 11.75 | 7.54 |
| Automotive Class | **Yes** | No | No | No |

and floating output combination provided by the proposed converter is novel. Most significantly, the SIMO converter qualifies for automotive application in particular and other high voltage applications in general.

## References

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# Chapter 5

# Conclusion and future work

## 5.1 Conclusion

A SIMO dc-dc converter is designed and integrated with a class-D audio amplifier for car-radio application. A systematic, application specific analysis and derivation of specifications is done in Chapter 2. Equivalence is made between a SISO and SIMO converter. A suitable power stage was configured to deliver a boost, buck and floating output. The controller is modeled based on the equivalence and a simplified but sufficient compensation is provided. The system level specifications are derived and the simulations are performed to meet the specifications at the behavioural level.

With the system level specifications derived in Chapter 2, the circuits required for the SIMO converter are designed at the transistor level in Chapter 3. As the automotive application is a HV application with the battery variation in the range 4-40 V, the SIMO converter circuit was divided into sub-blocks in different voltage-domains. This technique of separating the sub-blocks based on the supply voltages resulted in efficient and compact design of some of the blocks in low-voltage domain using CMOS devices. BCD devices were used to level shift between the voltage domains and in the power-stage. The physical design of the SIMO converter occupies an active area of 2.5 $mm^2$. The converter offers a peak efficiency exceeding of 86%

and meets the stringent automotive requirements, hence qualifying for the automotive class voltage regulation. The main target of the converter being the reduction of power dissipation in mute (quiescent) condition, the SIMO converter is expected to improve the overall system efficiency of the car-radio. Based on the performance of the first IC, the subsequent prototyping of the class-D power amplifier for field trials is underway. A patent application is filed describing the circuit techniques invented in the course of the research-work.

## 5.2 Future work

As a continuation of the research activity, an improved SIMO converter with higher performance specifications is being developed for the next generation car-radio. The feasibility study and area estimation for the SIMO converter are completed. Some of the improvements and alternatives that may be explored are:

1. SIMO converter functionality over the entire range of $V_{Battery}$ (4-40 V) using higher voltage (up to 60 V) power switches.
2. Improved driving techniques to reduce switching losses.
3. Alternative control techniques like current mode controller to improve load-transient response.
4. Alternative packages like flip-chip package to significantly reduce bond-wire mutual coupling and the ripples on floating outputs.