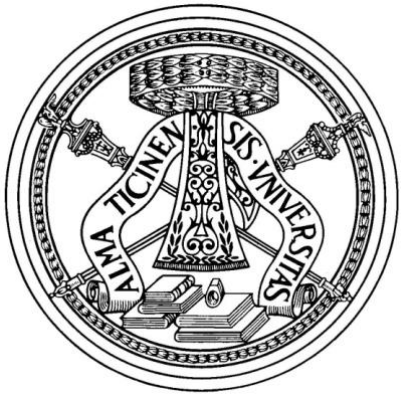

UNIVERSIT´A DEGLI STUDI DI PAVIA

Faculty of Engineering

Department of Industrial and Information Engineering

Ph.D. Course in

Microelectronics

Ph.D. Thesis

High Efficiency E-band Power Amplifiers and Transmitter in 55nm BiCMOS

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Abstract

This thesis presents the development of a new kind of power amplifiers and the design of a full E-band Transmitter designed in the analog integrated circuit laboratory of the University of Pavia. The mobile network structure is going to change drastically in the next years to handle the escalating needs for new standards and applications. Consequently, also the backhaul, i.e. the links connecting base stations to the central network, will undergo several modifications to allow higher performances in terms of speed and number of users and good quality of service. The power amplifiers presented in this work have been designed specifically to satisfy the requirements of the future backhaul transceivers, overcoming many challenging aspects of power amplifiers design at mm-Wave (30-300 GHz).

The power amplifier is the most power hungry block of E-band transmitters for backhauling. Especially, an idea for improving the power efficiency with emphasis in back-off region (i.e. when the power amplifier delivers output power lower than the peak value) has been proposed. The idea exploits a common-base transistor in the output stage, where the BE junction performs current-clamping to adjust the average (DC) current according to the actual output power. Two prototypes have been realized in 55nm SiGe-BiCMOS technologies, demonstrating performances beyond the state-of-the-art. In the single-path PA, Psat is 19dBm while OP1dB is 18dBm. The measured PAE peaks to 23% while at OP1dB and 6dB back-off it is 22% and 8.5%, respectively. The measured Psat and OP1dB for dual-path PA are 21.5dBm and 20.5dBm, 2.5dB higher than for the single-path PA. The maximum PAE is 22% while PAE at OP1dB and 6dB back-off is 20% and 7.2%, respectively.

As second major contribution, a direct conversion E-band transmitter focusing on signal path including up-conversion mixers and PAs has been designed and realized in 55nm SiGe-BiCMOS technology. Optimizations are performed from architecture level

down to transistor level to minimize the power consumption while delivering high linear output power. The measured OP1dB and maximum output power for the realized E-band transmitter are 20.3dBm and 22dBm, respectively. The image rejection ratio of transmitter without baseband calibration is 40dBc (above 50dBc with baseband calibration) while the bandwidth is in the frequency range of 66-88GHz.

Table of Contents

Chapter 1:
Introduction

The target of this chapter is to explain the need of revising the power amplifiers to be much more efficient than the recently published works. First of all, it is needed to get familiar with the environment in which this amplifier will be employed, the backhauling structure of the mobile network. Therefore, in the following, it will be described the current situation of the mobile network and in which direction it is going to evolve and why. In the end, it will be focused more on the design problems and characteristics of a power amplifier working at high frequencies to motivate the main features of the circuit developed in this PhD work.

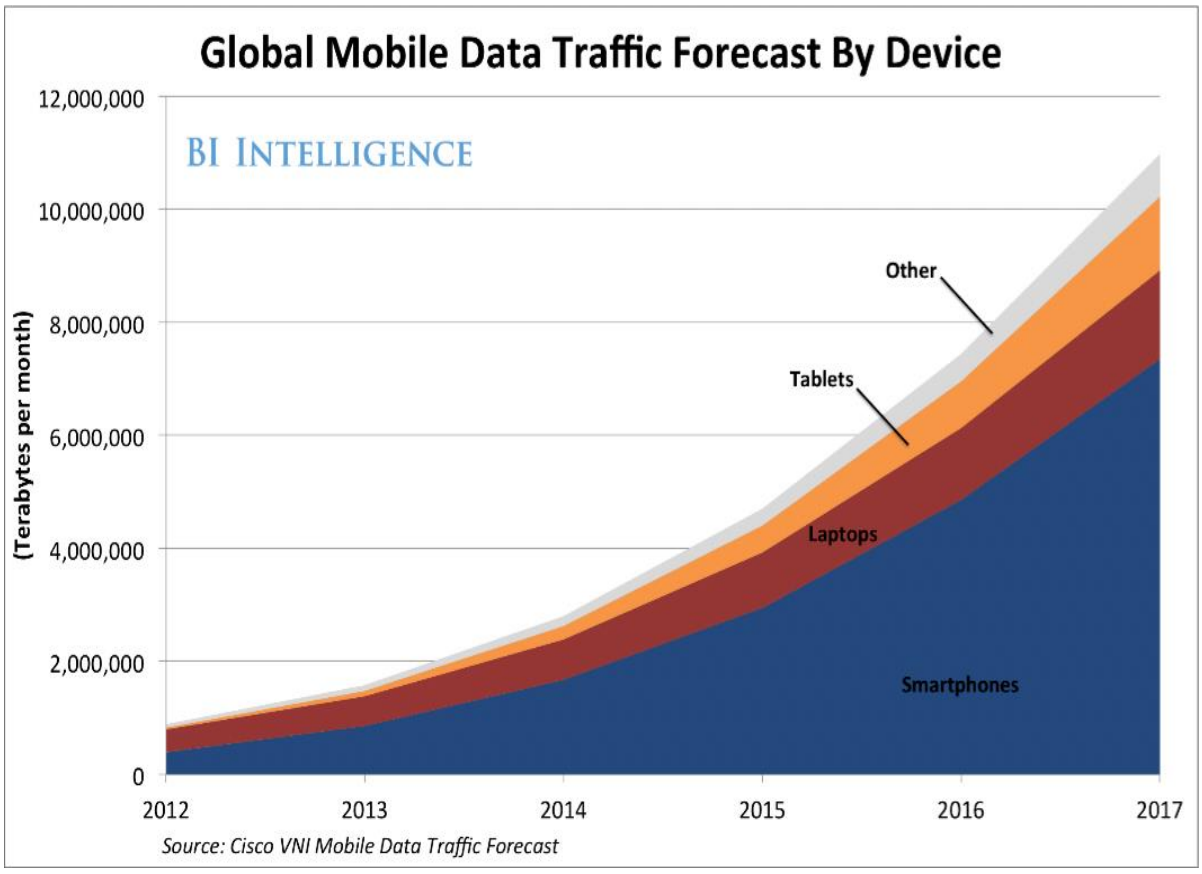

Figure 1.1: data traffic growth.

1.1: Mobile network evolution

In the last few years, the data traffic volume faced with an exponential growth, the rapid evolution and diffusion of smartphones, tablets and the development of new innovative applications loads the network with an incredible amount of traffic. An 11 exabytes per month data traffic is forecasted for the 2017 and even more in the years to come as it is shown in Figure 1.1. Not only the data traffic is growing but also the number of connected devices is increasing at a very fast rate, especially because of applications like the Internet of Things (IoT), machine to machine communication (M2M) and the internet of vehicles (IoV). Figure 1.2 shows that in a few years more than 30 billion devices will be connected to the network and the largest part belong to the IoT category.

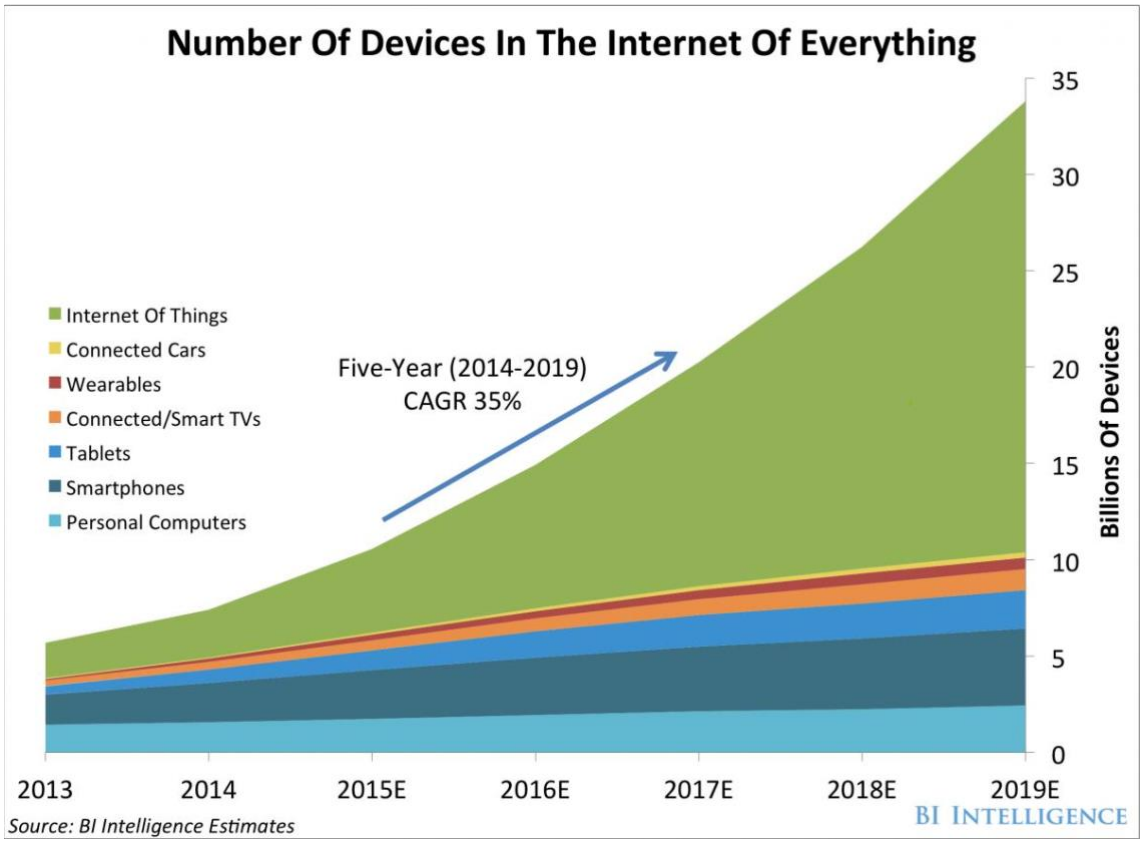

Figure 1.2: Forecasted number of connected device.

To maintain a good quality of service, the network must evolve to cope with the expected requirements of the years to come. Several groups were born to study and

guide this evolution, for example the METIS (Mobile and wireless communications Enablers for Twenty-twenty (2020) Information Society). It is a European consortium whose aim is to help with pre-standardization and regulation of the upcoming mobile wireless network. Their works focus on the main aspects which should be improved in the future years, especially capability and data rates. Moreover, the consortium will also help in defining requirements and specifications for many new applications. The METIS analysis pointed out several features that the new network should have to satisfy the users demands. It should be able to handle up to one thousand times more traffic than the existing network, have enough capability to manage between 50 and 500 billion devices, guarantee a latency lower than 1 millisecond and provide data rates going from 1 to 10 Gbps [1]. These are the characteristics of the next generation mobile network the so called 5G.

To satisfy these demanding specifications and realize this new complex network a lot of research is being carried on in different fields: multi-tier communication, MIMO systems, ultra-dense networks, mm-Wave backhauling and many other aspects are being explored and analysed to provide the knowledge necessary to meet the new standards. Martin Cooper, pioneer of the mobile communication systems, has highlighted the three most important factors regulating the capacity of the network. Respectively: the number of infrastructural nodes (i.e. base stations), the available spectrum and the link efficiency. The impact of these elements can be visualized even better observing the formula for the maximum throughput of the single user [2]:

$$C=m(\frac{w}{n})\log_2(1+\frac{S}{I+N}) \qquad (1.1)$$

Where **C** is the throughput, **n** is the number of user connected to the base station, **W** is the available bandwidth at the base station, **m** is the spatial multiplexing factor while **S**, **I** and **N** are the signal, interference and noise power at the receiver, respectively. The most immediate solution to increase **C** is to employ additional spectrum using for example the carrier aggregation technique. Employing multiple carriers, the transmitter

can operate on different non-contiguous portions of spectrum as if it had a larger bandwidth. It is a good technique able to achieve data rates in the order of the Gbps, but it is limited by the scarce spectrum available at microwaves frequencies. For this reason, the research is being pushed toward the mm-Wave range (30-300 GHz) where several gigahertz of bandwidth are available as shown in Figure 1.3 [3]. In particular, the bands around 60 GHz and the E-band (71-76 GHz and 81-86 GHz) seem promising since they are license free in almost every country. These frequency ranges are already exploited by radar and radio astronomic applications, but it is the first time they are used for mobile communications and therefore many questions and problems still need to be solved as will be explained.

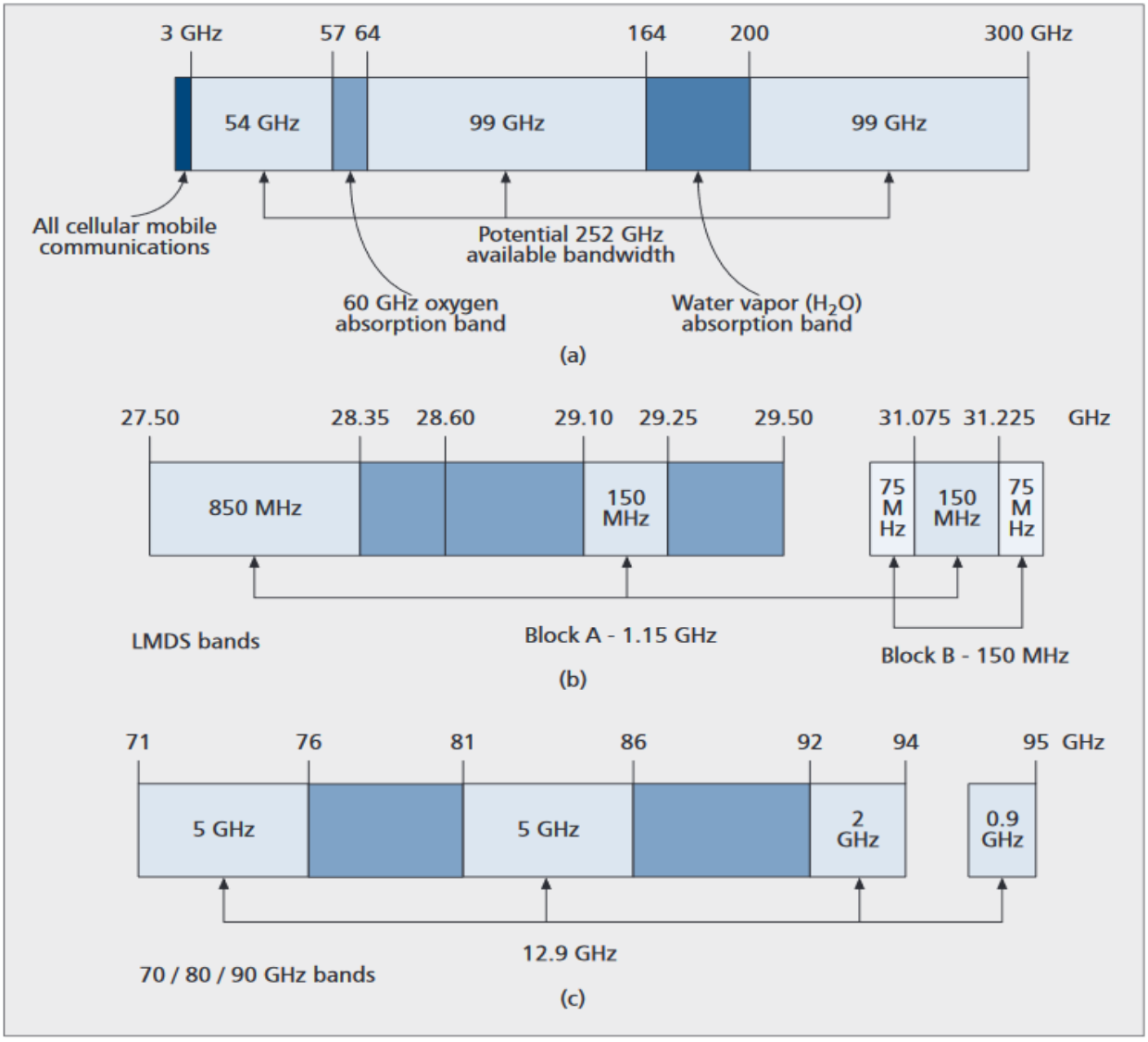

Figure 1.3: mm-Wave bandwidth representation [3].

Another important solution to increase **C** and therefore the performances of the network is reducing **n**, the number of users per cell. The best way to reduce **n** is increasing the number of base stations, achieving a more homogeneous distribution of the users between the different cells and therefore a lower number of users per base station. This principle is called cell splitting and has been carried out also for the past generations of the network (i.e. 2G, 3G, 4G). Now this concept is brought to the limit, the fifth generation (5G) network will employ a huge number of femto-cells, with a coverage between 50 and 200 meters, massively deployed in the most densely inhabited areas. In this way, the network will be able to handle many more users while providing high data rates. Besides the increased capacity ultra-dense networks have also other benefits, for example a reduced power consumption because of the short distance covered by the stations. The reduced range of the base station also lessens the path losses making the system more robust to noise. Spectrum enhancement and cell splitting together are called network densification process. This upcoming network evolution will be able to reach the targets described only if the backhauling structure undergoes a similar process, otherwise it would become the bottleneck of the entire system. In the following, it will be explained how the network is supposed to work and which are the features and problems of the backhaul.

1.2: Overview of the future mobile network structure

The next generation network will be an HetNet, a heterogeneous network. In fact, it will be organised as a multi-tier system where each layer has its own role. The higher layers belong to the legacy network (2G, 3G, 4G, WLAN...) and through the main base stations (MBS) will manage system synchronization, handover of users from one cell to another, connection to high mobility users and other delicate tasks. The ultra-dense-network of small cells (micro-, pico- and femto-cells) or small base stations (SBS) instead will provide extremely high data rates to the users whenever it is necessary. A

possible scenario for the future mobile communication system is represented in Figure 1.4, where the macro-cell provide connection all over the area and manages all the users helping them discover the SBSs that receive and transmit data from/to the core network via wireless or fibre backhauling.

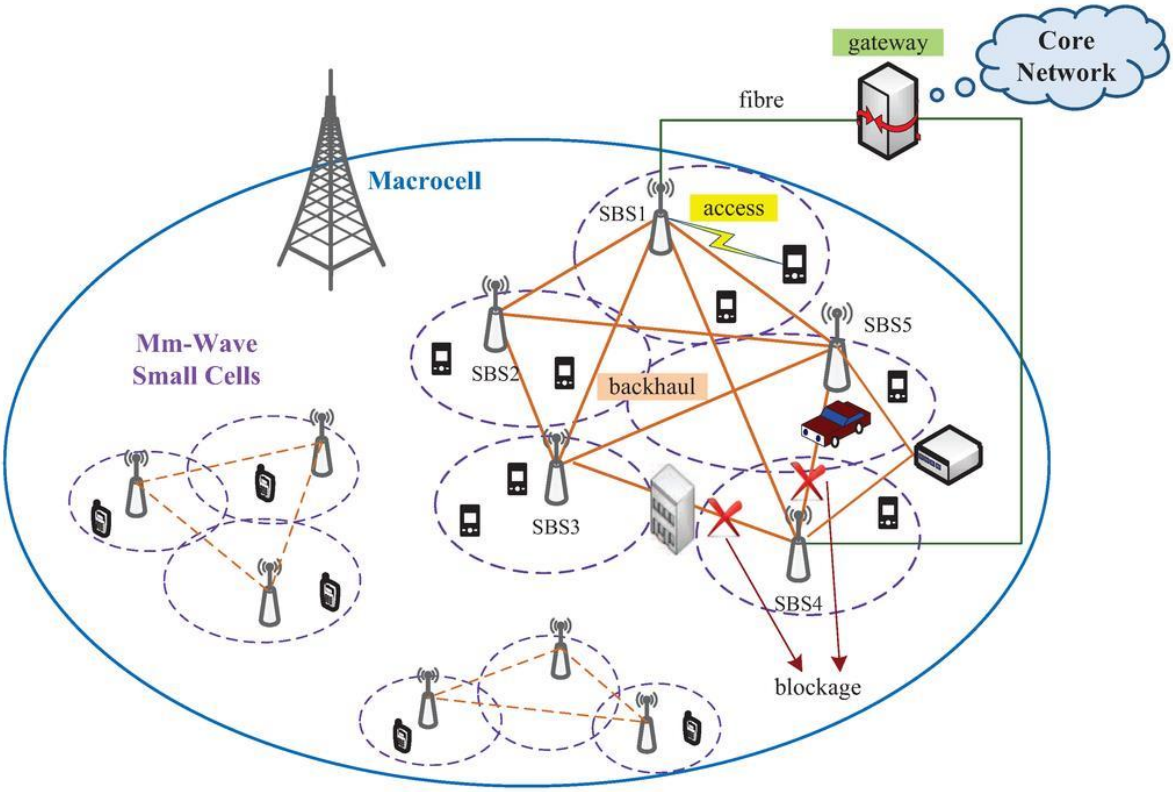

Figure 1.4: 5G network structure [4].

The main challenges are tied exactly to the backhaul structure connecting the base stations and the network. Nowadays, backhaul is done in two ways: via optical fiber or via wireless links. The fiber requires additional deployment costs but provides very high data rates, wireless links are cheaper, but because of the limited bandwidth available at microwaves frequencies they are less performing than fiber. Since the number of base stations will greatly increase, as shown in Figure 1.5, backhaul through fiber becomes way too expansive and impractical. Wireless backhaul instead could be the best way to implement the backhauling structure, but only if it could exploit the larger bandwidths available at mm-Wave frequencies. Another consequence of the high number of BSs is that the current transceivers will be replaced by fully integrated version based on CMOS and BiCMOS technology. The advantage of this choice is that

on a large-scale production the transceivers will become much cheaper than they are now, but IC design at high frequencies presents several problems, illustrated in the next paragraph, that needs to be solved to realize an efficient system.

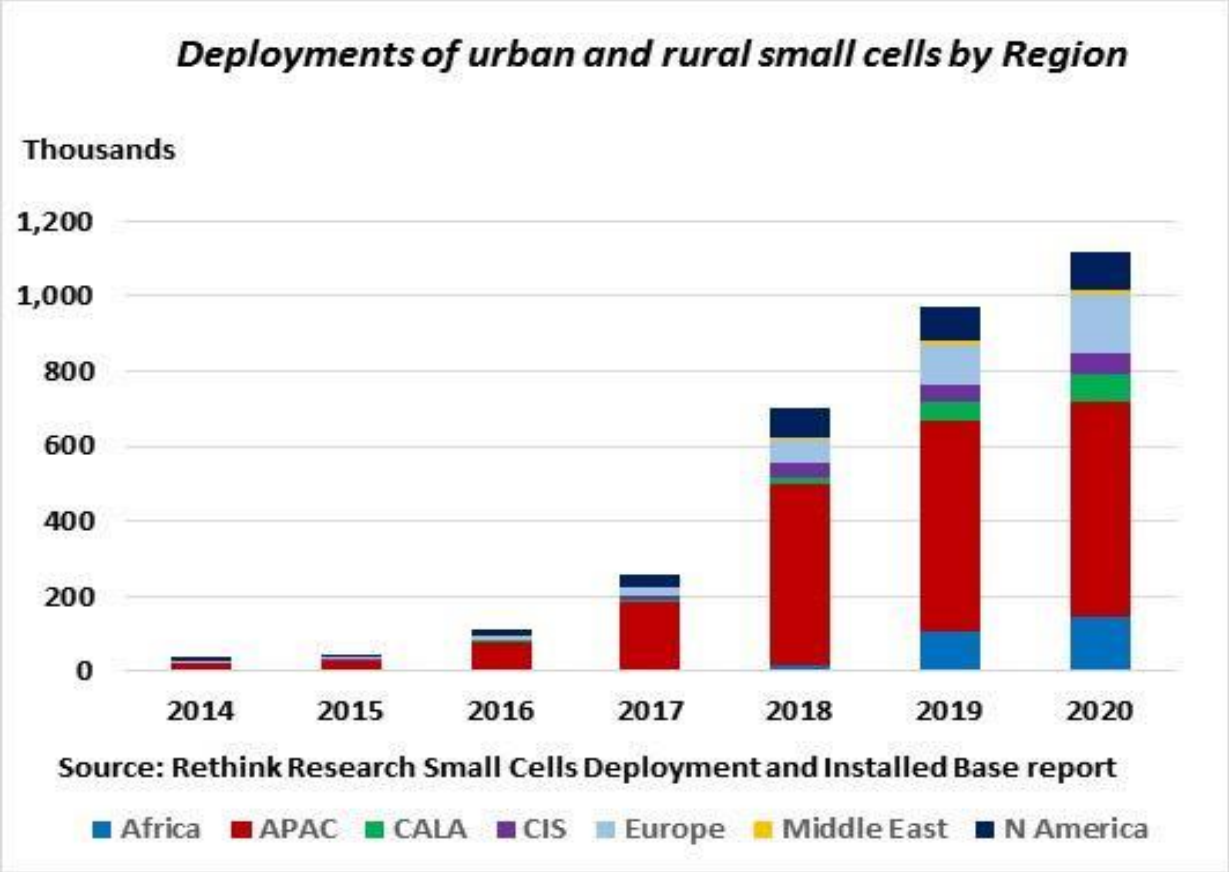

Figure 1.5: small-cells diffusion forecast.

1.3: Critical aspects of a Power Amplifier for next generation backhauling systems

As already said the new backhauling structure will rely on CMOS and BiCMOS technologies, because of their cheapness, compactness and low power consumption. Together with many advantages granted by this choice come a lot of problems tied to the transmitter side and especially to the power amplifier (PA) block. In fact, up to few years ago, integrating a mm-Wave power amplifier while achieving high output power and good efficiency was really a challenge and usually this block was built in a

different technology, like GaAs HBT (Hetero-junction Bipolar Transistor), leading to a more expansive transceiver. In fact, the lower integration level demands more packaging, more discrete components and larger die size. Since the number of transceivers will grow exponentially, the priority is to lower the costs and a fully integrated device is mandatory. Implementing a PA in CMOS or BiCMOS technology at mm Wave frequencies is difficult because in the EHF range (30-300GHz) parasitic components play a central role in the performances of the circuit imposing several constraints on the design. For example, the gain and size of the transistors at high frequencies are limited and therefore the use of cascaded stages and the implementation of power combining techniques is often mandatory to reach the design targets.

Moreover, now that the wavelength is comparable with the circuit dimension, passive elements need to be designed using microwave techniques. The employment of high order modulation schemes also contributes to make the power amplifier design the most critical challenge for designers. In fact, to boost even more the data rates and spectral efficiency of the system, the use of complex modulation is encouraged and clearly this has an impact on the linearity requirements of the transmitter. As the modulation order rises, so does its PAR (peak to average ratio). To ensure linearity across all the values of the signal the PA must be designed to have a 1dB compression point higher than the peak value of the modulation scheme. This can be already a challenging task but it is not the only problem of the amplifier. The PA will not work always at peak level but on average it will work in back-off where the PAE (power added efficiency) is usually much smaller as will be explained in Chapter 2. Since the first 60GHz silicon PA was presented in 2008 [5], a great effort has been done to improve the maximum output power, 1dB compression point and peak PAE, but the back-off efficiency is still extremely low (usually less than 3% at 6 dB back-off [6]) and remains one of the greatest challenge for the designers. Table 1.1 summarizes the main specifications for the transmitter side of a mm-Wave backhaul link depending on the adopted modulation scheme [7]. The power amplifier must provide an output power

in between 15 and 20dBm to be able to transmit over an acceptable distance and it must be able to operate linearly with every modulation scheme employed by the transceiver.

Table 1.1: backhaul budget link for 60Ghz transmitter.

Backhaul link budget analysis	64-QAM	16-QAM	QPSK	BPSK
Emitter				
Bandwidth (GHz)	1.76	1.76	1.76	1.76
P1 dB at PA output (dBm)	15	15	15	15
PA output backoff (dB)	8	5	3	3
Mean power at PA output (dBm)	7	10	12	12
PA-antenna interconnection loss (dB)	3	3	3	3
Emitted mean power (dBm)	10	13	15	15
Antenna gain (dB)	30	30	30	30
EIRP (dBm)	40	43	45	45
Channel				
Distance (m)	100	200	300	300
Attenuation coefficient	2	2	2	2
Carrier frequency (GHz)	64.8	64.8	64.8	64.8
Oxygen and rain attenuation (dB)	3.20	6.40	9.60	9.60
Path loss (dB)	−111.9	−121.1	−127.8	−127.8

In fact, depending on the data rate required, on the distance between different BS and on the channel's condition, the system can employ several modulation schemes each with its own characteristics. For high-speed, short links 64QAM can be used reaching almost 8 Gbps data rates. As the length of the link increase it's more and more difficult to keep the minimum SNR (Signal to Noise Ratio) required to guarantee a good BER (Bit Error Rate). To maintain a high quality of service the system switches

to simpler modulation scheme, like QPSK or BPSK, that allows more robustness to noise and reliability on longer paths at the cost of a lower data rate. As already pointed out, modulation schemes have an impact on efficiency, confirmed by Table 1.1. In fact, associated with each modulation there is a certain back-off factor that increases with the complexity of the modulation forcing the PA to work in the least efficient way.

1.4: Thesis organization

This thesis is focused on the analysis and design of power amplifiers employed in a transmitter designed in SiGe-BiCMOS technology for backhauling applications at E-band. A new amplifier circuit topology is investigated, leveraging the current clamping principle to maintain a superior efficiency also in back-off, where other devices achieve poor performance. A single path PA to test the idea and a dual-path PA to rise output power leveraging power combining, and also a prototype of full transmitter deploying the 2-path PAs were developed in the Analog Integrated Circuits Laboratory. The target of this thesis is to present the realized integrated circuits and it is organized as follows:

-Chapter 2: in this chapter, the most important metrics and features used to characterise a power amplifier are reported, for example the gain, the efficiency and PAE and 1dB compression point. Then, the most popular classes of power amplifier employed at mm-Wave and their characteristics are presented and compared, followed by a review of state-of-the art realizations.

-Chapter 3: the main topics of thesis are treated in these pages; all the chapter is focused on the common-base stage that exploits the current clamping principle. The reasons behind the common-base configuration, the current clamping principle, application and characteristics are all surveyed which provides adaptive bias current resulting in a remarkable improvement of the collector efficiency. In the end, it is presented the analysis of the linearity of this circuit and the analytical model that describes the third order intermodulation tone behaviour.

-Chapter 4: Design of PAs test chips are presented in this chapter. A single path PA and dual-path PA combining two equal single path PA through power combiner are described in every component. The loss of power combiner in dual-path PA is particularly critical to preserve high efficiency. The implemented combiner is compared with the output matching network in single path PA, proving a marginal performance penalty.

-Chapter 5: The presentation of the measurements setups and the results of the measurements are reported in this chapter, and compared to the performances of previously reported power amplifiers in the same frequency range.

-Chapter 6: The complete signal path structure in E-band transmitter is described in every block. Actually, the dual-path PA described in previous chapters is employed in this transmitter together with wideband up-conversion mixers. Then follows the presentation of the measurements setups, and experimental results are reported and compared against other E-band transmitters.

Chapter 2:
Mm-Wave Power Amplifiers

Generally, the target of designing a PA, shown in Figure 2.1, is to deliver the required power to a given load in the frequency range of application while keeping high efficiency. mm-Wave power amplifiers, needed for the backhauling structure operate in the E-band with an output power around 20dBm. In order to understand the peculiarities and the operation of the proposed topology, presented in the next chapters, main parameters and classes of the power amplifier are reviewed in this chapter. Finally, some recently published state of the art PA configurations will be investigated in details which leads to the conclusion that they suffer from poor efficiency in linear region. However, this issue is considerably decreased in the proposed PA.

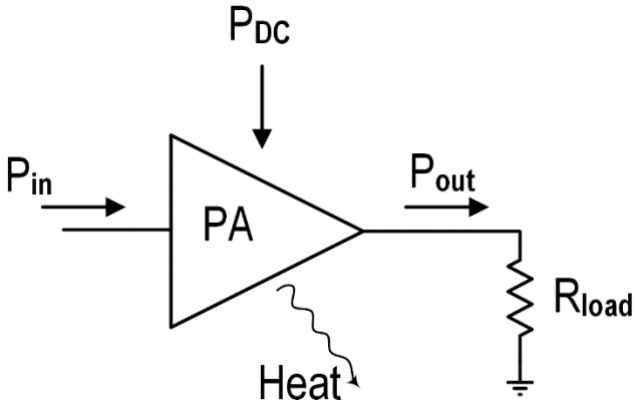

Figure 2.1: Power amplifier symbol.

2.1 : Power amplifier performance metrics

In this section, the parameters used to characterize a PA amplifier are explained.

2.1.1: Gain and bandwidth

The gain of a power amplifier is defined as:

$$G_{dB} = 10\log(\frac{P_{out}}{P_{in}}) \qquad (2.1)$$

where P_{out} is the output power and P_{in} is the input power.

PAs need to operate on the entire bandwidth of the communication standard in use. To achieve both high gain and wide band at mm-Wave, the use of cascaded stages is common practice. If we want to deliver high output powers, the output stage transistors must have a large size, that means a huge input capacitance; this can create problems to the driving circuit. Implementing one or more pre-driving stage allows an optimal driving of the output transistor at the cost of more power consumption.

2.1.2: Efficiency and PAE

The power amplifier is the most power-hungry block of the radio transmitter, and hence its efficiency is one of the most important parameters, especially in back-off region (when the output power is reducing) for backhauling applications. The efficiency can be defined in two ways; one is the collector efficiency (or drain eff. for MOSFET devices):

$$\eta = \frac{P_{out}}{P_{DC}} \qquad (2.2)$$

where P_{out} is the output power and P_{DC} is the power consumed from the supply.

The second definition takes the name of Power Added Efficiency (PAE):

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \left(1 - \frac{1}{G}\right)\frac{P_{out}}{V_{CC}I_{BIAS}} \qquad (2.3)$$

where P_{in} is the power at the input port, G is the gain, V_{CC} is the supply voltage and I_{BIAS} is the DC current drawn by the PA.

At low frequencies, where the input port dissipates little power and the high gain

makes P_{out} much bigger than P_{in}, the two measurements coincide. But as frequency rises, the gain falls and the power absorbed by the input becomes comparable with the output power of the stage. In this situation, the PAE represents a more accurate estimation of the efficiency.

2.1.3: Linearity

The PA input/output relation can be written as a polynomial where the coefficients α_i can be derived with different criterions:

$$y(t) = \alpha_1 x(t) + \alpha_2 x(t)^2 + \alpha_3 x(t)^3 \qquad (2.4)$$

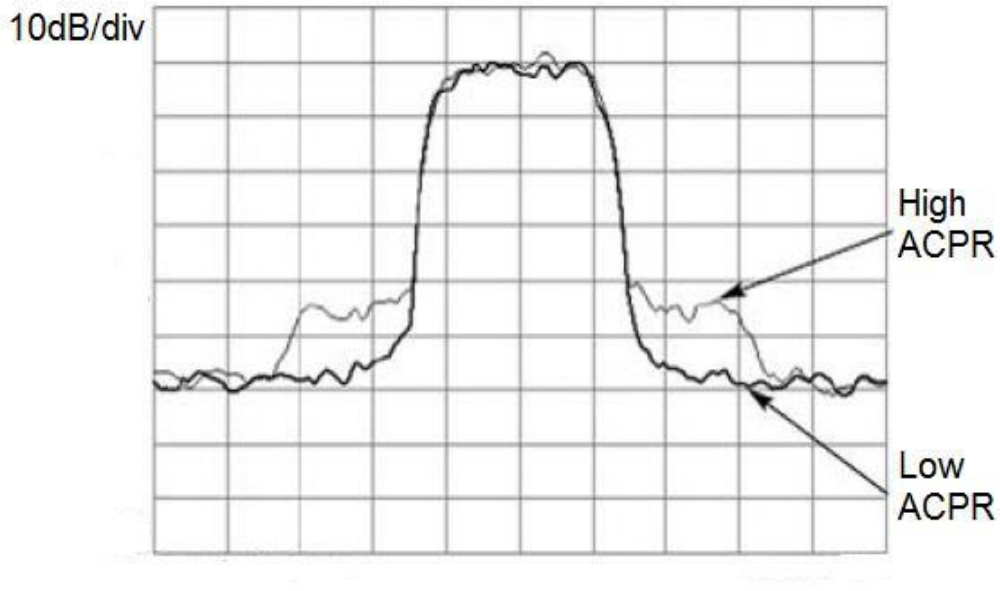

Figure 2.2: PA output spectrum and ACPR.

In power amplifiers, the non-linear effects can create various problems, and can be more or less important also depending on the modulation scheme adopted. Amplitude modulated signal can suffer from compression, meaning that the signal amplitude is deformed, leading to errors in reception. Moreover, variable envelope modulations generate spectral regrowth; this phenomenon can be described as an enlargement of the signal bandwidth at the output of the PA that falls in nearby channels disturbing them. This is exactly what Figure 2.2 shows, a comparison between the output spectra of two devices, one more linear and one with a stronger non-linearity. In the second

case, it is easy to observe the large sidebands caused by the spectral regrowth.

The adjacent channel power ratio (ACPR) is the parameter that allows to quantify this phenomenon. Calculating the ratio between the power leaked to the adjacent channel and the main channel power gives us the ACPR value. Each communication standard defines its own "masks" limits that need to be respected to ensure a certain quality of service. ACPR must be kept under a precise value not to fall out of these masks.

2.1.3.1: 1dB Compression Point

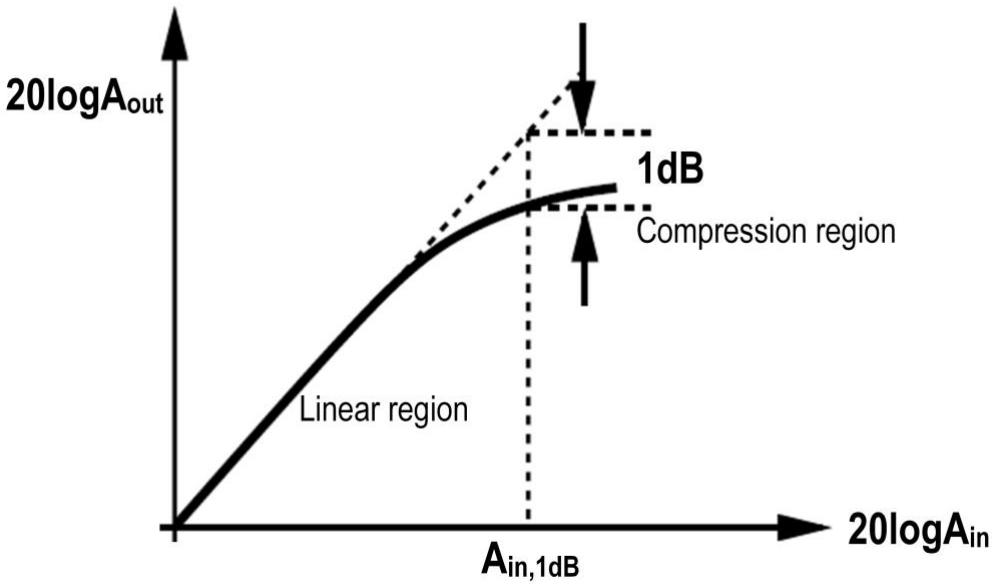

Figure 2.3: Gain compression and 1dB compression point.

Assuming an input signal is represented by $Acos(\omega t)$, we can evaluate (2.4) and observe that the amplitude of the fundamental harmonic at the output depends on α_1 and α_3:

$$V_O = \left(\alpha_1 + \frac{3}{4}\alpha_3 A^2\right) Acos(\omega t) \qquad (2.5)$$

In real circuits, these two coefficients have opposite signs and this leads to gain compression. The parameter of 1dB compression point is defined as the input amplitude that causes a 1dB reduction in the gain with respect to its ideal value (also

shown in Figure 2.3). The input 1dB compression point can be easily calculated with the following formula:

$$A_{1dB} = \sqrt{0.145 \left|\frac{\alpha_1}{\alpha_3}\right|} \qquad (2.6)$$

It can also be expressed in term of the output power level called OP1dB. PA designer needs to consider OP1dB to generate required power before compressing.

2.1.3.2: Intermodulation products

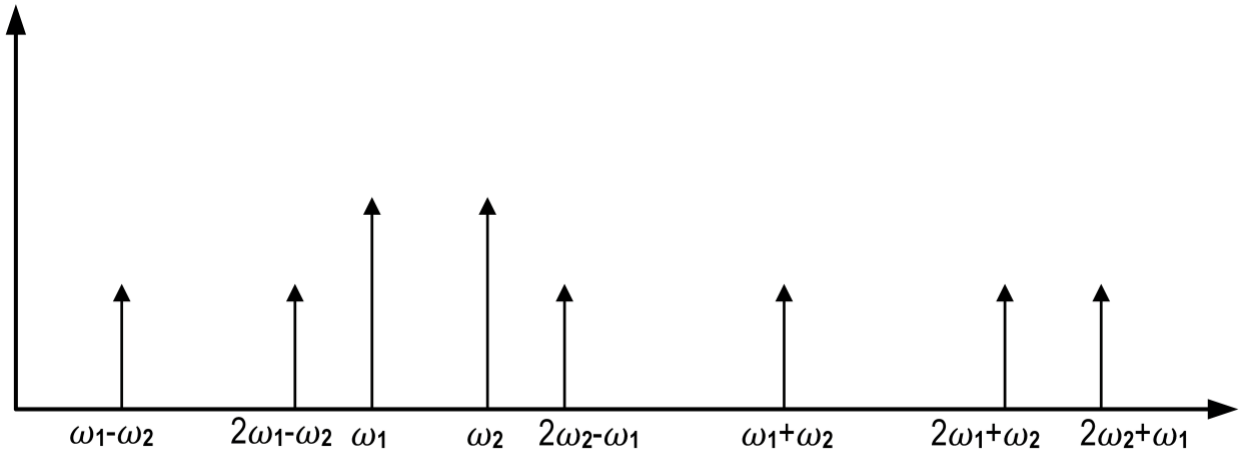

Figure 2.4: Intermodulation components generated by a two-tone input.

Intermodulation is another phenomenon tied to the linearity of the PA. When more than one signal is applied to the input of the amplifier, due to the non-linear behaviour of the device, the different tones interact with each other generating non-harmonic components at the output as shown in Figure 2.4. We can write an expression for these tones evaluating (2.4) with an input signal like: $x(t) = A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t)$.

The most relevant for PA are the third order intermodulation products at frequencies $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$. Third order intermodulation products (IM3) are a serious problem, because they fall in the neighbouring channels disturbing the reception and increasing the ACPR. By performing a two-tone test on an amplifier, IIP3 (input intercept of the third order) is derived, that by definition is the input signal level that

generates intermodulation tones as high as the fundamental at the output. This quantity actually is extrapolated and not measured directly because it may exceed the supply and also because compression heavily desensitize the device. IIP3 can be easily calculated with the following formula:

$$A_{IIP3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|} \qquad (2.7)$$

Or it can be estimated from the amplitude of the spectral components as [8]:

$$20\log A_{IIP3} = \frac{\Delta P}{2} + 20\log A_{in} \qquad (2.8)$$

$$\Delta P = 20\log A_{fund} - 20\log A_{IM3} \qquad (2.9)$$

where A_{in} is the input amplitude, A_{fund} is the amplitude of the fundamental output tone and A_{IM3} is the amplitude of the IM3 tone. Also, the OIP3 that would be the output power produced by the amplifier when the input is equal to the IIP3 can be expressed as:

$$OIP3_{dBm} = IIP3_{dBm} + Gain_{dB} \qquad (2.10)$$

2.1.3.3: AM/AM and AM/PM Distortions:

For PAs with modulated input signal, nonlinear distortions in amplitude (AM-to-AM conversion) and phase (AM-to-PM conversion) are important to be considered. AM/AM conversion and AM/PM conversion can be described as dependence of amplitude variation and phase shift upon the signal amplitude, respectively.

With a modulated input signal like: $x(t) = A(t)\cos(\omega t + \varphi(t))$, we can write an expression for the output like:

$$y(t) = g[A(t)]\cos(\omega t + \varphi(t) + \psi[A(t)]) \qquad (2.11)$$

Where g[A(t)] denotes the amplitude-dependent amplitude variation and $\psi[A(t)]$ is amplitude-dependent phase shift. Transconductance non-linearity can cause AM/AM distortion before occurring clipping while non-linear capacitors cause phase delay and then AM/PM distortion. In Chapter 4, the idea of using varactors to improve AM/PM non-linearity will be explained.

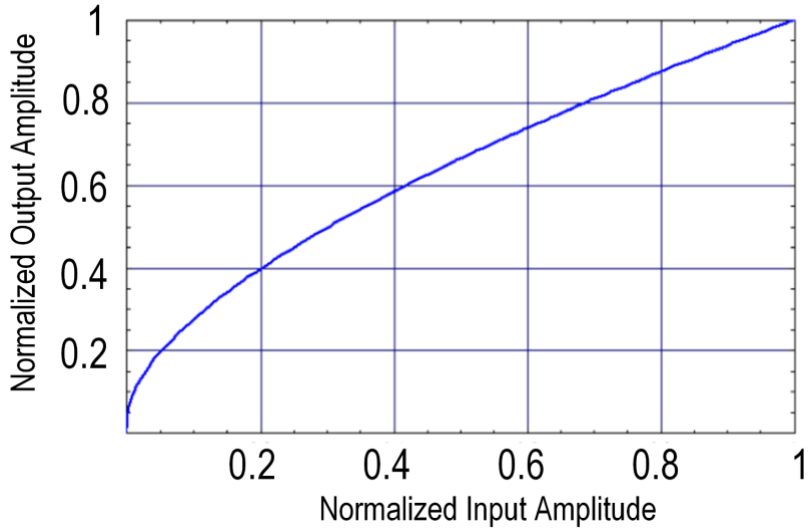

Figure 2.5: Typical AM-to-AM curve.

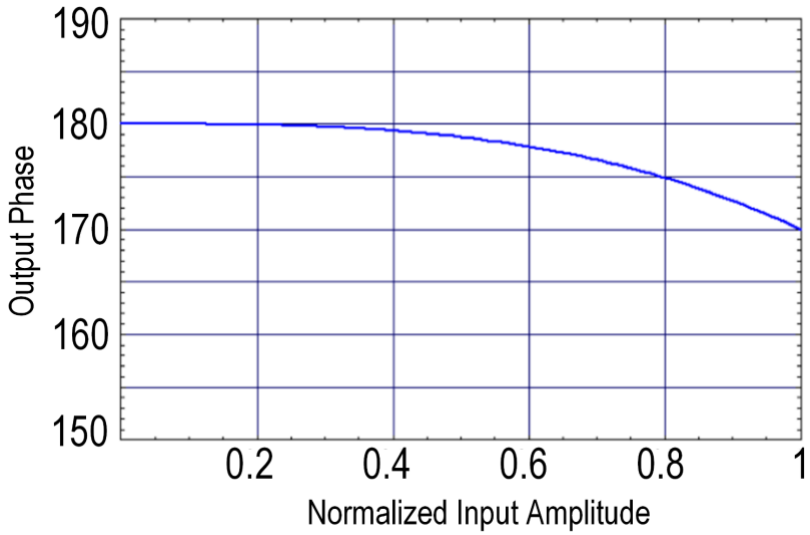

Figure 2.6: Typical AM-to-PM curve.

For a narrowband signal, we can partition the non-linearity into an amplitude-amplitude (AM-AM) component and an amplitude-phase (AM-PM) component as shown in Figure 2.5 and Figure 2.6.

2.2 : mm-Wave Silicon PAs

Power amplifier topologies are grouped in two fundamental categories; linear (class A, class B) and non-linear (class C, D, E). In mm-wave PAs, where transistors have limited gain, only linear PAs are of interest. Therefore, here it is given a brief explanation of linear PAs (Class A, Class B) operation, with emphasis on the efficiency. Then, a survey of the most relevant works in the literature will be presented, with the purpose of drawing a picture of the state-of the art performances.

2.2.1: Linear Power amplifiers

a) Class-A PA

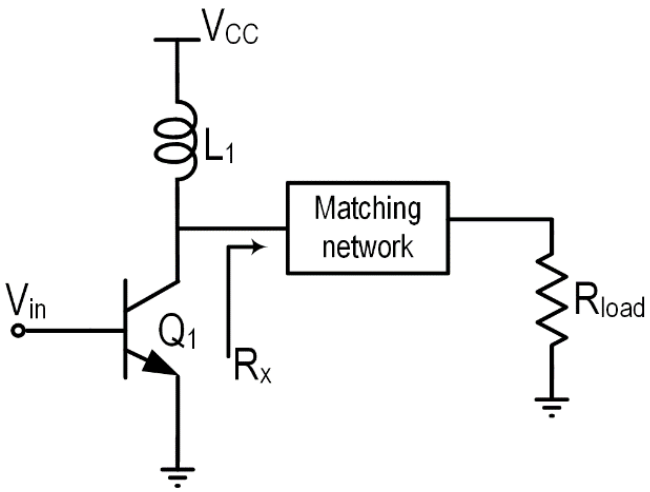

Figure 2.7: Class A common emitter configuration.

Class A power amplifiers are the most linear between all the classes, the transistor is biased in such a way that it (theoretically) never turns off for every value of the input signal, achieving a conduction angle of 360°. However, proper biasing is not ensuring complete linearity; in fact, if the swing is very large, the transconductance of the transistor can change considerably leading to non-linearity, anyway class A is for sure the most linear. The circuit in Figure 2.7 represents a possible configuration for a class-A power amplifier. It is a common emitter with an inductor as RF choke (to extend the collector swing above the supply voltage) and loaded by a matching network that

transforms the load to the value required to achieve the desired OP1dB and output power level.

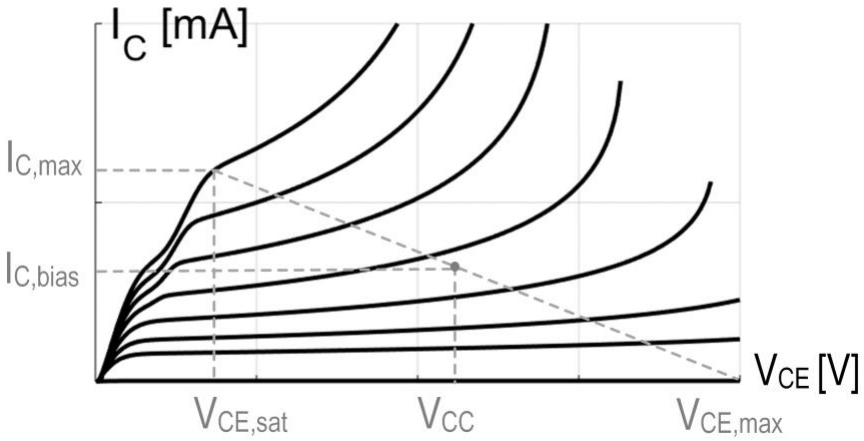

Figure 2.8: biasing point of the class A amplifier.

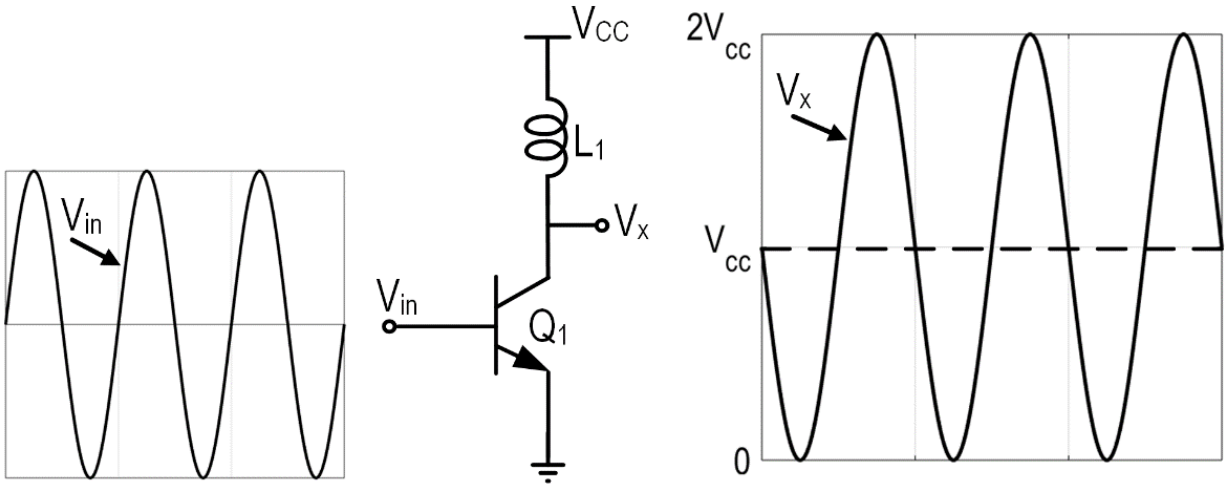

Figure 2.9: class A, ideal output voltage waveform.

In Figure 2.8, the biasing point of a class A amplifier is shown. It is chosen in such a way that the transistor is always operating in the active region. In fact, saturation and breakdown regions must be avoided to ensure linearity. In an ideal class A, the collector voltage has a peak-to-peak swing bounded ideally to $2V_{CC}$ as shown in Figure 2.9, but in a real design to avoid entering the saturation and breakdown region, the peak-to-peak value is reduced to $V_{CE,max} - V_{CE,sat}$. The parameter of $V_{CE,sat}$ is the minimum collector-emitter voltage that maintains the transistor in the active region while $V_{CE,max}$

is the maximum collector-emitter voltage avoiding entering breakdown region.

To calculate the class A efficiency, it is necessary to apply (2.2) and therefore we need an expression for P_{out} and P_{DC}. The first is the power delivered to a load R_x by a sinusoidal signal of amplitude V_x and can be written as:

$$P_{out} = \frac{V_x^2}{2R_x} \qquad (2.12)$$

To calculate P_{DC}, remember that the inductor sets a collector voltage of V_{CC} , and that R_x is the impedance seen at the collector, and then the DC current must be equal to $\frac{V_{CC}}{R_x}$. Therefore, P_{DC} assumes the following expression:

$$P_{DC} = V_{CC} I_{DC} = \frac{V_{CC}^2}{R_x} \qquad (2.13)$$

The ratio of (2.12) and (2.13) represents the efficiency of the amplifier:

$$\eta = \frac{V_x^2}{2V_{CC}^2} \qquad (2.14)$$

To calculate the maximum ideal efficiency of the class A, we need to make three assumptions: first, the collector voltage must be a sinusoid with a peak swing equal to the supply voltage V_{CC}, second, when the collector reaches 0V the non-linearity introduced by the transistor must be considered negligible, and third, the matching network has no losses. In this case, η reaches 50% at the maximum Pout. In real designs, as explained earlier, the maximum swing is a bit smaller than the ideal one, leading to a maximum efficiency typically around 40%. The collector voltage swing V_x is not a very meaningful parameter in a PA, since usually we deal with power quantities, so it is better to express efficiency in function of the output power and maximum output power. To do this, we need just to observe that:

$$P_{out,max} = \frac{V_{CC}^2}{2R_x} = \frac{1}{2} I_{DC} V_{CC} = \frac{1}{2} P_{DC} \qquad (2.15)$$

Then η can be written as:

$$\eta = \frac{1}{2}\frac{P_{out}}{P_{out,max}} \qquad (2.16)$$

(2.16) shows that the Class-A efficiency is bounded to 50% at the maximum Pout, and decreases linearly with Pout when the PA is operated in back-off (Pout<Pout,max).

b) Class-B PA

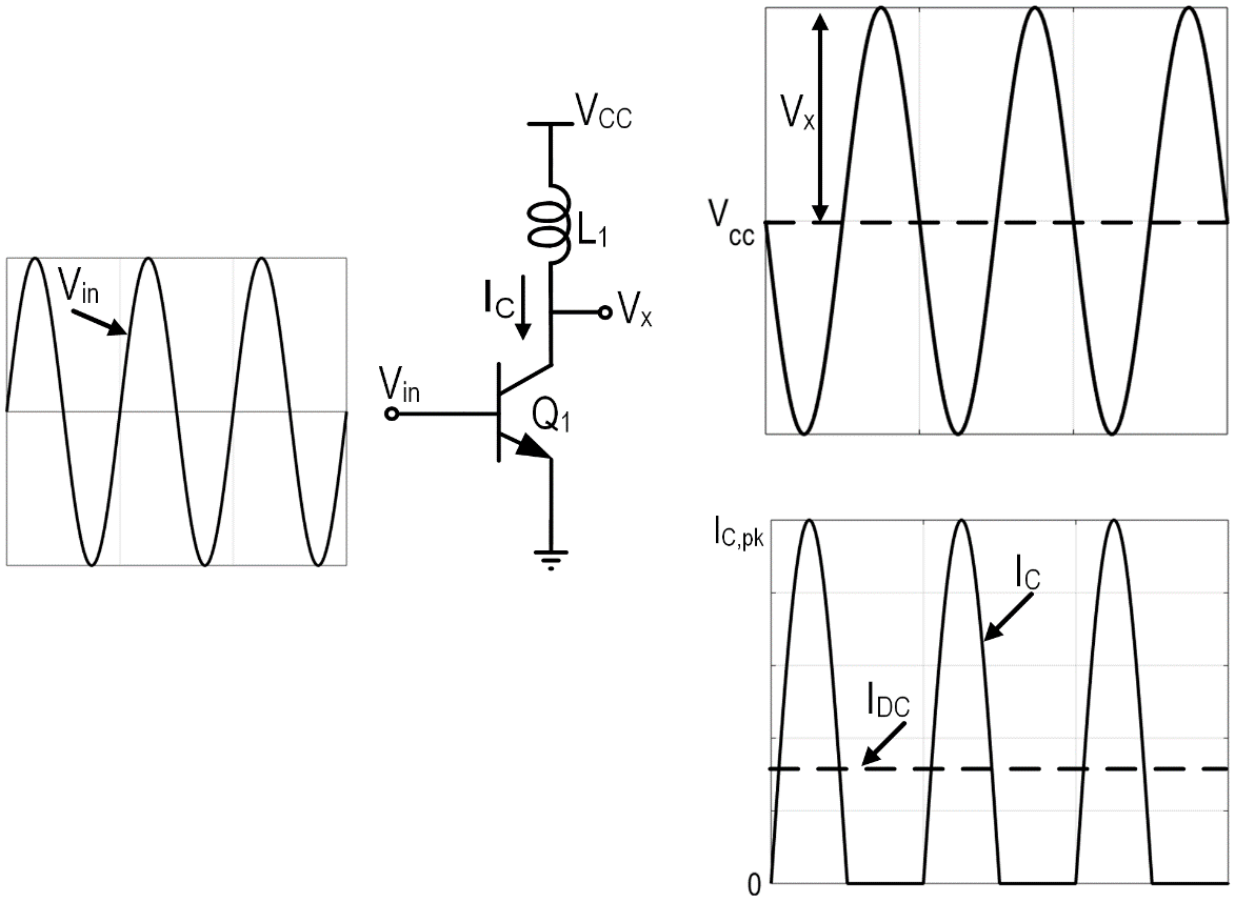

Figure 2.10: class B voltage and current waveforms (maximum efficiency swing).

Class B power amplifier trades linearity for a higher efficiency. Biasing the transistor at the edge of turn-on we impose a conduction angle of 180° degrees, reducing the dissipated power. The circuit is equal to the one used for class A (Figure 2.7), but the biasing point is different. Basically, the transistor in class B turns on just

for half period and generates a rectified current sinusoid I_C that flows into the load (Figure 2.10). This waveform is filtered by the matching network that produces a voltage sinusoid at the output.

Let's analyse more in detail the collector current. Since it is a rectified sinusoid, it can be written as the product between a sinusoid and a square wave toggling between 1 and 0. Expanding the square wave using its Fourier series, we can perform the calculations that give us the amplitude of the dc and fundamental components.

$$I_C = I_{C,pk}\sin(\omega t) \times \left[\frac{1}{2} + \frac{2}{\pi}\left(\sin(\omega t) - \frac{1}{3}\sin(3\omega t) + \frac{1}{5}\sin(5\omega t) \ldots\right)\right] \quad (2.17)$$

where $I_{C,pk}$ is proportional to the input signal ($V_{in}g_m = I_{C,pk}$). The product between the two components at frequency ω gives a dc term equal to $I_{C,pk}/\pi$ (shown also in Figure 2.10), while the product between the sine and the dc term of the square wave gives a fundamental tone of $0.5\, I_{C,pk}\sin(\omega t)$. Since the matching network at the collector is tuned to work around ω, the higher harmonics of I_C will be suppressed and only the fundamental tone will appear at the output. Then the output power is:

$$P_{out} = \frac{1}{4} I_{C,pk}^2 R_x \quad (2.18)$$

where R_x is the impedance seen at the input of matching network from collector. The DC power can be written as:

$$P_{DC} = I_{DC}V_{CC} = \frac{I_{C,pk}}{\pi}V_{CC} \quad (2.19)$$

then through (2.2), we calculate the efficiency as:

$$\eta = \frac{\pi}{4}\frac{I_{C,pk}R_x}{V_{CC}} \quad (2.20)$$

Observing that $I_{C1} = \frac{V_x}{R_x}$, where $V_x$is the collector voltage swing, leads to:

$$\eta = \frac{\pi}{4}\frac{V_x}{V_{CC}} \qquad (2.21)$$

For $V_x = V_{CC}$, the efficiency is around 79%. Also in this case, the efficiency can be expressed as a function of the output power. Remembering expressions (2.12) and (2.15), efficiency can be written as:

$$\eta = \frac{\pi}{4}\sqrt{\frac{P_{out}}{P_{out,max}}} \qquad (2.22)$$

Basically, we have to choose between class A and class B that are the only classes able to work at 80GHz while generating a useful amount of output power (≅ 20 dBm) with a good efficiency.

Looking at η and comparing (2.16) with (2.22), the choice seems easy; class B is for sure superior with respect to class A. In fact, not only the peak efficiency is almost 30% higher, but also in back-off, its performance is significantly better.

Recalling (2.14), the formula for class A efficiency, it is easy to observe the quadratic dependence of η on the output swing. This behaviour leads to a serious degradation of the efficiency as the PA works more and more in back-off. To improve the situation, different techniques can be employed. For example, scaling the bias current of the transistor together with V_X. This is the same principle that makes class B so efficient. As observed in (2.19), the DC power consumption changes with I_{C1}, that is proportional to the input signal. Therefore, at lower input levels, the PA draws less power from the DC supply increasing its efficiency with respect to the regular class A whose DC power consumption is constant. If the same concept was applied to a class A power amplifier, its I_{DC} would become $\frac{V_X}{R_X}$ leading to:

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{V_X}{2V_{CC}} \qquad (2.23)$$

The efficiency would change linearly with V_X, as in a class B amplifier, granting a

higher back-off. To get back to the ideal 50%, also the supply voltage should change accordingly to the swing, but it is a difficult task to design such a variable supply and moreover a supply modulator requires additional voltage headroom that limits the output power.

Considering the 6dB back-off case (corresponding to a swing equal to half V_{CC}), supposing a 1.8 V supply, in regular class A, an 12.5% efficiency is achieved, while using (2.21) we can calculate a class B collector efficiency equal to 39% at back-off. In summary, class-B operation is highly desirable as long as power efficiency is considered. However, for a given transistor, the gain in class B is half that of class A and since the gain of devices at mm-wave is low, class B is not widely used.

2.2.2: mm-Wave PAs State-Of-The-Art

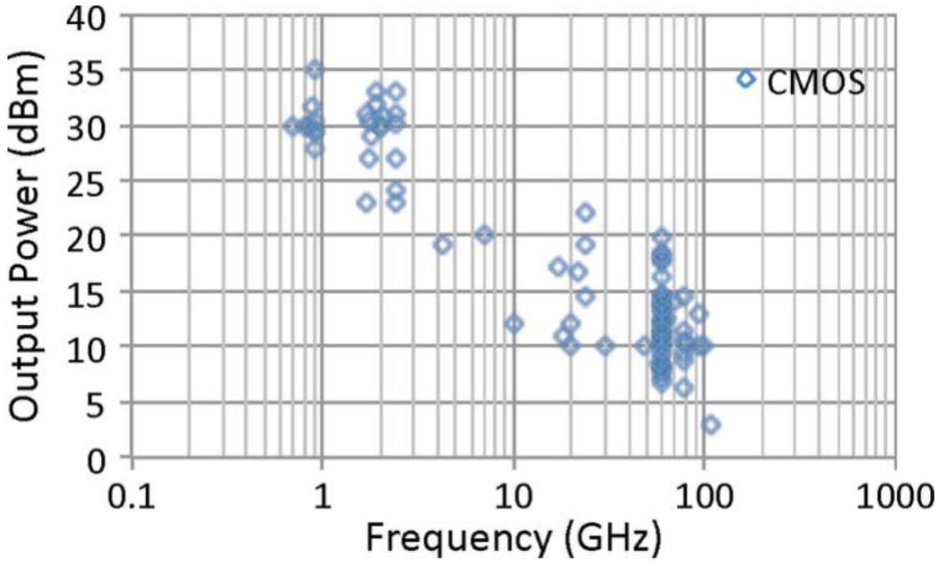

Figure 2.11: Comparison of OP1dB of CMOS PAs [9].

In the last decade, much efforts have been spent to improve mm-Wave PAs performance both in CMOS and in BiCMOS technologies. Two main characteristics must be emphasized when analysing and comparing different works from literature:

a) The maximum output power (Psat) and 1dB-compression output power (OP1dB);

b) The PA power efficiency (PAE) at Psat, OP1dB and back-off.

The output power corresponding to 1dB gain compression of CMOS PAs over broadband can be compared in Figure 2.11 [9]. According to this plot, OP1dB decreases as frequency increases.

Figure 2.12 indicates the OP1dB of both CMOS and SiGe PAs, mostly for the frequency range of 24-90GHz. From this plot provided by literature review, it can be concluded that SiGe Technology does not provide a major advantage compared to CMOS PAs.

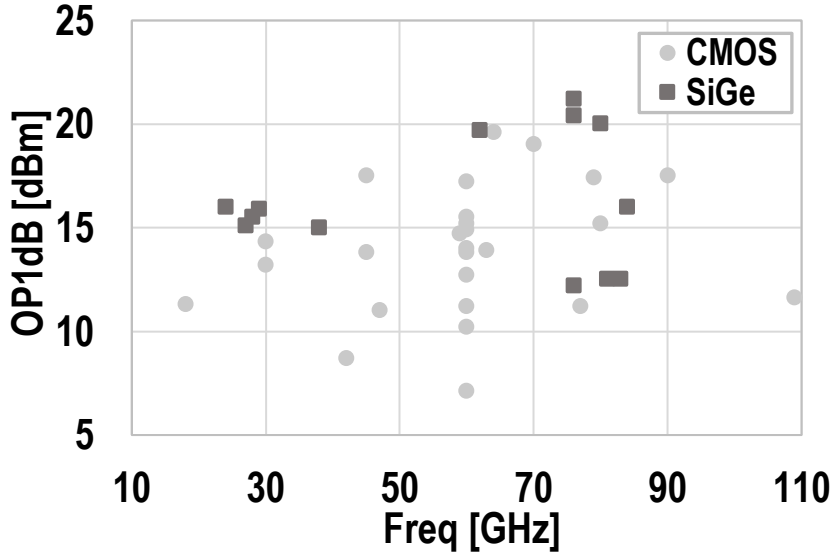

Figure 2.12: Comparison of OP1dB of silicon PAs.

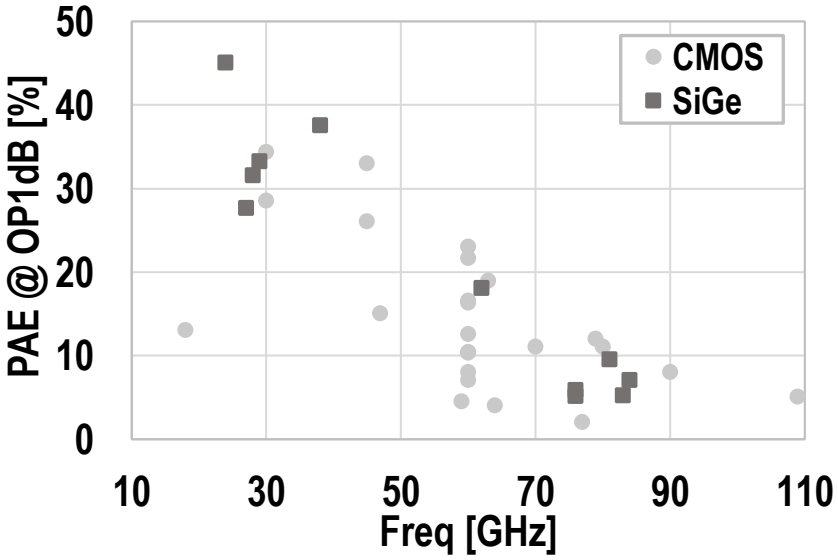

Figure 2.13: Comparison of PAE of silicon PAs at OP1dB.

Figure 2.13 prepared by literature review shows the PAE of silicon PAs at OP1dB, at the onset of the linear range, at different operating frequency. The efficiency drops drastically when frequency increases. The efficiency at OP1dB is much lower than the theoretical limits of class-A and class B, because of:

1) Loss of matching network.
2) $V_{C,max} \ll V_{CC}$ yielding $OP1dB \ll Psat$

From Figure 2.14, it can be observed that when output power is decreasing in back-off, its efficiency is drastically reducing. Comparing Figure 2.13 and 2.14 verifies that efficiency in back-off region drops very much compared to PAE at OP1dB, because most of the PAs are biased in class A which means they have constant DC current consumption independently from Pout.

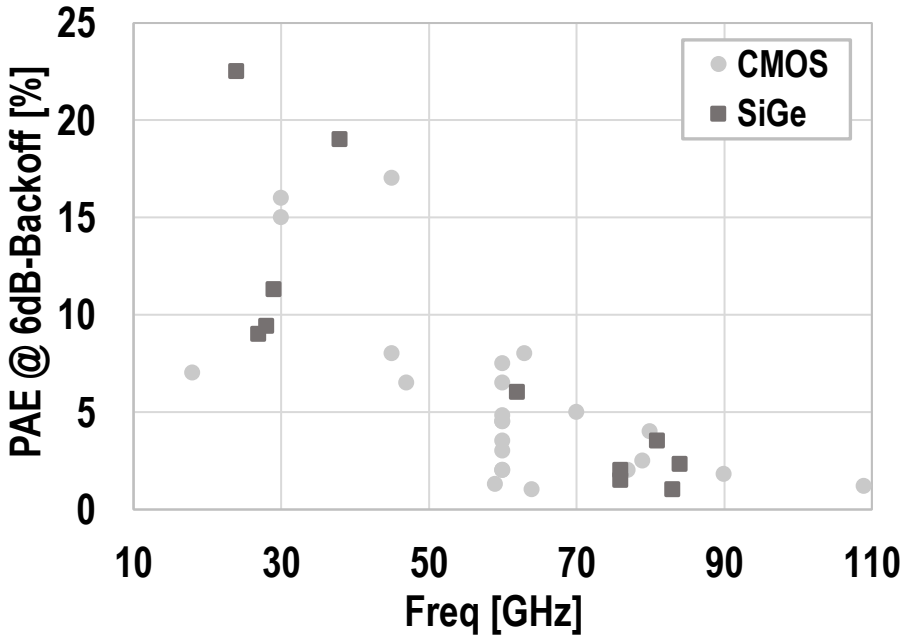

Figure 2.14: Comparison of PAE of silicon PAs at 6dB-backoff from OP1dB.

In the following, four configurations of CMOS PA and SiGe PA will be reviewed in details with some observations on their works. Finally, the performances of some recent published PAs in both CMOS and SiGe technologies will be summarized.

1. CMOS 4-way PA

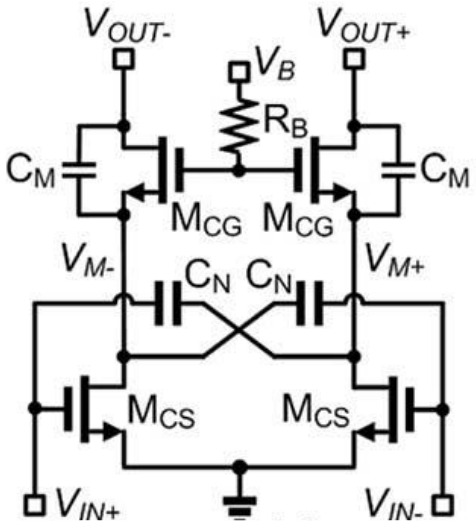

Figure 2.15: Schematic of the neutralized bootstrapped cascode amplifier [10].

[10] presents 4-way combining PA in 40-nm CMOS for E-band applications employing cascode amplifier to increase the output voltage swing without over-stressing transistors as shown in Figure 2.15. Also, neutralization technique was proposed to neutralize the gate-to-drain capacitance of the transistor and therefore enhance the power gain and stability. The proposed PA achieves a measured Psat and OP1dB of 22.6dBm and 18.9dBm, respectively. with 19.3% peak PAE. The measured PAE at Psat and OP1dB are 19.3% and 10.7%, respectively, while efficiency at 6dB back-off from OP1dB is 3.3% which can be estimated from the plot.

There is a 3.7dB difference between Psat and OP1dB which causes significant drop in efficiency at OP1dB compared to the peak PAE. As discussed before, PAE at back-off is critical, however, it is very poor in this paper.

2. CMOS Doherty PA

[11] proposes a mm-wave transformer-based Doherty without using additional building blocks such as a supply modulator and an input signal processor as shown in Figure 2.16.

In this topology, the class AB main amplifier is ON for the whole range of input power, but the class C auxiliary amplifier is OFF for low input power resulting in power saving. The transformer-based Doherty topology needs amplifiers with high output impedance to achieve this enhancement of back-off efficiency. When the input power is low and then auxiliary amplifier is OFF, the finite output impedance of the auxiliary amplifier results in efficiency degradation. It is hard to have mm-wave CMOS amplifiers with high output impedance due to short channel effects and parasitic drain–source capacitance of the transistors.

The tuning inductor at the output of auxiliary amplifier is proposed to resonate with the parasitic output capacitance, and then high impedance is seen at low power levels. Moreover, when the auxiliary amplifier becomes ON at high input power, the LC tuning circuit acts as a step-down impedance transformer. Thus, the auxiliary amplifier sees lower load impedance compared to the main amplifier resulting in further improvement of the back-off efficiency.

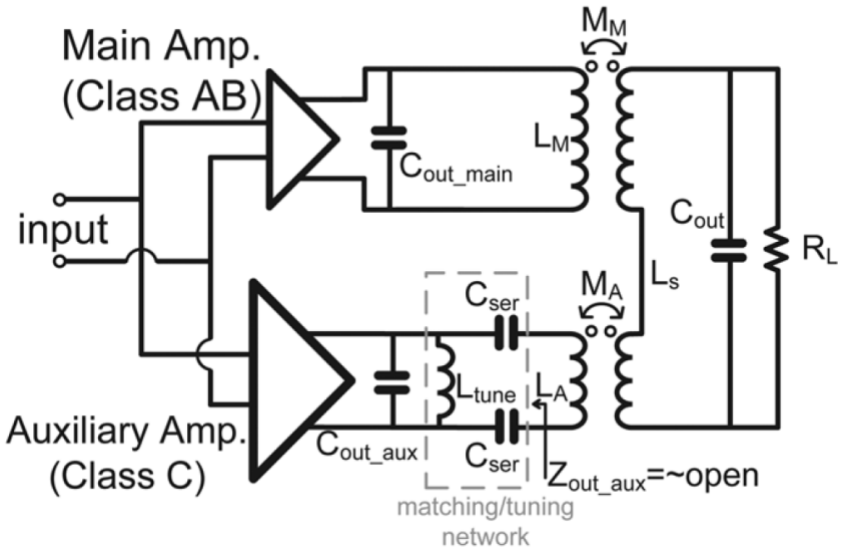

Figure 2.16: Schematic of the transformer-based Doherty PA for mm-wave applications using asymmetrical transformer and matching/tuning network [11].

The second implementation achieves 21dBm Psat at a 1.5V supply. The peak PAE and PAE at OP1dB and 6-dB back-off are 13.6%, 12.4%, and 7%, respectively. Even if this PA demonstrates very low drop in efficiency at OP1dB compared to the peak

PAE and a higher PAE at 6dB-backoff, at least two time better than other recent published mm-wave PAs, however, peak PAE and PAE at OP1dB are still not high enough.

3. SiGe 16-way PA

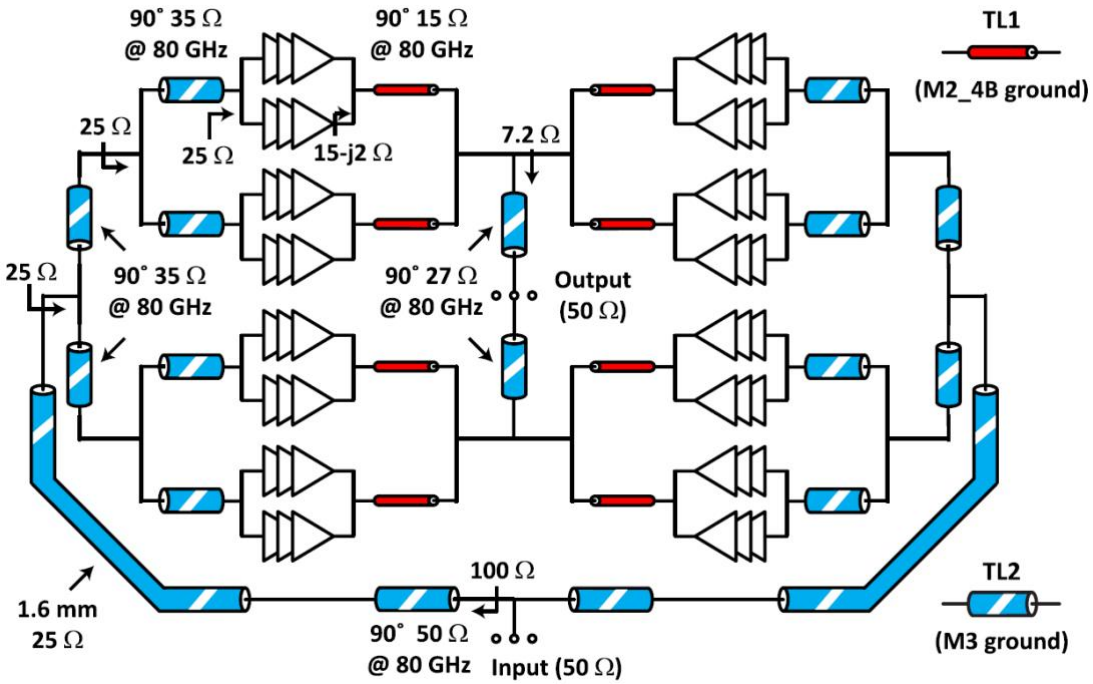

Figure 2.17: Schematic of the 16-way power-combining amplifier [12].

A fully integrated 16-way power-combining amplifier for 67–92GHz applications was implemented in 90-nm SiGe-HBT technology [12]. As presented in Figure 2.17, this 16-way power amplifier employs three-stage common-emitter single-ended PAs, and reactive λ/4 impedance transformation networks for power combining. The three-stage single PA achieves a Psat of 14.3–16.4dBm at 68–99GHz. The power combining PA has a Psat of 25.3–27.3dBm with PAE of 5-12.4% at 68–88 GHz. It can be estimated from the plots in the paper that 16-way PAs has a OP1dB of 20-22.3dBm with PAE of 3.5% at 22.3dBm OP1dB while PAE at 6dB-backoff from OP1dB is only 1.5%. Even though this PA delivers highest Psat to our knowledge, however, there is a significant difference between Psat and OP1dB, and also PAE performance of this PA is very low.

4. SiGe Dual-Path PA

A dual-path, three-stage transformer-coupled common-base power amplifier was fabricated in 130nm SiGe-BiCMOS, and its schematic is shown in Figure 2.18 [13]. The collector-emitter neutralization is introduced to increases reverse isolation and stability.

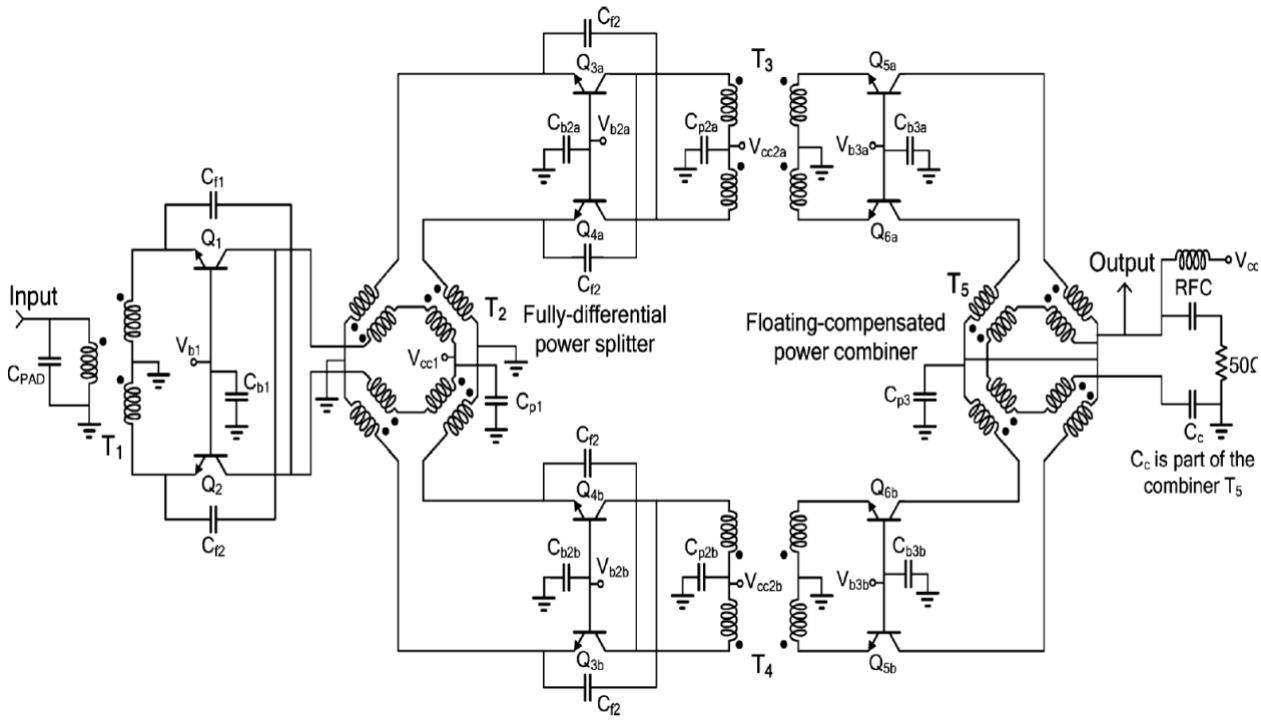

Figure 2.18: Simplified schematic of the 3-stage, transformer-coupled PA [13].

This PA produces peak output power of 20.1dBm and peak PAE of 18% at 62GHz. Another version of this PA in the frequency range of 79–87.5GHz was also implemented to show frequency scalability of the design. The 79GHz PA prototype achieves 18dBm Psat and 9% peak-PAE at 84GHz from a 2.5V supply.

This configuration of PA is the only one that employed common-base as gain stages. Common-base gain stage shows collector-emitter breakdown voltage larger than 3V, resulting in less than 1dB difference between OP1dB and Psat at 62GHz, and 2dB difference at 80GHz which is desirable and will be studied more in the next chapter. Accordingly, PAE at OP1dB is close to peak PAE. However, the overall performance of this PA shows poor efficiency.

2.3 : Conclusions

In summary, silicon E-band PAs with maximum Pout close or above 20dBm in saturation (Psat) have been reported, both in CMOS [10], [11], [14], [15] and BiCMOS technology [13], [16], [17]. A record Psat of 27dBm was also demonstrated by making extensive use of power combining [12]. To the authors' knowledge, the highest power added efficiency (PAE) reported so far is in the range of 19-22% with PAs driven into the saturation region [10], [14]. However, at the edge of the useful linear range, i.e. at OP1dB, PAE is limited to 6-12% only and PAE drops quickly when Pout is reduced further, being 1-3% only at 6dB back-off from OP1dB. The topology [11] keeps reasonably good efficiency in back-off by resorting to a Doherty architecture, but at the cost of design complexity and limited PAE at Psat and OP1dB.

A key issue at the origin of the poor PAE in linear range is the relatively large separation between Psat, where efficiency peaks, and OP1dB. Most of the reported E-band PAs are based on a common-source/emitter output stage which suffer from soft saturation. OP1dB is up to 2-3dB below Psat leading to 40-50% PAE penalty. Furthermore, class-A biasing is commonly selected for maximum gain [10], [12], [16], at the cost of a faster roll-off of PAE in back-off. Class-AB may slightly improve PAE in back-off, thanks to a supply current which partially scales with Pout, but at the cost of gain reduction [10], poor linearity (AM-PM in particular [18]), and still suffering from soft saturation.

Chapter 3:

Common-base current clamping Power Amplifier

In this chapter, the main topic of the thesis would be introduced which is idea proposed in the output stage of the power amplifier presented in "***A SiGe BiCMOS E-Band Power Amplifier with 22% PAE at 18dBm OP1dB and 8.5% at 6dB Back-Off Leveraging Current Clamping in a Common-Base Stage***" [19]. Firstly, the advantageous of the common base configuration versus the common emitter would be displayed and then the concept of current clamping is explained.

3.1: I-V Curves Comparison between common-base and common-emitter configurations

Differently from field-effect devices, bipolar junction transistors (BJT) show a significant dependence of the output I-V curves on the stage topology, e.g. common-emitter (CE) vs common-base (CB), suggesting investigation of the most suited configuration for best PA performance [21]. Desirable transistor features are high breakdown voltage, flat output curves and a minimum voltage drop to operate in active region (typically denoted as V_{knee}). In addition, stability against temperature variation is key, being the devices subject to significant self-heating effects. This issue is particularly relevant in modern SiGe technologies, where device shrinking and use of shallow and deep trench isolations are responsible for thermal resistance increase [22].

The break-down voltage and temperature stability of the BJT are strongly influenced by the impedance level at the driving terminals [22]. To gain insight, Figure 3.1 compares the I-V output curves for the same BJT, with emitter area of 10x0.24μm^2 and geometry of 5xCBEBC, in CE and CB configurations. The device thermal resistance is ~600°K/W.

3.1.1: Common-Emitter Behavior

When operated in CE, the BJT can be driven with high or low impedance by forcing the base current I_B, (Figure 3.1a) or the base-emitter voltage V_{BE} (Figure 3.1b). When I_B is injected, the effect of self-heating is a reduction of the collector current I_C due to a negative thermal-electric feedback [22], [23], leading to the negative slope of the I-V curves visible in the region of highest power dissipation. In this configuration, the maximum Pout is limited by avalanche breakdown. Under high electric field, holes generated by impact ionization in the base-collector junction flow back toward the base and increase the base-emitter voltage, leading to a progressively larger I_C that eventually destroys the device [24]. From Figure 3.1a, the collector-emitter breakdown voltage with open base, BV_{CEO}, is ≈1.5V and the maximum collector voltage swing ensuring reliable operation is limited to 550 $mV_{0\text{-}pk}$ only. The slope of the load-line in Figure 3.1a corresponds to 13.7Ω. The simulated OP1dB and Psat at 80GHz, assuming a loss-less matching network and the transistor supplied at 1V, are 9.3dBm and 11.5dBm, respectively.

When V_{be} is set by a voltage source, impact-ionization generated holes flowing out from the base are shorted to ground and the breakdown voltage is drastically increased to V_{CE}>2V (Figure 3.1b). On the other hand, at fixed V_{be} the thermal-electric feedback becomes positive leading to a sharp increase of I_C due to self-heating and thermal instability [22], [23]. Thermal breakdown is now the major limiting factor to Pout, because the maximum device current must be reduced, compared to Figure 3.1a, to limit the risk of thermal runaway. The slope of the load line in Figure 3.1b corresponds

to a load resistance of 26Ω and the simulated OP1dB and Psat are 10.8dBm and 13.6dBm, only a marginal improvement compared to the forced-I_B situation. In both cases, the large separation of 2-3dB between OP1dB and Psat can be attributed to the variable (signal dependent) slope of I_C and the smooth transition from off-state (V_{CE}=0, I_C=0) to active region with a relatively large V_{knee} ≈0.4-0.5V.

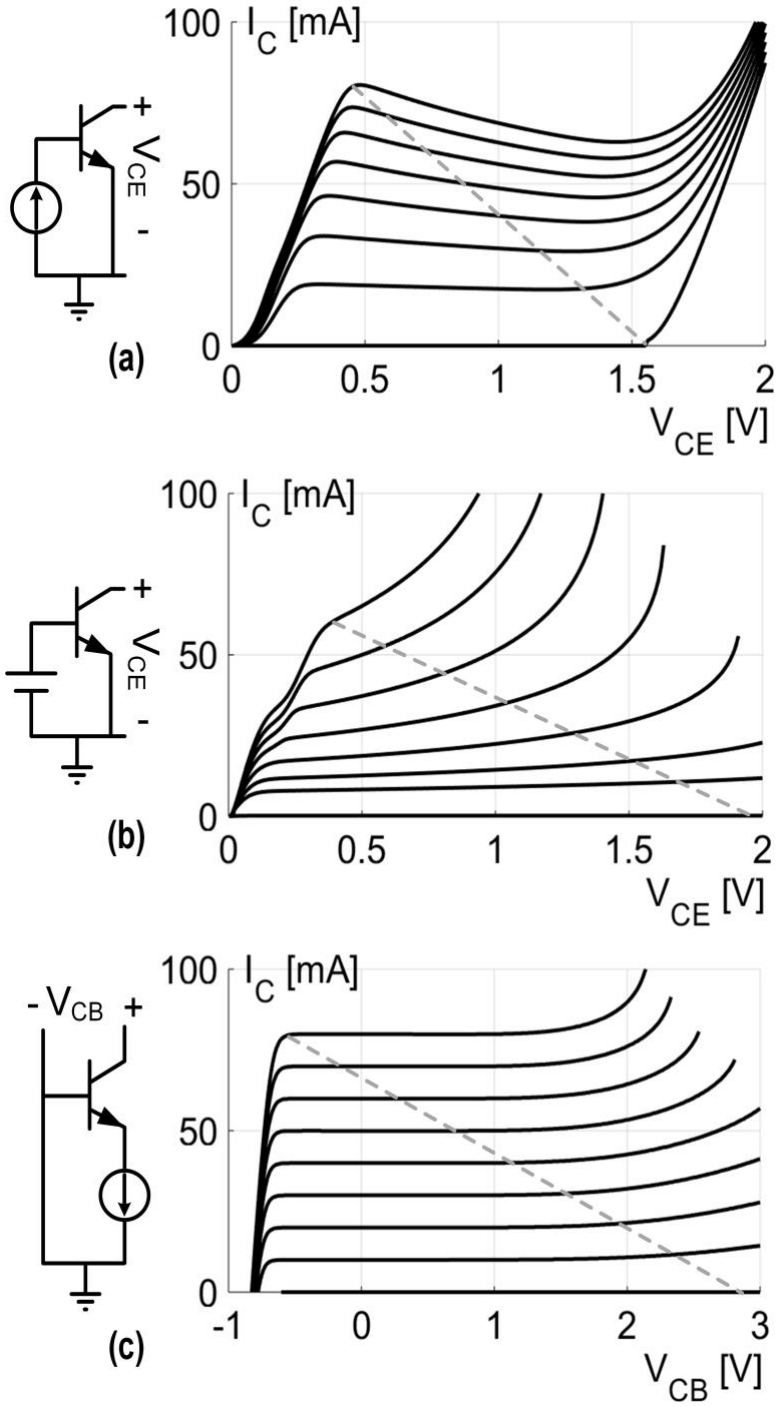

Figure 3.1: I-V curves and load-line for the same transistor in different configurations.

3.1.2: Common-Base Behavior

The transistor in CB yields a remarkable performance improvement, as visible from the I-V curves in Figure 3.1c. The low impedance at the base keeps high avalanche breakdown voltage, while the large transistor degeneration set by the emitter current source drastically improves the temperature stability, leading to flat I_C curves over a wide output voltage range. The slope of the load line in figure 3.1c is 42Ω and, at 1.8V supply, OP1dB and Psat are 15.6dBm and 16.6dBm, respectively.

For a fixed transistor size, the CB configuration allows a remarkably larger output power than CE. Moreover, the higher optimum load resistance requires less impedance transformation of the antenna resistance, limiting the loss of the output matching network. Finally, thanks to the flat I-V curves and the sharp transition from off-state to the active region (with $V_{knee}\approx 0.2V$) OP1dB is only 1dB lower than Psat, thus yielding a PAE at the onset of the PA linear region close to the peak value. Finally, it is worth mentioning that the CB stage breaks the parasitic feedback set by C_μ (the base-to-collector capacitance) that in CE amplifiers is responsible for gain penalty and stability issues and at high frequency the CB configuration may provide comparable or larger power gain than CE.

Combining the CE and CB transistors in a cascode stage enables larger output voltage swing, compared to the CE alone, and may limit self-heating by distributing the power dissipation among the two devices. However, the separation between OP1dB and Psat is larger than in the CB alone, because of the higher V_{knee} required to keep in active region two staked devices.

3.2: Current Clamping in the Common-Base Stage

The concept of current clamping applied to the CB configuration is proposed in this

section. It will be shown that if the high impedance at the emitter of the CB amplifier is provided by an inductor or a resonant LC-tank, current-clamping can be exploited to achieve a DC current in the transistor which tracks the envelop of the signal current. This rises the PAE in back-off, i.e. when the amplifier delivers envelop modulated signals, or a continuous wave signal with Pout lower than Psat. Current clamping in the CB stage leads to a PAE profile in power back-off like a CE amplifier in class-B, but with negligible penalty in gain or linearity. The well-known diode voltage clamping circuit, shown in Figure 3.2a, reproduces the input (sinusoidal) waveform at the output, clamped to ground by adding a DC voltage component equal to the peak value [25]. In this work, the current-mode implementation of this principle is proposed to set a DC current in the PA output stage tracking the peak signal value.

3.2.1: Current Clamping Implementation

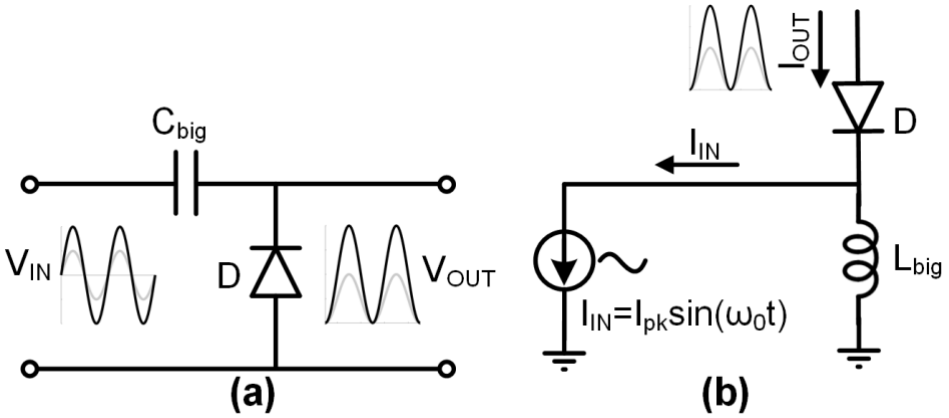

Figure 3.2: Diode voltage-mode **(a)** and current-mode **(b)** clamping circuits.

The diode current-clamping circuit is depicted in Figure 3.2b. It is derived from the voltage-mode counterpart by replacing the series capacitor with a shunt inductor, and considering the diode current in place of the voltage across the diode. Shown in Figure 3.3, the CB stage lends itself to exploiting of this principle. The diode and inductor in Figure 3.2b are implemented with the base-emitter junction of Q_1 and inductor L_E. First, let us assume the parasitic capacitance C_{BE}=0. If the base bias voltage, V_b, is set for low quiescent current in Q_1 (ideally zero), the transistor is off during the first half

negative cycle of $I_{IN}(t)$ and L_E charges up to I_{pk}. Then, the DC current of Q_1 and L_E equals I_{pk}. Q_1 turns on with emitter current $I_E(t)=I_{pk}+I_{pk}\sin(\omega_0 t)$. Assuming L_E ideally infinite, Q_1 never switches off and operates in class-A. With L_E large but finite, the inductor is partially discharged by the non-zero emitter resistance, and Q_1 turns-off for a very short time interval in each cycle allowing the inductor to be recharged and track I_{pk}. As a result, the average collector current of Q_1 scales with the envelope of the signal current, similarly to an ideal class-B common-emitter stage.

3.2.2: High Frequency Effects

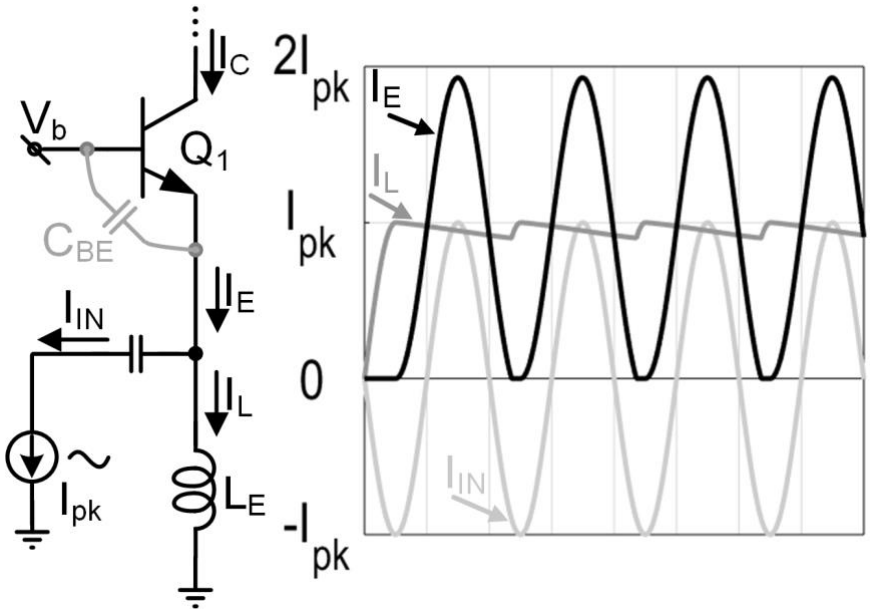

Figure 3.3: Current clamping in a common-base stage and current waveforms.

If the principle of current clamping technique is exploited at high frequency, the effect of C_{BE} becomes more and more important. When Q_1 is off, C_{BE} absorbs part of the signal current, slowing-down the L_E charging. The effect is shown in Figure 3.4, plotting the simulated inductor current, I_L, when the frequency of the input current source in Figure 3.3 is 80GHz.

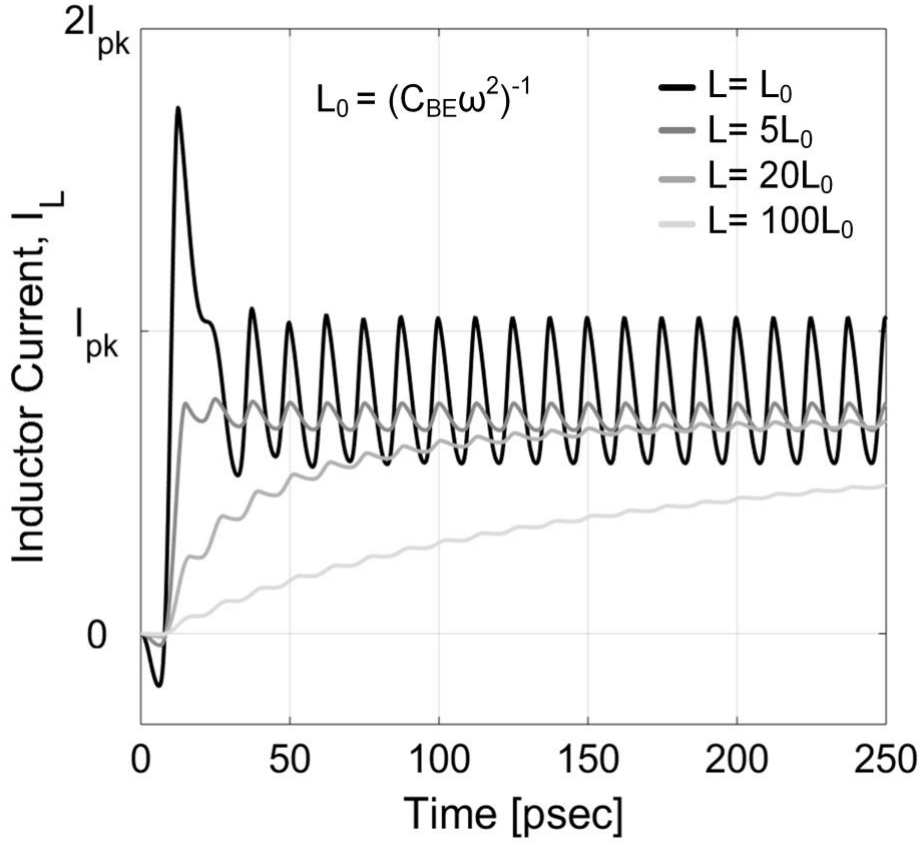

Figure 3.4: Inductor current for the circuit in Figure 3.3 versus time when input frequency is 80GHz, at different values of L_E.

Different values of L_E normalized to L_0 (resonating with C_{BE} at 80GHz) are considered. L_E charges with an exponential-like transient and the time required to reach steady state can be reduced scaling down the inductor value. The ripple rises, when reducing L_E, but the final average of I_L is not affected. Interestingly, looking carefully at Figure 3.4 and comparing with I_L plotted in Figure 3.3, the effect of C_{BE} is a slightly lower steady-state DC current, $I_{DC} \approx 0.8 I_{pk}$. This implies that Q_1 operates more in class-AB, with a conduction angle less than 360°, yielding a mild efficiency improvement. The reason can be qualitatively explained as follow. Without C_{BE}, when Q_1 turns-off $I_L = I_{IN}$ and the L_E is recharged to I_{pk} in each cycle very quickly. In this case, the emitter voltage $V_e(t)$ looks like a train of high and narrow positive pulses, with harmonic rich content. With C_{BE}, only a fraction of I_{IN} charges L_E, thus Q_1 is off for a longer time, and the steady-state average current is reduced. Looked at in frequency domain, C_{BE} decreases the impedance at the emitter node for harmonics of I_{IN} making $V_e(t)$ more

sinusoidal. Being the average of $V_e(t)=0$, the conduction angle of Q_1 is reduced.

From Figure 3.4, if a too large L_E is selected (e.g. $L_E=100xL_0$) I_L reaches steady state after several cycles of the input signal. This corresponds to a narrow bandwidth to track changes of the input signal envelope, possibly impairing the PA performance when driven by a modulated signal. The charging time can be reduced to 2-3 cycles only by selecting $L_E < 5xL_0$. On the other hand, to maximize the stage current gain $I_{C,\omega_0}/I_{in}$ (being I_{C,ω_0} the fundamental component of I_C), it is convenient to size L_E resonating with C_{BE}, maximizing the impedance at the emitter node at fundamental frequency.

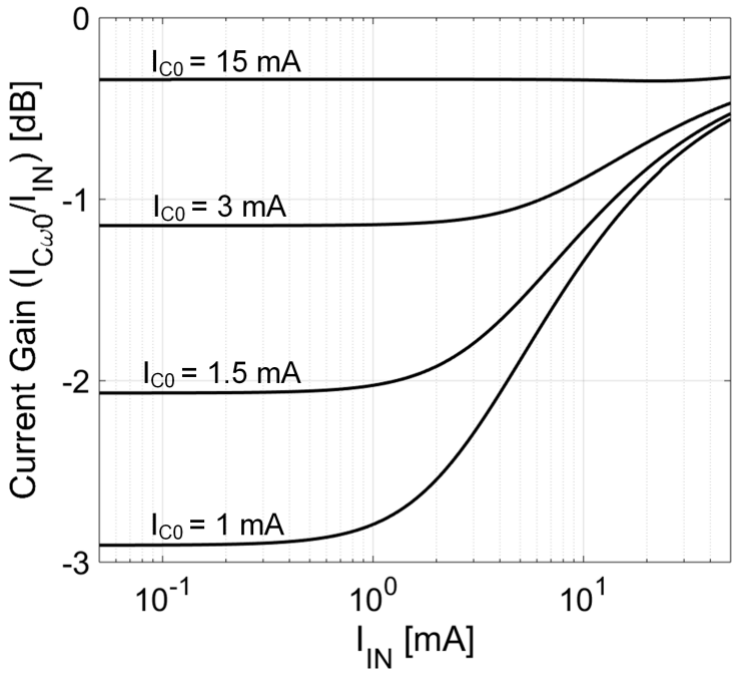

Figure 3.5: Current gain for the common-base stage in Figure 3.3 at different values of the quiescent current.

The finite L_E-C_{BE} tank loss resistance forms a current divider with r_e, the equivalent steady-state emitter resistance of Q_1. r_e decreases when the average current in Q_1 increases, and the latter scales with the input signal amplitude. Therefore, the current divider is responsible for current gain expansion. To gain insight, the current gain is reported in Figure 3.5. Simulations are performed with different values of the quiescent current I_{C0}, the DC collector current when $I_{IN}=0$, set by the base bias voltage V_b. I_{IN} is swept from 0.5mA to 50mA, corresponding to 60dB dynamic range. The gain

expansion is reduced by rising I_{C0}, determining an upper bound for r_e. With I_{C0}=3mA the gain variation is 0.7dB, and it can be further reduced to less than 0.1dB by rising I_{C0} to 15mA.

3.2.3: Linearity Analysis

Figure 3.6 shows the results of two-tone simulation with f_1=79.5GHz, f_2=80.5GHz and I_{C0}=7mA. The average inductor (and transistor) current tracks the input envelope and, compared to biasing in class-A with I_{C0}=I_{pk}=50mA, the peak envelope value, the average current consumption is reduced by ~50%, corresponding to a remarkable 2x improvement of the collector efficiency.

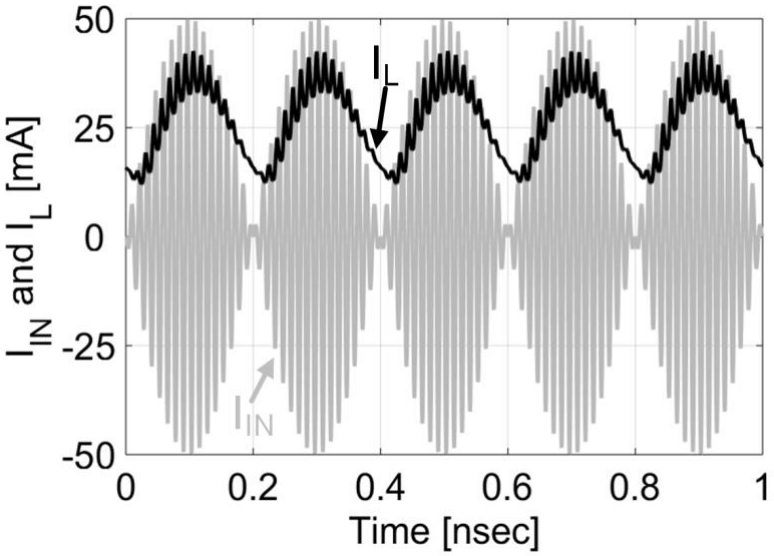

Figure 3.6: Two-tone transient simulation.

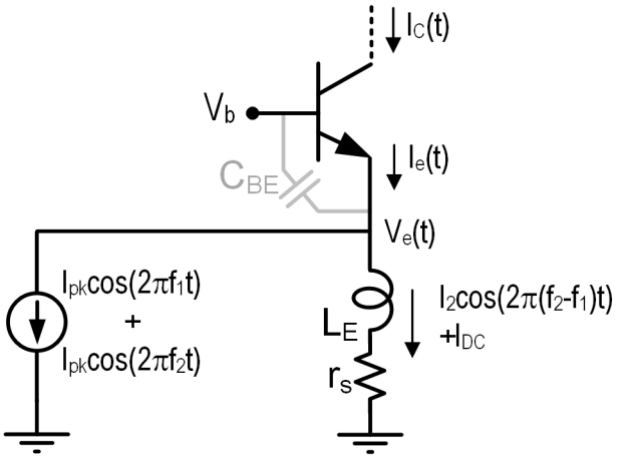

Figure 3.7: Circuit for calculation of IM3 on collector current.

To evaluate the linearity of this PA, we consider the circuit in Figure 3.7 with L_E resonating with C_{BE}. With a two-tone input current, the non-linear distortion of Q1 generates intermodulation products. The input currents flow entirely through Q_1. Moreover, the second order distortion of Q_1 generates a strong component in the emitter current $I_2\cos(2\pi(f_2-f_1)t)$.

As a result, $I_e(t)=I_{pk}\cos(2\pi f_1 t) + I_{pk}\cos(2\pi f_2 t)+I_2\cos(2\pi(f_2-f_1)t)+I_{DC}$. The emitter voltage, $V_e(t) = V_b - \eta V_T \, ln\left(\frac{I_e(t)}{I_S}\right)$ (being I_S the reverse saturation current) can be approximated with the third-order polynomial expansion near $I_e=I_{DC}$:

$$V_e \sim \left.\frac{dV_e}{dI_e}\right|_{I_{DC}} I_e + \left.\frac{d^2V_e}{dI_e^2}\right|_{I_{DC}} I_e^2 + \left.\frac{d^3V_e}{dI_e^3}\right|_{I_{DC}} I_e^3 \qquad (3.1)$$

$$= -\eta V_T \left(\frac{I_e(t)}{I_{DC}} - \frac{I_e^2(t)}{2I_{DC}^2} + \frac{I_e^3(t)}{3I_{DC}^3}\right)$$

where V_T~26mV (at ambient temperature), η is the non-ideality factor of Q_1.

First, the amplitude of the current at (f_2-f_1), I_2, is estimated. The component at frequency (f_2-f_1) of $V_e(t)$ is generated by (1) the components at f_1, f_2 through the second power of $I_e(t)$ in (3.1), (2) the component $I_2\cos(2\pi(f_2-f_1)t)$ multiplied by the linear term in (3.1) and (3) the components at f_1, f_2 with the component at (f_2-f_1) through the third power of $I_e(t)$ in (3.1) which is negligible compared to the others:

$$V_e|_{f_2-f_1} = \eta V_T \frac{I_{pk}^2}{2I_{DC}^2} - \eta V_T \frac{I_2}{I_{DC}} \qquad (3.2)$$

where I_{pk} is the amplitude of the input tones and I_{DC} is the average current of Q_1. At low frequency (f_2-f_1) the reactance of L_E is negligible compared to the inductor series resistance r_s. As a result, I_2 is found solving $I_2 = V_e|_{f_2-f_1} / r_s$:

$$I_2 = \frac{\eta V_T}{2I_{DC}} \frac{I_{pk}^2}{(r_s I_{DC}+\eta V_T)} \qquad (3.3)$$

The IM3 components of $V_e(t)$, are generated by (1) the components at f_1 and f_2 of $I_e(t)$ through the third power of $I_e(t)$ in (3.1), (2) each current component at f_1, f_2 with the component at (f_2-f_1) (with amplitude given by (3.3)) through the second-power of

$I_e(t)$ in (3.1), and (3) each current component at f_1, f_2 with the component at (f_2-f_1) through the third-power of $I_e(t)$ in (3.1) which is negligible:

$$V_e|_{2f_2-f_1,2f_1-f_2} = -\frac{\eta V_T}{4}\left(1-\frac{\eta V_T}{r_s I_{DC}+\eta V_T}\right)\frac{I_{pk}^3}{I_{DC}^3} \qquad (3.4)$$

Because of the finite equivalent parallel resistance of the L_E-C_{BE} resonator, R_P, IM3 on $V_e(t)$ generates IM3 tones on the emitter (and collector) current, with magnitude calculated by dividing (3.4) by R_P, yielding (3.5):

$$I_C|_{IM3} \sim \frac{\eta V_T}{4R_P}\left(1-\frac{\eta V_T}{r_s I_{DC}+\eta V_T}\right)\frac{I_{pk}^3}{I_{DC}^3} \qquad (3.5)$$

IM3 simulations, considering Q=19 for L_E, are reported in figure 3.8 (black curves) for different values I_{C0}. The prediction from (3.5) assuming I_{DC}=I_{C0} are added in the plot as grey lines. At low signal amplitude, Q_1 operates in class-A (with I_{DC}=I_{C0}) and the magnitude of the IM3 tones rises with the third power of I_{pk}, in good agreement with (3.5). When I_{pk}>>I_{C0}, current clamping yields I_{DC} increasing linearly with Ipk. In this region, the IM3 flattens, in agreement with what predicted by (3.5) with $I_{DC} \propto I_{pk}$, and the signal over distortion ratio improves. From a design perspective, the analysis suggests that linearity is improved by increasing R_P and reducing r_s, thus maximizing the quality factor of L_E. But the most effective design choice is rising I_{C0}, as evident from Figure 3.8. Nonetheless, it is worth noticing that the stage is very linear, also at

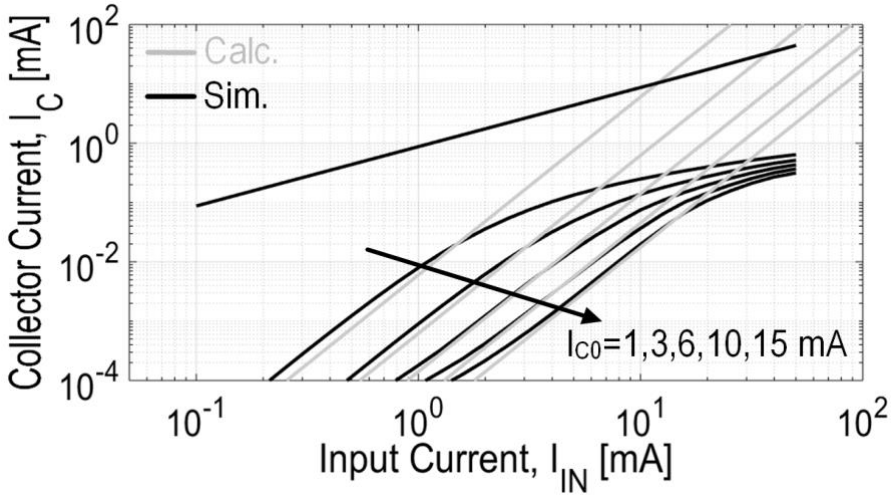

Figure 3.8: IM3 simulations on collector current.

relatively low I_{C0}. As an example, extrapolating the IM3 curve for I_{C0}=10mA yields an intercept point with the fundamental tone at I_{out}=140mA. Assuming the transistor is loaded by the optimal R_L=42Ω (giving OP1dB=15.6dBm, as discussed previously), the OIP3 is 26.1dBm, i.e. more than 10dB above OP1dB.

3.3: Conclusion

The advantage of I-V curves in CB against CE has been studied by simulations and thanks to the flat I-V curves observed in CB configuration, OP1dB is very close to the Psat. Also, the concept of current clamping applied to the CB transistor configuration has been proposed in this chapter. Finally, it has been shown that the DC supply current in a CB stage can be made scalable with the signal swing, improving further the efficiency in back-off without compromising gain and linearity.

Chapter 4:
E-band Power Amplifiers designs

The PAs have been designed in the STMicroelectronics 55nm SiGe BiCMOS technology [26]. This technology (BiCMOS055) is developed on a 300mm wafer line in STMicroelectronics featuring 8 copper metal layers and 1 aluminum capping layer [26]. Table 4.1 presents the thickness of metal layers.

Table 4.1: Thickness of metal layers in BiCMOS055.

	M1	M2X-M5X	M6Z, M7Z	M8U	ALUCAP
Thickness [μm]	0.17	0.19	0.875	2.91	1.45

BiCMOS055 features Low Power (LP) and General Purpose (GP) CMOS devices and 0.45 μm2 6T-SRAM bit cell. Three collector flavors, leading to different maximum current gain transit frequency (f_T) / BV_{CEO} trade-offs for the High Speed (HS), Medium Voltage (MV) and High Voltage (HV) HBTs are available. HS HBT selected in the PAs design exhibits 320 GHz f_T and maximum oscillation frequency of 370 GHz (f_{MAX}) while the typical values of BV_{CEO} and BV_{CBO} are 1.5V and 5.2V, respectively. Collector of the HS HBT is formed by a standard 'buried layer + epitaxy + sinker / deep trenches / SIC' module. Emitters are scalable in width and length with a minimum area of 0.10x0.30 μm^2.

Two different PAs have been realized: a two-stage differential amplifier (single-path PA) and a second version where two amplifiers operate concurrently to rise output power through a transformer-based power combiner (dual-path PA).

4.1: Single-path PA

Before starting the design of single-path PA, it is worth to go deeper into the superiority of CB PA performance against class-A/AB CE alternative at 80GHz and add the investigation of their large signal characteristics.

The schematic diagrams of the two amplifiers are shown in Figure 4.1. Considering the analysis in Section 3.1, low driving impedance is selected for the CE, yielding better performance than the alternative with high base impedance, thanks a breakdown voltage exceeding BV_{CEO}. In Figure 4.1, the CB and CE transistors are followed by an L-type matching network, scaling the 50Ω resistance to the optimal load that maximizes Psat. The matching networks are designed assuming finite quality factor for the inductor (Q_L=20) and capacitor (Q_C=10). The CB transistor delivers Psat=16.2dBm with an emitter area of 5x10x0.2μm^2. According to the analysis in Section 3.1, at given transistor area the CE stage delivers ≈3dB lower Psat than the CB. The transistor in the CE amplifier is then sized with twice the emitter area, A_e=10x10x0.24μm^2, delivering the same Psat of the CB amplifier. The CB transistor is biased at I_{C0}≈10mA, and current clamping rises the average current with Pout. For the CE amplifier two cases are considered: class-A operation, with I_{C0}≈60mA and class-AB, with I_{C0}≈10mA. In class-AB the amplifier shows 0.5dB gain expansion. The simulations results are summarized in Table 4.2. The CB amplifier features the highest power gain. The peak collector efficiency of the CB, at Pout≈Psat, is 37%, close to the class-A CE but lower than class-AB. The superior linearity of CB yields the highest OP1dB of 15.1dBm. The PAE at OP1dB and 6dB back-off of the CB stage outperform the CE in class-A. The PAE of CE in class-AB is only slightly lower than CB, but the class-AB amplifiers features very low gain, challenging the design of the driver stage, and a poor linearity, with OIP3 of 14.5dBm only.

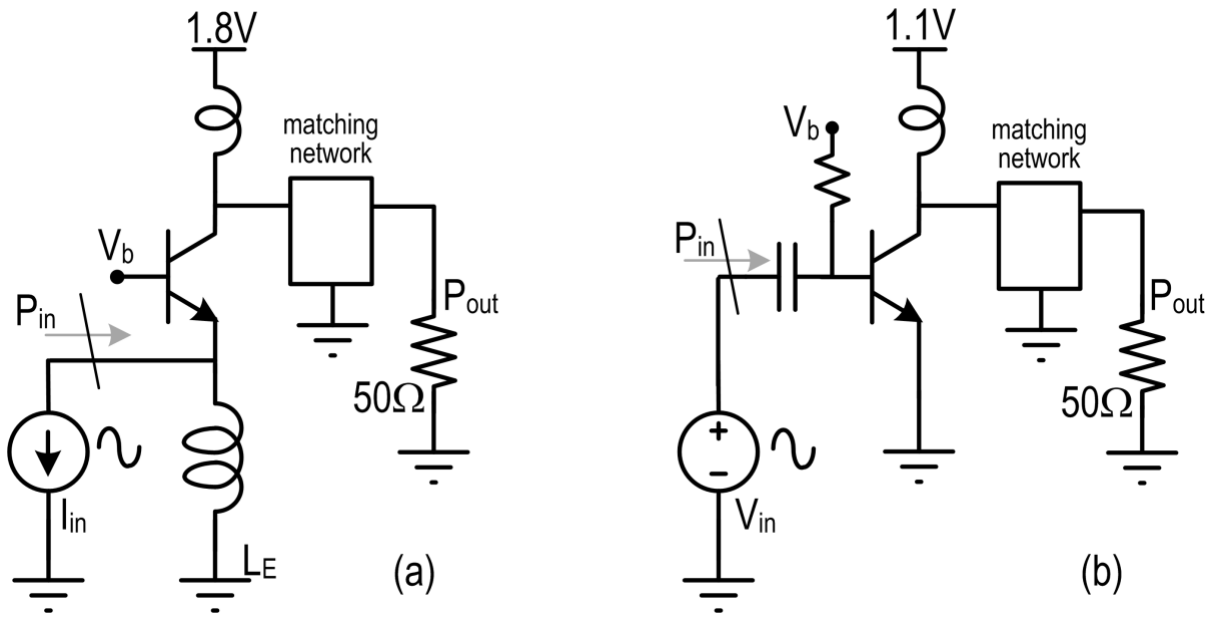

Figure 4.1. Schematics of a CB (a) and CE (b) amplifiers.

Table 4.2. CB and CE amplifiers comparison.

	CB	CE, Class A	CE, Class AB
Power Gain (dB)	9.3	7.5	5
P_{sat} (dBm)	16.2	16.1	16.1
Peak Collector Efficiency (%)	37	35	48
OP_{1dB} (dBm)	15.1	13	14.2
PAE @ OP_{1dB} (%)	33	19.5	26.4
PAE @ 6dB back-off (%)	18	6	13.5
OIP3 (dBm)	26	25.5	14.2

The schematic of the differential PA is shown in Figure 4.2. The size of the transistors in the output stage, $Q_{1a,b}$, is the same considered in Chapter 3 and the I_C-V_{CB} static curves are shown in Figure 3.1c. The supply voltage is V_{CC1}=1.8V and the quiescent current is set to 2x13mA, yielding negligible gain expansion and sufficiently high linearity not to limit the amplifier OIP3. When delivering the maximum Pout, current clamping rises the average current above 100mA. Transformer T1, inductors $L_{1a,b}$ (modeling the metal paths toward the GSG pad) and the pad capacitance realize

the output matching network, scaling the 50Ω load to a differential resistance seen across the collectors of $Q_{1a,b}$ of approximately 70Ω // 60pH. The 1:1 transformer is realized in the top most metal layers and the matching network loss, estimated with EMX electromagnetic simulations, is roughly 0.7dB. Since stability of a CB stage is compromised by the parasitic inductance at the base terminal, $Q_{1a,b}$ are closely laid-out, minimizing the length of the connections from the base to the virtual ground node (V_{b1}), and local bypass capacitance is placed close to $Q_{1a,b}$, from V_{b1} to ground. Moreover, MOM neutralization capacitors of 9fF (not shown in Figure 4.2), cross-coupled from the collectors to the emitters of $Q_{1a,b}$ are added to further improve stability and reverse isolation.

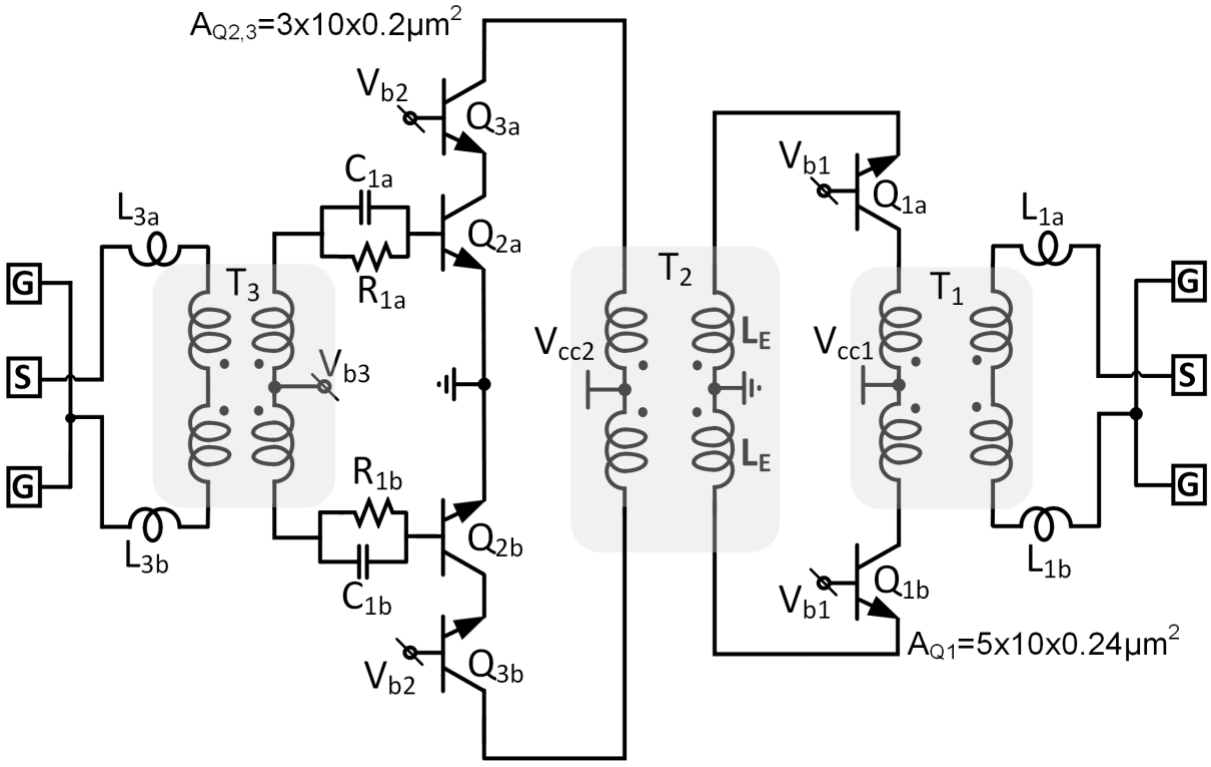

Figure 4.2: Schematic of the two-stage differential power amplifier [19].

The driver adopts a cascode configuration, with $Q_{2a,b}$ and $Q_{3a,b}$ of emitter area A_e=3x2μm², for high output impedance. Transistors are biased in class-A (with 2x24mA from V_{CC2}=2.3V) to achieve maximum transconductance gain and linearity. An inter-stage matching network, realized with transformer T2 tuned on transistors parasitic capacitances, introduces a current gain of ~3 [27]. The simulated quality factor for the transformer inductors ranges from 19 to 22. The simulated power gain

from driver output to the PA output is 7.5dB. The input impedance of the amplifier is matched to 50Ω with transformer T3, $L_{3a,b}$ and the capacitance of the input pad, while resistors $R_{1a,b}$ ensure unconditional stability also at low frequency.

The simulated gain at 80GHz center frequency is 20.5dB and OP1dB is 18dBm. The IM3 generation is mostly determined by the exponential V-to-I characteristic of the driver stage and the simulated OIP3 is 25dBm. AM-PM distortion arises from the non-linear parasitic capacitances at the collector of $Q_{3a,b}$ and at the emitter of $Q_{1a,b}$. The capacitance increases with voltage swing at the nodes, leading to a signal-dependent phase shift of the resonant inter-stage passive network. A pair of thick-oxide varactors with maximum capacitance of 60fF, shown in Figure 4.3a is connected at the collectors of $Q_{3a,\,b}$ to limit AM-PM distortion. Figure 4.3b shows the equivalent capacitance with a sinusoidal voltage of increasing amplitude applied across the varactors pair. The capacitance decreases with signal amplitude, thus compensating the opposite behavior

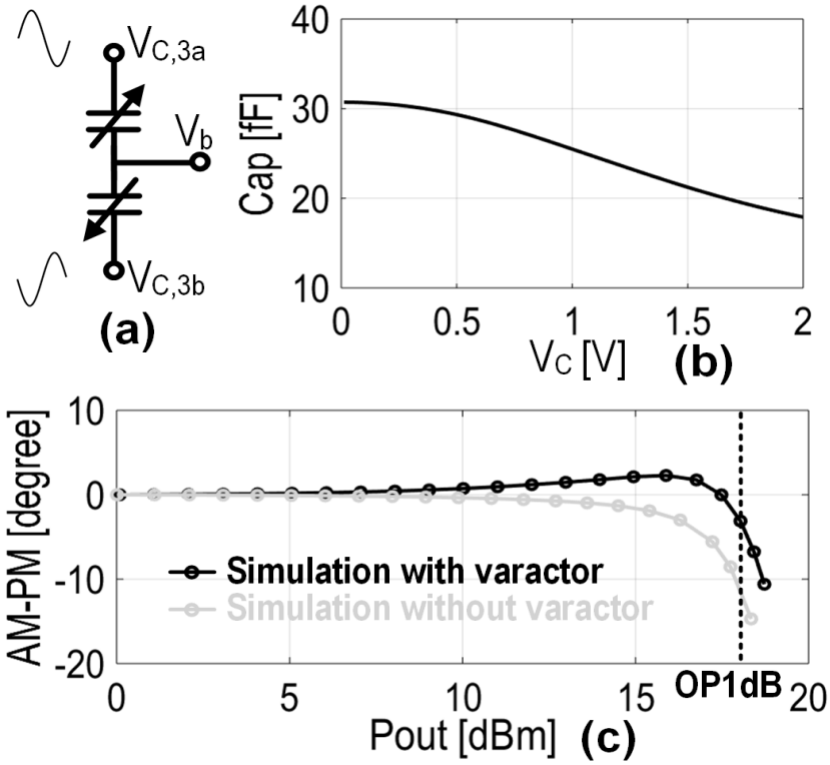

Figure 4.3: Varactors for AM-PM distortion compensation **(a)**. Equivalent capacitance vs amplitude of the differential signal at nodes $V_{C,3a\text{-}b}$ **(b)**. Simulated AM-PM distortion of the PA with and without varactors **(c)**.

of the transistors parasitics. The bottom plot in Figure 4.3c shows the simulated AM-PM distortion of the full PA. By adding the varactors, AM-PM is reduced from -12° to +/-1.5° for P_{out} below OP1dB.

4.2: Dual-path PA

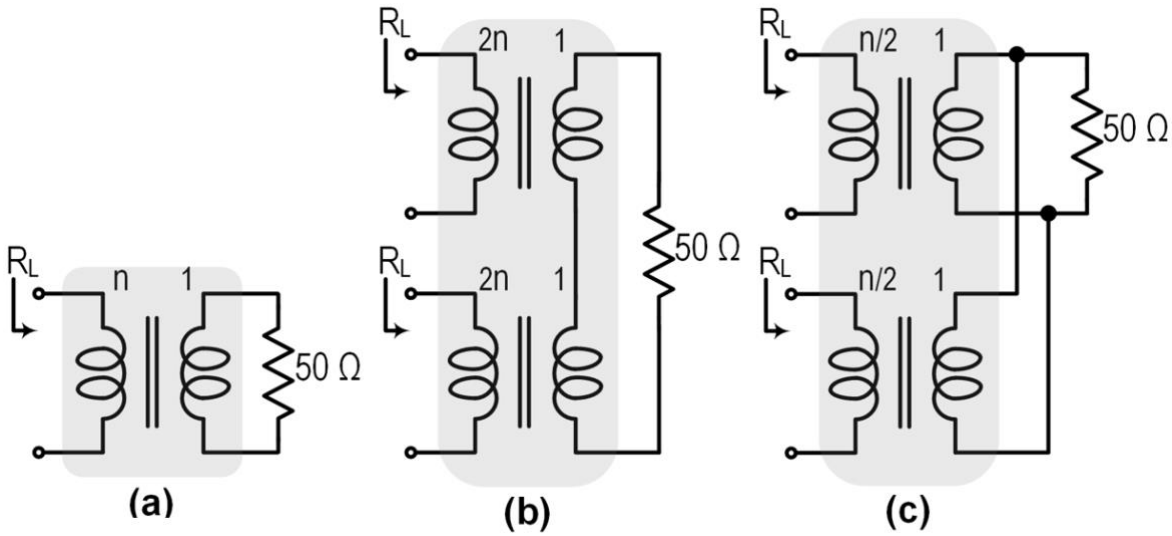

Figure 4.4: Impedance matching with a transformer **(a)**, series power combiner **(b)** and parallel power combiner **(c)**.

A second PA has been designed, comprising two amplifiers with the same active core described in previous section, but with the input and output matching networks replaced by a transformer-based power splitter and combiner, respectively.

Providing the loss of the combiner is the same as the matching network in the single-path PA, the output power can be theoretically doubled maintaining the same efficiency. But, compared to a simple matching network, transformers in a power combiner are required to provide higher impedance transformation ratio, leading to higher loss. To clarify the issue, a transformer-based matching network and two-path series and parallel power combiners are shown in Figure 4.4a and Figure 4.4b,c, respectively. The transformer in Figure 4.4a scales the antenna resistance (R_{ant}) to the optimal load resistance for the PA (R_L), with an impedance ratio $n=R_{ant}/R_L$ (corresponding to the turn ratio of an ideal transformer). In the single-path PA, $R_{ant}=50\Omega$ and $R_L=70\Omega$ achieved with 1:1 transformer. To keep the same R_L with power

combining, a different number of turns in the primary or secondary windings is required, similar to [10], [24], [28], [29], limiting the magnetic coupling, k, or the quality factor, Q, of the transformer coils. Being the transformer power loss minimized by maximizing the kQ product [27], [30], the combiners in Figure 4.4b,c would introduce a remarkably higher loss than the matching network in the single-path PA.

Figure 4.5 shows the 3D layout and the equivalent circuit of the two-path combiner designed in this work. It is composed of two 1:1 series-connected transformers co-designed with the access lines connecting the PA outputs. The two transformers (with input terminals A-A_1, B-B_1) are realized by splitting the top winding of a transformer having the same structure used in the matching network of the single-path PA, optimized for minimum loss. The impedance at terminals A-A_1, B-B_1 (31Ω//30pH) is then scaled up to the optimal load for each PA (70Ω//60pH) by properly sizing the characteristic impedance, Z_0=24Ω, and electrical length, θ=22°, of the access lines. From simulation, the difference between the admittance seen at the four input ports of the combiner is within 0.5dB. Figure 4.6 shows the simulated power loss versus frequency. At 80GHz, the combiner adds only 0.4dB loss compared to the transformer matching network in the single-path PA. As a result, the expected peak P_{out} from the dual-path PA is 2.6dB higher, with only a marginal impact on the power efficiency.

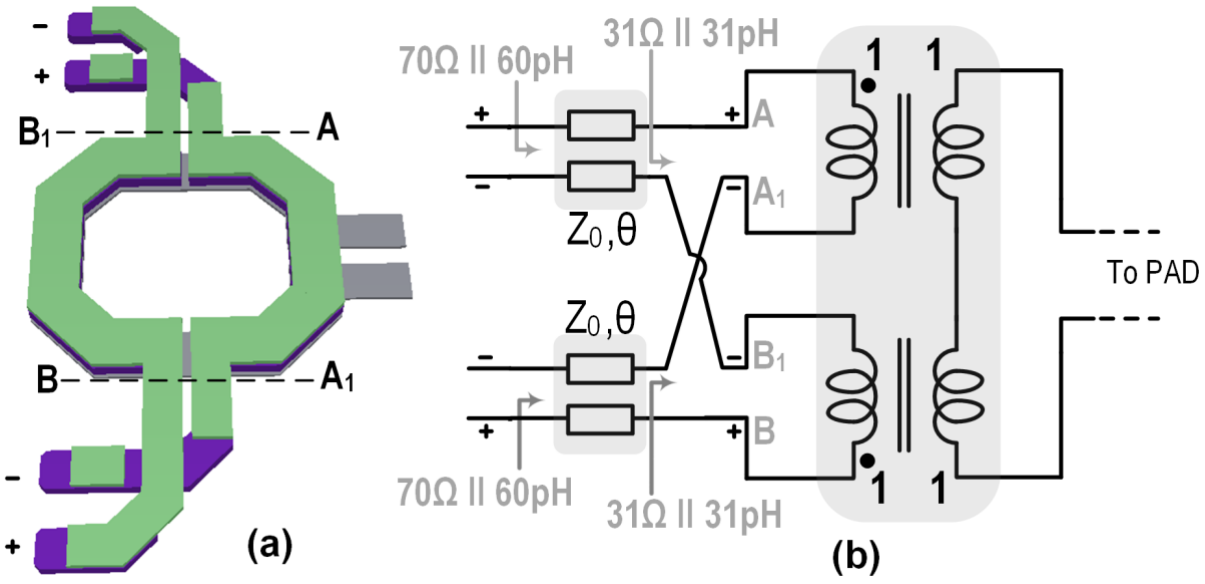

Figure 4.5: 3D layout view of the power combiner **(a)** and equivalent circuit model **(b)**.

The same combiner is used as power splitter at the input, without any modification. Input impedance matching is achieved by adding a resistive loss at input of the PAs, leading to ~1dB power gain reduction.

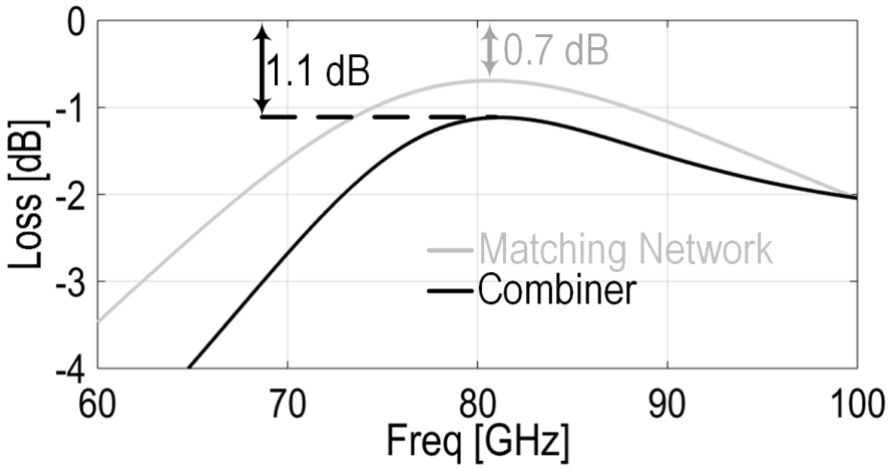

Figure 4.6: Loss of the transformer matching network in single-path PA and of the combiner in the dual-path PA.

4.3: Conclusion

In this chapter, PAs based on a CB output stage have been presented. Compared to the CE, CB topology allows higher output power and enhanced linearity with OP1dB only 1dB lower than Psat, where efficiency peaks. Moreover, the BJT can be exploited to implement current clamping, so that the DC current tracks the signal current, yielding efficiency enhancement in back-off without compromising gain and linearity. Besides, transformer based power splitter and combiner in dual-path PA are capable of impedance transformation with low insertion loss. Accordingly, dual-path PA is able to deliver 2.5dB more output power while keeping high efficiency.

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Chapter 5:

E-band Power Amplifiers measurement setup and results

The die microphotographs of the PAs are shown in Figure 5.1. The area occupation is 0.24mm^2 and 0.32mm^2 for the single and dual-path PAs, respectively. In this chapter, the measurement devices and setup will be explained and shown. Then, the measurement results of single-path PA and dual-path PA will be presented.

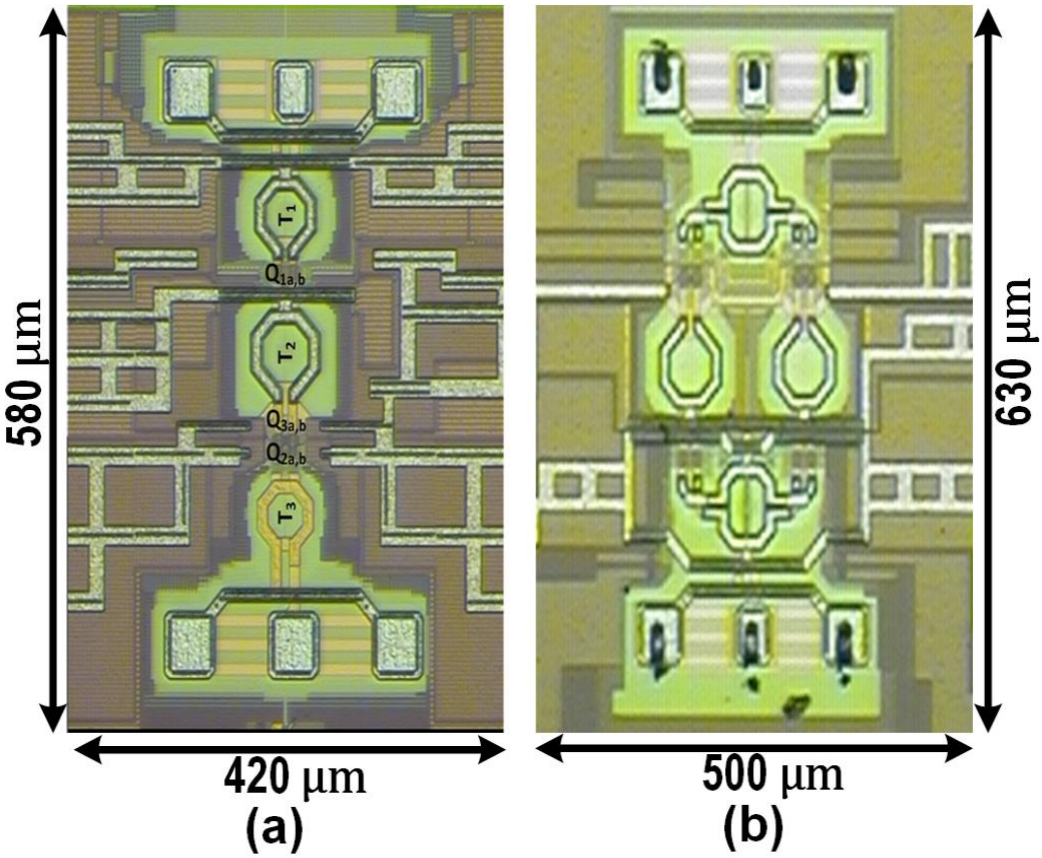

Figure 5.1: Chip microphotographs. Single-path PA **(a)** and dual-path PA **(b).**

5.1: Measurement Setup

RF board hosting the chip is shown in Figure 5.2. Supply voltage and biasing currents were provided to the chip by another dedicated board connected to the supply generators (Figure 5.2).

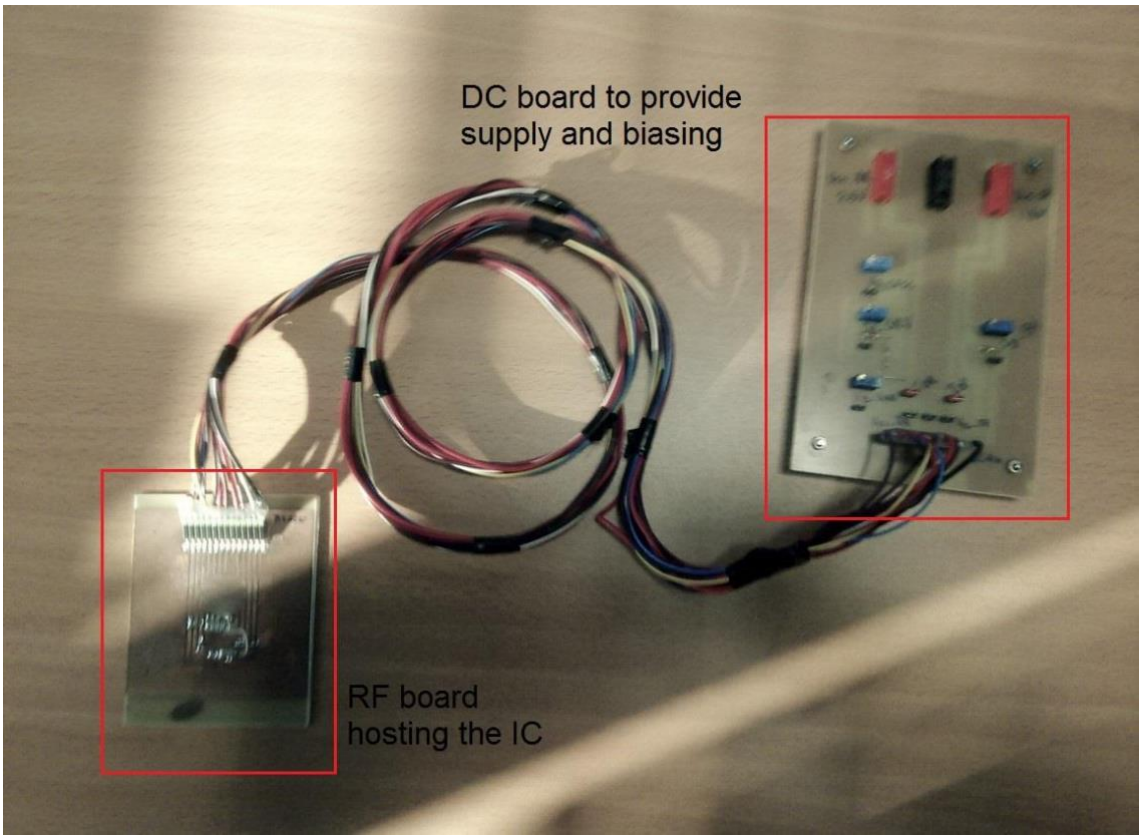

Figure 5.2: RF board hosting the chip and DC board for supply and biasing.

5.1.1: S-parameters Measurement

The small signal measurements were performed in the analog integrated circuit laboratory of the university of Pavia. The measurement required a vector network analyzer (VNA) and two extension mixers used to translate the signal generated and received by the VNA at higher frequencies, outside the nominal range of the VNA. These devices are shown in Figure 5.3. The chip was mounted on a board and then placed on a plate where the probes connected to the VNA could land on the pads.

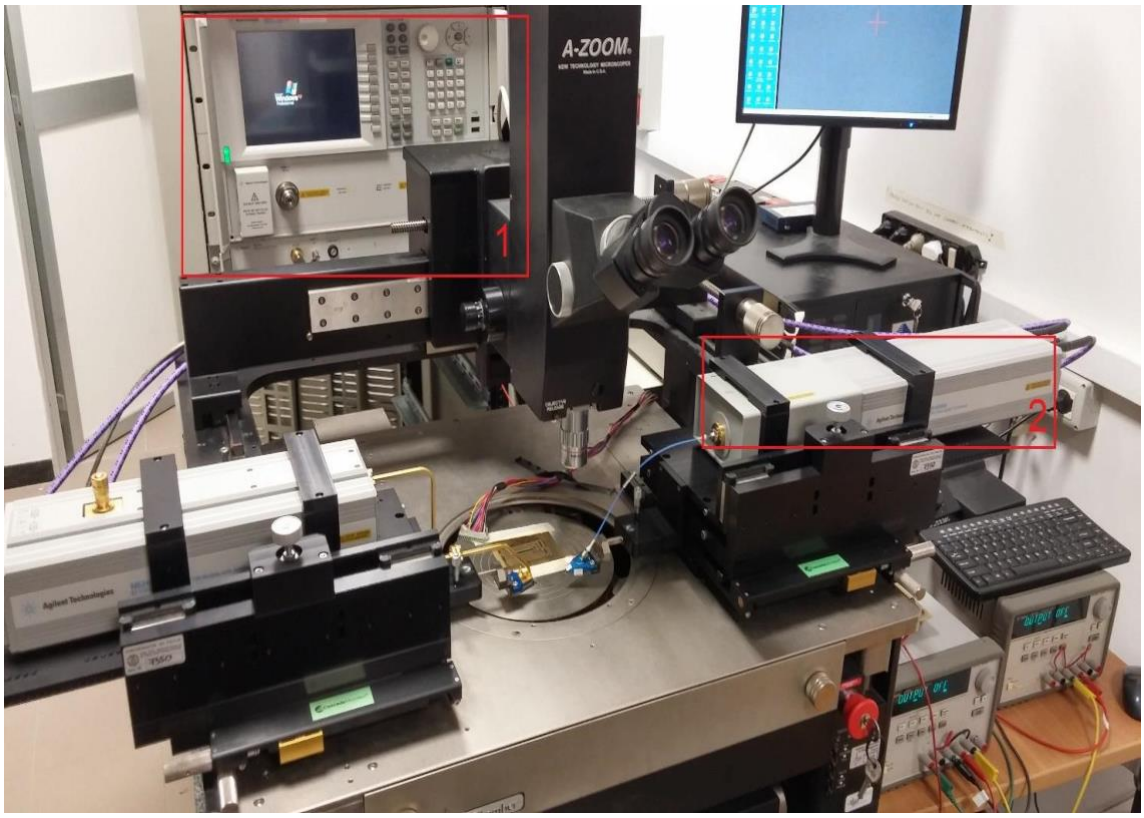

Figure 5.3: small signal measurements setup, **1**. VNA, **2**. Mixer.

The first step toward an accurate measurement is the calibration of the VNA. Basically, it is like a test where the probes are connected to short circuits, open circuits and 50 Ohm loads. Through calibration the VNA records the characteristics of all the elements (mixers, probes, cables, waveguides...) connected between the instrument ports and the DUT (device under test), so that they can be removed to obtain correct results during real measurements.

5.1.2: Large Signal Measurement

Large signal measurements were performed in Huawei laboratories in Milan with a slightly different setup. Instead of the mixers a combination of signal generator and frequency multiplier was used to produce the input signal, while the readings at the output were done with a power meter. Moreover, a programmable attenuator was necessary since the signal generator provided a fixed amplitude signal. All the components are shown in Figure 5.4.

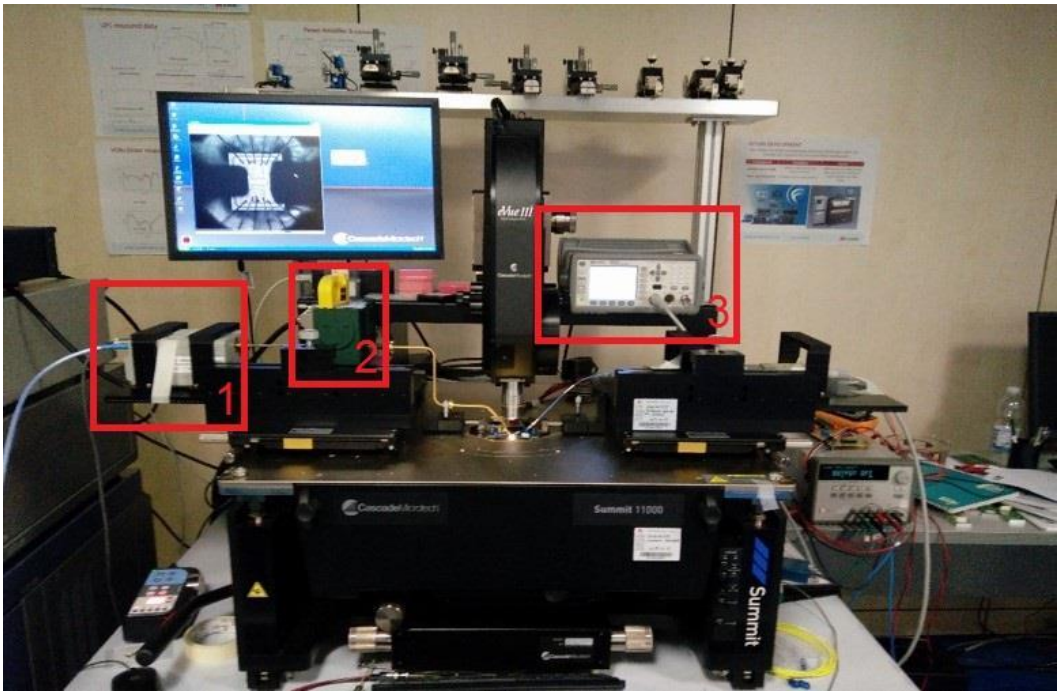

Figure 5.4: large signal measurements setup, **1**. Source, **2**. Programmable attenuator, **3**. Power meter.

5.1.3: OIP3 Measurement

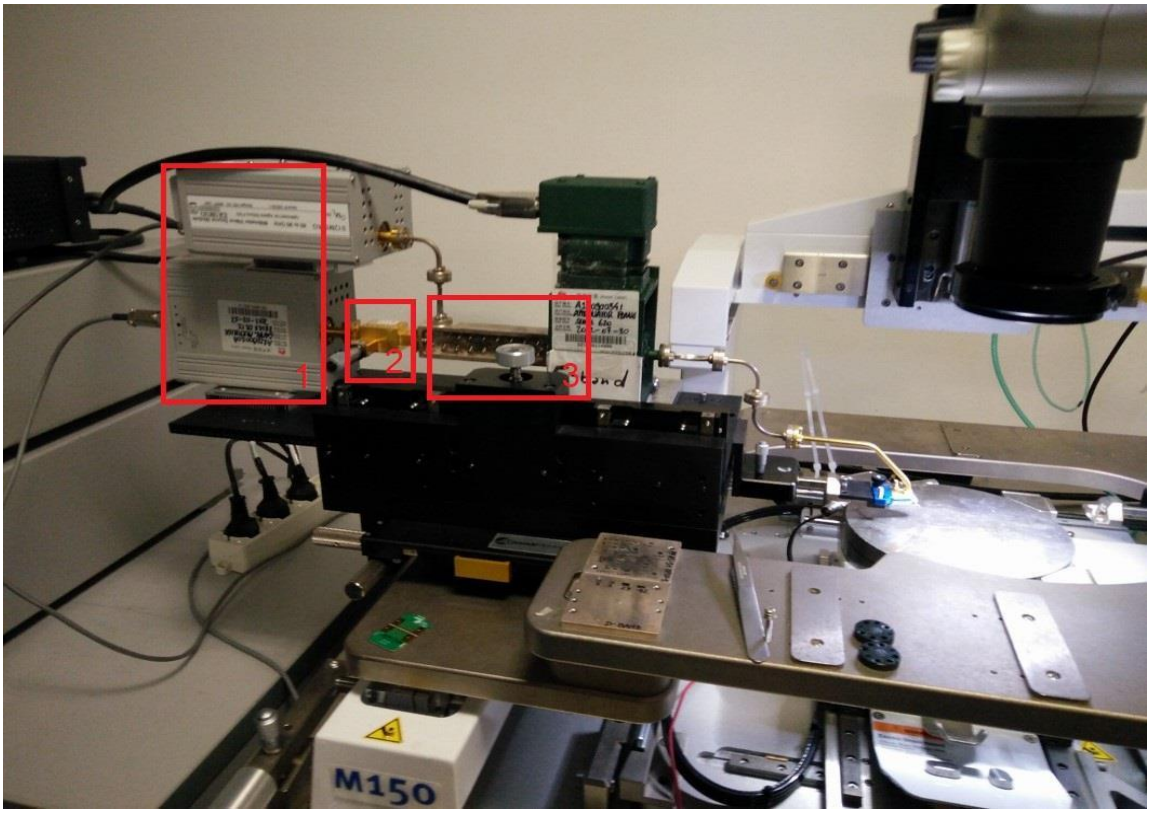

Figure 5.5: OIP3 measurements setup, **1**. Sources, **2**. Fine attenuator, **3**. Power combiner.

To perform the two-tone test on the PA, the setup has to be further modified. A second signal generator together with one more attenuator and a power combiner is needed as shown in Figure 5.5. The new attenuator is necessary to correct eventual mismatch in the amplitude of the tones that should be equal while the power combiner is used to feed them to the amplifier. For intermodulation measurements, the power meter at the output is replaced with a spectrum analyser, able to distinguish the power at the different spectral components.

5.2: Measurement Results

The measured parameters are the input and output impedance (S11, S22), the gain (S21), the reverse isolation (S12), the saturation output power, the 1dB compression point, the efficiency and the OIP3. The results are reported in the following plots. Measured S-parameters across 50-100GHz are shown in Figure 5.6 and Figure 5.7.

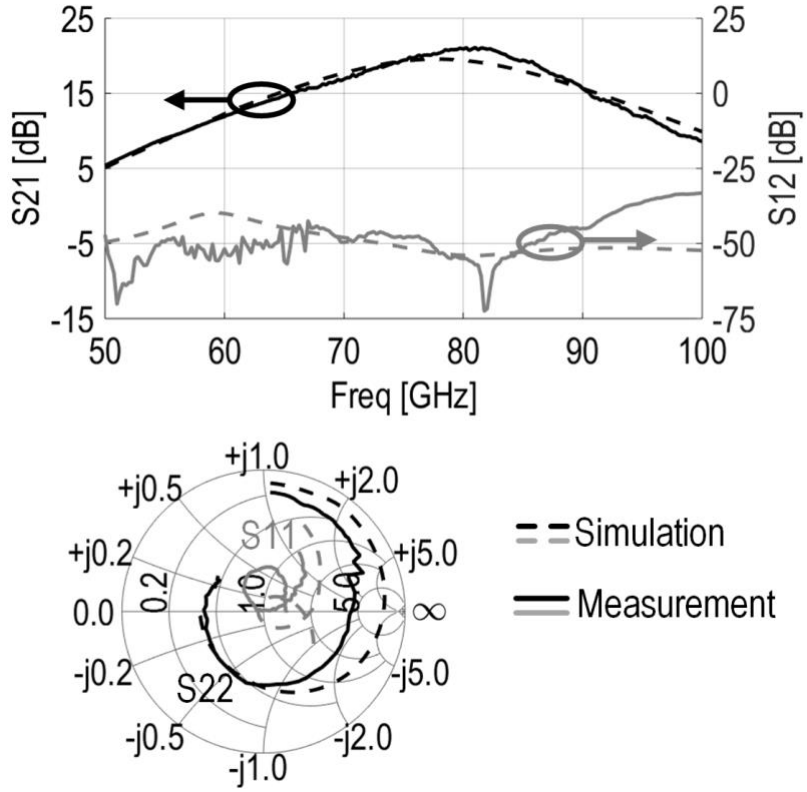

Figure 5.6: Measured and simulated S-parameters on the single-path PA.

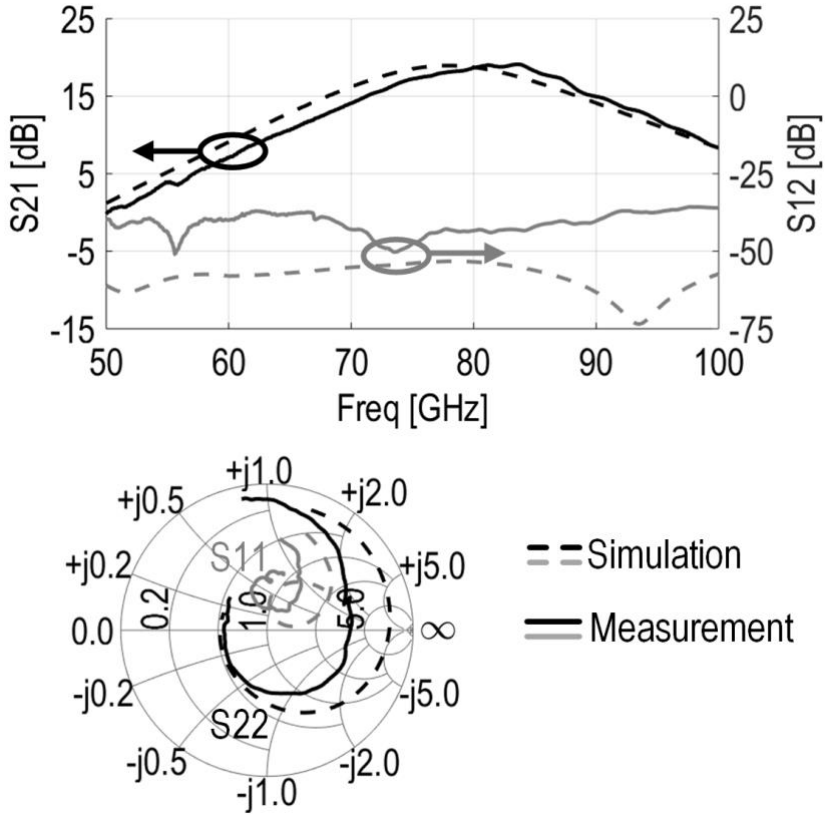

Figure 5.7: Measured and simulated S-parameters on the dual-path PA.

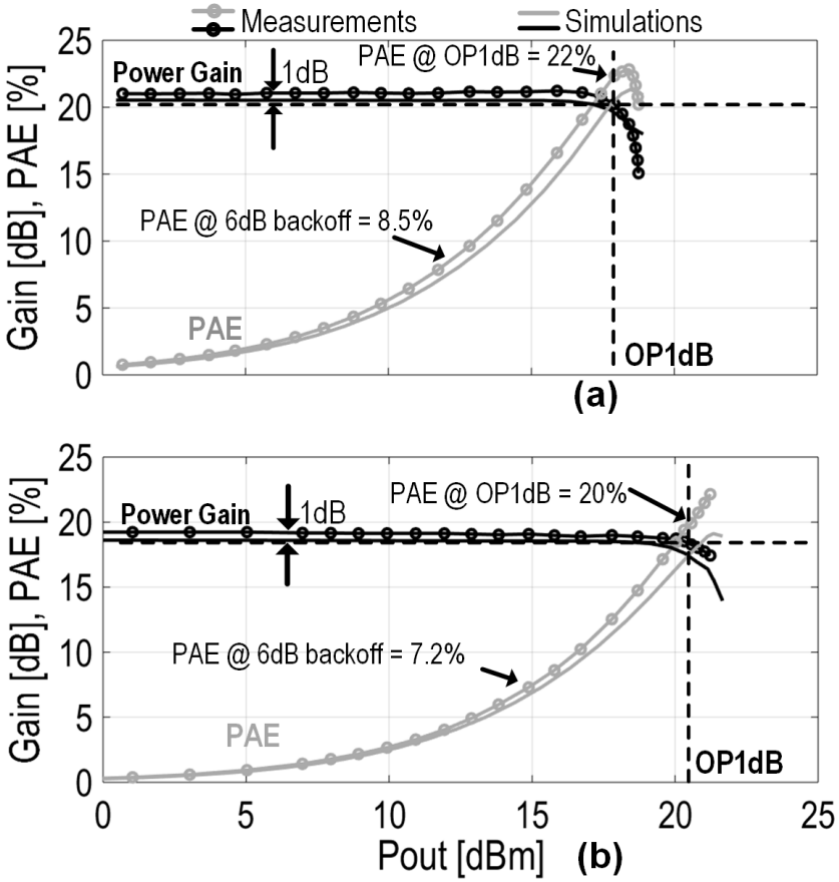

Figure 5.8: Gain and PAE vs P_{out} for the single-path PA **(a)** and dual-path PA **(b)**.

Good agreement between measurement and simulations is achieved over the full frequency range. The peak gain (S21) of the single-path PA is 21dB at 80GHz and -3dB bandwidth is from 71 to 86GHz. S21 of the dual-path PA is 19.1dB at 83GHz with -3dB bandwidth of 73-88GHz. The reverse isolation (S12) is lower than -30dB for both PAs, while the input reflection coefficient (S11), shown on Schmitt charts, is below -10dB from 60GHz to 100GHz.

The large signal measurements were carried out with a power meter and a calibrated power source. Figure 5.8 plots the measured power gain and PAE at 80GHz frequency versus output power for the two amplifiers. In the single-path PA (Figure 5.8a), Psat is 19dBm while OP1dB is 18dBm. The measured PAE peaks to 23% while at OP1dB and 6dB back-off it is 22% and 8.5%, respectively. The measured Psat and OP1dB for dual-path PA (Figure 5.8b) are 21.5dBm and 20.5dBm, 2.5dB higher than for the single-path PA, as expected from the analyses in Chapter4-B. The maximum PAE is 22% while PAE at OP1dB and 6dB back-off is 20% and 7.2%, respectively. Simulations, reported with continuous lines in Figure 5.8, are in good agreement with measurements.

Figure 5.9 shows the measured DC current of the driver and output stage for the single-path PA versus P_{out}. The DC current of the driver, biased in class-A, is almost constant, while the DC current of the output stage, leveraging current clamping, rises with P_{out} and follows the expected trend ($\propto \sqrt{P_{out}}$). From OP1dB to 6dB back-off, the output stage power dissipation is roughly halved, yielding a 2x higher efficiency

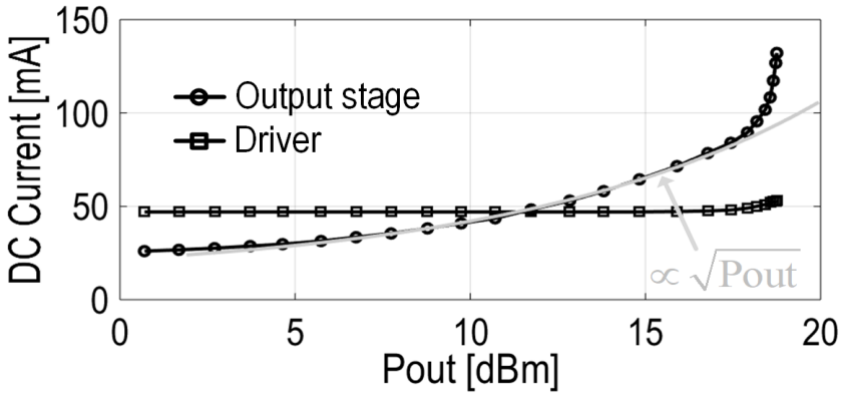

Figure 5.9: DC Currents versus P_{out} for the single-path PA.

compared to a class-A stage. Similar results have been measured on the dual-path PA.

Figure 5.10 summarizes the large signal performance of the single-path PA across frequency. Psat is 20dBm at 70GHz and reduces to 17.5dBm at 90GHz. Over the same frequency band, OP1dB ranges from 19dBm to 17dBm while PAE at Psat and 6dB back-off from OP1dB is always above 20% and 7%, respectively. With the dual-path PA, the same measurements have been limited across 75-85GHz due to the lower gain and the limited available power from the measurement setup. OP1dB ranges from 21.5dBm to 19.5dBm with PAE always above 16%.

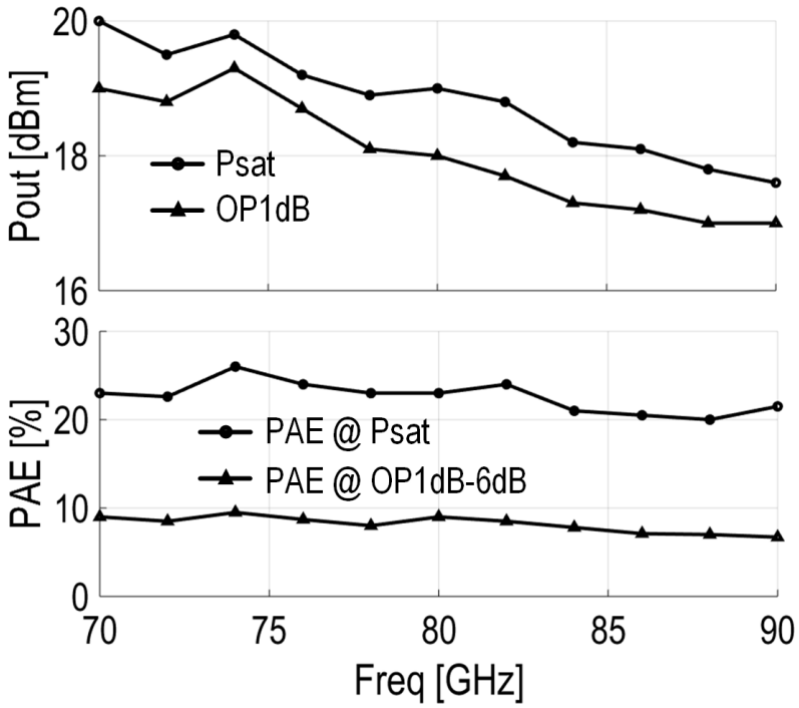

Figure 5.10: Output power and PAE of the single-path PA versus frequency.

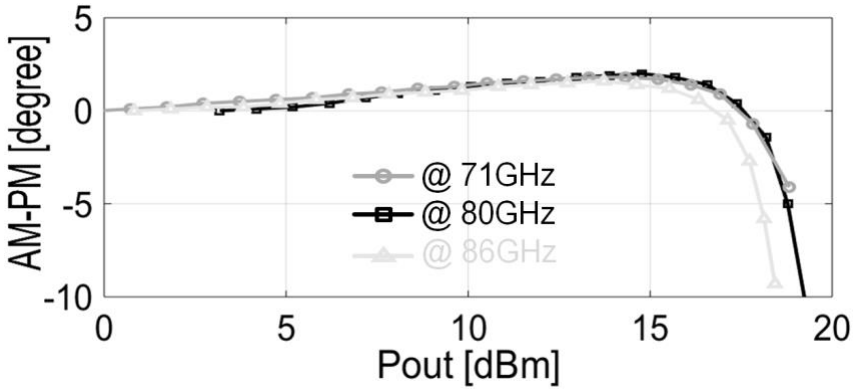

Figure 5.11: AM-PM measurements on the single-path PA.

The results of AM-PM distortion measurements on the single-path PA are reported in Figure 5.11. The phase variation with P_{out} up to OP1dB at 71GHz, 80GHz, and 86GHz are within 1.8º, 2º, and 1.6º, respectively.

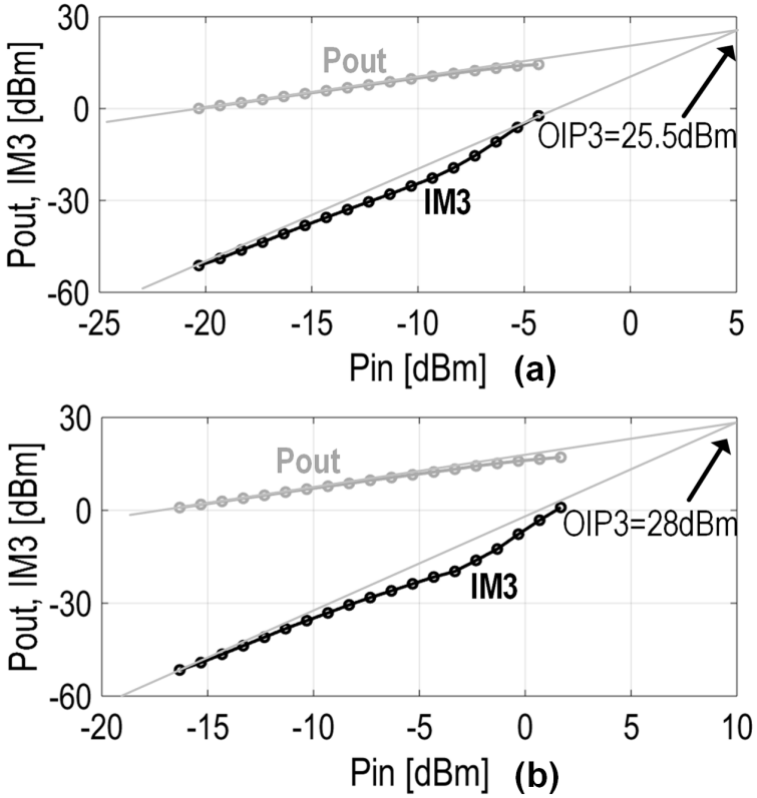

Figure 5.12: OIP3 measurements at 80GHz. Single-path PA **(a)** and dual-path-PA **(b)**.

Figure 5.12 shows the OIP3 test results on the two PA versions, performed by applying two tones at +/- 100MHz from 80GHz center frequency. The OIP3 of the single-path PA is 25.5dBm, while the OIP3 of the dual-path PAs is 28dBm. Measurements have been carried out with different tone spacings and center-frequencies and proved consistent results with OIP3 variations within 1.5dB.

Due to the lack of measurement equipment, performances with modulated signals are evaluated through simulations, with SpectreRF Envelope Analysis. The reliability of simulations is supported by the good agreement with the measurement presented so far in this section. Figure 5.13 shows the simulated constellation at the PA outputs with a 3Gbit/s 64QAM signal. The peak Pout is 18.4dBm and 21.5dBm for the single-path

PA and the dual-path PA, respectively. The average Pout is ~6.5dB lower. The Error Vector Magnitude (EVM) of the two constellations is below -28dB without any signal pre-distortion.

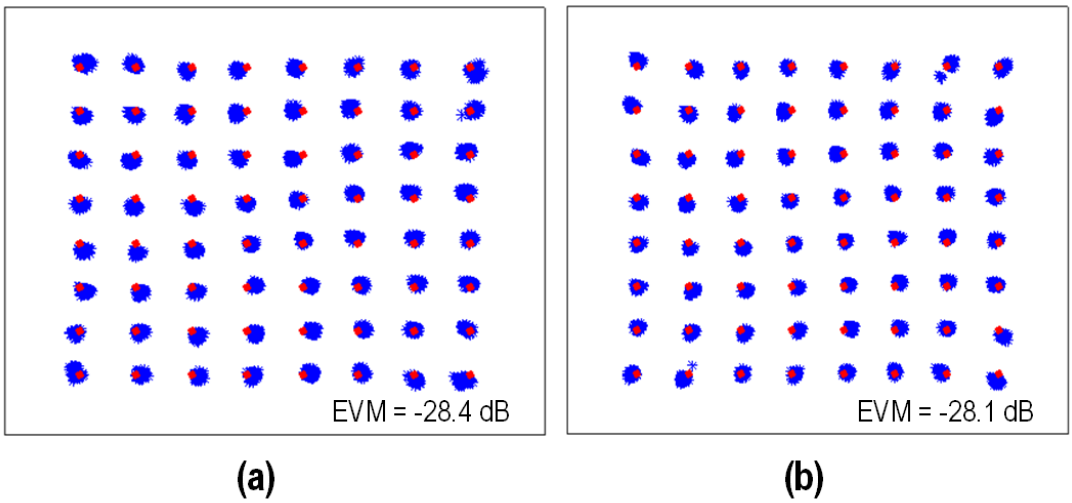

Figure 5.13: 3Gb/s 64-QAM constellations at 80GHz. Single-path PA at peak P_{out} of 18.4dBm **(a)** and dual-path PA at peak P_{out} of 21.5dBm **(b)**.

Table 5.1: Performance summary and Comparison.

Reference	This Work		[11]	[16]	[10]	[12]	[14]	[31]	[13]
Tech.	55nm SiGe		90nm SiGe	180nm SiGe	130nm SiGe	40nm CMOS	40nm CMOS	65nm CMOS	40nm CMOS
Supply (V)	1.8 / 2.3		1.8	4	2.5	1.8	0.9	1	1.5
Freq. (GHz)	80		76	83	84	73	80	79	72
Gain (dB)	21	18.5	21.2	25	27	25.3	18.1	24.2	18.7*
BW (GHz)	15	15	14	9.6	8.6	7.6	15.2	10	21
Psat (dBm)	19	21.5	24	14.7	18	22.6	20.9	19.3	21
OP1dB (dBm)	18	20.5	21.3	12.5	16	18.9	17.8	16.4	19.2
PAE,max (%)	23	22	11.6	8.1	9	19.3	22.3	19.2	13.6
PAE @ OP1dB (%)	22	20	6.2*	5.7*	7.5*	10.7	12	10*	12.4
PAE @ 6dB back-off (%)	8.5	7.2	2.5*	1.5*	2.5*	3.3*	3.3*	2.5*	5.7
Area (mm^2)	0.24	0.32	3.52	0.34	0.68	0.25	0.19	0.855	0.19
Topology	2-stage, cascode & CB	2-way combining 2-stage, cascode & CB	8-way combining 3-stage, CE	2-way combing 2-stage, cascode	4-way combining 3-stage, CB	4-way combining 2-stage, NBCA	4-way combining 2-stage, CS	8-way combining 4-stage, CS	Doherty (cascode)

*: estimated from measurement plots

Finally, experimental results are summarized in Table 5.1 and compared with E-band silicon PAs in the recent literature. The single-path PA reaches 18dBm OP1dB without power combining, while other PAs, except [13], make use of power combining to deliver comparable or lower OP1dB. The two PAs proposed in this work demonstrated a PAE at OP1dB and 6dB power back-off which is nearly 2x or more higher than PAE of other silicon PAs (a notable exception is [13], that keeps reasonably good efficiency in back-off by resorting to a Doherty architecture, but at the cost of

design complexity and limited PAE at OP1dB). This was made possible by the high linearity of the common-base output stage and by exploiting current clamping as a technique to scale the supply current with output power.

5.3: Conclusion

Following the previous chapters, PAs based on a CB output stage have been realized and measured. Thanks to the current clamping exploited in CB, measured DC current of the output stage in PA tracks the square root of output power, yielding higher efficiency in back-off. Two different test chips, realized in SiGe BiCMOS, demonstrated OP1dB of 18dBm and 20.5dBm at 80GHz, with an improvement of PAE compared to previously reported silicon PAs operating at the same frequency.

Chapter 6:

E-band Transmitter Design and Measurements

The E-band transmitter has been designed in the STMicroelectronics 55nm SiGe-BiCMOS technology [26]. The dual-path PA described in previous chapters has been employed in this transmitter to deliver high linear and efficient output power. First, the design of transmitter will be explained. Then, the measurement results of the realized chip will be presented in the following.

6.1: Transmitter Design

The schematic of the direct-conversion E-band transmitter including quadrature LO generation and signal path is shown in Figure 6.1. Focusing on signal path, it includes high-linearity up-conversion mixers with DC-coupling and emitter-degeneration technique which drives dual-path PAs.

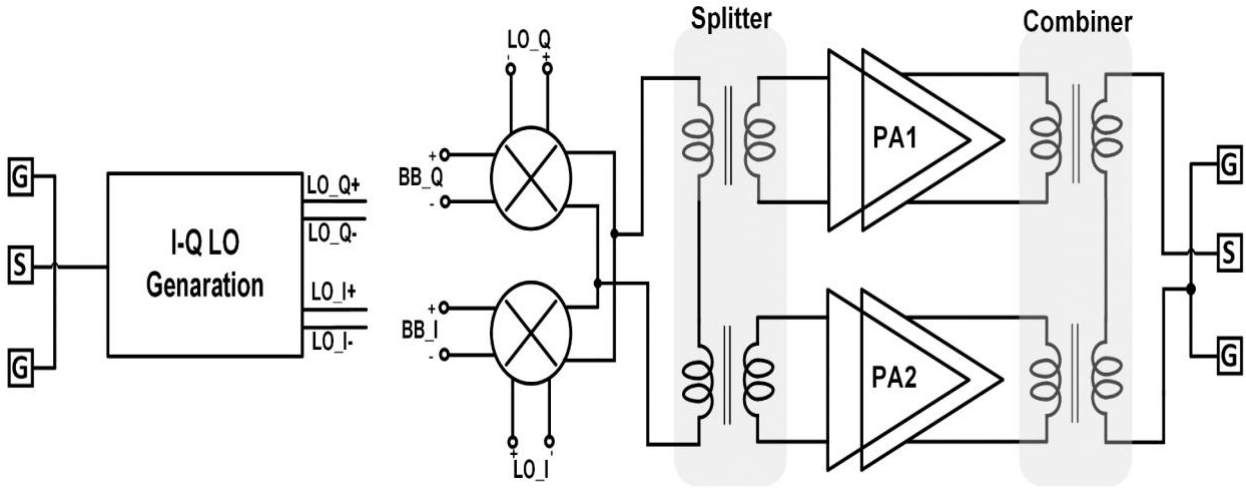

Figure 6.1: Schematic of the full E-band transmitter.

The configuration of dual-path PA is the same as the one already presented in previous chapters. Therefore, only the configuration of up-conversion mixers will be described in the following. Figure 6.2 shows the schematic of the employed mixers which is basically differential gilbert cell. The load is the splitter connecting to two succeeding PAs, estimated with EMX electromagnetic.

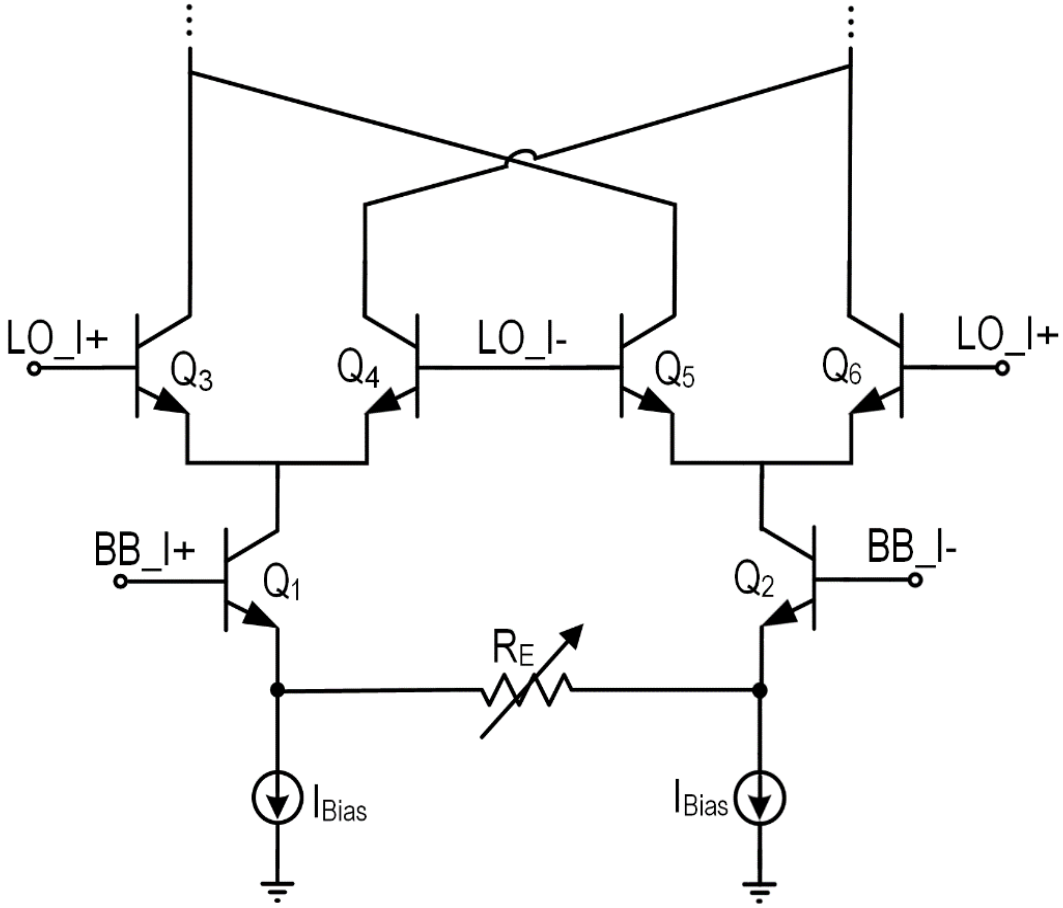

Figure 6.2: Schematic of the up-conversion mixers.

The base-band inputs (BB_I+ and BB_I-) are DC-coupled provided by digital to analog converter (DAC) for calibration and the IF bandwidth is up to 1GHz. The bias currents and the size of the transistors in the trans-conductance stage and switching stage ($Q_{1\text{-}6}$) are considered in a way to preserve high f_t defining as frequency of unity current gain. The supply voltage is 2.3V which connects directly to the same supply voltage of drivers in the dual-path PA. The quiescent current is set to 2x7mA, yielding sufficiently high linear trans-conductance not to limit the mixer OP1dB and OIP3, and accordingly the overall performance of transmitter.

To control gain in PVT variations, tunable emitter degeneration resistor is employed as depicted in Figure 6.2.

From the systematic point of view, the target specifications for the mixer is to achieve OP1dB and gain of higher than 4dBm and 5dB, respectively. The layout of quadrature mixers is shown in Figure 6.3. It has been tried to be symmetric for minimizing the LO leakage and also even-order harmonics coming from device mismatches.

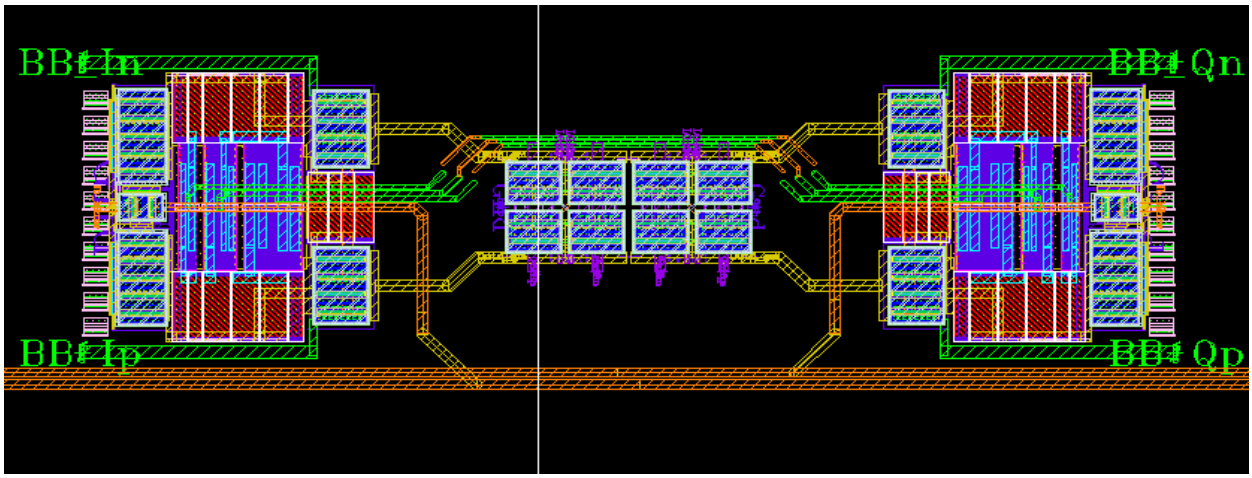

Figure 6.3: Layout of the up-conversion mixers.

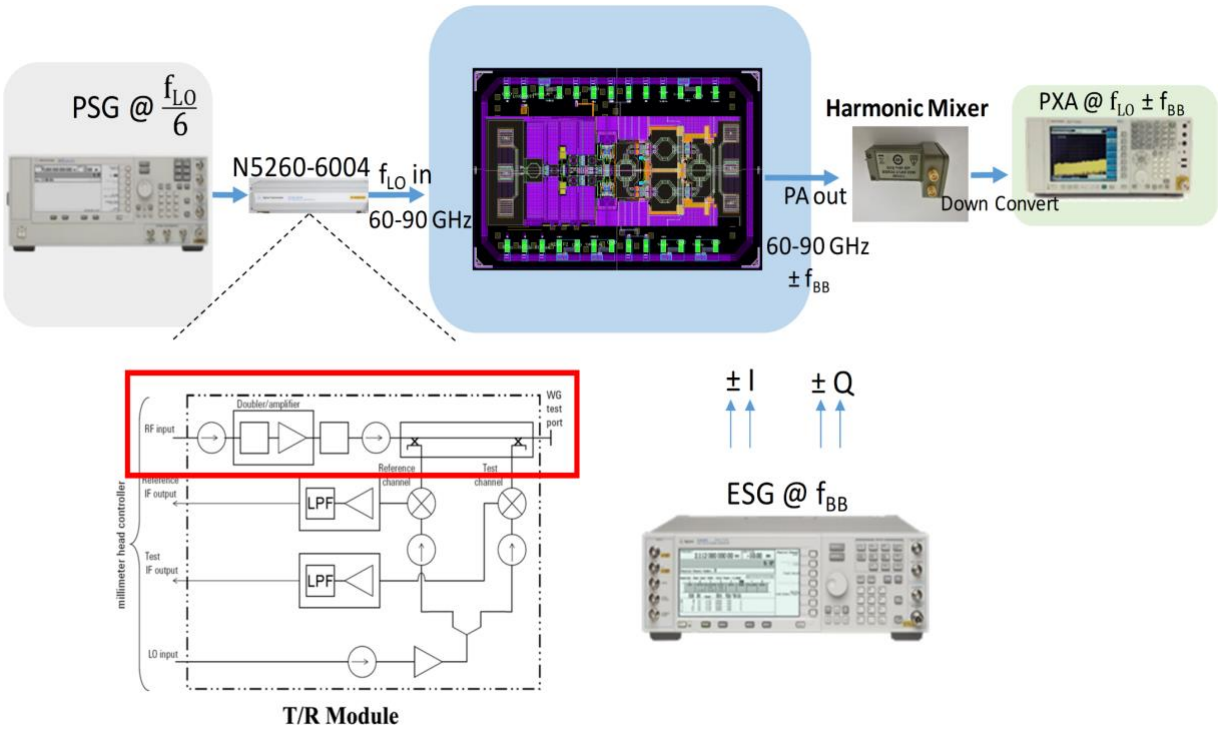

Figure 6.4: Measurement setup of the E-band transmitter.

6.2: Measurement Setup

The whole setup including devices to characterize the fabricated chip is shown in Figure 6.4. The required input LO to be applied to the chip is at the frequency around 80GHz which is provided by the combination of PSG delivering LO at the frequency of $f_{LO}/6$ and the following up-conversion harmonic mixer which gives the sixth harmonic of its input. The output of transmitter which is at the center frequency of 80GHz is connected to another harmonic mixer to down convert and then the spectrum will be shown on PXA. The differential quadrature base-band inputs are provided with ESG device.

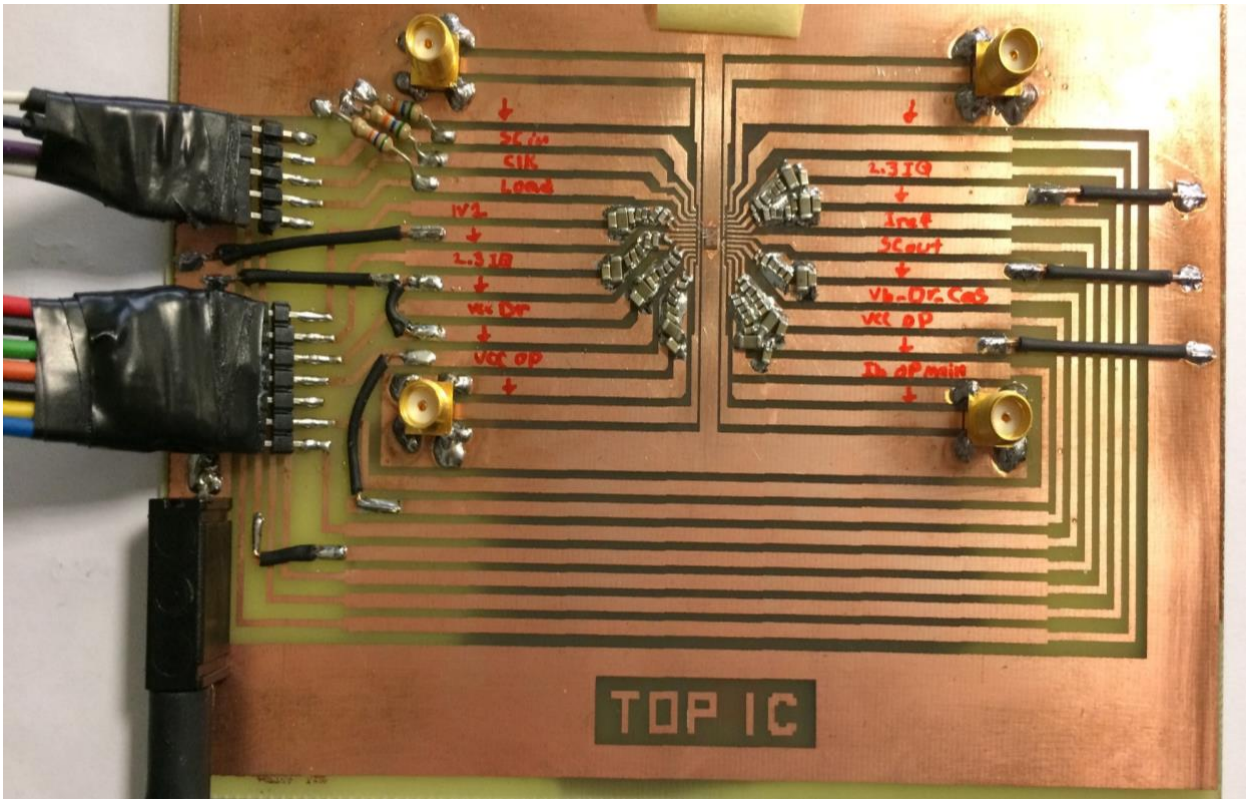

Figure 6.5: RF board hosting the transmitter chip.

The RF board hosting the chip is shown in Figure 6.5. The quadrature base-band signals will connect through SMA connectors as shown in Figure 6.5. Supply voltage and biasing currents were provided to the chip by another dedicated board connected to the supply generators. Figure 6.6 shows the chip under probes in probe-station setup.

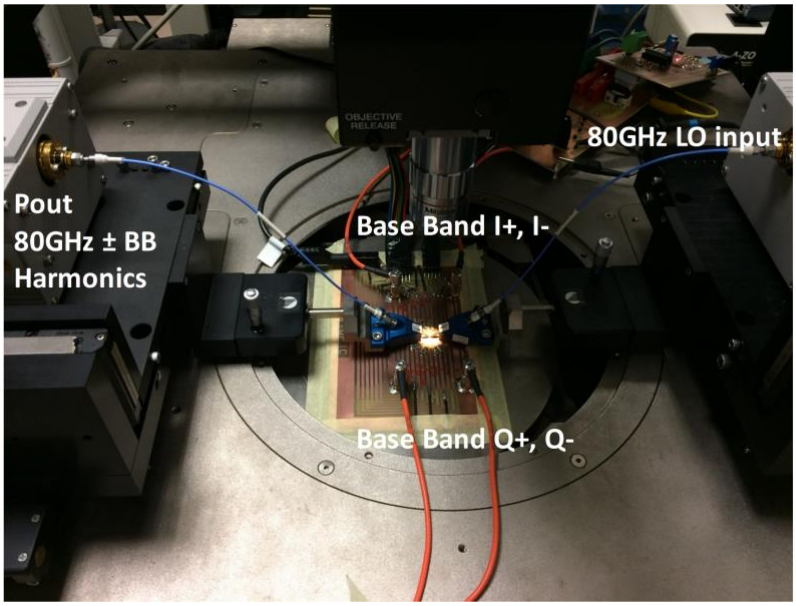

Figure 6.6: RF board hosting the transmitter chip.

6.3: Measurement Results

The die microphotograph of the realized transmitter is shown in Figure 6.7. The area occupation is 4.8mm^2. The measured parameters are the gain, the saturation output power, the 1dB compression point and the image rejection ratio (IRR). The results are reported in the following plots.

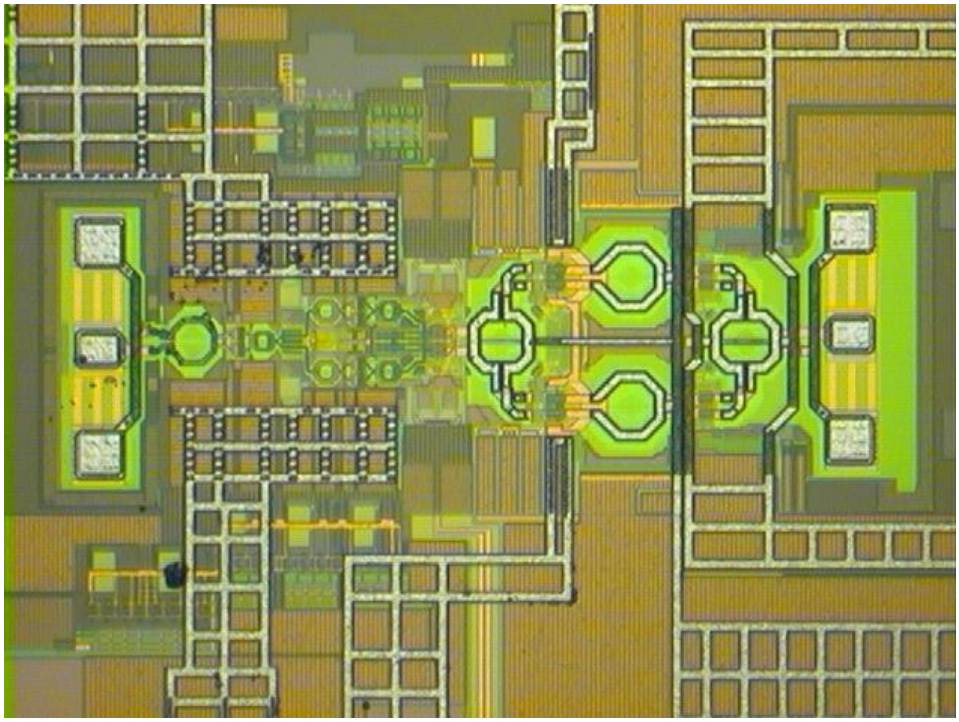

Figure 6.7: Chip microphotograph.

Figure 6.8 shows large signal measurement at 80GHz. The measured maximum gain is 21.3dB. This realized transmitter achieves Psat of 22dBm with OP1dB of 20.3dBm, the same as the dual-path PA results.

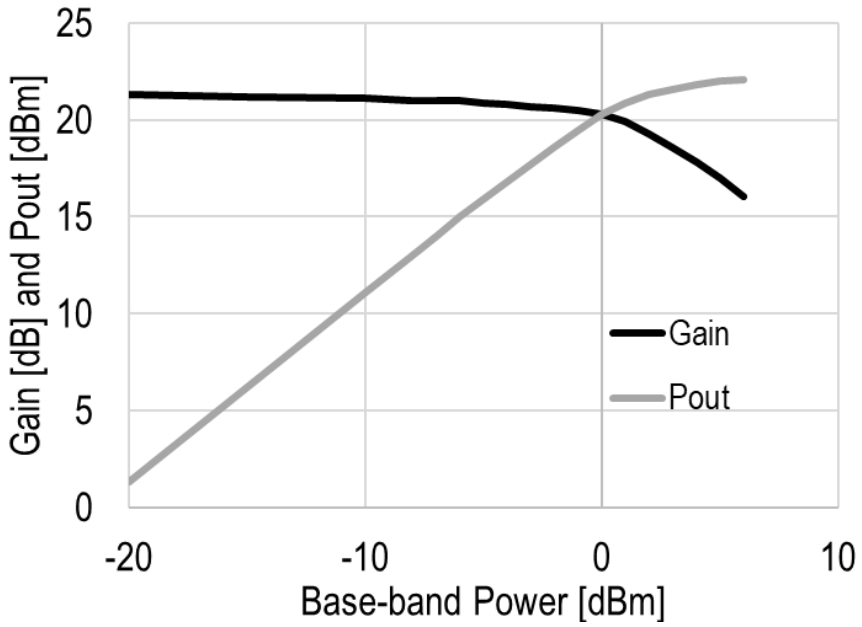

Figure 6.8: Measured Gain and output power versus base-band power at 80GHz.

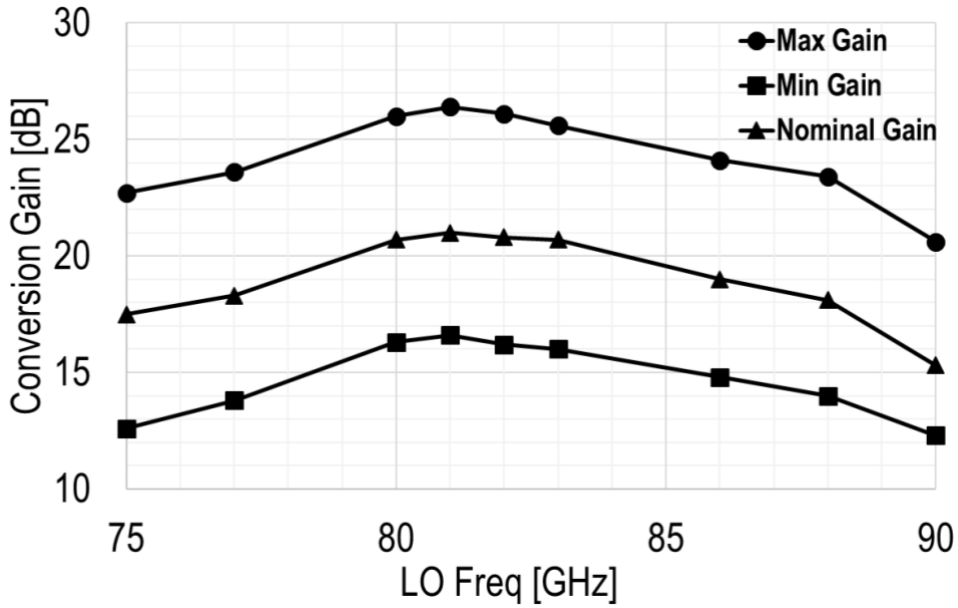

Figure 6.9: Measured tunable conversion gain of transmitter versus LO frequency.

Figure 6.9 shows the tunable conversion gain of the chain by sweeping the emitter-degeneration resistor. From this plot, it can be observed that this TX can have a 10dB variation in gain. Figure 6.10 presents the output power of the transmitter across frequency. Psat is 22dBm at 80GHz and reduces to around 19dBm at 76GHz and

88GHz while OP1dB ranges from 20.3dBm to 17.4dBm. As shown in Figure 6.11, PAE at Psat, OP1dB, and 6dB back-off from OP1dB is always above 9%, 7%, and 2%, respectively.

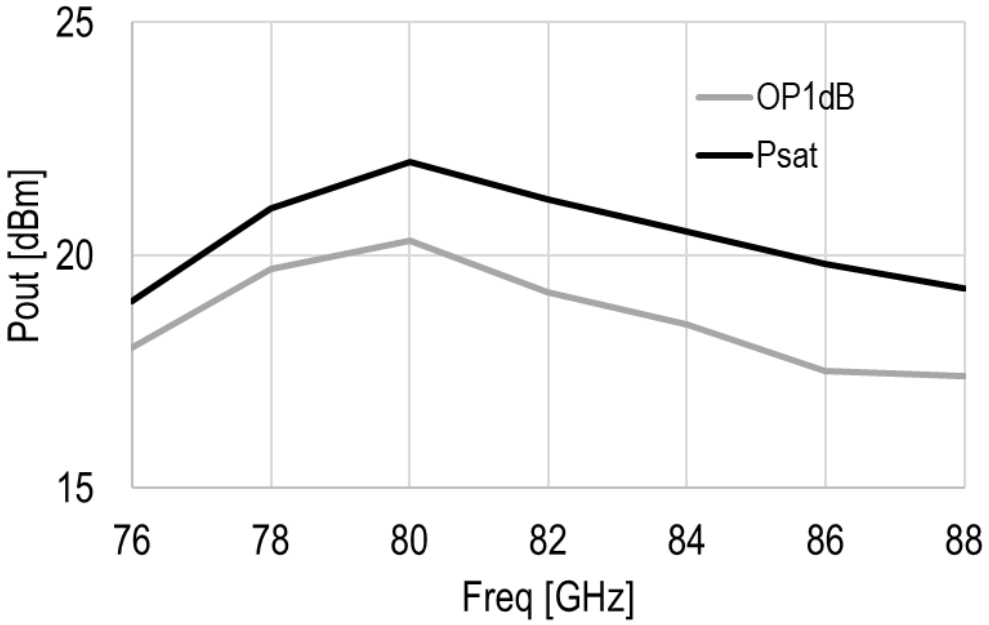

Figure 6.10: Output power of the transmitter versus frequency.

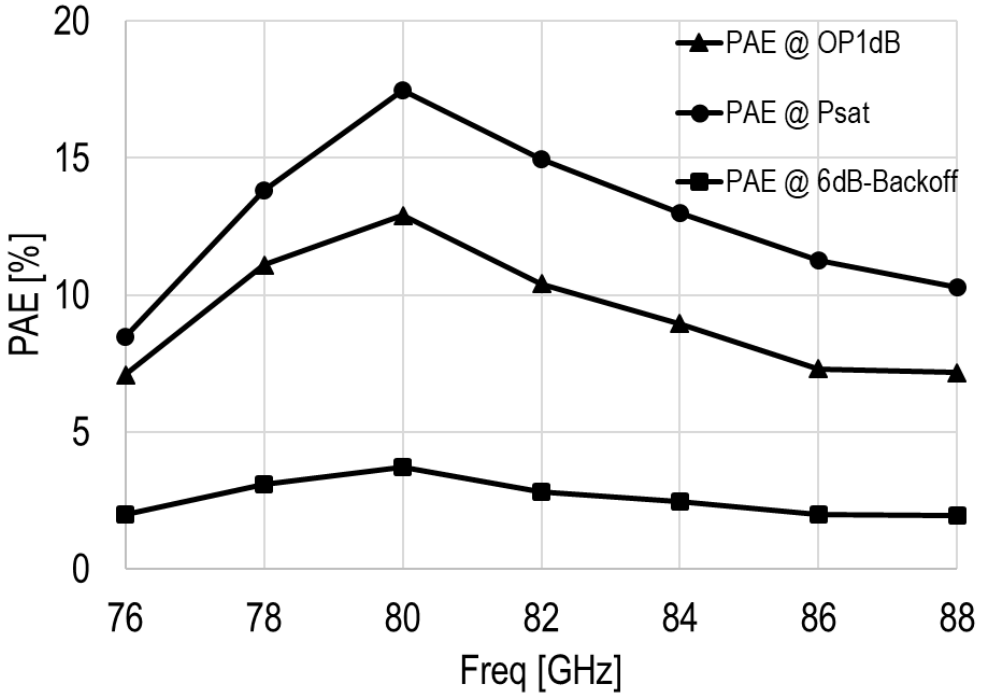

Figure 6.11: Efficiency of the transmitter versus frequency.

Finally, experimental results are summarized in Table 6.1 and compared with E-band silicon Transmitters in the recent literature. Measured TX performances compare favourably against Infineon product and research works in terms of bandwidth, IRR and delivered output power. The achieved OP1dB of 20.3dBm is likely the largest reported to date for silicon transmitters at E-band.

Table 6.1: Performance summary and Comparison.

Reference	This Work	Infineon	[32]	[33]	[34]	[35]	[36]
Tech.	55nm SiGe	SiGe	90nm SiGe	55nm SiGe	130nm SiGe	40nm CMOS	65nm CMOS
Freq. (GHz)	80	81/83/86	71-86	71-76/81-86	71-76/81-86	71-76/81-86	64-84
Gain (dB)	21.3	18.9/20.9/24	22.8	24/22	38	11	0
Psat (dBm)	22	8.3/9.2/10.8	7.4-10	18.8-20@71-76 18-18.8@81-86	18	20.9	11 @60GHz
OP1dB (dBm)	20.3	3.9/4.9/6.9	N.A.	14-15.2@71-76 8.5-13.3@81-86	16	8.8	8.3 @60GHz
IRR (dBc)	40	30	>26	N.A.	25	>30	40
Power Consumption (mW)	907 @ Psat	102	330	575	1350	1800	114
Architecture	Direct Conversion	Direct Conversion	Sliding-IF Weaver	Super-heterodyne	Super-heterodyne Sliding IF	Direct Conversion	Sub-Harmonic

6.4: Conclusion

For mobile network backhauling, direct conversion E-band transmitter focusing on signal path including up-conversion mixers and PAs has been designed and realized in 55nm SiGe-BiCMOS technology. The dual-path PA chip explained in previous chapters has been exploited in transmitter chip to deliver high linear power. In order to apply 80GHz signal to the E-band PAs, linear dc-coupled up-conversion mixers have been designed to convert low frequency signal (below 1GHz) to 80GHz. Optimizations are performed from architecture level down to transistor level to minimize the power consumption while delivering high linear output power. Measured OP1dB for the realized E-band transmitter is 20.3dBm which is likely the largest OP1dB in the literature. This chip achieves maximum output power of 22dBm. The image rejection ratio of transmitter without baseband calibration is 40dBc (above 50dBc with baseband calibration) while the bandwidth is in the range of 66-88GHz.

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