Design Techniques for High-Speed ADCs in Nanoscale CMOS Technologies

Ph.D. Thesis by
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To
my mother
&
my father

Acknowledgements

First of all, I would like to thank my advisor Prof. Edoardo Bonizzoni for all the guidance he has provided and for all the support and the opportunities he has given me during my Ph.D. studies and before. I am very grateful to him.

I am grateful to Prof. Franco Maloberti for his technical guidance and for giving me the opportunity to write my Master's Thesis under his supervision. That opportunity eventually opened the way for this Ph.D. position. I am very glad that I have known him and I have been able to work with him.

I would like to thank my co-advisor from industry, Matteo Signini, and to all the others from the ADG-ADD Castelletto R&D Group at STMictoelectronics; Claudio Bona, Simone Bianchi, Antonella Canobbio, Mario Nicotera and Gianluigi Boarin for all their help and guidance during the project that I have done with them. It would not be possible to finalize it in a really short time if there was not their huge effort.

I had the pleasure to work with the then PhD fellow Dante Muratore and it resulted in a valuable publication. I would like to thank him for being such a good colleague.

I would like to thank all the good friends from the IMS Lab at University of Pavia, whom I have known through the years. To name some of them, Arun, Nicola, Yilkal, Waqar, Elisabetta, Flavio and also Prof. Alessandro Cabrini. It was always a pleasure to have them nearby for a little chit-chat and a cup of coffee. I also would like to thank Prof. Malcovati for always being available for helping.

I would like to thank Farshad and İbrahim for their very precious friendship. They were fellows from the Istanbul Technical University, then they have become fellows in PhD. I am very glad that I had the occasion to get to know them better during these last few years in Pavia.

I would like to thank my family, especially to my father İzzet, my mother Kadriye and my sister Merve, also my friends from Turkey whom I consider as a part of my family; for their endless love and support during long years of study away from them and making me feel their warmth each and every time.

Last but not least, I feel very fortunate to have you, Valentina, beside me during all these years. It would not be the same without you. Thank you.

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Chapter 1
Introduction

Last few decades have seen a digital revolution in the electronics thanks to the rapidly advancing semiconductor technology. As predicted by G. Moore in his famous article [1], the level of integration has dramatically increased at a large pace. With this aggressive semiconductor technology scaling, the size and the cost of integrated functionality have been reduced significantly, especially for digital computing. However, the nature is analog and to utilize the tremendous digital computational power offered by the modern semiconductor technology, there should be a "bridge" or a "doorway" [2]. Thus, analog-to-digital converters (ADCs) represent one of the crucial circuit blocks of the modern technology and play a key role in bridging the analog to the digital for a wide range of applications with frequencies from DC to the few tens of GHz.

Broadband communication systems have been transformed significantly by the available digital signal processing (DSP) capabilities and introduction of the digital modulation schemes. The rate of the received and transmitted data has substantially increased in the recent years for both for wireless and wireline communication. For modern transceivers, the trend is shifting the analog functionality such as filtering, frequency translation and gain into the digital domain to increase the system flexibility and the precision, to reduce the overall size and the cost by eliminating several off-chip components. The amount of the transferred analog functionality depends on the position of the ADC on the receiver chain. The ultimate goal is realizing software-defined systems [2, 3], where the ADC is connected directly to the antenna or to the transducer and executing all the required operations into the digital domain. Such a software-defined receiver is depicted in Fig. 1.1.

1.1 Motivation

The trend of transferring analog functionality into the digital domain is getting combined with the ever increasing data rates in modern broadband communication systems. The ADCs used in those systems should have higher bandwidth and higher

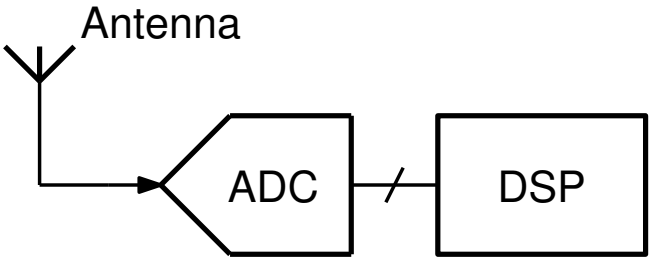

Fig. 1.1 A software-defined radio receiver.

dynamic range. Adding up to the digital functionality significantly increases the area occupied by the digital section in modern communication system-on-chips (SoCs). Therefore, the priority is given to reducing the area and the power consumption of the digital part when a technology node is chosen [4]. The scaled CMOS technologies are preferred in SoCs for higher power efficiency, smaller area and higher speed for the digital section [4]. However, these technologies create several problems to the analog circuit design such as reduced supply voltage and output impedance of the transistors [5].

Considering the above discussed arguments, *the motivation of this thesis is developing circuit techniques to improve power efficiency, bandwidth and dynamic-range for high-speed ADCs implemented in scaled CMOS technologies, as they are getting more and more demanded by the modern communication systems.* In this thesis three regions of the modern communication system application space are covered:

1. Medium resolution and high-speed single-channel successive-approximation-register (SAR) ADCs, since they are dominating the very high-speed medium resolution time-interleaved ADCs [6]. The area and power efficiency of the SAR ADCs make them appealing as a channel in the massively interleaved ADCs used in wireline and optical communication receivers [3].
2. High-resolution SAR ADC based time-interleaved ADCs with sampling frequency higher than 1 GHz as they are good candidates for replacing the power hungry pipeline ADCs in power efficient direct radio frequency (RF) sampling applications [8]. These ADCs are commonly used in cellular communication receivers for the standards such as the 4G Long Term Evolution (LTE) and the upcoming 5G in which the whole RF band is converted and no down-conversion is used.
3. High-resolution and wide bandwidth continuous-time (CT) sigma-delta modulator ($\Sigma\Delta$M) ADCs as they are appealing solutions for the wideband wireless radio receiver applications. The implicit anti-aliasing filter and signal filtering capabilities of the power-efficient CT $\Sigma\Delta$M ADCs have made these ADCs widespread in the cellular handset applications [9] as well as the car radio receivers [4, 10]. In these applications the common characteristic is converting the whole band and performing the channel filtering in the digital domain. This

allows to removing the external filtering components and reducing the system size [3]. Moreover, there are efforts to replace pipeline ADCs with few hundred MHz bandwidth used in base transceiver stations (BTS) [13].

1.2 Thesis Organization

The thesis is organized as follows:

Chapter 2 starts with a brief introduction to the application space of high-speed single-channel SAR ADCs. The conventional SAR ADC and its limitations on the speed are discussed and existing solutions found in the open literature are presented. Multi-bit per cycle (multi-bit/cycle) technique can significantly boost the conversion speed of the conventional SAR ADC. However, the reference generation is the issue in this technique. A novel preamplifier structure for multi-bit/cycle SAR ADCs is presented. The preamplifier combines the reference generation and the voltage gain. The advantages and limitations of the proposed preamplifier are discussed in detail. The preamplifier concept is applied to an 8-bit 700 MS/s subranging multi-bit/cycle flash-SAR ADC in 65nm CMOS technology. The design details and the measurement results of the fabricated chip are presented and the conclusions on the chapter are drawn.

Chapter 3 presents a background timing skew calibration technique for flash-assisted time-interleaved (FATI) SAR ADCs with multiple flash ADCs. Examples from the prior art in timing skew calibration techniques and the specific timing skew calibration methods dedicated to the FATI SAR ADCs are given. The proposed two-step timing skew calibration method is discussed in detail along with the considerations on the implementation, the hardware requirements and the limitations. The benefits of the proposed method on the channel randomization are also presented. Following the behavioral simulation results the conclusions on the chapter are drawn

Chapter 4 presents a CT $\Sigma\Delta$M ADC for multi-standard car radio applications. The Section 4.1 briefly introduces the car radio trends and the advantages of the multi-standard radio receiver architectures. The following section discusses the advantages of the CT $\Sigma\Delta$M over the discrete-time (DT) $\Sigma\Delta$M and the system level considerations for CT $\Sigma\Delta$M ADCs. The second half of Chapter 4 presents a 40 MHz BW, 70 dB SNDR CT $\Sigma\Delta$M ADC implemented in 28nm fully-depleted silicon-on-insulator (FD-SOI) CMOS. The design choices and circuit blocks are presented in detail. A novel hybrid data rotational shifter structure is presented and the advantages of the structure are discussed. At the end of the chapter the layout of the ADC and the chip as well as the post-layout simulations are presented and finally the conclusions of the chapter are drawn in the Section 4.4.

Chapter 5 draws the conclusions of the thesis and discusses the future work.

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Chapter 2
An 8-bit 700 MS/s Sub-ranging Flash-SAR ADC in 65nm CMOS

2.1 Introduction

Medium resolution (6 - 8 bits), high-speed (500 MS/s - 1000 MS/s) single-channel ADCs are used in applications such as digital oscilloscopes [1] and satellite receivers [2]. However, the main driving application for these ADCs are the multi-GHz time-interleaved structures. The data rates of wireline communication standards are pushed to increase dramatically by the huge amount of data transfer in data-centers. The recent ethernet standards such as 56 Gb/s and 100 Gb/s use spectrally efficient modulation schemes such as PAM-4 due to the large losses of the conventional electrical channels. However, the drawbacks of the PAM-4 like inter-symbol interference (ISI) sensitivity increase the equalizer complexity dramatically to be robustly implemented in analog domain [3]. Therefore, ADC based serial-links are used to transfer these complex operations to the digital domain to benefit from the flexibility of the DSP. The ADCs to be used in PAM-4 systems generally have 7-8 bit resolution and up to 28 GHz sampling rate for the 56 Gb/s standard [4]. This asks for large number of interleaved channels. However, for high sampling frequencies and large number of channels, the power consumption and complexity of the clock distribution becomes a concern [5]. Reducing the number of time-interleaved channels to achieve a given aggregate sampling frequency is possible by increasing the sampling speed of the channel ADCs. Therefore, it is important to find techniques to improve the speed of the single channel ADCs while maintaining the power efficiency.

SAR ADCs are commonly used in these highly interleaved ADCs for PAM-4, given their simple implementation, excellent power efficiency and its compatibility with the advanced nano-scale CMOS technologies which favor digital processing over the analog processing. However, SAR ADCs are inferior to the flash ADCs and binary/multi-bit search ADCs in terms of speed and techniques to improve the speed of the SAR ADCs are popular research topics. This chapter is structured as follows: in the Section 2.2 the speed issues of the conventional SAR ADCs are explained and in the Section 2.3 the techniques in literature to improve the speed

of the single-channel SAR ADCs are summarized. The Section 2.4 introduces a novel reference generation technique for the multi-bit/cycle SAR ADCs and the Section 2.5 presents an 8-bit 700 MS/s sub-ranging flash-SAR ADC fabricated in 65nm CMOS technology which uses the introduced preamplifier among other speed improving techniques. Finally the Section 2.6 draws the conclusions of the Chapter 2.

2.2 Conventional SAR ADC and Its Limitations on Speed

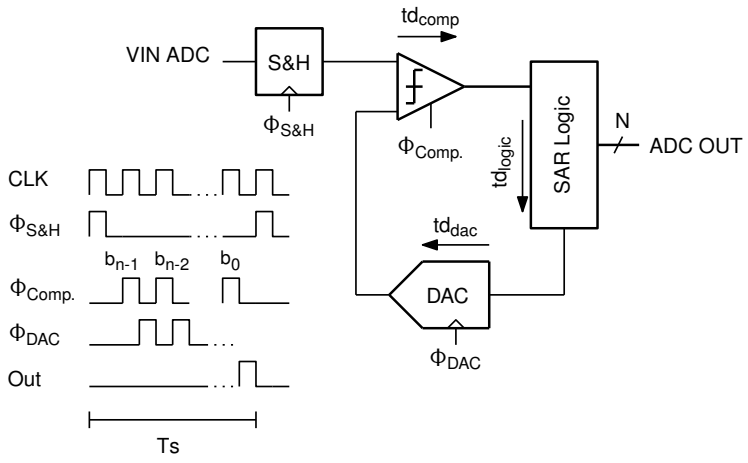

Fig. 2.1 Block diagram and timing diagram of a conventional SAR ADC.

The conventional SAR ADC which is depicted in Fig. 2.1 uses the binary-search algorithm for the analog-to-digital conversion and requires N clock cycles to resolve N-bits. The circuit is composed of a sample-and-hold (S&H) block, a comparator (which is basically a 1-bit ADC), a digital-to-analog converter (DAC) and a register logic. The DAC of the SAR ADC can be capacitive [6], resistive [15] or current-mode [8]. The SAR ADCs with capacitive DACs which are called charge-redistribution SAR ADCs [6] are commonly preferred over the other types due to their important features. The input signal can be sampled onto the capacitive DAC and the DAC has zero static power consumption.

The timing-diagram of the SAR ADC is depicted in Fig. 2.1. At the beginning of the conversion the input is sampled and it is held throughout the conversion. After the sampling of the input, the first comparison is done to determine the most significant bit (MSB). The MSB is held in the register, and according to the MSB value, the DAC gives the next reference value to generate the residue. This process goes on until the least significant bit (LSB) is determined.

The SAR ADC has several very attractive aspects which made it one of the dominant ADC architectures in the open literature [9]. First, the SAR ADC doesn't employ operational amplifiers. The difficulty in obtaining the high gain in scaled CMOS technology nodes has become an issue. This, along with the increasing interest in power efficiency shifted the focus to the ADC architectures without the operational amplifiers. Second, the SAR ADCs potentially achieve high-resolutions. Third, SAR ADCs are able to achieve zero-static power consumption. The last but not least, the comparator offset is not problematic since it manifests itself as an offset of the ADC transfer function which can be corrected easily. These aspects yield the SAR ADCs digital friendly and their implementation in scaled CMOS technologies very convenient [10], [11].

One of the main drawbacks of the conventional SAR ADC is the sequential resolving of the bits. The conversion time of a SAR ADC, therefore, linearly increases with the resolution of the ADC. For the N-bit, single-bit per cycle conventional SAR ADC depicted in the Fig. 2.1, the sampling period T_s is expressed as:

$$T_s = (N+2)\, t_{SAR} \tag{2.1}$$

where t_{SAR} denotes the loop delay which is the time required for resolving the single bit. The loop delay has basically three components and it is given as:

$$t_{SAR} = t_{comp} + t_{DAC} + t_{logic} \tag{2.2}$$

where t_{comp}, t_{DAC} and t_{logic} are the comparator delay, the DAC settling time and the SAR logic delay, respectively.

The DAC delay t_{DAC} stems from the settling requirements. The DAC should settle to half LSB to maintain the accuracy of the conversion. For the capacitive DAC, the time required for half-LSB settling is given by:

$$t_{DAC} = \tau_{DAC}\, N\, ln(2) \tag{2.3}$$

where $\tau_{DAC} = C_{DAC}\, R_{sw}$ is the time-constant of the DAC. C_{DAC} is the total array capacitance and R_{sw} is the on resistance of the DAC driving switches. The straightforward way to improve the DAC settling time is reducing the total array capacitance or the on-resistance of the switches. The on resistance of the switch can be reduced by increasing its aspect ratio, using CMOS implementation or using bootstrapping techniques [12]. Bootstrapped switches are not area efficient for this purpose, considering the large switch count. Latter two are generally used in the SAR ADCs in literature, however increasing the aspect ratio too much has diminishing returns since the switches load the preceding logic. On the other hand, the size of C_{DAC} depends on the DAC structure used (e.g. binary [6], C-2C [13,14], split DAC [15,16]), and it can be reduced by using one of the techniques such as C-2C or split-DAC. Whatever the capacitive DAC structure, the minimum unit capacitance C_u of the array for a given resolution is limited by the kT/C noise and the linearity. Generally, for medium resolutions the kT/C noise is not the limiting factor and as soon as the matching requirements are satisfied, very small capacitors can be used. These capac-

itors generally are not offered in the design-kit libraries, therefore very small custom capacitors can be used to improve the settling time and power efficiency [17, 18].

The above discussed fundamental limitations of the SAR ADC on speed has recently led to some architectural innovations such as asynchronous clocking [19–21], multi-bit/cycle [15, 22–25], redundancy and loop-unrolled SAR ADC architecture [26–28]. These architectural innovations aim to improve the SAR ADC speed by attacking a component or the combination of the components of the total cycle delay given in Equation 2.2. The following subsections explain the advantages and drawbacks of the mentioned speed improvement techniques in detail.

2.3 Techniques to Improve the Speed of a Single-Channel SAR ADC

2.3.1 Asynchronous Clocking

The conventional synchronous SAR ADCs use an external clock with the frequency of $N\,F_s$ (where $F_s = 1/T_s$) to generate the phases of conversion as depicted in Fig. 2.1, where N is the resolution of the ADC. This introduces two important disadvantages. First, the power consumed on the clock distribution becomes an issue, especially for the higher sampling rates. Second is the inefficient use of the allocated time for comparators. If the time required for a comparator to make a decision is denoted as T_{cmp}, it can be expressed for a latch with a preamplifier stage as [19]:

$$T_{cmp} = \frac{\tau}{A_o - 1} \cdot ln\frac{V_{FS}}{V_{res}} \tag{2.4}$$

where τ is the time constant of the latch, A_o is the small-signal gain of the preamplifier, V_{FS} is the full scale voltage of the ADC, and V_{res} is the residue signal at the input of the comparator. During the successive-approximation algorithm V_{res} changes from cycle to cycle. In synchronous SAR ADCs, the time allocated for the comparator is equal for each cycle and it should be chosen according to the worst case, for which the V_{res} is equal to half-LSB. Therefore, even if all the other decisions would take less time compared to the worst case, the comparator uses equal time at each cycle.

The asynchronous SAR ADC introduced in [19] circumvents the issues discussed above. The SAR performs the bit-cycling in a domino-like fashion in which a logic block generates a ready signal as soon as the comparator makes the decision and the next cycle begins. In this way, the time lost in easy decisions can be saved and large gains in the sampling rate are achieved. The external clock is only used for the sampling phase. Therefore the external clock has a frequency equal to the sampling frequency and the high-frequency clock issue is resolved. The drawback of the asynchronous SAR ADC is the metastability of the comparator. Since the bit-cycling depends on the completion of the preceding cycle, when the metastability

occurs, the conversion may take very long time or even get stuck. This causes the reduction of SNR in asynchronous SAR ADCs. An additional logic circuit is added in [20] to deal with the issue.

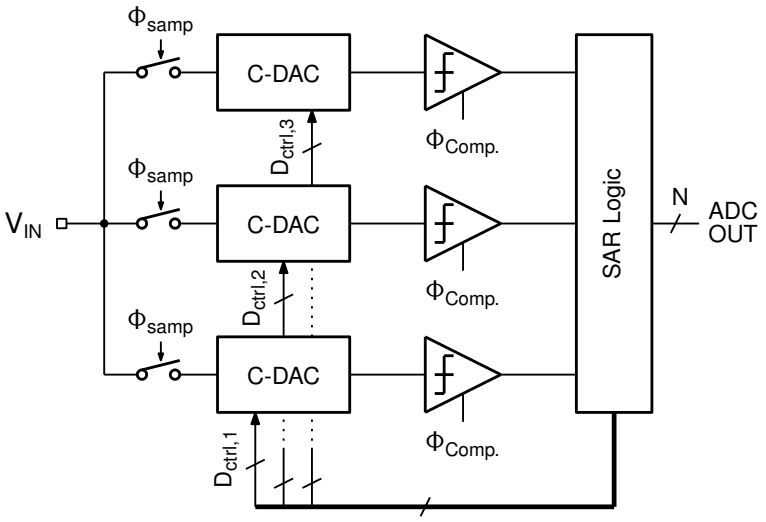

Fig. 2.2 Multi-bit/cycle SAR ADC with multiple CDACs [22].

2.3.2 Multi-bit per cycle SAR ADCs

Multi-bit per cycle (multi-bit/cycle) SAR ADC techniques focus on reducing the overall cycle number. For instance, resolving 2-bits per cycle would halve N in Equation 2.1 and theoretically double the SAR ADC speed. The approach was first introduced in [22], which uses a flash-ADC like structure to resolve 2-bits per cycle. Fig. 2.2 depicts the block diagram of the approach. The architecture employs three capacitive DACs to generate the three levels required in each cycle and three comparators for the decision. The input is sampled onto each of the three DACs. Introducing multiple DACs and comparators causes some issues for this architecture. The offset of the comparators entails non-linearity at the output, which is not the case for the conventional SAR ADC. By employing multiple DACs, the input capacitor and the area of the ADC increases considerably.

Fig. 2.3 depicts the approach presented in [15] where the three capacitive DACs (CDACs) have been replaced by a resistive DAC. This removes the necessity for multiple DACs. The sampling circuits and the reference switches are interpolated to reduce the number of components. Nevertheless, the disadvantage of this tech-

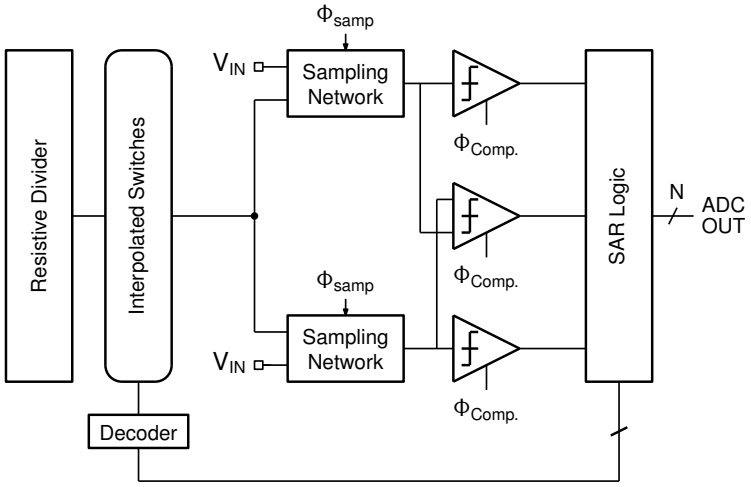

Fig. 2.3 Multi-bit/cycle SAR ADC with resistive DAC [15].

nique is the increased complexity and area overhead caused by the large number of switches and the static power consumption of the resistive divider.

The recent research focus for the multi-bit/cycle SAR ADCs is on reducing the CDAC number and the size. In [24] a 2-bits/cycle SAR ADC is presented where the CDACs are interpolated to remove one capacitive DAC. The size of the DAC is further reduced by employing a bridge capacitor and custom unit capacitors. In [23], the size of the CDAC is greatly reduced by using the subranging and hybrid resistive - capacitive DAC. In the work presented in [25] to reduce the input capacitance posed by the ADC and to reduce the number of CDACs, two separate CDACs are used for signal and reference.

2.3.3 Loop-unrolled SAR ADCs

The comparator in a conventional SAR ADC must wait for the DAC to settle to start the conversion. Therefore, t_{comp} and t_{DAC} cannot occur simultaneously. However, t_{logic} can be overlapped with t_{comp} or t_{DAC}, if not completely eliminated. The work presented in [26] is based on this idea and the architecture is called loop-unrolled SAR ADC. The proposed ADC employs N comparators for an N-bit ADC. After the decision of a bit, the comparator of that cycle passes its output to the ready signal generation logic and the capacitive DAC simultaneously. Thereby the DAC settling occurs while the signal to start the next bit cycle passes to the next comparator and t_{logic} is eliminated from the critical delay. An issue with the technique is the offset mismatch of the multiple comparators, as seen in multi-bit/cycle architectures.

The calibration or redundancy can be used to mitigate the effects of this mismatch [27, 28].

2.3.4 Redundancy

The penalty of the DAC settling on the speed of the SAR ADC can be mitigated by using the redundancy. Redundancy allows tolerating and absorbing the errors during the conversion. The redundancy can be introduced by additional decision levels [29], additional conversion steps [30] or by using a radix smaller than 2 [31]. The common idea is to have overlapping trajectories to recover the errors at the steps up to a certain limit determined by the level of the redundancy used. By reducing the time required by the DAC settling, the speed of the SAR ADC can be improved substantially. The drawback of the technique is the increased number of successive-approximation steps. However, as stated in [21], "the time saved by relaxing the DAC settling is generally much longer than the extra cycles needed to resolve all bits".

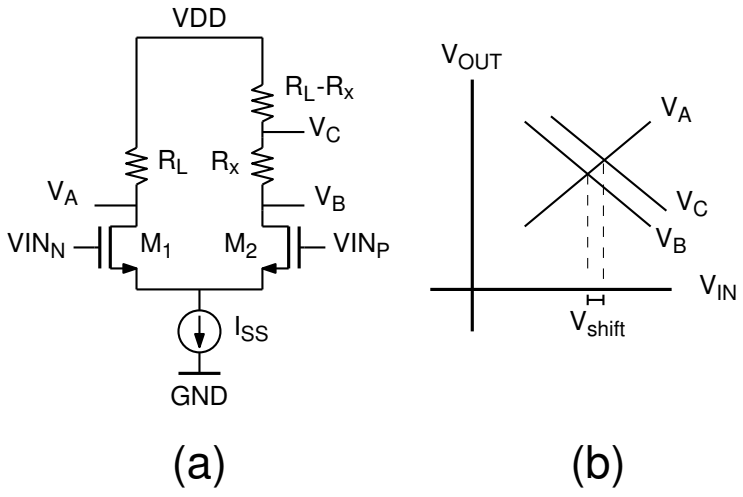

Fig. 2.4 Multiple threshold generating preamplifier concept.

2.4 Preamp with threshold generation for the multi-bit per cycle SAR ADCs

The benefits of the multi-bit per cycle SAR ADC structures are diminished by the necessity of the multiple DACs in case of capacitive approach and the complexity of the switch network in case of resistive approach. Even if the interpolation of the DACs and switches reduces the complexity, it remains as a problem for multi-bit/cycle SAR ADCs. Therefore, an efficient technique is required for the reference generation.

The work presented in this thesis and reported in [32] introduces a novel way to implement the multi-bit per cycle operation in SAR ADCs. The schematic of the concept is depicted in Fig. 2.4. The method is based on a resistively loaded differential pair in Fig. 2.4(a). The load resistor R_L is divided in two parts, R_x and $(R_L - R_x)$. By tapping the common node of these two resistors which is denoted as V_C, a shifted version of the input output characteristic of V_B is obtained. As depicted in Fig. 2.4(b), the intersection of the two voltages V_A and V_C is V_{shift} volts higher than the intersection of V_A and V_B on the V_{IN} axis. Therefore, two comparators using these two node pairs as the input will have switching thresholds V_{shift} volts apart from each other.

The value of the V_{shift} is given by:

$$V_{shift} = \frac{1}{4}\frac{R_x}{R_L}\frac{I_{SS}}{g_m} = \frac{1}{2}\frac{R_x}{R_L}\frac{1}{g_m/I_d} \tag{2.5}$$

where the g_m/I_d is the transconductance efficiency of the input transistors. The values of the tail current I_{SS}, the input transconductance g_m and the load resistor R_L are determined by the speed and resolution requirements of the ADC. Therefore, the R_x remains as the variable to obtain the required shift values. By increasing the R_x, larger threshold values can be implemented.

There are two key advantages of the proposed amplifier for threshold generation. First, the CDAC is not used for threshold generation but for residue generation. Therefore, it is not required to have multiple CDACs as in conventional multi-bit/cycle implementations. There should be only one CDAC, independently of the number of bits resolved per cycle. Second, although the preamplifier has static power consumption, it is not wasted as in the multi-bit/cycle approaches which employ resistive reference generation. In the proposed approach, the current consumed to implement the voltage gain is reused to generate the thresholds. Preamplifiers are employed to improve the speed and input referred offset of the comparators, therefore, the advantages of using a preamplifier are twofold.

The approach shown in Fig. 2.4 for generating a single positive threshold value can be generalized to obtain the reference voltages required for multi-bit/cycle SAR ADCs. The examples for 2-bit/cycle and 3-bit/cycle cases are shown in Fig. 2.5 and Fig. 2.6, respectively. The required reference values can be obtained by taking the combination of various tap voltages. For instance, for the 2-bit/cycle amplifier

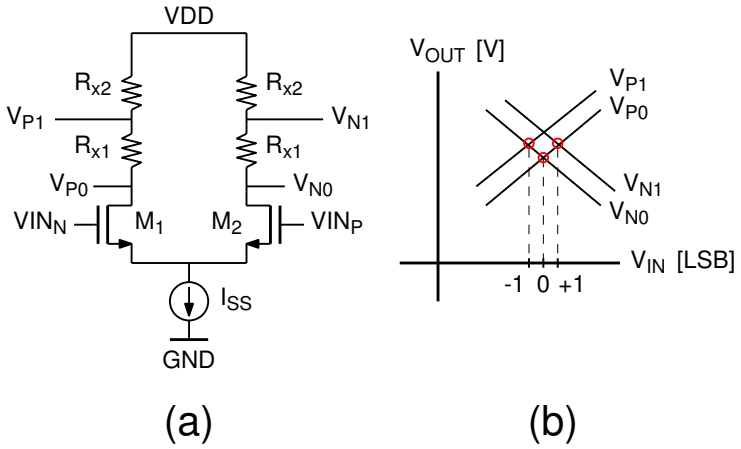

Fig. 2.5 2-bit/cycle implementation of the preamplifier.

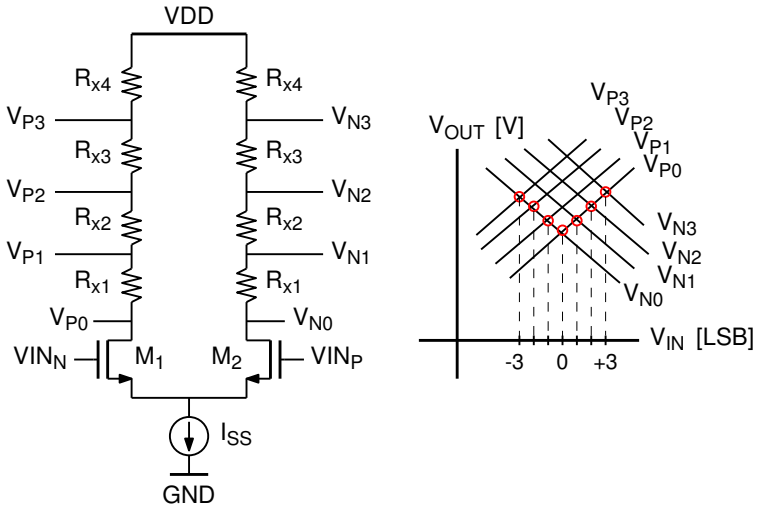

Fig. 2.6 3-bit/cycle implementation of the preamplifier.

depicted in Fig. 2.5, the 0 LSB threshold value can be obtained with the V_{P0} - V_{N0} combination or the V_{P1} - V_{N1} combination.

As shown in Equation 2.5, the threshold value depends on R_x. However, there are limits on the value of R_x. It is obvious from the Fig. 2.4 that R_x can not be larger than R_L. This puts a limit on the maximum differential threshold voltage which can be implemented with the approach. Defining the $V_{shift} = k\,V_{lsb}$, the maximum value of k can be expressed as:

$$k_{max} = \frac{I_{SS}/2}{g_m\, V_{lsb}} = \frac{1}{g_m/I_d\, V_{lsb}} \tag{2.6}$$

At k_{max}, R_x is equal to R_L therefore the $k < k_{max}$ condition should be satisfied. Since g_m, I_{SS} and V_{lsb} are determined by the ADC specifications, k_{max} is a limiting factor for the preamplifier for large input ranges. For instance, the ranges of the steps for a conventional 8-bit 2-bit/cycle SAR ADC are:

- Step 1: 0-256 LSB
- Step 2: 0-64 LSB
- Step 3: 0-16 LSB
- Step 4: 0-4 LSB

If the ADC full-scale voltage is 1 V and the g_m/I_d ratio of the input transistors are 10, then the k_{max} results in 25.6, which means that theoretically the preamp can not be used in the first two steps of the conversion. The input range can be increased through the transconductance efficiency of the input transistors with the power penalty. However, even if the g_m/I_d is taken 2.5, the range increases 4 times and it can not cover the full-scale. Moreover, lowering the transconductance efficiency of the input transistors is problematic in low supply voltages of the nanoscale technologies and an transconductance efficiency less than 10 is not convenient due to the headroom considerations. This issue calls for subranging [33], as the ADC presented in this work employs.

The second issue is related to the voltage gain of the preamplifier. In Fig. 2.4, the single-ended voltage gain from VIN_P to the tap V_C is denoted as $A_{v,C}$ and can be expressed as:

$$A_{v,C} = \frac{V_C}{VIN_P} = g_m(R_L - R_x) = gmR_L(1 - \frac{R_x}{R_L}) \tag{2.7}$$

It is clear from the equation that the voltage gain is maximum and equal to $A_v = g_m\, R_L$ at V_B where $R_x = 0$ and linearly decreases with increasing R_x. The gain loss can be compensated by increasing the R_L, but this would reduce the bandwidth of the amplifier for a given gain-bandwidth product. Therefore, to maintain the power efficiency of the technique and the accuracy of the SAR step, the number of taps should be limited to a certain value. This value, denoted as $k_{max,gain}$, can be calculated with a relationship between the allowed gain reduction and the implemented number of taps.

$$\frac{A_{v,C}}{A_{v,B}} = (1 - (g_m/I_d\, k_{max,gain}\, V_{lsb}) \tag{2.8}$$

where $A_{v,B}$ is defined in the same manner as $A_{v,C}$ in Equation 2.7. Then the $k_{max,gain}$ is given as:

$$k_{max,gain} = \frac{1 - A_v/A_{v,max}}{(g_m/I_d)\, V_{lsb}} \tag{2.9}$$

where A_v is the lowest allowed single-ended gain and $A_{v,max}$ denotes the single-ended gain at nodes V_B and V_A. The choice of A_v is arbitrary and depends on the input referred offset of the latches connected to the preamplifier and the accuracy requirements of the step.

The current consumption of the preamplifier can be calculated with the following Equation 2.10

$$I_{SS} = 2\,\frac{g_m}{g_m/I_d} \tag{2.10}$$

where the g_m denotes the transconductance and the g_m/I_d denotes the transconductance efficiency of the input transistors. The transconductance efficiency is mostly determined by the headroom since it is given by $g_m/I_d = 2/V_{ov}$. The transconductance of the transistors can be calculated using:

$$g_m = C_{load}\,GBW \tag{2.11}$$

where C_{load} is the load of the preamplifier and GBW is its gain-bandwidth product. The GBW of the preamplifier can be expressed as:

$$GBW = \frac{A_v}{\tau} \tag{2.12}$$

The gain of the preamplifier depends on the latch offset and the LSB size of the SAR step. τ is the time-constant of the dominant pole and depends on the allowed settling time of the preamplifier and the LSB size of the SAR step. τ can be expressed as:

$$\tau = \frac{t_{sett}}{(N_{adc} + 1 - m)\,ln(2)} \tag{2.13}$$

where N_{adc} is the resolution of the ADC and m is the multiplying factor for the LSB of the SAR step where $V_{lsb,step} = 2^m\,V_{lsb,adc}$.

Using the equations from (2.10) to (2.13), the tail current of the preamplifier for a SAR step can be calculated using:

$$I_{SS} = \frac{4\,(N_{adc} + 1 - m)\,ln(2)\,C_{load}\,V_{offset,latch}}{g_m/I_d\,t_{sett}\,V_{lsb}} \tag{2.14}$$

The Equation 2.14 can be used to optimize the current of the preamplifier for different SAR steps which have different load, latch offset and LSB size.

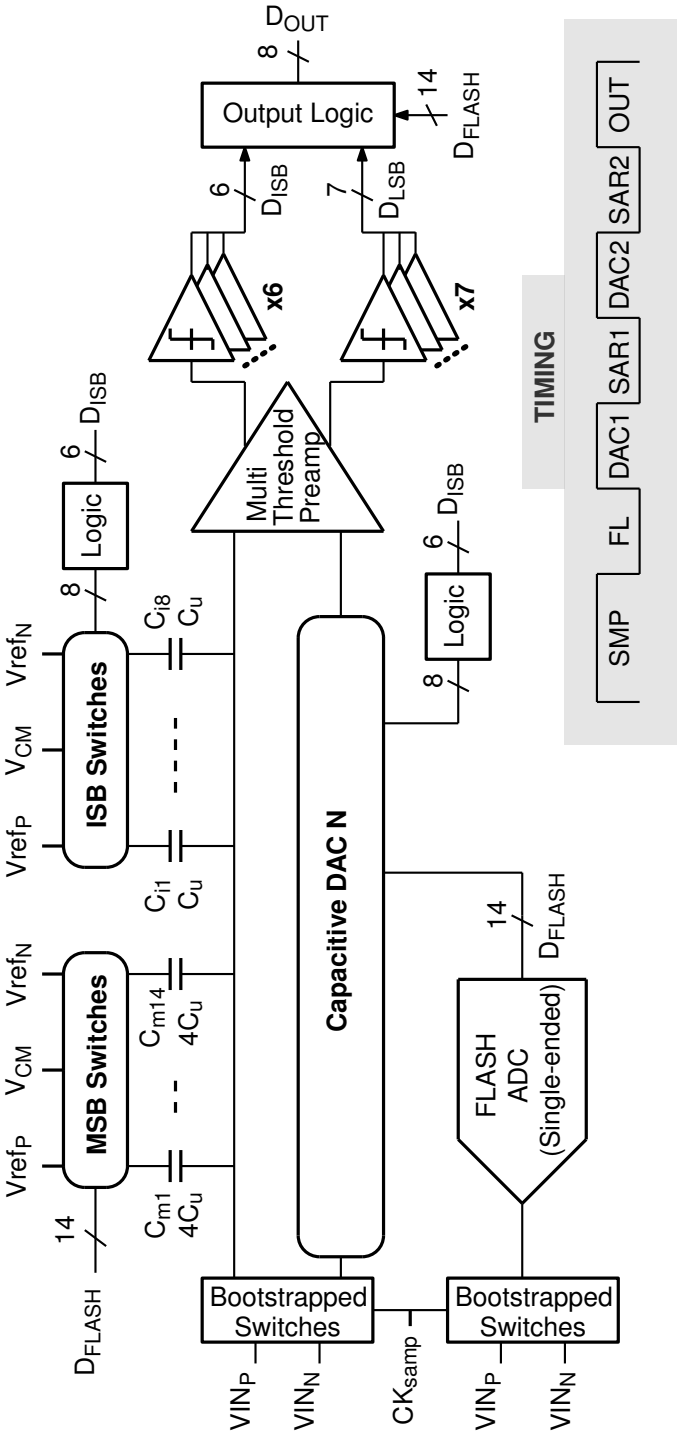

Fig. 2.7 Block diagram of the ADC.

2.5 An 8-bit 700 MS/s Sub-ranging Flash-SAR ADC in 65nm CMOS

2.5.1 Overview of the ADC

The techniques discussed in Section 2.3 can be combined to improve the power consumption and speed further. The ADC presented in this section combines multi-bit/cycle SAR with loop-unrolling and redundancy to achieve 8-bit resolution at 700 MS/s in a 65nm CMOS technology [32].

The multiple-threshold generating preamplifier presented in Section 2.4 offers important advantages to the multi-bit/cycle SAR ADC operation such as requiring only one capacitive DAC and combining the reference generation and the preamplifier functions. However, as discussed in the same section, the output range of the preamplifier calls for the subranging to reduce the dynamic range of the step. Since the work is aiming 700 MS/s, the number of steps should be low. Therefore, flash ADC is chosen for the first stage of the ADC as it requires only one step for the conversion.

The bit distribution among the flash ADC and SAR steps has impact on many aspects of the ADC, such as the time allowed for the comparator decision and the DAC settling, and the capacitive DAC size. The full-scale of the first SAR step can be used to determine the distribution. The achievable gain for a gain stage is limited in scaled technologies. Therefore, keeping the gain loss low is taken as a criteria on choosing the dynamic-range of the first SAR step. Considering a single-ended gain reduction of -3 dB, $k_{max,gain}$ is found to be equal to 15.8 using the Equation 2.9. Therefore, the full-scale of the first SAR step can be 32 LSB, where LSB is for 8-bits. This automatically sets the minimum resolution of the flash ADC of the first step as 4-bits. As discussed in [34], distributing the flash and SAR resolutions equally achieves good power efficiency. 1-bit redundancy is added to the flash ADC and the first SAR step considering the advantages discussed in Section 2.3.4.

The block diagram of the ADC is shown in Fig. 2.7 together with the timing diagram. In the first step a 4-bit flash ADC with 1-bit redundancy resolves first 3-bits. The output of the flash ADC directly controls the thermometric MSB section of the capacitive DAC to generate the residue. The residue is applied to the multiple threshold generating preamplifier which is connected to the first SAR step (SAR-1) resistive loads and the ISB (Intermediate Significant Bit) bank of latches. The 6 ISB latches resolves 3-bits with 1-bit redundancy for the SAR-1. The ISB latches then directly drive the capacitive DAC. The loop-unrolled operation eliminates the logic delay for this SAR step. Following the second DAC step, the residue is again applied to the multi-bit/cycle preamp but this time it is connected to the second SAR step (SAR-2) resistive load and the LSB latch bank. The SAR-2 stage resolves 3 LSB and passes the output to the logic. The output logic combines the bits and finalizes the conversion.

Fig. 2.8 shows the placement of the reference levels for the conversion steps where A represents the coarse step (Flash ADC), B the intermediate step (SAR-1) and C the fine step (SAR-2).

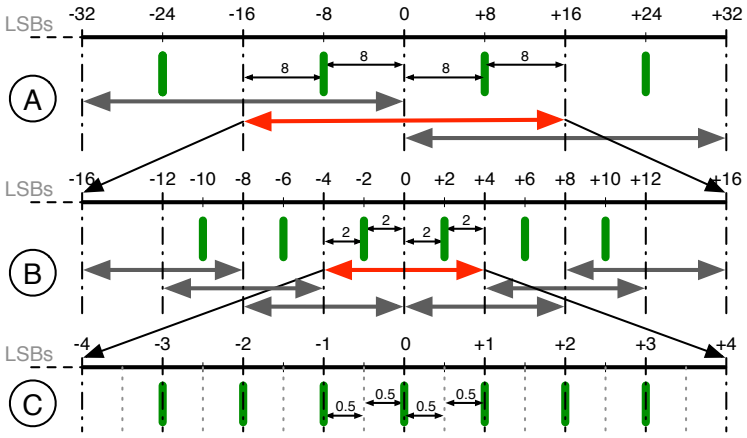

Fig. 2.8 Successive-approximation path of the ADC (Taken from [32]).

The presented work uses techniques to act on all the principal delay components of the SAR operation. A smaller capacitive DAC is used to reduce the DAC settling time, the loop-unrolling reduces greatly the logic delay, the multi-bit/cycle architecture reduces the cycle number, an improved sense amplifier latch reduces the comparator delay and the multiple threshold generating preamplifier enables the multi-bit operation without any additional capacitive or resistive DACs. The following subsections give details on the blocks and then present the measurement results of the fabricated ADC.

2.5.2 Circuit Blocks

2.5.2.1 Capacitive DAC

The multi-bit/cycle operation realized with the proposed preamp requires only one CDAC and it is used only for the input sampling and the residue generation. A conventional binary weighted CDAC for an 8-bit SAR ADC would have total number of unit capacitors equal to $2^8 C_u = 256 C_u$. In this work, 3 LSBs are resolved in the SAR-2 stage and it does not drive the DAC since the outputs are directly passed to the logic. Therefore, the size of the CDAC can be reduced to 5 bits and the C_u can be sized according to the LSB of the SAR-1 step. Since the LSB of the flash step is 4 times the LSB of the SAR-1 step, the unit capacitor for the flash section becomes $4C_u$. Total capacitance becomes $14 \times 4C_u + 8 \times C_u = 64C_u$. The total DAC

capacitance of the ADC is 75% less than what required by the conventional binary weighted CDAC. The reduction is even more if the multiple CDACs required for the conventional multi-bit/cycle SAR ADC are considered.

The unit capacitor size to satisfy the kT/C noise requirements for an 8-bit ADC is equal to 8.8 aF for a full-scale range of 1.2 V. The 65nm CMOS technology used in this work offers MOM capacitors with minimum size of 9 fF. Therefore, for more reliable operation and less layout effort, the minimum size MOM capacitor of 9 fF from the design-kit is used as the unit capacitor. This unit capacitor size also satisfies the kT/C noise and matching requirements for the given resolution. The total array capacitance becomes equal to 576 fF.

2.5.2.2 Improved Sense Amplifier Latch

The comparator architectures employed in recent high-speed ADC architectures in literature are dominantly based on the dynamic voltage sense amplifier latch (Strong-ARM latch) which is depicted in Fig. 2.9 [35]. The structure is basically comprised of cross-coupled inverters, an input differential pair and enable and reset switches. Being fully dynamic, it has virtually zero static power consumption and fast-response. The latch uses only one clock phase for enable and reset.

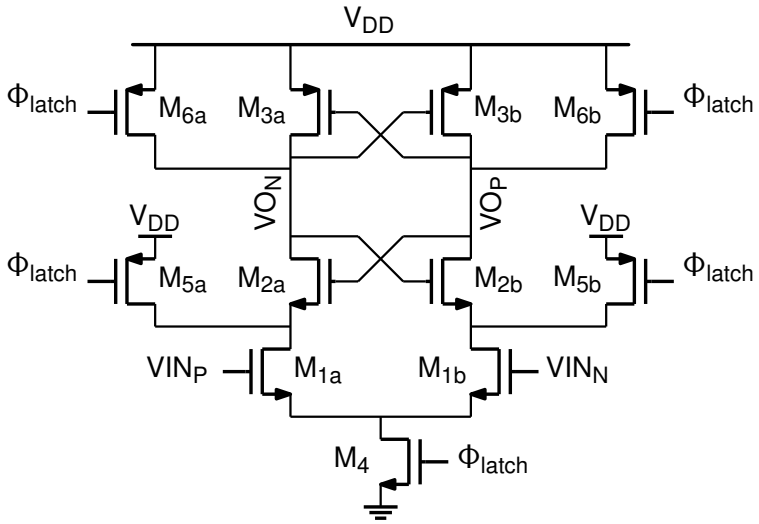

Fig. 2.9 Dynamic voltage sense amplifier latch (Strong-ARM latch) [35].

The regeneration speed of the latch can be analyzed by dividing the regeneration phase into two sub-phases [36]. In the first phase, when the enable signal goes high, the total capacitance on the output nodes starts to discharge with different rates, depending on the polarity and magnitude of the differential input voltage ΔV_{in}. This

phase continues until one of the PMOS transistors of the cross coupled inverters turns on. Assuming $VIN_P > VIN_N$, the delay associated to this phase can be expressed as:

$$t_o = \frac{C_L V_{thp}}{I_P} \tag{2.15}$$

where I_P is the drain current of M_{1a}, C_L the total load capacitance at the output node and V_{thp} the threshold voltage of the PMOS devices in the regenerative loop.

In the second phase, the positive feedback gets activated and a strong regeneration occurs. This phase continues until the voltage difference of the output nodes reaches $V_{DD}/2$ and a logical decision is taken. The delay in this phase is can be calculated as:

$$t_{latch} = \frac{C_L}{g_{m,eff}} ln\left(2\frac{\Delta V_{out}}{V_o}\right) \tag{2.16}$$

where $g_{m,eff}$ is the effective transconductance of the latch and V_o denotes the voltage difference of the output nodes at the beginning of the second sub-phase (at t_o). V_o is defined for the conventional voltage sense amplifier latch as:

$$V_o = V_{thp}\sqrt{\frac{8\beta_n}{I_o}}\Delta V_{in} \tag{2.17}$$

where $\beta_n = \frac{W}{L}\mu_n C_{ox}$ is defined for the input transistors M_{1a} and M_{1b}.

The total comparison time $t_{cmp,std}$ of the standard Strong-ARM latch can be then expressed as

$$t_{cmp,std} = \frac{C_L V_{thp}}{I_P} + \tau_{latch} ln\left(\frac{1}{V_{thp}}\frac{\Delta V_{out}}{\Delta V_{in}}\sqrt{\frac{I_0}{2\beta_n}}\right) \tag{2.18}$$

where $\tau_{latch} = \frac{C_L}{g_{m,eff}}$ is the time constant of the latch. $\Delta V_{out} = \frac{V_{DD}}{2}$ is the output swing for which the decision is made and ΔV_{in} is the comparator differential input.

For an input signal ΔV_{in} small, the latch input is close to the common mode voltage, so $I_0 = 2I_P$ can be calculated as shown in [37]

$$I_0 = \frac{\beta_n}{9}\left[\sqrt{3(V_{DD} - V_{thn})^2 - 2V_{cm}^2} - V_{cm}\right]^2. \tag{2.19}$$

where β_n is the transconductance parameter of NMOS, V_{thn} the threshold voltage and V_{cm} is the input common-mode voltage.

In this work, an improved Strong-ARM latch [38] depicted in Fig. 2.10 is used. A DC current source is inserted in parallel with the enable switch transistor M_4 while the reset transistors on the drain nodes of the input differential pair transistors are removed. These modifications have improving effects on the speed and kickback noise of standard structure as explained shortly.

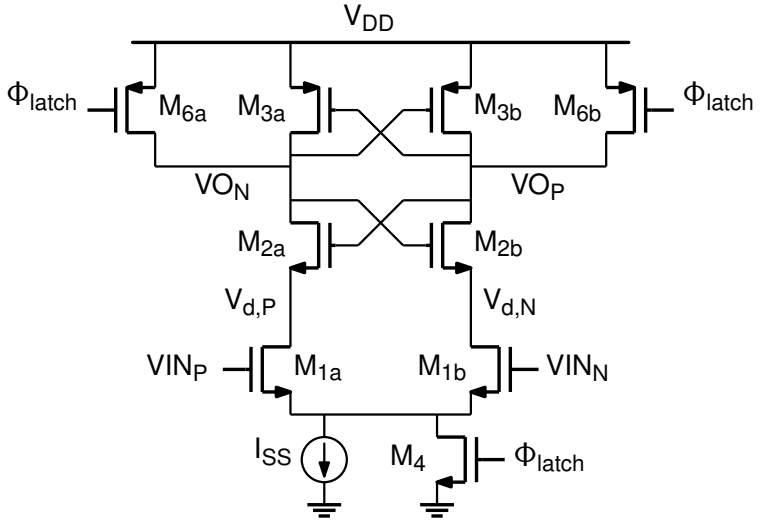

Fig. 2.10 Improved Strong-ARM latch [38].

The regeneration speed analysis of the structure can be done in a similar way to the conventional Strong-ARM latch, namely by dividing the regeneration phase into two sub-phases, t'_o and t'_{latch}.

For the improved Strong-ARM latch, the t'_o is given by

$$t'_o = \frac{C_L[V_{out,p}(initial) - (V_{DD} - V_{thp})]}{I_{P,on}}. \tag{2.20}$$

where $I_{P,on}$ is the drain current of M_{1a} during the latch phase and given by

$$I_{P,on} = \frac{I_{SS} + I_o}{2} + \Delta I_{IN} \tag{2.21}$$

where I_{SS} is the DC tail current of the input differential pair, I_o is the drain current of the tail switch M_4, and ΔI_{IN} is the differential current based on the input voltage.

For the improved structure, in the reset phase, the DC current source I_{SS}, the input differential pair transistors M_{1a}, M_{1b} and transistors M_{2a}, M_{2b}, M_{6a}, M_{6b} form a differential gain stage. Therefore, $V_{out,p}(initial)$ is determined by a common-mode voltage drop and the differential voltage output of the gain stage are given by:

$$V_{out,p}(initial) = V_{DD} - \frac{I_{SS}\, r_{ds,6a}}{2} - g_{m1b}\, r_{ds,6a}\, \Delta V_{in} \tag{2.22}$$

It can be noticed from (2.15) that t_o can be decreased by reducing the time required to reach $V_{DD} - V_{thp}$. Equation 2.20 demonstrates that the nominator decreases and at the same time the denominator increases compared to (2.15). Therefore, t'_o is expected to be lower than t_o of the standard Strong-ARM latch.

In the second phase, the positive feedback gets activated and strong regeneration occurs. The proposed structure has a modified V_o due to the DC current. It is denoted as V'_o and it is expressed as:

$$V'_o = \frac{2\,V_{out,p}(initial)\sqrt{2\beta_n(I_{SS}+I_o)}\Delta V_{IN}}{I_{SS}+I_o} + 2\left|\Delta V_{out,p}(off)\right| \tag{2.23}$$

where $\left|\Delta V_{out,p}(off)\right|$ is the differential unbalance from the gain stage in the reset phase. Hence, the regeneration delay for the proposed structure is given by:

$$t'_{latch} = \frac{C_L}{g_{m,eff}} ln\left(\frac{\frac{V_{DD}}{2} - V_{thp}}{V'_o}\right). \tag{2.24}$$

and the total comparison time of the improved Strong-ARM latch is expressed as:

$$t_{cmp,imp} = \frac{C_L[V_{out,p}(initial) - (V_{DD} - V_{thp})]}{I_{P,on}} + \frac{C_L}{gm_{,eff}} ln\left(\frac{\frac{V_{DD}}{2} - V_{thp}}{V'_o}\right). \tag{2.25}$$

Equations 2.16 and 2.24 show that decreasing t_{latch} is possible by increasing V_o. Note that, for the proposed sense amplifier latch, V'_o is increased by means of the reset gain stage. However, the logarithmic dependence of t'_{latch} to V'_o reduces the speed improvement for this phase. Fig. 2.11 shows empirical plots of $t_{cmp,std}$ and $t_{cmp,imp}$ as a function of I_{SS} using Equations 2.18 and 2.25 for generic 65nm CMOS process. A t_{cmp} improvement from 13% to 24% for I_{SS} ranging from 1 µA to 20 µA is obtained.

Transistor level simulations are performed to demonstrate the improvements of the latch. Both latches are sized to have offset standard deviation of σ_{os} = 14.5 mV. I_{SS} = 10 µA is used as for this current the power consumption of both latches gets equal. ΔV_{in} = 4 mV and $V_{CM,in}$ = 0.6 V is used in regeneration speed simulations.

Transient waveforms of the compared structures are given in Fig. 2.12. If the comparison is considered completed when the differential output voltage reaches $V_{DD}/2$, t_{cmp} is found to be 37.1 ps while $t_{cmp,imp}$ is only 30 ps. The performance of the proposed latch can be further improved by using a proper load inverter switching threshold as proposed in [38].

Dynamic latches generate more kickback noise compared to their static and class-AB counterparts [39]. This is mainly due to two mechanisms: the rail-to-rail swing at the drain terminal of the differential pair coupling to the input through C_{gd}, and the charge injection of the input transistors due to the dynamic change of region of operation (off-saturation-triode). The comparator used in this work reduces the effect of both mechanisms. The former is tackled by removing the reset transistors on the drain nodes of the differential pair, which reduces the voltage swings on these nodes. Whereas the latter is tackled by the DC current source, as it keeps the input transistors on in the reset phase. This decreases the charge fluctuation due to the change of operation mode.

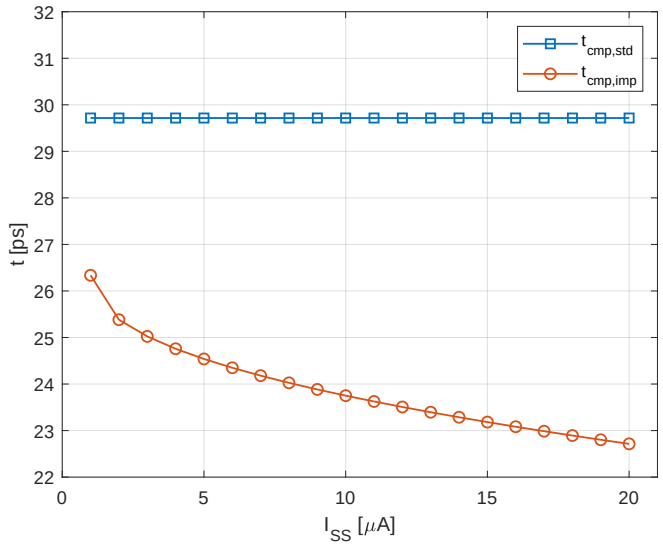

Fig. 2.11 Empirical $t_{cmp,std}$ and $t_{cmp,imp}$ as a function of I_{SS}.

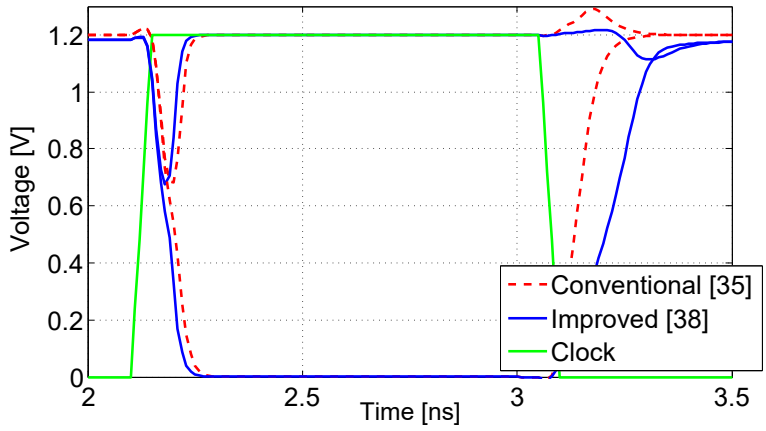

Fig. 2.12 Transient output comparison of the standard and the improved sense amplifier latch.

In order to mimic the resistive string used in this design, kickback noise simulations have been done for a 3-bit flash ADC structure using a resistive Kelvin divider with $R_U = 2\,\text{k}\Omega$. The worst case scenario is at the middle point of the divider, where the equivalent output resistance is $R_{out} = 2^{N-1}R_U$. Both the standard and the proposed comparators were tested and the difference in the kickback noise is plotted in Fig. 2.13 as a function of the unit resistance. The proposed solution is noticeably more robust against kickback perturbations.

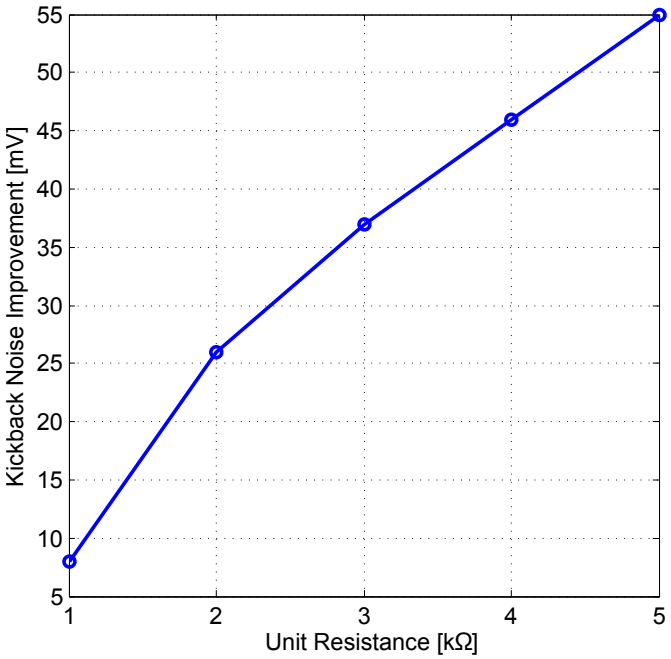

Fig. 2.13 Kickback noise improvement over the conventional Strong-ARM latch as a function of the resistive divider unit resistance when the improved Strong-ARM latch is used.

From Fig. 2.12, it can be noticed that removing the reset transistors from the drain node of the differential pair slows down the reset phase of the latch. This is not necessarily a problem if the comparator is not used at a 50% duty cycle as it is the case of the proposed design. Similarly in architectures where the comparators have small duty cycle such as asynchronous SAR, loop-unrolled SAR or comparator-based asynchronous binary search (CABS) [40] ADCs, improved Strong-ARM latch may prove useful.

2.5.2.3 Flash ADC with Reference Voltage Sampling

The first 4-bits (with 1-bit redundancy) of the ADC is resolved by a single-ended flash ADC which is composed of a resistive divider and 14 improved Strong-ARM latches. As explained in the Section 2.5.2.2, the improved Strong-ARM latch has less kickback noise compared to the conventional one. Although the magnitude of the kickback noise is reduced, the mismatch between the kickback noise on the resistive divider and the sampling capacitance remains as an issue. This issue is due to the mismatch of the impedance seen by the gates of the input transistors. In Fig. 2.14, the the gate of transistor M_1 sees the parasitic capacitance of the reference node C_p and the equivalent resistance of the divider at the reference node. Whereas

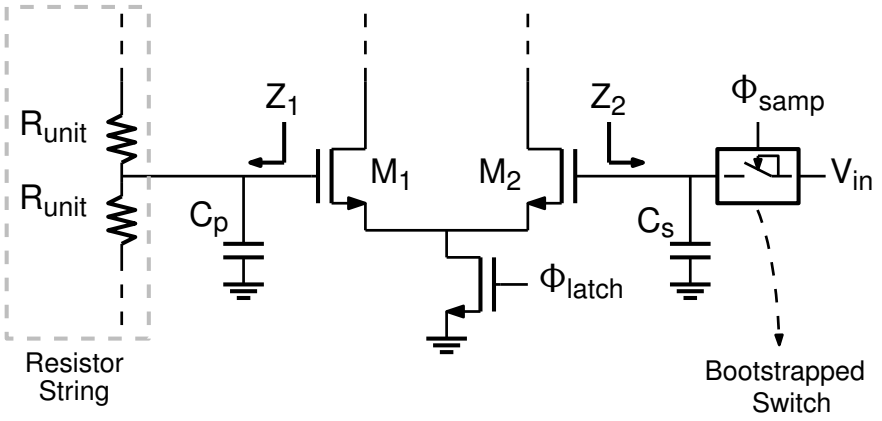

Fig. 2.14 Kickback mismatch issue in flash ADC.

the gate of the transistor M_2 sees the sampling capacitor C_s. The kickback mismatch introduces a systematic differential nonlinearity (DNL) and it becomes problematic for small differential input voltages to the comparator. To mitigate the effects of the kickback noise mismatch on the flash ADC comparators, the reference voltages are sampled onto a capacitor whose value is equal to the sampling capacitors'. The reference sampling switches are either NMOS or CMOS (for the motivations explained shortly) switches rather than bootstrapped NMOS due to the area considerations. Since for differential input the voltages at $V_{d,N}$ and $V_{d,P}$ (see Fig. 2.10) and the channel charge on the input transistors M_{1a} and M_{1b} (see Fig. 2.10) are close in value, the residual mismatch due to these two components would be small.

However, the channel charge on the reference sampling switches depends on the reference voltage to which they are connected. Since the reference voltages cover the ADC full-scale, a large variation of the channel charge is expected. On the other hand, the input sampling switches are bootstrapped, and their channel charge stays constant for a first- order approximation. Therefore, the dominant component of the residual kickback noise mismatch is the charge injection mismatch of the sampling switches. To circumvent this issue, the reference sampling switch channel widths are fine-tuned in post-layout. On higher reference voltages, reference sampling switches become slower in settling. Therefore, PMOS switches are used for the three switches from the top. However, this changes the polarity of charge injection and reduces the effectiveness of the technique for these reference levels. In order to solve the issue, CMOS switches are used for these reference sampling switches as depicted in Fig. 2.15(a). Here, PMOS switches are used for main sampling function whereas NMOS switches keeps the polarity of the charge injection same as the switches below. NMOS reference sampling switches are used for the rest of the reference voltages and it is depicted in Fig. 2.15(b). Post-layout systematic DNL plot for the flash ADC is shown in Fig. 2.16 and the maximum DNL is 0.06 LSB, where LSB stands for the overall ADC LSB.

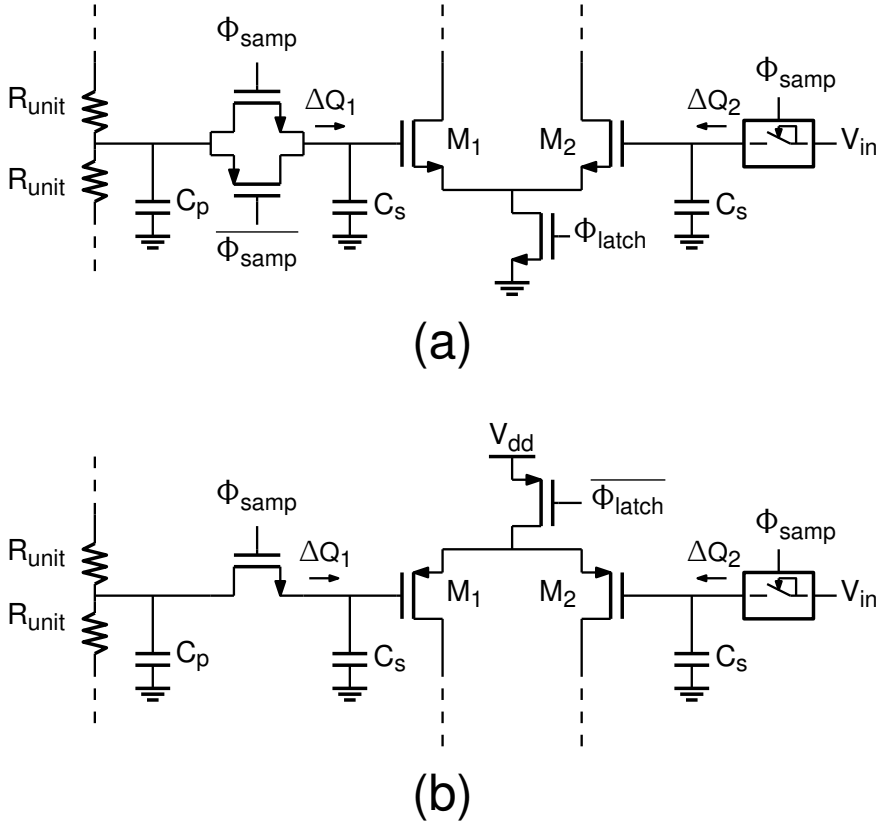

Fig. 2.15 Kickback mismatch compensation in flash ADC with CMOS ref. sampling switch (a) and NMOS ref. sampling switch (b).

2.5.2.4 Preamp with Multiple-Threshold Generation

The preamp with the multiple-threshold generation is employed in the SAR-1 and SAR-2 stages. SAR-1 and SAR-2 stages are both 3-bit/cycle and SAR-1 step has 1-bit redundancy to relax the DAC settling and comparator offset requirements. As shown in Fig. 2.8, the SAR-1 and SAR-2 stages have different threshold levels and different accuracy requirements. This calls for separate preamps for each SAR cycle, as done in conventional single-bit/cycle loop-unrolled architectures where each step has its own comparator. However, in this case the offset mismatch of the preamplifiers would be an issue. Hence, this work uses a single differential pair with two pairs of resistive load strings, one for each SAR cycle. The preamplifier switches from one to the other depending on the SAR cycle in progress. Switching between the load strings causes large settling times of the output nodes which is a penalty for the achievable speed of the ADC. Therefore, as a speed-power consumption

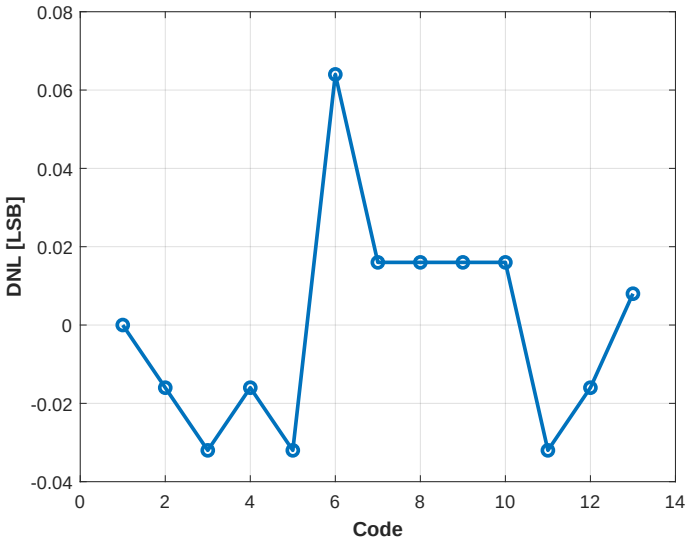

Fig. 2.16 Post-layout systematic DNL of the flash ADC.

trade-off, a dummy differential pair is added to avoid the output nodes to clip to the supply. The schematic of the preamplifier is shown in Fig. 2.17. The preamplifier is calibrated using the tail current I_{SS} for the more accurate SAR-2 cycle.

The preamplifier is connected to two banks of latches, one for SAR-1 step and one for SAR-2. The improved sense amplifier latch from Section 2.5.2.2 is employed in both banks. The connection schemes of the latches for SAR-1 and SAR-2 steps are given in Table 2.1 and in Table 2.2 respectively. SAR-2 step latches are designed with a additional parallel input differential pair to be foreground calibrated by external voltages.

Table 2.1 Preamplifier output combinations of the SAR-1 stage.

SAR-1 Step Threshold	**VIN$_P$**	**VIN$_N$**
-10 LSB	V_{P0-1}	V_{N10}
-6 LSB	V_{P0-1}	V_{N6}
-2 LSB	V_{P0-1}	V_{N2}
+2 LSB	V_{P2}	V_{N0-1}
+6 LSB	V_{P6}	V_{N0-1}
+10 LSB	V_{P10}	V_{N0-1}

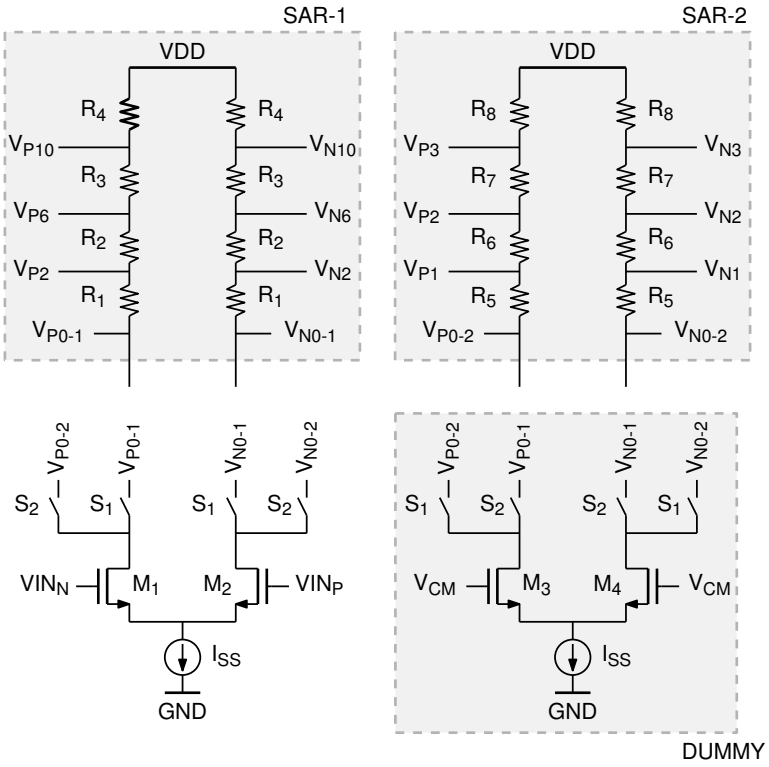

Fig. 2.17 Schematic of the multiple-threshold generating preamplifier with dummy input differential pair.

Table 2.2 Preamplifier output combinations of the SAR-2 stage.

SAR-2 Step Threshold	$\mathbf{VIN}_P$	$\mathbf{VIN}_N$
-3 LSB	V_{P0-2}	V_{N3}
-2 LSB	V_{P0-2}	V_{N2}
-1 LSB	V_{P0-2}	V_{N1}
0 LSB	V_{P0-2}	V_{N0-2}
+1 LSB	V_{P1}	V_{N0-2}
+2 LSB	V_{P2}	V_{N0-2}
+3 LSB	V_{P3}	V_{N0-2}

2.5.2.5 Switch Driving Logic

Generation and distribution of the digital control signals in high-speed ADCs can contribute more than 50% of the total power consumption and introduce a significant delay in the critical paths. In fact, in modern technologies, the regenerative time of a dynamic latch is comparable to the delay introduced by a few logic gates.

This design uses a shift-register-free logic block based on a clock divider in order to reduce the complexity of the timing control generation, as Fig. 2.18 shows. An external clock, CLK_EXT, at twice the sampling frequency is divided into two clock signals running at the sampling frequency and shifted by 90°. A combinational logic circuit provides all the phases required for the converter to work properly, while internal feedbacks ensure non-overlapping conditions in the generation of the signals. An external signal, RES_EXT, can reset the timing logic.

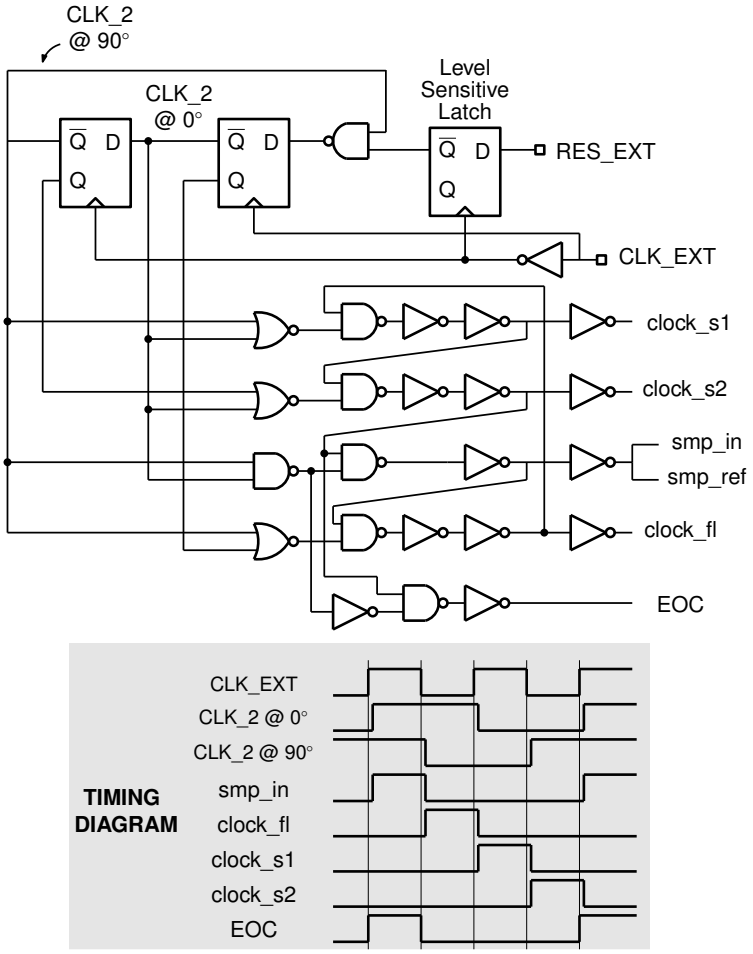

Fig. 2.18 Schematic and timing diagram of the timing logic based on a clock divider.

Apart from the sampling signals, *smp_in* and *smp_ref*, which sample both the input and the reference for the flash ADC, three clock signals are required for start each step of the converter. These are *clock_fl*, *clock_s1* and *clock_s2*. Finally, an end

of conversion signal (*EOC*) concludes the conversion cycle. The timing diagram of the clock phases is given in Fig. 2.18.

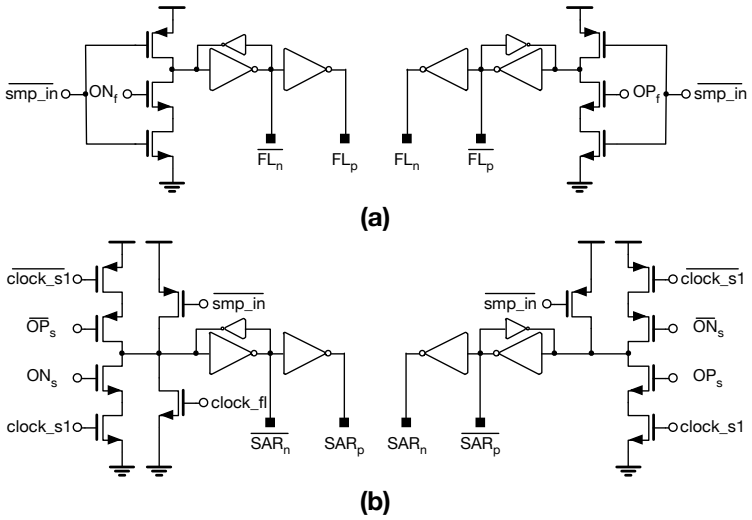

Fig. 2.19 Switch driving registers. (a) MSBs section. (b) ISBs section.

Another critical block in SAR ADCs is the switch driving registers. These registers collect the output of the comparators and feed them back to the capacitive DAC in order to arrange the next approximation in the searching algorithm. The delay introduced by this block is added to the critical feedback path in the SAR operation and can drastically limit the speed operation of the converter [41].

The proposed solution in Fig. 2.19 introduces only a 3-gate delay from when the output of the comparator is ready to when the actual switch at the bottom plate of the DAC is driven. In the MSBs section in Fig. 2.19(a), the clock signal $\overline{smp\_in}$ first sets the outputs such that the switches at the bottom plates of the DAC are all open. In fact, FL_p and FL_n drive the PMOS switches tight to the positive reference, while $\overline{FL_p}$ and $\overline{FL_n}$ drive the NMOS switches tight to the negative reference. After the sampling, the logic is ready to sample the output of the flash comparators OP_f and ON_f. Based on the latch decision, either one side or the other is reset choosing which side of the DAC is set to '1' and which is set to '0'. There are 14 such structures connected between each comparator of the flash ADC and each capacitor of the MSBs section in the capacitive DAC.

In a similar way, the ISBs section is controlled by the circuit in Fig. 2.19(b). $\overline{smp\_in}$ reset to an open condition the switch drivers. Next, the signal *clock_fl* sets the positive DAC section to '1' and the negative one to '0' for the 'test' step of the SAR algorithm. Finally, the output of the SAR comparators OP_s and ON_s are read. The nomenclature used is the same as the one used for the flash section. There

are 6 such structures connected between each comparator of the first SAR step and each capacitor of the ISBs section in the capacitive DAC. The remaining two unit capacitances in the SAR section are connected one to the positive reference and the other to the negative one, following the searching algorithm requirements.

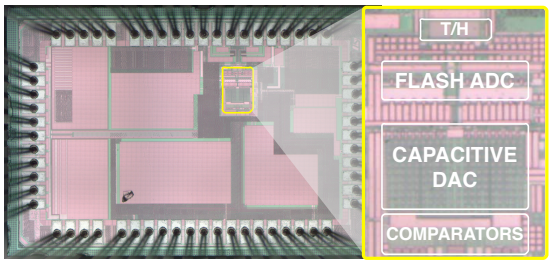

Fig. 2.20 Die photo of the fabricated chip.

2.5.3 Measurement Results

The presented ADC has been fabricated in a 65nm 1.2-V CMOS process. The design uses a standard multi-chip module of 1000 x 1500 μm^2 which includes a decimation filter for the ADC outputs. The active area of the converter is 150 x 220 μm^2 excluding the decimation filter. The chip micrograph is given in Fig. 2.20 with a magnified view of the active area of the ADC. The main circuit blocks have been highlighted.

Fig. 2.21 shows the evaluation board. The chip is bounded to the board to reduce the parasitics for the high-speed traces. An on-board buffer chip is used between the ADC outputs and the logic analyzer. The calibration voltages required for the foreground calibration of the preamplifier and the LSB latches are generated on-board using a resistive divider. The voltage references and the supply voltages are provided using the lab instruments.

Fig. 2.22 shows the measured DNL ([-0.65 : +0.75] LSBs) and the best fit integral nonlinearity (INL) ([-0.79 : +0.94] LSBs). The DNL and INL were measured using the histogram method with a sampling frequency f_s = 700 MS/s to account for dynamic non-linearities which may occur at high frequencies.

Figg. 2.23 and 2.24 give the measured output spectra at f_s = 500 MS/s for low and near Nyquist input frequencies, respectively. Whereas, Figg. 2.25 and 2.26 give the output spectra at f_s = 700 MS/s for low and near Nyquist input frequencies, respectively. The outputs were decimated by 25x and the FFTs were calculated with 16384 points. For near Nyquist input frequencies, the ADC achieves 45.2 dB (effective number of bits (ENOB) = 7.22 bits) at f_s = 500 MS/s and 41.6 dB (ENOB = 6.62 bits) at f_s = 700 MS/s. Third harmonic tones at −52 dBFS for f_s = 500 MS/s and −47 dBFS for f_s = 700 MS/s limit the spurious-free dynamic range (SFDR) at

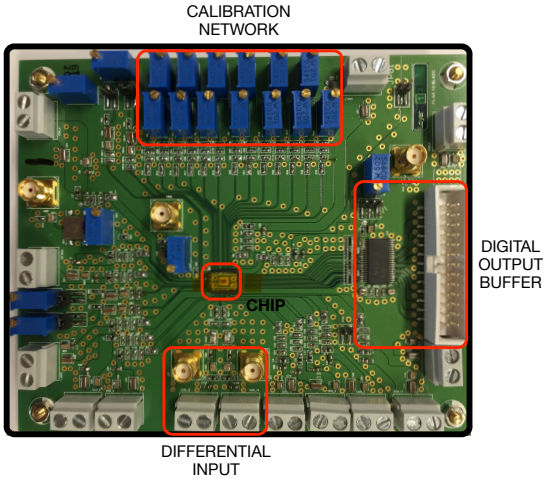

Fig. 2.21 Evaluation board.

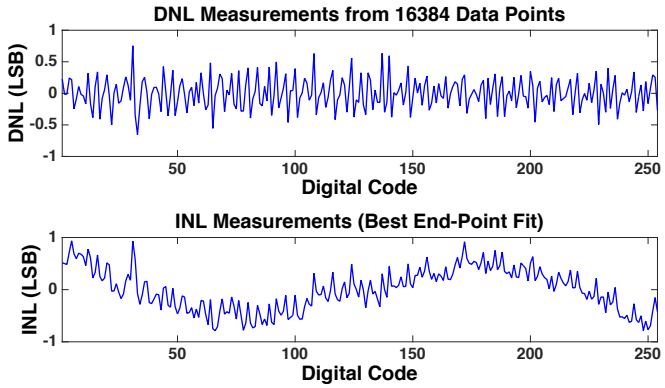

Fig. 2.22 Measured DNL and INL.

near Nyquist input frequencies. The main limitation to the ADC performances is thought to be the linearity of the input S&H block at high frequencies.

Fig. 2.27 shows the signal-to-noise and distortion ratio (SNDR) measured with a full-scale sine wave input signal as a function of the sampling frequency for different supply voltages. At the nominal supply voltage, the measured ENOB remains higher than 7 bits for sampling frequencies up to 800 MS/s, with a maximum of 7.5 bits. Fig. 2.28 shows the SFDR measured with a full-scale sine wave input signal as a function of the sampling frequency for different supply voltages. At the nominal supply voltage, the third order tone amplitude remains below the noise floor for sampling frequencies up to 700 MS/s.

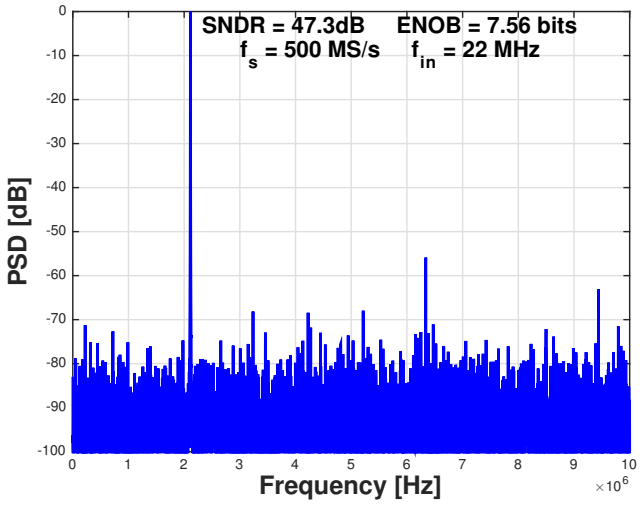

Fig. 2.23 Measured output spectrum at f_s = 500 MS/s for f_{in} = 22 MHz (Output decimated by 25x, 16384 pt. FFT).

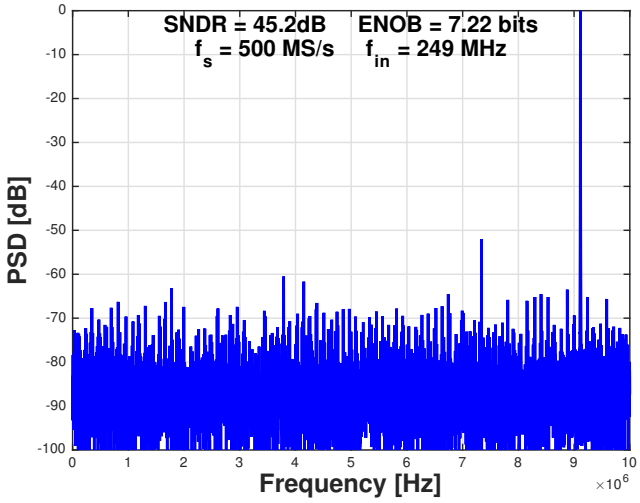

Fig. 2.24 Measured output spectrum at f_s = 500 MS/s for f_{in} = 249 MHz (Output decimated by 25x, 16384 pt. FFT).

Fig. 2.29 shows the measured SNDR at the nominal supply voltage as a function of the input signal frequency for different sampling frequencies. The performances drop significantly for f_s = 800 MS/s and input frequencies higher than 200 MS/s.

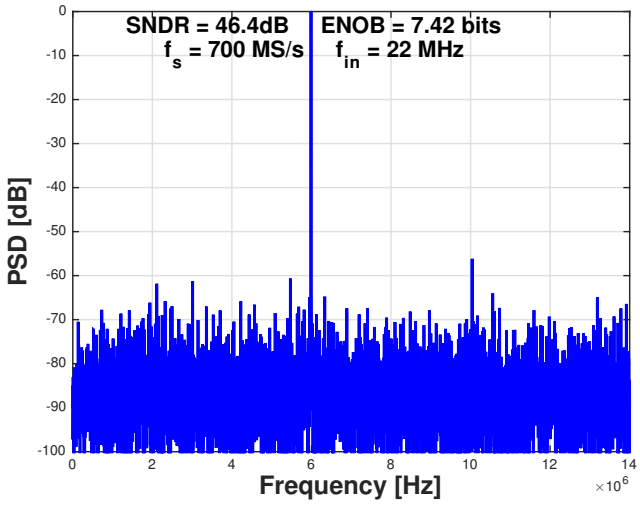

Fig. 2.25 Measured output spectrum at f_s = 700 MS/s for f_{in} = 22 MHz (Output decimated by 25x, 16384 pt. FFT).

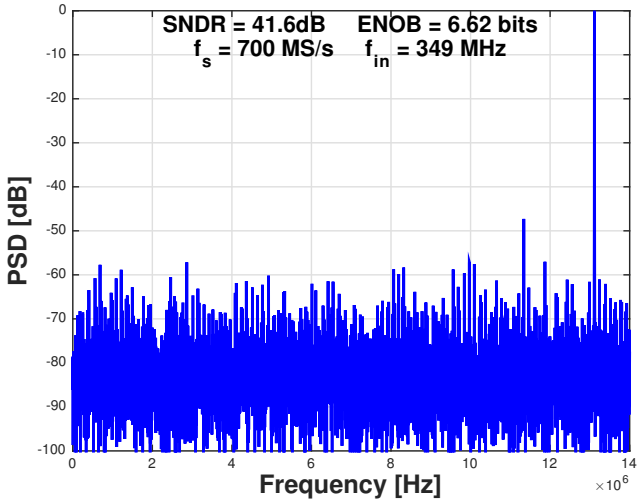

Fig. 2.26 Measured output spectrum at f_s = 700 MS/s for f_{in} = 349 MHz (Output decimated by 25x, 16384 pt. FFT).

The drop at near Nyquist input frequencies is due to the jitter noise introduced by the sampling network.

The total power consumption of the ADC is 5.96 mW (for V_{DD} = 1.2 V). The figure of merit at f_s = 0.7 GS/s is 86.7 fJ/conversion-step. Fig. 2.30 shows the power

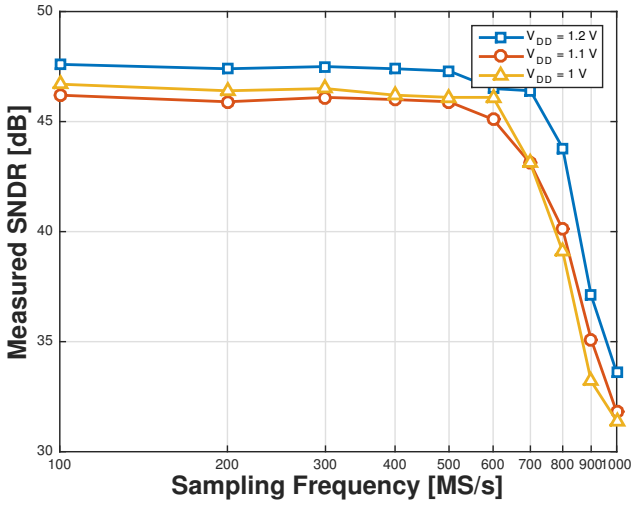

Fig. 2.27 Measured SNDR as a function of the sampling frequency for different supply voltages.

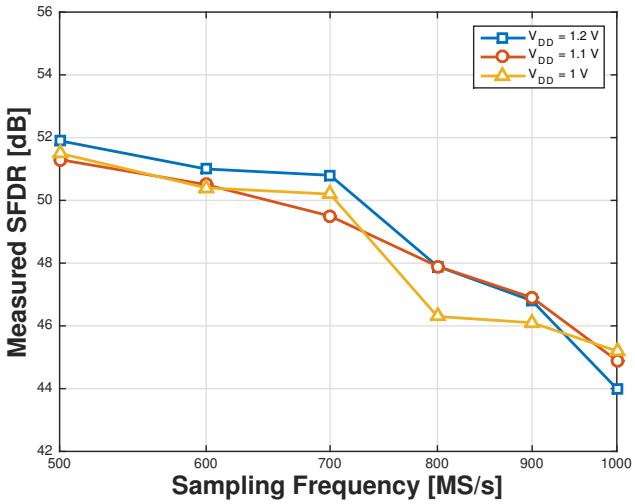

Fig. 2.28 Measured SFDR as a function of the sampling frequency for different supply voltages.

breakdown of the ADC, identifying in the digital section and the latches the power hungry part of the circuit. Scaling down the technology to 32nm node would reduce by a factor 4 that contribution, with a reduction of the consumed power by about 45%.

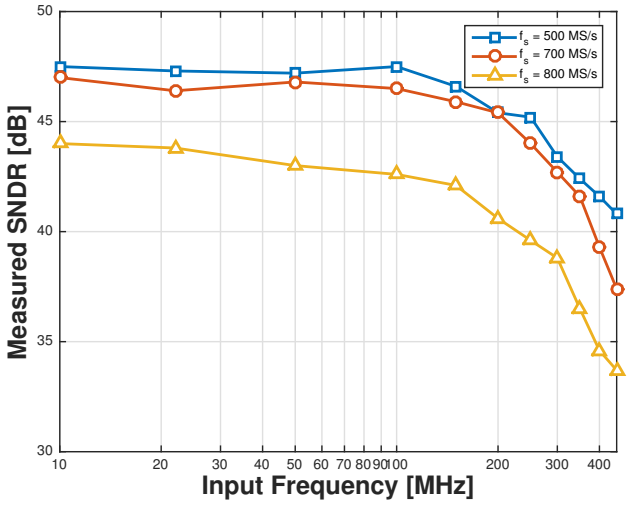

Fig. 2.29 Measured SNDR as a function of the input frequency for different sampling frequencies.

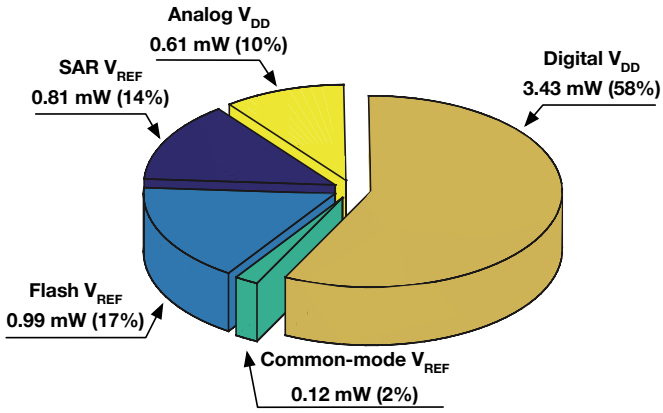

Fig. 2.30 Power breakdown of the ADC.

Table 2.3 summarizes the ADC performances and provides a comparison with state-of-the-art single channel SAR ADCs.

2.6 Conclusions

Single-channel SAR ADCs are heavily dominating the medium-resolution multi-GHz ADC application space by being utilized as a channel of time-interleaved

Table 2.3 Performance summary and comparison table.

	[23]	[21]	[15]	[25]	**This Work**
Technology	28nm	32nm	65nm	45 nm	**65nm**
Resolution	8 bits	8 bits	8 bits	7 bits	**8 bits**
Supply Voltage	1 V	1 V	1.2 V	1.25 V	**1.2 V**
SNDR near Nyquist	43.3 dB	39.3 dB	44.5 dB	40.8 dB	**41.6 dB**
Sampling Speed	0.75 GS/s	1.2 GS/s	0.4 GS/s	1 GS/s	**0.7 GS/s**
Power	4.5 mW	3.06 mW	4 mW	7.2 mW	**5.96 mW**
FoM/conv.-step	50 fJ	34 fJ	73 fJ	80 fJ	**86.7 fJ**
Area	0.004 mm^2	0.0015 mm^2	0.024 mm^2	0.016 mm^2	**0.03** mm^2

ADCs, mostly due to their simple yet very versatile structure and compatibility to the advanced nano-scale CMOS technologies. Clock distribution and calibration complexity as well as the area concerns of the heavily interleaved A/D converters call for faster single-channel SAR ADCs to reduce the channel number. The speed shortcomings of the conventional SAR ADCs can be circumvented using various methods in the open literature, such as asynchronous clocking, multi-bit/cycle operation, loop-unrolling or employing redundancy. These methods can be combined to achieve higher sampling rates and improve the power efficiency at these speeds.

In this chapter, a novel technique to generate the thresholds required for the multi-bit/cycle SAR ADCs was presented. The technique efficiently combines the preamplifier and the reference generation functions. The number of required capacitive DACs for the ADC is only one since the references are generated it the outputs of the preamplifier. This relieves the input capacitance and the area issues encountered in the conventional multi-bit/cycle SAR ADCs.

An 8-bit 700 MS/s sub-ranging SAR ADC was presented which was fabricated in 65nm CMOS technology. The ADC employs the proposed preamplifier with multiple-threshold generation for multi-bit/cycle operation. Moreover, it uses redundancy and loop-unrolling. Sub-ranging is employed to cover the input range which the preamplifier is not able to cover. A single-ended flash ADC constitutes the first step of the conversion. The flash ADC uses a reference sampling technique and fine-tuning by design to mitigate the systematic DNL. An improved Strong-ARM latch structure is used both in flash and SAR stages. The analysis and the simulations have demonstrated significant speed improvement and kickback noise reduction compared to the conventional Strong-ARM latch. The multiple-threshold generating preamp uses separate resistive loads for the SAR steps and employs a dummy differential pair to reduce the settling time penalty which occurs when the loads are switched. Loop-unrolling operation relaxes the SAR logic complexity and reduces the logic delay. A divider based logic generates the required phases for the conversion. Dynamic logic gates are used at the switch driving registers to improve the logic delay further.

The measurement results have shown a competitive Walden Figure-of-Merit of 86.7 fJ/step achieved at Nyquist.

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Chapter 3
A Timing Skew Calibration Method for Time-Interleaved FATI ADCs

3.1 Introduction

SAR ADCs have been the ADC of choice for the wide range of conversion speeds and resolutions due to their power efficiency and versatility [1]. For those conversion speeds beyond the achievable limit of a single SAR ADC, time-interleaving [2] is widely used. By increasing the number of channels in a time-interleaved (TI) ADC, the aggregate sampling speed increases. However, with large number of channels, the area, the input capacitance of the ADC and the mismatches due to the distribution of the analog input and clock phases becomes an issue [3]. Dealing with the errors due to the mismatches among the channels, namely offset mismatch, gain mismatch and timing skew may be complicated when the number of channels becomes considerable.

Flash-assisted TI (FATI) SAR ADCs employ, as the name suggests, a low-resolution front-end flash ADC to speed up the sampling speed of a TI SAR ADC [4]. The flash ADC, which is running at the overall sampling rate of the TI ADC, resolves the first few MSBs and passes the result for the LSB conversion to the cascaded time-interleaved SAR ADCs. Hence, the number of required successive approximation steps is less and the time required for the conversion is reduced proportionally to the resolution of the flash ADC. This allows to reduce the number of interleaved channels for a given overall sampling rate as the conversion speed of each channel is improved. Reducing the number of channels is important in TI ADCs as the issues such as area, clocking complexity and power consumption are mitigated and the calibration of interleaving errors becomes less complex . In [5], two FATI SAR ADCs are interleaved for a further increase in the speed. A two channel time-interleaved FATI ADC is depicted in Fig. 3.1.

This chapter proposes a timing skew calibration technique for time-interleaved FATI ADCs. The calibration method with low hardware complexity, works in the background and requires no additional reference channels. Correction is achieved via controlled delay lines in the analog domain. An important advantage of the proposed technique is that it facilitates the randomization of channels in multiple

flash FATI ADCs. Section 3.2 provides an overview of the timing skew calibration techniques in TI ADCs, whereas Section 3.3 focuses on prior art in timing skew calibration dedicated to FATI ADCs. Section 3.4 gives details of the proposed method while in Section 3.5 channel randomization issues in time-interleaved FATI ADCs are discussed. In Section 3.6 hardware considerations are provided. The Section 3.7 discusses the limitations of the proposed technique. The simulation results are given in Section 3.8 and finally in Section 3.9 the conclusions are drawn.

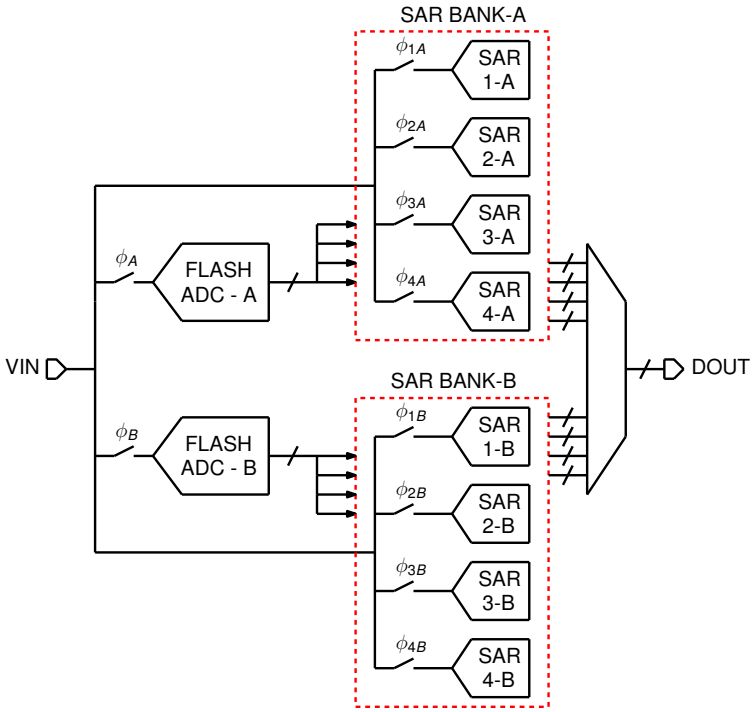

Fig. 3.1 Block diagram of a two channel time-interleaved FATI ADC.

3.2 Timing Skew Calibration in Time-Interleaved ADCs

Offset, gain and timing mismatches between the channels are important performance limiting factors for time-interleaved ADCs. Among them timing skew remains as an important performance bottleneck as the characteristics of timing skew induced errors, such as the input frequency dependency, yields the estimation and calibration of timing mismatch cumbersome. Therefore, the calibration of the timing skew in TI ADCs is an important topic. This subsection provides an overview for the

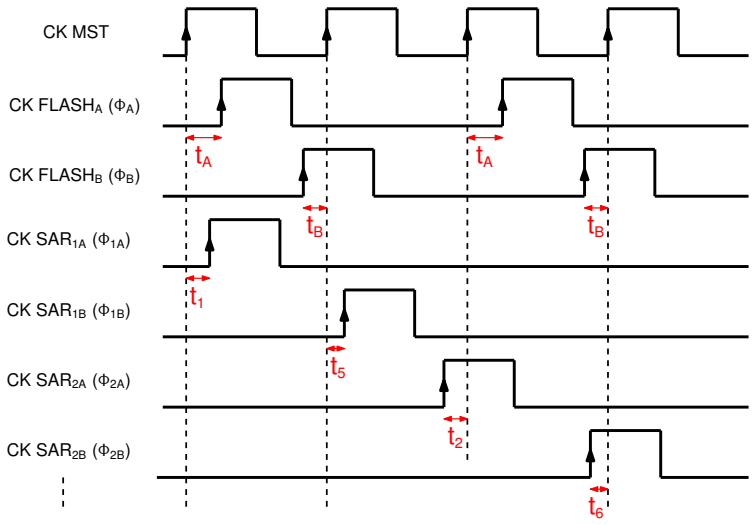

Fig. 3.2 Clock phases of a two channel time-interleaved FATI ADC depicted in Fig. 3.1.

prior art in two phases of timing skew calibration in TI ADCs, namely estimation and correction.

Precise estimation of the timing skew is possible using test signal with known characteristics. In this case, the calibration is done in the foreground and the ADC operation should be stopped for the calibration. In [6], a pulse train with fast edges is applied to the ADC input and the timing skew of the channels is estimated iteratively using an FFT. In [7] and [8] a sine-wave input test signal with known amplitude and frequency is employed to extract the offset, gain and timing mismatch information using an FFT of each channel. A very critical drawback of the foreground calibration techniques is that the ADC should be stop its regular operation for the calibration. If the application requires ADC to operate continuously, then the calibration circuit can not track the process, voltage and temperature (PVT) variations.

Background estimation techniques are attractive as they do not require the ADC to halt the normal operation for calibration, they do not require test signals and they can perform the estimation from a wide range of input signals. An approach to the background timing skew estimation is employing additional channels as the reference. In [9], two additional ADC channels are used, one as a timing reference and the other is to calculate the derivative of the input signal. In [10], an additional ADC channel is combined with a time-to-digital converter (TDC) for the skew estimation. The work presented in [11], employs 8 auxiliary channels for the timing skew calibration of a 16 channel TI ADC. There are several drawbacks regarding the use of additional channels. Firstly, the modulation of input impedance due to the switching of the reference channels can result in the spurious tones at the output [12]. Moreover, for TI ADCs with small number of channels, additional reference channels may pose an overhead for area and power consumption. In [13], authors use only a

comparator as the additional reference channel which mitigates the area issue. The works presented in [3, 14–16] use skew estimation algorithms which do not require additional channels.

Once the timing skew is estimated, the correction can be done in the digital domain or in the analog domain. Finite impulse response (FIR) filters [17] can be used to correct the timing skew in the digital domain. However, a high correction resolution increases the number of filter taps dramatically [12]. In [14], both the estimation and the correction is done in the digital domain. Due to the use of precise digital reconstruction filters, a third of the overall power consumption is from the timing skew calibration section which penalizes the FoM [18]. Correction of timing skew in analog domain by utilizing the voltage controlled delay lines is commonly preferred due to its simplicity [3, 9–11, 15, 16]. The jitter introduced by the voltage controlled delay lines should be kept low to avoid any performance degradation due to the jitter induced noise [3].

3.3 Timing Skew Calibration Techniques for FATI ADCs

A timing skew calibration technique dedicated to a single-channel FATI ADC is proposed in [16]. The block diagram of the technique is depicted in Fig. 3.3. In this method, the timing skew information is extracted via the variance of the SAR ADC outputs. The timing reference for the skew estimation is the flash ADC, therefore no additional reference is required. If there is a skew between the flash ADC and one of the SAR ADC channels, the distribution of the SAR ADC outputs changes and the variance of the SAR ADC output increases as depicted in Fig. 3.3. In a conventional flash-SAR ADC, this mismatch would cause a conversion error. However, redundant levels added to the conversion algorithm allow to absorb the errors due to the skew between the flash ADC and SAR ADC while retaining the variance information. Exploiting this fact, an algorithm is employed to minimize the variance, which results in minimizing the skew between the flash ADC and the SAR ADC channel. The variance is calculated in the digital domain and in the background, for all the SAR channels. At the end of the calibration sequence, the skews of the channels are aligned to each other and to the flash ADC. Timing errors are corrected via controlled delay lines. The estimation method is shown to be robust against the noise and the offset of the comparators [16].

The time-interleaved FATI ADC presented in [5] calibrates the timing skew for each of the flash ADCs and SAR ADCs separately, using the low jitter master clock of the converter as the timing reference. The master clock samples the divided version of itself at the input of the respective comparators of the flash and the SAR ADCs and, depending on the result of the comparison, the direction of the skew is determined. Using controlled delay lines the errors are corrected in analog domain. The method has drawbacks. It relies on precise comparators which calls for comparators calibration. Moreover, the accuracy of the technique depends on the

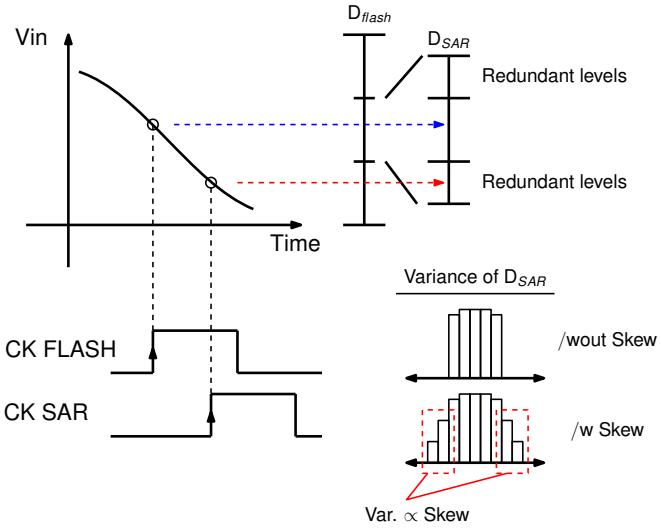

Fig. 3.3 The calibration technique proposed in [16].

rise time of the sampled reference clock. Therefore, this skew estimation method increases the analog circuit complexity and makes it more susceptible to errors.

3.4 Proposed Timing Skew Calibration Method

3.4.1 Two channel time-interleaved FATI ADC

The method proposed in [16] is a statistical skew estimation method in the digital domain and it is shown to be robust against flash ADC comparators offset and flash ADC and SAR ADC comparators noise. A disadvantage of the technique is that, unless the clock skews of the flash ADCs match exactly, it can not be used for interleaved FATI ADCs. Indeed, when there is a skew among the flash ADCs, SAR ADCs in different banks will be referred to different references, therefore there will be a systematic mismatch among the banks at the end of the calibration.

Fig. 3.4 explains the situation in a tabular form for the time-interleaved FATI SAR ADC shown in Fig. 3.1. The timing skew calibration technique reported in [16] is applied to each bank separately. This phase is denoted as Calibration-1. The initial skews of the FLASH ADC-A and FLASH ADC-B are t_A and t_B, respectively. At the end of Calibration-1, the skews of the Bank-A SAR ADCs will be t_A whereas the skews of the SAR ADCs of the Bank-B will be equal to t_B (assuming infinite correction resolution) as they get aligned with their respective flash ADCs. In this case, the time-interleaved FATI ADC reduces to a two-channel TI ADC since in

terms of the timing skew, SAR ADCs in a bank are equal to each other. As a result, for a two channel time-interleaved FATI ADC with 4 SAR ADCs in each bank, all the interleaving spurs except the one located at $f_s/2 - f_{in}$ are calibrated where f_s is the sampling frequency of the TI ADC and f_{in} is the input signal frequency. Both SNDR and SFDR are limited by this spur.

ADC BANK	SAR CHANNEL	TIMING SKEW		
		Initial	Post Cal.-1	Post Cal.-2
BANK A	SAR 1A	t_1	t_A	t_{final}
	SAR 2A	t_2	t_A	t_{final}
	SAR 3A	t_3	t_A	t_{final}
	SAR 4A	t_4	t_A	t_{final}
BANK B	SAR 1B	t_5	t_B	$t_{final} + \varepsilon$
	SAR 2B	t_6	t_B	$t_{final} + \varepsilon$
	SAR 3B	t_7	t_B	$t_{final} + \varepsilon$
	SAR 4B	t_8	t_B	$t_{final} + \varepsilon$

Fig. 3.4 Tabular representation of the calibration phases of the proposed method.

Considering the fact that after the separate bank calibration, only the spur at $f_s/2 - f_{in}$ remains, the variance-based calibration technique of [16] can be combined with another one to eliminate the remaining spur to have a complete timing skew calibration. In this work the auto-correlation based timing skew estimation technique proposed in [15] is employed for this purpose since it does not require a timing reference. It is shown in [15] that the averaged difference of the difference of outputs gives a result proportional to the timing skew between two channels. By minimizing this average value, one minimizes the skew among the channels.

The proposed method is depicted in Fig. 3.5 and is applied to a two channel time-interleaved FATI ADC. The usage and the function of the randomization logic block depicted in the figure will be explained in the following Section 3.5. The first phase of the calibration (Calibration-1) is for aligning the skews of the SAR ADCs belonging to a bank, taking their respective flash ADC as reference. As stated above, this phase uses the method proposed by [16]. Using a single variance calculation block, the variances of the SAR channel outputs are minimized through a proper algorithm. Skews are aligned using controlled delay lines. This step reduces the dis-

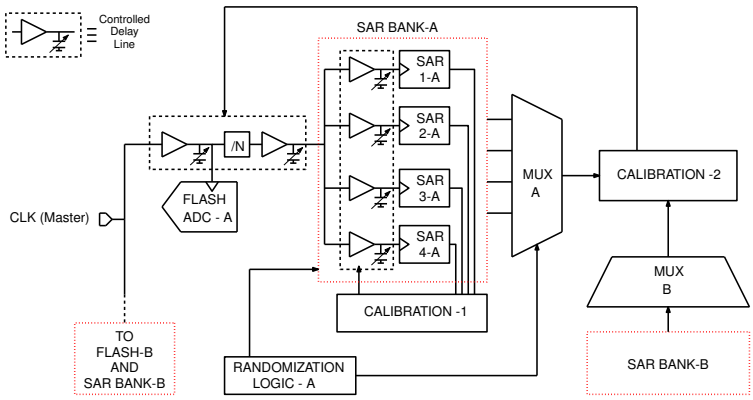

Fig. 3.5 Proposed timing skew calibration technique (inputs and outputs of flash ADCs and SAR ADCs are omitted for the sake of simplicity).

tortion greatly and increases the SNDR. However, as already mentioned, the SFDR is limited by the spur located at $f_s/2 - f_{in}$.

In the second phase (Calibration-2), the skews of the banks are aligned. The multiplexed outputs from the banks are taken and the average of differences is calculated [15]. Using the existing linear relationship between the skew and the averaged Calibration-2 output, the magnitude and the sign of the skew are estimated. The correction is applied to only one of the FATI ADC channels to align the channels. In the corrected FATI channel both the flash ADC and the SAR ADCs are corrected to keep the alignment obtained in the Calibation-1. As given in Fig. 3.4, at the end of the Calibration-2, timing skews of the Bank-A are aligned to t_{final} whereas the Bank-B timing skews are aligned to the $t_{final} + \varepsilon$. Here ε represents the residual skew between the banks and it depends on the resolution of estimation and correction phases. It is clear that the larger the ε is, the larger the residual spur located at $f_s/2 - f_{in}$ becomes.

3.4.2 Four channel time-interleaved FATI ADC

The proposed method can be easily extended and applied to time-interleaved FATI ADCs with more than two FATI channels. Increasing the FATI channels number has no effect on the hardware requirements of the Calibration-1 as the variance calculation block will be common to all the SAR channels. Only the calibration duration increases since the number of channels to be calibrated increases. For the Calibration-2, a 4-channel version of the auto-correlation based skew estimation method proposed in [15] can be used. As it will be discussed in following Section 3.6, this introduces additional hardware.

3.5 Channel Randomization

Timing skew calibration circuits improve the SNDR and the SFDR of the ADC greatly. However, the spurious tones due to the residual interleaving errors may still limit the performance. In this case, using the randomization of channels [19] is a simple technique to spread the time-interleaving spurs over the spectrum, therefore further improving the SFDR.

Channel randomization in FATI ADCs is straightforward. However when the FATI ADCs are interleaved, channel randomization has drawbacks. One drawback is related to the routing. In standard time-interleaved FATI ADCs, the flash ADC outputs would go only to the related bank of SAR ADCs. On the other hand, to implement the channel randomization, outputs of both flash ADCs should be connected to all of the SAR channels. The issue is depicted in Fig. 3.6 for a two times interleaved FATI SAR ADC. An n-bit flash ADC has $((2^n) - 1) = Nc$ digital outputs. If the TI ADC has $2M$ channels (M denotes the number of SAR channels in a bank), both flash ADCs should drive $2MNc$ wires and these wires should be routed in front of the SAR ADC banks. For medium and highly interleaved FATI ADCs, serious congestion problem arises. Apart from the routing, this issue creates a power consumption overhead. Since the flash ADCs in such a scheme operate at multi-GHz sampling frequencies, driving such a high number of flash outputs can be costly in terms of power consumption.

Each SAR bank can be randomized separately as depicted in Fig. 3.7 to avoid routing and power consumption issues. In this case, the inter-connections of the flash ADCs and the banks are equal to the non-randomized case. By randomizing the banks separately, long term averages of the timing mismatches of the banks will be different. Therefore, when the outputs are multiplexed finally, due to the difference between the averages of the banks, the TI ADC will behave like a two-channel one. It is similar to the case encountered after the Calibration-1 phase and it is explained above. An interleaving spur proportional to the difference of averages appears at $f_s/2 - f_{in}$. The other interleaving spurs get distributed over the Nyquist interval due to the channel randomization. By maintaining the sufficient correction resolution, the remaining spur can be reduced to a point where it is buried in the noise floor and the full benefit of the channel randomization is obtained. Randomization logic block depicted in Fig. 3.5 uses the technique proposed in [20]. Instead of operating at $f_s/4$, each SAR runs at $f_s/3$ to allow for the randomization between two available channels. Hence, auxiliary channels for the randomization can be avoided.

3.6 Hardware Requirements

The first phase of the calibration requires counters to generate the histogram and a small memory, a multiplier and an accumulator for the variance calculation [16]. The hardware complexity of Calibration-1 does not change with the total number of channels since the same block is shared among all of the SAR ADC channels.

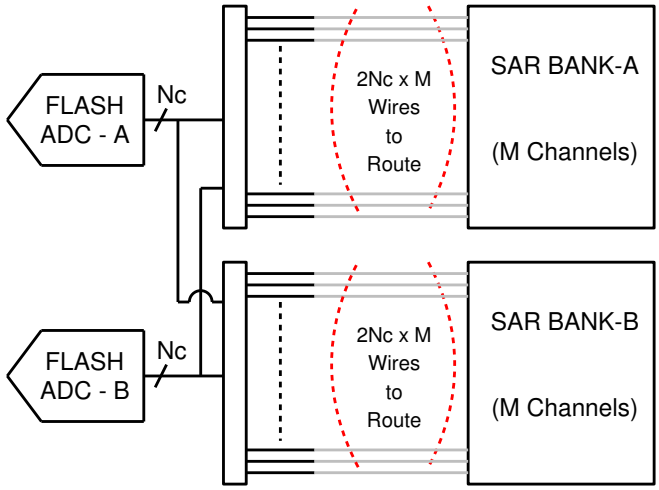

Fig. 3.6 Congestion due to channel randomization in time-interleaved FATI ADC.

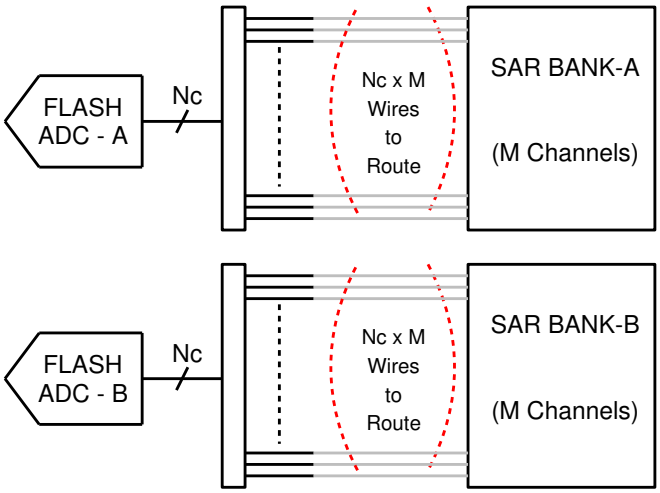

Fig. 3.7 Bank channel randomization in time-interleaved FATI ADC.

Calibration-1 block operates at the speed of one SAR channel as it takes samples from one channel at a time. Therefore, the proposed technique does not add complexity or power consumption overhead for Calibration-1 phase.

The hardware requirements for the second phase of calibration are reduced when compared to the 8-channel regular TI ADC which employs the method in [15]. In the proposed technique, the required calculations for Calibration-2 are performed for two channels with two registers, 3 subtractors and 1 averaging block. An 8-

channel TI ADC would use 8 registers, 7 averaging blocks and 21 subtractors for the timing estimation using the same method.

Hardware Overview

Calibration-1 (for N_{ch} channels, N_{bank} banks)	
1 Histogram Calculation Block	
1 Variance Calculation Block	

Calibration-2		
	This Work (N_{ch} ch., N_{bank} banks)	Ref. [15] (N_{ch} ch.)
Registers	N_{bank}	N_{ch}
Subtractors	$3 \times (N_{bank} - 1)$	$3 \times (N_{ch} - 1)$
Averaging Blcks.	$N_{bank} - 1$	$N_{ch} - 1$

Fig. 3.8 The hardware overview of the proposed technique.

The proposed method can be extended and applied to time-interleaved FATI ADCs with more than two FATI channels. The overview of the hardware requirements for an N_{bank} times interleaved FATI SAR ADC with total number of SAR channels equal to N_{ch} (where $M = N_{ch} / N_{bank}$) which uses the proposed technique is given in Fig. 3.8. Increasing the FATI channels number has no effect on the hardware requirements of the Calibration-1 as the variance calculation block will be common to all the SAR channels. Only the calibration duration increases since the number of channels to be calibrated increases. For the Calibration-2, the hardware requirements are compared with a TI ADC which has N_{ch} channels and employs the method of [15]. The number of required blocks is proportional to the number of banks in the case of the proposed method while for the reference method it is proportional to the number of channels.

The proposed method reduces the hardware required for the second calibration phase dramatically. Even if the hardware added by the first phase of calibration decreases the margin of this reduction, this additional hardware runs at lower frequency and it is shared among the SAR ADC channels. Therefore, both phases combined, the proposed method still can be considered advantageous in terms of hardware.

3.7 Limitations

Timing skew estimation techniques may suffer from misdetection and divergence issues. Both of the estimation phases used in this work have requirements on the characteristics of the input signals [15, 16]. The Calibration-1 requires a busy input signal with sufficiently large amplitude to cross at least one of the flash ADC reference voltages. Moreover, the input frequency of the ADC should not be an integer multiple of the clock frequency of a channel. Finally, the characteristics of the input signal should be maintained during the calibration since the estimation algorithm relies on the statistics of the input. Main limitation of the Calibration-2 phase is the constraint on the frequency of the input signal. To obtain the convergence of the algorithm, input frequency should not be equal to the $f_s/2$. Nevertheless, it is demonstrated in [15] that the algorithm is able to converge for the input signals which consist of a tone at $f_s/2$ and a band-limited random signal.

One of the shortcomings of the proposed method is the duration of the calibration. The Calibration-1 phase should use large number of points for reliable SAR channel output statistics [16]. In [16], 2^{17} samples are used to calculate the variance of the SAR output for each channel. The samples are taken with a rate equal to the clock frequency of a SAR channel since a single variance block is shared among the channels. The Calibration-1 duration t_{cal1} for an N_{bank} times interleaved FATI SAR ADC with N_{ch} SAR channels can be expressed as:

$$t_{cal1} = N_{conv} (N_{ch})^2 N_{cal1} T_s \tag{3.1}$$

where N_{conv} is the number of variance calculation cycles required for skew estimation algorithm to converge, N_{cal1} is the number of samples used for variance calculation and T_s is the sampling period of the TI ADC. N_{ch} is expressed as:

$$N_{ch} = N_{bank} M \tag{3.2}$$

where N_{bank} is the number of FATI ADC banks, M is the number of SAR ADC channels in a bank. t_{cal1} is independent of the number of banks and depends on the total number of SAR channels. For a 2-bank, 8-channel 4 GS/s TI ADC which uses 2^{16} samples and it takes 10 calibration cycles for each channel to converge, then the Calibration-1 phase takes 11 ms.

Calibration-2 phase requires significantly less time compared to the Calibration-1 phase. Duration of this phase depends on the number of samples used for the skew estimation and the number of cycles for the convergence of the algorithm. The Calibration-2 duration t_{cal2} for an N_{bank} times interleaved FATI SAR ADC with N_{ch} SAR channels can be expressed as:

$$t_{cal2} = 2 N_{conv} (N_{bank} - 1) N_{cal2} T_s. \tag{3.3}$$

The t_{cal2} is proportional to the number of SAR banks N_{bank}, and does not depend on the total number SAR channels N_{ch}. For a 2-bank 8-channel 4 GS/s TI ADC which uses 2^{16} samples and it takes 10 calibration cycles for each channel to con-

verge, then the Calibration-2 phase takes 0.5 ms. Required time for the whole calibration for the proposed technique then becomes approximately 11.5 ms. The type of the application determines if this calibration duration meets the requirements.

3.8 Simulation Results

A behavioral model of a 10-bit two-times interleaved FATI ADC with 8 SAR ADC channels is used to demonstrate the effectiveness of the proposed method. The offset and gain mismatch of the channels are assumed to be calibrated using the methods such as [17], [21], [22], so that the model includes only the timing skew. The considered flash ADCs have 4-bit resolution and the SAR ADCs have 7-bit resolution with 1-bit redundancy. The considered sampling speed is 4 GS/s. Timing skews for the flash ADCs and SAR ADCs are generated with normal distribution with a standard deviation of 1 ps and a mean value of 0. In each of the calibration phases, 2^{16} samples are used to perform the timing skew estimation.

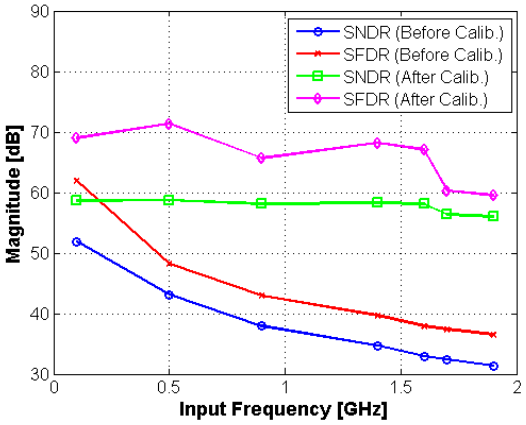

Fig. 3.9 Simulated SNDR and SFDR as a function of the input signal frequency.

Fig. 3.9 depicts the simulated SNDR and SFDR as a function of the input signal frequency for an input magnitude of -3 dB$_{FS}$. Correction step size of 100 fs is used for both Calibration-1 and Calibration-2. It can be noticed that, after applying the proposed calibration procedure, the SNDR and the SFDR of the ADC remains almost constant in the entire Nyquist range. Due to the correction step size, there is a small drop at high frequencies.

The simulated output spectra of the ADC before and after Calibration-1 for an input signal frequency of 1.9 GHz and magnitude of -3 dB$_{FS}$ are given in Fig. 3.10. Please note that time-interleaving spurs are largely cleared. The spur due to the average timing skew between the banks is present at $f_s/2 - f_{in}$ and it is slightly increased.

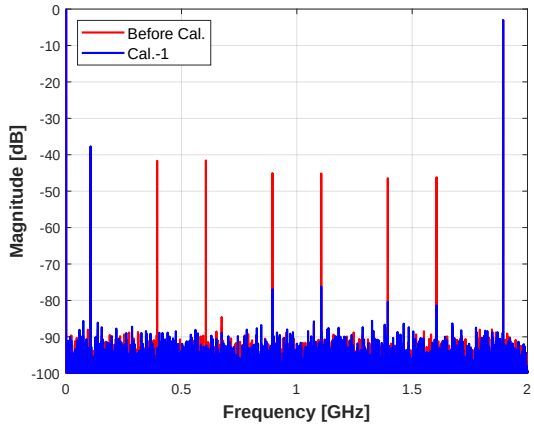

Fig. 3.10 Simulated output spectra before and after Calibration-1 (16384 point FFT, f_{in} = 1.9 GHz, A_{in}= -3 dB_{FS}, Correction step = 100 fs).

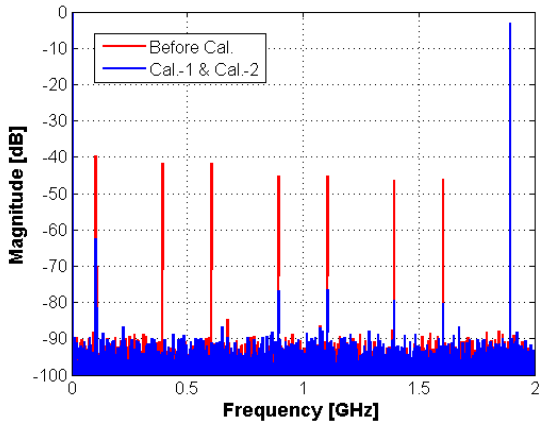

Fig. 3.11 Simulated output spectra before and after calibration (16384 point FFT, f_{in} = 1.9 GHz, A_{in}= -3 dB_{FS}, Correction step = 100 fs).

Fig. 3.11 shows the spectrum without calibration and after both calibration phases. Applying the Calibration-2 reduces the spur at $f_s/2 - f_{in}$ by approximately 20 dB. The residual spur is due to the limits of the correction and it can be further reduced by employing smaller timing correction steps.

Fig. 3.12 depicts the simulated output spectrum of the ADC when the calibration and the channel randomization are combined. The spur at $f_s/2 - f_{in}$ is not changed as expected from the separate randomization of the banks and the wideband SFDR [23] remains around 60 dB. The narrowband SFDR [23] is improved by 10 dB when compared to the case without the randomization and is equal to 85 dB. This allows

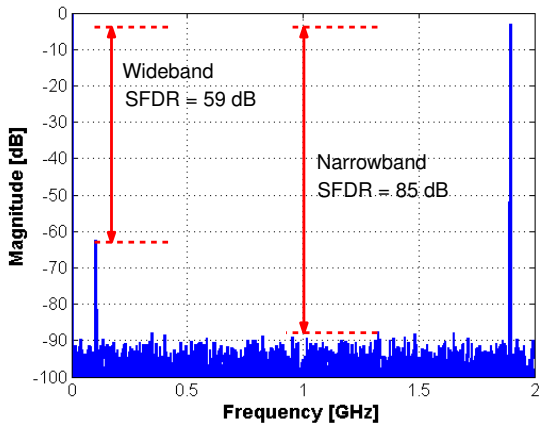

Fig. 3.12 Simulated output spectrum after calibration and channel randomization (16384 point FFT, f_{in} = 1.9 GHz, A_{in}= -3 dB_{FS}, Correction step = 100 fs).

one to use the ADC with higher performance for narrowband signals by filtering out the residual spur, as done in so-called ”ping-pong” scheme [24].

3.9 Conclusions

A timing skew calibration method for time-interleaved FATI ADCs is proposed. The method uses the combination of variance based and auto-correlation based timing skew estimation in digital domain with reduced hardware complexity. It works in the background and no auxiliary analog blocks for timing-reference are required. The method also facilitates the channel randomization which reduces the routing complexity and saves power. Behavioral simulations have demonstrated that the method works effectively up to Nyquist frequency.

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Chapter 4
40 MHz BW, 70 dB SNDR CT ΣΔM ADC in 28nm FD-SOI CMOS

4.1 Introduction

Terrestrial radio tuners have been the base of the in-car infotainment since their introduction decades ago. The modern cars offer very sophisticated infotainment systems which combine functions such as entertainment, traffic information, navigation & points of interest and media playback [1]. Nevertheless, the terrestrial radio tuner is still a crucial element for in-car infotainment systems, either for consumer preferences or for accessibility and wide broadcasting coverage of the analog standards such as amplitude modulation (AM) and frequency modulation (FM).

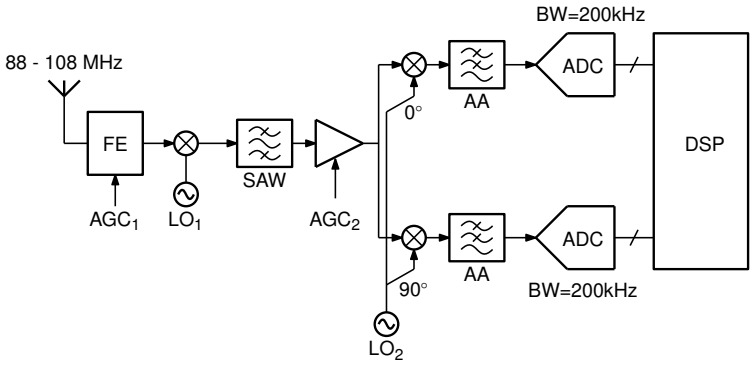

Fig. 4.1 A Superheterodyne radio receiver for FM band reception.

Traditionally, car-radio tuners use the superheterodyne structure [2]. A superheterodyne receiver for FM radio is depicted in Fig. 4.1. The issue with the architecture is the external components and the tunable intermediate frequency (IF) local oscillator (LO) which should have very low phase noise. These problems can be alleviated by employing the wideband IF ADC concept [3] which is depicted in

Fig. 4.2. With this structure, the channel tuning and channel filtering operations are moved to baseband DSP unit which reduces the cost and complexity considerably. Only one LO is required to down convert from RF to IF. The flexibility of the system increases substantially as the tuning, channel filtering and variable-gain amplifier (VGA) operations are moved to DSP. By using a CT ΣΔM ADC, the anti-aliasing filters preceding the ADCs can be removed too. The drawbacks of the architecture are the following. First, as no in-band filtering takes place before the ADC, there is no in-band selectivity [3]. Second, the VGA is moved to DSP, therefore the dynamic range (DR) of the ADC should be increased accordingly against the strong interferers. These two points make clear that the wideband IF architecture demands an ADC with large bandwidth and high dynamic range.

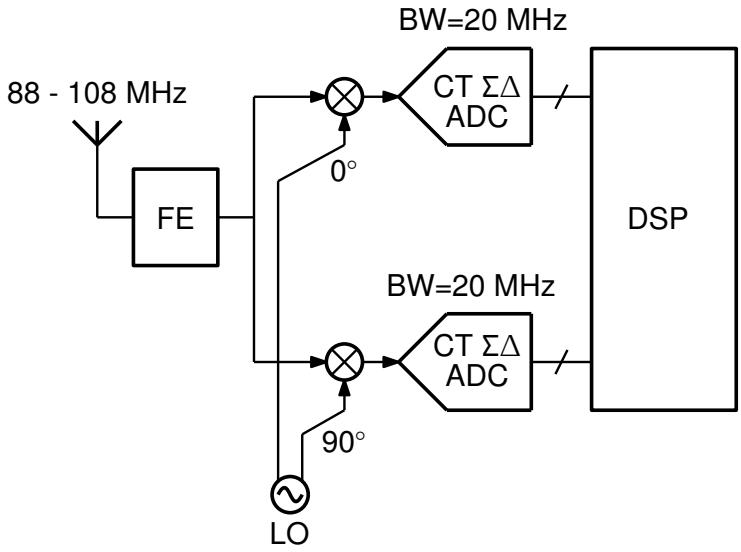

Fig. 4.2 Wideband IF ADC concept.

Modern terrestrial radio tuners receive legacy analog standards such as AM/FM beside their digital counterparts such as digital audio broadcasting (DAB) and HD Radio. Considering the large volume low profit characteristic of the tuner market [4], the integration of a multi-standard tuner becomes important to reduce the silicon area and the power consumption while giving large flexibility as seen in software-defined radios. One such receiver architecture is depicted in Fig. 4.3. The idea is having different front-ends for different bands while sharing a wideband ADC and doing the channel selection and additional filtering in the digital domain. The wideband ADC should have the bandwidth to cover the widest transmission band. For a receiver which covers the AM, FM and DAB bands, the DAB bandwidth is the widest of all and equal to 70 MHz. If a quadrature conversion is adopted, the ADC

should have the bandwidth of 35 MHz. Moreover, the dynamic range and the linearity of the ADC should satisfy the requirements of all the standards. For instance, required total harmonic distortion (THD) for the DAB is around -80 dBc whereas AM asks for -100 dBc [5]. Therefore, the AM standard sets the stringent requirements on the DR and linearity of the ADCs.

In this chapter, a CT ΣΔM ADC for a multi-standard car radio receiver is presented. The aimed specifications for the ADC are:

- **Bandwidth**: 40 MHz
- **Dynamic Range**: 70 dB

The power consumption is generally not the primary concern in automotive applications, therefore, no specification is given. The linearity should be maximized to satisfy the reception quality of the receiver.

The outline of the chapter is following: in Section 4.2 the system-level considerations on CT ΣΔM ADCs are given, in Section 4.3 the designed ADC, its circuit blocks and the simulation results are presented and the conclusions are drawn in Section 4.4.

The research work presented in this chapter is done within the scope of a project in collaboration with the STMicroelectronics.

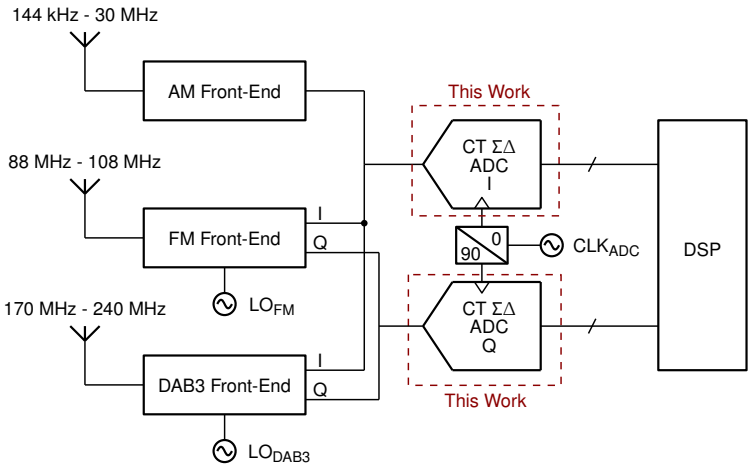

Fig. 4.3 A multi-standard tuner for car radio.

4.2 System-Level Considerations

4.2.1 Continuous-time Sigma-Delta Modulation

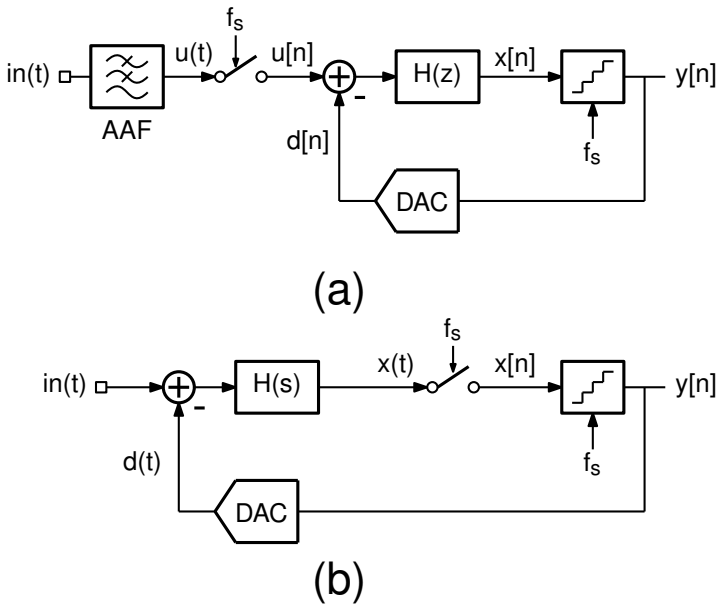

Fig. 4.4 A DT ΣΔM (a) and a CT ΣΔM (b).

The block diagrams of DT and CT ΣΔMs are depicted in Fig. 4.4(a) and Fig. 4.4(b), respectively. DT ΣΔMs offer advantages such as precise loop-filter coefficients and the insensitivity to the stray capacitances [6]. However, CT loop-filter realizations have several advantages over the DT implementations.

In CT implementations, the sampling operation takes place inside the loop. This introduces three important advantages. First, the errors of the sampling circuit are shaped by the loop, therefore the sampling nonidealities have reduced impact. Second, the CT modulators are free from the kT/C noise. In DT ΣΔMs, achieving high-resolution necessitates large sampling capacitors. Driving large capacitors at high-frequencies becomes problematic and it is a significant contributor to the overall power consumption for high-speed, high-resolution DT ΣΔM ADCs. Third, the CT ΣΔM operation results in an implicit anti-aliasing filter [7] which alleviates the issue of anti-aliasing filter which precedes the DT ΣΔM ADCs.

The CT ΣΔMs can achieve potentially higher speed with good power efficiency. This is demonstrated by numerous implementations in the open literature. The CT

integrators do not require the complete settling of their outputs which is a significant advantage in terms of power consumption.

On the other hand, there are few disadvantages of the CT modulators. First, loop-filter coefficients are set by the product of a resistor and a capacitor value. This product shifts dramatically with process variations and if not tuned the modulator may get unstable. In DT modulators, these coefficients are set by the ratio of capacitor values and they are highly accurate in the presence of process variations. Second, the CT modulators are sensitive to the effects such as excess loop delay and jitter, which are minor problems for the DT ΣΔMs. Most of these issues have system level or circuital solutions or they are popular research topics. Therefore, especially for high-resolution wideband ADCs, the CT ΣΔM ADC is very attractive and widely used solution.

4.2.2 Loop-filter

The chosen noise transfer function (NTF) can be implemented with various type of loop-filter architectures. Firstly, it can be single-loop or multi-loop. In this work a single loop architecture is used to avoid issues encountered in multi-loop architectures such as quantization noise leakage [8].

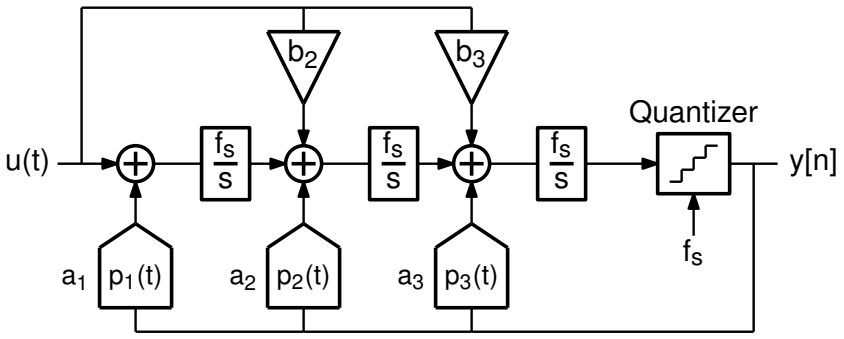

Fig. 4.5 A CIFB loop-filter structure.

The zeros of the loop-filter can be implemented with feed-back or feed-forward coefficients. A cascade of integrators with feed-back (CIFB) structure is shown in Fig. 4.5. The structure has feed in coefficients b_2-b_0 to reduce the signal swing at the output of the integrators. With the CIFB structure a flat signal transfer function (STF) can be implemented, which is useful for receiver applications. Having various feedback DACs, the precise and the fast paths are detached which is useful to maintain the stability and optimize the system. However, in CIFB structure the signals at the outputs of the integrators contain a signal component on top of the shaped

quantization noise. Therefore, they have large swings. If the integrator gain is lowered to reduce the swings, the input-referred noise increases, and nonlinearity of the loop-filter degrades. Feed-in coefficients can be used to reduce the swings; however, they have the same effect since they reduce the loop-gain of the integrators. One other drawback of the CIFB structure is the number of feedback DACs, which can be problematic in terms of area.

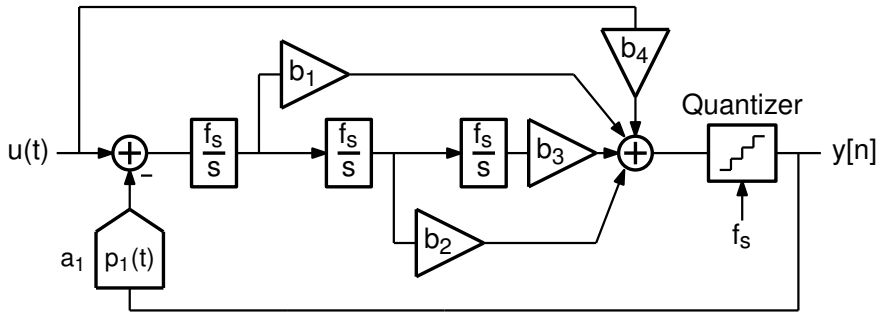

Fig. 4.6 A CIFF loop-filter structure.

Cascade of integrators with feedforward (CIFF) shown in Fig. 4.6 alleviates some of the issues encountered with the CIFB structure. It has only one feedback DAC at the input of the modulator and the signal component is canceled at the input. The integrators process only the quantization noise (theoretically) and they have smaller output swings. Therefore, the noise and linearity performances of the CIFF structure is better compared to the CIFB. The drawback of the CIFF structure is the STF peaking, which can be problematic for the receivers in hostile environments with large blockers present. Unlike the CIFB, in CIFF structure, the precise and the fast paths are not detached, which makes the first integrator very important in terms of stability. Moreover, the CIFF structure offers less anti-aliasing compared to the CIFB.

The cascade of integrators with feedforward-feedback (CIFF-B) structure shown in Fig. 4.7 is a combination of the CIFF and CIFB architectures. As in CIFB, the fast and precise loops are independent. The second integrator does not have a DAC input, therefore, the signal swing at its output is relatively small. The CIFF-B shows STF peaking but its magnitude is smaller than the peaking seen in CIFF. The linearity and noise performances are improved as in CIFF, compared to CIFB structure. The anti-aliasing performance is better than in the case of the CIFF but inferior to the CIFB. As a summary, the CIFF-B structure offers a good-trade off between the CIFF and CIFB architectures.

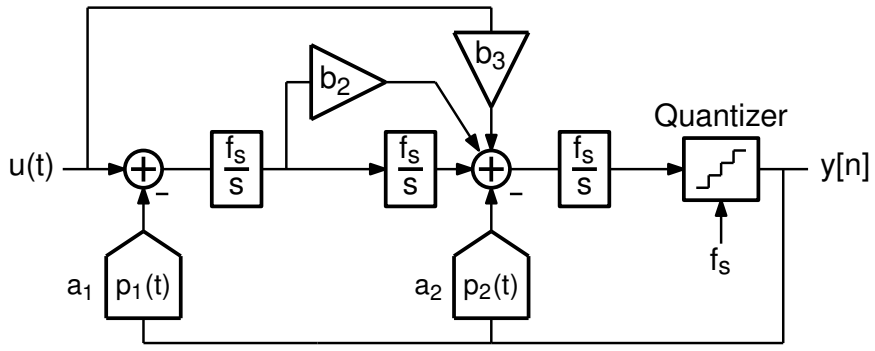

Fig. 4.7 A CIFF-B loop-filter structure.

4.2.3 Quantizer

The number of quantization levels is an important aspect of the ΣΔM ADCs. The single-bit ΣΔM ADCs use only one comparator as a quantizer which makes the implementation easier. The absolute linearity of the two-level feedback DAC makes the single-bit ΣΔM ADCs very attractive. However, the achievable Signal-to-Quantization-Noise Ratio (SQNR) of a single-bit ΣΔM ADC is lower for a given OSR and modulator order compared to the multi-bit implementations. Increasing the modulator order is problematic in terms of the stability. Increasing the oversampling ratio (OSR) increases the sampling rate and puts stringent requirements on the integrators. Single-bit ΣΔM ADCs have large LSB size which increases the jitter sensitivity and degrades the integrator linearity [9]. The jitter sensitivity of the single-bit ΣΔM ADCs can be reduced by using techniques such as finite impulse response (FIR) DAC [10], however the sampling rate drawback persists. Recently, techniques were presented to relax the sampling rate limitations on the FIR DAC [11].

On the other hand, multi-bit ΣΔM ADCs are useful to keep the modulator order and the sampling rate in moderate levels. It improves the stability of the loop filter and it reduces the jitter induced noise. The most important drawback of the multi-bit implementations is the nonlinearity of the feedback DACs due to the unit element mismatches. This issue can be circumvented by using dynamic-element matching (DEM) techniques or calibration.

4.2.4 DAC Pulse Shape

The DAC pulse shape choice is an important step for CT ΣΔMs unlike the DT counterparts. In DT ΣΔM, the feedback is based on the charge transfer operation and the total transferred charge at the end of the cycle is the important parameter. Therefore, DT ΣΔM dominantly use the switched-capacitor (SC) DACs which approximates

the impulse. In CT ΣΔMs, the feedback charge is integrated over time. The shape of the DAC determines the loop filter parameters and has impact on the characteristics of the CT ΣΔM ADC such as jitter tolerance and operational transconductance amplifier (OTA) linearity. Both the temporal and amplitude nonidealities degrade the performance of the CT ΣΔM ADCs.

Rectangular pulse shapes are commonly used in CT ΣΔM ADCs since they can be easily implemented by switched resistor or switched current. The main disadvantage of the rectangular pulse shapes is their jitter penalty. switched-capacitor or switched-capacitor resistor (SCR) DACs can be used to increase the jitter immunity. However, large pulses of current seen in the SC and SCR DACs can be problematic for the integrators' linearity and may cause interference problems for the receiver applications. Moreover, it has been demonstrated in [12] that the anti-aliasing feature of the modulator is degraded when the SC and SCR DACs are used. There are several other examples of "shaped" DAC pulses against the jitter problem such as sine-shaped DAC. However, these DACs require additional hardware for the implementation.

4.2.5 Excess Loop Delay

In an ideal CT ΣΔM, there is no delay between the quantizer clock and DAC outputs. However, in practice, both quantizer and DAC have delay. This delay between the quantizer clock and the DAC output is called "excess loop delay" (ELD). DT ΣΔMs virtually insensitive to ELD whereas for CT modulators it may have serious effects.

For the non-return-to-zero (NRZ) DACs, the non-zero delay pushes the DAC pulse into the next cycle. As stated in [13], this increases the modulator order by one. Depending on the amount of delay, the maximum stable amplitude (MSA) reduces considerably, and for large inputs, the modulator may go into the instability. For the high speed CT ΣΔM ADCs the problem is more serious since the delay may constitute a large portion of the period. The mitigation or compensation of the ELD is crucial for the CT ΣΔM ADCs.

The mitigation of the ELD effects can be done by coefficients tuning or reducing the out-of-band (OOB) gain of the NTF [13]. Another approach is using the DAC waveform shapes with less sensitivity to ELD, such as return-to-zero (RZ) or exponentially decaying (e.g. SC DAC and SCR DAC).

For high-speed modulators the ELD takes a large portion of a period and mitigation techniques may not be effective. For these modulators ELD compensation techniques are adopted. A commonly used ELD compensation technique is achieved by introducing an additional feedback path at the input of the quantizer [14]. This path adds another degree of freedom for the control of the increased modulator order. With this compensation technique, the modulator can be compensated for the ELD up to one-period. The disadvantage of this approach is an additional DAC and a summing node at the input of the quantizer. Nevertheless, the technique offers a robust compensation [15] and it is commonly used. A variant of the method

which eliminates the need for the summing node is the ELD compensation using a digital differentiator. The compensation DAC is ported to the input of the last integrator, which exploits the virtual ground of the integrator. In [13], the method is implemented with the combination of half-return-to-zero (HRZ) and NRZ DACs, whereas in [16] a more simple implementation which uses only NRZ DACs was proposed.

4.2.6 Jitter

The statistical variation of the sampling frequency is called "clock jitter" and it depends on the impurity of the sampling clock [17]. In CT ΣΔM ADCs, the sampling jitter is effective on two clocked elements: the quantizer sampling clock and the DAC. The effect of jitter on the quantizer is negligible since it is shaped by the NTF. However, the effect of the jitter on the feedback DAC is a serious issue in CT ΣΔMs. The transferred charge to the integrator is modulated by the jitter at the pulse edges of the DAC. The DAC input contains the input and the quantization noise, therefore the jitter induced noise for a CT ΣΔM includes the input signal and quantization noise contents. For the white noise jitter approximation, the in-band noise due to jitter can be expressed as [18]:

$$J = \frac{\sigma^2_{\Delta T_s}}{T_s^2} \frac{\sigma^2_{lsb}}{\pi OSR} \int_0^{\pi} \left|(1-e^{-j\omega})NTF(e^{j\omega})\right|^2 d\omega \tag{4.1}$$

where $\sigma^2_{\Delta T_s}$ is the variance of the clock jitter, T_s is the sampling time, σ^2_{lsb} is the variance of the quantization noise and OSR is the over-sampling ratio of the modulator.

Equation 4.1 shows that the in-band jitter noise is proportional to the area under the $\left|(1-e^{-j\omega})NTF(e^{j\omega})\right|^2$ curve. NTF is small within the band, therefore the in-band jitter noise is closely related to the OOB behavior of the NTF. This term can be reduced by reducing the OOB gain of the NTF or employing an optimized NTF shape as proposed in [19]. The variance of the quantization noise σ^2_{lsb} is proportional to the quantizer step-size. Therefore, multi-bit quantizers give better jitter tolerance compared to the single-bit quantizers. Equation 4.1 also shows that the in-band component of the jitter can be reduced by increasing the OSR.

4.2.7 Circuit Noise

Apart from the quantization noise and the jitter induced noise, the achievable signal-to-noise ratio (SNR) is limited by the thermal noise of the transistors and the resistors. As seen in the other effects, the closer the noise source to the ADC input, the more it has impact. Therefore, the noise of the input resistor, of the first integrator

and of the first DAC are the most critical among the thermal noise sources in the ADC and the allowed noise from the following stages can be relaxed to scale down the current consumption. The quantization noise may include harmonics and may increase due to various effects such as excess loop delay. Therefore, in practice the thermal noise occupies much larger part than the quantization noise on the overall noise budget [9].

4.3 40 MHz BW, 70 dB SNDR CT ΣΔM ADC in 28nm FD-SOI CMOS

4.3.1 Overview of the ADC

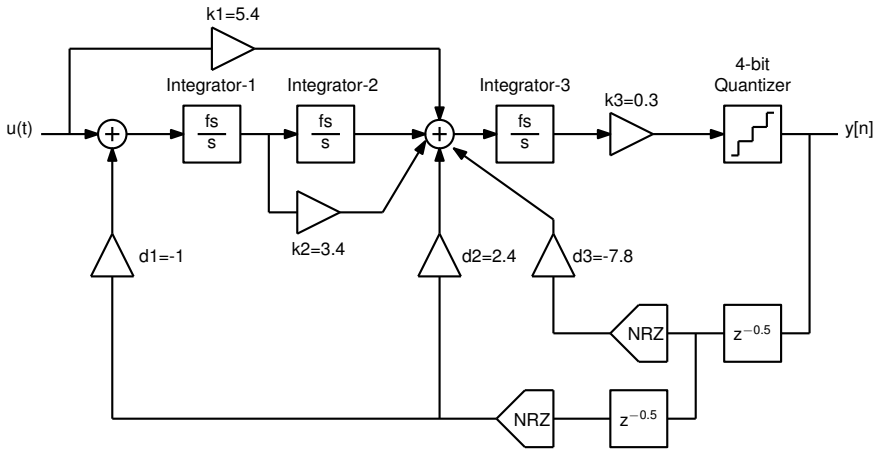

Fig. 4.8 Block diagram of the modulator employed in this work.

The block diagram of the third-order CIFF-B CT modulator with 4-bit quantizer employed in this work is depicted in Fig. 4.8 and the schematic diagram of the ADC is given in Fig. 4.9. As discussed in Section 4.2.2, the feedforward-feedback combination offers several advantages regarding the given specifications in this work. The NTF and STF of the modulator is shown in Fig. 4.10. The NTF is synthesized using the ΔΣ Toolbox by R. Schreier [20], without optimized zeros since for the given OSR and 4-bit quantizer the quantization-noise is low enough for the specifications. Out-of-band gain of the NTF is equal to 4 to reduce the effects of the jitter and improve the stability of the modulator as well as to have enough suppression for the nonlinearity and the noise of the DAC2 and DAC3. The modulator is compensated for a whole period of ELD to give enough time for the data-weighted-averaging

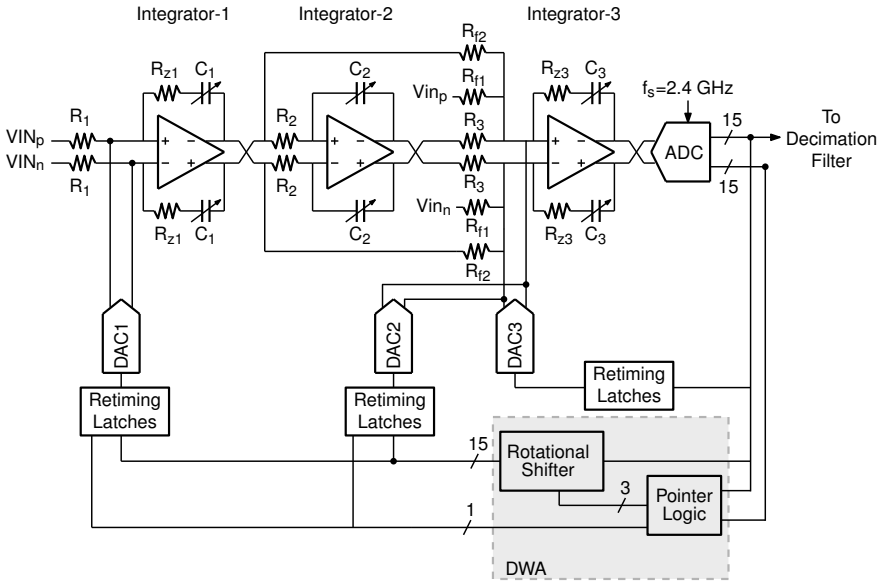

Fig. 4.9 Schematic of the ADC.

(DWA) block. ELD compensation with digital differentiation is used to eliminate the summing node. d_2 and d_3 implement the combined ELD feedback and the loop-filter feedback. The simulated SQNR as a function of the input signal amplitude for the synthesized NTF is shown in Fig. 4.11, the MSA of the modulator is -1 dB and the DR is 101.5 dB.

The input feedforward path k_1 is added to reduce the voltage swing at the output of the Integrator-3. This increases the STF peaking and the peaking is 16 dB around $0.3\,f_s$. The block diagram of the receiver FM chain is depicted in Fig. 4.12. A transimpedance amplifier (TIA) precedes the ADC and filters the input, therewith the STF peaking is reduced. Fig. 4.13 shows the transfer functions of the TIA and filtered STF. The TIA is modeled by two poles at 50 MHz, according to the specifications of the receiver. As can be seen from the figure, the peaking is reduced to the negligible levels.

R_{z1} and R_{z3} in Fig. 4.9 are used to cancel the right-half-plane zero for the Integrator-1 and the Integrator-3 respectively. All the integrating capacitors are tunable as a countermeasure for the RC time-constant variations due to the process spread. Feed-forward paths k_1 and k_2 are implemented with resistors R_{f1} and R_{f2} respectively. The feed-forward resistors are not tunable as the simulations have shown that by tuning only C_3 the RC time-constants remain in the safe range and the stability is not jeopardized. DWA is applied to DAC1 and DAC2 to improve their linearity.

The input resistance R_1 of the modulator is chosen to achieve 80 dB SNR with -6 dBFS input and it is equal to 400 Ω. Then the nominal unit current of the DAC1 becomes equal to 83.3 μA and the integrating capacitor C_1 becomes equal to 1 pF.

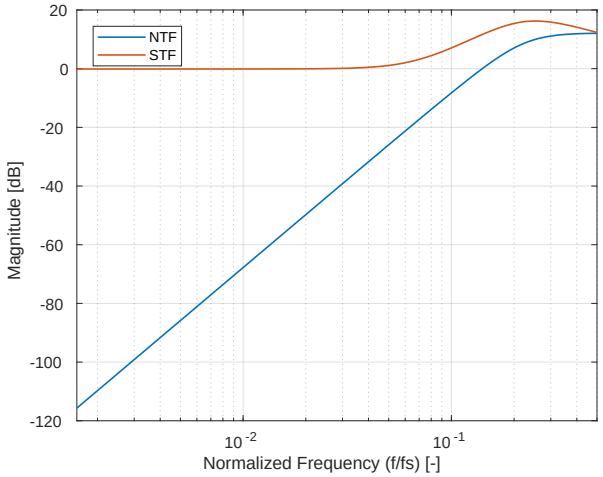

Fig. 4.10 NTF and STF of the CT modulator used in this work.

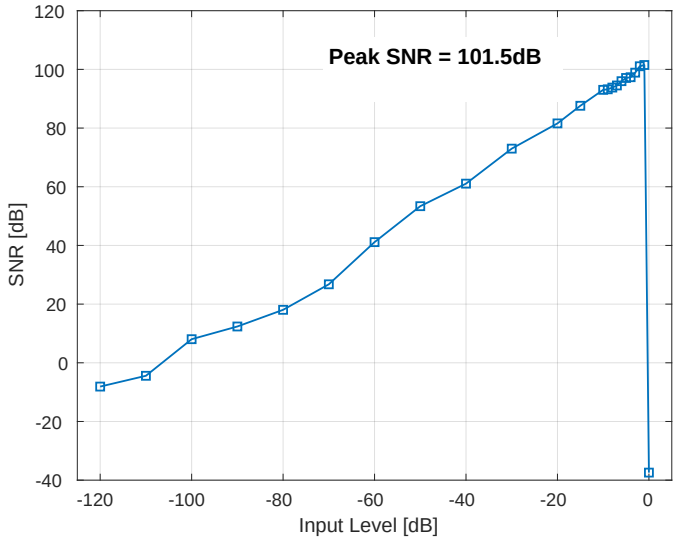

Fig. 4.11 SQNR as a function input amplitude.

The input resistors of the Integrator-2 and Integrator-3 are scaled by 5. Therefore, both R_2 and R_3 are equal to 2 k Ω and, C_2 and C_3 are equal to 200 fF. The unit current of the DAC3 is equal to 37.5 μA and of the DAC2 is equal to 12.5 μA.

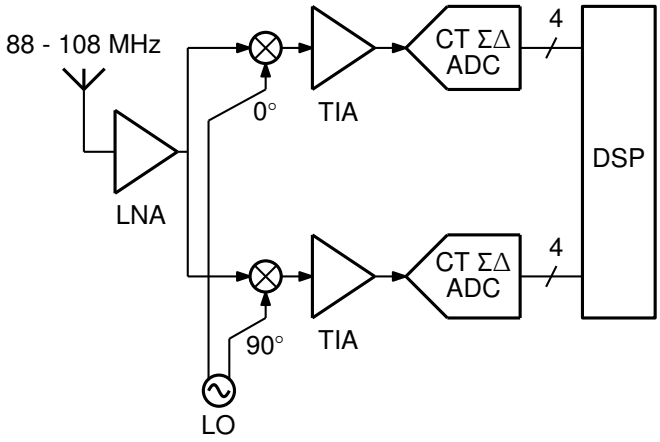

Fig. 4.12 Block diagram of the FM chain.

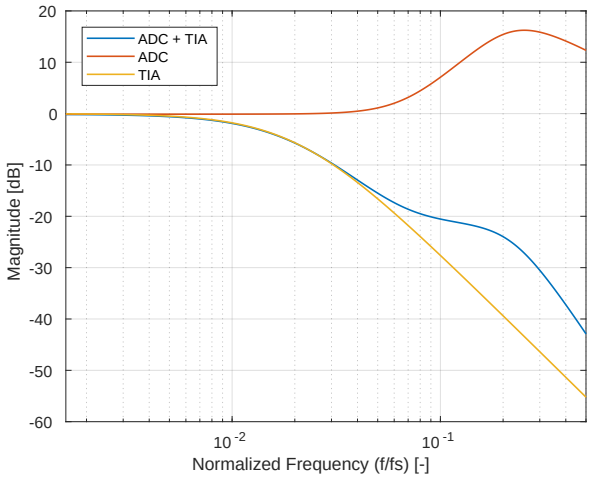

Fig. 4.13 Simulated STFs for ADC, TIA and TIA and ADC cascade.

4.3.2 Integrators

Common implementations of the CT integrators for CT ΣΔM ADCs are active-RC and Gm-C structures. Active-RC integrators are closed-loop therefore have improved linearity. However, the feedback reduces the open-loop bandwidth of the amplifiers, therefore limiting its speed. On the other hand, the Gm-C integrator is open-loop and it is fast. Gm-C integrators suffer from the non-linearity of the Gm

block, which can be fairly high [21]. Since the linearity is one of the concerns in this work, all the integrators in the ADC are active-RC integrator type.

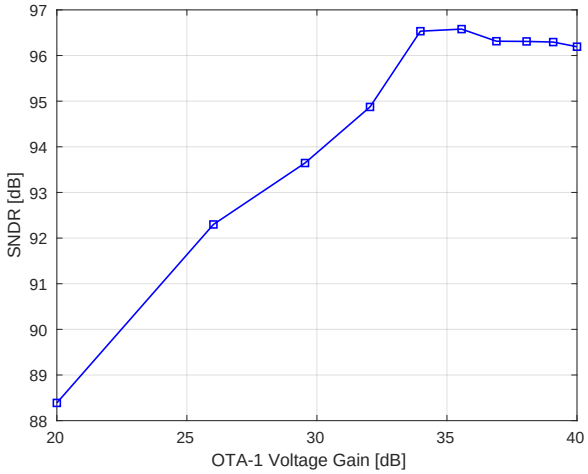

Fig. 4.14 SNDR as a function of DC voltage gain of the OTA-1.

The amplifier in the active-RC integrator can be an opamp or an OTA. Maintaining low the output impedance in opamps limits the output swing of the amplifier. The OTA has high output impedance. However, low output impedance is obtained by strong negative feedback [9]. Morever, it has almost rail-to-rail swing and hence it is used in the integrators of this work.

Three specifications are of concern in the OTA to be used in the integrators, namely the DC gain (A_v), the gain-bandwidth product (GBW) and the nonlinearity. In DT ΣΔMs, the finite DC gain of the integrator causes lossy integrators, which changes the location of the NTF zeros and reduces the noise shaping. An analogous issue is encountered in the CT ΣΔMs. Fig. 4.14 shows the results for the DC gain sweep of the first integrator. The DC gain of the OTA should be higher than 35 dB to have no SNR loss.

The finite GBW of the OTA creates a gain error and additional poles in the integrator transfer function [22]. The former shifts the pole locations as seen in the finite DC gain case whereas the latter causes excess loop delay. Both have a detrimental effect on the noise-shaping and the stability of the modulator. The finite GBW of the OTA can be modeled by a simple 1-pole model [22] for the OTAs with large phase margin or a more complex model [23] which takes into account the elements such as zero-nulling resistor and input capacitance of the OTA. Fig. 4.15 shows the SNDR as a function of the GBW for OTA-1 and OTA-3. GBW of the OTA-1 does not affect SNDR for values equal to $0.5\,f_s$. On the other hand, the GBW of OTA-3 is critical for SNDR and a GBW greater than $2\,f_s$ is required. In addition to GBW related SNDR loss, there is additional loss due to the resistive paths at the input of the

Integrator-3. However, this loss is not significant since the overall SNR is thermal noise limited.

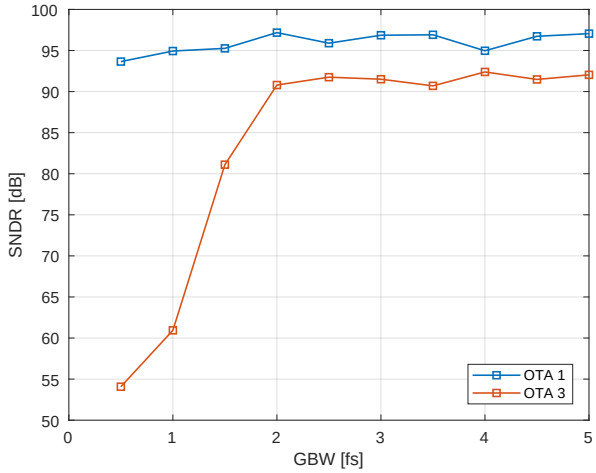

Fig. 4.15 SNDR as a function of GBW for the OTA-1 and OTA-3.

The nonlinearity of the OTA has different effects in single-bit and multi-bit modulators. It causes harmonic-distortion for single-bit CT ΣΔMs [24], whereas for multi-bit modulators it increases the in-band noise, as it mixes down the out of band quantization noise into the band [25]. To see the effects of the first OTA nonlinearity on the ADC, a parameter β which models the nonlinearity of an active-RC integrator is used [25]. β is given in [26] by:

$$\beta = \frac{2\,g_3}{g_m(g_m R)^3} \tag{4.2}$$

where g_m is the OTA transconductance, g_3 is the third-order nonlinearity of the OTA transconductor and R is the input resistance of the integrator. Fig. 4.16 shows the SNDR and SFDR of the ADC as a function of β.

The integrators use two-stage feed-forward compensated OTAs. The feed-forward compensated OTAs [27–29] have become very popular for high-speed CT ΣΔM ADCs in literature. Unlike the Miller OTAs, the compensation is done without a compensation capacitor therefore without the pole-splitting. This increases the achievable bandwidth considerably, compared to the Miller OTA with the same power consumption. The drawback of the feed-forward compensation OTAs are the pole-zero doublets which degrade their settling behavior. However, in CT ΣΔM ADCs, the settling is irrelevant and feed-forward OTAs perform well in the high-speed CT ΣΔM ADCs where they help to achieve good power efficiency.

Fig. 4.17 shows the schematic and transconductance block diagram of the two-stage feed-forward compensated OTA used in this work. The first stage of the OTA

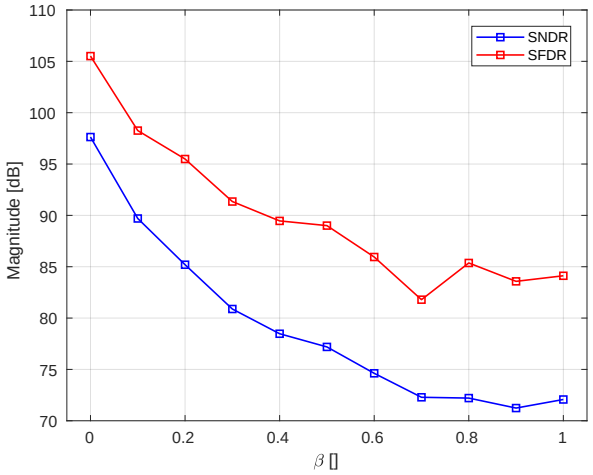

Fig. 4.16 SNDR & SFDR as a function of OTA-1 third-order nonlinearity β.

is a differential pair with active load. M_3 and M_2 implement the Gm_1 of the slow-path. The second stage implements the Gm_2 of the slow-path and Gm_3 of the fast-path. M_6 implements the Gm_2. Gm_3 is composed of two paths (for each output), namely M_8 and M_{10} to re-use the biasing current. M_8 is directly connected to the input and the latter is AC coupled. AC coupling is used to allocate the required headroom for the common-mode feedback transistor M_{12}. First and second stages have separate common-mode feedback (CMFB) networks. The first stage CMFB is a single-stage structure whereas the second stage has a two-stage structure. The post-layout Bode Plot for the output of the OTA is shown in Fig. 4.18 for $C_{load} = 1\ pF$. The GBW is 7.2 GHz and the phase-margin (PM) is 89.95 degrees. Integrator-2 and Integrator-3 use the same OTA without any current scaling. The in-band integrated input referred noise of the OTA is 320.8 pV^2 and the third-order nonlinearity HD_3 of the Integrator-1 is equal to -67 dBc.

The RC time-constant variations due to the process spread may become large and cause SNR degradation or instability in CT ΣΔMs. To maintain a robust operation, the RC time-constant of the integrators should be tuned. Fig. 4.19 shows the effect of the RC time-constant variation on the SNR for the modulator in this work. 3-bit manually controlled capacitor tuning networks to cover ±14% are used to compensate for the process shifts on the RC time constant of the integrators. The feedback capacitor of the first integrator is 1 pF whereas the second and third feedback capacitors are 200 fF. To have more reliable unit capacitors due to the smaller unit capacitor size for the second and third integrators, the capacitors are connected in series to obtain a smaller capacitance. The schematic of the tuning network for Integrator-1 is depicted in Fig. 4.20(a) whereas the tuning network for the second and third integrators is shown in Fig. 4.20(b).

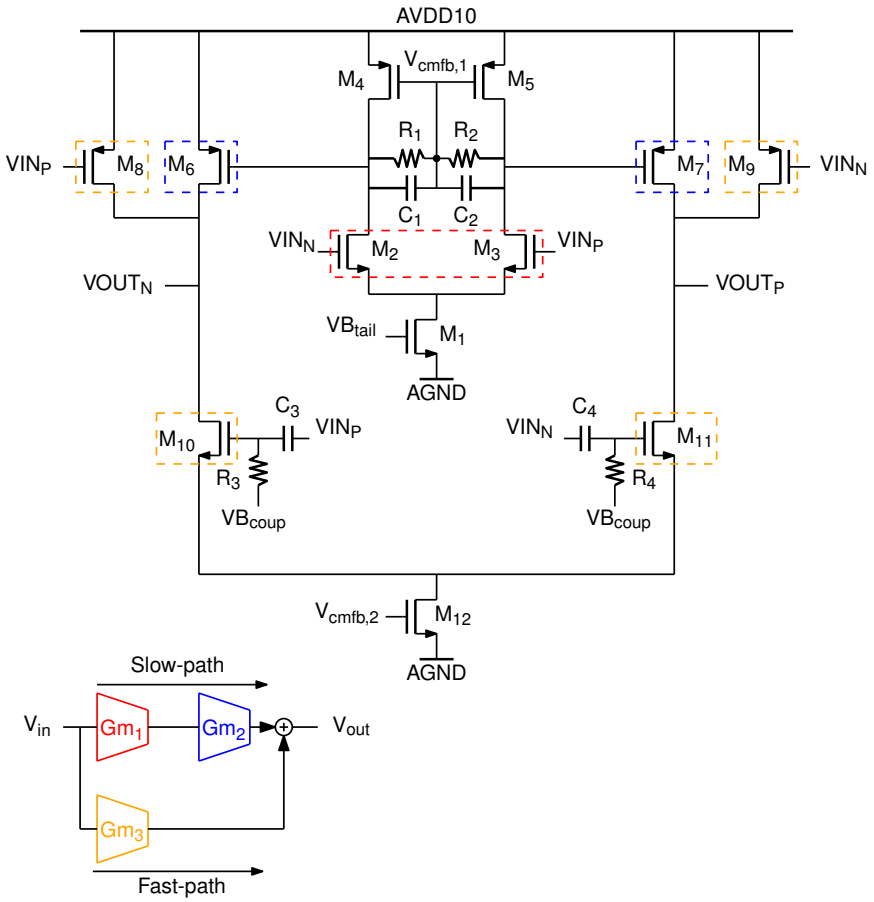

Fig. 4.17 Two-stage feed-forward compensated OTA.

4.3.3 Flash ADC

The quantizer speed is especially important in high-speed ΣΔM ADCs due to the limited decision time. For the modulator used in this work, the quantizer has approximately a quarter of the period considering the ELD compensation DAC delay. Flash ADCs are dominantly used in the ΣΔM ADCs with multi-GHz sampling rates for their superior speed and moderate complexity in low resolutions.

Quantizer takes place at the output of the loop-filter and its errors are shaped by the complete NTF. However, even with the relaxed element accuracy requirements, the offset of the comparators can be important especially for the linearity critical applications such as the one in this work. Figg. 4.21 and 4.22 show the simulated standard deviation of the comparator offset versus SNDR and THD respectively. Note that the THD decreases by 5 dBc when the offset standard deviation goes from

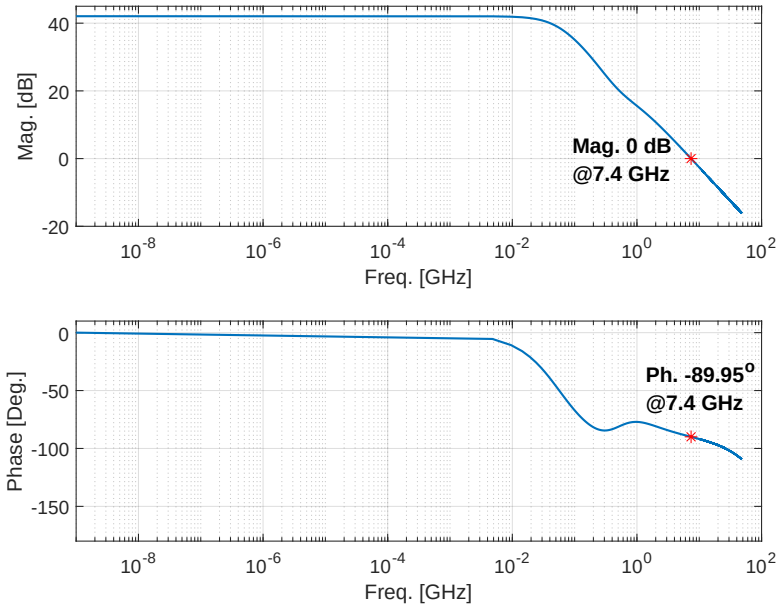

Fig. 4.18 Bode plot of the post-layout OTA (for $C_{load} = 1\ pF$).

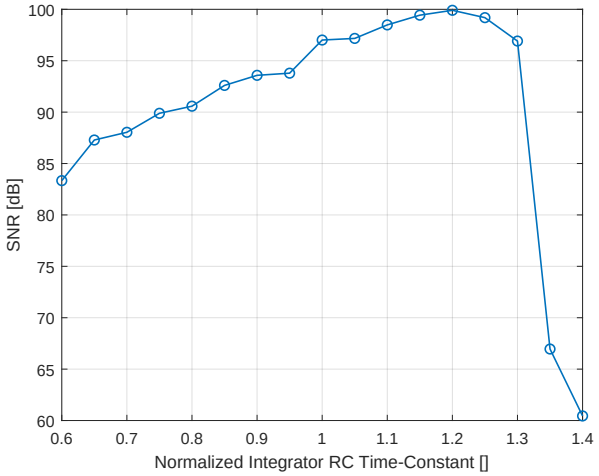

Fig. 4.19 SNR as a function of integrator RC time-constant.

0.1 LSB to 0.2 LSB while the SNDR decreases by 2.5 dB. Therefore, considering the stringent THD requirements, the comparators of the quantizer are designed for 0.1 LSB of offset standard deviation.

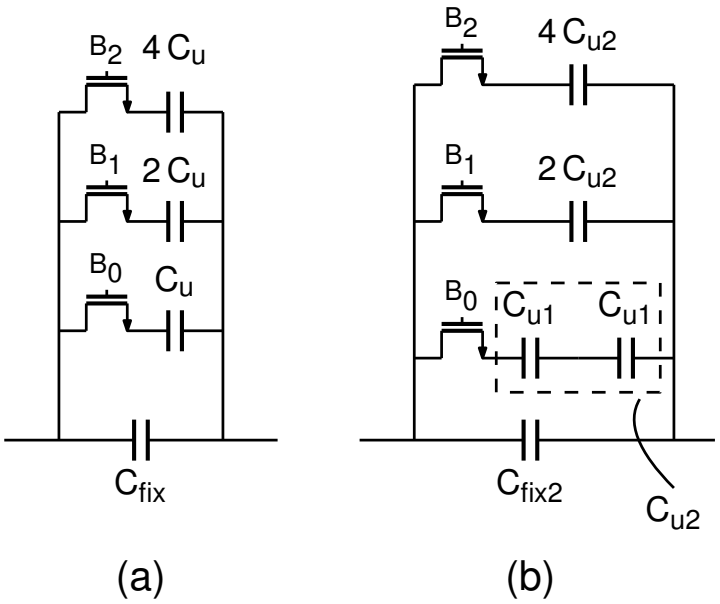

Fig. 4.20 Capacitor tuning bank of the Integrator 1 (a), Integrator 2 and 3 (b).

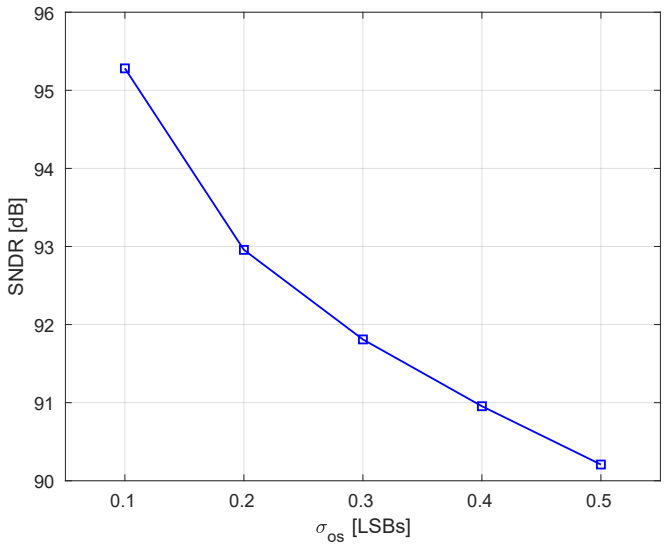

Fig. 4.21 SNDR as a function of the comparator offset standard deviation σ_{os}.

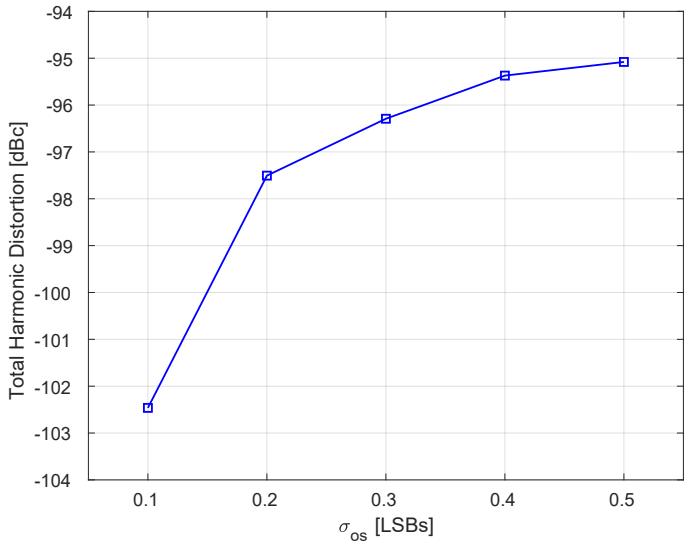

Fig. 4.22 THD as a function of the comparator offset standard deviation σ_{os}.

The flash ADC is composed of 15 three-stage comparators and a resistor string for reference voltage generation. The voltage swing at the input of the flash ADC is scaled by 2 in the modulator and the resistor string generates the voltage references between 750 mV and 250 mV. The three-stage comparator is depicted in Fig. 4.23 and it is composed of a 4-input preamplifier, a Strong-ARM latch and an SR Latch. The preamp reduces the input referred offset of the following latch stages and reduces the kickback noise due to the switching activity of the ARM Latch. The clocked ARM latch latches the output of the preamplifier with high gain. SR Latch is added to hold the output of the comparator for the whole period since Latch-1 gets reset in every cycle. Both of the outputs of comparator are utilized to reduce the total load at one input. The symmetric SR latch architecture proposed in [30] generates Q and $\overline{Q}$ at the same time, therefore it is beneficial for optimizing the feedback timings, since both of the outputs are utilized.

The input referred offset standard deviation σ_{os} of the comparators is 2 mV and the whole flash-ADC consumes 15 mA from 1 V supply.

4.3.4 Feedback DACs

Feedback DACs can be considered among the most critical blocks of a CT ΣΔM ADC. The noise and linearity of the outer feedback DAC is not shaped by the loop, therefore its accuracy and noise should be in the order of the overall ADC resolution.

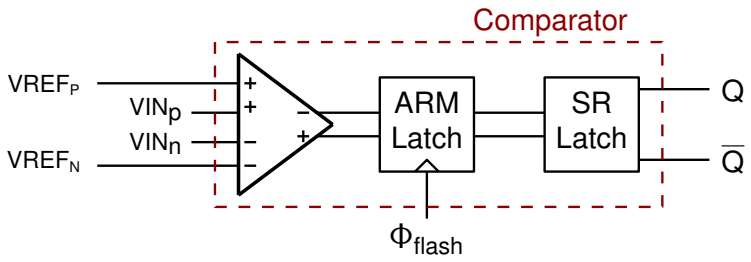

Fig. 4.23 Three-stage comparator used in flash-ADC quantizer.

Figg. 4.24 and 4.25 show SNDR and THD, respectively, of the ADC as a function of the DAC1 unit element mismatch standard deviation $\sigma_{mismatch,DAC1}$. DAC mismatch is a serious limitation in achieving the given specifications for the case without DWA. Figg. 4.24 and 4.25 demonstrate that even employing the DWA, DAC1 unit element mismatch standard deviation should be lower than 0.4% to achieve the given THD specification.

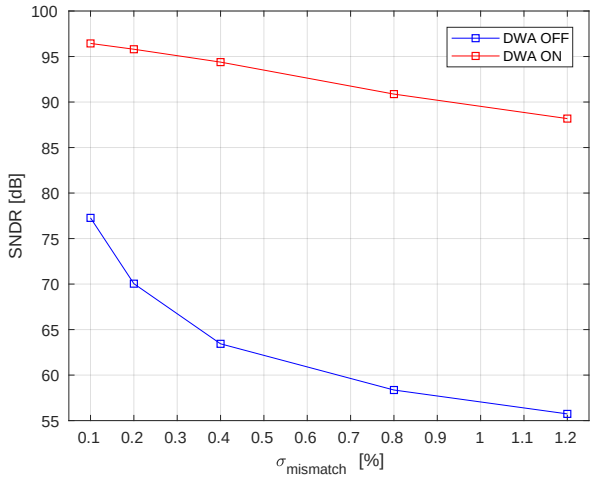

Fig. 4.24 SNDR of the ADC as a function of $\sigma_{mismatch,DAC1}$.

As discussed previously, the NRZ DAC is advantageous over the RZ DAC in terms of jitter immunity and SC DAC in terms of the integrator linearity. Therefore, NRZ DACs are used for all the feedback DACs in this work. The NRZ DAC pulse shape can be implemented using switched resistors or switched currents. Switched resistor has very small thermal noise and its simple structure eases the layout. However, the resistors of the DAC load the virtual ground of the OTA, which reduces the integrator closed-loop gain [9]. This degrades the linearity of the integrator and

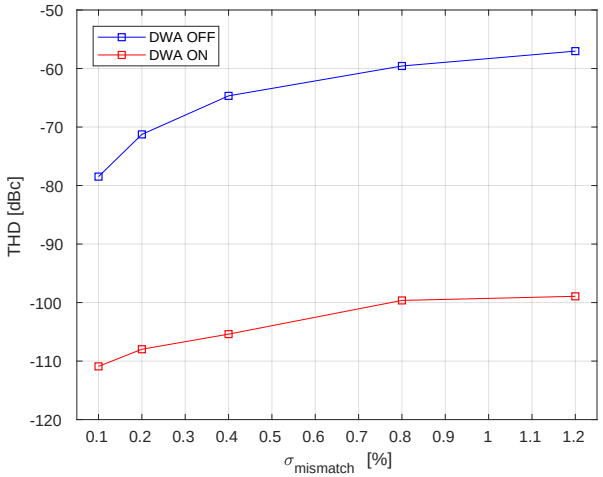

Fig. 4.25 THD of the ADC as a function of $\sigma_{mismatch,DAC1}$.

increases the contribution of the OTA noise. Moreover, the reference voltage noise of the switched resistor appears directly at the DAC input and it is cumbersome to filter the reference noise [9].

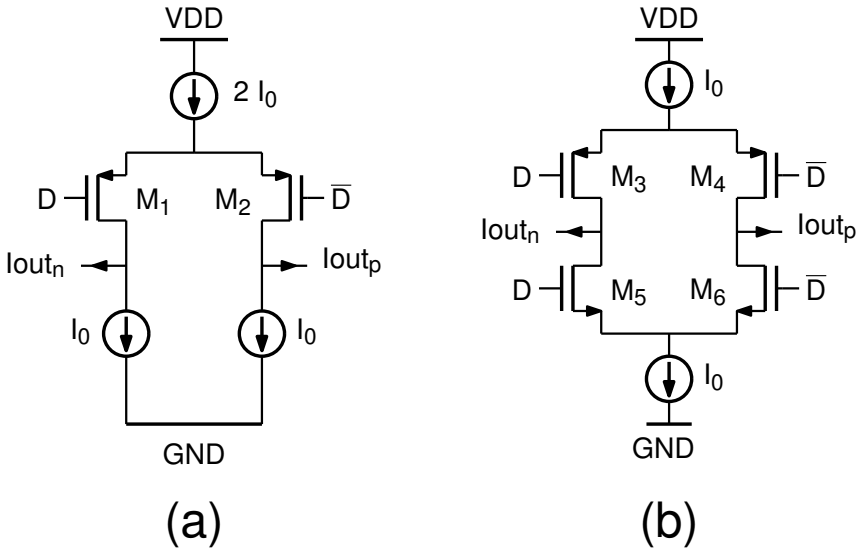

Fig. 4.26 Current-steering DAC Cells.

Current-steering (CS) DACs are inferior to the switched resistor DACs in terms of noise [9]. However, they have few advantages over the resistive DACs which make them appealing for this work. First, the CS DAC does not load the virtual ground of the integrators at low frequencies. Therefore, it achieves better integrator linearity and the OTA noise contribution is lower. Second, the CS DAC reference voltages are connected to the gate of the bias transistors which makes the filtering the reference noise straightforward.

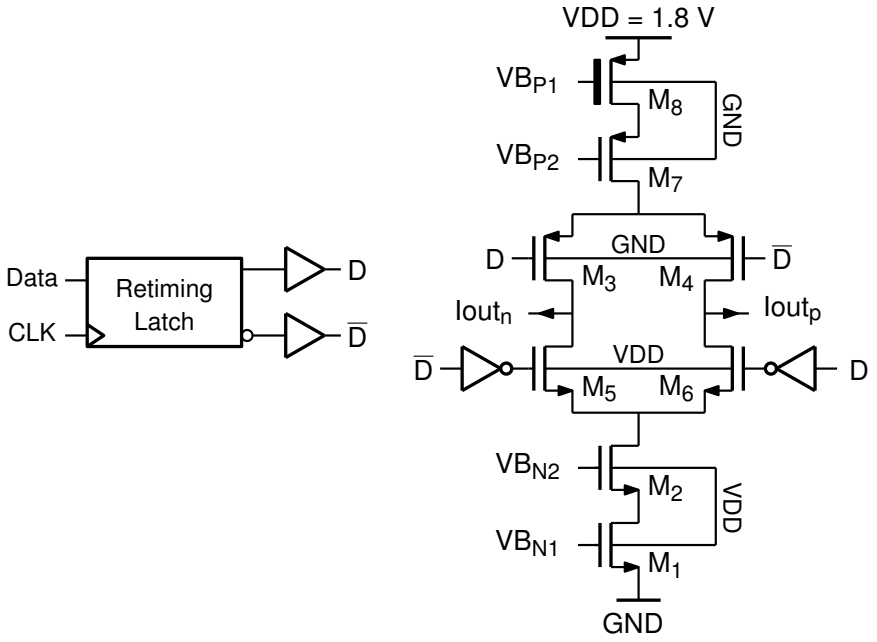

Fig. 4.27 Schematic of the Complementary DAC Cell.

Commonly used CS DAC cells are shown in Fig. 4.26. The basic CS DAC cell (for PMOS implementation) is shown in Fig. 4.26(a) and it is composed of two PMOS switches and 3 current sources. One of the output currents is generated by subtracting the currents. The cell uses $4I_0$ to generate $2I_0$ differential output current. On the other hand, complementary CS DAC cell [31] shown in Fig. 4.26(b) requires half the current for the same differential output current. Moreover, the complementary CS DAC cell introduces less thermal noise compared to the basic CS DAC cell, as it has only two current sources connected to output. Drawbacks of the complementary CS DAC cell is the headroom issue [6] and the data signals. The cell has a pair of PMOS switches and a pair of NMOS switches and even if they are controlled by the same data and the complement of the data, the crossing points are different for the pairs.

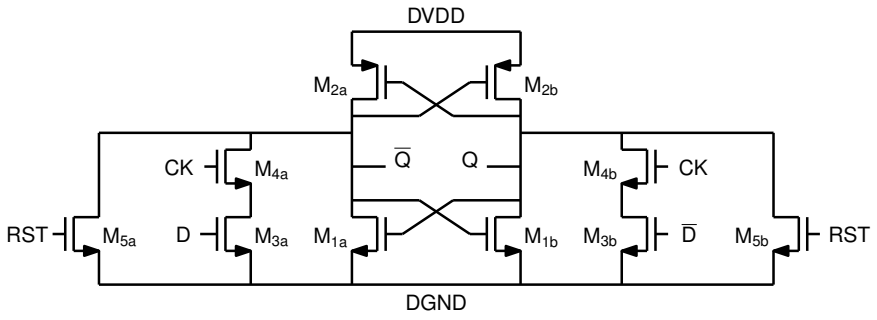

Fig. 4.28 Driver Latch of the DAC3.

The complementary current-steering DAC cell used in this design is depicted in Fig. 4.27. 1.8 V supply is used to reduce the noise and improve the matching of the PMOS current source transistor M_8. For improved reliability with the 1.8 V supply M_8 is a thick oxide flipped-well PMOS. The rest of the current-steering cell is composed of the thin oxide flipped-well transistors. Current source transistors M_8 and M_1 are sized to obtain the required matching. Cascode transistors M_2 and M_7 are added to increase the output impedance and isolate the common source node of the switch transistors from the large capacitance posed by the current source transistors to mitigate the nonlinearity of the cell [32]. All of the transistors in the cell use forward-body-biasing to reduce the threshold voltage of the transistors and relax the headroom issues. The mirror factor of the biasing is kept below 1 to reduce the noise contribution of the bias network and the reference. The cell is driven by a single retiming latch with small clock-to-Q delay, which is shown in Fig. 4.28 for DAC3 and Fig. 4.29 for DAC1 and DAC2. As will be explained shortly, the only difference of the DAC1 and DAC2 driver latches from the one of the DAC3 is the embedded input data multiplexer. The driver latch generates its outputs with low-crossing point. The high-crossing signals for NMOS switch pair is locally generated with a pair of inverters as shown in Fig. 4.27.

4.3.5 DWA and Novel Rotational Shifter Structure

DAC nonlinearity due to mismatch is an important limiting factor in the design of the converter. An effective way to deal with the DAC element mismatch without knowing the actual values of the errors is the DEM techniques [8]. DWA [33] is a widely used DEM algorithm, in which errors due to the mismatch is averaged and first-order shaped. Therefore, the technique not only spreads the spurs over the frequency but also improves the SNR of the converter in case of element mismatch. Fig. 4.30 shows the implementation of the algorithm. It is based on two main operations, namely the pointer logic and the rotational shifting. The pointer logic cal-

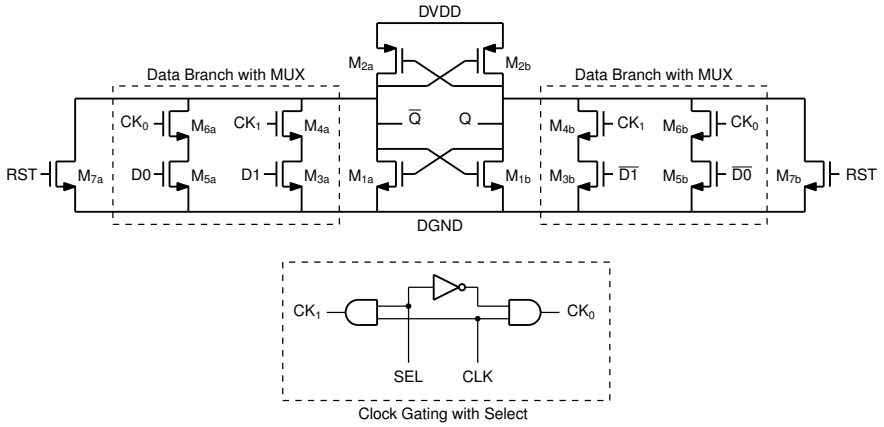

Fig. 4.29 DAC retiming latch with embedded 2-to-1 multiplexer.

culates the starting index of DAC elements based on the previous pointer value and the current quantizer output. This operation can be implemented to work out of the sigma-delta loop, therefore it is less critical in terms of timing [34]. For the cases where the pointer generation is the time limiting operation, techniques such as interleaved DWA [35] can be found in the literature. In this work, an RTL synthesized conventional pointer logic that complies with the timing requirements is used in the ADC.

On the other hand, the rotational shifting operation is the bottleneck of the DWA for high-speed ΣΔM ADCs as it is in the feedback loop of the ADC. A period of the ADC can be expressed as:

$$T_s = t_{quantizer} + t_{shift} + t_{dac} \tag{4.3}$$

where $t_{quantizer}$ is the time required for quantization, t_{shift} is the rotational shifter delay and t_{dac} is the DAC delay, which is composed of the driver latch regeneration time and the parasitic signal and DAC output delay. Commonly, the quantization

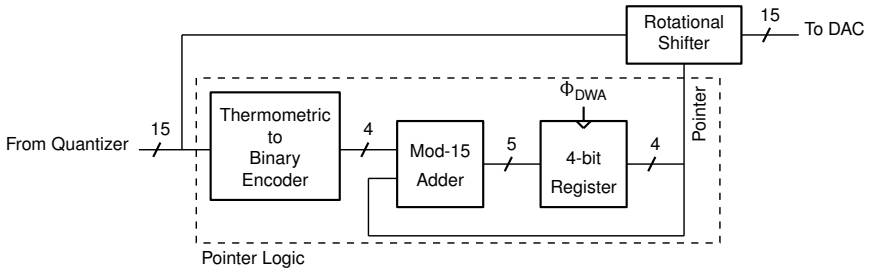

Fig. 4.30 Block diagram of a conventional DWA implementation.

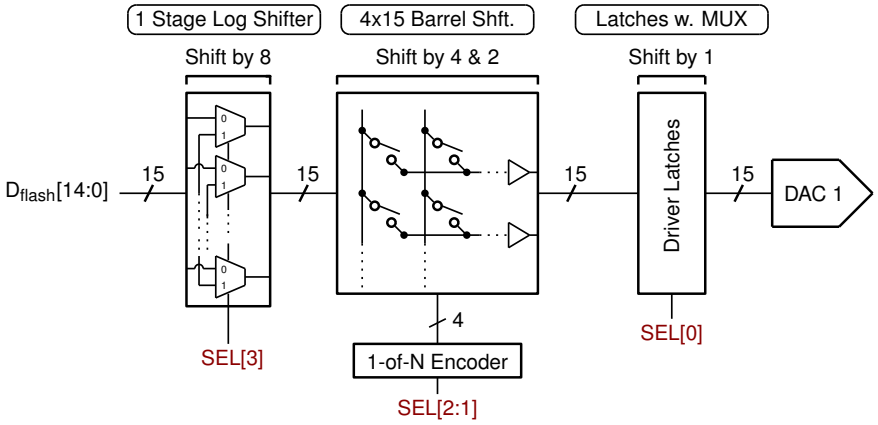

Fig. 4.31 Block diagram of the proposed rotational shifter.

takes half of the period which leaves half period for the rotational shifting and the DAC delay. For multi-GHz sampling rates this becomes an issue. For instance, in this work the time allowed for shifter and DAC is nominally equal to 208 ps.

The reference shuffling technique [36, 37] has been proposed to relax the element rotation logic timing. Instead of rotating the data between the quantizer and the DAC, the technique rotates the reference voltages of the comparators, thereby taking the rotation out of the critical path. The method is used in [38] for 1.4 GHz sampling rate. In [39] the Time-Interleaved Reference Data-Weighted-Averaging (TI-RDWA) has been introduced for a CT ΣΔM ADC working at 5 GS/s to overcome the reference voltage settling delay. However, as stated in [40], the drawback of the reference shuffling technique stems from being analog in nature. In the nano-scale technologies, working with gate voltages around the half-supply penalizes the settling of the switches considerably, which asks for large switches with more parasitic capacitances. Therefore, a digital solution is sought in this work.

Two types of rotational shifters are commonly used in DWA, namely the barrel shifter and the logarithmic shifter. The barrel shifter is a high-speed block, as it is a single-stage design. The number of transistors is $O(N^2)$ and the input capacitance is $O(N)$, where N is the word-length [41]. The word length is equal to the quantizer level in this application. For the 16 level quantizer used in this work, the number of switches would be $(N-1)^2 = 255$. The work presented in [40] uses a barrel shifter for 9 level quantizer. As indicated in the work, the shifter has 500 ps delay in 65 nm CMOS. There are three main issues with the barrel shifter. First, the pointer should be one-hot encoded which gives a delay penalty [41]. Second, as stated in [42], multiplexers with inputs more than 4-8 pose excessive parasitic capacitances. In [40], 8-to-1 multiplexers are used for 3-bit quantizer and a 4-bit quantizer would require 16 of the 16-to-1 multiplexers. Third, as stated above, the input capacitance of the barrel shifter linearly increases with the quantizer level, which may have

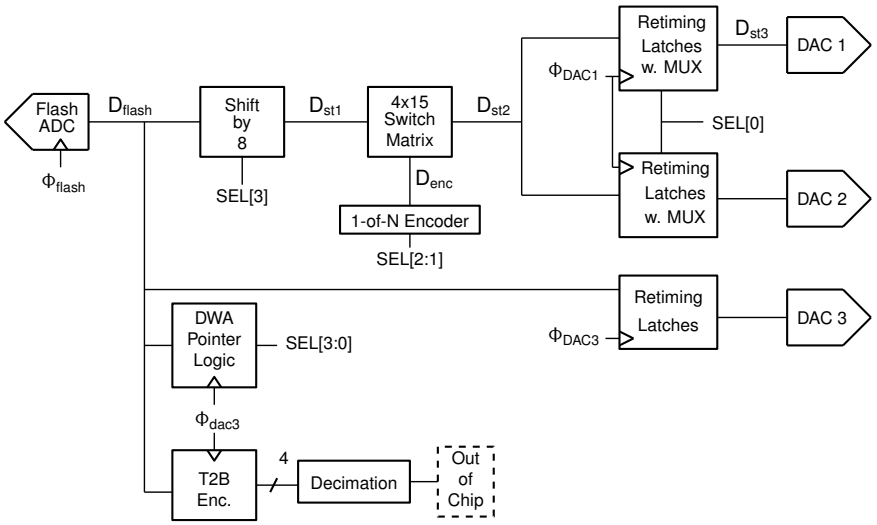

Fig. 4.32 Block diagram of the ADC feedback network.

negative effect on the delay of the preceding quantizer. The total delay of a barrel shifter can be expressed as:

$$t_{barrel} = t_{encoder} + t_{tg} + t_{buffer} \tag{4.4}$$

The logarithmic shifter uses a multi-stage approach for a trade-off between the mentioned drawbacks of the barrel shifter and total delay. It is commonly used in DWA implementations in the literature [34, 43]. The total number of transistors is $O(N\,log_2N)$ and the number of stages is equal to log_2N. The logarithmic shifter does not require an encoded select input and can use the pointer in binary form directly out of the pointer logic. Apart from the delay penalty of the multi-stage approach, another drawback of the logarithmic shifter is the doubling of the interconnect length from one stage to the next one, which would penalize the delay seriously in nano-scale technologies [41]. The delay of a logarithmic shifter can be expressed as:

$$t_{log} = log_2(N)\,t_{mux} \tag{4.5}$$

where t_{mux} is the delay of a 2-to-1 multiplexer and N is the number of quantizer levels.

The above discussions make clear that a fast and simple shifter structure is required to achieve the aimed sampling rate of 2.4 GHz while utilizing the DWA technique. This thesis introduces a novel multi-stage shifter structure which theoretically has delay of a barrel shifter while having less number of transistors and less input capacitance. Fig. 4.31 shows the block diagram of the shifter. The starting point of the structure is a barrel shifter as the speed of the shifter is the primary con-

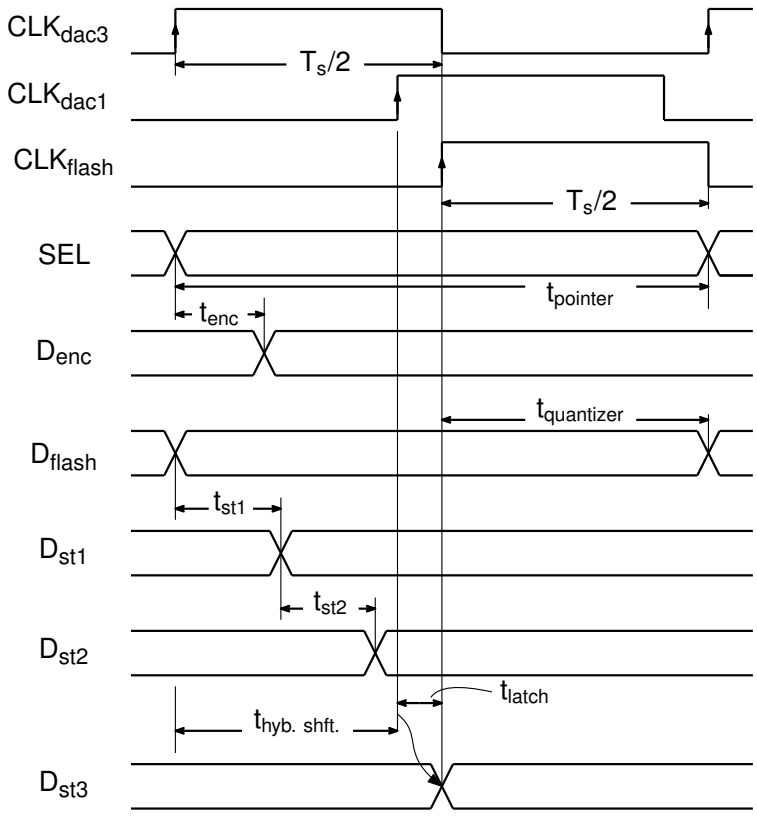

Fig. 4.33 Timing diagram of the ADC feedback network.

cern. Recalling that the input capacitor and the number of transistors are function of N, the barrel shifter can be optimized by reducing the N. Since $N = 2^b$, where b is the resolution of the quantizer, this means reducing the number of bits in the quantizer. However, this work uses a conventional loop-filter architecture and the resolution of the quantizer can not be reduced. Another way of reducing the N in the barrel shifter is performing only a part of the complete rotation. For instance, if the barrel shifter performs only shift steps by 1,2 and 4 instead of doing 1,2,4 and 8, the size of the shifter would be half. As discussed above, the encoder time is actually wasted as it adds to the delay of the shifter. Therefore, this work moves the shift-by-8 operation to be performed in parallel with the encoder to reduce the shifter size without increasing the delay. This stage can be implemented with 2-to-1 multiplexers, as in logarithmic shifters. As a result, the delay of the shifter remains equal to the delay of a barrel shifter while the number of switches in the barrel shifter halves. Including the number of switches added by the log shifter, the total number of switches becomes 180. This is equal to the 80% of a single stage barrel shifter. A side benefit of the modification is the reduction in the input capacitance

of the rotational shifter. This allows a better optimization of the whole rotational shifter delay using methods such as logical effort [44].

The size of the barrel shifter can be reduced further by removing another bit. The crucial point for a high-speed application is to keep the total delay constant. In this work, this is done by embedding the shift-by-1 operation in the DAC driver latch. The driver latch with embedded 2-to-1 multiplexer is shown in Fig. 4.29. The structure is based on the driver latch used for DAC3 (see Fig. 4.28). The data path of the latch is doubled to have the two inputs required for the multiplexer. The select function is embedded in the clock signal of the latch by gating the clock with a simple combinational logic. According to the value of the signal SEL, one of the data paths gets clocked and the selected data is latched. Since one of the clock transistors always stays off, the output sees an additional load composed of the drain junction capacitance and gate-drain overlap capacitance. This has a negligible effect on the clock-to-Q delay of the latch as it adds only 3.2 ps at the schematic level. On the other hand, the delay of the clock gating logic is more significant and it is 21 ps. Recognizing that the select signal is expected to be ready at the beginning of the shifter operation, this delay can be eliminated by anticipating the clock by the delay of the clock gating logic. Therefore, with the proposed latch structure with embedded multiplexer, the shift-by-1 function can be implemented with negligible additional delay. The resulting delay $t_{hyb.shft.}$ of the proposed structure can be expressed as:

$$t_{hyb.shft.} = max\{t_{enc}, t_{st1}\} + t_{st2} \tag{4.6}$$

where t_{enc} is encoder delay, t_{st1} is the log. shifter stage delay, and t_{st2} is the delay of the switch matrix.

The feedback data path diagram of the ADC is depicted in Fig. 4.32 and its timing diagram is depicted in Fig. 4.33. The post-layout simulation results for the delays of the proposed structure is given in Table 4.1. From the table, it can be noted that the delay of the encoder and the first stage overlaps as explained above, therefore the time required for the encoder is utilized. The delay of the switch matrix is slightly lower than the first stage, mostly due to the delay of the buffers with a large load coming from the long data lines of the DAC inputs. The clock-to-Q delay t_{latch} of the DAC retiming latches (excluding the clock-gating delay) is 52 ps. The sum of $t_{hyb.shft.}$ and t_{latch} results in 194 ps which remains inside the allocated half-perriod equal to 208 ps.

Table 4.1 Post-layout delay values for the ADC feedback.

	Delay value
t_{enc}	80 ps
t_{st1}	74 ps
t_{st2}	62 ps
$t_{hyb.shft.}$	142 ps
t_{latch}	52 ps

4.3.6 Layout of the ADC and Post-layout Simulation Results

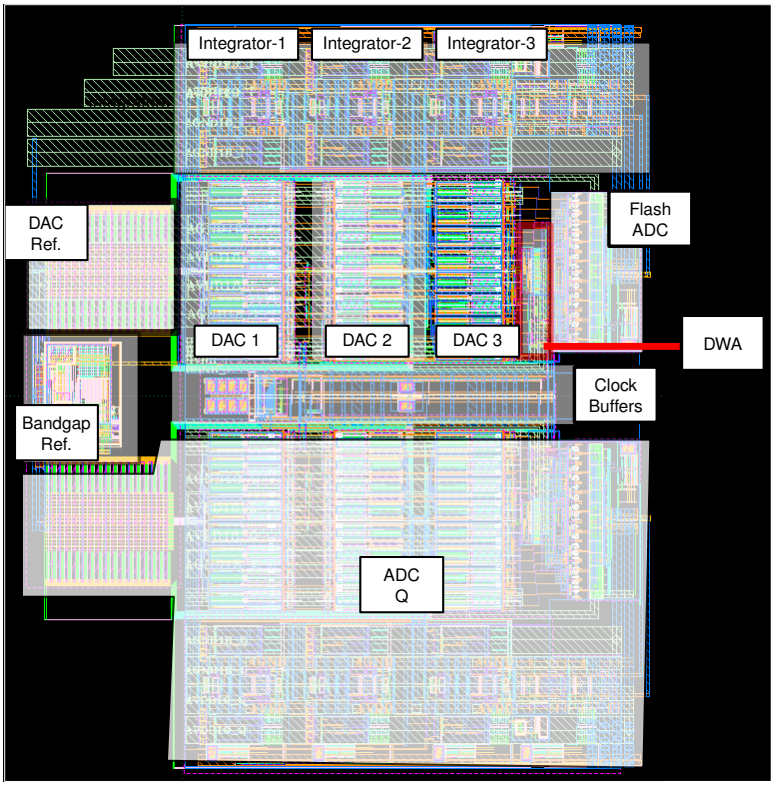

Fig. 4.34 Layout of the ADCs I & Q.

The ADC has been sent to fabrication in 28nm FD-SOI CMOS process from STMicroelectronics and the measurements are expected to start in early 2019. The layout of the I & Q ADCs is shown in Fig. 4.34. The ADCs are placed in a symmetric way and common blocks such as bandgap reference and clock buffers are placed between the two ADCs. The blocks of each ADC are placed to minimize the delay between the blocks. The loop is folded at the input of the flash ADC. In this way, the delay of the DWA and DAC3 paths is minimized, while the load of the Integrator-3 is increased. The loop delay due to the increased load capacitance of the Integrator-3 is less critical compared to the feedback path as the Integrator-3 has large margin in terms of GBW. Fig. 4.35 shows the layout of the test-chip. A decimation filter block and an SRAM memory were integrated on the same-chip with the ADC and they are indicated on the Fig. 4.35. The SRAM is added for fast data acquisition from the decimation input as well as from various taps along the decimation filter path for the testing purposes. The chip will be put in a BGA package.

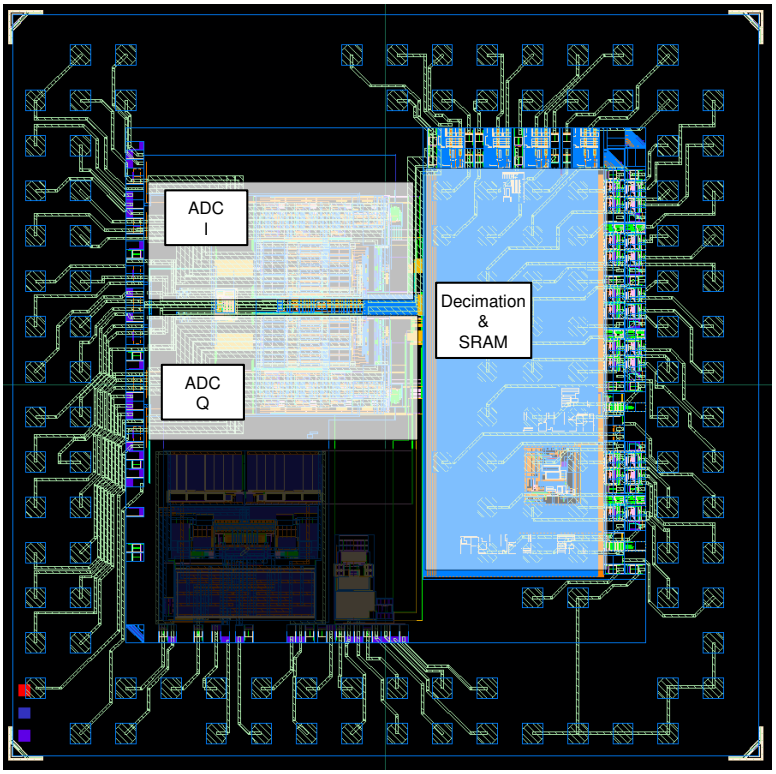

Fig. 4.35 Layout of the fabricated chip.

The simulated output spectrum of the ADC is given in Fig. 4.36(a) for f_{in} = $9.1MHz$ and input amplitude of $-6dBFS$. The obtained SNDR is 68.8 dB, when only the quantization noise is present. There is an out-of-band peaking which is due to the excess-loop delay due to the layout parasitics. Detailed in-band spectrum is shown in Fig. 4.36(b). HD_2 is equal to -76 dBc whereas the HD_3 is equal to -74 dBc. The large HD_2 is thought to be the result of Intersymbol Interference (ISI), in which the asymmetrical switching of the DAC cells are shown to generate even-order distortion components, even when the modulator is differential [46]. The THD of the ADC is -73.4 dBc.

Fig. 4.37 shows the post-layout noise distribution of the ADC for $f_{in} = 9.1MHz$, input amplitude of $-3dBFS$. The jitter induced noise is added using the white-noise jitter model (see Section 4.2.6) with the jitter standard-deviation $\sigma_j = 1ps$. DAC noise and the quantization noise are the most significant contributors. Large quantization noise stems from the parasitic excess loop delay, and the OOB quantization noise folded into the in-band due to the dynamic DAC errors. The noise contributions of the second and third integrator stages as well as DAC2 and DAC3 are found to be negligible. The ADC achieves 70.3 dB SNDR with the thermal noise and the

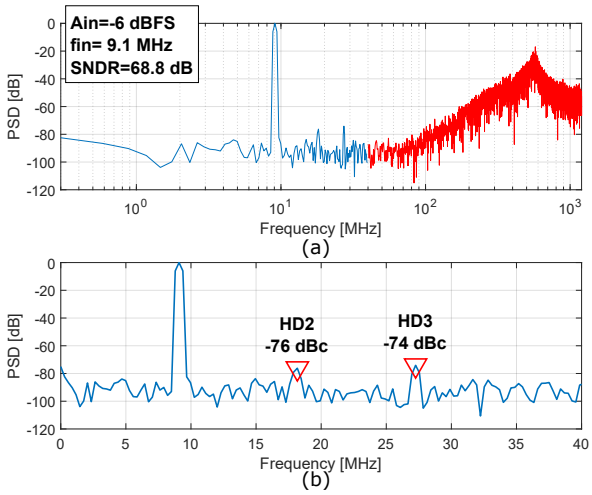

Fig. 4.36 Output Spectrum of the ADC (a), in-band detail of the spectrum (b).

jitter induced noise added to the quantization-noise extracted from the post-layout transient simulation.

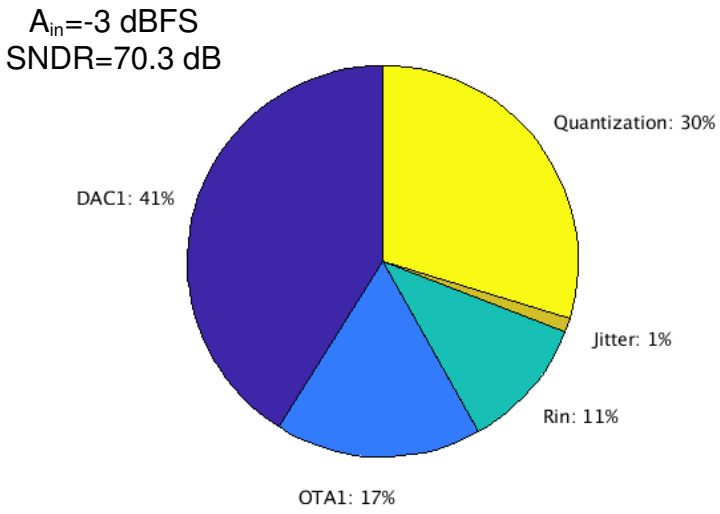

Fig. 4.37 Post-layout thermal noise distribution of the ADC.

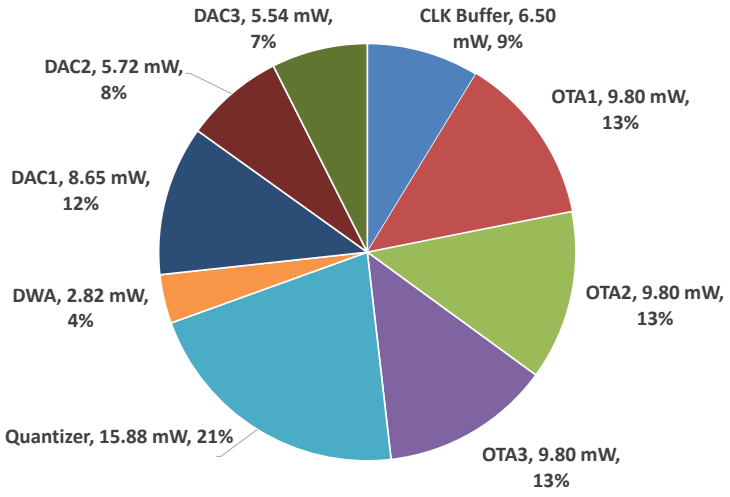

Fig. 4.38 Power breakdown of the ADC.

The power breakdown of the ADC is shown in Fig, 4.38. The loop-filter and the quantizer are the main contributors to the total power consumption of 77 mW. The Walden-FoM and the Schreier-FoM are commonly used to compare the performance of ΣΔM ADCs. The Walden-FoM is expressed as:

$$FoM_W = \frac{Power}{2BW\,2^{ENOB}} \tag{4.7}$$

where $ENOB = (SNDR_{max} - 1.76)/6.02$. The Schreier FoM is defined as:

$$FoM_S = DR(dB) + \frac{BW}{Power} \tag{4.8}$$

Table 4.2 presents the performance summary of the ADC and the comparison with some of the CT ΣΔM ADCs in the literature with similar bandwidths.

4.4 Conclusions

Multi-standard car radio receivers offer the reception of modern digital-radio standards such as HD Radio and DAB as well as the analog standards broadcasting standards such as AM and FM. A wideband IF ADC structure is a good candidate for these receivers as it moves a large part of RF analog front-end functions such

Table 4.2 Performance summary and comparison table of the ADC.

	[47]	[38]	**This Work**
Technology	28nm	65nm	**28nm FD-SOI**
Active Area	0.9 mm^2	0.8 mm^2	**0.35** mm^2**
Supply Voltage	0.9/1.8/-1.0 V	1.3 V	**1.0/1.8 V**
Bandwidth (BW)	45 MHz	50 MHz	**40 MHz**
Sampling Freq.	3.2 GHz	1.229 GHz	**2.4 GHz**
OSR	35	12.3	**30**
$SNDR_{max}$	72.6 dB	62.9 dB	**70.3 dB***
DR	90 dB	69.5	**72 dB***
Power	235 mW	88 mW	**77 mW***
FoM_W	748 fJ/step	770 fJ/step	**360 fJ/step**
FoM_S	172 dB	157 dB	**159.15 dB**
*: Simulated. **: Decimation logic is excluded.			

as channel filtering and tuning to the baseband digital signal processing unit which offers flexibility as well as significant area and cost reductions. The ADC is shared among the front-ends of the receiver and it is the challenge of the multi-standard receivers. The ADC should have wide bandwidth to be able to convert all of the bands at once and at the same time it must have large DR to compensate for the lack of channel filtering.

In this chapter, a CT ΣΔM ADC for multi-standard car radio receivers is presented. The bandwidth of the ADC is 40 MHz and the sampling-rate is 2.4 GHz. The ADC aims to achieve 70 dB SNDR and high-linearity as the primary specifications. The third-order CT modulator employs a CIFF-B loop-filter architecture and 4-bit quantizer for an SQNR of 102 dB. The digital differentiation ELD compensation scheme is used to eliminate the summing node at the input of the quantizer. Active-RC integrators are used for better linearity. The integrators use feed-forward OTAs for higher achievable GBW. A flash ADC with three-stage comparators is employed as a quantizer. NRZ pulse shapes are used for all the DACs. DACs use complementary current-steering architecture for improved power efficiency and lower noise.

A DWA scheme is used to suppress the non-linearity due to the DAC element mismatch. The element rotation of the DWA is an issue in high-speed sigma-delta ADCs for the strict timing requirements. The single-stage barrel shifters are fast, however their complexity and input capacitance rapidly increases when the number of the bits in the quantizer. The select bits of the barrel shifter should be encoded and the time required for the encoder is another drawback. In this work a hybrid rotational shifter structure is presented. The structure separates the shift-by-8 step to execute it in parallel with the encoder operation. The shift-by-8 block is done as in logarithmic shifters and uses 2-to-1 multiplexers. In this way, the input capacitor of the shifter and the complexity of the barrel shifter is reduced. For the second step

of the optimization, the shift-by-1 operation is embedded in the retiming latches of the DAC by adding the latch another data-clock path and gating the clock of the data using the select signal. The modification adds little complexity and delay to the conventional retiming latch. The resulting rotational shifter theoretically has the same delay as a barrel-shifter for the given quantizer resolution and reduces the input capacitance of the shifter. The shifter has post-layout delay of 142 ps.

Post-layout simulations have shown that the designed ADC achieved DR of 71 dB and maximum SNDR of 70 dB with -74 dBc THD. The HD_2 due to the ISI and the HD_3 due to the dynamic errors of the current-steering DAC dominates the THD. The SQNR is greatly reduced due to the parasitic loop delays and the DAC dynamic non-linearity. The ADC consumes 77 mW from 1 V and 1.8 V supplies. The ADC is fabricated in 28nm FD-SOI CMOS technology from STMicroelectronics and the measurements are expected to start in early 2019.

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Chapter 5
Conclusions

5.1 Thesis Contribution

This thesis has studied techniques to improve the speed, dynamic range and power efficiency of three different high-speed ADC architectures. These ADCs are aimed to be used in modern broadband communication systems implemented in nanoscale CMOS. The main contributions of the thesis are following.

The multi-bit/cycle SAR ADCs have high potential to increase the conversion speed of the conventional implementations. The multi-bit/cycle SAR ADC implementations in the open literature draw attention to two main issues. First is generating the multiple reference values required for each step. Conventional method is employing more than one DAC with the capacitive DAC or using a single-resistive DAC with a complex switch network. Both solutions increase the area of the converter that can be an important issue for the massively interleaved ADCs. Second issue is the offset of the comparators. Comparator offset is not a concern for the conventional SAR ADCs. However, the multi-bit/cycle SAR ADCs employ more than one comparator and mismatch of their offsets leads to nonlinearity of the ADC transfer function. Employing comparator offset calibration or using preamplifiers are common techniques to mitigate the effects of the offset. This thesis presents a preamplifier structure which generates the reference voltages required for a multi-bit/cycle SAR ADC. The presented structure solves the main drawbacks of the multi-bit/cycle SAR ADCs. Since the reference voltages are generated using the preamp, the CDAC is merely used for the input sampling and the residue generation. Therefore, multiple CDACs are not required and the area as well as the input capacitance of the converter can be reduced significantly. Both improvements serve the time-interleaved architectures. The static power consumption of the preamplifier can be justified as it is used to provide voltage gain which also mitigates the input referred offset of the latches. This thesis also presents an analysis on the proposed preamplifier, which may prove useful for the design of the circuit.

In this thesis, a method to calibrate the timing skew of flash-assisted time-interleaved analog-to-digital converters is proposed. The calibration is performed

in two steps and composed of a variance based and of an auto-correlation based timing-skew estimation. There are three significant attributes of the method. First, both estimation phases are performed in the digital domain and require low hardware. Second, the technique is suitable for the FATI SAR ADCs that employ multiple flash-ADCs, in other words the time-interleaved FATI SAR ADCs. Third, the channel randomization is facilitated with the use of the proposed method.

CT ΣΔM ADCs offer attractive features for wireless receivers. CT ΣΔM ADCs with single-bit quantizers can be used to achieve the stringent linearity requirements of these receivers. However, increasing dynamic range and bandwidth requirements impose high sampling frequencies to CT ΣΔM ADCs with single-bit quantizers which yields the circuit design and maintaining stability of the modulator cumbersome. Multi-bit quantizers are used to achieve the required specifications with a lower order modulator and OSR. However, the DAC nonlinearity is serious issue in this case. DWA has been commonly used to mitigate the effects of the DAC nonlinearity. Rotational element shifting operation is an issue for sampling rates on the order of GHz. This thesis presents a novel hybrid shifter structure for element rotation. There are three major features of the proposed shifter structure. First, it theoretically has the delay of a fast single stage barrel shifter, although it is multistage. Second, the transistor number, the complexity and the input capacitance of the shifter is lower compared to the barrel shifter. Third, since the shifter is multistage, it lends itself to be optimized further in terms of delay, using the techniques such as logical effort. A CT ΣΔM ADC for multi-standard car radio applications is also presented with the considerations and details of design.

5.2 Future Work

Improvements to the presented research work in this thesis are following:

5.2.1 Multi-bit/cycle Subranging Flash-SAR ADC

Asynchronous SAR ADCs broke the 1 GS/s barrier for the single-bit per stage 8-bit structures [1]. Asynchronous clocking increases the conversion speed significantly for SAR ADCs. Moreover, a clock signal faster than the sampling frequency is not required, which can substantially improve the power efficiency. The SAR ADC in this thesis uses a shift-register-free logic block based on a clock divider which requires a clock signal with only frequency of $2f_s$. Nevertheless, the power consumed on digital section correspond to 58% of the overall consumption. Therefore, the ADC would benefit substantially from the asynchronous clocking in terms of speed and the power consumption.

The SAR ADC presented in this work has another major contributor to the power consumption, namely the flash ADC and the preamplifier. The flash ADC remains

idle after its turn and the current consumed on the resistive divider is wasted. A solution to this issue may be a capacitive reference generation as the one presented in [2]. The preamplifier in this work shares a single differential pair for two SAR steps, however, the dummy technique employed to improve the settling of the reference voltages reduces the power efficiency of the method. Therefore, another technique for the settling issue of the reference voltages at the load switching would serve to increase the power efficiency of the proposed preamplifier.

5.2.2 Timing skew calibration method for FATI ADCs

In this thesis the idea of the concept is explained and the effectiveness of the proposed calibration method is shown through the behavioral MATLAB simulations. However, extensive simulations on the effect of system and circuit nonidealities should be performed.

For the sake of demonstration, this work uses the technique presented in [3] for the second phase of the calibration. There are many candidate techniques for this phase in the open literature and a study may be done to find the most suitable method for the purpose. For instance, if the second calibration phase is done with a variance based skew estimation, the variance calculation block can be shared between the calibration phases. This would reduce the hardware overhead considerably.

5.2.3 CT ΣM ADC for multi-standard car radio receivers

CT ΣΔM ADC uses DWA to mitigate the static-nonlinearity. However, in high-speed CT ΣΔM ADCs the dynamic errors are problematic too, as the reported post-layout simulations have shown. Therefore, the feasibility of the countermeasures against the dynamic DAC errors such as ISI correction [4] or the RZ DACs should be done to improve the linearity and dynamic range of the ADC.

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Appendix A
List of Publications

The list of publications from the research carried out during the PhD studies is given below.

1. **A. Akdikmen**, E. Bonizzoni and F. Maloberti, "A Timing Skew Calibration Method for Time-Interleaved FATI ADCs," *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, 2018, pp. 1-5.

2. **A. Akdikmen**, E. Bonizzoni and F. Maloberti, "A third-order time-interleaved $\Sigma\Delta$ modulator," *2017 13th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, Giardini Naxos, 2017, pp. 117-120.

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