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Doctoral Thesis in Microelectronics
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Design of Wideband Architectures for Modern Communication Standards

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Declaration of Authorship

I, Arianna Coccia, declare that this thesis titled, 'Design of Wideband Architectures for Modern Communication Standards' and the work presented in it are my own. I confirm that:

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"Do or Do Not. There is No Try"

Maestro Yoda

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Abstract

Facoltà di Ingegneria
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Doctor of Philosophy

Design of Wideband Architectures for Modern Communication Standards

by Arianna Coccia

Modern communication standards demand wideband solutions, with increasing channel bandwidths. At the same time, massive MIMO is quickly approaching, asking for low-cost and low-power architectures. This thesis is focused on the design of RF blocks, suitable for state-of-the-art applications. The work is divided in two parts. In the first one an innovative transmitter architecture based on a current-mode passive mixer topology with a closed-loop RF amplifier is presented. The second part deals with the analysis and design of a broadband, inductorless noise-cancelling low-noise transconductance amplifier. Measurement (TX) and simulation (TX and LNTA) results are reported, to validate the proposed designs.

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Abbreviations

AC	**A**lternating **C**urrent
ACLR	**A**djacent **C**hannel **L**eakage **R**atio
BB	**B**ase **B**and
BOM	**B**ill **O**f **M**aterial
BP	**B**and **P**ass
BS	**B**and **S**top
CA	**C**arrier **A**ggregation
CG	**C**ommon **G**ate
CIM3	**C**ounter **I**ntermodulation **P**roduct **3**
CM	**C**ommon **M**ode
CMFB	**C**ommon **M**ode **F**eed **B**ack
CS	**C**ommon **S**ource
DB	**D**ouble **B**alanced
DC	**D**irect **C**urrent
eMBB	**e**nhanced **M**obile **B**road **B**and
FDD	**F**requency **D**ivision **D**uplexing
HP	**H**igh **P**ass
IM2	**I**nter **M**odulation **2**
IM3	**I**nter **M**odulation **3**
IIP2	**I**nput **I**ntercept **P**oint **2**
IIP3	**I**nput **I**ntercept **P**oint **3**
IO	**I**nput **O**utput
IoT	**I**nternet **o**f **T**hings
LNA	**L**ow **N**oise **A**mplifier
LNTA	**L**ow **N**oise **T**ransconductance **A**mplifier
LO	**L**ocal **O**scillator

LP	**L**ow **P**ass
LTE	**L**ong **T**herm **E**volution
LTI	**L**inear **T**ime **I**nvariant
MBCM	**M**irror **B**ased **C**urrent **M**ultiplier
MIMO	**M**ulti **I**nput **M**ulti **O**utput
mMTC	**M**assive **M**achine **T**ype **C**ommunications
MOS	**M**etal **O**xide **S**emiconductor
NR	**N**ew **R**adio
OOB	**O**ut **O**f **B**and
PAD	**P**ower **A**mplifier **D**river
PPA	**P**re **P**ower **A**mplifier
RF	**R**adio **F**requency
RX	**R**eceiver
SAW	**S**urface **A**coustic **W**ave
SB	**S**ingle **B**alanced
TDD	**T**ime **D**ivision **D**uplexing
TIA	**T**rans **I**mpedance **A**mplifier
TVWS	**TV W**hite **S**pace
TX	**T**ransmitter
uRLLC	**u**ltra **R**eliable **L**ow **L**atency **C**ommunicans

To my sister Clarissa

Introduction

In recent years, the diffusion of wireless devices, in developed and emerging economies, has enabled everyone to communicate. It follows that modern communication standards have to coexist with the previous generations, while satisfying the new requirements. The continuous demand for higher data rates has led to the opening of several new bands in the sub-6GHz range to mobile communications with channel bandwidth up to 100MHz. At the same time, low power and low cost architectures represent the best solution to meet the requirements of the increasingly popular massive-MIMO techniques.

In order to enable multi-band operation and to improve connection quality through diversity and multiple-input multiple-output (MIMO) techniques, several transceiver chains are integrated on the same chip and connected to multiple antennas, each covering a sub-set of the desired bands. The addition of external filtering, i.e. SAW filter or duplexers avoids signal degradation caused by mutual interference, self-interference and out-of-band transmitter emissions but substantially complicate the board and the Input/Output PADs. In this way, not only the cost of the system will be limited by the external components, but also such a complicated routing limits system integration scaling down, main feature of modern technologies. Therefore, minimizing the external component counts represents a key goal in transceiver research, but it faces very stringent requirements in terms of receiver and transmitter noise and linearity.

These system considerations are even more true, in the broadband scenario that characterizes the new standards. Considering the design of a TX/RX chain: the transmitter needs to keep the emission (out-of-band noise and non-linearity) in the receiving band as low as possible, in order to avoid compromising the receiver performance. On the other hand, RX design needs to be prompt to handle high interferers. Plus, in both cases, power consumption is another important parameter (MIMO systems). This thesis is divided in two main parts, where a transmitter and a LNTA implementations are proposed.

The used simulation environment is Cadence Virtuoso® System Design Platform.

Part I describes the design of a current-mode transmitter, based on a passive upconversion mixer that combines the I and Q signals into a virtual ground provided by a closed-loop RF amplifier. In Chapter 1 a brief description of the new generation

standards is provided, together with the design motivation. An analysis of the state-of-the-art is carried out in Chapter 2, while Chapter 3 describes in greater detail the proposed transmitter. Measurements results are summarized in Chapter 4, while Chapter 5 concludes this part.

Part II reports the analysis and design of a broadband noise-canceling LNTA, aiming at TVWS applications. Chapter 6 describes the TVWS scenario and explains the project motivation. In Chapter 7 the review of similar implementations are analysed and the LNTA topology is described. The simulation results are gathered in Chapter 8 and Chapter 9 draws the conclusions of the second part.

Part I

A Wideband SAW-Less Transmitter Operating in Closed-Loop with Embedded RF Filtering

Chapter 1

An introduction to 5G

Modern communication standards demand wireless transmitter to cover a wide carrier frequencies range and attaining increasingly channel bandwidths. In the first part of this dissertation, the design of a wideband SAW-less TX with embedded RF filtering, enclosed within a resistive loop is presented. This chapter presents the 5G sub-6GHz environment, starting from the analysis and considerations presented in [7] and lists the challenges related to SAW-less architectures, in addition to general system considerations.

1.1 General considerations

The arrival of LTE (Long Term Evolution) has made an important change into people everyday life, although it can be questionable that it had a larger impact than any other technology to developed and emerging economies, giving benefits to any kind of user.

The mobile industry represents the world's leader engine of innovation, because of the exponentially increasing smartphone adoption and the high quality service provided by the LTE. In most countries, in fact mobile is the main platform to Internet access.

However, this growing environment will keep rising, by extending the network coverage even to rural areas, making the mobile services more and more affordable, providing relevant content and increasing digital skills.

Starting with the availability of LTE data, an exponential growth of data consumption is keeping approaching. It follows the *Data flywheel effect*, which combines mobility, good network performance and desirable content into a virtuous cycle [7] (Fig.1.1).

At this point, as the user experience improves, the consumed data increases, following the trend of 'data demand' that has always been one of the main target of mobile industry, since the arrival of LTE.

Actually, to provide the required higher throughput, new techniques have been developed, making the *wheel* running faster.

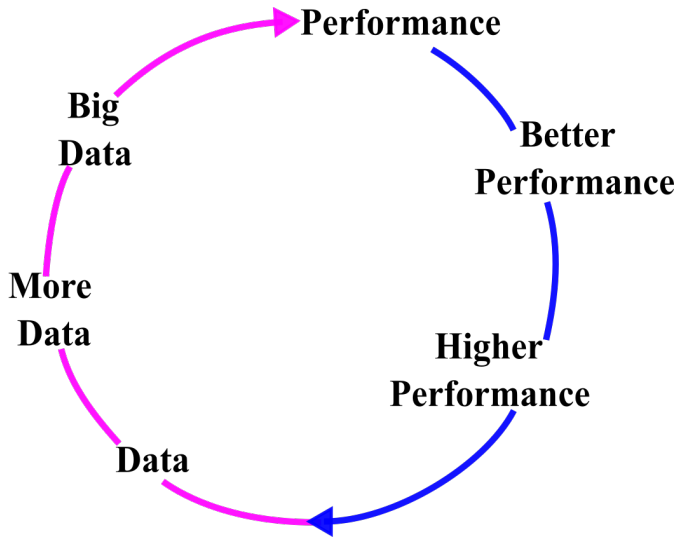


Figure 1.1: DataFly Wheel effect

Mobile communications are now moving into the 5G world that can be considered an evolution of the previous LTE but also a revolution, thinking about the 5G New Radio (NR).

According to [7] the definition of 5G can be satisfied by driving the average data throughput in tens of gigabits per second ranges.

The current 3GPP standards, moving towards the 5G requests, is able to provide 2 to 3 times greater data rates, exploiting new standardized methods (Fig.1.2):

- eMBB (Enhanced mobile broadband) based on growing the system capacity, aiming at 1000x capacity. This aspect will characterize the sub-6GHz 4G and 5G
- uRLLC (Ultra reliable low latency communications) that is very important for critical implementation, requiring high reliability and availability, in addition to very low latency
- mMTC (Massive machine-type communications) strictly correlated to the IoT (Internet of Things) applications, thus requiring low cost and low data rate

1.2 Towards 5G

As reported in Eq.(1.2) (Shannon-Hartley theorem) the capacity of a link depends on the number of data streams, bandwidth and channel noise.

$$C\left(\frac{B}{S}\right) = MB\log[2]\left(1+\frac{S}{N}\right) \tag{1.1}$$

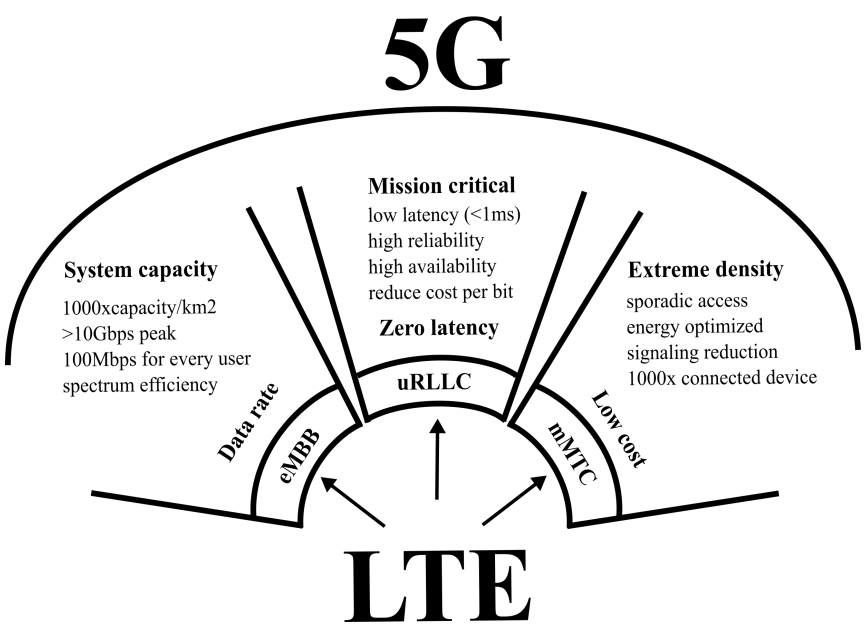


Figure 1.2: 5G targets

where C is the channel capacity in bits/second, M is the number of channels (related to massive MIMO applications), B is the bandwidth and $\frac{S}{N}$ it the signal to noise ratio.

At this point, the main goal in modern standard is to increase the data rates, as already stated. To achieve this goal it is possible to:

- increase the bandwidth
- increase the number of paths M
- increase the Transmit Power (S)
- reducing the noise (N)

Different techniques have been proposed to attain the required performance. Wider bandwidth can been achieved through carrier aggregation (CA), the modulation order has been improved and also MIMO is under deeply investigation.

Carrier Aggregation is a new technique in which different channels are used to cover a wider bandwidth, with the help of a supplementary carrier.

Increasing the complexity of the modulation allows to increase the number of bits per symbol or data rate. However, in order to obtain the expected results, the SNR must be improved.

From the transmitter point of view, the RF amplifier must minimize the emission and noise level. At the same time the TX should also be able to manage a wider dynamic range, to maximize efficiency which is extremely important in these applications.

The number of paths is another key point, as deeply related to MIMO approach, used to increase the mobile systems bandwidth, involving to send and receive more than one data stream onto a single radio, exploiting at the same time the use of multiple antennas.

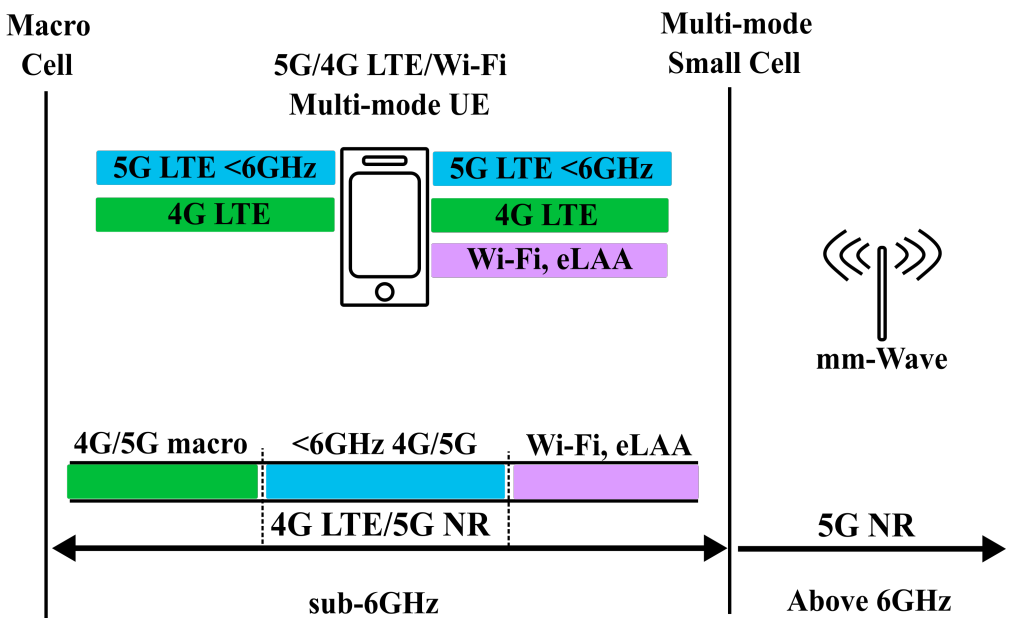


Figure 1.3: Skyworks vision of the 5G ecosystem

Taking into account all the previous considerations, the RF front-end circuitry complexity is increasing, in order to guarantee the claimed performance.

Fig.1.3 shows the 5G environment. There are two main frequency range of activities: sub-6GHz and at mmWave. The first one represent the range of application of the architecture proposed in this work.

In this frequency range, both traditional 4G LTE systems and modern 5G NR should coexist. It follows that the design challenges (reported in the next section) are quite similar to the typical LTE architectures. However, wider bandwidth for higher throughput is an additional request.

Eventually, 5G represents the next step of the 4G architectures, where all the old features need to be achieved and improved.

1.3 Modern standard communication platforms

5G communications below 6GHz are characterized by highly demanding New Radio (NR) interface. Wireless transmitter should be able to cover a wide carrier frequencies range, with channels up to 100MHz.

Compatibility with the previous standards is also a critical point, in fact the number of frequencies and the coexistence of multiple standards represent a limit for the platform costs and performance.

This aspect is even more critical considering the ever-growing approach of massive-MIMO techniques, to meet the demanded high data-rate. This implies the need of interactions among many antennas that further increase the complexity of the communication chains and platforms.

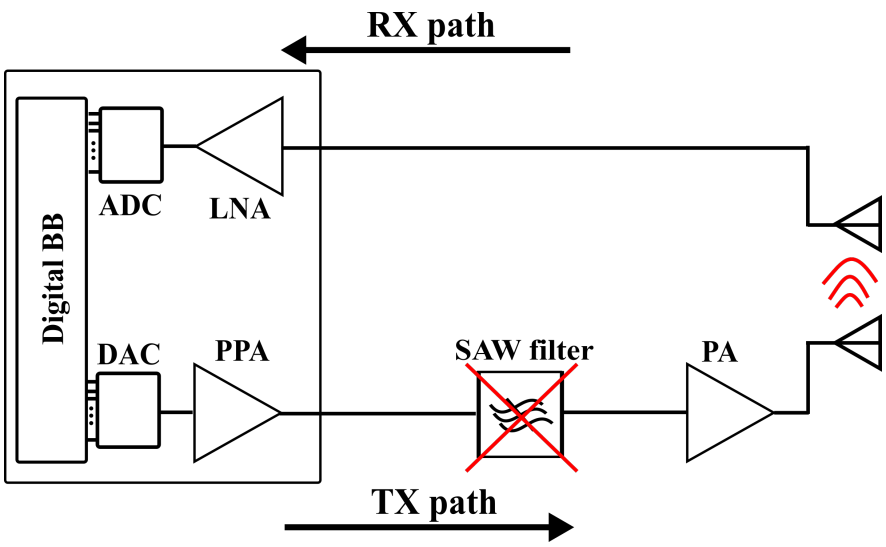


Figure 1.4: Typical SAW-less scenario

5G communication operates both in TDD and FDD. In the former case, the isolation between TX and RX is provided by the switching operation, the latter instead requires the help of external SAW filters/duplexers in order to avoid an unwanted leakage from the transmitter to the receiver. Both TDD and FDD have multiple bands of operation, each one asking for a specific filter.

The several numbers of Input-Output (IO) PADs require to externally connect the receiver to the transmitter and viceversa, strongly limiting the scalability of the CMOS process. The chip dimension, indeed, can be dominated by the IO PADs number and space occupation, making the possibility of exploitation of the technology scaling-down harder.

Although each antenna is able to work in a wideband frequency range, the burden of the external passive components will become unacceptable. Cost and performance will be strongly affected, since SAW filters (and also duplexers) are bulky and costly. For this reason, they become the dominant cost contributors and together with the complexity of the board, they will impact the Bill of Material (BOM) in a significant way.

Hence, modern architectures need to eliminate these bulky, costly and above all not tunable filters, which are not suitable for the state-of-the-art requirements (Fig.1.4).

However, removing the external filtering comes not for free. It actually makes the transceiver design even more challenging. The most sensitive part of the transceiver (the analog front-end) can be compromised, unless a different design approach is proposed.

There are two main issues, related to the leakage from TX to RX and they become even more crucial in a wideband scenario, as the one of modern communication standards:

- linearity: the transmitted signal represents the biggest blocker for the small receiver signal, together with many other interferers. Along the RX chain intermodulation or other non-linear effects may happen, causing undesired signals into the

receiver bandwidth or compression of the chain. However, this is a main concern of the RX design.

- out-of-band emission: out-of-band noise and non-linearity of the transmitter can degrade the front-end performance, when falling in the RX channel, which is actually quite close to the TX, in a wideband scenario. It is therefore important to keep the emission low, as it will be deeply described later in this work.

The architecture described in this thesis is quite innovative, as concern the design approach and it is able to achieve a wide signal bandwidth, still maintaining the out-of-band emissions low.

Chapter 2

State-of-the-art transmitters

State-of-the-art transmitters are presented in this chapter, which compares the possible solutions, highlighting advantages and drawbacks of the different implementations. This represents the starting point in the proposed transmitter design.

Although current-mode passive mixers, followed by a base-band transimpedance amplifier is recognized as the most effective receiver architecture, because of its outstanding linearity and noise, in transmitters several solutions are still researched with both active and passive mixers. In fact, classic analog topologies, based on a RF pre-power amplifier (PPA), are strongly limited by the efficiency-linearity trade-off, becoming even more important under technology and temperature variations.

This section presents different approaches, coming from the state-of-the-art, to the problem of TX design.

2.0.1 Power-mixer [1]

This work describes a fully reconfigurable multi-standard TX, reported in Fig.2.1. The operation are in voltage-mode for the base-band that consists into a DAC and two Biquad cells and it adopts an up-conversion power mixer. A variable gain V-I converter works as interface between the two domains (BB and RF), driving the mixer in class A/B.

This architecture, as a representative of power-mixer transmitter, eliminates the PPA and achieves good linearity, without using pre-distortion, however it is not very efficient.

2.0.2 Direct-digital [2]

The "all-digital radio transceiver" represents a recent trend, where the RF functions are digitally implemented, but it suffers of large out-of-band noise due to quantization and efficiency is quite poor. Moreover, in order to achieve the optimum linearity performance

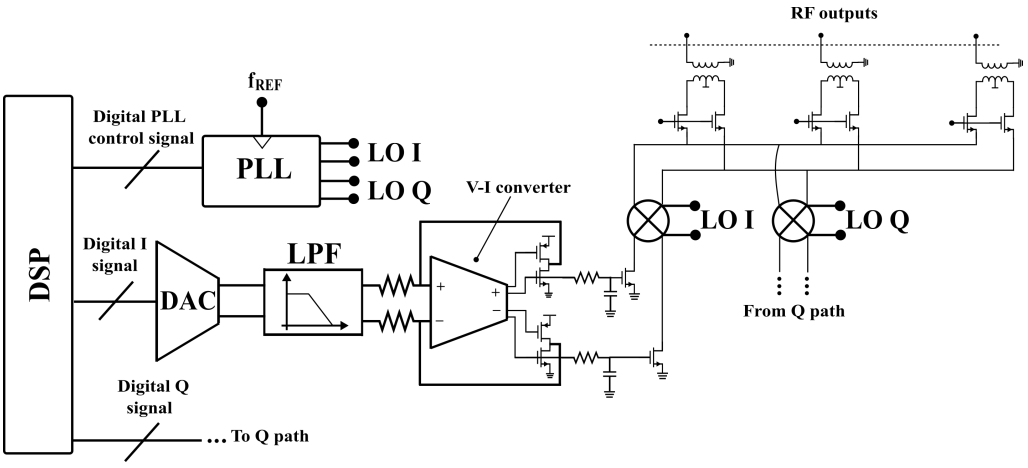


Figure 2.1: Class A/B power mixer TX

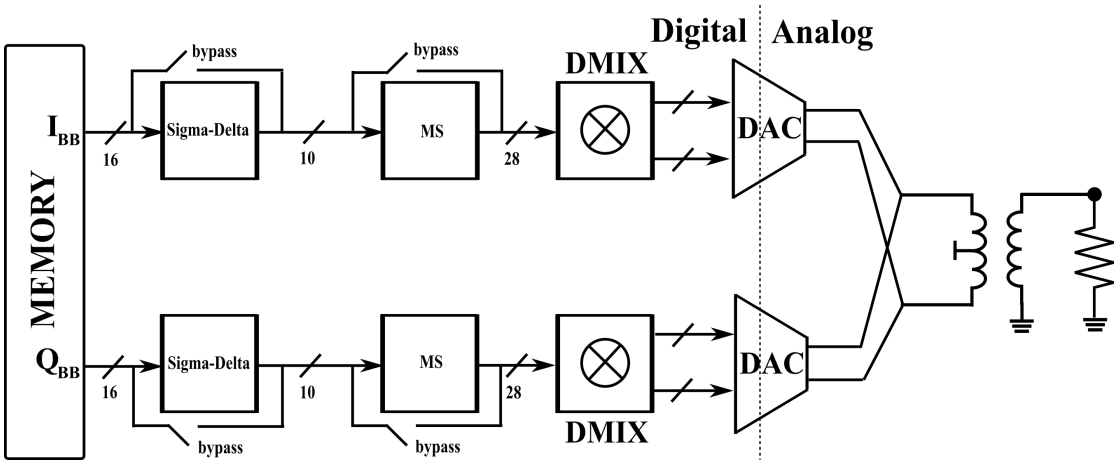


Figure 2.2: All digital RF transmitter

it needs pre-distortion that is not compatible with the massive MIMO approach, where many antennas interact with each other.

In this work, quantization noise in the RX band is reduced using a FIR notch that however costs extra power (Fig.2.2).

2.0.3 Voltage-mode passive mixers [3–5]

In literature, different and advanced transmitter architectures are based on voltage-mode passive mixers. In order to achieve high mixer linearity and avoid early compression, the voltage swing at the output must be constrained. It follows that either a low output power is delivered or a PPA is still necessary, as noticeable in the reported works.

Plus, even if a higher output power can be achieved, the performance are shown in back-off conditions.

Fig.2.3, Fig.2.4 and Fig.2.5 report three different voltage-mode passive mixers architectures, showing all the previously described drawbacks.

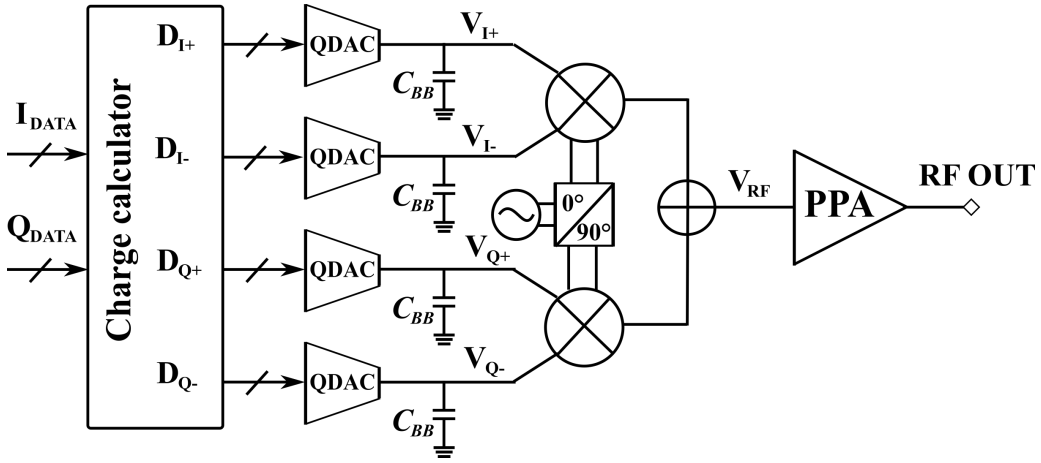


Figure 2.3: QDAC based transmitter

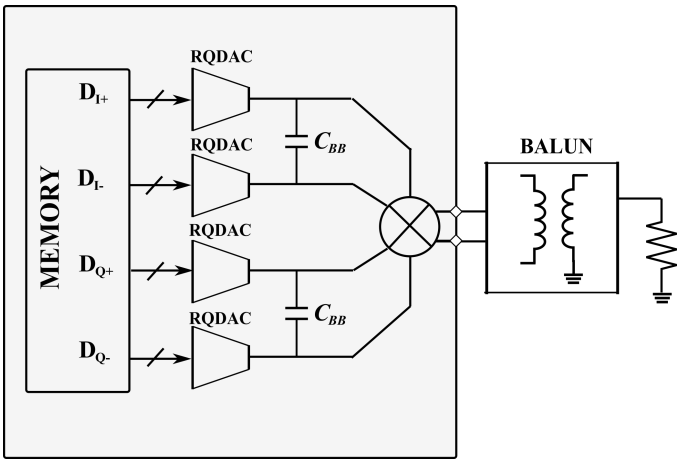


Figure 2.4: RQDAC based transmitter

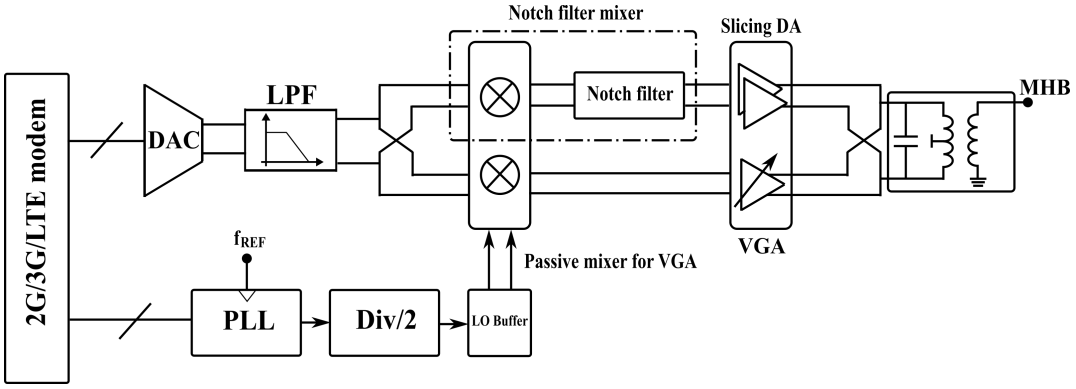


Figure 2.5: Transmitter with notch filter mixer

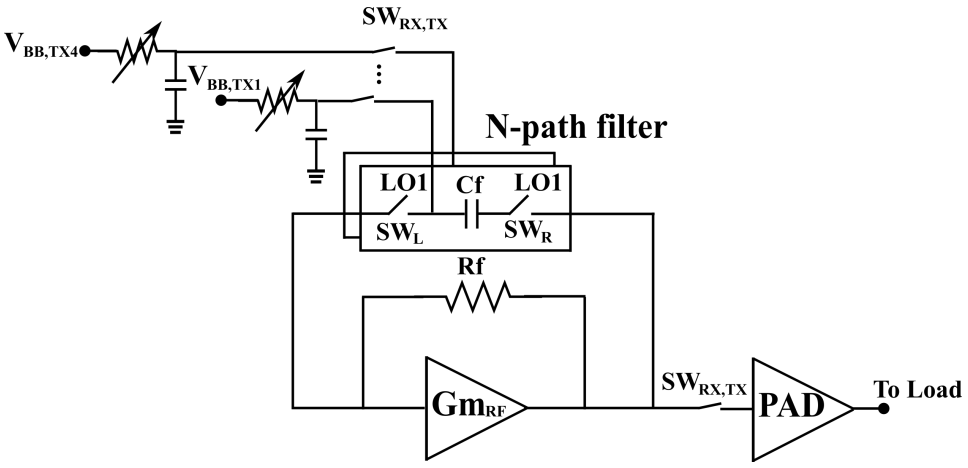


Figure 2.6: N-path SC gain loop TX

2.0.4 Current-mode passive mixers [6]

Current-mode passive mixers are hindered by the issue of creating a good virtual ground after up-conversion. For this reason, the idea of a transmitter architecture "symmetrical" to the state-of-the-art receiver is just a recent trend.

This work (Fig.2.6) describes a current-mode passive mixer, where a single-stage RF amplifier closed in feedback through a N-path filter implements the virtual ground. The transfer function is narrow-band (although the new standards are moving to wideband solutions) and it is exploited to reduce the OOB noise.

The single-stage amplifier attains a limited gain, therefore a single-ended PPA has been introduced, but it is not included inside the loop. For this reason, the linearity and driving capability issues are simply shifted to the PPA level.

Chapter 3

Circuit description

The proposed current-mode passive mixers transmitter is explained in this chapter, with a detailed description of the three-stage RF amplifier. A general introduction to N-path filters helps understanding the loop gain behaviour of the implemented TX that is qualitatively analysed, showing a band-pass filtering function, helping to solve the stability issue of the closed-loop solution.

3.1 Proposed TX architecture

3.1.1 N-path filters

As well explained in [8], the idea behind the concept of "N-path filters" goes back in the history. In fact, in [9] a narrow band-pass (BP) filter was proposed, based on a down-converter, a low-pass (LP) filter and an up-converter. Later, this basic concept has been applied in the "commutated networks" of [10], which implement a center-frequency tunable switched-RC band pass filter and a band stop (BS) filter. However, because of the lack of transistors, mechanical switches have been used.

In 1960 [11] N-path filters have been proposed as a sliced version of the circuit of [9], which realizes a multiple (N) paths topology, where each path is active at a specific time as reported in Fig.3.1.

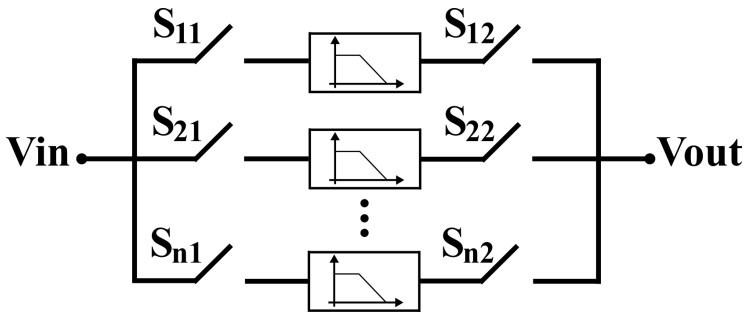


Figure 3.1: N-path filter: basic idea

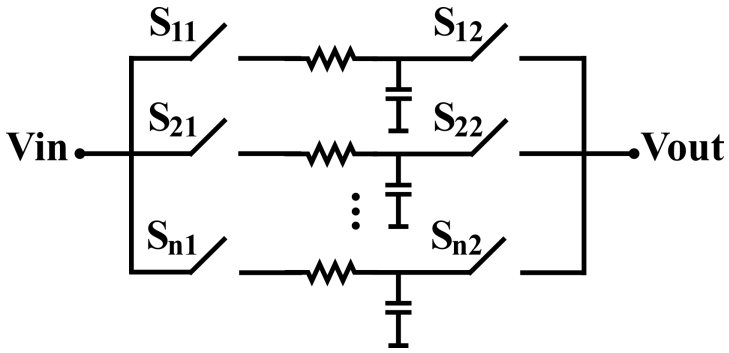


Figure 3.2: N-path filter: RC low pass

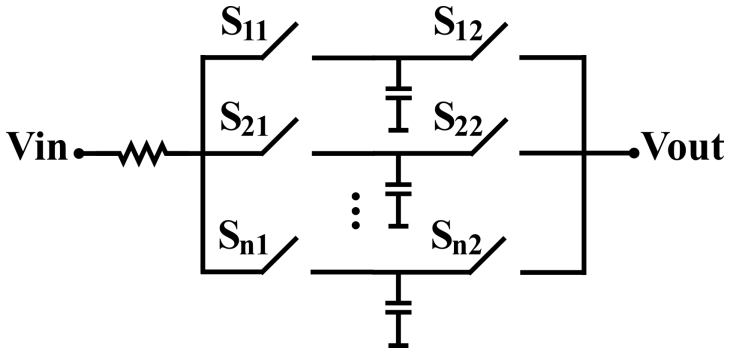


Figure 3.3: N-path filter: only capacitors

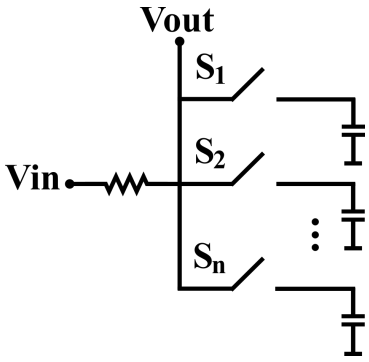


Figure 3.4: N-path filter: one switches set

Designing LP (HP) filters is much easier than BP (BS) filters. On the basis of this consideration, exploiting down and up-conversion, it is possible to realize BP (BS) filters, based on LP (HP). Indeed, this is the general idea of N-path filtering, where instead of performing an RF filtering, at first the signal is down-converted to base-band by the first set of switches, then this down-converted version is lowpass (highpass) filtered and finally, the signal is up-converted again (Fig.3.1).

Starting from Fig.3.1, the circuit can be simplified as follows:

- the LP filter can be implemented as a simple RC filter (Fig.3.2);
- the resistor R is connected in each phase, therefore it can be moved before the first set of switches (Fig.3.3);

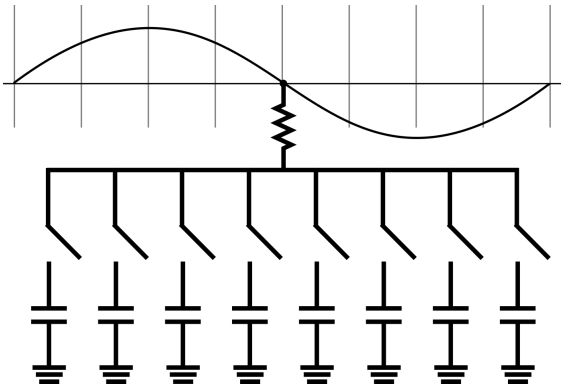


Figure 3.5: N-path filter: time domain analysis

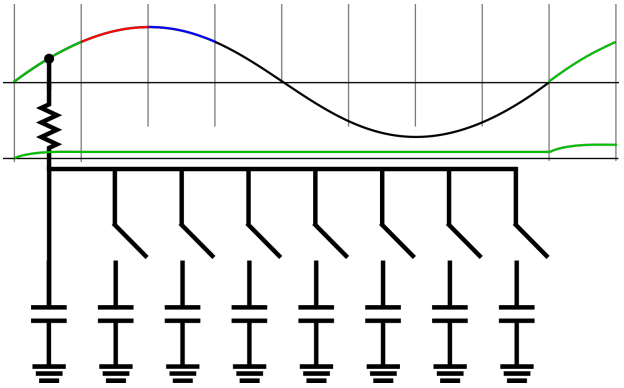


Figure 3.6: DC value charging one capacitor

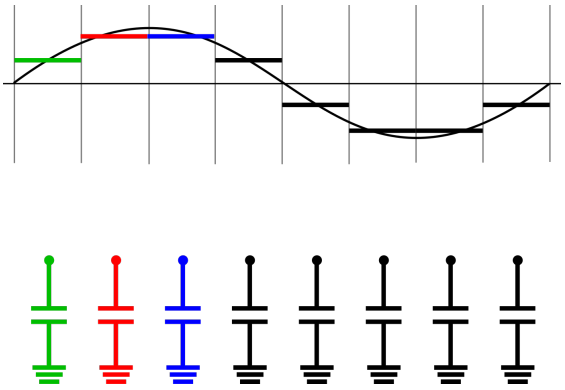


Figure 3.7: DC values stored on the capacitors

- the second set of switches can be removed, since when the switches are closed the output signal can be taken after the input R (Fig.3.4);

A frequency domain analysis is reported in [11], while in [11–15] it is discussed the time domain functionality.

Considering Fig.3.5, a simple time domain explanation can be provided, supposing at first that the clock frequency is equal to the input frequency. In each cycle, the capacitor is charged through the resistor at the input sinusoid value, with an RC time constant that is very large, in particular much greater than the time the switch is closed.

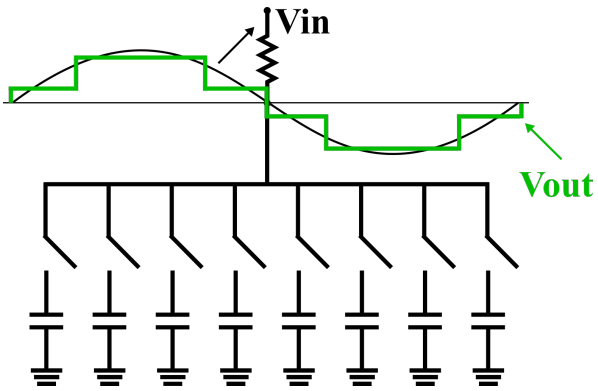


Figure 3.8: N-path filter: staircase approximation of the input signal

For this reason, the capacitance can charge just a little, each time the corresponding switch is on, since it sees always the same portion of the input sinusoid (Fig.3.6). Hence, after many cycles the dc voltage on the capacitance will be equal to the average value of the sinusoid in that interval (Fig.3.7).

Eventually, the output signal will look as a staircase approximation of the input signal, which becomes closer to the real sinusoid as the number of phases and capacitors increases.

On the other hand, if the input signal frequency is different from the clock frequency, each time the capacitors will see a different portion of the input signal, with the results of a final average DC voltage of the input signal equal to zero. It follows that for input frequency equal to the clock frequency the output is equal to the input, while for different frequencies the output is zero, resulting into a BP filter behaviour.

One of the main advantage of N-path filters is related to the way they can be implemented. In fact, they are basically realized with switches and capacitors, making CMOS technology the most suitable candidate for this kind of circuits. For this reason, the technology scaling and improvements have led to a renewed interest in this field. However, there are further positive characteristics. Indeed, the filter Q is extremely high (depending on the ratio of RC bandwidth and clock frequency) and simply changing the clock frequency, allows quick filter tuning.

As regards noise performance, the N-path filter shows good results, due to the zero DC current through the capacitance that allows low in-band noise. At the same time, the linearity is good as well since, in-band, the voltage swing across the switches is quite small, while out-of-band the signals are attenuated. Furthermore, the power consumption required to drive the switches scales with technology.

Unfortunately, this kind of circuits suffers of frequency folding and also harmonics represent a big issue in their behaviour.

An interesting and deeper discussion about N-path filters and their applications is also provided in [16] and [17], where LTI models of these time-varying architectures are

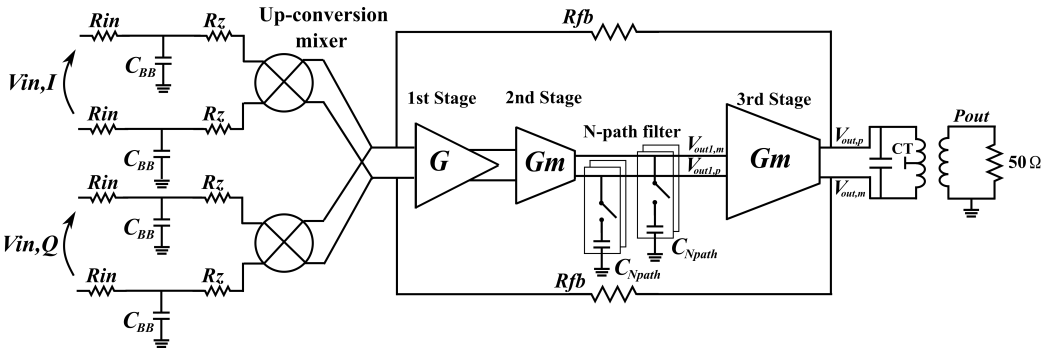
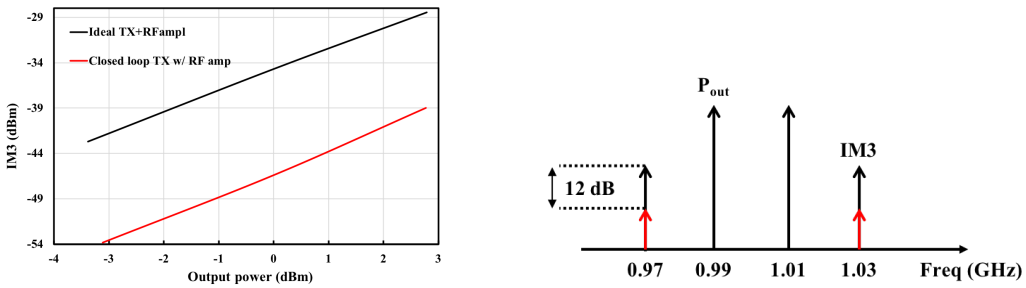


Figure 3.9: Architecture of the proposed transmitter



(a) IM3 vs output power **(b)** Two tones test output spectrum

Figure 3.10: Driver amplifier IM3 suppresion due to closed-loop operation

described and can be very useful, for a better understanding on how these circuits work.

3.1.2 Closed-loop TX

The architecture of the proposed transmitter is shown in Fig.3.9. The topology is wide-band and, as the one described in [6], it is based on a current-mode passive mixer.

The base-band resistors R_{in} (300 Ω) perform the voltage-current conversion and together with the capacitors C_{BB} (5 pF) attain a first order low-pass filtering, setting the input signal bandwidth to 100 MHz.

R_z, equal to 80 Ω, represents the last base-band component. Its role is crucial both for stability and noise performance, but it will be discussed in the following sections. The direct (I) and quadrature (Q) base-band signals are up-converted by the current-mode passive mixer and added up into the RF virtual ground, which is the bottle-neck of the entire design. In fact, providing a good virtual ground at clock frequency (around GHz) represents one of the main challenge in this topology.

In order to overcome this issue, the transmitter RF side has been realized as a three-stage amplifier with a broadband resistive feedback ($R_f = 170$ Ω). This loop, not only is able to provide the virtual ground but also performs the current to voltage conversion, directly driving the primary of the output balun.

The proposed topology is entirely closed-loop (no external RF PAD), which represents a new feature compared to the other state-of-the-art solutions. It follows that some significant advantage of closed-loop systems, most of them distortion related, are embedded into this architecture. In fact, the distortion of the push-pull output stage of the amplifier is significantly suppressed by the loop.

Simulation results reported in Fig.3.10 compare the distortion generated by the output stage when operating in open-loop with the distortion produced by the driver, when it is enclosed in the proposed solution. At reasonable power level, an improvement of 12 dB can be observed.

However, closed-loop operation implies stability issues that, in this particular structure have been solved in a non-conventional way. In fact, a N-path filter, switched at the clock frequency, has been inserted as load of the second RF amplifying stage, as noticeable in Fig.3.9. As explained in the previous section, its behaviour is band-pass, ensuring high loop gain around the transmitter carrier frequency, while limiting the out-of-band gain. In this way, differential loop stability can be achieved even with process and temperature variations.

Eventually, all the advantages related to N-path filters, that is low power consumption, good noise and linearity performance and easy tuning are inherent in this solution. Above all, the circuit simplicity (only switches and capacitors are needed) allows compatibility with scaled technology, which is one of the main advantage of the whole TX chain.

The following section will describe the loop gain behaviour, showing simulation results that will help understanding in a qualitative way how this time-varying loop works.

3.2 Loop gain analysis

3.2.1 Linearity and stability considerations

The proposed architecture (Fig.3.9), being closed-loop, implies stability concerns. The closed-loop RF amplifier consists of a three-stage topology that allows to achieve sufficiently high gain. Unfortunately, the phase margin can be quite low, unless a solution for compensation is introduced.

At this point, it is important to remember that the transmitter needs high gain just in the bandwidth of interest, while out-of-band, not only for stability but also to improve noise performance a filtering behaviour is preferable.

This supports the choice of a N-path filter as load of the second amplifier stage. Basically, it corresponds to the introduction of controlled pole, realized with switches and capacitors, which gives to the loop gain a band-pass shape, as noticeable in the black curve of Fig.3.11. Fig.3.12 reports the phase of the loop.

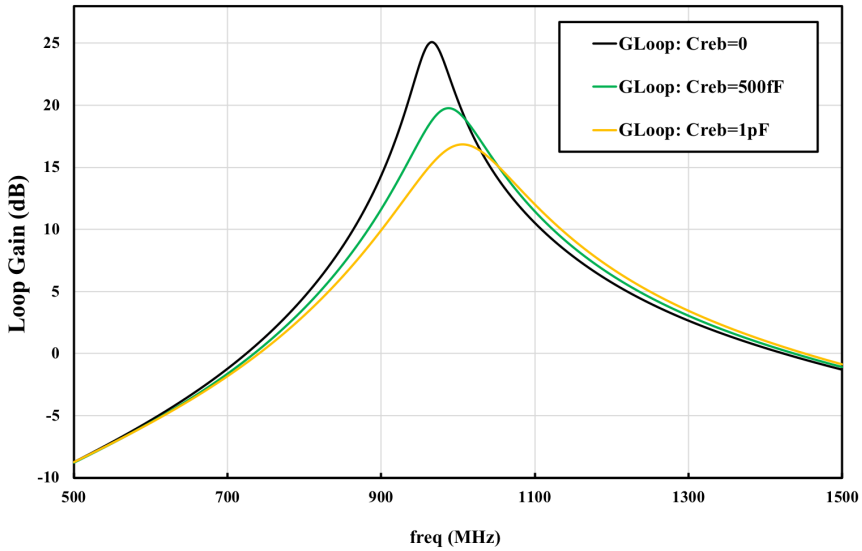


Figure 3.11: Loop gain w/o and with the rebalancing auxiliary mixer optimization

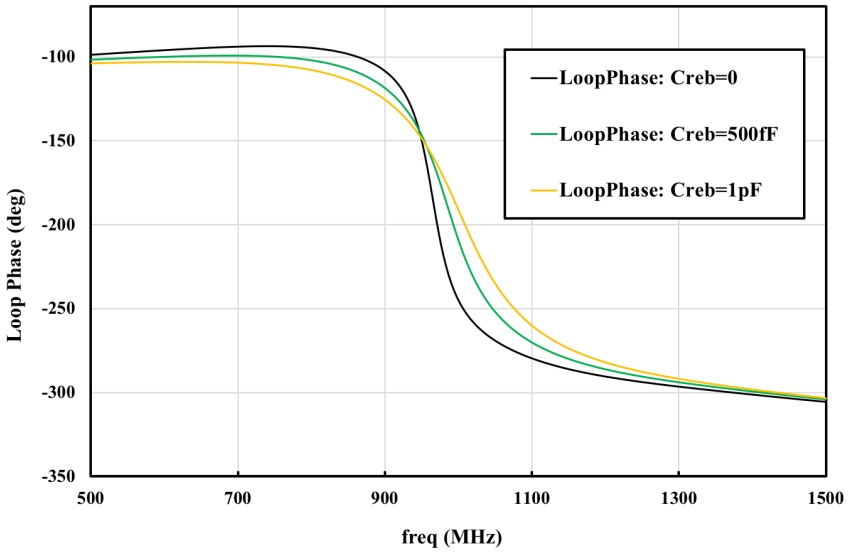


Figure 3.12: Loop phase w/o and with the rebalancing auxiliary mixer optimization

The N-path filter is clocked at the transmitter carrier frequency (f_{LO} equal to 1GHz), ensuring in this way a good virtual ground in the desired channel bandwidth. It follows that the loop works properly just in the frequencies of interest, while its gain starts decreasing far away from the carrier, as required by the application.

Despite the simplicity of the network, the N-path filter design is quite crucial. The switches needs to be big enough to manage the RF signals without introducing distortion and the capacitors size must be chosen considering a trade-off between stability and linearity performance, without neglecting the area consumption.

Considering linearity at first, the value of the N-path capacitor is equivalent to 15 pF single-ended, resulting in a loop gain -3 dB bandwidth of about 23 MHz, above and below the carrier frequency with a peak gain of 25 dB. Hence, until the loop is working, it will manage to keep the distortion of the output stage low, as already explained and demonstrated in the previous section.

In order to increase the Q of the loop gain, to achieve higher values, the N-path capacitance must be increased. However, this will narrow the gain bandwidth, therefore intermodulation products that fall far away from the carrier will degrade the distortion performance, since not compressed by the loop. It follows that at very low frequency offsets linearity performance will be better, but in a wideband applications fashion a broadband loop gain represents a smarter choice.

As concerns stability, a qualitative and intuitive analysis is provided, which together with simulation results served as a basis for the circuit design.

At first, once the N-path is inserted in the loop, three resonating structures are present: the up-conversion mixer that with C_{BB} basically consists in another N-path filter, the second-stage load N-path filter and the output balun. Considering that the Q of the output balun is extremely low, the issue may concern the up-conversion mixer and the N-path filter.

The BB capacitance, as already described sets together with the input resistance the input low-pass filter cut-off frequency, and its value is quite low (5 pF). At the same time, the N-path capacitance is set for a wide loop gain bandwidth to 15 pF. It means that the poles of the two filters can be dangerously closed to each other.

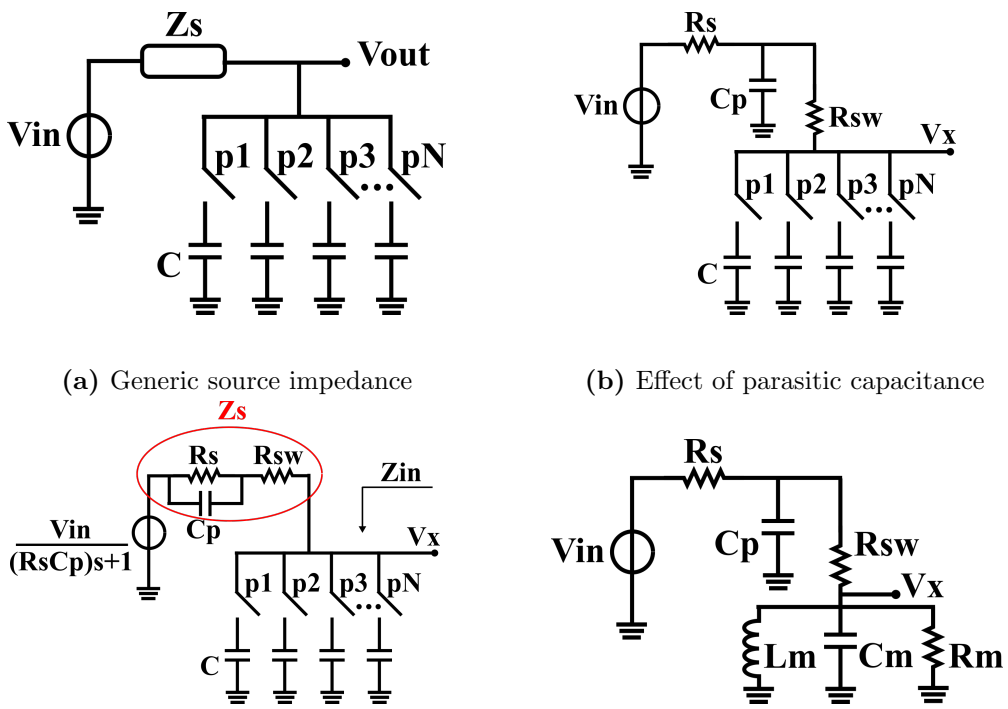
Thus, to improve the phase margin (and also noise performance as it will be later explained) another base-band resistance R_z is put in series to the mixer, moving the zero that is usually set by the on-resistance of the switches to lower frequencies, to tackle the N-path pole.

Finally, the operational amplifier poles should be accurately set to higher frequencies, so that their contribution could be considered negligible.

3.2.2 Effect of parasitic capacitance on N-path filter

In order to understand the effect of parasitics capacitance on the designed TX, a general description of N-path filter affected by parasitics is required, since the mechanisms are actually the same occurring in the proposed architecture.

Parasitic capacitances represent one of the biggest issue to deal with, when designing a N-path filter. As reported in [17], the N-path filter can be modelled with a RLC tank. For this reason, the intuitive expectation is that the addition of parasitic capacitance at the input node will lower the center frequency of the filter, without introducing loss. However, voltage losses are actually introduced. In fact, modelling the input



(a) Generic source impedance

(b) Effect of parasitic capacitance

(c) Equivalent source impedance

(d) RLC equivalent model

Figure 3.13: The effect of parasitic capacitance on the N-path filter

impedance of the filter with a RLC tank, if the inductance L and capacitance C values are independent from the parasitic capacitance, the value of the resistance R decreases, increasing C_{par} value.

The transfer function of the filter reported in Fig.3.13a around the LO frequency (f_{LO}) is [18, 19]:

$$T(\omega_{LO} + \Delta\omega) = \frac{Y_s(j(\omega_{LO} + \Delta\omega))}{\frac{NCj\Delta\omega}{sinc^2(\frac{\pi}{N})} + \sum_{m=-\infty}^{+\infty} \frac{Y_s(j(Nm+1)\omega_{LO})}{(1+mN)^2}} \tag{3.1}$$

Following the rationale of [18], the series at the denominator of Eq.(3.1) can be called Y_{eff}, thus Y_{in} of Fig.3.13a will become:

$$Y_{in} = Re\{Y_{eff}\} - Re\{Y_s\} + j\left(\frac{NC\Delta\omega}{sinc^2(\frac{\pi}{N})} + Im\{Y_{eff}\} - Im\{Y_s\}\right) \tag{3.2}$$

The effect of parasitic capacitance can now be studied, starting from Eq.(3.1) and Eq.(3.2), with reference to Fig.3.13b. The circuit of Fig.3.13b is converted to the topology in Fig.3.13c, to obtain an equivalent solution of Fig.3.13a.

At this point, $Y_s(s)$ is equal to $\frac{1}{R_s+R_{sw}} \frac{R_sC_ps+1}{R_s//R_{sw}C_ps+1}$.

The transfer function of the circuit in Fig.3.13c from V_{in} to V_x can be calculated as:

$$T(\omega_{LO}+\Delta\omega)=\frac{1}{jR_s//R_{sw}C_p\omega_{LO}+1}\frac{1}{R_s+R_{sw}}\frac{1}{j\left(\frac{NC\Delta\omega}{sinc^2(\frac{\pi}{N})}+Im\right)+Re} \tag{3.3}$$

where:

$$Re=\frac{1}{R_s+R_{sw}}\sum_{n=-\infty}^{+\infty}\frac{1+(1+nN)^2(R_s//R_{sw})R_sC_p^2\omega_{LO}^2}{(1+nN)^2\left[1+(1+nN)^2(R_s//R_{sw})^2C_p^2\omega_{LO}^2\right]} \tag{3.4}$$

$$Im=\frac{1}{R_s+R_{sw}}\sum_{n=-\infty}^{+\infty}\frac{(R_s-R_s//R_{sw})C_p\omega_{LO}}{(1+nN)\left[1+(1+nN)^2(R_s//R_{sw})^2C_p^2\omega_{LO}^2\right]} \tag{3.5}$$

Therefore, from Eq.(3.3) the new center frequency of the N-path filter can be computed and it can be noticed (Eq.(3.6)) that it is shifted to lower frequency:

$$\omega_c=\omega_{LO}-\frac{Imsinc^2(\frac{\pi}{N})}{NC} \tag{3.6}$$

Modelling the input impedance of the filter with a RLC tank (Fig.3.13d) is useful to understand the origin of the losses of the filter due to the capacitance. The values of the components are described in the following equations:

$$\frac{1}{R_m}=Re-\frac{1}{R_s+R_{sw}}\frac{1+(R_s//R_{sw})R_sC_p^2\omega_{LO}^2}{1+(R_s//R_{sw})^2C_p^2\omega_{LO}^2} \tag{3.7}$$

$$C_m=\frac{NC}{2sinc^2(\frac{\pi}{N})} \tag{3.8}$$

$$L_m=\frac{1}{C_m\omega_{LO}^2} \tag{3.9}$$

It results that only the resistive part of the tank is affected by the parasitic capacitance, indeed R_m decreases as C_p increases, causing filter losses.

In summary, the effect of parasitic capacitance of a N-path filter causes:

- lowering of the effective impedance, reducing the peaking of the bandpass filter
- shifting of the center frequency with respect to the desired value

The higher the switching frequency, the worse is the filter behaviour. Reducing the harmonic contents of the filter, which corresponds to an increase in the number of phases, can mitigate this effect. In fact, shortening the switching time will also minimize the charge sharing between C and C_p. However, if most of the parasitic capacitance is due to the switches, then increasing the number of phase is not a suitable solution.

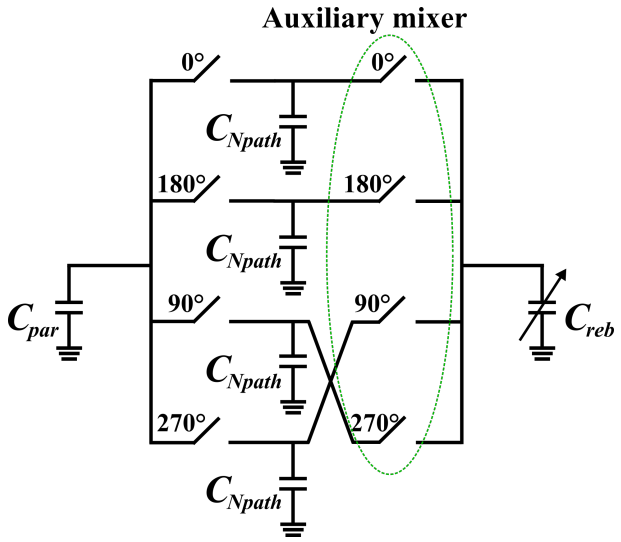


Figure 3.14: N-path filter with rebalacing auxiliary mixer

3.2.3 Rebalancing auxiliary mixer

Considering the proposed transmitter, the N-path filter, introduced as load of the second stage, really suffers the issue of parasitic capacitance, especially as concern the alignment of the center frequency with the carrier frequency.

This happens because the RF nodes of this filter, corresponding to the output of the second stage and the input of the third one, see a big parasitic capacitance, despite it has been minimized as much as possible during the layout drawing.

For this reason, as shown in Fig.3.11, the center frequency of the loop gain is shifted at a lower frequency. In literature, different solution to correct this alignment can be found [18], based for instance on G_m cells. The same option can be adopted also for the closed-loop TX, but it will cost extra power consumption, directly proportional to the amount of phase shifting.

It is instead possible, introducing an auxiliary mixer, to perform the rebalancing operation without increasing considerably the power consumption and the complexity of the system. As reported in Fig.3.14, an auxiliary mixer is added at the base-band side of the filter.

It samples the voltage stored on the N-path capacitors, due to the RF parasitic capacitance C_{par} and it up-converts it on a variable capacitance C_{reb}, whose purpose is to emulate the RF parasitic. However, the order of the sampling phases in the auxiliary mixer is opposite with respect to the N-path one. For this reason, when the voltage produced on C_{reb} is down-converted on the N-path capacitors, it appears as the image signal of the one produced by C_{par}, thus the two signals cancel out, reducing the shifting effect.

Fig.3.11 reports the simulated loop gain when the auxiliary mixer is not active and for different values of C_{reb}. It pops up that the peak has been moved back to the original

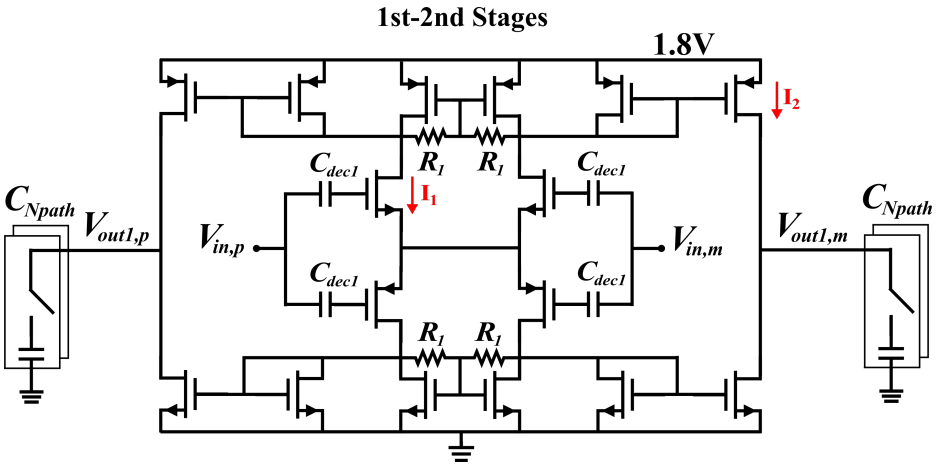


Figure 3.15: RF OpAmp first and second stage

center frequency, which corresponds to a symmetrical loop behaviour with respect to the carrier frequency.

Unfortunately, the peak gain is reduced, because of switched-capacitors contributions caused both by the N-path and the auxiliary mixer. However, as also presented in literature, the peak can be re-aligned but the losses cannot be recovered.

It results that a good trade-off between alignment and peaking needs to be found, when dealing with this kind of applications, which is the reason of having a degree of freedom in activating and de-activating the auxiliary mixer (through external programmability) as in the proposed architecture.

3.3 Three-stage RF operational amplifier

This section gives a detailed description of the RF amplifier topology. The first stage provides 12 dB of broadband differential gain. The second stage consists of a push-pull transconductor loaded by a differential N-path filter, clocked at the carrier frequency (f_{LO} equivalent to 1GHz). Eventually, the output signal is provided by the third stage, a push-pull cascoded transconductor.

The N-path filter, introduced to keep the circuit differential stability under control, is seen by common-mode (CM) signals as a large capacitive load. In addition, the up-conversion mixer pole is also present. It follows that common-mode stability could be undermine.

Fig.3.15 shows the schematic of the first and second stages of the RF amplifier.

The first stage design has been carried on, in order to drastically reject CM signals up to frequencies well above the carrier, still providing at the same time enough gain to achieve the required linearity and noise performance.

The NMOS-PMOS input stage presents AC coupled inputs, allowing to bias the NMOS and PMOS with different DC voltages provided by the circuit in Fig.3.16. Basically,

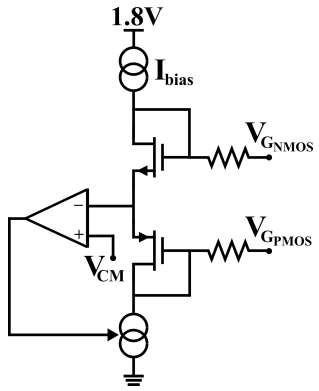


Figure 3.16: Bias circuit of the RF OpAmp first stage

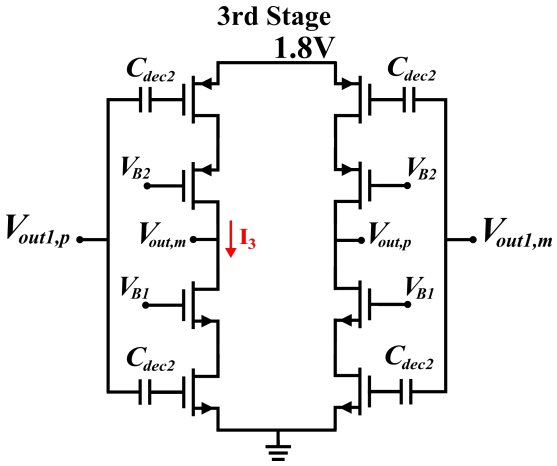


Figure 3.17: RF OpAmp third stage

a current source injects the desired bias current (or a scaled replica) in two diode-connected devices (NMOS and PMOS respectively) stacked onto a tail current source, whose current is closed-loop controlled.

In fact, the proposed circuit Fig.3.16 is not only able to properly bias the gate of the NMOS and PMOS devices, but it also sets the CM node (the sources of the two devices) to a desired voltage. In fact, when the CM voltage departs from the target value, the closed loop control, implemented with a simple operational amplifier (classic differential pair with active load), changes the tail current value, in order to return to the supposed operating condition. For this reason, the amplifier bias can be easily scaled down with the supply voltage, as well as for the current.

Considering the small signal behaviour, the topology of Fig.3.15 basically consists of two back-to-back CMOS differential pairs, which exploits current-reuse mechanism that helps achieving a differential transconductance equal to twice the transconductance (g_m) of each transistor. It follows lower current consumption and noise.

The differential pairs presents an active load of current mirrors that easily bias the second stage, where the signal currents are also recombined.

On the other hand, the common-mode transconductance corresponds to the parasitic conductance to ground at the common-source node. At the same time, the CM load impedance is twice smaller than the differential one, further increasing the required common-mode rejection.

The bias currents are $I_1 = 608\mu A$ and $I_2 = 2.4mA$. The input decoupling capacitance is $C_{dec1} = 2pF$, while the load resistance is $R_1 = 2k\Omega$.

The third (output) stage, reported in Fig.3.17, implements a cascoded class-A/B push-pull topology that directly drives the differential load. This in quite innovative, with respect to the state-of-the-art transmitters. In this way, the output voltage swing is constrained between the supply rails, making the architecture compatible with deeply scaled transistors even for 1.8V supply.

Despite the voltage swing (i.e. the voltage efficiency) is about halved, the current efficiency is doubled, keeping the overall efficiency almost constant. Moreover, different from all the previous transmitter, the output stage that is the output driver is included in the feedback loop, allowing the output signal to closely approach the rails, without degrading the linearity performance. In fact, as already demonstrated in the previous section, the distortion of this stage is killed by the loop, as in a usual closed-loop operational amplifier.

The bias current is $I_3 = 4mA$. The input decoupling capacitance is $C_{dec2} = 8pF$. The cascode bias voltages are internally set by a resistive voltage divider to the nominal condition of $V_{B1} = 1.2V$ and $V_{B2} = 0.6V$, in order to leave enough voltage headroom to the transconductor devices, when large signal occurs.

The output stage is actually implemented with sliced version of the circuit reported in Fig.3.17, introducing a programmability degree of freedom. This helps reducing the static current in case of low power delivering, in order to maintain good efficiency even in this condition.

The differential output is eventually converted to single-ended, by an on-chip balun with a turns ratio close to 1.

Chapter 4

Prototype and measurements

In this chapter the prototype measurement results are reported and compared with the state-of-the-art solutions.

4.1 Systems considerations

The emission generated by the transmitter in the adjacent receiver bandwidths constitutes one of the main challenge in TX design. This becomes even more important in the state-of-the-art SAW-less applications. In fact, SAW filters do not represent an option in wideband systems, since they are bulky, costly and lossy. Above all, these are narrow band filters, characterized by en extremely low tuning capability.

For this reason, reducing TX signal emission has become a key point to meet modern standard requirements of:

- out-of-band noise
- linearity

4.1.1 Out-of-band noise

If on the receiver side of the chain the in-band noise is crucial, for transmitter the biggest issue is represented by the noise out-of-band. The traditional approach was to put a SAW filter before the power amplifier to eliminate this undesired leakage, however, as already mentioned, in recent years SAW-less applications are in order.

Therefore, a low-noise transmitter must be designed, optimizing the structure to provide some filtering along the chain.

Considering the proposed architecture (Fig.3.9), the main noise contributors (according to theory and simulations) near the carrier frequency are represented by the feedback resistors, followed by the base-band resistors. Then, the third contribution is given by the amplifier input stage, whose noise transfer function would increase as the mixer up-converted impedance drops.

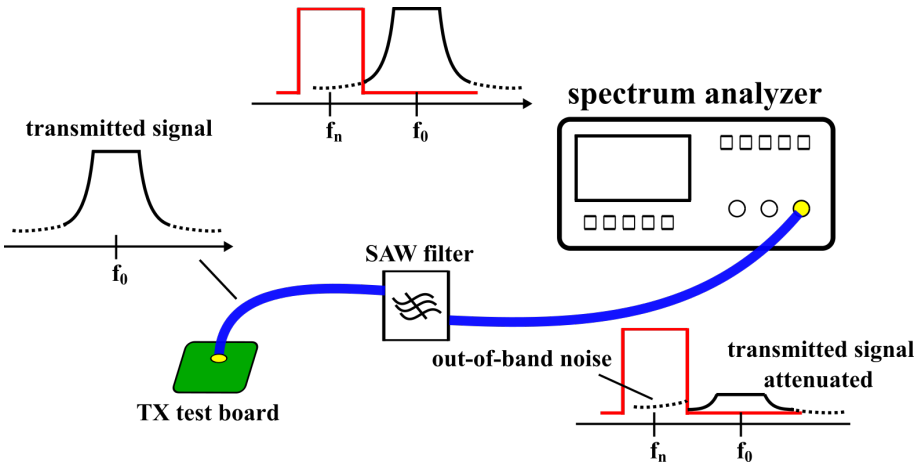


Figure 4.1: Out-of-band noise measurement setup

The resistors R_z added in series to the mixer, not only improve the stability margin (as explained in the previous section) but they also avoid the up-converted impedance dropping, keeping the noise of the first stage at an acceptable level, until the filtering effect of N-path occurs at large frequency offsets.

The procedure to measure output noise emission of an integrated transmitter is usually the following: the RF output is connected to the spectrum analyzer through a SAW/duplexer filter chosen accordingly to the signal carrier. In this way, the stop-band of the external filter will attenuate the transmitted signal, while the noise will pass unchanged, with the exception of the insertion loss.

Thus, the noise can be measured avoiding the instrument saturation as shown in Fig.4.1.

Actually, when the LO signals are provided with an external signal generator to the on-chip dividers, a further SAW filter is used to attenuate the phase noise of the aforementioned instrument.

Finally, it must be said that, it is quite hard to discriminate between noise and non-linearities, during this kind of measurements, especially when the transmitted power reaches the peak values.

For the proposed prototype the LO frequency has been set to 965 MHz, with a signal frequency of 970MHz, delivering a power of 3 dBm after de-embedding the losses. In this condition, the measured output noise at 80 MHz offset from the carrier is -153.5 dBc/Hz.

4.1.2 Linearity

4.1.2.1 ACLR

The Adjacent Channel Leakage Ratio(ACLR) or Adjacent Channel Power Ratio(ACPR) measurement gives information about the linearity of the transmitter [20, 21]. This kind

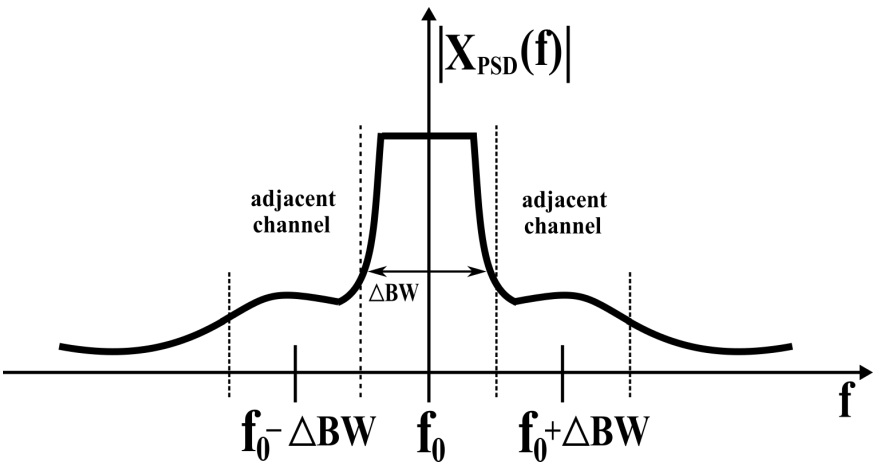


Figure 4.2: Adjacent channel emission spectrum

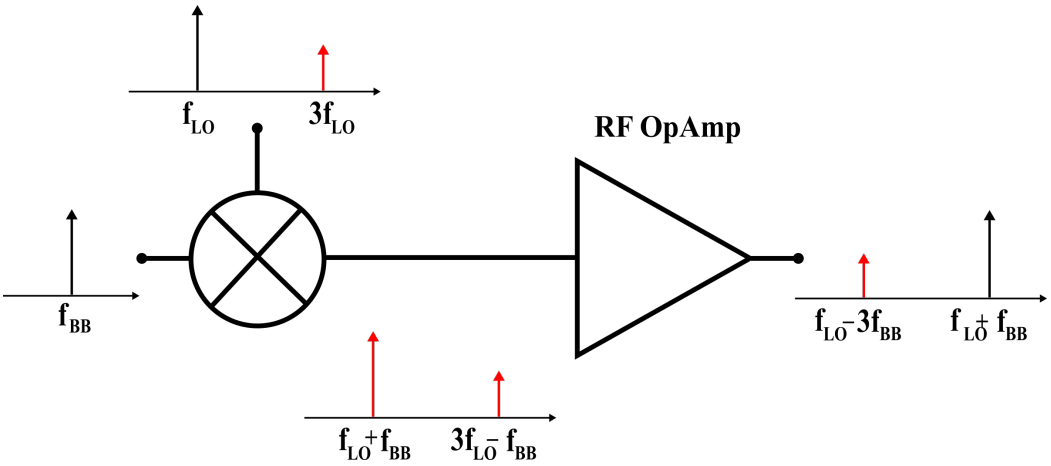


Figure 4.3: CIM3 generation

of unwanted emissions should be firmly restricted such that interference with the other radio systems is kept low.

The adjacent channel emission level is one of the most important parameter in TX architecture. It is generally defined as the ratio between the adjacent channel power, integrated on a specific bandwidth, and the total delivered power in the transmission channel as reported in Eq.(4.1):

$$ACLR = \frac{\int_{f_0-\Delta BW/2}^{f_0+\Delta BW/2} PSD(f)\,df}{\int_{f_0-\Delta 3BW/2}^{f_0-\Delta BW/2} PSD(f)\,df} \tag{4.1}$$

where $PSD(f)$ is the Power Spectrum Density of the transmitted signal. This concept is clarified in Fig.4.2.

Basically, the adjacent channel powers come from spectral regrowth and non-linearity of the amplification stages, which in the proposed architecture are reduced by the closed-loop operations.

4.1.2.2 CIM3

The Counter third order intermodulation products (CIM3) is more and more recognized as another important linearity parameter in transmitter characterization. As reported in [22], the CIM3 results from the 3rd-order intermodulation (IM3) product of signals around f_{LO} and $3f_{LO}$ when using 25% or 50% duty-cycle LO signals for mixer driving.

In fact, if the frequency of the input signal is equal to f_{BB}, after the up-conversion mixer and the RF amplifier, the desired transmitted signal at $f_{LO}+f_{BB}$ will be produced, together with an undesired CIM3 component at $f_{LO} - 3f_{BB}$.

In particular, for 25% duty-cycle LO, after the up-conversion of the base-band signal (f_{BB}), assuming a lower sideband I-Q rejection, the mixer output will show a component at $f_{LO}+f_{BB}$ and $3f_{LO}-f_{BB}$. These two tones are intermodulated by the non-linearity of the amplifier, resulting in an intermodulation product at $f_{LO} - 3f_{BB}$ at the transmitter output (Fig.4.3).

From this rationale, it becomes clear that in order to reduce CIM3 contribution, the odd harmonics of the LO signals should be suppressed. Different solutions have been proposed in literature, such as harmonic rejection, but most of them requires calibration or off-chip filtering components.

On the other hand, another possibility is to modify the LO signals duty-cycle or number of phases, in order to suppress the LO harmonics. However, this solution, which is actually the most suitable for the proposed transmitter, will put extra design effort on the LO signals generators (dividers), implying above all an increase in power consumption that will reduce the overall architecture efficiency.

4.2 Measurement results

The chip prototype, highlighted in Fig.4.4 belongs to a multi-project chip, implemented in TSMC 28nm CMOS technology and its active area is equivalent to $0.28mm^2$. In order to perform the testing, the chip has been bonded on a dedicated printed circuit board (PCB) designed with the software Autodesk EAGLE.

An on-chip digital interface allows to turn on and off the desired circuit in the multi-project chip. The programmability bits are provided off-chip by the SPI (serial peripheral interface) NI USB-8451 (National Instruments), controlled by the dedicated software. Once the chip is correctly programmed, it is biased through National Instruments current (NI-9265) and voltage (NI-9263) modules, mounted on the National Instrument chassis cDAQ-9171 (Chassis compactDAQ).

The chip was tested with an operating frequency equal to 1GHz, with the exception of out-of-band noise measurements, where the LO frequency has been moved to 965MHz.

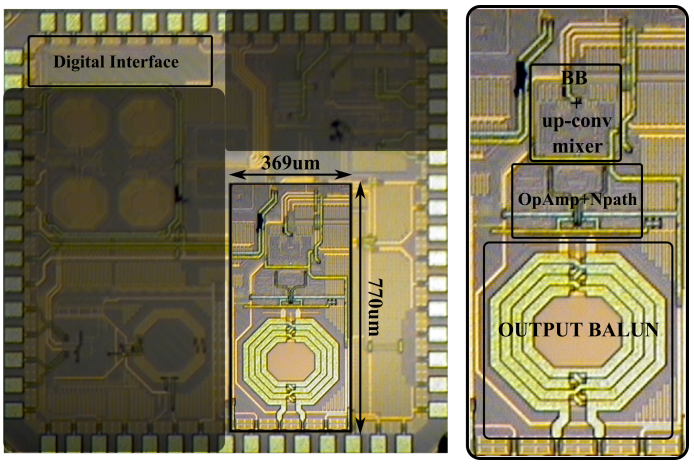


Figure 4.4: Chip prototype

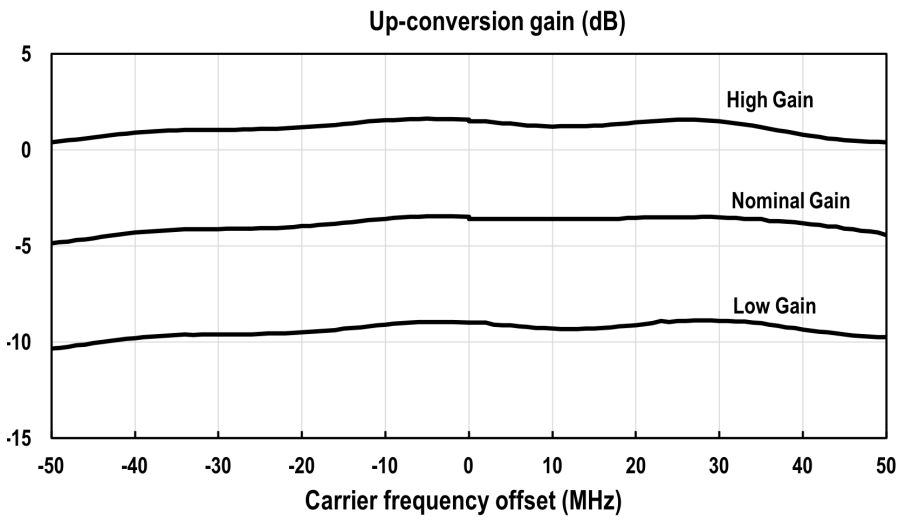


Figure 4.5: Up-conversion gain

The LO signals are provided by the Agilent N5183A MXG signal generator and the 25% duty-cycle is obtained with an on-chip divider.

The BB signals in case of a single-tone or two tones test are given by the Agilent E8257D PSG signal generator, while in case of modulated signal test the input is provided by Agilent E4438C ESG Vector Signal Generator.

The output signal has been observed on the PXA Signal Analyzer N9030A.

The transmitter is able to achieve a maximum measured output power, delivered to the load of 8 dBm, after de-embedding the cable and PCB (printed circuit board) losses (around 1.7 dB).

The up-conversion gain is reported in Fig.4.5. The base-band resistors, as well as the feedback one can be programmed through a digital interface. In fact, it is possible to reduce their value in order to increase or decrease the up-conversion gain by 5 dB. It

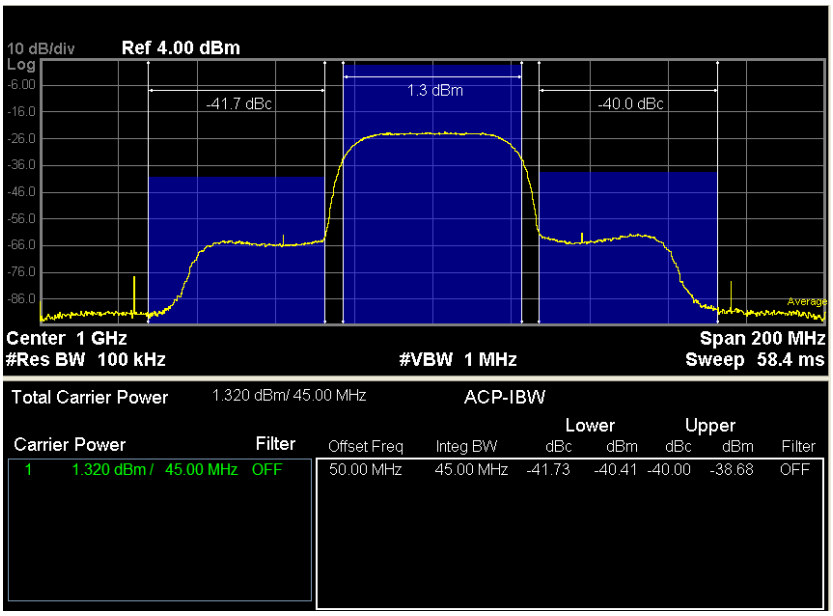


Figure 4.6: ACLR with modulated output spectrum

is noticeable that, in all the three gain configurations, a signal bandwidth exceeding 100MHz has been measured, aligned with the state of the art required bandwidth.

The measured output spectrum for a QPSK 50MHz-RF bandwidth modulated signal is reported in Fig.4.6. The ACLR, in this condition, is equal to -40 dBc, for a corresponding output power of 3 dBm.

Fig.4.7 shows the output spectrum for a single-tone input signal corresponding to 3.9 dBm output power, where the CIM3 is -47 dBc. The CIM3 has also been measured for different BB frequency, with respect to the output power and the results are reported in Fig.4.8. The CIM3 behaviour is quite interesting, in fact, for an output power of 3 dBm its value is better than -49 dBc for single-tone frequency offsets up to 25MHz.

As already mentioned, the out-of-band noise, considering an output power of 3dBm at a frequency offset of 80MHz away from the carrier, corresponds to -153.5 dBc/Hz. The measurement setup is reported in the previous section (Fig.4.1).

Table 4.1 summarizes the prototype measurements, in comparison with the state-of-the art solutions that implement different kind of architectures, the one analysed in Chapter 2. The active area of the proposed transmitter is lower than all the other topologies that also have an on-chip balun, at the same time it is not much bigger with respect to the solutions with an external balun.

The most noticeable result is represented by the RF bandwidth, which is equal to 50MHz. This value is more than twice with respect to the other implementations.

Although a wider bandwidth has been achieved, the other performance are aligned with the state-of-the art. In fact, considering 3 dBm of average output power, the

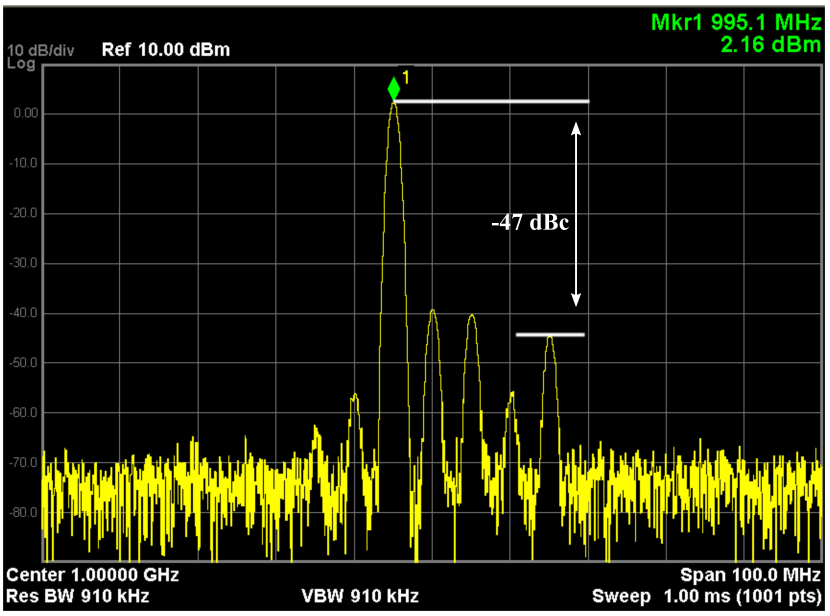


Figure 4.7: CIM3 at 3.9 dBm output power spectrum

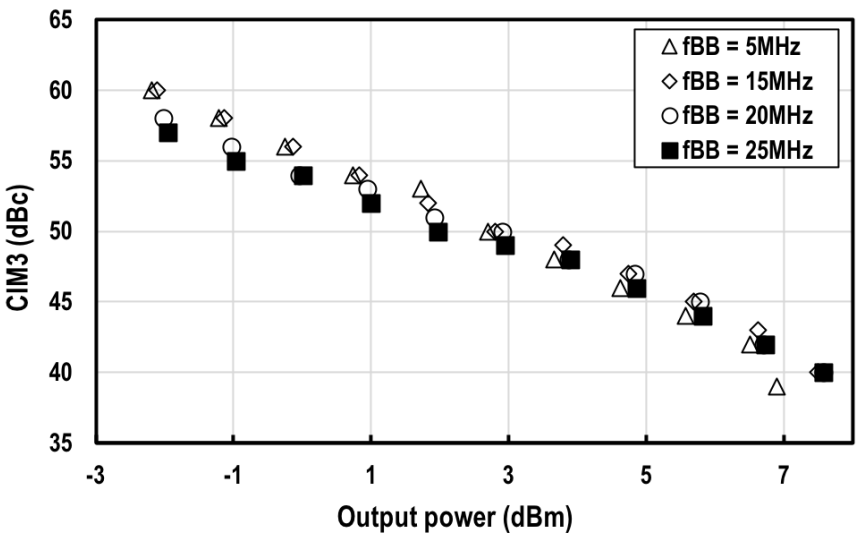


Figure 4.8: CIM3 for different single tone output power and BB frequency

ACLR is -40 dBc and CIM3 is -49. These values are close to the one of [6], which also exploits a current-mode passive mixer, but reaching a 4 dB lower delivered power.

Other implementations, such as [2, 4], achieve better results but exploiting digital pre-distortion. [5] shows very good CIM3, attained trapping the third harmonic of the LO signal, unfortunately this is not beneficial for the ACLR, which is almost equal to the one achieved in the proposed TX, but with a narrow band.

The out-of-band noise has been measured with a carrier frequency of 965MHz and a signal frequency of 970MHz. The delivered power is equal to 3 dBm, after de-embedding

	This work	[1] ISSCC'13	[3] ISSCC'15	[4] ISSCC'16	[2] ISSCC'17	[5] ISSCC'18	[6] ISSCC'16
Technology	28nm	55nm	28nm	28nm	28nm	14nm FinFET	65nm
Architecture	Closed loop passive power mixer	Power mixer	QDAC	RQDAC	ΔΣ+MS DAC	Notch filter mixer	SC GLoop+ Gain boost Npath filter+ PAD
Integrated balun	YES	YES	NO	NO	YES	YES	NO
Chip area [mm^2]	0.28	1.3	0.25	0.22	0.82	1.04	0.038
Supply Voltage[V]	1.8/1.2	1.8	0.9/1.8	0.9/1.1	0.9/1.5	NA	1.1/2.5
Power Cons. (Pout) [mW]	57.6 (3)	101 (4)	41.3 (1)	11.1 (-3.5)	150 (3)	113.2 (3.1)	31.3 (-1.2)
Pout max [dBm]	8	6	1	3.5	3	6.3	-1.2
RF BW [MHz]	50	20	20	20	20	20	10
η(Pout) [%]	3.7 (3)	2.4 (4)	3 (1)	4 (-3.5)	1.3 (3)	1.8 (3.1)	2.4 (-1.2)
CIM3(Pout) [dBc]	-49 (3)	-57.1 (2.3)	<-50 (1)	<-50 (-3.5)	-67 (3)	-62.6 (2.1)	-49 (-1)
ACLR(Pout) [dBc]	-40 (3)	-40.9 (4)	-42 (1)	-49 (-3.8)	-61 (0.9)	-44.7 (3.1)	-41.6 (-1.2)
Pre-distortion	NO	NO	NO	YES	YES	NA	NO
Noise @offset [dBc/Hz]	-153.5 @80M	<-154	-155 @45M	-158 @45M	-155 -163	-157.8 @80M	-156 @45M

Table 4.1: Table of comparison

the losses of the SAW-filter used to perform the measurements. Its value is -153.5 dBc/Hz, at a frequency offset of 80MHz.

Another outstanding results for the closed-loop TX, considering the lack of an external PA, is the maximum delivered output power that corresponds to 8 dBm, which is the highest compared with the competitors.

The power efficiency of the proposed design achieves 3.7% for a delivered power of 3 dBm. This is the best result with respect to the other designs, with the exception of [4]. Nonetheless in [4], the maximum transmitted power is 4.5 dB lower and it also relies on pre-distortion.

Chapter 5

Conclusion

In the first part of this dissertation, a closed-loop transmitter based on current-mode passive mixers has been presented.

The base-band stage performs a voltage to current conversion, while introducing a low-pass filtering function, with a cut-off frequency of 100MHz, which represents the signal bandwidth.

The up-conversion passive mixer combines the I and Q currents into a RF virtual ground, implemented with a three-stage RF amplifier enclosed into a wideband resistive feedback.

The first stage of the OpAmp is a current-reuse pre-amplifier, realized with two back-to-back differential pairs that allows to achieve a wideband differential gain, while strongly rejecting the common-mode signals. Its output currents are recombined into a DC-coupled transconductor, which drives a N-path circuit that ensures the circuit stability. Finally, the output stage is a push-pull cascoded transconductor that constraints the output signal within the supply, allowing circuit scalability.

The closed-loop structure improves the linearity performance suppressing the output stage non-linearities, without pre-distortion, keeping the efficiency quite high.

Measured results shows a RF bandwidth of about 50MHz. Considering a 3 dBm delivered power, the average power consumption at 1.8V of supply voltage is around 57.6 mW, resulting in an efficiency of 3.7%. The ACLR is -40 dBc, while the CIM3 is -49 dBc. The noise at 80MHz offset from the carrier is -153.5 dBc/Hz.

Part II

A TVWS LNTA with Balanced Output Employing a Low-Noise Current Multiplier

Chapter 6

System considerations

The second part of this dissertation deals with the 40nm design and simulations of a low-noise transconductance amplifier for TVWS applications. The standard covers a sub-GHz spectrum range and demands a broadband solution, as most of the cases in modern communications. An architecture analysis, concerning RX IIP2 is also presented in this chapter. Most of the material here presented comes from [23] (IEEE copyright 2017) and [24] (Elsevier copyright 2018).

6.1 TV-White Space environment

Recently, an efficient utilization of the available radio spectrum is becoming an important issue in signal communication. The frequency band from 54 to 862 MHz shows several "spectrum holes", also known as "white spaces", resulting from the transition from analog to digital TV. In these available channels, the spectrum is used just for a small fraction of time or even not used at all. Fig.6.1 gives a qualitative illustration of the explained spectral distribution.

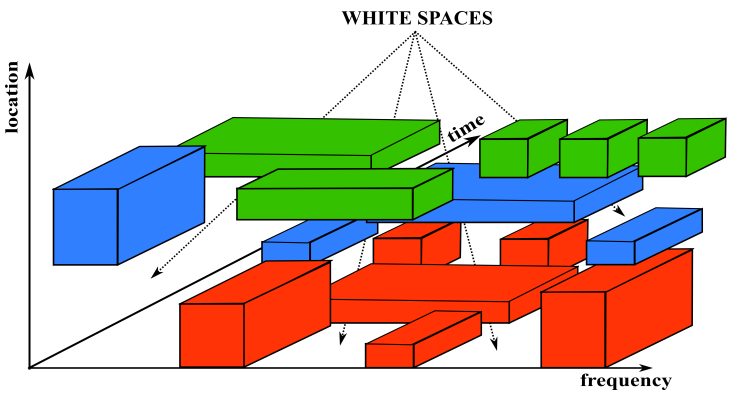


Figure 6.1: Spectrum holes

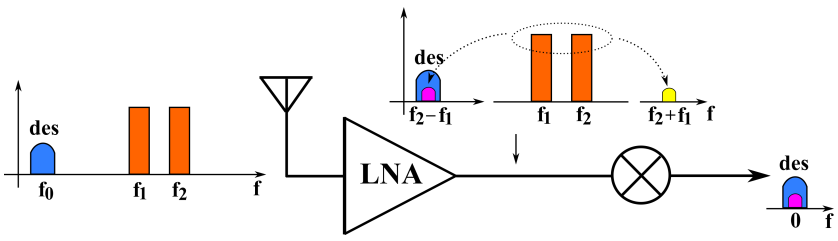


Figure 6.2: Second order distortion in wideband receiver

In order to increase the spectrum utilization efficiency, new advanced techniques such as spectrum sensing have been proposed, allowing dynamic spectrum allocation strategy [25]-[26]. From the radio terminal point of view, the "white spaces" environment presents several challenges not only in terms of wideband spectrum sensing but also in detection and avoidance of big interferers [27–30].

In conventional architecture based on narrow-band receiver, the large out-of-band (OOB) interferers are eliminated by fixed-frequency external pre-selection surface acoustic wave (SAW) filters, which however are bulky, expensive and not tunable [31–33].

For this reason, the general trend is to replace these filters with on-chip circuit solutions, moving the bottle-neck to receiver design that needs to achieve wide bandwidth and high linearity. Different proposal have been focused on IIP3 improvement [34, 35]. Nonetheless, IIP2 is as well important.

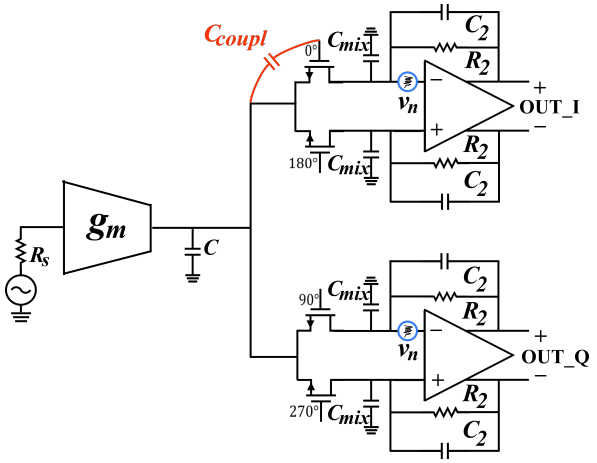
As reported in [36], considering the wideband input spectrum, LNA IIP2 is a big concern. The spectrum profile of a classical wideband environment is shown in Fig.6.2, where even before down-conversion, the IM2 product of two interferers at frequency f_1 and f_2 may fall on top of the wanted signal (as f_2-f_1). Moreover, the use of external balun should be avoided to lower costs and area consumption.

Considering all the previous requirements, a single-ended input balanced output low-noise transconductance amplifier (LNTA) is a suitable candidate to be implemented into a receiving chain for TVWS applications.

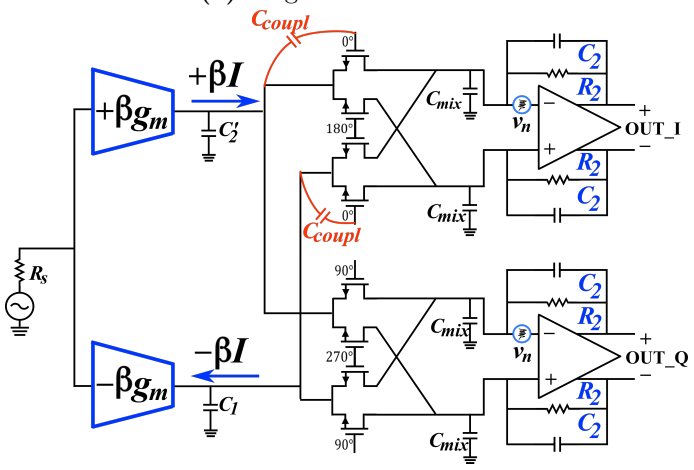
6.2 Architecture analysis

The TVWS environment is characterized by several, large interferers, even up to -8 dBm [25], which distribute along the wide bandwidth. Therefore, in this scenario, receiver design is very demanding in terms of linearity that becomes a key challenge, introducing the need of high IIP2 and IIP3.

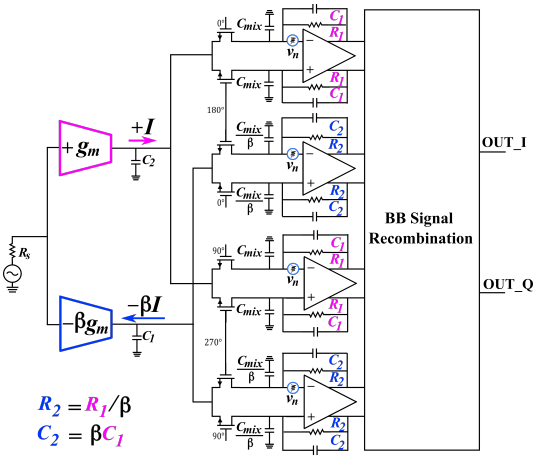
The current-mode receiver, as stated at the beginning of this dissertation, represents the most suitable architecture that allows to achieve high linearity and broad bandwidth. The LNTA output signal, which can be either single-ended or differential, is processed by passive mixers and baseband (BB) transimpedance amplifiers (TIAs).



(a) Single-balanced mixer



(b) Double-balanced mixer



(c) Noise-canceling RX with unbalanced RF currents and BB recombiner

Figure 6.3: Receiver architectures

In literature, different techniques to improve the receiver IIP3 such as derivative superposition, feedback and post-distortion [35] has already been proposed, since third-order intermodulation and linearity have been deeply investigated in recent years, due to the standards stringent requirements. For this reason, this analysis will mainly focus on IIP2, which in a direct down-conversion receiver is usually degraded by the mixer [36] [37] [38] that produces second-order intermodulation (IM2) terms because of four mechanisms: 1) threshold (V_{th}) and 2) size (β) mismatch of the MOS devices working as mixer switches; 3) coupling of the RF signals to the LO lines and 4) coupling of the LO signals to the RF lines.

The architecture of the receiver strongly affects the second-order intermodulation product. In Fig.6.3a, a receiver model, where the LNTA presents a single-ended output and the mixer is single-balanced is reported; otherwise Fig.6.3b shows a balanced output LNTA followed by a double-balanced mixer. Typically [39], broadband noise-cancelling receivers present, before down-conversion, differential but unbalanced signals.

This architecture (Fig.6.3c) consists of two single-balanced mixing paths, which present different base-band transimpedance gain, to achieve noise cancellation together with a further BB recombination stage. In this case, it is possible to examine the circuit, as concern the IIP2, as a single-balanced down-converter.

In Fig.6.4, the simulated IIP2 for a SB and a DB receiver are reported, where the effect of the previous four mechanisms can be studied one at a time. It can be noticed that the IIP2 of SB and DB down-converters is equal and quite high in case of β or V_{th} mismatch (Fig.6.4a and Fig.6.4b).

On the other hand, Fig.6.4c shows the IIP2 due to coupling effects between the LO and the RF signal lines, modelled with a capacitor C_{coupl}. This is often the dominant contributor in a single-balanced down-converter, where a large IM2 generates if the LO signal couples with the single-ended RF line. Instead, in the double-balanced mixer, the undesired signal couples onto differential lines; therefore, to a first order approximation it can be seen as a common-mode contribution. For this reason, the IIP2 of a SB receiver is expected to be much worse with respect to the DB receiver case, as proved in [39].

On the basis of the previous analysis, for the IIP2 to be high, a double-balanced architecture is required, leading to the need of a balanced outputs LNTA. However, in a broadband scenario, the IIP2 of the LNTA is as well important and could be easily achieved with a fully differential LNTA topology. Unfortunately, this solution needs an input broadband balun, which will potentially limit the bandwidth and increase the costs.

Therefore, the next chapter will describe in deep details a single-ended input balanced output LNTA, with a self-calibration loop for IIP2 optimization. Furthermore, a noise and distortion analysis of the circuit will be provided to support to the design choices.

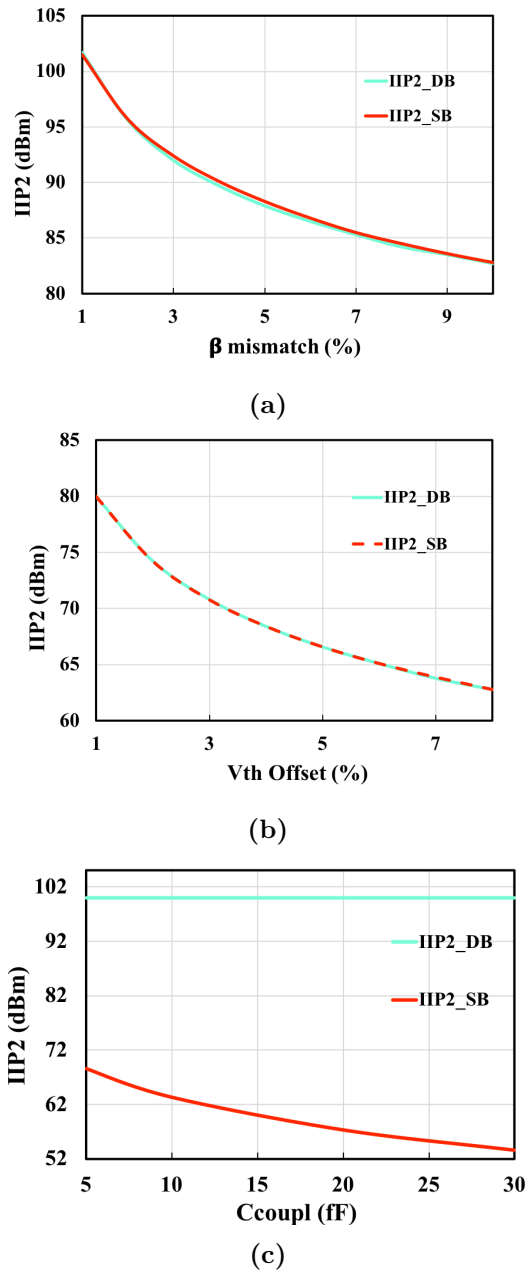


Figure 6.4: Simulated RX IIP2 with SB and DB mixers: a) β mismatch; b) V_{th} mismatch; c) RF-LO coupling

Chapter 7

Circuit description

This chapter reports a review of the LNA aiming at similar applications, presented in literature. An analysis and description of the proposed noise-cancelling LNTA is also proposed, together with linearity and noise considerations.

7.1 Review of noise-canceling Low-Noise Amplifiers

Noise-cancelling architectures perform broadband low-noise amplification, achieving at the same time high linearity performance [39–53]. [40] describes a broadband, inductorless common-gate (CG) common-source (CS) LNTA, where the noise and third order distortion of the former stage (CG) is cancelled out by the parallel high-transconductance of the latter (CS). However, its output is single-ended, making this LNTA not suitable for TVWS or generally speaking, broadband applications.

The LNTAs reported in [41]-[43] present the same issue as the previous architecture. In this case, [41] and [42] exploit the PMOS and NMOS complementary properties to improve the second-order linearity performance, while [43] aims at improving IIP3 through derivative superposition techniques.

[44]-[48] show low-noise amplifiers with differential outputs. In [44] the noise-cancelling condition is fulfilled at the differential output voltage, loading the output of the common-source and common-gate stages with resistors of different values. This rebalancing operation is needed, because (for low-noise) the CS transconductance is larger than the CG one. In [45] and [46] the same topology is improved adding a local feedback between the CG-CS stages, allowing a reduction in current consumption of the common-gate, still achieving noise cancellation.

The introduction of a linear feedback from the common-mode output voltage to the input is a good solution to cancel the IM2 product of the low-noise amplifier as explained in [47]. [48] proposes another interesting topology, consisting of a resistive-feedback

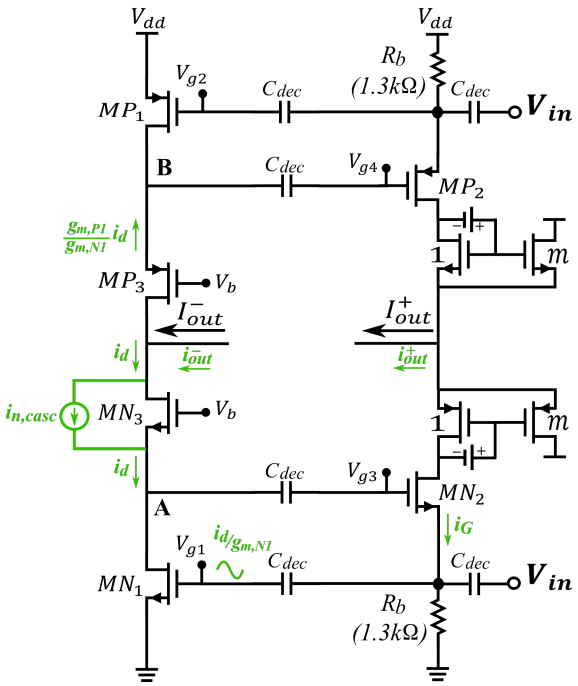


Figure 7.1: Proposed CG-CS noise-cancelling LNTA

LNA, which exploiting an LC tank load, where the inductance value guarantees the output voltage balance, is able to perform tunable band-pass filtering.

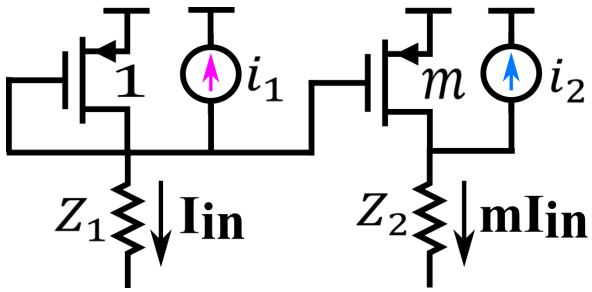
Unfortunately, all the previously presented solutions work with a voltage-mode output with the addition of a further RF transconductor, resulting in early compression and low IIP3.

Moving the voltage amplification and rebalancing operation at base-band level, that means working at RF only in current-mode will help improving the linearity performance, since at BB, large OOB blockers can be easily filtered out [39] (model in Fig.6.3c). The drawback of this architecture comes form RF-LO coupling; in fact, if the LO signal couples on the two unbalanced RF lines, just a small percentage will cancel as common-mode, limiting the IIP2 of the receiver as in a SB mixer front-end. Moreover, to achieve the noise-cancelling condition, the signals at the base-band stage need to be correctly recombined, requiring an additional stage.

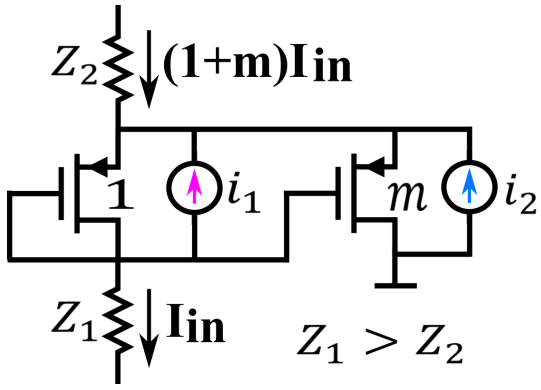
7.2 Proposed noise-canceling LNTA

In order to meet the previously discussed requirements, the proposed LNTA shows a single-ended input and balanced output signals [23]. The topology, reported in Fig.7.1, is an improved version of the classical CG stage, combined with a CS path, to perform noise and distortion cancellation as already reported in the previous section.

The first improvement regards the addition of a local feedback between the CG stage and the cascoded CS stage, which allows to lower the current consumption in the CG



(a) Classic current mirror



(b) MBCM

Figure 7.2: Noise models

branch, as similarly reported in [45]. The second one is the introduction of a mirror-based current multiplier at the output of the common-gate to obtain balanced output signals before down-conversion.

Considering the first point, the gate of the common-gate device MN2 (MP2) is connected to the source of the CS cascode transistor MN3 (MP3), corresponding to node A (B) in Fig.7.1. In this way, the LNTA input impedance is reduced by a factor 1+G, where G is the gain available at node A (B), given by the CS stage acting as an inverting amplifier (i.e. $1+g_{\mathrm{m,MN1}}/g_{\mathrm{m,MN3}}$ or respectively $1+g_{\mathrm{m,MP1}}/g_{\mathrm{m,MP3}}$). In this way, the transconductance of the common-gate device MN2 (MP2) can be reduced, still maintaining 50 Ω matching, leading to the possibility of a lower bias current for the CG branch, which not only means less power consumption, but also the CG can be biased with large resistors, instead of external choke inductors. It follows a reduction in area and cost, an improved bandwidth and still good noise performance.

The LNTA has been designed for G equal to 1, that is cascode and CS devices have the same transconductance ($g_{\mathrm{m,MN3}}$=$g_{\mathrm{m,MN1}}$) and the CG transconductance $g_{\mathrm{m,CG}}$ ($g_{\mathrm{m,MN2}}$+$g_{\mathrm{m,MP2}}$) is about 10 mS.

It is noticeable that the LNTA noise and distortion performance are not degraded, even though the impedance at the source of the cascode devices (MN3, MP3) is lowered by the local feedback, because noise/distortion contribution of MN3 and MP3 is cancelled out at the differential output, as intuitively shown in Fig.7.1. In fact, looking at Fig.7.1,

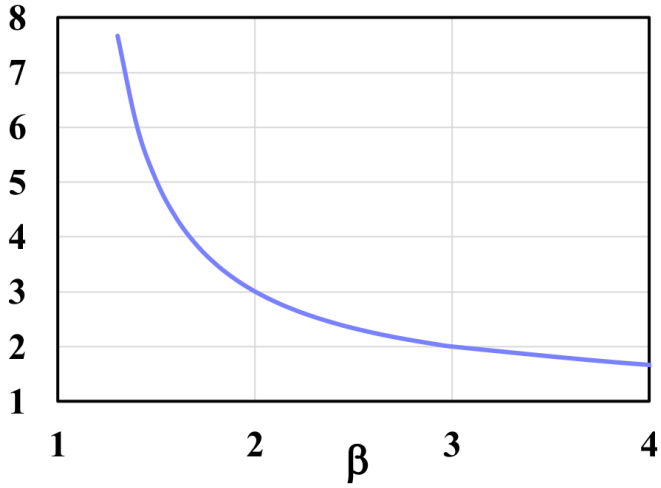


Figure 7.3: MBCM noise reduction factor

noise/distortion of the cascode MN3 is modelled as a current generator i_{casc}. Part of this current (i_{d}) will appear at the drain of MN3 and flow through MN1. This current will cause a voltage $i_{\mathrm{d}}/g_{\mathrm{m,MN1}}$ to appear at the gate of MN1, resulting in a current i_{G} flowing in the common-gate branch as well as a current $(g_{\mathrm{m,MP1}}/g_{\mathrm{m,MN3}})i_{\mathrm{d}}$ flowing into MP1. At this point, the total current at the positive output is $i^{+}_{\mathrm{out}}=\beta(i_{\mathrm{d}}/g_{\mathrm{m,MN1}}R_{\mathrm{s}})$ and the one at the negative output is $i^{-}_{\mathrm{out}}=i_{\mathrm{d}}(g_{\mathrm{m,MN1}}+g_{\mathrm{m,MP1}})/g_{\mathrm{m,MN1}}$. Since $\beta=(g_{\mathrm{m,MN1}}+g_{\mathrm{m,MP1}})R_{\mathrm{s}}$, noise and distortion of MN3 cancel out at the differential output, as well as noise/distortion of MP3.

As regards the second topology improvement, in order to maintain a low noise figure (NF), the transconductance gain of the CS stage $g_{\mathrm{m,CS}}$ $(g_{\mathrm{m,MN1}}+g_{\mathrm{m,MP1}})$ is usually designed to be around 2-4 times $1/R_{\mathrm{s}}$, on the other hand the transconductance gain of the CG is usually equal to $1/R_{\mathrm{s}}$ to ensure input matching. Unfortunately, this will lead to unbalanced RF signals at the output of the two transconductance paths (CS and CG), which will need to be rebalanced prior down-conversion to provide high receiver IIP2.

In order to rebalance the signals, a non-inverting amplification should be apply at the output signal current of the CG branch. [41] exploits a classic current mirror Fig.7.2a. However, this solution introduces considerable noise, while applying an unwanted sign inversion. A mirror-based current multiplier (MBCM) in Fig.7.2b is proposed, exploiting the low loading given by the following mixing stage.

In this circuit, instead of taking the scaled replica of the input current at the drain of the mirroring device, as in a classic mirror, the output is taken at the common source of the two transistors, providing higher gain and correct amplification sign. In fact, the classic mirror provides a current gain β equal and opposite in sign with respect to the mirroring factor m, while in the MBCM the current gain β=m+1.

In the standard mirror, the total input-referred current noise is:

$$i^2_{in,std} = 4KT\gamma g_m(1 + \frac{1}{\beta}) \tag{7.1}$$

Considering equal current gain, the input-referred noise current in the MBCM corresponds to:

$$i^2_{in,MBCM} = 4KT\gamma g_m(1 - \frac{1}{\beta}) \tag{7.2}$$

A noise reduction factor can be calculated Eq.(7.3), taking the ratio of Eq.(7.1) and Eq.(7.2) and its values are reported in Fig.7.3 as a fuction of β.

$$\frac{i^2_{in,std}}{i^2_{in,MBCM}} = \frac{\beta + 1}{\beta - 1} \tag{7.3}$$

It can be noticed that for β up to 4, considered a reasonable set of values in this application, the noise introduced by the MBCM with respect to the standard mirror is much lower. The LNTA has been designed for a β equal to 2, which results in a noise reduction factor of 3.

7.3 LNTA IIP2 analysis and optimization

The previous section widely stressed the importance of the second order inter-modulation in a broadband scenario. Although the receiver has been designed in order to meet the high IIP2 specifics, optimizing the LNTA IM2 is also quite relevant to achieve the application requirements. Indeed, this section deals with the second-order distortion analysis with reference to Fig.7.4. The contribution of the two amplifying stages (CG and CS) are studied one at a time, in order to check which one affects the distortion at most.

The common-gate device MN2 introduces a second-order intermodulation contribution that is modelled with a current source i_{CG}=$g''_{\mathrm{m,MN2}}(1+G)^2 v^2_{\mathrm{in}}$, where $g''_{\mathrm{m,MN2}}$ represents the second-order non-linear transconductance of the CG device MN2 and G is the amplification of the input signal, given by the common-source device MN1 and its cascode MN3 combined in the local loop.

At this point, half of this current i_{CG} is seen at the non-inverting output, amplified by the current gain β, while the other half is absorbed by the source resistance R_{s}, because of impedance matching. This portion of i_{CG} will appear at the inverting output multiplied by a factor $g_{\mathrm{m,CS}}/g_{\mathrm{m,CG}} = \beta$ without changing polarity.

Therefore, the IM2 contribution of MN2 will be rejected at the differential output, where it behaves as a common-mode. This rationale strictly holds for in-band IM2, that is in a frequency range where the impedance matching is strong and it can also be applied to MP2, MN3 and MP3.

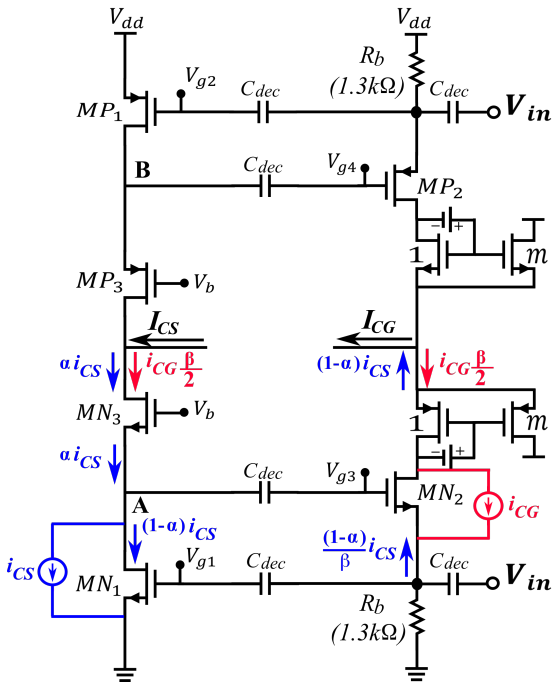


Figure 7.4: LNTA IM2 generation and propagation

Moving the analysis to the common-source device MN1, its distortion contribution is represented with a current source $i_{\mathrm{CS}}=g''_{\mathrm{m,MN1}}v_{\mathrm{in}}^2$. At the drain of MN1, because of the local loop (MN1, MN2 and MN3) the impedance is low, meaning that only a small fraction of i_{CS}, αi_{CS}, will be injected in the inverting output. The other part, $(1-\alpha)i_{\mathrm{CS}}$ will be mirrored at the non-inverting output, multiplied by a factor $1/(g_{\mathrm{m,CS}}R_{\mathrm{s}})$ at first, then amplified by $\beta(=g_{\mathrm{m,CS}}R_{\mathrm{s}})$.

Hence, the IM2 contribution of MN1 (as well as the one of MP1) at the differential output will appear unchanged and equal to i_{CS}, making it the dominant factor in second-order distortion of the LNTA.

A possible solution to adjust the LNTA IIP2 relies on the complementary topology of the amplifier, which allows to cancel out the IM2 exploiting the opposite polarity of the two second-order transconductance of MN1 and MP1.

Usually, the devices are biased around a sweet spot, that unfortunately leads to sharp IIP2 degradation across process corners, voltage and temperature variations [40] [44]. However, the introduction of an automatic control loop is able to keep the LNTA IIP2 under control (Fig.7.5). The PMOS side of the common-source branch is divided into 18 slices: one slice is fixed (always connected), while the others can be turn on and off through control bits (6 binary coded), allowing the control loop to set the effective size of MP1. The common-mode feedback (CMFB) sets the gate bias voltage of MP1 (V_{GMP1}), which in presence of a large RF signal applied at the LNTA input, is able to vary in order to keep the average currents of MP1 and MN1 equal to each other. V_{GMP1}

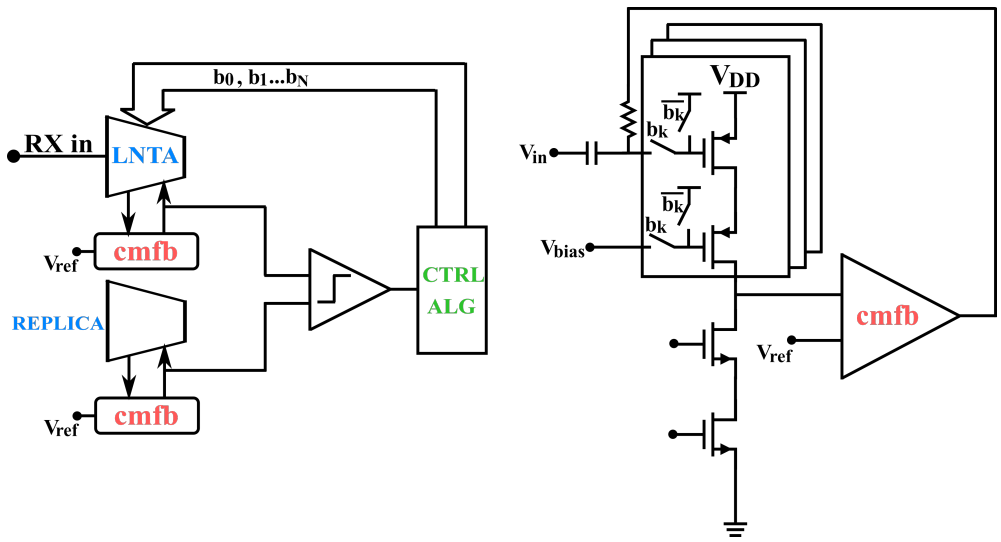


Figure 7.5: LNTA IIP2 automatic control loop

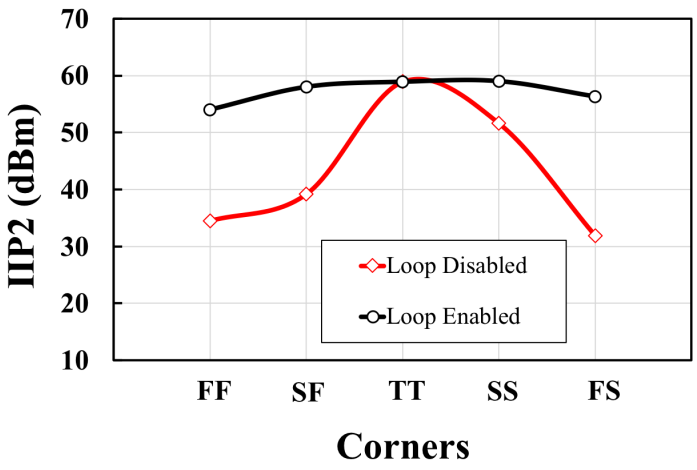


Figure 7.6: LNTA IIP2 with and without optimization

will stay constant, even in presence of a large RF signal, if $g''_{\mathrm{m,MN1}} = -g''_{\mathrm{m,MP1}}$, which represents the optimum condition for IIP2.

This optimum case can be detected considering the variations of V_{GMP1} of the main LNTA with respect to its replica, where no RF input signal is applied. This circuit is turned on just in case calibration is needed, avoiding wasting power. Fig.7.6 reports the comparison between the LNTA IIP2 with enabled and disabled control loop, showing a typical value of 59 dBm that drops to 32 dBm in the worst corner, when the loop is disabled. In case of enabled loop, the IIP2 is ensured to be at minimum 54 dBm across all the corners.

7.4 Baseband noise analysis

In Chapter 6 a comparison between the receiver architectures, claims the double-balanced topology to achieve better performance in terms of second-order distortion with respect to the unbalanced one.

However, the proposed balanced LNTA, suitable for double-balanced mixing (Fig.6.3b) presents an additional advantage, concerning the noise contribution of the BB operational amplifiers. In fact, as already explained, if the LNTA outputs are unbalanced, the need of recombining signals at base-band level demands the use of two single-balanced mixer, each one followed by two TIAs and an extra recombination stage (Fig.6.3b). Moreover, to properly perform signals recombination, the BB stages that follow each SB mixer provide different transimpedance gains.

Modelling the opamps noise with an equivalent input noise source v_{n}, whose power spectral density is $4KTR_{\mathrm{n}}$, where R_{n} is the equivalent noise resistance, a brief comparison of the BB noise contribution in the two architectures can be provided.

Assuming equal total power consumption, each of the four opamps in the unbalanced topology (Fig.6.3c) burns half power with respect to the balanced one (Fig.6.3b). It follows that the equivalent noise resistance R_{n} of the unbalanced BB opamps is twice that in the balanced one ($R_{\mathrm{nUB}} = 2R_{\mathrm{nBB}}$).

Furthermore, taking as reference Fig.6.3, the output load of the LNTA of the balanced and unbalanced receiver is modelled as a capacitance for the CS path as well as for the CG. Therefore, the switched-capacitor approximation described in [54] can be used to compute the base-band driving impedance.

Now, considering the source resistance and the BB stages as the only noise sources, it is possible to calculate the total output noise contributions:

$$v^2_{PORT,out} = 8KTR_s\left(\frac{G_{sig}}{2}\right)^2\frac{\pi^2}{8} \tag{7.4}$$

$$v^2_{R_{nBB},out} = 4KTR_{nBB}2\left[G^2_{n,BAL} + \left(G_{n,BAL} - 1\right)^2\right] \tag{7.5}$$

$$v^2_{R_{nBB},out} = 4KT2R_{nBB}2\left[G^2_{n,UNB1} + \left(G_{n,UNB1} - 1\right)^2 + G^2_{n,UNB2} + \left(G_{n,UNB2} - 1\right)^2\right] \tag{7.6}$$

where:

$$G_{sig} = \frac{2\sqrt{2}}{\pi}\frac{R_1}{R_s} \tag{7.7}$$

$$G_{n,BAL} = 1 + \frac{R_1}{\beta}f_{ck}\left(C_1 + C_2'\right) \tag{7.8}$$

$$G_{n,UNB1} = 1 + \frac{R_1}{\beta}f_{ck}C_1 \tag{7.9}$$

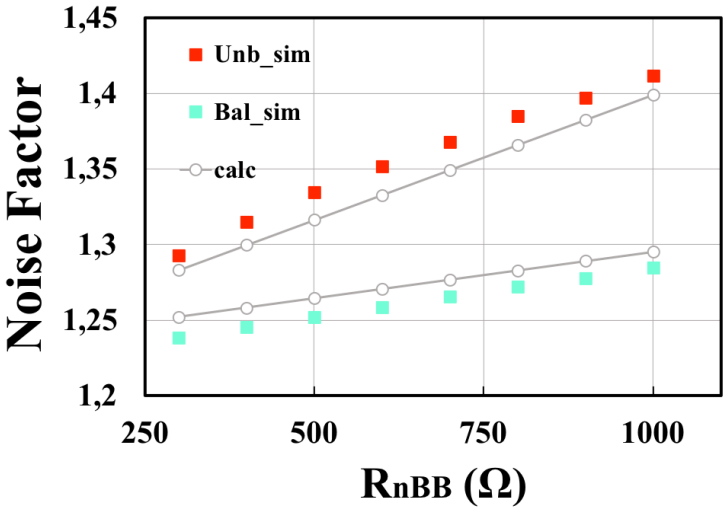


Figure 7.7: Receiver base-band Noise Factor

$$G_{n,UNB2} = 1 + R_1 f_{ck} C_2 \tag{7.10}$$

In this analysis, the load capacitance of the common-source branch is considered equal for both balanced and unbalanced architecture (C_1), while the output load of the common-gate branch in the balanced structure ($C_2^{'}$) is equivalent to the one of the CG branch of the unbalanced (C_2) plus the parasitic capacitance of the mirror-based current multiplier. Combining the previous expressions, the receiver noise factor (F_{BB}) due to BB and source contributions can be calculated in this way:

$$F_{BB} = \frac{v^2_{R_{nBB},out} v^2_{PORT,out}}{8KTR_s\left(\frac{G_{sig}}{2}\right)^2} \tag{7.11}$$

resulting into the following expressions for the balanced and unbalanced architectures respectively:

$$F_{Bal,gen} = \frac{\pi^2}{8}\left\{1 + \frac{4R_sR_{nBB}}{R_1^2}\left[1 + 2\left(\frac{R_1}{\beta} f_{ck}(C_1 + C_2^{'})\right)^2 + 2\frac{R_1}{\beta} f_{ck}(C_1 + C_2^{'})\right]\right\} \tag{7.12}$$

$$F_{Unb,gen} = \frac{\pi^2}{8}\left\{1 + \frac{16R_sR_{nBB}}{R_1^2}\left[1 + (R_1 f_{ck})^2\left(\frac{C_1^2}{\beta^2} + C_2^2\right) + R_1 f_{ck}\left(\frac{C_1}{\beta} + C_2\right)\right]\right\} \tag{7.13}$$

Eq.(7.12) and Eq.(7.13), if $C_1 = C_2 = C_2^{'} = C_{par}$ are approximated as follows:

$$F_{Bal} = \frac{\pi^2}{8}\left\{1 + \frac{4R_sR_{nBB}}{R_1^2}\left[1 + 8\left(\frac{R_1}{\beta} f_{ck} C_{par}\right)^2 + 4\frac{R_1}{\beta} f_{ck} C_{par}\right]\right\} \tag{7.14}$$

$$F_{Unb} = \frac{\pi^2}{8}\left\{1 + \frac{16R_sR_{nBB}}{R_1^2}\left[1 + \left(\frac{R_1}{\beta} f_{ck} C_{par}\right)^2 (1 + \beta^2) + \frac{R_1}{\beta} f_{ck} C_{par}(1 + \beta)\right]\right\} \tag{7.15}$$

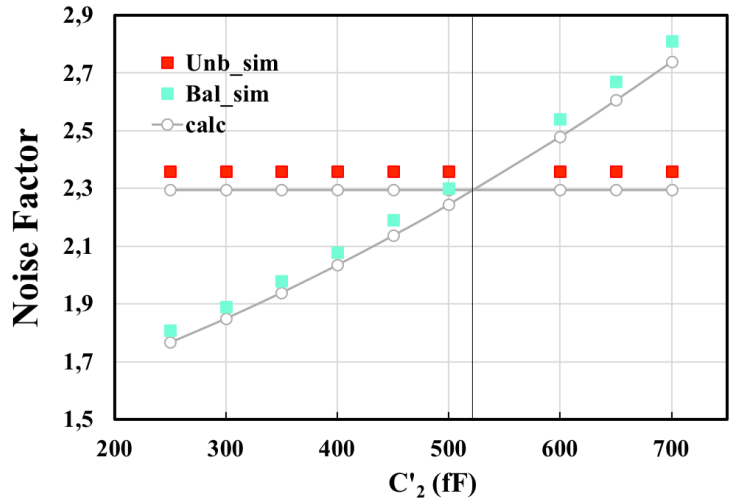


Figure 7.8: BB Noise Factor vs $C_2^{'}$

In the unbalanced topology, a BB transimpedance of the CG path β times higher than that of CS path is required, therefore the opamp noise will be affected by a higher gain. Upon recombination, the CG path will give higher noise contribution, since the output signals are equal.

In the balanced case, instead, the noise is equal to the one of the CS path of the unbalanced receiver.

Fig.7.7 reports the comparison between the calculated and simulated F_{BB} of balanced Eq.(7.14) and unbalanced Eq.(7.15) LNTA receivers as a function of R_{nBB}, considering $\beta = 2$. It can be noticed that to obtain the same F_{BB}, the R_n of the opamp in the balanced architecture can be 2.5 times higher than the one of the unbalanced topology, resulting in significant power saving.

Finally, since good agreement between calculated and simulated results has been observed, it is possible to rely on the computed values of Eq.(7.12) and Eq.(7.13) with respect to $C_2^{'}$, in order to check how greater the parasitic capacitance of the mirror-based current multiplier should be, to make the noise factor of the balanced receiver become worse than the one of the unbalanced.

Fig.7.8 reports the above mentioned results. In particular, $F_{Unb,gen}$ is constant, since it does not depend on $C_2^{'}$; on the other hand, $F_{Bal,gen}$ increases proportionally with $C_2^{'}$, becoming higher than $F_{Unb,gen}$ for $C_2^{'}$ equal or greater than $520fF$.

Considering a CS capacitance $C_1 = 300fF$ and a CG $C_2 = 200fF$, having $C_2^{'} = 520fF$ corresponds to the sum of the CG contribution of 200fF plus a mirror parasitic capacitance of 320fF, which is quite unlikely in very scaled technologies.

Hence, even as concerned noise performance of the entire receiving chain a good design of the balanced LNTA achieves better results compared with the unbalanced counterpart.

Chapter 8

Simulation results

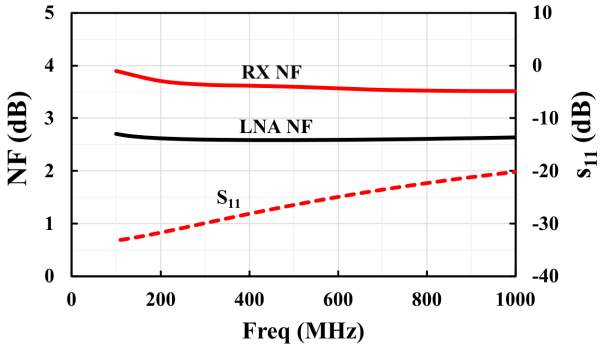
The 40nm design has been simulated and the results are summarized in this chapter, where a comparison table shows the advantages of the proposed solution with respect to the state-of-the-art.

The proposed architecture was designed and simulated in 40nm TSMC CMOS technology, in order to achieve the TVWS requirements. The LNTA, shown in Fig.7.1, is biased with 260 μA in the common-gate branch, while the common-source branch draws 1.45 mA. The total LNTA power consumption is 3 mW, considering the 1.8 V power supply. The diode-connected device of the mirror-based current multiplier presents a battery (resistive voltage drop of 400 mV) and a bypass capacitor, which provides an optimization of the CG branch voltage headroom.

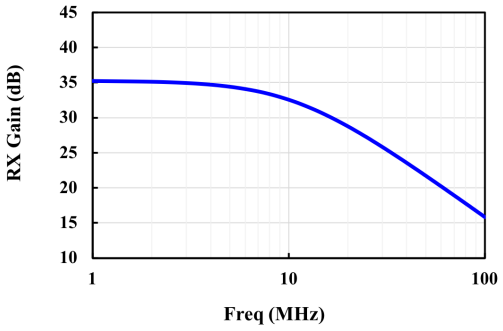
The double-balanced mixer that follows the LNTA is clocked with a 25% duty-cycle LO, injecting the signal current into the base-band stage. The TIA transfer function introduces a 10 MHz pole, which is aligned with the TVWS specifications. The operational amplifier of the BB stage is a three-stage topology with double zero compensation, similar to the solution adopted in [40]. The unity-gain bandwidth is 1.5 GHz, with a

	This work	[40]	[44]	[45]	[43]	[41]
Freq [GHz]	0.1-1	0.8-2.1	0.2-5.2	0.2-3.8	0.3-1	0.15-0.76
Vdd [V]	1.8	1.5	1.2	0.85	3.3	1.8
Pdc [mW]	3	17.4	21	3.2	16	24.4
NF [dB]	<2.6	2.6	<3.5	3.5-4.1	<2.7	2.9
s_{11} [dB]	<-20	-8.5	<-10	<-9	<-11	NA
LNA IIP3 [dBm]	1	16	>0	-3.8	>12	9.5
LNA IIP2 [dBm]	54	NA	>20	NA	NA	NA
Technology [nm]	40	130	65	130	130	180

Table 8.1: Table of comparison



(a) Input return loss (s_{11}) and NF



(b) Down-conversion gain

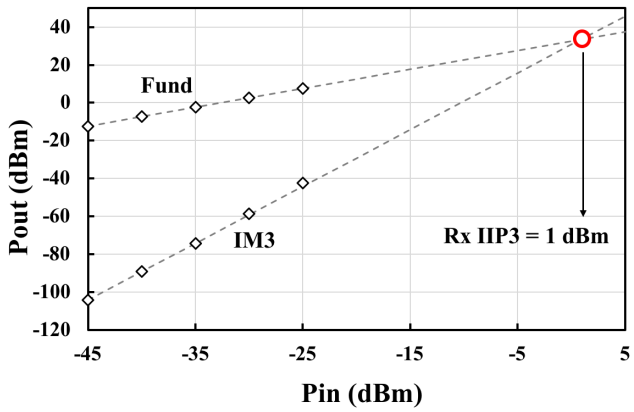
Figure 8.1: Simulation results

current dissipation of 3 mA that corresponds to a signal path power consumption of 13.8 mW.

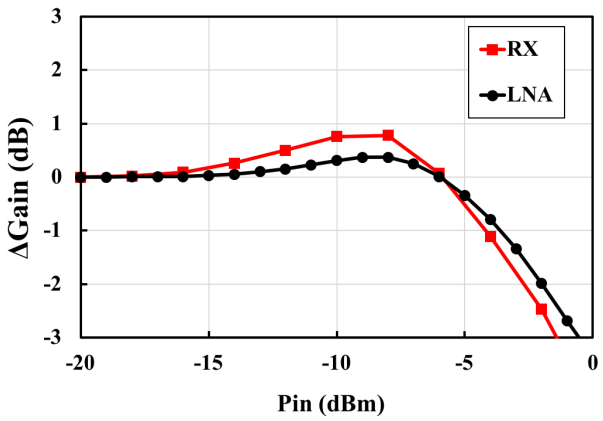
Fig.8.1a reports the simulated s_{11} that is lower than -20 dB, resulting in good input matching from 100 MHz to 1 GHz. At this operating frequency range the receiver noise figure (NF) varies from 3.5 to 3.9 dB, with a LNTA NF of 2.6-2.7 dB. The simulated down-conversion gain is equal to 35 dB with a -3dB drop at 10 MHz, as it can be noticed in Fig.8.1b

The IIP3 of the receiving chain has been simulated with two 5 MHz spaced tones and it is equal to 1 dBm, as well as the stand alone LNTA IIP3 (Fig.8.2a). Considering an out-of-band (OOB) blocker at 100 MHz offset from the carrier frequency, the in-band gain compression is equal to -4 dBm for the entire receiver chain and -3 dBm for the LNTA (Fig.8.2b).

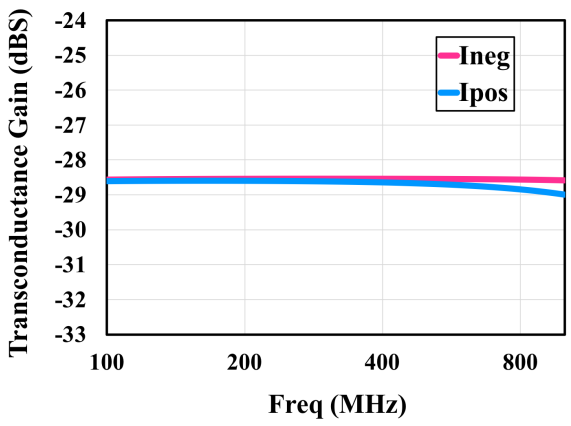
The LNTA transconductance gain is reported in Fig.8.2c. The use of the MBCM allows to achieve good balancing between the output current of the CG and CS signal paths, whose mismatch is always lower than 0.5 dB. For this reason, the receiver contribution to the IM2, mainly due to mixers coupling effects, can be considered negligible. Hence,



(a) RX and LNTA IIP3



(b) RX and LNA gain compression



(c) LNTA transconductance gain

Figure 8.2: Simulation results

the RX IIP2 is affected by the LNTA (Fig.7.6) that can be considered the bottleneck of the whole chain.

The simulated LNTA performance are summarized in Table 8.1, in comparison with other LNAs, designed for similar applications. [41] and [43] also show simulation results, while the others report measurements. NF and power dissipation of the proposed solution are equal or better than all the others. The IIP3 is also better than [44] and [45]. Although compared with the other three designs the IIP3 is lower, it can be pointed out that [40] and [42] need calibration to perform reliable distortion cancellation, while [43] adopts a design optimization that is suitable also for the proposed work. Finally, the IIP2 is also higher than the one presented in the table.

Chapter 9

Conclusion

This work describes an inductorless, noise-cancelling CG-CS LNTA. A mirror-based current multiplier has been introduced into the common-gate branch, providing signal recombination at the RF side of the chain, which allows double-balanced mixing. In this way, the noise-cancelling condition is achieved, as well as better distortion and noise performance of the entire receiver. The additional calibration algorithm, controlling the LNTA biasing, keeps the IIP2 high enough for TVWS applications.

Appendix A

TX output spectrum measurements

In this brief, further measurement results concerning the closed-loop transmitter described in the first part of this thesis are provided.

Fig.A.1 reports the result of the two tones test: the IM3 values are reported with respect to the power of one of the two output tones. If an input sinusoid is applied at different base-band frequencies, up to 50MHz, which corresponds to a RF bandwidth of 100MHz, at the output of the TX two tones will appear, together with their intermodulation products.

This measurement gives a further indication of the transmitter adjacent channel emission. In fact, considering an output power of 0dBm for the single tone, meaning a total output power of 3dBm (since there are two tones), the HD3 is around -43 dBc, closed to the measured ACLR.

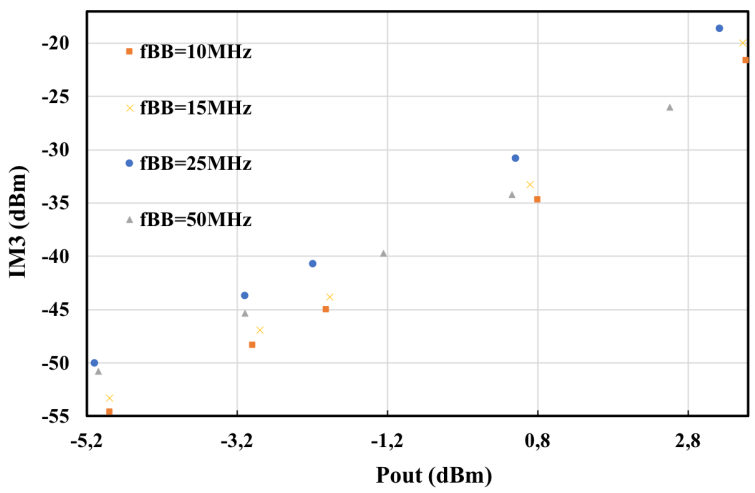


Figure A.1: Two-tones test: output IM3 values

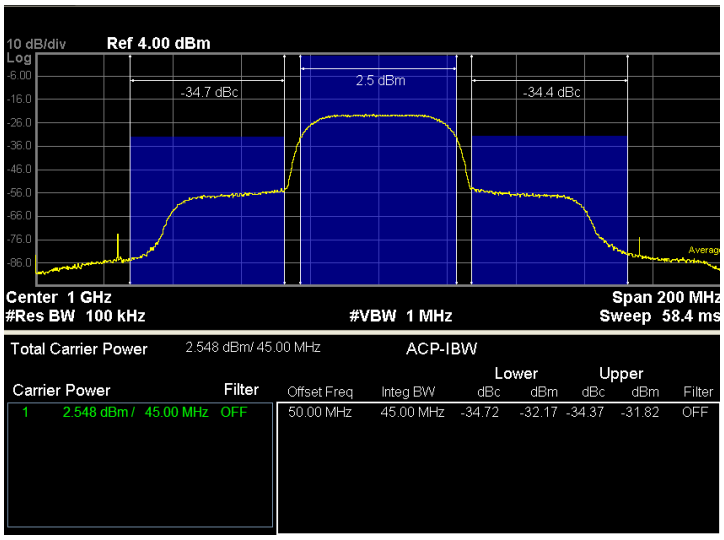


Figure A.2: ACLR measured with a 16 QAM signal

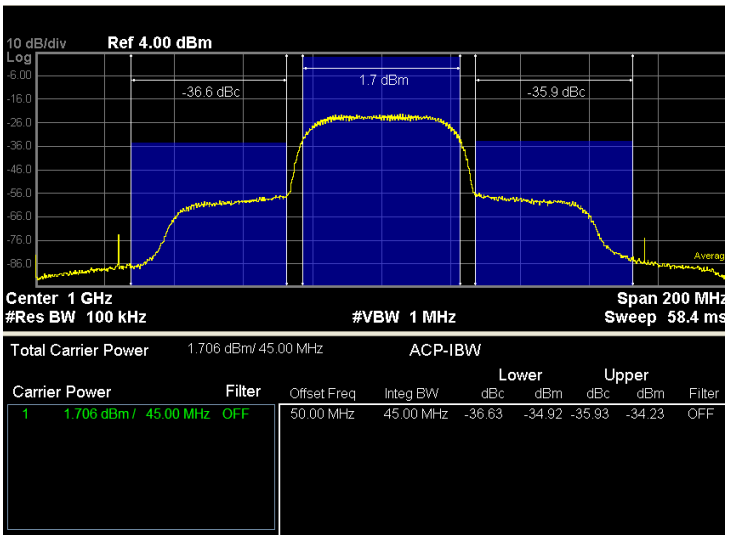


Figure A.3: ACLR measured with a 64 QAM signal

Further ACLR measurements are reported in Fig.A.2 and Fig.A.3, considering different modulated input signals, still achieving a 50MHz RF bandwidth. In the first case (Fig.A.2), where a 16QAM signal is applied, an output power of 4.2 dBm is achieved de-embedding the cable and PCB losses with an ACLR of -34.4dBc, while in the 64QAM test the output power corresponds to 3.4 dBm (ACLR closed to -36).

To be consistent, it must be said that, in both cases the test has been performed in maximum up-conversion gain configuration of the transmitter, obtained halving the BB resistances, thus doubling the BB LP filter cut-off frequency.

Bibliography

[1] P. Rossi, N. Codega, D. Gerna, A. Liscidini, D. Ottini, Y. He, A. Pirola, E. Sacchi, G. Uehara, C. Yang, and R. Castello, "An LTE Transmitter Using a Class-A/B Power Mixer," in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2013, pp. 340–341.

[2] E. Roverato, M. Kosunen, K. Cornelissens, S. Vatti, P. Stynen, K. Bertrand, T. Korhonen, H. Samsom, P. Vandenameele, and J. Ryynänen, "All-digital RF Transmitter in 28nm CMOS with Programmable RX-band Noise Shaping," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, 2017, pp. 222–223.

[3] P. E. P. Filho, M. Ingels, P. Wambacq, and J. Craninckx, "A Transmitter with 10b 128MS/S Incremental-Charge-Based DAC Achieving -155dBc/Hz Out-Of-Band Noise," in *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, 2015, pp. 1–3.

[4] P. E. P. Filho, M. Ingels, P. Wambacq, and J. Craninckx, "A 0.22mm^{2}CMOS Resistive Charge-Based Direct-Launch Digital Transmitter with -159dBc/Hz Out-Of-Band Noise," in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, 2016, pp. 250–252.

[5] Q. Liu, D. Kwon, Q. Bui, J. Choi, J. Lee, S. Baek, S. Heo, and T. B. Cho, "A 1.4-to-2.7GHz High-Efficiency RF Transmitter with an Automatic 3F$_{LO}$-Suppression Tracking-Notch-Filter Mixer Supporting HPUE in 14nm FinFET CMOS," in *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, 2018, pp. 172–174.

[6] G. Qi, P. Mak, and R. P. Martins, "A 0.038mm2 SAW-less Multiband Transceiver Using an N-Path SC Gain Loop," in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, 2016, pp. 452–454.

[7] D. B. S. K. P. Gammel, D.R. Pehlke and K. Walsh, "5G in Perspective: a Pragmatic Guide to What's Next," *White Paper (Skyworks)*, 2017.

[8] E. A. M. Klumperink, H. J. Westerveld, and B. Nauta, "N-path Filters and Mixer-First Receivers: A Review," in *2017 IEEE Custom Integrated Circuits Conference (CICC)*, 2017, pp. 1–8.

[9] N. Barber, "Narrow Band-Pass Filter Using Modulation," *Wireless Engineer*, pp. 132–134, 1947.

[10] B. D. Smith, "Analysis of Commutated Networks," *Transactions of the IRE Professional Group on Aeronautical and Navigational Electronics*, vol. PGAE-10, pp. 21–26, 1953.

[11] L. E. Franks and I. W. Sandberg, "An Alternative Approach to the Realization of Network Transfer Functions: The N-path filter," *The Bell System Technical Journal*, vol. 39, no. 5, pp. 1321–1350, 1960.

[12] A. Fettweis, "Steady-State Analysis of Circuits Containing a Periodically-Operated Switch," *IRE Transactions on Circuit Theory*, vol. 6, no. 3, pp. 252–260, 1959.

[13] R. Fischl, "Analysis of a Commutated Network," *IEEE Transactions on Aerospace and Navigational Electronics*, vol. ANE-10, no. 2, pp. 114–123, 1963.

[14] Y. Sun and I. Frisch, "A General Theory of Commutated Networks," *IEEE Transactions on Circuit Theory*, vol. 16, no. 4, pp. 502–508, 1969.

[15] T. Strom and S. Signell, "Analysis of Periodically Switched Linear Circuits," *IEEE Transactions on Circuits and Systems*, vol. 24, no. 10, pp. 531–541, 1977.

[16] M. Darvishi, R. van der Zee, and B. Nauta, "Design of Active N-Path Filters," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 12, pp. 2962–2976, 2013.

[17] M. Darvishi, "Active N-path filters: Theory and design," 2013.

[18] M. Darvishi, R. van der Zee, E. A. M. Klumperink, and B. Nauta, "Widely Tunable 4th Order Switched G¡formula formulatype="inline"¿¡tex Notation="TeX"¿$_m$¡/tex¿¡/formula¿-C Band-Pass Filter Based on N-Path Filters," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 3105–3119, 2012.

[19] A. Mirzaei, H. Darabi, and D. Murphy, "Architectural Evolution of Integrated M-Phase High-Q Bandpass Filters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 1, pp. 52–65, 2012.

[20] Q. Gu, "RF System Design of Transceivers for Wireless Communications," *Springer, First Edition*, 2006.

[21] B. Razavi, "RF Microelectronics," *Prentice Hall, Second Edition*, 2011.

[22] Y. Chen, N. Fong, B. Xu, and C. Wang, "An LTE SAW-less Transmitter Using 33% Duty-Cycle LO Signals for Harmonic Suppression," in *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, 2015, pp. 1–3.

[23] A. Coccia, D. Manstretta, and R. Castello, "A TVWS LNTA with Balanced Output Employing a Low-Noise Current Multiplier," in *2017 13th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, 2017, pp. 45–48.

[24] A. Coccia, S. Tijani, D. Manstretta, and R. Castello, "A TVWS Receiver with Balanced Output Self-Calibrated IIP2 LNTA Employing a Low-Noise Current Multiplier," *Integration*, vol. 63, pp. 283–290, 2018. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0167926017306193

[25] IEEE Std 802.22, "Cognitive Wireless RAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications: Policies and Procedures for Operation in the TV Bands."

[26] A. C. NB Carvalho and R. Gómez-García, "White Space Communication Technologies," *Cambridge University Press*, 2014.

[27] T. Forbes and R. Gharpurey, "A 2 GS/s Frequency-Folded ADC-Based Broadband Sampling Receiver," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 9, pp. 1971–1983, 2014.

[28] R. T. Yazicigil, T. Haque, M. R. Whalen, J. Yuan, J. Wright, and P. R. Kinget, "Wideband Rapid Interferer Detector Exploiting Compressed Sampling With a Quadrature Analog-to-Information Converter," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 12, pp. 3047–3064, 2015.

[29] T. Haque, R. T. Yazicigil, K. J. Pan, J. Wright, and P. R. Kinget, "Theory and Design of a Quadrature Analog-to-Information Converter for Energy-Efficient Wideband Spectrum Sensing," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 2, pp. 527–535, 2015.

[30] T. Haque, M. Bajor, Y. Zhang, J. Zhu, Z. Jacobs, R. Kettlewell, J. Wright, and P. R. Kinget, "A Direct RF-to-Information Converter for Reception and Wideband Interferer Detection Employing Pseudo-Random LO Modulation," in *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2017, pp. 268–271.

[31] T. Ogami, M. Tani, K. Ikada, H. Kando, T. Wada, H. Obiya, M. Koshino, M. Kawashima, and N. Nakajima, "A New Tunable Filter Using Love Wave Resonators for Reconfigurable RF," in *2014 IEEE MTT-S International Microwave Symposium (IMS2014)*, 2014, pp. 1–3.

[32] B. van Liempd, A. Visweswaran, S. Ariumi, S. Hitomi, P. Wambacq, and J. Craninckx, "Adaptive RF Front-Ends Using Electrical-Balance Duplexers and Tuned SAW Resonators," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 11, pp. 4621–4628, 2017.

[33] T. Wada, T. Ogami, A. Horita, H. Obiya, M. Koshino, M. Kawashima, and N. Nakajima, "A New Tunable SAW Filter Circuit for Reconfigurable RF," in *2016 IEEE MTT-S International Microwave Symposium (IMS)*, 2016, pp. 1–4.

[34] H. K. Subramaniyan, E. A. M. Klumperink, V. Srinivasan, A. Kiaei, and B. Nauta, "RF Transconductor Linearization Robust to Process, Voltage and Temperature Variations," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 11, pp. 2591–2602, 2015.

[35] H. Zhang and E. Sanchez-Sinencio, "Linearization Techniques for CMOS Low Noise Amplifiers: A Tutorial," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 1, pp. 22–36, 2011.

[36] B. Razavi, "Cognitive Radio Design Challenges and Techniques," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 8, pp. 1542–1553, 2010.

[37] S. Chehrazi, A. Mirzaei, and A. A. Abidi, "Second-Order Intermodulation in Current-Commutating Passive FET Mixers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 12, pp. 2556–2568, 2009.

[38] D. Manstretta, M. Brandolini, and F. Svelto, "Second-order intermodulation mechanisms in CMOS downconverters," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 3, pp. 394–406, 2003.

[39] D. Murphy, H. Darabi, A. Abidi, A. A. Hafez, A. Mirzaei, M. Mikhemar, and M. F. Chang, "A Blocker-Tolerant, Noise-Cancelling Receiver Suitable for Wideband Wireless Applications," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 2943–2963, 2012.

[40] W. Chen, G. Liu, B. Zdravko, and A. M. Niknejad, "A Highly Linear Broadband CMOS LNA Employing Noise and Distortion Cancellation," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 5, pp. 1164–1176, 2008.

[41] R. Xu, L. Sun, and J. Wen, "A highly linear wideband CMOS LNA adopting current amplification and distortion cancellation," in *2008 9th International Conference on Solid-State and Integrated-Circuit Technology*, 2008, pp. 1512–1515.

[42] T. Chung, H. Lee, D. Jeong, J. Yoon, and B. Kim, "A Wideband CMOS Noise-Canceling Low-Noise Amplifier With High Linearity," *IEEE Microwave and Wireless Components Letters*, vol. 25, no. 8, pp. 547–549, 2015.

[43] G. Varga, C. P. Heising, A. Ashok, I. Subbiah, M. Schrey, and S. Heinen, "A highly linear broadband LNA for TV white spaces and Cognitive Radio applications," in *2015 German Microwave Conference*, 2015, pp. 296–298.

[44] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "Wideband Balun-LNA With Simultaneous Output Balancing, Noise-Canceling and Distortion-Canceling," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 6, pp. 1341–1350, 2008.

[45] H. Wang, L. Zhang, and Z. Yu, "A Wideband Inductorless LNA With Local Feedback and Noise Cancelling for Low-Power Low-Voltage Applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 8, pp. 1993–2005, 2010.

[46] J. Kim and J. Silva-Martinez, "Wideband Inductorless Balun-LNA Employing Feedback for Low-Power Low-Voltage Applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 9, pp. 2833–2842, 2012.

[47] D. Manstretta, "A Broadband Low-Power Low-Noise Active Balun With Second-Order Distortion Cancellation," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 2, pp. 407–420, 2012.

[48] J. Sturm, S. Popuri, and X. Xiang, "CMOS noise canceling balun LNA with tunable bandpass from 4.6 GHz to 5.8 GHz," in *2014 21st IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, 2014, pp. 84–87.

[49] R. Zhang, Z. Lu, and D. Chen, "A low-power noise-canceling LNA with downward impedance transformer and resistive feedback," in *2014 12th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, 2014, pp. 1–3.

[50] B. Guo, J. Chen, L. Li, H. Jin, and G. Yang, "A Wideband Noise-Canceling CMOS LNA With Enhanced Linearity by Using Complementary nMOS and pMOS Configurations," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 5, pp. 1331–1344, 2017.

[51] D. Im, I. Nam, H. Kim, and K. Lee, "A Wideband CMOS Low Noise Amplifier Employing Noise and IM2 Distortion Cancellation for a Digital TV Tuner," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 3, pp. 686–698, 2009.

[52] J. Y. Liu, J. Chen, C. Hsia, P. Yin, and C. Lu, "A Wideband Inductorless Single-to-Differential LNA in 0.18μm CMOS Technology for Digital TV Receivers," *IEEE Microwave and Wireless Components Letters*, vol. 24, no. 7, pp. 472–474, 2014.

[53] A. L. T. Costa, H. Klimach, and S. Bampi, "Ultra-low voltage wideband inductorless balun LNA with high gain and high IP2 for sub-GHz applications," in *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2016, pp. 289–292.

[54] M. Sosio, A. Liscidini, and R. Castello, "An Intuitive Current-Driven Passive Mixer Model Based on Switched-Capacitor Theory," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 60, no. 2, pp. 66–70, 2013.