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Ph. D. School in Microelectronics

Ph.D. Thesis

A 110-nm Extended-Range Data Converter for Three-Axis Capacitive MEMS Accelerometer

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Cerco sempre di fare ciò che non sono capace di fare, per imparare come farlo.
(Pablo Picasso)

Contents

List of Figures

List of Tables

Abstract

This Thesis is devoted to the architectural study, design, and measurements of an analog-to-digital converter in a 110-nm CMOS technology tailored for reading out a three-axis accelerometers in consumer applications.
An extended-range converter including a first-order incremental *ADC* and a *SAR ADC* has been designed with particular attention to power consumption, area, linearity, and resolution.
The adopted *ADC* architecture offers the advantage of simplicity of the digital part, low power consumption and area occupation, while the co-existence of an oversampling based converter (incremental *ADC*) and a Nyquist-rate converter (*SAR ADC*) allows us to meet specifications in terms of output data rate, linearity, and noise.
The *ADC* Matlab model described in Chapter 2 has been used to guide the transistor level design of the switched-capacitor implementation. Design and simulation results are presented in detail in Chapter 3.
Test chip measurements are shown in Chapter 5 in order to verify simulation results.
The fabricated device achieves 16-bit linearity, 0.87-$\frac{\mu V}{\sqrt{Hz}}$ noise density at 1-V input signal with less than 100 μA current consumption and less than 0.1 mm^2 area occupation.
The switched-capacitor design requires the presence of an anti-aliasing filter to reduce noise folding from the accelerometer front-end channel.
A continuous-time implementation of the incremental *ADC*, exploiting the filtering action of the integrator, allows removing the anti-aliasing filter.
Chapter 4 analyzes the design of this solution in details.
More than 30% current consumption reduction is obtained while a slight

worsening of linearity is forecast by transistor level simulations.
Future perspectives and possible improvements of the design will conclude the Thesis.

Introduction

Inertial sensors are nowadays widely used in a number of different applications. The possibility to integrate micro-electro-mechanical systems (MEMS) inertial sensors and the readout electronics in the same die or in the same package allows a significant reduction of fabrication cost and area occupied [2] [3].

This intrinsic advantage of MEMS inertial sensors is the key for their success in the consumer market where minimum cost and area occupied are crucial. Capacitive MEMS Accelerometers and Gyroscopes, along with their readout electronic circuitry, can nowadays sense, analyze and elaborate three-dimensional movement of an object in space with high sensitivity, low power consumption, and low temperature dependence at extremely low cost.

The specifications of the electronic readout circuitry for such devices, while somehow depending on the application, focus on area and power consumption, especially for consumer application. This requires the study and implementation of circuit architectures where these parameters are minimized, while meeting the requirements of medium-high linearity and low noise.

Capacitive MEMS accelerometers transduce acceleration into a capacitive variation [4] [5] [6] [7]. This variation is sensed, amplified, and then converted from the analog to the digital domain (for data processing) by an analog-to-digital converter (ADC).

This work deals with the architectural study, design, and measurement of an ADC for a three-axis MEMS accelerometer for consumer application.

Chapter 1

Data Converters for MEMS Accelerometers

Capacitive MEMS accelerometers offer the advantage of high sensitivity, low temperature dependence, linearity, and low power consumption. A change of acceleration (a mechanical quantity) is transduced into a capacitive variation (electrical quantity). This capacitive variation needs to be measured, amplified, and then converted into digital world by an Analog to Digital Converter (ADC) for data processing.

This work is related to the detailed study, design, and testing of an ADC for a MEMS accelerometer for consumer application (TDK-InvenSense accelerometer).

In the first part of the chapter a brief review of the mechanical principle of operation of the MEMS accelerometer along with an example of electronic circuitry for capacitance measurement will be presented.

In the second part, after an introduction to Analog to Digital Converters and their specifications, requirements for the ADC of this work will be clarified.

In the last part an ADC architecture will be chosen and the principle of operation presented.

1.1 MEMS Accelerometer: Principle of Operation

A three-axis accelerometer is a device that senses the mechanical quantity acceleration on three different axis: x,y,z. A MEMS accelerometer can be seen as a spring-mass-dumper system, as shown in Figure 1.1. A proof mass is anchored to a frame with an elastic support.

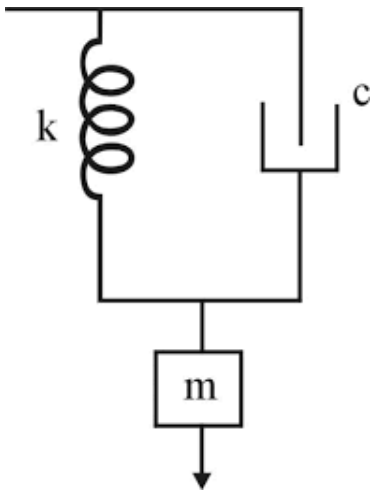

Figure 1.1: Spring-mass-dumper system

The equivalent lumped electrical model is shown in Figure 1.2, where

- zC represents, as a capacitive impedance, the spring coefficient k. $C = \frac{1}{k}$;
- zR represents, as a resistive impedance, the dumper c. $R = c$;
- zL represents, as an inductive impedance, the mass m. $m = L$;
- F represents, as a voltage, an external force;
- $\dot{x}$ represents, as a current, the velocity.

It follows that:

$$\dot{x} = sx = \frac{F}{ms + c + \frac{k}{s}} \tag{1.1}$$

Since $F = ma$, the displacement x of the proof mass is a measure of the acceleration.

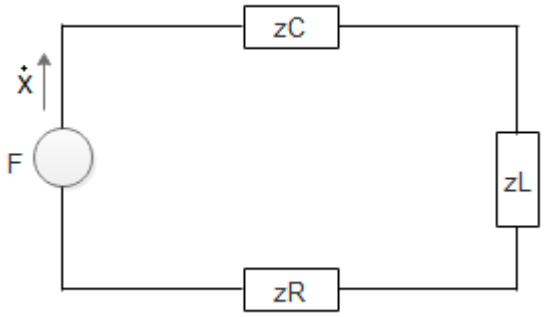

Figure 1.2: Spring-mass-dumper system: electrical model

1.2 Capacitive Transduction

The displacement x of the proof mass can be sensed in several ways. For example it can be transduced into a capacitive variation [1].

Focusing on the capacitive approach, in the parallel plate hypotesis, the proof mass can be seen as a moving plate between two fixed electrodes (Figure 1.3).

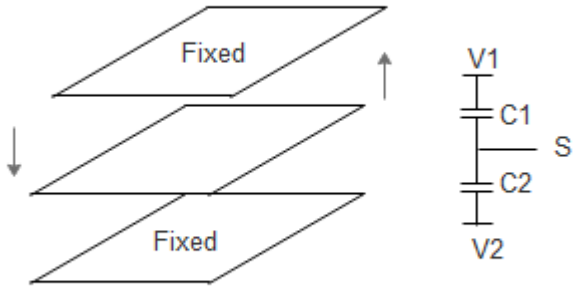

Figure 1.3: Capacitive transduction: parallel plate model

Two AC voltages with opposite phases $V1$ and $V2$ can drive capacitors $C1$ and $C2$. A non-zero voltage at node S is related to a differential capacitive variation ($C1$-$C2$) and will represent the displacement x of the proof mass.

[1] Piezoelectric and piezoresistive sensors measure the deformation of the support.

1.3 Circuits for Capacitance Reading

Capacitance variation has to be read and amplified. Continuous-time or discrete-time solutions can be adopted. A review of readout architectures can be found in [8] [9] [10].

Here a simple switched capacitor implementation with correlated double sampling will be briefly discussed. It is an example of the so called $C2V$ circuit, which is the front-end between the mechanical part of the MEMS and the ADC studied in this work.

Figure 1.4 represents a simplified scheme of the above mentioned switched capacitor technique for capacitance reading.

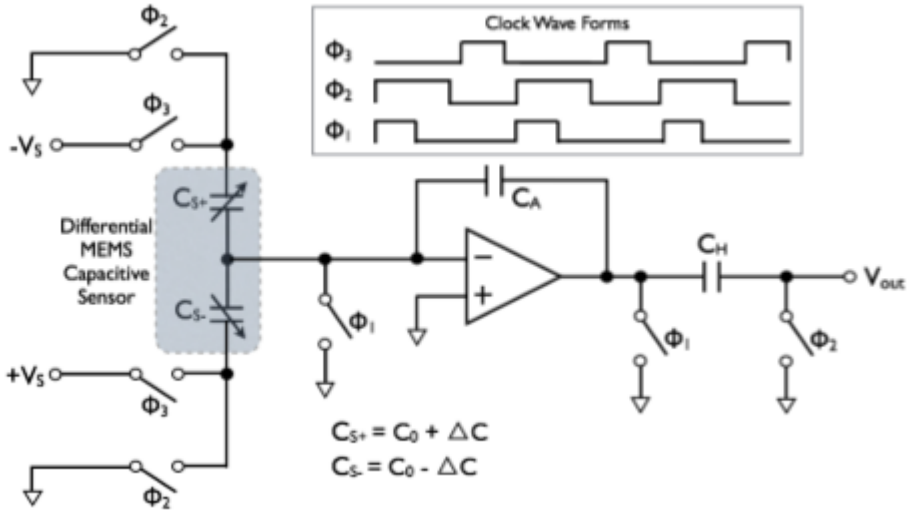

Figure 1.4: C2V example with correlated double sampling

The sensor capacitance variation ΔC is read and amplified. The output of this circuit, neglecting the role of Φ_1, is

$$V_{out} = \frac{2\Delta C}{C_A} Vs$$

Φ_1 and C_H allow canceling offset and low-frequency noise. When Φ_1 and Φ_2 are both high, C_H is discharged. Then Φ_1 goes low (while Φ_2 is still high). Noise and offset (V_{NO}) are stored on the left plate of C_H.
When Φ_2 goes low and Φ_3 goes high the circuit amplifies the signal from the

sensor. The right plate of C_H should go to $V_{out} = \frac{2\Delta C}{C_A} Vs + V_{NO}$, but since V_{NO} was stored on the left plate before, the quantity V_{NO} is canceled.

The quantity V_{out} contains the information on the variation of capacitance of the sensor. This information needs to be converted into digital domain for data processing. This is indeed the role of the Analog to Digital converter.

1.4 Analog to Digital Converters

1.4.1 Introduction to Analog to Digital Converters

An Analog to Digital Converter (ADC) is the bridge between analog and digital worlds. To transform the information, an incoming analog signal at the input of an ADC needs to be sampled in time and quantized in amplitude. Clearly, both of these operations introduce an error which can not be avoided.

In order to correcly reconstruct the signal, Nyquist-Shannon Theorem requires a sampling frequency equal or greater than the maximum frequency of the analog signal.
Regarding quantization, it is trivial to understand that the larger is the number of quantization levels, the more accurately the information is transformed.

For a detailed theory review of Analog to Digital Converters one can refer to [11] [12].

1.4.2 Nyquist-Rate and Oversampling Converters

A general dinstinction in $ADCs$ can be found between Nyquist-rate and oversampling converters.
In Nyquist-rate converters the sampling frequency is equal to or slightly greater than the limit imposed by the Nyquist-Shannon Theorem.

If f_B is the bandwith of the signal, $2f_B$ is the Nyquist limit and F_s the sampling frequency of the converter, then $OSR = \frac{F_s}{2f_B}$.

Typically OSR for Nyquist-rate converters is less than 8 [12]. Oversampling converters use instead a large OSR value (even in the order of hundreds).
The different approach of the two types of converters can be explained with

the aid of Figure 1.5.

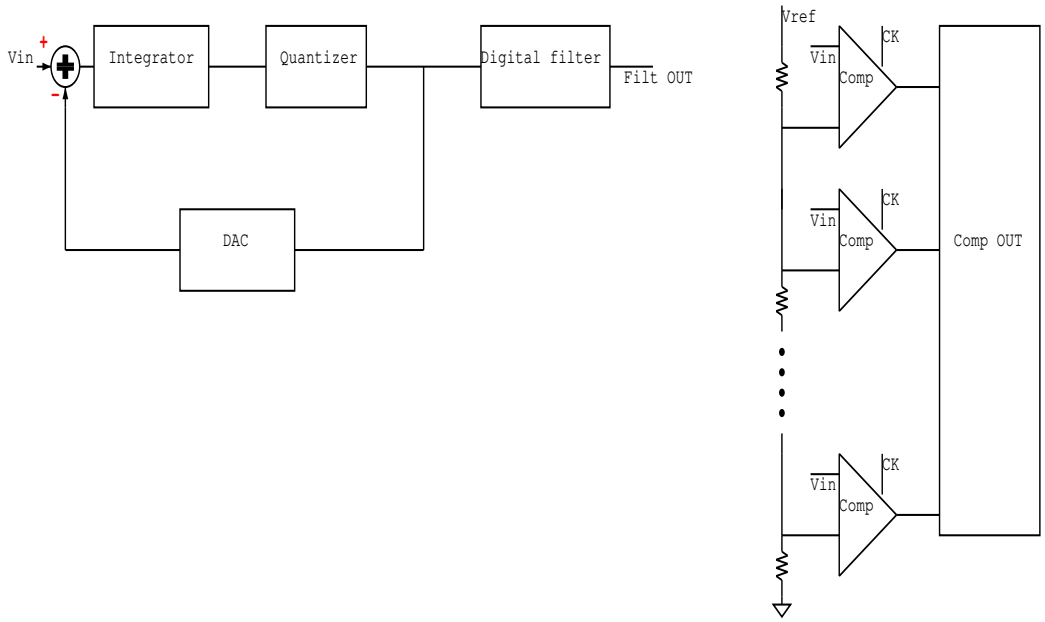

Figure 1.5: Example of Nyquist rate and oversampling converters

On the right side of Figure 1.5 a full-flash architecture is shown. To resolve n bits, $2^n - 1$ comparators and a resistive string are used in order to compare the input signal with all the quantization levels. The conversion is immediate. Only one clock cycle is enough to decide the position of the input signal with respect to the converter thresholds. The output of the comparators represents the digitized information.

On the left side of Figure 1.5 an example of the loop of a first order sigma-delta converter is represented. The input signal is integrated and then a comparison (for example with respect to zero) is performed by a comparator. A single bit DAC feeds back the output to a summing node. The fed back output is subtracted from the input signal and the error is integrated. This procedure is repeated N times. The output of the converter is the bitstream of the comparator.

While comparators are used in both cases (to quantize an analog signal into a digital one) the approach is totally different.

It is possibile to surmise here that if speed of conversion is the main

requirement, the first approach is clearly better.
With one clock cycle one can convert an analog signal into a digital signal.

The sigma-delta converter is instead better if resolution is the main concern. For instance a DC signal can be injected into the sigma-delta loop a number of times N sufficient to have the required resolution in the output information.

While it is possible to find a great variety of converters [11] [12], Nyquist rate converters offer the advantage of speed of conversion and reduced power consumption, but their resolution is often limited by the accuracy of components. Also their area rapidly increases when the number of bits to be resolved increases. Their use is generally limited to low and medium resolutions (8 to 12 bits).

Oversampling converters are widely used when high resolutions are required. They are much less sensitive to accuracy and mismatch of components (mainly due to the presence of the feedback loop) and their area is limited. The drawback is represented by speed of conversion and the need for high clock frequencies when the signal bandwidth increases.

1.4.3 Data Converter Specifications

Performances of Data Converters are evaluated (and different architectures are compared) with tens of different specifications.
While power consumption and area are self explained, a definition of non-linearity of a converter needs to be clarified. The input-output characteristic of an ADC is ideally a staircase with all steps of equal width. Assuming for example a decimal digital output code, every step should also increase of a value of unity the digital output of the converter. A fit between an ideally reconstructed output and the input would lead to a unity slope straigth line ($y = x$) with value zero for zero signal. This is actually not true because of the ADC non-idealities.
Offset error is the real value converted for zero signal applied, while **gain error** is represented by the slope of the previously mentioned fit with respect to unity.

One of the main concerns in data converters is the linearity of the conversion. Two definitions are usually adopted: DNL **(differential non-linearity)** and

INL **(integral non-linearity)**.
DNL is defined as the difference between the width of the steps of the converter and the ideal value of 1 LSB[2]. It is usually expressed in LSB or fraction of LSB dividing the above mentioned difference by the value of an LSB.

Figure 1.6 gives a visual representation of the DNL errors of a real ADC.

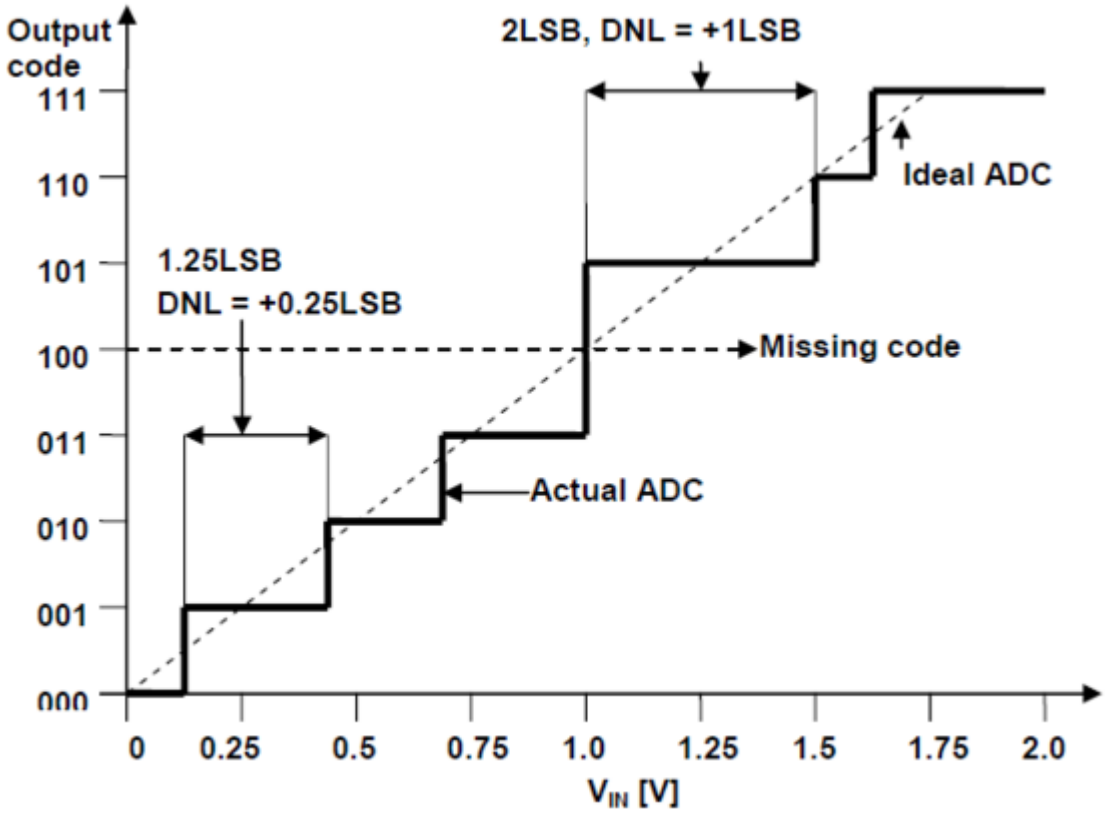

Figure 1.6: DNL of an actual 3-bit converter

Figure 1.6 reveals the possibility for an ADC to "jump"codes. Missing codes need to be clearly avoided.
Another possibile error is represented by non-monotonicity, when an increasing input generates a decreasing step. This is the most serious issue since it can create positive feedback loops.
The INL is simply the cumulative sum (the integral) of the DNL over the converter range. It is also defined as the distance of the actual converted value

[2] LSB: least significant bit.

from the linear fit of the conversion over full scale. Linear fit can be a best straigth line (least square method) or a straigth line drawn between the first value of the converter and full scale.
Noise performance of an ADC is usually measured in terms of **signal-to-noise ratio (**SNR**)** or **noise density** (noise per unit bandwidth). Amplitude quantization introduces an error which is usually treated as white noise [11]. The ratio between the power of a sinusoidal input signal and the power of this white noise floor gives the SNR of a converter. The SNR is related to the number of bits (assuming sinusoidal input and white quantization noise) with the equation

$$SNR = 6.02n + 1.76 \text{ [dB]}$$

If the signal-to-noise ratio of an actual converter is measured, then the effective number of bits can be defined as

$$ENOB = \frac{SNR - 1.76}{6.02}$$

Apart from quantization, operational amplifiers or other components (e.g. resistors, switches, noisy supplies, etc...) determine the overall noise performance of a converter.
Linearity of a converter can also be expressed in terms of distortion. A non linear converter will generate a frequency spectrum characterized by harmonic distortion. $SFDR$ **(spurious free dynamic range)** and HD **(harmonic distortion)** are useful parameters: $SFDR$ is the ratio between the RMS value of the input signal and the RMS value of the highest harmonic, while HD is the ratio between the RMS value of the input signal and the RMS value of the sum of the first ten harmonics.
While it is difficult to define an exaustive parameter to evaluate the overall performance of a converter, $FoMs$ **(figures of merit)** are commonly used in literature. As an example the Schreier FoM is here reported

$$FoM_{Schreier} = DR + 10 \log \left(\frac{Power}{Bandwidth} \right)$$

.

Noise and linearity were treated separately and it should be clear that they are totally different. While in behavioral models or simulations the two

concepts can be analyzed and simulated separately, in ADC testing this is not possible.
It is useful to anticipate here an alternative way to measure linearity, which will be used in the ADC measurements in Chapter 5.
Linearity can be approached in a statistical way. Since noise is uniformly distributed, a reasonable solution to measure linearity (DNL) is to count codes occurences (N_{occ}) when a slow ramp is applied to the converter. With a sufficient number of samples per LSB (to take into account the effect of noise) DNL of code x is defined as

$$DNL_x = \frac{N_{occ_x}}{N_{mean}} - 1 \tag{1.2}$$

where N_{mean} is the value of the average of occurrences. Ideally $DNL_x = 0$. A missing code has $DNL = -1$. Non monotonicity of one LSB or a step width of $2LSB$ are indicated by $DNL = +1$. INL will simply be the cumulative sum of the DNL values.

1.5 Specifications of MEMS Accelerometer Converter

Data converters for TDK-InvenSense accelerometer address the consumer market. The priorities, when a chip has to be integrated in a system like a Tablet or a mobile phone, are surely a small area and a reduced power consumption. The second requirement clearly introduces concerns when the current available for amplifiers is in the range of few μA.
In Table 2.1 specifications are defined. Since the product will be released on the market, **specifications are protected by an** NDA. Values indicated in Table 2.1 give an idea of the order of magnitude required for the design.

Technology available for the design has a minimum channel length of 130 nm (shrunk to 110 nm) with a nominal supply voltage of 1.5 V.

Table 1.1: Data Converter specifications

Parameter	*Spec*	*Unit*
Current consumption	< 100	μA
Area	< 0.1	mm^2
Linearity-INL	0.2	% at 16 bit
Linearity-DNL	± 1	LSB at 16 bit
Resolution	12	bit (ENOB)
Signal range	1	V
Signal bandwidth-single channel	15	kHz

1.6 ADC Architecture Choice

The need for sensing acceleration along three different axis (x, y, z), which are three totally different informations, leads to an architectural crossroad. One can use three $ADCs$ (one for each channel) or one ADC for all the three channels. Since area and power consumption are the most important specifications for this design, the choice of a single ADC can be reasonable.
It is clear that processing three uncorrelated informations with a single circuit can be problematic. The idea is to multiplex x,y and z accelerometer axis with a round robin algorithm. The schematic block diagram is shown in Figure 1.7. The most important thing to notice is the need for a reset signal. The ADC and $C2V$ circuits contain capacitors which are devices with a memory. It is necessary to erase their memory whenever a single axis information has been processed.
The other issue with a single channel-single ADC choice is the speed of conversion. The time slot for a single axis conversion, assuming a required output data rate, is divided by 3. The ADC has to be faster.

Architecture choice is mainly related to the nominal resolution required: 16 bits. This resolution, from previous considerations, is difficult to achieve with a Nyquist-rate converter. An oversampling converter can be a better choice.
Incremental $ADCs$ are periodically-reset oversampling converters. Their

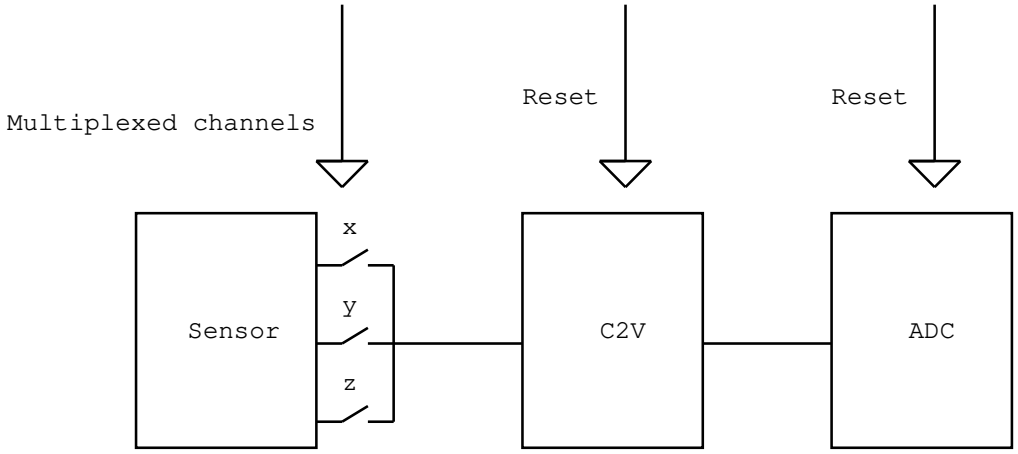

Figure 1.7: 3 axis multiplexing principle

principle of operation is clarified in [13] [14]. The block diagram of a first-order incremental *ADC* is shown in Figure 1.8.

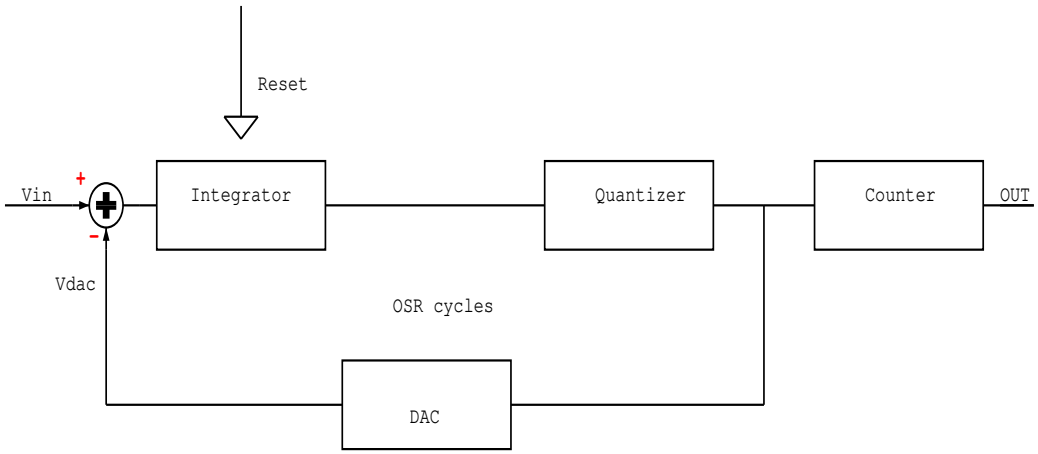

Figure 1.8: Block diagram of a first-order incremental *ADC*

These converters offer single sample precision and high linearity, which are key requirements for this design, and the periodic reset is crucial for sensor multiplexing. A first-order converter would require 2^{16} clock cycles to resolve 16 bits, while for a second-order 257 clock cycles are sufficient [13]. The advantages of a first-order converter are the small area required and the simplicity of the digital filter that follows the *ADC* (a simple counter). The disadvantage of

a first-order structure is that it is slow. While a second-order converter is a reasonable choice, to further improve output data rate, a possibility is to use a first-order converter (with its intrinsic advantages) combined with the information stored at the output of the integrator at the end of each conversion (also called **residue**). A similar approach has been used in [15] [16].
When an input signal is processed by an incremental converter, the output information is the result of comparisons performed by the quantizer. The error introduced in terms of quantization is stored at the output of the N_{th} integrator for an N_{th}-order converter. This is an analog signal that can be further converted with a fast ADC, increasing the overall resolution.
The charge redistribution SAR converter is a power efficient solution for performing this task. It easily allows to achieve resolutions in the order of 10 bits [17] [18] [19], performing a number of comparisons equal to the number of bits to be resolved plus one for signal sampling[3] with only one comparator.

16 bits of resolution can be achieved with different combinations of incremental and SAR ADC resolutions. An increase in the number of bits resolved by the incremental ADC reduces the accuracy required by the SAR ADC (which is mainly related to accuracy of the capacitive array elements), but it also reduces the speed of the overall ADC. For every bit added to a first-order incremental ADC, indeed, the number of clock cycles required is doubled.
The power consumption requirement for an incremental ADC is related to the clock frequency. Since, from specifications, the single channel bandwidth (BW) requirement is 15 kHz, 7 bits (6 bits single ended) from the incremental ADC can be obtained with a clock frequency $Fc = 2\ BW\ 2^6$=2 MHz. This clock frequency is related to the GBW[4] of the operational amplifier used for the integrator and allows to respect the power consumption requirement. Therefore, 9 bits should be resolved by the SAR ADC. 2 bits redundancy will be left in the sum to avoid distortion in the reconstructed signal.

The principle of operation of this **extended range converter** is shown in Figure 1.9

Significant blocks are the **Integrator** (with its gain G), the **Quantizer**

[3]This is true for a binary search algorithm SAR ADC with no redundancy.
[4]GWB: Gain-bandwidth product.

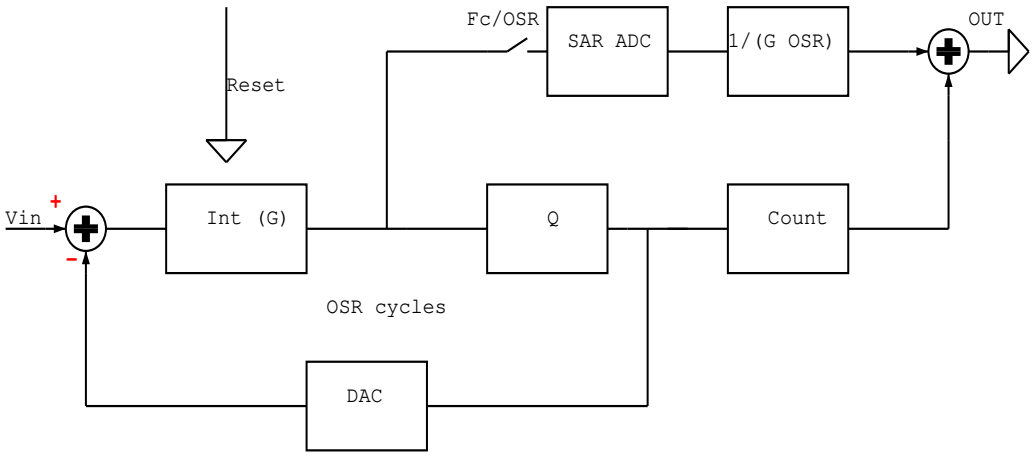

Figure 1.9: Extended range converter block diagram

(Q), the **Digital Counter** and the *SAR ADC* which converts the residue. Reconstruction of the signal needs to take into account that every conversion of the *SAR ADC* should be divided by the interstage gain between the two converters. Reconstruction is the sum of the output of the incremental *ADC* and its quantization error (converted by the *SAR ADC*).

1.7 Top-Level Architectural Choices

The incremental *ADC* will be designed both with a discrete-time and a continuous-time architecture (see Chapter 3 and Chapter 4, respectively). Since signal reconstruction is a sum, the reference voltages of the incremental *ADC* and of the *SAR ADC* have to be the same, to avoid non-linearity. The discrete-time solution also requires an anti-aliasing filter. The simplified single-ended schematic of the discrete-time switched-capacitor (SC) incremental *ADC* is shown in Figure 1.10, while the charge redistribution *SAR ADC* structure is shown in Figure 1.11.

The use of a sign detecting structure allows to halve the area ($n-1$ comparisons are performed for n bit resolution: the remaining bit is obtained with sign detection). During sampling phase, comparator inputs are hold to the common mode voltage (V_{CM}) and bottom plate of the capacitors samples

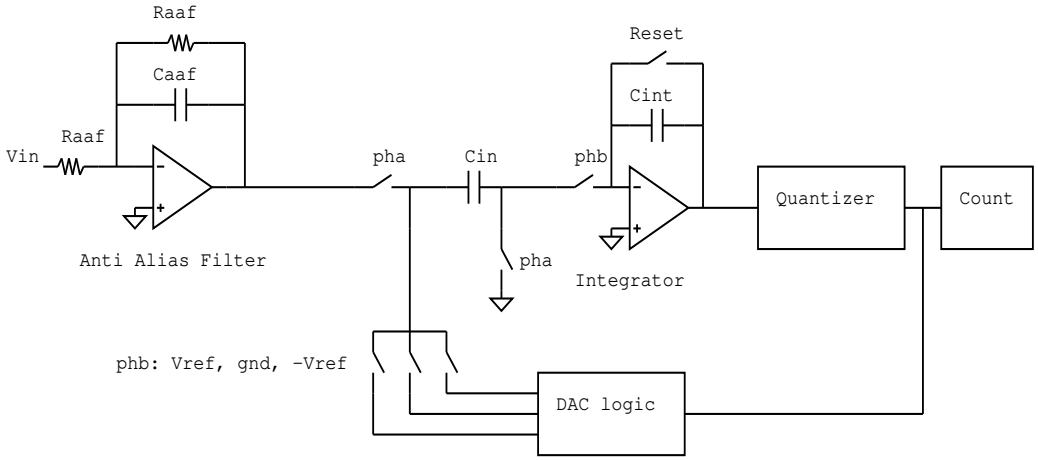

Figure 1.10: Structure of the SC incremental ADC

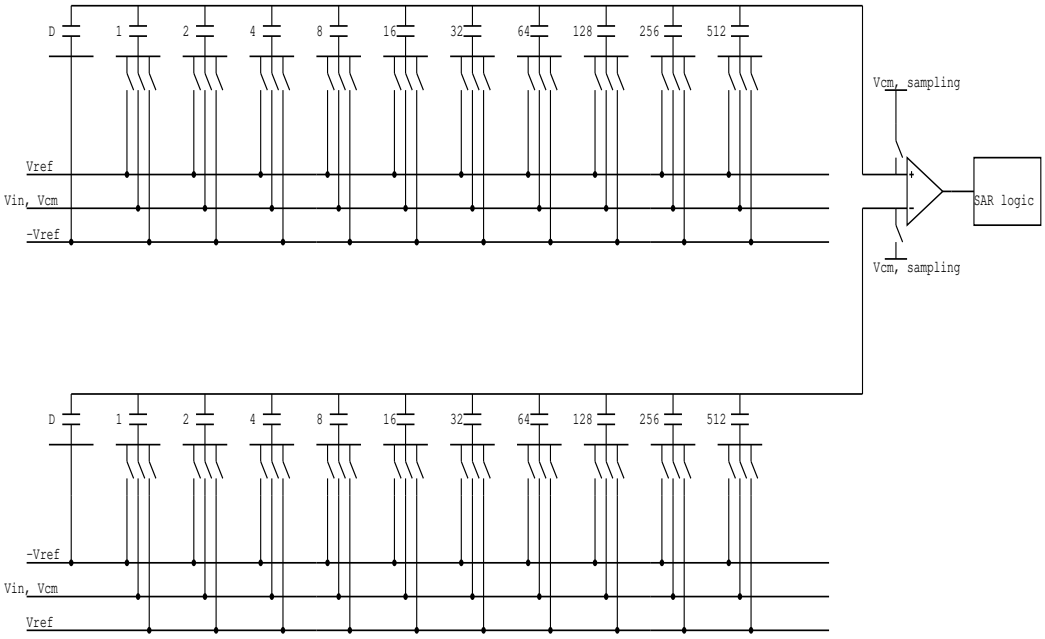

Figure 1.11: Structure of the SAR ADC

the output of the integrator. After sampling, all bottom plates are connected to V_{CM}[5]. This allows sign detection. After that, the binary search algorithm is performed. Capacitors are connected to V_{ref} or $-V_{ref}$ sequentially. Ten comparisons are performed.

Finally a top level timing diagram of the extended range conversion is shown in Figure 1.12.

It follows that the time required for a sample conversion for a single axis of the Accelerometer is about 40 μs. Time of conversion is the sum of 64 clock cycles of the Incremental, four clock cycles for SAR sampling and the following 11 cycles required for SAR conversion.

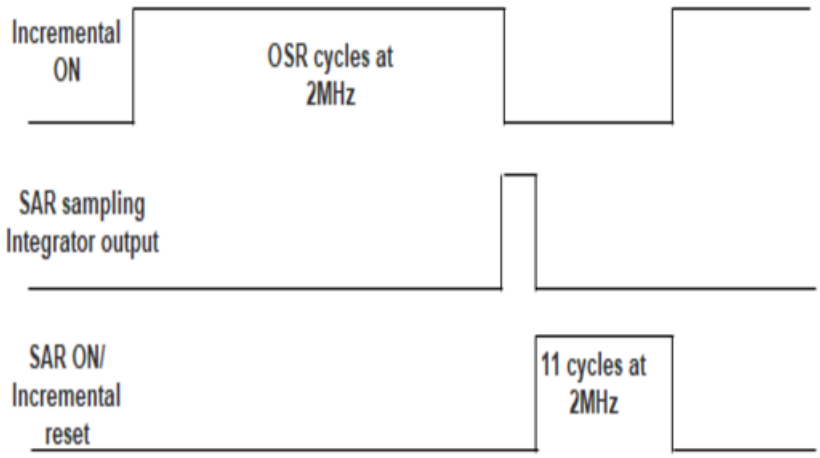

Figure 1.12: Top-level timing diagram of the extended range conversion

1.8 Conclusions

In this chapter a brief introduction on MEMS Accelerometers was given. The main aim of this first part of the Thesis was to motivate the choice of the

[5] V_{CM} and V_{in} switches are put together only to simplify the picture.

ADC architecture. Even though other possibilities are available, an Extended Range Incremental-SAR *ADC* achieves, at least from a theoretic point of view, requirements of reduction of area and power consumption for consumer application. Also great single sample performances can be obtained, which are crucial for the three-axis Accelerometer. In the following chapters a Matlab model for behavioral simulations will be introduced. For a detailed analysis of the design of single analog blocks one can refer to Chapter 3 and Chapter 4.

Chapter 2

ADC Modeling

Modeling and behavioral simulations are traditionally used to simulate the performances of an ADC. Transistor level simulations would in fact require too long transient simulations that take an unreasonable amount of time.
In this chapter a Matlab model will be created and used for this purpose. Equations that regulate the operation of the extended range ADC will be described, implemented and simulated. Non idealities will also be introduced and their effects on SNR and linearity analyzed. Information acquired will guide the transistor level design.

2.1 ADC Equations

A switched-capacitor (SC) first-order incremental A/D converter can be modeled with the following equation [13]

$$V = OSR\, G\, V_{in} - NV_{ref}\, G \tag{2.1}$$

where

- V is the output of the integrator in the loop after OSR cycles
- OSR is the oversampling ratio
- G is the gain of the integrator (ratio between integrating and input capacitors $\frac{C_{in}}{C_{Int}}$)

- N is the output of the counter
- V_{ref} is the ADC reference voltage

The output of the integrator after OSR cycles is the quantization error of the incremental conversion and will be used for a fine conversion ($SAR\ ADC$ conversion).

Resolution of the incremental converter depends on the oversampling ratio. In an ideal first-order converter $2^{nbits} = OSR$ holds (single-ended implementation). A resolution of 16 bits (nominal) are needed for this application. Increasing the number of cycles in the incremental converter will slow down the time required for the overall conversion but will reduce the number of bits to be resolved by the $SAR\ ADC$ conversion. Rearranging (2.1) as

$$Vin = \frac{N}{OSR} V_{ref} + \frac{V}{OSR\, G} \tag{2.2}$$

(thus recombining the input signal) it is also clear that increasing the oversampling ratio gives a further advantage. The conversion from $SAR\ ADC$, when referred to the input signal will be divided by ($OSR\, G$). This means that also its noise requirements will be relaxed if a large OSR is used.
Equation (2.2) implies that the whole conversion is a weighted sum of the two ADC conversions. It is recommended to use of the same reference for both the incremental and the SAR converter. This is very important not to degrade the overall linearity because of mismatches between the two references.

2.2 High-Level Architectural Choices

2.2.1 Incremental ADC

The choice of the optimum OSR was obtained in Chapter 1. The value chosen was 64 with $F_c = 2$ MHz.
Therefore, 7 bits are resolved by the incremental conversion. Theoretically, a 9 bit $SAR\ ADC$ should complete the conversion (actually, 11-bit $SAR\ ADC$ is needed as explained in Section 2.2.3).

Traditionally, 1 bit quantizer is used for first-order sigma-delta converters allowing the use of an inherently-linear two-level DAC. For this application a 3 level (1.5 bits) quantizer is implemented. The use of a three-level DAC retains the advantage of linearity but gives the possibility not to inject the reference signal (and its noise) during every incremental cycle for small signals. The signal-to-noise ratio for small signals is then increased[1]. Two comparators are therefore needed.

In order to simplify the discussion let us assume a unitary reference voltage. Assuming a full scale of ± 1 in a fully differential implementation, the quantizer thresholds can be chosen to be in the order of 0.25-0.35. This leaves some margin on the residue voltage (output of the integrator after OSR cycles) with respect to full-scale. Offsets or other non-idealities in the conversion therefore do not saturate the $SAR\ ADC$.

2.2.2 Incremental ADC Behavioral Simulation

A power-spectral density PSD of the incremental converter alone will give some interesting results. With a full-scale sinusoidal input, results in Figure 2.1 are obtained.

FFT results show that the quantization error is not shaped as in a first-order sigma-delta modulator [14]. It is useful to recall here that the PSD of the quantization error in a sigma-delta modulator is multiplied in frequency by the term $(2\sin(\pi f T_s))^2$ which gives the well known first-order high-pass shape (see Figure 2.2).

By contrast, in an incremental ADC, the quantization error has the typical shape as in a Nyquist rate converter. This fact can be intuitively explained.
Noise shaping is related to the fact that the digital output of the sigma-delta contains a differentiated version of the quantization error. This attenuates low-frequency components.
Incremental $ADCs$, on the other hand, are periodically reset. The memory of the converter is erased after OSR cycles. The $OSR + 1$ sample is no more related to the previous ones. The in-band noise attenuation is still present

[1]See also Chapter 4 for jitter immunity

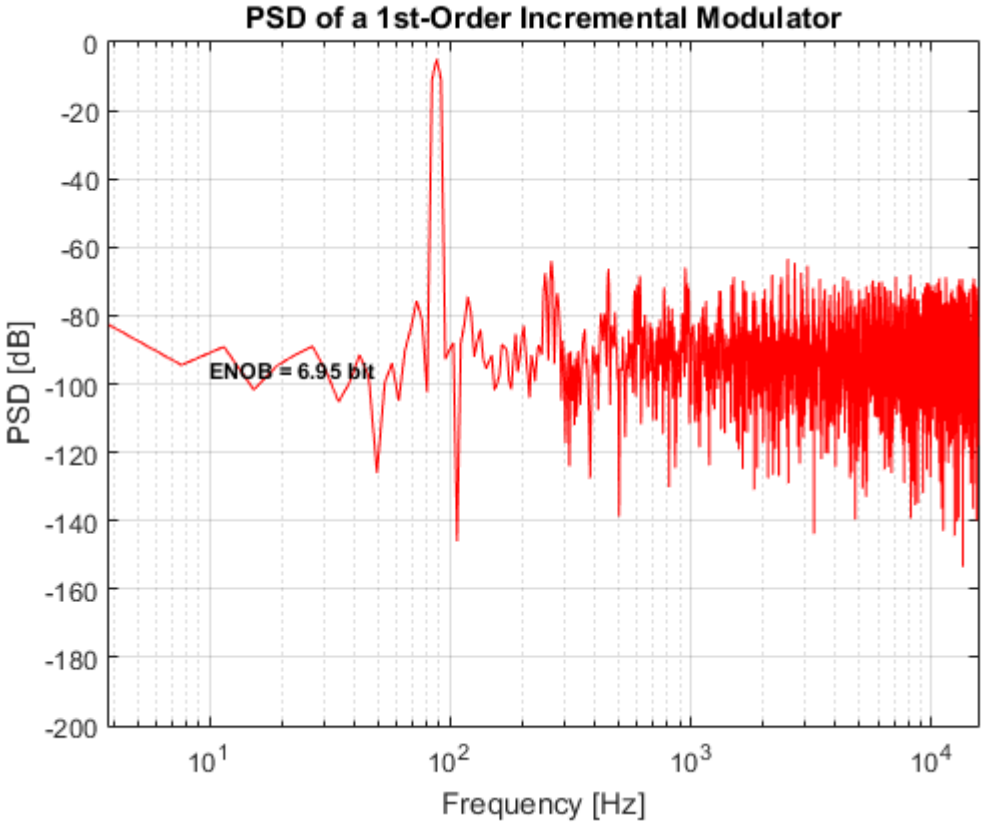

Figure 2.1: PSD of the first-order incremental ADC: $OSR = 64$, full-scale sinusoidal input, quantizer thresholds: 0.3077 V_{ref}

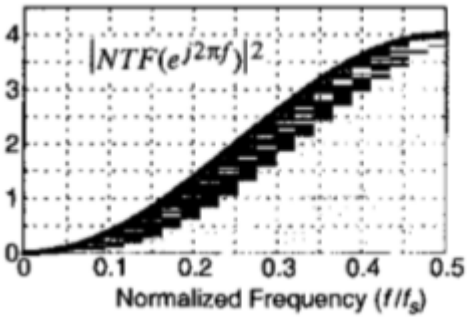

Figure 2.2: First-order noise shaping in sigma delta modulators

for single samples, but it does not exist anymore looking at a spectrum of N samples (in this case the 2^{13} samples of the FFT). This is indeed the price to pay for the periodic reset.

Figure 2.3 represents an example for a high OSR value. Increasing OSR for instance to 1024 would give 11 bits. (fully differential implementation). Notice again that the PSD is totally flat (as expected).

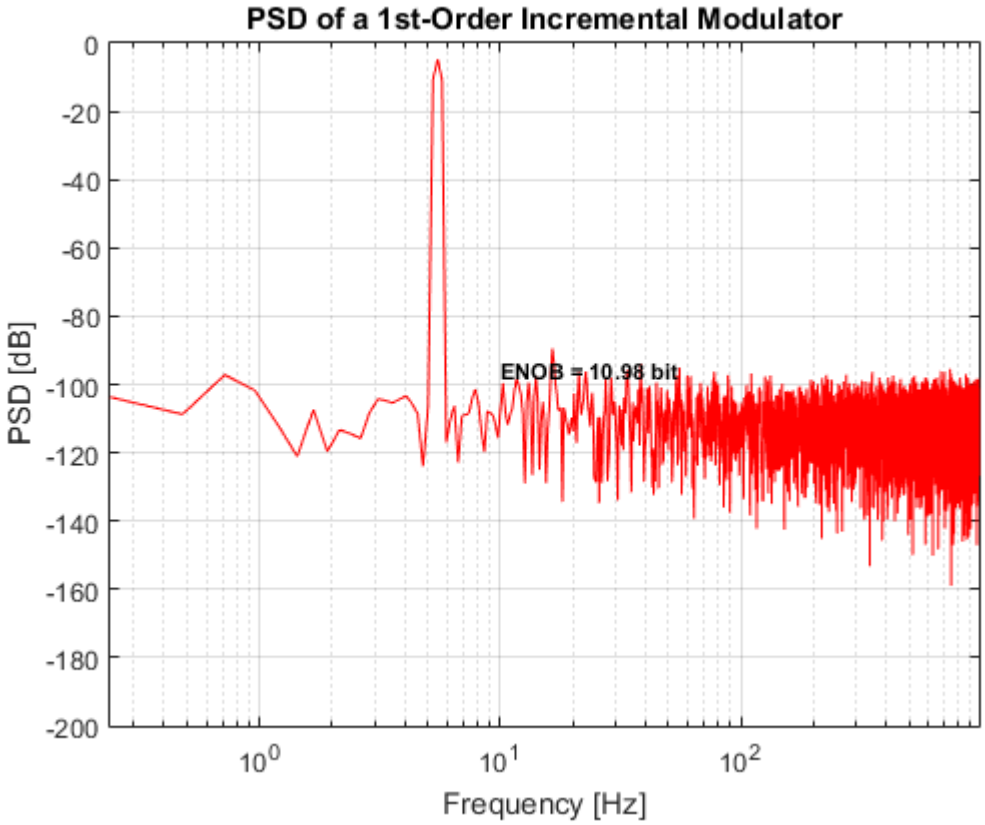

Figure 2.3: PSD of the first-order incremental ADC: $OSR = 1024$, full-scale sinusoidal input, quantizer thresholds: 0.3077 V_{ref}

In Figure 2.4 the residue of the incremental conversion is bounded with a reasonable margin with respect to full-scale. The residue value after the OSR cycles of the incremental conversion is then sampled and converted by a SAR ADC.

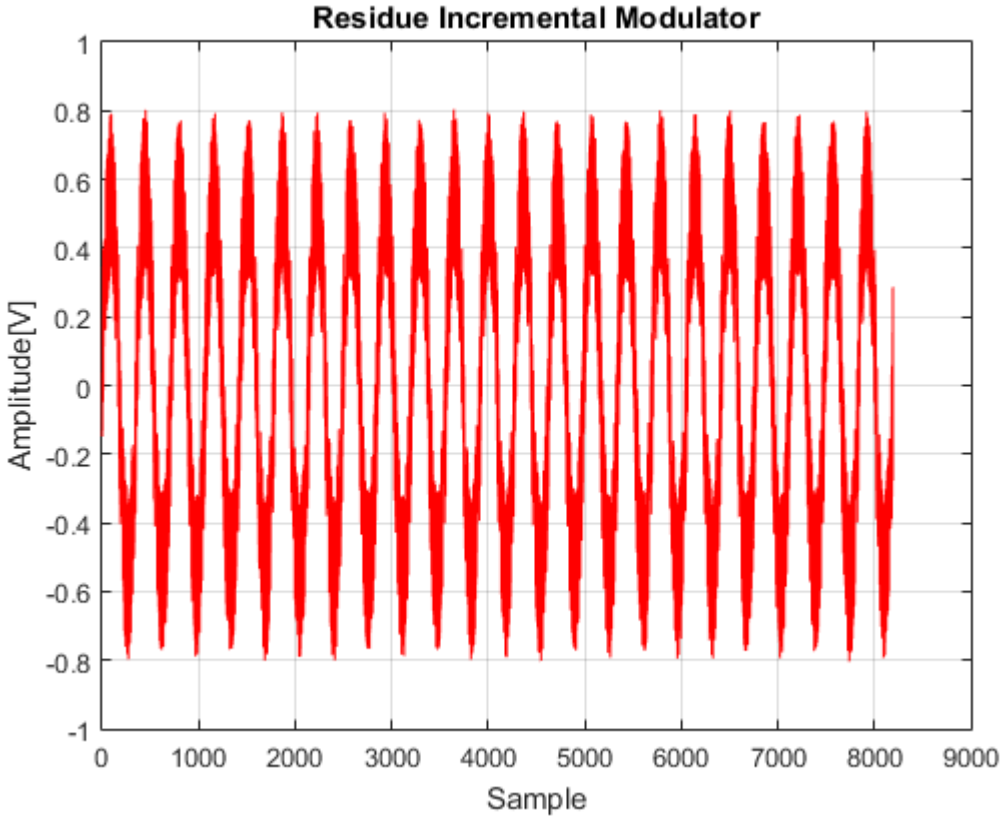

Figure 2.4: Residue of the incremental ADC: $OSR = 64$, full scale sinusoidal input, quantizer thresholds: 0.3077 V_{ref}

2.2.3 SAR ADC

SAR ADC conversion is performed sampling an input signal and then performing M comparisons of the signal with different thresholds [17] [18] [19]. A binary successive approximation algorithm is performed.
For a fully differential implementation the *ADC* (a comparator) can at first detect the sign of the input signal (1 bit resolved) and than compare it with $\frac{V_{ref}}{2}$, $\frac{V_{ref}}{4}$ $\frac{V_{ref}}{8}$ etc... An alternative way without the sign detection is presented in [18].

In this work, an 11-bit *SAR ADC* is needed. Recalling (2.2) it is clear that the overall converted value is achieved as the sum of the incremental *ADC* output and the *SAR ADC* output.
The LSB of the incremental conversion can be expressed as $\frac{2V_{threshold}}{2^6}$ and the LSB of the SAR conversion as $\frac{2V_{ref}}{2^{11}}$.

To have 18 bits (7 from incremental *ADC* and 11 from *SAR ADC*) the reference of *SAR ADC* should be divided by 4 ($\frac{V_{threshold}}{V_{REF}}$ ratio is 0.25 if thresholds are 0.25 with a unitary reference).
This would saturate the SAR conversion. A *SAR ADC* reference scaling with respect to the incremental reference *ADC* would also introduce non-linearity due to non-idealities in the scaling operation.
In the end, two bits are used as redundancy without reference scaling to avoid *SAR ADC* saturation and 16 bits are nominally achieved.

2.2.4 Extended Range Conversion

Figure 2.5 shows the PSD of a nominal conversion with extended range. All elements in the *ADC* are supposed to be ideal. Only quantization is taken into account. Notice once again that the spectrum is flat.
From this ideal model, in the following sections, non-idealities will be added to the model in order to have fundamental guidelines for the transistor level design.

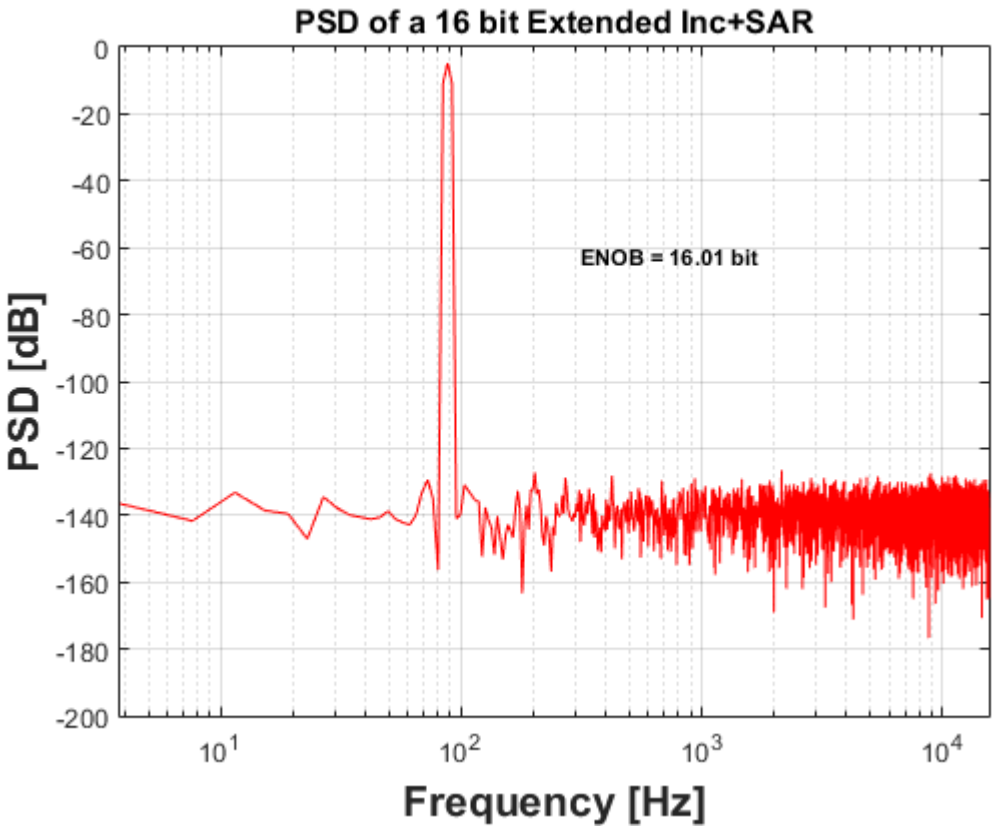

Figure 2.5: PSD of the extended range ADC: $OSR = 64$, full scale sinusoidal input, quantizer thresholds: 0.3077 V_{ref}

2.3 Integrator Finite Slew-Rate, Bandwidth and DC Gain

The response of the SC integrator should ideally follow the equation

$$V_{out} = \frac{C_{in}}{C_{int}} V_{in} \tag{2.3}$$

However, when a voltage step is applied to the integrator the real behavior is different.

Let us assume first that the integrator has infinite slew rate and DC gain, but finite gain-bandwidth product (GBW). The response is linear and the operational amplifier exhibits a linear settling. Under the hypothesis of single-pole response, the settling time depends on the GBW of the integrator loop gain.

The resulting error is proportional to the input signal. It follows that the finite GBW effect in an incremental or sigma-delta converter is a gain error [12].

The Extended conversion, however, exhibits non-linearity (DNL) due to limited GBW. Indeed, suppose that a small signal (near zero) is converted by the ADC. The result of the incremental conversion is zero, while the $SAR\ ADC$ provides a certain value.

When the input signal increases and the result of the incremental conversion becomes +1, the result of the overall conversion is given by (2.2) with $N = 1$. In the ideal case, the transition from 0 to 1 of the coarse ADC ($DNL = 0$) requires that the incremental ADC output, summed with the value given by $SAR\ ADC$ is 1 code greater than the value converted by the SAR alone just before the transition from 0 to +1 of the incremental ADC output.

This is possible only if the integrator settles with the same accuracy as $SAR\ ADC$ resolution. With proper timing, the integrator has half a clock period to settle. From

$$e^{\frac{-t\beta}{\tau}} = \frac{1}{2^{11}} \tag{2.4}$$

and

$$\tau = \frac{1}{2\pi f_{GBW}} \tag{2.5}$$

where β is the feedback factor $\frac{C_{int}}{C_{in}+C_{int}}$ and $t = \frac{T_c}{2}$, it follows:

$$f_{GBW} = \frac{ln(2^{11})}{2\pi t\beta} \tag{2.6}$$

Assuming a variation of GBW due to process and temperature of the order of 30%, a value of about 10 MHz is required to avoid performance degradation.

An example of non-linearity of the extended range conversion is shown in Figure 2.6, where the integrator has 5 MHz GBW.

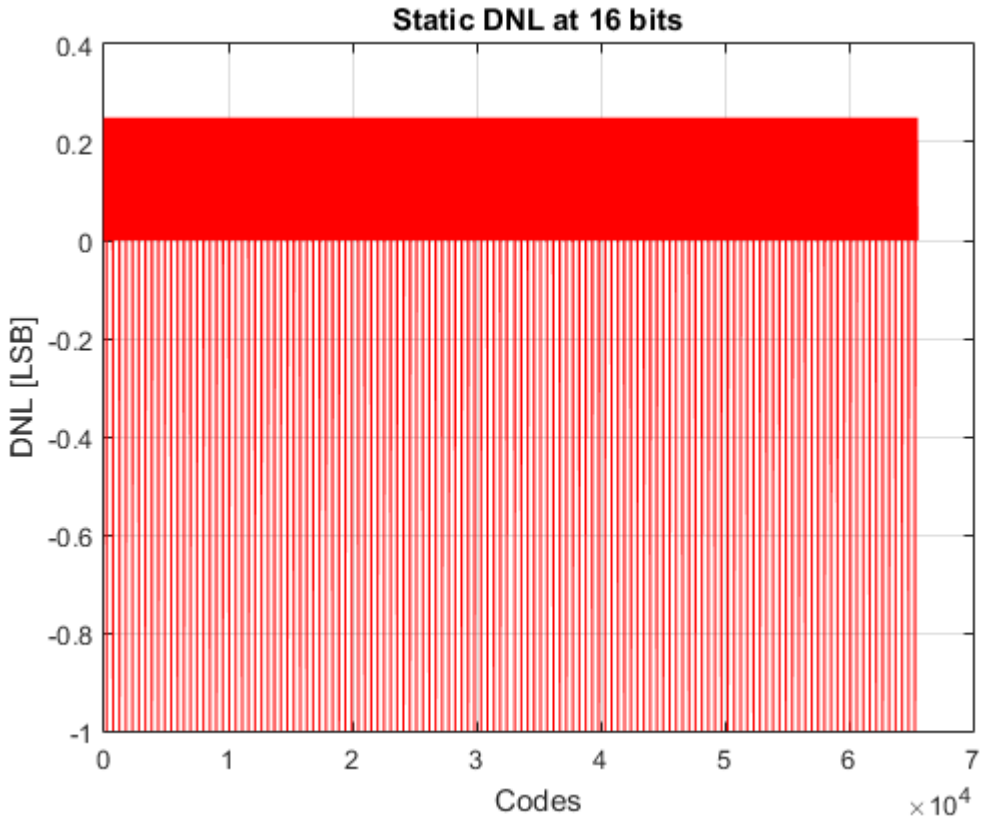

Figure 2.6: Static DNL at 16 bits: non linearity due to the effect of limited GBW

At every transition of the coarse ADC a peak in the DNL curve is evident. Missing codes ($DNL = -1$) are present.

Another effect to be taken into account is the large signal behavior of the integrator. For large signal, before beginning the linear settling, integrator features a slewing phase.

Slew-rate is a non-linear phenomenon that reduces the time available for linear settling.

From the equations in [12], it seems at a first glance that reducing the GBW has positive effect. Indeed, the initial slope of the integrator, with a certain input signal, reduces if GBW reduces. The problem is that also the slew-rate (SR) reduces.
In a two-stage Miller compensated OTA the GBW is $\frac{gm_{input}}{C_c}$. If MOS transistors operate in sub-threshold region gm_{input} is proportional to the bias current.
The slew-rate (SR) is $\frac{I_{input}}{C_c}$. It follows that reducing the bandwidth by a factor two also reduces the SR by the same amount.

Let us suppose to have 10 μA bias current. If the input MOS transistors are in the sub-threshold region they behave as bipolar transistors. Their transconductance gm is $\frac{Id}{n\,V_T}$. Suppose that $n = 1.5$, then $gm = 266$ μS. In order to have 5-MHz GBW, $C_c = 8.5$ pF. It follows that $SR = 1.2$ $\frac{\mathrm{V}}{\mu\mathrm{s}}$.

The use of the real value of the reference voltage here is advisable. The required slope depends indeed on the absolute value of the reference.

In Figure 2.7 the values $SR = 1.2$ $\frac{\mathrm{V}}{\mu\mathrm{s}}$ and $GBW = 5$ MHz are used in the Matlab model. Strong non-linearity (missing codes and non-monotonicity) is again present at transitions between the coarse and the fine conversions.

Increasing the GBW by a factor two (also increasing SR by the same factor) reduces this effect. Results with 10-MHz GBW and $SR = 2.4$ $\frac{\mathrm{V}}{\mu\mathrm{s}}$. are presented in Figure 2.8 and Figure 2.9.

Linearity has improved but it still suffers from limited slew rate. Also INL is shown for the sake of completeness. This confirms that the system is not linear and linear system considerations based on GBW are not sufficient to forecast the behavior of the integrator.
The model shows that, fixed the GBW at 10 MHz, a $SR = 10$ $\frac{\mathrm{V}}{\mu\mathrm{s}}$ substantially eliminates the non-linearity.

DC gain effect can be taken into account with the following formula:

$$V_{out} = V_{in}\frac{C_1}{C_2 + \frac{1}{A}C_1 + \frac{1}{A}C_2} \tag{2.7}$$

Figure 2.10 shows the overall linearity with $A = 60$ dB.

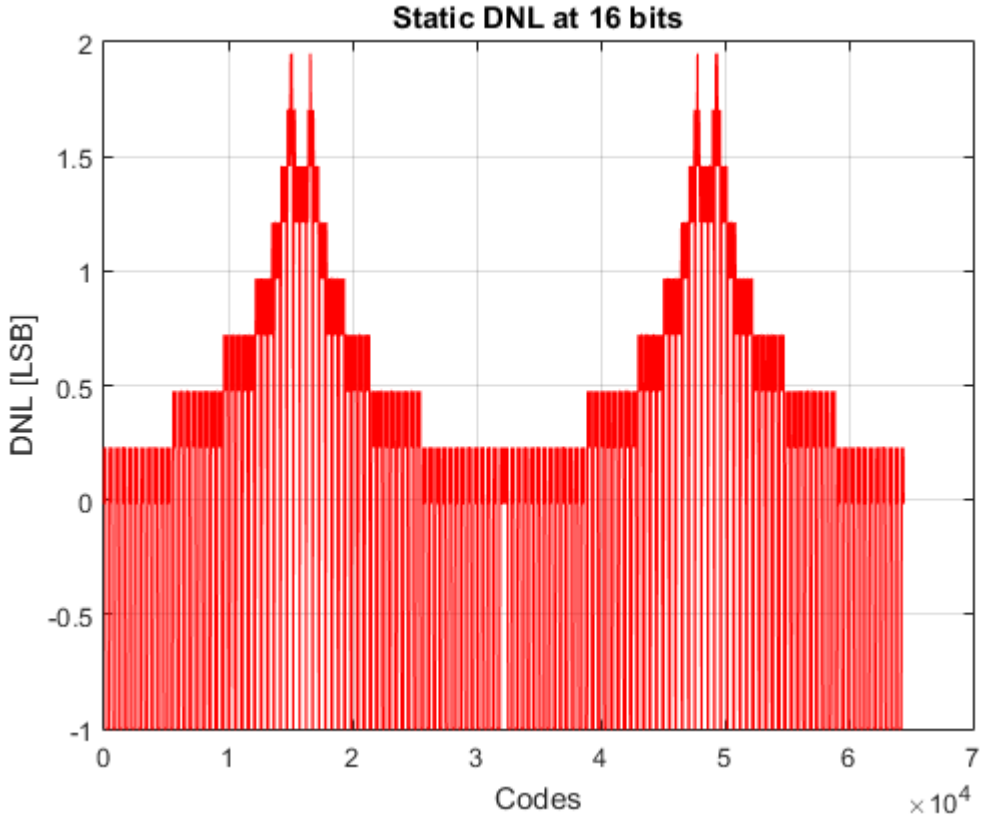

Figure 2.7: Static DNL at 16 bits: non-linearity due to the effect of limited SR and GBW

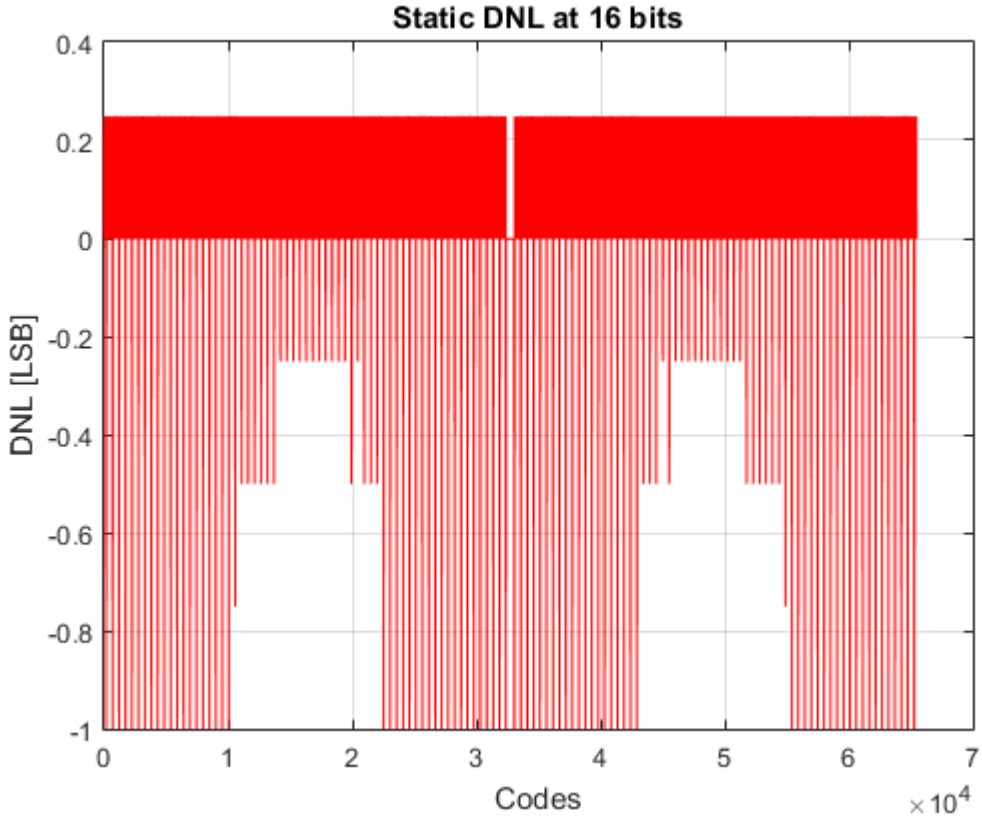

Figure 2.8: Static DNL at 16 bits: non-linearity reduced. Limited SR and GBW

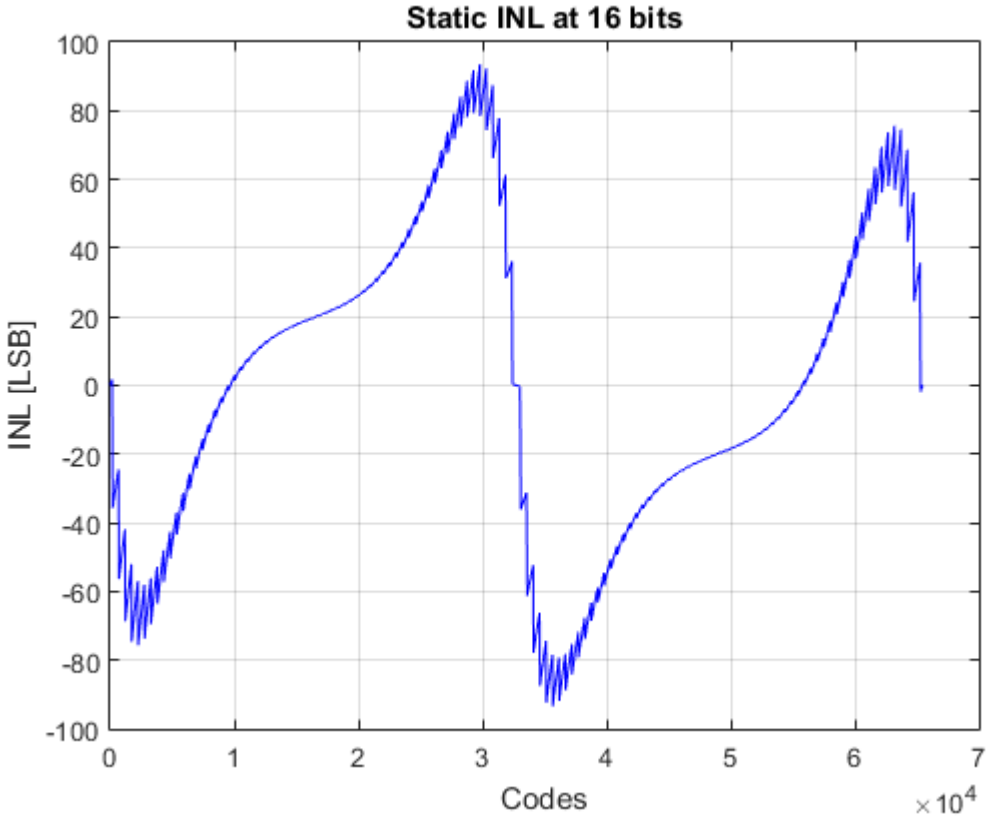

Figure 2.9: Static INL at 16 bits: non-linearity reduced. Limited SR and GBW

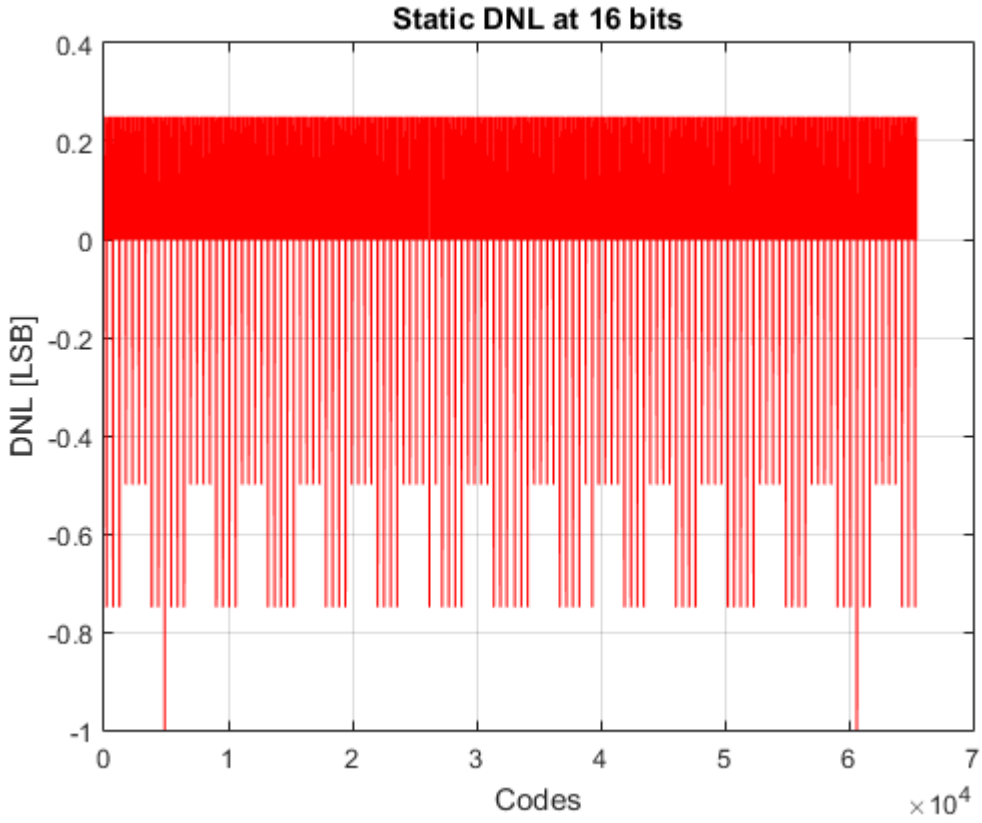

Figure 2.10: Static DNL at 16 bits: non-linearity due to finite DC gain

A DC gain of 80 dB is a value that does not affect linearity and will be chosen for the design.

2.4 Voltage Reference Requirements

Reference voltage choice is determined by specification in terms of signal range required by the ADC (see Table 2.1).
With a supply of 1.5 V the reference can be chosen as 1.3 V. This value determines the full scale of the ADC and the LSB.
LSB will be

$$\frac{2V_{Ref}}{2^{16}}$$

.

The reference voltage buffer requirement in terms of GBW follows the same considerations done for the integrator. If the reference is realized using a buffer with unity feedback factor its GBW requirement for the incremental ADC is given by (2.6) with $\beta = 1$. The GBW required to avoid non-linearity is of the order of 7 MHz.
The $SAR\ ADC$ reference, which will be the same reference used for the incremental converter, has almost twice the time allowed for settling within an LSB (500 ns) with respect to the incremental converter.

2.5 SAR ADC Non-Linearity

The last source of non-linearity in the extended range conversion is represented by the $SAR\ ADC$ capacitive array.
Non-linearity in a charge redistribution $SAR\ ADC$ comes from mismatch among capacitors (smaller capacitors, larger mismatch). The structure is parasitic insensitive[2].
Another source of non-linearity is represented by systematic errors in the layout. We can surmise that capacitors are smaller or bigger than nominal design values. This sources of error can be added to the Matlab model.

[2]In a split DAC array the LSB top plate parasitic generates non-linearity.

The input of the comparator in a *SAR ADC* evolves, during the bit-cycling phase [3], following the equation

$$V_{SAR_{in}} = \sum_{k=1}^{nbit-1} V_{ref} \frac{C_k(1+\epsilon_k)b_k}{\sum_{j=1}^{nbit} C_k(1+\epsilon_k)} \tag{2.8}$$

where ϵ_k is the percentage error associated with single capacitors with respect to their nominal value and b_k is one or zero depending on the result of the comparison between the input signal and the *SAR* thresholds.

Equation (2.8) gives important hints on the *ADC* linearity. The error allowed on the single capacitor depends on the resolution of the *SAR ADC* (in this case 11 bits). Because of sign detection, the number of comparisons is 10. The error on the largest capacitor, in order to avoid non-linearity, has to be lower than $\frac{100}{2^{10}}\%$. The error on the single capacitor also affects the total capacitance of the array (C_{tot}-denominator in (2.8)) while the same percentage error generates worse non linearity behavior if related to bigger capacitors. One can notice that the same percentage error on smaller capacitors has indeed less effect.
Since smaller capacitors suffer from greater mismatch errors, the last property is fundamental for the feasibility of the *SAR ADC* converter. It is possible to scale down capacitors to very small values (given a certain mismatch from the technology).

The most important issue for the layout is to avoid large systematic errors in the array.

2.6 Noise Analysis

2.6.1 Thermal Noise

Figure 2.5 shows the *PSD* obtained with an ideal extended range conversion. The only noise source is the quantization error. In a n bit converter the power

[3] The equation only wants to represent the evolution of the comparator input due to the binary search algorithm.

of the quantization error, expressed in V^2 is

$$V_{quant}^2 = \frac{LSB^2}{12} \tag{2.9}$$

This is the noise contribution due to quantization in an ideal n bit converter. Indeed, amplitude quantization introduces an error intrinsic in the operation of approximation of a continuous amplitude signal (analog signal) into a discrete one (digital signal).

Clearly other sources of noise are present in a real converter.
In a SC incremental converter the first limiting noise source is the thermal noise. Thermal noise is caused by the on-resistance of the switches. It can be shown that [20] the integrated power (referred to the input of the converter) of this noise contribution is

$$V_{thermal}^2 = \frac{kT}{C_{in}} \tag{2.10}$$

In a fully differential implementation four $\frac{kT}{C_{in}}$ terms should be added to the model to account for all the required input branches. Equation (2.10) referred to the converter bandwidth allows to define the sizing of input and integrating capacitors. Since thermal and quantization noise are uncorrelated, their powers have to be summed. This means that, if thermal noise power equals quantization noise power, 0.5 bits of resolution will be lost:

$$4\frac{kT}{C_{in}OSR} = \frac{LSB^2}{12}$$

and hence

$$C_{in} = \frac{4kT}{\frac{LSB^2}{12}OSR} \tag{2.11}$$

To obtain 15.5 bits, $C_{in} = 1.97$ pF.

The results shown in Figure 2.11 confirm the validity of (2.11). For area requirements and in order to reduce the driving capability required for the anti-aliasing filter, the capacitance value chosen is 100 fF instead. This clearly increases the thermal noise floor well above the quantization noise, as shown in Figure 2.12.

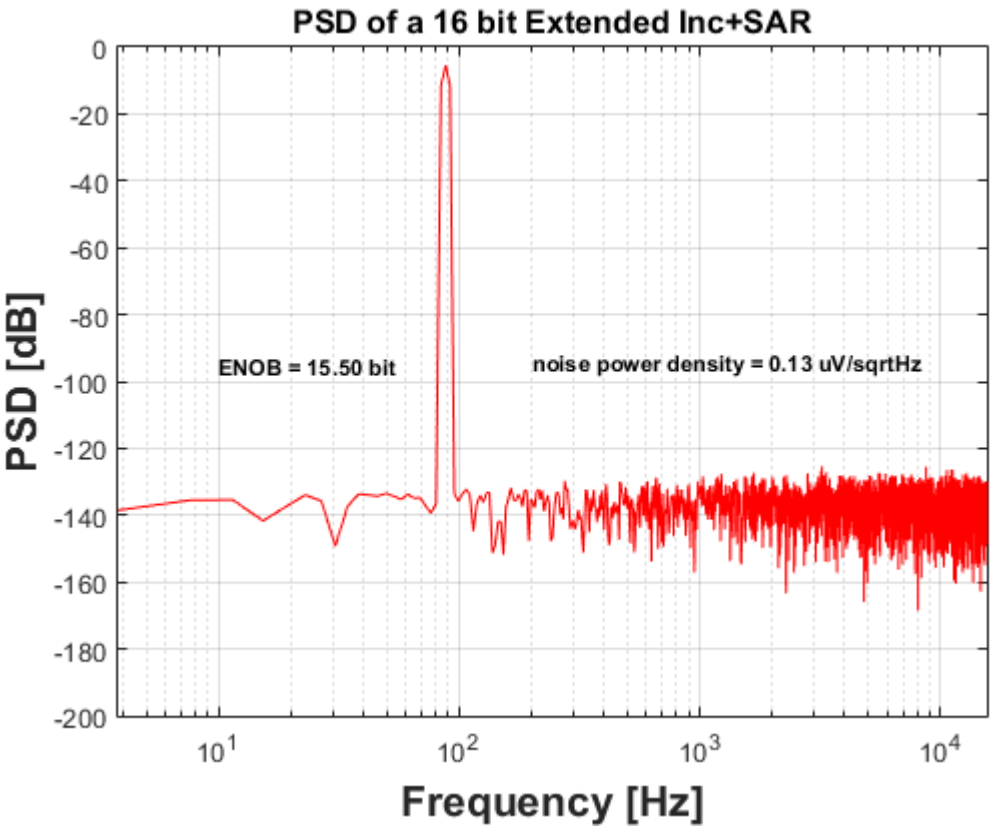

Figure 2.11: $\frac{kT}{C}$ noise effect on the converter resolution

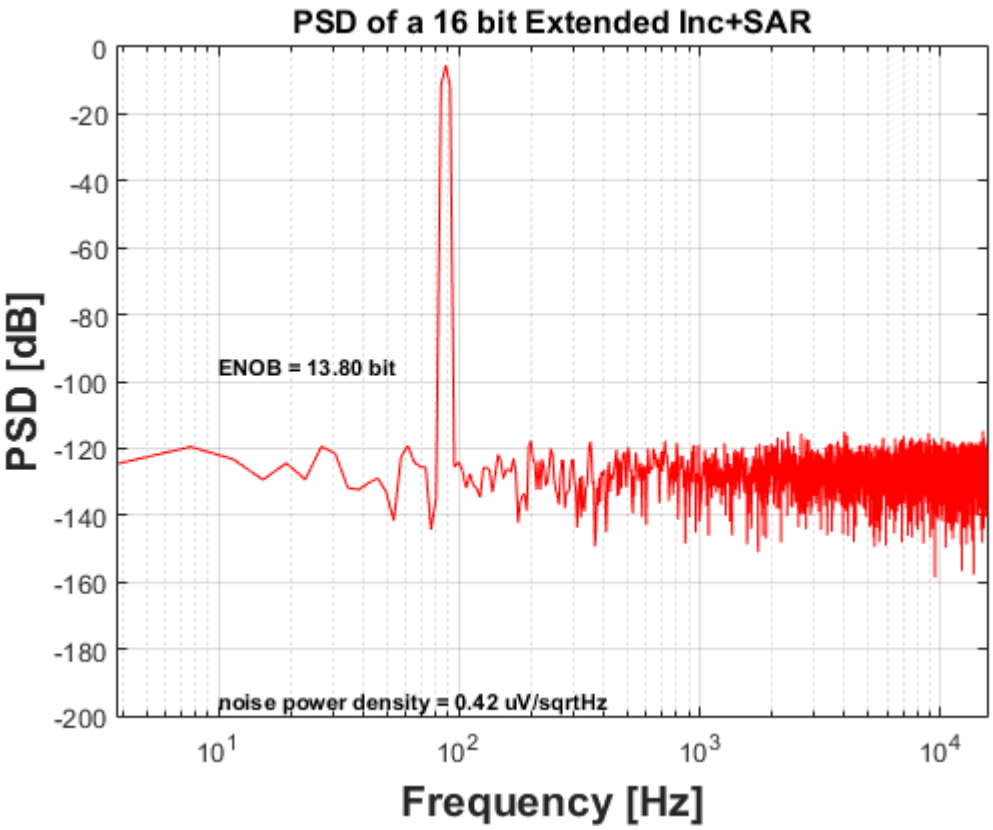

Figure 2.12: $\frac{kT}{C}$ noise effect on the converter resolution with 100 fF input capacitance

2.6.2 Integrator and Anti-Aliasing Filter Noise

An-anti aliasing filter in front of the converter is often used in discrete-time converters to prevent folding of unwanted high-frequency signals in the baseband when sampling [11]. In this application the anti-aliasing filter is used to avoid that spurs and noise around the sampling frequency (2 MHz), coming from the accelerometer channel, fold into the baseband. This block is an active *RC* first-order filter. Its noise is injected at the input of the converter. The integrator noise is the other fundamental noise source limiting converter resolution.

Both the integrator and the anti-aliasing filter are based on operational transconductance amplifiers (OTA). Their noise contribution will be determined with simulations with Spectre RF in Chapter 3. It is anyway possible to define here, as usual, fundamental guidelines for the design.

The OTA noise PSD consists of flicker ($\frac{1}{f}$) and white (or thermal) noise contributions (Figure 2.13).

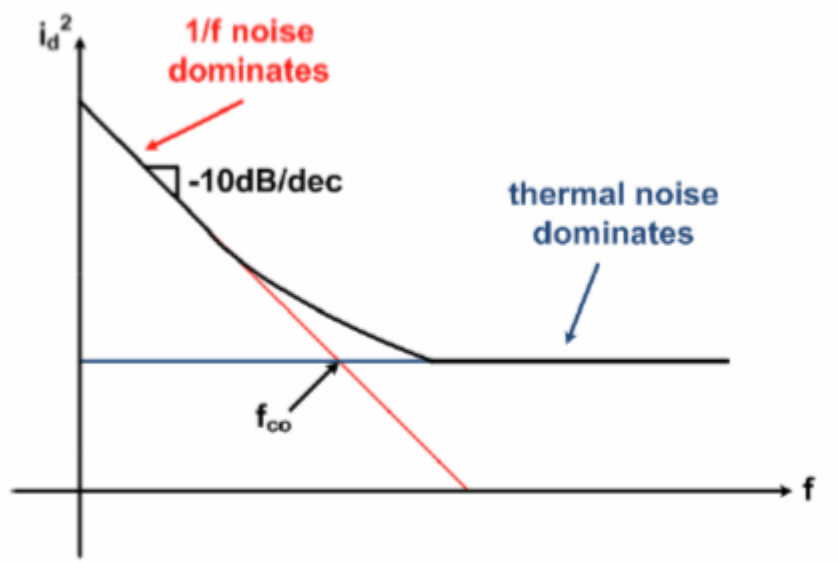

Figure 2.13: OTA noise: flicker and thermal noise. After the corner frequency white noise dominates

Both the integrator and the anti-aliasing filter need some sort of offset cancellation technique. Chopping will be used in this design. This techniques

modulates the offset (and $\frac{1}{f}$ noise) at the chopping frequency (and its odd harmonics) [21]. This means that the noise spectrum, after chopping, can be approximatively considered white. The thermal noise density of a MOS transistor, when referred to its gate, can be well approximated as [20] [22]

$$V_n^2 = \frac{4kT\gamma}{gm} \left[\frac{V^2}{Hz}\right] \tag{2.12}$$

In a standard Miller compensated OTA the main noise contributors to the input referred noise are the input pair transistor.
It is useful to anticipate here that in the folded-cascode topology adopted in this design, to meet the specifications in terms of gain and GBW, major contributors are also the current source devices. Six MOS transistors significantly contribute to noise (the two input pair devices and four current sources). The total input referred noise can then be approximated as

$$V_n^2 = \frac{8kT\gamma}{gm_{input-pair}}(1 + \frac{2gm_c}{gm_{input-pair}}) \, [\frac{V^2}{Hz}] \tag{2.13}$$

where $gm_{input-pair}$ and gm_c are the transconductances of the input pair and of the current sources, respectively. In a discrete-time converter, the noise is actually sampled at F_c. This causes folding of the components around the sampling frequency and its multiples into the baseband.

The noise PSD at the output of the OTA is then strongly attenuated for frequencies higher that the GBW value of 10 MHz. With a rough approximation it is possible to limit noise folding at the GBW value. This means that (2.13) needs to be multiplied by a factor 5.

To define the value of gm (and consequently the current necessary for the $OTAs$), we can use the equation

$$V_n^2 = 5\frac{8kT\gamma}{gm_{input-pair}}(1 + \frac{2gm_c}{gm_{input-pair}}) = \frac{LSB^2}{12BW} \tag{2.14}$$

Under the condition that $gm_c = gm_{input-pair}$

$$gm_{input-pair} = \frac{120kT\gamma}{\frac{LSB^2}{12BW}} \tag{2.15}$$

It follows that gm=38 μS.

The calculated value of *gm* is added to the Matlab model. Again 0.5 bits of noise are lost (Figure 2.14). It is clear that, with the choice of 100-fF input capacitance the thermal noise will dominate over the noise of the transistors.

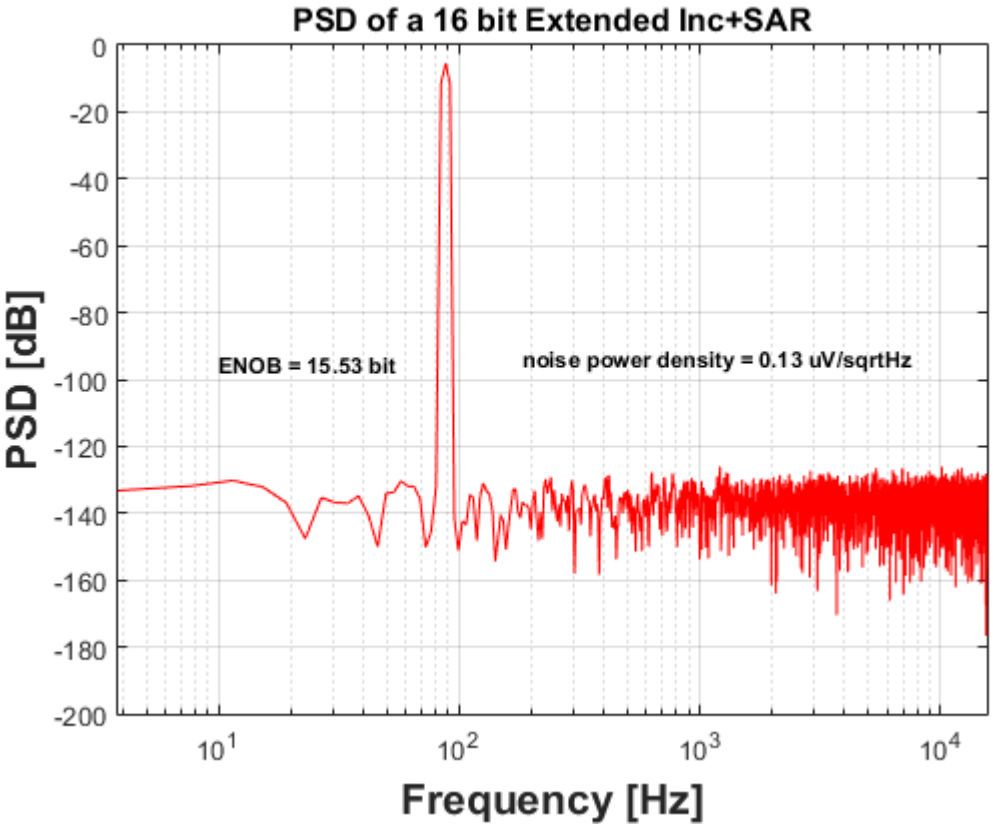

Figure 2.14: Integrator noise effect on the converter resolution

2.6.3 Reference Noise

The reference voltage generation for the *ADC* requires a buffer. This buffer has to be implemented with a resistive division (see Chapter 3). Its noise, assuming the same power consumption used for the integrator, will be higher. It should be recalled here that the incremental conversion is performed with a 3 level quantizer. This means that the noise of the reference voltage will be relevant only for high signal.

2.6.4 SAR ADC Noise

The *SAR ADC* relevant noise contribution with respect to quantization noise is caused by the reference voltages and by the input referred noise of the comparator. *SAR ADC* noise is anyway negligible for the overall resolution of the converter. This will be clarified in Chapter 3.

2.7 Conclusions

In this chapter a Matlab model for the extended range conversion has been developed. Starting from the fundamental equations of the converter, the ideal behavior of the *ADC* has been simulated.
Then, the different non-idealities and their effect on noise and linearity of the converter have been evaluated.

A summary table of the nominal performances and *ADC* characteristics is shown below.

Table 2.1: Data Converter nominal performances and characteristics

Parameter	*Spec*	*Unit*
Current consumption	< 100	μA
Area	< 0.1	mm^2
Linearity-INL	± 1	LSB at 16 bit
Linearity-DNL	± 1	LSB at 16 bit
Resolution (nominal)	16	bit
Full scale voltage	1.3	V
LSB	40	μV
Conversion time (single axis)	40	μs

Transistor level simulations will clearly give more accurate results.

Chapter 3

Switched Capacitor Incremental and SAR ADC Design

This chapter will analyze in detail the design of the analog blocks of the incremental and *SAR ADCs*. Analog block requirements, coming from the Matlab model described in Chapter 2, will guide the design. Transistor level simulations will use Spectre simulator and the option SpectreRF.

3.1 Biasing Circuit

The biasing structure for all the analog blocks is illustrated in Figure 3.1. Every block has its own local bias[1]. An input current is supplied to a diode connected NMOS. A current mirror biases other two branches for the generation of voltages V_{bpc} and V_{bp} for biasing PMOS cascode transitors.
A PMOS cascode current mirror acts as bias for another branch to generate voltage V_{bnc} for biasing the NMOS cascode transistors.
In order to have large r_{ds} (drain to source resistance) in cascode structures[2], long devices are required. For current sources the length L is about 10 times the width W.

[1]This approach is usually called current distribution. While voltage distribution reduces power consumption, local bias generation is much more robust and avoids variations of the biasing conditions (gate voltages) among different blocks.

[2]Long devices with high r_{ds} increase the gain of a cascode structure.

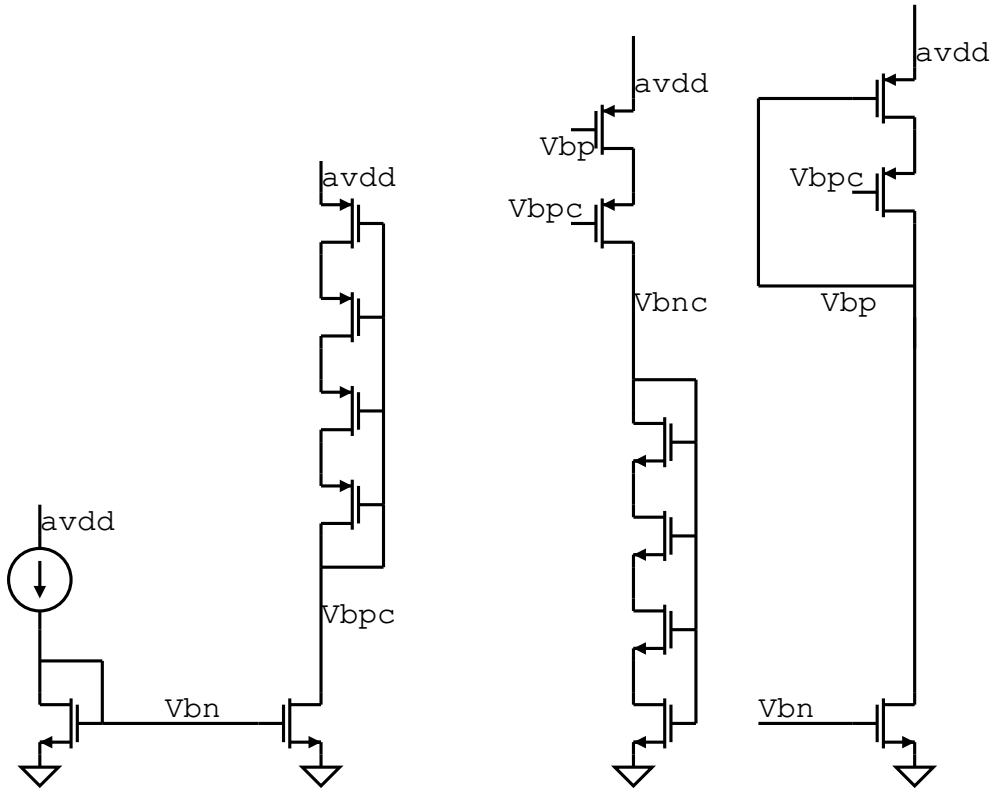

Figure 3.1: Biasing scheme for the analog blocks

3.2 Incremental ADC Integrator

3.2.1 Integrator Timing

The integrator used in the incremental ADC is the most critical block of the entire design. Indeed, its performances affect linearity and noise of the whole system. A switched-capacitor implementation requires two non-overlapping clock phases to drive the switches (Figure 3.2) [12].

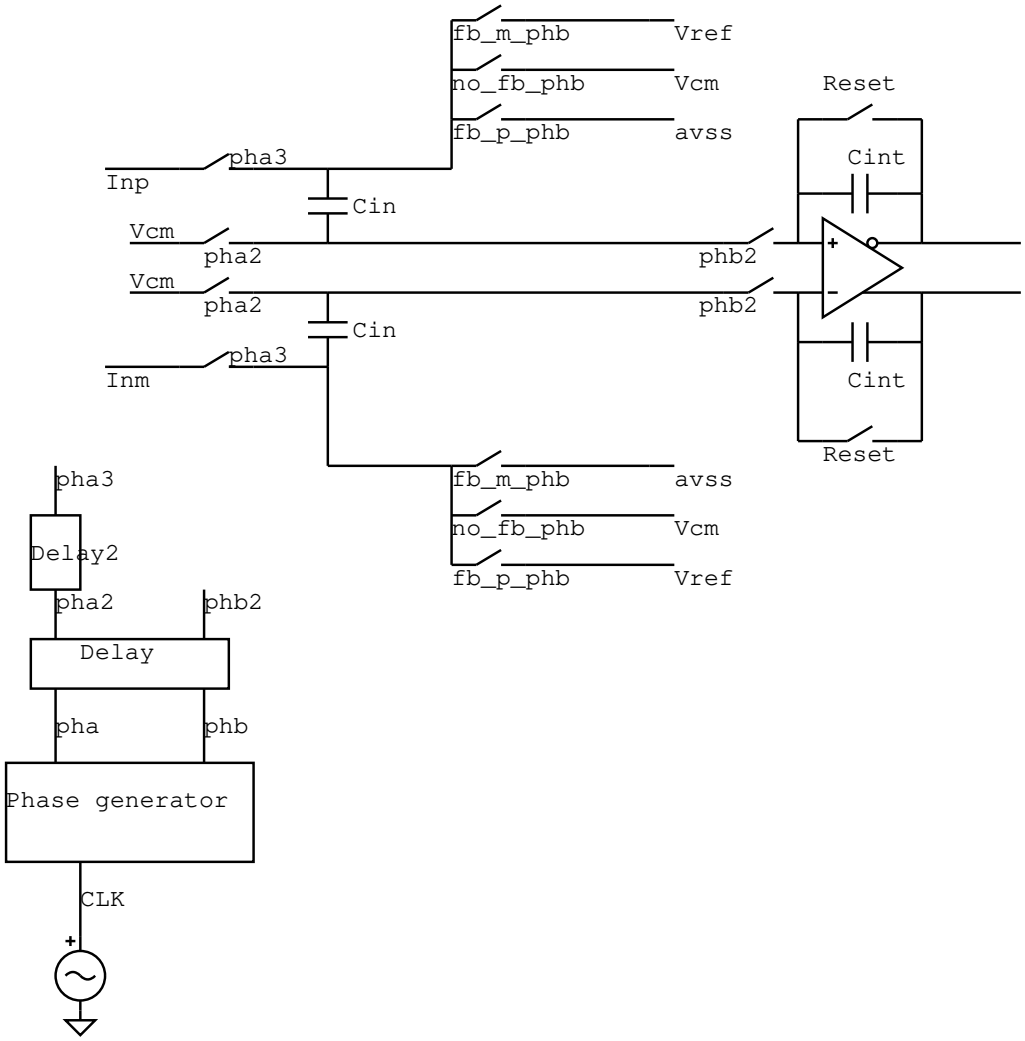

Figure 3.2: SC ADC switches

During phase a (pha) the input signal is sampled on the input capacitors.

During phase b (phb), the integration phase, the integrator output settles. The timing diagram, from the simulation test bench, is shown in Figure 3.3. In

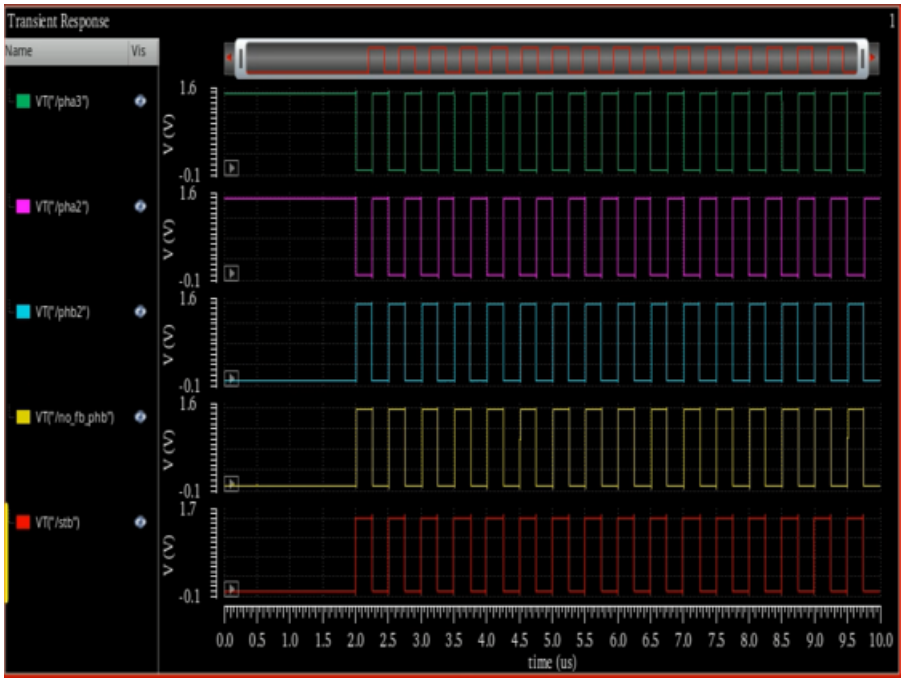

Figure 3.3: SC ADC timing

order to avoid non-linearity in the conversion [20], the bottom plate switch of the input capacitor C_{in} has to be turned off first, before the top plate switch turns off and the integration phase begins ($pha2$ slightly anticipates $pha3$ in Figure 3.2 and Figure 3.3). The comparator strobing (stb) is performed about 10 ns before the beginning of the integration phase.

3.2.2 Integrator Analog Design

The Matlab model indicates guidelines for the OTA design. The linearity of the conversion is affected by DC gain, slew-rate, and bandwidth of the OTA. The Matlab model suggests to have 10 MHz GBW and at least 80 dB DC gain.

The transconductance gm required is of the order of 38 μS from noise requirements. The tail current required in the OTA then turns out to be 3 μA.

The maximum output swing of the integrator is basically the full-scale signal

applied when the output of the integrator is slightly below the comparator threshold. For this design, choosing 850 mV and 450 mV as thresholds for the quantizer with 650-mV common mode voltage at the output of the OTA and a 1.3-V reference voltage, the largest voltage at the output of the integrator is 1.175 V (about 300 mV below the analog VDD). Given this large output swing requirement and the need for a high DC gain, a two stage OTA is required with a cascode topology in the first stage. A folded-cascode two stage OTA is then used (Figure 3.4)

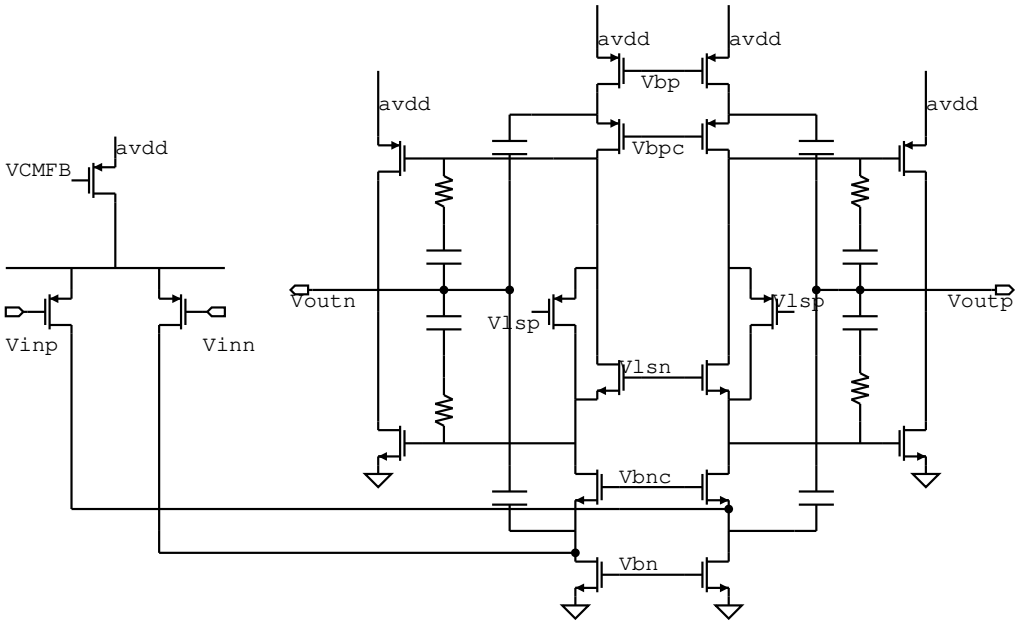

Figure 3.4: Schematic of the OTA used in the SC integrator

Given the tight specification on current consumption, MOS transistors operate in subthreshold region with low currents. Their transconductance in this condition is given by the well known relation

$$gm = \frac{I_d\, q}{n\, k\, T} \tag{3.1}$$

For a two stage OTA, the gain-bandwidth product can be found at frequency

$$GBW = \frac{gm_{in}}{C_c} \tag{3.2}$$

Since $gm_{in} = 38\ \mu$S and the GBW specification is 10 MHz, the compensating capacitance required is 605 fF.

In a Miller compensated two stage OTA the output pole is approximatively at frequency

$$p_2 = \frac{gm_{out}}{C_L} \tag{3.3}$$

where gm_{out} is the transconductance of the second stage and C_L is the load capacitance.

C_L in this case is the sum of the input capacitance of the comparators and the parasitic capacitance of the integrator feedback capacitors[3].

In order to avoid the need for increasing current in the output branch of the OTA (to push the non-dominant output pole away from GBW in frequency), a possible solution is compensating with the approach presented in [23]. In this case, the GBW of the OTA remains at the same frequency as in (3.2), while the output pole is moved approximatively at frequency

$$p_2 = \frac{gm_c gm_{out} R_{eq}}{C_L} \tag{3.4}$$

This relationship can be obtained with the aid of the equivalent circuit shown in Figure 3.5

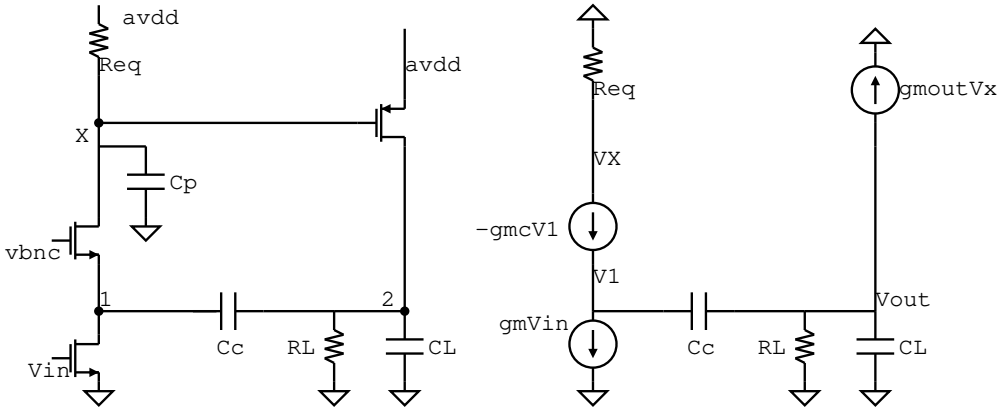

Figure 3.5: Simplified circuit to obtain relationship (3.4)

In the following calculations we assume the parasitic capacitance (C_p) at node X to be negligible. This allows to have a transfer function with two poles and one zero, that gives insight into the circuit behavior (after some further

[3]A certain amount of load capacitance is also introduced by capacitors used for common mode feedback detection.

approximations).
Solving KCL at nodes X, 1 and 2, we obtain

$$\begin{cases} \frac{-V_x}{R_{eq}} + gm_c V_1 = 0 \\ -gm_c V_1 + (V_{out} - V_1)sC_c - gm_{in}V_{in} = 0 \\ -gm_{out}V_x - \frac{V_{out}}{R_L} - sV_{out}C_L - (V_{out} - V_1)sC_c \end{cases} \tag{3.5}$$

which leads to

$$\frac{V_{out}}{V_{in}} = \frac{R_L R_{eq} gm_{in} gm_c gm_{out} - sC_c R_L gm_{in}}{s^2 C_L C_c R_L + s(gm_c(C_c R_L R_{eq} gm_{out} + (C_c R_L + C_L R_L)) + C_c) + gm_c} \tag{3.6}$$

The second, third, and fourth terms in the first-order term of the denominator are negligible compared to $(gm_c(C_c R_L R_{eq} gm_{out})$ This leads to a transfer function with two poles located at

$$\begin{cases} s = -\frac{\sqrt{C_c^2 R_L^2 R_{eq}^2 gm_c^2 gm_{out}^2 - 4C_L C_c R_L gm_c} + C_c R_L R_{eq} gm_c gm_{out}}{2C_L C_c R_L} \\ s = \frac{\sqrt{C_c^2 R_L^2 R_{eq}^2 gm_c^2 gm_{out}^2 - 4C_L C_c R_L gm_c} - C_c R_L R_{eq} gm_c gm_{out}}{2C_L C_c R_L} \end{cases} \tag{3.7}$$

It follows that pole splitting is achieved and the non-dominant pole is approximatively at (3.4). A right-half plane zero is located at $\frac{gm_c gm_{out} R_{eq}}{C_c}$.
This zero is at higher frequency than GBW.

In the previous analysis the parasitic capacitance C_p at node X was neglected. Being in parallel with R_{eq} its effect is to lower the value of the equivalent impedance of the cascode for high frequencies, affecting (3.4) and also the position of the zero.
The equivalent resistance R_{eq} of the cascode configuration is very high. It follows that at the GBW frequency the parasitic capacitance will dominate over the resistance. In order to reduce this effect it is helpful to split the compensating capacitance C_c. The total value of C_c remains the same, but part of the compensation is connected from the output of the first stage to the output of the second stage as in a traditional Miller compensation scheme.
The Miller capacitance is in series with the parasitic capacitance at node X and its effect is then beneficial for stability.
In this design $\frac{2}{3}C_c$ is chosen as cascode compensation. The remaining $\frac{1}{3}C_c$ is left for the Miller compensation.

Simulation results for stability of the OTA are presented in Figure 3.6. The minimum phase margin is 61° in the worst temperature-process corner. With

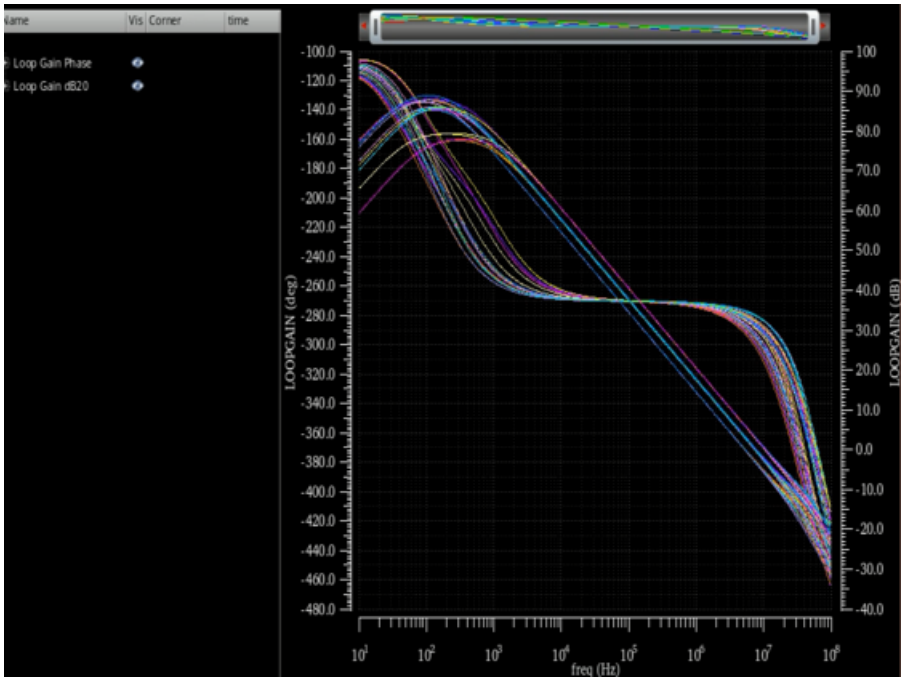

Figure 3.6: Loop gain of the integrator in the different simulation corners

this compensation scheme, the current consumption in the OTA output stage is 1.5 μA.

High slew-rate values can be achieved in the output stage with class AB operation. This has a positive side effects also on stability since the equivalent output conductance will be the sum of the transconductances of the PMOS and the NMOS transistors. Level shifters are needed for proper biasing, as well as branches (not shown for simplicity in Figure 3.4) to generate the bias voltages $Vlsp$ and $Vlsn$.

The maximum slew-rate is determined by the current flowing from the PMOS cascode branch of the first stage both through the cascode and Miller compensation capacitances. The current in the first-stage PMOS cascode branch has to be designed to have the ratio $\frac{I_{cascode}}{C_c}$ equal to the value determined by the Matlab model. The value $I_{cascode} = 1.5$ μA is a good choice to provide some margin from process and temperature variations.

The offset of the OTA is canceled by chopping operation. This well known

technique [21] modulates the offset and $\frac{1}{f}$ noise at the chopping frequency and its odd harmonics.
Half of the incremental conversion is performed with a positive offset, the other half with negative offset, thus canceling its effect. The assumption is that the offset does not change during one conversion. This is reasonable considering that the offset changes with temperature, but the conversion takes only tens of μs.

The last design issue is represented by the operation of the integrator when the residue has to be sampled on the $SAR\ ADC$ array. The integrator output load in this case increases from about 200 fF to the $SAR\ ADC$ array capacitance.
A reasonable solution to avoid oscillation is to decouple the $SAR\ ADC$ capacitance from the output of the integrator with a resistor. This introduces a zero in the transfer function, preserving stability.

3.3 Anti-Aliasing Filter

The input signal is sampled at frequency F_c by the ADC. In this application input signal frequencies of interest are around DC (acceleration signal detected by the MEMS accelerometer). However, noise coming from the accelerometer channel (in particular from the $C2V$ amplifier) at F_c will fold to DC because of aliasing.
In order to attenuate this effect an anti-alias filter is needed. In this design an active RC filter is used. The specifications require its cut-off frequency to be chosen a decade before F_c.
The RC time constant has then to be chosen accordingly. Digital trimming is required to compensate for process variations. A two stage OTA is required for the filter (given the output swing requirement) with high DC gain to avoid distortion in the incoming signal. The same OTA structure used in the incremental ADC integrator is chosen. The chopping technique is again used to cancel offset.

3.4 Voltage References

Figure 3.7 shows the schematic of the single ended voltage reference generator. It is a two stage OTA compensated with the same approach used for the incremental ADC integrator. Its tail current is 3 μA. The output voltage is set to 1.3 V by a feedback resistive divider, starting from the 1.2-V bandgap voltage.

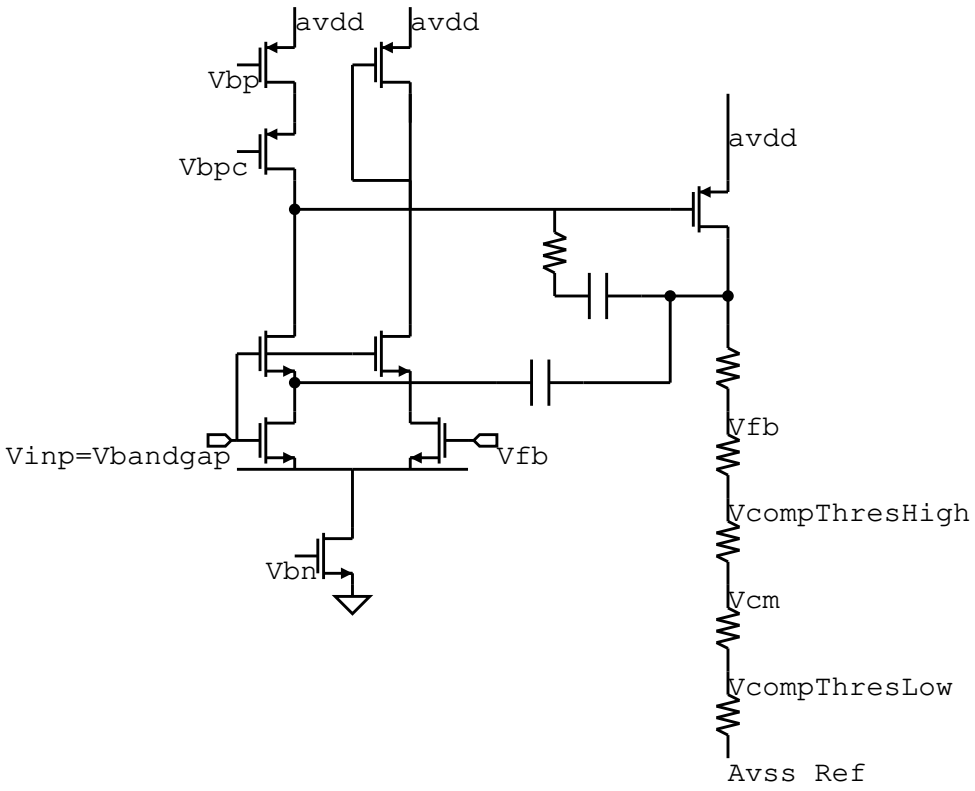

Figure 3.7: Voltage reference generator

From the resistive divider in Figure 3.7 the comparator thresholds are also obtained. In order to allow proper operation of the reference generator, the NMOS cascode transistors of the first stage are connected to the input signal (bandgap voltage). As stated in Chapter 2 the same reference voltage has to be used for incremental and $SAR\ ADCs$ [4].

[4]avss is used as the negative reference voltage.

3.5 Comparators

Two strobed comparators are needed for the incremental ADC[5] and one comparator is needed for $SAR\ ADC$ operation. The structure designed is similar in both cases, the only difference being that during incremental conversion the two comparators need to perform a comparison between two thresholds which are 450 mV and 850 mV, while in the SAR conversion, the threshold is zero.

Pre amplification (with gain in the order of ten)is used to reduce the input referred offset and the kickback of purely dynamical comparators (Figure 3.8). Gain stages are realized with a PMOS input pair and diode connected NMOS devices[6], while the dynamic latch is realized with two cross coupled inverters.

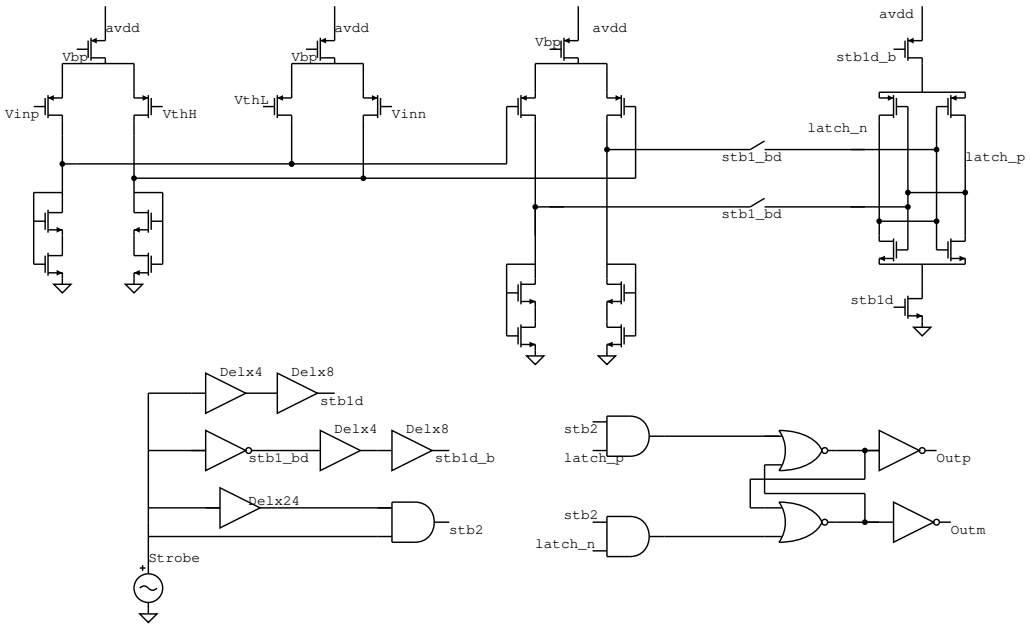

Figure 3.8: Comparator

Simulations have to be performed to verify the offset and the behavior of the comparators in incremental mode when the input signal is near the thresholds. The offset can be evaluated with a slow input ramp during MonteCarlo

[5]A three level quantizer is used.

[6]This gain structure allows fast response while the gain is in the order of ten for a single amplification stage.

simulations. The comparator output should flip exactly when the input exceeds one of the thresholds. Transistor mismatch causes an equivalent shift of the thresholds. The difference between the ideal flip point and the actual one is the offset of the comparator. In incremental operation the simulated offset is 5 mV. This value does not affect the incremental conversion accuracy since comparators are in a favorable position in the incremental loop. In *SAR ADC* operation the pre-amplification current needs to be increased a little bit in order to reduce the input referred offset. The *SAR ADC* comparator offset in fact introduce an offset in the whole conversion[7].

The comparator current consumption is of the order of 2 μA. When the input signal (output of the integrator) is near thresholds, the pre-amplification stages work in a balanced condition. They have to amplify the small difference between input and threshold voltages and provide it to the latch with fast settling. Figure 3.9 shows the simulation results when the input of the comparator goes from full scale positive to 1 mV below threshold. This is the most critical situation. When the output of the integrator is far away from thresholds, the pre amplifier is unbalanced and behaves in a non-linear fashion. The output provided to the latch does not settle, but the decision is anyway correct due to the large displacement between the inputs.

3.6 SAR ADC

Ideal conversion from the *SAR ADC* can be simulated using ideal capacitors. An example of the conversion is shown in Figure 3.10, where the evolution of the inputs of the comparator and timing are represented. As a sanity check, the algorithm converges at less than one *LSB* at the last comparison.

The *SAR ADC* samples the input signal on the *DAC* capacitors. Then sign detection is performed. After that, 10 comparisons take place to resolve 11 bits (10 comparisons plus sign detection).
The comparator has the same structure of Figure 3.8, with only one input differential pair in the pre-amplification stage to perform the comparison

[7] *SAR ADC* comparator offset has to be anyway divided by the interstage gain ($G\,OSR$) to evaluate its effect at the input of the whole *ADC*.

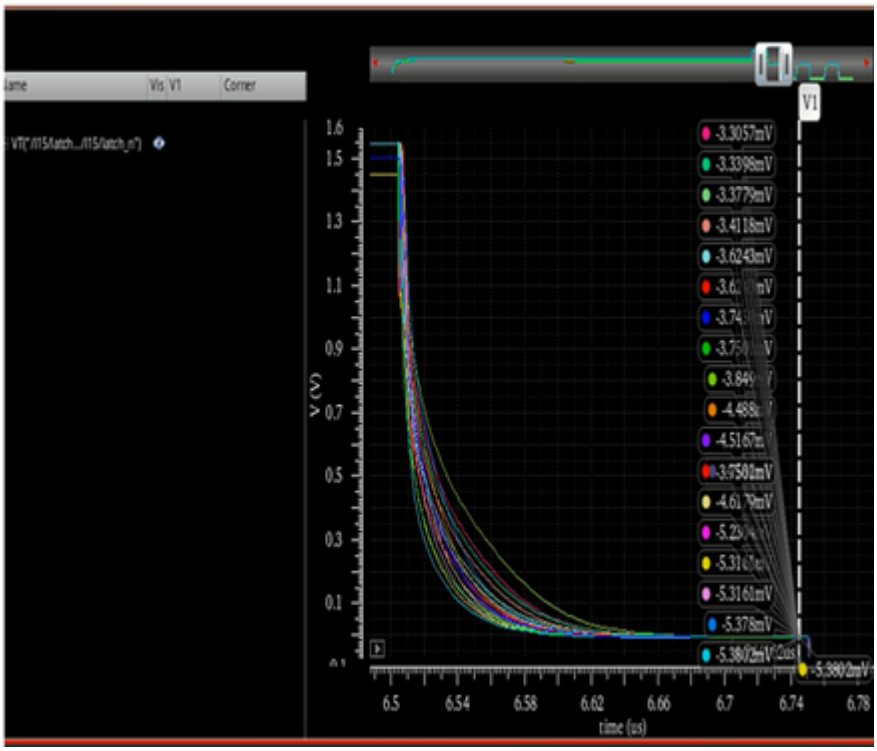

Figure 3.9: Comparator latch input settling near threshold

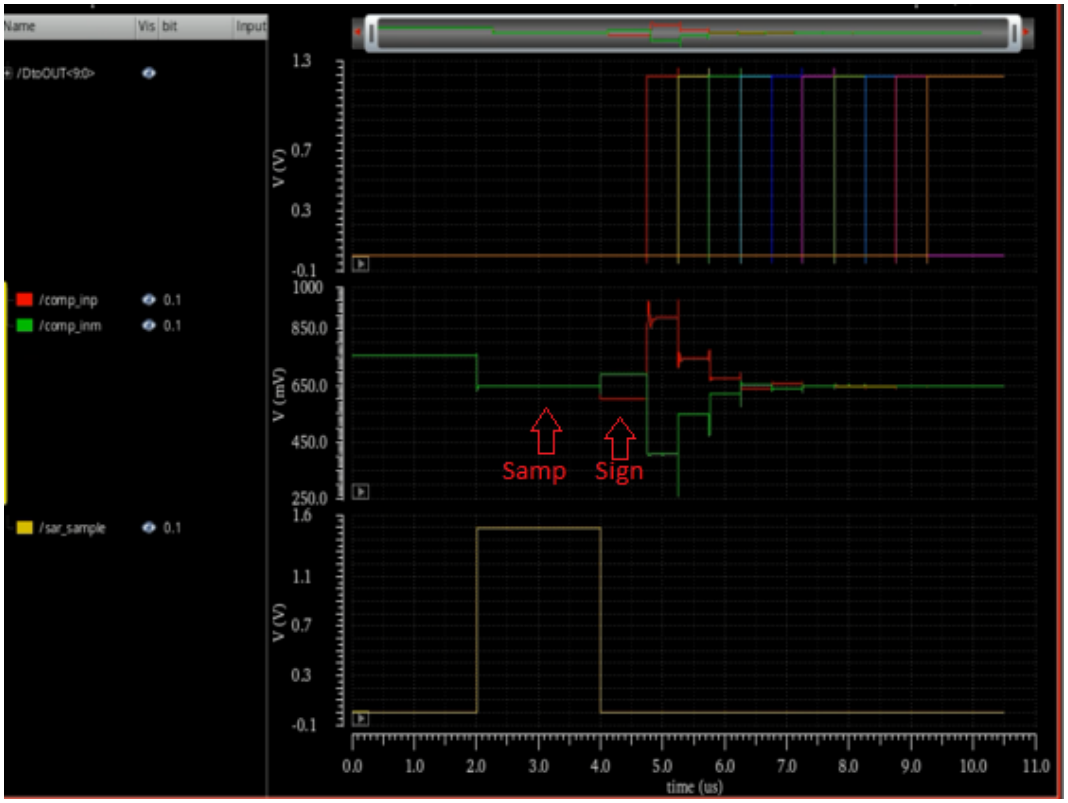

Figure 3.10: SAR ADC conversion and timing

between its inputs. Linearity of the stand alone *SAR* conversion is shown in Figure 3.11.

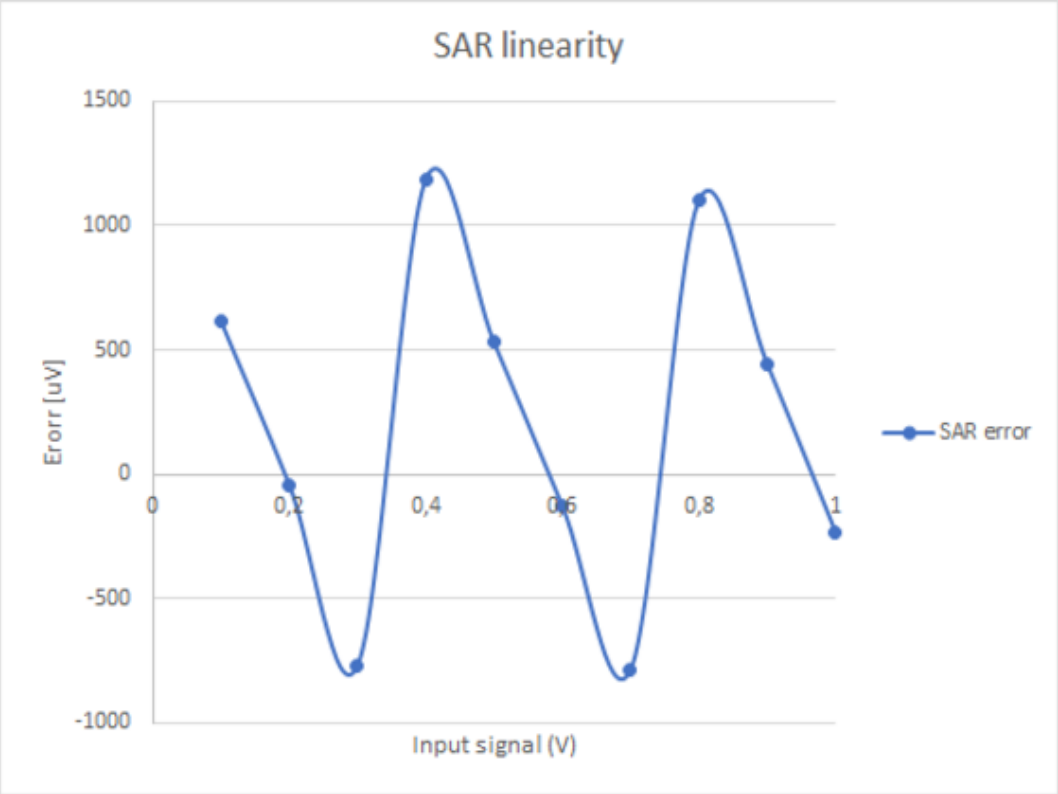

Figure 3.11: SAR ADC linearity

The most critical issue in the *SAR ADC* design lies in the layout of the array. As stated in Chapter 2 the major concern deals with large capacitors in the array. An interesting layout structure is presented in [24] and will be used for this design. The layout floorplan for a single array is shown in Figure 3.12. In Figure 3.12 every square represents a unit capacitor. The largest capacitance (*MSB* capacitance: 512 unit capacitors) is identified with number 1, the smallest (unit capacitor) is identified with the number 10. Dummies (D) are added to reduce border effects. The symmetrical structure allows to reduce the effect of possible gradients in the layout.

In order to carefully simulate the effect of the layout of the capacitors, the developed Matlab model can be used. The capacitance values extracted from the layout (Table 3.1) can be added to the Matlab model in order to evaluate

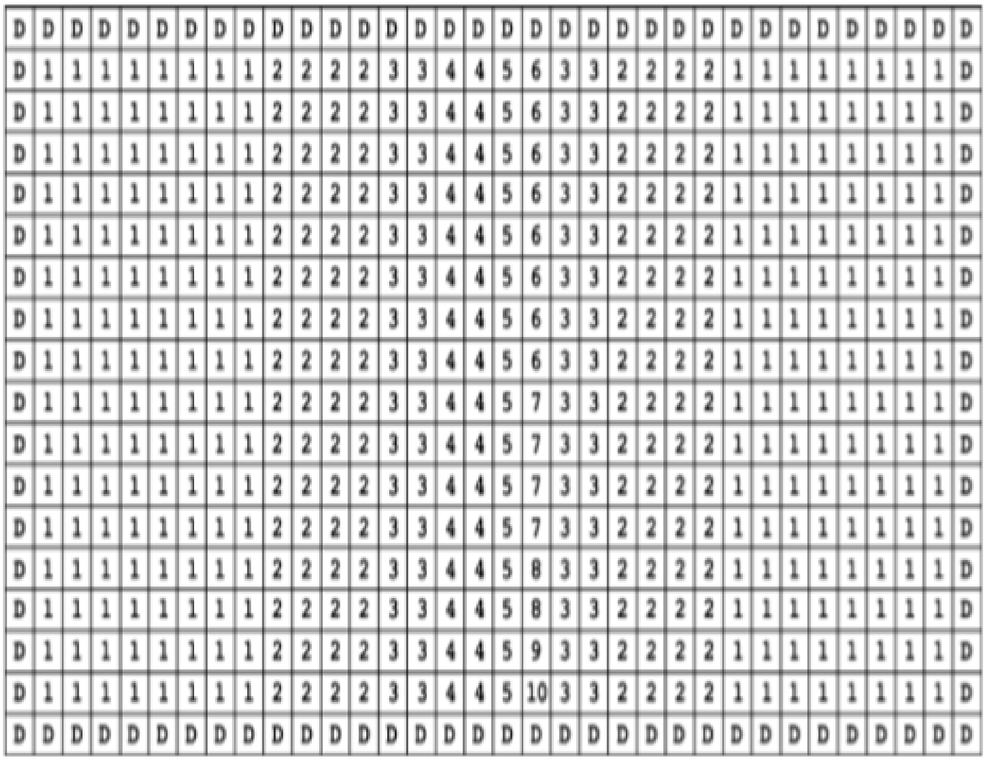

Figure 3.12: SAR ADC layout floorplan

the effect on linearity of the whole *ADC*.

Table 3.1: Layout extracted capacitance

	Nominal	*Error*[%]	*Extracted*
Cap1	512	4.316	534.1
Cap2	256	4.317	267.05
Cap3	128	4.247	133.44
Cap4	64	4.199	66.68
Cap5	32	4.167	33.33
Cap6	16	4.374	16.70
Cap7	8	4.6	8.36
Cap8	4	4.925	4.2
Cap9	2	5.791	2.12
Cap10	1	7.193	1.07

The average error (in the order of 4 %) with respect to the nominal value (due to the capacitance of the interconnections for instance) is irrelevant. It can be considered as if the unit capacitor were 4 % larger. As expected, the value of the smaller capacitors deviates from the average. This is due to the matching error. Only bigger capacitors benefits from the symmetry of the structure.
Differential and integral non linearity are evaluated with the Matlab model with a fine input ramp ($\frac{LSB}{8}$ steps are performed), as shown in Figure 3.13 and Figure 3.14.

3.7 Overall Linearity

The *ADC* overall linearity can be simulated with Spectre at 27° C (transient simulation). Results are shown in Figure 3.15. The integral non linearity is between ±1 LSB.

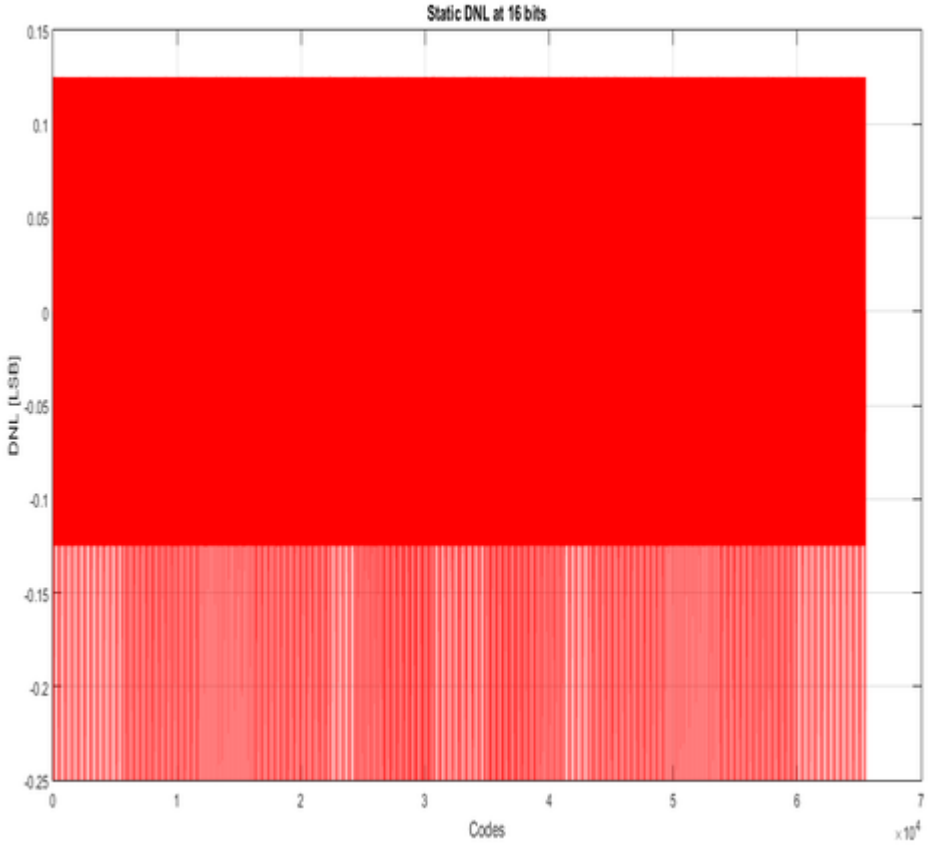

Figure 3.13: SAR ADC DNL error due to layout of the capacitors

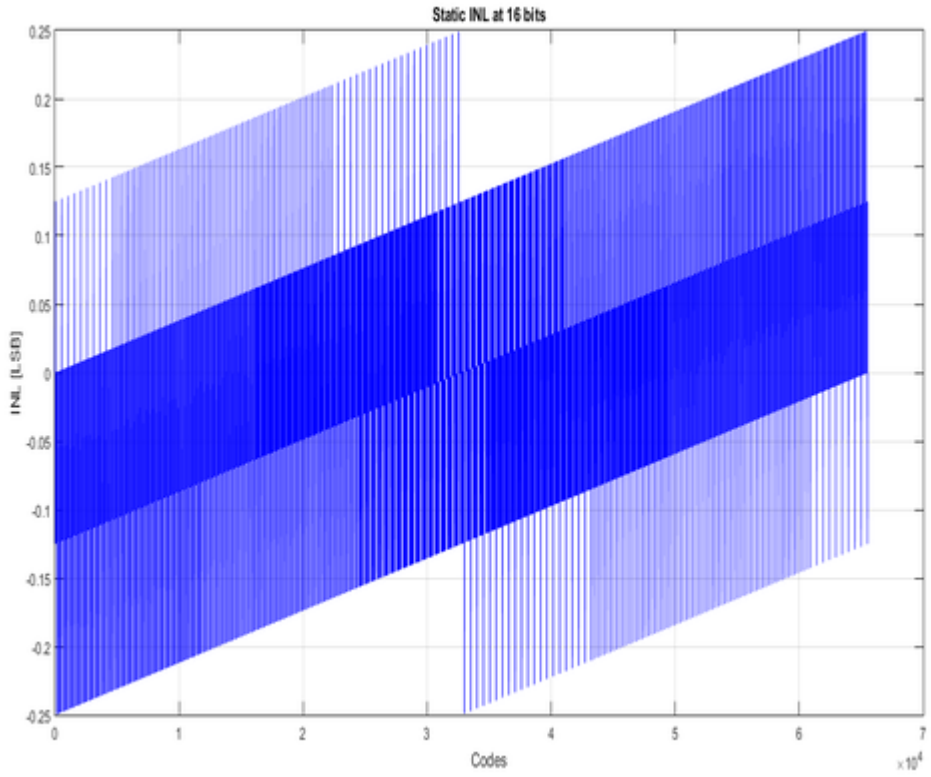

Figure 3.14: SAR ADC INL error due to layout of the capacitors

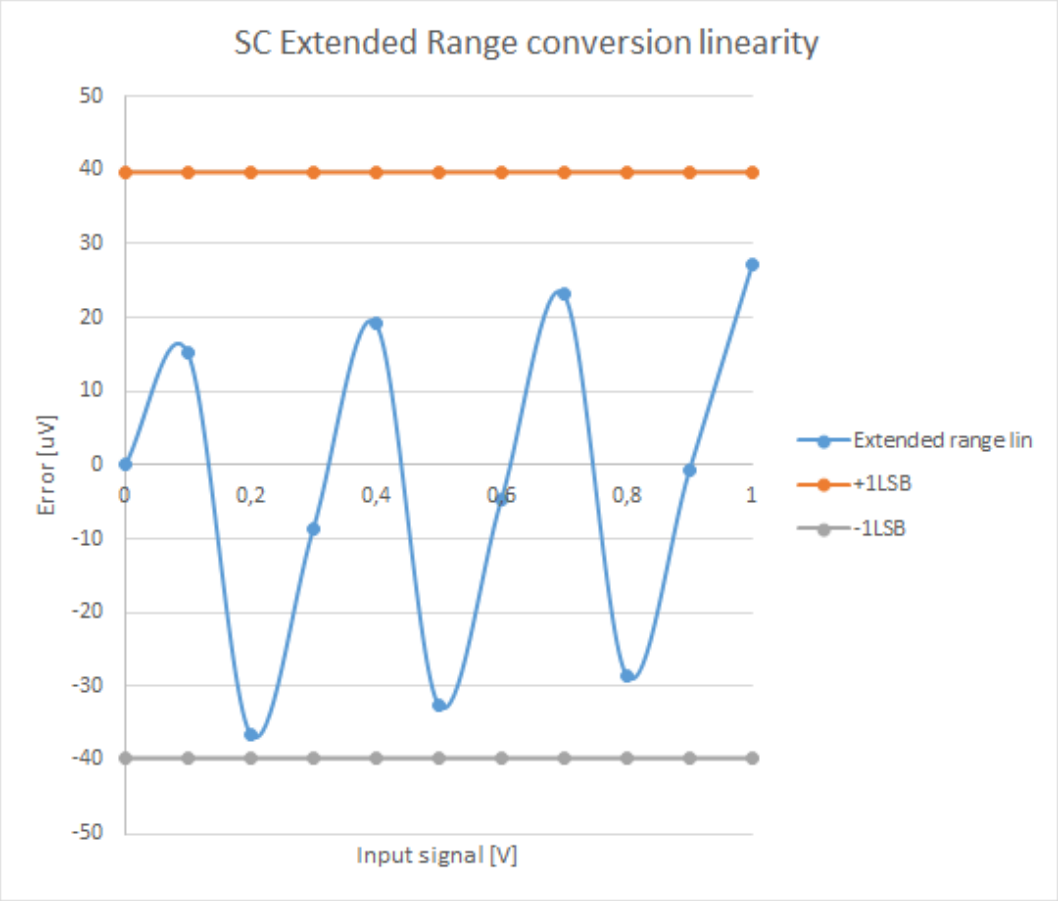

Figure 3.15: Extended-range ADC overall linearity

3.8 Noise Analysis

3.8.1 Noise of the Analog Blocks

A theoretical noise analysis was performed in Chapter 2. Preliminary results were achieved with reasonable approximations. Transistor level simulations are required for achieving more accurate results.
Guidelines for noise simulations in sigma-delta modulators are given in [25]. The testbench used for noise simulations of the integrator used in the incremental *ADC* is shown in Figure 3.16. It consists of the integrator followed by an **ideal S/H** which samples the noise process every clock cycle (T_c) and holds it for a whole period [26].

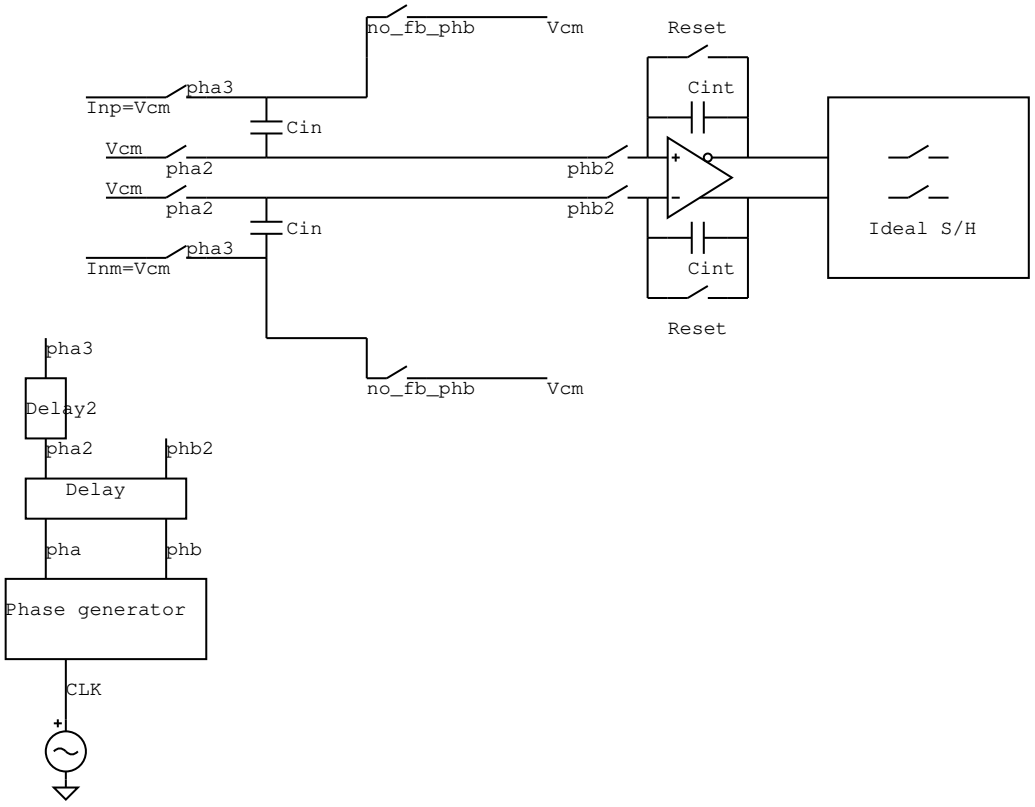

Figure 3.16: Test bench used for the noise simulation of the integrator used in the incremental ADC

This testbench reproduces the way the *ADC* works. Every clock cycle

the output of the integrator is sampled. This means that noise process itself is sampled. The PSD at the output of the ideal S/H has to be evaluated till $\frac{F_c}{2}$. This spectrum is anyway multiplied by a sinc function due to the zero-order hold operation introduced by the S/H. It is also possible to instruct the simulator to provide the input referred noise. The integrator noise PSD referred to the input of the ADC was obtained with a PSS (periodic steady state) analysis and $PNOISE$ (periodic noise) analysis. Results are shown in Figure 3.17, where both thermal noise and integrator noise are simulated.

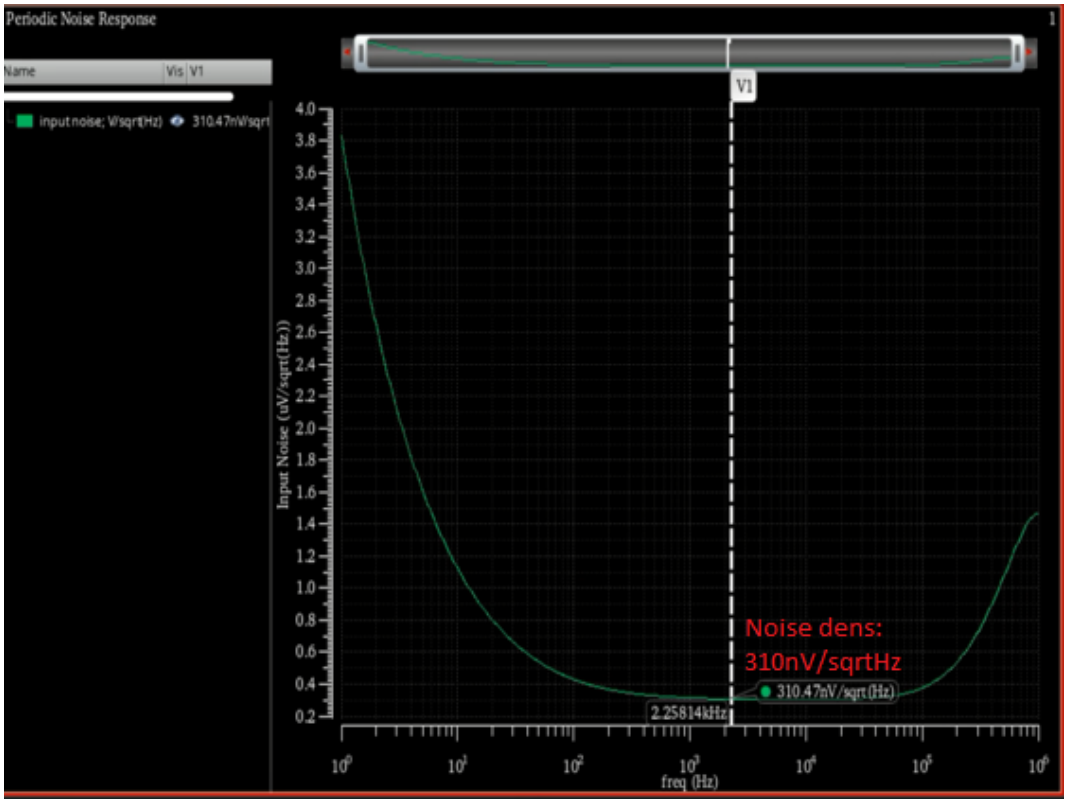

Figure 3.17: Simulated integrator noise ($PNOISE$ analysis)

Recalling that flicker noise will be canceled by chopping operation, white noise is, as expected, dominated by thermal noise ($\frac{kT}{C}$). In the $PNOISE$ analysis 50 sidebands[8] were used, so that noise folding is considered until a

[8]The maxsideband parameter is used by the simulator to define the upper limit of frequency folding.

decade after GBW[9]. This gives more accurate results with respect to hand calculations. In a similar way, the reference voltage generator and the anti-aliasing filter noise contributions can be estimated. Also their PSD need to take folding into account. Their output noise PSD is injected at the input of the ADC.
The anti-aliasing filter noise is highly dominated by the thermal noise of its input and feedback resistors. Its noise (folded) is indeed quite relevant to the overall conversion.
Similarly noise contribution from the reference buffer has an impact on the conversion. It is important anyway to remember here that the use of a three-level quantizer will attenuate the reference noise contribution for low signals.
While for the integrator and the anti-aliasing filter noise the chopping operation will result in a white noise spectrum, flicker noise of the reference voltages has to be taken into account with a more precise model[10]. The colored noise model in [27] can be used for the reference voltage generator. Overall noise simulation results will be presented in Section 3.8.2.

The $SAR\ ADC$ noise contribution comes from the reference voltage and the input referred noise of the comparator.
It is here useful to remember that the conversion (and its noise) from the $SAR\ ADC$, when referred to the input of the converter, has to be divided by the interstage gain ($OSR\ G$) . As an example, the reference voltage noise can be evaluated as the rms noise obtained integrating the PSD of the reference voltage generator when it works in SAR mode (Figure 3.18). The integrated noise value obtained is 400 μV_{rms}. This value can be added to the Matlab model on the residue of the integrator. It means that it should be quadratically summed to the noise of the incremental conversion in the same position. The noise from the $SAR\ ADC$ turns out to be substantially negligible with respect to the noise of the incremental ADC[11].

[9]Since the sampling frequency is 2 MHz, noise folding is considered until 100 MHz.
[10]For a SC implementation noise folding anyway whitens the noise.
[11]The rms voltage noise from the anti-alias filter in the same position is five times larger for instance.

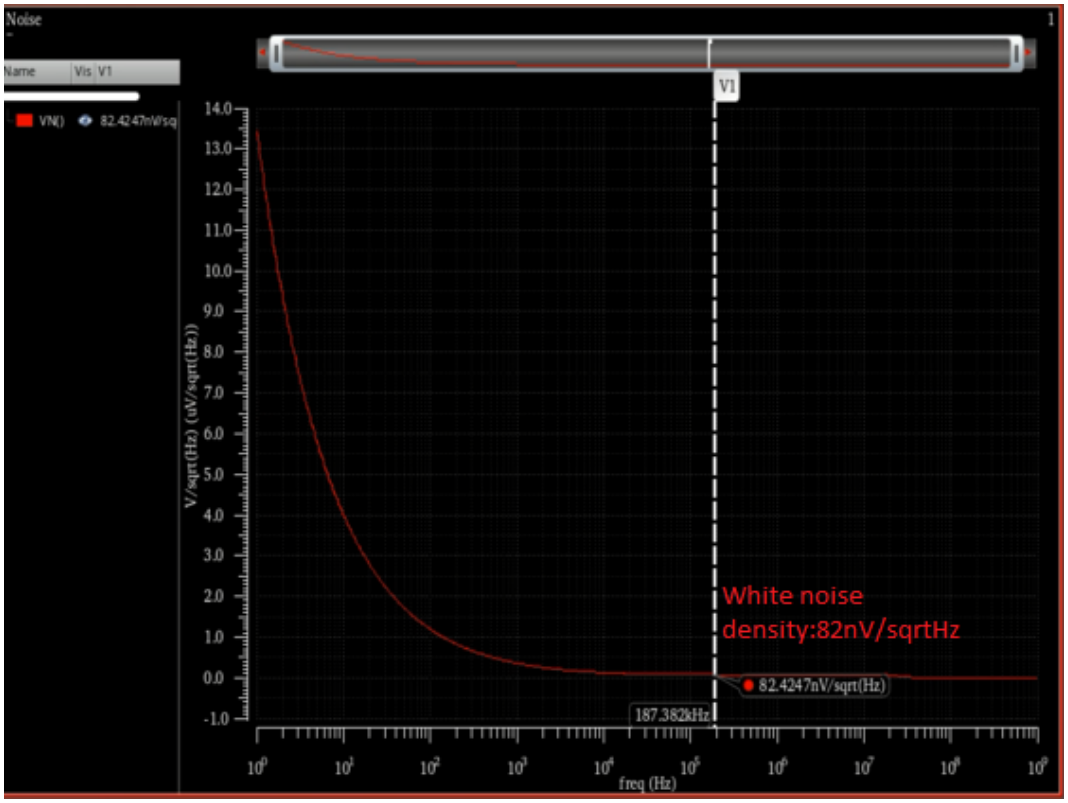

Figure 3.18: Simulated reference voltage noise in SAR mode

3.8.2 Overall Noise Simulated with the Matlab Model

The noise $PSDs$ obtained with SpectreRF can be introduced into the Matlab model for behavioral simulations of the complete ADC. To correctly evaluate their contributions, all the noise $PSDs$ in the incremental are referred to the input of the ADC.
The transfer function from the input of the converter to the output of the integrator after OSR cycles can be written as

$$H(f) = \frac{1 - e^{-2i\pi fOSRT_c}}{1 - e^{-2i\pi fT_c}} \tag{3.8}$$

Anti-alias filter, reference buffer and integrator $PSDs$, shaped by (3.8), can be added to the residue of the incremental conversion (output of the integrator)[12], along with noise contribution from the reference voltage of the $SAR\ ADC$. Also the input referred noise of the $SAR\ ADC$ comparator can be added[13]. The results are shown in Figure 3.19.

3.9 Conclusions

The transistor level design of the single analog blocks was analyzed in detail following the guidelines provided by the Matlab model. Simulation results, obtained with a transistor-level simulator, were presented. Linearity and noise analyses were performed on the different analog blocks. A summary of the achieved results is shown in Table 3.2

These blocks have been integrated in a test chip along with some standard digital circuitry to perform conversions. The digital blocks are the counter required for incremental conversion and the SAR register.
For the test chip, supplies will be externally provided and the reconstruction of the overall extended range signal (combination of incremental and $SAR\ ADC$ outputs) are performed externally from the raw data taken from two different

[12]It is important to underline that these $PSDs$, before being added to the Matlab model, need to be compensated for the effect of the zero-order hold used in simulation.

[13]Also in this case, noise contribution from the $SAR\ ADC$ comparator is negligible with respect to the other noise sources.

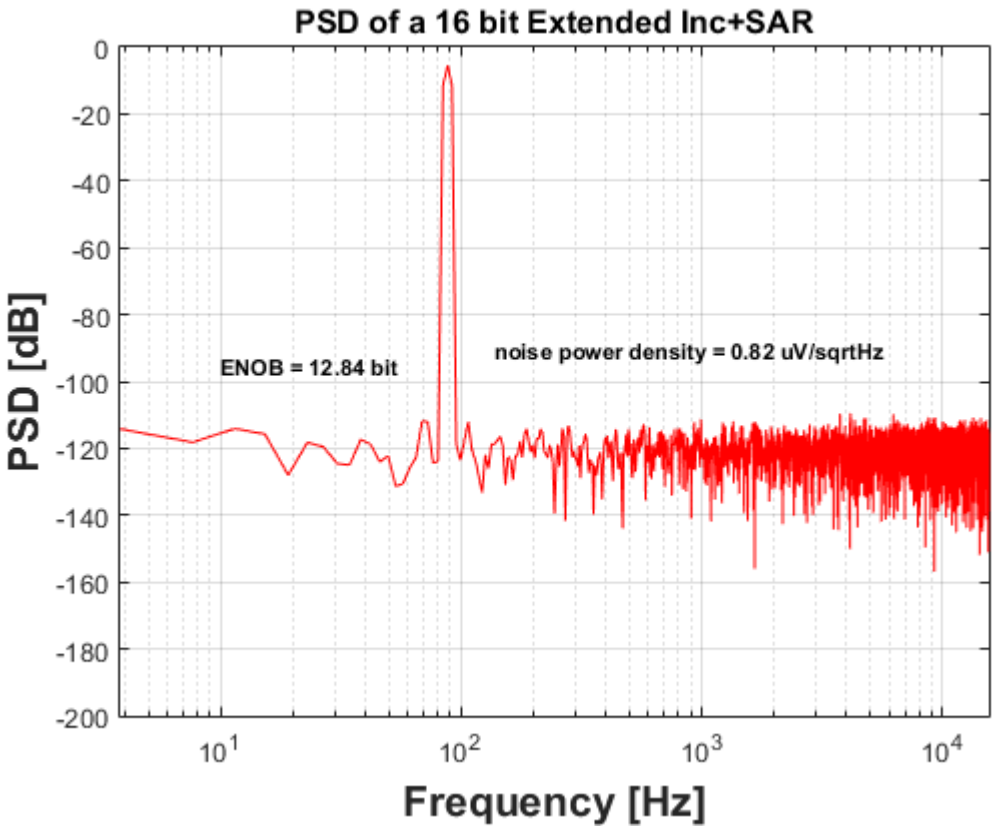

Figure 3.19: Overall ADC noise PSD and ENOB (noise from simulated analog SC blocks)

Table 3.2: Simulation results for the SC extended-range ADC

Parameter	*Simulation*	*Specification*	*Dominant Contributors*
Current Consumption	60 μA	<100 μA	Int, AAF and Ref
Area	<0.1 mm^2	<0.1 mm^2	SAR Caps, CMFB and AAF Res
Linearity-INL	$\pm$1 LSB (typ)	< 0.2%	Settling and slew of the Int
Linearity-DNL	$\pm$0.25 LSB (typ)	$\pm$1 LSB at 16 bits	Mismatch SAR caps
Resolution (ENOB)	12.8 bits	12 bits	Int and AAF
Signal Range	1.3 V	1 V	–
Signal Bandwidth Single Channel	15 kHz	15 kHz	–

registers[14].

[14]Reconstruction of the signal is realized by software (Matlab).

Chapter 4

Continuous Time Incremental ADC Design

This chapter will explore an attractive alternative for the design of the extended-range *ADC*: a continuous-time implementation of the incremental *ADC*. Advantages and disadvantages of the continuous-time (CT) solution with respect to the switched-capacitor discrete-time (DT) implementation will be analyzed. Simulation results will be presented.

4.1 Advantages of CT vs DT Implementation

4.1.1 Inherent Anti-Aliasing Filtering

In Chapter 3 the need for an anti-aliasing filter was discussed. A CT implementation of the incremental *ADC* offers inherent anti-aliasing effect. Accurate calculations can be found in [14].

For a first-order incremental *ADC* the CT system is equivalent to its DT counterpart preceded by a sinc filter with sampling period T_c, due to the CT integrator action. The input signal is convolved in the time domain with a rectangle (Figure 4.1). This means that folding from F_c and its multiples into the baseband will be highly attenuated.

Figure 4.2 shows the behavior of the sinc function squared. This function multiplies in the frequency domain the incoming signal power (and noise power)

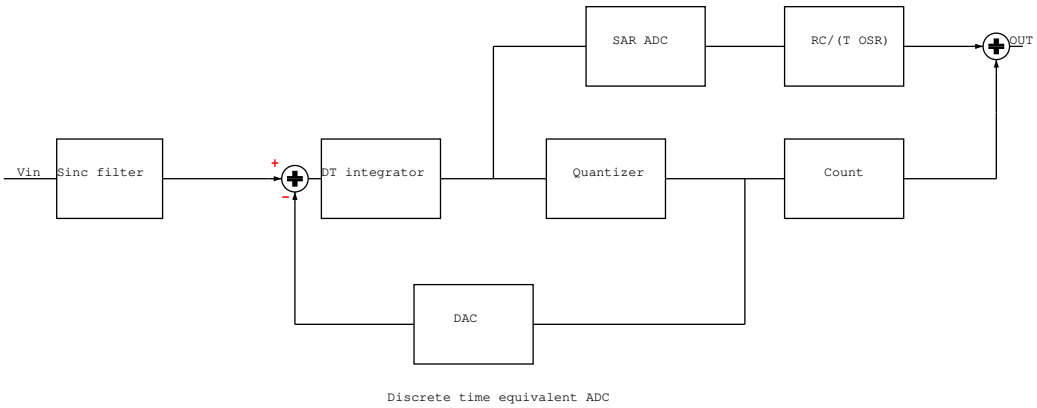

Figure 4.1: Continuous-time incremental *ADC*

components present at the input of the *ADC*. It is interesting to evaluate the attenuation of noise folding from the first sideband (2 MHz) into the baseband (15 kHz), assuming a unitary power signal (Figure 4.3). Noise power and spurs coming from the accelerometer channel at 2 MHz will be multiplied by the zero of the sinc transfer function. In the baseband, the maximum power attenuation has a much higher value than the attenuation achieved with the first order *RC* filter discussed in Chapter 3.

This filtering action leads another advantage of the CT implementation. Indeed, since the sampling operation of the converter happens after the integrator, device noise folding is also highly attenuated. A very small amount of noise is folded into the converter baseband. This means that noise specification can be achieved with much less currents in the integrator. Moreover, the anti-aliasing filter can be removed, allowing further reduction of the power consumption.

4.1.2 Relaxation of Integrator Requirements

The other main advantage of the CT solution is the relaxation of the integrator requirements. The response of the integrator to a step signal is a ramp. This means that the maximum slope that the integrator has to provide is limited by the value of the reference and the equivalent gain of the

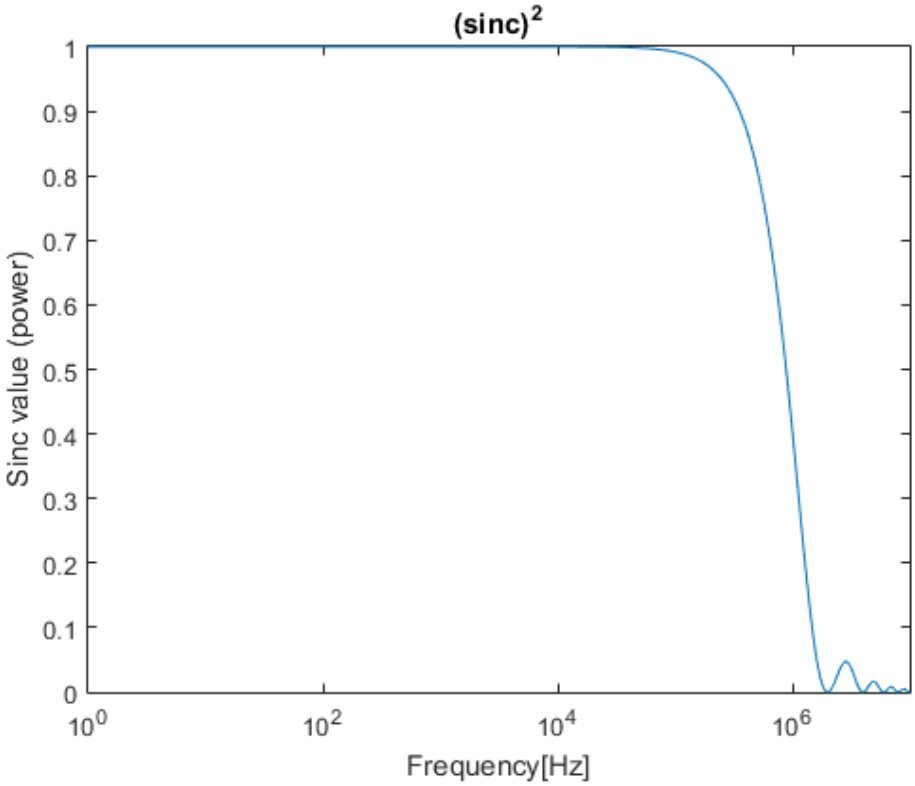

Figure 4.2: Squared sinc function

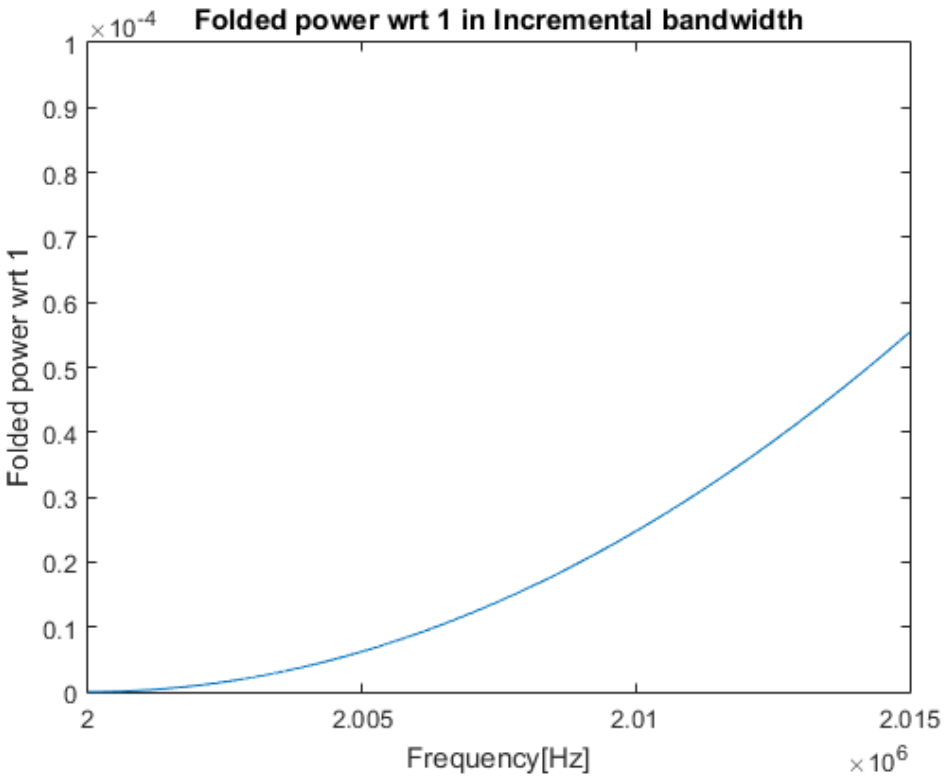

Figure 4.3: Folded power in the baseband

converter[1]. For this application the reference voltage is 1.3 V. This means that the integrator should in the worst case provide 650 mV (equivalent gain of 0.5) in 500 ns or, equivalently, 1.3 $\frac{\mathrm{V}}{\mu\mathrm{s}}$. It is useful to recall here that the slew-rate requirement for the DT solution was of the order of 10 $\frac{\mathrm{V}}{\mu\mathrm{s}}$. Moreover, the GBW can be theoretically lower because fast settling is not required.

4.2 Disadvantages of CT vs DT Implentation

4.2.1 Temperature-Dependent Interstage Gain

For a DC signal, equation (2.2) can be rewritten for a CT incremental ADC as

$$V_{in} = \frac{N}{OSR} V_{ref} + \frac{V \cdot R \cdot C}{OSR \cdot T} \tag{4.1}$$

where

- T is the clock period
- R is the value of the input resistor of the RC integrator
- C is the feedback capacitor of RC the integrator

The reconstruction of the signal now consists of the sum of the incremental conversion result which is substantially temperature independent (within reasonable limits) and the conversion of the residue from $SAR\ ADC$, which is temperature dependent mainly due to the temperature dependence of resistor R, whose value changes about 10% over the considered temperature range. This means that the residue (output of the integrator after OSR cycles) changes accordingly.
This creates a sharp non-linearity every time a bit from incremental is added to the conversion. In the DT solution, the equivalent of $\frac{T}{RC}$ was $\frac{C_{in}}{C_{int}}$, i. e. a capacitance ratio, which is basically temperature independent. A solution to this problem will be presented in Section 4.3.

[1]The equivalent gain of the converter is $\frac{T}{RC}$ where T is the clock period and RC is the integrator time constant.

4.2.2 Virtual Ground Displacement

In a DT *SC* implementation only the voltages achieved at the end of the clock period are important. The integrator should settle within a certain limit at $t = nT_c$. Philosophically it can be stated that whatever happens during the clock period is somehow irrelevant. In a CT solution the situation is different. **The evolution of the signals during the clock period** totally matters. If the virtual ground of the integrator (V_M) shifts at some point during the clock period, for example, this means that the value integrated for a certain slot of time is $V_{in} - V_M$ instead of V_{in}, thus producing an error in the conversion.
It was previously mentioned that requirements on the integrator can be relaxed. This is true for the incremental *ADC* standalone, but actually it is not completely for the extended range conversion[2]. Indeed, suppose that GBW of the integrator is chosen as $2F_c$ (4 MHz). The time evolution of the RC integrator with one pole ($A(s) = \frac{A_0}{1+s\tau}$) can be obtained writing KCL at the virtual ground node (V_M) (Figure 4.4).

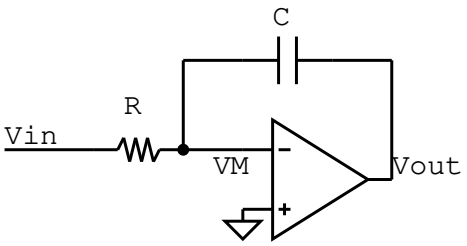

Figure 4.4: Simple integrator model used to calculate the transfer functions

Two relevant transfer functions can be obtained:

$$\frac{V_{out}}{V_{in}} = \frac{\frac{-GBW}{CR}}{s^2 + s(GBW + \frac{kR}{C} + \frac{GBW}{A_0}) + k\frac{GBW}{CRA_0}} \tag{4.2}$$

$$\frac{V_M}{V_{in}} = \frac{1 + s\frac{A_0}{GBW}}{s^2 + s(GBW + \frac{kR}{C} + \frac{GBW}{A_0}) + k\frac{GBW}{CRA_0}} \tag{4.3}$$

where

[2]It is also known that in CT sigma-delta modulators the GBW can be as low as twice the sampling frequency.

- R represents the input resistor
- C is the feedback capacitor
- A_0 is the integrator finite DC gain
- k is the number of resistive input branches ($k = 2$ when feedback is applied)

While (4.2) reveals that the output of the integrator for a step input signal is a delayed ramp with delay determined by the GBW value, it is interesting to evaluate the time response of the virtual ground.
Writing the denominator of (4.2) or (4.3) as $s^2 + s(GBW + \frac{kR}{C} + \frac{GBW}{A_0}) + k\frac{GBW}{CRA_0} = (s+a)(s+b)$, the inverse-Laplace transform for a step input gives

$$V_M(t) = V_{in}\frac{GBW}{RCA_0}\int_0^t \alpha_1 e^{-at} + \alpha_2 e^{-bt} dt \tag{4.4}$$

where

- $\alpha_1 = \frac{1-a\frac{A_0}{GBW}}{b-a}$
- $\alpha_2 = \frac{1-b\frac{A_0}{GBW}}{a-b}$

For $A_0 > 100$ the position of the pole near the origin in the denominator of (4.3) is only determined by the value of the DC gain. For DC gain going to infinity the pole goes to the origin. The position of the high frequency pole is determined by the value of GBW. For GBW going to infinity the pole goes to infinity.

If A_0 is large, the pole due to GBW shapes the virtual ground time response. The virtual ground settles to a value directly proportional to the input signal and dependent on GBW and $\frac{1}{RC}$, following an exponential behavior. This displacement of the virtual ground is of the order of tens of mV if GBW is 4 MHz and RC is 1 μs. The error introduced in the conversion can be calibrated following the procedure explained in Section 4.3.

4.2.3 Jitter

The last disadvantage of the CT solution with respect to its DT counterpart is the contribution of clock jitter. Indeed, a jitter δ in the clock period introduces and equivalent noise in the conversion due to the fact that the reference voltage enters as feedback for a time slot $T_c \pm \delta$ instead of just T_c. The jitter contribution will be taken into account when the noise of the CT converter will be analyzed.

4.3 ADC Calibration

4.3.1 Calibration Procedure

As mentioned before, the CT *ADC* requires some kind of calibration. Apart from a coarse digital calibration of the *RC* integrator time constant to account for process variations, the dependence of the ratio $\frac{T}{RC}$ on temperature and the virtual ground displacement need to be taken into account. Here the solution proposed is to measure the two parameters using the *SAR ADC*, in order to correct them. Both the virtual ground displacement and the variation over temperature of the resistance can be modeled as a multiplying factor m of the interstage gain $\frac{T}{RC}$. This factor m can be determined by applying subsequently a $+V_{ref}$ pulse and a $-V_{ref}$ pulse at the integrator input and converting in the digital domain the two resulting voltages at the integrator output with the *SAR ADC*. This leads to the following two equations:

$$\begin{cases} V_{ref}\frac{T}{RC}m + V_{os}\frac{T}{RC}m = SAR_1 \\ -V_{ref}\frac{T}{RC}m + V_{os}\frac{T}{RC}m = SAR_2 \end{cases} \tag{4.5}$$

where V_{os} is the offset of the integrator and SAR_1 and SAR_2 are the results of the two *SAR ADC* conversions, respectively.
Subtracting the two equations we obtain:

$$m = \frac{SAR_1 - SAR_2}{2V_{ref}\frac{T}{RC}}$$

This means that with the two values converted by the *SAR ADC*, a measure

of the variation of R with temperature and of the virtual ground displacement is obtained in the digital domain. The obtained factor m can then be used when combining the incremental and $SAR\ ADC$ conversions to achieve the correct value in the overall result.

4.3.2 Linear System Hypotesis

The calibration procedure presented in the previous section assumes that the system is linear. The virtual ground displacement that can be calculated from (4.4) comes indeed from an inverse-Laplace transform operation, which is a valid under the hypothesis of linearity of the system. From (4.4), the virtual ground displacement at time T_c with $GBW = 4$ MHz and $RC = 1$ μs for an input signal equal to 1.3 V is of the order of 50 mV. The small signal model validity of the MOS transistors (on which the linearity hypothesis is based), actually, does not hold any longer, since the operating point (the common mode voltage) is disturbed too much. Even doubling the value of GBW is not a good solution, both because the power consumption will increase and also because over temperature and process corners the GBW will decrease anyway, producing the same effect. A solution to this problem will be proposed in the next section.

4.4 Incremental ADC Integrator

The CT incremental ADC scheme is presented in Figure 4.5. The value chosen for the input and DAC resistors is 2 MΩ. It follows that the feedback capacitors are 500 fF[3]. While for Reference generation and comparators[4] the solutions discussed in Chapter 3 can be used, a different design needs to be realized for the integrator to reduce the virtual ground displacement. Figure 4.6 shows the structure of a Miller-compensated two-stage OTA that works as an integrator. It is possible to analyze the reasons of the virtual ground

[3]The RC time constant is 1 μs. With a 2 MHz clock, the previously defined equivalent gain is 0.5, as in the DT implementation, where $\frac{C_{in}}{C_{int}}$ was 0.5.

[4]Also the $SAR\ ADC$ structure is supposed to remain the same.

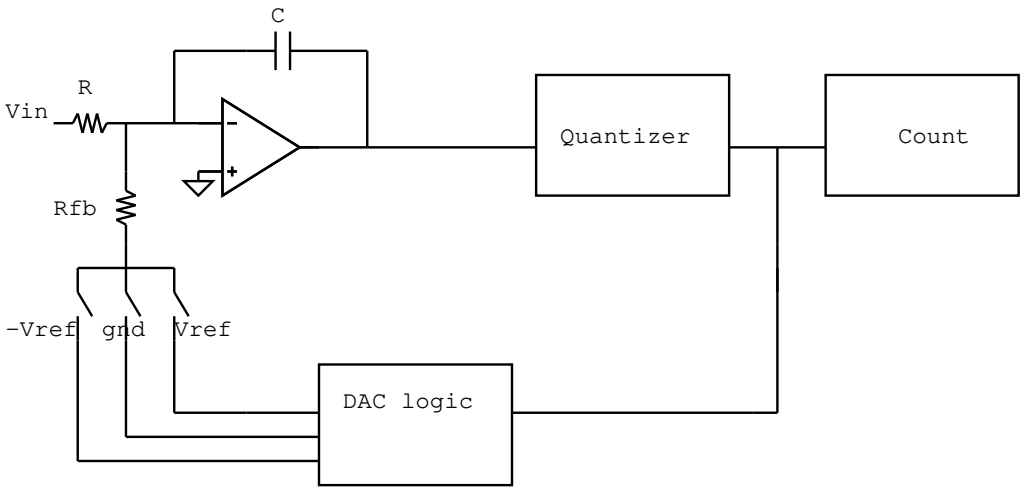

Figure 4.5: CT incremental *ADC* scheme

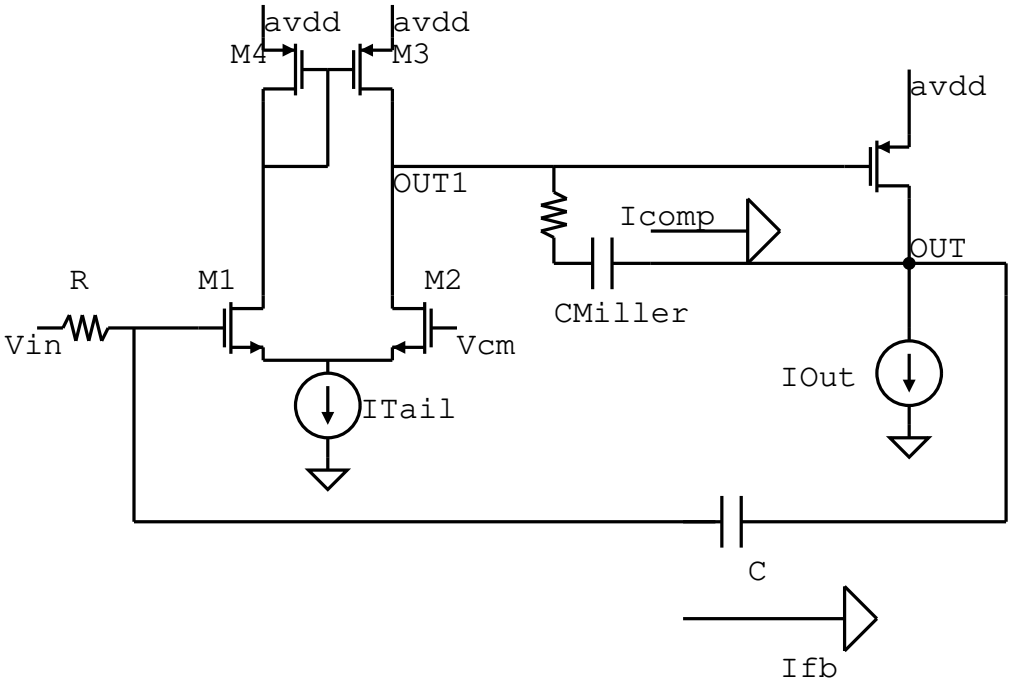

Figure 4.6: Structure of the Miller-compensated *OTA*

displacement.

If the input rises the output of the OTA (OUT) falls. This means that current I_{fb} flows as indicated in Figure 4.6.

Since the output of the first stage of the OTA ($OUT1$) rises, a current has to flow from the first stage to the second stage through the compensation path. This current must be provided by $M3$. Transistors $M3$ and $M4$ provide substantially the same current. Therefore, the gate of $M1$ has to rise, in order to accept the increase of current of $M4$.

When the RC time constant is small the output ramp will fall with a steeper slope. The output of the first stage also needs to rise more. The current through the Miller capacitance has then to increase.

Following the previous analysis, the virtual ground displacement augments. From another point of view the Miller capacitance has to be smaller to reduce this effect or equivalently the GBW has to be larger.

The intuitive explanation is readily confirmed by calculations. Under the hypothesis of infinite DC gain and fixed a bias condition for the transistors, if a positive step ΔV_{in} is applied to the input of the integrator, $I_{comp} = -C_{Miller}\frac{dV_{out}}{dt}$[5] flows through the compensation path. This current is provided by $M3$. Transistor $M4$ provides the same current and the gate of $M1$ rises. It is then possible to write $I_{comp} = gm_1\Delta V$, where ΔV is the gate to source voltage variation of $M1$. Moreover,

$$gm_1\Delta V = -C_{Miller}\frac{dV_{out}}{dt}$$

Since

$$\frac{dV_{out}}{dt} = -\frac{\Delta V_{in}}{RC}$$

then

$$gm_1\Delta V = -C_{Miller}(-\frac{\Delta V_{in}}{RC})$$

and finally

$$\Delta V = C_{Miller}\frac{\Delta V_{in}}{RC\ gm_1}$$

[5]Here the reasonable assumption is that the output-stage voltage variation is much larger than the voltage variation of the output of the first stage.

It is now clear that the virtual ground displacement depends on the values of GBW and RC time constant, as well as on the value of the Miller compensation capacitance. Since RC is fixed by the clock period T_c and we do not want to increase GBW, then only solution is to remove the compensation path.
It is well known that a two-stage OTA without compensation can not be stable [20, 22]. However, in a continuous-time application a **feedforward compensated** OTA structure can be used for implementing the integrator. The idea is to introduce a left half-plane zero in the integrator loop-gain transfer function. The basic idea is shown in Figure 4.7, where the feedforward path is provided by gm_{ff}.

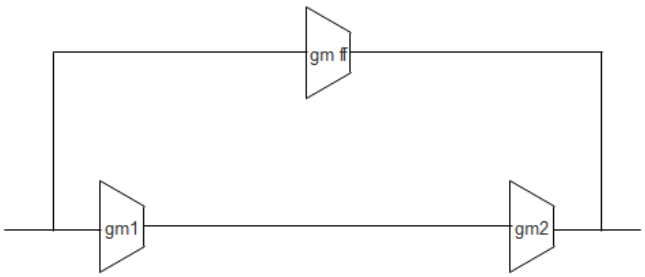

Figure 4.7: Principle of feedforward compensation

Pushing the zero at low frequencies to cancel one of the poles typically requires high power consumption [28]. A suitable alternative is to allow an initial 40 dB/decade slope of the loop gain and to use the zero to increase the phase margin near the GBW product.
It is important to underline here that the introduction of the zero in the transfer function lowers the speed of the closed-loop response. The GBW required is then higher[6]. The advantage of this structure is that it is easy to increase the GBW without consuming too much power.
The position of the two poles and of the zero can be found with the aid of Figure 4.8. A system of two KCL equations has to be solved:

[6]A feedforward compensated OTA is indeed not used for discrete time integrators in sigma-delta or incremental converters because of the presence of the zero.

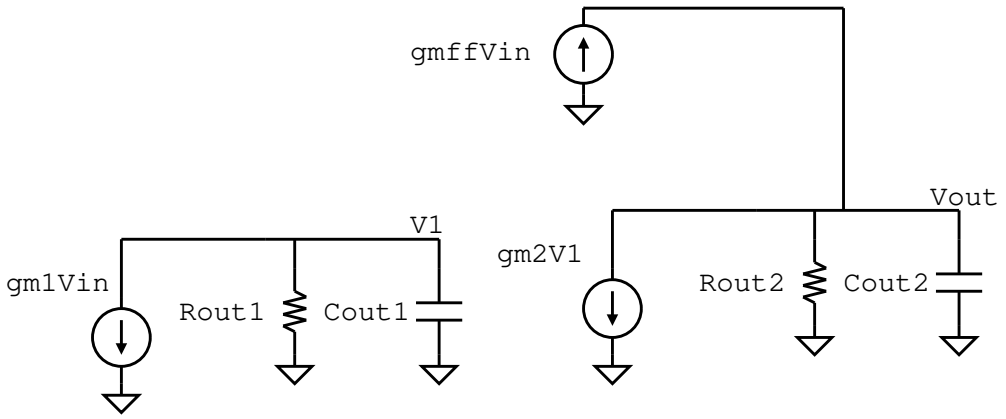

Figure 4.8: Small signal model for the feedforward OTA

$$\begin{cases} gm_1 V_{in} + \frac{V_1}{R_{out1}} + V_1 s C_{out1} = 0 \\ gm_2 V_1 + \frac{V_{out}}{R_{out2}} + V_{out} s C_{out2} - gm_{ff} V_{in} = 0 \end{cases} \tag{4.6}$$

from which one can obtain, after some slight approximations,

$$\frac{V_{out}}{V_{in}} = \frac{gm_2 gm_1 R_{out1} R_{out2} (1 + s\frac{gm_{ff} C_{out1}}{gm_2 gm_1})}{(1 + sC_{out1} R_{out1})(1 + sR_{out2} C_{out2})} \tag{4.7}$$

Equation (4.7) shows that the DC gain is the same as the gain of a conventional two-stage OTA. In case, it is possible to increase the DC gain with a folded-cascode first stage. Two poles are located in the same position as they were in the uncompensated OTA, while the zero position determines the phase margin. In order to have 60° at GBW, the position of the zero needs to be at $\frac{1}{2}GBW$.

The schematic of the OTA adopted in this design is represented in Figure 4.9. It is reasonable to choose a high GBW value which leaves some margin for temperature and process corners. With $GBW = 30$ MHz and C_{out2} fixed by the input capacitance of the comparators and the parasitic capacitance of the feedback capacitors

$$gm_{ff} = 2\pi GBW \cdot C_{out2} = 47\ \mu\text{S}$$

This means 2.5 μA current flows in the feedfoward transistors connected to the OTA output.

Once GBW is fixed, one can choose gm_1 and gm_2. In order to limit power

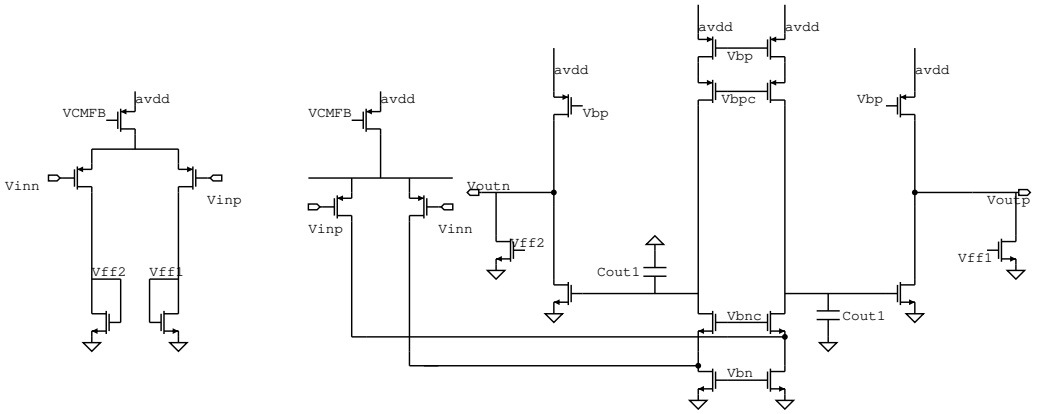

Figure 4.9: Schematic of the feedforward OTA

consumption, the tail current has been chosen as low as 500 nA.
The aim of the design is to have approximatively the same noise density of the switched-capacitor implementation, but with a reduced power consumption. Therefore, we chose $gm_1 = 5$ μS and $gm_2 = 24$ μS. This means 1.5-μA current in the NMOS transistor of the output stage[7].
The last equation says:

$$C_{out1} = \frac{2gm_1gm_2C_{out2}}{gm_{ff}^2} = 27\ fF.$$

This means that it is necessary to put a small explicit capacitance on the output of the first stage. To increase phase margin, in order to take into account the effect of process and temperature variations, C_{out1} can be increased to about 60 fF.
Virtual ground displacement for the feedforward design can be seen in Figure 4.10. The initial overshoot is due to the presence of the zero. It is important to control its amplitude to avoid distortion. Anyway the virtual ground settles at much lower value (as expected) and can be calibrated.
Simulation results for the loop gain are shown in Figure 4.11, where the effect of the zero is evident.

Interestingly, the common-mode feedback can exploit the same principle of the differential loop if the common-mode stage controls the tail currents

[7]The PMOS transistor current source of the output stage has to provide $I_{\mathrm{PMOS}} = I_{feedforward} + I_{NMOS_{Outputstage}} = 4$ μA.

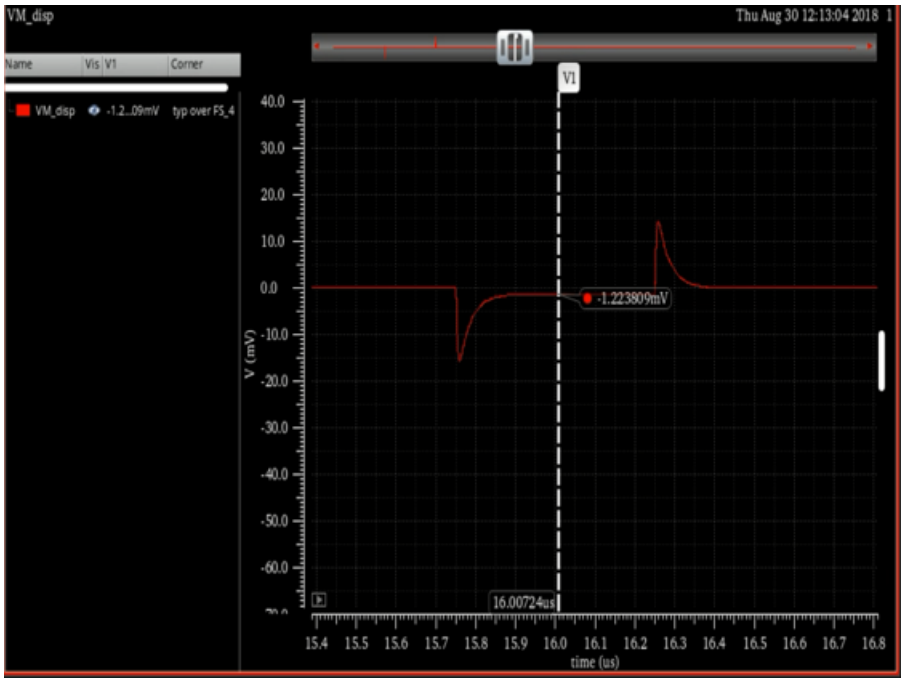

Figure 4.10: Virtual ground displacement in feedforward OTA

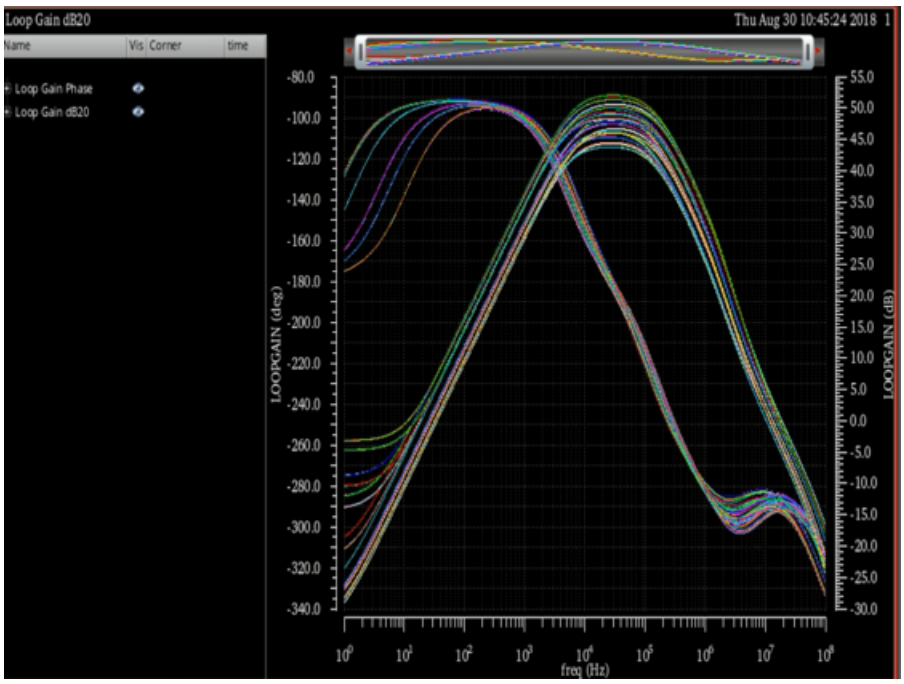

Figure 4.11: Loop gain corners of the feedforward OTA

of both the input pair and the feedforward structure. Gate control voltage V_{CMFB} is indicated in Figure 4.9.
The common-mode feedback stage structure is shown in Figure 4.12, where diode-connected devices are used in order to avoid the presence of another low frequency pole in the common-mode feedback loop gain.

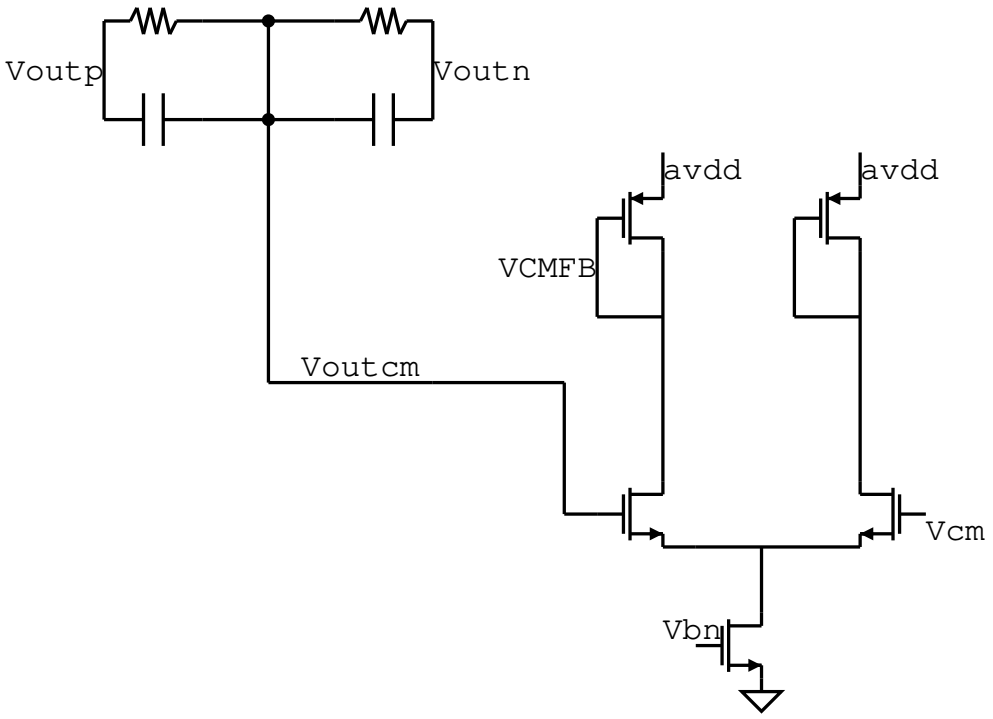

Figure 4.12: Common-mode feedback

4.5 Overall Linearity

The overall linearity of the CT converter can be simulated with Spectre (transient simulations). Simulation results, evaluated over temperature to verify the effectiveness of the calibration procedure, are shown in Figure 4.13. The overall accuracy is slightly worse than in the DT *SC* implementation, but still calibration is quite effective. The INL of the converter is between ± 2.5 LSB.

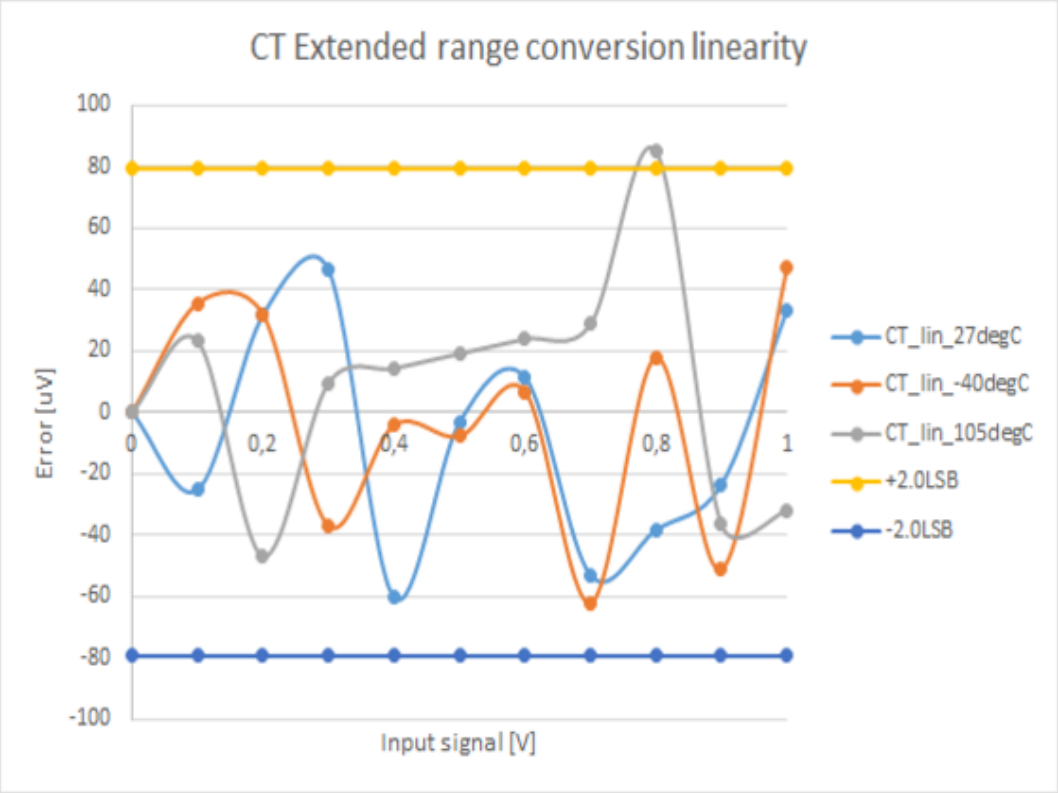

Figure 4.13: Continuous-time converter linearity

4.6 Noise Analysis

4.6.1 Integrator Noise

In Section 4.4 the integrator was designed to reduce the power consumption to the minimum possible value. The aim of the design was to obtain an overall *ADC* noise power spectral density similar to what achieved in the DT *SC* implementation (see Section 4.6.3), but with a reduction in the power consumption. This is reasonable since the sinc filter attenuation allows a minimum amount of folding.
The integrator, along with thermal noise from input and feedback resistors, is simulated with the same testbench used for the DT *SC* solution (see Section 3.8).
The results are shown in Figure 4.14, where chopping of the integrator is not performed[8].

4.6.2 Jitter Noise

A CT incremental *ADC* with continuous time feedback is sensitive to clock jitter [29]. In order to correctly evaluate this noise source, it is reasonable to consider jitter as an equivalent variation of the reference voltage.
Clock jitter is traditionally evaluated in the frequency domain, measuring phase noise. For this application *PLL* phase noise was measured at 10 MHz frequency with a spectrum analyzer and then scaled to the clock frequency of 2 MHz. The measured phase noise curve is shown in Figure 4.15.

Period jitter is the quantity of interest. This means that the phase noise curve of Figure 4.15 has to be high-pass filtered and then integrated over frequency. These operations allow us to obtain the rms period jitter, which turns out to be 167 ps. This value can be used in the Matlab model to evaluate the effect on the converter resolution.
The effect of jitter is anyway attenuated by the use of a three level quantizer. For small signals, indeed, the effect of clock jitter is negligible.

[8]Noise density of the CT integrator is higher since currents are lower. Input and *DAC* resistors have been also considered.

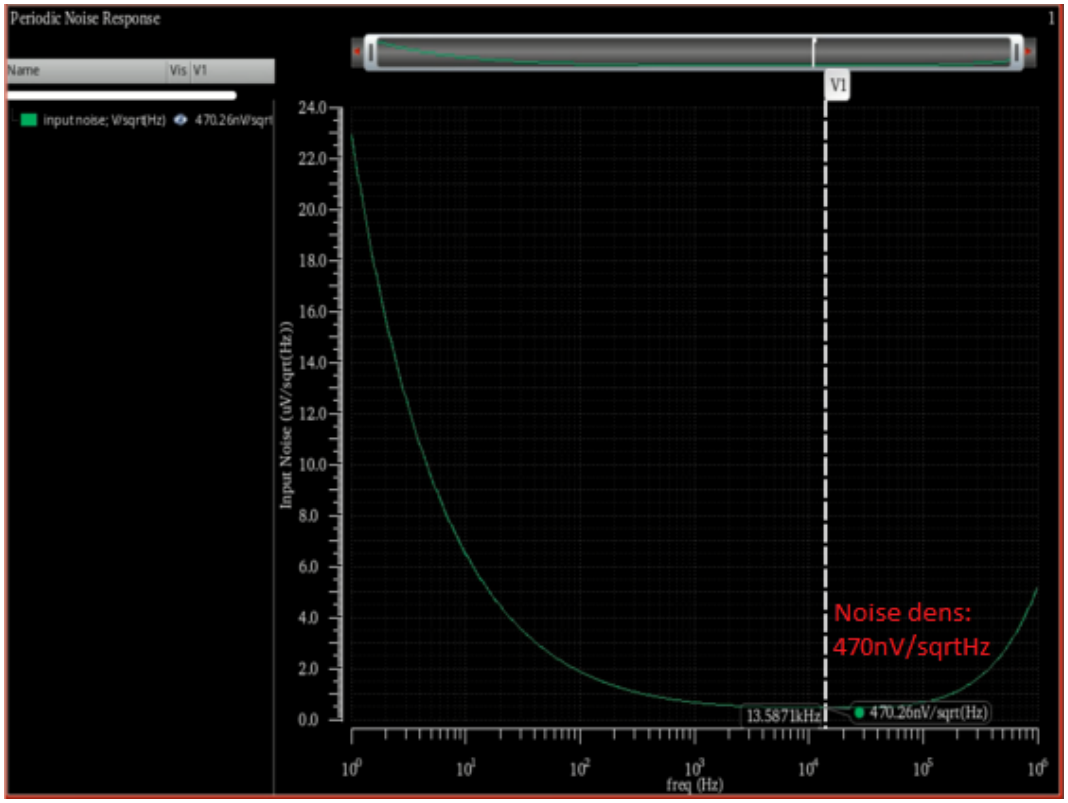

Figure 4.14: Continuous-time integrator simulated noise

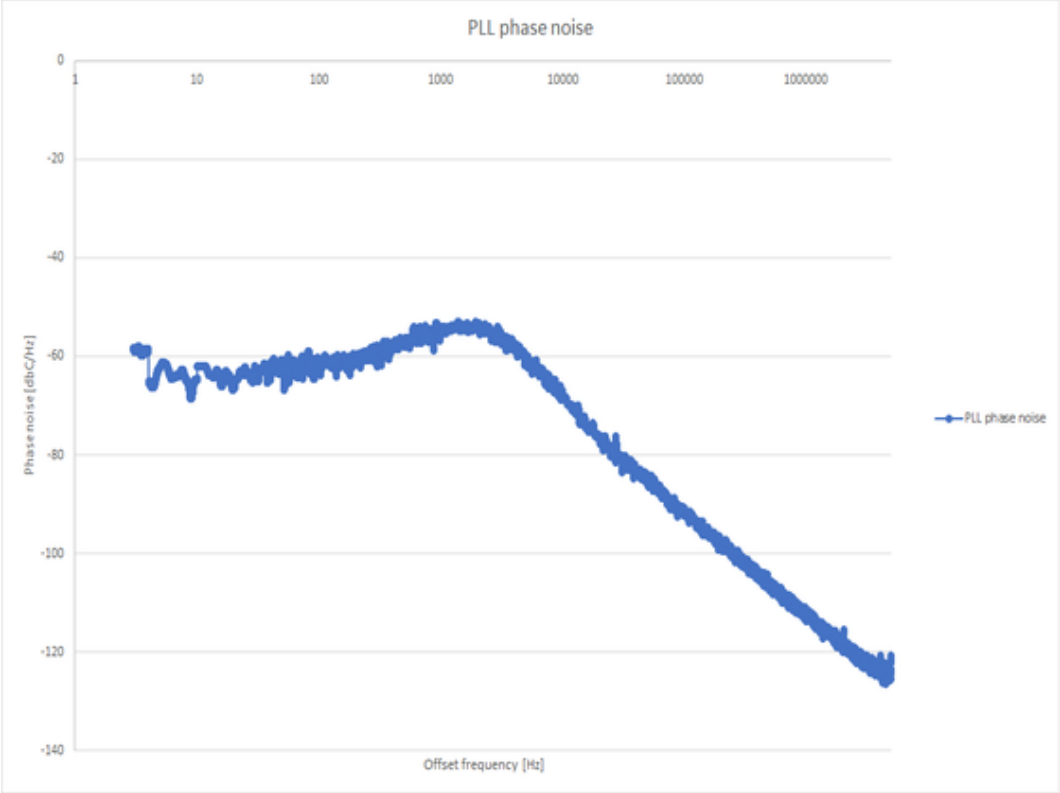

Figure 4.15: PLL phase noise curve at 10 MHz

4.6.3 Overall Noise Simulated with the Matlab Model

All the considered noise sources can be added to the Matlab model in order to evaluate their effect on the overall converter resolution. As expected, the achieved noise density is similar to what achieved with the switched capacitor implementation. Results are presented in Figure 4.16.

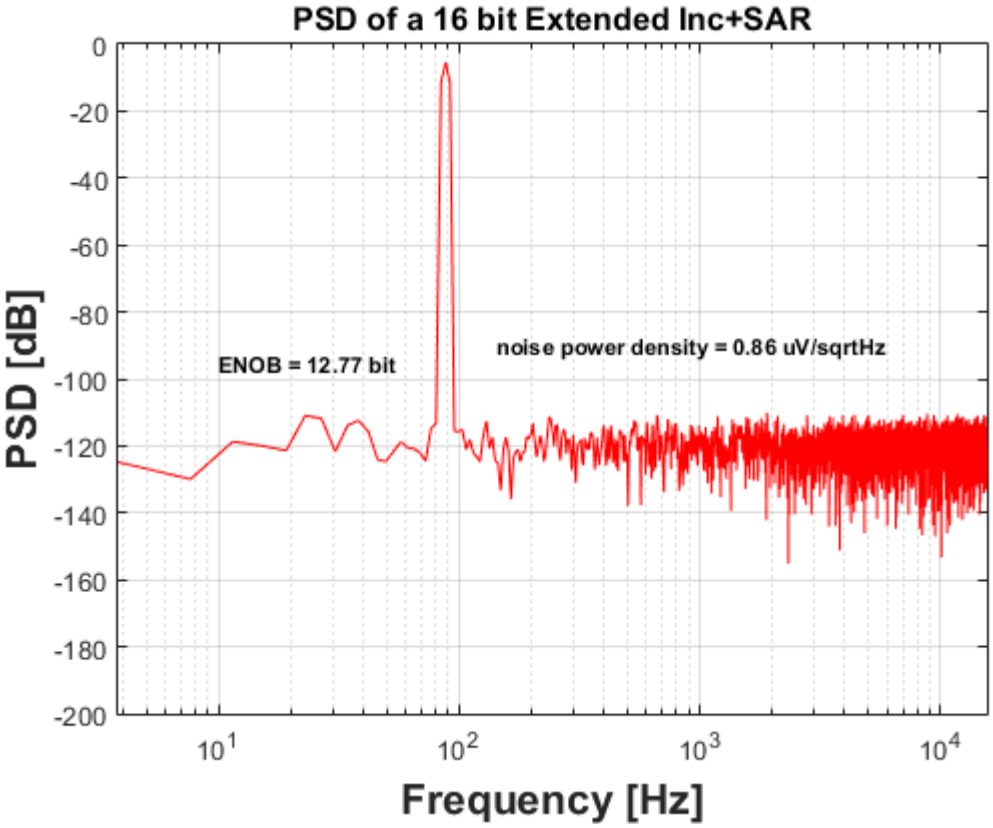

Figure 4.16: Overall noise power spectral density and ENOB (noise from simulated analog CT blocks)

4.7 Conclusions

The design of a CT incremental *ADC* was analyzed. The main focus was on the design of the CT integrator. Reasonable accuracy was achieved with a dedicated calibration procedure. A relevant reduction of the power consumption

is obtained, since the anti-aliasing filter is removed. A summary of the achieved results compared to the DT *SC* solution is reported in Table 4.1.

Table 4.1: Simulation results for DT and CT extended-range *ADCs*

Parameter	*Sim (CT)*	*Sim (DT)*	*Comparison*
Current Consumption	40 μA	60 μA	33% Reduction No *AAF*
Area	< 0.1 mm^2	< 0.1 mm^2	Similar Area
Linearity-INL	$\pm$2.5 LSB	$\pm$1 LSB	Effectiveness of calib in CT
Linearity-DNL	$\pm$0.25 LSB (typ)	$\pm$0.25 LSB (typ)	SAR Caps
Resolution (ENOB)	12.8 bits	12.8 bits	Same Noise
Signal Range	1.3 V	1.3 V	–
Signal Bandwidth Single Channel	15 kHz	15 kHz	–

Chapter 5

Test-Chip Measurements

In this Chapter, the measurement results obtained from the fabricared test chip will be presented. The test chip integrates the discrete-time implementation of the extended-range ADC.
After an introduction showing the measurement setup and instrumentation used, preliminary results on the linearity of the conversion will be presented. The consistency between measurements and specifications will also be checked. In the second part of the chapter the measurement results of the overall ADC linearity and noise will be performed.
A comparison with the state of art will conclude the Thesis.

5.1 Measurement Setup

The measurement setup used for the characterization of the test chip and a chip photograph are shown in Figure 5.1 and Figure 5.2.
The analog and digital supplies are external and decoupled to ground with 100 nF capacitors. The input signal for the ADC is given from one of the analog outputs of the National Instruments $NIDAQ$.
An external voltage ($NIDAQ\ DAC$) is also used as input of the reference generator (bandgap voltage).
The bias current is obtained with a resistance from a +5 V supply.
The test chip clock, SDA and SCL ($I2C$ signals for data ADC reading), are provided by an $FPGA$.

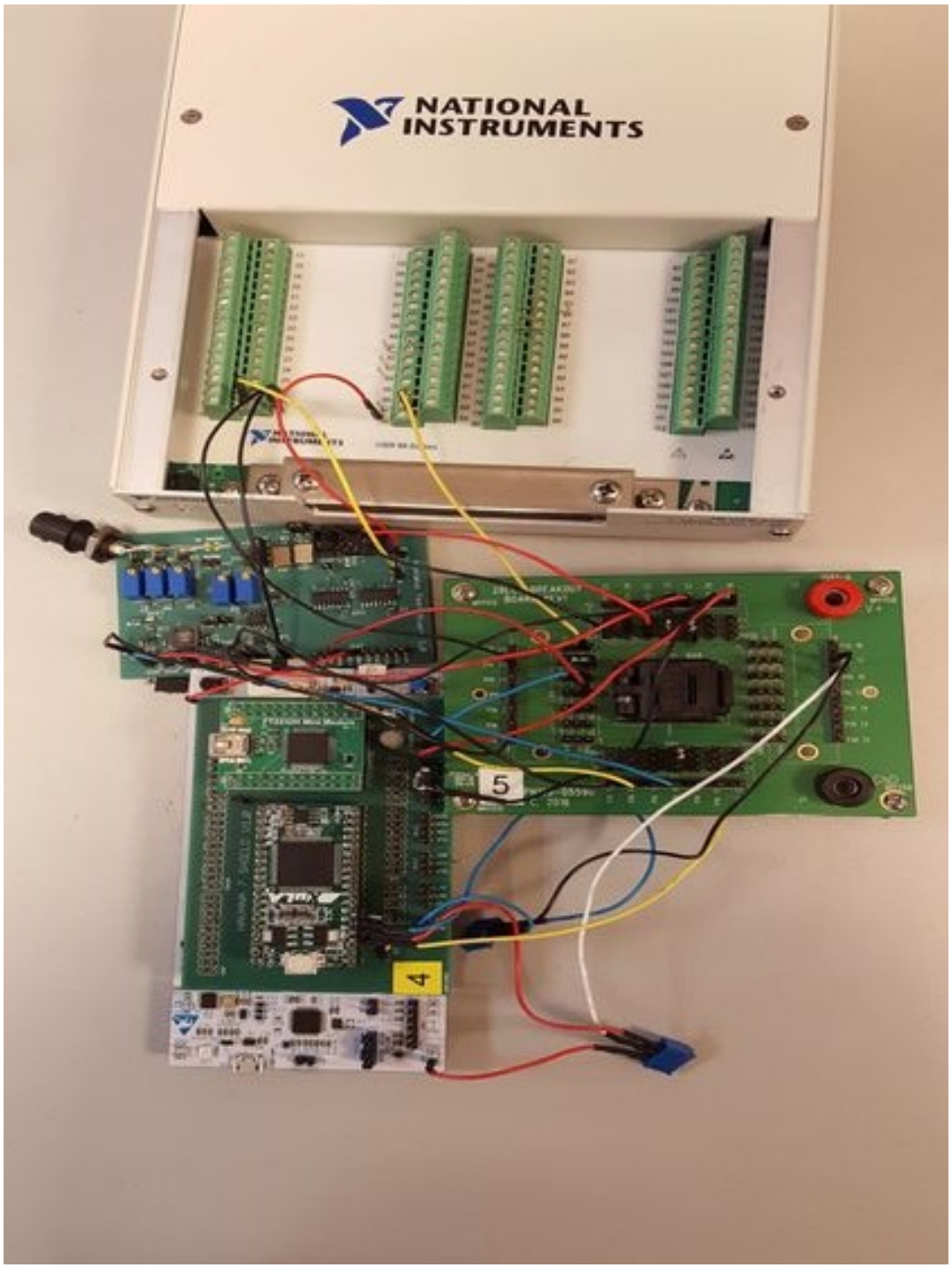

Figure 5.1: Measurement setup

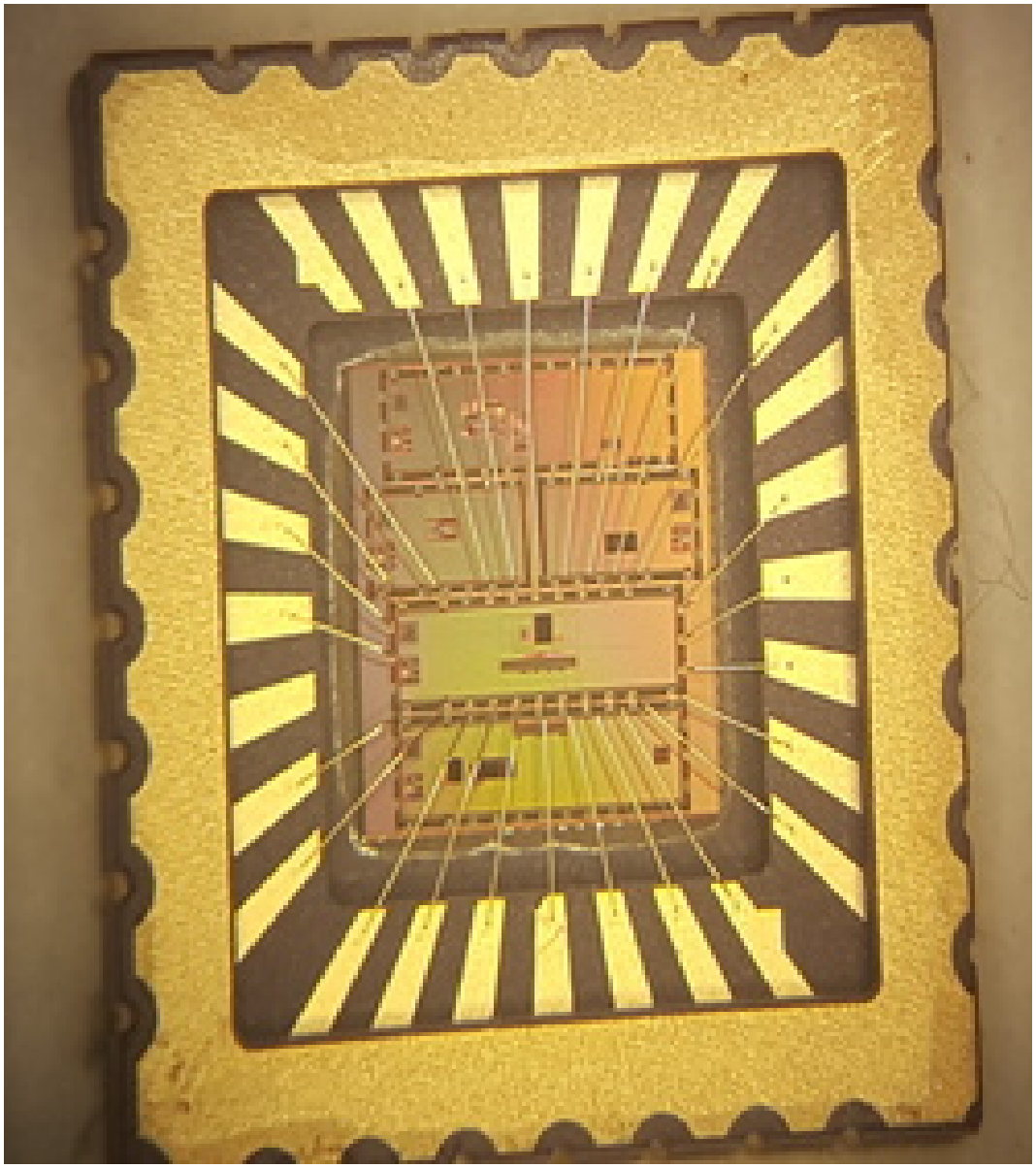

Figure 5.2: Test chip photograph

5.2 Initial Measurements

Preliminary measurements were performed to verify the overall performance of the extended-range *ADC* and check that the specifications are met.

A ramp with 20 points (50 mV equally spaced *DC* input values from 0 to 1 V) was used to determine offset and gain error and evaluate the integral non-linearity. In order to cancel the effect of noise of the converter, every measurement point is averaged on hundreds of conversions.

Results are shown in Figure 5.3, Figure 5.4, and Figure 5.5.

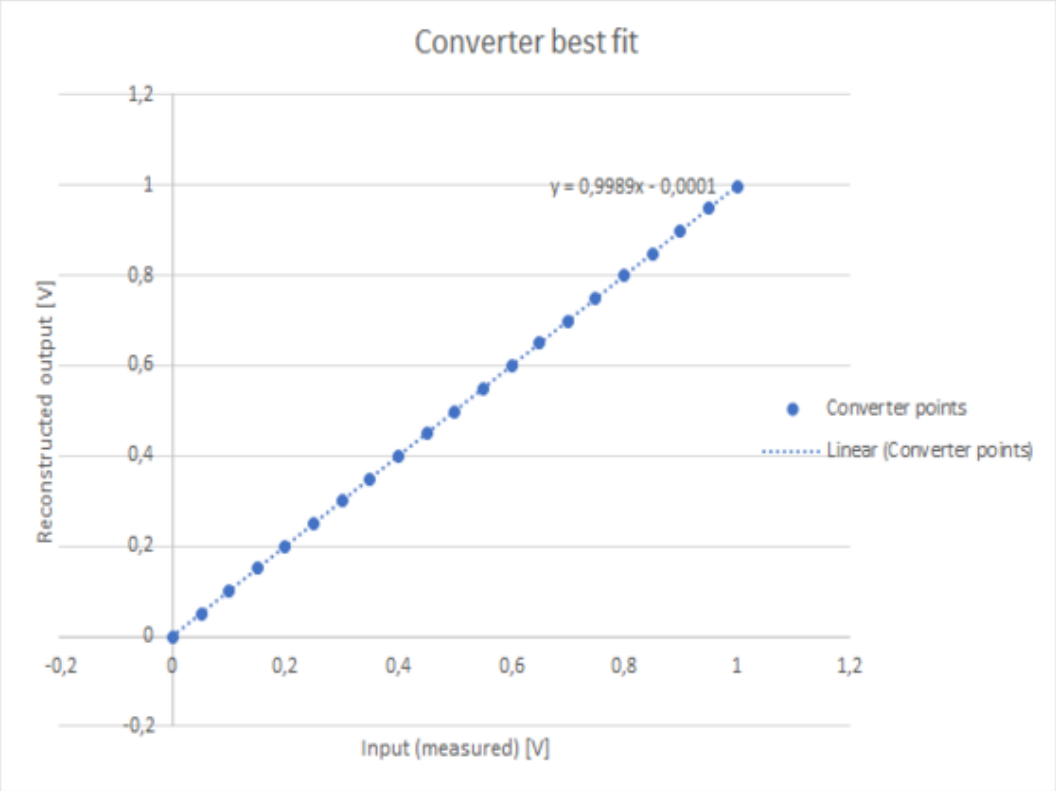

Figure 5.3: Linear fit of ADC output

While a more rigorous approach is needed to verify linearity of the conversion, a INL value slightly greater than simulation can be found around 600-700 mV input. This can be explained in terms of the large steps that the integrator performs in that range of signal (slew-rate) or in terms of a limited GBW value. This possibly introduces a slight non-linearity. Values are anyway well within specifications in terms of INL (Figure 5.5).

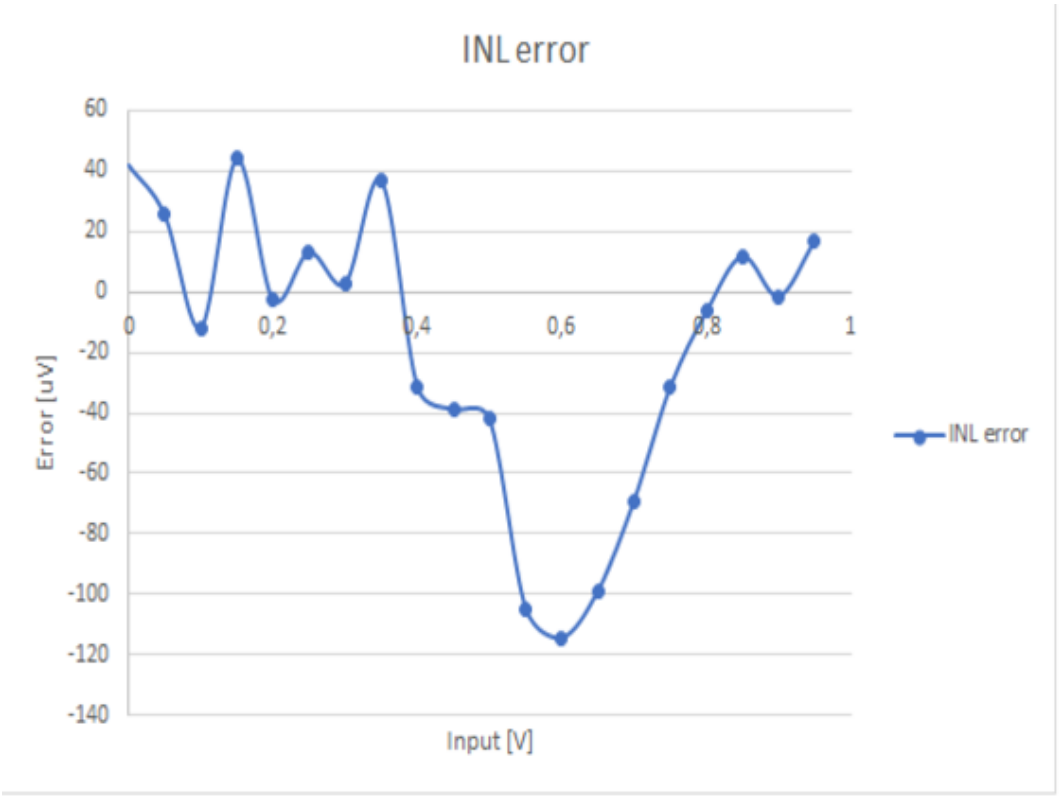

Figure 5.4: Integral non-linearity measured over 20 points

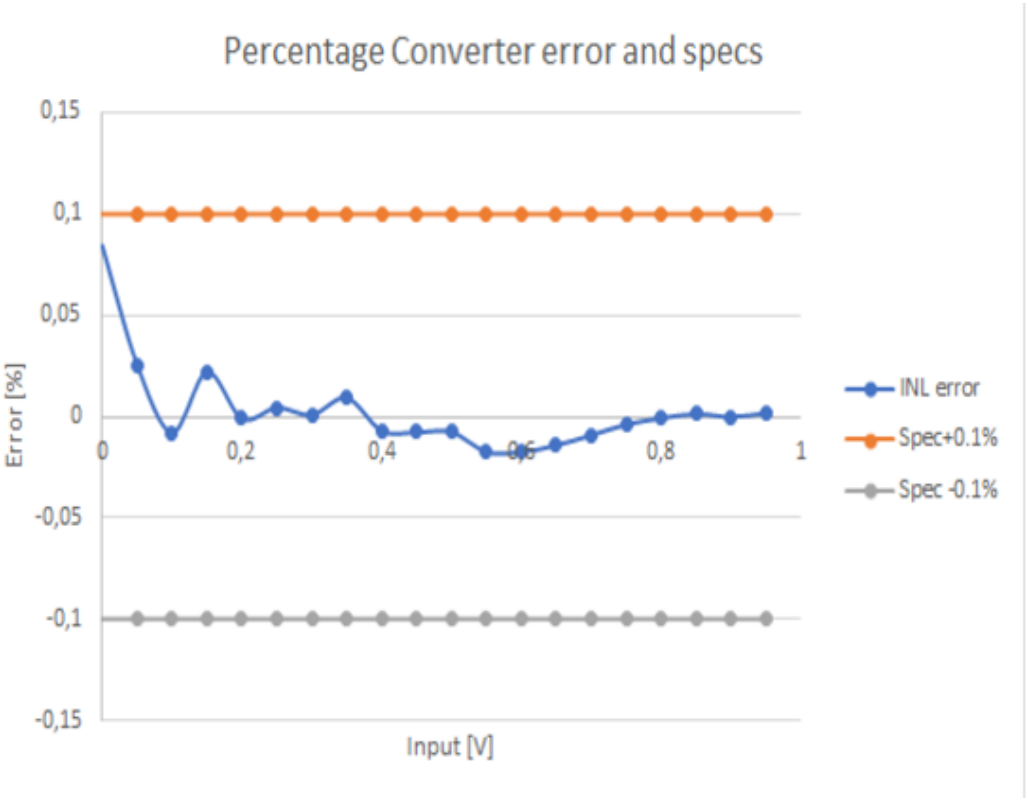

Figure 5.5: Integral non-linearity measured over 20 points and ±0.1% specification

5.3 Linearity and Noise Measurements

A more rigorous way to evaluate the overall linearity (DNL and INL) of the converter in the presence of noise is the method described in Chapter 1. The results obtained with this method are shown in Figure 5.6 and Figure 5.7.

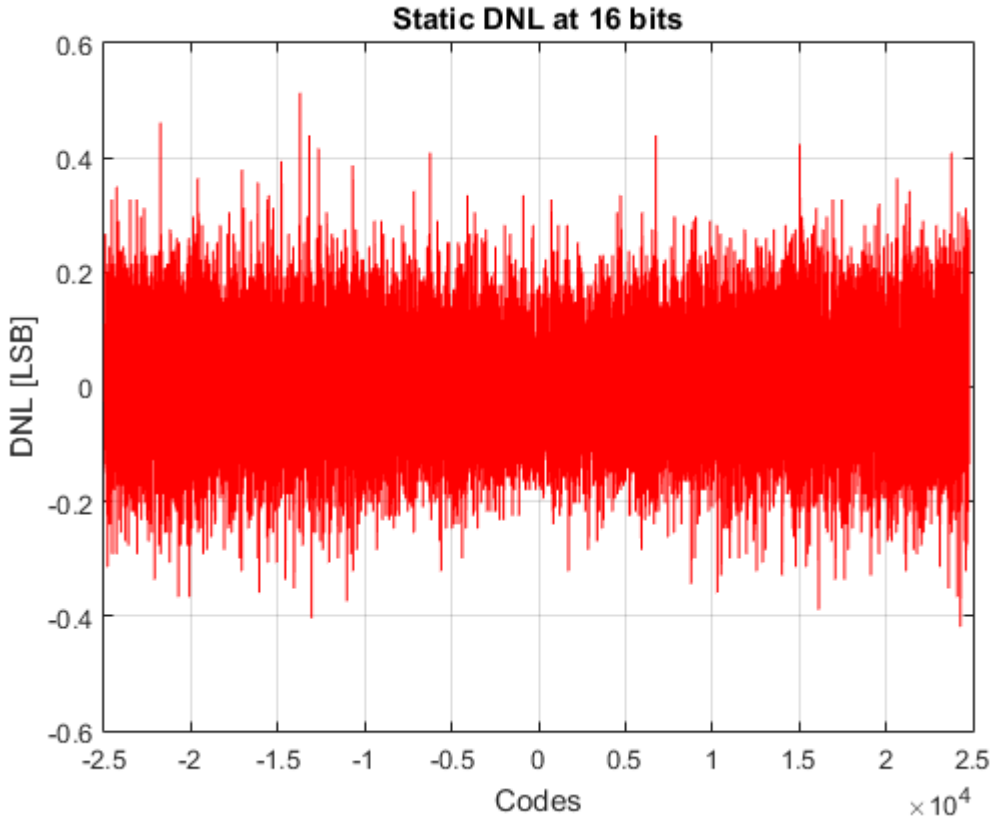

Figure 5.6: Measured differential non-linearity (DNL)

The number of points taken for every LSB is in the order of 150[1].
The analysis of DNL and INL reveals that the general behavior of the converter is acceptable .
The DNL values are between ± 0.5 LSB, mostly between ± 0.25 LSB and in line with the Matlab model simulations for linearity of the extended-range ADC, including the extracted capacitance of the $SAR\ ADC$ array.
A bit of concern is raised by the effect visible in Figure 5.7 and zoomed in

[1]The average of code densities is around 150.

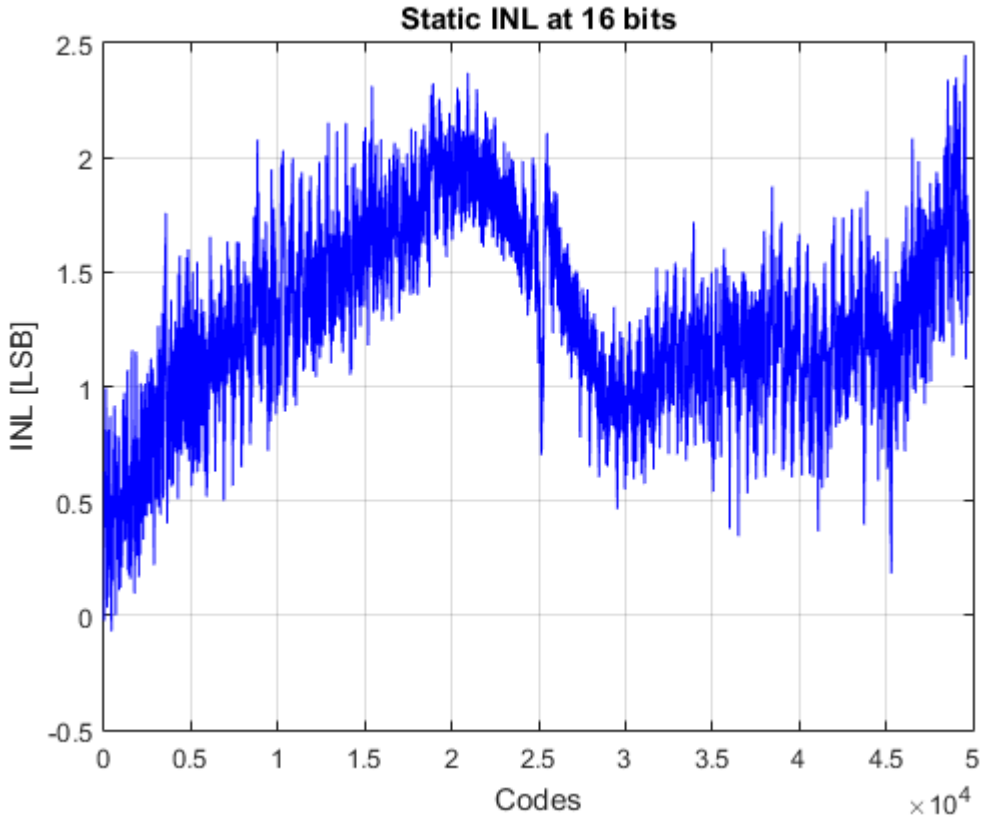

Figure 5.7: Measured integral non-linearity (INL)

Figure 5.8. This effect is related to a non-perfect alignment between the SAR

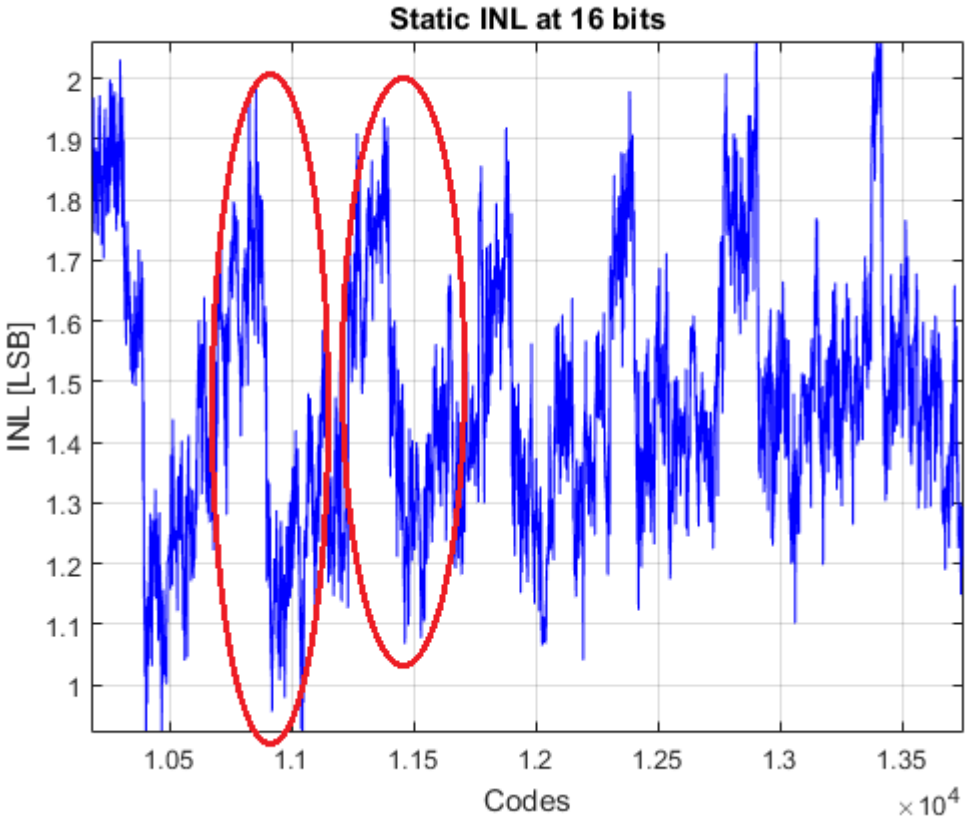

Figure 5.8: Zoom on integral non-linearity (INL) plot

ADC and incremental gains or, equivalently, to an error of the interstage gain between the coarse and the fine $ADCs$, which is not exactly equal to $\frac{C_{in}}{C_{int}}OSR$. This is due to the capacitive mismatch between the input and the integrating capacitors or to a GBW of the integrator not exactly matching simulations[2]. A solution to the problem could be increasing the value of the input and integrating capacitances or introducing the calibration methodology used and explained for the CT solution in Chapter 4.

In the CT case, indeed, the resistance variation over temperature and the virtual ground displacement were compensated for. Likewise, here the capacitance mismatch could be taken into account. Since a capacitive ratio does not change

[2]A reduction of the GBW can be due to the effect of a parasitic capacitance, on the Miller or cascode compensations, greater than expected. This reduces the ratio $\frac{gm}{C_c}$.

with temperature only one calibration value would be needed.
As for the GBW of the integrator, further post layout simulations need to be performed to verify parasitic effect on compensating capacitors.
Also a slight increase of the tail current of the integrator could be beneficial.

The noise performance was evaluated taking the standard deviation of the output of the $SAR\ ADC$. If the input signal is such that the output of the incremental ADC alone does not change its value in the presence of noise[3], the standard deviation of the value converted by the $SAR\ ADC$ is a measure of the converter overall noise. Measured values (standard deviations), divided by the interstage gain and the square root of the converter bandwidth, give the input referred noise power spectral density of the converter for different values of the input signal.
As expected, the noise power spectral density increases with the input signal since the reference generator is increasingly adding noise to the conversion. A comparison with simulated results is shown in Figure 5.9.

The difference between measured and simulated values can be explained in terms of the noise floor introduced by the measurement setup. Possibilities of improving the measurement setup will be considered, while the final product will include a Bandgap reference, as well as internal $I2C$ and supplies, significantly reducing the number of interconnections visible in Figure 5.1.

5.4 Result Summary and Comparison with the State-of-the-Art

Table 5.1 summarizes the measured performances of the ADC and compares them with simulation results.

A comparison with the state-of-the-art is instead shown inTable 5.2.

The measured results are compared with a solution where the coarse conversion is performed by a $SAR\ ADC$ while the fine bits are given by a first-order incremental ADC [30] and with the work described in [31], which is reported

[3]This happens if the converted value is away from a transition between the coarse and the fine ADC.

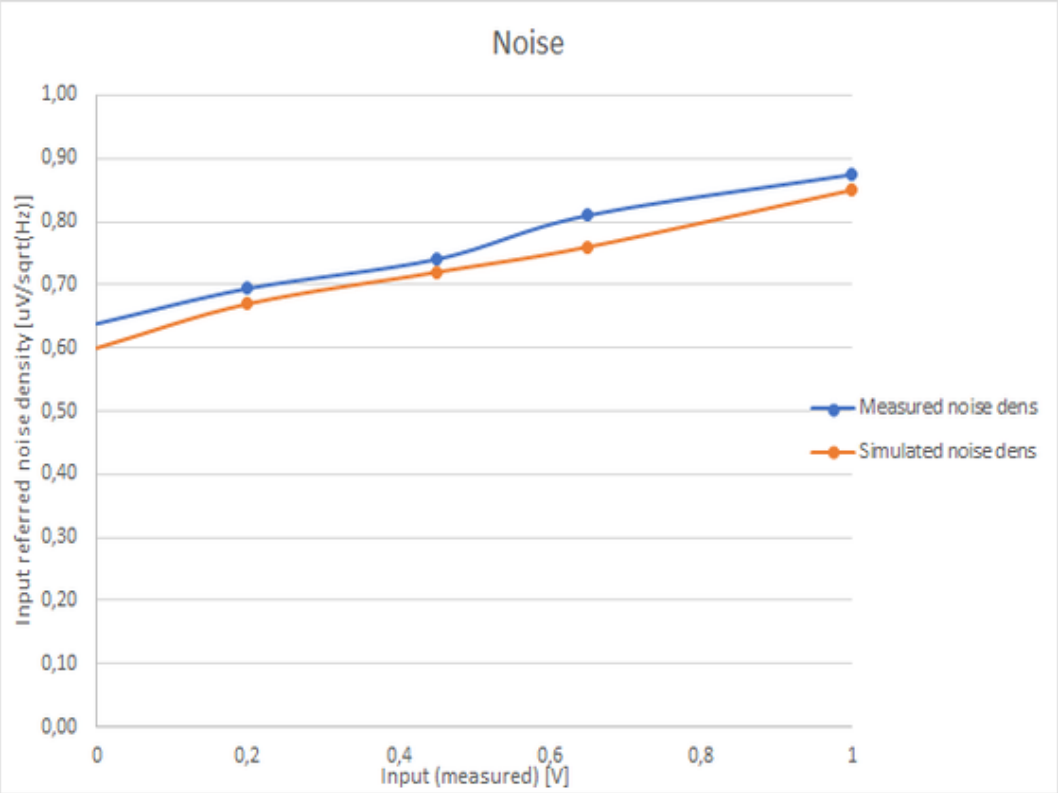

Figure 5.9: Noise measured over the whole *ADC* input range

Table 5.1: Result summary for the DT extended-range *ADC*

Parameter	*Measurement*	*Simulation*
Current Consumption	60 μA	60 μA
Linearity-INL	2.5 LSB (Code Density Test)	$\pm$1 LSB @ 16 bits
Linearity-DNL	$\pm$0.5 LSB (Code Density Test)	$\pm$0.25 LSB @ 16 bits
Noise density at 0 V	0.64 $\frac{\mu V}{\sqrt{Hz}}$	0.6 $\frac{\mu V}{\sqrt{Hz}}$
Noise density at 1 V	0.87 $\frac{\mu V}{\sqrt{Hz}}$	0.85 $\frac{\mu V}{\sqrt{Hz}}$

Table 5.2: Comparison with the state-of-the-art

Parameter	*ESSCIRC13 [30]*	*JSSCC15 [31]*	*This Work*
Architecture	10-Bit SAR+IADC1	IADC2+IADC1	IADC1+SAR
Process	0.6 μm	65 nm	110 nm
Power Consumption	64 μW	10.7 μW	90 μW
Bandwidth	9.75 kHz	250 Hz	15 kHz
Area	1.64 mm^2	0.2 mm^2	**<0.1** mm^2
ENOB	11.35 bit	14.78 bit	12.78 bit

as one of the greatest achievements in incremental $ADCs$.
It is interesting to notice that this work excels in terms of area reduction.

Until now the comparison was performed looking at similar ADC architectures where Incremental Converters where exploited.
A $SAR\ ADC$ is used in [1] as the ADC for a MEMS Accelerometer Front-End. Here linearity requirements are quite relaxed, while a split DAC array structure is used to reduce area occupation.
For a given technology, if a designer is limited by capacitance mismatch and has an area constraint (as usually happens), the split DAC array structure allows to extend the nominal resolution with a greater unit capacitance with respect to the standard SAR implementation.
From another point of view the same resolution can be achieved with a much smaller area. The great disadvantage is the sensitivity to the parasitic capacitance connected to the top plate of LSB array. Results achieved in terms of linearity can be affected as represented in Figure 5.10.

This example can be used to validate the approach chosen in this work also for medium-low resolutions.
10 bits of resolution in this case could have been divided between an Incremental ADC (5 bits for instance) and the 5 LSB bits left to the $SAR\ ADC$.
The requirements on $SAR\ ADC$ are in this case quite relaxed allowing also the use of the standard parasitic insensitive structure without a significant increase in area occupation.
Noise performances would be limited by the Incremental thermal noise. It

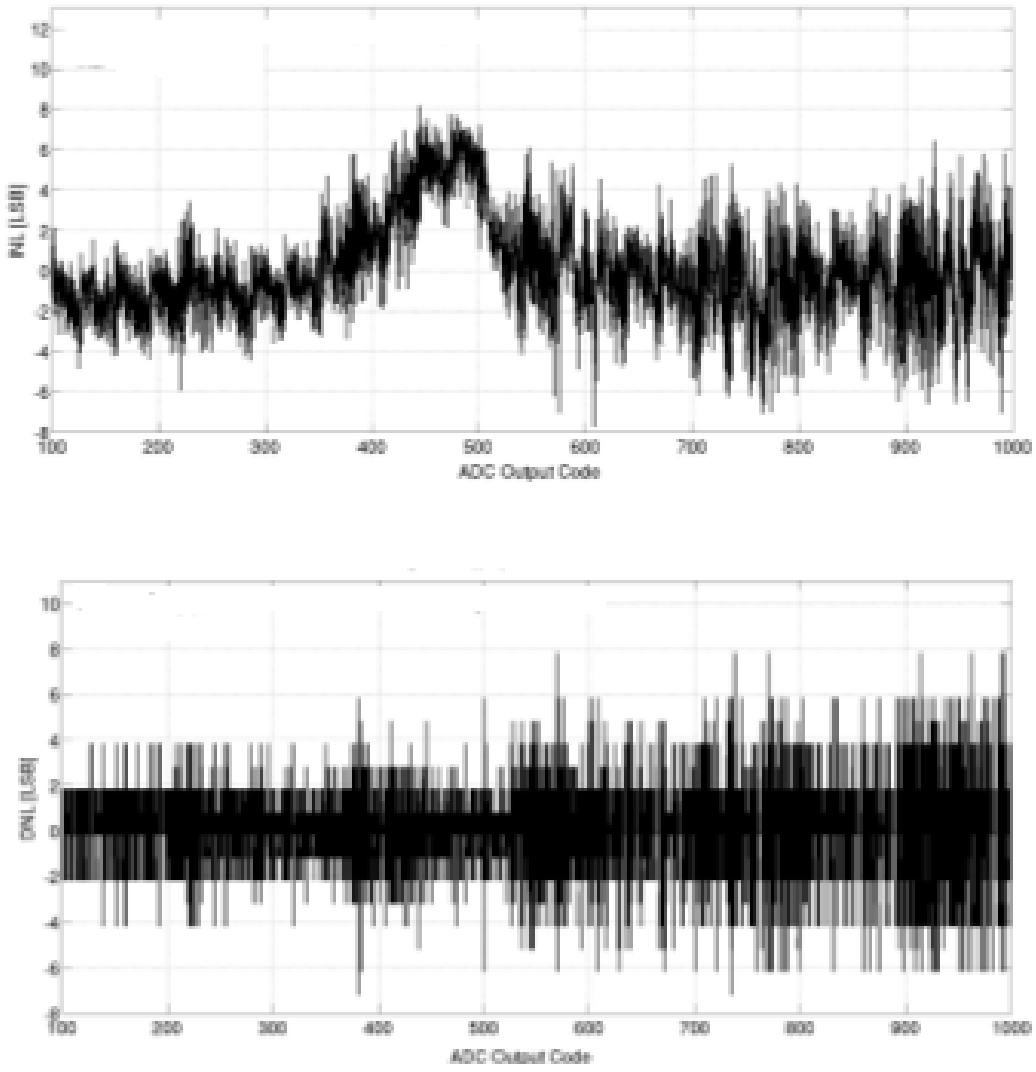

Figure 5.10: DNL and INL for the ADC in [1]

is useful here to remember that a significant capacitance is required only for resolutions above 14 bits. The only disadvantage would be the introduction of the incremental integrator and a slower operation required for the ADC. As often happens the choice of the best architecture is not straightforward.

One of the great advantages of the proposed First Order Incremental and $SAR\ ADC$ architecture is the extreme simplicity of the implementation used to achieve medium-high resolutions.
One integrator, three comparators (two for the Incremental ADC and one for the $SAR\ ADC$), a Counter, the SAR capacitance array and some standard logic for the $SAR\ ADC$.
This means very low power and minimum area occupation (see Table 5.2).

The work in [32] implements a Continuous Time Sigma Delta Modulator to obtain great power reduction and 15 bit resolution.

While results achieved are great in terms of resolution and power consumption, a much more complex implementation is required. Design choices are well explained in [32], Section II.
A third order modulator with a multibit quantizer is required. This means three integrators and 15 differential comparators are used in the design with an area occupation of 0.72 mm^2, a much greater value than that obtained in this work.

Continuous and Discrete time Sigma Delta Modulators are the usual choice for high resolution-audio applications.
When linearity and sample to sample precision are required, a First Order Incremental-SAR Extended range conversion seems a great choice for consumer sensor applications where extreme area reduction and very low power consumption are fundamental requirements.

Conclusions

A 110 nm extended-range *ADC* for a three-axis MEMS accelerometer, consisting of an incremental *ADC* stage followed by a *SAR ADC* stage, was modeled, designed, and tested. This *ADC* architecture exploits the advantages of an oversampling conversion for the coarse conversion along with the speed and power efficiency of *SAR ADC* for the fine conversion.

Starting from the design specifications, a Matlab model was created in order to simulate the behavior of the whole *ADC*.
The switched-capacitor implementation of the incremental and *SAR ADCs* have been designed at transistor level and integrated in a test chip, which has been fully characterized.
An interesting alternative for the design of the incremental *ADC* (continuous-time solution) was proposed. The use of a continuous-time incremental *ADC* allowed a relevant amount of power to be saved(Chapter 4).

Future activities will consist of further measurements on the test chip along with a possible tape-out of the continuous-time solution.
Meanwhile other simulations need to be performed on the switched-capacitor implementation in order to verify issues coming from measurement results (see Chapter 5).

The designed (and measured) switched-capacitor extended-range *ADC* excels in terms of area reduction due to the limited number of analog blocks and the simplicity of the digital circuitry required for the first-order incremental *ADC*, making it a robust and efficient solution for a multiplexed three-axis MEMS accelerometer.

Bibliography

[1] M. D. Matteis, A. Pezzotta, M. Sabatini, M. Grassi, M. Croce, P. Malcovati, and A. Baschirotto, "A 0.13µm-CMOS 90µW 51dB-SNR continuous-time accelerometer front-end with 10b SAR-ADC," *IEEE Sensors*, 2015.

[2] N. Yazdi, F. Ayazi, and K. Najafi, "Micromachined Inertial Sensors," *Proc. IEEE*, vol. 86, pp. 1640–1659, 2009.

[3] P. Michalik, A. Napieralski, D. Fernández, and J. Madrenas, "Technology-portable Mixed-signal Sensing Architecture for CMOS integrated z-axis Surface-micromachined Accelerometers," *17th Int. Conf. Mixed Design of Integrated Circuits and Systems (MIXDES 2010), Wroclaw, Poland*, pp. 431–435, 2010.

[4] F. E. H. Tay, J. Xu, and V. J. Logeeswaran, "A differential capacitive low-g microaccelerometer with mg resolution," *Sensors and Actuators A Physical*, pp. 45–51, 2000.

[5] H. Kulah, J. Chae, N. Yazdi, and K. Najafi, "A multi-step electromechanical sigma-delta converter for micro-g capacitive accelerometers," *IEEE Int. Solid-State Circuits Conference*, pp. 202–203, 2003.

[6] M. Lemkin and B. Boser, "A three axis micromachined accelerometer with a CMOS position-sense interface and digital offset-trim electronics," *IEEE Journal of Solid-State Circuits*, vol. 34, pp. 456–468, 1999.

[7] H. Kulah, J. Chae, N. Yazdi, and K. Najafi, "Noise analysis and characterization of a sigma-delta capacitive microaccelerometer," *IEEE J.Solid-State Circuits*, vol. 41, pp. 352–361, 2006.

[8] N. Yazdi, H. Kulah, and K. Najafi, "Precision Readout Circuits for Capacitive Microaccelerometers," *Sensors*, 2004.

[9] J. C.-C. Shiah, "Design Techniques for Low-Power Low-Noise CMOS Capacitive-Sensor Readout Circuits," 2007.

[10] P. D'Abramo, A. Maccioni, G. Pasetti, and F. Tinfena, "Advanced Sensor Solutions For Automotive Applications."

[11] R. J. V. de Plassche, *CMOS Integrated Analog-to-Digital and Digital-to Analog Converters*, Second ed. Springer US, 2003.

[12] F. Maloberti, *Data Converters*, 1st ed. Springer Verlag, 2007.

[13] J.Markus, J.Silva, and G.Temes, "Theory and Applications of Incremental Delta Sigma Data Converters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 51, 2004.

[14] S. Pavan, R. Schreier, and G. C. Temes, *Understanding Delta Sigma Data Converters*, 2nd ed. Wiley-IEEE Press, 2017.

[15] R.Harjani and T.A.Lee, "FRC: A method for extending the resolution of Nyquist rate converters using oversampling," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 45, 1998.

[16] C.Jansson, "A high resolution, compact, and low-power ADC suitable for array implementation in standard CMOS," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 42, 1995.

[17] Y. Zheng, Z. Wang, S. Yang, Q. Li, and L. Xiang, "A Novel Two-Split Capacitor Array with Linearity Analysis for High-Resolution SAR ADCs," *International Journal of Electronics and Electrical Engineering*, vol. 3, 2015.

[18] F. Hua, W. Qi, K. S. Bomeh, Y. Xiumei, and Y. Huazhong, "An 8-bit 180-kS/s differential SAR ADC with a time-domain comparator and 7.97-ENOB," *Journal of Semiconductors*, vol. 31, 2010.

[19] L.Lodola", "Design and automated characterization of a 10 bit SAR ADC for diffraction imaging at X-ray FELs," 2016.

[20] B.Razavi, *Design of Analog CMOS Integrated Circuits*. Mc Graw Hill, 2001.

[21] J. H. Huijsing, R. Wu, and K. A. A. Makinwa, *Precision Instrumentation Amplifiers and Read-Out Integrated Circuits*, 1st ed. Springer-Verlag New York, 2013.

[22] F. Maloberti, *Analog Design for CMOS VLSI Systems*, 1st ed. Springer US, 2001.

[23] B. K. Ahuja, "An Improved Frequency Compensation Technique for CMOS Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 18, 1983.

[24] C.-C. Liu, S.-J. Chang, G.-Y. Huang, and Y.-Z. Lin, "A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure," *IEEE Journal of Solid-State Circuits*, vol. 56, 2010.

[25] M.Terrovitis and K.Kundert, "Device Noise Simulation of Delta Sigma Modulators," The Designer's Guide Community.

[26] K.Kundert, "Hidden State in Spectre RF," The Designer's Guide Community.

[27] A. Fornasari, P.Malcovati, and F.Maloberti, "Improved Modeling of Sigma-Delta Modulator Non-Idealities in SIMULINK," *IEEE International Symposium on Circuits and Systems*, 2005.

[28] B.K.Thandri and J. Silva-Martinez, "A Robust Feedforward Compensation Scheme for Multistage Operational Transconductance Amplifiers With no Miller Capacitors," *IEEE Journal of Solid-State Circuits, Vol 38*, vol. 38, 2003.

[29] K.Reddy and S. Pavan, "Fundamental Limitations of Continuous-Time Delta-Sigma Modulators Due to Clock Jitter," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, 2007.

[30] S. Ha, J. Park, Y. M. Chi, J. Viventi, J. Rogers, and G. Cauwenberghs, "85db dynamic range 1.2mw 156ks/s biopotential recording IC for high density ECoG flexible active electrode array," *2013 Proceedings of the ESSCIRC*.

[31] C.-H. Chen, Y. Zhang, T. He, P. Y. Chiang, and G. C. Temes, "A Micro-Power Two-Step Incremental Analog-to-Digital Converter," *IEEE Journal of Solid-State Circuits*, vol. 50, 2015.

[32] S. Pavan, N. Krishnapura, R. Pandarinathan, and P. Sankar, "A Power Optimized Continuous-Time ADC for Audio Applications," *IEEE Journal of Solid-State Circuits*, vol. 43, 2008.

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