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Facoltà di Ingegneria
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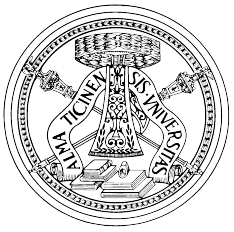

Doctoral Thesis in Microelectronics
XXXI Ciclo

Analysis and Design of Highly Linear Base-Band Filters for SAW-Less FDD Receivers

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Declaration of Authorship

I, Giacomo Pini, declare that this thesis titled, 'Analysis and Design of Highly Linear Base-Band Filters for SAW-Less FDD Receivers' and the work presented in it are my own. I confirm that:

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- Where I have consulted the published work of others, this is always clearly attributed.
- Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work.
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Abstract

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Analysis and Design of Highly Linear Base-Band Filters for SAW-Less FDD Receivers

by Giacomo Pini

Modern communication systems are characterized by the need for increased data-rate. This is typically achieved through a larger channel bandwidth, following the same trend already observed in the past. The number of bands and the number of antennas (MIMO) is expected to grow, as well. In this scenario, it becomes highly desirable to minimize the number of external RF filters in a transceiver, with the goal of limiting area occupation and cost of the system. From the Receiver (RX) side, this imposes strong linearity requirements, posing important design challenges in the base-band (BB) portion of the RX. In typical RX architectures, the first element after passive-mixer is a TIA or a high-order filter, which must be able to handle strong Out-of-Band blockers, without degrading SNR. Two different approaches in the TIA design are proposed here. The first one is based on the more "classical" OTA closed in shunt-feedback. Instead of adopting conventional Miller compensation, the proposed OTA exploits additional zeros created in both OTA and feedback path to achieve stability, achieving increased Gloop unity gain bandwidth (GBW = 1.5GHz). This has positive impact on IIP3, as demonstrated through an intuitive but quantitative linearity analysis. Following this approach, a Stand-Alone 20-MHz-BW TIA is designed, achieving +50.5dBm OOB IIP3 and +21 μV_{RMS} in-band noise with 5.4mW consumption. The second proposed TIA is based on the Regulated-Cascode architecture, which is suitable to achieve a TIA bandwidth in the order of ∼100MHz, compatible with the expected Sub-6GHz 5G channel BW. The basic Regulated-Cascode architecture is modified adding a positive capacitive feedback, with benefits for selectivity. Such capacitor improves the Q of the CC poles and adds one additional pole, allowing to implement a 130-MHz-BW 3$^{\text{rd}}$ order Butterworth *current* filter. The filter is integrated in a Mixer-First RX achieving 5.5dB NF, with +21dBm IIP3 at $\Delta f/f_{BW} = 3$, and blocker P_{1dB} of +3dBm at $\Delta f/f_{BW} = 6$. In comparison with the State-of-the-Art around $\sim$ 15x larger bandwidth is achieved, with $\sim 2-3$x smaller power consumption and comparable noise and linearity.

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Introduction

Mobile communications have become an essential part of people everyday life. The number of mobile subscribers has constantly increased over the years and is expected to grow further, leveraging on the widespread diffusion of mobile devices. The range of provided services has widened, starting from simple voice call services of the first mobile network and targeting today most evolved applications, like augmented reality and Internet of Things (IoT). Such continuous evolution pushes a constant research for improved mobile handsets, capable of communicating at a faster rate, with reliable connectivity and with extended battery life-time. From the Radio-Frequency (RF) design point of view this poses strong challenges on the transceivers (TRX) design. To increase data-rate, standards for mobile communications have evolved in such a way to extend as much as possible the channel width, while including an increased number of operative bands and possibly adopting more then one antenna in transmission and reception (MIMO). Focusing on the receiver (RX), weak desired signals have to be detected, while strong Out-Of-Band (OOB) interferers that come with them have to be filtered out. This operation must be performed introducing the minimum amount of noise and distortion, so that the overall signal over noise/distortion ratio ($SNDR$) at the output of the receiving chain is sufficient to guarantee correct detection of the information carried by the signal. In traditional RX designs the existence of multiple bands was managed by implementing several narrow-band receivers, including passive off-chip band-pass SAW filters attenuating the OOB interferers. While increased system complexity was typically compensated by Integrated-Circuit (IC) technology evolution, preserving area and cost of the chip, passive components don't scale correspondingly in number and cost. It becomes then highly desirable to design a single wide-band receiver capable of working over several bands and to make use of passives covering a wide frequency range, or to even completely remove them (SAW-Less). This poses important challenges to the RX from the linearity point of view, since it is required to handle strong un-filtered OOB blockers. In particular, since no filtering is performed at the RX-front end (LNA and Mixer), design of the baseband (BB) portion of the RX becomes very critical. In most cases, the first BB element after signal down-conversion is represented by a Trans-Impedance Amplifier

(TIA), converting the current coming from the passive mixer into voltage and providing filtering on the incoming signal. TIA design is made even tougher by the larger required channel bandwidth. This in fact implies that the TIA has to handle interferers that get closer and closer to the channel edge, being less attenuated. Two different solutions are proposed here for the design of highly linear TIAs for SAW-Less applications. In particular, the work is organized as follows:

In **Chapter 1** a panoramic overview on some of the most popular communications systems is presented, showing the evolution of wireless systems towards large bandwidths and more stringent performance. The main requirements and metrics that are relevant in RX design are quickly presented first. After a brief "historical" introduction on less recent wireless networks, more attention is devoted to the requirements that are specified by the newest mobile standards (4G and 5G), with particular focus on the RX specifications. Some hints are also provided about the future developments of mobile (Full-Duplex, mmWave-5G, Massive MIMO).

In **Chapter 2** the design of a closed-loop 20-MHz-BW TIA for SAW-Less LTE FDD Receiver is described in detail. Particular emphasis is devoted to the description of the OTA structure and on the stability analysis of the circuit. After presenting the architecture, measurements results performed on a 28nm Stand-Alone TIA prototype are shown. The same approach is also applied to a 20-MHz-BW 2^{nd} order Rauch filter which is designed to work as a TIA. Performance of this topology in terms of noise and linearity is assessed through simulation and comparison with the single pole TIA is shown.

In **Chapter 3** the implication of the adopted compensation technique on the linearity of the TIA is analyzed through an intuitive model capable of predicting dominant non-linear contributors in different frequency ranges. The same model is adopted to explain the advantage of the adopted frequency compensation technique if compared with more traditional solutions like Miller or Nested-Miller Compensation.

In **Chapter 4** the design of a 5G-oriented TIA implementing a 130-MHz 3^{rd} order filter is presented. The circuit adopts an improved-Regulated-Cascode instead of a closed-loop architecture, pursuing extended bandwidth, at the cost of lower in-band linearity. The proposed TIA is implemented in a Mixer-First Receiver, whose 28nm prototype measurements are shown.

Chapter 1

Evolution and requirements of wireless standards

Standards for wireless communication have evolved over the years to provide better quality of service and to serve an increasing number of connected users. Many new features have been introduced to maximise the amount of transmitted and received information, asking for increased system performance and complicating the design of wireless transceivers. In this introductory chapter the main metrics which are adopted to describe receiver performance are discussed. A quick overview on the evolution of wireless networks is provided, highlighting in particular those attributes and requirements which are relevant to the design of a receiver for user equipment. Albeit not formally frozen in an official standard, some hints are provided on the expected features of the next wireless standard generation, i.e. 5G.

1.1 Main communication metrics

Wireless communication entails a lot of operations that have to be performed both in the analog and in the digital domain. These consist for example in data modulation and transmission on the transmitter (TX) side, signal detection and reconstruction of the original information on the receiver (RX) side. Since wireless represents a crowded and hostile environment, every block has to be compliant with some specifications, in order to successfully co-operate with the rest of the system. Such requirements are typically specified in reference standards and translate into metrics which are specific to each block. In the following sub-sections attention will be focused on the RX. Some important concepts that are typically employed to quantify a Wireless RX performance

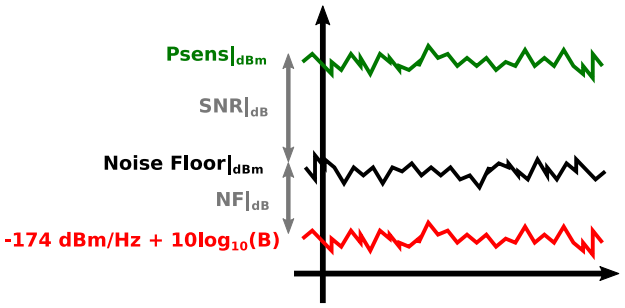


FIGURE 1.1: Simplified explanation of Noise Floor, NF, SNR and Sensitivity relationship

and that are useful for a thorough understanding of the remaining part of the work will be overviewed.

1.1.1 NF and Sensitivity

Since the receiver has to detect very small signals in a noisy environment, one of the main specs is represented by Sensitivity. This parameter in fact quantifies the smallest amount of input power that the receiver must be able to detect while ensuring sufficient signal to noise ratio (SNR) to guarantee proper demodulation of the signal [1]. Sensitivity is expressed by the following relation:

$$P_{sens}|_{dBm} = P_{Rs}|_{dBm/Hz} + 10 \cdot log_{10}B + NF|_{dB} + SNR_{min}|_{dB} \tag{1.1}$$

where $P_{Rs}|_{dBm/Hz}$ is the noise power spectral density of the source, i.e. the antenna, expressed in dBm/Hz, $SNR_{min}|_{dB}$ is the minimum required Signal-to-Noise ratio at the receiver output and B is the channel bandwidth. $NF|_{dB}$ is the receiver noise figure, defined as the ratio between SNR at the input and at the output of the receiver:

$$NF|_{dB} = 10log_{10}\left(\frac{SNR_{in}}{SNR_{out}}\right) \tag{1.2}$$

The sum of the first three terms in (1.1) is usually indicated as noise floor, representing the total receiver noise referred to the input of the RX. Assuming the receiver input is matched to the antenna (50Ω), the noise power spectral density of the antenna $P_{Rs}|_{dBm/Hz}$ equals KT, corresponding to $-174dBm/Hz$ and noise floor can be expressed as:

$$N_{floor}|_{dBm} = -174\left[\frac{dBm}{Hz}\right] + 10 \cdot log_{10}B + NF|_{dB} \tag{1.3}$$

The relationship between Noise Floor and Sensitivity is exemplified in Figure 1.1. The

minimum required SNR is the one that allows achieving the Bit-Error-Rate (BER) specified by the standard and depends on the employed modulation scheme. Qualitatively, the closer the point in the modulation constellation are, the higher is the required SNR, since detection becomes more sensitive to noise. Once SNR_{min} and required Sensitivity are known the maximum acceptable NF, being the actual requirement for the RF designer, can be computed from (1.1).

1.1.2 Non-Linearity

Another non-ideality possibly degrading SNR is non-linear distortion. Analog and RF circuits are typically analyzed under the small-signal approximation, considering the system as perfectly linear, under the assumption that the signal swing is low. Every electronic circuit exhibits however a non linear relation between the input $x(t)$ and the output $y(t)$ signals, which can be in first approximation expressed as a Taylor expansion:

$$y(t) \approx \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \tag{1.4}$$

This implies that if a sinusoidal signal at frequency ω_0 is applied to the input of the circuit, other products at integer multiples of ω_0 (harmonics) appear at the output together with the fundamental tone. Substituting $x(t) = A \cdot \cos(\omega_0 t)$ in (1.4) gives:

$$\begin{aligned} y(t) &= \alpha_1 A\cos(\omega_0 t) + \alpha_2 A^2 \cos^2(\omega_0 t) + \alpha_3 A^3 \cos^3(\omega_0 t) \\ &= \alpha_1 A\cos(\omega_0 t) + \frac{\alpha_2 A^2}{2}(1+\cos(2\omega_0 t)) + \frac{\alpha_3 A^3}{4}(3\cos\omega_0 t + \cos(3\omega_0 t)) \\ &= \frac{\alpha_2 A^2}{2} + \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right)\cos(\omega_0 t) + \frac{\alpha_2 A^2}{2}\cos(2\omega_0 t) + \frac{\alpha_3 A^3}{4}\cos(3\omega_0 t) \end{aligned} \tag{1.5}$$

From (1.5) it is clear that the term associated with the fundamental, i.e. the gain of the system, doesn't only depend on coefficient α_1 but also on $3\alpha_3 A^2/4$, which can significantly change if the amplitude of the input signal A increases. If coefficients α_1 and α_3 have opposite sign (like in a MOS differential pair [1]) the term associated with third order distortion *compresses* the gain, giving rise to an input/output characteristic which bends for high values of A, as schematically reported in Figure 1.2. A typical metric that is used to quantify compression is 1dB-compression point, which corresponds to the input signal amplitude (often expressed in dBm) that causes a 1dB reduction in the gain.

Another compression effect arises if a strong undesired signal (called blocker) comes with the small desired one. If in (1.4) it is assumed $x(t) = A_0\cos(\omega_0 t) + A_1\cos(\omega_1 t)$,

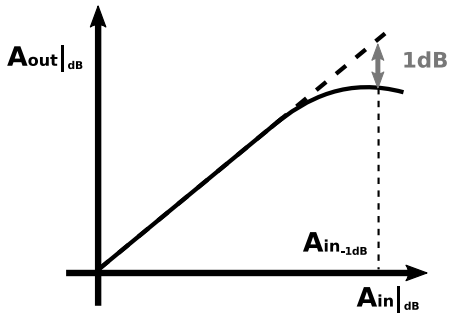


FIGURE 1.2: Schematic representation of gain compression in a non-linear system

the term associated with $\cos(\omega_0 t)$ becomes:

$$y(t) = \left(\alpha_1 + \frac{3}{4}\alpha_3 A_0^2 + \frac{3}{2}\alpha_3 A_1^2\right) A_0 \cos(\omega_0 t) + ... \tag{1.6}$$

From (1.6) it is clear that if the amplitude A_1 of the interferer increases, the gain of the desired signal ($A_0 \cos(\omega_0 t)$) drops. Called desensitization, this effect lowers the Receiver SNR and is particularly relevant when very large Out-of-Band (OOB) interferers are expected, as will be discussed in the following.

From the receiver point of view another mechanism still arising from non-linearity becomes particularly critical, i.e. third order intermodulation (IM3). This phenomenon arises when two tones at angular frequency ω_1 and ω_2 accompany the desired signal. If $x(t) = A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t)$ then $y(t)$ becomes:

$$\begin{aligned} y(t) = {} & \alpha_1(A_1 \cos\omega_1 t + A_2 \cos\omega_2 t) + \alpha_2(A_1 \cos\omega_1 t + A_2 \cos\omega_2 t)^2 + \\ & + \alpha_3(A_1 \cos\omega_1 t + A_2 \cos\omega_2 t)^3 \end{aligned} \tag{1.7}$$

which has components, associated with third order non-linearity, at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$:

$$\begin{aligned} y(t) = {} & ... + \frac{3\alpha_3 A_1^2 A_2}{4} \cos(2\omega_1 + \omega_2)t + \frac{3\alpha_3 A_1^2 A_2}{4} \cos(2\omega_1 - \omega_2)t + \\ & + \frac{3\alpha_3 A_1 A_2^2}{4} \cos(2\omega_2 + \omega_1)t + \frac{3\alpha_3 A_1 A_2^2}{4} \cos(2\omega_2 - \omega_1)t + ... \end{aligned} \tag{1.8}$$

Such mechanism is graphically explained in Figure 1.3, where it is shown that if the desired signal is at $\omega_0 = 2\omega_1 - \omega_2$, the IM product can fall onto the desired channel, degrading SNR. Receiver IM3 performance is evaluated through a two-tone test, where two sinusoids of equal amplitude A are applied to the input of the circuit and IM3 is observed at the output. IM3 performance could be quantified as the ratio of fundamental and IM3 components. However, from (1.8) it is clear that IM3 increases as A^3, meaning that the relative ratio between fundamental and IM3 raises as A^2. Since an amplitude-independent quantity is preferred, IM3 is usually quantified in terms of IIP3. Illustrated

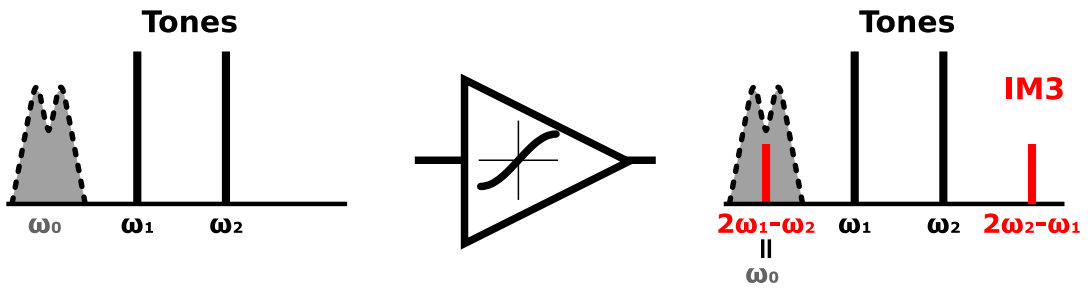


FIGURE 1.3: Schematic description of IM3 falling onto signal channel

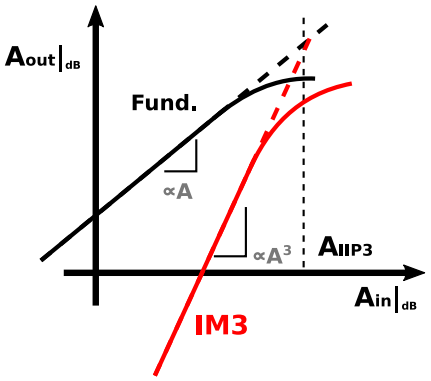


FIGURE 1.4: Behaviour of Fundamental and IM3 vs. input power on a *log-log* scale

in Figure 1.4, this metric represents the input amplitude level corresponding to the intersection between input referred fundamental and IM3. As shown in Figure 1.4, this quantity is independent on the amplitude of the two tones used for the test. At very larger power levels, however, higher order non-linearities may arise and the fundamental and IM3 slope deviate from their expected slope. As shown in Figure 1.4 intermodulation is then usually measured for lower input power levels and IIP3 is extrapolated following the slopes (1 and 3 in a *log-log* scale) of the fundamental and the IM3, resulting in (1.9):

$$A_{IIP3}|_{dBV} = A|_{dBV} + \frac{A|_{dBV} - A_{IM3}|_{dBV}}{2} \tag{1.9}$$

where $A_{IIP3}|_{dBV}$ is actual IIP3, $A|_{dBV}$ corresponds to $20 \cdot \log_{10} A$ and $A_{IM3}|_{dBV}$ is $20 \cdot \log_{10} A_{IM3}$, *referred to the input of the receiver*. The same formula applies with Fundamental and IM3 power expressed in dBm. Wireless standards typically specify a list of tests the receiver must comply with in terms of linearity. These specify the amplitude of possible interferers and their distance in frequency from the desired signal. Starting from this specs an interferers profile can be built and the receiver requirements in terms of Compression and IIP3 can be computed. Some detailed example will be provided in the following when describing in deeper detail the requirements for LTE standard.

1.2 Evolution of Cellular Networks

During the past three decades, wireless communications have continuously evolved to serve the ever increasing number of users and the growing demand for data services. From a system point of view, such evolution goes hand-in-hand with the need for increased data speed and higher capacity. Several factors contribute to satisfy these requirements. In this regard, it is instructive to consider Shannon's theorem, stating that the maximum achievable capacitance of a noisy channel is equal to [2]:

$$C = W \cdot \log_2 \left(1 + \frac{P}{N}\right) \tag{1.10}$$

where C represents the bit rate, W is the channel bandwidth, P is the average signal transmitted power and N is the noise power, assumed to have white power distribution. Looking at this relation, it is possible to point out the key factors that contribute to improve the achievable system capacity:

- **Bandwidth**: In (1.10) it can be observed that channel capacity (C) is tied to the Bandwidth (W) through a direct proportionality relation. As a result, the simplest way to increase data rate consists of extending the channel bandwidth. Following this approach, wireless networks have evolved in such a way to occupy multiple bands and to allocate increasing portion of spectrum to each user. As will be mentioned in the following most recent mobile systems also include the possibility of allocating different channels from the same or from different bands to a single user, according to the channel-aggregation paradigm. This enhances the maximum achievable data rate at the cost of an increased complexity;

- **Improved Modulation Schemes**: In order to maximize the peak data rate expressed by (1.10), spectrum occupation must be optimized. This is performed by assigning more bits per symbol, adopting higher order modulation schemes (e.g. 256QAM in LTE Rel 14). Denser constellations result, making it more challenging to detect each symbol in presence of interference and noise. Higher requirements in terms of SNR are then needed in the radio, making its design more challenging.

- **Multiple Antennas**: Another approach consists of multiplying the number of data-streams. Actually, one of the key technologies of recent wireless systems is Multiple-Input-Multiple-Output (MIMO), making use of multiple antennas both at the TX and the RX side. This involves sending more data-streams at the same time through the multiple antennas, multiplying the peak data rate correspondingly. The presence of multiple antennas enables also techniques like spatial diversity, which are implemented to improve reliability. MIMO comes with additional system

complexity, due to the multiple transmit and receive paths and to the additional operations which have to be performed in the digital domain to reconstruct the signal.

Wireless systems have evolved following the key points listed above. In the next part of this section a brief overview of the different wireless generations is shown, focusing in particular on the most recent LTE standard and on which evolutions are expected.

1.2.1 1G Generation

The first generation of mobile wireless network (1G) dates back to the beginning of 1980's. 1G networks were purely analog and they were mainly designed to provide voice services to mobile users. 1G was composed of different standards, which were developed for different geographical areas. For example, key access technologies were Advanced Mobile Phone Service (AMPS) in North America, Nordic Mobile Telephone (NMT) in Scandinavian countries and Total Access Communication System (TACS) in Western Europe. These standards were characterized by similar features. To give an example AMPS operated near the 850 MHz band, providing 832 30-kHz-spaced channels and used FM modulation [3]. Specifically AMPS used Frequency-Division-Duplexing (FDD), employing two separate frequency bands for transmitting and receiving. To solve the multiple access issue, 1G adopted Frequency Division Multiple Access (FDMA) scheme, assigning one channel per each user, suffering from poor capacity in crowded areas and requiring large frequency gaps between users to avoid interference. Other limitations affected this network generation, like weak hand-off reliability and security issues, but in spite of these 1G paved the way for successive generations and the widespread diffusion of mobile phones [3][4].

1.2.2 2G Generation

2G represents the second generation of mobile networks and it was introduced in the first 1990's. The most important breakthrough with respect to 1G was represented by the fact 2G was basically a digital technology. This improved voice capacity and enabled additional services like voice mails, mobile fax and Short Message Service (SMS). The main 2G access technology is represented by Global System for Mobile Communications (GSM). GSM was standardised by the European Communications Standard Institute (ETSI) as a unified cellular technology for European countries, becoming lately the most wide-spread cellular system in the world. GSM works over few different bands, which are summarised in Table 1.1, where frequency separation between RX and TX bands

GSM Band	TX-Band	RX-Band
GSM 450	450.4 MHz - 457.6 MHz	460.4 MHz - 467.6 MHz
GSM 480	478.8 MHz - 486 MHz	488.8 MHz - 496 MHz
GSM 850	824 MHz - 849 MHz	869 MHz - 894 MHz
GSM 900	876 MHz - 915 MHz	921 MHz - 960 MHz
DCS 1800	1710 MHz - 1785 MHz	1805 MHz - 1880 MHz
PCS 1900	1850 MHz - 1910 MHz	1930 MHz - 1990 MHz

TABLE 1.1: GSM operating bands

(FDD) is shown. GSM Channels are 200-kHz spaced and GMSK modulation scheme is used [5], reaching a peak data rate of 270 kb/s [3]. Time Division Multiple Access (TDMA) is used as a multiple-access method. TDMA is based on the allocation of the same channel to different users at different times. In comparison with the previous generation, the choice of TDMA and the increased channel bandwidth allowed multiple users to transmit on the same channel, enhancing system voice capacity and extending mobile services access to an increased number of users [6].

Further evolutions of the 2G networks are generally grouped in the so-called 2.5G generation. Such terminology indicates all those technologies which share the same radio interface with the GSM, while endowing additional features to improve the achievable data-rates and satisfy the increasing demand for mobile data services. One typical example is represented by General Packet Radio Service (GPRS). GPRS introduced packet switching, in contrast to GSM which was based on circuit switching. Instead of setting a dedicated channel (circuit) between users, when communication is established, packet switching splits data into blocks, called packets, which are transmitted across different paths trough the nodes of the network, limiting channel occupancy to the packet transmission duration. This makes packet switching more spectrally efficient and economically attractive, since the user can be charged only for the effective amount of transmitted information and not for the duration of the channel occupancy [3]. GPRS was able to make internet-type data services like web browsing available to the users, while extending the already existing services of GSM (e.g with point-to-multipoint calls). Another standard which was developed to overcome the data speed limitation of GSM and which is normally included in 2.5G is Enhanced Data Rates for GSM Evolution (EDGE). EDGE was developed with the aim of achieving increased data rates within the 200 kHz channel of GSM. To reach this goal EDGE introduced 8-PSK modulation, achieving a maximum theoretical speed of 473.6 kbit/s [7]. The tight proximity of points in the 8-PSK constellation requires however a higher SNR to detect signals with low BER, dictating for improved performance (lower noise) of the RX with respect to QPSK.

1.3 3G Generation

The foundation for the following generation of Mobile (3G) was established by the introduction of Code Division Multiple Access (CDMA) technique. Differently from FDMA and TDMA, in CDMA signals can overlap in frequency and time. However, a unique code is assigned to each TX-RX pair and every transmitted bit is multiplied by the assigned code before modulation. The same code is used at the receiver side to recover the original signal. Even if coding spreads the spectrum occupied by the transmitted signal (it is actually referred to as a "spread spectrum" technique), such multiple access scheme has the potential for improved system capacity, since several users can occupy the same spectrum. Two main competing standards were developed in the 3G framework, i.e. CDMA2000 and WCDMA (UMTS). As an example, the Universal Mobile Telecommunication System (UMTS) is characterised by 26 frequency bands operating in the range between 900 MHz and 2.1 GHz. Channel spacing is 5 MHz and the adopted modulation scheme is QPSK [8]. In its original implementation UMTS was capable of carrying data with speed up to 2 Mbps. Differently from GSM, which was implemented to provide voice service and included data services, UMTS is specifically optimised for data services, providing an increased number of users with internet-based broadband mobile services, like navigation and multimedia. Even if UMTS is basically an FDD system, it includes also some frequency bands operating in Time-Division Duplexing (TDD) scheme, transmitting and receiving on the same frequency band but in different time slots [9]. The increasing demand for internet access and data services pushed the development of an enhanced version of UMTS including High-Speed Packet Access (HSPA), which allowed reaching peak data rates of 14 Mbps [10].

1.4 4G LTE

1.4.1 LTE Overview

LTE stands for Long Term Evolution and is standardised by the Third Generation Partnership Project (3GPP). Its first official release (Rel 8) was frozen in 2008, with the goal of improving data capacity with respect to UMTS and satisfy the increasing demand for internet access and data services. In detail, the main goals of LTE are increasing user data rates, enhancing bit-rates at the cell-edge, improving spectral efficiency, guaranteeing greater flexibility in spectrum allocation and reducing power consumption for mobile devices. LTE has evolved in time going through LTE-Advanced (Release 10, 11 and 12) and LTE-Advanced-Pro (Release 13 and 14). To ensure seamless coverage, possibility of switching with other access technologies (like UMTS and GSM) is allowed

[11]. To enable its usage all around the world LTE is defined over a large number of frequency bands, making use of licensed frequencies from 700 MHz to 3.7 GHz and, starting from Release 14 also of unlicensed spectrum (5 GHz), introducing the so called licensed assisted access (LAA) concept. Frequency bands have increased over the years. In the recent Rel 14 they are numbered from 1 to 48 and from 65 to 70[12]. Bands from 1-32 and 65-70 are based on FDD duplexing, while the remaining ones operate in TDD. Following the same trend observed in former standards, LTE includes a larger channel bandwidth with respect to its prior generation. In particular, greater flexibility is provided by a variable carrier width, which can assume values of 1.4, 3, 5, 10 and 20 MHz [12]. This of course requires a higher reconfigurability for the receiver. Not all frequency bands support every possible channel bandwidth: for example band 1 works with channel bandwidths bigger or equal than 5 MHz while band 12 supports carriers with up to 10 MHz width. Pursuing increased data rates, LTE has to deal with issues related to multi-path transmission. In fact, when the symbol period starts approaching the time delay introduced by the channel, signal quality is likely to be degraded because of Inter-Symbol Interference (ISI). To overcome this issue LTE makes use of Orthogonal Frequency-Division Multiplexing (OFDM). In OFDM, the high-rate data stream is first converted from Serial to Parallel and N streams (having N-times lower data rate) are produced. These are then impressed on N different carrier frequencies, called sub-carriers. Total spectral occupation and data rate is unchanged with respect to a single-carrier modulation, but each of the N stream is now characterized by a lower bit-rate, allowing to tolerate a larger delay spread. Several modulation schemes are employed in LTE. In the original Rel 8 only QPSK and 16QAM were employed. In latest Releases these schemes were integrated with higher order modulation techniques, i.e. 64QAM and 256QAM. The adopted modulation changes depending on the signal quality. If a larger signal is detected (high SNR), higher order modulations are employed, while the system switches to lower-order QPSK in case the input signal is weak.

1.4.1.1 MIMO

To further increase achievable data-rate LTE makes use of multiple antennas in Base Station (BE) and User Equipment (UE), according to the Multiple-Input Multiple-Output (MIMO) approach. Three main advantages result from MIMO:

- **Spatial diversity gain**: Transmission over several antennas at which fading is sufficiently uncorrelated allows mitigating the multi-path fading effect. This allows improving signal quality but does not increase data rate;

- **Array gain**: Transmitted energy is concentrated in a well defined direction by controlling magnitude and phase of the signals fed to each antenna in the array (beam-forming). This makes also possible serving more users placed in different directions (Multi-User MIMO);
- **Spatial multiplexing gain**: Effective data-rate is increased by transmitting different data streams over different antennas using the same frequency and time resources, separating data streams at the receiver through different reference signals. This enables multiplying the effective data rate by the number of used antennas.

Primitive Release 8 LTE included 4x4 (4 Transmit and 4 Receive Antennas) MIMO mode in Downlink and 2x2 in Uplink, which allowed reaching 75 Mbps in Uplink and 300 Mbps in Downlink, thanks to spatial multiplexing and 20 MHz channel bandwidth. Evolved MIMO schemes were included in following releases, including 8x8 MIMO in Downlink and 4x4 in Uplink.

1.4.1.2 Carrier Aggregation

One of the main features introduced with LTE-Advanced to increase the signal bandwidth and link capacity is the possibility of grouping several carriers, implementing the so called Carrier Aggregation (CA). Each carrier, referred to as component carrier, can have one of the possible bandwidths specified in the original LTE release, guaranteeing backward compatibility with previous releases, allowing to reuse a significant part of the already developed technology and limiting costs.The maximum number of usable carriers is five, meaning that the maximum achievable bandwidth is 100 MHz. Several ways of aggregating are possible. The easiest one consists of grouping few contiguous carriers in the same band, in the so-called intra-band contiguous aggregation. If this is not possible, non-contiguous carriers can be chosen. They can belong to the same band (intra-band non-contiguous carrier aggregation) or even to different bands (inter-band carrier aggregation). The different available CA schemes are shown in Figure 1.5. Thanks to the combination of Carrier Aggregation and MIMO a peak data rate of 3 Gbps and 1.5 Gbps in Downlink and Uplink respectively are achievable in the latest LTE releases.

1.5 5G Generation

Most recent LTE releases have already started extending mobile services to new fields, like Industrial Internet of Things (IoT) and automotive Vehicle to Everything (V2X)

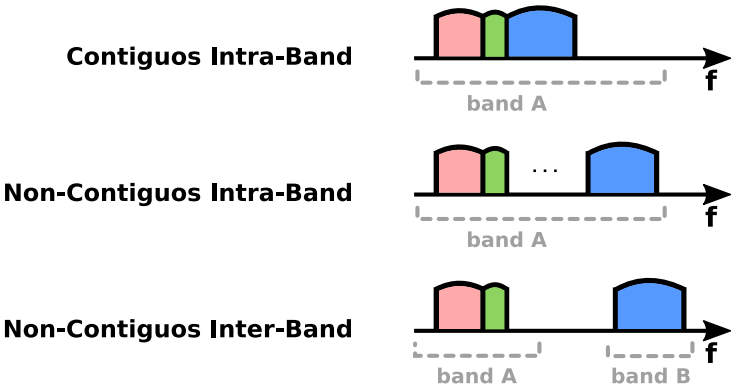


FIGURE 1.5: Carrier Aggregation schemes: Contiguous Intra-Band, Non-Contiguous Intra-Band and Non-Contiguous Inter-Band

communication. Next mobile generation (5G) is expected to further extend the range of available services, for example with Augmented Reality, digital TV, public safety and Drone Communications [13]. In June 2018 3GPP approved the completion of Rel 15, representing the first 5G specification standard, giving birth to the the so-called Phase 1 of 5G. This initial step in 5G represents a natural evolution of 4G and is thought to be used in strict co-operation with the existing technology. Following the same trend already highlighted in the previous section, Rel 15 introduces additional frequency bands covering the frequency range below 6 GHz, referred to as FR1 (or Sub-6-GHz radio) by 3GPP [14]. Frequency bands are further classified into FDD bands, TDD bands, Supplementary Downlink/Uplink Bands (SDL/SUL). The usable carrier bandwidths of 4G are widened, enlarging the available channels with 25, 30, 40, 50, 60, 80, 90 and 100 MHz carriers. In the last section of this chapter, some specifications for Release 15 will be presented as an example.

1.6 Future Developments

5G also includes a second set of available frequency bands, referred to as FR2 in [14], which has not been standardized yet and that is expected to be released by 2020. This portion of spectrum will be exploited in the Phase 2 of 5G and will cover the mm-Wave frequency range above 28 GHz. This is going to be one of the most revolutionary aspects of 5G, allowing to use a larger range of frequencies, offering regions with wide availability of spectrum. Following the same exponential growth of 1G-2G-3G and 4G, carrier bandwidths in the order of 1 GHz are very likely to be made available in Phase 2 (Figure 1.6), rising the peak data rate up to several tens of Gbps. One drawback of mm-Wave signals is the high propagation loss they suffer when traveling through obstacles like buildings. Due to this kind of limitations mm-Wave 5G is expected to

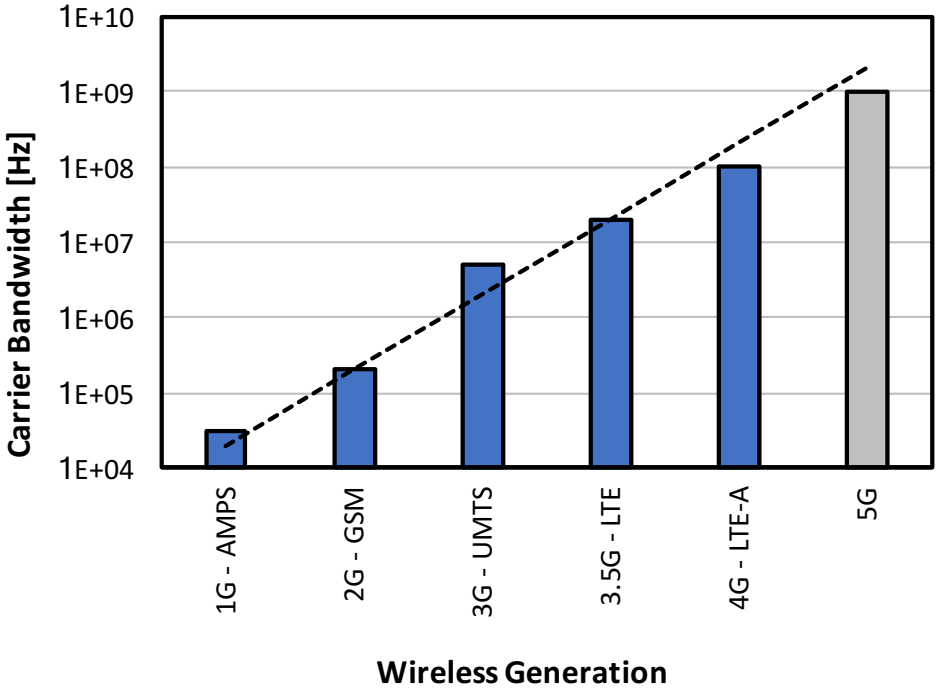


FIGURE 1.6: Channel Bandwidth vs. Wireless Generation

observe a strong cell densification process and to operate over an increased number of smaller cells [15]. Leveraging increased operation frequency and consequent antenna size reduction, an increased number of transmit and receive antenna elements (more than 16) is expected to be squeezed in a smaller space, exacerbating the trend already observed in 4G with MIMO and leading to the concept of massive-MIMO. This will also allow implementing directional beam-forming, allowing antennas to steer energy in a well defined direction, optimizing spectral efficiency (since more frequency re-use is allowed) and mitigating the issue of path loss. Another feature that is expected to be implemented in Phase 2 of 5G is the introduction of Full-Duplex. This corresponds to a Duplex scheme where the signal is transmitted and received at the same time on the same frequency band. Of course such technique is promising for doubled capacitance and better spectrum efficiency, but poses serious issues related to Self-Interference.

1.7 Example requirements

I this section some of the main requirements specified by mobile standards are presented and some quantitative examples are reported from the most recent release. Particular attention is devoted to those aspects which are relevant to the design of an RF receiver for

User Equipment (UE), i.e. those inherent to noise and non-linearity. These constraints will be is of interest for the following part of this work.

1.7.1 Sensitivity

Wireless standards specify a reference sensitivity power level (REFSENS) which, if applied at each of the two (or four) antenna ports, must guarantee a throughput that meets the indicated requirements for the assumed modulation and coding scheme (MCS), also called reference channel. Although it supports a plethora of MCSs, RF specifications are just given for a few of them, in order to reduce the number of required tests. For example, in Rel 15 specs are given for the low SNR reference channels adopting QPSK modulation with a code rate of 1/3. In this condition sensitivity is required to guarantee a throughput which is 95% of the maximum possible, corresponding to a required SNR of -1dB [11]. Sensitivity is specified by the standard for each band and for each allowed carrier bandwidth. The complete list is not reported here for lack of space, but as an example Band 1 is considered. For this band, $REFSENS = -100dBm$ for the 5-MHz channel and $REFSENS = -94dBm$ for the 20-MHz BW are specified. This value can be substituted in (1.1) to extract the required NF. Equation (1.11) results:

$$\begin{aligned} REFSENS = -94dBm = \\ = -174\left[\frac{dBm}{Hz}\right] + 10\log_{10}(20MHz) + NF|_{dB} + (-1) + IM|_{dB} - 3 \end{aligned} \tag{1.11}$$

IM is the so-called Implementation Margin, which is included to take into account all possible implementation non-idealities that can affect signal processing before the demodulator and that is assumed to be 2.5 dB in this testing conditions. The -3 dB term in (1.11) represents the diversity gain, which takes advantage of the fact the test is performed with two antennas, relaxing the required NF of the receiver. It results that the NF specification to fulfil this test is 8.5 dB.

1.7.2 Selectivity and Blocking Specs

Selectivity quantifies the ability of a receiver to detect the desired signal at the desired frequency in the presence of an interferer in adjacent channels or beyond, without causing excessive signal degradation. In particular, Adjacent Channel Selectivity (ACS) measures the receiver capability to properly operate in presence of an interferer in the adjacent channel.Two tests are specified for ACS. The first one is for a small adjacent interferer (Case 1). In Rel 15 this test is different for bands below 2.7 GHz and for

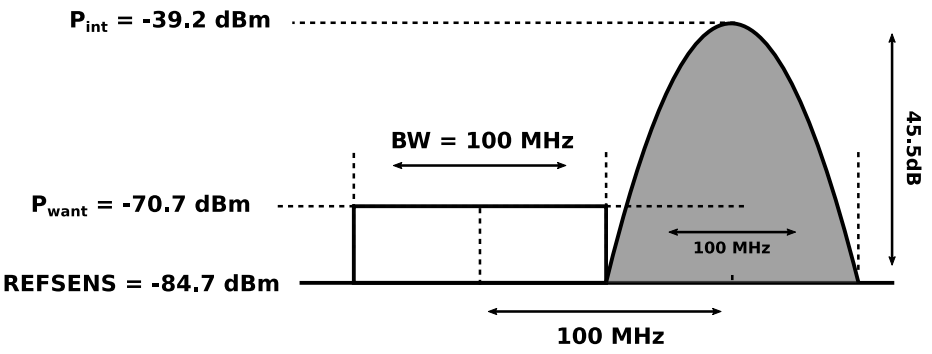


FIGURE 1.7: Case 1 for ACS Test with a 100-MHz channel BW

bands above 3.3 GHz. In both cases the desired signal is set to 14 dB above REFSENS level and the interferer has an amplitude which changes with the carrier bandwidth. In the low frequency bands the interferer is 5-MHz-BW modulated signal, while for the high frequency portion the interferer has the same BW of the signal. An example is reported in Figure 1.7 for a 100-MHz signal lying in the high frequency spectrum, which must be tested with a 100-MHz-BW interferer at REFSENS + 45.5 dB. Case 2 is for larger adjacent channel interferers. Interferer BW is the same as for Case 1 and its level is set to -25 dBm. Signal power changes according to RF band and of channel width. For example, for a 100-MHz channel in a RF band above 3.3 GHz, signal is at -56.5 dBm. In Narrow Band Blocking test, receiver performance is assessed in presence of a non-modulated Continuous-Wave (CW) signal at a small offset from the desired signal, typically less than the normal channel spacing. For Rel 15, this test must be performed with a CW blocker at -55 dBm power level while the desired signal level and blocker spacing depend on the channel BW. In the example of a 20-MHz-channel, the signal is 16 dB above REFSENS and blocker is at 10.2075 MHz offset. In-Band Blocking measures the receiver's ability to detect a wanted signal when an interfering signal falls into the receive band or into the 15 MHz above or below the band edge. The interfering signal is modulated and occupies the same BW as specified for ACS. Two requirements need to be met, the first one with an interferer of -56dBm in the second adjacent channel or further; the second with an interferer at -44 dBm in the third adjacent channel or larger frequency, up to 15MHz above the band edge. In this test the wanted signal is 9 dB above REFSENS for the 20 MHz BW. This is graphically exemplified inFigure 1.8. Out-of-Band Blocking test proves receiver capability of withstanding interferers lying more than 15 MHz above the RF-band edge. The wanted signal is set at the same level as for In-Band test. Interferer is a CW signal and it has a specified power P_{int} depending on its frequency offset from the band-edge. Three interferer frequency ranges are defined, as reported in Figure 1.8. P_{int} is -44 dBm from 15 MHz to 60 MHz offset from the band-edge, -30 dBm from 60 to 85 MHz and -15 dBm above 85 MHz. Also

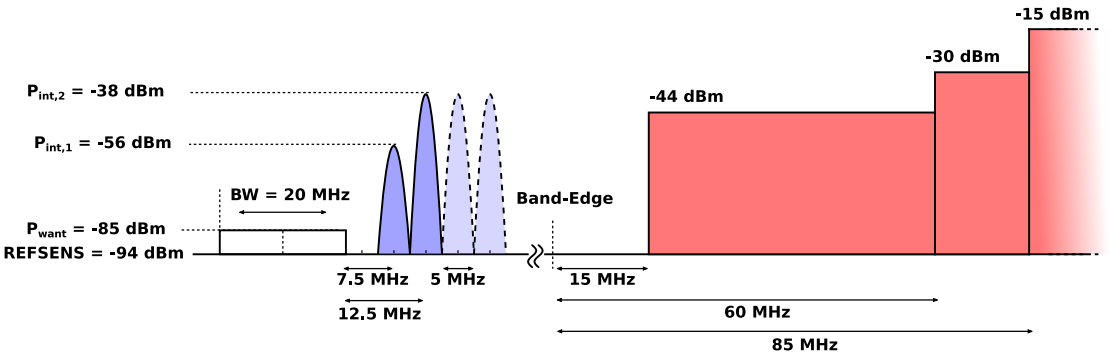


FIGURE 1.8: In-Band and Out-Of-Band Blocking Test for 20-MHz channel BW

explicit requirements in terms of intermodulation are given by Rel 15. To test IM3, a CW interferer and a modulated one have to be applied to the receiver, without degrading its performance beyond a certain extent (95% of maximum throughput must be achievable). Signal and interferers power are also in this test specified depending on the RF band and on the channel bandwidth. As an example for a 100-MHz channel in a frequency band below 2.7 GHz the test has to be performed with a -46 dBm CW signal at 7.5 MHz offset from the channel-edge and with another -46 dBm 5-MHz-BW modulated interferer at twice the frequency of the CW interferer. It is interesting in this regard to compute the necessary IIP3 to satisfy the spec. Signal is specified to be 16 dB above REFSENS for this test, which means the noise floor can be raised by the same amount to maintain a constant SNR. In band 41 for example, receiver reference sensitivity is -84.7 dBm. If we assume receiver was designed to barely satisfy sensitivity spec and SNR is 1.5 dB, it means noise floor is -86.2 dBm. To maintain overall noise and intermodulation combination below 16 dB, IM3 power must be at most -70.3 dBm. Equation (1.9) can be used to compute required IIP3:

$$\begin{aligned} IIP3_{min} &= P_{int} + \frac{P_{int} - P_{IM3}}{2} \\ &= -46dBm + \frac{-46dBm - (-70.3dBm)}{2} = -33.8dBm \end{aligned} \tag{1.12}$$

In most modern receivers this value is not particularly critical to be met. In the following chapter another situation where IIP3 requirement becomes much more stringent will be described and a possible solution will be presented.

1.8 Conclusions

In this Chapter a description of networks for mobile communication was done, together with an overview of the main requirements they mandate on the receiver. At this point it

should be clear that the general trend of mobile networks goes towards increased speeds, increased number of bands, multiplicity of antennas and extended carrier bandwidths. The presence of multiple operative bands and antennas makes it highly desirable to implement receivers which are able to operate over several bands, requiring to remove external RF filters and duplexers. This imposes important challenges on the design of the receiver, making requirements more stringent, especially from the linearity point of view. Together with the need for increased bandwidths, this reflects on a tougher design of the baseband portion of the RX, especially of its first block, which is in most cases a Trans-Impedance Amplifier (TIA). In the next chapter this point will be addressed in deeper detail and a possible TIA design will be presented.

Chapter 2

Highly Linear TIA for SAW-Less FDD Receivers

The design of analog baseband TIAs for cellular communications proves to be very difficult in recent standards, which endow increased channel bandwidths. Additional issues arise from the attempt of removing external SAW filters (to obtain a wide-band receiver), since the lack of external filtering let very strong blockers reach the baseband portion of the receiver basically unattenuated. The situation gets even more critical in Frequency-Division-Duplexing (FDD) systems where the removal of the external duplexer enhances the issue of TX signal Self-Interference (SI). Even in presence of SI Cancellation this situation requires the implementation of a very linear baseband (TIA) which must be capable of handling strong Out-of-Band blockers. In this chapter a possible implementation is proposed. The solution shown here is based on an Operational Trans-Conductance Amplifier (OTA) in closed-loop configuration, exploiting both forward and feedback passive components to achieve loop stability, instead of a more traditional Miller-Compensation. This solution is demonstrated to keep virtual-ground impedance low up to very high frequency, with benefit for linearity. Furthermore, the smaller adopted shunt capacitance guarantees low OTA noise in the TIA band. Measurements results are shown on a prototype demonstrating good performance in comparison with the State-of-The-Art. Most of the material reported in this chapter is reused from [16] (©2018 IEEE), in agreement with IEEE copyright policy on theses and dissertations.

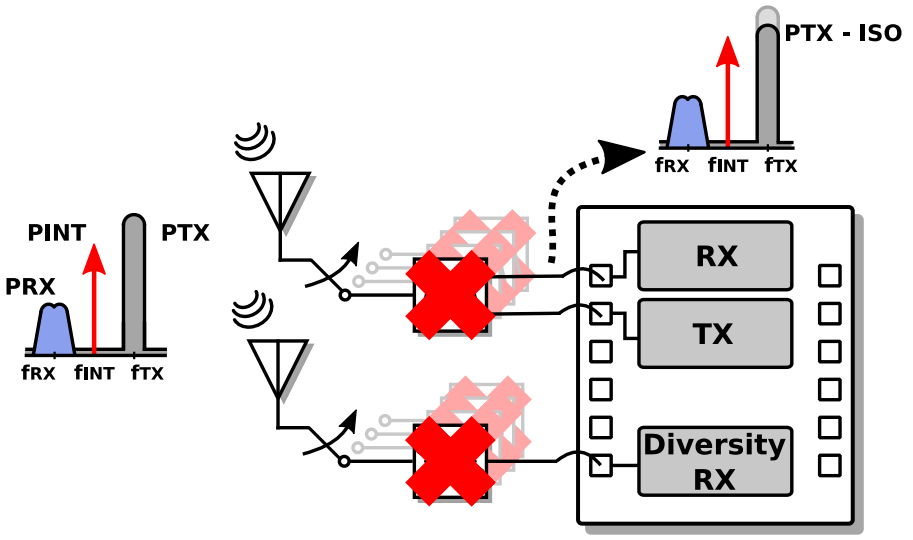


FIGURE 2.1: Schematic representation of a SAW-Less chipset

2.1 SAW-Less Receivers

In the previous chapter, some specifications were derived for a generic LTE/5G receiver (RX). Traditional IC RXs are designed assuming the presence of Surface Acoustic Wave (SAW) off-chip filters which attenuate Out-of-Band (OOB) blockers, significantly relaxing linearity performance of the RX itself. In Frequency-Division-Duplexing (FDD) systems SAWs are also used as Duplexers, connecting TX and RX to the antenna in a frequency-selective way. However, such filters entail a lot of issues, like high cost and area occupation. Furthermore, they have poor tunability, covering a limited number of bands. These aspects mean that as the number of frequency bands and antennas (MIMO) grows, these elements are likely to dominate area and cost of mobile platforms. A wide-band RX solution which is capable of working without external SAW filters, i.e. a SAW-Less RX, becomes then highly desirable. This entails however the need for improved RX linearity performance, since strong OOB blockers reach the front-end unattenuated, as schematically reported in Figure 2.1. Moreover in FDD systems a strong TX signal couples to the RX, due to the lack of isolation usually performed by the Duplexer. Several solutions have been proposed to implement Self-Interference-Cancellation (SIC) and relax linearity requirements for a SAW-Less RX [17–20]. Even if some degree of cancellation has been achieved, RX requirements remain stringent, as will be shown in the following.

2.1.1 SAW-Less RX Linearity Requirements

Some quantitative evaluation of the required SAW-Less RX linearity is performed relying on Rel 15 specs [14]. In the previous chapter it was shown that the User Equipment (UE) is required to operate also in presence of a strong OOB Continuous Wave signal. In FDD systems reduced TX-RX isolation can make such requirement much more challenging. Inter-Modulation (IM3) between the strong modulated TX signal coupling to the RX antenna and the CW blocker can in fact fall into the desired signal band, potentially degrading SNR. This situation is more critical for FDD bands which have small duplex separation, i.e. those bands where TX and RX signals are close. When performing OOB blocking test 3GPP specifies that, in case the desired channel bandwidth is 20 MHz, the wanted signal is assumed to be 9 dB above Reference Sensitivity [14], meaning that IM3 is allowed to rise the noise floor by the same quantity. This translates in a maximum Intermodulation power 8.4 dB above the noise floor. In this test the desired signal is assumed to be QPSK modulated, with a code ratio of 1/3, which requires SNR to be at least -1dB to achieve more than 95% of the maximum achievable throughput, as specified by the standard [14]. Some Implementation Margin (IM) is included here to account for non-idealities in the demodulator, so an SNR which is 2.5 dB higher than the minimum is targeted, resulting in $SNR = 1.5dB$. Intermodulation is then computed as in (2.1):

$$P_{IM,max} = P_{ref,sens} - 1.5dB + 8.4dB \tag{2.1}$$

where $P_{ref,sens}$ is the reference sensitivity specified by the standard expressed in *dBm*. If reference sensitivity is -94 dBm like in Band 1, maximum $P_{IM,max}$ results = *-87.1 dBm*. IIP3 specification can then be extracted as in (2.2):

$$IIP3_{min} = \frac{P_{CW} + 2(P_{TX} - ISO) - P_{IM,max}}{2} \tag{2.2}$$

where P_{CW} is the amplitude of CW blocker, P_{TX} is the TX average power, ISO is the effective isolation between TX and RX expressed in dB and $P_{IM,max}$ is expressed as in (2.1). Under the assumption that $P_{CW} = -15dBm$, $P_{TX} = +23dBm$ (as specified by the standard [14]) and $ISO = 15dB$, it results that the minimum required IIP3 equals +44dBm, an extremely difficult value to achieve in an actual receiver. Additional SIC is then required. In this regard, it is interesting to observe which is the minimum reference sensitivity level that can be obtained as a function of the RX IIP3, for different ISO levels. Plot in Figure 2.2 is obtained assuming $P_{CW} = -15dBm$, $P_{TX} = +23dBm$ and $NF = 8.5dB$. Even if some SIC technique is implemented, RX linearity requirement remain stringent. Assuming for example 20 dB of TX SIC is achieved (Total ISO = 35dB), required IIP3 is still +24 dBm.

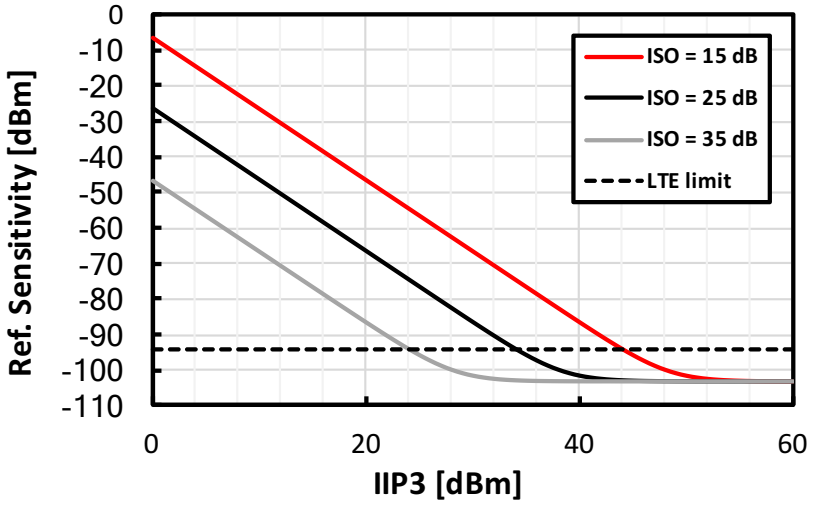


FIGURE 2.2: Achievable Reference Sensitivity vs. RX IIP3

2.2 Baseband Filter Requirements

In the design of a highly linear Receiver for SAW-Less FDD application, baseband portion deserves particular consideration. *For the universally used current-mode receiver architecture [21], the first block after the passive mixer is either a filtering trans-impedance amplifier (TIA) or a higher order filter [21–26]. In both cases, very stringent requirements are placed on this circuit (cit.[16] ©2018 IEEE).* First of all, OOB linearity of the TIA must be good enough not to limit RX IIP3, which was estimated in the previous section. In addition, baseband must guarantee low input impedance (Z_{in}) up to very high frequency, not to degrade linearity of the RX front-end. Typical TIA implementations are based on closed-loop Operational Transconductance Amplifier (OTA). Since in traditional OTA design stability is achieved through Miller-Compensation, Z_{in} tends to increase at high frequency due to the limited OTA bandwidth. This issue is typically counteracted by putting a big shunt capacitor connected at the TIA virtual ground node, providing low impedance path for high frequency components, as shown in Figure 2.3. *This serves several purposes:*

1. *It shunts the signal at the clock harmonics;*
2. *It maintains low input impedance across frequency to preserve both mixer IIP2 and IIP3 with strong OOB interferers [27];*
3. *It filters the higher frequency down converted interferers, improving TIA OOB IIP3.(cit.[16] ©2018 IEEE)*

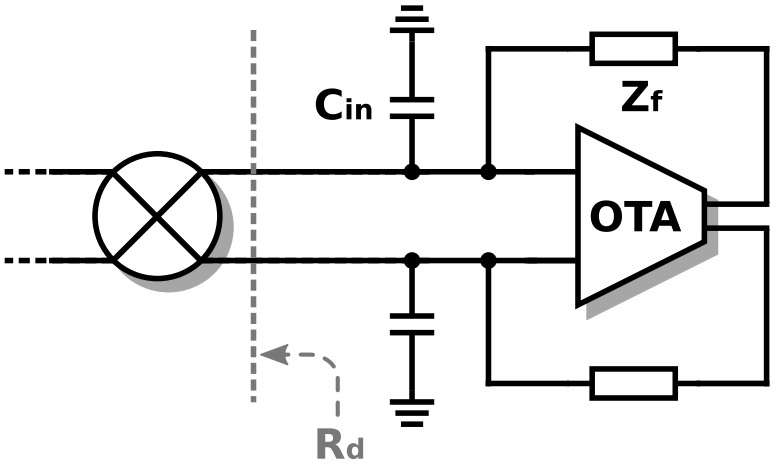


FIGURE 2.3: Closed Loop TIA with big input capacitance. Reused from [16] ©2018 IEEE

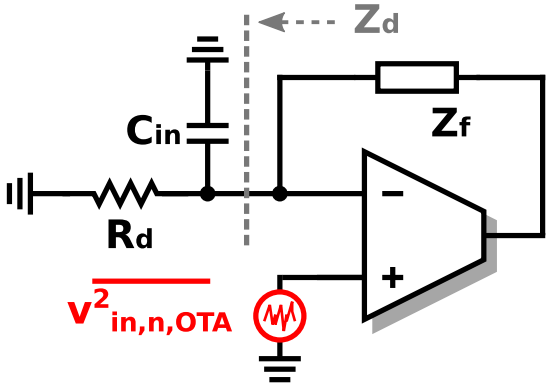


FIGURE 2.4: Single-ended TIA representation used for OTA NTF calculation

.Such capacitor can be in the order of hundreds of pF, like in [23] and [25]. Beside increasing area occupation, such a big capacitor can also introduce noise penalty. In fact, considering Input-Referred OTA noise voltage, it can be easily inferred from Figure 2.4 that its Noise Transfer Function (NTF) to the TIA output is equal to

$$NTF = \frac{\overline{v_{o,n,OTA}^2}}{\overline{v_{in,n,OTA}^2}} = \left|1 + \frac{Z_f}{Z_d}\right|^2 \tag{2.3}$$

where Z_f is the TIA feedback impedance and Z_d represents its driving impedance, given by the parallel of C_{in} and R_d in Figure 2.4. From (2.3) it can be obtained that, assuming $Z_f = R_f||C_f$, it follows:

$$NTF = \left|\frac{R_d + R_f}{R_d}\right|^2 \frac{\left|1 + \frac{sR_dR_fC_{in}}{R_d+R_f}\right|^2}{|1 + sR_fC_f|^2} \tag{2.4}$$

From (2.4) it is clear that NTF of OTA shows a zero at angular frequency $\omega_z =$

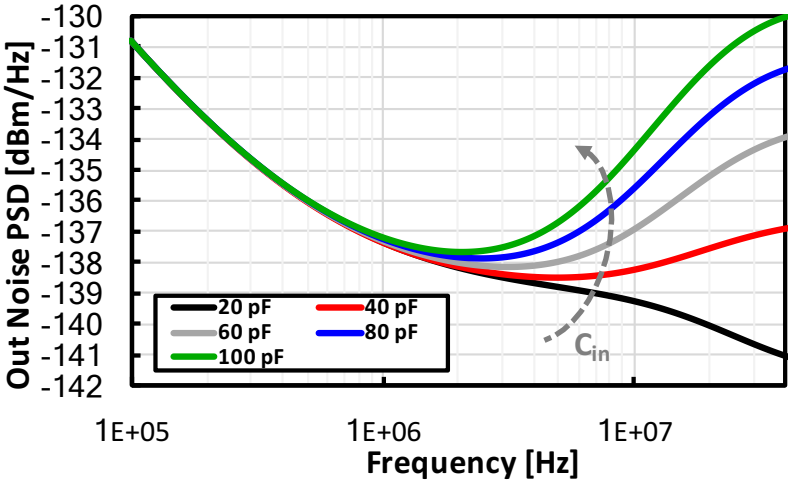


FIGURE 2.5: Output TIA noise Power Spectral Density (PSD) vs. C_{in}

$1/(C_{in}(R_d||R_f))$, which becomes $\omega_z \simeq 1/(C_{in}R_d)$ in case $R_f \gg R_d$. ω_z shifts to lower frequencies as C_{in} goes up, potentially degrading in-band noise of the TIA. This situation is depicted in a graphical way in the plot of Figure 2.5, where simulated output noise of the TIA described later in this chapter is reported for different values of C_{in}. If we assume for example that $R_d = 500\Omega$ and that cut-off frequency ω_0 of the TIA is 15 MHz, a 20-pF C_{in} produces a zero in NTF at $\omega_z = \omega_0$ and integrated OTA noise increases by 1.2 dB. *Beyond this value, however, the integrated noise increases with the square of C_{in}, quickly becoming unacceptable (cit.[16] ©2018 IEEE).*

It becomes then necessary to find an optimum value for the input capacitance C_{in}. *With respect to point 1 above, we see that the impedance of a 20 pF C_{in} is significantly smaller than the switches on-resistance R_{ON} (typically about 20 Ω) even at the lowest possible harmonic of the local oscillator (LO). (cit.[16] ©2018 IEEE).* In fact, assuming f_{LO} is 2 GHz, C_{in} shows 2Ω impedance at $2f_{LO}$. *Therefore, from this point of view, we have no reason to increase C_{in} beyond 20 pF. With respect to point 2 above, we need to ensure that the TIA input impedance Z_{in} remains below f_{LO} up to the highest blocker frequency (cit.[16] ©2018 IEEE)*, which in the following will be assumed to be at 400 MHz, which is reasonable for an LTE FDD transceiver. Input impedance Z_{in} can be expressed as the parallel of C_{in} and the impedance seen looking into the virtual ground node of the TIA (Z_{VG}). Since 20 pF is 20Ω at 400 MHz, either a bigger input capacitance (with noise penalty) or an OTA with large gain up to the blocker frequency are needed to fulfil the requirement on Z_{in}. With reference to point 3 above, if a broadband OTA solution is chosen, virtual ground impedance Z_{VG} becomes smaller than C_{in}, and a significant portion of the blocker current is absorbed by the OTA, which becomes critical from the IIP3 point of view.

In the literature, many continuous-time filters with a bandwidth of up to ten megahertz are presented [28–35]. Although some have good dynamic range (DR) [31], they do not always address all the specs of a BB channel filter, e.g. low input impedance. In [36] and [37], a receiver BB TIA is enhanced by placing a negative resistance in parallel with its input nodes. In [37], this is exploited to significantly improve the IB IIP3, but with small benefits on the OOB IIP3 and at the cost of extra noise and power consumption. Lower noise is achieved in a TIA [29] that uses a smaller input capacitance by boosting its value for OOB signals. Furthermore, a second-order filtering is implemented, which is beneficial for the following stages. However, its relatively high input impedance may degrade the mixer linearity (cit. [16] ©2018 IEEE).

2.3 TIA design

In order to extend the OTA bandwidth and achieve low TIA input impedance over a broad bandwidth with 20-pF C_{in}, an unconventional approach was adopted to ensure loop stability. In traditional general-purpose OTA design, where purely capacitive load is assumed, Miller compensation schemes are often used. Miller capacitors create one dominant pole in the OTA transfer function and push non-dominant poles above the unity gain bandwidth (GBW), increasing phase margin and guaranteeing OTA stability (cit. [16] ©2018 IEEE). In the design of BB TIAs this approach has the drawback of introducing a low frequency pole in the OTA transfer function. This pole limits the achievable GBW to about half the frequency of the non-dominant pole, which is given by the ratio between the g_m of the last stage of the OTA and the effective load capacitance C_{in}. *To gain a quantitative insight, targeting a GBW of 1.6 GHz with a 20-pF load capacitance would require an unpractically high transconductance of 400 mS (cit. [16] ©2018 IEEE)* for the last OTA stage. At the same time the low frequency dominant pole in the OTA gain A is responsible for a quick increase in the virtual ground impedance Z_{VG} of the TIA. In first approximation, according to Miller theorem, Z_{VG} can be expressed as:

$$Z_{VG} = \frac{Z_f}{1 + A(s)} \simeq \frac{Z_f}{A(s)} \tag{2.5}$$

where Z_f is the TIA feedback impedance and A(s) is the OTA voltage gain. From (2.5) it is clear that if gain drops Z_{VG} increases correspondingly.

In the proposed TIA design no Miller capacitors are used in the OTA. Stability is instead achieved by placing some additional zeros in the loop gain transfer function, both in the OTA forward path and in the feedback network. Putting such zeros close to GBW, a large Gloop is obtained over a broad frequency range. Gloop drops steeply for high frequency and recovers its 20 dB/decade slope close to the GBW, exploiting the

concept of conditional stability [38]. *This approach allows achieving much wider OTA bandwidth than a Miller compensation (cit. [16] ©2018 IEEE), as will be described in detail in the following.*

2.3.1 OTA design

In order to achieve high dc gain and maintain low in-band input impedance, the OTA is designed as a Three-Stage-OTA, whose detailed schematic is shown in Figure 2.6 and whose design parameters are listed in Table 2.1. The first stage consists of a PMOS Telescopic Cascode. Resistor R_c and capacitor C_c are introduced to provide an output impedance for this stage equal to:

$$Z_{O,1} = r_{out,1} // \frac{1}{j\omega C_{L,1}} // \frac{(1 + j\omega R_c C_c)}{j\omega C_c (1 + G_{m,L} R_c)} \tag{2.6}$$

where $r_{out,1}$ is the low-frequency output impedance of the Telescopic Cascode Stage, $C_{L,1}$ is the total capacitance loading the output node of this stage and $G_{m,L}$ is the equivalent trans-conductance of the load transistors $M_{3/4}$ degenerated by R_{deg}. The third term in (2.6), associated with R_c and C_c, is equivalent to the series combination of a capacitance $C_c(1 + G_{m,L}R_c)$ and a resistance $R_c/(1 + G_{m,L}R_c)$. The frequency shape of output impedance $Z_{O,1}$ is schematically reported in the insert of Figure 2.6. $Z_{O,1}(\omega)$ shows a low-frequency pole at:

$$\omega_{p,OTA,1} = \frac{1}{C_c(1 + G_{m,L}R_c) \cdot r_{out,1}} \tag{2.7}$$

and a high frequency zero at:

$$\omega_{z,OTA,1} = \frac{1}{R_c C_c} \tag{2.8}$$

$\omega_{z,OTA,1}$ is placed close to the TIA GBW to improve phase margin. At very high frequency, load capacitance $C_{L,1}$ produces another pole at frequency:

$$\omega_{p,OTA,2} \simeq \frac{G_{m,L}}{C_{L,1}} \tag{2.9}$$

The frequency behaviour of output impedance $Z_{O,1}$ can be explained intuitively. At low frequency C_c is an open-circuit and $Z_{O,1}$ is the output impedance of basic Telescopic Cascode. For high frequency, instead, capacitance C_c becomes a short and $Z_{O,1}$ reduces, becoming equal to the impedance provided by the diode connected transistor $M_{3/4}$ (degenerated by R_{deg}), i.e. $1/G_{m,L}$. This gives rise to the pole-zero highlighted before. For extremely high frequency $Z_{O,1}$ starts being dominated by the capacitive load of the following stage, introducing the high frequency pole ($\omega_{p,OTA,2}$). The output CM voltage of the first stage is set by the local feedback made of $R_{b,1}$ at low frequency and, at high

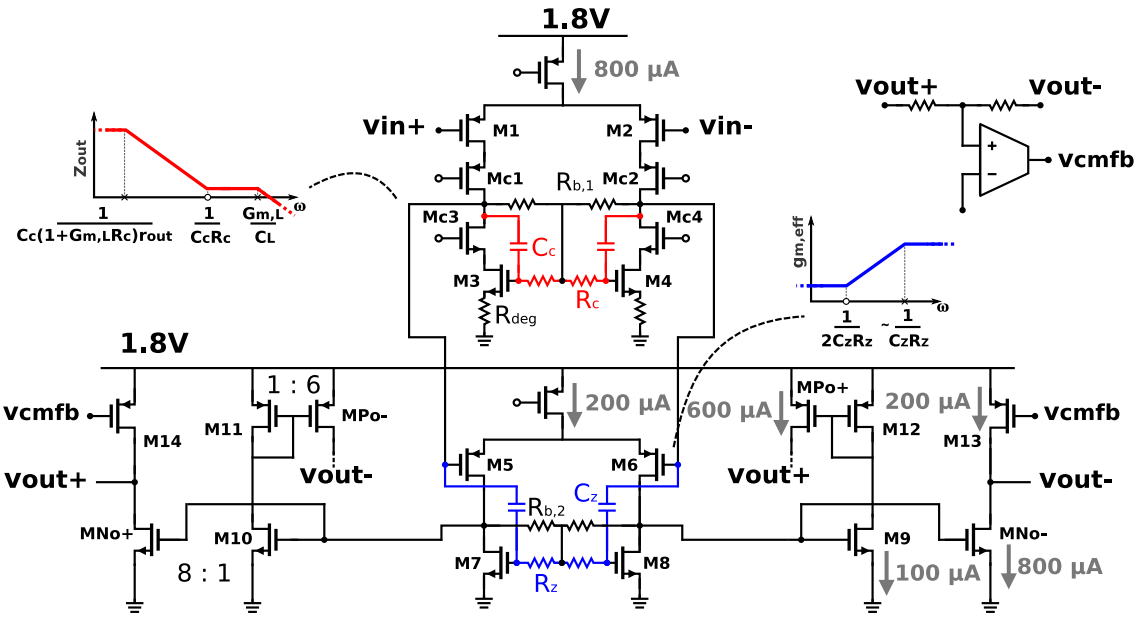


FIGURE 2.6: Detailed OTA schematic

Parameter	Value	Unit
$M_{1/2}$	140/0.08	$\mu m/\mu m$
$M_{c,1/2}$	20/0.04	$\mu m/\mu m$
$M_{c,3/4}$	8/0,04	$\mu m/\mu m$
$M_{3/4}$	20/0.2	$\mu m/\mu m$
$M_{5/6}$	20/0.06	$\mu m/\mu m$
$M_{7/8/9/10}$	2/0.08	$\mu m/\mu m$
$M_{11/12}$	6/0.08	$\mu m/\mu m$
$MPo+/Po-$	36/0.08	$\mu m/\mu m$
$MNo+/No-$	16/0.08	$\mu m/\mu m$
$M_{13/14}$	12/0.08	$\mu m/\mu m$
C_c	300	fF
R_c	500	Ω
R_{deg}	250	Ω
R_z	1	$k\Omega$
C_z	100	fF

TABLE 2.1: Design parameters for the proposed OTA

frequency, by capacitor C_c. Resistor $R_{b,1}$ is sized to be much bigger than $r_{out,1}$, so as not to affect the low frequency gain.

The second stage is a simple PMOS differential pair, which is designed to be low-power and to have large bandwidth. This is achieved through the network made of R_z and C_z. As schematically reported in Figure 2.6 this network boosts the effective g_m of this stage introducing a zero-pole doublet at frequency:

$$\omega_{z,OTA,2} = \frac{1}{R_z C_z (1 + \frac{g_{m,7/8}}{g_{m,5/6}})} \tag{2.10}$$

and

$$\omega_{p,OTA,3} = \frac{1}{R_z C_z} \tag{2.11}$$

This can be understood intuitively observing that above $\omega_{p,OTA,3}$, capacitance C_z shorts the gate of transistors $M_{5/6}$ and $M_{7/8}$, approximately doubling the equivalent g_m of the stage, assuming $g_{m,5/6}$ and $g_{m,7/8}$ are equal. Also one additional pole is produced at the output of this stage, i.e.

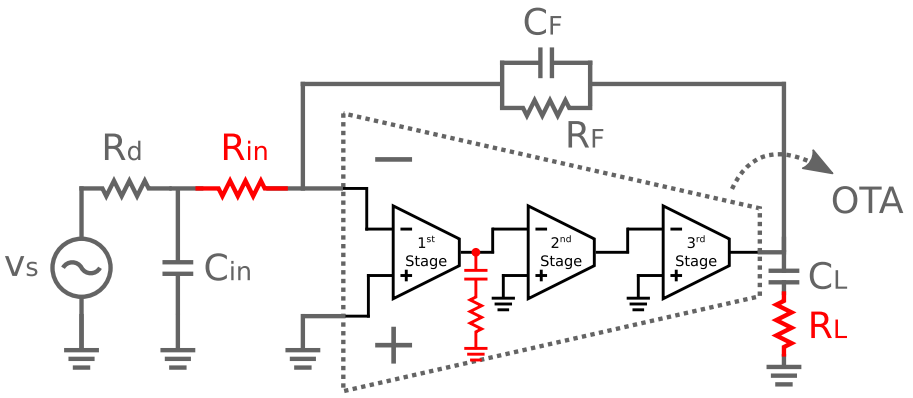
$$\omega_{p,OTA,4} = \frac{1}{r_{o,2} C_{L,2}} \tag{2.12}$$

where $r_{o,2}$ and $C_{L,2}$ are output resistance and total load capacitance of the stage, respectively. This pole, however, is cancelled by sizing R_z and C_z in such a way to have $\omega_{z,OTA,2} = \omega_{p,OTA,4}$. In this way the stage shows a single pole at $\omega_{p,OTA,3}$. In a similar way as for the input stage, also in the second stage CM is set through resistors $R_{b,2}$. Notice that $R_{b,2}$ makes $M_{7/8}$ appear as diode connected transistors for the bias current, so that through this connection also the output stage is biased.

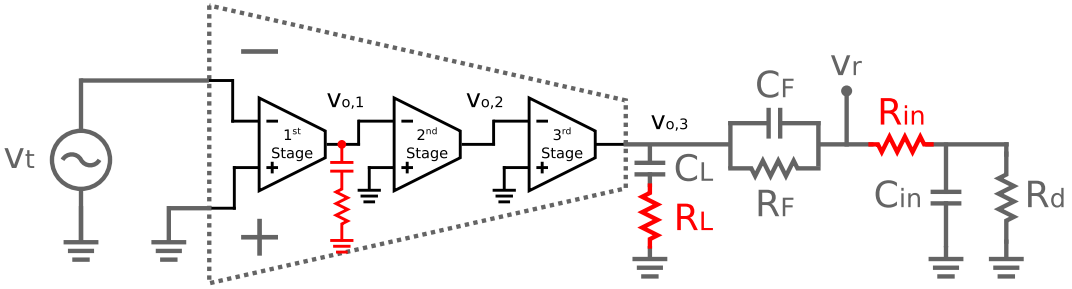
The output stage is implemented as a class AB stage, based on the crossed current mirror shown in Figure 2.6. NMOS transistors ($M_{O,N+/-}$) are driven directly by the output of the previous stage while the PMOS ($M_{O,P+/-}$) are driven through the current mirror made of transistors ($M_{9/10}$) and ($M_{11/12}$). Part of the bias current flowing through the PMOS output transistors is controlled by the CMFB, which is made of a conventional resistive divider and a two-stage OTA, setting output CM to $V_{DD}/2$. As will be highlighted in the following, in this design the output stage is made larger than what would be required in normal operating conditions, in order to directly drive the big off-chip probe capacitance (C_L), without any buffer. It is interesting to notice that, even if the output stage is pseudo-differential, it still shows good CM rejection. In fact, if the two inputs are driven with two signals with equal polarity, it is easy to see that the current in the output NMOS ($M_{O,N+/-}$) and PMOS ($M_{O,P+/-}$) devices have the same sign, meaning that only a small current portion flows through v_{out}, depending on the mismatch between current in the NMOS and PMOS output transistors.

2.3.2 TIA Stability

The complete TIA architecture is reported in Figure 2.7 and the passive components size are listed in Table 2.2 Even if it is implemented in differential form, the TIA is reported here as single-ended for the sake of clarity. Capacitance C_L represents the testing probe input capacitance, which is about 2 pF (differential) and is drawn here as a single-ended 4-pF capacitance. Resistors R_{in} in series with C_{in} and R_L in series with C_L are added to improve stability, as will be discussed in the following. Notice that the input signal is injected below R_{in}. This choice is motivated by the need to filter out clock harmonics



(A)

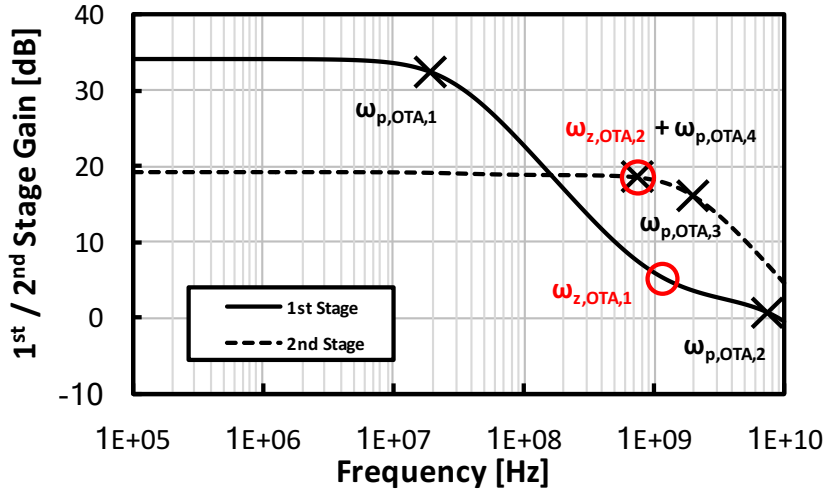


(B)

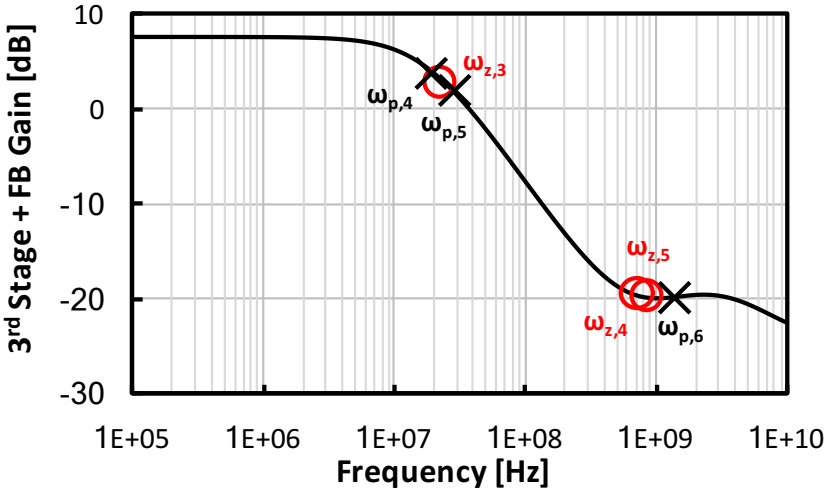
FIGURE 2.7: Schematic of the TIA architecture: a) actual circuit; b) Open-Loop circuit used for stability analysis

Parameter	**Value**	Unit
R_d	500	Ω
C_{in}	20	pF
R_{in}	13	Ω
C_F	3	pF
R_F	2.5	$k\Omega$
C_L	4	pF
R_L	50	Ω

TABLE 2.2: TIA design parameters



(A)



(B)

FIGURE 2.8: a) Gain of the 1st (solid line) and 2nd (dashed line) stages; b) Gain of the 3rd stage and passive feedback network

and has the drawback of adding a fixed real resistance in series to the virtual ground, raising in-band Z_{in}. It will be demonstrated in the following that this does not represent a limit for In-Band linearity of the receiver.

The loop gain is computed breaking the loop at the input of the OTA, injecting a test signal v_t and observing the return signal v_r, as shown in Figure 2.7b. The singularities of the OTA first and second stage were derived previously and the simulated transfer functions of these stages are reported in Figure 2.8a, where poles and zeros were highlighted for clarity. The high-frequency zero of the first stage $\omega_{z,OTA,1}$ is placed before the second stage pole $\omega_{p,OTA,3}$ to improve phase margin. Poles and zeros introduced by the third stage and the feedback network are listed below, assuming R_L and R_{in} are

much smaller than all other resistances and $C_{in} \gg C_F, C_L$. *In Figure 2.8b the simulated transfer function of the output stage and passive feedback network, i.e.* $v_r/v_{o,2}$ *in Figure 2.7b, is reported (cit.[16] ©2018 IEEE*). A low-frequency pole is introduced by C_{in} at frequency:

$$\omega_{p,4} = \frac{1}{R_d//(R_F + r_o)C_{in}} \tag{2.13}$$

where r_o is the finite output resistance of the OTA. R_{in} gives a high frequency zero at frequency:

$$\omega_{z,4} = \frac{1}{R_{in}C_{in}} \tag{2.14}$$

which is placed close to the Gloop GBW. This is very important to ensure stability, since significant phase shift is produced by the two low-frequency poles $\omega_{p,OTA,1}$ and $\omega_{p,4}$. Feedback components create a zero at

$$\omega_{z,3} = \frac{1}{R_F C_F} \tag{2.15}$$

and a pole at

$$\omega_{p,5} = \frac{1}{(R_F//r_o)(C_F + C_L)} \tag{2.16}$$

which is near the cut-off frequency. The large external probe capacitance C_L significantly reduces $\omega_{p,5}$, meaning that increased OTA bandwidth could be achieved using an on-chip buffer or an additional filtering stage as load. Resistor R_L creates a high frequency zero pole doublet at

$$\omega_{z,5} = \frac{1}{R_L C_L} \tag{2.17}$$

$$\omega_{p,6} = \frac{(C_F + C_L)}{C_F C_L (R_{in} + R_L)} \tag{2.18}$$

Loop gain transfer function is simulated after post-layout parasitics extraction. Magnitude and phase of the Gloop are reported in Figure 2.9a (black curve). *The loop has a gain of nearly 60 dB at dc which remains flat up to the feedback pole* $\omega_{p,4}$, *located around 18 MHz. Next, we find the first stage pole* $\omega_{p,OTA,1}$, *at 20 MHz, followed by the zero-pole pair* $\omega_{z,3}$-$\omega_{p,5}$, *near 20 and 32 MHz, respectively. Beyond 32 MHz, the curve starts decreasing with a slope of 40 dB/decade. Above* $\omega_{z,4}$, *located at 670 MHz, 20 dB/decade slope is resumed. Since* $\omega_{z,OTA,1}$ *(at about 1.1 GHz) is very close to* $\omega_{p,OTA,3}$ *the plot crosses the 0-dB axis with slightly less than 20dB/decade slope at 1.6GHz GBW, in the vicinity of the zero-pole doublet given by* R_L *and* C_L *(*$\omega_{z,5}$ *and* $\omega_{p,6}$*) (cit. [16] ©2018 IEEE).* Thanks to the added zeros, phase plot shows a high frequency increase, reaching its maximum close to GBW and guaranteeing 57° of phase margin.

TIA stability was simulated over all process corners and for different operating temperatures, including passive components variations. Singularity position is affected by the

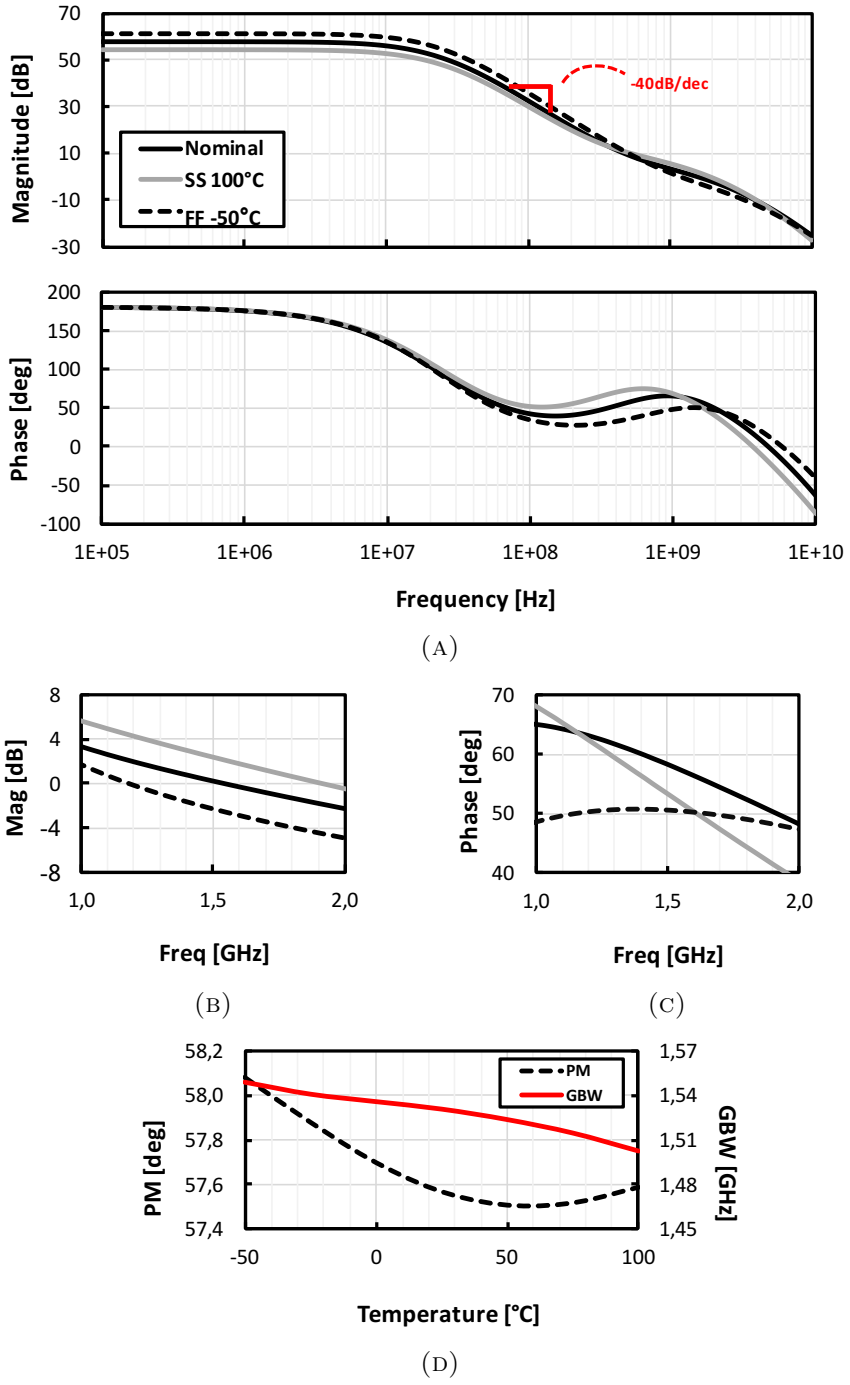


FIGURE 2.9: Post-Layout loop gain magnitude and phase simulation on nominal corner (black line), SS corner at 100°C (gray line) and FF corner at -50°C (dashed line): a) Bode plots; b) Zoom on the magnitude plot around GBW; c) Zoom on the phase plot around GBW; d) GBW and PM in TT corner vs. Temperature

Corner	TT			FF			SS			FS			SF		
Temp. [°C]	-50	25	100	-50	25	100	-50	25	100	-50	25	100	-50	25	100
GBW [GHz]	1.55	1.53	1.5	1.17	1.09	1.03	2.01	1.98	1.9	1.31	1.28	1.27	1.94	1.85	1.76
PM [deg]	58.1	57.6	57.6	50	52	54.5	45.3	42.5	41.3	59.3	60.5	61.6	51.5	51	51.5

TABLE 2.3: TIA corner stability

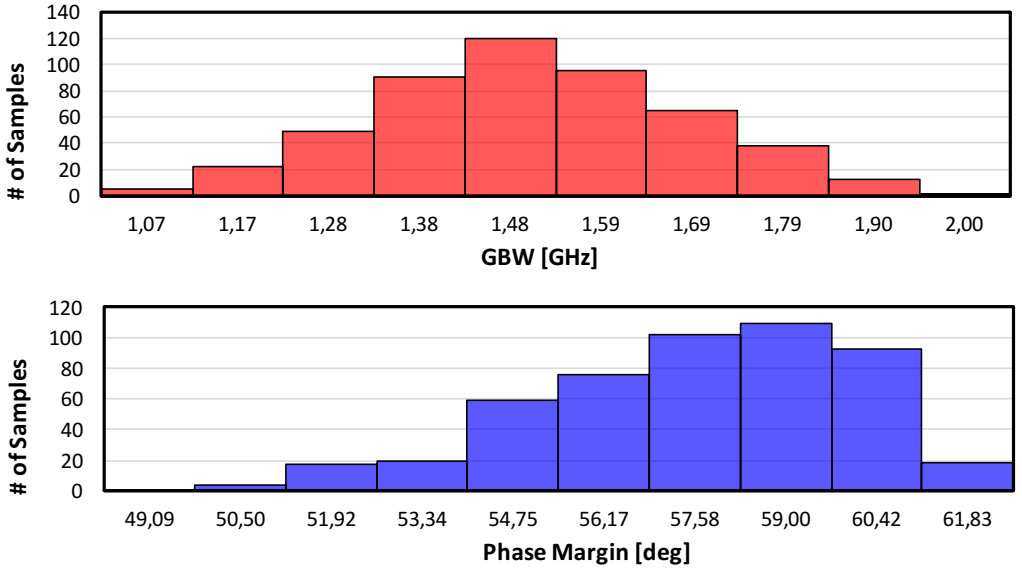


FIGURE 2.10: Montecarlo simulation of GBW and PM of the TIA loop gain

MOM capacitors and the poly-silicon resistors used in the feedback network and within the OTA. Having such passives low temperature coefficients (few hundreds ppm/°C), PM and GBW are stable across temperature as shown in Figure 2.9d and Table 2.3. Figure 2.9 shows the magnitude and phase response of the loop for extreme values of temperature and process demonstrating stability robustness. The most critical corner for stability is slow-slow (SS), where salicided poly-silicon resistor R_{in} strong variations lower $\omega_{z,4}$, increasing GBW to 1.9 GHz to give 41.2 ° of PM. Montecarlo simulation over 500 samples defines the effect of the mismatch. A standard deviation of 176 MHz in GBW and of 2.5° PM is obtained (cit. [16] ©2018 IEEE), as shown in the histograms of Figure 2.10.

From the plots reported above, it can be inferred that the OTA gain is higher than 30 dB up to 400 MHz[1], which is fundamental to maintain virtual ground impedance below switches R_{ON} up to such a frequency.

[1]Notice that in Figure 2.9a also feedback attenuation is taken into account. Above TIA cut-off frequency (20 MHz), feedback path can be approximated as the capacitive partition between C_F and C_{in}, giving approximately 17.5dB of attenuation

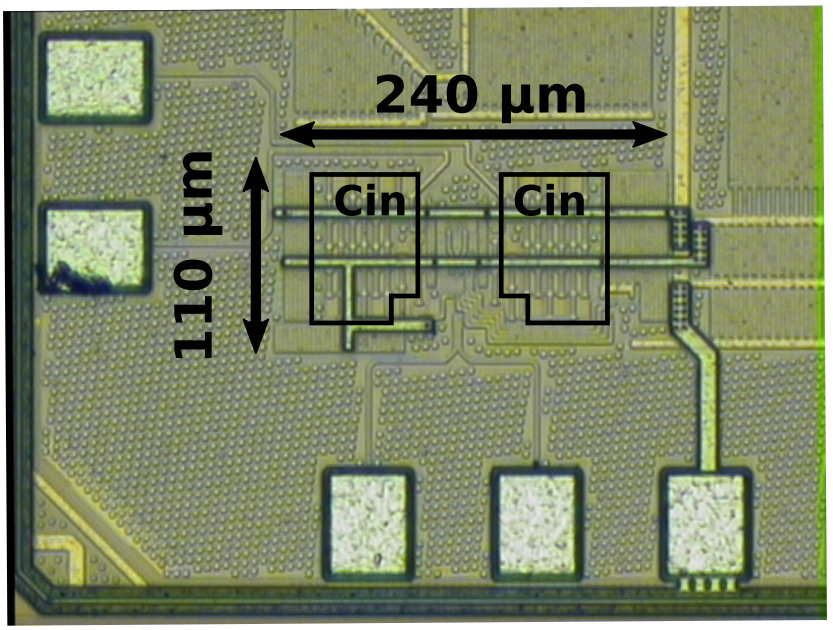


FIGURE 2.11: TIA prototype chip photograph. Picture reused from [16] ©2018 IEEE

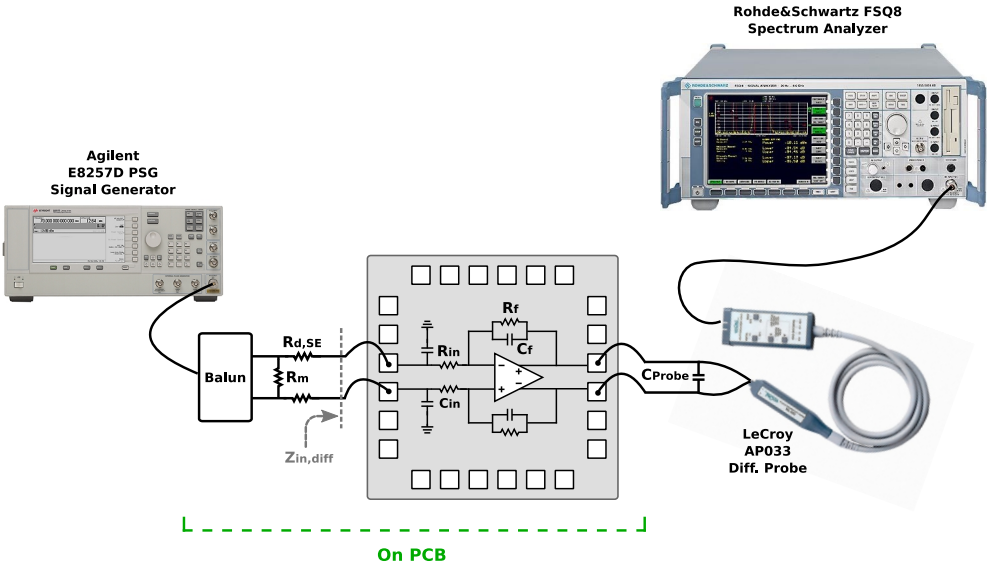


FIGURE 2.12: Setup for stand-alone TIA measurement.

2.4 Measurement Results

The proposed TIA was implemented and tested as a stand-alone filter. The prototype was fabricated in a tsmc 28nm CMOS process and the chip photograph is reported in Figure 2.11. Thanks to the reduced input capacitance, area is only 0.026 mm^2. The measurement setup is shown in Figure 2.12. The chip was wire-bonded on PCB and an external balun was mounted on board to convert the signal from single-ended to

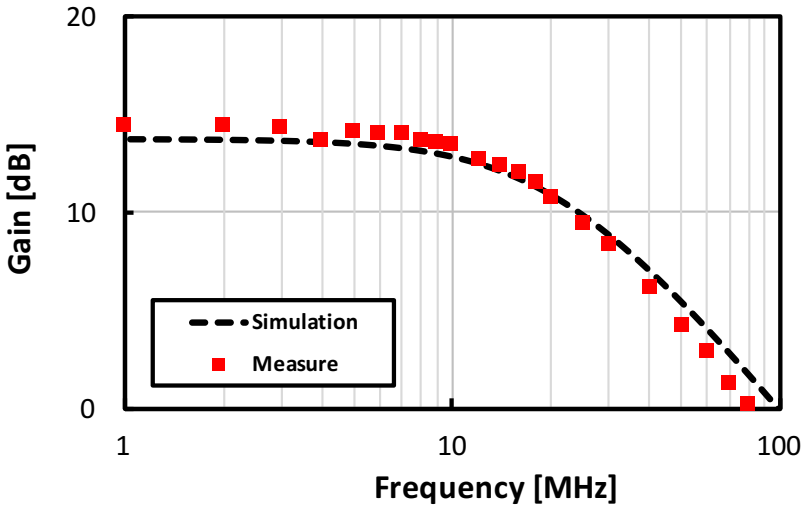


FIGURE 2.13: Measured Gain for stand-alone TIA

differential, while two 500-Ω resistors ($R_{d,SE}$) performed V-I conversion. These resistors emulate the driving resistance provided by the receiver front-end, which was estimated according to [39], considering the LTE diversity receiver proposed in [40]. The output is detected through a *LeCroy AP033* active differential probe, providing a 2-pF differential load. The TIA frequency response, given in Figure 2.13, shows 20 MHz cutoff frequency and 14 dB IB gain, consistently with an LTE channel[2]. *The output noise power spectral density (PSD), measured with 20-dB probe gain to overcome the spectrum analyser noise, given in Figure 2.14, shows no IB noise increase due to* C_{in}*. Main noise contributors are driving resistors, OTA, and feedback resistors. The IR noise* $V_{N,in}$ *integrated up to 16 MHz is 21.1* μV_{RMS}*. The differential TIA input impedance* ($Z_{in,diff}$) *is derived from* S_{11} *measurements with the 500* Ω *driving resistances substituted with 50-*Ω *ones. From Figure 2.15, the low frequency value is 25* Ω*, almost entirely due to* R_{in}*, while the resistance at the virtual ground node is only a few Ohms. At higher frequency, due to OTA gain reduction,* $Z_{in,diff}$ *increases but stays always below 32* Ω*, thanks to the large OTA bandwidth. For very high frequency* C_{in} *shunts the input, lowering* $Z_{in,diff}$ *again. Figure 2.16 shows a 1-dB compression point of almost 2 dBm on an IB tone at 5 MHz, which corresponds to an output swing very close to the supply (1.8V). Linearity is tested through a two-tone intermodulation test. A passive first-order 3-MHz low-pass filter is used after the TIA, to limit the intermodulation of the probe for high frequency tones, where low IM3 signals have to be detected. Figure 2.17a and Figure 2.17b show the IIP3 for IB (5-9 MHz) and OOB (100-199 MHz) tones, respectively. Figure 2.18*

[2]LTE maximum channel bandwidth is 20 MHz, corresponding to 10 MHz at BB. However, in contiguous Carrier-Aggregation 2x20 MHz bandwidths can be aggregated, requiring 20-MHz-BW filter at BB.

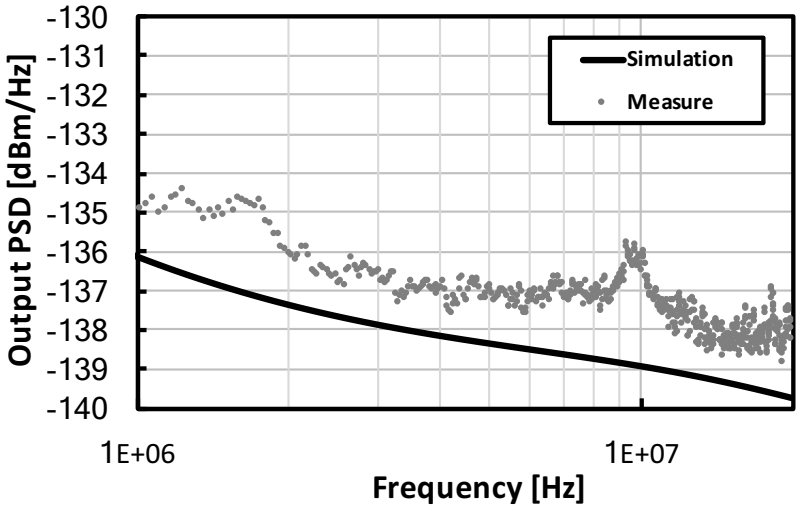


FIGURE 2.14: Measured Output Noise PSD for stand-alone TIA

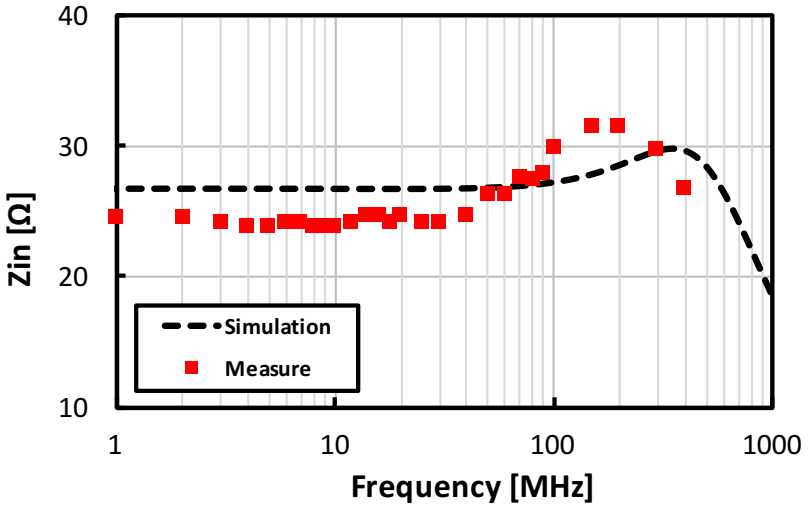


FIGURE 2.15: Measured differential input impedance ($Z_{in,diff}$) for the stand-alone TIA

is a plot of measured and simulated IIP3 vs. the first tone frequency, with IM3 always at 1 MHz. IIP3 starts from 31.5 dBm IB, it increases moving OOB and reaches 50.5 dBm at 100 MHz[3] *(cit. [16] ©2018 IEEE).* From the reported plot it is visible that IB IIP3 is around 9-dB smaller than what predicted by simulation (and by the model presented in Chapter 3), where ideal feedback resistors are used in the TIA (solid curve). If the effect of poly-silicon feedback resistors is included (dashed curve), good correspondence is achieved. Simulation was performed multiplying by a factor 3 the width of the

[3]In [41] IR-noise and IIP3 were referred to the primary of the balun, performing a 1:3 impedance transformation

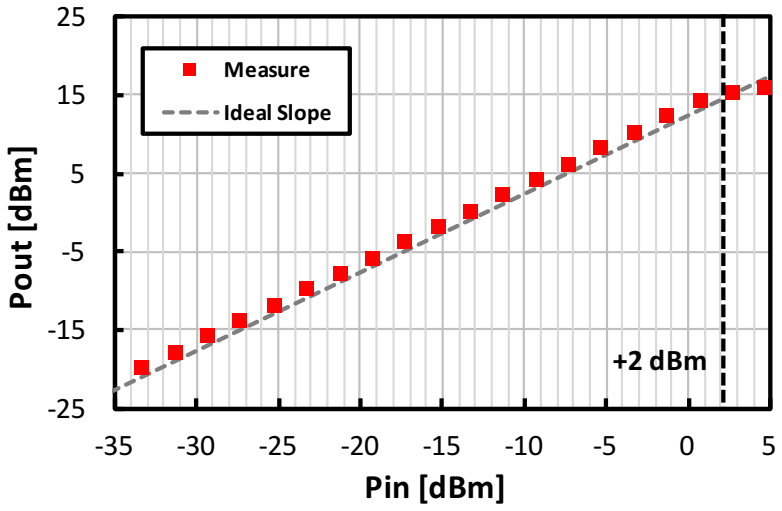


FIGURE 2.16: Measured IB 1dB compression point for the stand-alone TIA

poly-resistors (dotted curve), resulting in less than 3 dB of IB IIP3 degradation, demonstrating that this is not a fundamental limit for IIP3. The measured OOB IIP3 value corresponds to an IM3-Free-Dynamic-Range ($IMFDR_3 = 87.5dB$), where IMFDR is defined as in [31]:

$$IMFDR_3|_{dB} = \frac{2}{3}(IIP3 - P_{N,in}) = 87.5dB \tag{2.19}$$

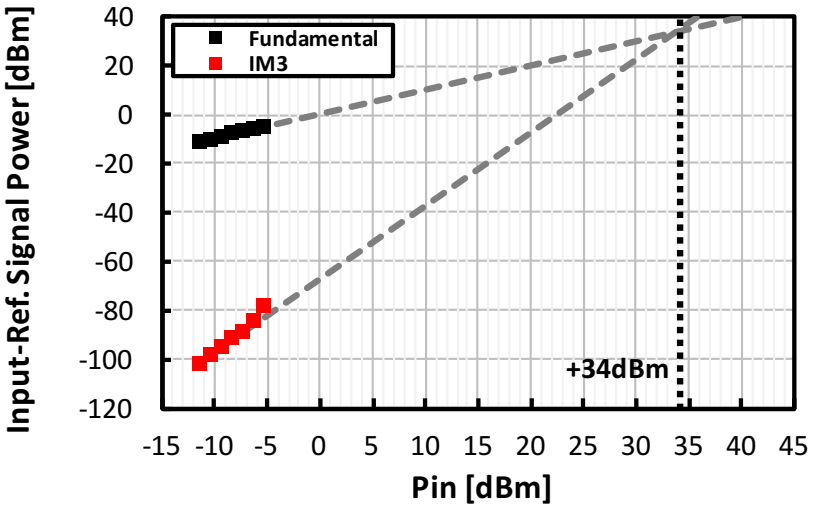
where $P_{N,in}$ is input-referred integrated noise power, expressed in *dBm*. OOB IIP3 was also tested versus IM3 frequency, keeping the first tone at 100 MHz and moving the second one to sweep IM3 frequency (Figure 2.19). IM3 remains flat over almost all the TIA band (up to 10MHz). This is made possible by the fact Gloop is flat over a broad frequency range, as will be discussed in deeper detail in Chapter 3.

TIA performance is summarized and compared with other State-of-The-Art filter implementations in Table 2.4. Both conventional (FoM_{conv}) and modified (FoM_{IM3}) figure-of-merit reported here are used for comparison [31]:

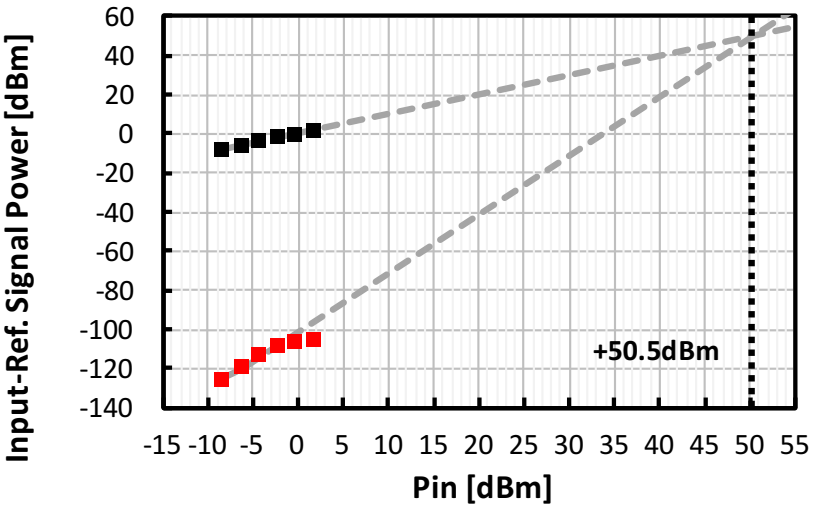
$$FoM_{conv} = IMFDR_3|_{dB} + 10\log\left(\frac{N \cdot f_0}{P_w}\right) \tag{2.20a}$$

$$FoM_{IM3} = FoM_{conv} + 10\log\left(\frac{f_{IM3}}{f_0}\right) \tag{2.20b}$$

where $IMFDR_3|_{dB}$ was defined in (2.19), N is the filter order, f_0 is the cut-off frequency and P_w is the dissipated power. The presented solution shows the highest OOB FoM. In particular, *the proposed TIA has conventional and modified OOB FoM's 2 and 6 dB above the previous best one [29], which has 7 times lower bandwidth (cit. [16] 2018*



(A)



(B)

FIGURE 2.17: Measured fundamental and IM3 IR power vs. P_{in} for a) 5-9 MHz tones and b) 100-199 MHz tones.

IEEE). IB FoM is 0.7 dB below the highest one ([31]). However, it was demonstrated through simulation (Figure 2.18) that 3.6 dB improvement in IB FoM could be achieved by simply enlarging the width of poly-silicon feedback resistors by a factor 3. *FoM's provide a useful way to compare different solutions given that high DR is the key goal in a filter. This, however, assumes that noise and distortion can be freely traded with each other by changing the gain in front of the filter. On the other hand, in practical cases, there may be a maximum gain that can be achieved before other limitations occur (cit. [16] 2018 IEEE).*

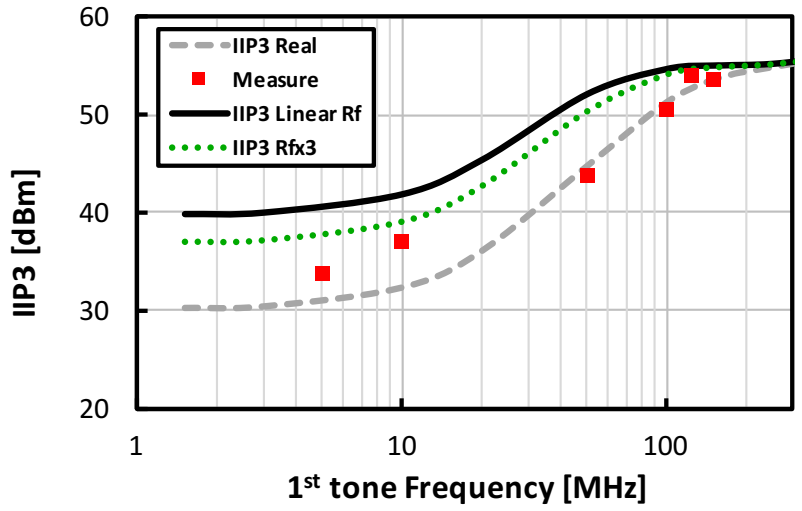


FIGURE 2.18: Measured IIP3 of the stand-alone TIA vs. 1^{st} tone frequency

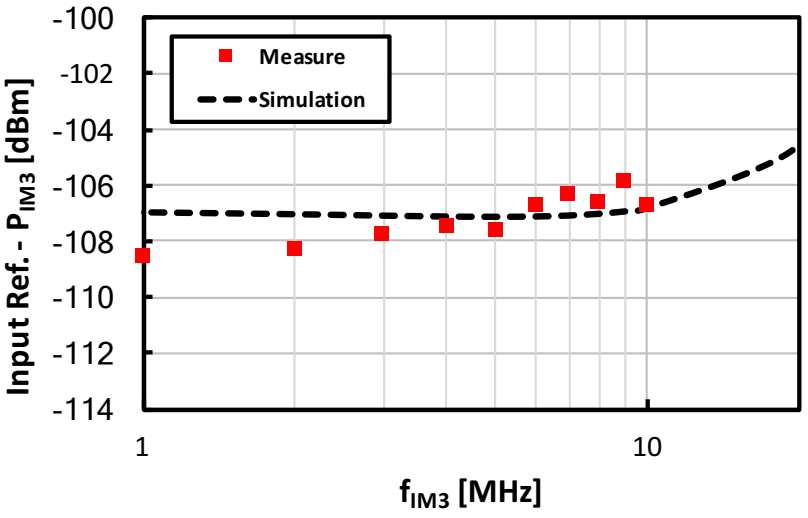


FIGURE 2.19: Measured IM3 of the stand-alone TIA vs. f_{IM3}

2.5 Actual Diversity Receiver Implementation

The TIA described here was integrated in a highly linear wide-band receiver for FDD and Full-Duplex (FD) diversity [40], including a passive Self-Interference Cancellation path. The receiver is schematically represented in Figure 2.20. The Low Noise Trans-Conductance Amplifier (LNTA) is made of two complementary P-N cross-coupled Common Gate (CG) amplifiers, working in class AB. Cross-Coupling produces some benefits in terms of LNTA noise and IM3 reduction. The LNTA current is injected into an ac-coupled passive mixer driven by a 25% duty-cycle LO. The proposed TIA is used as first

Parameters	**This Work**	[28] RFIC '13	[29] ISSCC '16	[29] ISSCC '16	[30] JSSC '09	[31] JSSC '15	[42] JSSC '10	[42] JSSC '10
Tech. [nm]	**28**	65	130	130	130	180	90	90
Area [mm^2]	**0.026**	0.29	0.45	0.45	1.53	0.14	0.5	0.5
Supply Voltage [V]	**1.8**	1.2	1.2	1.2	1	1.8	2.5	1.8
Power [mW]	**5.4**	3.4	1.92	1.92	3	1.38	1.26	0.15
f_0 [MHz]	**20**	14	2.8	12	5	33	2.8	2.8
N	**1**	5	2	2	5	4	4	4
IB IIP3 [dBm]	**31.5**	21.5	N/A	N/A	31.3	18	11	N/A
OOB IIP3 [dBm]	**50.5**	20.6	48.5	36.1	52.8	N/A	35.6	48.5
Noise $V_{N,in}$ [μV_{RMS}]	**21.1**	122	18.4	33.1	170	45	32	273
OOB $IMFDR_3$ [dB]	**87.5**	57.2	86.8	75.1	76.8	61.3	75	71.2
$IB-FOM_{conv}$ [$dB(J^{-1})$]	**170.4**	161	N/A	N/A	161.7	171.1	158.1	N/A
$OOB-FOM_{conv}$ [$dB(J^{-1})$]	**183.2**	160.4	181.5	176.1	176	N/A	174.5	179.9
$OOB-FOM_{IM3}$ [$dB(J^{-1})$]	**180.2**	155.9	174	172.3	165	N/A	167	172.4

TABLE 2.4: TIA performance summary and comparison with State-of-the-Art

BB stage, introducing a real pole at 20 MHz. As discussed above the TIA *ensures a low input impedance ($< 32\Omega$) at the mixer output, while the 20-pF capacitors to ground give a low impedance at very high frequency (above 400 MHz). The chip, fabricated in tsmc 28-nm CMOS, has 0.51-mm^2 active area. The receiver S_{11} is below -10 dB from 1.5 to 3 GHz. At 2 GHz, the gain and double-sideband (DSB) NF are 35 dB and 4.6 dB, respectively (cit. [16] ©2018 IEEE).* The receiver IB and OOB IIP3 (without self-interference cancellation) are +9.5 dBm (4-MHz offset) and +19 dBm (100-MHz offset). To assess the performance of the TIA in its real operating environment, its noise and IIP3 are referred to the receiver input, assuming perfectly linear and noise-less LNTA and mixer. The TIA noise, referred to the receiver input corresponds to a NF of 1.9 dB, meaning that the TIA contribution on the overall RX noise is small. *On the other hand, Figure 2.21 shows the impact of the TIA on the receiver IIP3, assuming perfectly linear front-end. IIP3 starts from around 10 dBm IB and reaches 29 dBm at 100 MHz offset. The much lower value of the TIA IIP3 when referred to the RX input is due to the >20 dB difference between the gain from RX input to TIA output and the TIA gain. Figure 2.21 clearly shows that the TIA is dominating IB receiver IIP3 (cit. [16] ©2018 IEEE)* and that series resistance R_{in} is not excessively degrading front-end linearity.

2.6 Second Order Rauch Implementation

While the majority of reported transceivers use a TIA as a first BB stage, several designs adopt a higher order filter after the passive mixer [23, 24, 26]. The proposed approach to OTA compensation can be generalized and applied to higher order filters, bringing new insights on the pros and cons of this important design choice. In the following the design of a 2$^{\text{nd}}$-order low-pass Rauch filter is discussed and compared with the 1$^{\text{st}}$-order TIA solution in terms of noise, linearity and input impedance.

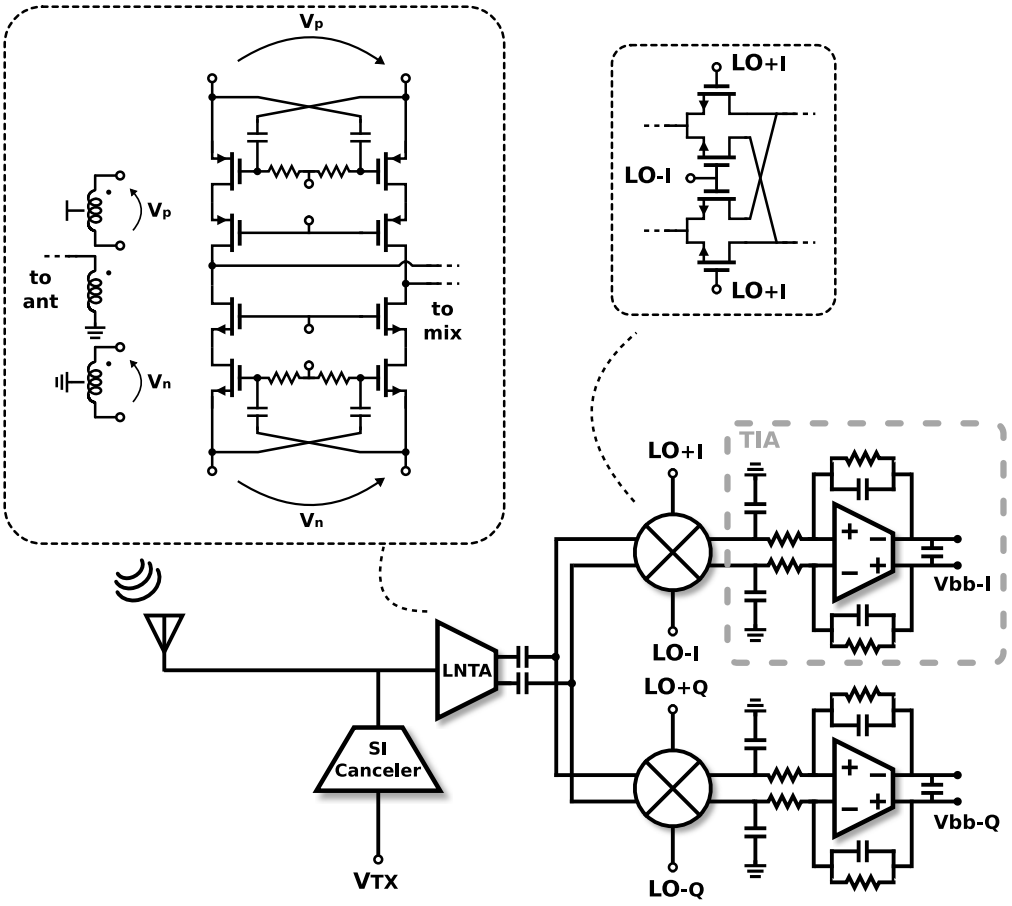


FIGURE 2.20: Conceptual representation of the RX described in [40] with details of LNTA and passive mixer.

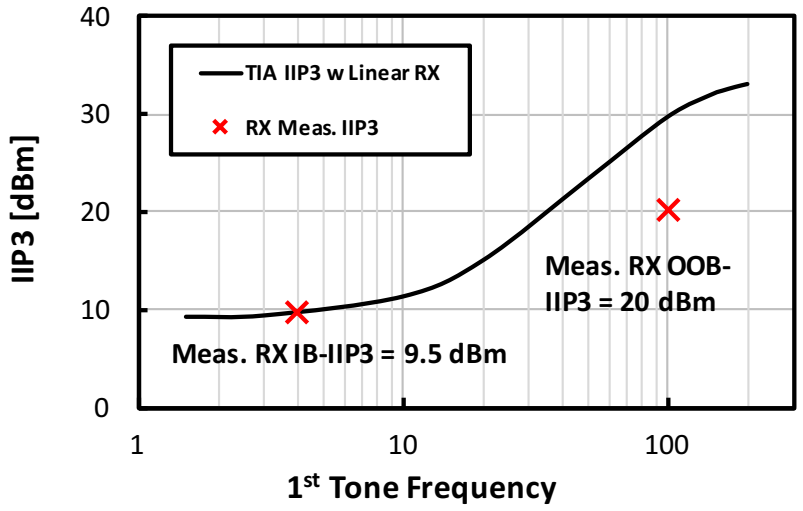


FIGURE 2.21: RX IIP3 with perfectly linear LNTA and mixer (solid line) and measured IB and OOB RX IIP3

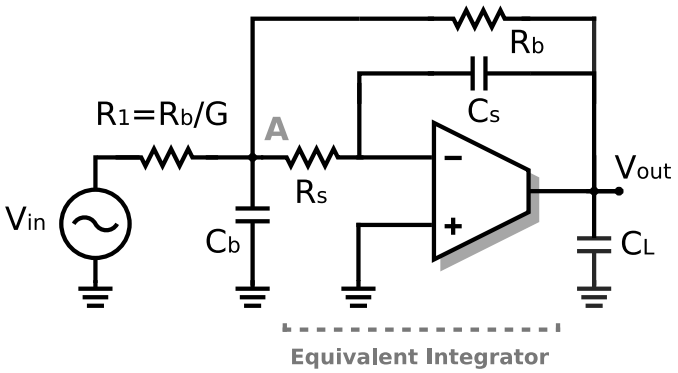


FIGURE 2.22: Single-ended schematic of the Rauch filter

2.6.1 The Rauch Filter

A widespread architecture which is capable of implementing a 2nd order filter using a single OpAmp/OTA is the Rauch filter. The single ended schematic of this filter is reported in Figure 2.22. The frequency behaviour of the circuit can be explained in an intuitive way. At low frequency, capacitors are open-circuits and the architecture reduces to the basic negative-feedback amplifier configuration, made of the OTA and resistors R_b and R_1, producing a gain G:

$$G = -\frac{R_b}{R_1} \tag{2.21}$$

At higher frequency, the circuit is equal to an active-integrator (made of the OTA, R_s and C_s), closed inside a feedback loop. This basically corresponds to an impedance gyrator, making the impedance at node A behave like an equivalent active-inductance. When the capacitance C_b is added between node A and ground, a 2nd order low pass-filter transfer function is obtained. The explicit 2nd order transfer function becomes equal to (2.22).

$$\frac{v_{out}}{v_{in}} = \frac{-G}{s^2(R_s R_b C_s C_b) + s(C_s(R_b + R_s(1+G))) + 1} \tag{2.22a}$$

$$\omega_0 = \sqrt{\frac{1}{R_s R_b C_s C_b}} \tag{2.22b}$$

$$Q = \frac{\sqrt{R_s R_b C_s C_b}}{C_s(R_b + R_s(1+G))} \tag{2.22c}$$

One possible design approach consists of expressing resistors and capacitors as multiples of fundamental resistance and capacitance R and C. In fact, one can set $R_b = R$, $R_s = m \cdot R$, $C_s = C$ and $C_b = n \cdot C$. Under these assumptions, equations (2.22b) and

(2.22c) become equal to (2.23a) and (2.23b):

$$\omega_0 = \frac{1}{RC}\sqrt{\frac{1}{mn}} \tag{2.23a}$$

$$Q = \frac{\sqrt{mn}}{1 + m(1 + G)} \tag{2.23b}$$

Once the gain (G) is set, m and n can be sized to achieve a certain Q according to (2.23b), while R and C can be selected to achieve the desired ω_0 (according to (2.23a)). If the Rauch filter has to be designed for a RX base-band, some additional constraints have to be taken into account, like low Z_{in} and low noise. In the following, a Rauch filter design more oriented to this kind of application will be discussed in deeper detail and some comparison with the TIA proposed at the beginning of this Chapter will be provided.

2.6.2 Design of Rauch Filter for Receiver BB

Starting from the proposed TIA, one possible approach to the Rauch filter design is keeping gain, BW and OTA power consumption constant. Driving impedance (R_1 in Figure 2.22) is set by the environment and cannot be controlled. It follows that, according to (2.21), once the gain is chosen, then also feedback resistance R is automatically set. Parameter m in (2.23a) and (2.23b) is set according to the desired input impedance, leaving n as the only parameter left to change the Q. The capacitance value C is then the only available degree of freedom left to control the cut-off frequency of the filter ω_0. If input impedance has to be kept low (for example $< 40\Omega$ differential), a small R_s and a very large input capacitance C_b (250pF) result. Through simulation it was verified that, if the same OTA presented in Section 2.3.1 is used, Rauch filter gives equal IB IIP3 and much better OOB IIP3 than the proposed TIA. This is motivated by the fact that in-band, where distortion is dominated by the output g_{ds}, output swing and Gloop are exactly the same in the two designs, producing equal amount of IM3 injection and compression, as will become more clear in the next chapter. Out-of-band the circuit takes advantage from the filtering performed at the input by the big input capacitance, lowering the swing on the input node and giving rise to a 28 dB improvement in IIP3 at 100-MHz offset. Unfortunately, such a big input capacitance is also responsible for a quick increase of the OTA noise in the band of the filter, producing an integrated noise 11 dB higher than the TIA. Even if the equivalent FoM is increased by 14 dB, such a big noise is very likely to overwhelm the entire receiver NF.

A better solution is to increase the filter gain until the IR noise is comparable with that of the TIA. A much smaller C_b (58 pF) results, at the cost of an increased R_s, rising

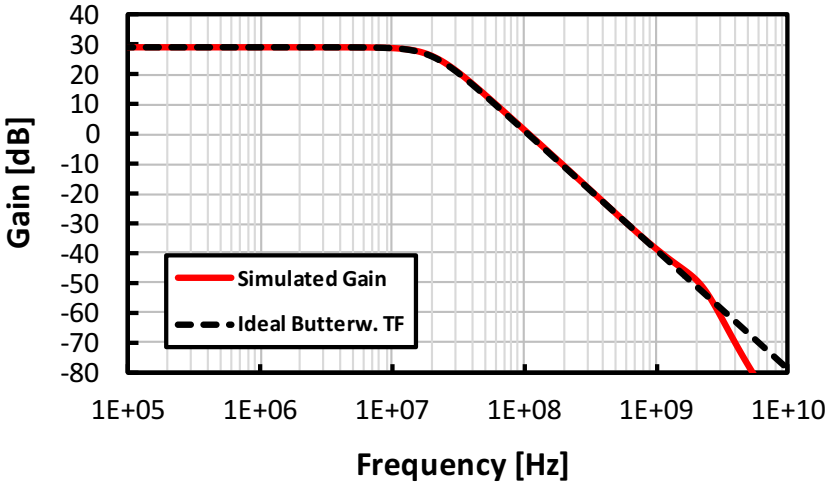


FIGURE 2.23: Simulated Rauch filter gain and comparison with an ideal $2nd$ order Butterworth filter with 29.5 dB IB Gain and 20 MHz f_0.

Parameter	**Value**	Unit
R_s	120	Ω
R_b	13.5	$k\Omega$
C_s	0.65	pF
C_b	58	pF
R_F	2.5	$k\Omega$
C_L	4	pF
G	30	

TABLE 2.5: Rauch design parameters

the overall input impedance. Table 2.5 reports the design parameters used to obtain a Butterworth filter (Q=0.7), with 20 MHz cut-off frequency and 29.5 dB IB gain, whose simulated transfer function is reported in Figure 2.23. In the designed Rauch filter the same OTA architecture of Figure 2.6 is adopted, doubling the current in the input stage, in order to achieve a comparable overall noise for the filter.

The same approach to stability is used as for the TIA: no Miller capacitor is used and feedback is exploited to improve phase margin. The circuit of Figure 2.24 is used to study the stability of the loop. The loop gain is given by the cascade of the frequency response of the loaded OTA and the voltage transfer function from v_{out} to v_B. The Rauch feedback network introduces two low-frequency poles:

$$\omega_{p,1} = \frac{1}{C_b(R_b + r_{out})//(R_b/G)} \tag{2.24}$$

and

$$\omega_{p,2} = \frac{1}{(C_s + C_L)(R_b//r_{out})} \tag{2.25}$$

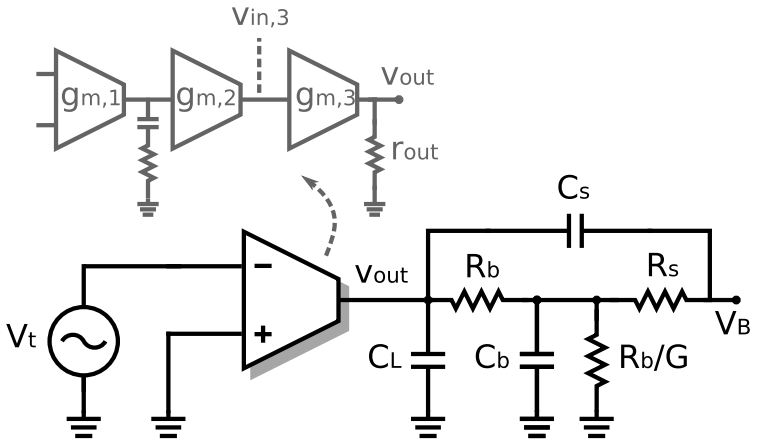


FIGURE 2.24: Open-loop circuit for stability analysis of the Rauch filter

and a high frequency pole:

$$\omega_{p,3} = \frac{(C_s + C_L)}{R_s C_s C_L} \tag{2.26}$$

where the assumption $R_b, r_{out} >> R_s$ is made. The feedback also adds in the Gloop two complex zeros, having equal ω_0 and Q as the poles of the closed-loop transfer function, which are fundamental to guarantee stability. The OTA poles and zeros are kept the same as in the TIA design (Section 2.3.2), with the only exception of $\omega_{p,OTA,1}$, which is shifted to 15 MHz to improve phase margin. With the component sizes reported in Table 2.5, 60° of phase margin at 1.5 GHz GBW is achieved, as shown in Figure 2.25, where the position of all singularities is explicitly indicated. The large Gloop GBW has the positive effect of attenuating the closed-loop transfer function Q sensitivity to OTA gain. This can be observed in Figure 2.23, where the proposed Rauch gain is shown to match very well to the ideal 2$^{\text{nd}}$ order Butterworth transfer function up to 1 GHz.

2.6.3 Simulation Results and performance comparison

The Rauch filter was evaluated only through simulation. To achieve comparable noise with the TIA, gain was increased to 29.5dB and current in the OTA first stage was doubled, increasing OTA power consumption by 28%, obtaining 24 μV_{RMS} of integrated IR noise, still 1dB worse than the TIA. As already mentioned in Section 2.6.1 the Rauch shows an equivalent RLC input impedance as reported in Figure 2.26. At low frequency the finite gain A_0 of the OTA produces a non-zero input resistance, given by the feedback resistance R_b divided by a factor $(1 + A_0)$ through the Miller effect. At higher frequency differential input impedance shows an inductive behaviour, reaching a peak value of $2 \cdot R_s$ at frequency ω_0 and then decreasing like $2/(s \cdot C_b)$. With the selected components values of Table 2.5, the peak resistance is 240 Ω at 20 MHz which reduces to 80 Ω at 60 MHz. It is important to notice how to achieve comparable noise performance with the

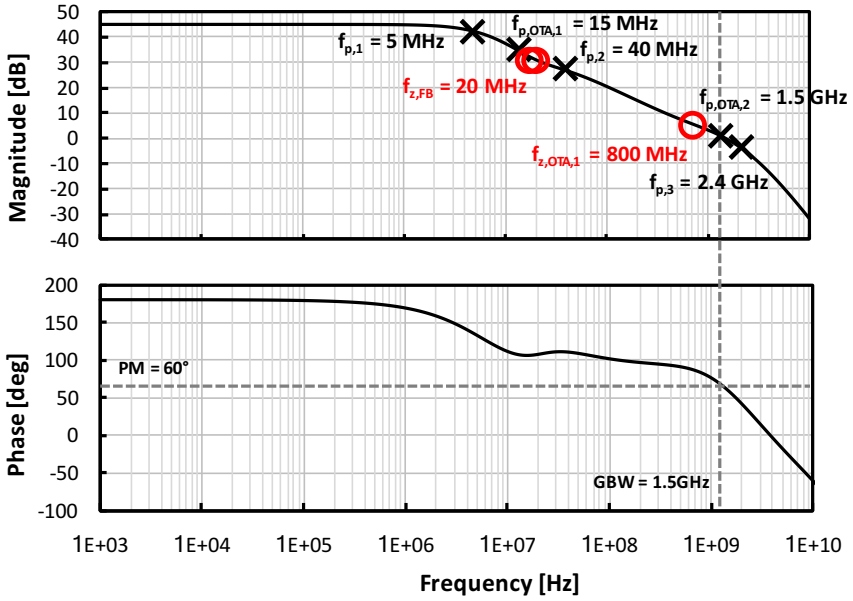


FIGURE 2.25: Magnitude and Phase plots of the Gloop for the Rauch filter designed according to Table 2.5

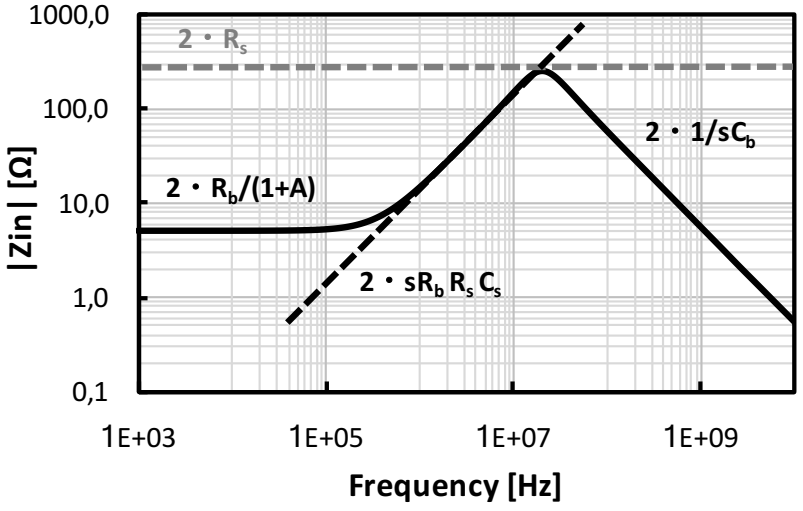


FIGURE 2.26: Simulated differential input impedance of the designed Rauch filter

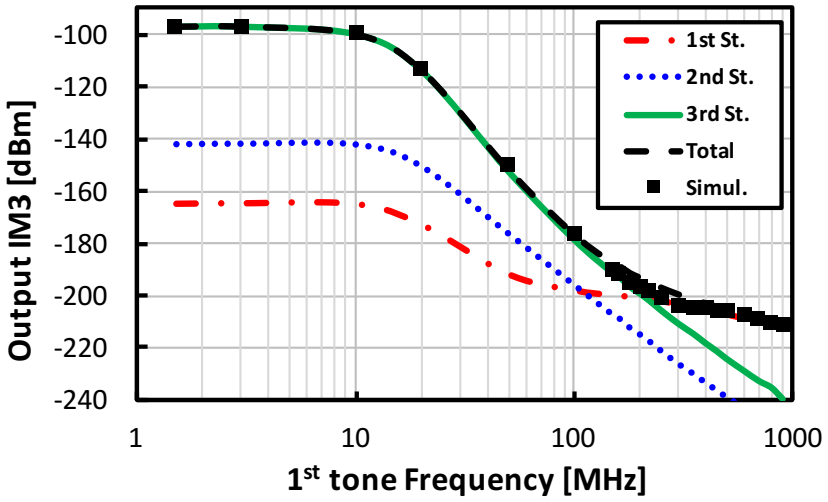


FIGURE 2.27: Simulated Output referred IM3 of the designed Rauch vs. Input tone frequency with -30 dBm input power.

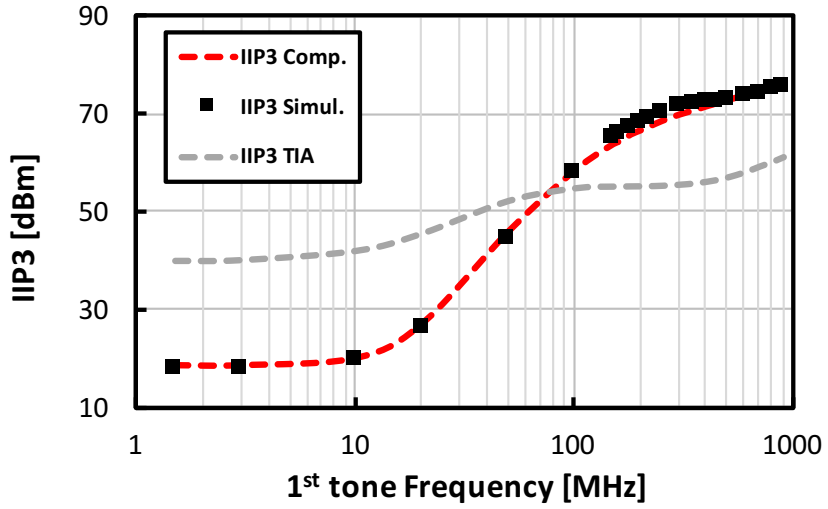


FIGURE 2.28: Simulated IIP3 of the designed Rauch vs. Input tone frequency and comparison with the TIA (IM3 at 1 MHz).

TIA, input impedance is increased, with potential degradation of the front-end IIP3. The Rauch output 1 MHz-IM3 vs. input tone frequency is shown in Figure 2.27, with -30 dBm input tones. Using the model described in Chapter 3 the IM3 contributions from each stage were isolated and reported in the same picture. At low frequency IM3 is clearly dominated by the output stage distortion. Through the same model it was also verified that, as for the TIA, the dominant IM3 contributor is the output g_{ds}. Due to the higher gain of the Rauch, a larger amount of IM3 is injected on the output node, and because of the lower feedback factor, IM3 compression is lowered. This leads to a lower

IB IIP3 than the TIA, as shown in Figure 2.28. Thanks to the filter 2^{nd}-order response, however, IM3 goes down very steeply (120dB/decade) beyond ω_0, corresponding to a 60 dB/decade increase in IIP3, which outpaces the TIA IIP3 at 70MHz. For very high frequency IIP3 saturates above 73 dBm, a much higher value than with the TIA, as visible from the plot of Figure 2.28. The achieved IIP3 at 100MHz offset, combined with the integrated IR noise and the power consumption, gives a FoM_{conv} (defined in (2.20a)) of $189dB(J^{-1})$, which is 8 dB worse than the same-gain Rauch implementation ($197dB(J^{-1})$), but still 6 dB better than the TIA ($183dB(J^{-1})$). If IM3 is shifted to 10 MHz, IIP3 at 100 MHz drops by 4 dB. This is motivated by the fact at 10 MHz the Rauch Gloop has already dropped with respect to the low-frequency value, determining a lower IM3 compression. It follows that modified FoM_{IM3} (defined in (2.20b)) is $183.9dB(J^{-1})$, just 3.9 dB better than the one of the TIA ($180dB(J^{-1})$).

2.7 Conclusions

A 20-MHz-BW TIA for SAW-Less FDD Receivers was described in this chapter. Relying on additional zeros in the OTA and in the feedback path, stability was achieved without any Miller-Compensation capacitors, widening the OTA bandwidth and improving linearity performance. Larger OTA bandwidth allowed also reducing the capacitance at the TIA input, resulting in better noise. The measured TIA prototype showed a FoM exceeding that of all previous works. The adopted compensation approach was also applied to a 2^{nd} order Rauch filter. Through simulation an even better FoM was verified, with comparable IR noise with respect to 1^{st} order TIA. This was however achieved at the cost of an increased Rauch input impedance, potentially degrading RX front-end linearity.

Chapter 3

Non-linearity model for closed-loop TIAs

In the previous chapter it was highlighted the importance of linearity in the design of a TIA for SAW-Less RX. In order to achieve good performance, it is important to have a good model for the linearity behaviour of the circuit. In this chapter an intuitive model for non-linearity analysis in a closed-loop TIA is presented, providing some important hints on the design choices to be adopted to optimize linearity in every frequency range. The proposed model is applied to the previously described TIA, showing good agreement with simulated and measured results. The same model is also applied to TIAs based on a Miller-Compensated Two-Stage-OTA and on a Nested-Miller Three-Stage-OTA, highlighting the advantages of the proposed topology in terms of linearity, compared with more traditional implementations. Most of the material reported in this chapter is reused from [16] (©2018 IEEE), in agreement with IEEE copyright policy on theses and dissertations.

3.1 Introduction

In this chapter it is presented a relatively simple model of closed-loop OTAs to describe 3^{rd} order intermodulation (IM3), which, as previously highlighted, is a particularly critical spec in the design of base-band (BB) circuits for wireless receivers. 2^{nd} order non-linearities are neglected here, assuming a fully differential structure for the OTA. The described approach is based on the one proposed in [43–46], where the linearized OTA response is used to extract the non-linear terms injected at the various nodes of the TIA, which are then referred to the output.

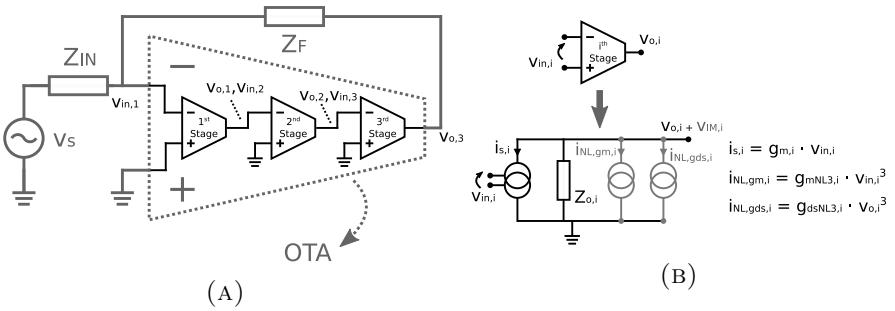


FIGURE 3.1: Simplified single-ended representation of the proposed model: a) overall loop; b) Single OTA Stage

3.2 Model description

A single-ended representation of the loop for a Three-Stage-OTA with no internal feedback is given in Figure 3.1. Each OTA stage is modelled as a trans-conductor ($g_{m,i}$), loaded by $Z_{o,i}$(Figure 3.1b), which includes both output resistance and capacitance. To simplify the analysis, the non-linearity is modelled at the OTA stage level, as opposed to the transistor level as in [43–45]. Furthermore, only two distortion terms are considered, the first due to the transconductance $g_{mNL3,i}$ and the second due to the output conductance $g_{dsNL3,i}$.

The procedure to get the output intermodulation is represented by the flowchart of Figure 3.2 and is applied to the OTA in Figure 3.1a. Some parameters must be first computed for each stage by either simulation or computation. In Step 1.a, the nonlinear coefficients $g_{mNL3,i}$ and $g_{dsNL3,i}$ are found simulating each stage separately, as described in Appendix A. In Step 1.b, the closed-loop swing versus frequency at the input and output of each stage is obtained. Finally, the closed-loop output impedance $Z_{o,CL,i}$, at the IM3 frequency (f_{IM3}) is computed by dividing the open-loop output impedance $Z_{o,OL,i}$ by the loop gain [1]*. The output intermodulation contributed by each stage is computed in Steps 2 to 5. In Step 2, the intermodulation injection is found. Applying two sinusoids of amplitude $A_{1,i}$ and $A_{2,i}$ and frequency ω_1 and ω_2, the two IM3 components in the i^{th} stage output current are located at $2\omega_1 - \omega_2$ and have strengths that depend on the signal amplitude at the input and output of the i^{th} stage as given in the following:*

$$i_{NLgm,i} = \frac{3}{4} g_{mNL3,i} A_{1,i}^2 A_{2,i} \cdot \sin((2\omega_1 - \omega_2)t) \tag{3.1}$$

$$\begin{aligned} i_{NLgds,i} = \frac{3}{4} g_{dsNL3,i} (A_{1,i} \cdot |G_i(\omega_1)|)^2 \cdot (A_{2,i} \cdot |G_i(\omega_2)|) \cdot \\ \cdot \sin((2\omega_1 - \omega_2)t + 2\angle G_i(\omega_1) - \angle G_i(\omega_2)) \end{aligned} \tag{3.2}$$

[1] Notice that $Z_{o,OL,3}$ also includes the loading of the feedback network

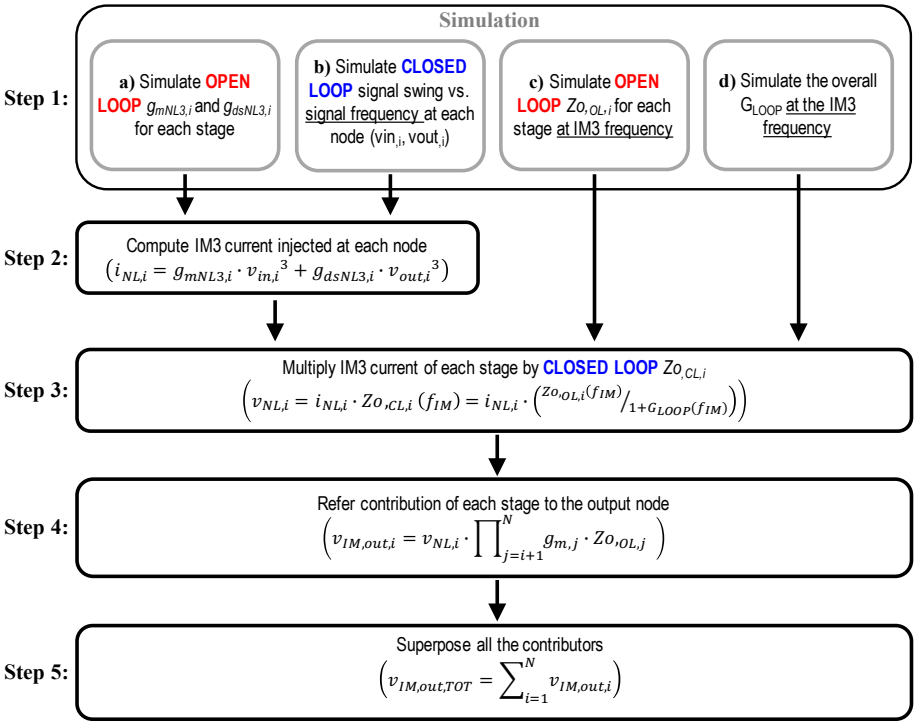


FIGURE 3.2: Flowchart of the adopted procedure for computing output IM3 of a closed-loop OTA

where $G_i(\omega_k)$ is the gain of the i^{th} stage at frequency ω_k and $g_{mNL,3}$ and $g_{dsNL,3}$ are the third order non-linear coefficients associated with g_m and g_{ds}. In Step 3, the IM3 voltage ($v_{IM,i}$) at the output of each stage is found by multiplying the total injected current $i_{NLgm,i} + i_{NLds,i}$ by the closed-loop output impedance $Z_{o,CL,i}$ at f_{IM3}, as given in (3.3) *(cit. [16] ©2018 IEEE).*

$$v_{IM,i} \cong \left(\frac{3}{4} g_{mNL3,i} A_{1,i}^2 A_{2,i} + \frac{3}{4} g_{dsNL3,i} (A_{1,i} \cdot |G_i(\omega_1)|)^2 \cdot (A_{2,i} \cdot |G_i(\omega_2)|)\right) \cdot \cdot \frac{|Z_{o,OL,i}(2\omega_1 - \omega_2)|}{1 + G_{LOOP}(2\omega_1 - \omega_2)} \cdot \sin((2\omega_1 - \omega_2)t) \tag{3.3}$$

In (3.3) the two non-linear terms are simply added in magnitude, neglecting their relative phase. This is based on the assumption that one term dominates in each frequency range, as will be verified in the following. *In Step 4, all $v_{IM,i}$ are referred to the output by multiplying them by $TF_{i\to out}$, i.e., the open-loop transfer function from the i^{th} stage output to the OTA output. $TF_{i\to out}$ is equal to the product of $g_{m,j} \cdot Z_{o,OL,j}$ at the IM3 frequency for all stages (j) following the i^{th} stage, as given in* (3.4) *(cit. [16] ©2018*

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$$v_{IM,out,i} = v_{IM,i} \cdot TF_{i \to out} = v_{IM,i} \cdot \prod_{j=i+1}^{N} g_{m,j} \cdot Z_{o,OL,j} \tag{3.4}$$

where N is the total number of OTA stages. *In Step 5, all output referred terms are summed as in* (3.5).

$$v_{IM,out,TOT} = \sum_{i=1}^{N} v_{IM,out,i} \tag{3.5}$$

The model provides three key pieces of information versus tone frequency and IM3 frequency (f_{IM3}):

1. *the total closed-loop intermodulation;*
2. *the stages that dominate distortion in a frequency range;*
3. *the mechanism that dominates distortion within a stage.*

Two key concepts are identified: distortion injection and distortion compression. The former represents the distortion a stage injects in the circuit, which depends on the voltage swing at the intermediate nodes at the frequency of the input tones. The latter, quantifies how much the distortion is reduced by the loop, which depends on the loop gain at the IM3 frequency (cit. [16] ©2018 IEEE). This theory can be simplified for the OTA first and last stage, which often dominate distortion, as is shown below.

For the last stage, whose $v_{IM,out,3}$ is given in (3.6)*, the injected distortion depends only on the output stage itself and not on any other OTA characteristic. This is because both the swing and the current at the output node are set only by the feedback network. The output stage distortion $v_{IM,out,3}$ is obtained by multiplying the injected distortion by the closed loop output impedance at f_{IM3} (cit. [16] ©2018 IEEE).*

$$\begin{aligned} v_{IM,out,3} &= (i_{NLgm,3} + i_{NLgds,3}) \cdot \frac{Z_{o,OL,3}(f_{IM3})}{1 + G_{LOOP}(f_{IM3})} \\ &\cong (i_{NLgm,3} + i_{NLgds,3}) \cdot \frac{1 + Z_F/Z_{in}(f_{IM3})}{g_{m,3} \cdot g_{m,1} Z_{o,OL,1}(f_{IM3}) \cdot g_{m,2} Z_{o,OL,2}(f_{IM3})} \end{aligned} \tag{3.6}$$

Equation (3.6) can also be expressed in terms of IIP3 as in (3.7):

$$v_{IIP3,3} = \sqrt{\frac{(4/3)G_{loop}(f_{IM3})}{\left(\frac{Z_F^2}{Z_{IN}^2}(f_1)\frac{Z_F}{Z_{IN}}(f_2)\right)\left(g_{dsNL3,3} + \frac{g_{mNL3,3}}{g_{m,3}^3 Z_{o,OL,3}^2(f_1) Z_{o,OL,3}(f_2)}\right) Z_{o,OL,3}(f_{IM3})}} \cdot \sqrt{\frac{Z_F}{Z_{IN}}(f_{IM3})} \tag{3.7}$$

where, with reference to Figure 3.1a, it was considered $v_{o,3}/v_s \cong Z_F/Z_{IN}, v_{in,3}/v_s \cong g_{m,1}Z_{o,OL,1}g_{m,2}Z_{o,OL,2}/G_{loop}$ and the assumption $Z_F \gg Z_{IN}$ was made to achieve a more manageable equation. It can be concluded that *to improve the closed-loop intermodulation distortion of the output stage, it is key to enhance the gain of the OTA at the IM3 frequency, i.e., up to TIA cutoff frequency ω_0 since intermodulation is increasing the noise floor when it falls within the signal bandwidth (cit. [16] ©2018 IEEE).* The first stage distortion is given by (3.8).

$$\begin{aligned} v_{IM,out,1} &= (i_{NLgm,1} + i_{NLgds,1}) \cdot \frac{Z_{o,OL,1}(f_{IM3}) \cdot g_{m,2}Z_{o,OL,2}(f_{IM3}) \cdot g_{m,3}Z_{o,OL,3}(f_{IM3})}{1 + G_{LOOP}(f_{IM3})} \\ &\cong (i_{NLgm,1} + i_{NLgds,1}) \cdot \frac{1}{g_{m,1}} \cdot \left(1 + \frac{Z_F}{Z_{IN}}(f_{IM3})\right) \end{aligned} \tag{3.8}$$

This relation can as well be expressed in terms of IIP3, considering $v_{in,1}/v_s \cong 1/G_{loop}$ and $v_{o,1}/v_s \cong g_{m,1}Z_{o,OL,1}/G_{loop}$, with reference to (Figure 3.1a):

$$v_{IIP3,1} = \sqrt{\frac{(4/3)G_{loop}^2(f_1)G_{loop}(f_2)g_{m,1}}{g_{mNL3,1} + g_{dsNL3,1}g_{m,1}^3 Z_{o,OL,1}^2(f_1) Z_{o,OL,1}(f_2)}} \cdot \sqrt{\frac{Z_F}{Z_{IN} + Z_F}(f_{IM3})} \tag{3.9}$$

The situation is the dual of the output stage. For a given input stage, distortion compression by the loop is independent from any characteristic of the OTA. On the contrary, distortion injection decreases increasing the OTA gain at the tone frequency (cit. [16] ©2018 IEEE). In typical OTA implementations, when the input tones frequency increases the OTA gain drops and the input stage distortion increases. It is therefore key to enhance the OTA bandwidth, maximising its gain at the frequency of the OOB tones, i.e. up to the maximum TX-RX band frequency distance. Alternatively, a big

Stage	Coefficient	Value	Unit
1^{st}	$(3/4) \cdot g_{mNL3,1}$	$3.22 \cdot 10^{-2}$	A/V^3
	$(3/4) \cdot g_{dsNL3,1}$	$3.58 \cdot 10^{-6}$	A/V^3
	$Z_{o,OL,1}(1MHz)$	16.4	$k\Omega$
	$TF_{1\rightarrow OUT}(1MHz)$	41.1	dB
2^{nd}	$(3/4) \cdot g_{mNL3,2}$	$9.32 \cdot 10^{-3}$	A/V^3
	$(3/4) \cdot g_{dsNL3,2}$	$-7.11 \cdot 10^{-6}$	A/V^3
	$Z_{o,OL,2}(1MHz)$	10.4	$k\Omega$
	$TF_{2\rightarrow OUT}(1MHz)$	22	dB
3^{rd}	$(3/4) \cdot g_{mNL3,3}$	$1.19 \cdot 10^{-3}$	A/V^3
	$(3/4) \cdot g_{dsNL3,3}$	$2.32 \cdot 10^{-5}$	A/V^3
	$Z_{o,OL,3}(1MHz)$	2.1	$k\Omega$
	$TF_{3\rightarrow OUT}(1MHz)$	0	dB
	$G_{LOOP}(1MHz)$	61.4	dB

TABLE 3.1: Model coefficients for the proposed OTA

shunt capacitor at the virtual ground node C_{in} *can achieve the same goal thanks to its low-pass filtering effect at the OTA input. Notice, however, that* C_{in} *cannot be increased arbitrarily since this may not only degrade noise but can also have an adverse effect on output stage linearity. In fact, when* C_{in} *is large enough to lower* Z_{IN} *before the TIA cut-off frequency* ω_0*, the loop gain starts to decrease in-band due to a reduction of the feedback factor and the IM3 of the output stage increases as its frequency nears* ω_0 *(cit. [16] ©2018 IEEE).* It can be concluded that, to improve IIP3 it is needed to increase the OTA gain at the highest OOB blocker frequency and at ω_0. This involves maximizing the OTA bandwidth and shaping its frequency response to have a larger than 20 dB/decade slope up to as near as possible the OTA GBW, while preserving stability. This is exactly the approach adopted in the OTA design described in Chapter 2.

3.3 Linearity Analysis of the Proposed Structure

The model described in the previous section is applied here to the TIA presented in Chapter 2 [2]. The non-linear current generators are found first. Each stage is simulated separately, as described in Appendix A, giving the results reported in Table 3.1.

Using the simulated gain from the input to each node, given in Figure 3.3, the signal swing at each intermediate node of the closed-loop TIA is computed (Step 1.b in Figure 3.2). Next, the open loop output impedance of each stage and the overall Gloop at f_{IM3} are found via simulation and reported in Table 3.1 (Step 1.c and 1.d). Non linear current injected by each stage is computed using the signal swing at each node and $g_{mNL3,i}$ and $g_{dsNL3,i}$ (Step 2). The $v_{NL3,i}$ is found applying (3.3), with the values

[2] In a multi-stage OTA closed in feedback, 2^{nd} order non-linearities coming from two stages may interact, resulting into 3^{rd} order non-linearity. In this design, however, since the first two stages are fully differential, at least up to very high frequencies, this effect is negligible.

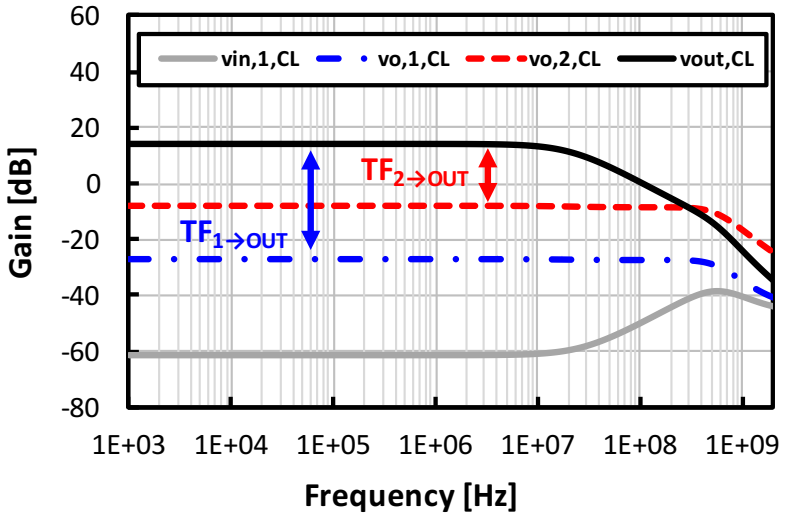

FIGURE 3.3: Intermediate nodes gain of the proposed TIA vs. frequency.

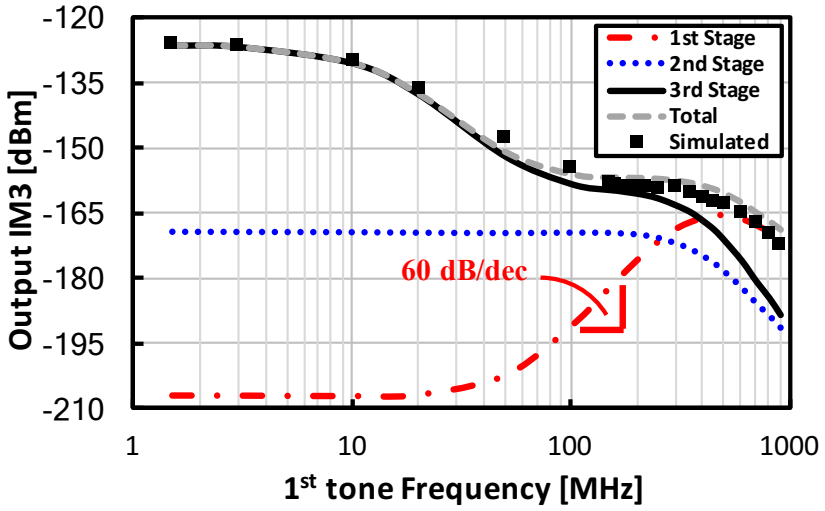

FIGURE 3.4: Simulated and computed IM3 at the TIA output vs. input tones frequency with the proposed OTA and contribution of single OTA stages.

of $Z_{o,OL,i}$ and Gloop of Table 3.1 (Step 3). Finally, equations (3.4) and (3.5) are used to get the total closed-loop IM3 at the output using the $TF_{i\rightarrow OUT}$ of Table 3.1.

Figure 3.4 plots IM3 vs. the first tone frequency for two -20 dBm input signals when the IM3 falls at 1 MHz. The difference between calculation and simulations is typically around 1 dB and always below 4 dB. The proposed method for OTA distortion analysis allows to separate IM3 contribution of each stage to the output as shown in Figure 3.4. This information is usually difficult to obtain, even using sophisticated distortion simulations [47]. It would require substituting all stages but the one under

consideration with an equivalent linear model while ensuring that the OTA frequency response is preserved across its entire frequency range of interest. From the reported plots it can be concluded what follows:

1. *The last stage dominates distortion up to 400 MHz;*
2. *Beyond this frequency the first stage dominates;*
3. *When the first stage starts to dominate, the overall IM3 starts to decrease with frequency;*
4. *The second stage never dominates distortion.*

The first stage starts from a very small value and rises beyond the first OTA pole at 20 MHz with a 60 dB/decade slope since, as the gain $A(\omega_{1,2})$ drops, the virtual ground signal increases as $1/A(\omega_{1,2})$ and the distortion increases as $1/A^2(\omega_1)A(\omega_2)$. Since the OTA gain at 400 MHz is still 30 dB, OTA input swing stays small enough to prevent excessive distortion injection in this range. The second stage has a broadband gain of about 20 dB and the swing at its input stays low and constant with frequency, making its distortion always negligible compared to that of the last stage [3] *(cit. [16] ©2018 IEEE).* Around 400 MHz C_{in} starts diverting the current from the OTA, making the overall IM3 decrease with frequency. It can be noticed that the presence of a wide-band second stage is critical to achieve low IM3. In fact, it helps compressing the distortion from the output stage by increasing the in-band loop gain and it strongly reduces distortion injection from the first stage by reducing the OTA input signal.

The method described above also allows to identify which distortion mechanism dominates within a stage, which is difficult to achieve even with sophisticated distortion simulations [47]. The output stage was identified to be the dominant one over a broad frequency range. In Figure 3.5 the g_m and g_{ds} non-linear contributors for this stage are separated and shown vs. frequency. From the plot it can be noticed that, *at low frequency, the large output swing makes g_{ds} non-linearity dominant. As a result, the output IM3 follows the frequency response of the TIA, i.e., beyond ω_0 it decreases with a slope of 60 dB/decade, leading to a sharp rise in the IIP3. Around 60 MHz, the g_m non-linearity takes over and the IM3 flattens out, leading to a plateau in the IIP3. This is because up to 400 MHz, the input current is completely absorbed by the OTA, hence both the swing at the input of the last stage and the g_m non-linearity are frequency independent. On the other hand, at higher frequency C_{in} absorbs part of the input current, lowering all types of distortion, including the one due to the output g_m. (cit. [16] ©2018 IEEE).* Notice

[3] This applies directly to g_m non-linearity. From the data in Table 3.1 it can be observed that, with a gain of about 10, the second stage g_{ds} non-linearity is of the same order of magnitude of its g_m non-linearity. Hence g_{ds} non-linearity is always negligible

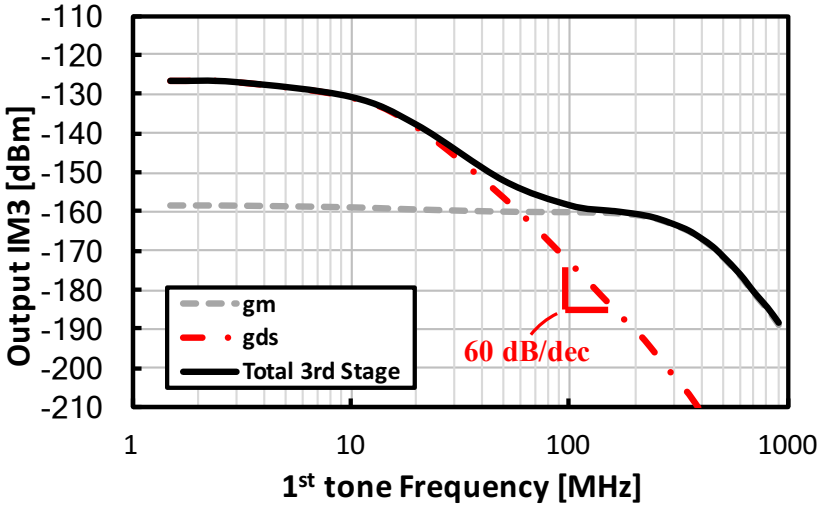

FIGURE 3.5: Non-linear contributors of the output stage

that, in a real receiver, the actual load seen by the TIA would be drastically smaller, i.e. below 100 fF (for an on-chip buffer or additional filtering stage as a load). *A smaller load results in a better linearity for the same OTA since the output stage needs to deliver less current*, resulting in a lower swing at its input node. *This means that the achieved IIP3 is smaller than the one achievable in the real receiver. Through simulation, 6 dB improvement in OOB IIP3 was demonstrated with 100 fF load capacitance.*

The above IM3 behaviour corresponds to the IIP3 shown in Figure 3.6, where the dominant source of distortion in each frequency range is indicated. Lowering the TIA trans-impedance gain would lower IM3 injection and improve IIP3 up to 60 MHz, i.e. where the third stage g_{ds} non-linearity dominates. Beyond this frequency, a larger output stage or higher gain in front of it are needed to further boost IIP3 (cit [16] ©2018 IEEE).

The proposed method also allows *to compute IM3 vs. f_{IM3} to find the worst case IB distortion energy due to blockers at different relative frequencies. To do this, the first tone is placed at 100 MHz and the second is moved so that f_{IM3} is swept within the TIA band. In Figure 3.7 we see that, as opposed to what generally happens, IM3 remains flat over almost all the TIA passband (cit. [16] ©2018 IEEE)*, following the frequency shape of the closed-loop output impedance.

This can be explained as follows:

1. *In the frequency range considered output stage non-linearity is the main contributor;*

2. *The two tones are sufficiently beyond ω_0 that the g_m non-linearity dominates;*

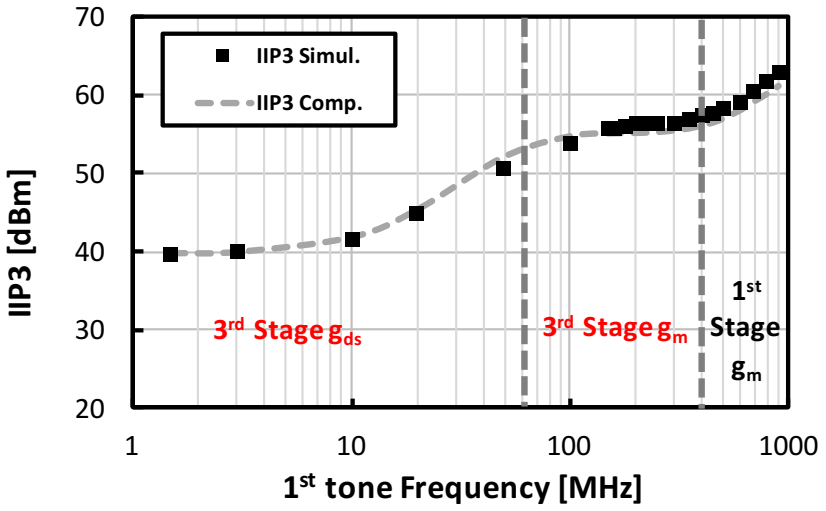

FIGURE 3.6: Simulated IIP3 of the TIA with the proposed OTA and dominating contributors

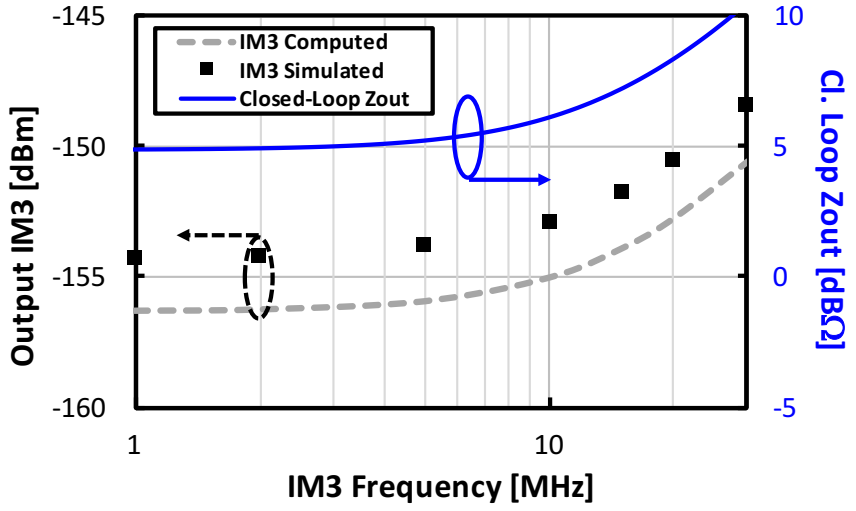

FIGURE 3.7: Simulated IM3 vs. IM3 frequency and closed-loop output impedance frequency shape

3. *The non-linearity injection at f_{IM3} is independent of the position of the tones and the non-linear current is directly injected into the output node;*

4. *The IM3 follows the frequency shape of the closed loop output impedance, which is almost flat in-band since the first OTA pole is near 20 MHz (cit. [16] ©2018 IEEE).*

3.4 Analysis of Miller-Compensated OTAs

The non-linearity model discussed above also applies to more traditional Miller - Compensated OTAs. In this section, a conventional Two-Stage Miller-Compensated OTA (MC) and a Three-Stage Nested-Miller-Compensated OTA (NMC) are included in the designed 20 MHz BW TIA and analysed from the non-linearity point of view. Because of the large number of variables and design parameters available, it is difficult to provide a fair comparison with the proposed OTA architecture. In this section a constant current consumption is kept. The same OTA stages used in Section 2.3.1 are employed, without any additional zeros in the loop. Miller-Capacitors are then added across these stages to achieve stability. Even if this may not represent an optimum design, it still provides good insights on the linearity behaviour of Miller-Compensated OTAs and on the differences with the proposed approach.

3.4.1 Two-Stage Miller-Compensated OTA

The analysis is first applied to a TIA with a Two-Stage MC OTA. The first and the last stage of the OTA of Section 2.3.1 are re-used and stability is achieved by placing a 0.5pF capacitor across the output stage, without putting additional zeros in the loop. A schematic picture of the TIA with MC OTA is shown in Figure 3.8.

Since in the original OTA the intermediate stage was very low power-consuming, its removal just lowers current consumption by 6.6%. The non-linear coefficients for the MC are the same as reported in Table 3.1. The open-loop output impedance at the intermediate node at $f_{IM3} = 1MHz$ ($Z_{o,OL,1}(1MHz)$) is 14.9 $k\Omega$, slightly smaller than the value in Table 3.1, because of the effect of Miller capacitor. The open loop output impedance $Z_{o,OL,3}(1MHz)$ is $1.9k\Omega$, as in the previous case. The closed-loop voltage gain from the input to the intermediate nodes of the MC is given in Figure 3.9, together with $TF_{1\rightarrow out}$, that is 22 dB at 1 MHz.

The simulated and computed output IM3 with -20 dBm input tones is reported in Figure 3.10.

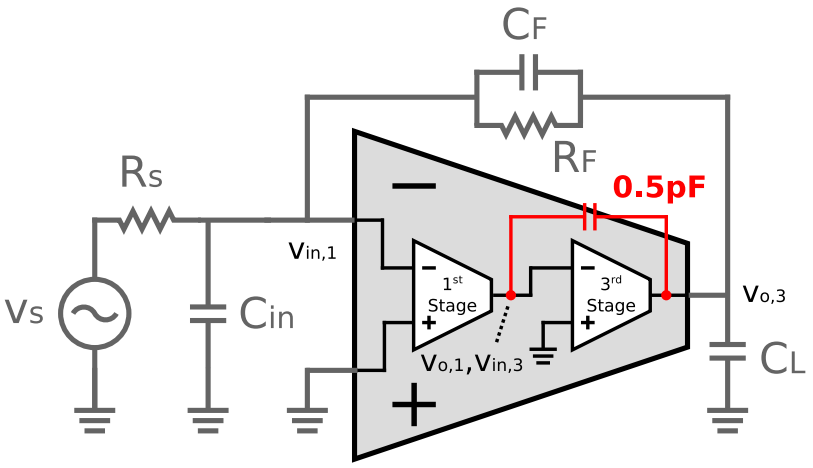

FIGURE 3.8: Schematic representation of the TIA with Two-Stage MC OTA

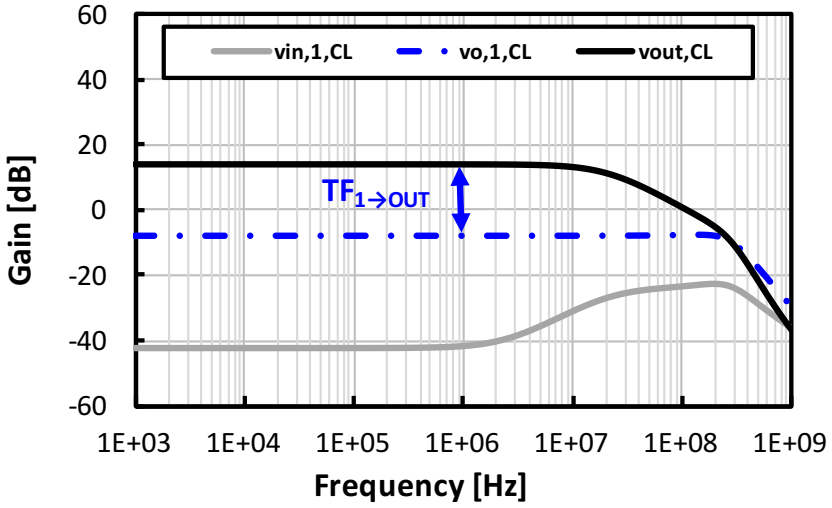

FIGURE 3.9: Closed-Loop gain at the intermediate nodes of the MC vs. frequency

At low frequency, the output stage is the dominant IM3 contributor, in turn dominated by g_{ds} non-linearity. The g_{ds} non-linear coefficient and the voltage swing on the output node are the same as in the proposed OTA, so the IM3 *injected* by the output stage is the same. However *compression* is lower in the MC. In fact, the OTA low frequency gain is about 20 dB lower than in the Three-Stage architecture, and so is the Gloop. Hence, a corresponding increase in the closed-loop output impedance is observed, which produces a 20-dB increase in IM3. For input tones above ω_0 the reduced swing at the output produces a drop in the IM3. However, IM3 stops decreasing around 20 MHz, in contrast with the proposed solution. The OTA gain, in fact, drops at 20 dB/decade above 2.5 MHz due to the Miller-Capacitor. This makes the swing at the input node and the input stage distortion to grow with 20 and 60 dB/dec slope, respectively. Near 20 MHz then, the first-stage IM3 overtakes the distortion of the output stage. For very

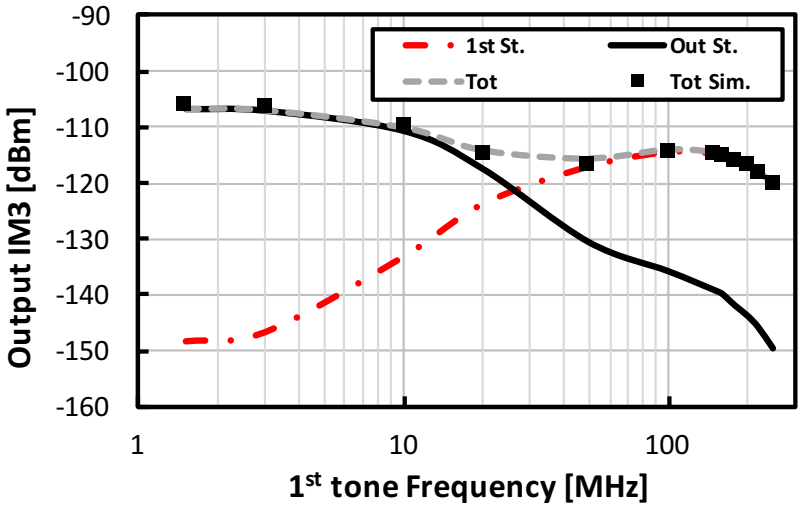

FIGURE 3.10: Simulated and computed IM3 at the TIA output vs. input tones frequency with MC OTA and contribution of OTA stages

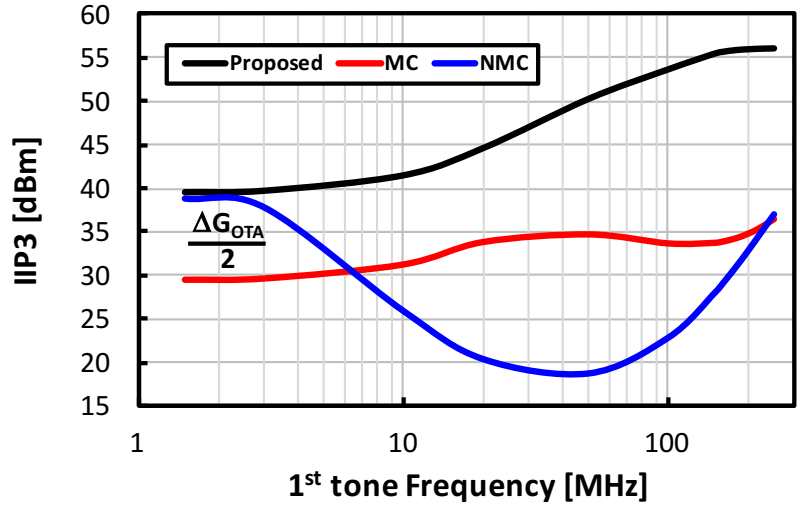

FIGURE 3.11: Simulated IIP3 of the TIA, with the proposed, MC and NMC OTA

high frequency, where the input capacitance starts filtering the input signal, the IM3 curve decreases again. The previous results correspond to the IIP3 shown in Figure 3.11. The IIP3 is flat up to ω_0 and increases beyond that, with the same shape as for the OTA of section Section 2.3.1. The MC IIP3, however, starts from a value $\Delta G_{OTA}|_{dB}/2$ lower (on a dB scale), where $\Delta G_{OTA}|_{dB}$ is the gain difference in dB of the two OTA topologies (20 dB). The MC IIP3, however, stops increasing around 20 MHz, stays flat for a while and starts going down because of the effect of input-stage g_m non-linearity. At very high frequency the IIP3 resumes growing due to the input capacitance filtering.

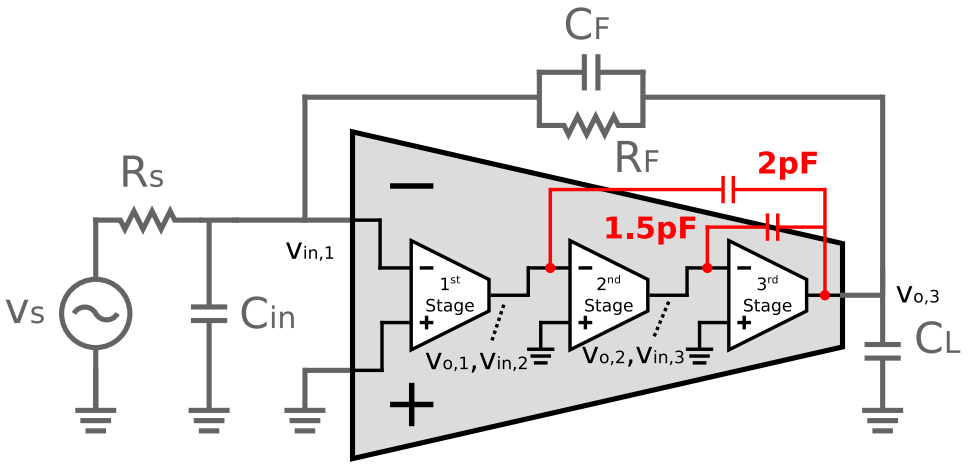

FIGURE 3.12: Schematic representation of the TIA with Three-Stage NMC OTA

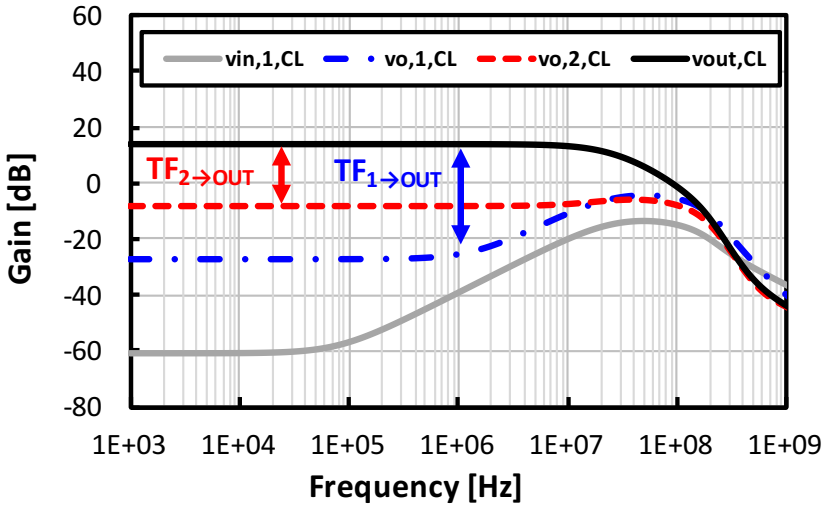

FIGURE 3.13: Closed-Loop gain at the intermediate nodes of the NMC vs. frequency

3.4.2 Three-Stage Nested-Miller-Compensated OTA

A 20-MHz-BW TIA based on a Three-Stage Nested Miller Compensated (NMC) OTA is considered in this section. The three stages are exactly the same as in Section 2.3.1, with equal current consumption. A 1.5-pF capacitor is placed across the output stage and a 2-pF capacitor closes the outermost loop, as schematically reported in Figure 3.12.

The simulated closed-loop gain at the intermediate nodes of the OTA is reported in Figure 3.13, while simulated and computed output IM3 for -20 dBm input tones is plotted in Figure 3.14, where the different IM3 contributors are isolated.

For very low frequency the output stage g_{ds} dominates non-linearity as in the MC and proposed OTAs. Beyond the dominant pole of the NMC OTA, which lies at a much

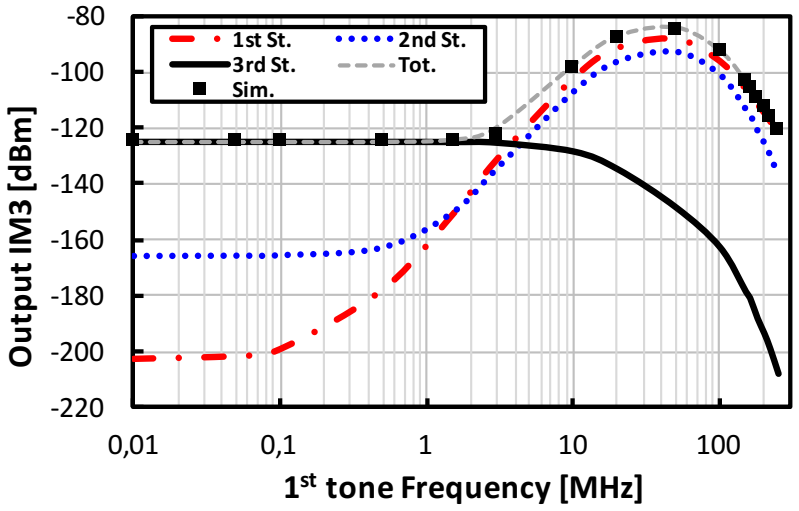

FIGURE 3.14: Simulated and computed IM3 at the TIA output vs. the input tones frequency with NMC OTA and contribution of OTA stages

lower frequency than the MC, the swing at the virtual ground node starts increasing with 20 dB/decade slope and g_m non-linear contribution of the first stage starts growing with 60 dB/decade, overwhelming the output stage contribution above 3 MHz. The plot of Figure 3.14 corresponds to the IIP3 given in Figure 3.11, where a comparison with the previously discussed topologies is done. For In-band signals IIP3 is the same as in the proposed Three-Stage-OTA. This is because in this frequency range:

1. The g_{ds} of the output stage dominates non-linearity;
2. The two OTAs use the same output stage and have the same output swing, producing the same amount of IM3 *injection*;
3. The closed-loop output impedance at f_{IM3} is the same, producing equal *compression*.

Beyond about 3 MHz the two curves diverge, because the NMC OTA starts being dominated by the input stage g_m non-linearity and its IIP3 drops with nearly 30 dB/decade slope. Notice that above 5 MHz the NMC OTA IIP3 becomes even worse than that of the MC OTA.

In conclusion, both Three-Stage OTAs achieve better In-Band IIP3 than the MC OTA, thanks to their larger loop gain. At higher frequency the low bandwidth of the NMC OTA makes its IIP3 to degrade earlier, eventually getting worse than that of the MC OTA. On the other hand the proposed OTA maintains a large gain and a low input swing over broad frequency, giving good linearity even for OOB signals.

Chapter 4

Design of a 130-MHz-BW TIA based on Modified Regulated-Cascode

As demonstrated in the previous chapters, closed-loop TIA solutions based on shunt feedback are promising for linearity and noise. However, if a closed loop TIA bandwidth in the order of 100-200 MHz is targeted, loop gain GBW of several GHz becomes necessary. This goal can be reached either burning large amount of current in the OTA or adopting some unconventional compensation technique like the one proposed in Chapter 2. An alternative approach to TIA design is based on "Open-Loop" architectures like the simple Common-Gate (CG) topology or the Regulated-Cascode, which are good candidates to satisfy the large bandwidth requirement of 5G, with reasonable power consumption and less stability concerns. In this chapter the Regulated-Cascode is modified by adding positive capacitive feedback, achieving a 3^{rd} order low-pass current filtering with 130-MHz-BW, consuming only 6 mA current. The proposed circuit is integrated in a Mixer-First Receiver, whose performance is demonstrated through chip measurements.

4.1 Common Gate "pipe" filter

In Chapter 1 it was highlighted how carrier bandwidths in excess of 100 MHz are expected for the next generation of mobile networks (5G). To implement TIAs with such a large bandwidth, current-domain filtering represents a viable way and Common-Gate (CG) architecture proves very suitable. One possible CG-based implementation was

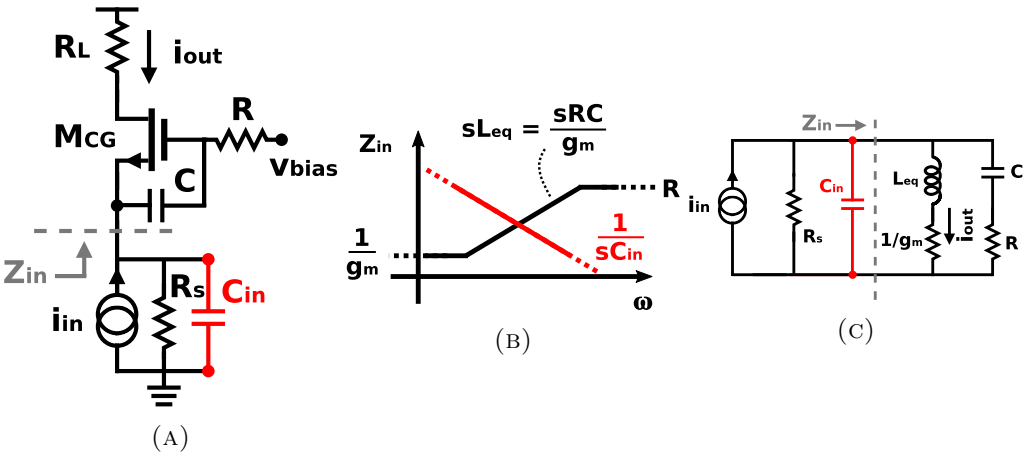

FIGURE 4.1: Schematic representation of simple pipe CG filter: a) actual circuit; b) Frequency behaviour of Z_{in}; c) Equivalent RLC model.

already proposed in [48] to realise wide-band RF filtering for TV tuners. The operating principle of the filter is graphically explained in Figure 4.1. In detail, the circuit schematic is depicted in Figure 4.1a, where the input signal is provided through an equivalent Norton generator with finite impedance R_S, modelling in a very simple way the driving impedance provided by the LNTA and mixer.

The frequency behaviour of the circuit can be explained as follows. For very low frequency signals, where capacitors are open, the CG operates as a simple cascode, showing input impedance $Z_{in} = 1/g_m$. At higher frequency capacitance C starts shunting the v_{gs} of CG transistor, producing an inductive-like impedance behaviour looking into the source of M_{CG}. A graphic representation of this frequency behaviour is schematically drawn in Figure 4.1b. If the shunt capacitor C_{in} is placed in parallel with Z_{in}, the circuit becomes equivalent to the RLC network depicted in Figure 4.1c, where it is easy to demonstrate that the current flowing through the equivalent inductor L_{eq} (actually the CG) is a low-pass filtered version of i_{in}, with a second order transfer function. The exact transfer function of the obtained biquad can then be computed:

$$H_{CG}(s) = \frac{i_{out}}{i_{in}} = \frac{g_m R_s}{(1+g_m R_s)\left(1 + s\frac{RC+R_sC+R_sC_{in}}{1+g_mR_s} + s^2\frac{RCR_sC_{in}}{1+g_mR_s}\right)} \tag{4.1a}$$

$$\omega_0 = \sqrt{\frac{1+g_mR_s}{RCR_sC_in}} \tag{4.1b}$$

$$Q = \frac{\sqrt{1+g_mR_s}}{RC+R_s+R_sC_{in}}\sqrt{RCR_sC_{in}} \tag{4.1c}$$

where g_m is the CG trans-conductance, while the other parameters are indicated in Figure 4.1a. From the equivalent circuit of Figure 4.1c, it can be inferred that the source resistance R_s appears in parallel to the equivalent inductor given by the CG, possibly

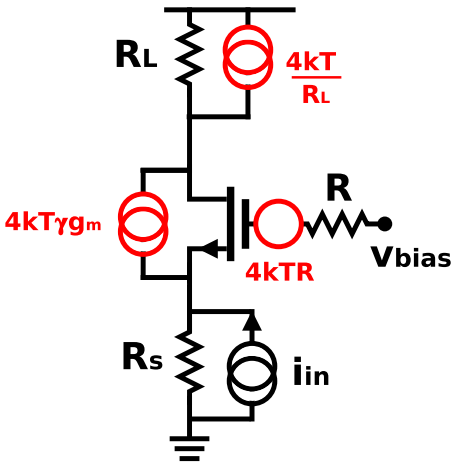

FIGURE 4.2: Circuit for low-frequency noise analysis of the CG

degrading the Q of the complex-conjugate (CC) poles in the biquad. This aspect was completely neglected in [48], since the circuit was driven by a trans-conductor having large output impedance. However, in the context of TIAs for 5G, resistance R_s becomes relevant, since the equivalent driving impedance provided by the mixer tends to reduce as the LO frequency is raised [39] and the situation becomes even more critical if a Mixer-First receiver is adopted, because the mixer is directly driven by the low 50Ω impedance of the antenna.

Noise analysis can be performed looking at the circuit of Figure 4.2, where the different noise contributor generators are highlighted. All the reported noise contributors are referred to the input current, obtaining the following expressions:

$$\overline{i^2_{in,gm}} = \frac{4kT\gamma}{g_m R_s^2} \tag{4.2a}$$

$$\overline{i^2_{in,R_L}} = \frac{4kT}{R_L}\frac{(1+g_m R_s)^2}{g_m^2 R_s^2} \tag{4.2b}$$

$$\overline{i^2_{in,R}} = \frac{4kTR}{R_s^2} \tag{4.2c}$$

In Chapter 2 it was already explained the importance of implementing a TIA with low input impedance. If this condition is imposed on the CG topology, a large current is needed in the CG branch, to maximize its g_m. This potentially represents an issue for noise, since the limited supply voltage would require to lower resistance R_L, making its noise contribution dominant, as can be inferred from (4.4c). It follows that CG "pipe" is suitable for achieving increased bandwidth, but suffers from load resistance noise drawback and limited Q. These two points will be addressed in the following by adding some circuit modifications.

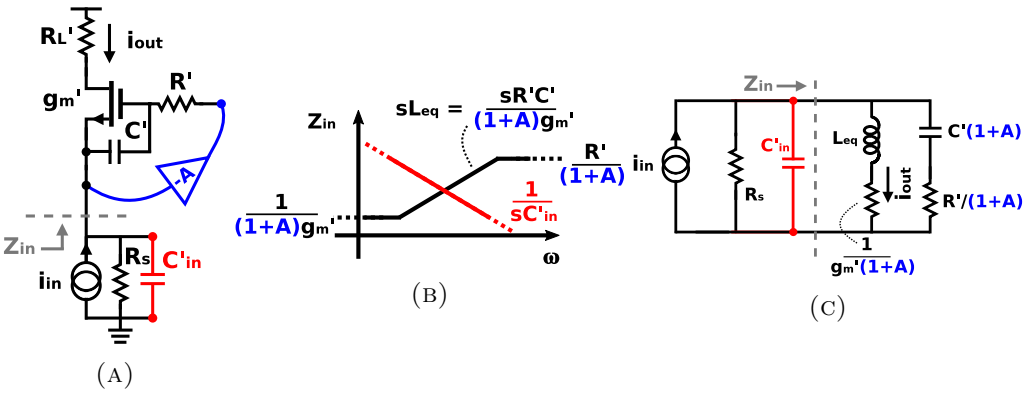

FIGURE 4.3: Schematic representation of Regulated-Cascode filter: a) actual circuit; b) frequency behaviour of Z_{in}; c) equivalent RLC model.

4.2 Regulated-Cascode Filter

The simple "pipe" CG filter can be modified as shown in Figure 4.3a. The resulting topology becomes similar to the so-called Regulated-Cascode architecture, which was already used in [49], [50] and [51] to implement very high frequency filters.

Such topology is simply obtained by adding the amplifier A, with finite output impedance R, between the source and the gate of the CG "pipe". It can be inferred that the low-frequency input impedance of the obtained circuit is equal to $1/(g_m(1+A))$. Such input impedance value is reduced by the factor (1+A) compared to the simple CG, meaning that the current in the CG branch of the Regulated-Cascode can be reduced by the same amount, while obtaining an input impedance equal to the simple CG "pipe" filter.

The frequency behaviour of the input impedance Z_{in} is the same as the "pipe" CG filter, with the only difference that the impedance associated with CG, R and C is scaled by $(1+A)$, as sketched in Figure 4.3b. The resulting *current* transfer function (i_{out}/i_{in}) becomes equal to:

$$H_{reg\_casc}(s) = \frac{i_{out}}{i_{in}} = \\ = \frac{g'_m R_s (1+A)}{(1+g'_m(1+A)R_s)\left(1+s\frac{R'C'+R_sC'(1+A)+R_sC'_{in}}{1+g'_m(1+A)R_s}+s^2\frac{R'C'R_sC'_{in}}{1+g'_m(1+A)R_s}\right)} \tag{4.3a}$$

$$\omega_0 = \sqrt{\frac{1+g'_m(1+A)R_s}{R'C'R_sC'_{in}}} \tag{4.3b}$$

$$Q = \frac{\sqrt{1+g'_m(1+A)R_s}}{R'C'+R_s(1+A)C'+R_sC'_{in}}\sqrt{R'C'R_sC'_{in}} \tag{4.3c}$$

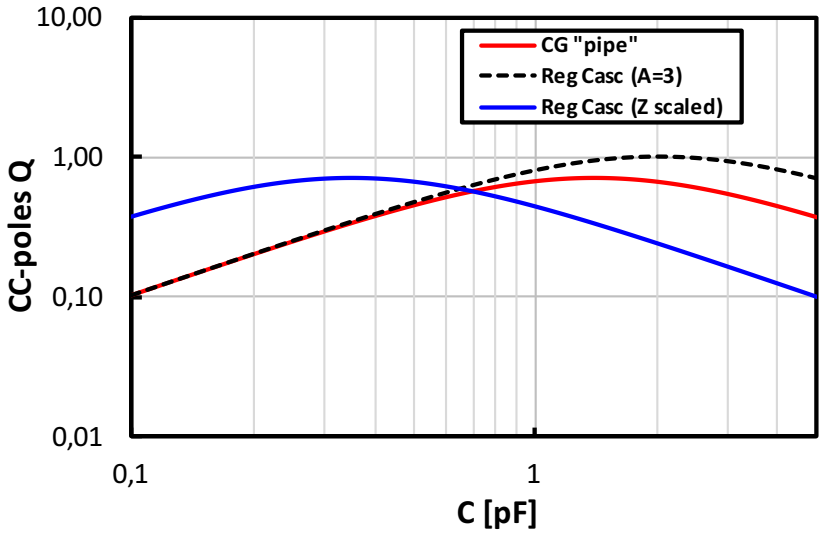

FIGURE 4.4: Q vs. C for CG and Regulated-Cascode with constant $\omega_0/2\pi = 160$ MHz

From Figure 4.3c it can be intuitively deduced that potential improvement in the achievable Q can be obtained with Regulated-Cascode. Amplifier A in fact scales down the impedance of the equivalent RLC network that models Z_{in} (Figure 4.3c), reducing the effect of the source impedance R_s. This is graphically shown in the plots of Figure 4.4, where the Q of CC-poles in a simple CG "pipe" filter (red line) and in a Regulated-Cascode with $A = 3$ is calculated versus capacitance C (C' in Regulated Cascode), changing C_{in} (C'_{in}) to keep constant ω_0. If A is added keeping $g'_m = g_m$ and $R' = R$ (dashed line), higher Q can be obtained. However, if a constraint exists on the input impedance, no benefit is obtained from this point of view, since the original impedance level of Z_{in} has to be restored acting on g'_m, R' and C'. This situation is depicted in Figure 4.4 (blue line), where g'_m is lowered by $(1 + A)$ and R' is increased by the same factor. It is easy to observe that the maximum achievable Q is the same. A possible solution for this issue will be presented in the following section.

The Regulated Cascode can however bring some benefits in terms of noise. In a similar manner as done for the simple CG, the input-current-referred noise contributors are computed:

$$\overline{i^2_{in,gm'}} = \frac{4kT\gamma}{(1+A)^2 g'_m R_s^2} \tag{4.4a}$$

$$\overline{i^2_{in,A}} = \frac{4kT}{g_{m,A} R_s^2} \frac{(A)^2}{(1+A)^2} \tag{4.4b}$$

$$\overline{i^2_{in,R'_L}} = \frac{4kT}{R'_L} \frac{(1+(1+A)g'_m R_s)^2}{(g'_m(1+A)R_s)^2} \tag{4.4c}$$

$$\overline{i^2_{in,R'}} = \frac{4kTR'}{R_s^2(1+A)^2} \tag{4.4d}$$

where A is assumed to be a simple Common-Source (CS) with trans - conductance $g_{m,A}$ and load resistance R'. Some assumptions are now done in order to perform some noise performance comparison between the two architectures. First, it is assumed that the low-frequency input impedance of the two topologies remains the same, i.e. that $g'_m = (1+A)g_m$. Second, it is assumed that the current saved in the Regulated-Cascode CG branch is used in A, so that $g_{m,A} = g_m \cdot A/(1+A)$ and that $R' = (1+A)/g_m$. Third, it is assumed the voltage drop on the load resistor in CG and Regulated-Cascode is the same, i.e. $R'_L = R_L/(1+A)$. Equations (4.5) become:

$$\overline{i^2_{in,gm'}} = \frac{4kT\gamma}{(1+A)g_m R_s^2} \tag{4.5a}$$

$$\overline{i^2_{in,A}} = \frac{4kT}{g_m R_s^2}\frac{A}{1+A} \tag{4.5b}$$

$$\overline{i^2_{in,R'_L}} = \frac{4kT}{R_L(1+A)}\frac{(1+g_m R_s)^2}{(g_m R_s)^2} \tag{4.5c}$$

$$\overline{i^2_{in,R'}} = \frac{4kT}{g_m R_s^2(1+A)} \tag{4.5d}$$

It can be observed from (4.5a) that the noise contributed by the CG transistor is reduced by the factor (1+A) in the Regulated-Cascode topology. However, also the additional noise contributed by amplifier A must be taken into account in the latter topology. The total noise given by (4.5a) and (4.5b) results to be exactly equal to (4.2a), so that, under the made assumptions, no benefit is produced by the Regulated-Cascode in transistors noise. On the contrary it is clear from (4.4c) and (4.5c) that noise contributed by the load resistor is actually lowered by the factor (1+A). Regarding noise contribution of resistor R, a fair comparison is difficult, since in the Regulated-Cascode its value is tied to the gain of the boosting stage A. However, if it is assumed that $R' = (1+A)R$, so that Q is the same in the two topologies, also noise contribution of resistor R' is lowered by (1+A).

4.3 Improved Regulated Cascode Filter

In the previous section it was concluded that the Regulated-Cascode reduces the noise contribution of load resistors but doesn't solve the issue of low achievable Q for the CC poles, producing limited selectivity in wireless receivers. This point is addressed here modifying the Regulated-Cascode architecture as shown in Figure 4.5. The Amplifier A is realised as a differential pair made of transistors $g_{m,A}$ and resistors $R_{A,x}$. Capacitors

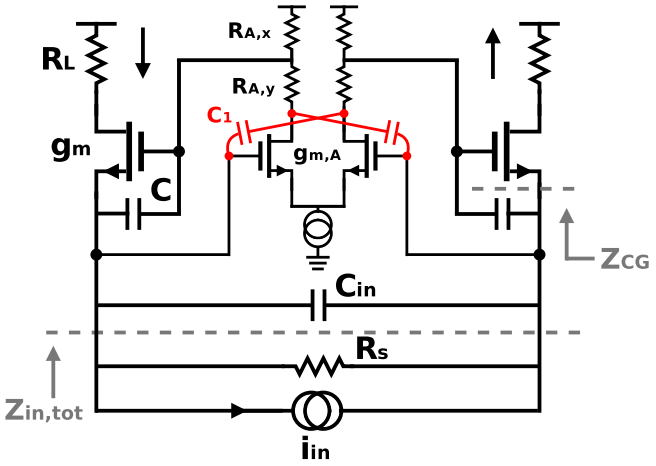

FIGURE 4.5: Proposed Modified Regulated-Cascode

C_{pfb} are connected in positive feedback to the high gain node created in amplifier A by adding resistors $R_{A,y}$. These capacitors are responsible for a two-fold effect. First, when computing Z_{in}, capacitance C_{pfb} produces a voltage drop on the v_{gs} of the CG transistor which has two poles and one zero. This creates a frequency behaviour for the impedance looking into the CG that rises with 40 dB/decade slope and then reduces to 20 dB/decade at higher frequency, as shown in the plot of Figure 4.6 (blue line). At the same time, C_{pfb} is reported as a negative shunt capacitance at the TIA input, so that the total equivalent input capacitance is reduced with respect to C_{in} for low frequency, increasing with 20 dB/decade near the filter cut-off and converging to C_{in} for higher frequency (green line of Figure 4.6). The resulting overall input-impedance of the TIA (red line of Figure 4.6) shows a 40 dB/decade drop near the cut-off frequency. The combination of the aforementioned effects produces two benefits from the selectivity point of view. First, the resulting *current* transfer function has three poles and one zero at higher frequency. Second, the achievable Q for the CC poles is increased with respect to the basic Regulated-Cascode filter.

The actual adopted filter implementation is reported in Figure 4.7. Common-Gate is realised as a stacked P-N CG, used to avoid tail current sources and their associated noise contribution. The boosting stage A is realised as a PN differential pair to save current (Only P-side is reported in the picture for the sake of clarity). Resistive load is made through the diode connected transistor $M_{x,1/2}$ (degenerated by R_{deg} to increase the gain of the stage), while the two different-gain nodes are obtained by connecting resistors R_1 and R_2 to form a voltage partition. The differential load of the boosting stage is given by $R_1 + R_2$, in parallel with the diode connected transistors $M_{x,1/2}$, whose equivalent $1/g_{m,x}$ is raised by the factor $(1 + R_1/R_2)$, in addition to being degenerated by resistor R_{deg}. The CM load of the stage, instead, is just made of the diode-connected

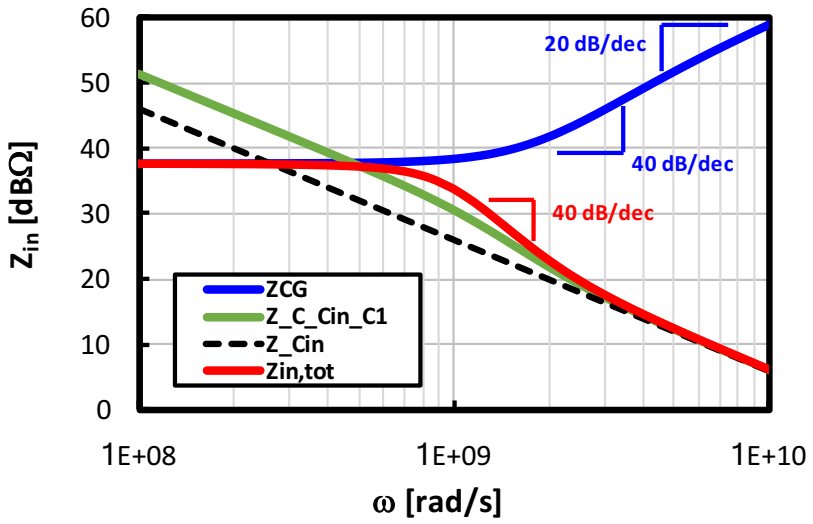

FIGURE 4.6: Input Impedance frequency behaviour for the Modified Regulated-Cascode

transistor $M_{x,1/2}$. It follows that the bias current in the CG branch is well defined, being a copy of the one flowing through M_x. A single CMFB loop is then necessary to set the source voltage of $M_{x,1/2}$ to $V_{dd}/2$. If transistors in the CG branch are properly sized, then their source voltage (the TIA input) also is automatically set. It must be noticed that the gate-source voltage drop on the diode-connected transistors $M_{x,1/2}$ doesn't leave any voltage room to maintain transistors $M_{A,P/N}$ in linear region. This is clear from Figure 4.8, where the detailed P-N boosting stage is reported. To overcome this issue a constant current i_{inj} is forced through resistor R_1, as shown in Figure 4.8, so as to lower M_x drain voltage (and rise it in the N-side), leaving enough room for M_A to properly operate. The output signal currents in the CG ($i_{out,p}/i_{out,n}$ in Figure 4.7) are recombined through two current mirrors (one P and one N), with 1:3 mirroring factor, producing the total output current i_{out}. The current mirror introduces a *voltage* high frequency pole, which cancels the zero in the *current* transfer function, so that the resulting overall transfer function of the TIA has a 3rd order low-pass frequency shape up to very high frequency. It's important to notice that the current is recombined on a high impedance node, leaving the possibility of adding one additional pole in the *voltage* transfer function.

The filter is designed to implement the TIA for a Mixer-First Receiver (MF-RX), which is schematically drawn in Figure 4.9. The chosen design parameters are listed in Table 4.1. CG g_m and gain A of the boosting stage are sized to achieve an in-band differential input impedance close to 100 Ω, which is transformed to 50 Ω at the RF port by the double-balanced mixer in the MF-RX, in line with the analysis performed in

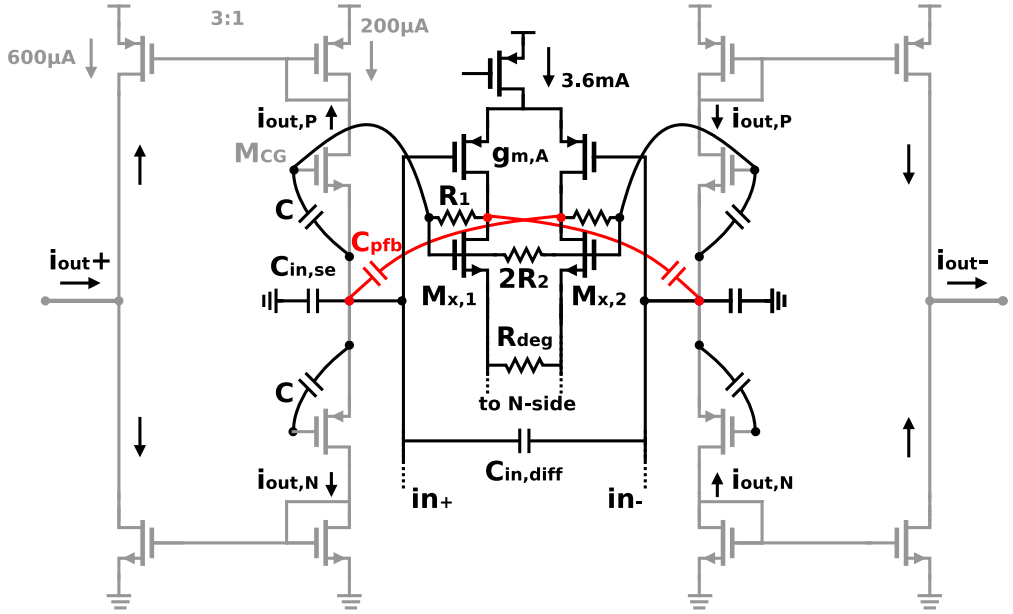

FIGURE 4.7: Actual schematic of the proposed filter

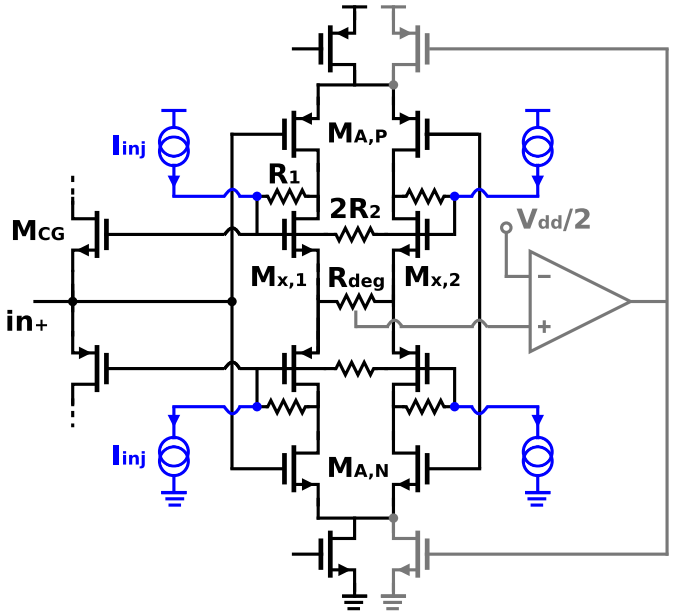

FIGURE 4.8: Detailed representation of the P-N Differential boosting (A) stage

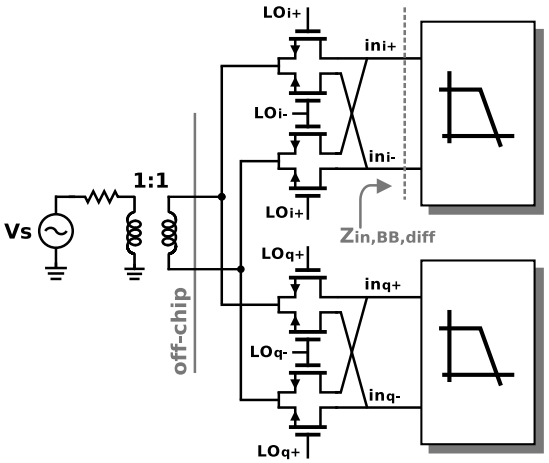

FIGURE 4.9: Overall Mixer-First RX schematic representation

Parameter	Value	Unit
$g_{m,CG}$	3	mS
$g_{m,A}$	35	mS
$g_{m,X}$	38	mS
$C_{in,se}$	10	pF
$C_{in,diff}$	36	pF
C	800	fF
C_1	3.2	pF
$R1$	1.5	$k\Omega$
$R2$	0.9	$k\Omega$
R_{deg}	110	Ω

TABLE 4.1: Modified Regulated-Cascode components size

[52]. The filter passive components, listed in Table 4.1, are sized to realise a 3rd order, 130-MHz-BW Butterworth filter.

4.4 MF-RX Implementation and Measurements

The complete Mixer-First RX prototype was fabricated in tsmc 28nm HPC technology. The chip photograph is shown in Figure 4.10. Core area occupation is 0.16mm^2, which is dominated by filter passive components.

Output buffers were integrated on-chip to prevent the TIA from being loaded by board traces and external probes. Buffers were designed to have 0-dB gain and a low-pass transfer function with a single-pole at 160 MHz, which was introduced to overcome the probe linearity limitations for out-of-band signals, where high linearity has to be measured. Buffers don't limit linearity and noise of the circuit and their transfer function and current consumption were de-embedded from measurements. The chip was

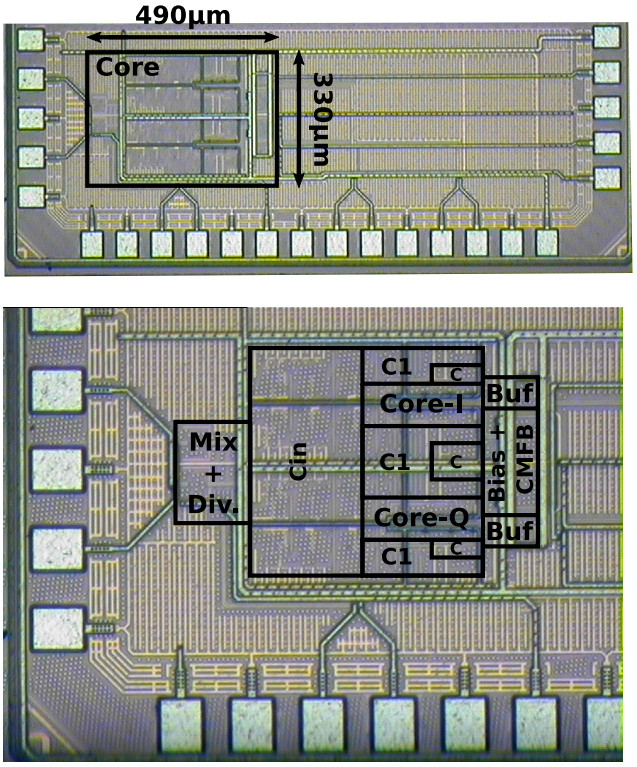

FIGURE 4.10: Chip photograph of the implemented MF-RX

mounted and wire-bonded on a PCB for measurements and the input differential signal was provided through an on-board 1:1 balun, whose losses were de-embedded. Clock was provided through an external signal generator working at $2xf_{LO}$, while I and Q phases were generated through an on-chip frequency divider.

Input matching was verified performing an S11 measurement through an *Agilent E8361C PNA* Network Analyzer. Results are shown in Figure 4.11 for several LO frequencies. As expected in a MF implementation, good matching was obtained around the LO frequency, where a relatively deep notch is observed, tracking the LO frequency. Input matching better than 12 dB was achieved over the measured range, which is limited at higher frequency to 2 GHz by the limited on-board RF balun operative range.

Receiver Gain was measured adopting the measurement setup shown in Figure 4.12, while a software routine was implemented in *NI Labview* to sweep the signal generator frequency. Gain vs. IF frequency is reported in Figure 4.13 for a 2-GHz LO. In-band gain at $f_{LO} = 2GHz$ is 32.4 dB and a 3rd order 130-MHz bandwidth Butterworth filter was obtained. After de-embedding the buffer transfer function a steep 60 dB/dec slope is achieved over the entire BB measured frequency range (up to 500 MHz). In-band gain variation vs. RF frequency was performed as well, showing a slight increase going to lower frequency (less than 2 dB at 1 GHz LO frequency). The plot is shown in Figure 4.14.

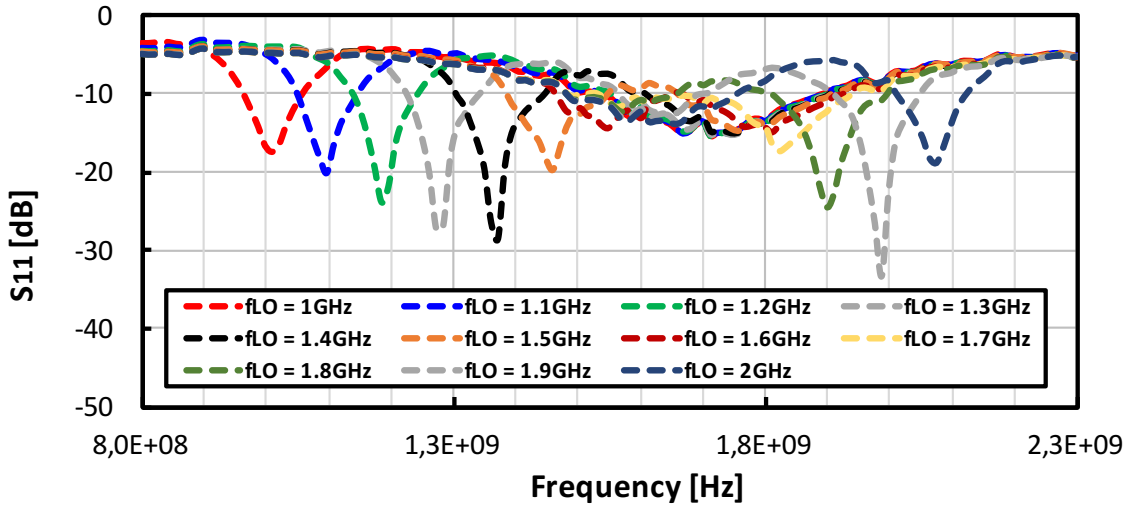

FIGURE 4.11: S11 measurement of MF-RX

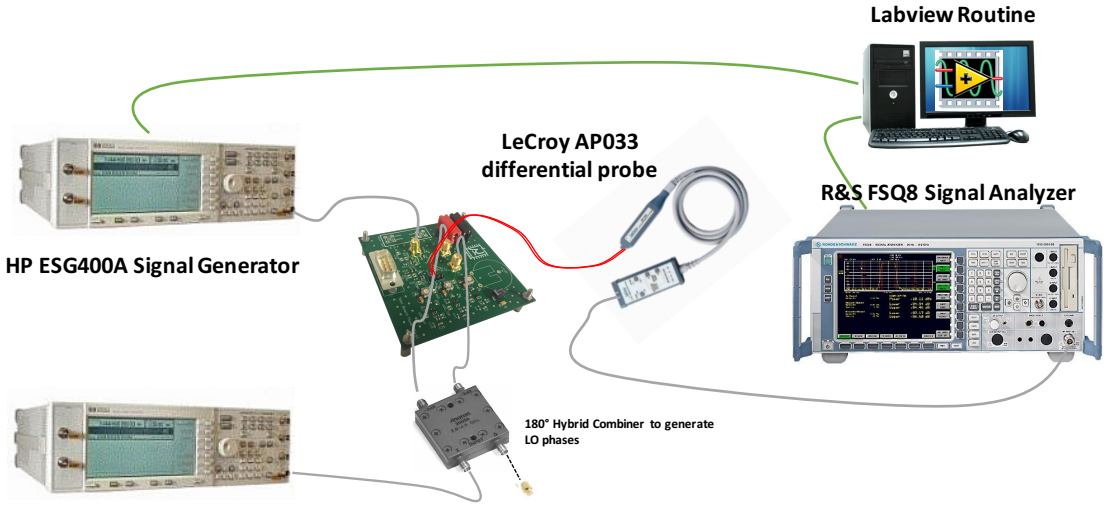

FIGURE 4.12: Instruments setup used for gain measurement

Linearity of the MF-RX was tested through a two-tones test, which was performed combining the signals from two *HP ESG4000A* signal generators by means of a *Suhner 4901 19.a* power combiner. In order to avoid linearity limitation for OOB tones, on-chip buffer was designed to have a single pole transfer function with 160-MHz bandwidth, which was de-embedded from measurements. In addition 20 dB of attenuation was placed in front of the probe, i order to lower its injected IM3. IIP3 was tested for different offset frequencies. In Figure 4.15 IIP3 is shown as function of the offset frequency Δf of the first tone with respect to $f_{LO} = 2GHz$. Second tone is placed at $f_{LO} - 2\Delta f + 10MHz f$ to maintain IM3 constant at 10 MHz (at BB). In band IIP3 is -14dBm. OOB IIP3 increases very steeply reaching +21 dBm at

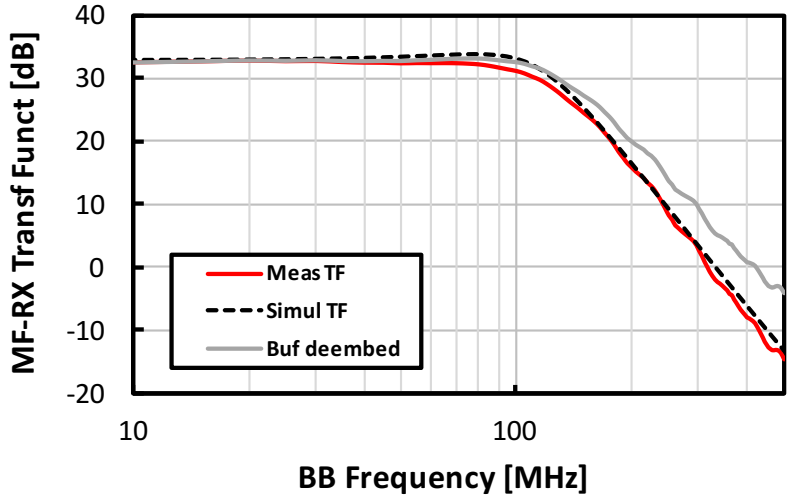

FIGURE 4.13: Measured MF-RX gain vs. IF frequency

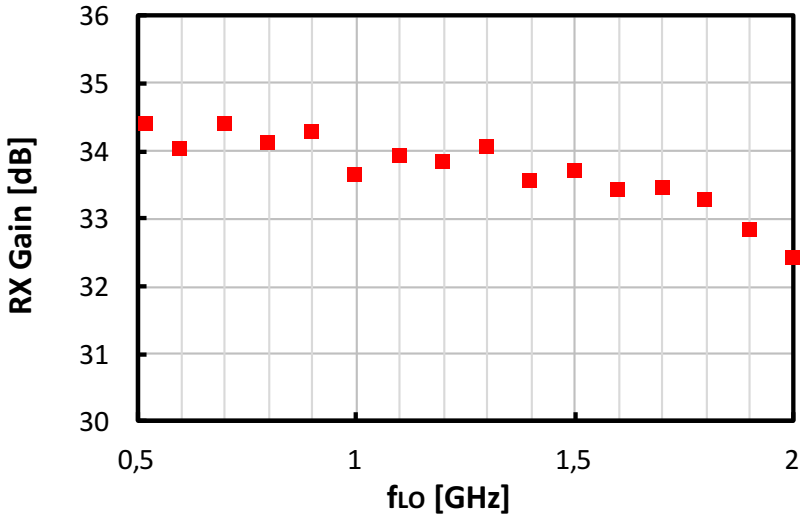

FIGURE 4.14: Measured MF-RX in-band gain vs. LO frequency

$\Delta f = 400MHz (\Delta f / f_{BW} = 3)$. Fundamental and Input-Referred (IR) IM3 power vs. tones power is shown in Figure 4.16, for two tones at 400MHz and 790MHz offset from the 2-GHz LO, demonstrating the expected IM3 slope (3 dB/dB) in the extrapolation point. For higher offset frequencies IIP3 saturates to +22 dBm, being limited by the mixer. This was confirmed through simulation of the MF-RX with a linearized model of the switch, showing a much better OOB IIP3 of +32 dBm, as reported in Figure 4.15. This was also confirmed performing an IIP3 measurement with the LO divider supply voltage increased to 1.4 V, achieving an OOB IIP3 of +25 dBm. As demonstrated by other implementations, this value does not represent a fundamental limit and can be

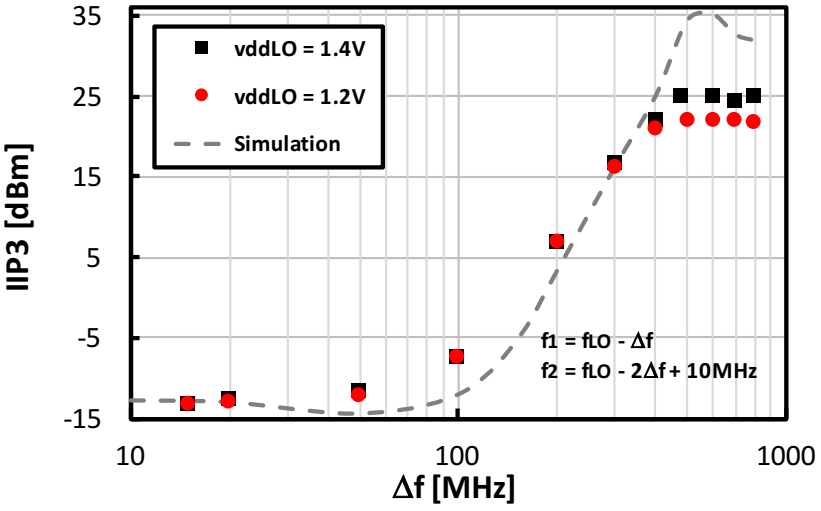

FIGURE 4.15: Measured IIP3 vs. first tone offset Δf

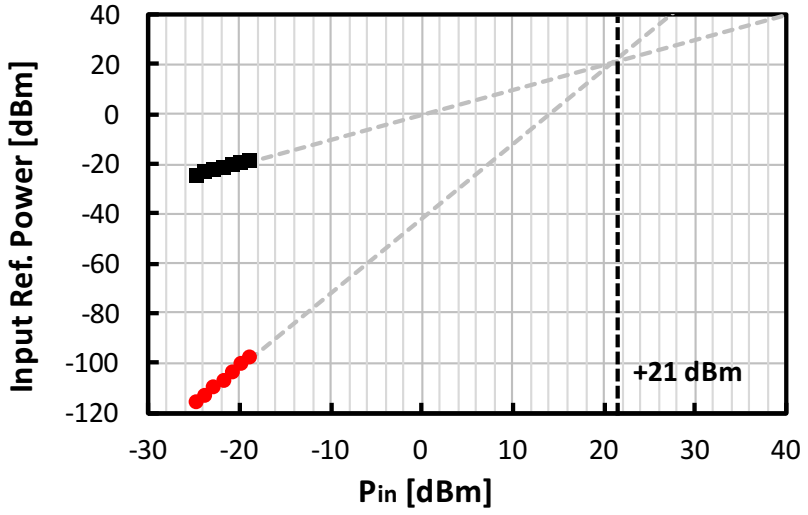

FIGURE 4.16: Input Referred Fundamental and IM3 power vs. tones input power

raised at the cost of higher current consumption in the clock distribution circuitry.

IIP2 was measured in a similar way as IIP3. IIP2 vs. Δf is reported in (Figure 4.17). In band IIP2 is +30 dBm and it increases to +70 dBm at $\Delta f = 400MHz$, as shown from IR fundamental and IM2 vs tones power in Figure 4.18.

Using the same measurement setup adopted for linearity also compression performance was tested. First, compression on an In-Band (IB) signal was measured sweeping the power of the input signal at $f_{LO} + 50MHz$ and observing the down-converted signal at the output of the MF-RX. From Figure 4.19 it can be seen that the gain compresses

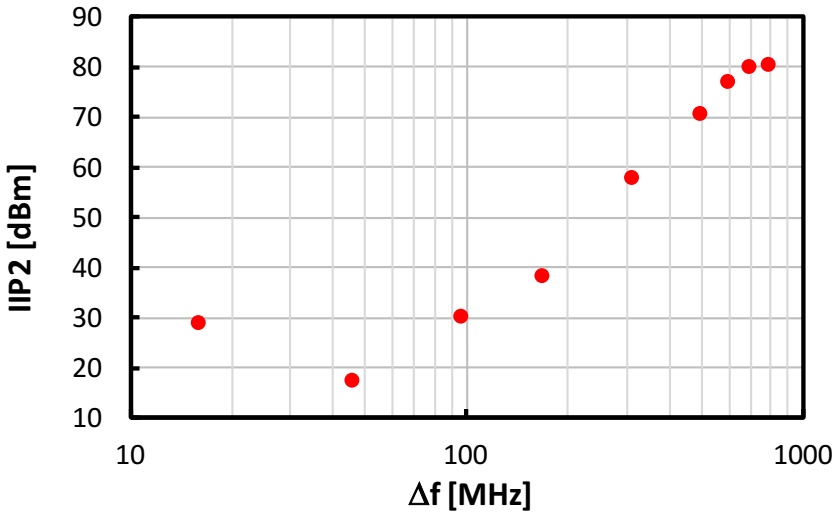

FIGURE 4.17: Measured IIP2 vs. first tone offset Δf

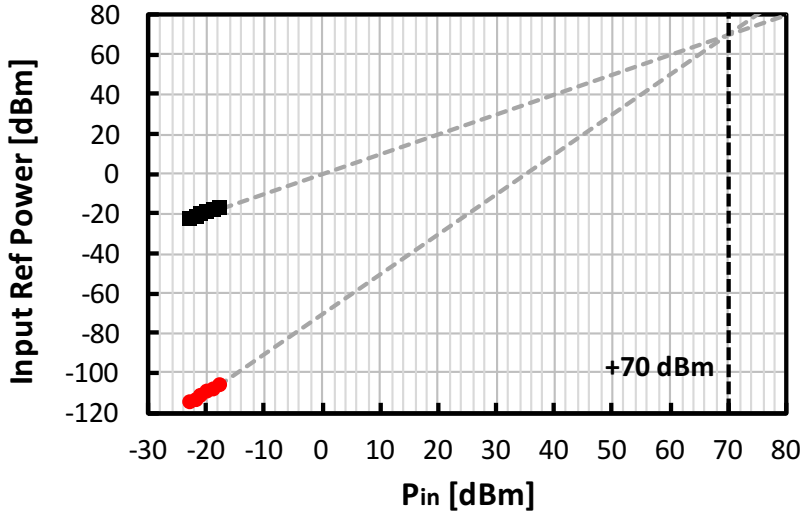

FIGURE 4.18: Input Referred Fundamental and IM2 power vs. tones input power

by 1 dB for a -27.5 dBm input signal. One of the main requirements in the design of wide-band RXs is good resilience to OOB interferers. An important metric is the so-called blocker 1dB compression point (B1dB), representing the IB small-signal gain compression as function of the power of a big OOB blocker. Small-signal gain was tested with blocker offset frequencies (with respect to LO) of $400MHz(\Delta f/f_{BW} = 3)$ and $800MHz(\Delta f/f_{BW} = 6.1)$. Results are shown in Figure 4.20. Gain compresses by 1 dB at $P_{in,BLK} = -4.4dBm$ for a 400 MHz offset blocker and at $P_{in,BLK} = +3dBm$ for 800 MHz offset blocker.

Noise degradation with an OOB blocker was measured too. To prevent reciprocal

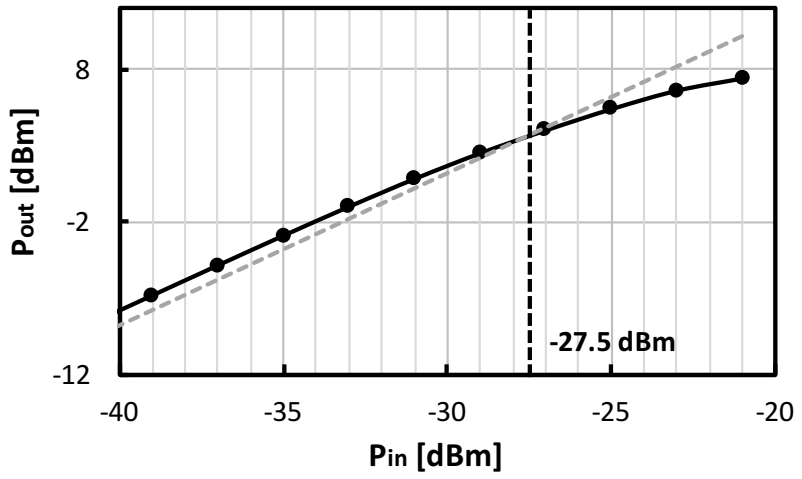

FIGURE 4.19: In-band compression

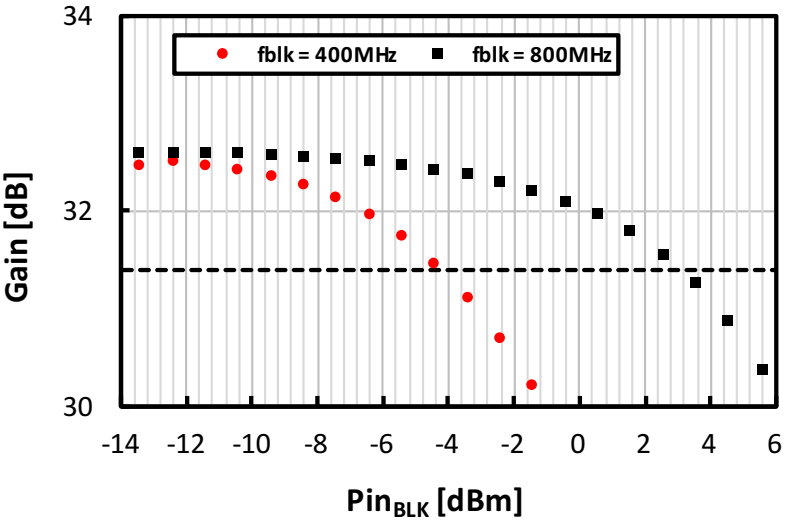

FIGURE 4.20: In-band compression with blockers at $f_{blk} = f_{LO} + 400MHz$ and $f_{blk} = f_{LO} + 800MHz$

mixing from corrupting noise measurement, external SAW filters were employed to attenuate phase noise of the 2xLO and blocker signal generators. In detail an *Anatech Electronics 4000B1033* SAW filter with 3950-4050MHz pass-band was connected after the $2\text{x}f_{LO} = 4GHz$ signal generator and a *Murata SAYEY897MBA0B0A* with 925-960 MHz pass-band was used to attenuate phase noise around $f_{blk} = 960MHz$. Noise Figure degradation vs. blocker power is reported in Figure 4.21. From the plot a 1 dB degradation in observed for $P_{blk} = -6dBm$, while a 0 dBm blocker degrades NF by 4.2 dBm. The measured value is still limited by reciprocal mixing of the phase noise introduced by the on-chip frequency divider. Measurement was also repeated increasing divider supply

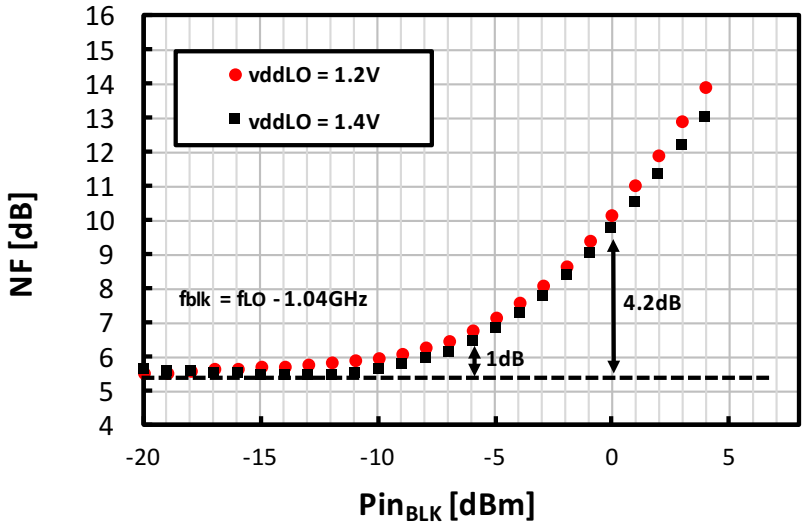

FIGURE 4.21: NF degradation vs. P_{blk} with blocker at $f_{blk} = 960MHz$ ($\Delta f = 1.04$ GHz)

voltage to 1.4V, observing slight improvement (1dB) in NF for higher P_{blk} values.

The achieved results are compared with other State-of-the-Art Mixer-First implementations in Table 4.2. In comparison with solutions [53] and [54] the proposed one achieves 3rd order filtering (as opposed to 1st of [53] and 2nd of [54]), with a much larger bandwidth ($\sim 15-20$x), $\sim 2.5-3$x lower power consumption and $\sim 3-5$x smaller area. In solution [53] the issue of limited switch linearity is addressed by adopting bottom plate mixing. Higher IIP3 and B1dB are achieved, at the cost of a 2.5x higher overall power consumption (more than 4x power consumption in LO-distribution) and 4.5 dB higher NF. The TIA bandwidth implemented in [53] is 20x smaller than the proposed solution. In [54] capacitive positive feedback is introduced in a more classical shunt feedback OTA to create two complex-conjugate poles and enhance TIA selectivity up to a relatively high frequency. Taking advantage of closed-loop operation, solution in [54] achieves much better B1dB. However IIP3 is comparable with the proposed solution at the same $\Delta f/f_{BW}$, despite the proposed implementation has 11 dB higher gain. Noise Figure in [54] is 2.5 dB better than than in this work for the same LO frequency, at the cost of a 3x higher power consumption. A Mixer-First solution achieving similar BW as the one proposed here is reported in [55]. A fair comparison with this solution is difficult since it this work an entire chip Transceiver for Basestations is presented and no information is provided about the Stand-Alone RX power consumption. The solution is anyway reported in Table 4.2 since to the knowledge of the author it represents the only Mixer-First implementation with comparable BW with the design described here.

	This work	ISSCC'17 [53]	JSSC'18 [54]	ISSCC'18 [55]
Technology	**28nm CMOS**	28nm	45nm SOI	65nm CMOS
Architecture	**Mixer-First RX**	N-path w bottom-plate mixing	MF w pos capacitive FB	Mixer-First RX
Area [mm^2]	**0.16**	0.49	0.8	68.7*
Supply [V]	**1.8/1.2**	1.2/1.0	1.2	1.8/1.3
Power Diss. [mW]	**21.6 (TIA) + 7.8mW/GHz**	38-96 (30 + 36mW/GHz)	50 + 30mW/GHz	N/A
Gain [dB]	**32.4**	16	21	N/A
TIA Order	**3**	1	2	1
RF BW [MHz]	**260**	13	20	200
LO Range [MHz]	**500-2000 (test balun limited)**	100-2000	200-8000	400-6000
NF [dB]	**5.5 (f_{LO} = 2GHz)**	10 ($f_{LO} = 2GHz$)	3 ($f_{LO} = 2GHz$)	12.5
IIP3 [dBm]	**+21 ($\Delta f/f_{BW}$ = 3)**	+30 ($\Delta f/f_{BW}$ = 3)	+23 ($\Delta f/f_{BW}$ = 3)	+12 ($\Delta f/f_{BW}$ = 1)
IIP2 [dBm]	**+70 ($\Delta f/f_{BW}$ = 3)**	+82 ($\Delta f/f_{BW}$ = 3)	+75 ($\Delta f/f_{BW}$ = 3)	+60
B1dB [dBm]	**+3 ($\Delta f/f_{BW}$ = 6.1)**	+10 ($\Delta f/f_{BW}$ = 6)	+10 ($\Delta f/f_{BW}$ = 6)	N/A

*Overall TRX Chip

TABLE 4.2: Comparison table with State-of-the-Art Mixer-First RXs

4.5 Conclusions

In this chapter a solution to implement a wide-bandwidth TIA for 5G applications was presented. The proposed circuit is based on an improved version of the Regulated-Cascode topology, which is able to realise a 3rd order Butterworth filter, guaranteeing good rejection of close-in blockers. The designed filter was integrated in a Mixer-First RX, capable of operating over different bands, which is highly desirable in a 5G platform. RX prototype was measured, demonstrating larger bandwidth in comparison with the State-of-The-Art, together with lower power consumption and similar linearity and noise performance. Good resilience to OOB blockers was demonstrated too, which is important in case filtering at the RF side of the RX is low.

Conclusions

In this work two different approaches to the design of highly linear base-band filters were discussed. The goal was to design a TIA capable of handling strong OOB interferers and compatible with the increased bandwidth of modern standards for mobile communications (4G, 5G).

A more traditional approach was considered first. In Chapter 2 in fact, a TIA based on a closed-loop OTA was presented, achieving 20-MHz-BW, consistently with the channel BW of LTE. To extend the benefits of closed-loop operation over a broader frequency range, OTA bandwidth was enlarged adopting an unconventional compensation technique, able to remove Miller-Capacitors, getting rid of the bandwidth limitations associated with them. Good IB and OOB IIP3 performance was achieved, together with a limited In-Band noise, thanks to the lower input capacitance value.

The advantages of the design strategy proposed in Chapter 2 in terms of linearity were demonstrated in Chapter 3 proposing an intuitive (but quantitative) method to analyse circuit behaviour in terms of IM3. This allowed to explain linearity behaviour of the circuit versus frequency, providing interesting insights into the mechanisms generating non-linearity and on OTA stages contributing IM3, leading to possible design strategies to optimize the circuit behaviour in each frequency range.

Another approach to the TIA design was proposed in the last chapter of this work. This was based on the Regulated-Cascode Architecture, which was improved to achieve better selectivity. With the proposed filter topology a 3^{rd} order *current* filter was achieved. A large 130-MHz BB-bandwidth was obtained with reasonable power consumption, at the cost of reduced IB linearity. However, thanks to the sharp filtering at the TIA input, good OOB linearity performance and good resilience to OOB blockers were achieved.

Appendix A

Non-linear coefficients calculation procedure

This Appendix describes how to extract the non-linear coefficients of each OTA stage. Equation (A.1) *is derived from* (3.3) *with the gain* $G(\omega)$ *of each stage rewritten as* $g_{m,i} \cdot |Z_{o,i}(\omega)|$

$$v_{IM,out,i} = \left(\frac{3}{4} g_{mNL3,i} A_{1,i}^2 A_{2,i} + \frac{3}{4} g_{dsNL3,i} (A_{1,i} \cdot g_{m,i} |Z_{o,i}(\omega_1)|)^2 (A_{2,i} \cdot g_{m,i} |Z_{o,i}(\omega_2)|)\right) \cdot \\ \cdot |Z_{o,i}(2\omega_1 - \omega_2)| \cdot \sin((2\omega_1 - \omega_2)t) \tag{A.1}$$

From (A.1)*, we see that when a stage is loaded by a low impedance, its* g_m *non-linearity is dominant since this reduces the output swing. On the contrary, when the load impedance is high, the large output swing makes the* g_{ds} *non-linearity dominant. With a 1* Ω *load at the stage output,* (A.1) *can be approximated by* (A.2)*:*

$$v_{IM,out,i} = \frac{3}{4} g_{mNL3,i} A_{1,i}^2 A_{2,i} \cdot (1\Omega) \cdot \sin((2\omega_1 - \omega_2)t) \tag{A.2}$$

Simulating the circuit intermodulation magnitude ($|v_{IM,out,i}|$*) with two input tones of amplitude* $A_{1,i}$ *and* $A_{2,i}$ *the* $g_{mNL3,i}$ *coefficient can be extracted by inversion of* (A.2)*, as shown in* (A.3)*:*

$$g_{mNL3,i} = \frac{4}{3} \frac{|v_{IM,out,i}|}{A_{1,i}^2 A_{2,i} \cdot (1\Omega)} \tag{A.3}$$

The same simulation is performed with no explicit load. At sufficiently low frequency, $Z_{o,i}(\omega)$ *is the parallel of the* r_{out} *of the output transistors, which is typically in the order of* $k\Omega$*. Putting the result of* (A.3) *in* (A.1) *we get* (A.4) *(cit. [16] ©2018 IEEE)*:

$$g_{dsNL3,i} = \frac{\frac{4|v_{IM,out,i}|}{3r_{o,i}} - g_{mNL3,i} A_{1,i}^2 A_{2,i}}{A_{1,i}^2 A_{2,i} (g_{m,i} r_{o,i})^3} \tag{A.4}$$

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