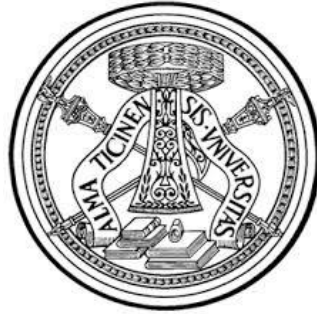


University of Pavia



Ph.D. Thesis in Microelectronics

XXXII Cycle

CMOS Continuous-Time Linear Equalizers for High-Speed Serial Links

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List of Acronyms

| | |
|--------------|----------------------------------|
| IoT | Internet of Things |
| CAGR | Compound Annual Growth Rate |
| EB | Exabyte |
| BER | Bit Error Rate |
| PCB | Printed Circuit Board |
| FEC | Forward Error Correction |
| DSP | Digital Signal Processing |
| NRZ | Non-Return-to-Zero |
| PAM-4 | Pulse-Amplitude-Modulation-4 |
| TX | Transmitter |
| RX | Receiver |
| ADC | Analog-to-Digital Converter |
| CTLE | Continuous-Time-Linear-Equalizer |
| FIR | Finite Impulse Response |
| FFE | Feedforward-Equalizer |
| DFE | Decision-Feedback-Equalizer |
| AFE | Analog Front-End |
| VGA | Variable-Gain-Amplifier |
| PLL | Phase-Locked Loop |
| CDR | Clock-and-Data Recovery |
| UI | Unit Interval |
| PSD | Power Spectral Density |
| ISI | Inter-Symbol Interference |
| BR | Bit Rate |
| RJ | Random Jitter |
| DJ | Deterministic Jitter |
| DDJ | Data Dependent Jitter |

BUJ Bounded Uncorrelated Jitter
FCBGA Flip-Chip Ball Grid Array
FEXT Far-End Crosstalk
NEXT Near-End Crosstalk
IL Insertion Loss
ICR Insertion Loss to Crosstalk Ratio
FOM Figure of Merit
LF Low Frequency
PVT Process-Voltage-Temperature
LMS Least-Mean-Squares
MSE Mean-Square-Errors
MMSE Minimum-Mean-Square-Errors
FVF Flipped-Voltage-Follower
CDF Common-Drain-Follower
TI Time-Interleaved

Abstract

The explosive growth of internet traffic, driven by multimedia, Internet of Things and cloud services, continuously pushes for higher bandwidth and aggressive scaling of I/Os for high-speed electrical links. Recent standards require transceivers working at 25~28Gb/s with NRZ (non-return-to-zero) modulation or 50~56Gb/s with PAM-4 (Pulse-amplitude-modulation-4) modulation. Channel impairments degrade the signal integrity significantly for transceivers working at such high data rate. To ensure link reliability, equalization is necessary for compensating channel impairments. Moreover, to achieve a target BER (bit-error-rate) with lower power consumption, accurate and energy-efficient equalization techniques have been exploited in recent transceivers design.

In receiver design, continuous-time-linear-equalizer (CTLE) shows its advantages for its low power consumption. This Ph.D. work has been focused on the study of analog equalization techniques and presents three different designs tailored to 25Gb/s NRZ, 56Gb/s PAM-4 and 112Gb/s PAM-4 respectively. First, a novel CTLE based on transversal architecture is presented. Thanks to the transversal architecture, it shows high accuracy to compensate inter-symbol interference (ISI) and flexibility to accommodate variable speed and channel profiles. The CTLE was realized in 28nm FD SOI technology and measurements are presented at data rate from 5Gb/s to 25Gb/s across 20dB-loss channels. Core power dissipation is 17mW from 1V supply and horizontal eye opening at $BER=10^{-12}$ is larger than 50%, comparing favorably against previously reported equalizers targeting similar data-rate and channel loss.

Recently, to satisfy the higher bandwidth demand, transceivers working at 50~56Gb/s per lane have been proposed. Since the impairments of channels used for 25-28Gb/s NRZ by increasing bandwidth significantly limit serial link data rate, a double bandwidth efficiency modulation PAM-4 is proposed to increase the data rate. In this dissertation, a fully analog PAM-4 receiver working up to 64Gb/s is presented. Receiver equalization relies on a flexible CTLE that can be optimally adapted at low, mid and high frequency independently, providing a very accurate inversion of channel transfer function. The CTLE meets the performance requirements of the CEI-56G-VSR standard without requiring DFE (decision-feedback-equalizer) implementation. The test chip is implemented in 28nm FD SOI technology, at the maximum speed, the receiver draws 180mA from 1V supply, corresponding to 2.8mW/Gb/s only.

Electrical interfaces used with 100Gb/s signaling are being investigated to satisfy the continual growth of bandwidth demand. In the newer Ethernet standard, IEEE 802.3ck, one-single lane 100Gb/s interfaces are specified. In this thesis, a 112Gb/s PAM-4 analog front-end designed in 7nm FinFet technology is presented. The target is to be merged with an analog-to-digital converter (ADC) based receiver so as to take advantage of high-performance digital signal processing (DSP) in 7nm FinFet technology. However, significant changes in transistor behavior, scaled supply voltage, and very different layout rules result in challenges in analog circuits design. Design considerations regarding linearity and bandwidth of analog circuits in 7nm FinFet technology are presented in this thesis. Simulation results prove the analog front-end can successfully recover 112Gb/s PAM-4 sequences transmitted through a 15dB Synectic channel.

Chapter 1 Introduction

1.1 Backgrounds

Internet services are extremely important in modern life. Nowadays, internet services like social media, HD video streaming, cloud services, big data, and Internet of Things (IoT) have pushed network traffic to grow exponentially. Most of the Internet services are being run in datacenters. The data from Cisco white paper shows that by the year 2019, 99% of the global network traffic is related to data centers [1]. Data centers could be treated as a “super-computer” in which there are high-density interconnections of servers, often stacked in racks that are placed in row as shown in Figure 1.1.

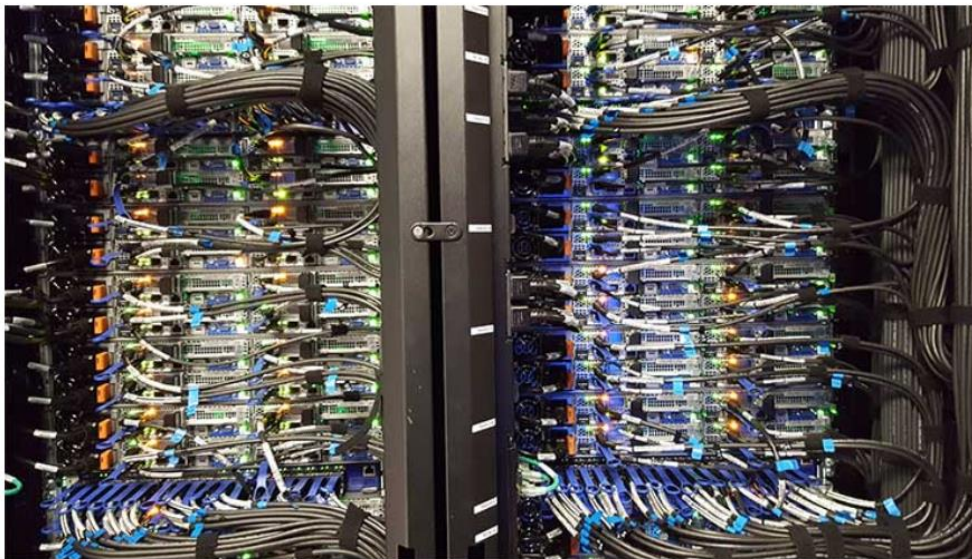


Figure 1.1 Interconnections of servers in data center

Furthermore, the growth of global network IPs is promoted by the demand of increasing Internet services. From the data of Cisco Visual Networking Index, global network IP traffic will grow at a Compound Annual Growth Rate (CAGR) of 26 percent from 2017 to 2022. As it forecasts the network IPs grow 3 times in every 5 years. The Annual global IP traffic will reach 4.8 ZB per year by 2022, or 396 exabytes (EB) per month as shown in Figure 1.2 [2].

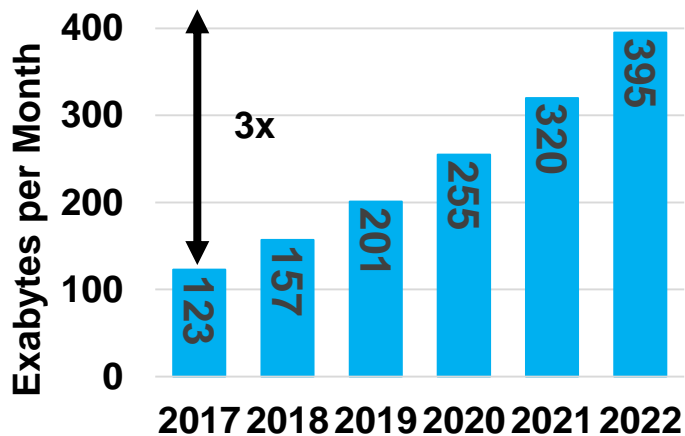


Figure 1.2 Global network IP traffic [2]

The continuous growth of network IP traffic drives the development of serial link communications standards. The standards formulate the performance requirements which usually consist of data rate, signaling modulation, channel loss, bit error rate (BER), forward error corrections (FEC), etc. of serial link communications for different applications. For instance, the recent standard OIF- CEI-56G [3] contains different applications from very short to long reach channel. Figure 1.3 shows the progress of standards, the data rate of serial link per lane has reached 56Gb/s, and the high parallel data rate has reached 400Gb/s. The planned future serial links will operate up to 100Gb/s per lane and 800Gb/s in parallel [14].

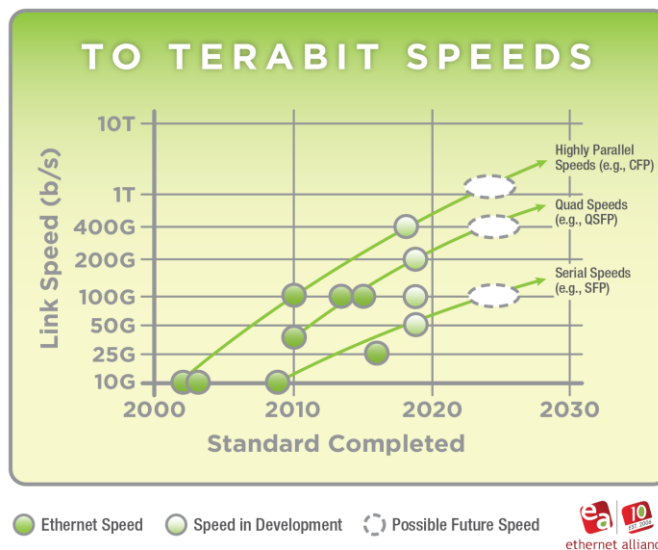


Figure 1.3 Serial link standards [58]

Several solutions have been proposed to satisfy the increasing demands of serial link communications standards. The data rates of serial link transceivers published in the last decade are summarized in Figure 1.4 [15]. The speed of transceivers has evolved from few Gb/s to 64Gb/s. The signaling scheme for transceivers operating up to nearly 30Gb/s has always been non-return-to-zero (NRZ) in which signals have two levels. The pulse-amplitude-modulation-4 (PAM-4), in which signal features 4-level to encode pairs of bits, has been introduced at >50Gb/s due to its doubled bandwidth efficiency.

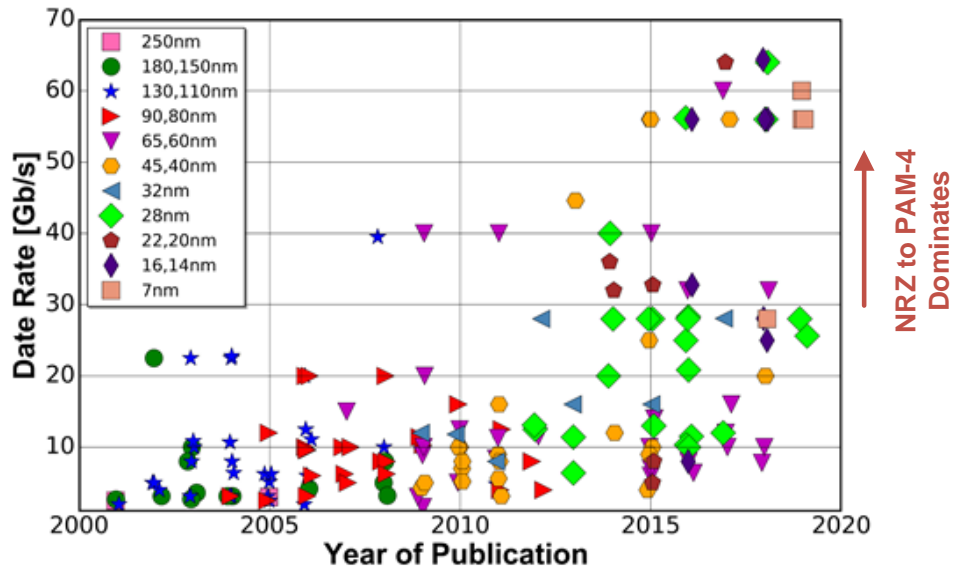
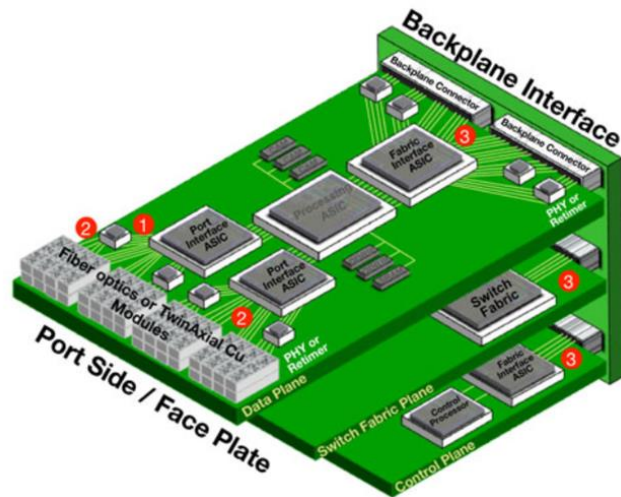


Figure 1.4 Speeds of serial links in literature [15]

1.2 High-speed serial link transceivers



Source: Synopsis

Figure 1.5 Backplanes inside a server

Inside a server, as shown in Figure 1.5, there are several ASICs to process, transmit and receive data through printed circuit boards (PCB) and backplanes. There are three different kinds of high-speed communication interfaces inside a server: (1) chip-to-chip port side interface which connects to the port side modules that have re-timers on both transmitter and receiver sides; (2) chip-to-module (PCB board) direct attach interface which directly connects to the port side modules. They do not include re-timers on their electrical input or output interfaces; (3) chip-to-backplane interface which drives aggregated high-speed signals across a capable backplane or mid-plane in a chassis [4].

The fundamental component for communications of the interfaces is the high-speed serial link transceiver, with the block diagram shown in Figure 1.6. Typically, the transmitter (TX) includes a serializer to convert parallel data into serial data, a pre-emphasis finite impulse response (FIR) filter to pre-shape the signals and an output driver. The receiver contains continuous-time-linear-equalizers (CTLE), decision-feedback-equalizers (DFE) to compensate the impairments from channels, a clock-and-data recovery (CDR) to extract a recovered timing phase for sampling and a deserializer to parallelize the serial data.

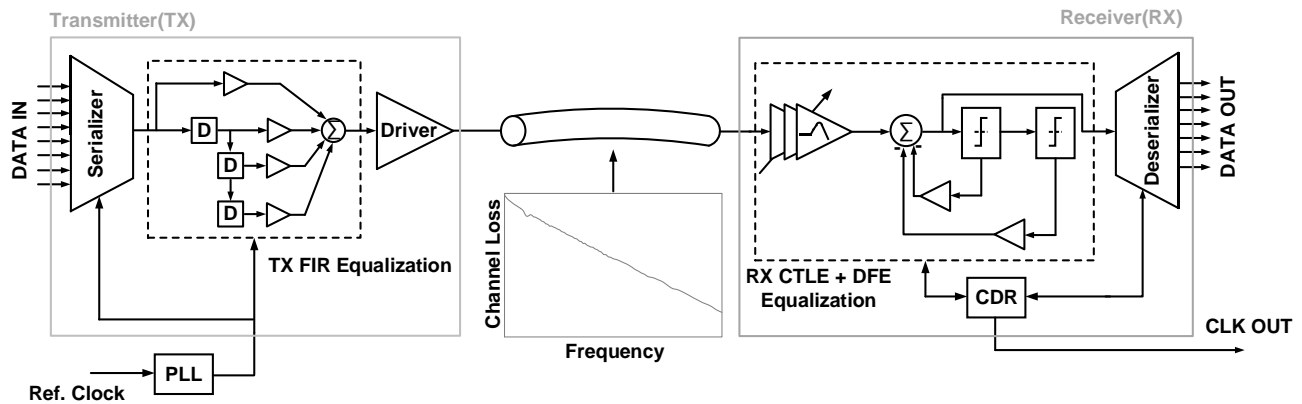


Figure 1.6 Serial link transceiver prototype

Receiver equalizations play a main role on recovering the data from channel impairments in the full transceiver since there's a peak-power limitation of transmitter equalizations [5]. The two types of equalizers: CTLE and DFE have very different power demands. Usually, a CTLE has a simple structure and consumes low power but its capability to compensate ISI is less than a DFE. However, a DFE is complex and power-hungry but has higher performance. In order to realize a power efficient transceiver for short-reach link that does not need powerful channel loss compensation, a receiver with only CTLE equalizations is cost-effective.

1.3 Overview

This thesis is divided into 7 chapters. Chapter 2 provides a background of wireline communications. The different signal modulations, the impairments from channels and the metrics of signal integrity are presented in this chapter. Chapter 3 introduces analog equalization techniques, and especially, CTLE equalizations are discussed in detail. This chapter includes the evolution of CTLEs and broadband techniques. In Chapter 4 an advanced flexible CTLE realized in 28nm FD-SOI is proposed. The equalizer features variable DC gain and two zeros that can be tuned independently. The transversal architecture makes it compatible with gradient descent algorithms, allowing optimal adaptation of the gain and zero frequency locations and improved equalization accuracy. Chapter 5 presents an analog front-end (AFE) for transceiver operating up to 64Gb/s in 28nm FDSOI. The AFE includes variable-gain-amplifiers (VGAs), and flexible CTLE with low, mid and high frequency channel loss compensation. The CTLE meets the performance requirements of CEI-56G-VSR without requiring DFE implementation. In Chapter 6, an analog front-end for an

ADC-based receiver operating up to 112Gb/s in 7nm FinFet is presented. The analog front-end comprises a variable-gain-amplifier (VGA), and a flexible CTLE with low, mid and high frequency channel-loss compensation, followed by and a buffer. Particular care was paid to reach adequate analog front-end linearity. Multiple broadband techniques are exploited in CTLE to extend the operating frequency above 28GHz.

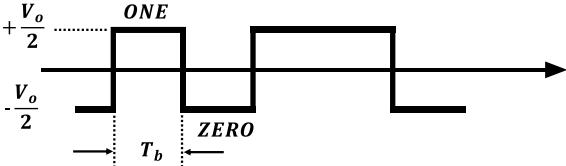
Finally, the Thesis is concluded with a summary and future work directions in Chapter 7.

Chapter 2 Background of wireline communications

2.1 Wireline communication signaling

2.1.1 NRZ Modulation

Pulse amplitude modulation is commonly employed in wireline communication signaling. NRZ (non-return-to-zero) signaling with two-level pulse amplitude modulation as shown in Figure 2.1 has been widely used in high-speed serial link transmissions. In wireline communications, a NRZ sequence is a binary sequence in which usually ones are represented by a positive voltage level and zeros are represented by a negative voltage level.



V_o : Amplitude

T_b : Bit Duration, also called Unit Interval (UI)

$1/T_b$: Bit Rate

Figure 2.1 NRZ signals

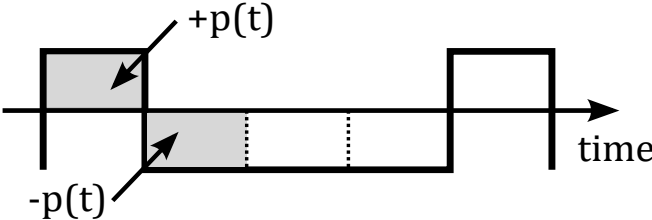


Figure 2.2 NRZ sequence $x(t)$

As shown in Figure 2.2, a NRZ sequence $x(t)$ can be expressed as: $x(t) = \sum_k b_k p(t - kT_b)$, where $b_k = \pm V_o/2$ and $p(t)$ is the rectangular pulse function. As such, the signal $x(t)$ is the sum of the product of time-shifted replicas of the square pulse ($p(t)$) and bits (b_k).

$$x(t) = p(t) * \sum_k b_k \cdot \delta(t - kT_b) \quad (* \text{ is convolution})$$

Defining:

$$y(t) = \sum_k b_k \cdot \delta(t - kT_b)$$

the power spectral density (PSD) of x(t) can be expressed as:

$$S_{xx}(f) = |P(f)|^2 S_{yy}(f).$$

where P(f) is the Fourier transform of p(t):

$$P(f) = T_b \left[\frac{\sin(\pi f T_b)}{\pi f T_b} \right].$$

If we assume the 'ONES' and 'ZEROES' have equal probability, the PSD of y(t) is:

$$S_{yy}(f) = \frac{b_k^2}{T_b}$$

and the PSD of x(t) results:

$$S_{xx}(f) = \frac{V_o^2}{4T_b} |P(f)|^2,$$

$$S_{xx}(f) = \frac{V_o^2}{4} T_b \left[\frac{\sin(\pi f T_b)}{\pi f T_b} \right]^2.$$

Figure 2.3 shows the PSD of x(t). It shows periodic behavior having power concentrated on a main lobe and replicas at higher frequency. It is interesting to note that power is zero for the frequencies $f = n/T_b$, where n is an integer number.

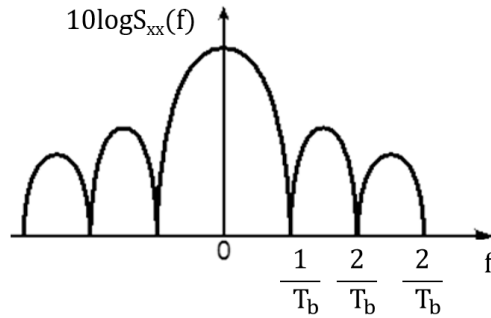


Figure 2.3 Power spectral density of a random NRZ sequence

2.1.2 PAM-4 Modulation

As the increasing data rate has reached 56Gb/s or above, frequency dependent impairments of backplane channel are problematic [7]. Therefore, the multi-level pulse amplitude modulation PAM-4, shown in Figure 2.4, which has twice the spectral efficiency in contrast to NRZ, has been proposed. A PAM-4 symbol contains 2-bits within one unit interval (UI), which correlates with the PAM-4 signal spectrum occupying half the bandwidth of a PAM-2 signal as shown in Figure 2.5. So, the Nyquist frequency of PAM-4 signaling is half of that of NRZ signaling. Many benefits

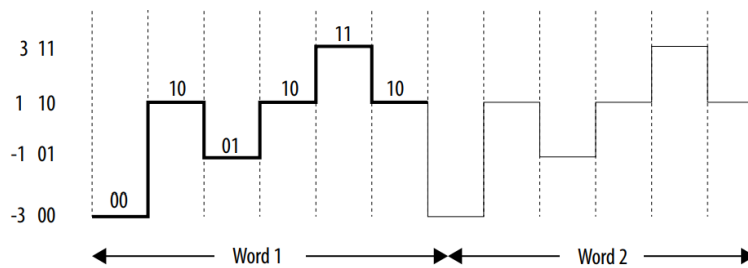


Figure 2.4 PAM-4 signaling

are associated with having half the Nyquist frequency. Compared to NRZ signaling with same Nyquist frequency, PAM-4 signaling doubles the density of data, achieving higher resolution in terms of signal levels. In a same sampling rate system, compared to NRZ signaling with same data rate, PAM-4 signaling has the same total noise power spread over a wider frequency so that the noise power in bandwidth goes down. However, considering that the maximum signal amplitude is constrained by the supply voltages, the levels in a PAM4 signal has 1/3 separation

compared to that of an NRZ signal. Therefore, PAM-4 suffers from an SNR loss of around $20 \log_{10} \frac{1}{3} = 9.5 \text{ dB}$.

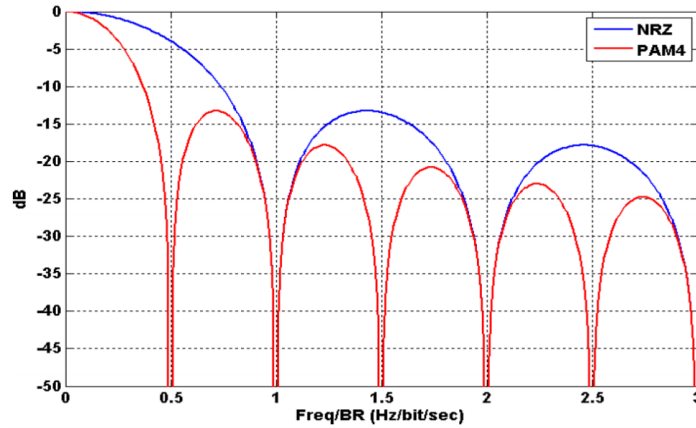


Figure 2.5 PSD of PAM signaling compared to PSD of NRZ [59]

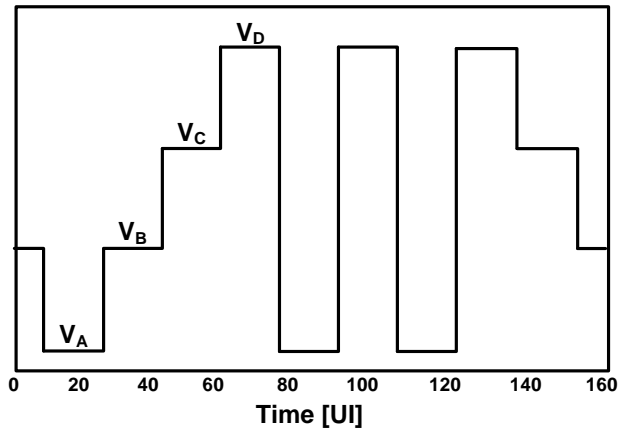


Figure 2.6 PAM-4 transmitter linearity test pattern

A PAM-4 transmitter linearity test pattern in which each symbol level is maintained for 16 consecutive identical symbols is shown in Figure 2.6. The linearity test pattern is used to measure the level separation mismatch ratio, R_{LM} , which indicates the vertical linearity of the signal. To assure that the level has been settled, regardless of pre/de-emphasis scheme, measure the settled symbol levels, V_A , V_B , V_C , and V_D , over 2 UIs starting 7 UIs after the transition. The minimum

signal level, S_{min} , is half of the swing between the closest adjacent symbols: $S_{min} = \frac{1}{2} \min (V_D - V_C, V_C - V_B, V_B - V_A)$, and the level separation mismatch ratio is:

$$R_{LM} = \frac{6 \cdot S_{min}}{V_D - V_A}$$

The spec from 100GBASE-KP4 requires $RLM \geq 0.92$ which is expected to serve as a performance benchmark [10].

2.2 Signal quality

2.2.1 Inter-symbol interference (ISI)

Inter-symbol interference (ISI) is a data-dependent form of interference in which one symbol interferes with previous and subsequent symbols. ISI is usually caused by multiple pulses transmitted through a bandwidth limited channel which is dispersive. The spreading of the pulse beyond its allotted time interval causes it to interfere with adjacent pulses as shown in Figure 2.7. The presence of ISI in the system degrades the signal-to-noise ratio and thus introduces errors in

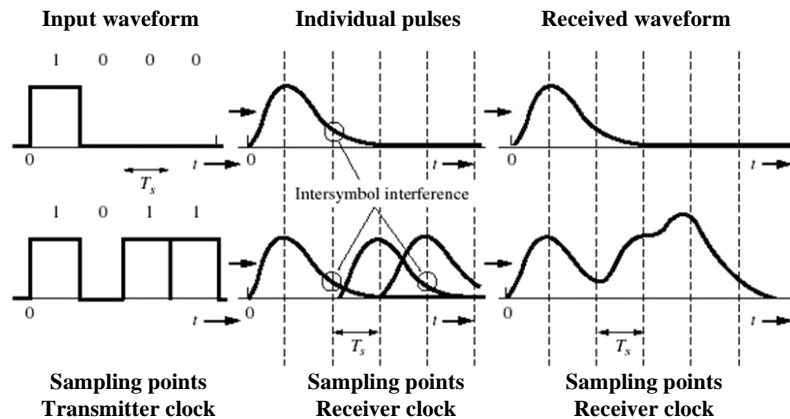


Figure 2.7 Example of ISI

the decision device at the receiver output. Therefore, in the design of the transmitting and receiving filters, the objective is to minimize the effects of ISI, and thereby deliver the digital data to its destination with the smallest error rate possible.

In communications, the Nyquist criterion defines the minimum bandwidth of a communication channel to transmit and receive signals without ISI. The Nyquist ideal channel is defined as:

$$P(f) = \begin{cases} -1/2W, & -W < f < W \\ 0, & |f| \geq W \end{cases}$$

$$p(t) = \text{sinc}(2Wt),$$

$$W = \frac{1}{2T_b} = \frac{BR}{2}.$$

This is a data sequence with a bit rate BR (bit/s) using a "sinc" pulse as shown in Figure 2.8. The W is called the Nyquist bandwidth that is equal to BR/2. However, "sinc" pulses are not causal and can only be approximated in practice. There are several approximated approaches such as "raised cosine" pulses or "square" pulses. The Nyquist frequency BR/2 keeps a good reference for the minimum bandwidth which gives negligible ISI for approximated implementations of "sinc".

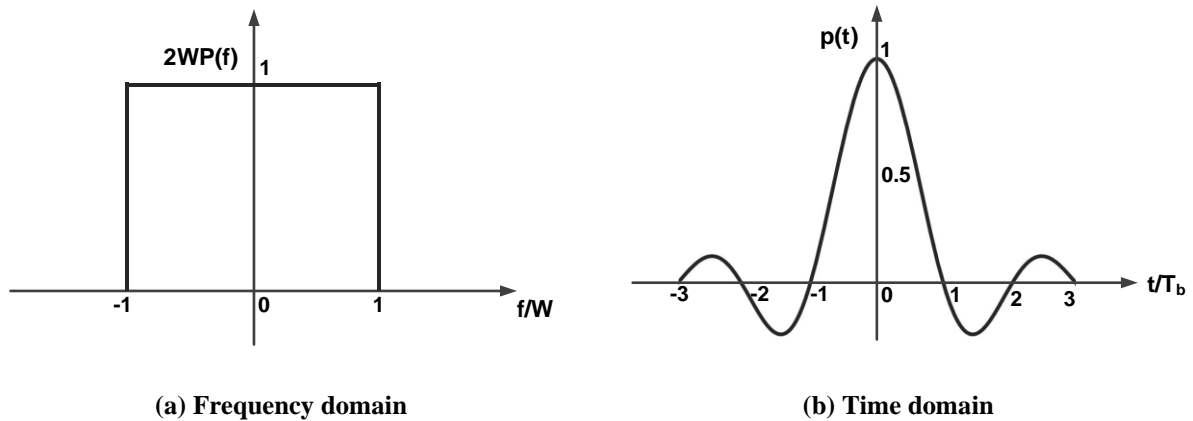


Figure 2.8 Nyquist ideal channel

2.2.2 Jitter

Jitter is defined as the variation of a signal edge from its ideal position in time as shown in Figure 2.9. In a serial communication system, jitter can affect timing margins and synchronization. Generally, there are two broad categories of jitter: random jitter and deterministic jitter. Random jitter (RJ) is caused by device noise. It is unbounded and assumed to have a Gaussian distribution. Usually it is specified as a root-mean-square (rms) value. Deterministic jitter (DJ) is bounded, with a well-defined minimum and maximum extent. It is usually expressed as a peak-to-peak (pk-pk)

value. Deterministic jitter can be further classified into subcategories: periodic jitter (PJ); data-dependent jitter (DDJ); and bounded uncorrelated jitter (BUJ). PJ can be defined as the time difference between the measured and nominal period. PJ is caused by clocks or other periodic sources that can modulate the transmitted edges.

DDJ is the jitter correlated with bit sequences in the data stream. DDJ is commonly caused by channel non-idealities (ISI) and duty-cycle distortion (difference in the rise and fall times). BUJ

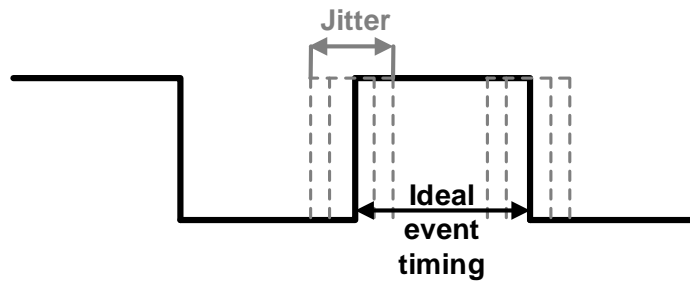


Figure 2.9 Example of jitter

is usually caused by crosstalk from adjacent links. BUJ is bounded due to finite coupling strength, and uncorrelated because it is correlated with the adjacent “aggressor” channels but not correlated with the “victim” channel. The total jitter composed of RJ and DJ can be organized in a jitter diagram tree that is shown in Figure 2.10.

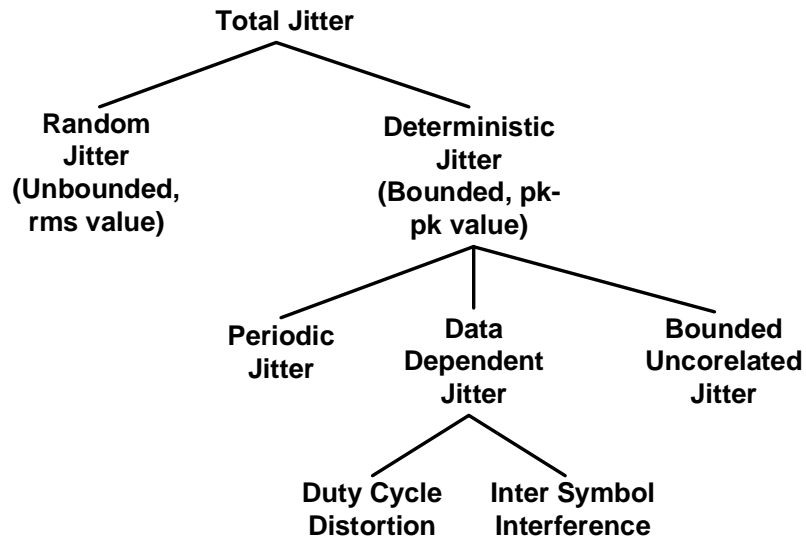


Figure 2.10 Total jitter diagram tree

2.2.3 Measurements of signal quality

Data eye diagrams are used to characterize a high-speed signal source and check the signal integrity. An eye diagram is constructed from a digital waveform by folding all the parts of the waveform corresponding to each individual bit into a short interval, as shown in Figure 2.11. The

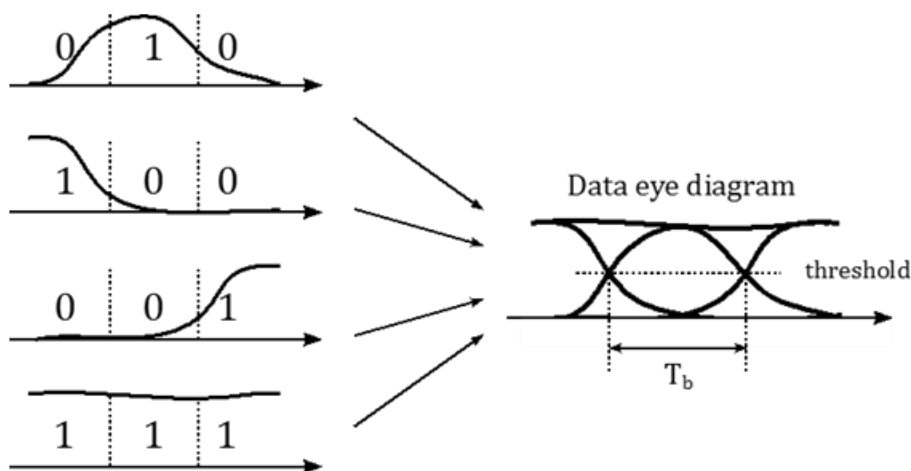


Figure 2.11 NRZ data eye diagram

eye diagram gives an intuitive way to evaluate bandwidth, attenuation, jitter, rise/fall time variations and noise margin in wireline communication systems.

The vertical and horizontal eye opening can be used to quantify the quality of the signal. We consider two conditions of the eye diagram, without and with additive Gaussian noise and random jitter. In the first case, which usually happens in circuit level design, the eye openings can be found in a straightforward way, as illustrated in Figure 2.12. The vertical eye opening is measured at the sampling instant (in the middle of the eye) and it can be normalized to full eye height (not including over- or undershoots). The horizontal eye opening is measured at the slice level (threshold) and can be normalized to a bit interval. The vertical eye closure is determined by Inter-symbol interference (ISI) [6], and the horizontal eye closure is determined by deterministic jitter (including data-dependent jitter and duty cycle distortion).

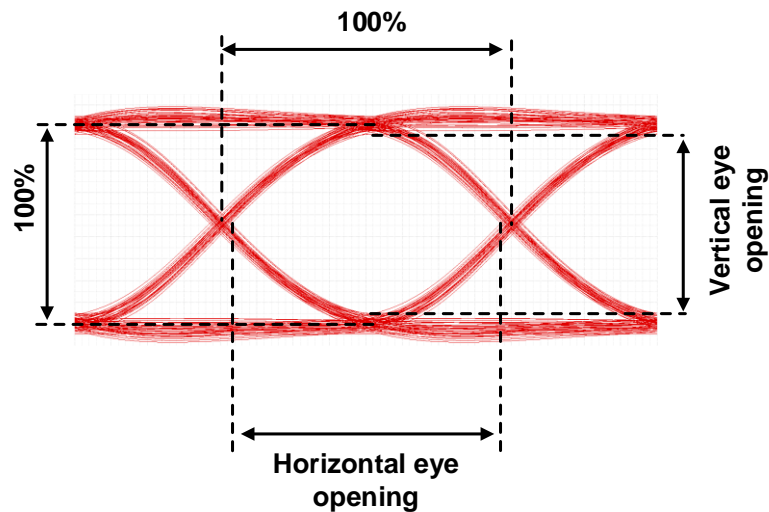


Figure 2.12 Eye openings of an eye diagram

In the second case, considering a signal with random noise, which is what happens in practice and observed in measurement, we should define the eye openings with statistical information. We can define a contour with same bit-error-rate (BER) in an eye diagram. BER can be determined by signal to noise ratio (SNR) [6]. SNR can be found from peak-to-peak amplitude V_o and noise RMS (root-mean-square) voltage σ : $SNR = V_o/2\sigma$, and it is given by: $BER =$

$Q\left(\frac{V_o}{2\sigma}\right)$ ($Q(x)$ is the error function that can be found in [6]). Thus, we can define a constant BER contour in an eye diagram. By sweeping the sampling instant and decision threshold, the same BER points can be found in an eye diagram. As shown in Figure 2.13, those same BER points construct a constant BER contour. If we make decisions inside a contour for a given BER, the resulting BER is less than that of the contour. In a system with noise and random jitter, we use eye margin instead of eye opening to evaluate the quality of signals. For a given BER, larger eye margins mean larger design margins for decision threshold and sampling instant.

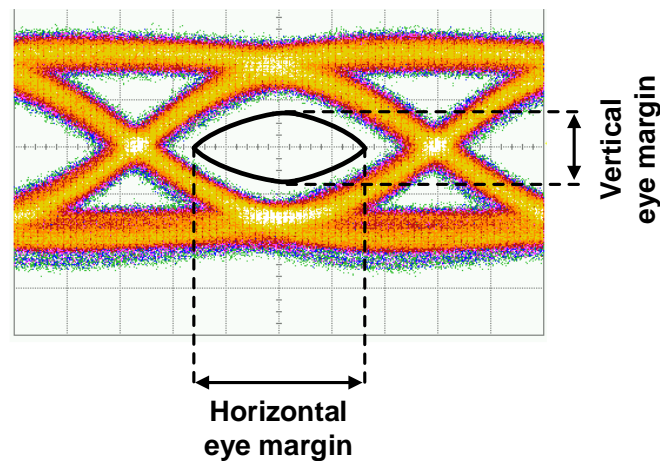


Figure 2.13 BER contour in eye diagram

Eye margins can be measured with an instrument called Bit Error Rate Tester (BERT) that has a pulse pattern generator and an error detector. The setup of bit error testing is shown in Figure 2.14 (a). The data stream is sent by a pulse pattern generator through the communications channel, and the error detector slices the data signal at the decision threshold V_{TH} and samples it at the instant t_R . The recovered bits are compared with the transmitted bit sequence to determine the BER, which is displayed on the error detector. By scanning the sampling instant t_R and setting the decision threshold V_{TH} at the center of the vertical eye, a horizontal scan can be performed. As the sampling instant moves from the center to the right or the left, the BER is degraded due to less SNR. The resulting curve named “bathtub” is shown in Figure 2.14 (b) and

(c). The horizontal eye margin is defined as the interval between the two points on the left and right side of the eye where the bathtub curve assumes a specified BER value. Similar to the horizontal scan, a vertical scan is performed by scanning the decision threshold V_{TH} and setting the sampling instant t_R at the center of the horizontal eye. As the threshold voltage moves from the center to the up or down, the BER is also degraded. The vertical eye margin for a specified BER with vertical scan bathtub is shown in Figure 2.14 (c).

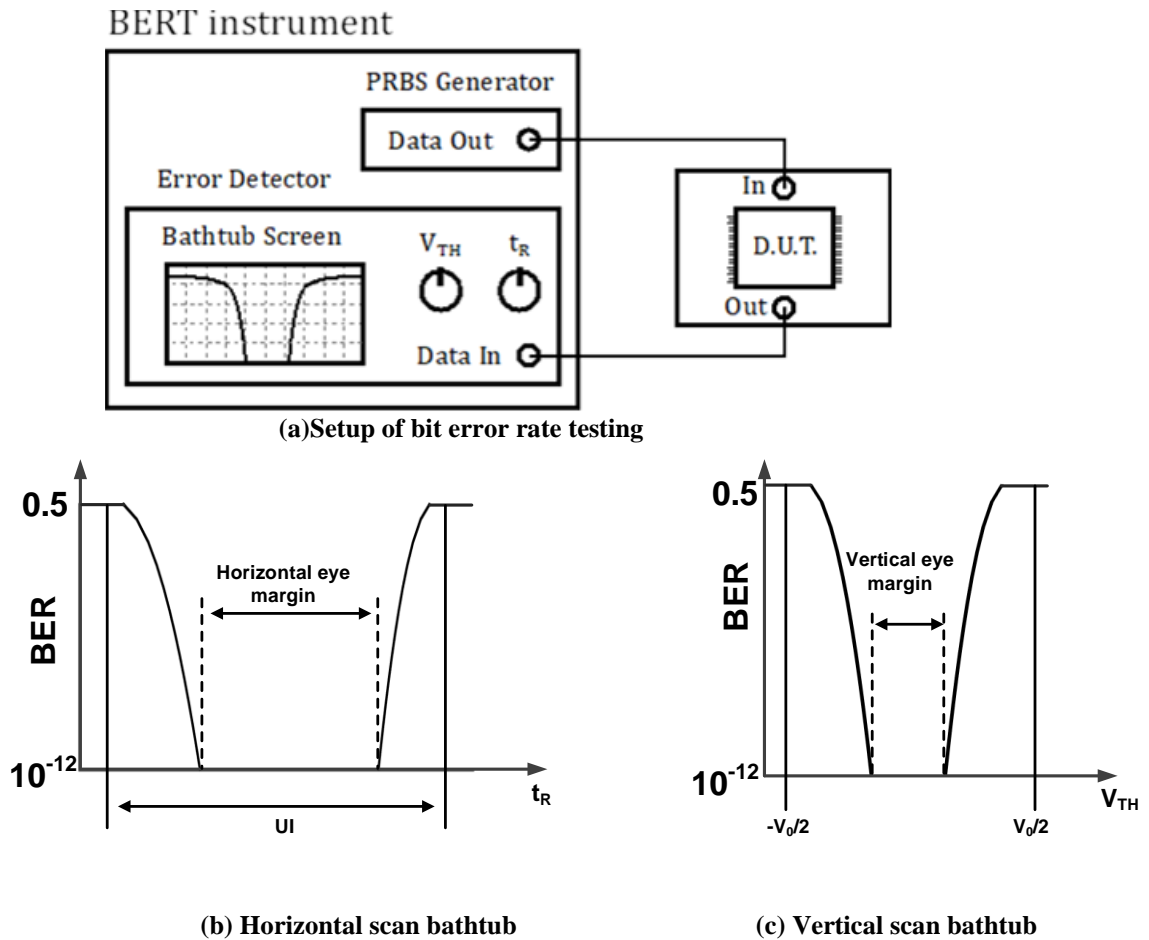


Figure 2.14 Bit error rate testing

2.3 Channel characteristics

Different applications need different types of channels. The characteristics of the channel strongly depend on its type. The backplane channel, as shown in Figure 2.15, is used in board-to-board connections and it is the target framework of this thesis. The backplane channel is a printed circuit board containing connections (slots) for expansion boards and allows for communication between all connected boards.

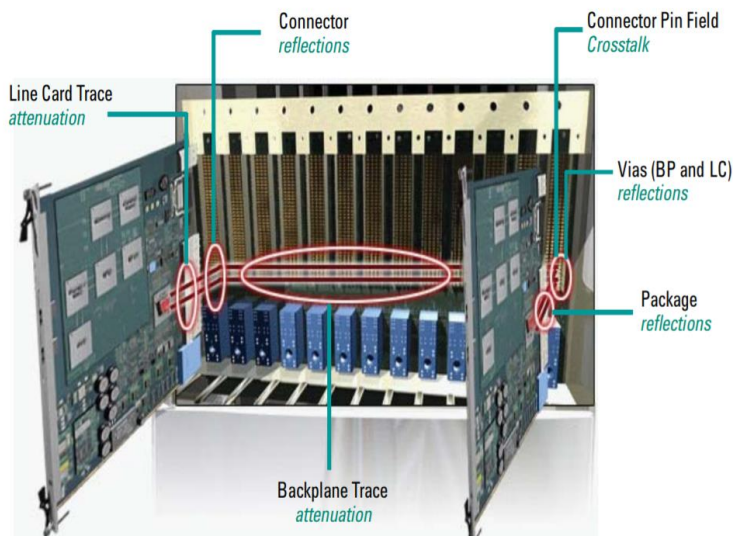


Figure 2.15 Backplane channel [60]

As shown in Figure 2.15, a backplane trace can be treated as a PCB transmission line used for moving signals from the transmitters to their receivers boards. A PCB transmission line is composed of two conductors: a signal trace and a return path which is usually a ground plane. The volume between the two conductors is made up of the PCB dielectric material. There are usually two basic types of signal transmission line interconnects used in PCBs: microstrips and striplines.

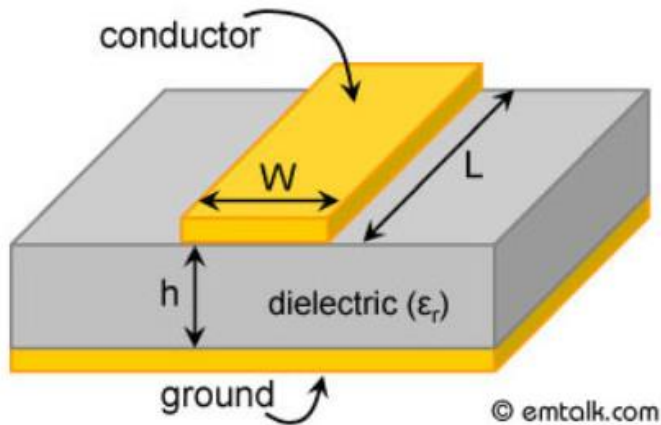


Figure 2.16 Microstrip

Figure 2.16 shows a model of microstrip. It includes a single conducting trace for the signal and a conducting ground plane, which provides the return path for the signal. They are separated by a dielectric layer known as substrate. Because the trace is not shielded, it is susceptible to cross-talk with adjacent signal lines.

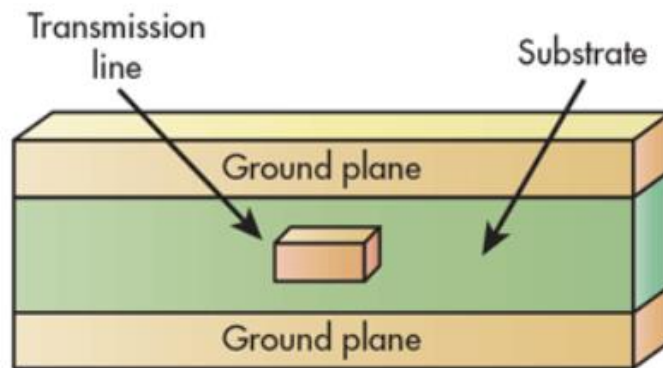


Figure 2.17 Stripline

Figure 2.17 shows a stripline. In contrast to a microstrip, the trace for the signal is located on the inner side of a PCB. The trace is isolated on each side by the PCB dielectric layer and then a conducting ground plane is located on top and bottom for the signal return path. Thanks to this

shielded structure, the stripline is much more robust to crosstalk and commonly employed in backplanes.

There are several impairments in the backplane channel that degrade signal integrity at data rates above a few gigabits per second. The frequency dependent impairments, reflections, and cross-talk in backplane channels will be discussed in the following sections.

2.3.1 Frequency-dependent impairments

In order to illustrate the frequency-dependent dispersion and attenuation of backplane channels, distributed element models are used to represent the PCB transmission line. As shown in Figure 2.18, the distributed element model is used to represent the channel through an infinite cascade of RLGC sections, where R, L, G, and C are values for unit/length (Ω / m , H / m , S / m and F / m respectively).

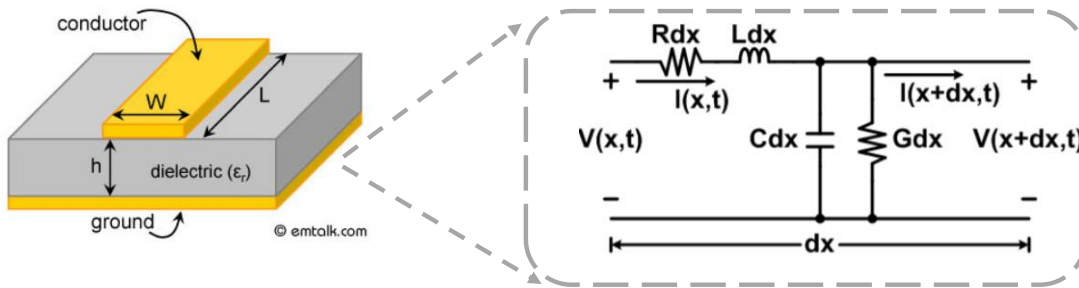


Figure 2.18 Distributed element model of the transmission line

The transmission line equations:

$$\frac{\partial V(x,t)}{\partial x} = -RI(x,t) - L \frac{\partial I(x,t)}{\partial t},$$

$$\frac{\partial I(x,t)}{\partial x} = -GV(x,t) - C \frac{\partial V(x,t)}{\partial t}.$$

The time-harmonic form:

$$\frac{d^2V(x)}{dx^2} = \gamma^2V(x),$$

$$\frac{d^2I(x)}{dx^2} = \gamma^2I(x).$$

Solutions of the time-harmonic transmission line equations:

$$V(x) = V_{f0}e^{-\gamma x} + V_{r0}e^{-\gamma x}$$

$$I(x) = I_{f0}e^{-\gamma x} + I_{r0}e^{-\gamma x}$$

where V_{f0}, V_{r0} are the voltages of forward and reflected wave respectively, I_{f0}, I_{r0} are the currents of forward and reflected wave respectively and γ is the propagation constant: $\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)}$.

Other meaningful parameters are the transmission line characteristic impedance: $Z_o = \frac{V(x)}{I(x)} = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$ and the signal phase velocity: $v = \omega/\beta$.

A first impairment introduced by the lossy transmission line is due to the frequency dependence of the signal phase velocity. The latter can be indeed approximated as $v \approx \left(\sqrt{LC} \left[1 + \frac{1}{8} \left(\frac{R}{\omega L} \right)^2 + \frac{1}{8} \left(\frac{G}{\omega C} \right)^2 \right] \right)^{-1}$. The frequency dependence causes dispersion and distortion of the signal shape as it propagates along the line.

For low loss condition, we can assume $R/\omega L, G/\omega C \ll 1$. The propagation constant can be simplified as $\gamma = \alpha_R + \alpha_D + j\beta$, where $\alpha_R \approx \frac{R}{2Z_o}$ is resistive loss and $\alpha_D \approx \frac{GZ_o}{2}$ is the dielectric loss.

The resistive and dielectric losses cause attenuation. Furthermore, in the case R and G are frequency dependent, the attenuation is also frequency-dependent. A more detailed analysis is presented in the following paragraphs.

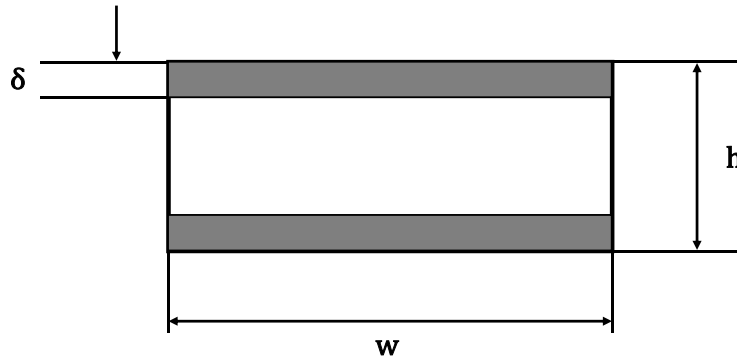


Figure 2.19 Skin effect in rectangular conductor

The conductive layers in a PCB transmission line suffer from skin effect i.e. the AC current density J in a conductor decreases exponentially from its value at the surface J_s according to the depth d from the surface, as follows [8]:

$$J(d) \approx J_s e^{-d/\delta}$$

where δ is called the skin depth. A rectangular conductor is shown in Figure 2.19. The skin depth, δ , is the thickness where the current density falls by e^{-1} relative to the surface of the conductor:

$$\delta = \sqrt{\rho / \pi \mu f}$$

where ρ and μ are the resistivity and magnetic permeability of the conductor. An important parameter is the critical frequency, f_s , defined as the frequency at which the skin depth equals to half the conductor height:

$$f_s = \frac{\rho}{\pi \mu (h/2)^2} .$$

Till looking at Figure 2.19, at low frequency $f < f_s$, the conductor resistance R can be approximated as $R = R_{DC} = \frac{\rho}{wh}$. At high frequency $f > f_s$, R can be approximated as $R = \frac{\rho}{2w\delta} = R_{DC} \sqrt{\frac{f}{f_s}}$. In this region, the resistive loss in the transmission line propagation constant can be expressed as

$$\alpha_R = \frac{R_{DC}}{2Z_0} \sqrt{\frac{f}{f_s}} .$$

Dielectric losses α_D are due to an alternating electric field that causes dielectric atoms to rotate and absorb signal energy in the form of heat. This loss is linearly proportional to the frequency of the signal traveling along the line and it is quantified by the loss tangent $\tan(\delta_D)$ that is defined as: $\tan(\delta_D) = \frac{G}{\omega C}$. The dielectric loss in the transmission line propagation constant can be expressed as

$$\alpha_D = \pi f \tan(\delta_D) \sqrt{LC} .$$

The lower is the tangent loss, the lower are the dielectric losses. Table 1.1 shows some typical dielectric materials for PCB and the respective $\tan(\delta)$.

Table 2.1 Dielectric material [8]

| Material | $\tan(\delta)$ |
|------------|----------------|
| FR4 | 0.035 |
| Poliimmide | 0.025 |
| GETEK | 0.010 |
| Teflon | 0.001 |

With the purpose of designing electronic equalizers for the PCB line imperfection it is useful to introduce a closed-form expression for the total loss profile [61], combining resistive and dielectric losses:

$$Loss(f) = \exp[-k_s L(1 + j)\sqrt{f} - k_d Lf]$$

where L is the line length, k_s and k_d are coefficients related to the skin and dielectric loss respectively. From the above equation, the impact of resistive loss, due to skin effect, rises with the square root of the signal frequency while the dielectric loss rises linearly. Therefore, at low frequency, the resistive loss is dominant, while as frequency increases, the dielectric loss becomes

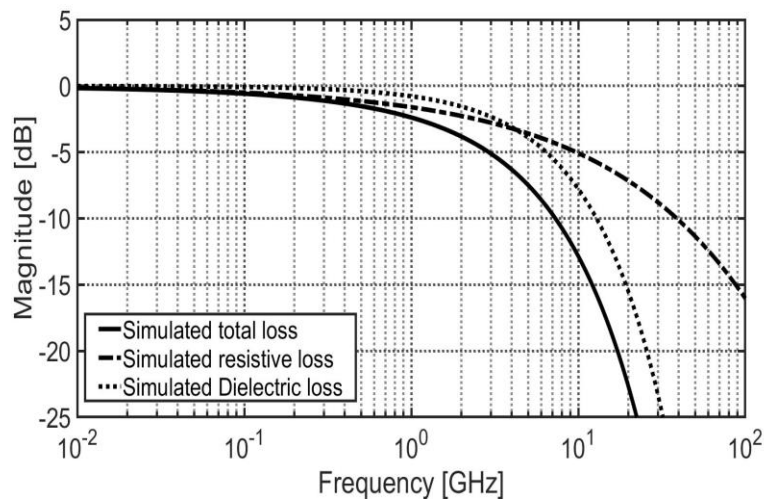


Figure 2.20 Crossover between skin and dielectric loss

relevant and the skin effect negligible. To gain insight, a typical channel transfer function is depicted in Figure 2.20, where the loss is separated in the two contributions.

2.3.2 Reflections

Impedance discontinuities on a backplane channel cause reflections. Such reflections result in notches in the frequency domain which degrade the signal integrity. Figure 2.21 shows a simplified model of a backplane channel. Impedance discontinuities occur where a trace changes direction, changes shape or interfaces to another component. Backplane vias, connectors, and packages of the transceivers are the locations at which impedance discontinuities usually occur.

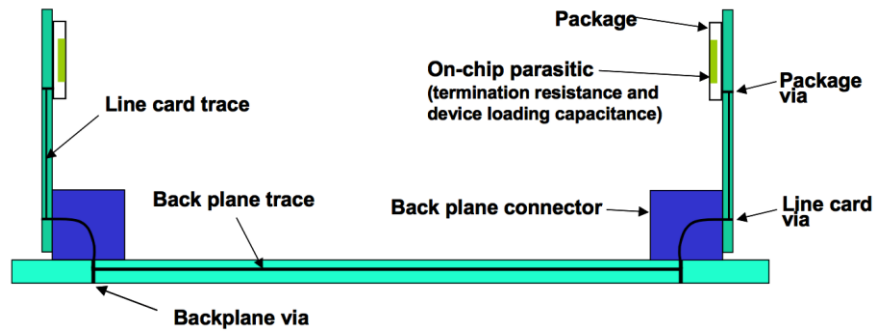


Figure 2.21 Simplified model of a backplane channel

Backplane vias are used to connect different PCB layers. They are significant contributors to signal integrity issues due to reflections. Backplane vias are made by drilling a hole through the board which is plated by copper. Backplane vias behave like stubs (an extra piece of the line) which can be modeled as an open-ended stub connected to the transmission line as shown in Figure 2.22.

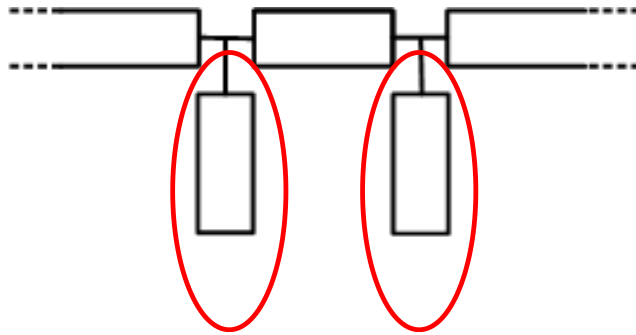


Figure 2.22 Via stub model

Vias introduce notches in the frequency response, which block signal propagation along the transmission line at certain frequencies as shown in Figure 2.23. The frequency location of the notches is related to the physical location and length of the open stubs and the dielectric constant of the material used.

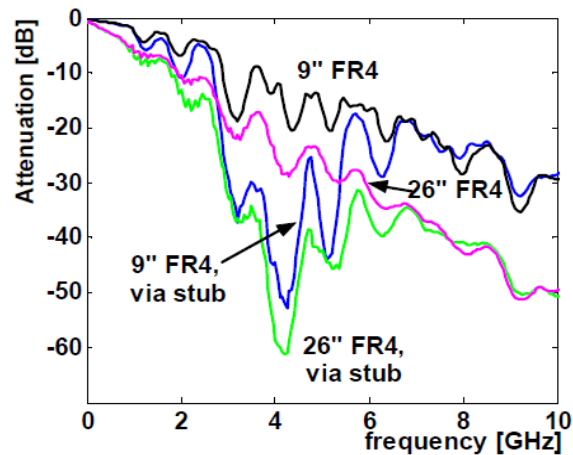


Figure 2.23 Measured notches caused by via stub [62]

Backplane connectors, shown in Figure 2.24, are used to transfer signals from two different PCBs. Typically, differential pair density is between 16-32 pairs/cm. The impedance mismatch of backplane connectors causes reflections. Moreover, the pins of connectors cause cross-talk due to poor isolation.

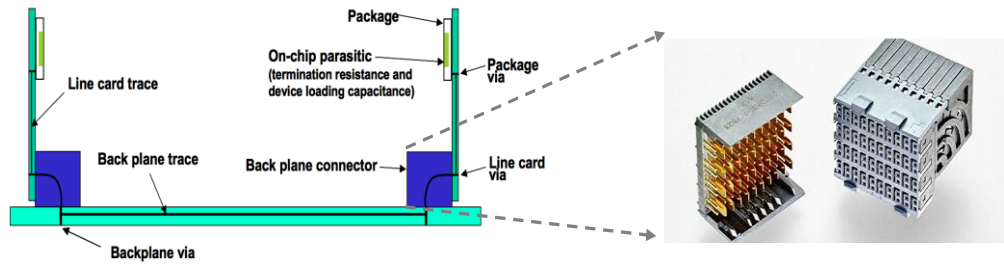


Figure 2.24 Backplane connector

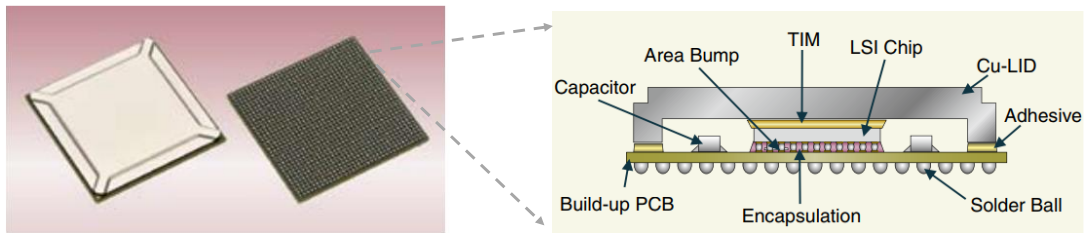


Figure 2.25 Flip-chip ball grid array package

The dies of the transceivers are enclosed in packages that provide protection and connection to the PCB board. There are several kinds of packaging for different applications. Flip-chip ball grid array (FCBGA), which has better heat dissipation efficiency and pin density is the one used in the projects described in this thesis and it is shown in Figure 2.25. The solder ball and bump used for interconnections can result in reflections due to impedance mismatch. The frequency response of a FCBGA package is shown in Figure 2.26, showing the effect of reflections and attenuation.

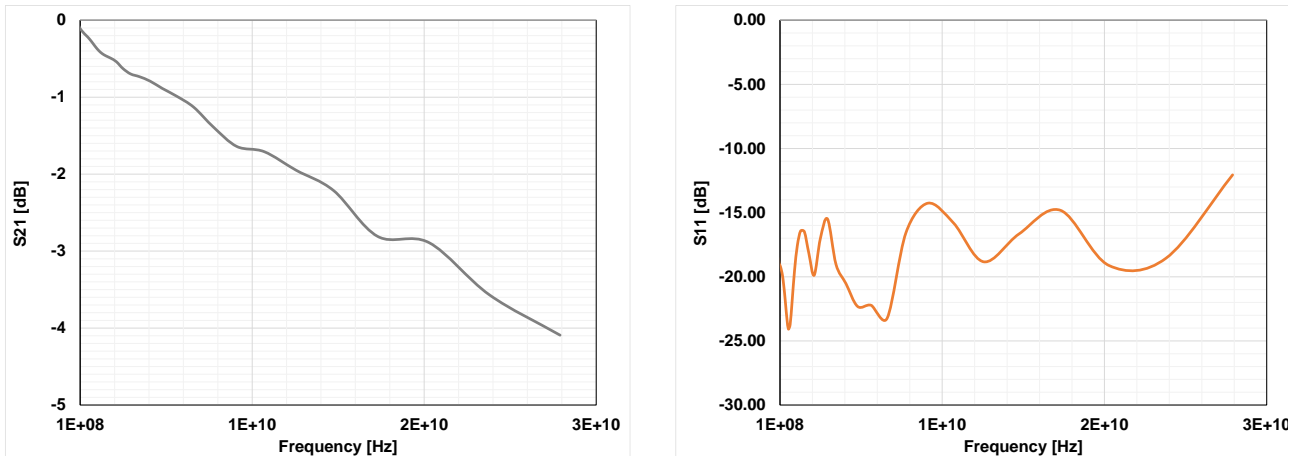


Figure 2.26 Measured frequency response of a FCBGA package

2.3.3 Crosstalk

Crosstalk is a measure of the unwanted signals that couple between various components of the channel and can be measured in both the time and frequency domains. Crosstalk occurs at multilane serial links due to poor isolation of connectors and PCB traces [11]. Figure 2.27 shows 2 types of crosstalk, far-end-cross-talk (FEXT) and near-end-cross-talk (NEXT). FEXT is referred to as a forwarding wave travels to the different end of the cable, and NEXT is referred to as a reverse wave traveling to the same end of the cable where the desired signal starts. It is worth noticing that NEXT is more critical because the interfering signal is not attenuated by the channel.

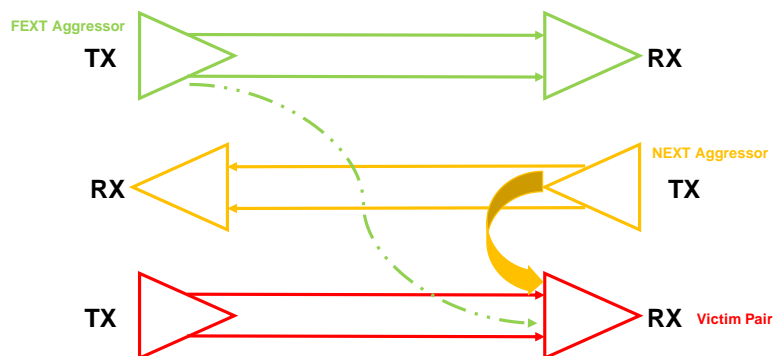
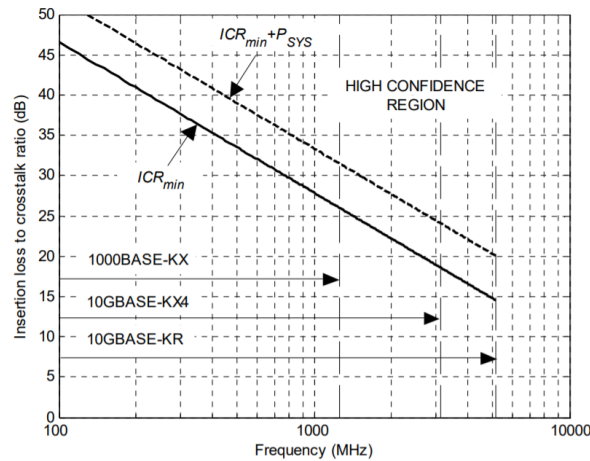


Figure 2.27 Crosstalk

High-speed serial link transceivers use differential signaling to reject common mode aggressors. However, crosstalk is canceled partially at high data rates because real differential pairs have asymmetries that translate common-mode aggressors to differential mode.

In order to accurately describe the limitations of crosstalk in passive interconnects, a new parameter called ‘insertion loss (frequency response of passive channel) to crosstalk ratio’ (ICR) has been introduced. It is computed as the ratio (in dB) of the insertion loss to the total crosstalk. The power sum of individual NEXT aggressors (PSNEXT) can be defined: $PSNEXT(f) = -10\log(\sum_n 10^{-NEXT_n(f)/10})$ where $NEXT_n(f)$ is the crosstalk loss, in dB, of the near-end



P_{sys} : system configurations penalty which is a design margin for transmitter to receiver configuration ratio extremes

Figure 2.28 ICR requirement

aggressor n. The power sum of individual FEXT aggressors (PSFEXT) can be defined: $PSFEXT(f) = -10\log(\sum_n 10^{-FEXT_n(f)/10})$ where $FEXT_n(f)$ is the crosstalk loss, in dB, of the far-end aggressor n. The power sum of the individual NEXT and FEXT aggressors (PSXT) can be defined: $PSXT = -10\log(10^{-PSNEXT(f)/10} + 10^{-PSFEXT(f)/10})$. Figure 2.28 shows the ICR requirement for different data rates from IEEE 802.3ap [12].

In newer standards, such as IEEE 802.3bj, the ICR was replaced with a new metric called ‘integrated crosstalk noise’ (ICN) which takes into account the spectrum of the excitation signal. ICN computes the total RMS voltage of FEXT and NEXT crosstalk noise. It is defined as: $\sigma_{total} = \sqrt{\sigma_{fx}^2 + \sigma_{nx}^2}$. The IEEE 802.3bj proposes maximum ICN versus insertion loss (IL) [13]:

$$\sigma_{total} \leq \begin{cases} 8 & 4dB \leq IL \leq 10.4dB \\ 12.1 - 0.393 * IL(dB) & 10.4dB < IL \leq 22.64dB \end{cases}$$

Chapter 3 Analog equalization techniques

Abstract

A continuous-time-linear equalizer is a peaking filter with high-frequency gain boosting transfer function that effectively compensates the frequency attenuation and dispersion of a channel. A continuous-time equalizer requires less power consumption and smaller chip area compared to a decision feedback equalizer (DFE), and thus it is an attractive solution for low-power high-speed serial receivers. In this chapter, the evolution of CTLEs is introduced. In order to provide precise equalizations, the CTLE evolves from one stage to multiple stages, and the low frequency equalizer is introduced to remove the residual ISI due to skin effect. As an alternative to conventional CTLEs, the split-path equalizer, which divides the signals into multiple paths is presented. Thanks to the split-path structure, the CTLE can tune DC gain and zeros' frequency independently. So that it gives more flexibility to shape the transfer function. Broadband techniques are helpful to extend the operating frequency of CTLEs. Inductive peaking and negative capacitance techniques that are widely implemented in tens of Gb/s transceivers are introduced.

3.1 Introduction

In order to compensate the channel impairments presented in chapter 2, equalization is a key part, necessary in wireline communication transceivers. A block diagram of a wireline communication transceiver, based on mixed signals equalization, is shown in Figure 3.1. Generally, there are three main categories of equalizers, feed-forward-equalizer (FFE), continuous-time-linear-equalizer (CTLE) and decision-feedback-equalizer (DFE). The FFE is usually realized as a finite-impulse-response (FIR) filter. It is implemented in the transmitter and it is exploited to introduce pre-emphasis on the signal sent to the channel. If embedded in the transmitter, the signal is still digital in nature and the FIR filter is realized in a mixed signals way with clocked flip-flops as delay elements. Pure analog FIR filters, without any clock, can also be implemented in the receiver but designing continuous-time delay elements is challenging, requiring large area and power consumption [16]. DFE is a non-linear equalizer in the receiver, with a feedback FIR filter after the decision device (slicer) that restores the digital information from the received signal. DFE is very powerful to cancel the signal energy located far away from the peak of the received symbols (post-cursor) without introducing noise amplification. But DFE needs relatively large power

consumption and hardware complexity and therefore several receivers in short reach links are

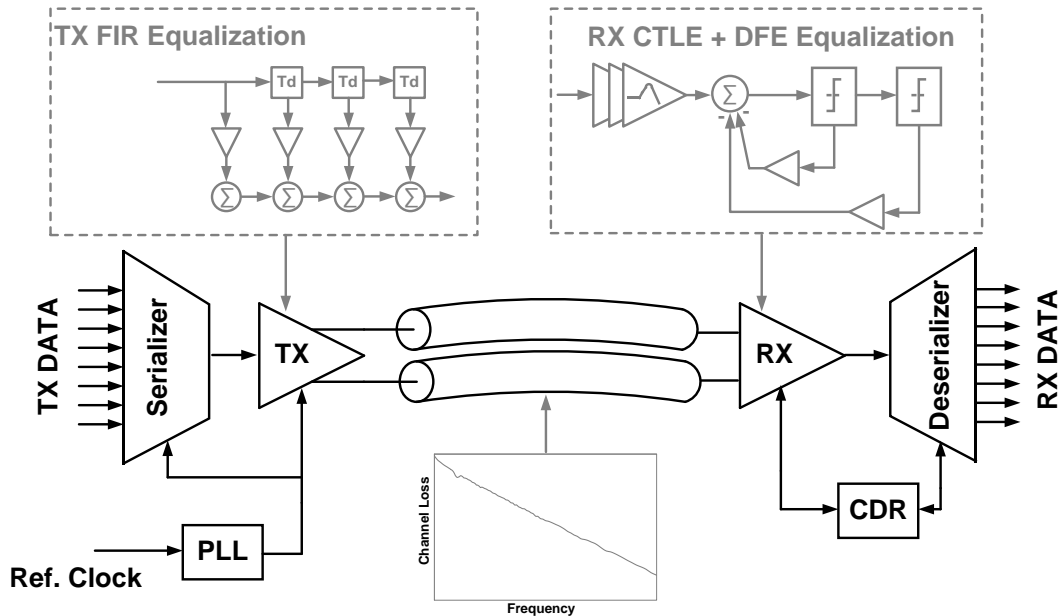


Figure 3.1 Transceiver based on mixed signals equalization

implemented with only the CTLEs for power and area savings [17]. Traditionally, the CTLE is realized with a differential pair degenerated by a parallel resistance-capacitance impedance that introduces a zero-pole pair to boost the high frequency gain and compensate the high frequency loss of the channel. However, state-of-the-art CTLE evolved from this simple implementation toward more complicated structures, e.g. with a split-path approach [18]. The CTLE is always present and plays a major role in shaping the transfer function of the receiver. A more in-depth analysis of CTLE characteristics, both in frequency domain and time domain, is presented in this chapter. Moreover, to satisfy the increasing data rate requirements, necessitating circuits operating at higher and higher frequency, broadband circuit techniques implemented in state-of-the-art CTLEs are also introduced in this chapter. Typically, a receiver with only CTLE is able to compensate channel loss at Nyquist frequency up to 20dB [25] [28].

3.2 CTLE operation and evolution

State-of-the-art wireline communication transceivers must embrace and specify faster data rates to satisfy the increasing bandwidth demand of the communication infrastructure. To achieve a good Figure of Merit (FOM), transceivers employ CTLE as a low-cost, low power option. This drives a continuous evolution of the CTLE to support higher speed and improve equalization performances.

The traditional CTLE is realized with a simple differential pair with resistive and capacitive, R_s - C_s , degeneration, shown in Figure 3.2 (a), that introduces a zero-pole pair in the transfer function, plotted in Figure 3.2 (b). The transfer function can be expressed as: $\frac{V_{out}}{V_{in}}(s) = \frac{g_m R_L}{1 + \frac{g_m R_s}{2}} \frac{1 + s/\omega_z}{1 + s/\omega_{p1}} \frac{1}{1 + s/\omega_{p2}}$, where $\omega_z = \frac{1}{R_s C_s}$, $\omega_{p1} = \frac{1 + \frac{g_m R_s}{2}}{R_s C_s}$, $\omega_{p2} = \frac{1}{R_L C_L}$. By tuning R_s and C_s , the zero-pole pair can be moved in frequency. Moreover, DC gain or equivalently the high frequency boost, is also changed by R_s . If the desired signal amplitude is fixed at the output of the receiver, a variable-gain-amplifier (VGA) is necessary to compensate the DC gain variation of the CTLE.

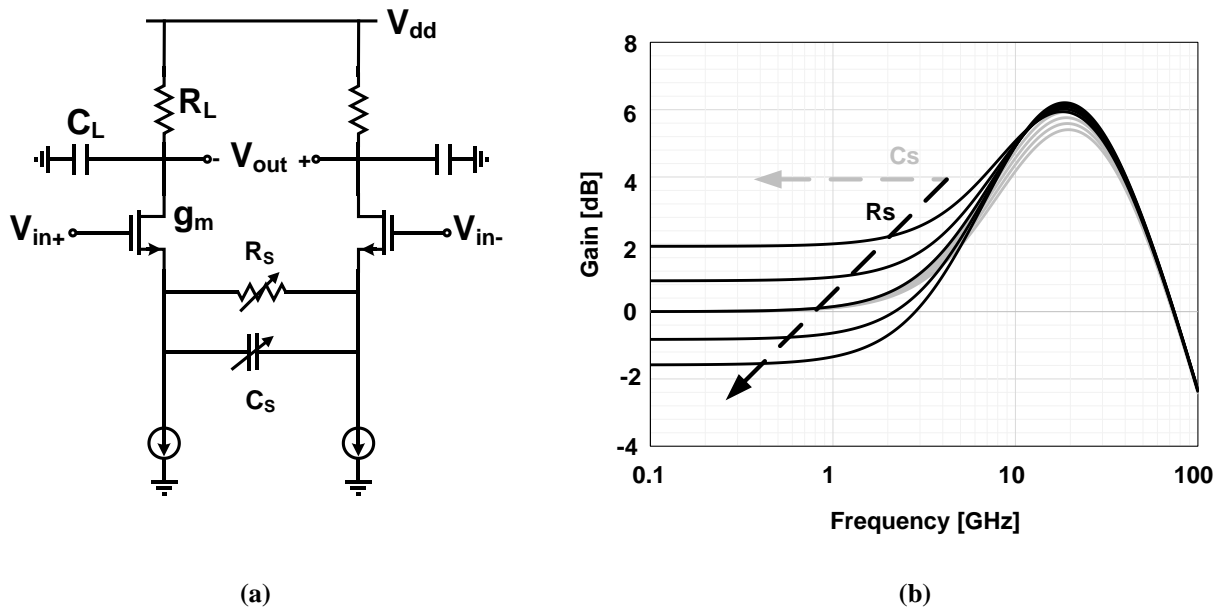


Figure 3.2 Schematic of traditional CTLE and transfer function

The high-frequency boost of CTLE compensates the high-frequency loss of a channel. In the following paragraphs, the characteristics of CTLE are analyzed both in frequency and time domain. Insights will be given to explain how the CTLE characteristics influence the eye diagram.

3.2.1 One-stage equalizer

Figure 3.3a plots the inverse magnitude of the frequency response of a Synectic channel [61], widely used in 25Gb/s communication, and the transfer function of a one-stage CTLE. By using this equalizer cascaded with the channel, the loss at Nyquist frequency (12.5Gb/s) is reduced from

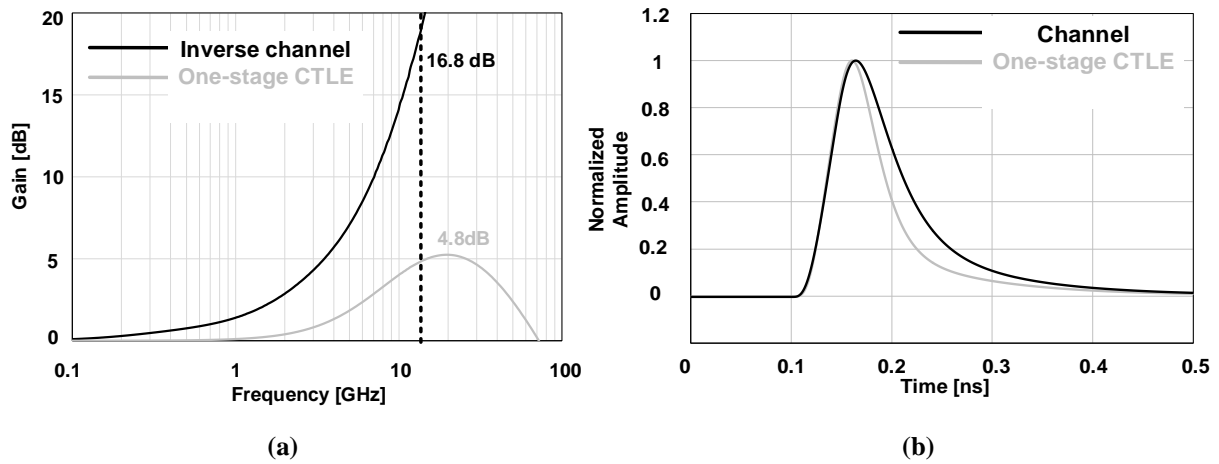


Figure 3.3 Frequency and symbol response of channel and CTLE

Table 3.1 Cursors in symbol response of the channel and one-stage CTLE

| | 1st pre-cursor | 1st post-cursor | 2nd post-cursor | 3rd post-cursor |
|----------------|----------------|-----------------|-----------------|-----------------|
| Channel | 0.20 | 0.57 | 0.25 | 0.13 |
| One-stage CTLE | 0.13 | 0.40 | 0.14 | 0.08 |

16.8dB to 12dB. Figure 3.3b shows the single-symbol response of the channel alone and of the channel with the cascaded CTLE. Clearly, the addition of the CTLE reduces the pulse-spreading effect across the bit boundary. Looking at the eye diagrams, shown in Figure 3.4., the inter-symbol interference is reduced by introducing the CTLE after the channel.

Looking again at Figure 3.3, the inverse of the channel response has a sharper slope than the response of the one-stage CTLE at Nyquist frequency. This is attributed to the dielectric loss of the channel, relevant as the operation frequency increases.

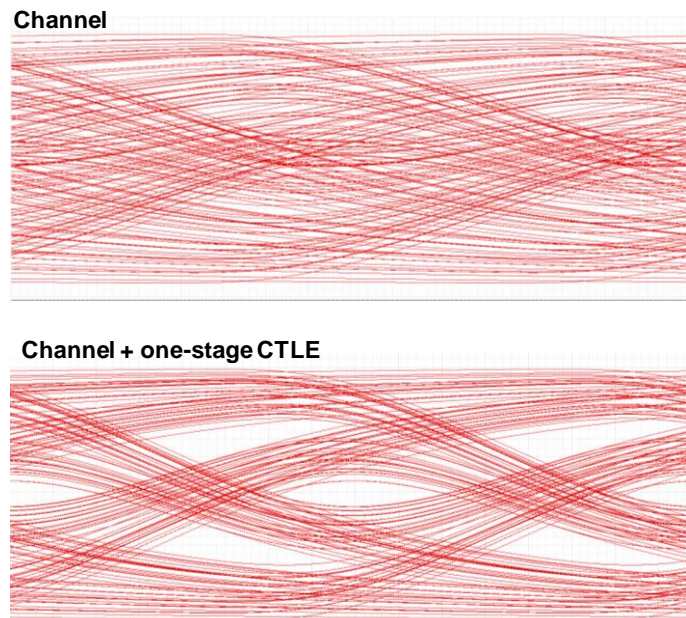


Figure 3.4 Eye diagram of one-stage CTLE equalization

3.2.2 Cascaded equalizer

The equalization of one-stage CTLE is not enough to follow the slope of a 15~20dB loss channel. For better compensation of the channel loss, one possible solution is to cascade multiple CTLE stages. This yields a more precise equalization at Nyquist frequency with the help of an additional zero-pole pair. Figure 3.5 shows the enhanced frequency compensation from a two-stage cascaded CTLE, both in the frequency domain and in the isolated symbol time-domain response. Both horizontal and vertical eye openings are further improved and are shown in Figure 3.6.

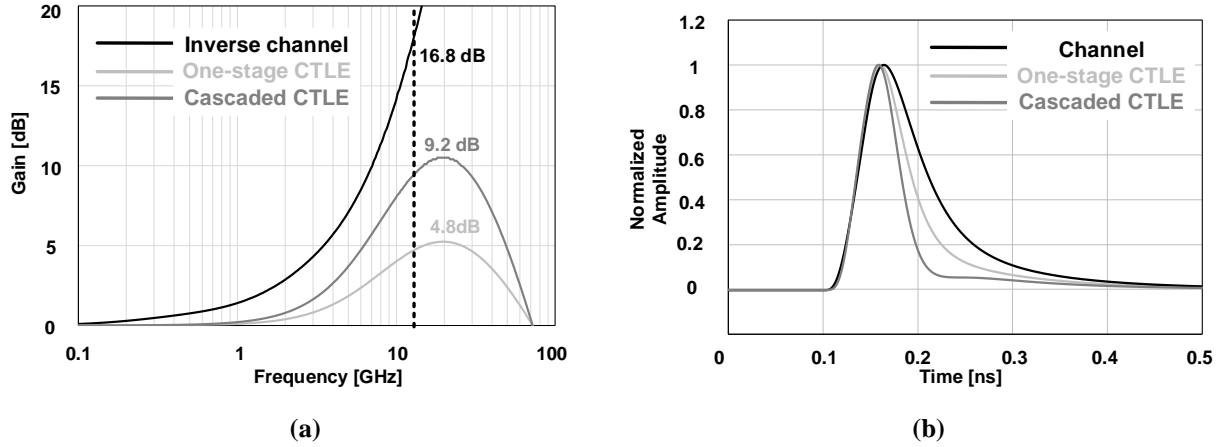


Figure 3.5 Frequency and symbol response of one-stage and cascaded CTLE comparison

Table 3.2 Cursors in symbol response of the channel, one-stage and cascaded CTLE

| | 1st pre-cursor | 1st post-cursor | 2nd post-cursor | 3rd post-cursor |
|----------------|----------------|-----------------|-----------------|-----------------|
| Channel | 0.20 | 0.57 | 0.25 | 0.13 |
| One-stage CTLE | 0.13 | 0.40 | 0.14 | 0.08 |
| Cascaded CTLE | 0.08 | 0.21 | 0.05 | 0.04 |

Channel + Cascaded CTLE

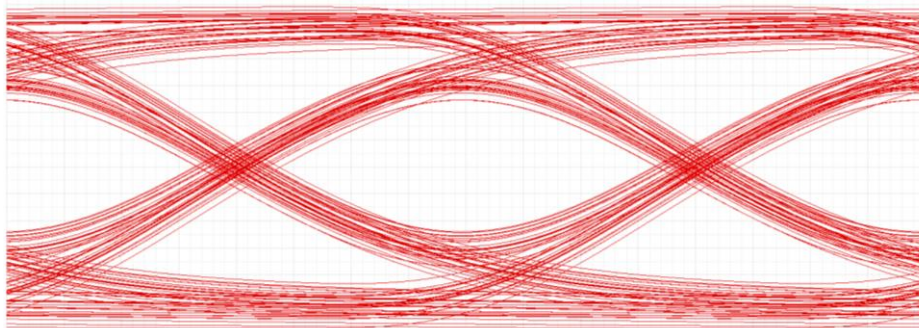


Figure 3.6 Eye diagram of a cascaded CTLE equalization

3.2.3 Low frequency equalizer

On the contrary of dielectric loss, the skin effect which is responsible for the resistive loss of the channel, is critical for equalization at low frequency. The skin effect introduces a smooth roll-off in the channel profile in the lower frequency region. Looking at the isolated symbol response in time domain, the skin effect introduces a small but long tail of ISI. This mechanism is responsible for signal integrity issues with long sequences of equal bits. The low frequency (LF) equalizer is proposed to compensate the skin effect. There are multiple methods to realize a LF equalizer, with a feedback or feedforward structure [19-20]. In the simplest case, an additional RC degenerated differential pair can be added to shape the LF transfer function, as shown in Figure 3.7. Figure 3.8 compares the frequency response and isolated symbol response eye diagram with and without the LF equalizer.

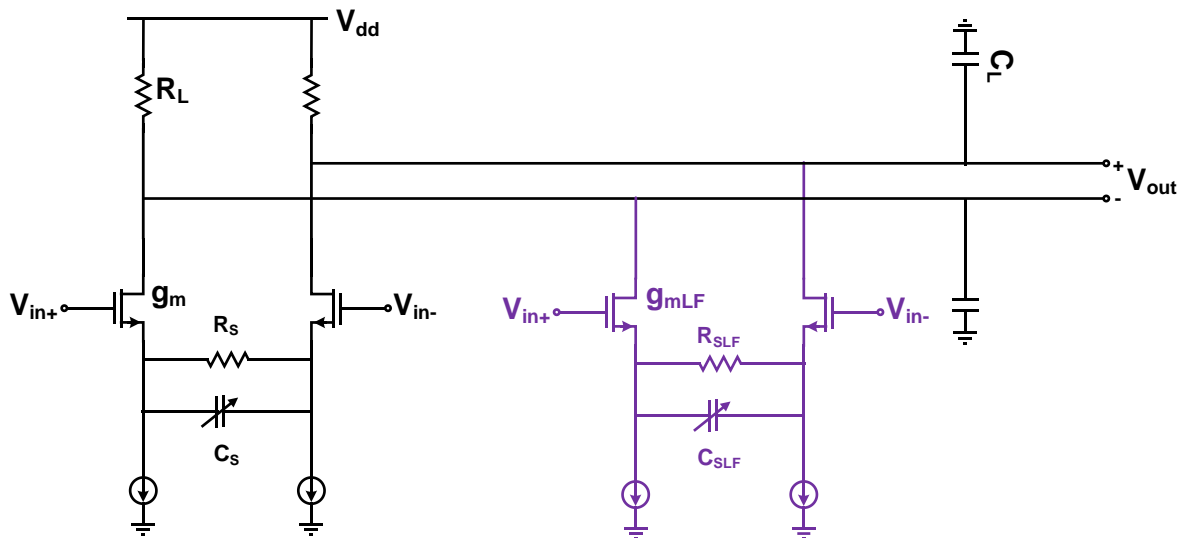
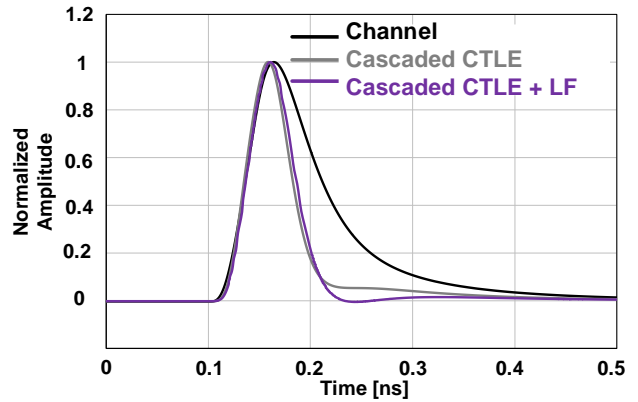
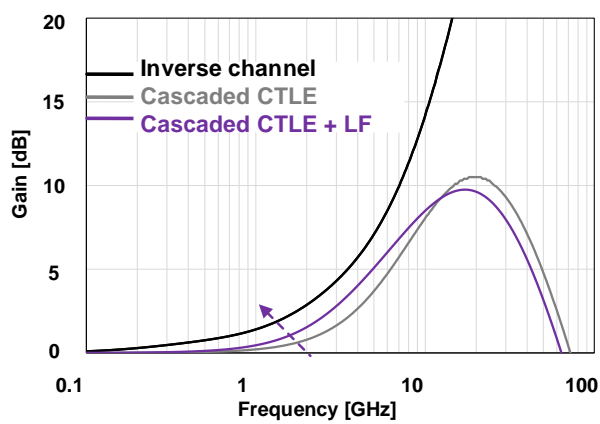


Figure 3.7 Schematic of a single CTLE with LF equalizer

The symbol response with the LF equalizer shows reduced ISI, especially in the tail of the symbol as shown in Table 3.3. Figure 3.9 shows the eye diagrams with and without LF equalization. Both vertical and horizontal eye openings are significantly improved with the aid of LF equalization.



(a)

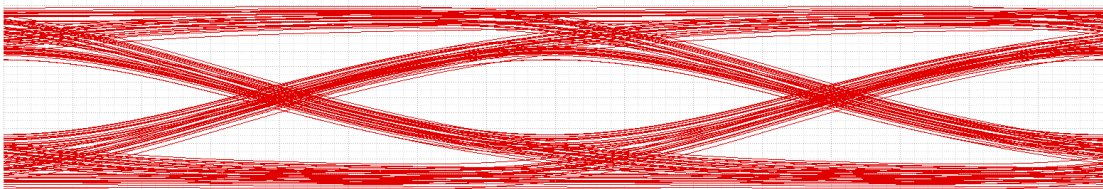
(b)

Figure 3.8 Frequency and symbol response of the cascaded CTLE with/without LF equalizer

Table 3.3 Cursors in symbol response of the channel, cascaded CTLE and cascaded CTLE with LF equalizer

| | 1st pre-cursor | 1st post-cursor | 2nd post-cursor | 3rd post-cursor |
|-----------------------|----------------|-----------------|-----------------|-----------------|
| Channel | 0.20 | 0.57 | 0.25 | 0.13 |
| Cascaded CTLE | 0.08 | 0.21 | 0.05 | 0.04 |
| Cascaded CTLE with LF | 0.08 | 0.23 | -0.005 | 0.01 |

Channel + Cascaded CTLE



Channel + Cascaded CTLE + LF Equalizer

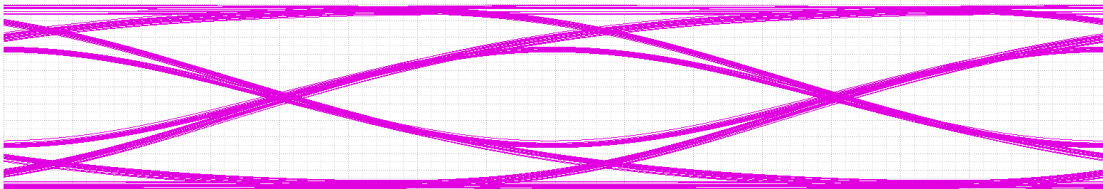


Figure 3.9 Eye diagram of the cascaded CTLE with/without LF equalizer equalization

3.2.4 Split-path equalizer

The split-path equalizer, which divides the signals into multiple paths, can be an alternative to the degenerated differential pair [21]. A simple split-path is shown in Figure 3.10, in which one path comprises a high pass filter to amplify the high frequency component and the other path is an all pass filter or a low pass filter to match the time delay of the first path. Instead of tuning R_s and C_s in the degenerated differential pair, the gain of the variable-gain-amplifier (VGA) A_0 and B_0 are used to change the DC gain and zero position in this equalization scheme. This architecture

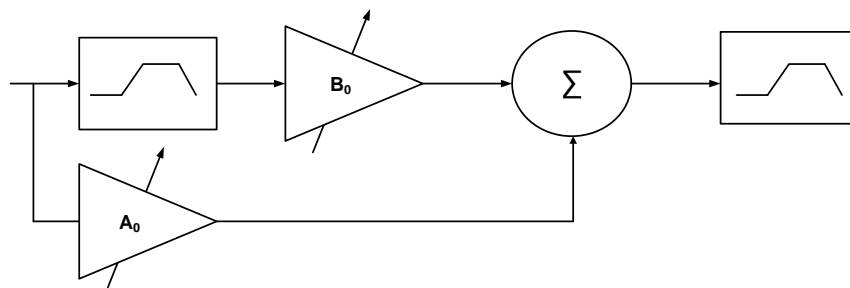


Figure 3.10 Block diagram of a simple split-path equalizer

provides an option to change the DC gain and zero position independently. Furthermore, the resolution of VGAs, which are commonly implemented with transconductors, can be made much finer than what achievable by trimming Rs and Cs. Therefore, a more precise shaping of the transfer function targeting the inverse of the channel profile can be achieved with this structure. An advanced split-path equalizer shaping the transfer function in piece-wise is shown in Figure 3.11. The analog equalizer consists of three different paths in order to create the desired frequency response. Two bandpass filters are followed by variable-gain-amplifiers (VGA) that allow independent gain control at f_1 and f_2 . The gain at frequency f_1 and f_2 can be adjusted separately, and it relaxes the adaption engine to get optimum tuning. The VGA gain A_0 provides a path for low frequency data. The bandpass filter is implemented by a differential pair with an RLC load, including a varactor that allows tuning of the center frequency. The VGA is implemented using a differential pair with resistive degeneration controlled by switches. The split-path equalizer enables a separately tuning of zeros position, which provides a method to flexibly shape the transfer function in a multiple zeros system [22].

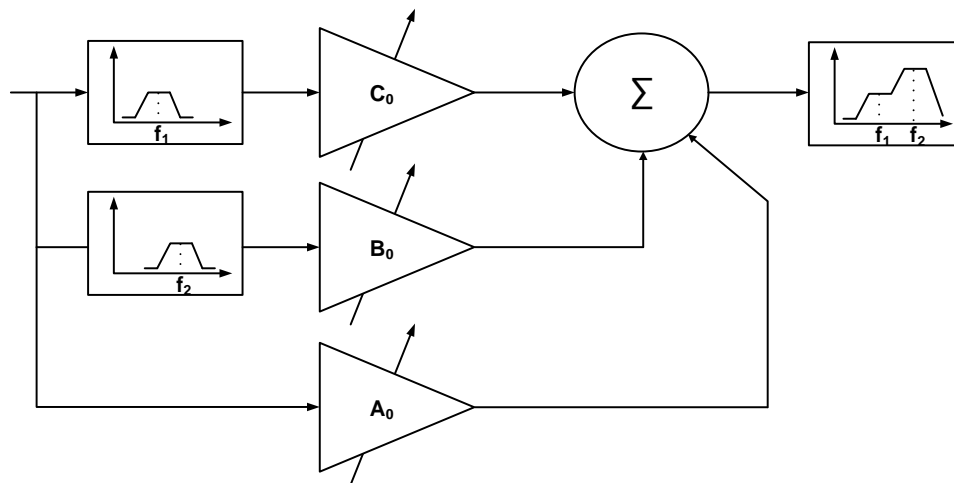


Figure 3.11 Block diagram of an advanced split-path equalizer

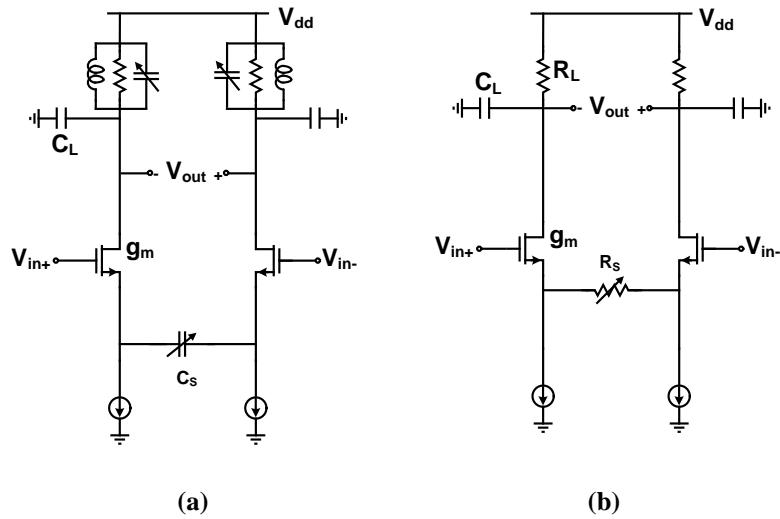


Figure 3.12 Schematic of the bandpass filter (a) and VGA (b)

3.3 Broadband techniques

As the operating frequency of analog equalizers increases, broadband techniques are necessary to extend the bandwidth of the gain stages. There are several ways to extend bandwidth, in this chapter the inductive peaking and negative cap canceling techniques will be presented.

3.3.1 Inductive peaking

With the advent of monolithic inductors, inductive peaking techniques have become feasible in integrated circuits. The idea is to allow the capacitance that limits the bandwidth to resonate with an inductor, thereby improving the speed. The resonance must, of course, occur with minimal peaking and overshoot so as to provide a well-behaved response to random data.

Shunt peaking

Shunt peaking is a bandwidth extension technique in which an inductor connected in series with the load resistor shunts the output capacitor. The simplified schematic showing this technique is reported in Figure 3.13. Treating the transistor as a small-signal dependent current source, the gain is simply the product of the transistor transconductance, g_m , and the impedance of the passive load,

$Z(s)$. Because the transistor transconductance is approximately constant over frequency, only the impedance is considered hereafter. For the shunt-peaked network that is shown in Figure 3.13b:

$$Z(s) = \frac{R_L + sL_d}{1 + sR_L C_{fixed} + s^2 L_d C_{fixed}}$$

The inductor L introduces a zero that rises the impedance with frequency, compensating the decreasing impedance of the capacitor, and thus extends the 3dB bandwidth. An equivalent explanation for increased bandwidth is reduced rise time. That is, the inductor rejects current flow through the resistive branch so, in response to an input step, more current initially charges output capacitor reducing the rise time.

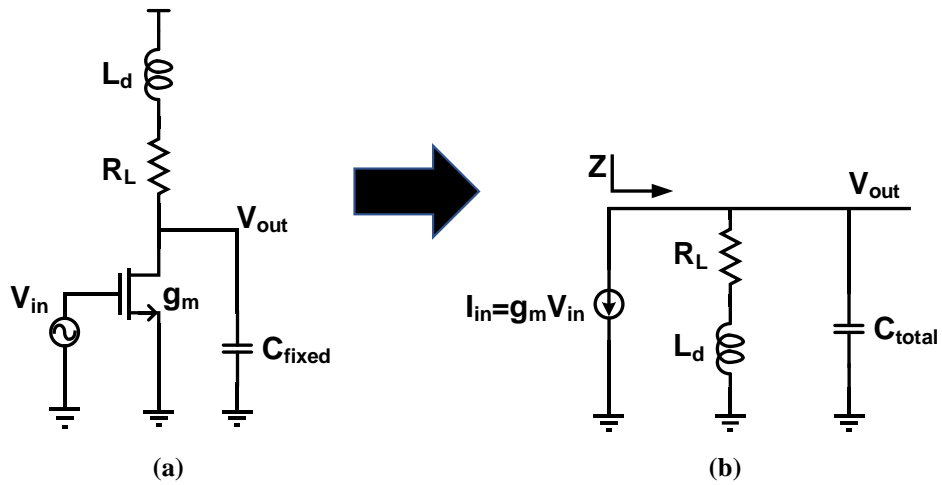


Figure 3.13 Shunt peaking schematic and equivalent small signal model

Defining the parameters $m = \frac{R_L^2 C_{total}}{L_d}$, $\omega = \frac{1}{R_L C_{total}}$. The shunt peaking network can be expressed

as
$$Z(s) = \frac{1 + s/m\omega_0}{1 + s/m\omega_0 + s^2/m\omega_0^2}$$
.

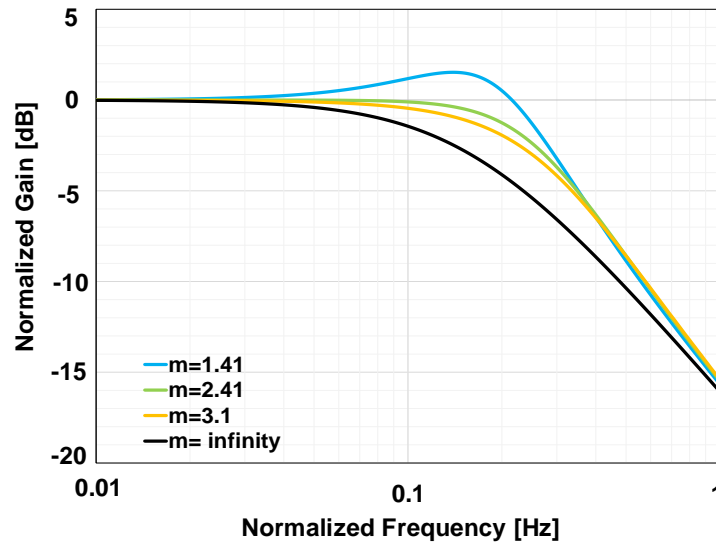


Figure 3.14 Frequency response of an amplifier with shunt peaking

The normalized voltage gain of the stage, for different m values, is plotted in Figure 3.14. $m=1.41$ gives the maximum bandwidth extension, $m=2.41$ gives the maximally flat response, $m=3.1$ gives the response with maximally flat phase.

Shunt series peaking

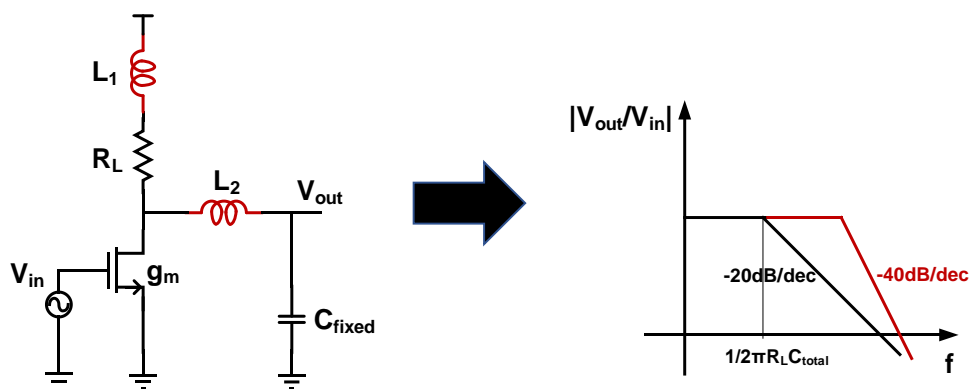


Figure 3.15 Schematic and simplified transfer function of shunt series peaking

Series peaking can be added to the shunt peaking structure to realize shunt-series peaking. The additional series peaking converts the system to a second order filter to further improve the bandwidth extension. Also, the roll-off of the voltage gain is sharper than that of shunt-only inductive peaking. As a drawback, the series peaking enlarges the time delay of the amplifier.

3.3.2 Negative capacitance

In order to reduce the bandwidth limiting effect due to the capacitance at a given node, an active network presenting a negative capacitance can be added to the node. Differential signal paths lead themselves to this method particularly well.

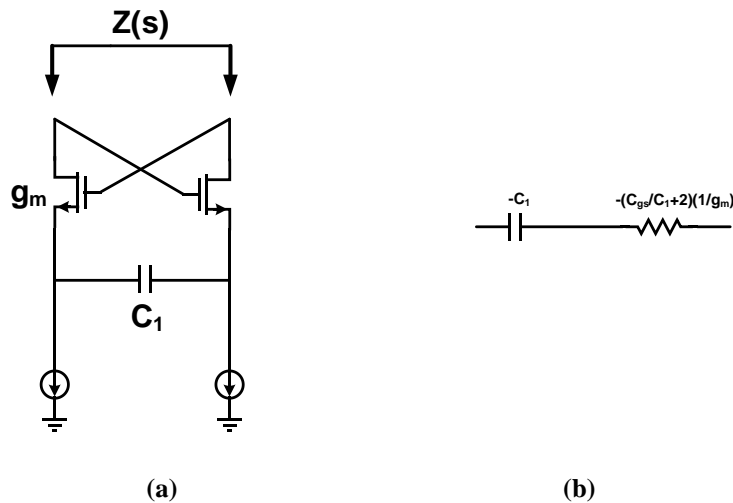


Figure 3.16 Schematic of negative capacitance and simplified small signal model

The negative capacitance can be implemented with a cross-coupled differential pair with capacitive-only degeneration. The impedance at the drain of the transistors in Figure 3.16 is

$$\frac{1}{Z} = \frac{-1 + sCgs/g_m}{\frac{1}{sC_1} + (\frac{Cgs}{C_1} + 2) \frac{1}{g_m}}$$

At angular frequencies well below the ω_T of the transistors ($\omega \ll \omega_T = g_m/C_{gs}$), the second term in the numerator is negligible, yielding an impedance consisting of a negative capacitance that is equal to $-C_1$ in series with a negative resistance equal to $-(C_{gs}/C_1+2)(1/g_m)$.

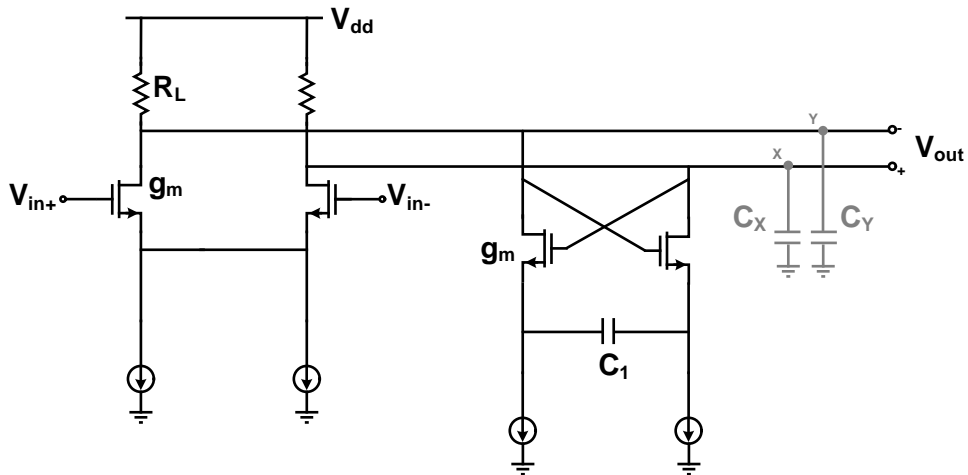


Figure 3.17 Example of negative capacitance canceling

Figure 3.17 shows a typical arrangement employing this technique to (partially) cancel the capacitance at nodes X and Y . For complete cancellation, $2C_1 = C_X = C_Y$. However, if, due to mismatches, $2C_1 > C_X$, then the cross-coupled pair may turn into a relaxation oscillator. It can be shown that the condition of oscillation is given by $g_m R_L \geq \frac{C_1}{C_1 - C_X/2}$ [6]. The circuit may still exhibit significant ringing and hence introduce ISI even without oscillation. For this reason, the cross-coupled pair is commonly exploited only for partial cancellation of C_X and C_Y , particularly if a small ISI is desired.

3.4 Equalizer adaptation overview

In order to optimize the equalization for varying channels, process-voltage-temperature (PVT) and different data rates, it is mandatory to implement the adaptation loop to tune the equalizer. The general concept of equalizer adaptation is illustrated in Figure 3.18 [21]. In the adaptation loop, an error signal is generated by measuring the quality of the equalizer performance, and then the tuning signal generator converts the error signal into a tuning signal to adjust the coefficients of the equalizer.

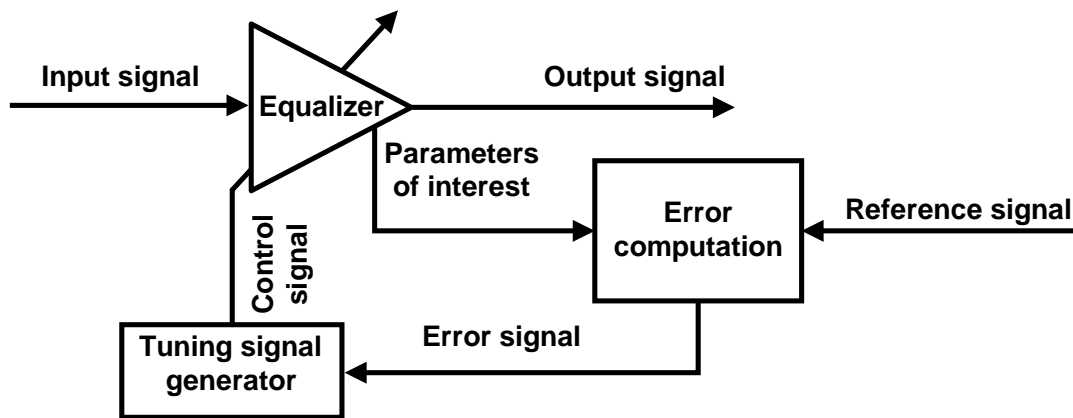


Figure 3.18 Equalizer adaptation concept

Several adaptive algorithms based on different approaches to calculating the error signal have been implemented in advanced analog equalizers. In paper [25], the spectrum balancing technique is implemented by measuring the power spectrum density of low-frequency and high-frequency components. In paper [63], the error signal in the adaptive algorithm is calculated by comparing low-frequency and high-frequency average amplitude. In paper [64], an eye monitor is included in the adaption loop to record the data-edge distribution of the output waveforms, and the target of the algorithm is to minimize the standard deviation of the data-edge.

Another popular algorithm in which the error signal is calculated by comparing the mean-square-errors (MSE) between recovered signals and reference signals is widely implemented in recently published equalizers [21]. The general concept of the algorithm of the MSE is shown in Figure 3.19. If there are N variables $p = [p_1 p_2 \dots p_N]^T$ of the equalizer, the cost function $J_{MSE}(p)$ is defined as: $J_{MSE}(p) = E[(y - d)^2] = E[e^2]$. Since it's not practical to measure the statistics of signal d and y for calculation of average- square-errors, the main implementations are least-mean-squares (LMS) that consist of the instantaneous value instead of the expected value. The cost function $J_{LMS}(p)$ is defined as: $J_{LMS}(p) = (y - d)^2 = e^2$. For the equalizer in which the state-signals are uncorrelated like the transversal filter, the cost function surface is guaranteed unimodal as shown in Figure 3.20 [30]. Thus, the Gradient-descent search LMS algorithm can be applied to such kinds

of equalizers. The variables of the equalizer are updated as $p(k + 1) = p(k) - \mu \cdot \nabla J_{LMS}(p)$, where μ is a constant to determine the convergence speed.

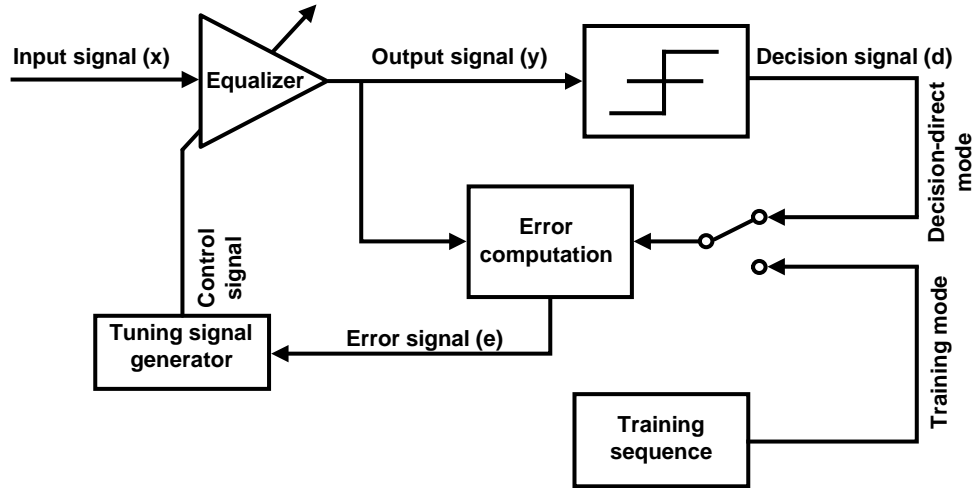


Figure 3.19 MSE adaptation concept

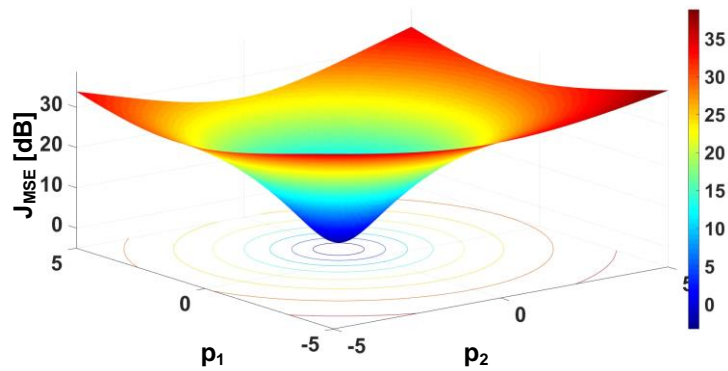


Figure 3.20 Cost function surface with uncorrelated state-signals

Chapter 4 Flexible transversal continuous-time linear equalizer operating up to 25Gb/s in 28nm CMOS

Abstract

A flexible transversal continuous-time linear equalizer is presented in this chapter. Transceivers for backplane serial links at 25Gb/s and beyond demand equalizers with high accuracy and flexibility in matching the channel response. To satisfy the high accuracy requirement, in this chapter, a very flexible continuous-time linear equalizer (CTLE) with a transversal architecture is proposed. In chapter 3, the concept to tune gain and zeros separately in a split-path equalizer have been shown. Similar to such an approach, the proposed equalizer features variable DC gain and two zeros that can be tuned independently. The transversal architecture makes it compatible with gradient descent algorithms, allowing optimal adaptation of the gain and zero frequency locations and improved equalization accuracy. The CTLE was realized in a 28nm CMOS technology and measurements are presented at data rate from 5Gb/s to 25Gb/s across 20dB-loss channels. Core power dissipation is 17mW from 1V supply and horizontal eye opening at BER= 10^{-12} is larger than 50% UI, comparing favorably against previously reported equalizers targeting similar data-rate and channel loss.

4.1 Introduction

As introduced in chapter 1, the explosive growth of internet traffic, driven by multimedia and cloud services, continuously pushes for higher bandwidth and aggressive scaling of I/Os for high-speed electrical links. Ensuring link reliability and low power consumption are key design targets in view of the increased I/O densities on the same chip. Recent standards have been introduced to support NRZ signaling with data-rate up to 25-28 Gb/s and transceivers built-in advanced CMOS technology nodes have been demonstrated [20, 23]. At this speed, typical backplanes of few tens of cm length introduce a channel loss in excess of 30dB at Nyquist frequency, and improvement in channel equalization is mandatory as a consequence of the large inter-symbol interference (ISI). Equalizers must be flexible, operating at variable speed over different channels, and continuously adapted to counteract environmental drifts (temperature and humidity) responsible for a slowly varying channel transfer function. The common practice at

receiver side is the combination of a simple continuous-time linear equalizer (CTLE) with the decision feedback equalizer (DFE). The CTLE has evolved from a simple high-pass filter to more complex topologies with multiple zero-pole pairs in transfer function to have a more accurate channel loss compensation [20]. Considering the shape of a typical channel transfer function, the slope of the attenuation profile rises with frequency, and it ranges between 10dB/dec to 30 dB/dec. To get accurate channel inversion, tuning zeros of CTLE separately is necessary. Analog tuning techniques have been proposed in recent adaptive equalizers [24-28]. However, those techniques are not able to control multiple zeros of the equalizer independently, so that they are not suitable to optimize the frequency of multiple CTLE zeros separately.

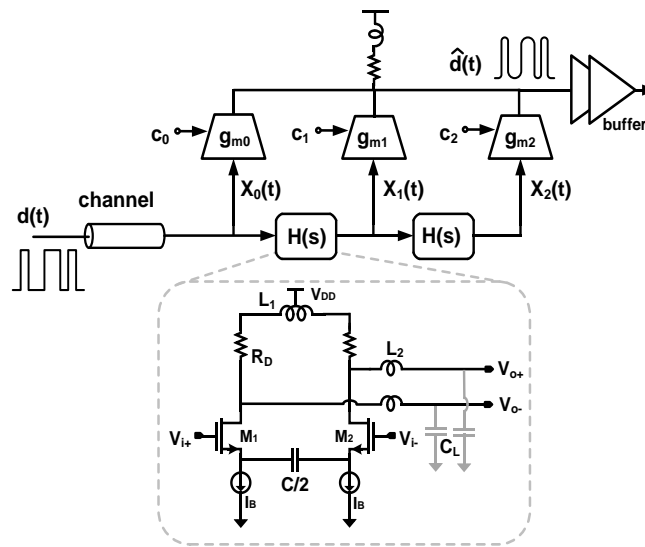


Figure 4.1 Block diagram of the transversal CTLE and schematic of the block $H(s)$ (single-ended signals are used in the block diagram for better readability)

This work describes a CTLE with the transversal architecture shown in Figure 4.1, featuring a transfer function with variable gain and multiple zeros. The transversal configuration allows CTLE adaptation with gradient descent algorithms, such as LMS, thus allowing optimal tuning of the gain and zero frequency locations for fine equalization. The equalizer has been published in [29]. The CTLE architecture is described in section 4.2 of this chapter, and circuit design considerations are presented in section 4.3, while measurement results and comparison are shown in section 4.4. From experimental results, the equalizer, realized in 28nm CMOS, recovers ~ 20 dB loss at data rate variable from 5Gb/s to 25Gb/s, over backplanes of different lengths. The horizontal eye opening at $BER=10^{-12}$ is equal or larger than 50%, and the core

power dissipation is 17mW from 1V supply. Experimental results compare favorably against previously reported equalizers targeting similar data-rate and channel loss.

4.2 Equalizer architecture and design

The transversal path of the equalizer in Figure 4.1 is composed of capacitively degenerated differential pairs with transfer function $H(s)$. Transconductors are connected at the input, intermediate and output taps, and the output currents are summed in a shared resistive load providing the output signal $\hat{d}(t)$. Each differential pair introduces ideally a zero in the origin and, assuming that poles are at frequency sufficiently high, $H(s) \approx \tau s$ with $\tau = R_D C$. Therefore, the approximated transfer function of the equalizer is:

$$\begin{aligned} H_{eq}(s) &= c_0 + c_1 \tau s + c_2 (\tau s)^2 \\ &= c_0 (1 - s\tau_{z1})(1 - s\tau_{z2}) \end{aligned} \quad (4.1)$$

with

$$\tau_{z1,2} = \tau (-c_1 \pm \sqrt{c_1^2 - 4c_0 c_2}) / 2c_0. \quad (4.2)$$

Equation 4.1 proves that the equalizer features variable DC gain and two zeros with time constant τ_{z1} and τ_{z2} . From equation (4.2), the zeros can be shifted across frequency by changing the transconductors gains ($c_0..c_2$) or the time constant $\tau = R_D C$.

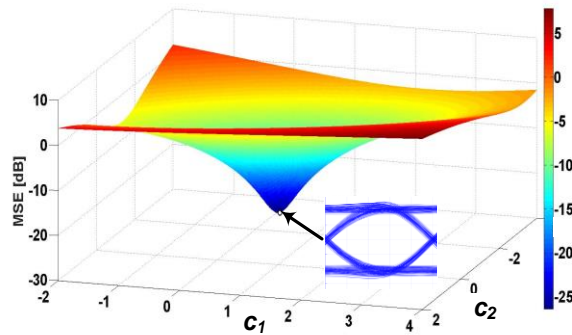


Figure 4.2 MSE surface at 25Gb/s of the equalizer cascaded with a 20dB loss backplane channel

Thanks to the transversal architecture, the CTLE response is a linear combination of the control coefficients ($c_0..c_2$). As a result, considering the Mean Square Error, $MSE = E[(\hat{d}(n) - d(n))^2]$ ($\hat{d}(n)$ is the ideal output signal and $d(n)$ is the output signal from the equalizer), as the performance criterion for adaptation, the MSE surface is a paraboloid [30], with a regular shape and a global minima. To gain insight, Figure 4.2 shows the MSE surface versus c_1 and c_2 ($c_0=1$ is assumed), simulated with Matlab at 25Gb/s data-rate considering a 20dB loss backplane channel model. With an eye amplitude of 1V0pk, the minimum MSE is -26dB (the eye diagram at the point of minimum MSE is reported as an inset in Figure 4.2). Similar results were achieved considering a broad variety of backplane channel models. Thanks to the regular shape of the surface in Figure 4.2, adaptation with convergence to the optimal set of coefficients can be achieved with a gradient descent algorithm, by using the eye monitor circuits commonly available in a receiver, for MSE estimation. The transversal equalizer architecture allows also the implementation of a fast convergence signed-LMS algorithm by adding comparators (not implemented in this chip) to sense the equalizer state signals at the intermediate nodes of the transversal path [30]. Matlab simulations confirm the importance of using two zeros, located at different frequencies, to improve equalization. In fact, the minimum MSE with a single zero ($c_2=0$), or with two zeros at the same frequency ($c_1=2\sqrt{c_0c_2}$) rises from -26dB to -14dB and -16dB respectively.

Finally, it is worth noticing that the same transfer function given by equation (4.1) can be achieved by cascading two differential pairs with shunt RC source degeneration, the common circuit topology for CTLE as discussed in Chapter 3 [24, 25]. The DC gain and zero locations could be controlled by tuning the degeneration resistors and capacitors, but the equalizer response is not linear with respect to the control parameters. As a result, the MSE surface is irregular and may have local minima as shown in Figure 4.3, thus making adaptation with gradient descent more difficult and not ensuring convergence to the optimal result. Moreover, the lack of access to the equalizer's internal state signals precludes the simple implementation of the LMS algorithm.

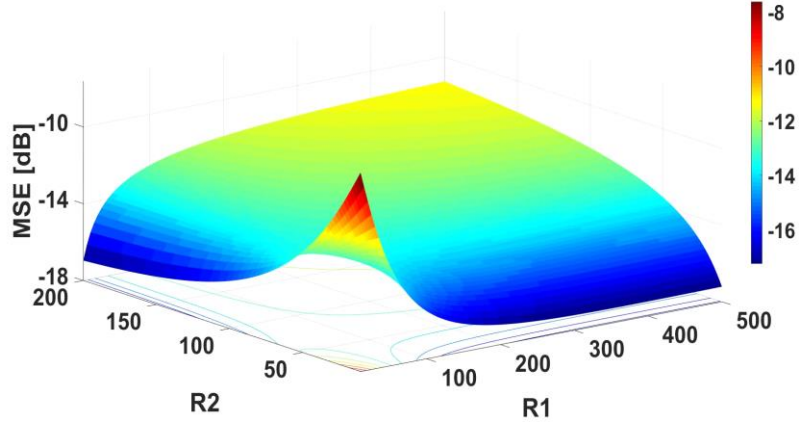


Figure 4.3 MSE surface from a cascaded CTLE

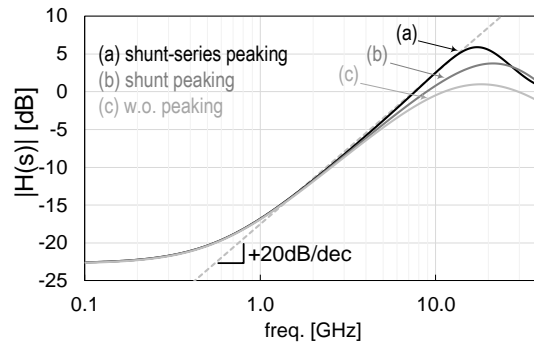


Figure 4.4 Simulated $H(s)$ with different peaking inductors combinations

4.3 Equalizer circuits design

The equalizer was designed in a 28nm CMOS technology targeting 25Gb/s maximum data rate. The two capacitively degenerated stages in Figure 4.1 are designed to approximate the idealized transfer function $H(s)=\tau s$. Neglecting the effect of inductive peaking, the transfer function can be expressed as:

$$H(s) = -\frac{sR_D C}{1 + s\frac{C}{g_{m1,2}}} \frac{1}{1 + sC_L R_D}$$

where poles are

$$\omega_{p1} = \frac{g_{m1,2}}{C} \quad \omega_{p2} = \frac{1}{C_L R_D}$$

Setting the frequency of poles much larger than the interested frequency (0~12.5GHz), the approximation $H(s)$ is well matched. For each stage, the bias current is 4mA and M1,2 are 20 μ m/28nm transistors featuring $g_m=18$ mS. From equation (4.2), being $\tau=R_D C$, rising C moves the CTLE zeros at low frequency (as required for operation at low data-rate) without requiring excessive gain of taps c_1, c_2 (i.e. power consumption) or reducing c_0 , the low-frequency CTLE gain, yielding SNR penalty. At the minimum capacitance value ($C=150$ fF) the pole at the source nodes of M1,2 is at $g_m/2\pi C=19$ GHz. The load resistors R_D are 135 Ω . Shunt (L_1) and series (L_2) peaking inductors are added for bandwidth extension while driving the load capacitance ($C_L\sim 55$ fF) mostly determined by the cascaded tap amplifier. The simulated transfer function $H(s)$ when $C=150$ fF without peaking, with L_1 only and with L_1-L_2 is shown in Figure 4.4. With shunt-series peaking $H(s)$ peaks at 17.5GHz and fits well the idealized transfer function $H(s)=\tau s$, with $\tau=20$ psec, (dashed line in Figure 4.4) from 1GHz to above the Nyquist frequency at 25Gb/s ($f_N=12.5$ GHz). The finite resistance of the tail current sources I_b is responsible for gain flattening below 1GHz. As long as the gain is low, this effect does not compromise the equalization performance, being it compensated by adjusting c_0 , the control coefficient that sets the overall DC gain of the equalizer.

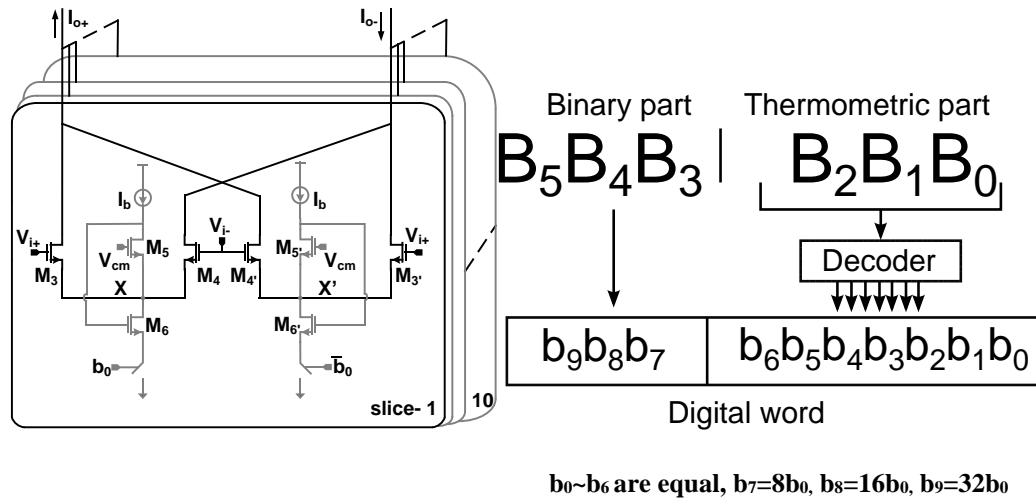


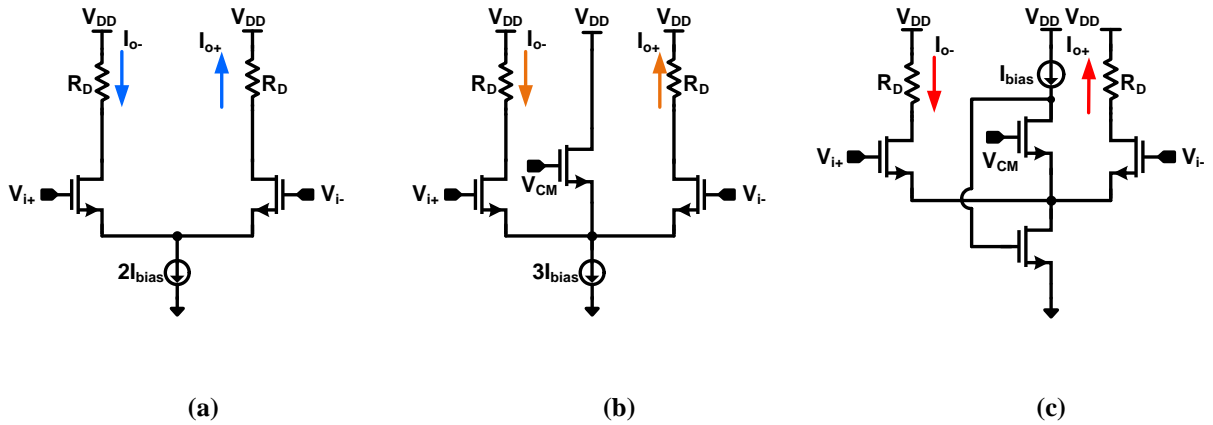
Figure 4.5 Schematic of a tap amplifier

The simplified circuit schematic of a tap amplifier is drawn in Figure 4.5. Each amplifier comprises ten slices in parallel providing a gain programmable with 6-bit resolution. The three identical tap

amplifiers (g_{m0} , g_{m1} , g_{m2} in Figure 4.1) are connected to the same load to control the gain. To ensure gain monotonicity with respect to the digital control code, essential for adaptation, a combination of binary- and thermometric-weighted slices are used. The circuit in each slice is made of two differential transconductors ($M_{3,4}$ and $M_{3,4'}$) driven by the same input signals but delivering currents with opposite sign, allowing the overall gain to span from negative to positive values.

The linearity of a traditional differential pair is poor due to the fixed tail current source. A pseudo-differential pair has better linearity without removing the limit set by the constant biasing current source, but requires a proper circuit for setting the bias point independently from the input common-mode. Based on this, a class-AB pseudo-differential pair with a flipped-voltage follower is proposed. Transistors $M_{5,5'}$ are biased at the gate with the common mode of the input signal (sensed at the center tap of a resistive divider, not shown) and together with $M_{6,6'}$ form flipped voltage followers forcing low impedance at the common source nodes X , X' . In this way $M_{3,4}$ and $M_{3,4'}$ work as Class-AB pseudo-differential pairs, featuring enhanced linearity. The flipped-voltage follower provides better sourcing capability and keeps the common source node more stable than using a simpler common drain transistor as shown in Figure 4.6b. This is proved by the simulated transfer characteristic in Figure 4.7 for the 3 transconductors in Figure 4.6. The flipped voltage follower transconductor has twice the linear range than a simple differential pair, at the same quiescent current, leading to an input 1dB compression point near $1V_{pk-pk}$. In this way the equalizer can withstand large input swing with low distortion, thus preserving high SNR when recovering large channel loss. The quiescent current consumption of each tap amplifier is 3mA and maximum gain is 14mS.

The output currents from the three-tap amplifiers in the equalizer are summed in a shared load, realized with resistors and shunt peaking inductors for bandwidth extension. The equalizer is followed by a programmable-gain two-stage buffer to drive the instruments for experimental characterization.



- (a) Differential pair
- (b) Differential pair with common-drain-follower (CDF)
- (c) Differential pair with flipped-voltage-follower (FVF)

Figure 4.6 Tap amplifier topologies

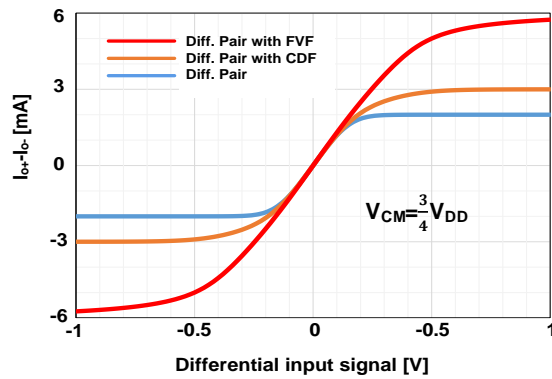
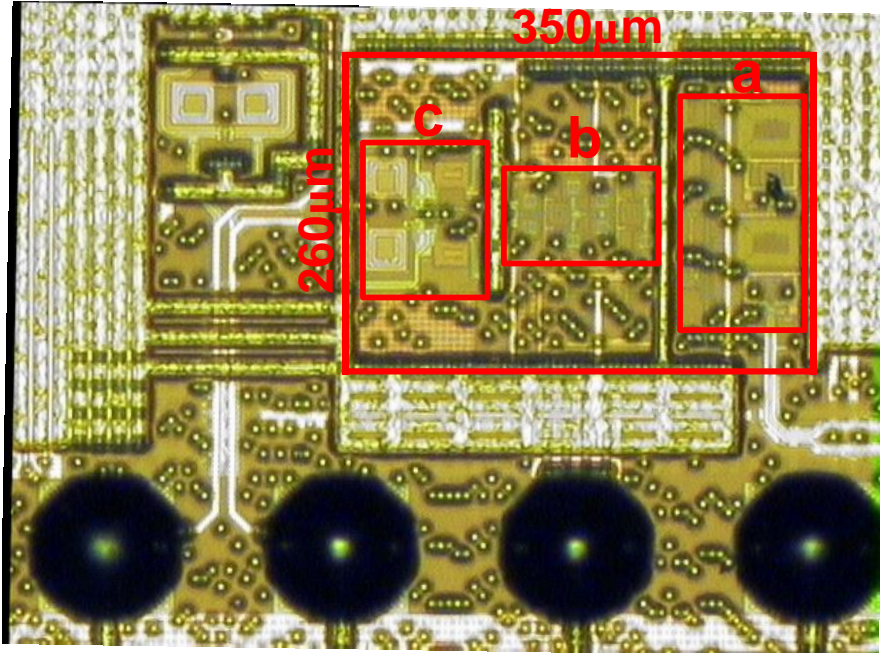


Figure 4.7 Simulated trans-characteristics

4.4 Experimental results

Prototypes of the equalizer have been fabricated in a 28-nm CMOS process from STMicroelectronics. A photograph of the die is shown in Figure 4.8, where the core active area (260 μm x 350 μm) is highlighted. Test chips were encapsulated in plastic flip-chip BGA packages and mounted on a PCB for testing. The equalizer core power dissipation is 17mW and the cascaded buffer, withstanding high voltage swing with low distortion, needs 18.5mW, from 1V supply.



a: Input buffer, b: Core equalizer, c: Output buffer

Figure 4.8 Chip photograph

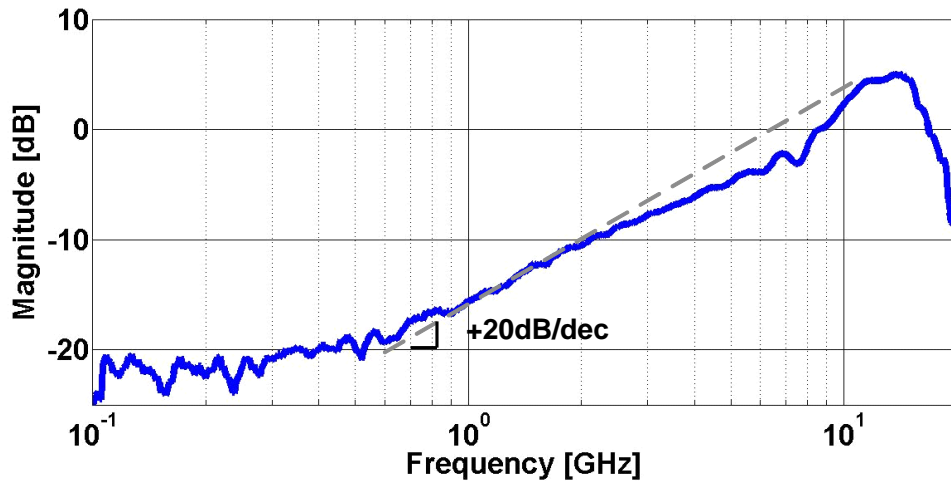


Figure 4.9 Measured transfer function of one stage $H(s)$ of the transversal path

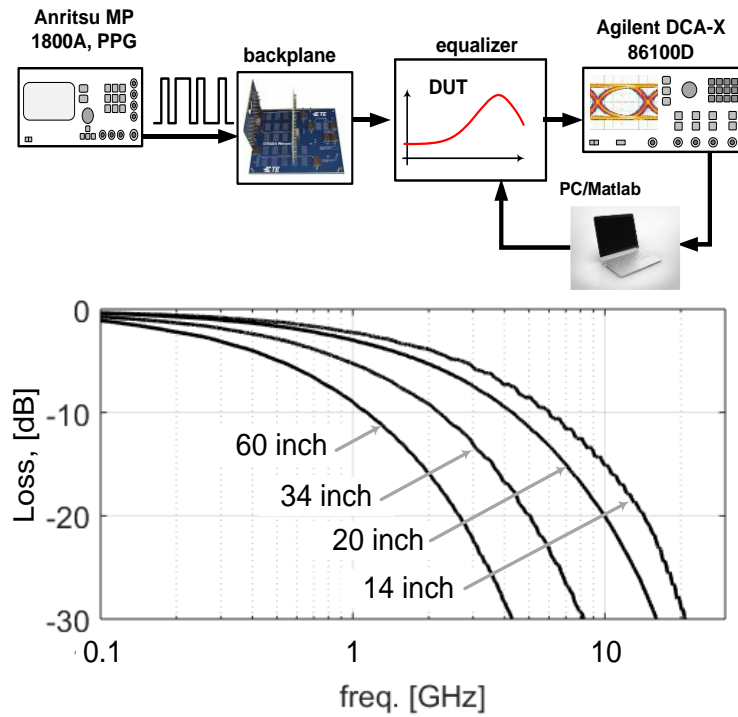


Figure 4.10 Experimental setup and loss of the different backplanes used for measurements.

First, the AC response $H(s)$ of one stage in the transversal path was tested, with a Vector Network Analyzer, by subtracting (in decibel scale) two consecutive measurements performed with the following sets of coefficients: $(c_0=0, c_1=c_{1max}, c_2=0)$ and $(c_0=c_{0max}, c_1=0, c_2=0)$. The measured transfer function can be calculated: $H(s)_{mea} = \frac{c_{1max}\tau s}{C_{0max}}$. Neglecting the mismatches of tap amplifiers, we can get $C_{1max} = C_{0max}$, and $H(s)_{mea} = H(s) = \tau s$. The result is shown in Figure 4.9. Compared to the simulated transfer function in Figure 4.4, the frequency of gain peaking (14GHz) is slightly less than expected, likely due to the underestimation of layout parasitics, but still higher than the Nyquist frequency at 25Gb/s. Equalization tests were performed with the setup in Figure 4.10. The equalizer is fed by PRBS sequences from a pulse-pattern generator transmitted over backplane channels of different lengths. The output of the equalizer is connected to a high-speed oscilloscope and the waveforms are recorded with a PC, running a Minimum-Mean-Square-Error (MMSE) adaptation algorithm to control the gain of the tap amplifiers through the on-chip I²C interface. The MSE is calculated in Matlab by comparing the sampled output data from the oscilloscope with the training sequences saved in Matlab. The flow-chart of the algorithm is shown in Figure 4.11. The PC loops continuously while updating the tree coefficients c_i ($i=0,1,2$). At each iteration, $MSE(c_{i-1LSB})$ and $MSE(c_{i+1LSB})$ are estimated from the scope trace and compared. The coefficient is then incremented or decremented according to the lower MSE value. The adaptation code was developed for testing the equalization performance, and it was not optimized for convergence speed.

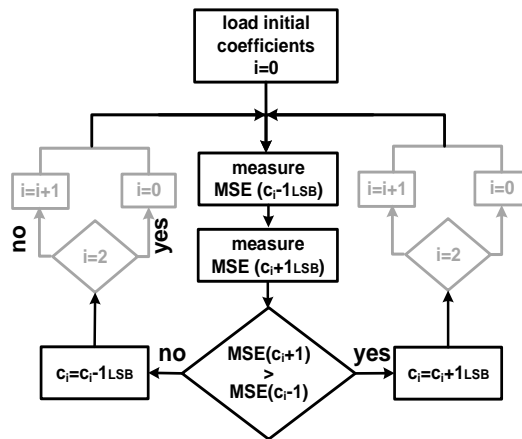


Figure 4.11 Flow-chart of MMSE adaptation algorithm.

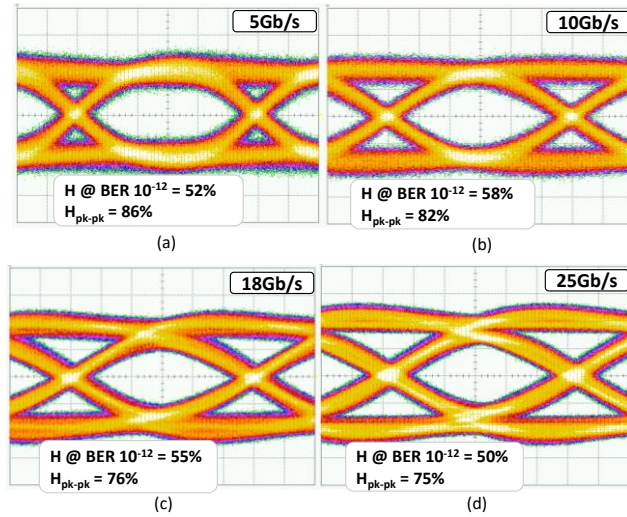


Figure 4.12 Eye diagrams after channel (20dB loss) and equalizer at data rate from 5Gb/s to 25Gb/s.

Measurements have been performed on four backplane channels, of different lengths, with the attenuation profiles reported in Figure 4.10. For each channel, the data rate is selected to have nearly 20dB loss at Nyquist. The eye diagrams, after equalization at 5Gb/s, 10Gb/s, 18Gb/s, and 25Gb/s, are reported in Figure 4.12. The pk-to-pk horizontal opening at $BER=10^{-12}$ is equal or larger than 75% and 50% respectively, yielding a good timing margin. At maximum speed, measurements were repeated by adapting the equalizer with only (a) one zero and (b) two zeros kept at the same frequency. The horizontal opening at $BER=10^{-12}$ is reduced to less than 29%, proving the advantage of having multiple zeros with frequency locations adapted independently. The performance of the transversal CTLE is summarized and compared against other equalizers targeting similar data-rate and comparable channel loss in Table 4.1. Thanks to the high flexibility and optimal adaptation, the proposed equalizer demonstrates finer equalization capability, yielding the highest horizontal eye openings at competitive power consumption.

Table 4.1 Performance summary and comparison

| | [24] | [28] | [31] | [32] | This work |
|---------------------------|------------------|-------|-----------------------|------------------|-----------|
| Architecture | CTLE & 1-tap DFE | CTLE | CTLE & 1-tap DFE | CTLE & 1-tap DFE | CTLE |
| Tech. | 65nm | 40nm | 45nm | 40nm | 28nm |
| Gb/s | 20 | 5-20 | 20 | 22 | 5-25 |
| Loss (dB) | 22 | 18.5 | 26.3 | 16 | 20 |
| Power (mW) | 37 | 25.2* | 13.2 | 19.2 | 17 |
| H @ BER=10 ⁻¹² | -- | -- | 26% @10 ⁻⁸ | 26% | 50% |
| H _{pk-pk} | 71.6% | 45.8% | -- | -- | 75% |
| FoM (mW/Gb/s) | 1.85 | 1.26 | 0.65 | 0.87 | 0.68 |

* including power for adaptation hardware

$$\text{FoM is defined by power efficiency: } FoM = \frac{\text{Power (mW)}}{\text{Data rate (Gb/s)}}$$

4.5 Conclusions

A continuous-time linear equalizer with a transversal architecture has been developed in the first part of the Ph.D. program. The equalizer transfer function features variable DC gain and two zeros, while the transversal architecture simplifies adaptation, allowing optimal tuning of the gain and zero frequency locations separately for improved equalization accuracy. Measurements on a 28nm CMOS test chip demonstrated >50% horizontal eye opening at 5-to-25Gb/s data rate, across channels with 20dB loss and with 17mW core power consumption.

Chapter 5 PAM-4 analog front-end for 64Gb/s transceiver in 28nm CMOS FDSOI

Abstract

A PAM-4 analog front-end for a transceiver operating up to 64Gb/s in 28nm CMOS FDSOI, tailored to short-reach electrical links is presented. The analog front-end includes variable-gain-amplifiers (VGAs), and flexible CTLE with low, mid and high frequency channel loss compensation. The VGA combines two different topologies that give high linearity and flat frequency response. The receiver equalization is based only on the flexible CTLE which proves a very accurate channel inversion through a transfer function that can be optimally adapted at low, mid and high frequency independently. The CTLE meets the performance requirements of CEI-56G-VSR without requiring DFE implementation. As a result, timing constraints for comparators in data and edge sampling paths may be relaxed by using track-and-hold stages, saving power consumption. The full transceiver (TX, RX and clock generation) operates from 16Gb/s to 64Gb/s in PAM-4 and 8Gb/s to 32Gb/s in NRZ. A TX-to-RX link at 64Gb/s, across a 16.8dB-loss channel reaches 10^{-12} minimum BER and 0.19UI horizontal eye opening at $BER=10^{-6}$, with 5.02mW/Gb/s power dissipation.

5.1 Introduction

The constant growth of digitally intensive services, such as the Internet of Things (IoT), multimedia on demand, cloud storage and cloud computing, is driving the continuous upgrade of telecommunication infrastructures and data-centers to support an exponential network traffic increase. New standards for electrical interconnects, addressing the need for higher communication speed, introduced PAM-4 in the migration path from 28Gb/s per lane to 56Gb/s and beyond (112Gb/s projects are currently in progress) [33].

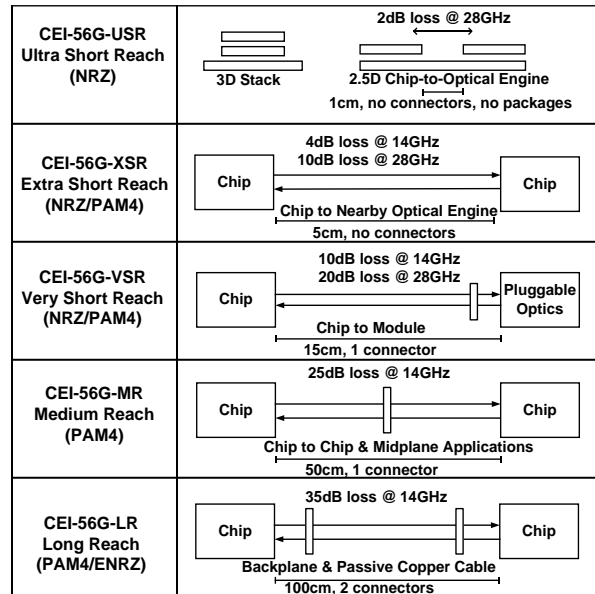


Figure 5.1 Application space of 56Gb/s links [33]

An intense industry effort is presently underway toward the development of complete 56Gb/s PAM-4 transceivers [7, 34-37] and building blocks at 112Gb/s are being investigated [38][39]. Compared to NRZ, each symbol in PAM-4 carries twice the information, thus limiting the spectral occupation theoretically to 50%. The more efficient use of the available link bandwidth, paired with a reduced clocking frequency and the continuous evolution of CMOS technologies, should enable links speed increase while limiting the overall systems costs and the power dissipation normalized to bit rate. But, compared to NRZ, the design of PAM-4 transceivers entails many new challenges and trade-offs. The intrinsic 1/3 eye amplitudes of PAM-4 leads to the SNR penalty, and transitions between non-adjacent levels with finite rise and fall times reduce the horizontal eye openings [40]. As a result, PAM-4 transmitters are required to deliver maximum signal swing with a very wide equivalent bandwidth [41-44]. In addition, the linearity of the transceiver building blocks is extremely critical to avoid distortion of the four PAM levels and preserve signal integrity. Also, the equalization becomes more demanding. In fact, the multilevel signal suffers from increased sensitivity to channel loss and reflections because the smallest transitions (i.e. between adjacent levels) are impaired by inter-symbol interference (ISI) generated by 3-times larger pk-to-pk transitions [45]. This corresponds to a 3-times larger impact of ISI, compared to NRZ, thus mandating much finer channel equalization before symbols detection. Finally, transceivers must

comply with legacy components, supporting a wide interval of data-rates and NRZ signaling at reduced speed, still maintaining power efficiency.

The application space envisioned for 56Gb/s electrical interfaces is depicted in Figure 5.1. Very different scenarios are considered, from ultra-short links between chips mounted within the same package, with negligible interconnect loss and reflections, up to long-reach links where the electrical interface must cope with up to 1mt-long channels (either backplane or cable) and the severe reflections generated by multiple packages and connectors. The harsh operating condition of long-reach links is driving the migration toward ADC-based receivers, where complex and flexible equalization and symbol detection are performed by digital signal processing (DSP) [46-48]. 56Gb/s PAM-4 receivers, implemented in state-of-the-art 16nm FinFet technology, demonstrated operation over 30-35dB channel loss at 14GHz Nyquist frequency, with a normalized power consumption (excluding the DSP power) in the range 4.4-6.6mW/Gb/s [7][36][37]. Considering the DSP power, the total RX power consumption reported in [37] is above 8mW/Gb/s. To improve the energy efficiency over links with reduced channel loss and reflections, e.g. in medium- or very-short-reach links for chip-to-chip or chip-to-module interconnects (Figure 5.1), power scalable ADC-based receivers have been proposed [36][37]. But for such applications, analog PAM-4 receivers may offer higher power and area saving [41][49]. A main limiting factor to the efficiency of analog receivers is the implementation of the decision feedback equalizer (DFE). PAM-4 requires hardware triplication and improved resolution, compared to NRZ, rising challenges to satisfy critical DFE feedback timing at low power also with advanced CMOS technology nodes [41].

In this chapter, a PAM-4 analog front-end for transceiver operating up to 64Gb/s is presented. The CTLE of the analog front-end features a transfer function optimally adapted at low, mid, and high frequency, allowing to meet the performance requirements of CEI-56G-VSR scenario with margin. Not requiring DFE, relaxed timing constraints allow implementing data, edge and eye monitor detection with track-and-hold stages, drastically reducing the power requirements. At 64Gb/s the full receiver requires 180mW from a single 1V supply, corresponding to 2.8mW/Gb/s only. The full transceiver operates from 16Gb/s to 64Gb/s in PAM-4 and from 8Gb/s to 32Gb/s in NRZ. A TX-to-RX link at 64Gb/s across a 16.8dB-loss channel proves 10^{-12} minimum BER and 0.19UI horizontal eye opening at BER= 10^{-6} , with 5.02mW/Gb/s power dissipation (comprising RX, TX and clocks generation).

This chapter is organized as follows. Section 5.2 presents the receiver architecture and building blocks are described in Section 5.3. Exhaustive experimental results are provided in Section 5.4, followed by the conclusions.

5.2 Analog front-end architecture

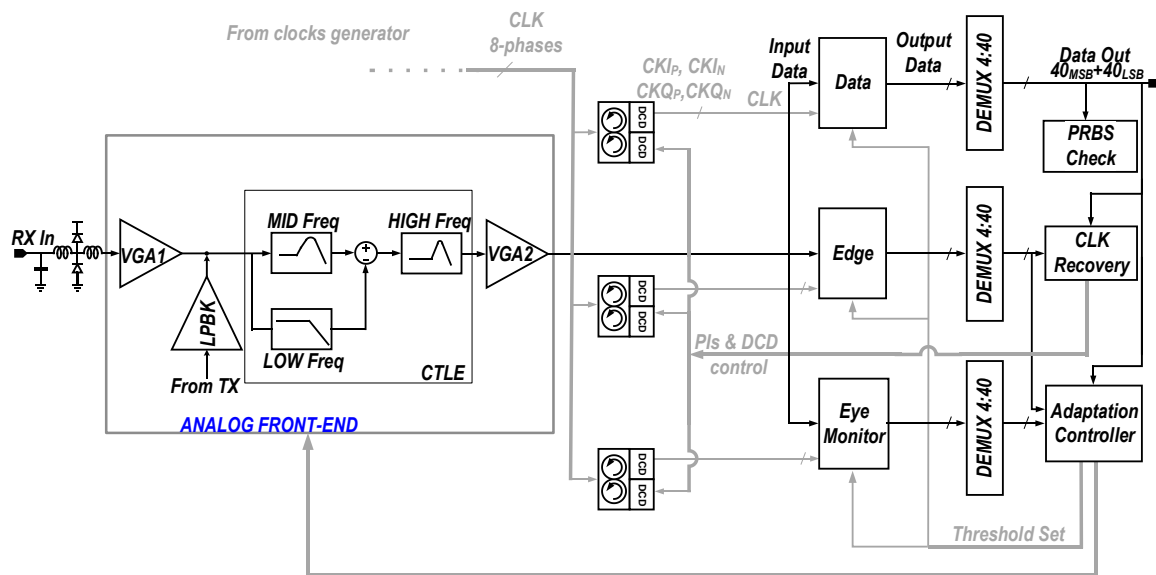


Figure 5.2 Receivers block diagram

The receiver architecture is shown in Figure 5.2. The receiver operates at quarter-rate, leveraging two differential clocks in quadrature. The analog front-end comprises an input T-coil peaking network, two variable gain amplifiers (VGA1 and VGA2) and a 2-stage continuous-time linear equalizer (CTLE) with low-frequency boost. The input network provides wide-band input impedance matching compensating pad, ESD protection, and input capacitance, and sets the correct common mode voltage for the analog front-end. VGA1 adjusts the signal swing to keep the CTLE in the linear range, while VGA2 is used for fine amplitude control at the samplers input. The output of the analog front-end feeds the RX sampling stage for data recovery and PAM4 to binary decoding. Three parallel sampling paths have been adopted for data, edge, and monitor respectively.

Since the receiver operates at quarter-rate, after data sampling, thermometer to binary decoders provide 4MSB+4LSB NRZ streams, further parallelized by 4:40 demultiplexers. Data path outputs are also used by the clock recovery unit, in combination with the outputs of the edge path, to set the optimal clock sampling phase. Early-late information for the second-order clock-recovery, driving the Phase Interpolators, is derived after demultiplexers, allowing selective removal of undesired PAM4 transitions in the digital domain. The undesired PAM4 transitions are from simultaneous LSB/MSB transitions. Those transitions have undesired timing distributions at the LSB comparator threshold [40]. Furthermore, data path outputs are used by the adaptation controller, in combination with measurements performed through the eye monitor path, to implement the digital calibration engine. Specifically, the integrated eye monitor builds PAM-4 signal statistics for adaptation of the samplers' thresholds, VGA gains, and CTLE frequency response. Finally, data path outputs are used by the integrated PRBS BER checker. Offsets in the analog front-end and in each comparator are calibrated with dedicated autozeroing routines at start-up.

Details of the most critical stages in the analog front-end, i.e. VGAs and CTLE, and of the sampling stages are provided in the next subsection.

5.3 Analog front-end circuits

5.3.1 Variable gain amplifiers

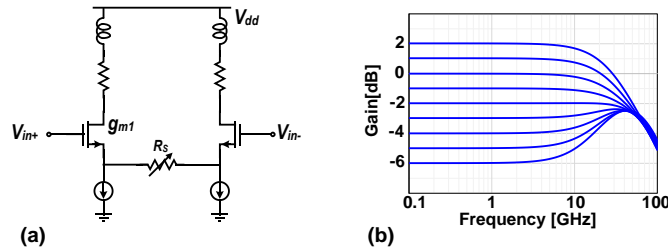


Figure 5.3 VGA realized with resistive source degeneration (a) and frequency response (b)

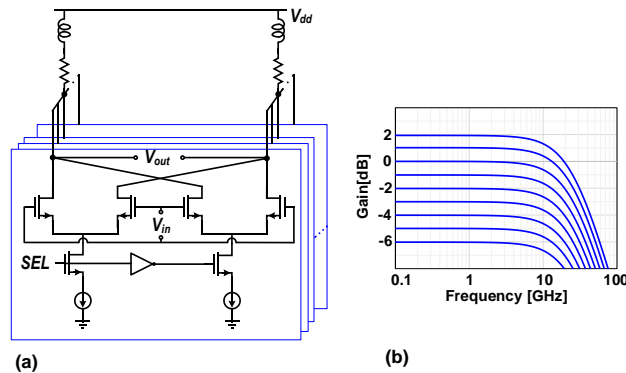


Figure 5.4 VGA based on cross-coupled differential pairs (a) and frequency response (b)

The most popular VGA circuit configuration, depicted in Figure 5.3a, consists of a differential pair with programmable resistive source degeneration [47][48]. Besides its simplicity, this circuit configuration has the advantage of low input capacitance and good linearity, particularly when the gain is decreased to accommodate a large input signal. However, at the minimum gain, the stray capacitance at source terminals of the two transistors introduces unwanted high frequency boost, given by $1+g_m R_s/2$ (being g_m the transistors transconductance and R_s the degeneration resistance). As a result, the circuit suffers from significant bandwidth and group-delay variation across the gain settings, as shown by the plot of the simulation in Figure 5.3b. Furthermore, achieving fine and linear gain control steps is difficult. The alternative VGA implementation in Figure 5.4a makes use of a thermometric array of differential pairs with cross-coupled outputs [50][51]. In each element of the array, only one of the two differential pairs is turned on,

according to the SEL control bit. Different gain values are then achieved by properly programming the bus of SEL controls. As proved by the simulations in Figure 5.4b, this solution overcomes the main limitations of the VGA in Figure 5.3a, yielding a flat frequency response with constant bandwidth and accurate gain control. However, such improvements are achieved at the expense of a poorer gain compression, reduced bandwidth due to higher input and output capacitance, and slightly increased power consumption.

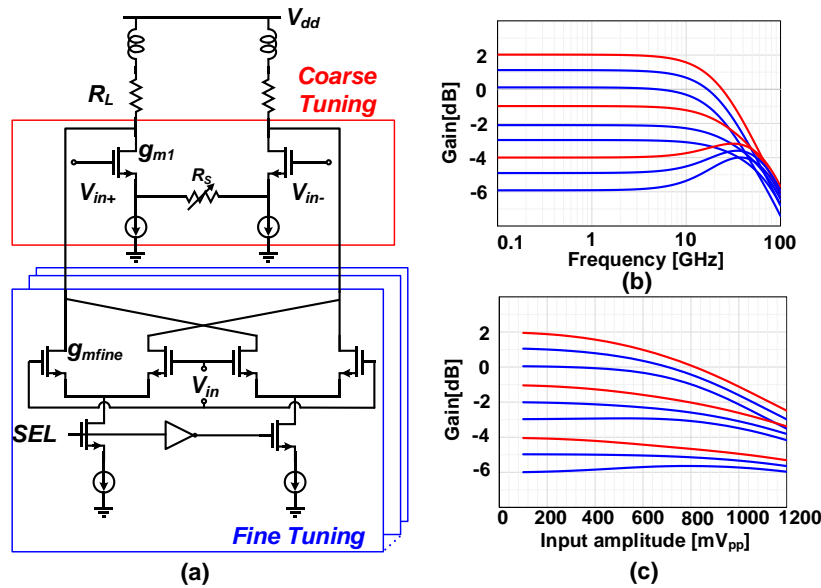


Figure 5.5 Circuit topology of the realized VGA (a), gain vs frequency (b), gain vs input amplitude (c)

The implemented VGAs combine the two above circuit topologies, as shown in Figure 5.5a, to exploit the respective advantages while mitigating the drawbacks. The differential pair with resistive degeneration provides a coarse gain control, while fine gain tuning is implemented using the thermometric array of cross-coupled differential pairs. The DC gain can be expressed: $G_{DC} = \left(\frac{g_{m1}}{1+g_{m1}R_S/2} + \sum g_{mfine} \right) R_L$. The frequency response is plotted in Figure 5.5b. Compared to a design based only on a resistively degenerated stage, the addition of the array of differential pairs in parallel reduces the required transconductance and degeneration resistance, limiting the unwanted high frequency peaking at the minimum gain setting from 3.8dB to 2dB. At the same time, the compression point improves when the gain is reduced, as shown by the simulations in Figure 5.5c, allowing to withstand a wide variation of input amplitude with negligible non-linear

distortion. The input 1dB-gain compression is 600mV_{pp} at the maximum gain of 2dB and it rises above 1.2V_{pp} when the gain is decreased to -6dB.

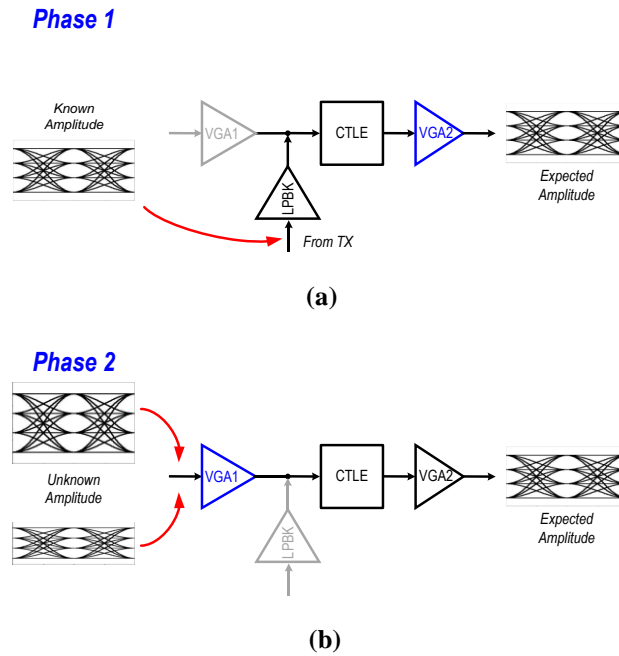


Figure 5.6 Gain calibration of VGA

The gain of the two VGAs is controlled with the approach shown in Figure 5.6. During initial calibrations, a signal with the optimal driving level for the CTLE is first generated by the TX, and injected through a loop-back path bypassing VGA1 (shown Figure 5.2). From eye monitor measurements, VGA2 is regulated to reach the desired amplitude at the input of the sampling stages. Then, VGA1 is calibrated in the actual operating condition, to restore the same amplitude at eye monitor input. Finally, during normal operation, VGA2 is jointly adapted with CTLE (the control variable in adaptation combines the gain of VGA2 and CTLE), compensating its gain variations across different settings of the transfer functions, while VGA1 maintains the optimal CTLE driving level independently from the actual RX input amplitude. The VGAs are designed with sufficient overlap between the coarse and fine gain settings. In this way, during normal operation, only the fine control code can be employed, avoiding potential issues arising from switching between the two different gain control techniques.

5.3.2 Continuous-time linear equalizer

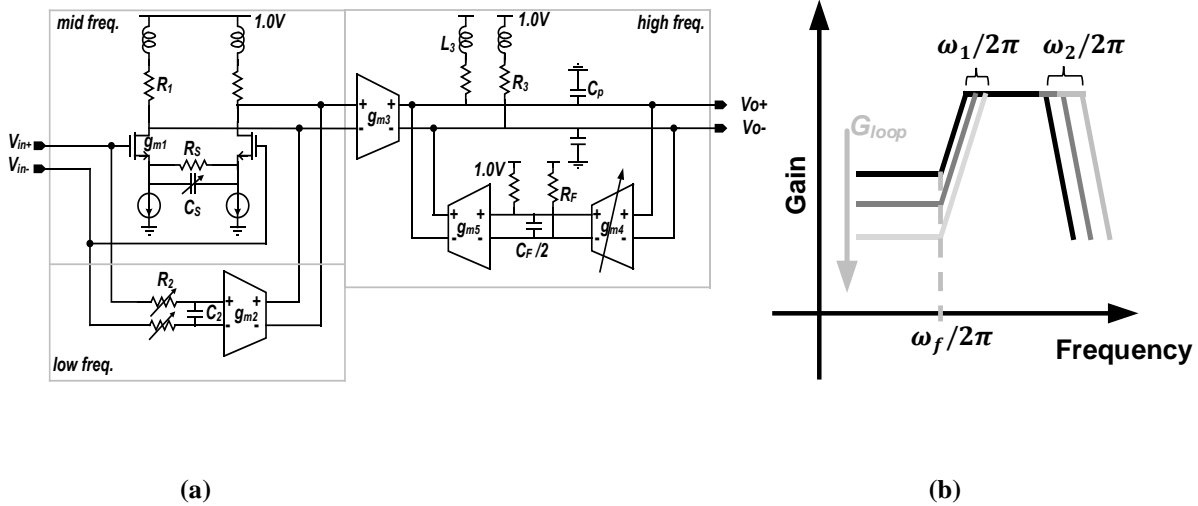


Figure 5.7 Circuit schematic of the continuous-time linear equalizer (a) and tuning of feedback equalizer (b)

The proposed CTLE consists of three stages, independently controlled, to match precisely the inverse of the channel response through a flexible shaping of the overall transfer function at low, mid and high frequency respectively.

The circuit schematic is drawn in Figure 5.7 (a). The RC-degenerated differential pair introduces a zero in the transfer function, shifted across frequency through the programmable degeneration capacitance C_s . Its purpose is to compensate the dielectric losses of the channel in the ~ 1 -10GHz frequency range by introducing up to 12dB peaking. The feed-forward path in the first stage, consisting of an RC network in series to a transconductance stage (R_2 - C_2 and g_{m2}), adds a mild ~ 1.5 -2dB peaking at low frequency, with a zero-pole pair that can be shifted from 0.2GHz to 1GHz by tuning R_2 . This stage refines the CTLE transfer function at low frequency, where the skin-effect loss determines a mild roll-off in the channel frequency response [19][20]. Both R_2 and C_s are tuned with an iterative algorithm, leveraging measurements performed by the eye monitor, to maximize the vertical and horizontal eye openings simultaneously. The iterative algorithm is heuristic based on sweeping all the combinations of R_2 and C_s .

The last stage of the CTLE, implemented with a feedback topology, introduces additional high-frequency boost (up to 6dB) to finely recover the steep roll-off of the channel profile close to Nyquist frequency. Neglecting the shunt peaking inductor L_3 , circuit analysis yields the following transfer function, from the input of g_{m3} to the output of the CTLE:

$$H_{HF}(\omega) = \frac{g_{m3}R_3}{1+G_{LOOP}} \frac{\left(1+j\frac{\omega}{\omega_f}\right)}{\left(1+j\frac{\omega}{\omega_1}\right)\left(1+j\frac{\omega}{\omega_2}\right)} \quad (5.1)$$

where $G_{LOOP}=g_{m5}R_3g_{m4}R_F$ is the static loop gain and $\omega_f=1/R_F C_F$. The two poles ω_1, ω_2 in equation (5.1) are given by:

$$\omega_{1,2} = \frac{\omega_f + \omega_p \pm \sqrt{\omega_f^2 + \omega_p^2 - 2\omega_f\omega_p(1+2G_{LOOP})}}{2} \quad (5.2)$$

with $\omega_p = 1/R_3 C_P$ the angular frequency of the parasitic pole at the output nodes of g_{m3} . To ensure stability with a wide margin, and to minimize distortion due to excessive group-delay variation, the stage is designed to operate with loop gain low enough such that, from (5.2), $\omega_{1,2}$ are real. In this condition, the dependence from G_{LOOP} of (5.2) can be linearly approximated, yielding:

$$\begin{aligned} \omega_1 &\approx \omega_f \left(1 + \frac{\omega_p}{\omega_p - \omega_f} G_{LOOP}\right) \\ \omega_2 &\approx \omega_p \left(1 + \frac{\omega_p}{\omega_p - \omega_f} G_{LOOP}\right) \end{aligned} \quad (5.3)$$

From (5.1) and (5.3), the peaking of the stage, i.e. $\max(|H_{HF}(\omega)|/|H_{HF}(\omega \rightarrow 0)|)$, is controlled by G_{LOOP} reducing the low-frequency gain and by pushing the two poles to higher frequency. Assuming that ω_p is sufficiently high, such that $\omega_2 \gg \omega_1$, $\max(|H_{HF}(\omega)|/|H_{HF}(\omega \rightarrow 0)|) = 1+G_{LOOP}$. The main advantage of the feedback topology is that the position of the zero in $H_{HF}(\omega)$ is constant. As a result, a very selective control of the CTLE transfer function can be achieved through G_{LOOP} at high frequency with negligible impact at low and mid-frequency, greatly simplifying the CTLE adaptation. The tuning of feedback equalizer is plotted in Figure 5.7 (b). The variation of low-frequency gain, leading to variation of the output eye amplitude, is compensated by VGA2 after the CTLE. Moreover, the feedback topology allows $H_{HF}(\omega)$ to be continuously adapted with a Least Mean Squares algorithm, during normal RX operation, by taking the CTLE output signal as gradient information and using the eye monitor for error slicing [30].

The equalization accuracy of the proposed CTLE is demonstrated through simulations considering an openly available reference channel for 56Gb/s short-reach links [52] in Figure 5.8. Simulations

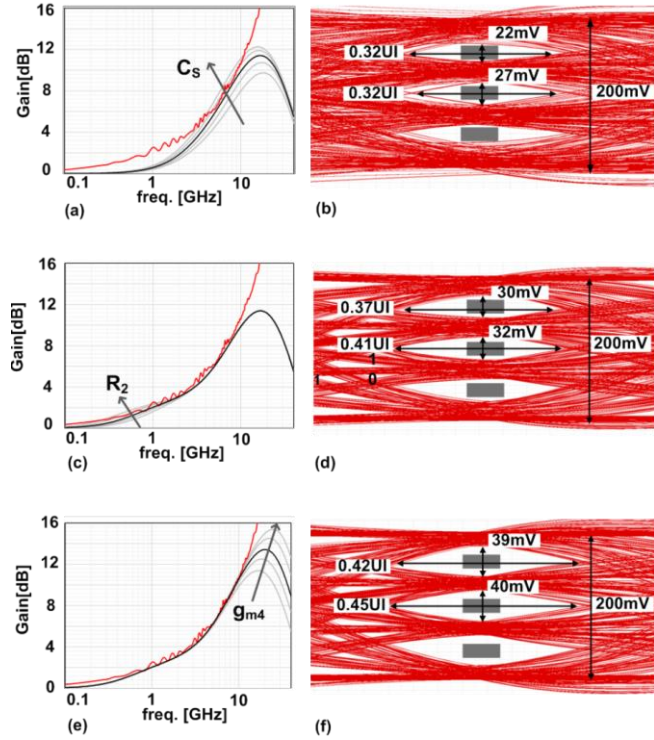


Figure 5.8 Frequency response and eye diagrams at different steps of the CTLE adaptation. Mid-frequency stage (a,b), low-frequency stage (c,d) and high-frequency stage (e,f)

follow the adaptation sequence implemented on the RX. First, the optimal CTLE response at mid frequency is found, by programming the degeneration capacitance C_s . The resulting transfer functions are reported in Figure 5.8a, together with the inverse of the channel response. The eye diagram corresponding to the optimal configuration is shown in Figure 5.8b. Then, the transfer function is tuned at low-frequency, by acting on R_2 . The corresponding CTLE transfer functions are reported in Figure 5.8c and the eye diagram after optimization in Figure 5.8d. Finally, the high frequency boost is adapted (Figure 5.8e), finely inverting the channel profile near Nyquist frequency. The resulting eye diagram is reported in Figure 5.8f. After completing the CTLE adaptation, the horizontal and vertical eye openings are 0.42UI and 39mV (over 200mV_{pp} eye amplitude). CEI-56G-PAM4 standard targets a raw BER of 10^{-6} , corresponding to $\sim 9.5\sigma$ for a gaussian distribution. The boxes in the middle of the eye diagrams in Figure 5.8 represent the sampling uncertainty due to the noise of the analog front-end ($\sigma_n \approx 2.4\text{mV}_{\text{rms}}$) and random jitter introduced by the clock-generation circuits ($\sigma_j \approx 290\text{fs}$). The RMS value of noise and random jitter

are estimated by integrating the power spectral density of noise (phase noise in clock-generation circuits) from simulation. The eye opening after CTLE adaptation (Figure 5.8f) meets the target BER with sufficient margin left to other transceiver impairments.

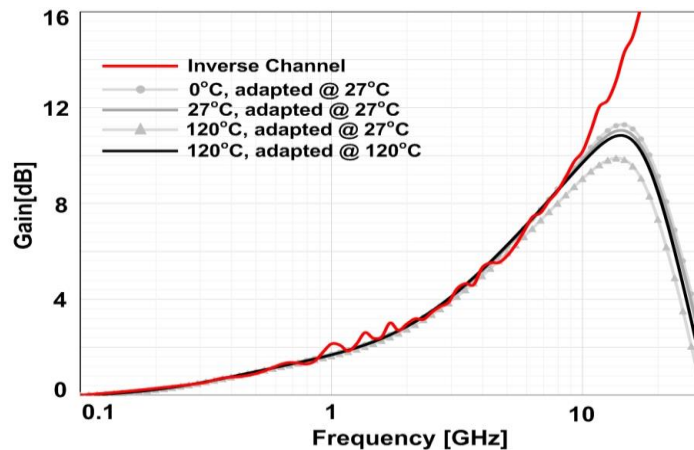


Figure 5.9 Temperature sensitivity of the CTLE transfer function.

Figure 5.9 shows the impact of temperature variations on the CTLE transfer function. After adaptation at room temperature, $T=27^\circ$, the CTLE maintains good channel inversion in the 0° - 120° range at low and mid frequency. The temperature increase has a remarkable impact only at high frequency, where the CTLE can be adapted in background with LMS, during normal operation. The black curve, matching closely the nominal transfer function at room temperature, represents the CTLE response when adaptation is performed at 120° .

5.4 Experimental results

The full photomicrograph of the fabricated test chip is shown in Figure 5.10, together with the breakdown of power consumption estimated from simulations. Several transceivers are stepped on the same die, interleaved by shared phase-locked loops (PLL) for clock generation.

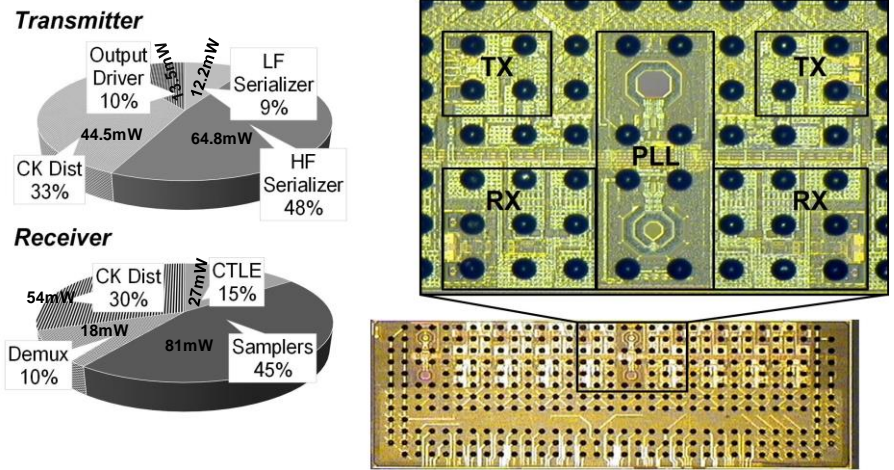
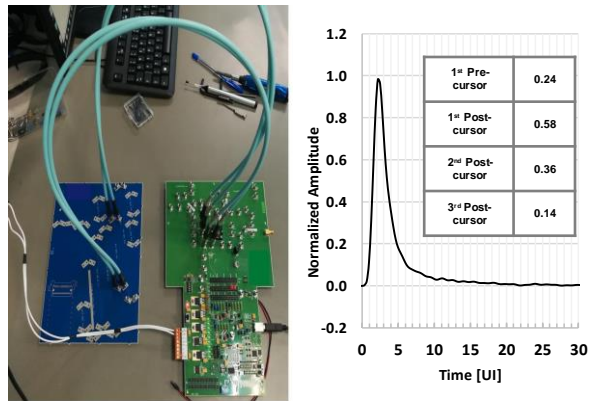


Figure 5.10 Chip photographs and breakdown of TX/RX power dissipation.

For testing, chips are assembled in standard BGA packages and mounted within a socket on PCB. Link tests have been performed by using TX and the RX with the experimental setup shown in Figure 5.11a. The TX-to-RX pulse response at 32Gb/s is shown in Figure 5.11b. The TX feeds a PCB channel of 10.6 cm length, test-board traces, connectors, and cables with a loss from BGA-to-BGA of 16.8dB at 16GHz. The TX FFE is statically configured for 2.8dB precursor pre-emphasis.



(a)

(b)

Figure 5.11 Experimental setup for the link tests (a) and TX-to-RX pulse response (b)

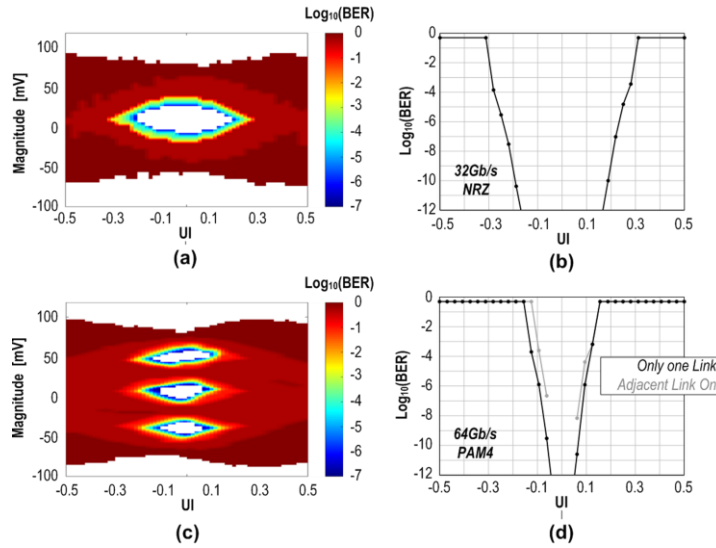


Figure 5.12 BER contour (a) and bathtub (b) at 32Gb/s NRZ. BER contour (c) and bathtub (d) at 64Gb/s PAM-4

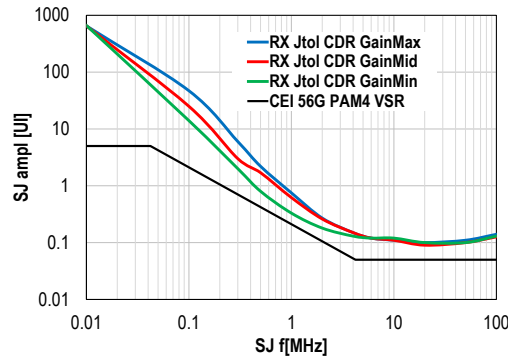


Figure 5.13 Jitter tolerance test at 64Gb/s PAM-4 @ BER=10⁻⁶

After running RX calibrations and adaptation, the signal quality at the samplers has been estimated through measurements performed with the on-chip RX eye monitor and BER checker. Figures 5.12a, and b shows the extracted BER contours and bathtub curves when a 32Gb/s NRZ signal is transmitted over the link. In this case, only the CTLE is employed for equalization at the RX side, and the horizontal eye opening at BER=10⁻¹² is 0.35UI. Figures 5.12c, and d plot the BER contours and the bathtub curve with PAM-4, at 64Gb/s. The horizontal opening at BER=10⁻⁶ is 0.19UI and the bathtub is still minimally open at BER=10⁻¹². The same measurements have been repeated with two adjacent transceivers operating simultaneously, to assess the robustness against crosstalk, mostly originated within the package. From the available package model, the estimated crosstalk

magnitude at RX input is 2.1mVpk-pk. The bathtub in Figure 5.12d proves a marginal penalty on the horizontal eye opening at BER=10⁻⁶.

Jitter tolerance tests have been performed feeding the RX with the signal generated by a laboratory PAM-4 pattern generator allowing to add sinusoidal Jitter of different amplitudes. The RX reference frequency is provided by a 100ppm crystal. The measured results, plotted in Figure 5.13, proves that the RX meets the CEI-56G-VSR mask with robustness against CDR loop gain variation. Finally, measurements are summarized and compared to PAM-4 receivers at similar data rate in Table 5.1. The performances of the presented receiver prove a remarkable improvement in power efficiency, compared to other implementations operating at comparable channel loss, despite realization in a less scaled technology node.

Table 5.1 Receiver summary and comparison.

| | [7] Frans, JSSC 2017 | [35] Im, JSSC 2017 | [37] Upadhyaya, ISSCC 2018 | | [36] Wang, ISSCC 2018 | | This work |
|--------------------------|--|--------------------------------|--|--------------------|--------------------------------|-------------------|------------------------|
| Technology | 16nm FinFet | 16nm FinFet | 16nm FinFet | | 16nm FinFet | | 28nm FDSOI- CMOS |
| Data Rate [Gb/s] | 56 | 56 | 56 | | 64 | | 64 |
| Link Loss [dB] | 31 | 10 | 32 | 7.5 | 29.5 | 8.6 | 16.8 |
| Equalization | TX-FFE, CTLE, 1-tap DFE, 24-tap FFE | TX-FFE, CTLE, 10-tap DFE | TX-FFE, CTLE, 1-tap DFE, 24-tap FFE | TX-FFE, CTLE | TX-FFE, CTLE, 16-tap FFE | TX-FFE, CTLE | TX-FFE, CTLE |
| Min. BER | ~10 ⁻⁸ | ~10 ⁻¹² | <10 ⁻¹² | <10 ⁻¹² | ~10 ⁻⁶ | ~10 ⁻⁴ | ~10 ⁻¹² |
| H @ BER=10 ⁻⁶ | 0.15 | 0.2 | 0.15 | 0.18 | N.A. | N.A. | 0.19 |
| Area [mm ²] | 14 (TX+RX) | 0.36 | 2.2(TX+RX) | | 0.163 | | 0.32 |
| Supply [V] | 0.9/1.2 | 0.9/1.2 | 0.85/0.9/1.2/1.8 | | 0.9/1.2 | | 1 |
| Power [mW] | 370* | 230 | 450 | 270 | 283.9* | 100* | 180 |
| FoM [mW/Gb/s] | 6.6* | 4.1 | 8 | 4.82 | 4.43* | 1.56* | 2.8 |

* DSP power not included

$$\text{FoM is defined by power efficiency: } FOM = \frac{\text{Power [mW]}}{\text{Data Rate [Gb/s]}}$$

5.5 Conclusions

A PAM-4 analog front-end together with the full receiver in 28nm FDSOI-CMOS supporting operation up to 64Gb/s has been presented. The merging of two different VGA topologies has allowed to reach good linearity and reduced unwanted peaking in frequency. A new CTLE circuit

topology, featuring high flexibility and accuracy to match the channel response has been proposed. The CTLE meets the equalization requirements of CEI-56G-VSR links with margin, allowing the implementation of a mostly-analog RX, without DFE, thus saving significant power consumption. At 64 Gb/s, a TX-to-RX link over 16.8dB-loss channel reaches 10^{-6} BER with a 0.19UI timing margin, requiring only 2.8mW/Gb/s for the full receiver.

Chapter 6 PAM-4 analog front-end for 112Gb/s receiver in 7nm FinFet

Abstract

The analog front-end for a PAM-4 receiver operating up to 112Gb/s in 7nm FinFet is presented in this chapter. It comprises a variable-gain-amplifier (VGA) and a flexible CTLE with low, mid and high frequency channel-loss compensation, followed by a buffer. Particular care was paid to design high linearity circuits, a key aspect to maintain PAM-4 signal integrity with the low supply voltage of 0.9V, constrained by the adopted technology. T-coil peaking and capacitance neutralization are exploited in CTLE to extend the operation frequency above 28GHz. The analog front-end can be used for short reach link or long reach link when merged with an ADC-based receiver back end. Simulations are performed with a reference channel (Synectic channel) featuring 15dB loss at Nyquist frequency. The results prove that this analog front-end can successfully support 112Gb/s PAM signaling.

6.1 Introduction

As presented in Chapter 1, the continuous growth of IP traffic pushes the development of serial link transceivers supporting higher speed. Recently, 100Gb/s per lane and 400Gb/s in four lanes physical layers are specified in IEEE 802.3ck Ethernet standards and 112Gb/s serial link transceivers are being investigated to double the data rate of 56Gb/s transceivers with improved power efficiency [53]. Digital circuits tremendously benefit from transistor scaling in 16nm or 7nm FinFet technology [54], such that the speed and power dissipation are improved while scaling the chip area. The development of transceivers combining analog circuits and digital systems may also take advantage of the higher performance of the digital circuits. However, the consolidated analog circuits developed in previous nodes, such as 28nm FD SOI, are not guaranteed to work properly with just scaling in 16nm/7nm FinFet technology due to significant changes in transistor behavior, new complex layout rules, and modeling techniques [55]. The analog design challenges in FinFet technology are also raised by lower operating voltages, severe impact of post-layout of small vias and fins, and a remarkable reduction of the allowed current density in the metal lines.

Thus, it is necessary to develop and optimize new analog circuits in FinFet technology. More complex broadband techniques should be introduced in analog circuits in order to meet the bandwidth demand at increasing speed. Moreover, the scaled supply voltage also impairs the linearity of the circuit, thus careful considerations should be taken into account to avoid large-signal distortion. The PAM-4 analog-front-end in this work is designed to be merged with an ADC-based receiver. Three are the main design targets: (1) providing $\sim 10\text{dB}$ boost at Nyquist frequency to relax the effective number of bits (ENOB) of the ADC [56], (2) driving the large input capacitance of shown by ADC, and (3) keep the output signal amplitude to be at the full-scale-range (FSR) of ADC. The goal of the full receiver is to recover 112Gb/s PAM-4 signals transmitted through a long reach channel. The ADC is currently under development, and the full transceiver can not be simulated at the time of writing. The simulations presented in this chapter comprise only the analog front-end and are performed on a test bench consisting of a PRBS31 worst-case signal generator, a Synectic channel [61] with 15dB loss at Nyquist frequency and the analog front-end followed by a capacitance modeling the ADC loading.

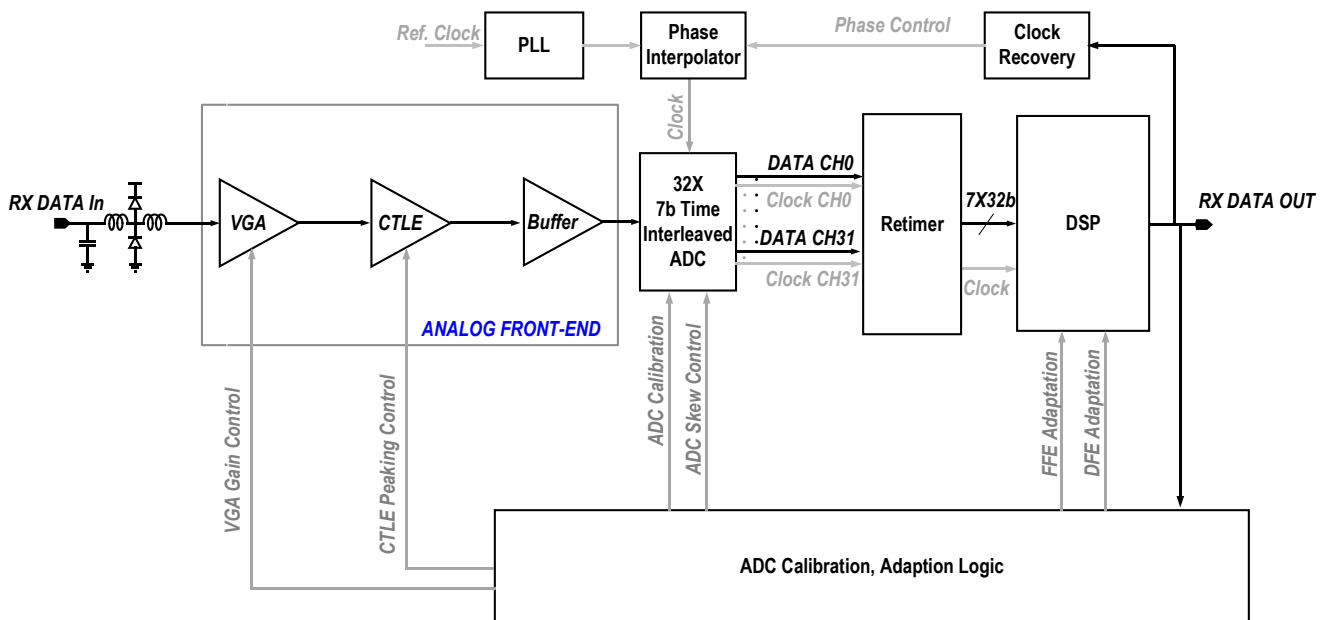


Figure 6.1 Architecture of the complete ADC based receiver

The architecture of the complete system is shown in Figure 6.1. The analog part of the receiver includes a T-coil input network, an analog front-end and a buffer. The T-Coil compensates the parasitic capacitance from the pad, ESD protection devices, and the input stage of the VGA. The analog front-end that includes a VGA, a CTLE and a buffer, provides power-efficient equalization and sets the input swing of the ADC match the FSR. The 7b 56-GS/s ADC is 32-way time-interleaved (TI) and it converts the differential analog input into digital signals. The ADC outputs are then retimed and sent to the DSP that includes FFE and DFE. The analog front-end architecture and circuits design are presented in section 6.2 and section 6.3 respectively, simulation results are summarized in section 6.4, and finally, conclusions and future work are presented in section 6.5.

6.2 Analog front-end architecture

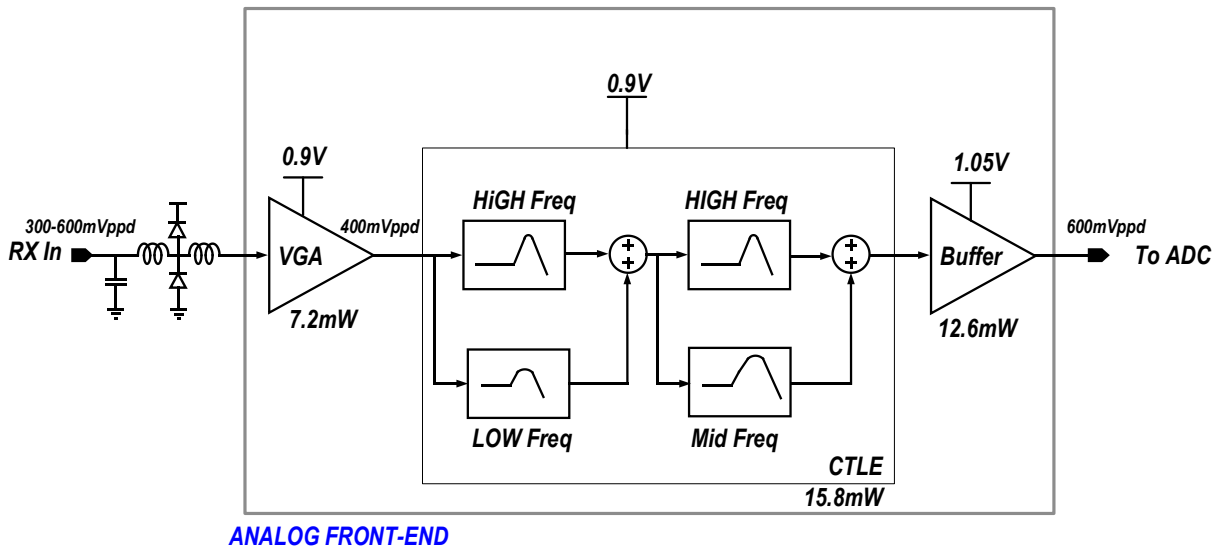


Figure 6.2 112Gb/s PAM-4 analog front-end architecture

The proposed analog front-end architecture is shown in Figure 6.2. Similar to the architecture in the previous chapter, it comprises an input T-coil peaking network, a variable gain amplifier, a 2-stage continuous-time linear equalizer (CTLE) that each consists of 2 paths, and a buffer. The VGA adjusts the input signals to guarantee that the CTLE works in its linear region. The CTLE

includes 2 stages high frequency equalizers that follow the slope of the inverse channel frequency response close to the Nyquist frequency, one low frequency equalizer corrects the long-tail effect, and one mid-frequency equalizer. The feedback architecture in the analog equalizer introduced in the previous chapter provides accurate tuning for channel inversion at high frequency. However, the main limitation of such architecture is that changing the feedback gain varies the DC gain of the equalizer and an accurate VGA has to be cascaded to keep a constant amplitude of the output signal. In this VGA, the fine gain control is achieved with Gilbert cells that suffer from large signal distortion due to the sense of resistive degeneration. In this analog-front-end, the 1-dB output compression point is very demanding, as it has to be larger than 1.25 times of the FSR of the ADC [56]. Therefore, the feedback analog equalizer followed by fine gain control VGAs is removed to alleviate circuits design challenges at a lower supply voltage. The VGA implemented in this front-end is a simple resistive degeneration differential pair. The total power consumption of this analog front-end is 35.6mW and the power of each block is shown in Figure 6.2.

6.3 CTLE circuits design for the analog-front-end

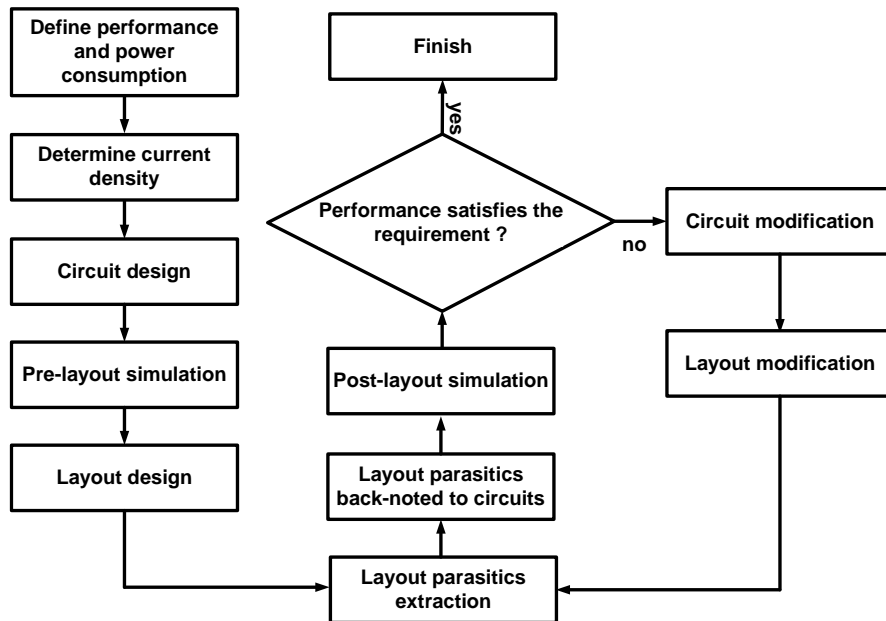


Figure 6.3 Circuit design flow-chart in 7nm FinFet technology

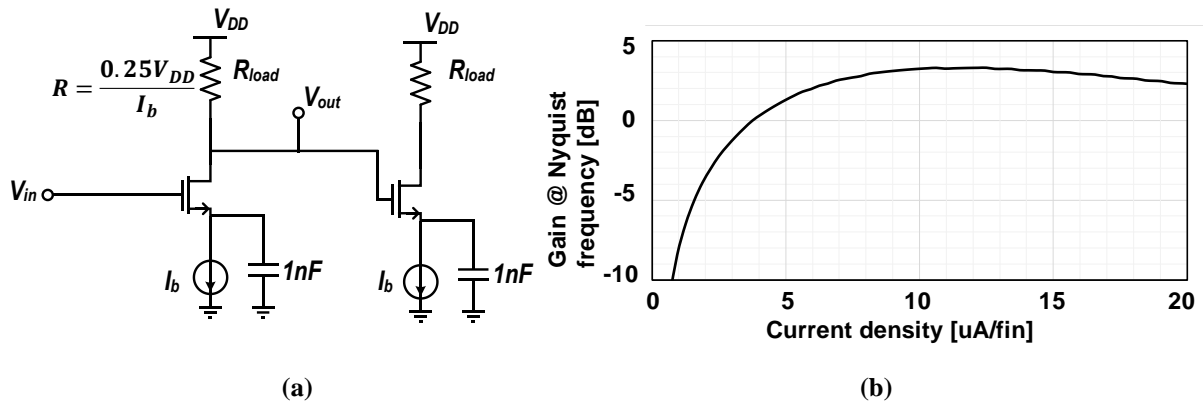


Figure 6.4 Current density test circuit (a) and gain at Nyquist frequency versus current density(b)

The flow-chart of circuit design in 7nm FinFet technology is shown in Figure 6.3. The performance requirements (gain, bandwidth, peaking, input/output swing, etc..) of the analog-front-end are defined by system simulations. The power consumption is defined by the total power consumption budget of the system. The current density is selected to maximize the boost at Nyquist frequency. The test circuit as shown in Figure 6.4 (a) to find the optimum current density consists of two single-stage amplifiers in which the dimension of the second stage amplifier depends on different load to the first stage, and the bias voltage of input and output are chosen to be $0.75V_{DD}$ to ensure the transistors operate at saturation region. As shown in Figure 6.4 (b), the current density is selected to maximize the voltage gain at Nyquist frequency. For the design of the circuit and layout, the harsh issue is to estimate the parasitics accurately. Typically, parasitic capacitors from interconnections and parasitic resistors from contacts in the layout are difficult to be estimated in pre-layout simulation. Thus, iterations to modify the layout and circuit are required until the performance is satisfied.

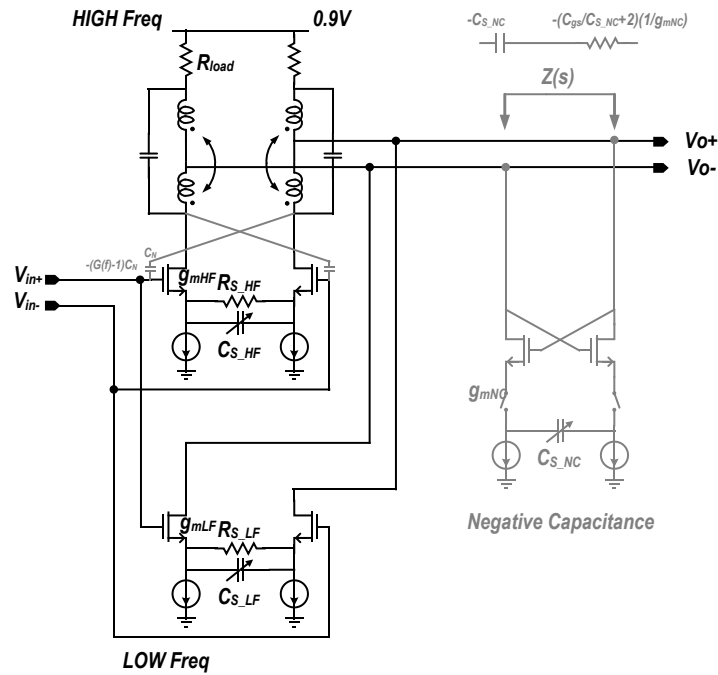


Figure 6.5 Schematic of proposed CTLE (first parts)

Figure 6.5 shows the first half part of the CTLE in Figure 6.2 which includes two differential degenerated differential pairs with a parallel RC impedance. Miller cancellation capacitance, peaking T-coils and a cross-coupled negative capacitance block are added for bandwidth extension. The second part of CTLE is similar to the first part, with the only difference that the resistance and capacitance used in low frequency equalizer are reduced to fit the shape of the channel at middle frequency. In 7nm FinFet technology, parasitics which result from fins and routings significantly limit the bandwidth of the circuit. In the pre-layout schematic design, shunt peaking is not enough efficient to extend the peaking frequency of equalizer. Therefore, T-coil peaking is incorporated in CTLE so as to provide a larger bandwidth extension factor [6]. In Figure 6.6, the performance achievable with a shunt peaking inductor and a T-coil network is compared. The value of the inductor is chosen to have a maximum flat magnitude of the load impedance. The high frequency peaking is introduced by the RC degeneration of the differential

pair. As the figure shows, T-Coil helps to extend peaking frequency from 20 GHz to 34 GHz. At schematic level design stage, this gives bandwidth margin for layout parasitics.

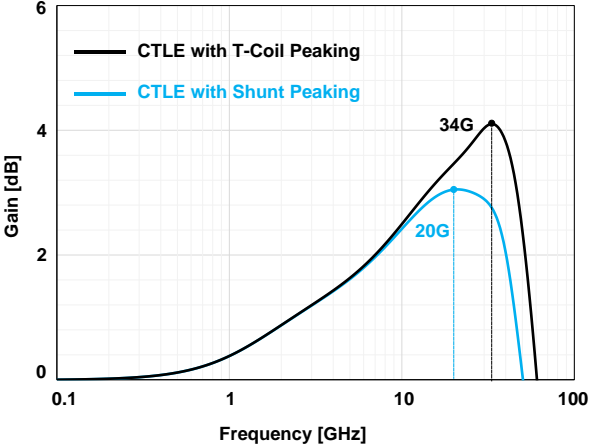


Figure 6.6 T-Coil peaking bandwidth extension

To further enhance the high frequency boost, negative capacitance is also introduced with the cross-coupled differential pair. As shown in Figure 6.5, the impedance can be approximated with a negative real part, $-(C_{gs}/C_{S_NC}+2)(1/g_{mNC})$, and a negative capacitance $-C_{SNC}$. The effect of the cross-coupled pair is shown In Figure 6.7. The negative capacitance provides extra boost at high frequency that enhances the equalization at Nyquist frequency.

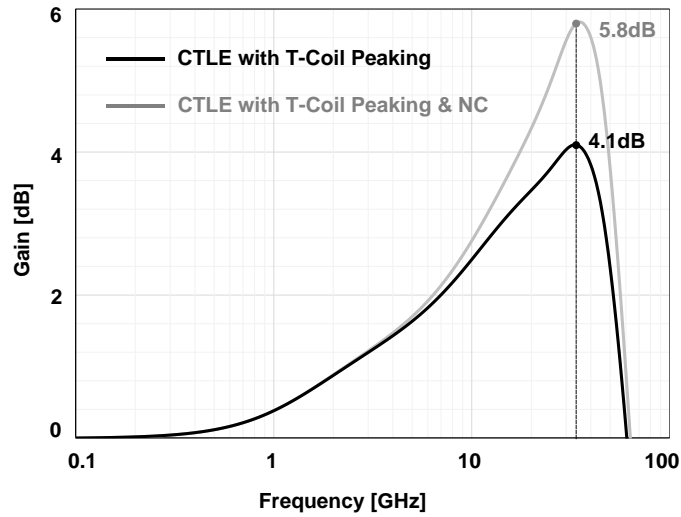


Figure 6.7 Negative capacitance peaking enhancement

6.4 Simulation results

The different transfer functions of CTLE are reported in Figure 6.8 and Figure 6.9 respectively. The plots prove the flexibility of CTLE for inverting different channel profiles. The negative capacitance provides extra peaking and design margins for additional parasitic capacitance that will be introduced by layout.

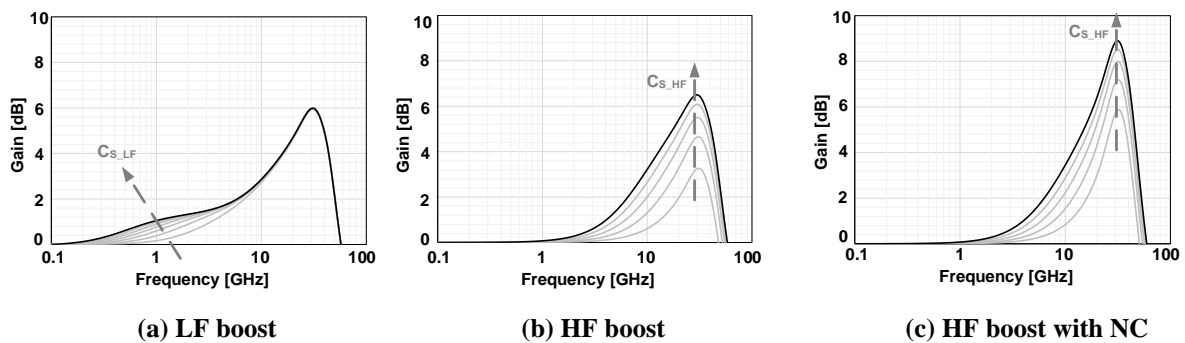


Figure 6.8 Transfer function of the of the first stage of the CTLE

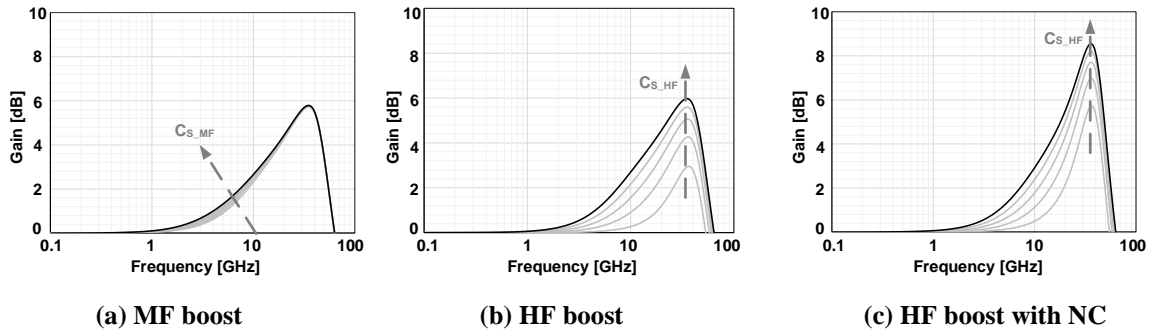


Figure 6.9 Transfer function the second stage of the CTLE

The large signal simulation of the complete analog-front-end is shown in Figure 6.10. The different plots show the low-frequency gain of the front-end, at different gain settings, with sinusoidal test signals. The 1dB compression point is larger than 1.25 times of the FSR of the ADC at all settings of VGA, which gives minimal impact on the BER of the full ADC based receiver [56]. The full scale of the ADC is expected to be 600mVppd

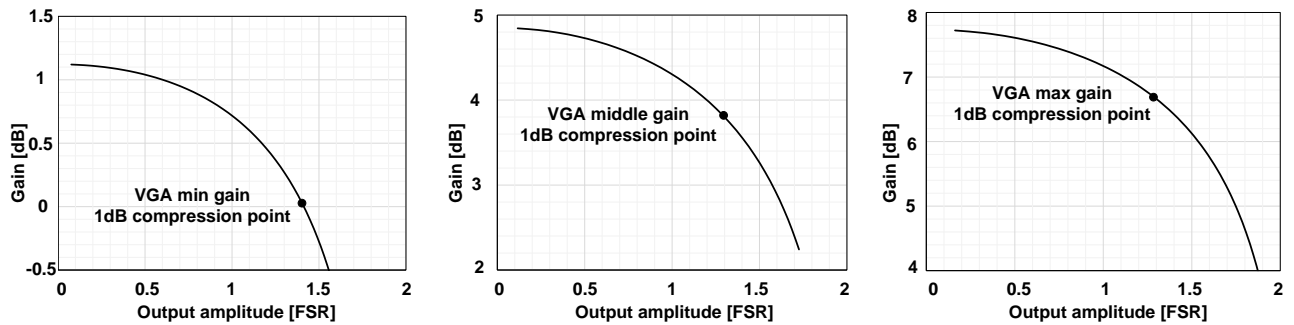


Figure 6.10 Large signal simulation of the complete analog-front-end

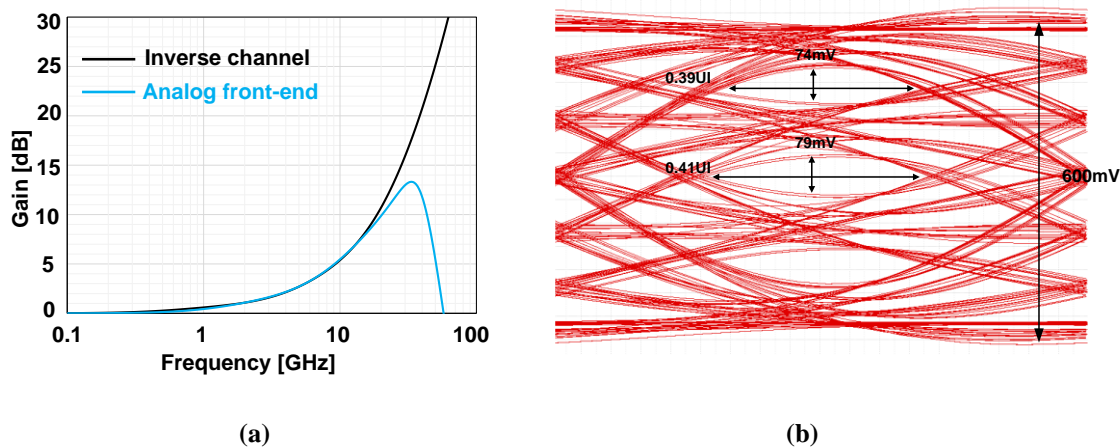


Figure 6.11 Simulated AC response (a) and eye diagram (b)

The equalizer is designed to compensate up to 15dB loss and tested with a Synectic channel model. The AC response and eye diagram of the channel followed by the front-end are shown in Figure 6.11. Simulation results prove the analog front-end works at 112Gb/s data rate with some bandwidth margin. The output signal amplitude is 600mVppd that satisfies the FSR demand of ADC.

6.5 Conclusions and future work

A PAM-4 analog front-end in 7nm FinFet designed to be merged with an ADC-based receiver, operating at 112Gb/s has been presented. A simple VGA circuit topology is used to limit the large signal distortion. In the CTLE, multiple broadband techniques are implemented to extend peaking frequency. Simulation results proved that the analog-front-end is able to work at 112Gb/s data rate with PRBS 31 worst-case sequences transmitted through a Synectic channel with 15dB loss at Nyquist frequency.

In the near future, layout design and further optimizations should be performed once layout parasitics are correctly estimated from post-layout simulations. In fact, issues may be raised from the layout parasitics, and some iterations between schematic and layout are expected to adjust the final frequency response of the front-end. As a further step, the full receiver comprising the front-

end connected to a behavioral model of the ADC has to be simulated to verify the overall performance.

Chapter 7 Conclusions and future work

7.1 Summary

Chapter 1 introduced backgrounds of serial link communications and high-speed serial link transceivers. The bandwidth demands of serial link communications, pushed by the continuous growth of global IP traffic, were introduced. The motivation to develop a low-power receiver with CTLEs was discussed.

Chapter 2 introduced the basic knowledge of serial link transceivers. Bandwidth efficiencies of NRZ and PAM-4 were compared, different kinds of channel impairments were summarized, and metrics to quantify the signal quality were presented.

Chapter 3 discussed analog equalization techniques. The evolution of CTLEs from a single stage to multiple stages with low frequency compensation was presented. In order to invert the channel transfer function accurately, the multiple stages CTLE with low frequency compensation showed its significant improvements. Multiple broadband techniques that are widely implemented in stage-of-the-art CTLEs are presented.

In Chapter 4, a very flexible CTLE with transversal architecture was presented. The equalizer transfer function features variable DC gain and two zeros, while the transversal architecture simplifies adaptation, allowing optimal tuning of the gain and zero frequency locations separately for improved equalization accuracy. The test chip was realized in 28nm CMOS FD-SOI. Measurement results demonstrated >50% horizontal eye opening at 5-to-25Gb/s data rate, across channels with 20dB loss and with 17mW core power consumption.

In Chapter 5, a PAM-4 analog front-end together with the full receiver in 28nm FDSOI-CMOS supporting operation up to 64Gb/s was presented. The merged VGA topology showed good performance in linearity and reduced unwanted peaking in frequency. A new CTLE circuit topology was proposed. The new CTLE features high flexibility and accuracy to match the channel response has been proposed. The CTLE meets the equalization requirements of CEI-56G-VSR links with margin, allowing the implementation of a mostly-analog RX, without DFE, thus saving significant power consumption. The measurement test was proved on TX-to-RX link over 16.8dB-loss channel. At 64Gb/s, the complete transceiver reached 10^{-6} BER with 0.19UI timing margin, requiring only 2.8mW/Gb/s for the full receiver.

In Chapter 6, a PAM-4 analog front-end in 7nm FinFet for an ADC based receiver operating up to 112Gb/s was presented. A simple VGA circuit topology was used in architecture to limit the large signal distortion. Multiple broadband techniques were also implemented to extend peaking frequency. Simulation results proved that the analog-front-end was able to work at 112Gb/s data rate with PRBS 31 worst-case sequences transmitted through a Synectic channel with 15dB loss at Nyquist frequency.

7.2 Future work

The demand for a higher speed serial link is unstoppable. The fast-growing cloud services are pushing the development of higher speed data centers [14]. The >100Gb/s serial links per lane for the next generation 800Gb Ethernet are currently exploited. For the 112Gb/s PAM-4 analog front-end in 7nm FinFet, optimizing the performance after post-layout extraction is the nearest target. Since there are many layout dependent effects that impact the bandwidth and linearity, some iterations between schematic and layout are expected to adjust the final response of the front-end. The physical layers of serial link transceivers are moving to advanced FinFet technology nodes. The transceivers with ADC-based receivers have shown its powerful performance [57] in long-reach channels (>30dB loss). However, the ADC is still a power-hungry component. For short-reach link (<20dB loss), a full-analog solution is also attractive to save power. In 16nm/7nm FinFet technology, analog designs are constrained by scaled supply voltage, parasitics of Fins and layout dependent effects. In order to realize a compact full-analog receiver, some new circuit topologies should be exploited. For example, replacing long-channel length transistors with stack of short-channel length transistors to make current tails saves area and reduces the parasitic resistance [55]. The very flexible CTLE with transverse architecture presented in Chapter 3 was not applied to 56Gb/s or 112Gb/s PAM-4 receivers. The reason is that the linearity of high-resolution VGAs impacts the PAM-4 system more than the NRZ system. To incorporate this CTLE architecture, it is rewarding to exploit new techniques to keep high linearity of VGAs.

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Appendix

List of publications:

- [1] **H. Zhang** ; E. Monaco ; M. Bassi ; A. Mazzanti “Five to 25Gb/s continuous time linear equaliser with transversal architecture” in *Electronics Letters*, Volume: 53, Issue: 25, Pages: 1629 – 1630, 2017.
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- [3] Emanuele Depaoli ; Enrico Monaco ; Giovanni Steffan ; Marco Mazzini ; **Hongyang Zhang** ; Walter Audoglio ; Oscar Belotti ; Augusto Andrea Rossi ; Guido Albasini ; Massimo Pozzoni ; Simone Erba ; Andrea Mazzanti, “A 4.9pJ/b 16-to-64Gb/s PAM-4 VSR transceiver in 28nm FDSOI CMOS” in *IEEE International Solid - State Circuits Conference (ISSCC)*, February 2018.
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