

UNIVERSITÀ DEGLI STUDI DI PAVIA

Facoltà di Ingegneria
Dipartimento di Ingegneria Industriale e dell'Informazione



UNIVERSITÀ
DI PAVIA

DOCTORAL THESIS IN MICROELECTRONICS
XXXII CICLO

**Design of Highly Linear and Low Power
Base-Band Filters for High Bandwidth
Current-Mode Receivers**

Supervisor:

Chiar.mo Prof. Rinaldo Castello

Coordinator:

Chiar.mo Prof. Guido Torelli

Author:

Mohammadmehdi DEILAM SALEHI

A thesis submitted in fulfillment of the requirements
for the degree of Doctor of Philosophy.

February 2020

Declaration of Authorship

I, Mohammadmehdi DEILAM SALEHI, declare that this thesis titled, “Design of Highly Linear and Low Power Base-Band Filters for High Bandwidth Current-Mode Receivers” and the work presented in it are my own. I conform that:

- This work was done wholly or mainly while in candidature for a research degree at this University.
- Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated.
- Where I have consulted the published work of others, this is always clearly attributed.
- Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work.
- I have acknowledged all main sources of help.
- Where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself.

Signed:

Date:

UNIVERSITÀ DEGLI STUDI DI PAVIA

Abstract

Facoltà di Ingegneria
Dipartimento di Ingegneria Industriale e dell'Informazione

**Design of Highly Linear and Low Power Base-Band Filters for High
Bandwidth Current-Mode Receivers**

by Mohammadmehdi DEILAM SALEHI

In recent years, lots of investments have been made on the telecommunication systems to develop their capabilities. Some brilliant ideas, like Smart cities and new technologies like Internet-Of-Things (IoT), opened many opportunities for the upcoming generation of wireless systems. Today, data transmission with the highest quality and security among a massive number of users is getting more feasible thanks to the high rate communication systems with higher bandwidth. Since the new wireless devices are surrounded by lots of unwanted signals as interferers, so the linearity of a wireless block can be one of the main challenges for new high bandwidth applications. This can get worse in a wireless receiver without off-chip filters, where the baseband filter after the mixer is the main filtering part. So the main challenge for the baseband part is designing high bandwidth filters with sufficient linearity. Two baseband filters are presented in this thesis, the first one which is the first-order Trans-Impedance Amplifier (TIA) filter in a current mode receiver is a 80 MHz bandwidth filter. The main challenge to design such a high bandwidth block is stability. Since the traditional compensation approaches like the Miller technique suffer the parasitic non-dominant pole effects, it is not possible to provide such a high bandwidth compensation. The main idea proposed here is using a parallel branch to add some zeros to the system in a high-frequency range and modify the phase behavior. Thanks to conditional stability coming from the compensation feedback branch, the TIA shows a huge open-loop gain that provides a noticeable input-referred IP3 (IIP3) more than +54 dBm with only 4.2 mw power consumption and $44 \mu V_{rms}$ integrated noise power at the input. The second design is a baseband filter with 200 MHz for 5G applications. The filter is a third-order filter consist of a second-order Rauch filter and first-order TIA filter. The receiver chain has a variable gain and bandwidth by less than 5 dB, noise figure. The measurement results show that the Rauch filter has an almost flat response (less than 1 dB fluctuation) in bandwidth and provides sufficient filtering to attenuate the blockers and reach to an output-referred IP3 (OIP3) more than +15 dBm. Both circuits design have been done in 28 nm TSMC technology.

Nomenclature

Abbreviations

IoT	Internet-Of-Things
TIA	Trans-Impedance Amplifier
OIP3	Output-referred IP3
IIP3	Input-referred IP3
MIMO	Multiple-In Multiple-Out
RX	Receiver side
TX	Transmitter side
OTA	Operational Transconductance Amplifier
DR	Dynamic range
SFDR	Spurious-free dynamic range
SNR	Signal to noise ratio
NF	Noise figure
OOB	Out-of-Band
IM	Intermodulation
IM3	Third-order intermodulation
LNTA	Low Noise Trans-conductance Amplifier
NTF	Noise transfer function
FFW	Feed-forward
LFB	Local feedback
f_u	Unity-gain bandwidth
BW	Bandwidth
GBW	Gain bandwidth product
PCB	Printed circuit board
PSD	Power spectral density
Q	Quality factor

Contents

Declaration of Authorship	ii
Abstact	iii
Contents	vi
List of figures	ix
List of tables	x
Introduction	1
1 Wireless Receiver Standards And Design Metrics	3
1.1 Receiver Architecture	3
1.2 Receiver Performance Metrics	4
1.2.1 Noise	4
1.2.2 Receiver Linearity	5
1.3 Cellular Network Generations	7
1.3.1 4G LTE	10
1.3.2 5G Generation	11
1.3.3 5G NR	13
1.4 Standard as a datasheet!	13
1.5 Conclusion	15
2 High Bandwidth TIA for Current-Mode Receiver	16
2.1 Current-Mode Receiver	16
2.2 Trans-Impedance Amplifier Overview	17
2.3 The Linearity Requirements Of A Saw-Less FDD Receiver	20
2.4 High Bandwidth OTA Design	21

2.4.1	Parallel-branch approach to compensate high band-width OTAs	22
2.4.2	Power-efficient high-bandwidth OTA with feed-forward compensation approach	24
2.4.3	Proposed structure: using local feedback (LFB) to compensate high frequency response	26
2.4.4	Circuit Level Design	27
2.4.5	G-Loop Analysis	30
2.4.6	Linearity Results	33
2.4.7	Measurement Results	36
2.4.8	Conclusion	40
3	High Bandwidth Base-band Filter for 5G Applications	41
3.1	Current-Mode Receiver for 5G application	41
3.2	Low-mode baseband filter structure	42
3.2.1	Filter loops stability	43
3.2.2	The receiver specifications	45
3.3	Second order filter design	47
3.3.1	Rauch filter properties	47
3.3.2	Second order filters comparison	50
3.4	Circuit level design	51
3.5	Measurements Results	55
3.6	New idea	60
3.7	Conclusion	62
	conclusion	64

List of Figures

1.1	Direct-conversion receiver block diagram	4
1.2	Acceptable input signal level: (a) dynamic range (b) spurious free dynamic range	5
1.3	1-dB gain compression plot	7
1.4	Third order nonlinear components product in desired signal bandwidth and IIP3 plot	8
1.5	Cellular network generations from 1G to 5G	9
1.6	Carrier Aggregation schemes	12
2.1	Current-mode receiver architecture.	17
2.2	TIA block diagram.	19
2.3	OTA's Noise model in TIA.	19
2.4	CW blocker and modulated TX leakage and the 3rd order intermodulation falling in the RX band.	21
2.5	Adding Zero compensation technique	22
2.6	Auxiliary parallel branches to add zeros in the different frequency range to the system, (a)three main stages in low frequency, (b)two stages in middle-frequency range, and (c) single stage in high frequency	23
2.7	Saving power by sharing the first stage between main and FFW path	24
2.8	Two different loops in system: (a) main loop which is dominant in low frequency, and (b) FFW loop which is dominant in frequencies close to unity gain bandwidth.	25
2.9	G-loop response: to improve the phase behavior, two G-loops should cross each other before the unity gain bandwidth	25
2.10	Gain loss and output clipping issue	25
2.11	LFB approach to enhance frequency response	26
2.12	Enhance bandwidth in proposed LFB approach in compared to FFW one at the same power consumption	26

2.13	Noise comparison between FFW and LFB approach, input-referred noise in LFB approach will increase because of the loading effect($Z_{FF-Load}$)	27
2.14	(a)P-N First stage (b)pole-zero doublets second stage	28
2.15	Push-pull output stage	29
2.16	high G_m stage	29
2.17	Decrease the noise injection by adding RC at the output of the high G_m stage in LFB approach and compare it with FFW approach	29
2.18	G-Loop analysis: (a) break the TIA's main loop (b) find poles and zeros position to assess the system stability	31
2.19	First and second stages' poles and zeros position	31
2.20	Last stage plus the feedback path with and without considering the Load effect of $Z_{FF-Load}$	32
2.21	The whole G-Loop response of the circuit, phase goes below zero degree in some frequency range	32
2.22	Nyquist plot diagram for conditional stable system	33
2.23	Post-Layout loop gain magnitude simulation on nominal corner, SS corner at +100 °C and FF corner at -50 °C	34
2.24	Montecarlo simulation of GBW and PM of the TIA loop gain	35
2.25	Simple non-linearity model of each stage of OTA	35
2.26	Input referred IIP3 of the TIA	36
2.27	TIA as a base-band filter in Current-mode receiver	37
2.28	TIA's (a)layout structure: vertical design to keep symmetry (b) chip photograph in 28 nm TSMC technology	37
2.29	TIA measurement setup	38
2.30	The frequency response of first order TIA filter	38
2.31	The output noise power of TIA	39
3.1	5G Current-mode receiver block diagram	42
3.2	LNTA structure	43
3.3	Third-order baseband filter: $2^{nd}Rauch + 1^{st}TIA$	43
3.4	The Rauch filter G-loop: (a) two main and FF loops (b): The main and FF G-loops' domination parts in frequency range	44
3.5	Filter G-loop response: (a)Rauch filter G-loop (b)TIA G-loop	45
3.6	The Rauch filter common-mode G-loop response	45
3.7	Receiver gain variation by filter's gain controlling	46
3.8	Receiver gain variation by front-end stages' gain controlling	46
3.9	Filter bandwidth variation	46
3.10	Rauch filter model	48
3.11	Differential input impedance of Rauch filter	49
3.12	Different components' noise contribution in Rauch filter	49
3.13	Open-loop model of Rauch filter	50

LIST OF FIGURES

3.14	Second order filters: (a) two real poles filter, (b)Two Thomas biquad filter	50
3.15	First stage circuit in Rauch and TIA filers	51
3.16	Middle stages in Rauch filter: (a) simple differential circuit (b) doublet pole and zero structure	52
3.17	Last stage structure: (a) parallel P-N circuit (b) common mode circuit	53
3.18	Folded cascode structure of feed-forward stage	53
3.19	Rauch filter's: (a)chip photograph (b) layout design structure . . .	55
3.20	Rauch filter:(a)PCB (b)measurement test bench	56
3.21	Rauch filter's low-gain mode	57
3.22	Rauch filter's high-gain mode	57
3.23	Rauch filter's output noise	58
3.24	Output inter-modulation tone amplitude by applying two tones at 180 and 190 MHz	58
3.25	Output inter-modulation tone amplitude by applying two tones at 300 and 430 MHz	59
3.26	IIP3 in terms of IM3 tone position	59
3.27	1dB gain compression plot	60
3.28	New structure to improve the noise behavior	61
3.29	Receiver chain gain variation	62
3.30	Receiver chain bandwidth variation	62

List of Tables

1.1	Telecommunication system development from 4G to 5G	12
1.2	5G band frequency division	14
2.1	Design parameters' value	30
2.2	TIA's parameters value	31
2.3	TIA's parameters value	37
2.4	TIA performance compared to other research works	39
3.1	Rauch filter's resistors and capacitors value	44
3.2	The whole receiver chain simulation results, NF and OIP3	47
3.3	Second order filters' performance comparison	51
3.4	Rauch filter's transistors size	54
3.5	TIA filter's components value	54
3.6	Components value on the PCB	55
3.7	Rauch filter performance compared to other research works	60
3.8	Design components value	61
3.9	Design components value	61

Introduction

Nowadays, wireless systems play a leading role in human communication. By increasing the number of users, many companies are planning to establish new standards and technologies to improve data transmission quality. Using multi-path transmission by multiple-In multiple-Out (MIMO) technology with some sophisticated modulation techniques in fifth generation of telecommunication system (5G) is a start point for the upcoming revolution in this industry. Thus, in the circuit level, the new wireless blocks should handle sufficiently high bandwidth to can provide a higher data rate. In a wireless receiver, the main question will be, how it can detect a weak signal surrounded by many other signals which play the interferers' role for the desired signal. In a traditional receiver, passive off-chip band-pass SAW filters were the typical approach to filter different standards' interferers. However, since external filters like SAW and Duplexer are expensive and occupy a large area compared to the rest of the device, they could not adapt to technology scaling. Hence, the main idea was SAW-Less receivers, which poses significant challenges to the receiver (RX) from the linearity point of view to tolerate un-filtered interferers. Since there is no filtering in the front-end part of the receiver, the main linearity challenge is related to the baseband filter after the mixer. In the current mode receiver structure, the baseband filter after the mixer is a trans-impedance amplifier (TIA), which is a first-order filter. Since increasing the new applications' bandwidth means less filtering for interferers closed to band edge, the linearity of baseband filter becomes the main design challenge. Moreover, since the new generation of the wireless system should be power efficient, power consumption is a critical design goal for high bandwidth devices. By considering all these concepts, the thesis is organized as follow

Chapter 1 explains the main metrics which are needed to asses any cellular system. By looking at the sensitivity and linearity constraints, the dynamic range of any system will be defined. After that, during a historical journey, different

network technologies from 1G to 5G will be discussed. The evolution route passes from simple analog 1G technology to much more complicated 5G that uses different technology like massive MIMO and millimeter wave, to expand the bandwidth and data rate.

Chapter 2 explains about the TIA as a baseband filter in a current mode receive. Traditionally there is a big capacitor at the input of the baseband filter to improve its linearity. For minimizing the occupied area and also improving noise behavior, the main solution is designing a high gain Operational transconductance amplifier (OTA) with sufficient bandwidth. The main issue for high gain and bandwidth OTA is how to make it stable? The traditional Miller approach is not adequate for high bandwidth applications because of the non-dominant poles effect and its large power consumption. The idea is using a parallel branch can add zeros in high-frequency range and make the circuit stable. The TIA made in this approach has 80 MHz bandwidth and consumes only 4.4 mw.

Chapter 3 explains another baseband filter with 200 MHz bandwidth for 5G applications. The filter makes third-order filtering by using a second-order Rauch filter plus first order stage. The gain and bandwidth of the filter can be controlled in a current mode receiver. The measurement results show Rauch filter has less than 1 dB fluctuation in bandwidth range with more than +15 dB for OIP3. With the same concept used in chapter 2, to compensate the system, a feed-forward branch is used to modify the phase behavior and guarantee stability.

Wireless Receiver Standards And Design Metrics

Communication systems establishment always faces lots of ups and downs to define practical standards that can provide a proper connection among a considerable number of users. In the past decades, lots of efforts have been made to extend standards' capabilities and develop communication circuit design to boost the transmission rate for multi-application goals. By looking at some required specifications for the communication system, this chapter provides a better insight into design metrics, especially for new generation of high bandwidth applications. Also, to see the new 5G standard capacity, a review of different generations' evolution will be presented.

1.1 Receiver Architecture

Heterodyne and direct-conversion receivers are the most commonly used architectures among many different receiver ones proposed in the last decades. However, simplicity and high level of integration of direct-conversion receivers make them the best choice for the new generation of SAW-less receivers [1,2]. Figure 1.1 shows the direct-conversion receiver block diagram. The signal received by the antenna contains the desired signal, adjacent channel, and in-band interference signals closed to wanted signal bandwidth. Since in some communication standards like LTE and WCDMA, which use frequency division duplexing (FDD) access technique, i.e., the transmitter (TX) and receiver (RX) operate together, the antenna is followed by a duplex filter to isolate RX side from TX one. Commercial duplexers provide an isolation of about 50dB [3,4] .

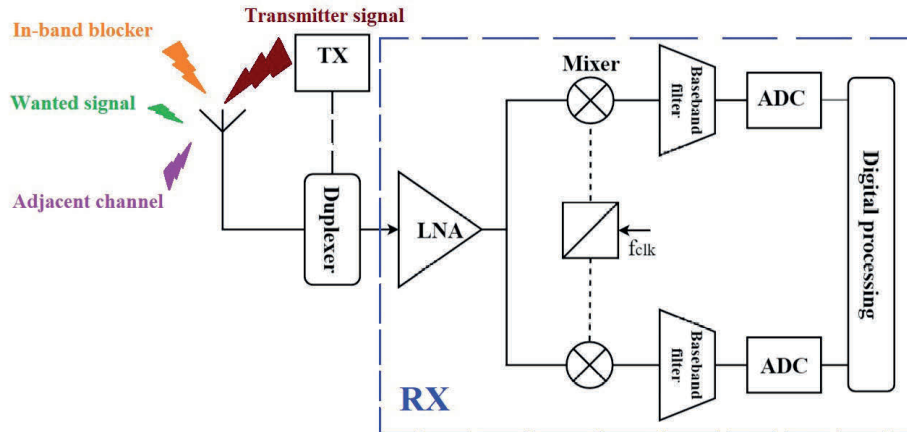


Figure 1.1: Direct-conversion receiver block diagram

1.2 Receiver Performance Metrics

In order to evaluate wireless receivers' performance, some metrics have to be defined. This section talks about the main parameters which are typically employed to characterize a wireless RX performance. The dynamic range is a figure of merit for receivers, which contains both noise and non-linear behavior effect of a cellular system. Dynamic range can be defined in different ways based on desired or interference signals. A simple definition of dynamic range (DR) refers to the maximum tolerable desired signal power divided by the minimum Sensible signal power. Based on this definition, while the minimum detectable signal is limited by the noise level, the compression defines the maximum signal amplitude, as shown in Figure 1.2a. In the second definition called the spurious-free dynamic range (SFDR), the upper bound which is limited by the Intermodulation (IM) products, is the maximum input level in a two-tones test in which the third-order IM products (IM3) do not exceed the integrated noise level of the receiver (Figure 1.2b).

1.2.1 Noise

Generally, noise in any electronic system can originate from three sources: thermal noise, shot noise and flicker noise. These small random fluctuations impose a lower bound for the minimum detectable desired signal, which is called sensitivity. In fact, this parameter determines the smallest value of input power that the receiver must be able to detect while ensuring sufficient signal to noise ratio (SNR) at the output of the system to guarantee proper demodulation of the signal [5]. Sensitivity

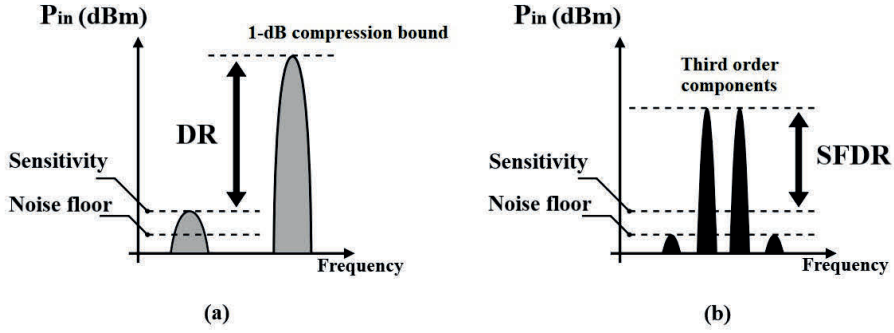


Figure 1.2: Acceptable input signal level: (a) dynamic range (b) spurious free dynamic range

can be expressed by the following equation

$$P_{\text{sensitivity}}^{(\text{dBm})} = P_{\text{Rs}}^{(\text{dBm/Hz})} + 10 \log_{10} (\text{BW})^{(\text{dB})} + \text{NF}^{(\text{dB})} + \text{SNR}_{\text{min,out}}^{(\text{dB})}, \quad (1.1)$$

where P_{Rs} is noise power spectral density of antenna, which should be calculated in desired bandwidth of BW, and SNR_{min} shows the minimum required signal to noise ratio at the output node to satisfy the modulation scheme requirements. NF expresses the noise figure of the receiver defined as the signal to noise ratio between input and output of the receiver chain

$$\text{NF}^{(\text{dB})} = 10 \log_{10} \left(\frac{\text{SNR}_{\text{in}}}{\text{SNR}_{\text{out}}} \right). \quad (1.2)$$

By modeling the emission of antenna as a source with 50Ω matched to the input of receiver, the noise power spectral density of source equals to $KT = -174\text{dBm/Hz}$, and hence the noise floor of system will be

$$\text{Noise}_{\text{floor}}^{(\text{dBm})} = -174^{(\text{dBm/Hz})} + 10 \log_{10} (\text{BW})^{(\text{dB})} + \text{NF}^{(\text{dB})}. \quad (1.3)$$

The noise floor is directly proportional to bandwidth. Thus, in the new generation of telecommunication systems with higher data rates and bandwidth, for a specific modulation scheme, the minimum detectable signal power will increase. By knowing the minimum SNR at the output of the receiver and acceptable sensitivity predefined by standard requirements, the maximum tolerable NF can be calculated by (1.1).

1.2.2 Receiver Linearity

Analog circuits under the small-signal approximation are typically considered as linear systems; however, any electronic circuit in reality shows a non-linear relation

between its input and output nodes, which can be approximated simply by the following equation

$$y(t) \approx a_1x(t) + a_2x(t)^2 + a_3x(t)^3, \quad (1.4)$$

where $x(t)$ and $y(t)$ are the input and output of the system, respectively. Thus, by considering the input signal as a single tone sinusoidal signal, $x(t) = A_0\cos(\omega_0t)$ and substituting in (1.4), we have

$$\begin{aligned} y(t) &\approx a_1A_0\cos(\omega_0t) + a_2A_0^2\cos^2(\omega_0t) + a_3A_0^3\cos^3(\omega_0t) \\ &= a_1A_0\cos(\omega_0t) + \frac{a_2A_0^2}{2}(1 + \cos(2\omega_0t)) + \frac{a_3A_0^3}{4}(3\cos(\omega_0t) + \cos(3\omega_0t)) \\ &= \frac{a_2A_0^2}{2} + \left(a_1A_0 + \frac{3a_3A_0^3}{4}\right)\cos(\omega_0t) + \frac{a_2A_0^2}{2}\cos(2\omega_0t) + \frac{a_3A_0^3}{4}\cos(3\omega_0t), \end{aligned} \quad (1.5)$$

where (1.5) shows the fundamental tone's gain, i.e., $a_1A_0 + \frac{3a_3A_0^3}{4}$ is related to the first and third components of signal approximation, which can significantly change when the amplitude of the input signal A_0 increases. Since in the MOS technology, the coefficients a_1 and a_3 have opposite sign, by increasing the input amplitude, the term associated with third-order distortion compresses the gain.

A typical metric to quantify the compression is 1dB-compression point, which corresponds to the input signal amplitude in which 1dB gain reduction occurs, as shown in Figure 1.3. The input-referred 1dB compression point is a metric to measure the large-signal performance of the receiver. Gain compression can result from a large desired signal, which can be controlled by gain reduction in the RX chain. On the other hand, If the gain compression comes from large blockers, more facilities like higher order baseband filter are required.

When there are two tones at the input node, for instance desired signal beside a strong unwanted signal (blocker), by putting $x(t) = A_0\cos(\omega_0t) + A_1\cos(\omega_1t)$ in (1.4), we find that

$$y(t) \approx \left(a_1 + \frac{3}{4}a_3A_0^2 + \frac{3}{2}a_3A_1^2\right)A_0\cos(\omega_0t) + \dots \quad (1.6)$$

The fundamental tone's gain can be dropped dramatically by a strong blocker, for instance, a large Out-of-Band (OOB) interferer.

The popular metric in wireless systems to assess the non-linearity is called input or output referred IP3 which is related to third-order inter-modulation tone's power(IM3). By considering two unwanted signals at the input, $x(t) =$

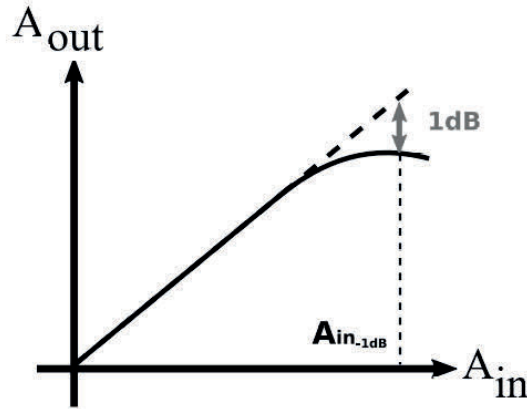


Figure 1.3: 1-dB gain compression plot

$A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t)$, (1.4) gives

$$\begin{aligned}
 y(t) \approx \dots + \frac{3a_3 A_1^2 A_2}{4} \cos(2\omega_1 + \omega_2) + \frac{3a_3 A_1^2 A_2}{4} \cos(2\omega_1 - \omega_2) \\
 + \frac{3a_3 A_1 A_2^2}{4} \cos(2\omega_2 + \omega_1) + \frac{3a_3 A_1 A_2^2}{4} \cos(2\omega_2 - \omega_1) + \dots,
 \end{aligned} \tag{1.7}$$

where $(2\omega_1 - \omega_2)$ and $(2\omega_2 - \omega_1)$ are third-order nonlinearity components called IM3 products. When those tones drop in desired signal bandwidth, by increasing the nonlinear distortion, they decrease the SNR of the system. By applying the same amplitude, A , for the desired signal and two unwanted tones as Figure 1.4 shows, in the certain amplitude of input signal A , which is called input-referred IP3 (or IIP3), the desired signal amplitude at the output node crosses the value of the IM3 products. In any wireless standard, there is a list of potential tests to assess the linearity of receivers. Each standard by defining the interferers amplitude and their position in terms of desired signal bandwidth gives a measure to the designer to determine proper specifications for system linearity.

1.3 Cellular Network Generations

Today, wireless networks are experiencing a noticeable step in their evolution. By looking at cellular networks advances during the past four decades, the number of users and applications increased dramatically. Lots of ideas and new technologies have been applied to speed up this evolution. This section presents a short review of the different generations of the cellular network from 1G to 5G. The

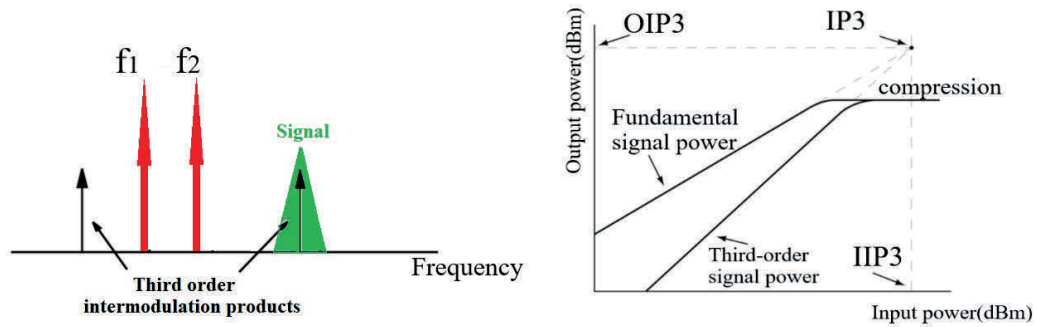


Figure 1.4: Third order nonlinear components product in desired signal bandwidth and IIP3 plot

main idea behind all the efforts and challenges of developing the wireless system comes from this question, how it is possible to increase the signal's data rate in a communication system efficiently?

Base on Shannon's theorem [6], the capacity of a telecommunication channel which shows the data rate is proportional to the bandwidth. Thus, the idea of boosting the data rate by increasing the signal bandwidth opened the new ideas to allocate, for instance, different channels from the same or different bands to a single user. It can be done according to the channel-aggregation approach or using advanced modulation schemes in Multiple-Input-Multiple-Output (MIMO) structure to improve the signal quality. Generally, a predefined frequency spectrum is allocated to a wireless system, but multiple access techniques provide the ability to share the available spectrum in an efficient way among users. For a wireless system, multiplexing can be done in different dimensions: Time (TDMA), frequency (FDMA and its variation OFDMA), and code (CDMA). Figure 1.5 shows a general deployment picture of different generations during the past decades.

The first generation(1G) of the cellular network was deployed in Japan during 1979, and it gained popularity in the US, UK, and Europe in the early 1980s. In 1981 many Scandinavian countries like Norway, Sweden, Denmark, Finland, Eastern Europe applied new standards known as NMT (Nordic Mobile Telephone), which were based on 1G technology. Similarly, AMPS (Advanced Mobile Phone System), which operated around the 850 MHz band providing 30-kHz-spaced channels, started to be established in North America and also TACS (Total Access Communications Systems) in UK [7]. 1G was based on analog technology, and because of limited frequency bandwidth and data transmission speed, it was only feasible for phone calls with low quality. The main features of 1G are listed below

- Frequency range from 800 MHz and 900 MHz

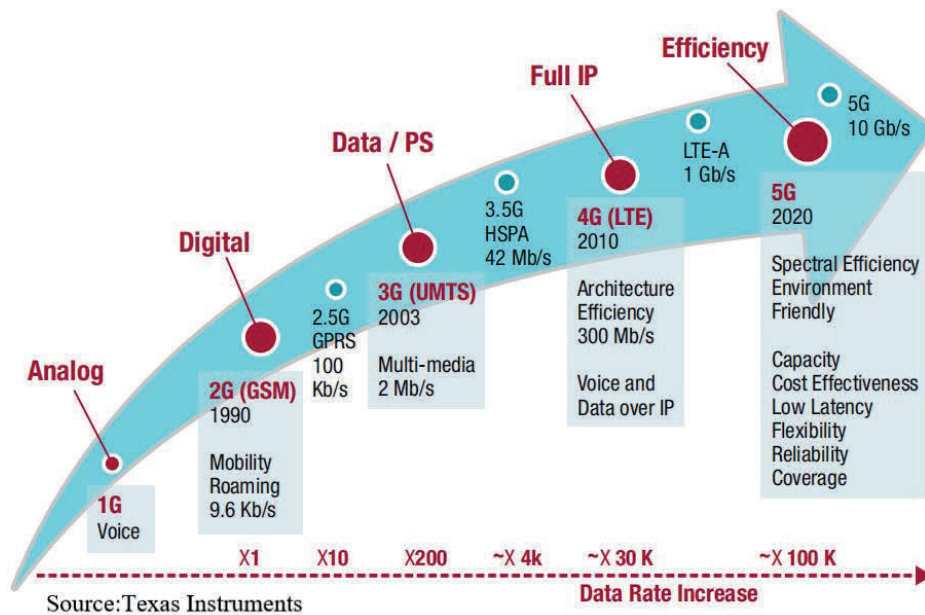


Figure 1.5: Cellular network generations from 1G to 5G

- Channels with a bandwidth of 30 kHz
- Modulation: Frequency Modulation (FM)
- Access technique: Frequency Division Multiple Access (FDMA)

However, its disadvantages are listed in the following

- Poor voice quality due to interference
- Poor battery life
- Less security (calls could be decoded easily)
- Limited cell coverage and users

The second-generation (2G) of wireless technology was established commercially first in Finland in 1991 by introducing digital technology for wireless transmission, also known as Global System for Mobile communication (GSM) [8]. 2G occupied the bandwidth of 30 to 200 kHz with 64 kbps maximum data rate, which is sufficient for data services like SMS and picture messages. In the mid-1990s, Qualcomm company, by introducing the Code-Division-Multiple-Access (CDMA), added more features than GSM to 2G in terms of spectral efficiency, number

of users, and data rate [9]. To support higher data rate, General-Packet-Radio-Service (GPRS) and Enhanced-Data-GSM-Evolution (EDGE) were introduced with the maximum data rate of 171 kbps and 473 kbps, respectively [10]. By summarising the 2G features, there will be

- Digital system
- Enhanced security
- Encrypted voice transmission
- Internet at a lower data rate

Although digitizing of telecommunication system gave us smaller devices, secure connection, and better call quality, it still suffers the limited number of users and low data rate. Thus, the new generation of cellular systems called 3G was pre-commercially launched in Japan.

The third-generation mobile communication started with the introduction of Universal-Mobile-Telecommunication-Systems (UMTS). UMTS, that employed wide-band CDMA (W-CDMA) with 5 MHz channel bandwidth, for the first time supported video calling on mobile devices. Smartphones became popular, and some applications were developed for them, which supported chat, email, games, web browsing, video streaming, and social media. In order to provide better quality and extend the new generations' applications, two technology: High-Speed-Downlink-Packet-Access (HSDPA) and High-Speed-Uplink-Packet-Access (HSUPA) were introduced in 3G which increased the data rate up to 2Mbps. Another advancement in the HSPA network is Evolved-High-Speed-Packet-Access (HSPA+), which can increase the transmission rates up to a peak speed of 42 Mbps uplink and 22 Mbps downlink theoretically using advanced encoding technique and multiple antennas to transmit and receive data requests [11].

1.3.1 4G LTE

The fourth-generation, which came around 2008, offers a higher data rate and handles more advanced multimedia services by introducing Long-Term-Evolution (LTE). The LTE was developed in following of UMTS and CDMA2000 systems and evolved later by releasing the LTE-Advanced (Release 10,11 and 12) and LTE-Advanced-Pro (Release 13 and 14) [12, 13]. The maximum speed of a 4G network for a mobile device and low mobility communication system is 100 Mbps and 1 Gbps, respectively. Complex modulation schemes and carrier aggregation are used to multiply uplink/downlink capacity and significantly improve data rate. By applying multi-path transmission to increase the data rate, LTE faced some issues;

for instance, while the data rate increases and the symbol package's time duration starts approaching the delay introduced by the channel, Inter-Symbol Interference (ISI) can occur which will degrade the signal quality. To address this issue, LTE uses Orthogonal Frequency-Division Multiplexing (OFDM) in which the high-rate data stream is converted to parallel and some streams with a lower data rate allowing to handle a larger delay. The new release of 4G can achieve a high data rate in combination with higher-order modulation up to 64 QAM and large bandwidth up to 20 MHz.

1.3.2 5G Generation

The fifth-generation goal is delivering ultra-fast internet and multimedia experience thanks to the advanced technologies. In order to achieve a higher data rate, it will use millimeter waves and unlicensed spectrum for data transmission. Some promising features which will be expected to see in 5G cellular system are listed below

- 1-10 Gbps connections
- Low latency in milliseconds (1 ms)
- 1000x bandwidth per unit area
- 10-100x number of users
- Higher security and reliability
- 90% reduction in network energy consumption
- Up to ten-year battery life for low power devices
- Uses technologies like small cells, beamforming to improve efficiency

Table 1.1 gives a better insight into the evolutionary role of 5G in telecommunication systems. 5G generation networks will be capable of supporting ten times more simultaneous connections than the 4G version.

A smart world such as smart cities and the most promising idea of IoT are some new concepts developing so fast along with 5G networks. In order to handle users' demands, the network must be efficient and cost-effective to support mobility, power efficiency, reliability, and security. Now, the question is how 5G can take this big step in telecommunication systems?

Actually, 5G technology will achieve its expected high efficiency using some modern and complex modulation techniques and some facilities like

Wireless System Generation		
Generation	4G	5G
Latency	10 ms	Less than 1 ms
Peak data rates	1 Gbps	10 Gbps
Number of mobile connections	8 billion (2016)	11 billion (2021)
Channel bandwidth Frequency band	20MHz 600MHz to 5.925 GHz	200MHz below 6GHz 600MHz–mmWave (for example, 28GHz, 39GHz, and onward to 80 GHz)

Table 1.1: Telecommunication system development from 4G to 5G

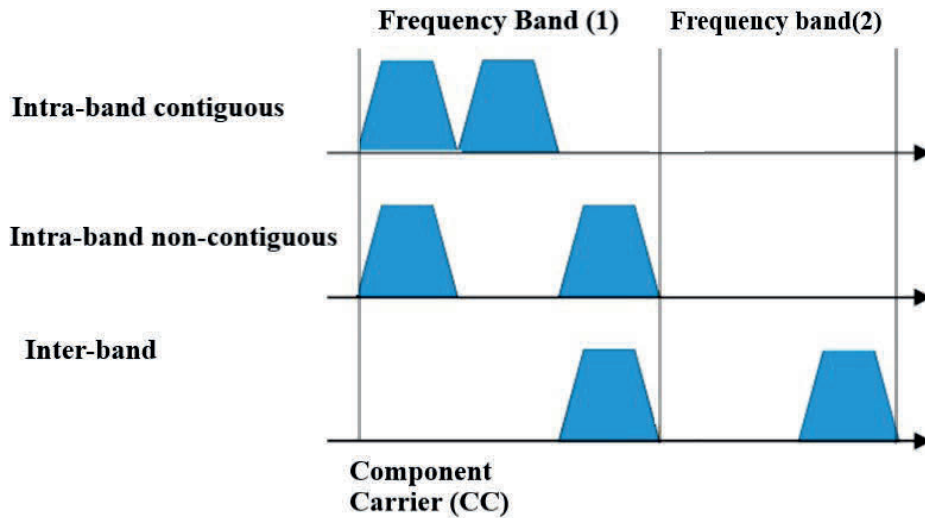


Figure 1.6: Carrier Aggregation schemes

Carrier Aggregation

Carrier aggregation (CA) is a technique used in LTE advanced to increase the signal bandwidth by grouping several carriers. The maximum number of allowed carriers is five, meaning that the maximum achievable bandwidth is 100 MHz. Aggregating can be done in different techniques as shown in Figure 1.6: intra-band contiguous in which two carriers are transmitted at neighboring channels in the same band, Intra-band non-contiguous with two carriers are in the same band but they are transmitted with channel spacing, and in Inter-band technique, different LTE bands are used for transmission simultaneously.

Small Cell Concept

In order to increase the efficiency of network, each cell can be divided into micro

1.4. Standard as a datasheet!

and pico cells. Spectrum re-usability allows to put more users in a small geographical area, and network can be used more efficiently.

Device to device communication

D2D communication is a technique that gives this ability to the network to let two adjacent devices communicate with each other directly. When the network is not accessible, one device can connect to another device.

MIMO Concept

Using multiple antennas in Base Station (BS) and User Equipment (UE), which is called the Multiple-Input Multiple-Output (MIMO) approach, increases the transmission rate in 5G applications. Transmitted signals in multi-path will be reflected from buildings, vehicles, and other stuff. The delay originated from these reflected signals will confuse the receiver side, and information could not be decoded correctly. In order to increase signal quality, multiple antennas are placed in different directions. Hence, to implement a MIMO technology, much complex signal processing is required at both transmitter and receiver sides.

1.3.3 5G NR

5G New-Radio is a new standard for ultra-fast 5G networks [14]. It will use the unlicensed spectrum below 6 GHz and above 6 GHz (millimeter range). Some of the proposed frequency range for 5G NR are: below 1 GHz bands like 600 MHz and 700 MHz for long-range transmission, 1GHz to 6 GHz unlicensed bands for higher bandwidth and millimeter wave spectrum above 24 GHz range. 5G NR system will offer a much faster and efficient network that can support billions of devices and technologies like the Internet of Things (IoT). Table 1.2 shows a proposed frequency band in the 5G cellular system in different countries [15].

1.4 Standard as a datasheet!

All standards define required specifications for a cellular system and introduce some techniques to measure them. This part presents a quick review of some measures to assess an RF receiver based on Texas Instrument notes [16]. For FDD systems, the transmitter power that leaks through the duplex filter in the RX side introduces extra distortion power which is

$$P_{\text{TXinRX}}(\text{dBm}) = P_{\text{TXnoise}}(\text{dBm/Hz}) + 10 \log_{10}(\text{BW}) - \text{ISO}_{\text{TXtoRX}}(\text{dB}), \quad (1.8)$$

where P_{TXnoise} is the power at the TX output in the RX band, $\text{ISO}_{\text{TXtoRX}}$ is the duplex filter rejection between TX and RX in the RX band, and BW is the bandwidth of the wanted signal.

5G Frequency Band		
Country/Region	Sub-6GHz spectrum	spectrum above 6GHz
USA	600MHz	27.5-28.35 GHz
	3100-3550 MHz	37-40 GHz
	3700-4200 MHz	64-71 GHz
UK	700 MHz (UK)	24.25-27.5 GHz
	2.3 GHz (UK)	
	3.4 GHz (UK)	
	694-790 MHz	
	3400-3800 MHz	
Japan	3600-4200 MHz	27.5-28.25 GHz
	4400-4900 MHz	
China	3300-3600 MHz	24.25-27.5 GHz
	4400-4500 MHz	37.25-43.5 GHz
	4800-4990 MHz	
India	3400-3600 MHz	24.5-29.5 GHz

Table 1.2: 5G band frequency division

When a large blocker is adjacent to the desired signal channel and has the same bandwidth, third-order intermodulation causes some of the blocker power leak into the wanted signal bandwidth that is called adjacent channel intermodulation. It can be estimated using the receiver chain's IIP3

$$P_{IM3}(\text{dBm}) = 3P_{\text{block}}(\text{dBm}) - 2\text{IIP3}(\text{dBm}), \quad (1.9)$$

where P_{block} is the RMS power of the blocker, and IIP3 is the cascaded IP3 at the antenna input. As aforementioned for FDD systems, the large TX signal leaks through the duplex filter into the RX. The intermodulation tone caused by blocker mixed with leakage from TX can drop in signal bandwidth, and hence its distortion power is equal to

$$\begin{aligned} & P_{\text{tx} \times \text{blk}}(\text{dBm}) \\ &= 3 \left(\frac{P_{\text{block}}(\text{dBm}) + P_{\text{TX}}(\text{dBm}) - \text{ISO}_{\text{TXtoRX}}(\text{dB})}{2} + \text{AF}(\text{dB}) \right) - 2\text{IIP3}(\text{dBm}), \end{aligned} \quad (1.10)$$

where P_{TX} is the TX output power in the BW of the wanted signal, and AF is the adjustment factor that is related to characteristics of the blocker.

Another important specification is the adjacent channel selectivity test, which is a measure of the receiver ability to receive a wanted signal in the presence of an adjacent blocker. The same concept for blockers measures the ability of the

receiver to detect a wanted signal in the presence of the blocker, which is not adjacent to the wanted signal. There are two different blockers test for in-band and out-of-band. For in-band blocker test, modulated blocker located inside the band plus a guard frequency range (usually 20 MHz on each side of the band for LTE). The modulated blocker is a LTE signal with the same bandwidth as the wanted signal up to 5 MHz, and a 5 MHz LTE signal for 10 and 20 MHz wanted signals bandwidth. The in-band blocker can be every where in the uplink band to a minimum distance of 1.5 times of the wanted signal bandwidth. The power level is either -43 dBm or -38 dBm, depending on the band. The out-of-band blocker is a CW tone located outside the uplink band plus the guard frequency range.

It is supposed also measure the phase noise of mixer, ADC dynamic range effect, and some other tests for 5G applications. All of them give a clear picture of the system capabilities and future developments.

1.5 Conclusion

Wireless systems have been experiencing lots of progress in recent years such as extending the bandwidth and lowering the power consumption. Providing sufficient linearity with lots of interferers in the new generation of wireless systems brings some new challenges for future designs. Hence, by introducing the new generation of cellular systems and an increasing number of users and higher transmission rate, it is expected to see the new ideas and structures can handle high bandwidth signals. Designing a high bandwidth baseband filter in a crowded new communication ambiance will face serious challenges, especially about linearity that will be discussed in the following chapters.

High Bandwidth TIA for Current-Mode Receiver

The receiver design has been dominated by using voltage-mode circuits for many years; however, the reduction of supply voltage by scaling down of the technology results in challenging issues regarding noise power, and gain compression at the receiver front-end. Large signal swings can easily generate non-linearity problems originating from signal clipping or large distortion. Moreover, the voltage-mode circuit requires high load impedance, which makes it challenging to use at high frequencies. To address all these obstacles, current-mode receivers were introduced. Low impedance nodes generate small-signal swings at both the input and output of each receiver block, and hence it is expected to have better linearity and a larger bandwidth in these structures. A Trans-Impedance Amplifier (TIA) is a base-band filter located after the passive mixer in the current-mode receiver to amplify a small in-band current to a large output voltage while attenuating the strong out-of-band current signal. The TIA structure is a closed-loop system composed of an Operational Trans-Conductance Amplifier (OTA) with a capacitive feedback load. In this chapter, a new approach is introduced to provide a stable OTA for high bandwidth applications. Simulation results show a high linear base-band filter with low power consumption.

2.1 Current-Mode Receiver

Figure 2.1 shows a saw-less current mode receiver. While traditionally, the LNA is supposed to be a voltage source, in current mode operation, it is called Low

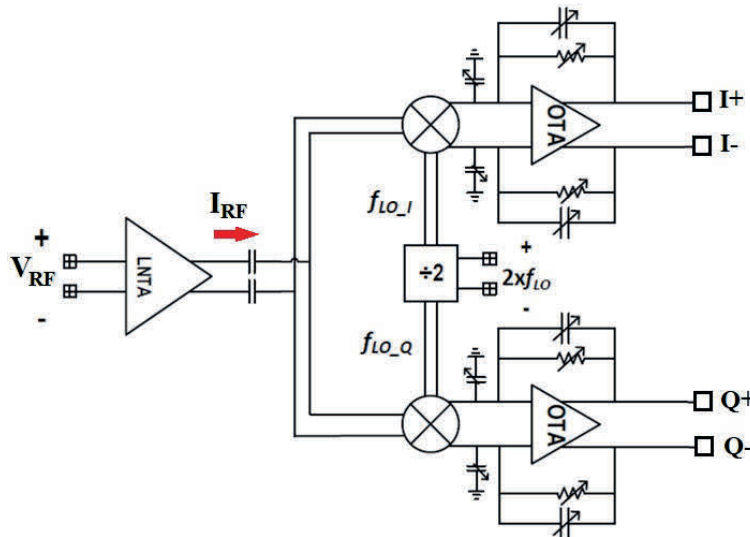


Figure 2.1: Current-mode receiver architecture.

Noise Trans-conductance Amplifier (LNTA), which converts input voltage signal to current at the output. The output current, which is down-converted to base-band using a passive mixer, is converted into voltage using TIA by doing first-order filtering on the signal. Since LNTA is the first block in the receiver chain, it is the most critical block in determining the noise contribution or sensitivity of the receiver, which all related to providing appropriate matching at its input to the duplexer. Passive mixers have gained much attention in recent years because of some characteristics that make them perfectly suitable for low-power solutions. Since they do not consume DC current, the flicker noise, which is a bottleneck for zero-IF structure, is noticeably negligible [17].

2.2 Trans-Impedance Amplifier Overview

As mentioned, for the current-mode receiver, the first block after the passive mixer is a TIA (first order filter) or a higher order filter [18–23]. TIA design aims to achieve a high gain in the desired signal bandwidth to suppress the noise coming from the following stages and provide a high out-of-band attenuation to reject large interferers. Being the first stage in base-band, TIA’s input impedance, noise, and linearity can limit the overall receiver chain performance. Low input impedance is necessary to keep the voltage swing sufficiently small at the output of the mixer and reduce the modulation on the mixer’s switch when large blockers appear. In high bandwidth applications because of the reduced loop gain of the OTA, close out-

of-band interference may easily saturate the OTA and increase the non-linearity distortions. Therefore, a TIA with high linearity and low input impedance over broadband is targeted. Ideally, the OTA has infinite gain and infinite bandwidth, meaning that the input impedance of the TIA, Z_{TIA} , is equal to zero (Figure 2.2), but in reality OTA has a finite gain and bandwidth, thus by considering $Z_f = R_f || 1/sC_f$ (which is the TIA's gain) and OTA as an one dominant-pole block, $A_v(s) = \frac{A_0}{1+s/\omega_p}$, the TIA's input impedance equals to

$$Z_{TIA} = \frac{Z_f}{1 + A_v(s)} = \frac{R_f \omega_{TIA} (s + \omega_p)}{s^2 + s(\omega_{TIA} + \omega_p(1 + A_0)) + \omega_{TIA} \omega_p(1 + A_0)}, \quad (2.1)$$

where $\omega_{TIA} = 1/R_f C_f$. Equation (2.1) shows that the limited gain-bandwidth product ($GBW = A_0 \omega_p$) increases Z_{TIA} and then non-linearity distortion at high frequency. For instance, the TIA filter in [24] with -3 dB bandwidth of 10 MHz provides 14 dB rejection at 50 MHz. If $R_f = 1k\Omega$, which means 60 dB transresistance gain in DC, with 1.8 v power supply and a rail-to-rail output, the maximum amplitude of interferer current signal without saturating the OTA at 50 MHz can be 9 mA.

To assess the linearity of mixer switches, as long as the drain-source voltage of a transistor remains far below the saturation voltage V_{DSAT} , the transistor is in the deep triode region and its on-resistance, R_{on} is very linear. For example, If the input impedance around 400 MHz is about 5 Ω , with a large 8 mA interferer at 400 MHz, the voltage swing at the input is 40 mV. For transistors in the strong inversion region, V_{DSAT} is generally more than 100 mV, and hence with 40 mv swing, the mixer still works linearly.

The conventional approach to bring down the input impedance and improve linearity is putting a big shunt capacitor C_{in} at the TIA virtual ground node, providing a low impedance path for high-frequency components, as shown in Figure 2.2. This capacitor must be big enough to provide sufficiently low impedance in the virtual node to bypass interferers and unwanted signals. It can be in the order of hundreds of pF [20,22]. In addition to increasing the chip area, such a big capacitor can also inject more noise to the TIA's output. By inserting input-referred OTA noise voltage in Figure 2.3, the noise transfer function (NTF) to the TIA output follows equation below

$$|NTF| = \left(1 + \frac{R_f}{R_{mix}}\right)^2 \left| \frac{1 + s(R_f || R_{mix})C_{in}}{1 + sR_f C_f} \right|^2, \quad (2.2)$$

where R_{mix} shows the mixer's output impedance.

Equation (2.2) shows a zero at $\omega_z = 1/C_{in}(R_f || R_{mix})$ which shifts to lower frequencies by increasing C_{in} . Thus, with a big capacitor, noise contribution starts to increase from lower frequencies. In the proposed design in this chapter, by

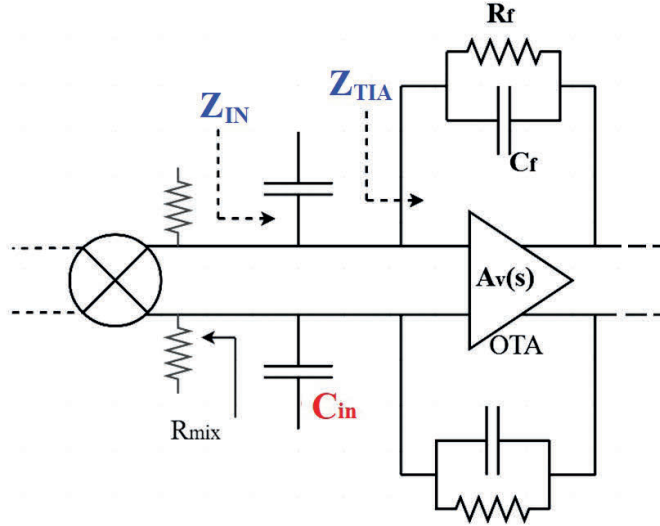


Figure 2.2: TIA block diagram.

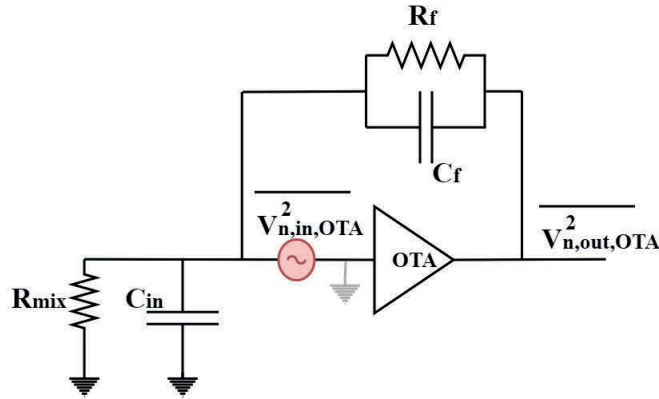


Figure 2.3: OTA's Noise model in TIA.

decreasing the capacitor value to 8 pF with $R_f = 2k\Omega$ and $R_{mix} = 500\Omega$, it is expected to see significant noise contribution close to the band edge. However, a big capacitor at the TIA input can serve several purposes [25]

1. It can bypass the clock harmonics in mixer's output. For instance $C_{in} = 8pF$ shows 5Ω at $2f_{LO}$ ($f_{LO}=2\text{ GHz}$) which is significantly smaller than the switches on-resistance R_{on} (typically about 20Ω);
2. As aforementioned, by lowering signal swing at the TIA's input, the linearity (IIP2 and IIP3) of mixer can improve even with strong OOB interferers [26]. Since $C_{in} = 8pF$ is 50Ω at 400 MHz, to ensure that the impedance after the mixer $Z_{in}=Z_i||1/sC_{in}$ remains low enough to the highest blocker frequency

(which will be at 400 MHz in LTE, FDD transceiver), an OTA with a high gain in blockers frequency is needed to lower the Z_{TIA} impedance and overall $Z_{\text{IN}} = \frac{1}{sC_{\text{in}}} || Z_{\text{TIA}}$.

3. And finally C_{in} improves TIA's out-of-band IIP3 by filtering the high-frequency down-converted interferers.

2.3 The Linearity Requirements Of A Saw-Less FDD Receiver

As mentioned before, in an FDD system, the leakage from the transmitter to the receiver input appears as a strong interference. In a wide-band receiver without SAW-filter and small isolation between TX and RX, the requirements on blocker tolerance will rise immensely. TX leakage mixes with an out of band blocker (close to the LO or a LO harmonics frequency) will fall in the desired receiver channel due to receiver non-linearity [27–29].

To have a better understanding of the linearity requirements, consider the LTE receiver in which the required minimum sensitivity is -94 dBm at 10 MHz bandwidth with a QPSK modulation scheme. It is needed to add 6 dB to the desired signal coming from the predefined blocking tests in LTE standard. Thus, with 1 dB for minimum SNR and wide-band intermodulation, the allowable noise power at the Rx input is -89 dBm. With the assumption that the 3rd-order intermodulation noise is 10 % of the acceptable noise floor, intermodulation is then computed

$$P_{\text{IMD},3} = -89 + 10 \log(0.1) = -99 \text{ dBm}. \quad (2.3)$$

IIP3 metric can then be extracted

$$\text{IIP3} = \frac{P_{\text{CW}} + 2(P_{\text{TX}} - \text{ISO}) - P_{\text{IMD},3}}{2}, \quad (2.4)$$

where P_{CW} is the amplitude of CW blocker, P_{TX} is the TX emission power, and ISO is the isolation between TX and RX.

Due to the standard's requirements for LTE-Advanced [30], a -15 dBm out-of-band CW blocker must be tolerated. Figure 2.4 shows a $P_{\text{CW}} = -15 \text{ dBm}$ and a modulated TX leakage $P_{\text{TX}} = +23 \text{ dBm}$ at predefined offset from RX signal based on standard. Using (2.4) and considering $\text{ISO} = +15 \text{ dB}$, the required IIP3 to satisfy a given $P_{\text{IMD},3}$ in (2.3) equals +50dBm, which is a noticeable IIP3 value in real wireless systems.

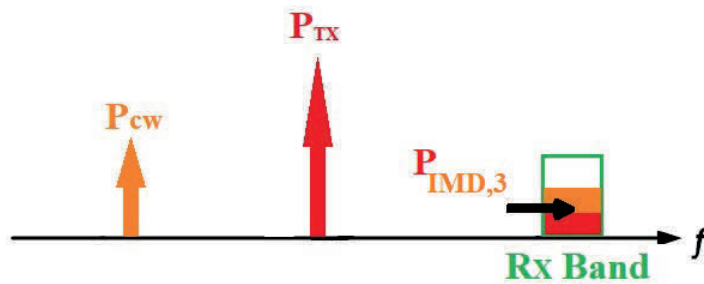


Figure 2.4: CW blocker and modulated TX leakage and the 3rd order intermodulation falling in the RX band.

2.4 High Bandwidth OTA Design

In the search for extending the TIA frequency range to use it as a filter in high bandwidth applications like 5G, the main question is that how it is possible to design a stable high bandwidth and gain OTA as a core of baseband filter? As mentioned, the conventional approach to improve the linearity of the mixer and TIA was putting a big capacitor, for example, 100 pF at the TIA's input which can limit the desired bandwidth dramatically. Thus, to extend bandwidth and improve the linearity of the circuit simultaneously, it is needed to propose a solution ensuring even by decreasing C_{in} , the voltage swing at the input of TIA remains small. An OTA with sufficiently high gain in desired bandwidth provides a low input impedance Z_{TIA} and compensates the big C_{in} value with keeping low the Z_{IN} (Figure 2.2) and then input swing voltage.

To design a high gain OTA in desired bandwidth, a multi-stage OTA is usually needed to boost the effective transconductance (G_m) of the OTA. Multi-stage OTAs with multiple poles in the transfer function (TF) increase the risk of instability in the system. The traditional approach to compensating a multi-stages amplifier is the Miller technique, which provides stability by bringing down the dominant pole and pushing non-dominant poles to a higher frequency. In this approach to extend bandwidth, very high G_m stages are needed, which increases the power consumption a lot.

Figure 2.5 shows another interesting approach introduced by [25], adding some zeroes to different nodes of the circuit to compensate the phase behavior and make the circuit stable. The TIA filter has 20 MHz bandwidth with 1.6 GHz unity-gain bandwidth. The system has two dominant poles introduced by big input capacitor, C_{in} , and the first stage's output pole around 20 MHz. The second stage is a high-bandwidth stage, which has a pole around unity-gain bandwidth. Hence, to compensate the dominant pole effects, two zeros were added to the system by

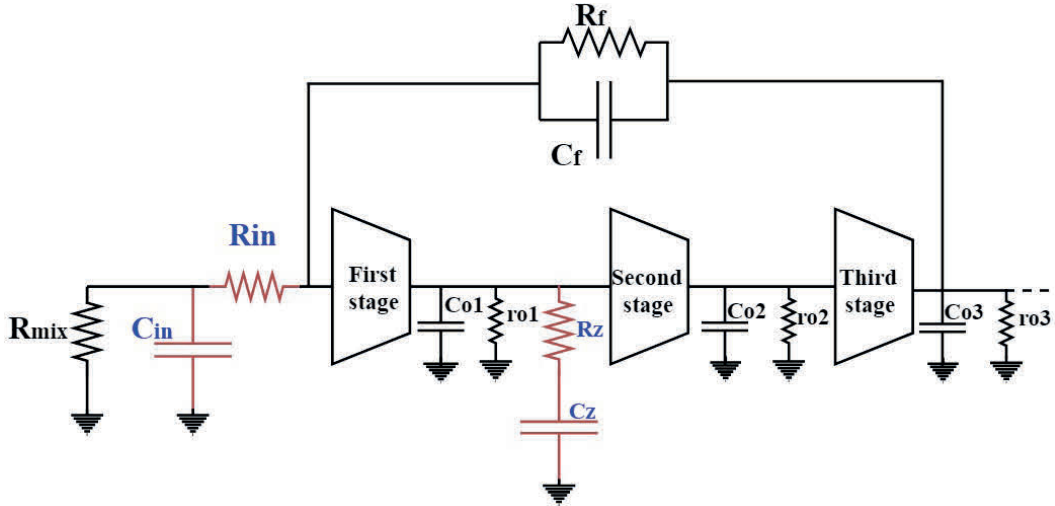


Figure 2.5: Adding Zero compensation technique

putting R_{in} in series with C_{in} at the TIA's input and $R_Z C_Z$ at the output of the first stage. These two zeros were located close to the unity-gain bandwidth. Hence, it is predictable that the phase shift decreases close to unity gain bandwidth and improves the phase margin of the system. Nevertheless, it is not possible to increase the bandwidth so much by using this approach. In higher frequencies, the non-dominant poles appear and constrain the phase behavior improvement. Hence, what can be done to extend bandwidth more?

2.4.1 Parallel-branch approach to compensate high bandwidth OTAs

In this part, the proposed architecture to extend an OTA's bandwidth will be presented. The challenge is how to add some zeroes to the system in frequencies close to unity gain bandwidth?

The idea is using the parallel auxiliary branches. Figure 2.6 shows an OTA with two parallel branches in feed-forward paths. In the low frequency (Figure 2.6a), only the main path conducts the signal. Thus, there are three stages with three active poles. By going to the middle-frequency range as shown in Figure 2.6b one feed-forward path will be active and bypasses two first stages in the main path. Hence, only two stages in this frequency range work actively, it is like one zero is added to the system.

Finally, in the Figure 2.6c at high frequency, the second auxiliary path bypasses all other branches. With only one active stage in frequencies close to unity gain bandwidth, there is only one active pole that can ensure the stability of the system.

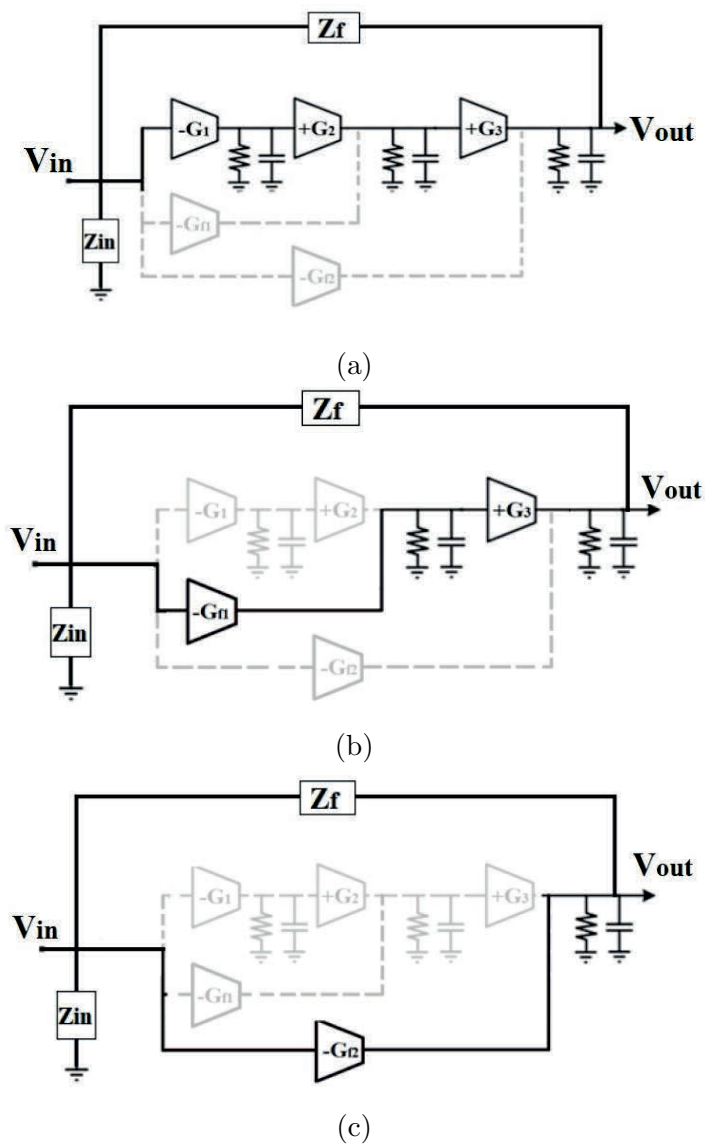


Figure 2.6: Auxiliary parallel branches to add zeros in the different frequency range to the system, (a)three main stages in low frequency, (b)two stages in middle-frequency range, and (c) single stage in high frequency

Thus, using parallel branches in high frequency is equal to adding zeros to the system to improve phase behavior. With several branches in parallel together, the power consumption of this structure is the main issue. Hence, the question now is how to design a power-efficient structure?

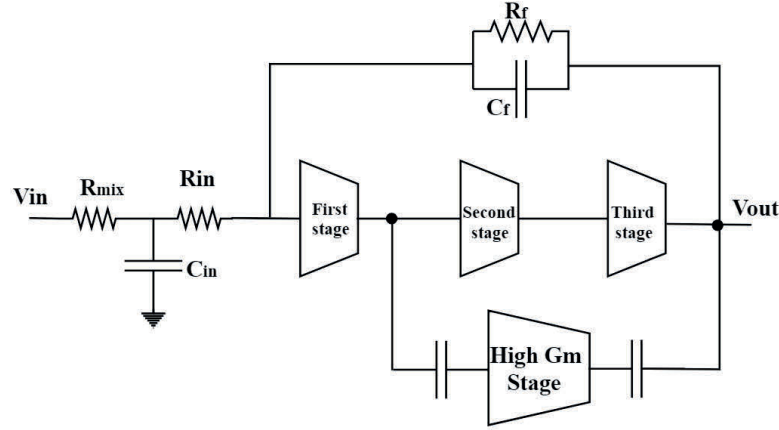


Figure 2.7: Saving power by sharing the first stage between main and FFW path

2.4.2 Power-efficient high-bandwidth OTA with feed-forward compensation approach

Figure 2.7 explains the idea to save power. The system has three stages in the main path and two stages in feed-forward (FFW). By sharing the first stage between the main path and FFW path, the FFW circuit's G_m is boosted instead of using only one power-hungry stage there. It has been done by putting ac coupling capacitors at the input and output of the high G_m stage, which makes it possible to separate dc bias of high G_m stage from others. Thus, not only the high G_m stage control the circuit behavior in higher frequency, its parallel structure can save the power efficiently.

As mentioned before, in the low frequency, the main path is active, and in the high frequency, the FFW one is dominant. Since the FFW path determines the unity-gain bandwidth of the system, a very large G_m is needed in this path. To analyze the stability of the system, different loops should be analyzed in the system. In the proposed circuit, there are two different loops: the main loop (Figure 2.8a) and the FFW loop, as shown in Figure 2.8b. As is evident in Figure 2.9, the FFW G-loop has a high-pass behavior, and in high frequency the whole G-loop response follows it. The main point is adding zero before unity-gain bandwidth (f_u). Thus, the crossing point (when two G-loops of main and FFW paths cross each other), which introduces the zero, should happen before f_u .

By considering the signal path in the FFW loop from V_t to V_F (Figure 2.10), it is obvious that the gain will be lost in the node 1 and 2 because of capacitive division. Thus, it means that to extend the bandwidth; additional power has to be burnt in high- G_m stage to have more G_m and then f_u . Moreover, since the high- G_m stage is a three-stacked P-N structure and its output is connected to the

2.4. High Bandwidth OTA Design

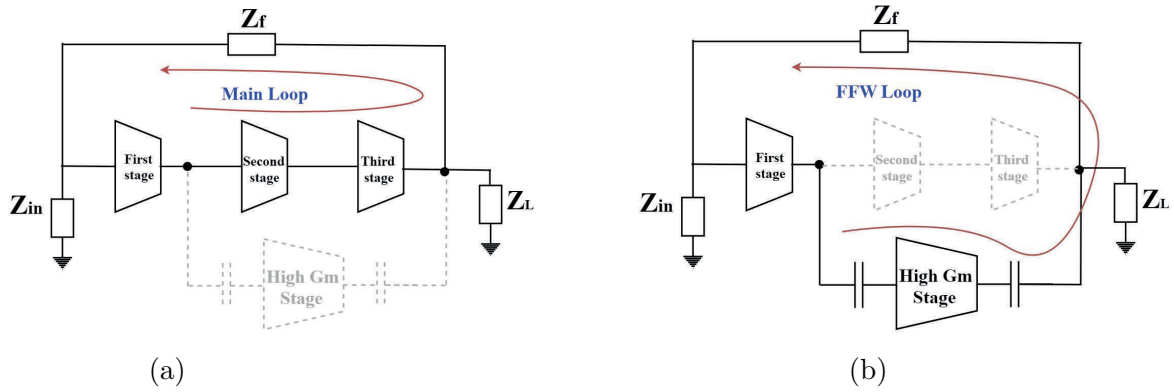


Figure 2.8: Two different loops in system: (a) main loop which is dominant in low frequency, and (b) FFW loop which is dominant in frequencies close to unity gain bandwidth.

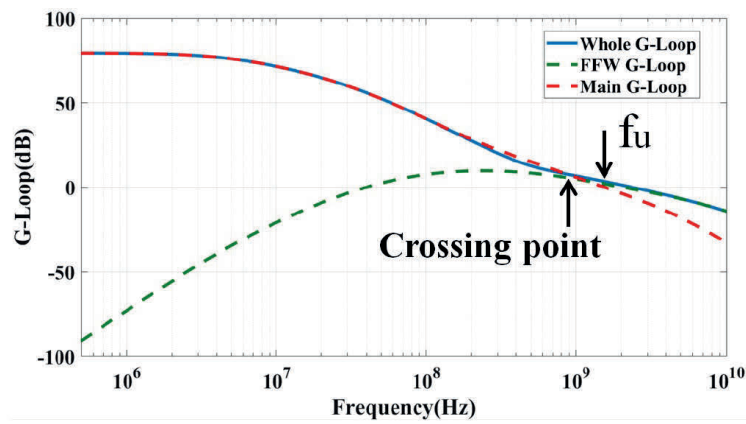


Figure 2.9: G-loop response: to improve the phase behavior, two G-loops should cross each other before the unity gain bandwidth

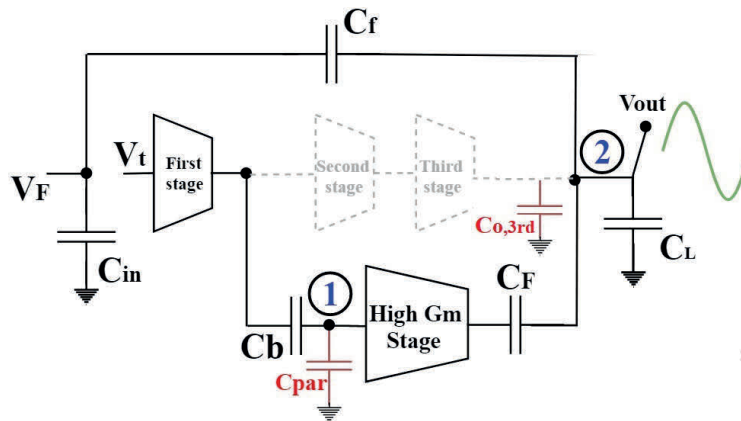


Figure 2.10: Gain loss and output clipping issue

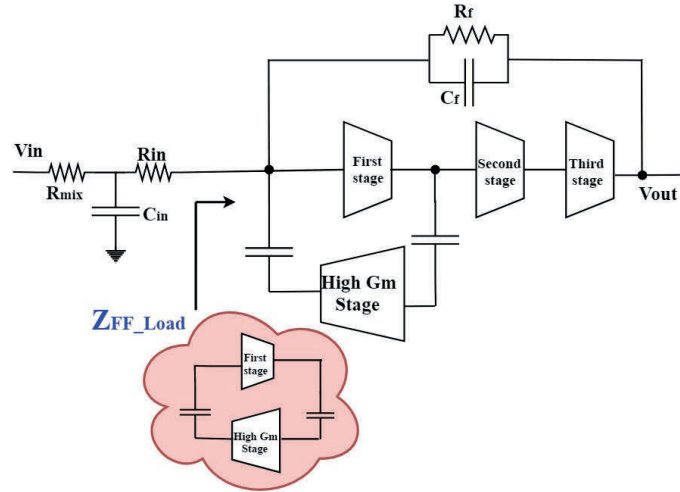


Figure 2.11: LFB approach to enhance frequency response

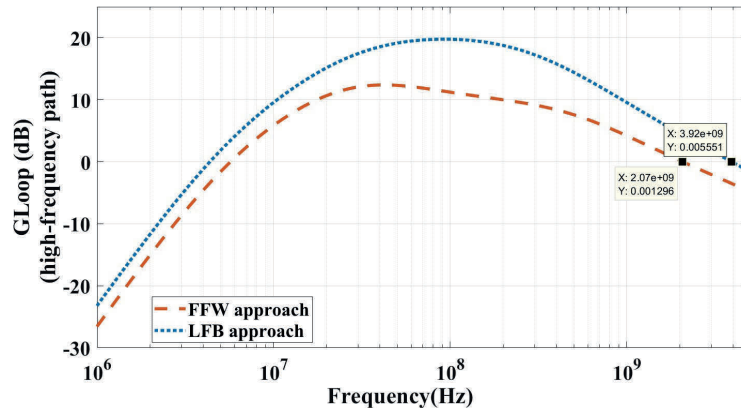


Figure 2.12: Enhance bandwidth in proposed LFB approach in compared to FFW one at the same power consumption

third stage, the output swing can be limited by the high- G_m stage and this can affect the circuit linearity.

2.4.3 Proposed structure: using local feedback (LFB) to compensate high frequency response

By connecting the high- G_m stage to the OTA's input, as shown in Figure 2.11, two main issues about the output node swing and signal loss in the FFW approach will be addressed. By avoiding capacitive division, more unity-gain bandwidth is achievable for the same power consumption compared to the FFW structure as shown in Figure 2.12. The local feedback loop consisting of the first and high- G_m

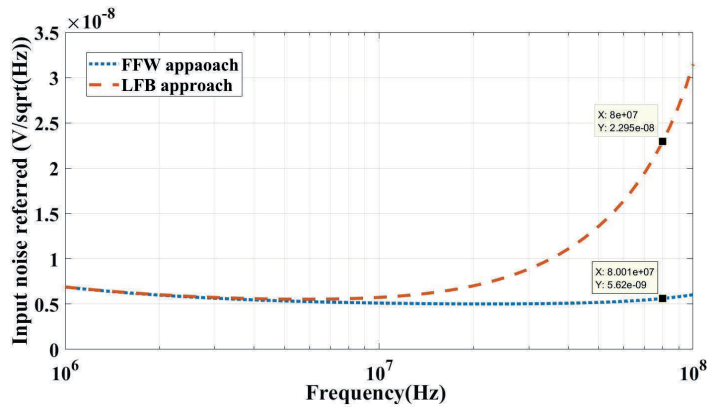


Figure 2.13: Noise comparison between FFW and LFB approach, input-referred noise in LFB approach will increase because of the loading effect ($Z_{FF-Load}$)

stage by loading the input node, $Z_{FF-Load}$, decreases input impedance which will increase input noise contribution based on (2.2) (Figure 2.13). Since for the same power consumption, boosting the bandwidth is the design goal, the LFB structure with more, but acceptable noise contribution is an appropriate choice for the high-bandwidth application. In the following section, some techniques will be presented to decrease noise contribution in the LFB approach.

2.4.4 Circuit Level Design

The circuit has three stages in the main path and a high- G_m stage in a local feedback branch to add high-frequency zero close to the f_u to extend the bandwidth. Figure 2.14a shows the first stage; a P-N cascode structure used to boost the gain and gm. By doubling the gm in the P-N structure, the power is saved, or for the same bias current, the noise contribution will be decreased for the first stage, which is the dominant part in noise contribution view. The top current source in P-side will be controlled by the common-mode circuit. Since the first stage is a high gain stage, it has one dominant pole at its output affected by the second and high- G_m stages loading effect.

The second stage shown in Figure 2.14b has local common-mode feedback inside itself to fix the output voltage. At low frequency, the G_m of the circuit equals only the PMOS transistor's transconductance (g_{mp}), on the other hand at high frequency, the signal is also amplified with NMOS transistors through C_Z capacitors, as a consequence the overall G_m will be $g_{mp} + g_{mn}$. From the stability point of view, there is one pole and zero close together that it is called doublets pole-zero which are located in $\omega_{p\text{-doublet}} = \frac{1}{R_Z C_Z}$ and $\omega_{z\text{-doublet}} = \frac{1}{R_Z C_Z (1 + \frac{g_{mn}}{g_{mp}})}$. The circuit takes advantage of doublet pole-zero to extend the bandwidth and improve the

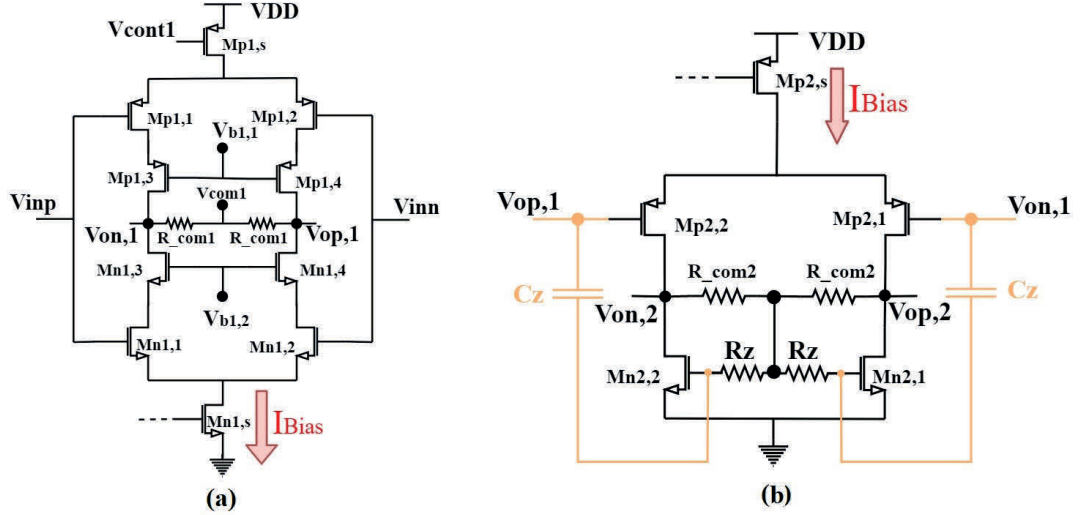


Figure 2.14: (a)P-N First stage (b)pole-zero doublets second stage

phase behavior of the circuit by canceling the effect of second stage's output pole.

The output stage is a push-pull stage as shown in Figure 2.15, that benefits the common-mode circuit to set the output voltage to $V_{DD}/2$. Figure 2.16 shows the complicated and challenging high- G_m stage with three stacked P-N stage, meaning multiply circuit transconductance by a factor of 6. The stage is ac coupled at input and output with three common-mode feedback stages to fix output nodes. A common-mode circuit to set the output voltage of the upside pair, one for the downside, and the other one in the middle to balance the top and bottom. From a stability point of view, not only the differential stability should be ensured, but also the common-mode stability must be checked for each common-mode circuit and for the whole system.

As mentioned before, by loading the TIA's input node, more noise power will be injected into the system. Since the high- G_m stage plays key role in high frequencies, it is possible to make its extra noise contribution to fall primarily out of desired bandwidth. Thus, by controlling its loading effect in bandwidth range, the noise contribution will decrease. One possible solution is playing with R_b and C_b values at the input of high- G_m stage to increase input impedance in bandwidth range. Moreover, decreasing the gain in the local feedback path can shrink the noise injection even more by adding R_{FF} and C_{FF} at the output, as shown in Figure 2.16. Figure 2.17 compares the input-referred noise in the modified version of the LFB approach with the FFW one. Decreasing the gain means that we are missing the bandwidth at the same time, and hence there is a trade-off between the bandwidth and noise contribution. By using several common-mode circuits in

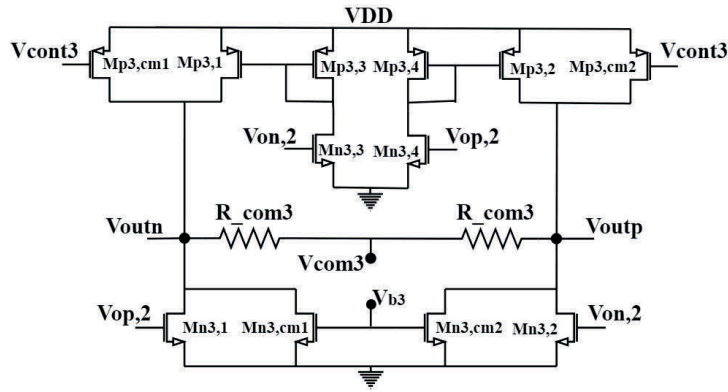


Figure 2.15: Push-pull output stage

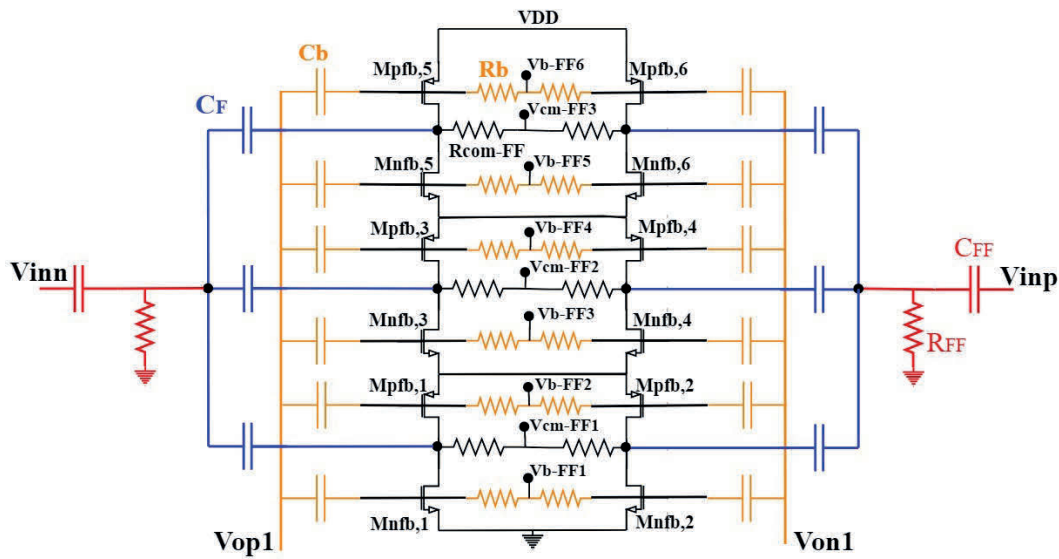


Figure 2.16: high G_m stage

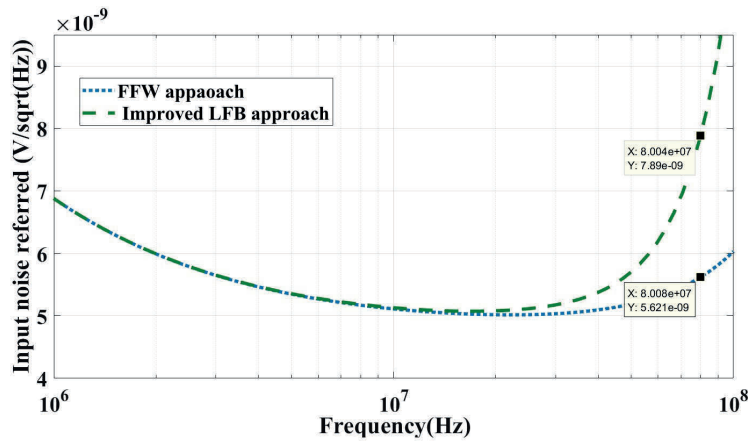


Figure 2.17: Decrease the noise injection by adding RC at the output of the high G_m stage in LFB approach and compare it with FFW approach

Parameter	Value($\mu m/\mu m$)
$M_{p1,1}$ and $M_{p1,2}$	100/0.1
$M_{n1,1}$ and $M_{n1,2}$	76/0.1
$M_{p1,3}$, $M_{p1,4}$, $M_{n1,3}$ and $M_{n1,4}$	16/0.1
$M_{p2,1}$ and $M_{p2,2}$	4/0.08
$M_{n2,1}$ and $M_{n2,2}$	6/0.08
$M_{p3,1}$ and $M_{p3,2}$	14/0.08
$M_{n3,1}$ and $M_{n3,2}$	18/0.08
$M_{p3,3}$, $M_{p3,4}$, $M_{n3,3}$ and $M_{n3,4}$	4/0.08
$M_{p3,cm1}$ and $M_{p3,cm2}$	3/0.08
$M_{n3,cm1}$ and $M_{n3,cm2}$	2/0.08
$M_{pfb,1}$, $M_{pfb,2}$, $M_{pfb,3}$, $M_{pfb,4}$, $M_{pfb,5}$, $M_{pfb,6}$	18/0.035
$M_{nfb,1}$, $M_{nfb,2}$, $M_{nfb,3}$, $M_{nfb,4}$, $M_{nfb,5}$, $M_{nfb,6}$	16/0.035
Resistor	Capacitor
$R_z=1.5\text{ k}\Omega$	$C_z=40\text{ fF}$
$R_b=3\text{ k}\Omega$	$C_b=200\text{ fF}$
$R_{FF}=230\ \Omega$	C_F and $C_{FF}=2.4\text{ pF}$

Table 2.1: Design parameters' value

the high- G_m block, the noise injected from the power supply and ground to input node are expected to be negligible. Design parameters are listed in the Table 2.1.

2.4.5 G-Loop Analysis

To have a better understanding about circuit stability, the system G-Loop, V_f/V_t , can be calculated by opening the loop at the input of the OTA, injecting a test signal V_t and observing the return signal V_f as shown in Figure 2.18a and consider each stage's poles and zeros position (Figure 2.18b). The first stage has a dominant pole at around $\omega_{P,1}=1/R_{L1}C_b$ and a zero coming from the high G_m stage's loading effect at $\omega_{Z,1}=1/R_bC_b$. There is a pole and zero close together around 2 GHz and two high-frequency poles after 20 GHz. As mentioned before, the second stage has doublet pole and zero and the output pole at $\omega_{P,2}=1/R_{L2}C_{L2}$. The Last stage plus the feedback path has the second dominant pole of the system at $\omega_{P,3}=1/R_{Mix}C_{in}$ and a zero $\omega_{Z,2}=1/R_{in}C_{in}$ thanks to the input resistor, R_{in} close to the unity gain-bandwidth. There are some other poles and zeros that cancel each other or located at very high frequency. The TIA's parameters listed in Table 2.2. Figure 2.19 shows the first stage's zero and the second stage's pole are in the same position, and hence cancel each other.

2.4. High Bandwidth OTA Design

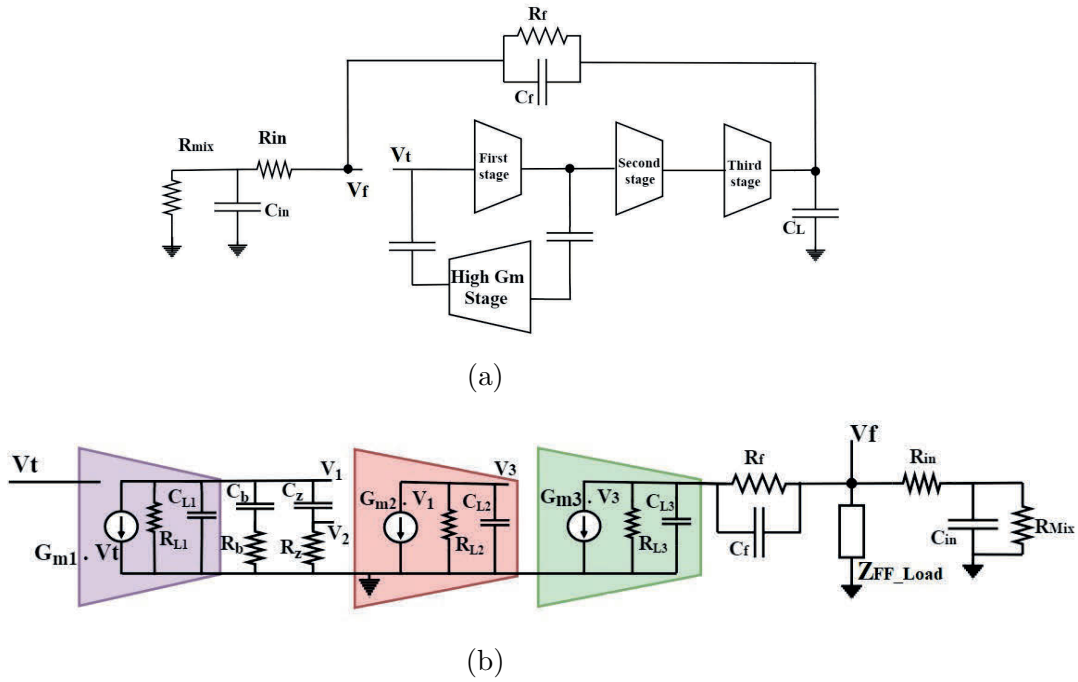


Figure 2.18: G-Loop analysis: (a) break the TIA's main loop (b) find poles and zeros position to assess the system stability

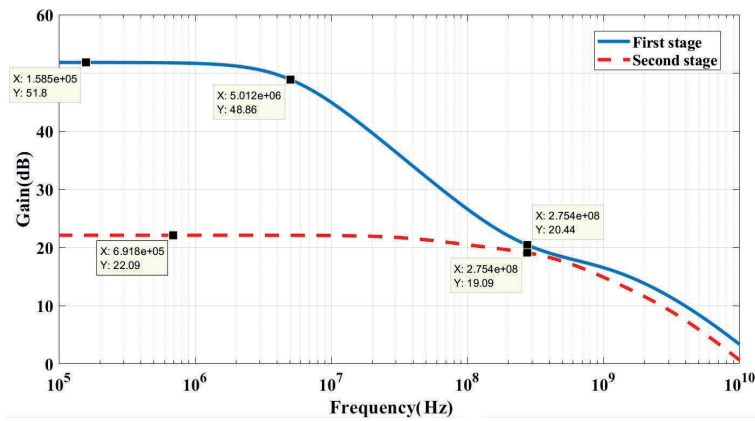


Figure 2.19: First and second stages' poles and zeros position

Resistor	Capacitor
$R_{in}=10 \Omega$, $R_{Mix}=500 \Omega$	$C_{in}=8 \text{ pF}$
$R_F=2 \text{ k}\Omega$	$C_F=1 \text{ PF}$

Table 2.2: TIA's parameters value

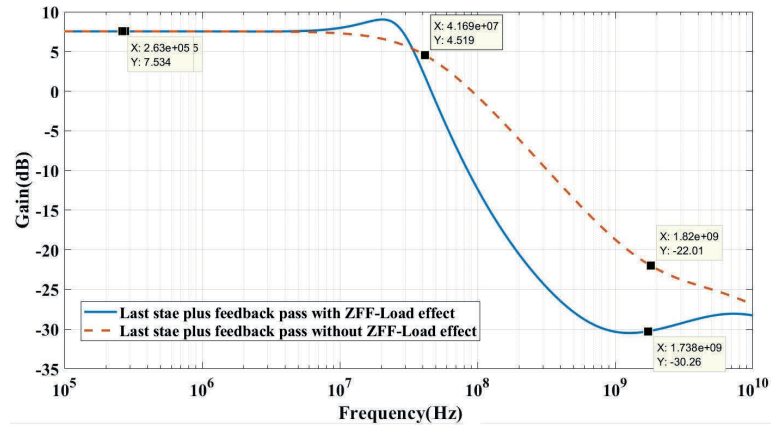


Figure 2.20: Last stage plus the feedback path with and without considering the Load effect of $Z_{FF-Load}$

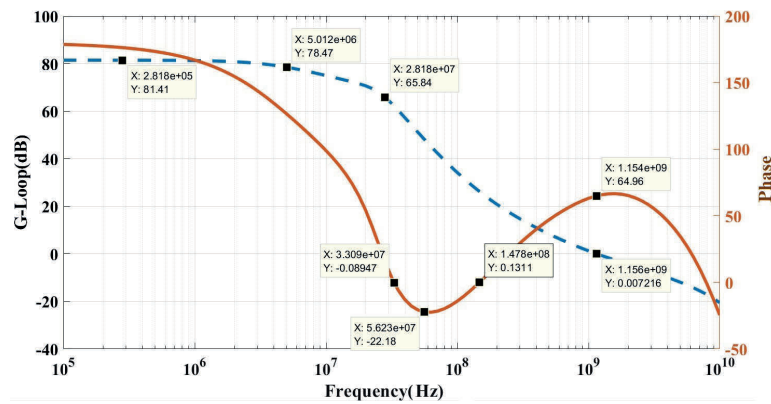


Figure 2.21: The whole G-Loop response of the circuit, phase goes below zero degree in some frequency range

Figure 2.20 demonstrates that the local feedback loop by loading the input node decreases the gain and introduces some complex poles and zeros to the system. The overall G-Loop response has been shown in Figure 2.21 with more than 80 dB gain. In some range of frequency, the phase plot goes below zero degree while the gain is positive. On the other hand, where the gain meets 0 dB, there is sufficient phase margin to say circuit is stable; now the question is that this system is really stable or not?

It is a situation called conditional stability and it is not possible to judge the system stability by only looking at the bode diagram. Thus, in this case, the Nyquist plot should be checked. As shown in Figure 2.22, although the phase reaches 180 degrees on the left side of the (-1,0) point, the contour does not encircle it, therefore the system will be stable. It is obvious in this situation by decreasing

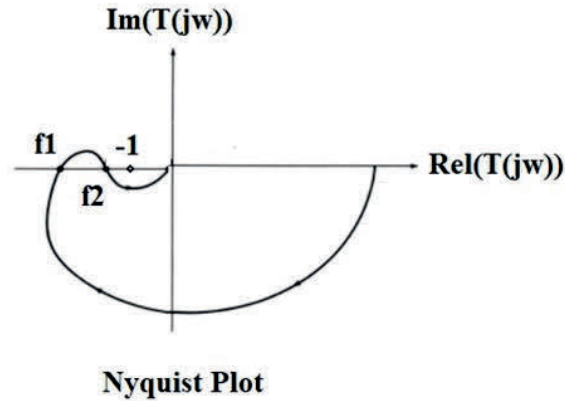


Figure 2.22: Nyquist plot diagram for conditional stable system

or increasing the gain noticeably, the system can go to instability, for instance, by injecting a large signal to the system, some stages are forced to saturate, by losing the gain there is such a possibility for oscillation.

Figure 2.23 shows the magnitude response of the loop in different process corners and operating temperature. The loop demonstrates stability with $GBW=1.16$ GHz and 64 degree phase margin (PM) in nominal corner mode. The most critical corner for stability is Fast-Fast (FF), where poly-silicon resistor, R_{in} , strong variations shifts $\omega_{Z,2}=1/R_{in}C_{in}$ to a higher frequency, and hence by increasing GBW to 1.4 GHz, PM will drop to 42 degrees. Montecarlo simulation over 400 samples denotes the mismatch effect. A standard deviation of 170 MHz around 1.05 GHz for GBW and of 4.4 degree around 63 degree for PM is obtained, as shown in the histograms of Figure 2.24.

2.4.6 Linearity Results

As mentioned before, the linearity plays the main factor in TIA design for SAW-Less receivers. The second-order non-linearity is neglected considering a fully differential structure for the OTA. The simple approaches to analysis the circuit non-linearity proposed in different articles, [31–33] is based on a simple model for each stage shown in Figure 2.25. Each stage is modeled as a transconductor (g_{m1}), loaded by Z_o , and to analyze the non-linearity, only two distortion terms are considered. The first one due to the transconductance g_{m3} and the second one comes from the output conductance g_{ds3} . By applying two sinusoidal signals of amplitude A_1 and A_2 at frequency ω_1 and ω_2 , the inter-modulation components power (IM3) located at $2\omega_1 - \omega_2$, depends on the signal amplitude at the input

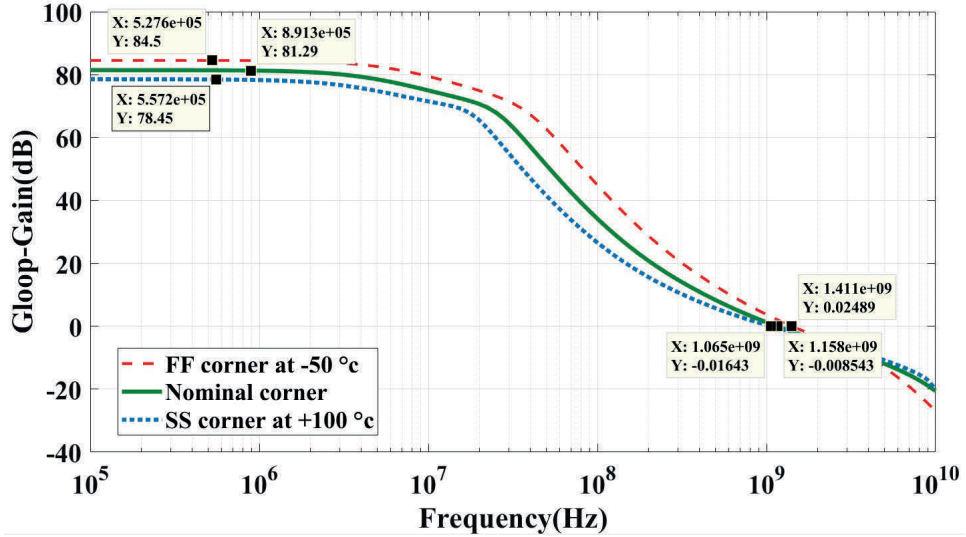


Figure 2.23: Post-Layout loop gain magnitude simulation on nominal corner, SS corner at +100 °C and FF corner at -50 °C

and output of the each stage as given in the following equations

$$i_{gm3} = \frac{3}{4}g_{m3}A_1^2A_2 \sin(2\omega_1 - \omega_2)t \quad (2.5)$$

$$i_{gds3} = \frac{3}{4}g_{ds3}(A_1 \cdot |G_{w1}|)^2(A_2 \cdot |G_{w2}|) \sin((2\omega_1 - \omega_2)t + 2\theta_1 - \theta_2), \quad (2.6)$$

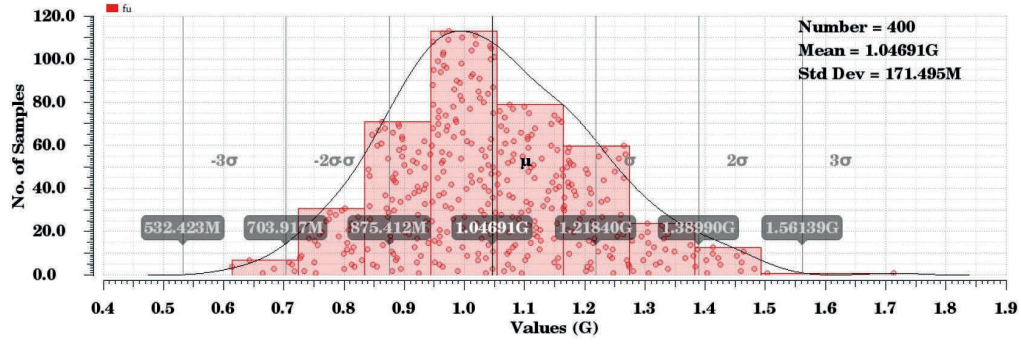
where G_{ω_i} and θ_i are the gain and phase of the each stage at ω_i respectively, g_{m3} and g_{ds3} are the third order non-linear coefficients. The IM3 voltage ($v_{IM,i}$) at the output of each stage is found by multiplying the total injected current $i_{gm3,i} + i_{gds3,i}$ by the closed-loop output impedance $Z_{oCL,i}$ at f_{IM3} , as given in following equation

$$v_{IM,i} = \left(\frac{3}{4}g_{m3}A_{1,i}^2A_{2,i} + \frac{3}{4}g_{ds3}(A_{1,i} \cdot |G_{w1,i}|)^2(A_{2,i} \cdot |G_{w2,i}|) \right) \times \frac{Z_{oOL,i}(2\omega_1 - \omega_2)}{1 + G_{Loop}(2\omega_1 - \omega_2)} \sin(2\omega_1 - \omega_2)t, \quad (2.7)$$

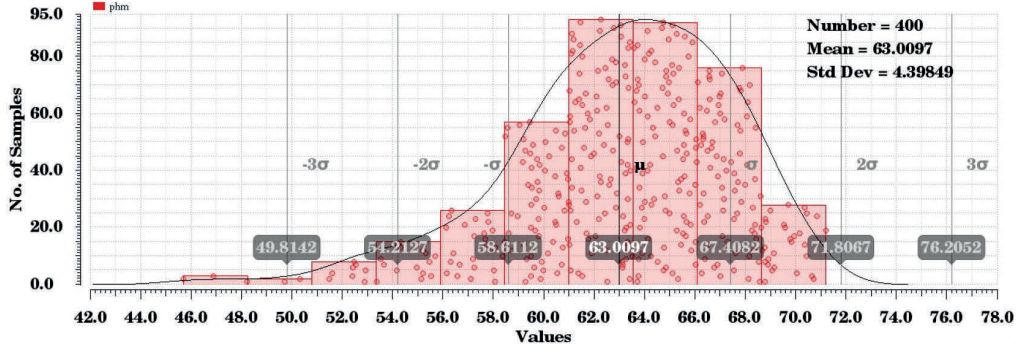
where $Z_{oOL,i}$ is the open-loop output impedance of each stage.

Based on (2.7), two definitions for non-linearity distortion can be presented: distortion injection and distortion compression. The distortion injected by each stage in the circuit depends on the voltage swing at the intermediate nodes at the frequency of the input tones. Distortion compressed by the loop depends on the loop gain at the IM3 frequency. Generally, it can be said to improve the circuit linearity, an OTA with sufficiently high bandwidth and gain is needed to compress

2.4. High Bandwidth OTA Design



(a) GBW [MHz]



(b) Phase Margin [deg]

Figure 2.24: Monte Carlo simulation of GBW and PM of the TIA loop gain

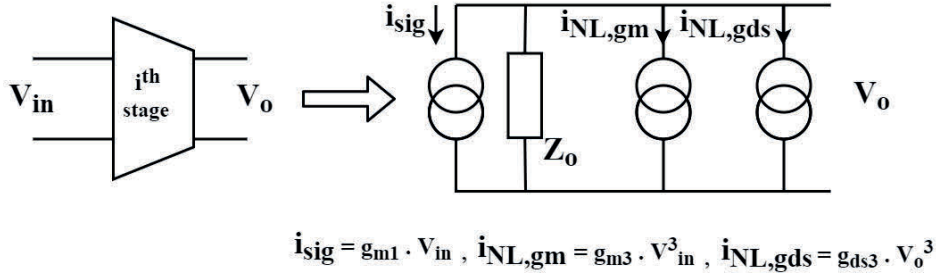


Figure 2.25: Simple non-linearity model of each stage of OTA

distortion and reduce injection. In low frequency, the linearity is expected to be limited by a large swing at the output of the last stage. Thus, by increasing the frequency and dropping the TIA's gain after band edge (80 MHz), it is expected the to see improvement in linearity in the middle-frequency range. At high-frequency range where the first stage has still noticeable gain compared to other stages, the g_m non-linearity of the first stage can be dominant.

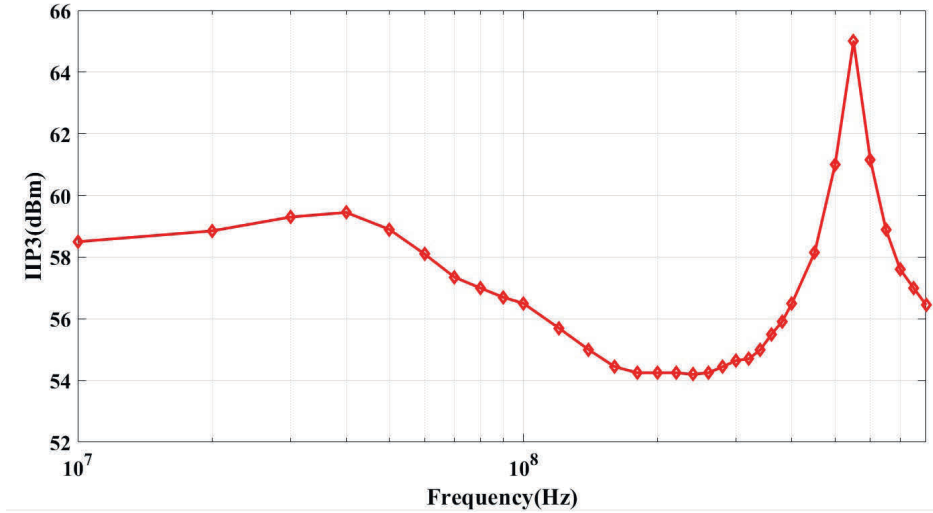


Figure 2.26: Input referred IIP3 of the TIA

Figure 2.26 shows the input-referred IP3 (IIP3) for the TIA, as it can be seen in some frequency range contrary to what was expected, the IIP3 dropped. One explanation is the loading effect of LFB path at the input node ($Z_{FF-Load}$); by decreasing the G-Loop gain and increasing the input node swing, it is obvious to inject more non-linearity to the system. Again in high frequency, the first stage's non-linearity forces IIP3 to fall down, however in a higher frequency range, input capacitor (C_{in}) fix input node variation, and by filtering non-linear component, the IIP3 will increase. Despite weird behavior in the IIP3 plot, it shows such a high value, more than +54 dBm in all frequency range thanks to high gain made in G-Loop and conditional stability.

2.4.7 Measurement Results

(Notice: since the fabricated chip starts to oscillate by putting the nominal biasing current for the first stage (for unknown reasons), a lower current is injected to the first stage to keep stability. Thus, by missing the G-loop gain, it is expected to have lower IIP3 in result). As aforementioned, TIA as a base-band filter is the last block in a current mode receiver depicted in Figure 2.27. To measure the TIA's specifications as a stand-alone block, it is disconnected from the front-end part by switching off the mixers' switches. The TIA was fabricated by tsmc 28 nm protocols. The whole occupied area is around 0.018 mm^2 thanks to decreasing the input capacitor to 8 pF as listed in Table 2.3. As can be seen in Figure 2.28a, four stages were put in the vertical plan in layout to provide symmetric design for better matching. Figure 2.28b shows the chip photograph of the whole receiver

Resistor	Capacitor
$R_{in}=10\ \Omega$, $R_{Mix}=500\ \Omega$	$C_{in}=8\ \text{pF}$
$R_F=2\ \text{k}\Omega$	$C_F=1\ \text{PF}$

Table 2.3: TIA's parameters value

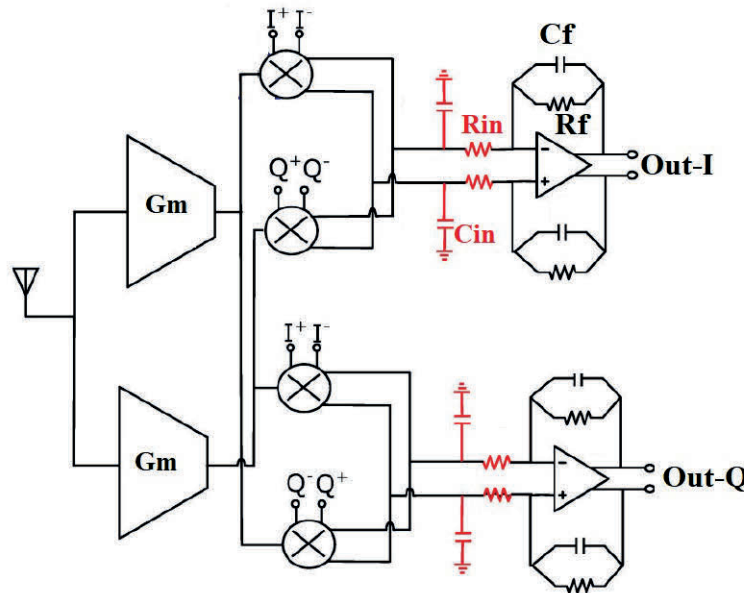


Figure 2.27: TIA as a base-band filter in Current-mode receiver

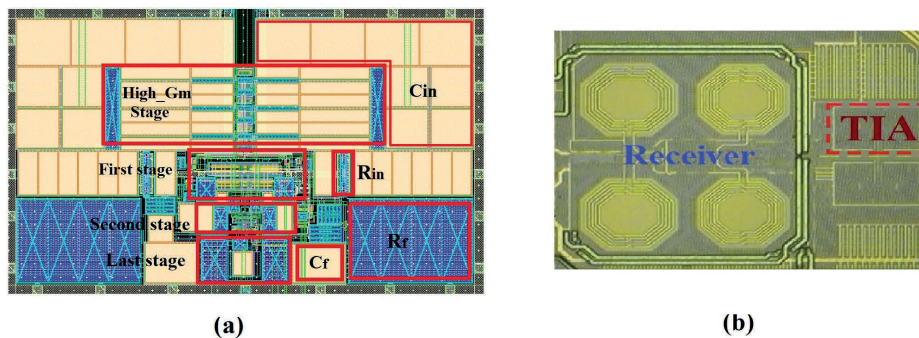


Figure 2.28: TIA's (a) layout structure: vertical design to keep symmetry (b) chip photograph in 28 nm TSMC technology

and the TIA.

The measurement setup has been shown in Figure 2.29, where the chip was mounted on the PCB by a bonding machine [25]. The signal goes to the board by an external balun converting the single-ended input signal to two differential

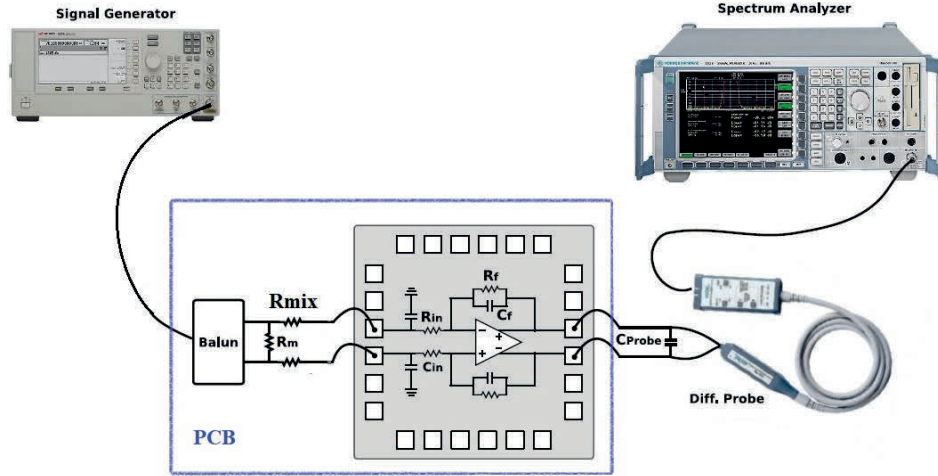


Figure 2.29: TIA measurement setup

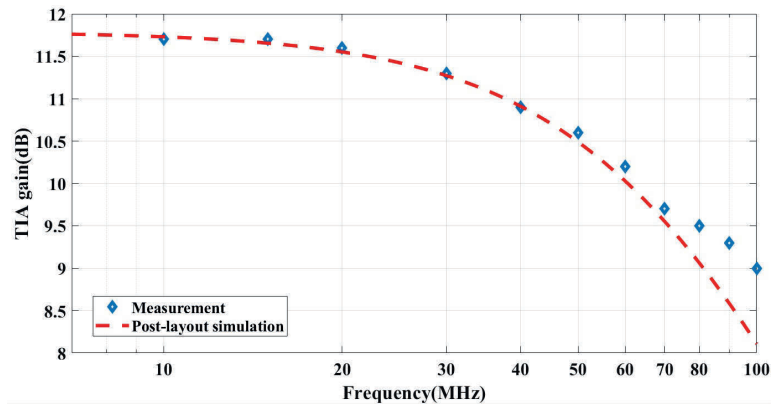


Figure 2.30: The frequency response of first order TIA filter

ones. Two 500Ω input resistors (R_{Mix}), which do V-I conversion, emulate the driving resistance of receiver front-end estimated according to [36]. By considering 500 fF differential capacitance for the probe used to measure output signal, Figure 2.30 shows in-band gain measurement and post-layout simulation results of TIA. The TIA has 11.8 dB gain with 80 MHz cutoff frequency. The output noise power spectral density (PSD) given in Figure 2.31 shows less than $-139 \text{ dBm}/\sqrt{\text{Hz}}$ in-band noise power. The in-band noise measured with 20-dB probe gain mode (to overcome the spectrum analyzer's noise), will increase close to band edge by decreasing input impedance of TIA due to C_{in} . The main noise contributors are driving resistors through the mixer, OTA's first stage, and feedback resistors. The input-referred noise power integrated up to 64 MHz (80 percent of bandwidth) is

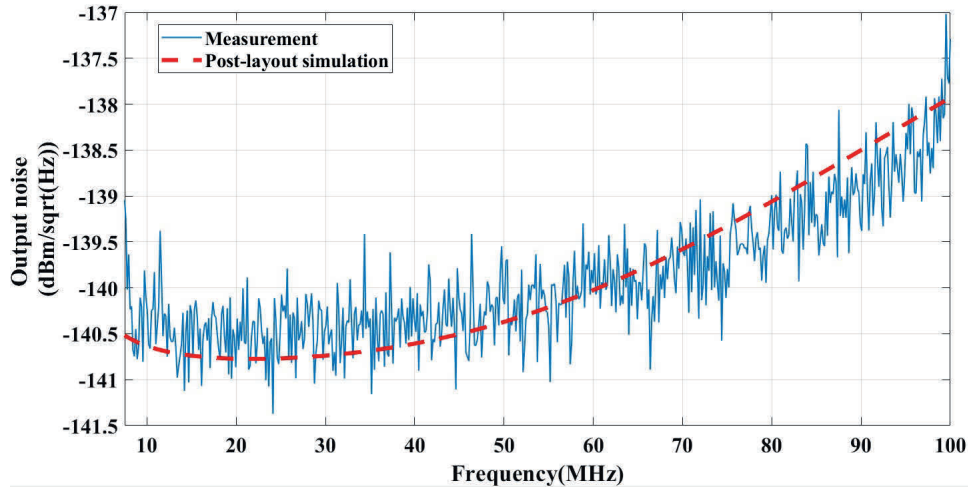


Figure 2.31: The output noise power of TIA

Parameter	State-of-The-Art			
	This work	ESSCIRC(2019) F. Fary [34]	Springer(2019) D'Amico [35]	JSSC(2018) G. Pini [25]
Technology(nm)	28	28	28	28
Supply(V)	1.8	1.1	0.9	1.8
Order	1	6	3	1
BW(MHz)	80	50	132	20
Power(mw)	4.2	3.63	0.34	5.4
OOB IIP3	54	16.5	5.5	41
$V_{n,rms}$	44	540	257	21.1
$FOM(dBJ^{-1})$	188	154.8	163.6	176.7
$f_{IM3}(MHz)$	40	39	119	10
$FOM_{IM3}(dBJ^{-1})$	185	153.7	163.2	173.7

Table 2.4: TIA performance compared to other research works

44 μV_{RMS} . The input-referred IP3 measured by applying two tones at 50 and 98 MHz (with inter-modulation frequency at 2 MHz), shows 30.1 dBm compared to 42.6 dBm in post-layout simulation. To compare the TIA performance with other State-of-The-Art filter implementations, the figure of merit is defined in two

different ways as below

$$\text{FOM} = \text{IMFDR}_3 + 10 \log \left(\frac{N \cdot \text{BW}}{\text{Power}} \right) \quad (2.8)$$

$$\text{IMFDR}_3 = \frac{2}{3}(\text{IIP3} - P_N) \quad (2.9)$$

$$\text{FOM}_{\text{IM3}} = \text{FOM} + 10 \log \left(\frac{f_{\text{IM3}}}{\text{BW}} \right), \quad (2.10)$$

Where N and P_N are the filter order and input-referred noise power, respectively. Table 2.4 shows post-layout simulations of TIA compared to others' measurement results.

2.4.8 Conclusion

A high bandwidth TIA as a first-order filter for the current mode receiver was explained in this chapter. Extending the bandwidth to 80 MHz by using the local feedback approach and lowering the power consumption in structure and circuit level, improved the overall performance of the TIA compared to the all other works. Moreover, the noise power contribution and occupied area on the chip were decreased by shrinking the input capacitor thanks to the high GBW product OTA [37].

High Bandwidth Base-band Filter for 5G Applications

The fifth generation of telecommunication system introduces some new challenges for receiver design. Trying to extend the bandwidth closed to 200 MHz and providing sufficient linearity at the same time are the main critical issues in any recent research works. Designing a high bandwidth base-band filter that can attenuate out-of-band blockers properly in new multi-standard applications is the main struggle for designers in 5G systems. Burning less power, especially for mobile applications and improving the sensitivity, are also other parameters that should be considered in any new design. In this chapter, a third-order base-band filter in a current mode receiver is explained. The filter, which consists of a second-order Rauch filter and a first-order TIA as a buffer, has 200 MHz bandwidth, and it is supposed to provide more than 15 dBm, OIP3 at the output of receiver chain. A feed-forward approach in both Rauch and TIA filters is used to make them stable. Post-layout and measurement results show that the circuit accurately follows the design specifications.

3.1 Current-Mode Receiver for 5G application

Figure 3.1 shows a current-mode receiver with +46 dBm maximum gain in the whole chain. The receiver has two transformers to control the gain in the whole chain. The baseband filter after the passive mixer with 8 GHz local oscillator has two different modes: low-mode frequency from dc to 200 MHz and high-mode one from 400 MHz to 1 GHz. In the low mode, the baseband filter is going to be

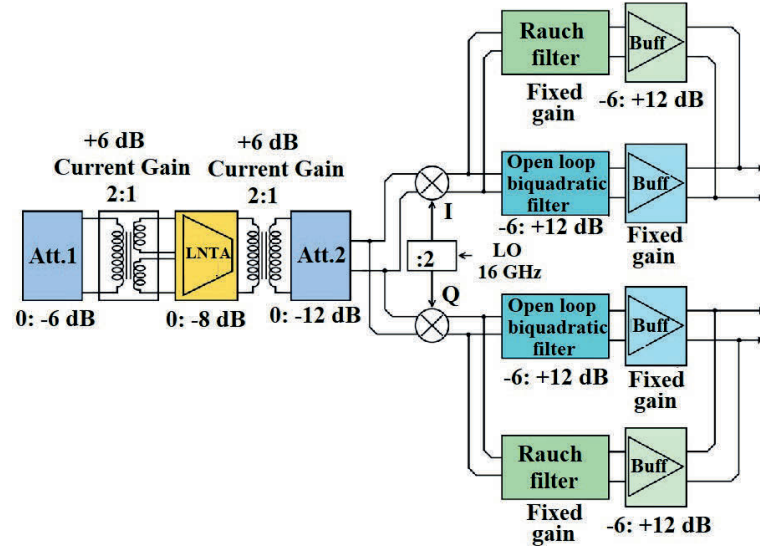


Figure 3.1: 5G Current-mode receiver block diagram

designed in such a way to have gain variation and bandwidth control possibility. Some gain variation also is defined in LNTA stage and transformers to provide 44 dB total gain control in the receiver side. The whole receiver chain should be sufficiently linear to provide more than 15 dBm of OIP3; and it is expected to have less than 5 dB for noise figure(NF) in maximum gain mode. The Figure 3.2 shows the variable gain LNTA structure plus transformer; the LNTA has a P-N structure to save power.

3.2 Low-mode baseband filter structure

The low-mode baseband filter is a third-order filter composed of a second-order Rauch filter plus first-order TIA, as shown in Figure 3.3. Rauch filter has four stages in the main path and one parallel feed-forward branch(FF) to guarantee stability in the high-frequency range. TIA with the same structure has three stages in its main path, so with two different loops working together, the main challenge is keeping the stability of the whole chain. The filter gain is going to be changed in TIA's part by variable resistors, R_{var} , and filter bandwidth will be controlled by changing the resistors and capacitor values in four modes: 25, 50, 100 and 200 MHz bandwidth.

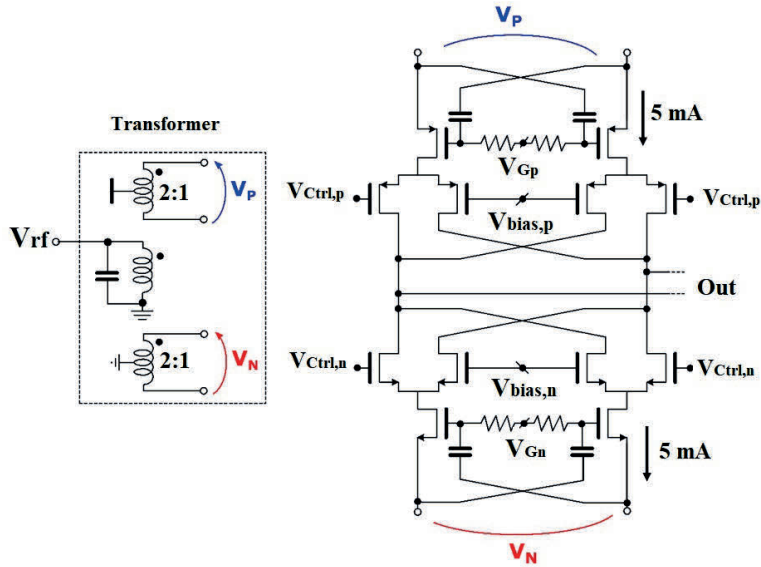


Figure 3.2: LNTA structure

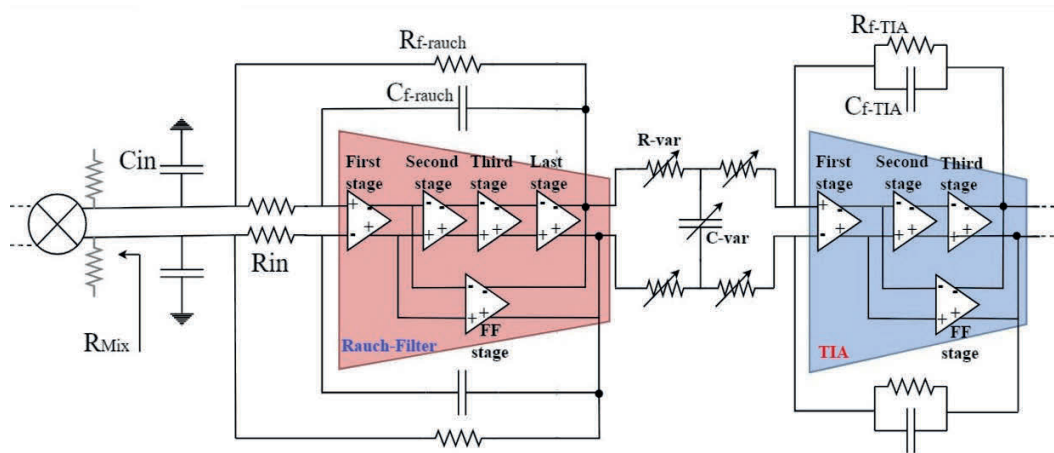


Figure 3.3: Third-order baseband filter: 2^{nd} Rauch + 1^{st} TIA

3.2.1 Filter loops stability

Following the same approach as in the previous chapter, to consider the loop stability, it is preferred to break each loop to two different loops: one loop included the main path is dominant in the low-frequency range and the other one passing through the feed-forward path for higher frequency range as shown in Figure 3.4a and b. In low-frequency range, the main path is dominant, and in higher frequency close to unity gain bandwidth, the FF path determines the G-loop response. As

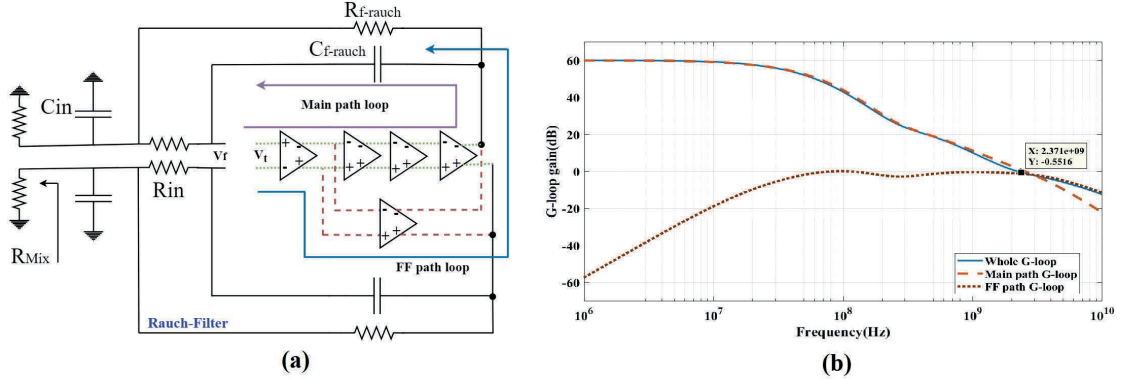


Figure 3.4: The Rauch filter G-loop: (a) two main and FF loops (b): The main and FF G-loops' domination parts in frequency range

Resistor	Capacitor
$R_{in}=90 \Omega$	$C_{in}=8.5 \text{ PF}$
$R_{f-rauch}=2 \text{ k}\Omega$	$C_{f-rauch}=250 \text{ fF}$
$R_{var}=250 \Omega$	$C_{var}=1.5 \text{ PF}$
$R_{f-TIA}=1 \text{ k}\Omega$	$C_{f-TIA}=600 \text{ fF}$

Table 3.1: Rauch filter's resistors and capacitors value

mentioned before, the FF auxiliary branch by adding zero to the system and improving its phase behavior extends the bandwidth and keeps the stability of the circuit. Figure 3.5a and b show the whole G-loop responses for Rauch and TIA filters based on the filter's design parameter value shown in Table 3.1, the mixer loading impedance, R_{Mix} , is around 200Ω . The unity-gain bandwidth and phase margin for Rauch and TIA loops are 2.4 GHz ,68 degree and 4.3 GHz, 54 degree respectively, which guarantee the whole system stability.

In addition to differential loops in Rauch and TIA parts, there are several common-mode loops in the circuit that must be checked for stability. The main concern for common-mode stability comes from the Rauch filter's main path loop which has four stages, where a differential loop has a negative feedback response, a common-mode loop will show a positive feedback one. By keeping the gain of common-mode G-loop, sufficiently lower than 0 dB, the circuit can be stable even with positive feedback. Figure 3.6 shows the common-mode G-loop gain, which is around -40 dB at 10 GHz, so even with a positive loop, the circuit will not oscillate.

3.2. Low-mode baseband filter structure

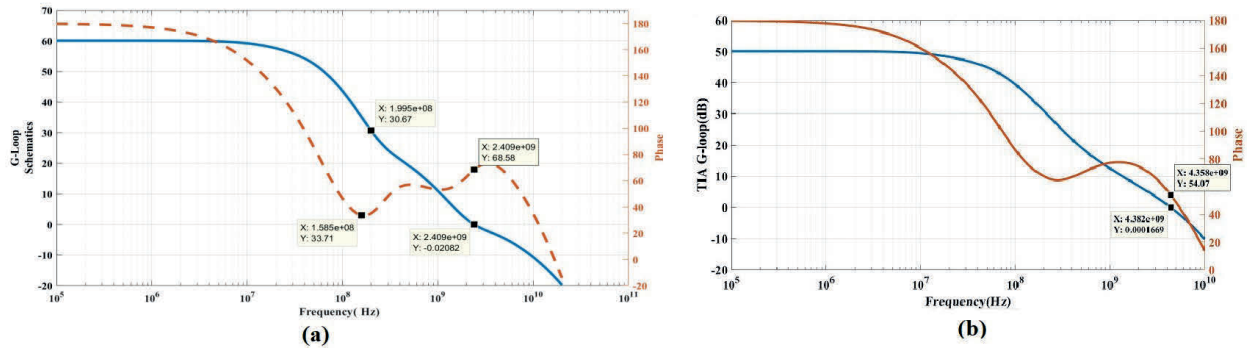


Figure 3.5: Filter G-loop response: (a)Rauch filter G-loop (b)TIA G-loop

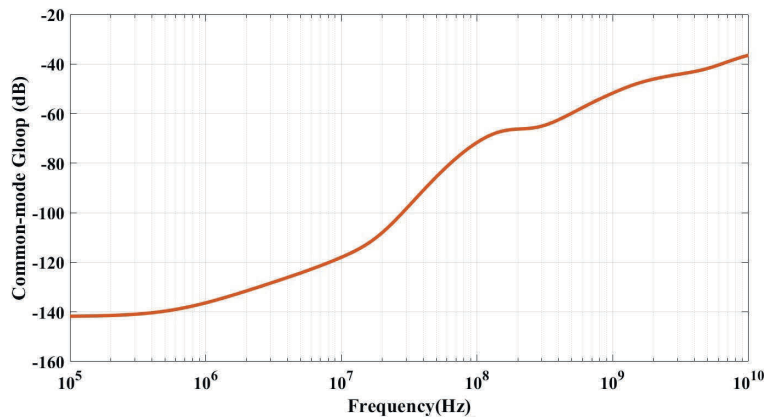


Figure 3.6: The Rauch filter common-mode G-loop response

3.2.2 The receiver specifications

As aforementioned, the receiver has 46 dB gain at maximum level, and as shown in Figure 3.1, the gain can be controlled in different stages. The first and intermediate transformers provide 18 dB gain variation, 8 dB gain control in LNTA, and finally 18 dB for baseband filters. Figure 3.7 shows 18 dB gain variation with 6 dB step from 46 dB to 28 dB. The gain changes by the variable resistor in front of the TIA filter that controls TIA's gain. Figure 3.8 also shows the gain variation controlled by transformer(3dB) and LNTA(8dB). The filter is expected to have more than 33 dB filtering at a frequency equal to four times its bandwidth and less than 1 dB gain ripple in the flat region. The filter bandwidth can be controlled by changing the capacitor values from 25 MHz to 200 MHz as shown in Figure 3.9. The filter satisfies more than 33 dB rejection and less than 1 dB fluctuation in bandwidth range.

To check the circuit linearity, two tones at 175 MHz and 170 MHz are applied to

3. High Bandwidth Base-band Filter for 5G Applications

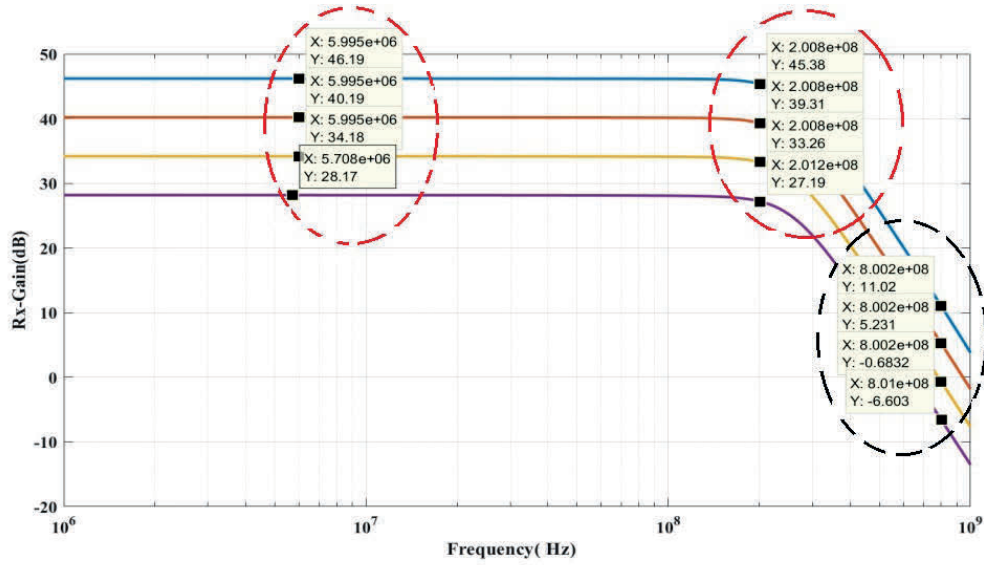


Figure 3.7: Receiver gain variation by filter's gain controlling

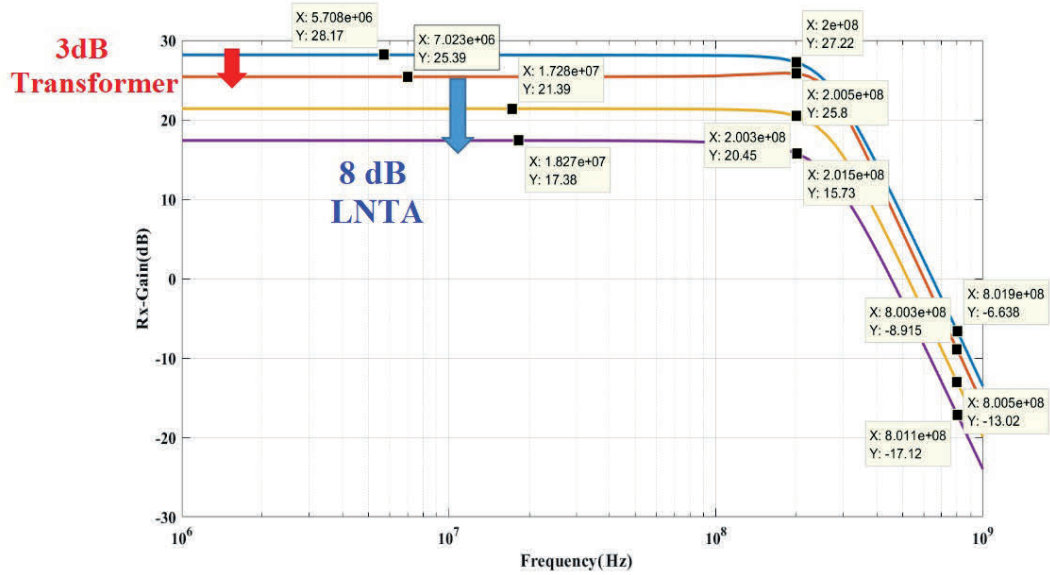


Figure 3.8: Receiver gain variation by front-end stages' gain controlling

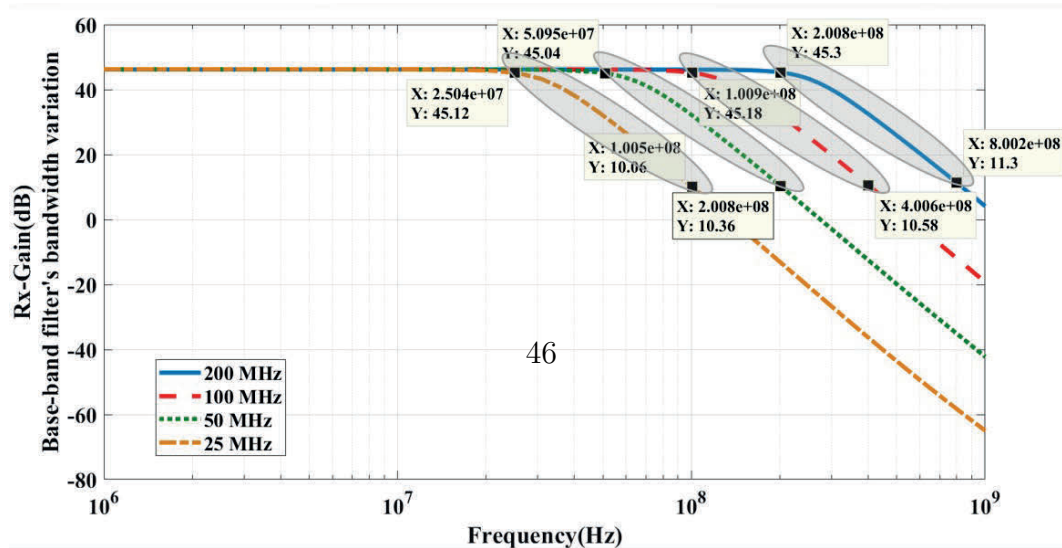


Figure 3.9: Filter bandwidth variation

Gain(dB)	NF(dB)	Requested NF(dB)	OIP3(dBm)	Requested OIP3(dBm)
46	4.94	5	38.7	15
40	4.97	9.2	36.2	15
34	5.06	13.4	31.1	15

Table 3.2: The whole receiver chain simulation results, NF and OIP3

the receiver input. By looking at 180 MHz as the intermodulation frequency, more than 15 dBm output IP3 is needed in all gain levels in the whole receiver chain. From the noise point of view, the NF in maximum gain level should be less than 5 dB, and it is expected to increase 0.7 dB by each dB gain degradation. Table 3.2 summaries the simulation results for the whole receiver chain. It is clear that decreasing the gain will drop the output IP3, and increases the noise contribution; however, Table3.2 shows the results meet the requested specifications for all gain values.

3.3 Second order filter design

Although high order baseband filters design can increase the design challenges compared to the first-order filters (like TIA), they can provide more freedom for designers [20, 22, 38]. In the following sections, the second-order Rauch filter will be explained and compared to other structures.

3.3.1 Rauch filter properties

A well-known structure that can implement a 2^{nd} order filter using only an OTA is Rauch filter [39]. Figure 3.10 shows a Rauch filter by considering the mixer driving impedance as a resistive load(R_m). The signal transfer function, $H(s) = V_{OUT}/I_{IN}$, of the Rauch filter is a biquad equation

$$H(s) = \frac{G}{1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}} \quad (3.1)$$

in which: $G = R_2$, $\omega_0 = \sqrt{\frac{1}{R_1 C_1 R_2 C_2}}$, $Q = \frac{1}{\omega_0 C_2 \left(R_1 + R_2 + \frac{R_1 R_2}{R_m} \right)}$

Based on Table 3.1, the quality factor(Q) and ω_0 of proposed Rauch filter are around 0.83 and 255 MHz respectively; which guarantee less than 1 dB inband ripple for 200 MHz bandwidth. Moreover, 8.5 pf input capacitor with the total

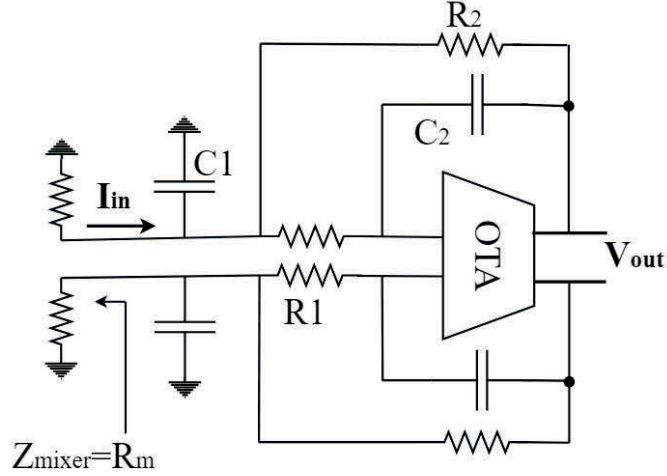


Figure 3.10: Rauch filter model

resistive impedance equal to 60Ω at the input can provide sufficient linearity and noise power at the output node. The feedback resistor R_2 determines the inband trans-impedance gain and the time constants R_1C_1 and R_2C_2 set the selectivity. The Rauch filter's input impedance behaves like an RLC resonant network because of a gyrator circuit created by R_2 and the integrator $\frac{1}{sR_1C_2}$. At low frequency, the virtual-ground node follows the inductance behavior, while after the cut-off frequency, the impedance will be set by C_1 as shown in Figure 3.11, where $A(s)$ is the OTA's transfer function. At the cut-off frequency, the inductance and the capacitance resonate together, and the input impedance meets its maximum value equal to $2R_1$.

Figure 3.12 shows different components' noise contribution. The noise transfer function of each element at the output node can be expressed by the following equations

$$\frac{V_{out,n}}{V_{n,r2}} = \frac{1}{S^2(R_1C_1R_2C_2) + SC_2(R_1 + R_2) + 1} \quad (3.2)$$

$$\frac{V_{out,n}}{V_{n,r1}} = \frac{1 + SR_2C_1}{S^2(R_1C_1R_2C_2) + SC_2(R_1 + R_2) + 1} \quad (3.3)$$

$$\frac{V_{out,n}}{V_{n,ota}} = 1 + \frac{1 + SR_2C_1}{S^2(R_1C_1R_2C_2) + SC_2(R_1 + R_2) + 1}. \quad (3.4)$$

While the noise transfer function of R_2 is flat in-band and follows the signal transfer function, thanks to the high pass noise shaping due to zero at $1/R_2C_1$ for input resistor, R_1 and OTA, they have a less in-band contribution in output integrated noise power [40]. The noise amplification can be reduced by shifting the

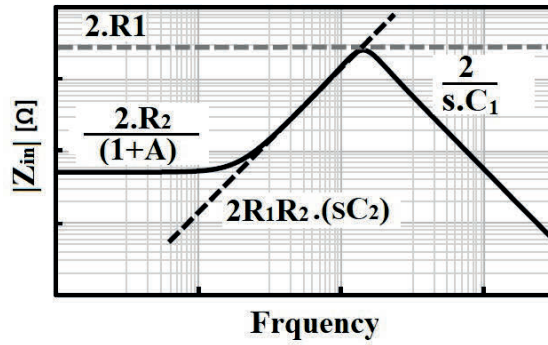


Figure 3.11: Differential input impedance of Rauch filter

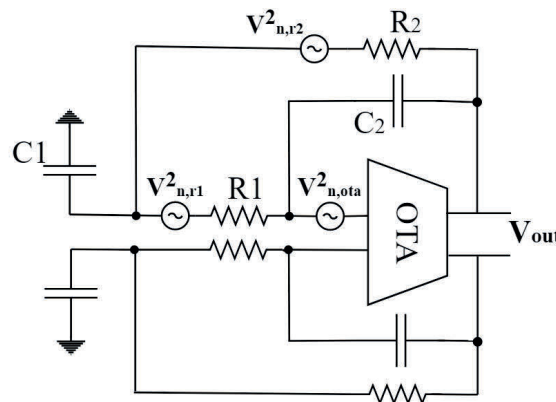


Figure 3.12: Different components' noise contribution in Rauch filter

zero position further to a higher frequency. It is possible by decreasing the input capacitor value, C_1 , but to keep the same cut-off frequency, the input resistor, R_1 should be increased which means there is a trade-off between noise contribution and input impedance.

Figure 3.13 shows the open-loop model of Rauch filter, which gives a better insight into its poles and zeros positions. By calculating the transfer function between V_t and V_f , the G-loop introduces two poles in low frequency at ($R_2, r_{out} \gg R_1$)

$$\omega_{p1} = \frac{1}{C_1 [(R_2 + r_{out}) || R_m]} \quad (3.5)$$

$$\omega_{p2} = \frac{1}{(C_2 + C_L)(R_2 || r_{out})}, \quad (3.6)$$

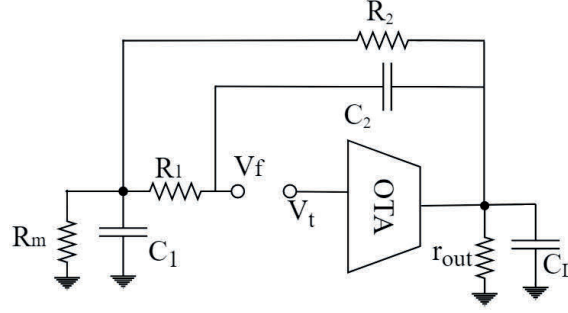


Figure 3.13: Open-loop model of Rauch filter

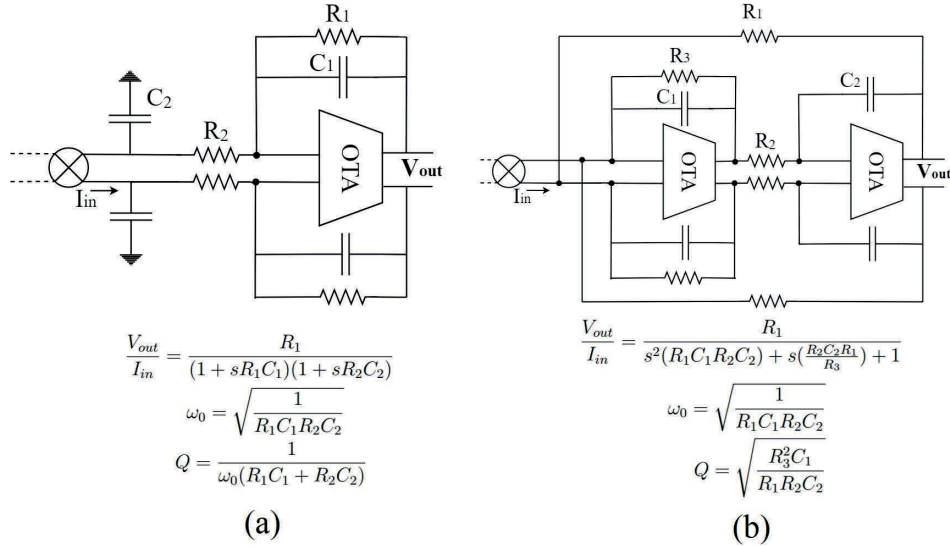


Figure 3.14: Second order filters: (a) two real poles filter, (b) Two Thomas biquad filter

and a high frequency pole at

$$\omega_{p3} = \frac{1}{R_1 \frac{C_2 C_L}{C_2 + C_L}} \quad (3.7)$$

The loop also has two complex conjugated zeros that keep stability of the whole structure.

3.3.2 Second order filters comparison

In this section, the Rauch filter performance will be compared to two other second-order filters, as shown in Figure 3.14. While for the filter with two real poles, the

Filter structure	Two real poles filter	Two Thomas filter	Rauch filter
Selectivity	Medium	High	High
Input impedance	Medium	Medium	Low
Linearity	Medium	Medium	High
Noise	Medium	Medium	Low
Power	Medium	Medium	Low

Table 3.3: Second order filters' performance comparison

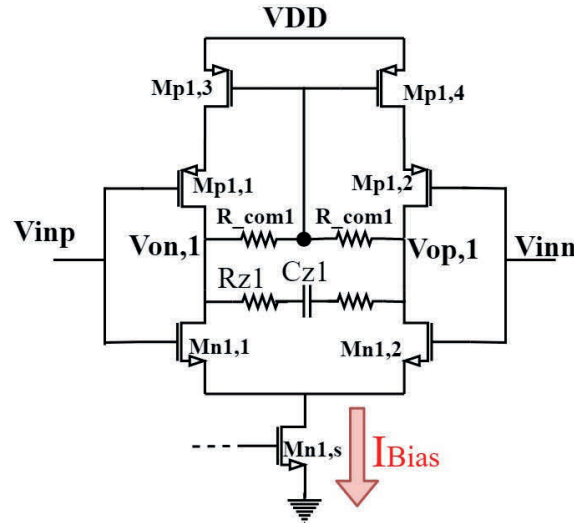


Figure 3.15: First stage circuit in Rauch and TIA filters

quality factor, Q , is always less or equal to 0.5 which results in poor selectivity but good stability [41], the Two Thomas design can have a Q larger than 0.5 with complex conjugated poles; however, to provide sufficient linearity in this structure, the system should burn lots of power to extend the bandwidth and boost the gain for OTAs. Table 3.3 compares different parameters in Rauch and two other filters. As the table shows, the Rauch filter can provide a low power and noise design with good selectivity compared to other structures, so Rauch filter is one of the best choices for high linear and low power baseband filters in the new high-bandwidth generation of telecommunication systems.

3.4 Circuit level design

This part talks about the whole baseband filter structure at the circuit level. Figure 3.15 shows the first stage in both Rauch and TIA structure. The first stage

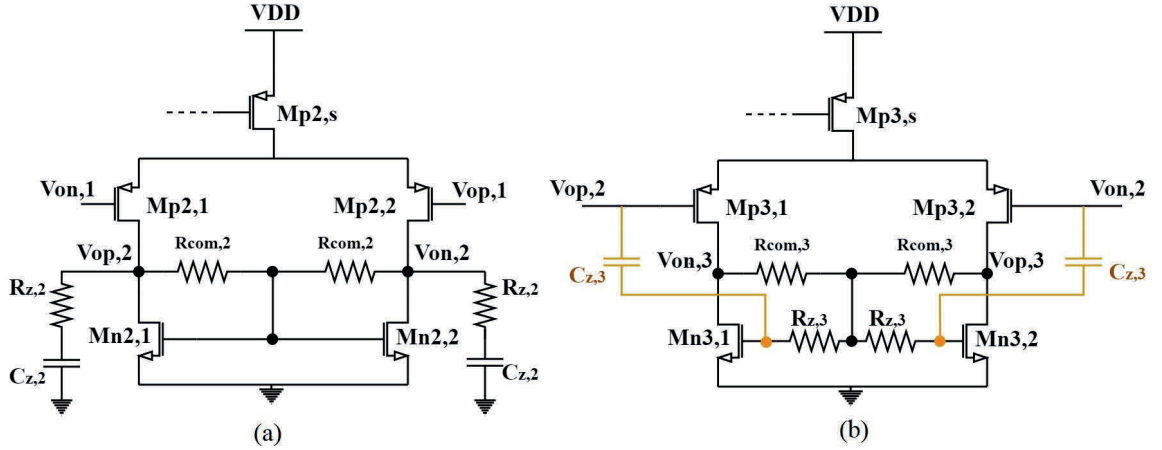


Figure 3.16: Middle stages in Rauch filter: (a) simple differential circuit (b) doublet pole and zero structure

has local common-mode feedback through $M_{p1,3}$ and $M_{p1,4}$ to fix output nodes and benefits from a power-efficient parallel P-N structure to increase the circuit transconductance(g_m).

The first stage has a dominant pole at the output node and its effect on phase behavior is modified by adding a zero through a series RC net, R_{z1} and C_{z1} to that node. The second and third stages in Figure 3.16 play role as the middle stages to boost the gain. The second stage is a simple PMOS differential stage and the same idea like the first stage, the added zero by the RC network at the output node improves the overall phase behavior of the system. The third stage has a doublet pole and zero structure like the TIA circuit in the previous chapter, and as aforementioned, it helps to provide a sufficient gain in a high-frequency range. The last stage in the main path is a P-N circuit, as shown in Figure 3.17. To fix the circuit output, two common mode circuits for P and N side are used to provide proper symmetry between the top and downside of the last stage and guarantee common-mode stability.

The feed-forward stage with a folded cascode structure, bypasses the middle and last stages, as shown in Figure 3.18. By ac coupling at input and output nodes and putting four transistors in each branch, the total G_m is boosted by a factor of four. Mixing the folded cascode and parallel approach ideas introduces a power-efficient structure with sufficient room for a swing at the output node, which is important for the linearity of the whole circuit. As mentioned in the previous chapter, the low voltage room at the output node by potentially saturating some stages can decrease stability and even make the whole system unstable. Like the last stage, there are two common-mode feedback circuits for upside and downside

3.4. Circuit level design

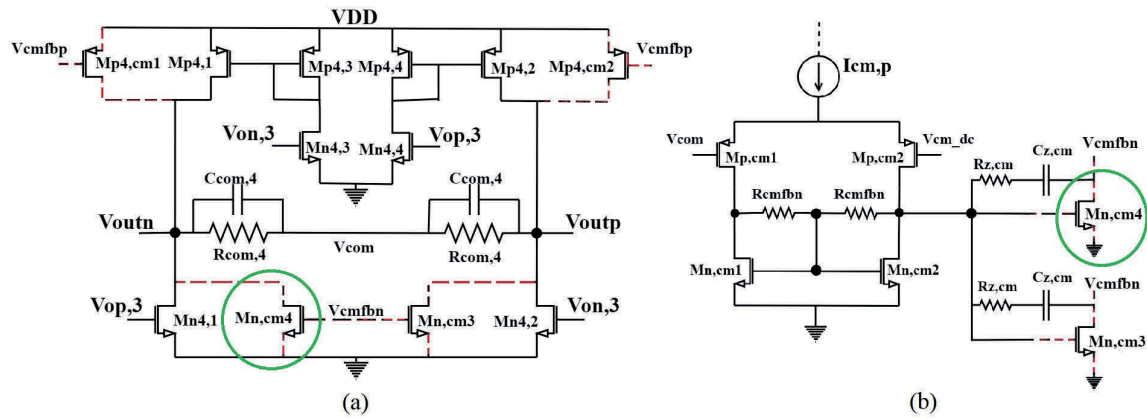


Figure 3.17: Last stage structure: (a) parallel P-N circuit (b) common mode circuit

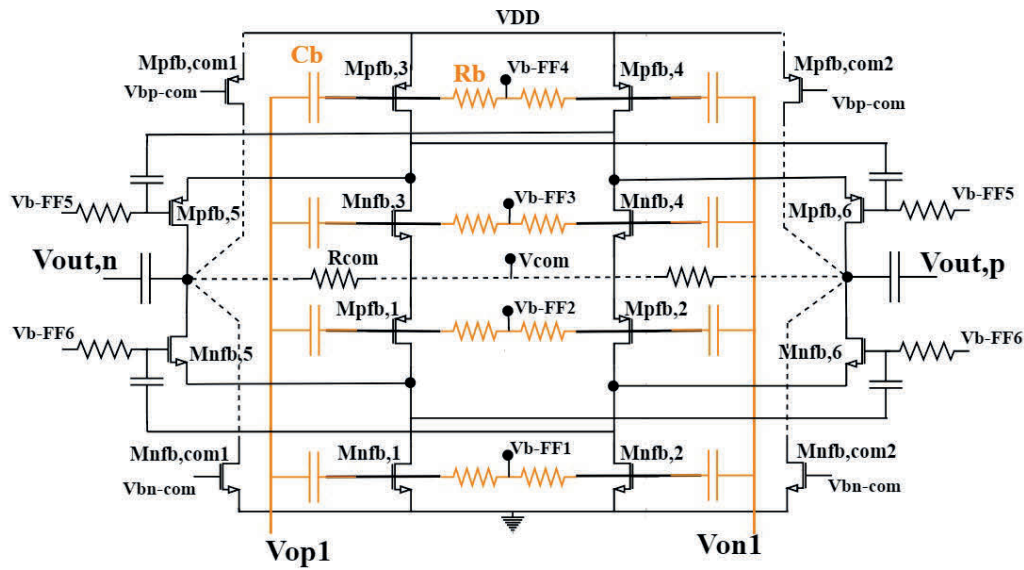


Figure 3.18: Folded cascode structure of feed-forward stage

to keep fixed the output nodes.

Table 3.4 shows all components value used in Rauch filter design. While the first stage is the main power-hungry stage with 1.5 mA, the last and feed-forward stages burn 1 mA. The total current consumption in Rauch filter is 5.3 mA with 1.5 V voltage supply. The TIA filter with three stages in the main path and the feed-forward stage that connects the first stage's output to the last one has the same stages similar to Rauch filter. Table 3.5 summaries all components value in TIA filter.

Parameter	Value($\mu m/\mu m$)
$M_{p1,1}$, $M_{p1,2}$, $M_{n1,1}$ and $M_{n1,2}$	80/0.04
$M_{p1,3}$, $M_{p1,4}$	20/0.1
$M_{p2,s}$	8/0.2
$M_{p2,1}$ and $M_{p2,2}$	8/0.08
$M_{n2,1}$ and $M_{n2,2}$	4/0.08
$M_{p3,s}$	12/0.2
$M_{p3,1}$, $M_{p3,2}$	4/0.08
$M_{n3,1}$ and $M_{n3,2}$	2/0.08
$M_{n4,1}$, $M_{n4,2}$, $M_{p4,1}$ and $M_{p4,2}$	8/0.08
$M_{n4,3}$, $M_{n4,4}$, $M_{p4,3}$ and $M_{p4,4}$	2/0.08
$M_{p,cm1}$, $M_{p,cm2}$	8/0.08
$M_{n,cm1}$, $M_{n,cm2}$	8/0.15
$M_{n,cm3}$, $M_{n,cm4}$	24/0.15
$M_{nfb,1}$, $M_{nfb,2}$, $M_{pfb,3}$ and $M_{pfb,4}$	19.2/0.03
$M_{pfb,1}$, $M_{pfb,2}$, $M_{nfb,3}$ and $M_{nfb,4}$	14.4/0.03
$M_{pfb,5}$, $M_{pfb,6}$, $M_{nfb,5}$ and $M_{nfb,6}$	4.8/0.03
Resistor	Capacitor
$R_{z1}=120 \Omega$	$C_{z1}=50 \text{ fF}$
$R_{z2}=500 \Omega$	$C_{z2}=150 \text{ fF}$
$R_{z3}=250 \Omega$	$C_{z3}=100 \text{ fF}$
$R_{z,cm}=3 \text{ k}\Omega$	$C_{z,cm}=100 \text{ fF}$

Table 3.4: Rauch filter's transistors size

Parameter	Value($\mu m/\mu m$)
$M_{p1,1}$, $M_{p1,2}$, $M_{n1,1}$ and $M_{n1,2}$	40/0.04
$M_{p1,3}$, $M_{p1,4}$	20/0.06
$M_{p2,s}$	10/0.2
$M_{p2,1}$ and $M_{p2,2}$	12/0.08
$M_{n2,1}$ and $M_{n2,2}$	3/0.08
$M_{n4,1}$, $M_{n4,2}$, $M_{p4,1}$ and $M_{p4,2}$	12/0.08
$M_{n4,3}$, $M_{n4,4}$, $M_{p4,3}$ and $M_{p4,4}$	6/0.08
Resistor	Capacitor
$R_{z1}=500 \Omega$	$C_{z1}=250 \text{ fF}$
$R_{z2}=750 \Omega$	$C_{z2}=120 \text{ fF}$

Table 3.5: TIA filter's components value

R-matching	R1	R2	C-parasitic	C-probe
55Ω	500Ω	110Ω	8 pF	500 fF

Table 3.6: Components value on the PCB

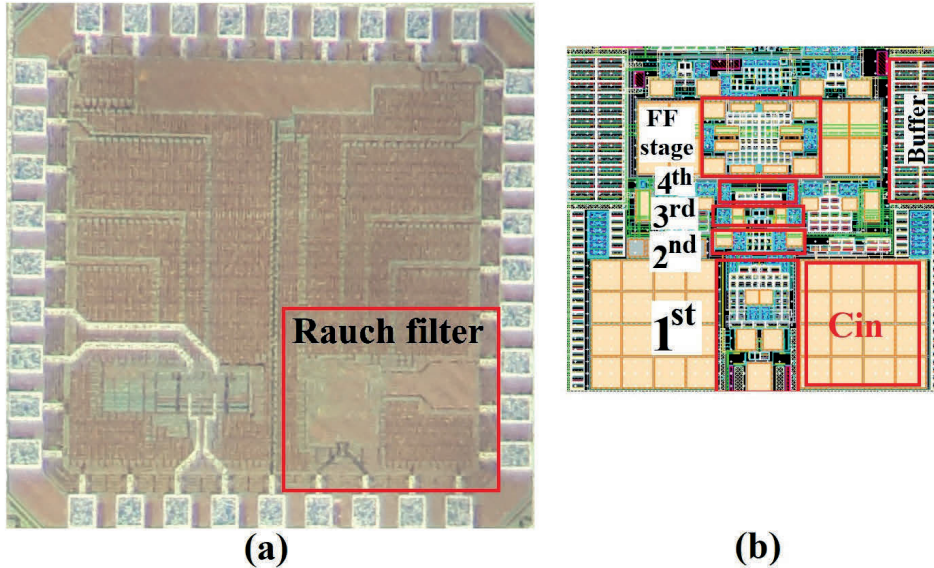


Figure 3.19: Rauch filter's: (a) chip photograph (b) layout design structure

3.5 Measurements Results

A second-order Rauch filter was fabricated in 28nm TSMC technology. The Rauch filter plus an output buffer occupies around 0.027 mm^2 of the chip area. The Rauch layout keeps symmetry in design thanks to its vertical structure shown in Figure 3.19. To test the Rauch filter as a stand-alone circuit, the differential signal was applied from outside through an off-chip balun which is a transformer with a turn ratio of one, so a 55Ω resistor is used after that to provide proper matching to the input source. Figure 3.20 shows the Printed circuit board(PCB) made to test the Rauch filter and measurement test bench.

Table 3.6 shows components value inside or off-chip located on the PCB. The filter gain can be controlled in two different levels by using resistors R_1 , R_2 and output switches. The output buffer is supplied by 6mA off-chip current source through a bias-Tee, which isolates the DC and RF parts of the circuit and protects the chip against supplies' noise. Bias-Tee circuit is a combination of variant inductors and capacitors which can work properly from low to high-frequency range; measurement result shows less than 1.5 dB insertion loss for bias-tee from DC to around 800 MHz. All measurements for gain and linearity tests have been done

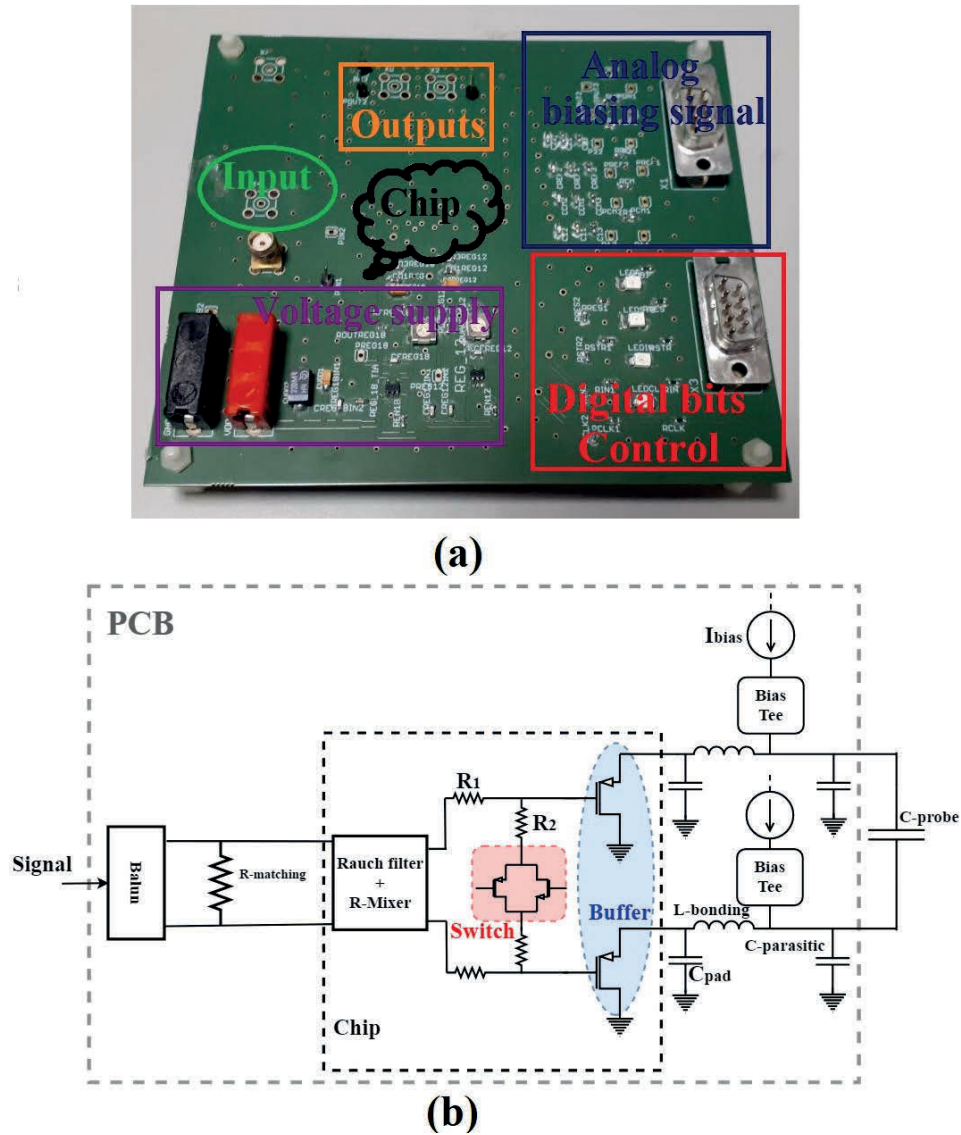


Figure 3.20: Rauch filter:(a)PCB (b)measurement test bench

by Rohde and Schwarz RT-ZD40 differential probe.

To change the filter gain, digital bits are applied to output switches located before buffers. Figures 3.21 and 3.22 show the post-layout and measurement results for the Rauch filter in low and high gain modes which are 3.6 dB and 16.5 dB, respectively. The measurement responses show almost flat responses in bandwidth and perfectly follow the post-layout ones with less than 1 dB difference. Noise measurement has been done by AP033 active differential Probe. Probe can provide gain by a factor of 10 which is a typical setup for noise measurements.

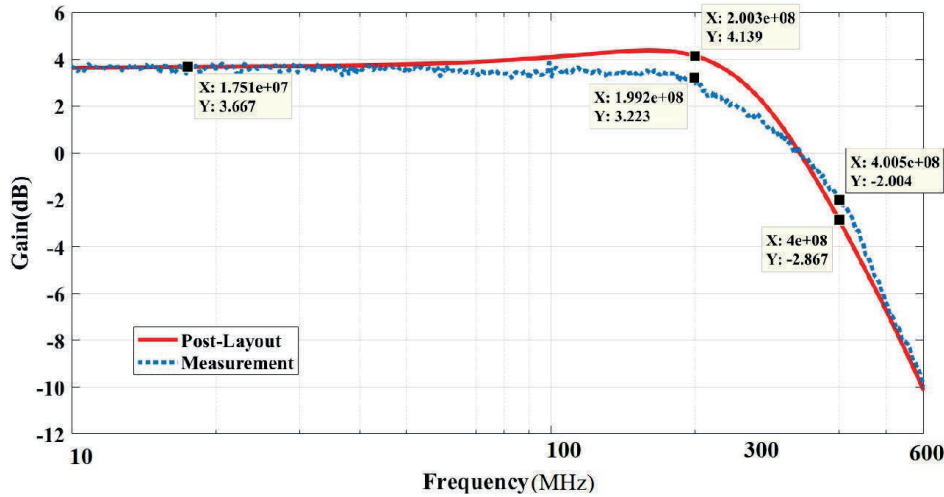


Figure 3.21: Rauch filter's low-gain mode

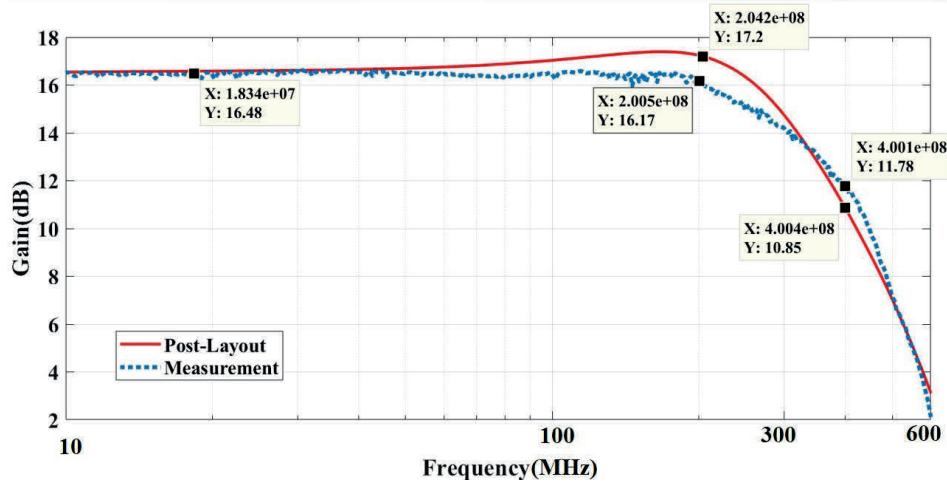


Figure 3.22: Rauch filter's high-gain mode

Figure 3.23 compares the output noise power of post-layout and measurement results. The measurement result follows post-layout one with less than 2 dB coming from bias-tee and some parasitic elements at the output node. The simulation results also show that the input resistor, $R_{in} = 90\Omega$ has the main contribution in noise power. The simulation result for NF, by putting the fabricated Rauch in the receiver chain, shows around 4.5 dB which is less than the proposed number, 5dB, in design goals.

To test the linearity, two tones should be applied to the circuit to measure the inter-modulation tone at the output. To see the effect of the in-band tone, two tones applied at 180 MHz, 190 MHz, and by measuring the output IM3 at 170

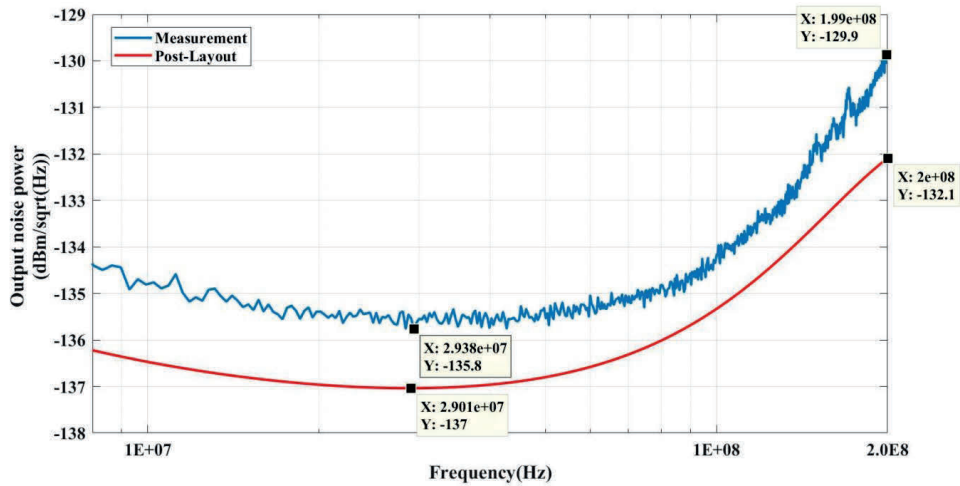


Figure 3.23: Rauch filter's output noise

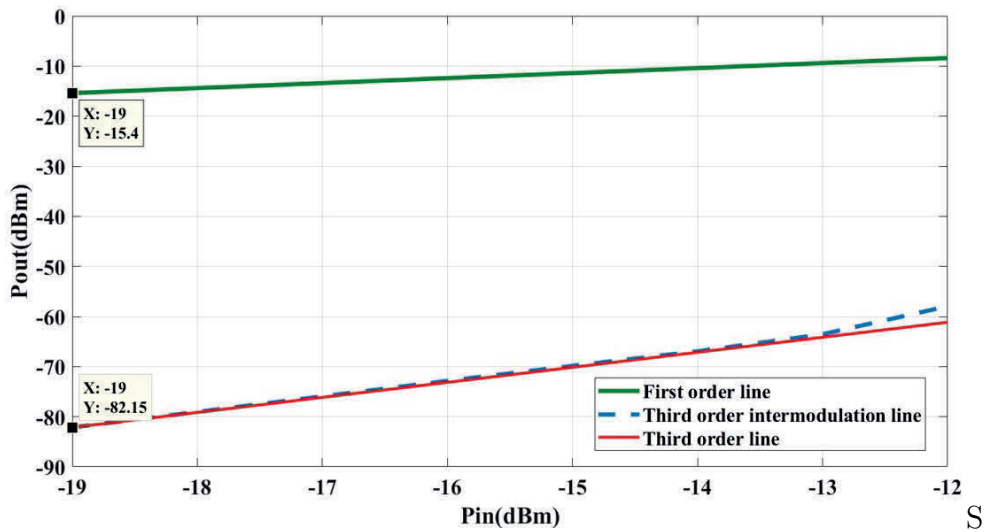


Figure 3.24: Output inter-modulation tone amplitude by applying two tones at 180 and 190 MHz

MHz as shown in Figure 3.24, the input-referred IP3 in low-gain mode is +14.3 dBm compared to +16.5 dBm calculated in post-layout simulation. With the same measurement procedure, by applying two out-of-band tones at 300 MHz and 430 MHz, measured and simulated IIP3 are +17.7 dBm and +18.9 dBm, respectively. The measurement results again show that the fabricated filter can satisfy design requirement which is more than +15 dBm OIP3.

The inter-modulation tone's position effect on linearity is analyzed by applying the first tone at 100 MHz and moving the second one from 10 MHz to 190 MHz by step 10 MHz, the measured IIP3 will drop by moving the IM3 tone to a higher

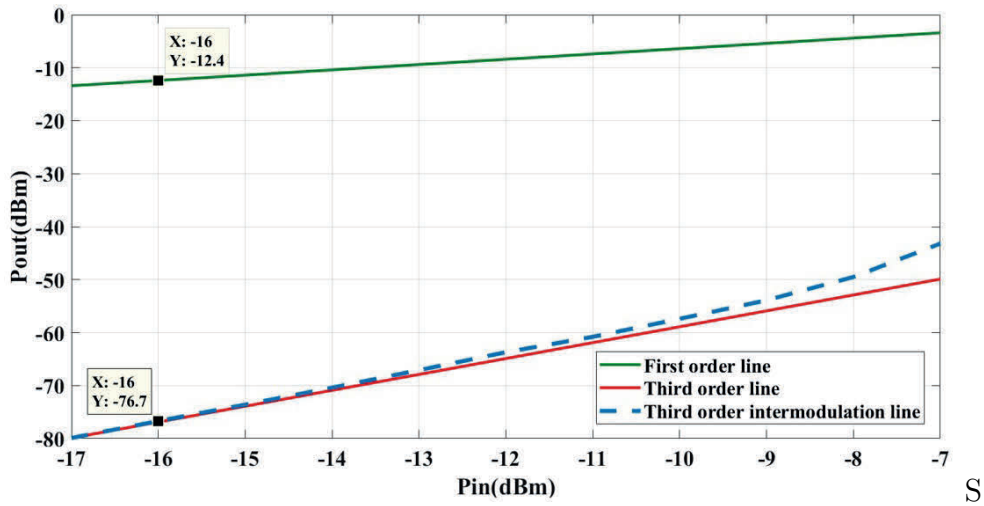


Figure 3.25: Output inter-modulation tone amplitude by applying two tones at 300 and 430 MHz

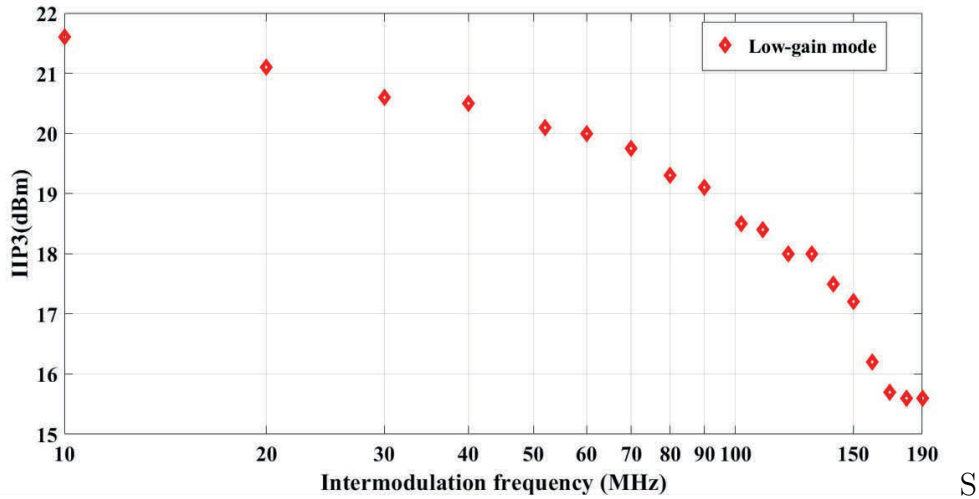


Figure 3.26: IIP3 in terms of IM3 tone position

frequency as shown in Figure 3.26. By getting close to the band edge and losing the G-loop gain, the non-linearity is expected to increase, so the IIP3 drops, as shown in the plot. In addition to IIP3 measurement, 1-dB gain compression point can show the system linearity from a different point of view. Figure 3.27 demonstrates -3.2 dBm as 1dB input compression point by applying 100 MHz tone and changing the input tone power from -30 to 0 dBm. Since the measurement has been done in high-gain mode, so the output can easily swing rail to rail without saturation concern. To have a better understanding of the design performance, Table 3.7 compares the Rauch filter’s measurement results with other similar research works.

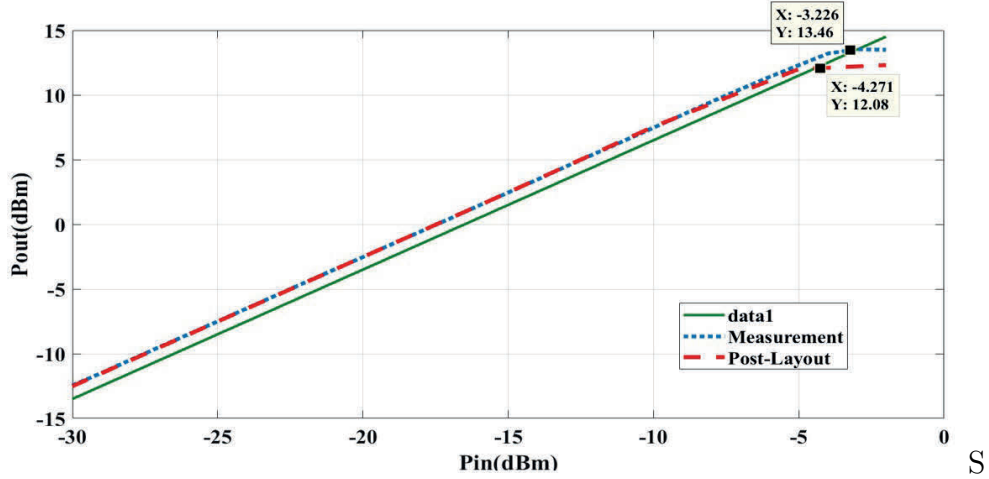


Figure 3.27: 1dB gain compression plot

State-of-The-Art				
Parameter	This work	IEEE Trans.(2012) S.D'Amico [42]	IEEE Trans.(2013) Le Ye [43]	ISSCC(2015) J.Lechevallier [44]
Technology(nm)	28	90	180	28
Supply(V)	1.5	1.2	1.8	1
Order	2	6	6	3
BW(MHz)	200(-1dB)	255(-3dB)	240(-3dB)	459(-3dB)
Power(mw)	7.9	2.28	4.1	5.6
IIP3(dBm)	14.3 f_1 : 180 MHz f_2 : 190 MHz	14 f_1 : 70 MHz f_2 : 80 MHz	12.5	2.4 f_1 : 300.5 MHz f_2 : 299.5 MHz
$V_{n,rms}$	68	199	203	126
IMFDR3(dB)	56.5	50	49	45
FOM _{IM3} (dBJ ⁻¹)	162.9	162	...	157

Table 3.7: Rauch filter performance compared to other research works

3.6 New idea

As mentioned before, the resistor R_{in} at the input of the Rauch filter has the main contribution in noise power, so decreasing this resistor can improve the noise behavior of the system. To design a third order filter with Rauch and TIA parts, one interesting solution can be changing their positions by putting the TIA as

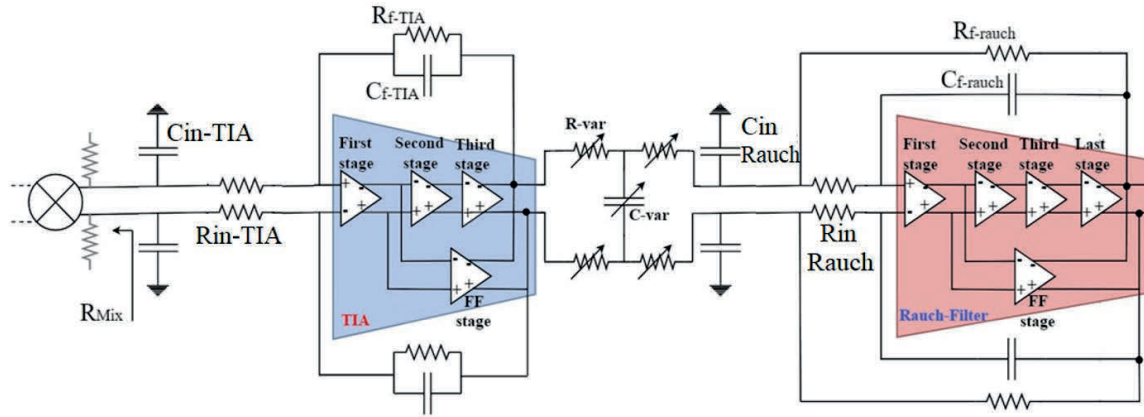


Figure 3.28: New structure to improve the noise behavior

Resistor	Capacitor
$R_{in-TIA}=10 \Omega$	$C_{in-TIA}=4 \text{ pF}$
$R_{f-TIA}=1.4\text{k}\Omega$	$C_{f-TIA}=600 \text{ fF}$
$R_{var}=250 \Omega$	$C_{var}=1.2 \text{ pF}$
$R_{in-Rauch}=100 \Omega$	$C_{in-Rauch}=10 \text{ pF}$
$R_{f-Rauch}=1.4\text{k}\Omega$	$C_{f-Rauch}=300 \text{ fF}$

Table 3.8: Design components value

Gain(dB)	NF(dB)	OIP3(dBm)
45.5	3.25	33.8
39.5	4.15	33.5
33.5	6.95	31.8

Table 3.9: Design components value

the input stage, as shown in Figure 3.28. The TIA's input resistor, R_{in-TIA} is around 10Ω compared to 90Ω for Rauch filter. Table 3.8 summarised the design components' value for the proposed structure in which the input capacitor is only 4 pF . Figure 3.29 and 3.30 show the whole receiver chain's frequency response in different gain and bandwidth levels. All plots satisfy design specifications, less than 1 dB gain fluctuation in bandwidth and more than 33 dB filtering from 200 MHz to 800 MHz .

Table 3.9 presents the NF and OIP3 results. By comparing the new result with the old ones, it is obvious the NF in high gain level drops from 4.94 dB to 3.25 dB by decreasing the input resistor.

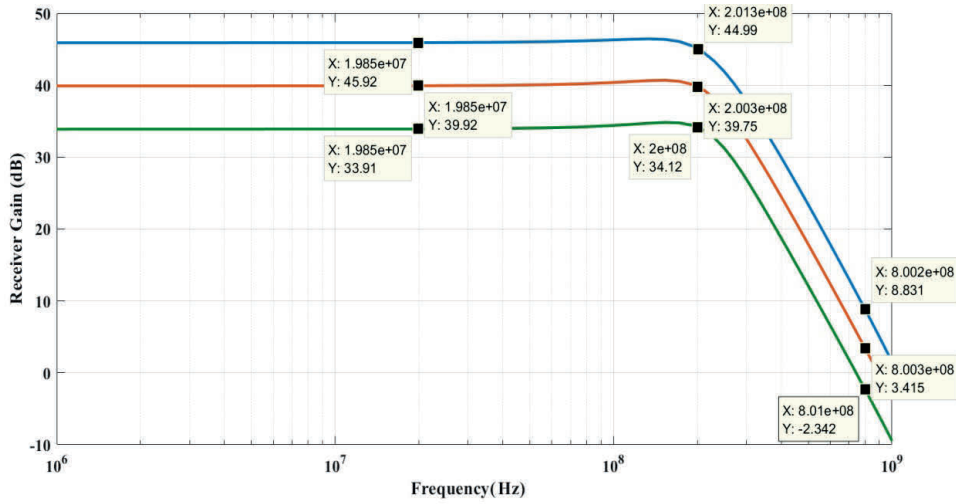


Figure 3.29: Receiver chain gain variation

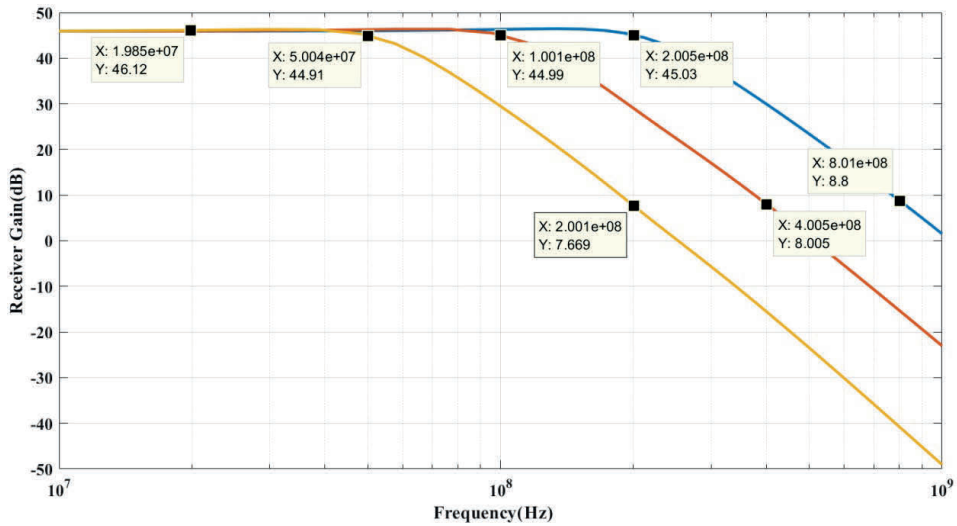


Figure 3.30: Receiver chain bandwidth variation

3.7 Conclusion

The new generation of telecommunication systems for 5G applications need base-band filters that provide sufficient filtering in different gain and bandwidth levels. The baseband filter designed in this chapter was a third-order filter using a combination of second-order Rauch and first-order TIA filter. The proposed filter has 200 MHz in maximum bandwidth level and respects all design requirements with NF less than 5 dB and OIP3 more than +15 dB for the whole receiver chain.

3.7. Conclusion

The measurement results of the fabricated chip to test the Rauch part follows post-layout simulation results accurately. The new structure also was suggested to improve the noise power contribution of whole chain.

Conclusion

The new generation of the wireless system opened new challenges by introducing a higher data rate. Higher bandwidth, which means more interferer closed to band edge, introduces some new challenges, especially about linearity for SAW-LESS receivers.

In this thesis, two high bandwidth baseband filter for current mode receivers were presented. The first one was a TIA with 80 MHz using a local feedback approach to extend the bandwidth and make the circuit stable. Thanks to the conditional stability concept, the linearity of the circuit in and out of the band shows the IIP3 more than +54 dBm. With the parallel structure used in different stages, the power consumption is almost 4.4 mW.

The next one is 200 MHz third-order filter designed for 5G applications. A combination of second-order Rauch filter plus TIA with less than 1 dB ripple in bandwidth made the third-order filter, which provides more than 33 dB filtering beyond 800 MHz. Moreover, the gain and bandwidth of the filter can be changed in the receiver chain. The manufactured chip is the Rauch part that shows proper matching with post-layout results. The filter has NF less than 5 dB and OIP3 more than 15 dBm. Since in Rauch filter, the main noise contributor is the input resistor, to decrease the noise power, the proposed idea is using TIA as the first stage in a third-order filter.

Bibliography

- [1] A. Abidi, “Direct-conversion radio transceivers for digital communications,” *IEEE Journal of Solid-State Circuits*, vol. 30, no. 12, pp. 1399–1410, Dec 1995.
- [2] N. Poobuapheun, W. Chen, Z. Boos, and A. M. Niknejad, “A 1.5-v 0.7–2.5 GHz CMOS quadrature demodulator for multiband direct-conversion receivers,” *IEEE Journal of Solid-State Circuits*, vol. 42, no. 8, pp. 1669–1677, Aug 2007.
- [3] R. Ruby, P. Bradley, J. D. Larson, and Y. Oshmyansky, “PCS 1900 MHz duplexer using thin film bulk acoustic resonators (FBARs),” *Electronics Letters*, vol. 35, no. 10, pp. 794–795, May 1999.
- [4] R. Ruby, P. Bradley, J. Larson, Y. Oshmyansky, and D. Figueredo, “Ultra-miniature high-Q filters and duplexers using FBAR technology,” in *2001 IEEE International Solid-State Circuits Conference. Digest of Technical Papers. ISSCC (Cat. No.01CH37177)*, Feb 2001, pp. 120–121.
- [5] B. Razavi, “Rf MICROELECTRONICS,” in *Upper Saddle River, NJ, USA: Prentice Hall Press*, 2011.
- [6] C. E. Shannon, “Communication in the presence of noise,” *Proceedings of the IRE*, vol. 37, no. 1, pp. 10–21, Jan 1949.
- [7] R. E. Sheriff and Y. Fun Hu, “Mobile satellite communications,” in *John Wiley & Sons*, 2001.
- [8] “Digital cellular telecommunications system (phase 2+); radio transmission and reception (GSM05.05 version 8.5.1 release 1999),” in *ETSI EN 300 910, Tech. Rep., v8.5.1 (2000-11)*.

-
- [9] Qualcomm Technologies Inc., “The evolution of mobile technologies: 1G TO 2G TO 3G TO 4G LTE,” in [Online]. Available: <https://www.qualcomm.com/videos/evolution-mobile-technologies-1g-2g-3g-4g-lte>.
- [10] T. Halonen, J. Romero, and J. Melero, “GSM, GPRS and EDGE performance: evolution towards 3G/UMTS .” in *Chichester, England: John Wiley & Sons, 2004*.
- [11] H. Holma and A. Toskala, “WCDMA for UMTS: HSPA evolution and LTE .” in *Chichester, England: John Wiley & Sons, 2010*.
- [12] S. Sesia, I. Toufik, and M. Baker, “LTE-the UMTS long term evolution: From theory to practice, 2nd ed.” in *Chichester, England: John Wiley & Sons, 2011*.
- [13] “LTE; evolved universal terrestrial radio access (E-UTRA); user equipment(UE) radio transmission and reception (3GPP TS 36.101 version 14.3.0 release 14),” in *ETSI TS 136 101, Tech. Rep., v14.3.0 (2017-04)*.
- [14] “5G NR; user equipment (UE) radio transmission and reception; part 1: Range 1 standalone (3GPP TS 38.101-1 version 15.2.0 release 15),” in *ETSI TS 138 101-1, Tech. Rep., v15.2.0 (2018-17)*.
- [15] 5G FREQUENCY BANDS, in <https://www.rfpage.com/what-are-5g-frequency-bands/>.
- [16] TEXAS INSTRUMENTS, “Rf sampling for multi-band radios,” in <https://www.ti.com/cn/lit/an/sbaa328/sbaa328.pdf>.
- [17] S. Zhou and M.-C. Chang, “A CMOS passive mixer with low flicker noise for low-power direct-conversion receiver,” *Solid-State Circuits, IEEE Journal of*, vol. 40, no. 5, pp. 1084–1093, May 2005.
- [18] M. Valla, G. Montagna, R. Castello, R. Tonietto, and I. Bietti, “A 72-mw CMOS 802.11a direct conversion front-end with 3.5-db nf and 200-khz 1/f noise corner,” *IEEE Journal of Solid-State Circuits*, vol. 40, no. 4, pp. 970–977, April 2005.
- [19] H. Darabi, “Highly integrated and tunable RF front-ends for reconfigurable multi-band transceivers,” in *IEEE Custom Integrated Circuits Conference 2010*, Sep. 2010, pp. 1–8.

- [20] I. Fabiano, M. Sosio, A. Liscidini, and R. Castello, "Saw-less analog front-end receivers for TDD and FDD," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 12, pp. 3067–3079, Dec 2013.
- [21] Y. Lien, E. Klumperink, B. Tenbroek, J. Strange, and B. Nauta, "A mixer-first receiver with enhanced selectivity by capacitive positive feedback achieving +39dbm IIP3 and <3dB noise figure for SAW-less LTE radio," in *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, June 2017, pp. 280–283.
- [22] D. Murphy, H. Darabi, A. Abidi, A. A. Hafez, A. Mirzaei, M. Mikhemar, and M. F. Chang, "A blocker-tolerant, noise-cancelling receiver suitable for wideband wireless applications," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 2943–2963, Dec 2012.
- [23] M. Tsai, C. Liao, C. Wang, Y. Lee, B. Tzeng, and G. Dehng, "A multi-band inductor-less saw-less 2G/3G-TD-SCDMA cellular receiver in 40nm CMOS," in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, Feb 2014, pp. 354–355.
- [24] J. C. Zhan, B. R. Carlton, and S. S. Taylor, "A broadband low-cost direct-conversion receiver front-end in 90 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 5, pp. 1132–1137, May 2008.
- [25] G. Pini, D. Manstretta, and R. Castello, "Analysis and design of a 20-MHz bandwidth, 50.5-dBm OOB-IIP3, and 5.4-mw TIA for SAW-Less RECEIVERS," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 5, pp. 1468–1480, May 2018.
- [26] H. Khatri, P. S. Gudem, and L. E. Larson, "Distortion in current commutating passive cmos downconversion mixers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 11, pp. 2671–2681, Nov 2009.
- [27] I. u. Din, J. Wernehag, S. Andersson, S. Mattisson, and H. Sjöland, "Wide-band SAW-Less receiver front-end with harmonic rejection mixer in 65-nm CMOS," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 60, no. 5, pp. 242–246, May 2013.
- [28] C. Luo, P. S. Gudem, and J. F. Buckwalter, "0.4–6 GHz, 17-dBm 1-dB, 36-dBm IIP3 channel-selecting, low-noise amplifier for SAW-less 3G/4G FDD receivers," in *2015 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, May 2015, pp. 299–302.

-
- [29] Song Hu, Weinan Li, Yumei Huang, and Zhiliang Hong, “Design of a high-linearity RF front-end with IP2 calibration for SAW-less WCDMA receivers,” in *2011 9th IEEE International Conference on ASIC*, Oct 2011, pp. 1090–1093.
- [30] “3GPP, 3rd-generation partnership project; technical specification; LTE; evolved universal terrestrial radio access (E-UTRA); user equipment (UE) radio transmission and reception (release 10), 3GPP TS 36.101 version 10.3.0r,” June 2011.
- [31] P. Wambacq, G. G. E. Gielen, P. R. Kinget, and W. Sansen, “High-frequency distortion analysis of analog integrated circuits,” *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 46, no. 3, pp. 335–345, March 1999.
- [32] B. Hernes and W. Sansen, “Distortion in single-, two- and three-stage amplifiers,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 5, pp. 846–856, May 2005.
- [33] G. Palumbo and S. Pennisi, “High-frequency harmonic distortion in feedback amplifiers: analysis and applications,” *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 50, no. 3, pp. 328–340, March 2003.
- [34] F. Fary, L. Mangiagalli, E. Vallicelli, M. D. Matteis, and A. Baschirotto, “A 28nm bulk-cmos 50MHz 18 dbm-IIP3 Active-RC analog filter based on 7 GHz UGB OTA,” in *ESSCIRC 2019 - IEEE 45th European Solid State Circuits Conference (ESSCIRC)*, Sep. 2019, pp. 253–256.
- [35] S. D’Amico, M. D. Matteis, A. Donno, and A. Baschirotto, “A 0.9 v 3rd-order single-opamp analog filter in 28 nm bulk-cmos,” in *Analog Integrated Circuits and Signal Processing*, January 2019, p. 155–167.
- [36] M. Sosio, A. Liscidini, and R. Castello, “An intuitive current-driven passive mixer model based on switched-capacitor theory,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 60, no. 2, pp. 66–70, Feb 2013.
- [37] M. D. Salehi, D. Manstretta, and R. Castello, “A 150-MHz TIA with un-conventional OTA stabilization technique via local active feed-back,” in *2019 15th Conference on Ph.D Research in Microelectronics and Electronics (PRIME)*, July 2019, pp. 5–8.
- [38] Y. Lien, E. Klumperink, B. Tenbroek, J. Strange, and B. Nauta, “A mixer-first receiver with enhanced selectivity by capacitive positive feedback achieving

- +39dbm IIP3 and <3db noise figure for saw-less LTE radio,” in *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, June 2017, pp. 280–283.
- [39] F. Ciciotti, F. Fary, M. De Matteis, and A. Baschiroto, “28nm implementation aspects of a 0.9v 75MHz 4th-order Rauch analog filter,” in *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2019, pp. 1–5.
- [40] A. Pirola, A. Liscidini, and R. Castello, “Current-mode, WCDMA channel filter with in-band noise shaping,” *IEEE Journal of Solid-State Circuits*, vol. 45, no. 9, pp. 1770–1780, Sep. 2010.
- [41] M. Tsai, C. Liao, C. Wang, Y. Lee, B. Tzeng, and G. Dehng, “A multi-band inductor-less SAW-less 2G/3G-TD-SCDMA cellular receiver in 40nm cmos,” in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, Feb 2014, pp. 354–355.
- [42] S. D’Amico, M. De Blasi, M. De Matteis, and A. Baschiroto, “A 255 MHz programmable gain amplifier and low-pass filter for ultra low power impulse-radio UWB receivers,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 2, pp. 337–345, Feb 2012.
- [43] L. Ye, C. Shi, H. Liao, R. Huang, and Y. Wang, “Highly power-efficient active-rc filters with wide bandwidth-range using low-gain push-pull opamps,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 1, pp. 95–107, Jan 2013.
- [44] J. Lechevallier, R. Struiksmma, H. Sherry, A. Cathelin, E. Klumperink, and B. Nauta, “5.5 a forward-body-bias tuned 450MHz GM-C 3rd-order low-pass filter in 28nm UTBB FD-SOI with >1dbvp IIP3 over a 0.7-to-1v supply,” in *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, Feb 2015, pp. 1–3.